

Trench Corner Rounding Technology Using Hydrogen Annealing for Highly Reliable Trench DMOSFETs

Sang-Gi Kim, Jongdae Kim, Jin Gun Koo, Kee Soo Nam, and Kyoung-Ik Cho
 Micro-Electronics Technology Laboratory, ETRI, Yusong P.O.Box 106, Taejeon, 305-600 Korea
 Tel: 82-42-860-5272, Fax: 82-42-860-6108, e-mail: sgkim@cadvax.etri.re.kr

Abstract

A new trench corner rounding technique has been developed by using pull-back and hydrogen annealing process. This technique provides highly controllable trench corner rounding by micro structure transformation of silicon at the corner of the trench, leading to uniform gate oxide, higher breakdown voltage, and lower leakage current.

Introduction

One of the key issues to apply trench devices such as automotive and telecommunication, portable handy terminals, and DC/DC converting markets is to reliability, which is accomplished by the trench corner rounding (TCR) for the purpose of decreasing leakage, and increasing breakdown voltages [1-3]. The TCR has become the most common and important isolation and gate formation technology for trench double diffused MOSFET (DMOSFET). In this paper, a new process of TCR of high density trench DMOSFETs using hydrogen annealing is proposed. This technology is capable of forming trench DMOSFET structure with corner rounding at top and bottom corner of the trench structure.

Experimental Results and Discussion

The process sequence for fabricating trench DMOSFETs using pull-back and hydrogen annealing was shown in Fig. 1. The key process steps are: a) TEOS oxide deposition and trench region definition, b) trench formation, c) Pull-back of TEOS oxide (50~100nm) to adjust trench corner

rounding radius, d) Subsequently, hydrogen annealing process to form rounded trench corner, damage recovery and annealing effect, e) gate oxide growth (50nm) on the sidewall of the trench followed by depositional of a layer of polysilicon to fill the trenches, and etch-back planarization of the doped polysilicon. The high quality trenches using magnetically enhanced reactive ion etching were performed in an applied materials model P-5000 dry etching system at chamber pressure of 120 mtorr and RF power of 550 watts.

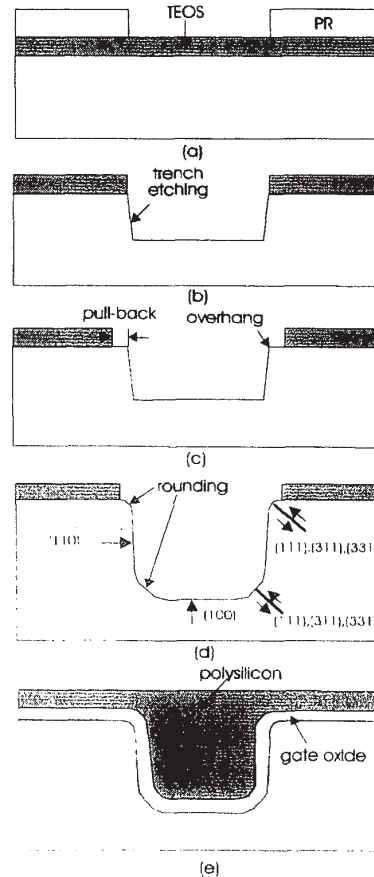


Fig. 1. Process sequence of the proposed trench corner rounding using pull-back and hydrogen annealing. Oxide mask was pull-backed before hydrogen annealing to adjust rounded corner radius.

Fig. 2 is a cross section of the trench structure for trench DMOSFETs. The HBr and SiF₄ chemistry were used He-O₂ as additives to form the trench. We observed good etching characteristics at the chemistries of additive SiF₄ 30 % and He-O₂ 40 % [4]. AFM surface view obtained from plasma etching condition is shown in Fig. 3, a surface roughness of 17 Å (RMS value of 3.1 Å). In this process, 2000 Å of TEOS deposited at 710°C to form trench etching and 1000 Å of was etched to make pull-back area, as shown in Fig. 2.

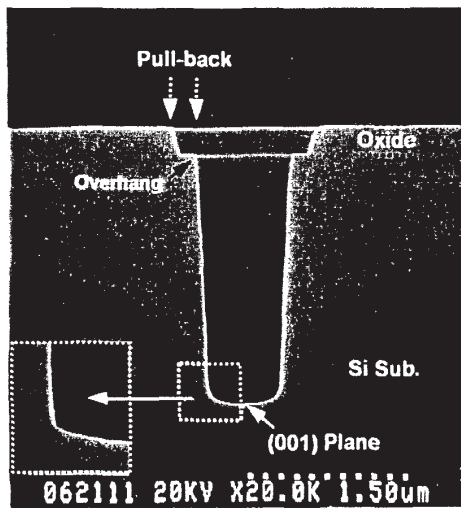


Fig. 2. Cross-sectional SEM photograph of trench formation with oxide pull-back was 10nm.

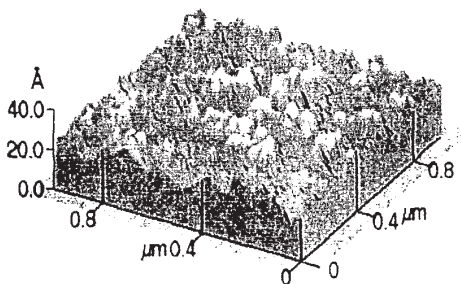
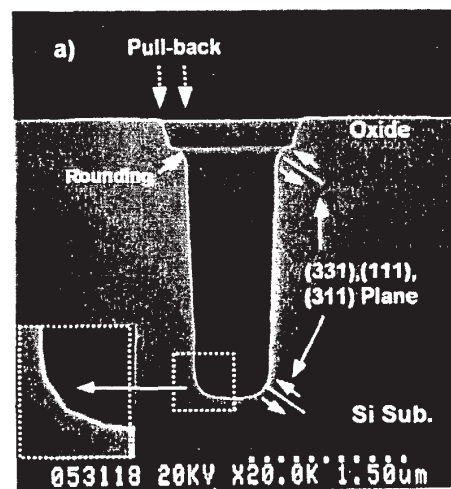


Fig. 3. AFM morphologies of trench etching surface roughness at the HBr/SiF₄ with 45% in He-O₂ chemistries, surface RMS roughness of 3.1 Å.

Fig. 4(a) shows a good trench structure with trench rounding at the top and bottom corners after annealing at 950°C, 30 torr, for 90sec by vacuum rapid thermal process in hydrogen ambient. Silicon migration phenomenon occurs at high temperature with hydrogen ambient annealing. At the higher annealing temperature and the lower pressure condition silicon surface can easily transform [5]. There are 3 different planes at the top and bottom corner, 3 specific gliding (331), (111), (311) directions for each planes along which the dislocation of silicon occurs. Fig. 4 (b) shows the SEM photograph by using hydrogen annealing after oxide pull-backed of high density trench formation for trench DMOSFETs.

A high-resolution lattice image of silicon etched sidewall-to-bottom edge with hydrogen annealing for corner rounding are shown in Fig. 5. The planar defects lying below the etched surface planes show a similar lattice damage. Also it shows the presence of a 20 Å residue layer. This residue layer was considered to be a passivation layer of defect formation during plasma etching and also makes the etched surface smoother with less surface roughness.



(a)



Fig. 4. SEM photograph of high density trench corner rounding using hydrogen annealing at 950°C, 30 torr for 90sec after oxide pull-backed: (a) cross section and (b) top view.

The HRTEM micrograph of the bottom to corner transition region, uniformly covered with residue layer. Defect region marked with open triangle was observed below the residue layer. On the other hand, the surface without noticeable residue layer showed severe atomic scale roughness.

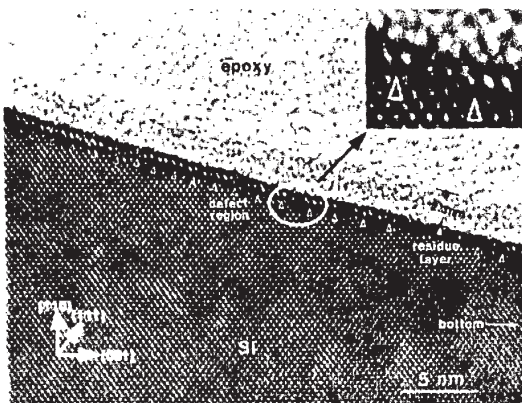


Fig. 5. HRTEM micrograph of the bottom to corner transition region, uniformly covered with residue layer.

The etch induced defects were found in the edge region of trench bottom with depth of 10 Å and decreased at the trench corner region. Fig. 6 shows the cross-sectional SEM photograph of a trench filling DMOSFET structures with and without hydrogen annealing. Figs. 6 (a) and (b) show the trench structures fabricated by the conventional and the proposed methods, respectively. The overhang is shown at the top trench corner and non-uniform oxide is formed along the trench surface, especially thinner oxide at the top and bottom corner of the trench, as shown in Fig. 6(a). However, Corner rounding and uniform oxide layer is shown in Fig. 6 (b). This is due to the pull-back and hydrogen annealing, leading to the silicon migration and crystal orientation reform from (100) to (111). This crystal orientation reform increases the oxide growth rate at the top and bottom corner of the trench, corresponding to the thicker oxide compared to the original orientation.

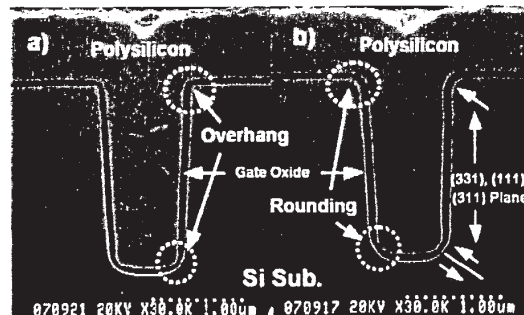


Fig. 6. Cross-sectional SEM photograph of trench filling: (a) conventional method without hydrogen annealing and (b) with hydrogen annealing at 950°C, 30 torr for 90sec.

The breakdown voltages of the trench DMOSFETs fabricated with and without hydrogen annealing are shown in Fig. 7. There is a distinct difference between the two samples and it can be seen that the breakdown voltage of the conventional

sample is about 29V and the breakdown voltage of the hydrogen annealed sample shows about 35V.

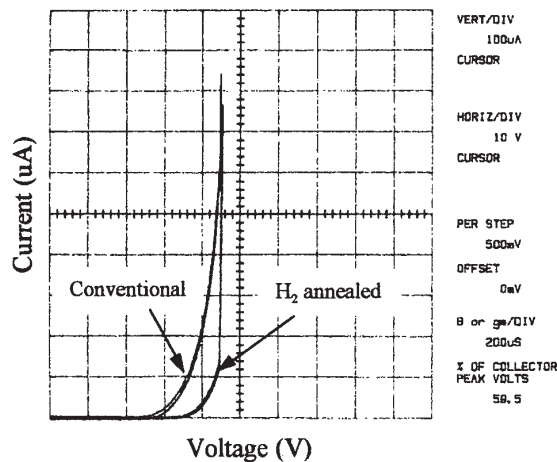


Fig. 7. Breakdown voltage characteristics of TCR DMOSFETs with and without hydrogen annealing.

This result conforms that the on-state voltage and the turn-off loss can be greatly improved by smoothing the TCR. The Id-Vd characteristics of TCR DMOSFET with hydrogen annealing are shown in Fig. 8. The reasonable drain current was obtained 45.25A at $V_{gs} = 10V$, $V_t = 2V$, pulse width 250 μs . An on-resistance of 100 m Ω is obtained at gate voltage of 10V and 5A source to drain current.

Conclusions

In summary, a new process technique for trench corner rounding at the bottom and top of the trench using pull-back and hydrogen annealing.

This technique provides trench corner rounding by pull-back and silicon migration, and uniform gate oxide thickness by the crystal orientation reform at the corner of the trench, resulting in higher breakdown voltage and lower leakage current.

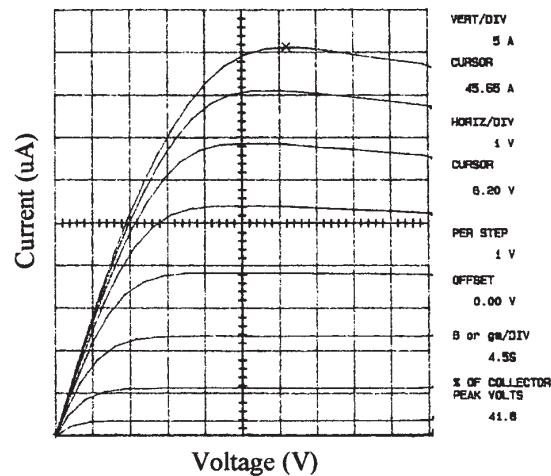


Fig. 8. Id-Vd characteristics of TCR DMOSFETs with hydrogen annealing.

Reference

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