

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

**FORCE MOS TECHNOLOGY, CO.,
LTD.,**

Plaintiff,

v.

ASUSTEK COMPUTER, INC.,

Defendant.

**Civil Action No. 2:22-cv-00460-JRG
JURY TRIAL DEMANDED**

DECLARATION OF DAVID KUAN-YU LIU, Ph.D.

I, Dr. David Kuan-Yu Liu, declare and state as follows:

I. INTRODUCTION

1. My name is David Kuan-Yu Liu, Ph.D. I have been retained by Defendant ASUSTek Computer, Inc. (“ASUS” or “Defendant”) to opine and provide expert testimony related to U.S. Patent Nos. 7,629,634 (the “’634 Patent”), 7,847,346 (the “’346 Patent”), and 7,812,409 (the “’409 Patent”) (collectively, the “Asserted Patents”) in the above-captioned matter.

2. In this declaration, I opine on the scope and meaning of certain claim terms that appear in the Asserted Patents. Relatedly, I also opine on the level of ordinary skill in the art for each of the ’634, ’346, and ’409 Patents, which is relevant to understanding how a person of ordinary skill in the art (“POSITA”) would understand the scope and meaning of the claims of those patents.

3. This declaration is based on the information currently available to me. To the extent additional information becomes available, I reserve the right to amend and supplement this statement and my analysis and opinions. For example, to the extent Plaintiff Force Mos Technology, Co., Ltd. (“Force MOS” or “Plaintiff”) provides new information about its proposed

constructions, proffers new evidence, or responds to my opinions related to ASUS's proposed constructions, I reserve the right to review and respond.

4. My understanding is that the Court will hold a claim construction hearing. If I am called upon to testify at this hearing or any other proceeding about this declaration, I may cite other documents or information similar to that specifically identified herein or such information that is responsive to any testimony or evidence provided by Force MOS. I may also prepare and use presentations, graphics, animations, demonstrations, and other aids to explain my analysis and opinions.

II. SUMMARY OF OPINIONS

A. Summary of Claim Construction Opinions for the '634 Patent

5. My understanding is that Force MOS has asserted claims 1-9 of the '634 Patent. My further understanding is that Force MOS and ASUS dispute the scope and meaning of certain claim terms that appear in claims 1-9 of the '634 Patent, as well as their dependent claims, to the extent the same claim terms appear in the dependent claims.

6. My understanding is that Force MOS claims the earliest priority date for the '634 Patent is February 23, 2008, which is the filing date of U.S. Patent Application Serial No. 12/036,243. As of that date, a POSITA for the '634 Patent would have earned a Master's degree in electrical engineering (or a related field) and had at least two years of relevant work experience in the field of integrated circuit design and manufacturing.

7. In my opinion, ASUS's proposed constructions for the terms in the '634 Patent are correct, and Force MOS's proposed constructions are incorrect, for the reasons discussed in this declaration. Specifically, a POSITA would have found the claim terms to have the meaning proposed by ASUS.

B. Summary of Claim Construction Opinions for the '409 Patent

8. My understanding is that Force MOS has asserted claim 1 of the '409 Patent. My further understanding is that Force MOS and ASUS dispute the scope and meaning of certain claim terms that appear in claim 1 of the '409 Patent, as well as their dependent claims, to the extent the same claim terms appear in the dependent claims.

9. My understanding is that Force MOS claims the earliest priority date for the '409 Patent is December 4, 2006, which is the filing date of U.S. Patent Application Serial No. 11/633,366. As of that date, a POSITA for the '409 Patent would have earned a Master's degree in electrical engineering (or a related field) and had at least two years of relevant work experience in the field of integrated circuit design and manufacturing.

10. In my opinion, ASUS's proposed constructions for the terms of the '409 Patent are correct, and Force MOS's proposed constructions are incorrect, for the reasons discussed in this declaration. Specifically, a POSITA would have found the claim terms to have the meaning proposed by ASUS or would have found those terms indefinite where ASUS has proposed that the term is indefinite.

C. Summary of Claim Construction Opinions for the '346 Patent

11. My understanding is that Force MOS has asserted claims 1-7 and 16-20 of the '346 Patent. My further understanding is that Force MOS and ASUS dispute the scope and meaning of certain claim terms that appear in claims 1-7 and 16-20 of the '346 Patent, as well as their dependent claims, to the extent the same claim terms appear in the dependent claims.

12. My understanding is that Force MOS claims the earliest priority date for the '346 Patent is November 26, 2008, which is the filing date of U.S. Patent Application Serial No. 12/292,780. As of that date, a POSITA for the '346 Patent would have earned a Master's degree

in electrical engineering (or a related field) and had at least two years of relevant work experience in the field of integrated circuit design and manufacturing.

13. In my opinion, ASUS's proposed constructions for the terms of the '346 Patent are correct, and Force MOS's proposed constructions are incorrect, for the reasons discussed in this declaration. Specifically, a POSITA would have found the claim terms to have the meaning proposed by ASUS.

III. EDUCATIONAL BACKGROUND AND PROFESSIONAL EXPERIENCE

14. I have personal knowledge or have developed knowledge of these technologies based upon education, training, or experience, of the matters set forth herein.

15. My curriculum vitae ("CV") is attached hereto as Exhibit A and provides an accurate identification of my background and experience. Among other things, my CV includes a list of my issued patents and publications for at least the last 30 years. My curriculum vitae also includes information about my expert witness experience, with case numbers where available. Below is a short summary of my professional qualifications:

16. I received a Bachelor of Science in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D. degrees in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

17. I worked on a novel Conductivity Modulated Power MOSFET for my Ph.D. thesis. The novel device uses a trench injector to facilitate an optimal tradeoff between the breakdown voltage and ON-Resistance of a Power MOSFET (Vertical DMOS) through the use of a minority carrier injector.

18. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. At Texas Instruments, my job responsibilities included process integration, device modeling, high-

voltage CMOS process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

19. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (AMD) where I was a key contributor in optimizing Flash cell and periphery devices in AMD's CMOS-based 0.5 μm and 0.35 μm Flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology for accommodate x-decoder transistors and high voltage transistors for negative gate erase operation. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

20. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next- generation memory devices.

21. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

22. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75nm CMOS technology node, a half node version between 90nm and 65nm).

23. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

24. Since 2007, I have served as a technical consultant where I have provided expert

advice regarding Flash memory technology, CMOS process technology, and semiconductor device physics.

25. I am not now and have never been an employee of the Defendant.

IV. MATERIALS CONSIDERED AND METHODOLOGY

26. To prepare this declaration, I have considered and reviewed the '634, '346, and '409 Patents and their file histories. I also considered the competing claim construction proposals of Force MOS and ASUS. To prepare this declaration, I also have relied upon my education, knowledge and experience with MOSFETs, telecommunication and radio systems, wireless systems, networking, computing, and software, as well as my extensive background detailed below. As already discussed, Exhibit A to this declaration is a copy of my curriculum vitae, which further sets forth my education and experience. Exhibit B sets forth a complete list of all materials I have considered to prepare this declaration.

27. To prepare this declaration, I also have relied upon my understanding of certain legal principals regarding claim construction. I am not an expert in patent law. I therefore have relied upon the statement of legal principles set forth in this declaration, conversations with legal counsel as needed to further inform me about relevant legal principles, and also my experience as a technical expert in patent cases including as it relates to claim construction and the meaning of claim terms to a person of ordinary skill in the art.

V. COMPENSATION

28. I am being compensated at \$550.00 per hour for non-testifying work and \$600.00 per hour for testifying work, including reimbursement for reasonable and necessary out-of-pocket expenses incurred in connection to my engagement. My compensation is based solely on the amount of time that I devote to this proceeding and is in no way contingent on the nature of my

findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

VI. LEGAL PRINCIPLES FOR CLAIM CONSTRUCTION

29. Within this declaration, I apply my understanding of certain legal principles to opine on the scope and meaning of the disputed claim terms. However, I am not a lawyer or an expert in patent law. The paragraphs below set forth my understanding of these legal principles.

A. General Claim Construction Principles

30. My understanding is that a patent claim should be interpreted based on what it would mean to a POSITA as of the priority date of the patent. Among other information, the claim language and the specification are relevant to determining the meaning of the patent claim. Because a claim is interpreted according to its meaning to a POSITA, the knowledge, education, and experience of a POSITA are also relevant to determining the scope and meaning of a patent claim.

31. A primary source for construing a claim term is the plain and ordinary meaning to a POSITA of the claim term itself, if the POSITA would understand that there is one, based on the context of the specification and the prosecution history. My understanding is that the claims are to be construed from the terms as written. The language of the claims is not to be rewritten through interpretation. Other claims in the patent can also be informative because claim terms are normally used consistently throughout the patent. It is also my understanding that language in a claim should not be construed so as to render claim language superfluous.

32. I understand that the claims are construed in light of the specification as understood by a POSITA. One should look to the specification and other intrinsic evidence for assistance in understanding a claim term because a patentee may have ascribed a particular meaning to a term.

However, unless stated otherwise in the patent document or the prosecution history, it is my understanding that limitations from the specification generally should not be read into the claims.

33. I also understand that the prosecution history of a patent provides the record of the examination of a patent application before the U.S. Patent and Trademark Office (PTO). The prosecution history provides evidence of how the patent examiner and the inventor understood the patent application and the claims and can therefore be instructive on how to interpret the claims. It is my understanding that arguments or amendments made concerning one patent application can be instructive as to the meaning of like terms in another related patent application

34. My understanding is that in certain circumstances, the words in a patent claim may differ from and not be given their plain and ordinary meaning. One circumstance is when the applicants act as their own lexicographer by clearly setting forth a definition of a claim term that may differ from the plain and ordinary meaning it would otherwise possess. Another circumstance is when the applicant includes or provides an intentional disclaimer, or disavowal, of claim scope. My understanding is that an applicant may act as their own lexicographer, or disclaim or disavow claim scope, in either the specification or the prosecution history of the patent, for example, by making amendments to the claims during prosecution or by making assertions to the PTO about the differences between the claimed inventions and the prior art.

35. My understanding is that extrinsic evidence may also be used in understanding the meaning of a claim term. Extrinsic evidence includes dictionaries, treatises, expert testimony, and prior art. But I understand that one should first look to the intrinsic evidence in construing the claims.

B. Indefiniteness and Terms of Degree

36. My understanding is that a patent claim is indefinite if the claim fails to inform, with reasonable certainty, those skilled in the art about the scope of the invention, when the claim is read in light of the specification and the prosecution history.

37. My understanding is certain patent claim terms may also be so-called terms of degree, meaning that the term uses a word or terminology that implicates some amount, level, or extent (e.g., “big” or “small,” “high” or “low,” “close” or “far,” etc.). My understanding is that for a term of degree, the specification must provide objective boundaries about the meaning of the degree and the range of amounts or values that are within the claim scope, as well as outside of the claim scope. My further understanding is that if the specification does not provide any objective boundaries for the meaning and scope of the term of degree, then the term is indefinite.

VII. STATE OF THE ART FOR THE ASSERTED PATENTS

38. At the effective filing dates of the Asserted Patents, a POSITA would have known that the development of MOSFETs, and specifically Power MOSFETs, focuses on the tradeoff between minimizing the ON-Resistance and maximizing the breakdown voltage capability, for a given device area.

39. The key evolutionary advancement of the Power MOSFET involves going from a planar DMOS (Double-Diffused MOS) to a trench MOSFET, where the gate and its associated channel of the transistor is folded vertically onto a trench into the silicon. While the use of a trench Power MOSFET reduces the ON-Resistance significantly through the reduction of the junction FET (JFET) component, the dopant profile optimization of the body region and the drift region continues to be the key feature in this optimization effort.

40. However, even for well-designed doping profiles in the drift region (N-region) and the body region (P-region) in an N-channel MOSFET that minimizes the channel resistance (R_{ch})

and achieves a target avalanche breakdown voltage strength, the breakdown voltage capability could nonetheless be degraded due to the phenomena of punch-through of the body region between the drain and the source.

41. This punch-through could come from the presence of a resistive contact of the body region to the source region. Any current that is generated from the reverse biased P-N junction (the junction between drift region and the body region) can trigger the lowering of the barrier between the drain and source of the transistor in the off-state, and causes premature breakdown or conduction of the device even before the target avalanche breakdown voltage is reached.

42. Thus, while most of the work in the field at this time focused on optimizing the doping profiles of the body region and the drift region, a significant portion of these efforts also focused on the doping profile around the source/body contact in order to generate a low resistive ohmic contact to connect both the N⁺ source and the P- body of the transistor.

43. With the further evolution of using a trenched source contact to contact both the source region and the P body region, the doping profiles of the body surrounding both the sides and the bottom of the trench have significant impact on the resistivity of the ohmic contacts required to connect both the source and the body.

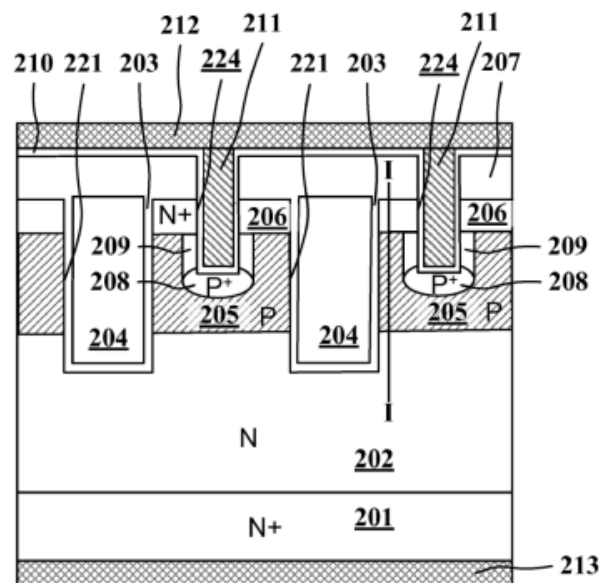
VIII. THE '634 PATENT

A. Overview of the '634 Patent

44. The '634 Patent is directed to a trenched Metal-Oxide-Semiconductor Field Effect Transistor ("MOSFET"), a type of semiconductor structure that is used to significantly reduce the surface area occupied by the channel of the transistor on the silicon, which in turn reduces the ON-resistance of the device for a given device area. This type of semiconductor structure was well-known in the art and to the POSITA at the time of the filing date of the '634 Patent (February 23, 2008). '634 Patent at 1:5-9.

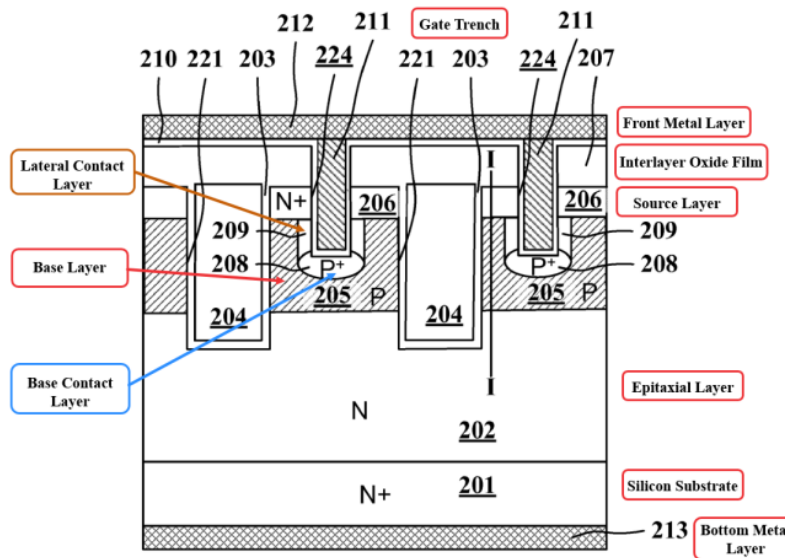
45. The '634 Patent addresses the issue of poor ohmic contact on the sidewall of the trenched source contact to the body region due to poorly engineered doping concentration profile. *Id.* at 1:35-45.

46. The '634 Patent, in particular, is directed to “a lateral contact layer” along the sidewalls within the base layer (205) of the source contact trenches. *Id.* at 1:5-9, 1:66-67, 2:23-26, 3:50-4:6, Fig. 2G. The lateral contact layer described in the '634 Patent is shown below in Figure 2G as 209. *Id.* at Fig. 2G, 3:50-4:6.



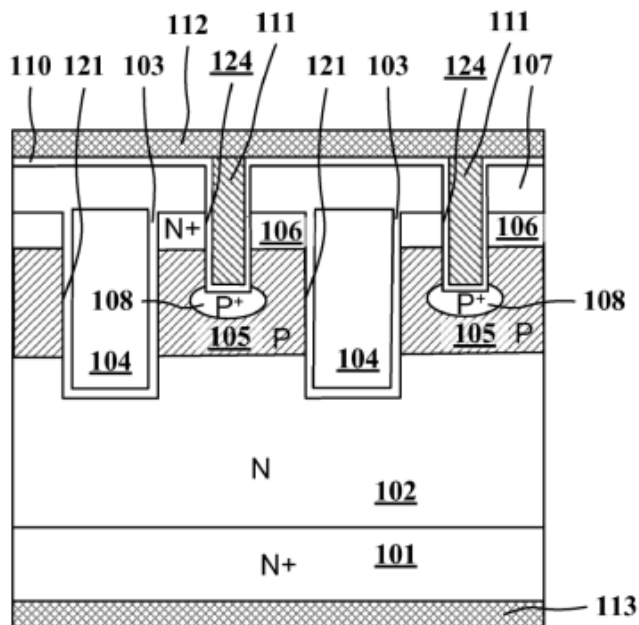
'634 Patent, Figure 2G

47. The '634 Patent describes the lateral contact layer (209) as being doped to P*-type, the base contact layer (208) at the bottom of the source contact trench is P+-type, and the body of the MOSFET (205) is P-type. *Id.* at 3:50- 56, 3:65-4:6, 5:9-15. Doping concentration P* is doped more heavily than P but less than P+. *Id.*



'634 Patent, Figure 2G (annotations added)

48. The '634 Patent also discloses that a trench MOSFET with near-identical structure already existed in the prior art as of the effective filing date, including the claimed drain region, body region, source region, front metal layer, interlayer oxide film, bottom metal layer, trench gates formed on top of the source layer and extending down through the base layer to a portion of the epitaxial layer, and source contact trenches formed on top of the source layer and extending down through the source layer to a portion of the base layer with a heavily doped base layer at the bottom of the trench. *Id.* at 1:5-9, 1:18-41, Fig. 1 (Prior Art). Figure 1 depicting the prior art as admitted by the '634 Patent is shown below.



'634 Patent, Figure 1 (Prior Art)

B. The '634 Patent File History

49. I understand that U.S. Patent Application No. 12/036,243 (the "'243 Application"), titled "TRENCHED MOSFET WITH TRENCHED SOURCE CONTACT," was filed on February 23, 2008, and issued as the '634 Patent on December 08, 2009. *Id.* at 1 (Cover); FORCE-MOS0000039 at 86-124. I also understand that, on July 15, 2009, a telephonic examiner-initiated interview took place, where the examiner and the applicant discussed the lateral contact layer "covering [the] entire trench sidewall[.]" the prior art, and claim language. *Id.* at 65. On July 28, 2009, the examiner issued a Notice of Allowance and Fees Due on Claims 1-9 with examiner amendments to Claim 1, and the following Reasons for Allowance: "Claim 1 limits the trench MOSFET to having a trench in which the base and entire sidewall are covered with the lateral contact layer. Kobayashi (US 6,888,196) covers the base and only a portion of the trench sidewall with the lateral contact layer." *Id.* at 67-68.

C. The Asserted Claims and Disputed Claim Language

50. My understanding is that Force MOS has asserted Claims 1-9. I have reproduced Claim 1 below, with the disputed claim terms shown in ***bold italics***.

Claim 1:

[1.pre] A trench MOSFET with a trench source contact, comprising:

[1.a] a semiconductor region having a drain region, a body region and a source region, comprising, a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;

[1.b] a front metal layer formed on the upper surface of said semiconductor region;

[1.c] an interlayer oxide film formed between said source layer and said front metal layer,

[1.d] a bottom metal layer formed on the lower surface of said semiconductor region;

[1.e] ***a plurality of trench gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer*** to a portion of said epitaxial layer; and

[1.f] a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer; wherein the ***sidewalls of said trenches in said base layer*** are covered by the lateral contact layer; wherein the bottom base of said trenches in said base layer are covered by the base contact layer.

D. Person of Ordinary Skill in the Art (“POSITA”)

51. I am informed and understand that the claims of a patent are judged from the perspective of a hypothetical construct involving a “person of ordinary skill in the art,” or POSITA. The “art” is the field of technology to which the patent is related. I understand that the purpose of using the viewpoint of a POSITA is for objectivity. I understand that a POSITA is presumed to

know and be familiar with the relevant art in the field at the time of invention and is also presumed to possess an average level of creativity. In determining who would be a person of ordinary skill, I considered at least the following criteria: (a) the type of problems encountered in the art; (b) prior art solutions to those problems; (c) the rapidity with which innovations are made; (d) the sophistication of the technology; and (e) the education level of active workers in the field.

52. I understand that Force MOS claims the earliest priority date for the '634 Patent is February 23, 2008, the filing date of U.S. Patent Application Serial No. 12/036,243. It is my opinion that a POSITA for the '634 Patent would have earned a Master's degree in electrical engineering (or a related field) and had at least two years of relevant work experience in the field of integrated circuit design and manufacturing. I consider myself a POSITA of the '634 Patent because I had at least the level of a POSITA in the relevant timeframe.

E. Construction of the Agreed Terms of the '634 Patent

53. I understand the parties have agreed to the meanings of the following terms in the '634 Patent:

Term	Construction
“front” ('634 Patent, cl. 1)	The side of the three-dimensional device to which the photolithography was applied
“top” ('634 Patent, cl. 1) “upper” ('634 Patent, cl. 1)	Referring to the direction of the “front” (e.g., the top surface of a layer refers to the side of the layer that is facing toward the front of the device)
“bottom” ('634 Patent, cls. 1, 17) “lower” ('634 Patent cl. 1) “downwardly” ('634 Patent, cl. 1)	Referring to the direction of the “back” (e.g., the bottom surface of a layer refers to the side of the layer that is facing toward the back of the device)

F. Construction of the Disputed Claim Terms of the '634 Patent

1. “the sidewalls of said trenches in said base layer”

“the sidewalls of said trenches in said base layer” – '634 Patent Claim 1	
ASUS’s Proposed Construction	Force MOS’s Proposed Construction
“entire sidewalls of said trenches in said base layer”	Plain and ordinary meaning: “the portions of the source contact trenches’ sidewalls which are in the semiconductor material’s base layer”

54. Based on the specification and file history of the '634 Patent, it is my opinion that this claim term should be construed according to ASUS’s proposed construction, which is “entire sidewalls of the said trenches in said base layer.”

55. This claim term appears only in asserted claim 1 as shown below:

[1.f] a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer; wherein ***the sidewalls of said trenches in said base layer*** are covered by the lateral contact layer; wherein the bottom base of said trenches in said base layer are covered by the base contact layer.

56. The '634 Patent explains the admitted prior art as providing a MOSFET where “the P+-type region is located *only* at source contact trench bottom.” '634 Patent at 1:33-35, Fig. 1 (Prior Art) (emphasis added). In contrast, the '634 Patent describes the purported invention as a MOSFET with distinct base contact and lateral contact layers, wherein the base contact layer covers the bottom of the source contact trench and the lateral contact layer covers the entirety of the remaining sidewalls of the trench in the base layer. *E.g., id.* at 1:43-45 (“The present invention provides a new structure of trenched MOSFET structure with a trenched source contact which improves the lack of the prior art.”), *id.* at Fig. 2G. The '634 Patent states that “[t]he P+-type base layer (208) and the P*-type lateral contact layer (209) are formed at the bottom and sidewall of the source contact trenches (224) respectively.” *Id.* at 5:9-12. Further, the '634 Patent figures depict

the lateral contact layer and base contact layer as separate layers and provide two, separate implantation methods for forming the bottom base contact layer in addition to the lateral contact layer. *Id.* at 3:50-4:6, Figs. 3A and 3B. The base contact layer in the '634 Patent is created with a 90° Implantation angle respective to the epitaxial layer while the lateral contact layer is created with a 45° to 80° implantation angle. *Id.* at 3:50-53.

57. I understand the examiner distinguished Kobayashi on the basis that the “entire” sidewall of the source contact trench in the base layer was covered by the lateral contact layer in the '634 Patent, as opposed to only being partially covered as in Kobayashi. FORCE-MOS0000039 at 67. This “entire” sidewall distinction was cited during an examiner initiated interview and as a reason for allowance. *Id.* at 65, 67. A screenshot from the notice of allowance is reproduced below:

Reasons for Allowance

2. Claims 1-9 are allowed.
3. The following is an examiner's statement of reasons for allowance:

Claim 1 limits the trenched MOSFET to having a trench in which the base and entire sidewall are covered with the lateral contact layer. Kobayashi (US 6,888,196) covers the base and only a portion of the trench sidewall with the lateral contact layer.

Claims 2-9 are allowed as being properly dependent upon allowed claim 1.

Id. at 67.

58. I also understand that the motivation for this alleged invention of the '634 Patent is to address that the sidewalls of the source contact trench have no ohmic contact (due to low doping concentration of P base). '634 Patent at 1:36-37. A POSITA would understand that a scenario of not having the entire sidewalls of the said trenches in the said base layer would still result in having

a portion of the sidewall of source contact trench lacking an ohmic contact. This would compromise the benefits of the alleged invention.

59. Accordingly, it is my opinion that “the sidewalls of said trenches in said base layer” should mean “the entire sidewalls of the said trenches in said base layer.”

60. I disagree with Force MOS’s proposed construction for the plain and ordinary meaning of “the sidewalls of said trenches in said base layer” because this construction ignores the arguments Force MOS made to distinguish the prior art reference Kobayashi. I understand it is against claim construction principles for a party to recapture a patent’s claim scope that was relinquished during prosecution of that patent.

61. Accordingly, it is my opinion that “the sidewalls of said trenches in said base layer” should be construed as the “entire sidewalls of said trenches in said base layer.”

2. “a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer”

“a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer” – ’634 Patent Claim 1	
ASUS’s Proposed Construction	Force MOS’s Proposed Construction
“a plurality of trenched gates covered by said interlayer oxide film are formed and extend from above said source layer through said base layer”	Plain and ordinary meaning: “trenched gates are formed from top of source layer and extend down through the base layer (i.e. gates need not “extend from above” said source layer)”

62. Based on the specification and file history of the ’634 Patent, it is my opinion that this claim term should be construed according to ASUS’s proposed construction, which is “a plurality of trenched gates covered by said interlayer oxide film are formed and extend from above said source layer through said base layer.” I disagree with Force MOS’s proposed construction, which purportedly relies on the plain and ordinary meaning, because it ignores the claim term’s

use of “formed *on* top of” and instead replaces it with “formed *from* the top of.” This construction effectively rewrites the claim and fails to give proper meaning to “formed on top of.”

63. This claim term appears only in asserted claim 1 as shown below:

[1.e] *a plurality of **trenched gates covered by said interlayer oxide film** are formed **on top of said source layer extending downwardly through said base layer** to a portion of said epitaxial layer; and*

64. Figures 2C and 2D (reproduced below) help understand this claim term and the proposed constructions.

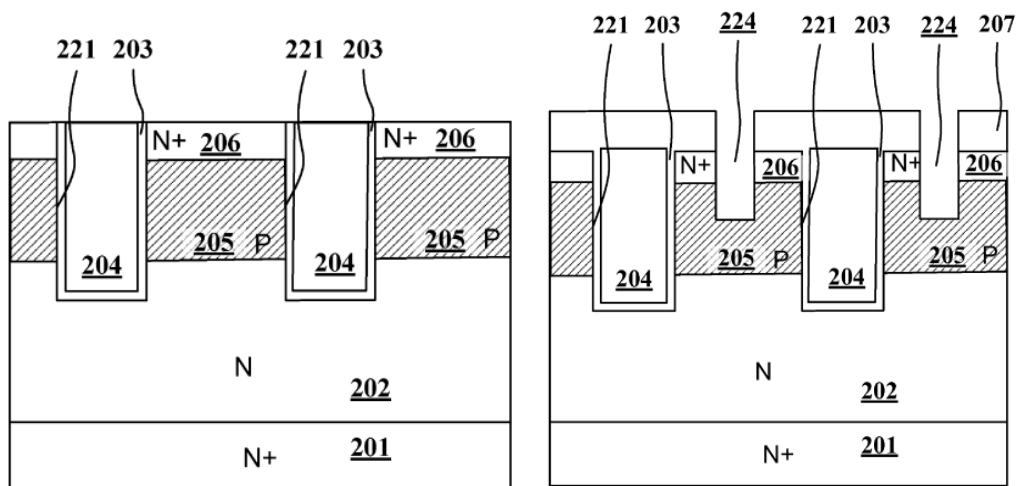


Fig. 2C

Fig. 2D

Figure 2C depicts the formation of a plurality of trenched gates (204) and a plurality of gate oxide films (203) by etching back the oxide film and polysilicon such that they are left only on the interior of each of the gate trenches (221). '634 Patent at 3:26-31. Figure 2D, on the other hand, depicts the formation of a plurality of source contact trenches (224) by etching through the P-type base layer (205), the interlayer oxide film (207), and the N'-type source layer (206). *Id.* at 3:46-49.

65. Referring to both Figures 2C and 2D, the claim requires that the trenched gates (204), which are covered by the interlayer oxide film (207), are formed *on top of* the source layer (206) and extend downwardly through the base layer (205). As depicted in Figure 2D, the trenched

gates (204) are formed slightly above the source layer (206) and then extend downwardly into the base layer (205). Thus, a POSITA would understand the “trenched gates . . . formed on top of” in the context of the claim, specification, and the figures to mean to the trench gates are positioned or extend slightly above the source layer.

66. Outside of the '634 Patent, dictionary definitions provide further support for a POSITA's understanding of the word “on” when used in the context of the claim. For example, Webster's Ninth New Collegiate Dictionary defines “on” as “used as a function word to indicate position in contact with and supported by the top surface of.” “On,” Webster's Ninth New Collegiate Dictionary, 1989, Merriam-Webster Inc., p. 823 (ASUS_CC_000046 at 49). The American Heritage College Dictionary defines “on” as “used to indicate position above and supported by or in contact with” or “[u]sed to indicate contact with or extend over (a surface).” “On,” The American Heritage College Dictionary, Third Edition, 1997, Houghton Mifflin Company, p. 953 (ASUS_CC_000030 at 32). And finally, The American Heritage Dictionary of the English Language defines “on” as “[u]sed to indicate: a. Position upon and above the surface of; point in contact with and support by the surface of . . . b. Contact with any surface, regardless of position.” “On,” The American Heritage Dictionary of the English Language, 1981, Houghton Mifflin Company, p. 917 (ASUS_CC_000034 at 38). All of these dictionary definitions indicate that “on” contemplates a position supported by or above something else.

67. Force MOS's proposed construction, which purportedly relies on the plain and ordinary meaning, fails to acknowledge that the claim requires “formed on top of” rather than “formed from the top of.” Force MOS's proposed construction states that the “trenched gates are *formed from top of* source layer and extend down through the base layer (i.e. gates need not “extend

from above” said source layer).” The specification of the ’634 Patent does not support this construction.

68. I have reproduced a magnified view of the trench gates and source layer portions of Figure 2D.

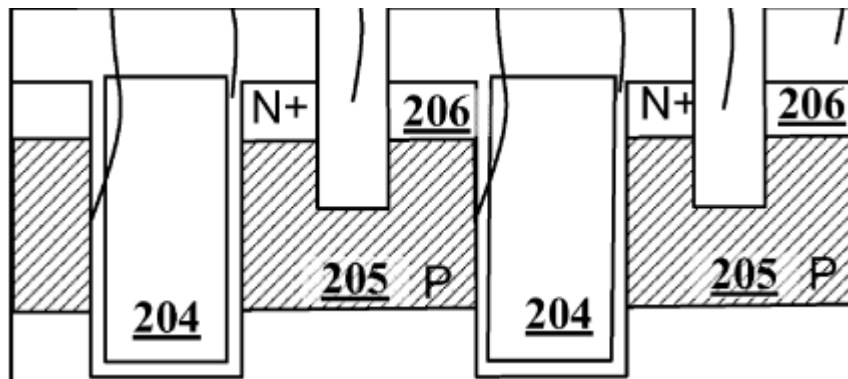


Fig. 2D

69. As shown, Figure 2D clearly depicts the trenched gates (204) that are not coplanar with or on the same level as the source layer (206). Instead, the trenched gates are positioned or extend above the source layer. Given that there are 3 distinct relative positions of the trenched gates with respect to the source layer: trenched gates positioned above the source layer, trenched gates positioned coplanar with the source layer, and trenched gates positioned below the source layer; I would understand that the use of the term “on top of” is meant to give meaning to the relative position of the trench gate to the source layer. It would be inconsistent with the specification for Force MOS to ignore what Figure 2D depicts. Thus, I disagree with Force MOS’s attempt to rewrite the claim’s requirement of “formed on top of” the source layer to “formed from the top of” the source layer when the patent shows the opposite. If it was Force MOS’s intent to claim “formed from the top of,” it would have used such language in the claim and depicted coplanar trenched gates with the source layer. It did not and the language of the claim accompanied by the teaching of the ’634 Patent specification should be given effect.

70. Further, Force MOS's proposed "formed from the top" language would suggest a process step to a POSITA, which is inconsistent with claim 1 of the '409 Patent since this claim is directed to a device. In addition, Force MOS's proposal is inconsistent with the typical process flow for manufacturing such a device. In particular, the formation of the base and source regions would typically occur after the formation of the trench gate. *See e.g.*, '346 and '634 Patents.

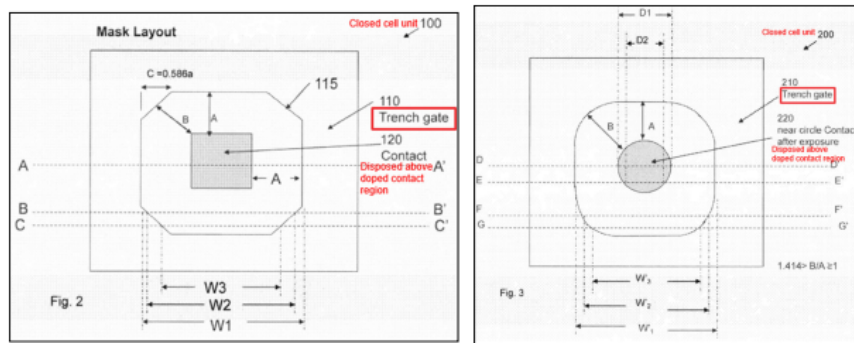
71. Accordingly, it is my opinion that "a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer" should be construed as "a plurality of trenched gates covered by said interlayer oxide film are formed and extend from above said source layer through said base layer."

IX. THE '409 PATENT

A. Overview of the '409 Patent

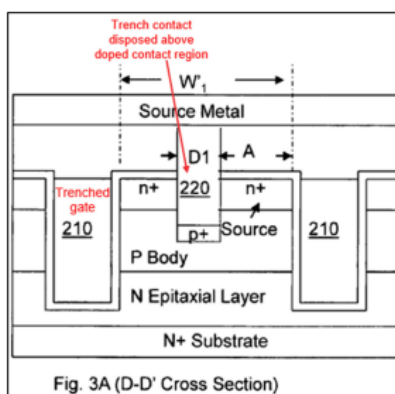
72. The '409 Patent relates to a trenched semiconductor power device. '409 Patent at 1:7-13 ("This invention relates generally to the cell structure, device configuration and fabrication process of power semiconductor devices."). The '409 Patent states in the "Description of the Related Art" that trenched semiconductor power devices already existed in products and disclosures. *Id.* at 1:14-17.

73. The '409 Patent discloses a trenched semiconductor power device with a "closed cell unit" 200/100 of a MOSFET device, which includes a trenched gate 210/110 surrounding a metal contact 220/120. The metal contact 220/120 is disposed above a doped contact region, as shown below in (annotated) Figures 2-3 and 3A of the '409 Patent. *Id.* at 4:4-7.



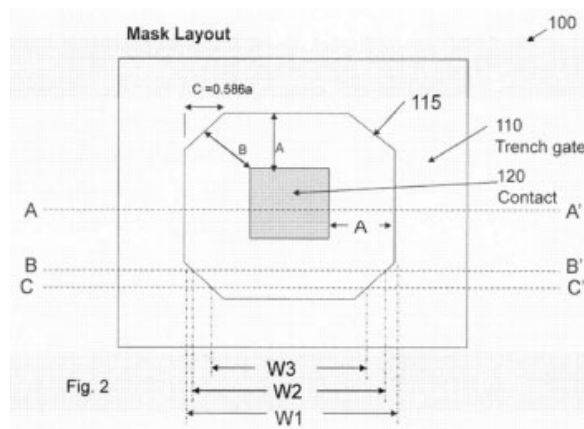
'409 Patent, Figure 2 (annotated)

'409 Patent, Figure 3 (annotated)

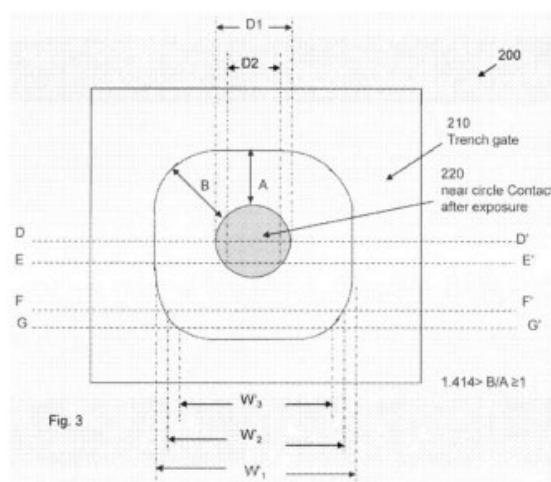


'409 Patent, Figure 3A (annotated)

74. The '409 Patent discloses closed cells designed with substantially square-shaped cells with truncated corners. *Id.* at 4:57-62; *id.* at Fig. 2. The “truncated corners are formed by design layout not process.” *Id.* (showing the mask layout). During the lithography process, the truncated corners naturally become rounded from exposure. *Id.* (“It is by nature that truncated corners in layout as that shown in FIG. 2 and becomes rounded as shown in FIG. 3.”). Figure 3 also shows that the square contact 120 (Fig. 2) naturally becomes a circular shaped contact 220 (Fig. 3) after exposure. *Id.* at 4:53-57.

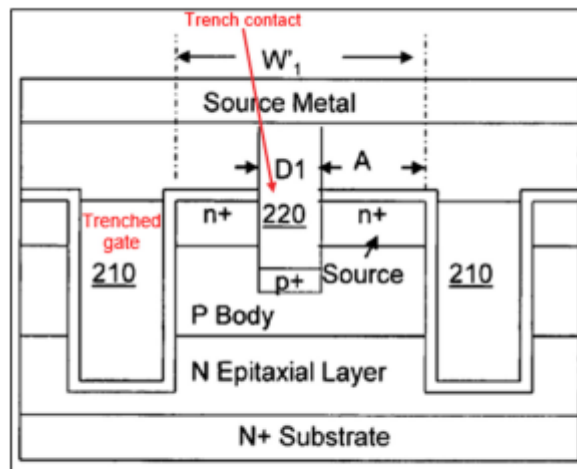


'409 Patent, Figure 2



'409 Patent, Figure 3

75. The '409 Patent discloses a circular trench contact 220 that is “extended into the body region through the source region of the closed semiconductor power cell” and is “in contact with a p+ contact dopant region disposed immediately below the [circular] trench contact.” *Id.* at 4:25-33; *id.* at Fig. 3A. Meanwhile, the trenched gates 210 and the gate oxide lining of the trenched gates 210 are disposed at a distance away from the circular trench contact 220. *Id.* The source and body regions are disposed between the gate oxide lining and all circumferential points of the circular trench contact 220. *Id.* The source and body regions are in contact with the circular trench contact 220. *Id.*



'409 Patent, Figure 3A (annotated)

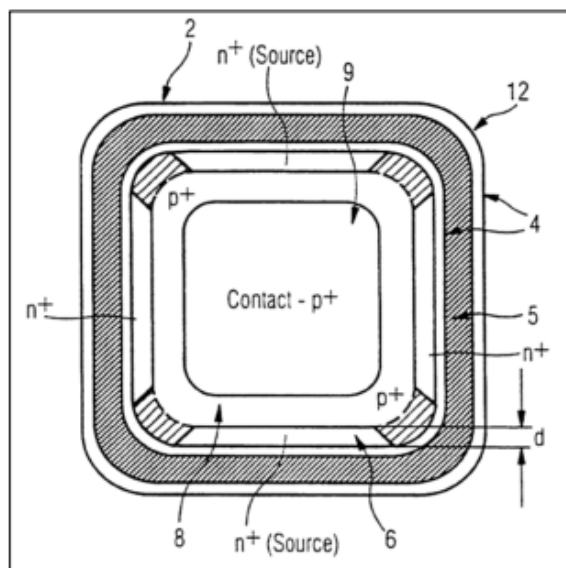
76. Finally, the circular trench contact 220 is filled with a contact metal plug that is connected to a source metal. *Id.*; *id.* at Figure 3A; *id.* at 5:26-7; *see also id.* at Fig. 1C.

B. The '409 Patent File History

77. U.S. Patent Application No. 11/633,366 (the “’366 Application”), titled “TRENCH MOSFET WITH CELL LAYOUT, RUGGEDNESS, TRUNCATED CORNERS,” was filed on December 4, 2006, and issued as the ’409 Patent on October 12, 2010. ’409 Patent at Cover; FORCE-MOS0000227 at 250. The ’366 Application was filed with 18 original claims and listed Fu-Yuan Hsieh as the inventor. FORCE-MOS0000227 at 235-38. In response to an examiner’s Action mailed October 6, 2008 for Election and Restriction, the applicant withdrew claims 14-18 relating to methods for making semiconductor devices. *Id.* at 264.

78. The application received a first office action dated January 26, 2009, rejecting all pending claims on the basis of anticipation and obviousness. *Id.* at 275-86. On April 15, 2009, the applicant amended the pending claims to include (1) a square shaped closed cell with rounded corners in amended claim 1 and with truncated corners in amended claim 13 (now claim 6); and (2) a circular trench contact hole disposed in the center of the closed cells. *Id.* at 305. This

amendment was made to overcome the Pfirsh reference (U.S. Patent No. 6,541,818), which applicant admitted disclosed “a closed cell with square trench gate with rounded corner [2] and square contact with rounded corner [9].” *Id.* I have provided the Pfirsh top view below for reference.



Pfirsh Fig. 2

79. The application received a second and final office action dated July 15, 2009, rejecting all pending claims on the basis of indefiniteness and obviousness. *Id.* at 315-24. On October 14, 2009, the applicant submitted a Request for Continued Examination and amended the pending claims to include a circular trench contact disposed at a distance away from a gate oxide lining of a trench gate from all circumferential points of the circular trench contact in claim 1 and claim 13 (now claim 6). *Id.* at 338. This amendment was made to overcome the Pfirsh reference (U.S. Patent Pub. No. 2022/0006703) in view of the Iman reference (U.S. Patent No. 6,867,083).

80. The application received a third and final office action dated January 10, 2010, rejecting all pending claims on the basis of obviousness. *Id.* at 355-64. On April 2, 2010, the applicant amended the pending claims to include (1) a circular trench contact comprising a hole

opened from a top surface of a semiconductor surface, sidewalls surrounded by and in contact source and body regions, and source and body regions disposed between the hole and trenched gates in amended claim 1; and (2) a contact resistance reduction metal layer disposed above a contact metal plug and below a bottom surface of a source metal in claim 5 (now claim 2). *Id.* at 369-71. This amendment was made to overcome the Pfirsh reference (U.S. Patent Pub. No. 2022/0006703) in view of the Blanchard reference (U.S. Patent No. 6,621,107). *Id.* at 358. On August 5, 2010, the examiner issued a Notice of Allowance and Fees Due, and the '409 Patent issued on October 12, 2010. *Id.* at 395.

81. On October 12, 2018, the '409 Patent expired due to non-payment of maintenance fee. *Id.* at 422. Four years later, on July 12, 2022, the applicant submitted a Petition for Acceptance of Delayed Payment of Maintenance Fees. *Id.* at 405-09. Applicant had failed to pay the 7.5 year maintenance fee which the last day to pay was October 12, 2018. *Id.* at 422. This petition was dismissed on October 12, 2022 for failure to meet the petition requirements. *Id.* at 432-34. On October 28, 2022, the applicant submitted a second Petition for Acceptance of Delayed Payment of Maintenance Fees. *Id.* at 442-47. This petition was also dismissed on December 14, 2022 for failure to meet the petition requirements as well as nonpayment of the 11.5 Year maintenance fee, which was due no later than October 12, 2022. *Id.* at 488-94. On February 14, 2023, the applicant submitted a third Petition for Acceptance of Delayed Payment of Maintenance Fees. This petition was also dismissed on March 17, 2023 for failure to meet the petition requirements as well as non-payment of the 11.5 Year maintenance fee which was due no later than October 12, 2022. On February 14, 2023, the applicant submitted a fourth Petition for Acceptance of Delayed Payment of Maintenance Fees. This petition was granted on May 24, 2023.

C. The Asserted Claims and Disputed Claim Language

82. My understanding is that Force MOS has asserted claim 1 of the '409 Patent. I have reproduced that claim below, with the disputed claim terms shown in ***bold italics***.

Claim 1:

[1.pre] A trench semiconductor power device comprising a plurality of trench gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:

[1.a] said trench gates surrounding said transistor cells as closed cells constituting ***substantially square-shaped*** cells with ***rounded corners***;

[1.b] each of said closed cells further includes a ***circular trench contact*** disposed substantially in a central portion of said closed cells, penetrating through a source region surrounding said trench gates and extending into a body region encompassing said source region;

[1.c] said circular trench contact comprises a hole opened from ***a top surface of said semiconductor substrate*** and is filled with a contact metal plug wherein sidewalls of said hole are surrounded by and in contact said source and body regions and ***said circular trench contact is separate from said trench gates with said source region and body region disposed between a gate oxide lining of said trench gates and all circumferential points of the circular trench contact***; and

[1.d] said contact metal plug connected to a source metal disposed on top of said circular trench contact.

D. Person of Ordinary Skill in the Art (“POSITA”)

83. I am informed and understand that the claims of a patent are judged from the perspective of a hypothetical construct involving a “person of ordinary skill in the art,” or POSITA. The “art” is the field of technology to which the patent is related. I understand that the purpose of using the viewpoint of a POSITA is for objectivity. I understand that a POSITA is presumed to know and be familiar with the relevant art in the field at the time of invention and is also presumed to possess an average level of creativity. In determining who would be a person of ordinary skill,

I considered at least the following criteria: (a) the type of problems encountered in the art; (b) prior art solutions to those problems; (c) the rapidity with which innovations are made; (d) the sophistication of the technology; and (e) the education level of active workers in the field.

84. I understand that Force MOS claims the earliest priority date for the '409 Patent is December 4, 2006, the filing date of U.S. Patent Application Serial No. 11/633,366. It is my opinion that a POSITA for the '634 Patent would have earned a Master's degree in electrical engineering (or a related field) and had at least two years of relevant work experience in the field of integrated circuit design and manufacturing. I consider myself a POSITA of the '409 Patent because I had at least the level of a POSITA in the relevant timeframe.

E. Construction of the Disputed Claim Terms of the '409 Patent

1. "rounded corners"

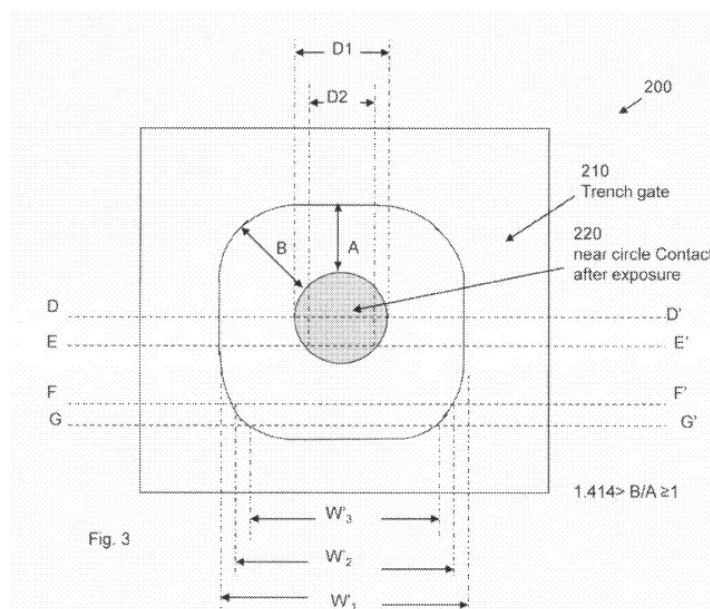
"rounded corners" – '409 Patent Claim 1	
ASUS's Proposed Construction	Force MOS's Proposed Construction
"corners that are truncated by design layout and then rounded"	Plain and ordinary meaning: "corners having a curved shape (i.e. like a portion of a circle or oval)"

85. Based on the specification and file history of the '409 Patent, it is my opinion that this claim term should be construed according to ASUS's proposed construction, which is "corners that are truncated by design layout and then rounded." I disagree with Force MOS's proposed construction for the plain and ordinary meaning of "rounded corners" because it is too broad and contrary to the file history.

86. This claim term appears only in asserted claim 1 as shown below:

[1.a] said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with ***rounded corners***;

87. The specification and file history of the '409 Patent support ASUS's proposed construction. In particular, the '409 Patent describes rounded corners in only one context—with respect to Figure 3 (shown below). '409 Patent at 2:10-20; 4:53-64. In addition, during prosecution, the applicant characterized the “rounded corners in the amended claim 1” as “structural features . . . shown in Fig. 3” of the '409 Patent (reproduced below). FORCE-MOS0000227 at 305. As described in the '409 Patent, to form the “rounded corners” in Figure 3, *truncated corners are first formed by design layout*. '409 Patent at 2:10-20; 4:53-64. Then, the *truncated corners become rounded* after exposure during photolithography. *Id.* at 4:53-64.



88. The '409 Patent also states that Figure 1A (reproduced below) is prior art, with the figure showing a top view of a square-shape trench gate (20) with a square-shape trenched contact (15) in the middle. *Id.* at 1:20-23. A POSITA would understand that Figure 1A represents the mask layout of a square-shaped trench gate and not the actual top view of a trench gate for a device that has gone through the manufacturing process of photolithographic exposure to pattern the trench gate. Due to the physics of optical lithography, the corners of a rectangular feature, including a square feature, would be rounded naturally during the mask exposure process. An

analogy of this would be filling a square-shaped balloon with air, which would cause the square shape to be inevitably rounded. In fact, it would take tremendous amount of effort in applying what is known as Optical Proximity Correction, or OPC, to obtain a mere resemblance of a somewhat sharp corner after the exposure. Thus, it is well known in the art that corners become somewhat rounded as a natural/incidental result of lithography.

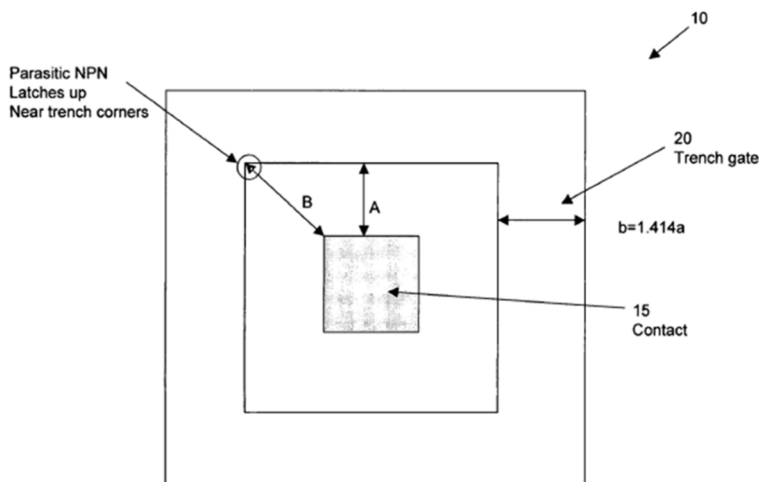
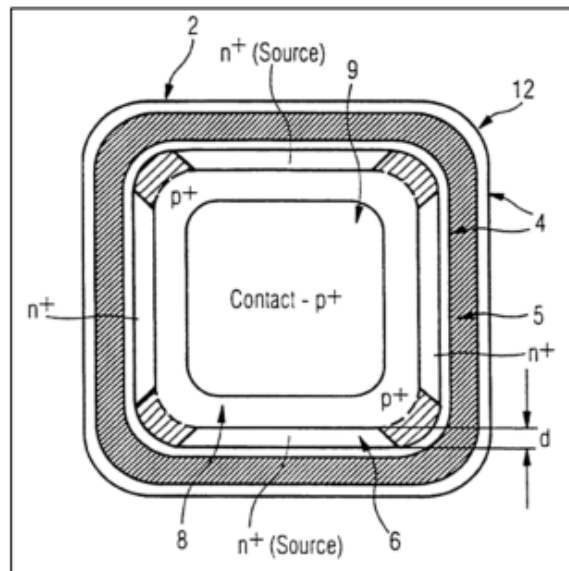


Fig. 1A (Prior Art)

89. The specification of ‘409 Patent supports a POSITA’s understanding of Figure 1A being a mask layout. The ‘409 Patent at 2:14-17 states that “the manufacturing process includes a step of exposure through the mask such that the square contact becomes approximately circular shaped contact and truncated corners become smoother.” The ‘409 Patent at 2:58-60 also admits that the rounding occurs “by nature.” In light of these statements, the fact that the contact in Figure 1A is shown as square-shaped with sharp corners is indeed a confirmation to a POSITA that Figure 1A is a mask layout and that during the manufacturing process, Figure 1A’s sharp corners would naturally become rounded and smoother.

90. Further, during prosecution, the applicant amended claim 1 (which is also the current claim 1) by adding the “rounded corners” to distinguish the closed cells of the Pfirsch

reference, reproduced below. Specifically, applicant distinguished claim 1 from Pfirsch “which has a closed cell with *square trench gate with rounded corner* . . . as shown in Fig. 2 . . . in Pfirsch.” FORCE-MOS0000227 at 305 (emphasis added).



Pfirsch Fig. 2

91. Accordingly, it is my opinion that the “rounded corners” of claim 1 should be construed as “corners that are truncated by design layout and then rounded.” At the time of filing of the ’409 Patent (Dec. 4, 2006), a POSITA would have understood that “rounded corners” refers to corners that are *truncated by design and subsequently rounded by lithography*.

92. In contrast, the “rounded corners” in claim 1 of the ’409 Patent cannot mean a naturally or incidentally rounded corner of a trench gate that was designed to be square, as proposed by Force MOS. Not only did Force MOS amend the claims away from such interpretation but also this interpretation would cover the prior art. For example, if Force MOS’s proposed construction for “rounded corners” is applied, then after lithography the layout of Figure 1A would naturally or incidentally contain “corners having a curved shape (i.e. like a portion of a circle or oval).” I understand that under the principles of claim construction, it would be improper

for Force MOS’s proposed construction to cover a prior art design or seek to recapture claim scope that was given up during prosecution.

2. “circular trench contact”

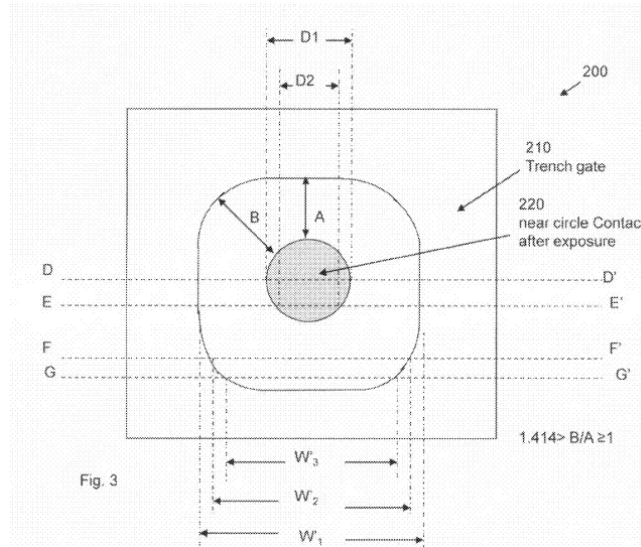
“circular trench contact” –’409 Patent Claim 1	
ASUS’s Proposed Construction	Force MOS’s Proposed Construction
“trench contact that is a circle by design layout”	Plain and ordinary meaning: “trench contact having a form shaped like a circle from a top-view cross-sectional perspective”

93. Based on the specification and file history of the ’409 Patent, it is my opinion that this claim term should be construed according to ASUS’s proposed construction, which is “trench contact that is a circle by design layout.” I disagree with Force MOS’s proposed construction of the plain and ordinary meaning for “circular trench contact” because it is inconsistent with the ’409 Patent’s file history and the specification.

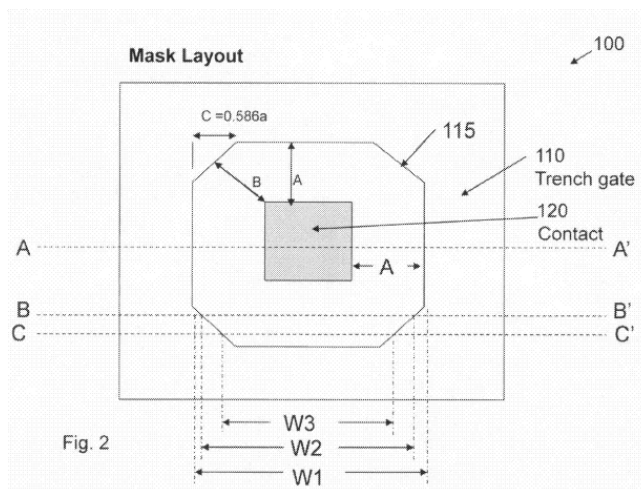
94. This claim term appears only in asserted claim 1 as shown below:

[1.b] each of said closed cells further includes a ***circular trench contact*** disposed substantially in a central portion of said closed cells, penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;

95. Similar to the “rounded corners” claim term, ASUS’s proposed construction is supported by the specification and file history of the ’409 Patent. In particular, the ’409 Patent describes the circular trench contact (200) only with respect to Figure 3 (as shown below). ’409 Patent at 4:25-48, Fig. 3.



96. Figure 2 (shown below) depicts a mask layout of an embodiment of the claimed invention wherein the contact 120 is square. The patent states that the “square contact [of Figure 2] becomes approximately circular shaped” through the “process for manufacturing the semiconductor power device.” *Id.* at 4:53-56. A POSITA would understand that both the circular shaped trench contact and the truncated corners would be “formed by design layout not process. . . . Such configuration is formed . . . because of the photolithography.” *Id.* at 4:57-61; *id.* at 4:62-64 (“A MOSFET device shown in Fig. 3 is another embodiment that can be produced by applying a design layout that implemented as on of the manufacturing processes.”).



97. In addition, during prosecution of the '409 Patent, applicant amended claim 1 (which is also the current claim 1) by removing “hole” from “circular trench contact hole” FORCE-MOS0000227 at 370. The applicant made this amendment, among others, to distinguish the pending claims from two references—Pfirsch and Blanchard—the examiner relied on to reject the claim. *Id.* at 358. The applicant stated that the “the trenched contact shape of the Schottky diode in Blanchard is square, rectangular, hexagonal or octagonal (Figs. 4A-4E, 8, 9A-9D and 10) shape but not circular shape as the present patent application.” *Id.* at 378.

98. Below, I have reproduced Figs. 4A-4C from Blanchard (U.S. Patent No. 6,621,107), which are top views of the MOSFET and Schottky diode structures of the invention. As depicted, the applicant assessed the shape of a trenched contact shape based on the design of the mask layout and not by the final product of the manufacturing process. Stated differently, for a trench contact to be “circular” as claimed, a POSITA would understand that it would be designed in that way and not made circular by the manufacturing process.

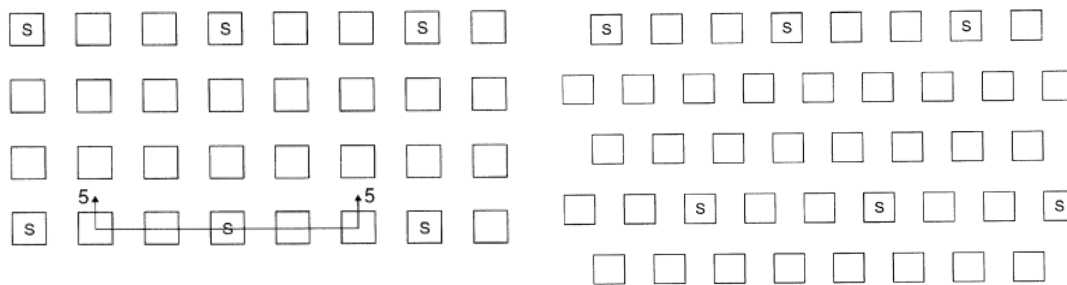


FIG. 4A

FIG. 4B

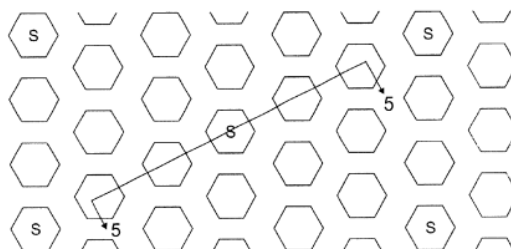


FIG. 4C

99. Accordingly, it is my opinion that the “circular trench contact” of claim 1 should be construed as “trench contact that is a circle by design layout.” At the time of filing of the ’409 Patent (Dec. 4, 2006), a POSITA would have understood that a “circular trench contact corners” would refer to trench contacts that were designed to be circular and were further rounded by lithography.

100. I disagree with Force MOS’s proposed construction for the plain and ordinary meaning of “circular trench contract,” which it contends means “trench contact having a form shaped like a circle from a top-view cross-sectional perspective.” It is my opinion that Force MOS is taking inconsistent positions with respect to the “circular trench contact.” During prosecution, Force MOS argued that the shape of a trench contact is determined from the design layout of the MOSFET before manufacturing. Now, Force MOS’s proposed construction shifts this perspective away from the design layout to after the MOSFET has been manufactured. This is wrong. A POSITA, in light of the ’409 Patent file history, would understand that the way to properly assess whether a trench contact is circular is to look at the design layout, not the final manufactured MOSFET.

3. “substantially square-shaped”

“substantially square-shaped” – ’409 Patent Claim 1	
ASUS’s Proposed Construction	Force MOS’s Proposed Construction
“from a top-view cross-sectional perspective, a square-shape that satisfies a design rule that the greatest difference between the longest distance and the shortest distance between the circular trench contacts and the trenched gates is significantly less than a predefined value”	Plain and ordinary meaning: “from a top-view cross-sectional perspective, having a largely or essentially square shaped, other than the recited ‘rounded corners’”

101. Based on the specification and file history of the ’409 Patent, it is my opinion that “substantially square-shaped” should be construed according to ASUS’s proposed construction, which is “from a top-view cross-sectional perspective, a square-shape that satisfies a design rule

that the greatest difference between the longest distance and the shortest distance between the circular trench contacts and the trenched gates is significantly less than a predefined value.” I disagree with Force MOS’s proposed construction for the plain and ordinary meaning of “substantially square-shaped” because it is inconsistent with the specification of the ’409 Patent.

102. The term “substantially square-shaped” appears in one limitation of asserted claim 1, which is reproduced below:

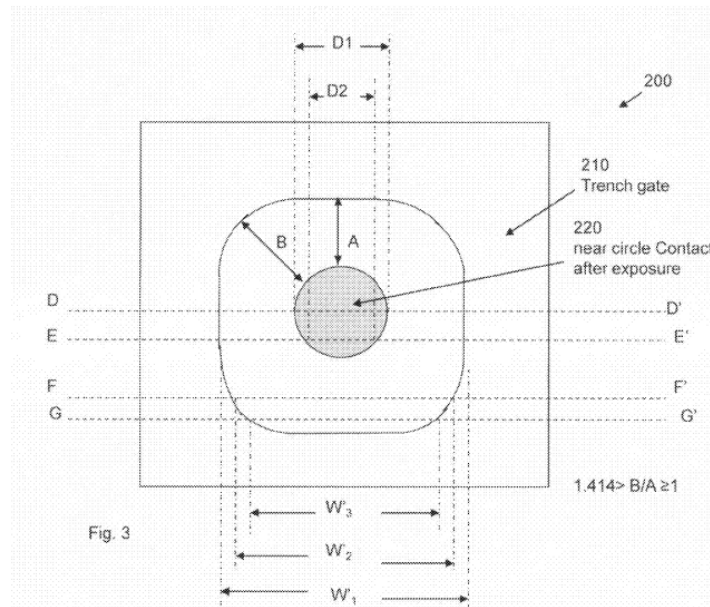
[1.a] said trenched gates surrounding said transistor cells as closed cells constituting *substantially square-shaped* cells with rounded corners;

103. The ’409 Patent characterizes the “invention” at 2:24-30 as follows:

Another aspect of the *present invention* [is] to provide new and *improved closed cell configuration of a semiconductor power device with a design rule that the greatest difference between the longest distance and the shortest distance between the source/body contact and the trenched gate is significantly less than a predefined value to achieve an improved device ruggedness*. In an exemplary embodiment, the ratio of the longest distance to the shortest distance is less than 1.414 to achieve an improved device-ruggedness over the conventional squared-shaped closed cell layout.

104. The purported “invention” as described above is consistent with the requirement that the corners of the cell are truncated *by design* and subsequently rounded during lithography, as I have explained above in § IX.E.1. As further described in the patent at 4:4-13:

The doped contact region 220 is formed with substantial circular shape and the trenched gate is formed with rounded corners 215. The distance from the edge of the circular doped contact region 220 to the trenched gate 200 including the distance B to the rounded corners 215 and to the distance A to the edges of the trenched gate are substantially the same, i.e., $B=A$.



105. This discussion of the relationship between B and A (of Fig. 3) above also refers to the distance between the source/body contact and the trenched gate of the square cell configuration.

106. A POSITA at the time of the filing of the '409 Patent would therefore understand the purported “invention” to require a “design rule that the greatest difference between the longest distance and the shortest distance between the source/body contact and the trenched gate is significantly less than a predefined value to achieve an improved device ruggedness.” A POSITA would further understand that “substantially squared-shaped” of claim 1 is in the context of making “the space between the trenched gate and the metal contact more uniform in the closed cell to enhance the device ruggedness,” according to the specification of the '409 Patent at 2:5-7. Having merely an essentially square-shaped from the top view would not satisfy the design rule requirement of making the said space more uniform.

107. Accordingly, it is my opinion that “substantially square-shaped” of claim 1 should be construed as “from a top-view cross-sectional perspective, a square-shape that satisfies a design rule that the greatest difference between the longest distance and the shortest distance between the circular trench contacts and the trenched gates is significantly less than a predefined value.”

108. In contrast, “substantially square-shaped” in claim 1 of the ’409 Patent cannot mean “from a top-view cross-sectional perspective, having a largely or essentially square shaped, other than the recited ‘rounded corners,’” as proposed by Force MOS. Not only did Force MOS amend the claims away from such interpretation but also this interpretation would cover the prior art. *See supra* § IX.E.1. I understand that under the principles of claim construction, it would be improper for Force MOS’s proposed construction to cover a prior art design or seek to recapture claim scope that was given up during prosecution.

109. Further, Force MOS’s proposed plain and ordinary meaning includes “having a *largely* or *essentially* square shaped,” which does not provide any clarity to a POSITA relative to the original claim term.

4. “a top surface of said semiconductor substrate”

“a top surface of said semiconductor substrate” – ’409 Patent Claim 1	
ASUS’s Proposed Construction	Force MOS’s Proposed Construction
Indefinite or, in the alternative, “the top surface of the bottom base layer of the semiconductor power device”	Plain and ordinary meaning: “from a top view cross-sectional perspective, the circular trench contact is in the shape of a circular hole, and the circular contact trench penetrates into the top surface of the semiconductor (i.e. having a structure consistent with, prior to being filled with the contact metal plug, a trench with a cylindrical shape oriented having been etched into the semiconductor)” “a top surface of said semiconductor substrate” means the “the top surface of the semiconductor material, where top refers to being in the direction toward the semiconductor’s front side, i.e. the side where primary photolithography was performed”

110. Based on the specification and file history of the ’409 Patent, it is my opinion that the term “a top surface of said semiconductor substrate” is indefinite because it would be unclear

to a POSITA what the term refers to in the context of the claims, the specification, and the file history of the '409 Patent. Force MOS's proposed construction for the plain and ordinary meaning for this term only highlights why a POSITA lacks clarity for the term's meaning.

111. In the alternative, it is further my opinion that the term "a top surface of said semiconductor substrate" should be construed as "the top surface of the bottom base layer of the semiconductor power device," according to ASUS's proposed construction.

112. The term "a top surface of said semiconductor substrate" appears in one limitation of asserted claim 1, which is reproduced below:

[1.c] said circular trench contact comprises a hole opened from ***a top surface of said semiconductor substrate*** and is filled with a contact metal plug wherein sidewalls of said hole are surrounded by and in contact said source and body regions and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact; and

113. "[A] top surface of said semiconductor substrate" is indefinite because a POSITA's understanding of this claim term is inconsistent with what Force MOS contends to be the plain and ordinary meaning of the term. Force MOS contends the plain and ordinary meaning of "a top surface of said semiconductor substrate" is the "top surface of the semiconductor material, where top refers to being in the direction toward the semiconductor's front side, i.e. the side where primary photolithography was performed." It makes no sense to me how the semiconductor substrate is the *top* of the entire semiconductor material. I have found nothing to support Force MOS's proposed construction. In fact, I have found the opposite as discussed in the paragraphs below.

114. If Force MOS's proposed construction is applied, then a POSITA would have no understanding for this claim term in the context of the '409 Patent's claim language and

specification. The claim language itself provides no guidance that matches Force MOS's plain and ordinary meaning for "substrate." The claim simply recites "a plurality of transistor cells formed in a semiconductor substate" and "a hole opened from the top surface of said semiconductor substrate." The specification does not resolve this lack of clarity. Instead, the specification and figures use "substrate" in a way that a POSITA would generally understand the plain and ordinary meaning to be. A POSITA, when reading the '409 Patent, would not assume that substrate would refer to the top surface of the entire semiconductor material when nothing in the patent indicates as much.

115. It remains unclear to a POSITA what is meant by a "top surface of said semiconductor substrate" if its plain and ordinary meaning does not refer to the bottom or supporting layer. Force MOS is again attempting to re-write the claims through a purported plain and ordinary meaning construction. Force MOS's proposed plain and ordinary meaning construction assumes that a POSITA would know the terms carry a *different* meaning than the specification, figures, and the typical definition of "substrate" in this context. To the contrary, a POSITA would understand the substrate to be the bottom most layer of a semiconductor device, thus the context of the claim term (requiring a hole opened from the top of the bottom layer) and Force MOS's proposal (requiring the "substrate" to include substantially more than the bottom layer of the device) are contrary to the POSITA's understanding, the figures, and the specification. For all of these reasons, in my opinion, the claim term "a top surface of said semiconductor substrate" is indefinite.

116. If the Court decides this claim term is definite, then the Court should apply ASUS's proposed construction. ASUS's proposed construction is supported by a POSITA's general understanding of the term, by the patent's specification, and by technical and non-technical

dictionaries. Generally, a POSITA would understand that a semiconductor substrate is the supporting semiconductor layer upon which subsequent layers or materials are fabricated or attached. This is consistent with the specification of the '409 Patent, which states that the closed semiconductor power cell is supported on an epitaxial layer formed on top of a semiconductor substrate. '409 Patent at 1:48-50.

117. In addition, I have reproduced Figure 2A of the '409 Patent below. Figure 2A, along with Figures 2B and 2C are cross-sectional views of the semiconductor power device of the purported invention. *Id.* at 3:33-34, 3:42-45. The specification describes the device in Figure 2 as the “closed semiconductor power cell is supported on an epitaxial layer *formed on top of a semiconductor substrate.*” *Id.* at 3:48-50, 4:22-24. As depicted below, the “N+ Substrate” layer is located on the bottom layer of the power cell, and the “N Epitaxial Layer” is located above that layer. There is nothing below the N+ Substrate layer. Thus, in the context of the '409 Patent, a substrate is the bottom or supporting layer.

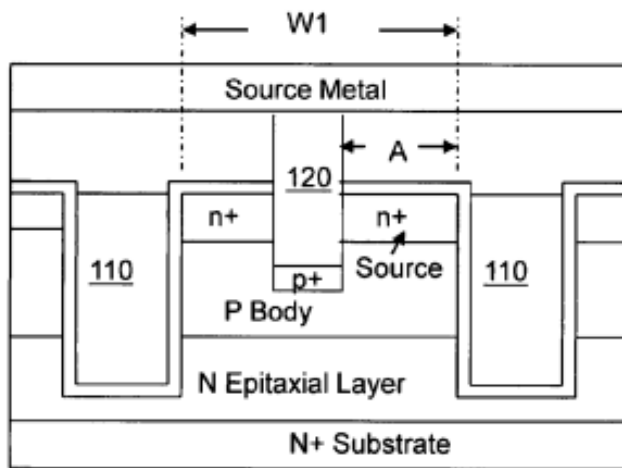


Fig. 2A (A-A' Cross Section)

118. Both technical and non-technical definitions provide further support that “substrate” refers to something on the bottom or a supporting material. The Institute of Electrical and Electronics Engineers (IEEE) is a professional association of electronics engineering, electrical

engineering, and other related disciplines. The IEEE provides a dictionary of standard terms and definitions that practitioners in the field of electronics frequently use as a reference. The IEEE defines “substrate” as “[t]he *supporting material* upon or within which an integrated circuit is fabricated or to which an integrated circuit is attached.” “Substrate,” IEEE Standard Dictionary of Electrical & Electronics Terms, Second Ed., 1978, p. 689 (emphasis added) (ASUS_CC_00041 at 45). The American Heritage College Dictionary, defines “substrate” or “substratum” as “*a foundation or groundwork*” and as “*the material on which another material is coated or fabricated.*” “Substrate,” The American Heritage College Dictionary, Third Edition, 1997, Houghton Mifflin Company, p. 1354 (ASUS_CC_000030 at 33).

119. Taking all of this together, it is my opinion that a POSITA would understand “a top surface of said semiconductor substrate” to be “the top surface of the bottom base layer of the semiconductor power device.” That is, the layer labeled as “N+ substrate” in Figure 2A.

120. Accordingly, it is my opinion that “a top surface of said semiconductor substrate is indefinite or, in the alternative, should be construed as “the top surface of the bottom base layer of the semiconductor power device.”

5. “said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact”

“said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact” – ’409 Patent Claim 1	
ASUS’s Proposed Construction	Force MOS’s Proposed Construction
“at all circumferential points along the sides of the circular trench contact, said source and body regions are located between the circular trench contact and the gate oxide lining of the trenched gates.”	Plain and ordinary meaning: “said circular trench contact is separate from said trenched gates” means “the circular trench contact is physically separated from the trenched gates” “with said source region and body region disposed between a gate oxide lining of said

	trenched gates and all circumferential points of the circular trench contact” means “all around the circumference of a circular trench contact, from a cross-sectional perspective, source and body regions are located between the circular trench contact and the gate oxide lining of the trenched gates”
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121. Based on the specification and file history of the '409 Patent, it is my opinion that this claim term should be construed as “at all circumferential points along the sides of the circular trench contact, said source and body regions are located between the circular trench contact and the gate oxide lining of the trenched gates,” according to ASUS’s proposed construction.

122. This term appears in one limitation of asserted claim 1, which is reproduced below:

[1.c] said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug wherein sidewalls of said hole are surrounded by and in contact said source and body regions and *said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact*; and

123. The claim language and the specification support ASUS’s proposed construction. Reading the claim language, a POSITA would understand that the claim requires that the source region and the body region be disposed between the gate oxide lining of the trench gates at *all* points around the circular trench contact. The claim’s use of “all” would indicate that at every point around the circular trench contact there would be a source region and a body region between the trench gate oxide lining.

124. As shown in Figure 3A, reproduced below, the claim requirements are satisfied where the red x’s are drawn because all around the circumference of the circular trench contact the source region and the body region are disposed between the trench gate oxide lining. However, the claim requires that *all* circumferential points of the circular trench contact, not some points,

would be disposed between the source region and the body region and the trench gate oxide lining. The blue x's show where this is not the case. At the blue x's, the circumferential points of the circular trench contact are nowhere near the trench gate oxide lining, the source region, or the body region.

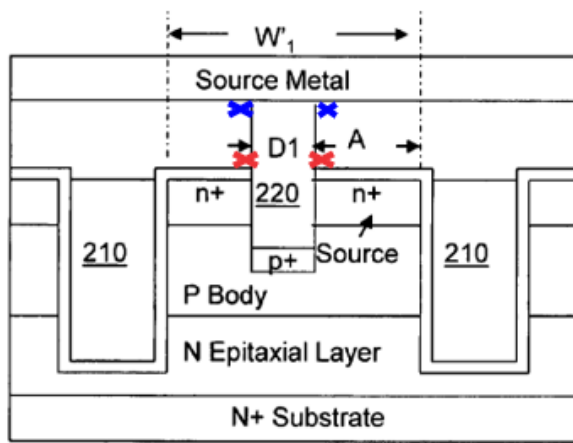


Fig. 3A

125. I disagree with Force MOS's proposed construction for the plain and ordinary meaning of this term. Force MOS's proposed construction for the plain and ordinary meaning for this term is "all around the circumference of a circular trench contact, from a cross-sectional perspective, source and body regions are located between the circular trench contact and the gate oxide lining of the trenched gates." This construction effectively reads out the claim requirement for "all" and just focuses on the circumferential points where the source region, body region, and trench gate oxide lining are located. The claim, however, is not as narrow, and this interpretation improperly limits the claim.

126. ASUS's proposed construction attempts to give meaning to the "all" of the claim consistent with what a POSITA would understand. A POSITA would understand that the claim's use of "all" means that every point around the circumference of the circular trench contact would be disposed between the source region, the body region, and the trench gate oxide lining. By

requiring that “at all circumferential points along the sides of the circular trench contact,” ASUS’s proposed construction provides exactly what the claim language requires.

127. Although the patent does not provide a figure depicting or disclosure describing an embodiment where every point around the circumference of the circular trench contact is disposed between the source region, the body region, and the trench gate oxide lining, a POSITA would still understand the requirements of the claim. The claim itself provides enough context and information.

128. Accordingly, it is my opinion that this claim term should be construed as “at all circumferential points along the sides of the circular trench contact, said source and body regions are located between the circular trench contact and the gate oxide lining of the trenched gates.”

VI. THE '346 PATENT

A. Overview of the '346 Patent

129. The '346 Patent is directed to a MOSFET including a plurality of power cells. To connect the front electrode to source regions of the power cells a source contact trench of a particular shape is used. The source contact trench used to connect to the power cells has vertical sidewalls in one area and tapered sidewalls in a separate area. A copper wire is then connected to the front metal. The purported invention is shown in Fig. 2:

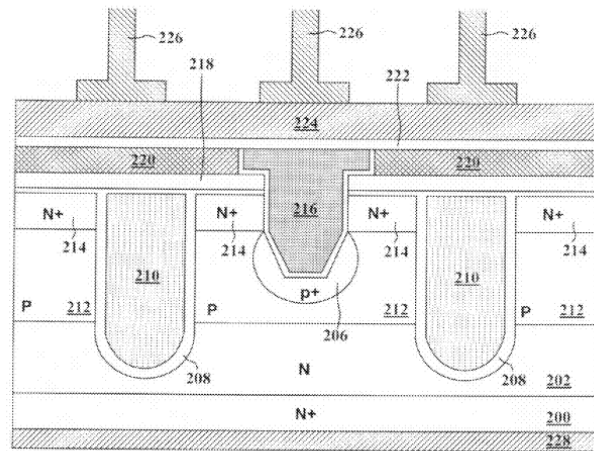


Fig. 2

130. Gates 210 control the flow of current from front metal 224 to rear metal 228. The front metal 224 is connected to the source region 214 and body region 212 by a metal plug in source contact trench 216. '346 Patent at 4:15-21, 34-36. The N+ substrate serves as the drain of the transistor. *Id.* at 3:27-29. The patent describes the shape of the plug within the source contact trench 216 as follows:

Especially, the sidewalls of source-body contact trench are perpendicular to the front surface of epitaxial layer within insulating layer and N+ source region 114 while is oblique within P-body region 212 with a taper angle less than 85 degree. . . . When etching through the second insulating layer and N+ source region, sidewalls of source-body contact trench 216a are substantially vertical (90+/- 5 degree) along the N+ source region while etching into P-body regions, sidewalls of source contact trench 216a has taper angle (less than 85 degree) respect to top surface of epitaxial layer, as shown in FIG. 3C.

Id. at 3:38-41, *id.* at 4:15-21.

131. The actual formation of the source contact trench of this particular shape is shown in Fig. 3C:

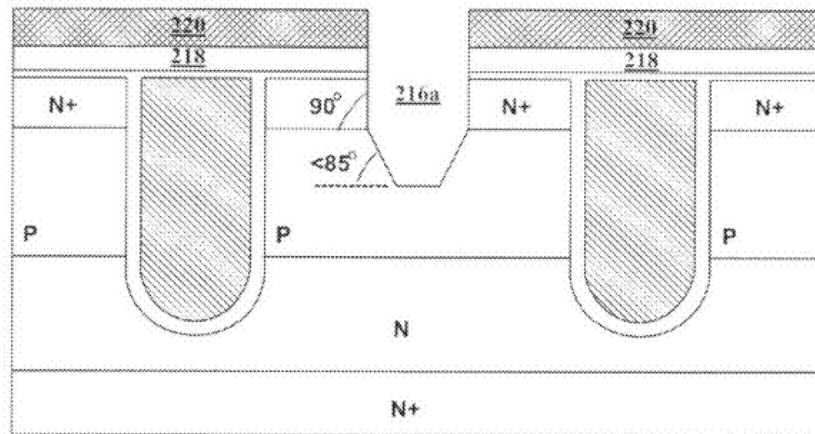


Fig. 3C

Trench 216 is shown formed with vertical sidewalls (“90°” with respect to the top surface of the epitaxial layer (N)) in the source regions (N+) and tapered side walls (“<85°” with respect to the top surface of the epitaxial layer (N)) in the body region (P). *See also id.* at 4:15-21.

B. The '346 Patent File History

132. I understand that U.S. Patent Application No. 12/292,780 (the “’780 Application”), titled “TRENCH MOSFET WITH TRENCH SOURCE CONTACT HAVING COPPER WIRE BONDING,” was filed on November 26, 2008, and issued on December 7, 2010. *Id.* at 1 (Cover); FORCE-MOS0000125 at 125. I also understand that, on April 6, 2010, the examiner issued a non-final rejection of the pending claims under 35 U.S.C. § 103 as being unpatentable over Hshieh et al. (5,629,543) in view of Lin et al. (2008/0080112). *Id.* at 167-70. On December 30, 2008, the applicant responded to the examiner’s rejection by distinguishing the claimed inventions from the Hshieh reference. *Id.* at 196. Specifically, the applicant stated, “Hshieh’s P+ deep region lacks the claimed, ‘penetrating through said second insulating layer and said source regions with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions, and further extending into P-body regions with tapered sidewalls with respect to said top surface of

said epitaxial layer.” *Id.* On October 1, 2010, the examiner was persuaded by the applicant’s arguments over the prior art and allowed the pending claims. *Id.* at 208.

C. The Asserted Claims and Disputed Claim Language

133. My understanding is that Force MOS has asserted claims 1-7 and 16-20. As relevant, I have reproduced Claim 1, Claim 16, and Claim 17 below, with the disputed claim terms shown in ***bold italics***.

Claim 1:

[1.pre] A trench MOSFET comprising a plurality of semiconductor power cells with each cell comprising a plurality of trench gates surrounded by a plurality of source regions of a first type conductivity above a plurality of body regions of second type conductivity above a drain region disposed on a bottom surface of a substrate, said trench MOSFET further comprising:

[1.a] a substrate of said first type conductivity;

[1.b] an epitaxial layer of said first type conductivity over said substrate, having a lower doping concentration than said substrate;

[1.c] a plurality of trenches extending into said epitaxial layer, ***surrounded by*** a plurality of said source regions of said first type conductivity above said body regions of said second type conductivity;

[1.d] a first insulating layer lining said trenches as gate oxide;

[1.e] a doped polysilicon of said first type conductivity as said trench gates overlying said first insulating layer;

[1.f] a second insulating layer disposed over said epitaxial layer to isolate a source metal which contacts said both source and body regions, from said doped polysilicon as said trench gates;

[1.g] ***a plurality of source contact trenches*** penetrating through said second insulating layer and said source regions ***with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions***, and ***further extending into said body regions with tapered sidewalls with respect to said top surface of said epitaxial layer***;

[1.h] a front metal disposed on the front surface of said trench MOSFET as said source metal;

[1.i] a backside metal disposed on the backside of said substrate as a drain metal;

[1.j] at least one copper wire electrically bonded to said source metal.

Claim 16:

[16.pre] A trench MOSFET comprising:

[16.a] a substrate;

[16.b] a drain metal below said substrate;

[16.c] an n epitaxial layer formed on said substrate;

[16.d] P-body regions formed on said n epitaxial layer;

[16.e] N+ source regions formed on said P-body regions;

[16.f] a plurality of insulating layers formed on said N+ source regions;

[16.g] a source metal formed on said insulating layers;

[16.h] trench gates extending through said N+ source regions, said P-body regions and said n epitaxial layer;

[16.i] *a plurality of trench source contacts comprising a plurality of sidewalls, two of said sidewalls substantially perpendicular to a top surface of said source regions and two other sidewalls tapered with respect to said source regions*, wherein said trench source contacts extend through said insulating layers, said N+ source regions, said P-body regions and said n epitaxial layer; and

[16.j] copper wire electrically bonded to said source metal.

Claim 17

[17.a] The trench MOSFET of claim 16, further comprising *P+ areas wrapping said sidewalls and bottom of said trench source contacts within said P-body regions* and an angle between said trench source contact sidewalls and said source region is 90+/-5 degrees within said source regions, and is less than 85 degrees within said P-body regions.

D. Person of Ordinary Skill in the Art (“POSITA”)

134. I am informed and understand that the claims of a patent are judged from the perspective of a hypothetical construct involving a “person of ordinary skill in the art,” or POSITA.

The “art” is the field of technology to which the patent is related. I understand that the purpose of using the viewpoint of a POSITA is for objectivity. I understand that a POSITA is presumed to know and be familiar with the relevant art in the field at the time of invention and is also presumed to possess an average level of creativity. In determining who would be a person of ordinary skill, I considered at least the following criteria: (a) the type of problems encountered in the art; (b) prior art solutions to those problems; (c) the rapidity with which innovations are made; (d) the sophistication of the technology; and (e) the education level of active workers in the field.

135. I understand that Force MOS claims the earliest priority date for the ’346 Patent is November 26, 2008, the filing date of U.S. Patent Application Serial No. 12/292,780. It is my opinion that a POSITA for the ’346 Patent would have earned a Master’s degree in electrical engineering (or a related field) and had at least two years of relevant work experience in the field of integrated circuit design and manufacturing. I consider myself a POSITA of the ’346 Patent because I had at least the level of a POSITA in the relevant timeframe.

E. Construction of the Agreed Terms of the ’346 Patent

136. I understand the parties have agreed to the meanings of the following terms in the ’346 Patent:

Term	Construction
“front” (’346 Patent, cl. 1)	The side of the three-dimensional device to which the photolithography was applied
“back” (’346 Patent, cl. 1)	The side of the three-dimensional device opposite the “front”
“top” (’346 Patent, cls. 1, 2, 16) “upper” (’346 Patent, cl. 18)	Referring to the direction of the “front” (e.g., the top surface of a layer refers to the side of the layer that is facing toward the front of the device)

“bottom” (’346 Patent, cls. 1, 17)	Referring to the direction of the “back” (e.g., the bottom surface of a layer refers to the side of the layer that is facing toward the back of the device)
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F. Construction of the Disputed Claim Terms of the ’346 Patent

1. “plurality of source contact trenches . . . with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions”

“plurality of source contact trenches . . . with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions” – ’346 Patent Claim 1	
ASUS’s Proposed Construction	Force MOS’s Proposed Construction
“a plurality of source contact trenches ... with vertical sidewalls substantially perpendicular to a top epitaxial surface within [entire/whole] said source regions”	Plain and ordinary meaning: “in the second insulating layer and source layer, the source contact trench has sidewalls that are largely or essentially perpendicular to the top of the epitaxial layer (the surface of the semiconductor in which the trenches have been etched into), i.e. no requirement as to “entire/whole” trench in source region being substantially perpendicular”

137. Based on my review of the ’346 Patent’s claims, its specification, and its file history, it is my opinion that this claim term should be construed as “a plurality of source contact trenches . . . with vertical sidewalls substantially perpendicular to a top epitaxial surface within [entire/whole] said source regions,” according to ASUS’s proposed construction. This term appears in one limitation of asserted claim 1, which is reproduced below:

[1.g] a plurality of source contact trenches penetrating through said second insulating layer and said source regions with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions, and further extending into said body regions with tapered sidewalls with respect to said top surface of said epitaxial layer;

138. In its July 6, 2010 reply to the examiner’s April 6, 2010 rejection, the applicant distinguished the uniquely shaped partially vertical, partially tapered structure of the claimed

source contact trenches over the less specific structure disclosed in the prior art cited by the examiner. FORCE-MOS0000125 at 196. Below, I have reproduced an excerpt from the applicant as well as the Figure 3F from Hsieh:

The P+ Deep Region of Hsieh and The Claimed Invention

The P+ deep region 24, regarded by the Examiner as the source contact trenches of the present invention, in Hsieh, is not a source contact trench 216a.

The P+ deep region of Hsieh provides electrical contact to the underlying P body region for the overlying metallization layer (Col. 2, lines 65-67 and Col. 3, lines 1-6).

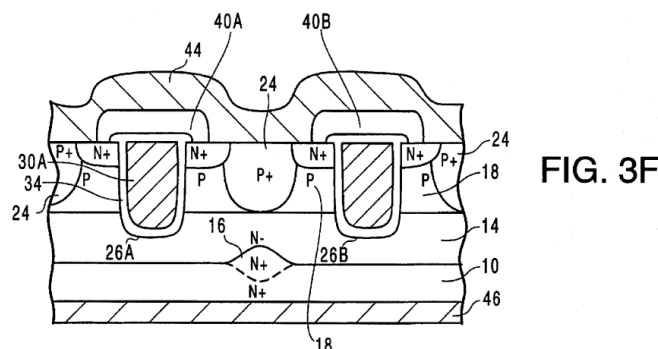
Furthermore, even if one were to consider the P+ deep region of Hshieh to be the claimed source contact trench, the structure of Hshieh's P+ deep region is fundamentally different from that of the claimed source contact trench.

Hshieh's P+ deep region lacks the claimed, "penetrating through said second insulating layer and said source regions with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions, and further extending into P-body regions with tapered sidewalls with respect to said top surface of said epitaxial layer." There is not enough structure illustrated in Hshieh's P+ deep region of Fig. 3F to determine the claimed tapered structure.

Lin is only offered for a teaching of “a front metal disposed on front surface of device as source metal and at least one copper wire is electrically bonded to said source metal.” (Office Action at page 3).

Lin however, does not remedy the deficiencies of Hshieh.

Accordingly, for all of the above reasons, the rejection of claims 1-7 as unpatentable over the combination of Hsieh and Lin should be withdrawn.



Following the applicant's remarks to distinguish the claims away from Hshieh, the examiner issued the pending claims.

139. Applicant’s statements here support my opinion that ASUS’s proposed correction that the source contact trenches of the claimed invention must have vertical sidewalls within the *entire or whole* source regions. In particular, applicant makes it clear that even if one were to consider the P+ deep region of Hshieh to be the claimed source contact trench, “it is not enough structure illustrated in Hshieh’s P+ deep region of Fig. 3F to determine the claimed tapered structure.” *Id.* This signals to me that the applicant considers the claimed invention to require the sidewalls to be vertical over the entire or whole source region perpendicular to the top of the epitaxial layer.

140. Force MOS’s proposed construction for this claim term seeks to evade the statements it made during prosecution. Force MOS cannot now argue the source contact trench of the claimed invention can have sidewalls “largely or essentially perpendicular to the top of the epitaxial layer” when Hshieh had that structure. Thus, Force MOS’s proposed construction cannot be correct if it both captures a prior art structure and is counter to statements made during prosecution.

141. Accordingly, it is my opinion that “plurality of source contact trenches . . . with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions” should be construed as “a plurality of source contact trenches ... with vertical sidewalls substantially perpendicular to a top epitaxial surface within [entire/whole] said source regions.”

2. “a plurality of trench source contacts comprising a plurality of sidewalls, two of said sidewalls substantially perpendicular to a top surface of said source regions”

“a plurality of trench source contacts comprising a plurality of sidewalls, two of said sidewalls substantially perpendicular to a top surface of said source regions” – ’346 Patent Claim 16	
ASUS’s Proposed Construction	Force MOS’s Proposed Construction
“a plurality of trench source contacts comprising a plurality of sidewalls, two of said sidewalls substantially perpendicular to a	Plain and ordinary meaning:

top surface of said source regions within entire/whole said source regions”	“substantially perpendicular to a top surface of said source regions” means “essentially perpendicular to the top of the source regions (i.e. the surface of the semiconductor in which the trenches have been etched into)” No requirement that entire/whole source region have substantially perpendicular side walls
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142. Based on my review of the ’346 Patent’s claims, its specification, and its file history, it is my opinion that this claim term should be construed as “a plurality of trench source contacts comprising a plurality of sidewalls, two of said sidewalls substantially perpendicular to a top surface of said source regions within entire/whole said source regions,” according to ASUS’s proposed construction. This term appears in one limitation of asserted claim 16, which is reproduced below:

[16.i] a plurality of trench source contacts comprising a plurality of sidewalls, two of said sidewalls substantially perpendicular to a top surface of said source regions and two other sidewalls tapered with respect to said source regions, wherein said trench source contacts extend through said insulating layers, said N+ source regions, said P-body regions and said n epitaxial layer; and

143. It is my opinion that the same reasoning I applied for the “plurality of source contact trenches . . . with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions” term applies here. Therefore, I incorporate that analysis herein to support ASUS’s proposed construction for this claim term.

3. “plurality of source contact trenches . . . further extending into said body regions with tapered sidewalls with respect to said top surface of said epitaxial layer”

“plurality of source contact trenches . . . further extending into said body regions with tapered sidewalls with respect to said top surface of said epitaxial layer” – ’346 Patent Claim 1	
ASUS’s Proposed Construction	Force MOS’s Proposed Construction

“a plurality of source contact trenches ... further extending into said body regions with tapered sidewalls [within entire/whole body regions] with respect to said top surface of said epitaxial layer”	Plain and ordinary meaning: “as the source contact trench extends into the body region, it has sidewalls that are tapered (that is, the source contact trench in the body has narrower portions than portions in the source region), i.e. no requirement as to ‘entire/whole’ trench in body region be tapered”
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144. Based on my review of the ’346 Patent’s claims, its specification, and its file history, it is my opinion that this claim term should be construed as “a plurality of source contact trenches . . . further extending into said body regions with tapered sidewalls [within entire/whole body regions] with respect to said top surface of said epitaxial layer,” according to ASUS’s proposed construction. This term appears in one limitation of asserted claim 1, which is reproduced below:

[1.g] *a plurality of source contact trenches* penetrating through said second insulating layer and said source regions with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions, and *further extending into said body regions with tapered sidewalls with respect to said top surface of said epitaxial layer*;

145. In its July 6, 2010 reply to the examiner’s April 6, 2010 rejection, the applicant distinguished the uniquely shaped partially vertical, partially tapered structure of the claimed source contact trenches over the less specific structure disclosed in the prior art cited by the examiner. Below, I have reproduced an excerpt from applicant as well as the Figures 2 and 3C from the ’346 Patent:

The Source Metal of Hsieh and The Claimed Invention

The source metal, regarded by the Examiner as element 44 (Fig. 3F) of Hsieh is in direct and horizontal planar contact with both N+ source region 20 and P+ deep body contact region depicted as deep body region 24 (Fig. 3F, col. 3, lines 2-3 and col. 4 line 54) formed by P+ ion implantation.

In contrast to the present invention as shown in Figs. 2 and 3C, for example, the trench MOSFET has source contact trench 216a (Fig. 2) which penetrates through N+ source region 214 and further extends into the P-body region 212. The source metal in the present invention vertically connects to the N+ source region and P+ region through a Tungsten plug as opposed to being in horizontal planar contact.

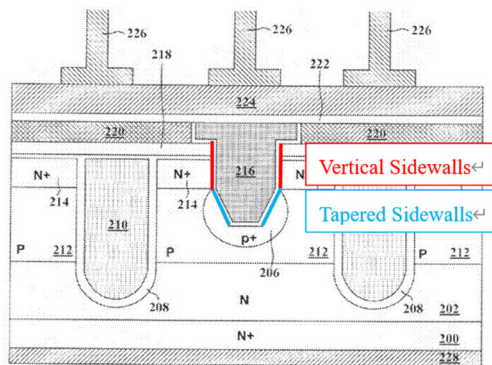


Fig. 2

Fig. 2 of US'346 illustrating Claim 1 (annotated)

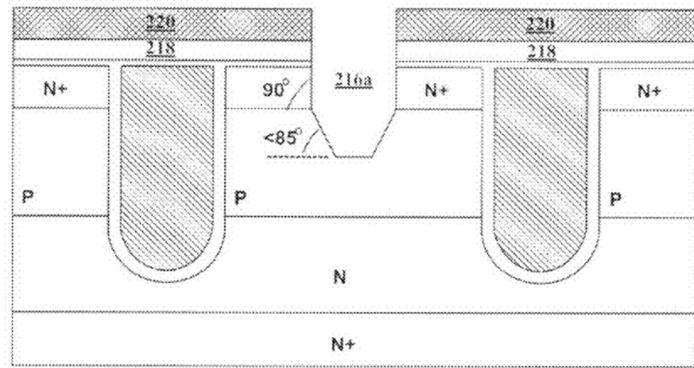


Fig. 3C

FORCE-MOS0000125 at 195-96; '346 Patent at Figs. 2, 3C.

146. Applicant's statements during prosecution indicate that applicant characterizes Figures 2 and 3C as the purported invention of the '346 Patent. As shown in annotated Figure 2, the sidewalls (blue) are tapered within the entire or whole body P-body region (212). Therefore, I agree with ASUS's proposed construction because it is consistent with the figures of the '346 Patent and with applicant's admissions during prosecution.

147. Force MOS's proposed construction for the plain and ordinary meaning fails to account for statements in the file history and the figures in the patent itself. Force MOS cannot argue that there is "no requirement as to the 'entire/whole' trench in the body region be tapered" when the intrinsic evidence establishes otherwise.

148. Accordingly, it is my opinion that “plurality of source contact trenches . . . further extending into said body regions with tapered sidewalls with respect to said top surface of said epitaxial layer” should be construed as “a plurality of source contact trenches . . . further extending into said body regions with tapered sidewalls [within entire/whole body regions] with respect to said top surface of said epitaxial layer.”

4. “a plurality of trench source contacts comprising a plurality of sidewalls, . . . two other sidewalls tapered with respect to said source regions”

“a plurality of trench source contacts comprising a plurality of sidewalls, . . . two other sidewalls tapered with respect to said source regions” – ’346 Patent Claim 16	
ASUS’s Proposed Construction	Force MOS’s Proposed Construction
“a plurality of trench source contacts comprising a plurality of sidewalls, . . .two other sidewalls tapered with respect to said source regions within entire/whole said body regions”	Plain and ordinary meaning: “tapered with respect to said source regions” means “sidewalls that are tapered with respect to the top of the source regions (i.e. the surface of the semiconductor in which the trenches have been etched into), that is, the source contact trench has narrower portions deeper in the trench” No requirement that entire/whole body region have tapered side walls

149. Based on my review of the ’346 Patent’s claims, its specification, and its file history, it is my opinion that this claim term should be construed as “a plurality of trench source contacts comprising a plurality of sidewalls, . . .two other sidewalls tapered with respect to said source regions within entire/whole said body regions,” according to ASUS’s proposed construction. This term appears in one limitation of asserted claim 16, which is reproduced below:

[16.i] a plurality of trench source contacts comprising a plurality of sidewalls, two of said sidewalls substantially perpendicular to a top surface of said source regions and two other sidewalls tapered with respect to said source regions, wherein said trench source contacts extend through said insulating layers, said N⁺ source regions, said P-body regions and said n epitaxial layer; and

150. It is my opinion that the same reasoning I applied for the plurality of source contact trenches . . . further extending into said body regions with tapered sidewalls with respect to said top surface of said epitaxial layer” term applies here. Therefore, I incorporate that analysis herein to support ASUS’s proposed construction for this claim term.

5. “P+ areas wrapping said sidewalls and bottom of said trench source contacts within said P-body regions”

“P+ areas wrapping said sidewalls and bottom of said trench source contacts within said P-body regions” – ’346 Patent Claim 17	
ASUS’s Proposed Construction	Force MOS’s Proposed Construction
“P+ areas [completely encompassing/enclosing] [the two other sidewalls tapered within entire/whole body regions with respect to said source regions] and [a] bottom of [the plurality of trench source contacts] within said P-body regions”	Plain and ordinary meaning: “P+ region follow contours of sidewalls and bottom of trench source contact” “No requirement that P+ regions completely encompass tapered sidewalls”

151. Based on my review of the ’346 Patent’s claims, its specification, and its file history, it is my opinion that this claim term should be construed as “P+ areas [completely encompassing/enclosing] [the two other sidewalls tapered within entire/whole body regions with respect to said source regions] and [a] bottom of [the plurality of trench source contacts] within said P-body regions,” according to ASUS’s proposed construction. This term appears in one limitation of asserted claim 17, which is reproduced below:

[17.a] The trench MOSFET of claim 16, further comprising ***P+ areas wrapping said sidewalls and bottom of said trench source contacts within said P-body regions*** and an angle between said trench source contact sidewalls and said source region is 90+/-5 degrees within said source regions, and is less than 85 degrees within said P-body regions.

152. The ’346 Patent provides ample disclosure to support ASUS’s proposed construction for this term. The specification consistently refers to the P+doped area “wrapping” around the tapered sidewalls of the trench source contact. *See* ’346 Patent at 2:19-21 (“P+ area to

wrap the bottom and the slope sidewalls of the trench source contact . . .”); *id.* at 2:54-56 (same); *id.* at 4:26-29 (same); *id.* at 3:43-45 (“[A] heavily P+ doped area 206 is formed wrapping the slope trench and bottom in P-body region 212 . . .”). It is my opinion that when the patent refers to “wrapping,” it goes beyond mere “following the contours of sidewalls and [the] bottom trench source contact,” as Force MOS contends. Instead, the patent contemplates the P+ areas completely encompassing or enclosing the tapered sidewalls with the body region. Figures 2 and 3D (reproduced below) reinforce this interpretation.

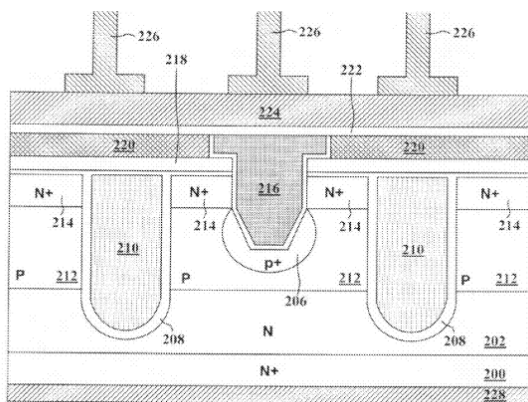


Fig. 2

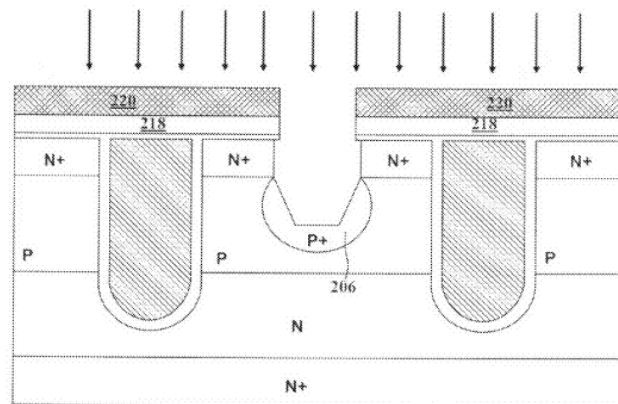


Fig. 3D

As depicted, the P+ area 206 in both figures goes all way around the trench source contact 216 such that the tapered sidewalls are entirely covered.

153. Further, a POSITA would understand from the specification that the purpose of the P+ implant is to enhance avalanche capability. *Id.* at 4:26-29. As such, a non-ohmic contact region would be created if the P+ area does not cover all the sidewalls and bottom of the trench source contact, especially in the sidewall area that is adjacent to the N+ region. Such a non-ohmic contact region would not achieve the stated purpose of enhancing the avalanche capability.

154. Force MOS’s proposed construction for the plain and ordinary meaning of this term bears no relation to the specification and the above-reproduced figures. Under Force MOS’s proposed construction, a P+ region that follows contours of sidewalls and bottom of trench source

contact would not “wrap” at all. It would be nothing more than a P+ area liner around the tapered sidewalls of the trench source contact. This is not what the claim requires. The P+ area must wrap around the tapered sidewalls of the trench source contact. ASUS’s proposed construction serves this purpose and is consistent with what the claim requires.

155. Accordingly, it is my opinion that “P+ areas wrapping said sidewalls and bottom of said trench source contacts within said P-body regions” should be construed as “P+ areas [completely encompassing/enclosing] [the two other sidewalls tapered within entire/whole body regions with respect to said source regions] and [a] bottom of [the plurality of trench source contacts] within said P-body regions.”

I declare under penalty of perjury that the foregoing is true and correct.

Executed this 30th day of January, 2024 at Fremont, CA.

Respectfully Submitted,



Dr. David Liu

EXHIBIT A

DAVID KUAN-YU LIU, Ph.D.

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PROFESSIONAL PROFILE

- Technical expert with over 20 years of industrial experience in the development of advanced CMOS devices and process technology, with special emphasis on non-volatile semiconductor memory devices and process technology, and high-voltage semiconductor devices, with additional 12 years of experience serving as expert consultant.
 - Named inventor on 99 US patents.
- Consultant and expert witness for past 15 years in semiconductor intellectual property evaluation and patent litigation, with deposition experience and successful ITC trial testifying experience.
- Successful track record in transitioning products from development phase to high-volume manufacturing phase, both as an individual contributor and as manager/director.
- Co-founder of an LLC in the development and licensing of intellectual property with emphasis on embedded flash memory technology.
- Co-founder of a semiconductor memory start-up company (Progressant Technologies, Inc.); participated in its successful sale to Synopsys, Inc.
- Fluent in Mandarin Chinese (native language) and English; over 10 years experience as real-time translator of church sermons and proficient in written translation.

EDUCATION

Stanford University, Palo Alto, California

Ph.D., Electrical Engineering (1989)

Thesis: Physics and Technology of Novel Conductivity-Modulated Power MOSFET's

M.S., Electrical Engineering (1985)

Coursework in integrated-circuit technology, semiconductor device physics, computer modeling of semiconductor devices and fabrication processes, and solid-state physics

University of California, Berkeley, California

B.S., Electrical Engineering (1983)

Certificate of Distinction (awarded annually to the top EECS graduate)

KEY EXPERT WORK EXPERIENCE:

Case:	Element Capital. vs. Beijing BOE Display Technology Co., Ltd.
Jurisdiction:	Civil Action No. 2:22-cv-00118-JRG Eastern District of Texas
Work Product:	Expert consulting work relating to OLED technology. Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 3 patents.
Nature of Case:	Civil action.
Counsel:	Retained by Fish & Richardson (Contact: Linhong Zhang)
Date:	4/23 – Current

Case: **Daedalus Prime LLC vs. Samsung Electronics Co.,**
Jurisdiction: Civil Action E.D. TX, Marshall Div., No. 2:22-cv-353
Eastern District of Texas, Marshall Div., and
Investigation No. 337-TA-1336
Work Product: Expert consulting work relating to FINFET process technology.
Patent analysis and prior art review toward preparation of IPR
petition material and draft of declaration on 2 patents. Source code
database viewing (GDS layout and process flow documents) for
supporting of non-infringement position.
Nature of Case: Civil action and ITC Investigation on Certain Semiconductor Devices,
Mobile Devices Containing the Same and Components Thereof..
Counsel: Retained by Fish & Richardson (Contact: Kevin Su)
Date: 10/22 – 4/23

Case: **Netlist, Inc. vs. Samsung Electronics Co. Ltd. et al.,**
Jurisdiction: Civil Action No. 2:21-cv-00463
Eastern District of Texas
Work Product: Expert consulting work relating to memory modules.
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Tony Nguyen)
Date: 8/22 – Current

Case: **Vervain, LLC vs. Micron Technology & related IPR Petition**
Jurisdiction: Action No. 6:21-cv-00487-ADA
Western District of Texas
Work Product: Patent analysis and prior art review toward preparation of IPR
petition material and draft of declaration on 4 patents, all 4 petitions
instituted, and deposed on both initial declaration and reply
declaration.
Counsel: Retained by Orrick, Herrington & Sutcliffe LLP (Contact: Jared
Bobrow)
Date: 8/21 – 2/23

Case: **Monterey Research vs. Qualcomm PTAB Matter**
Work Product: Patent analysis and prior art review toward preparation of IPR
petition material and draft of declaration.
Counsel: Retained by Jones Day (Contact: David Cochran)
Date: 12/21 – Current

Case: *Semiconductor Energy Laboratory Co., OLED Patent Matters*
Jurisdiction: Action No. 8:21-cv-00554-JAK-ADS
Central District of California
Work Product: Expert for infringement on 3 patents relating to OLED driver circuit and layout, responsibilities include source code viewing, GDS layers viewing, and claim charts review.
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Bryan Basso)
Date: 9/21 – 4/22

Case: *Apple Inc. IPR Petition for U.S. Patents 6,622,108 & 6,807,505*
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Erise IP (Contact: Paul Hart)
Date: 8/21 – 9/21

Case: *Texas Instruments IPR Petition*
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: Josh Griswold)
Date: 9/20 – 4/21

Case: *Micron Technology vs. UMC/JinHua*
Jurisdiction: Case No. 4:17-CV-06932-MMC
United States District Court for the Northern District of California
Work Product: Testifying expert, trade secret documents review, and declaration submission.
Nature of Case: Trade secret contention of Micron confidential documents.
Counsel: Retained by Jones Day (Contact: Randy Kay)
Date: 3/17 – Current

Case: *SK Hynix vs. BitMicro*
Jurisdiction: Investigation No. 337-TA-1097
United States International Trade Commission
Work Product: Testifying expert for non-infringement on 2 patents, issued expert rebuttal report, deposition taken, issued witness statement.
Nature of Case: ITC infringement case concerning module stacking of SDRAM.
Counsel: Retained by Fish Richardson (Contact: Joseph Colaanni)
Date: 11/18 – 4/19

Case: *Rohm Company IPR Petition*
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: Matt Colvin)
Date: 4/18 – 8/18

Case: *Apple Inc., vs. Qualcomm Incorporated*
Jurisdiction: Case No. 3:17-CV-02402
United States District Court for the Southern District of California
Work Product: Patent analysis and prior art review toward preparation of IPR
petition material and draft of declaration, 2 depositions taken.
Counsel: Fish & Richardson (Contact: Tony Nguyen)
Date: 1/18 – 5/19

Case: *Macronix vs. Toshiba*
Jurisdiction: Investigation No. 337-TA-1046
United States International Trade Commission
Work Product: Testifying expert for infringement and non-invalidity on 2 patents,
claim construction analysis, technical tutorial, database viewing for
evidence gathering, issuing expert report and expert rebuttal report,
deposition taken for 2 patents, issued witness statement and rebuttal
witness statement, testified in ITC court on both infringement and
invalidity.
Nature of Case: ITC infringement case concerning advanced NAND Flash memory.
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 4/17 – 10/18

Case: *Novatek Microelectronics Corp. IPR Petition*
Work Product: Patent analysis and prior art review toward preparation of IPR
petition material and draft of declaration.
Counsel: Retained by Kroub, Silbersher & Kolmykov PLLC (Contact: Sergey
Kolmykov)
Date: 2/17 – 4/17

Case: *Taiwan Semiconductor Manufacturing Company IPR Petition*
Work Product: Patent analysis and prior art review toward preparation of IPR
petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: John Goetz)
Date: 7/15 – 4/17

Case: *Triune Systems, LLC vs. Wayne Chen, et al.,*
Jurisdiction: Case No. 296-03209-2013,
District Court of Collin County, TX
Work Product: Testifying expert, database viewing, expert report, video-taped
testimony
Nature of Case: Defending against trade secret contention.
Counsel: Retained by Gordon & Rees LLP (Contact: Robert Bragalone)
Date: 5/15 – 9/15

Case: ***Macronix vs. Spansion***
Jurisdiction: Investigation No. 337-TA-922
United States International Trade Commission
Work Product: Testifying expert, claim construction analysis, technical tutorial, database viewing for evidence gathering, expert report, expert rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 9/14 – 1/15

Case: ***Macronix vs. Spansion***
Jurisdiction: Investigation No. 337-TA-909
United States International Trade Commission
Work Product: Database viewing for evidence gathering, support technical content of expert report, support technical content against rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Winston & Strawn (Contact Michael Murray)
Date: 5/14 – 1/15

Case: ***Keranos, LLC v. Analog Devices et. al.***
Jurisdiction: Civil Case No. 2:10-CV-00207
United States District Court for the Eastern District of Texas
Work Product: Claim Chart Generation and Claim Construction
Nature of Case: Patent infringement case concerning split gate Flash memory cell
Counsel: Retained by Agility IP (Contact Michelle Breit)
Date: 2/09 – 2/14

Case: ***Silicon Storage Technology, Inc. v. Xicor, LLC***
Jurisdiction: Civil Case No. CV 10-01515
United States District Court for the Northern District of California
Work Product: Expert report and declarations
Nature of Case: Matter concerning United States Reissue Patent RE38,370 on the process of flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 6/11 – 10/11

Case: ***Fast Memory Erase, LLC v. Spansion et.al.***
Jurisdiction: Civil Case No. 3:10CV-481
United States District Court for the Northern District of Texas
Work Product: Declarations
Nature of Case: Defending Motion for Attorney Fees.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/10 – 6/10

Case: *Fast Memory Erase, LLC v. Spansion et.al.*
Jurisdiction: Civil Case No. 3-08cv0977M
 United States District Court for the Northern District of Texas
Work Product: Testifying expert: issuing expert report, declarations, and deposition taken.
Nature of Case: Patent infringement case concerning minimizing source current during erase of Flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/09 – 5/10

EXPERIENCE:

10/07 to present: **Technical Consultant/Expert Witness**

Serving as a technical consultant and advisor in the area of semiconductor device and process technologies. Expert witness in ITC cases and district court cases, with successful testifying experience in trial hearing. Depositions taken at least 6 times for both litigation cases and IPR petitions. Experienced in source code viewings of circuit schematics and GDS layouts; seasoned in reverse engineering of integrated circuits, as well as techniques for de-processing and analyzing semiconductor chips. Responsibilities including gathering and reviewing of evidence, issuing declaration on claim construction, giving technical tutorial, issuing expert report and expert rebuttal report. Technical consultant for evaluating numerous flash memory and CMOS image sensor patent portfolios for licensing and acquisition consideration. Assessed qualitative merits of each patent portfolio and identified potential infringers and potential licensees. Generated numerous claim charts against potential infringers based on published patents, technical papers and datasheets, and reverse engineering reports.

10/07 to 4/11: **Jonker, LLC**

Inventor and Partner. Developed an intellectual property (IP) portfolio (7 U.S. patents granted and 3 U.S. patent applications pending) on zero-cost CMOS-logic-compatible embedded flash memory. Successfully negotiated the acquisition of this IP portfolio by a major semiconductor company.

8/04 to 10/07: **Maxim Integrated Products, San Jose, California**

Senior Scientist. Responsible for developing embedded non-volatile memory process technology for battery management products. Duties included supervising the development of integrated process flows at the 0.35µm and 0.18µm CMOS technology nodes. Analyzed and solved process-related reliability issues.

- 5/00 to 8/04: **Xilinx, Incorporated, San Jose, California**
Senior Manager. Responsible for developing non-volatile memory process technology for flash and CPLD products, as well as advanced CMOS process technology (75nm node). Duties included supervising the development of integrated non-volatile memory process flows at multiple CMOS technology nodes to meet product application requirements. Analyzed and solved process-related reliability issues.
- 2/00 to 5/00 **Progressant Technologies, Fremont, California**
Co-Founder. Facilitated IP development and sale of the company to Synopsys, Inc.
- 9/98 to 2/00 **Programmable Silicon Solutions, Sunnyvale, California**
Director of Process Engineering. Responsible for developing a fully logic compatible embedded flash memory technology for WSMC (a semiconductor foundry). Developed a new integrated process flow to implement a proprietary flash cell in a high-performance logic process, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement. Applied interpersonal skills to align the goals of the foundry technology development group to that of PSS. Participated in the strategic planning of a technology roadmap and foundry strategy for the company.
- 9/97 to 9/98 **AMIC Technology, Santa Clara, California**
Director of Flash Technology. Responsible for developing 0.35μm ETOX-based flash memory technology. Prepared the business plan and technology roadmap. Developed a new integrated process flow, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement.
- 5/96 to 9/97 **Altera Corp., San Jose, California**
Device Engineering Manager. Responsible for technology development, process integration, and foundry interface for 0.35μm generation of logic and EEPROM programmable logic device technology. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, and product yield enhancement.
- 7/95 to 5/96 **Information Storage Devices, San Jose, California**
Technology Development Manager/Program Manager. Led a project team of 10 in technology development, process integration, and first product introduction, with a new foundry. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, resolution of sorting issues and yield enhancement.

5/92 to 7/95

Advanced Micro Devices, Sunnyvale, California

Member of Technical Staff. Led the development of low-energy/DINOR-type flash EPROM technology. Key individual contributor in optimizing the process and design of flash cell and periphery devices in AMD's 0.5 μ m and 0.35 μ m flash EPROM technologies. Duties included process integration, device modeling, and development of triple-well technology and high-voltage transistors for negative gate erase operation.

1/89 to 4/92

Texas Instruments, Dallas, Texas

Member of Technical Staff. Research and development of 16Mb generation of flash EPROM technology, as well as a new generation of antifuse-based FPGAs. Duties included process integration, device modeling, high-voltage CMOS process integration, and investigation of a novel source-side injection mechanism for EPROM channel hot-electron programming.

AWARDS/HONORS

U.C. Berkeley Certificate of Distinction Award, 1983

AEA Faculty Development Fellowship, 1983-1985

AMD Spotlight Award, 1995

PATENTS

1. U.S. Patent 5,106,773, "Programmable Gate Array and Methods for Its Fabrication" (with K-L. Chen and H. Tigelaar), issued April 21, 1992.
2. U.S. Patent 5,166,557, "Gate Array with Built-in Programmable Circuitry" (with K.-L. Chen), issued November 24, 1992.
3. U.S. Patent 5,202,576, "Asymmetrical Non-Volatile Memory Cell, Arrays, and Methods for Fabricating the Same" (with M. Wong), issued April 13, 1993.
4. U.S. Patent 5,219,782, "Sublithographic Antifuse and method for Manufacturing" (with K.-L. Chen), issued June 15, 1993.
5. U.S. Patent 5,250,464, "Method of Making a Low Capacitance, Low Resistance Sidewall Antifuse Structure" (with M. Wong), issued October 5, 1993.
6. U.S. Patent 5,264,384, "Method of Making a Non-Volatile Memory Cell" (with C. Kaya), issued November 23, 1993.
7. U.S. Patent 5,300,803, "Source Side Injection Non-volatile Memory Cell," issued April 5, 1994.
8. U.S. Patent 5,365,105, "Sidewall Antifuse Structure and Method for Making," issued November 15, 1994.
9. U.S. Patent 5,371,402, "Low Capacitance, Low Resistance Sidewall Antifuse Structure and Process" (with M. Wong), issued December, 1994
10. U.S. Patent 5,395,797, "Antifuse Structure and Method of Fabrication," issued March 7, 1995.
11. U.S. Patent 5,470,773, "Method of Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch" (with Y. Sun and C. Chang), issued November 28, 1995.
12. U.S. Patent 5,482,880, "Non-Volatile Memory and Fabrication Method," (with C. Kaya), issued January 9 1996.
13. U.S. Patent 5,517,443, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued May 14, 1996.
14. U.S. Patent 5,521,867, "Adjustable Threshold Voltage Conversion Circuit" (with Jian Chen), issued May 28, 1996.
15. U.S. Patent 5,534,455, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued July 9, 1996.
16. U.S. Patent 5,541,875, "High Energy Buried Layer Implant To Provide A Low Resistance P-Well in A Flash EPROM Array" (with Jian Chen), issued May 28, 1996.
17. U.S. Patent 5,590,076, "Channel Hot-Carrier Page Write," issued December 31, 1996.

18. U.S. Patent 5,596,531, "Method for Decreasing the Discharge Time of A Flash Memory Cell," issued January 21, 1997.
19. U.S. Patent 5,612,914, "Asymmetrical Non-volatile Memory Cell, Arrays and Methods for Fabricating Same" (with Man Wong), issued May 18, 1997.
20. U.S. Patent 5,624,859, "Method for Providing Device Isolation and Off-State Leakage Current for a Semiconductor Device," issued April 29, 1997.
21. U.S. Patent 5,625,220, "Sublithographic Antifuse," (with K.L. Chen), issued April 29, 1997.
22. U.S. Patent 5,646,430, "Non-volatile Memory Cell Having Lightly-Doped Source Region" (with C. Kaya), Issued July 8, 1997.
23. U.S. Patent 5,650,964, "Method of Inhibiting Degradation of Ultra Short Channel Charge-carrying Devices during Discharge," (with Jian Chen), Issued July 22, 1997.
24. U.S. Patent 5,652,155, "Method for Making Semiconductor circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued July 27, 1997.
25. U.S. Patent 5,656,509, "Method and Test Structure for Determining Gouging in a Flash EPROM Cell During SAS Etch," Issued July 29, 1997
26. U.S. Patent 5,661,059, "Boron Penetration to Suppress Short Channel Effect in P-channel Device," Issued August 26, 1997.
27. U.S. Patent 5,674,764, "Method of Making Asymmetrical Non-volatile Memory Cell," Issued October 7, 1997.
28. U.S. Patent 5,693,972, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self-Aligned Source (SAS) Etch in a Semiconductor Device," Issued December 2, 1997.
29. U.S. Patent 5,751,631, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued May 12, 1998
30. U.S. Patent 5,789,295, "Method of Eliminating or Reducing Poly1 Oxidation at Stacked Gate Edge in Flash EPROM Process," Issued August 4, 1998.
31. U.S. Patent 5,814,854, "Highly scalable FLASH EEPROM cell," Issued September 29, 1998.
32. U.S. Patent 5,814,864, "Semiconductor Circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued September 29, 1998.
33. U.S. Patent 5,912,836, "Circuit for Detecting Both Charge Gain and Charge Loss Properties in a Non-Volatile Memory Array," Issued June 15, 1999.
34. U.S. Patent 5,930,174, "Circuit and Method for Erasing Flash Memory Array," Issued July 27, 1999.
35. U.S. Patent 5,981,994, "Method and Semiconductor circuit for Maintaining Integrity of Field Threshold Voltage Requirements," Issued November 9, 1999.

36. U.S. Patent 5,995,418, "Circuit and Method for Erasing Flash Memory Array," Issued November 30, 1999.
37. U.S. Patent 6,026,017, "Compact nonvolatile memory," Issued February 15, 2000.
38. U.S. Patent 6,027,974, "Nonvolatile memory," Issued February 22, 2000.
39. U.S. Patent 6,088,263, "Non-volatile memory using substrate electrons," Issued July 11, 2000.
40. U.S. Patent 6,091,636, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued July 18, 2000.
41. U.S. Patent 6,127,225, "Memory cell having implanted region formed between select and sense transistors," Issued October 3, 2000.
42. U.S. Patent 6,159,800, "Method of forming memory cell," Issued December 12, 2000.
43. U.S. Patent 6,188,604, "Flash memory cell & array with improved pre-program and erase characteristics," Issued February 13, 2001.
44. U.S. Patent 6,185,133, "Flash EPROM using junction hot hole injection for erase," Issued February 6, 2001.
45. U.S. Patent 6,252,799, "Device with embedded Flash and EERPOM memories," Issued June 26, 2001.
46. U.S. Patent 6,326,265, "Device with Embedded Flash and EPROM Memories," Issued December 4, 2001.
47. U.S. Patent 6,417,550, "High voltage MOS devices with high gated-diode breakdown voltage and punch-through voltage," Issued July 9, 2002.
48. U.S. Patent 6,479,862, "Charge trapping device and method for implementing a transistor having a negative differential resistance mode," Issued November 12, 2002.
49. U.S. Patent 6,512,274, "CMOS-process compatible, tunable NDR (negative differential resistance) device and method of operating same," Issued January 28, 2003.
50. U.S. Patent 6,596,617, "CMOS compatible process for making a tunable negative differential resistance (NDR) device," Issued July 22, 2003.
51. U.S. Patent 6,624,026, "Nonvolatile Memory," Issued September 23, 2003.
52. U.S. Patent 6,680,245, "Method for making both a negative differential resistance (NDR) device and a non-NDR device using a common MOS process," Issued January 20, 2004.
53. U.S. Patent 6,686,631, "Negative differential resistance (NDR) device and method of operating same," Issued February 3, 2004.
54. U.S. Patent 6,693,027, "Method for configuring a device to include a negative differential resistance (NDR) characteristic," Issued February 17, 2004.
55. U.S. Patent 6,700,155, "Charge trapping device and method for implementing a transistor having a configurable threshold," Issued March 2, 2004.

56. U.S. Patent 6,711,063, "EEPROM memory cell array architecture for substantially eliminating leakage," Issued March 23, 2004.
57. U.S. Patent 6,835,979, "Nonvolatile Memory," Issued December 28, 2004.
58. U.S. Patent 6,969,894, "Variable threshold semiconductor device and method of operating same," Issued November 29, 2005.
59. U.S. Patent 6,972,234, "High Voltage MOS Devices with High Gated-Diode Breakdown Voltage and Punch-through Voltage," Issued December 6, 2005.
60. U.S. Patent 6,972,465, "CMOS process compatible, tunable negative differential resistance (NDR) device and method of operating same," Issued December 6, 2005.
61. U.S. Patent 7,067,873, "Charge Trapping Device," Issued June 27, 2006.
62. U.S. Patent 7,091,077, "Method of directionally trimming polysilicon width," Issued August 15, 2006.
63. U.S. Patent 7,109,078, "CMOS compatible process for making a charge trapping device," Issued September 19, 2006.
64. U.S. Patent 7,301,194, "Shrinkable and highly coupled double poly EEPROM with Inverter," Issued November 27, 2007.
65. U.S. Patent 7,436,710, "EEPROM memory device with cell having NMOS in a P pocket as a control gate, PMOS program/erase transistor, and PMOS access transistor in a common well," Issued October 14, 2008.
66. U.S. Patent 7,535,758, "One or Multiple-Times Programming Device," Issued May 19, 2009.
67. U.S. Patent 7,782,668, "Integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 24, 2010.
68. U.S. Patent 7,787,295, "Integrated circuit embedded with Non-volatile Multiple-Time Programmable memory having variable coupling," Issued August 31, 2010.
69. U.S. Patent 7,787,304, "Method of making integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 31, 2010.
70. U.S. Patent 7,787,309, "Method of operating integrated circuit embedded with Non-volatile One-Time Programmable and Multiple-Time Programmable memory," Issued August 31, 2010.
71. U.S. Patent 7,791,955, "Method of erasing a block of memory cells," Issued September 7, 2010.
72. U.S. Patent 7,835,184, "EEPROM memory cell with first-dopant-type control gate transistor, and second-dopant type program/erase and access transistors formed in common well," Issued November 16, 2010.
73. U.S. Patent 7,835,186, "Method of programming a selected memory cell," Issued November 16, 2010.

74. U.S. Patent 7,852,672, "Integrated Circuit embedded with Non-Volatile programmable memory having variable coupling," Issued December 14, 2010
75. U.S. Patent 7,876,615, "Method of operating integrated circuit embedded with Non-Volatile programmable memory having variable coupling related application data," Issued January 25, 2011
76. U.S. Patent 7,920,426, "Non-volatile memory programmable through areal capacitive coupling," Issued April 5, 2011
77. U.S. Patent 7,944,750, "Multi-programmable Non-Volatile Memory Cell," Issued May 17, 2011
78. U.S. Patent 8,203,861, "Non-Volatile One-Time Programmable and Multiple-Time Programmable Device," Issued June 19, 2012
79. U.S. Patent 8,208,299, "Integrated Circuit Embedded with Non-Volatile Programmable Memory Having Variable Coupling and Separate Read/Write Paths," Issued June 26, 2012
80. U.S. Patent 8,300,470, "Two Terminal Programmable Hot Channel Electron Non-Volatile Memory," Issued October 30, 2012
81. U.S. Patent 8,305,805, "Common Drain Non-Volatile Multiple-Time Programmable Memory," Issued November 6, 2012
82. U.S. Patent 8,325,519, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Ratio," Issued December 4, 2012.
83. U.S. Patent 8,580,622, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued November 12, 2013.
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86. U.S. Patent 8,705,263, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued April 22, 2014.
87. U.S. Patent 8,988,103, "Capacitively Coupled Logic Gate," Issued March 24, 2015.
88. U.S. Patent 9,064,192, "Automatic Valid Vote Count Storage using Secure Embedded Non-Volatile Memory," Issued June 23, 2015.
89. U.S. Patent 9,224,739, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued December 29, 2015.
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91. U.S. Patent 9,324,438, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued April 26, 2016.
92. U.S. Patent 9,558,813, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued January 31, 2017.
93. U.S. Patent 9,570,161, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.
94. U.S. Patent 9,570,175, "Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.
95. U.S. Patent 10,061,738, "Ephemeral Peripheral Device," Issued August 28, 2018.
96. U.S. Patent 10,115,467, "One time Accessible (OTA) Non-Volatile Memory," Issued October 30, 2018.
97. U.S. Patent 10,198,889, "Automatic Valid Vote Count Storage Using Secure Embedded Non-Volatile Memory," Issued February 5, 2019
98. U.S. Patent 10,559,700, "Zero Cost ANVM Cell Using High Voltage Devices in Analog Process," Issued February 11, 2020.
99. U.S. Patent 10,629,607, "Semiconductor CMOS Non-Volatile Memory Device," Issued April 21, 2020

(additional patent applications pending)

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EXHIBIT B

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

**FORCE MOS TECHNOLOGY, CO.,
LTD.,**

Plaintiff,

v.

ASUSTEK COMPUTER, INC.,

Defendant.

**Civil Action No. 2:22-cv-00460-JRG
JURY TRIAL DEMANDED**

MATERIALS CONSIDERED

PATENTS AND FILE HISTORIES	
U.S. Patent No. 7,629,634 (the “’634 Patent”)	FORCE-MOS0000001-14
U.S. Patent No. 7,847,346 (the “’346 Patent”)	FORCE-MOS0000015-26
U.S. Patent 7,812,409 (the “’409 Patent”)	FORCE-MOS0000027-38
File History for the ’634 Patent	FORCE-MOS0000039-124
File History for the ’346 Patent	FORCE-MOS0000125-226
File History for the ’409 Patent	FORCE-MOS0000227-494
U.S. Patent No. 6,621,107	
U.S. Patent No. 5,629,543	

PLEADINGS
Defendant’s List of Proposed Terms and Claim Elements for Construction Under Local Patent Rule 4-1
Defendant’s Preliminary Proposed Constructions of Claim Terms and Extrinsic Evidence Under Local Patent Rule 4-2
Defendant’s Preliminary Identification of Intrinsic and Rebuttal Extrinsic Evidence
Plaintiff’s Rule 4-1 Proposed Terms for Construction
Plaintiff’s Rule 4-2 Exchange of Preliminary Claim Constructions
Plaintiff’s Initial Disclosure of Intrinsic and Extrinsic Evidence for Inclusion in P.R. 4-3 Claim Construction Chart
Plaintiff’s Disclosure of Asserted Claims and Infringement Contentions, including accompanying claim charts for the ’634, ’346, and ’409 Patents
Petition for <i>Inter Partes</i> Review of the ’634 Patent (IPR2024-0093) and exhibits
Petition for <i>Inter Partes</i> Review of the ’409 Patent (IPR2024-0094) and exhibits
The Parties’ Claim Construction Briefing, Exhibits, and Declarations in <i>Alpha and Omega Semiconductor Ltd. & Alpha and Omega Semiconductor Inc. v. Force MOS Tech. Co., Ltd.</i> , No. 5:22-cv-05448-PCP (N.D. Cal.) (Dkts. 73, 74, 79, 80, 81, 82)

PRODUCTION DOCUMENTS		
ASUS_CC_000001	ASUS_CC_000006	ASUS_CC_000013
ASUS_CC_000022	ASUS_CC_000030	ASUS_CC_000034
ASUS_CC_000041	ASUS_CC_000046	FORCE-MOS0017070
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FORCE-MOS0017114	FORCE-MOS0017120	FORCE-MOS0017129
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FORCE-MOS0017736	FORCE-MOS0019324	FORCE-MOS0019344
FORCE-MOS0019355	FORCE-MOS0019362	FORCE-MOS0019368
FORCE-MOS0019384	FORCE-MOS0019402	FORCE-MOS0019414
FORCE-MOS0019421	FORCE-MOS0020231	FORCE-MOS0020270
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FORCE-MOS0020665	FORCE-MOS0020680	