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Semiconductor Power Devices

Physics, Characteristics, Reliability
Second Edition



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Chapter 9

MOS Transistors and Field Controlled Wide Bandgap Devices

9.1 Function Principle of the MOSFET

The MOSFET basic structure was investigated early [Hof63]. For the comprehension of the function of a MOSFET (Metal Oxide Semiconductor Field Effect Transistor), the surface of the semiconductor may be examined at first. The surface of a semiconductor is always a disturbance of the ideal lattice due to the lack of neighboring atoms. Therefore, a thin oxide will always be built up on the surface or other atoms and molecules are adsorbed. Thus, these surface layers are normally electrically charged.

A p-type semiconductor may be given as an example. Assumed is a positive charge on the surface (Fig. 9.1).

For a small positive charge we obtain

$$|qV_S| < E_i - E_F:$$

The hole-concentration/density on the surface is being reduced. The conduction band and the valence band are bent downwards. A depletion zone of the thickness h_d is built up.

A higher positive charge yields

$$|qV_S| > E_i - E_F:$$

In this case, the conduction and valence band are bent even stronger. In a small region at the surface the Fermi level is now closer to the conduction band than to the valence band. An inversion layer of the thickness h_i is being formed, in which electrons are the majority charge carriers.

Next to this is the depletion layer with the thickness h_d , which separates the inversion layer from the p-type area.

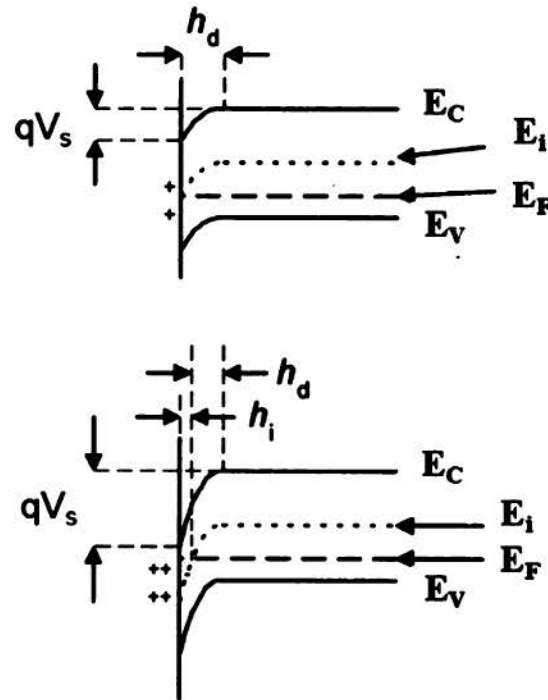


Fig. 9.1 Semiconductor surface. p-type semiconductor, positive charge on the surface

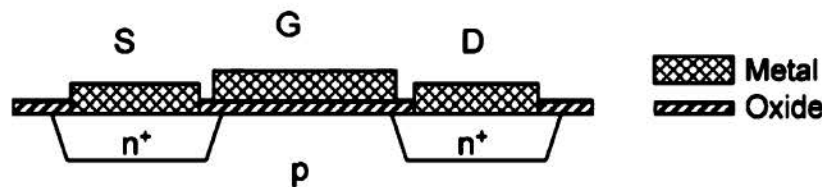


Fig. 9.2 Lateral n-channel MOSFET. Description: *S* Source, *G* Gate, *D* Drain

Having a negative charge on the p-type semiconductor, an accumulation layer of holes will be formed. The n-type semiconductor behaves similarly: With a positive charge at the surface, the accumulation layer is formed, with a negative surface charge a depletion zone is formed, with an increased negative charge the inversion layer.

Next, we assume a thin oxide film on the p-type semiconductor and apply a metallization on it. On this metal film a positive voltage is applied. Furthermore, two n⁺-areas are added and bonded as source and drain region. We have the simplest case of a lateral MOS field effect transistor shown in Fig. 9.2 [Hof63].

A positive voltage has the same effect as the positive surface charge: When a sufficient positive voltage at the gate is applied, both n-areas are connected by the inversion layer. Due to the gate voltage $V_G > V_T$ a current can flow between the drain and the source.

Gate-Source Threshold-Voltage V_T (n-channel-MOSFET):

The threshold voltage is the gate voltage, at which the generated electron concentration equals the concentration of the acceptors.

It has to be distinguished:

n-channel MOSFET: An n-type channel is formed in a p-area.

p-channel MOSFET: A p-type channel is formed in a n-area.

On closer inspection, it has to be considered that the oxide contains positive charges on the boundary surface to the semiconductor. These charges are in the order of 5×10^9 to $1 \times 10^{11} \text{ cm}^{-2}$. Moreover, the gate area of power-MOSFETs consists of a heavily n-doped poly silicon layer (see Figs. 9.4 and 9.5) and a potential difference already exists between gate and semiconductor due to the differing positions of the Fermi level in the n^+ -doped poly silicon and in the p-type semiconductor (concerning the n-channel MOSFET). Both effects function in the same way as an external positive gate-voltage and result in a reduction of the threshold voltage V_T . In case of a low doping of the p-area and a high oxide charge of the n-channel MOSFET, V_T is negative, even without gate voltage a channel exists. The definition of the threshold voltage mentioned above remains valid.

It has to be distinguished:

Depletion type: $V_T < 0$. The device is normally on and does not block before a negative gate-source-voltage $V_G < V_T$ is applied.

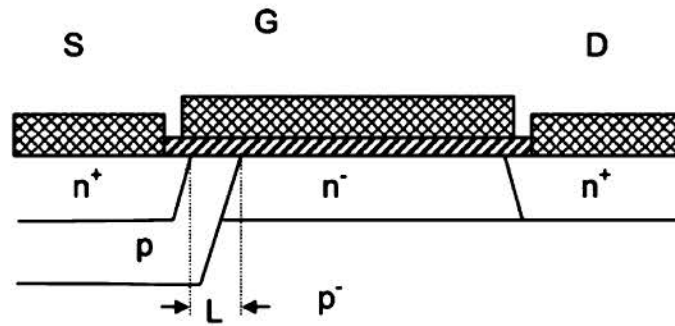
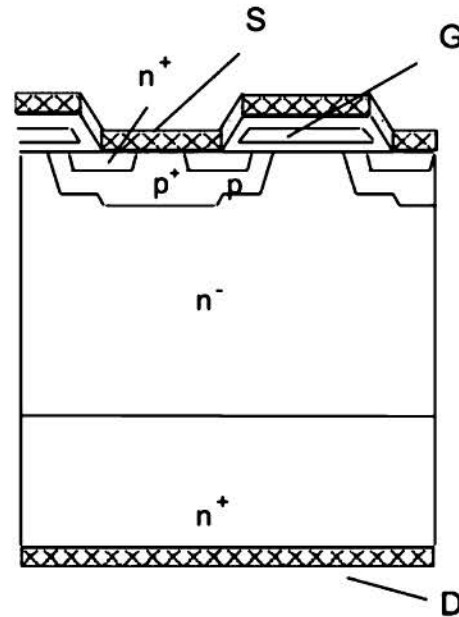
Enhancement type: $V_T > 0$. An n-channel only develops when $V_G > V_T$ (normally off device).

Usually, MOSFETs of the enhancement type are used in power electronics, because of the normally-off feature that is required in voltage source converters. Almost always n-channel MOSFETs are used, being more advantageous since the mobility of the electrons is much higher than that of the holes (see Chap. 2). Typically, the threshold voltage of modern devices is adjusted between 2 and 4 V.

9.2 Structure of Power MOSFETs

The configuration shown in Fig. 9.2 will sustain little drain-source voltage. Thus, a structure such as in Fig. 9.3, which is named DMOS (D = double diffused), is used from 10 V upwards. The lowly doped n^- -area, the drain extension area, takes over the blocking voltage.

Lateral DMOS transistors are frequently used in power ICs and in monolithic integrated power semiconductor-circuits ("smart power"). But they have the disadvantage of having a low current-load capacity, because the n^- -area consumes a large part of the surface of the semiconductor. If real "power" has to be controlled, a

Fig. 9.3 Lateral DMOS**Fig. 9.4** Vertical DMOS transistor. The gate electrode is poly-silicon

vertical MOSFET is realized by arranging the area for the space charge vertically [Lid79], see Fig. 9.4. Consequently, the volume of the semiconductor is utilized and the surface can be used for the formation of the gate-source cell structure.

On the surface of the semiconductor the individual cells are formed, which consist of p-wells and n⁺-source areas. A cross section of a cell can be seen in Fig. 9.4. The p-well is connected to the source metallization, so that the parasitic npn-transistor is shorted. In order that the short has very little resistance, the doping is increased at this spot by an additional p⁺-implantation, followed by a diffusion step. At the edges of the well is the channel, which is covered with the thin gate oxide. Above the oxide the gate electrode is applied, usually consisting of a heavily doped n⁺ poly-silicon. At one spot, mostly in the center of the chip, the gate electrode is brought to the surface to form a gate pad to which a bond wire can be attached.

Because the current has to flow through the inversion channel, many single cells are formed to gain a larger width of the channel. An example is given in Fig. 9.5. Here, the cells are of square form and arranged in a square pattern. The

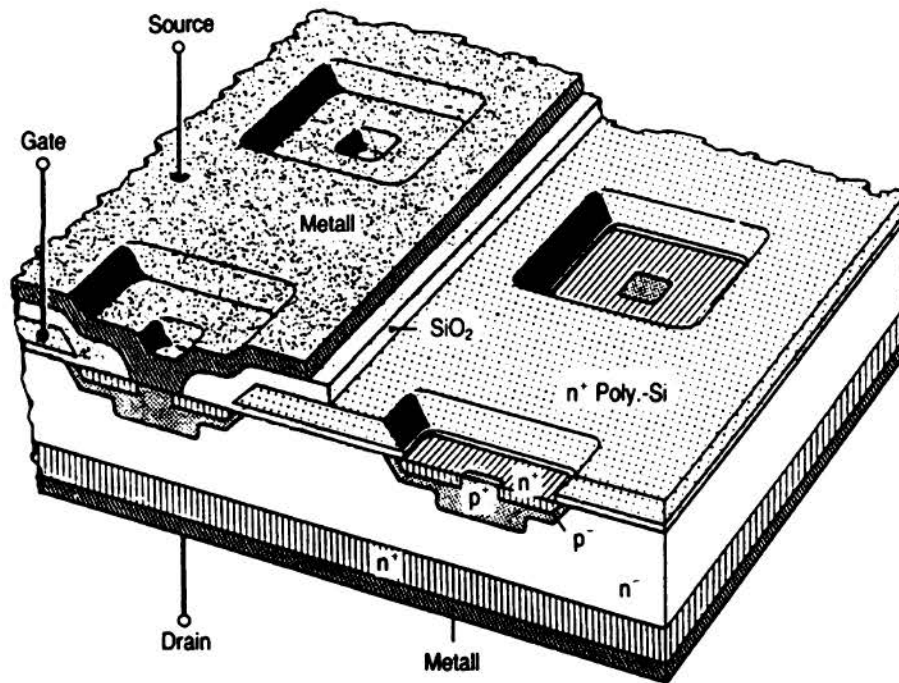
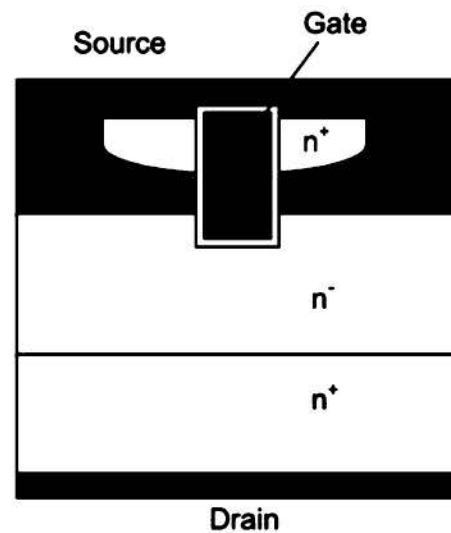


Fig. 9.5 Cell structure of a vertical DMOS. From [Ste92]

Fig. 9.6 Vertical trench-MOSFET



semiconductor surface area is used even more effectively with a hexagonal pattern, where the single cells are hexagonal, the so-called HEXFET structure [Col79].

The vertical DMOS (also called VDMOS) transistors are used in a wide field of applications, such as computer and electronic equipment power supplies with power factor correction front ends. Since the second half of the 1990s, with the introduction of the trench-MOS [Sod99] a further improvement has been made, in which the channel area is vertically arranged (Fig. 9.6). Due to this, a much smaller on-state resistance can be gained especially in the lower voltage range < 100 V.

9.3 Current-Voltage Characteristic of MOS-Transistors

Figure 9.7 shows the current-voltage characteristics of the MOSFET. The device is in the blocking state as long as a positive voltage V_D between drain and source is given and V_G is smaller than the threshold voltage V_T . The blocking voltage of the MOSFET is limited by the avalanche breakdown. Because the npn-transistor is suspended by a low resistance short, the blocking voltage of the MOSFET corresponds to the blocking voltage of the diode, which is formed by the p-well, the low doped base region and the n^+ -layer.

A current carrying channel is built for $V_G > V_T$, resulting in the given current-voltage characteristics. Similar to the current gain of bipolar transistors a transconductance is defined here. For low voltages V_D , the current-voltage characteristics have the form of a straight line. For a defined gate voltage V_G the resistance $R_{DS(on)} (= R_{on})$ is indicated.

The transition between the ohmic region and the pinch-off region is called the quasi saturation. This region is described by a parabolic curve.

In the reverse direction of the MOSFET a forward biased diode is present. As for a power diode, this diode forward characteristic is often approximated by a threshold voltage V_{F0} and a differential resistance.

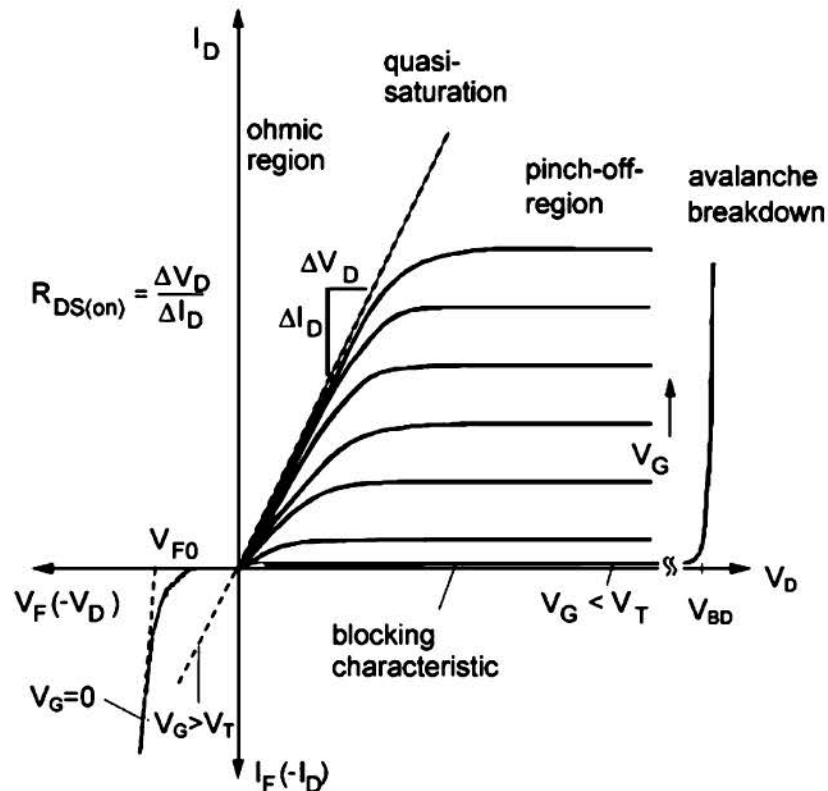


Fig. 9.7 Current-voltage characteristic of the MOSFET. Figure adapted from [Nic00]