

CONTACT RESISTANCE AND METHODS FOR ITS DETERMINATION

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The problem of low resistance ohmic contacts to silicon has been of considerable technological interest. In recent years this problem has received special attention owing to the effect of scaling in very-large-scale integration (VLSI) technology. The field of ohmic contacts to semiconductors comprises two independent parts. First there exists the material science aspect. The choice of a suitable metallization system, the proper semiconductor parameters and the method of the contact formation is not obvious. Then there is the question of the proper definition of the contact resistance and the way it is measured.

Several methods for contact resistance determination have been introduced in the past. All seem to have some drawbacks that either limit their usefulness or raise doubts as to their validity in certain situations. We shall discuss the two-, three- and four-terminal resistor methods of measurement. Relevant theoretical considerations will also be included.

For conventional integrated circuits with a moderate junction depth of 1–2 μm , aluminum is uniquely suited as a single-element metallization system. However, for VLSI applications it may become obsolete because of several well-defined metallurgical problems. Thus, other metallization systems have to be investigated. We shall briefly discuss some recent data on several other metallization systems. Finally, the problem of size effects on the contact resistance will be discussed. Recent experimental results suggest important clues regarding the development of alternative metallization systems for VLSI circuits and also point to revisions of estimates of achievable design rules.

1. INTRODUCTION

The trend in recent years toward very-large-scale integration (VLSI) has created a genuine need for new metallization systems and for reliable methods of measuring the contact resistance between the semiconductor material and the contacting metallization. This need results from the ever smaller contact area

available for carrier transport. A preferred metallization agent is metallurgically and electrically stable and is able to withstand moderately high temperature treatments. The latter are particularly experienced during interlevel dielectric deposition when a multilevel metallization scheme is used. The shrinking of device dimensions results in an increase in the contact resistance. Hence, the metallization candidate is also required to yield lower values of contact resistance. A well-defined method for contact resistance measurement is thus required in order to establish unambiguous values for this important parameter.

Owing to the many different methods that have been used over the years for measuring and analyzing the contact resistance, there exists some confusion as to the exact meaning of such terms as contact, contact resistance, specific contact resistance etc. The interest has always been in the contributions to the resistance whose origin is in the interface between the semiconductor and the metal. However, parasitic contributions from the semiconductor material seem always to have been included in the measurements. Such contributions are due to the current bending underneath the interface, current crowding at the entrance to the contact, and the spreading resistance. Theoretical calculations were, naturally, well defined in this respect and aimed at evaluating the interface resistance. This, however, could not be directly compared with the measured quantities. Nevertheless, implicit and explicit attempts to compare experimental and theoretical results have resulted in ambiguous definitions for some relevant terms. It is, therefore, of the utmost importance to define clearly all the relevant terms and thus to create a common basis for future discussions.

Yet another factor complicating matters is the state of the semiconductor surface at the time of the metal deposition. The surface is seldom expected to be absolutely clean of foreign contaminants and free of structural defects. For example, silicon surfaces are known to be always covered with a thin layer of SiO_2 known as the native oxide. Needless to say, such an insulating layer if present at the metal-silicon interface would certainly affect the interface resistance. Likewise, ion implantation damage to the surface, dislocations, impurities etc. are expected to influence the experimentally determined quantities. This very important factor has not always been given appropriate weight in discussing contact resistance results. Even more serious is the fact that many attempts have been made to compare theoretical and experimental results while ignoring this influencing factor. Conclusions thus obtained are sometimes difficult to justify.

In the present work the contact or contact region is meant to include the semiconductor junction and the metal overlayer, in addition to the interface between the two. The physical dimensions of the junction and metal regions considered as part of the contact region are understood to be determined by the contact window size and the depth and thickness of these two elements respectively. The term contact resistance then stands for the composite contributions originating at the interface and in the material underneath it. We shall neglect the relatively small contribution to the contact resistance which is due to the metal or alloy of metals. When the potential drop V across the contact region is essentially linear with respect to the current I the contact resistance $R_c = V/I$ is said to be ohmic. The product of the measured contact resistance and the contact area A , say, is customarily referred to as the specific contact resistance ρ_c .

This point is the cause of much confusion and hence deserves special attention. The quantity ρ_c defined above has a theoretical counterpart given by

$$\rho_1 \equiv \left(\frac{\partial J}{\partial V} \right)_{V=0}^{-1} \quad (1)$$

where J denotes the current density. The theoretical quantity, however, deals with the *interface* resistance and therefore should more properly be called the *specific interface resistance*. We labeled it ρ_1 so as to differentiate it from either ρ_c or R_c . Clearly, ρ_1 is independent of the actual contact area. On the basis of this property of ρ_1 a quadratic scaling rule has been postulated for the contact resistance²⁻⁴. This, of course, should not be the case for ρ_c as it is derived from R_c which has included in it various parasitic contributions in addition to the interface resistance. Indeed, as we shall discuss later, ρ_c is found to be a non-constant function of the contact window width W . To summarize, one always measures the contact resistance R_c from which the specific contact resistance ρ_c may be obtained. The latter quantity should not be compared with the theoretically derived specific interface resistance ρ_1 unless all parasitic contributions are first accounted for. These also depend on the particular method of the contact resistance measurement as will be discussed in what follows.

Several methods have been proposed for measuring the contact resistance in metal-semiconductor systems. It seems, however, that only three of the available methods are sufficiently different from each other to warrant a special discussion. The three different methods may be referred to as the two-, three- and four-terminal resistor structures. None of these seems to be truly capable of directly probing ρ_1 . Therefore, a clear knowledge of what is being measured by each method is required. We shall discuss in some detail these three methods and also mention other related structures that were apparently devised to improve on these. Some necessary theoretical considerations pertaining to the data analysis will be included too.

In the present paper we shall confine the discussion of experimental studies to contacts made to silicon substrates. To date, the most common metallization system to silicon employs aluminum or one of its alloys. These, however, may become obsolete for VLSI applications because of various problems that will be mentioned later. Other metallization systems envisaged for use in VLSI technology include metal silicides and refractory metals. In the first group platinum silicide has acquired special importance, presumably owing to its wide use in fabricating Schottky barrier devices. We shall discuss contacts to silicon made with platinum silicide as contact material and utilizing other metal combinations as an overlayer for interconnections.

With the advent of VLSI technology, the need has arisen for more sophisticated metallization systems. These include two- and even three-level metallization schemes. This situation has created a demand for a first-level metallization candidate that would be capable of withstanding higher processing temperatures than those common in LSI technology where aluminum is by far the principal metallization agent. Thus, various refractory metals have been considered in recent years for this purpose. Among these, molybdenum seems to possess most of the required characteristics. We shall, therefore, briefly discuss the use of molybdenum as a direct contact material and also in combination with platinum silicide.

The plan of the present paper is as follows. In Section 2 we shall give some

introductory remarks regarding the interface and the transport mechanisms across the interface. In Section 3 the three basic methods of contact resistance measurement will be presented along with some relevant theoretical discussions pertaining to the proper analysis of the experimental data. In Section 4 we shall briefly discuss some recently obtained experimental data including some new results. The contact size effect will be discussed in Section 5, and Section 6 will include a summary of the main points raised in this presentation.

2. RESISTANCE AND CARRIER TRANSPORT ACROSS THE INTERFACE

An ideal metal-to-semiconductor contact may be defined as one which allows charge carriers to flow in either direction without presenting any resistance at the interface. In reality, however, a potential barrier always develops at the interface. This presents an impediment to the current through the interface and also determines whether the contact is ohmic in character or else rectifying.

In order to make this presentation self-contained, it will be beneficial to consider some of the basic physics of metal-to-semiconductor contacts. A schematic illustration of the situation is given in Fig. 1 for the case of an n-type semiconductor (similar arguments apply to a p-type semiconductor). In the Schottky theory of barrier formation^{5,6} the barrier height ϕ_{Bn} (n stands for n-type) is given by

$$\phi_{Bn} = \phi_M - X_s \quad (2)$$

where ϕ_M is the metal work function and X_s is the electron affinity of the semiconductor. The magnitude of ϕ_{Bn} usually determines whether a given contact is rectifying or ohmic. For a metal contact to an n-type semiconductor to be ohmic, it is required that $\phi_M < \phi_s$, where ϕ_s is the semiconductor work function defined as $X_s + E_c - E_F$ with E_c denoting the conduction band energy level and E_F the Fermi level. In the above notation $\phi_M - \phi_s$ is the barrier for the flow of electrons from the semiconductor to the metal while $\phi_M - X_s$ is the barrier for the reverse flow of electrons from the metal to the semiconductor. To a first approximation, ϕ_{Bn} is constant for a given metal-semiconductor system, and it is unaffected by an applied voltage and moderate changes in the doping level of a lightly doped semiconductor.

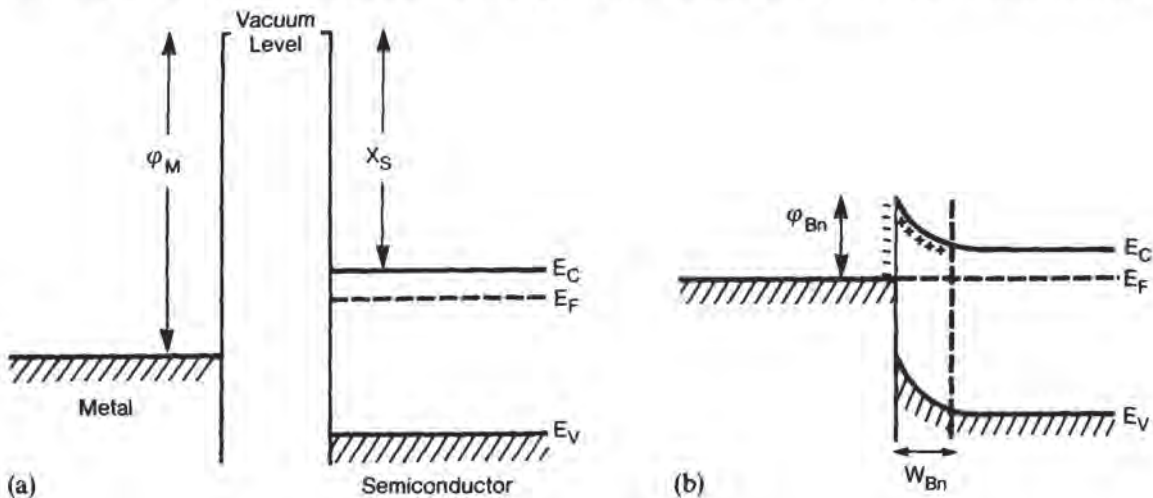


Fig. 1. An illustration of the metal-semiconductor (n type) interface (a) before and (b) after contact formation.

In cases where ϕ_{Bn} is relatively small, a nearly linear current–voltage relation develops indicating that the flow of carriers across the interface proceeds with equal ease in both directions. In such cases of ohmic behavior ϕ_{Bn} may even turn out to be a negative quantity. When this happens a dipole surface charge barrier is then the impediment to current through the interface. Thus, in all practical cases formation of a Schottky barrier is inevitable. The object of contact resistance studies is to devise means for minimizing the effects of the barrier on carrier transport through the interface. To this end a good theoretical understanding of both the barrier effects and the possible transport mechanisms is essential.

The first studies of current transport phenomena through metal–semiconductor interfaces are usually regarded to be those of Schottky⁵ and Mott⁷. Several possible conduction mechanisms have been proposed to describe the current through the metal–semiconductor barrier. These include the diffusion model^{5,6}, thermionic emission over the barrier⁸ and a combination of these two models^{9,10}. Most ohmic contacts to semiconductors, however, utilize conduction mechanisms other than emission over the barrier because for most metal–semiconductor pairs the barrier heights are too great. Depending on the dopant density and the temperature of application, two more conduction mechanisms can exist. These are the field emission^{11,12} (better known as the tunneling mechanism) and the thermionic–field emission mechanisms¹³. Both these mechanisms depend on narrowing of the barrier width W_{Bn} shown in Fig. 1(b).

The barrier width narrowing is achieved by increasing the dopant density underneath the interface. A higher doping level results in a thinner insulating space charge region beneath the interface whose width (*i.e.* the barrier width) for the case of n-type doping is given by

$$W_{Bn} = \left\{ \frac{2\varepsilon}{qN_D} \left(V_{bi} - \frac{k_B T}{q} \right) \right\}^{1/2} \quad (3)$$

Here $\varepsilon = \varepsilon_r \varepsilon_0$ is the semiconductor permittivity, q is the electronic charge, N_D is the donor density, k_B is the Boltzmann constant, T is the absolute temperature and V_{bi} is the built-in potential defined by

$$V_{bi} = \phi_{Bn} - (E_c - E_F) \quad (4)$$

which is the barrier height seen by the electrons of the conduction band. As is given by eqn. (3), the barrier width is inversely proportional to the square root of the doping density. Thus an increase in the latter will result in a thinner barrier through which electrons can more easily tunnel, even though the barrier height may remain unchanged. A thinner barrier may also be achieved by increasing the temperature. Hence the thermionic–field emission name for the conduction mechanism in cases where the doping density is not too high. For the case of a degenerately doped n-type semiconductor, W_{Bn} becomes so small (of the order of a few lattice spacings) that tunneling through the barrier is the dominant conduction mechanism even at room temperatures.

Tunneling theory is described in many fine works. Among these are the studies of Crowell and Rideout¹³, the work of Stratton¹⁴ and those of Padovani and Stratton¹⁵, Padovani¹⁶ and Chang and Sze¹⁷. The theoretical results in all these studies are similar. The work of Chang and Sze¹⁷, however, has the least number of

simplifying assumptions as it resorted to solving Schrödinger's equation on a computer. Its only disadvantage, perhaps, is that the results cannot be expressed in closed analytical forms. In some limiting cases analytical results were nevertheless obtained¹. The result of Crowell and Rideout¹³ for the general case of a thermionic-field emission conduction mechanism reads

$$I = I_s \left[\exp\left(\frac{qV}{nk_B T}\right) - \exp\left\{\frac{(n^{-1}-1)qV}{k_B T}\right\} \right] \quad (5a)$$

where V is the applied voltage and n is a dimensionless parameter known as the ideality factor. The value of n is usually very close to unity. In eqn. (5a) the saturation current I_s is given by

$$I_s = A^* A T^2 \exp\left(-\frac{\phi_{Bn}}{k_B T}\right) \quad (5b)$$

where A^* is the effective Richardson coefficient which, in general, depends on the crystal orientation. Chang *et al.*¹ obtained an approximate expression for the specific interface resistance (defined by eqn. (1)) for the case when the tunneling process dominates the conduction through the interface. This reads

$$\rho_1 \simeq \frac{1}{E_{00}} \exp\left(\frac{qV_{bi}}{E_{00}}\right) \quad (6a)$$

with E_{00} given by

$$E_{00} = \frac{\hbar}{2} \left(\frac{N_D}{\epsilon m^*} \right)^{1/2} \quad (6b)$$

where $\hbar$ is Planck's constant and m^* is the tunneling effective mass of the electrons. According to this theoretical result, the specific interface resistance should depend strongly on the doping density and the effective mass.

3. METHODS FOR CONTACT RESISTANCE DETERMINATION

Various methods of contact resistance measurement have been proposed and utilized. Generally, there exist three different methods of R_c determination. We name these three sufficiently different methods as the two-, three- and four-terminal resistor structures. Each of these, however, seems to have several versions. Most of them will be briefly mentioned later on. It is important to stress that none of the presently available methods of R_c measurement is capable of directly probing the specific interface resistance. This, as we have discussed, is the quantity that is derived in all the theoretical models. Thus, before a meaningful comparison can be made between experimental and theoretical results, it is necessary to separate the various contributions to the experimental quantity in order to single out that due to the interface. Such an analysis depends on the particular test structure. As we shall discuss in some detail in what follows, many factors may influence the experimental results and make this analysis very difficult. In fact, a successful attempt at such an unambiguous determination of the interface resistance is yet to be made.

3.1. The two-terminal resistor method

The two-terminal resistor method of measurement, of which two of its versions

are depicted in Fig. 2, is probably the simplest of all available methods. Except possibly for attempts to derive the contact resistance from diode characteristics, it seems that the first direct attempts made use of the two-terminal resistor structure.

The two-terminal resistor structure shown in Fig. 2(a) was first discussed by Sullivan and Eigler¹⁸ in the context of a semiconductor contact resistance determination. This structure consists of a homogeneous semiconductor sample with two identical contacts whose area is A . Current that is passed through this element is assumed to be uniformly distributed. Simultaneous measurements of the voltage drop (between points P and Q, say) and the current give the total resistance R_T in a straightforward manner. This quantity includes the interface resistance $R_I (= \rho_I/A)$ due to both interfaces, and in addition it includes the resistance of the bulk material. If the resistivity of the latter is ρ_B and the length is L , then the expression for R_I reads

$$R_I = \frac{1}{2} \left(R_T - \frac{\rho_B L}{A} \right) \quad (7)$$

While this version of the two-terminal resistor method has the virtue of analytical simplicity, it is experimentally highly impractical for structures of small contact area. Berger¹⁹ has discussed a modified structure with coplanar contacts. According to this model, knowledge of the sheet resistance would then enable the determination of R_c (not R_I). Nevertheless, it did not find much use either. As is the case with other similar methods to be discussed later, it also relies on evaluating the difference between two usually large quantities. This often gives relatively large errors which make the determination of small values for either R_I or R_c rather difficult.

A quite different two-terminal resistor structure was introduced by Cox and Strack²⁰ and subsequently used in many studies²¹⁻²⁶ (many other relevant references may be found in ref. 26). The particular arrangement in this structure is shown in Fig. 2(b). In this method an array of metal contacts (usually circular) of different sizes are fabricated on one side of a semiconductor slice of thickness t and resistivity ρ_B , while the other side is wholly metallized to provide a low resistance back-side contact. The total resistance between two suitable points (R and S in Fig.

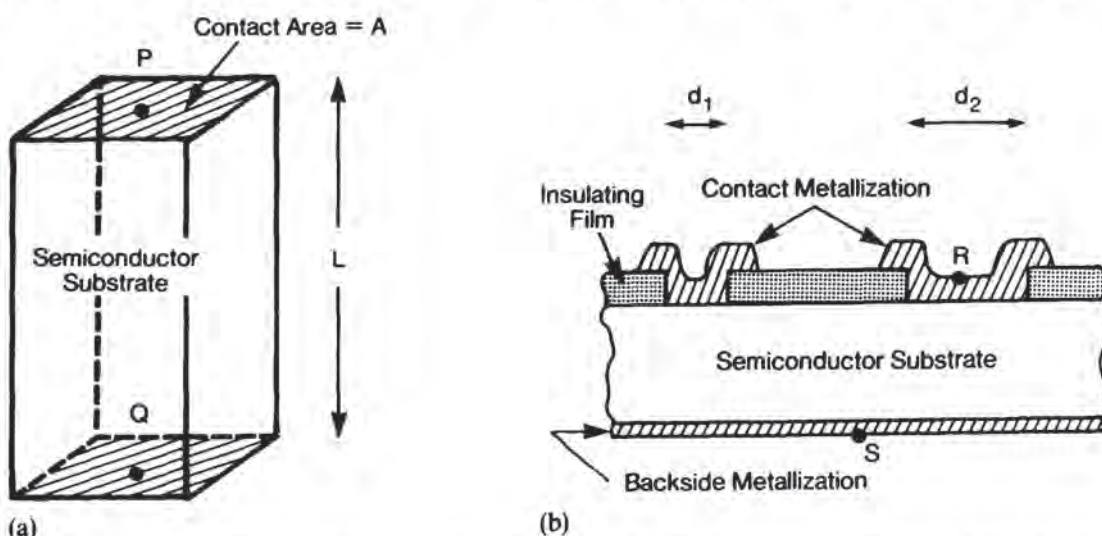


Fig. 2. Two-terminal resistor structures: (a) the simplest such structure; (b) the more realistic structure introduced by Cox and Strack²⁰.

2(b), say) is calculated by Cox and Strack to be

$$R_T = \frac{\rho_B}{\pi d} \tan^{-1} \left(\frac{4t}{d} \right) + R_i + R_o \quad (8)$$

where d is the contact diameter and R_o is a residual resistance due to the back-side contact. Experimental data obtained for several dot sizes should, in principle, suffice to determine the value of the interface resistance R_i by means of a curve fitting procedure. This assumes that the parameters ρ_B and t are known constants and that the diameters are accurately measured. The first term in eqn. (8) describes the contribution due to the spreading resistance and involves a correction factor which accounts for the finite thickness of the substrate. When the values of R_i happen to be small, this correction factor may not be adequate. In such cases a more precise evaluation may be obtained by making use of the integral expression derived by Brooks and Matthes²⁷:

$$R_T = \frac{\rho_B}{2d} \left\{ \int_0^\infty \frac{\sin x}{x} J_1(x) \coth \left(\frac{2xt}{d} \right) dx \right\}^{-1} + R_i + R_o \quad (9)$$

In this equation, $J_1(x)$ denotes the Bessel function of the first order. At the limiting cases when the ratio d/t either goes to zero or becomes very large, eqns. (8) and (9) both give the same values.

As was the case for the simpler two-terminal structure, here too the determination of R_i depends on the difference between large terms. Thus, it is not believed to be an adequate method in cases where ρ_i acquires extremely small values (less than $100 \Omega \mu\text{m}^2$). Also, the method is strictly correct only for a uniformly doped semiconductor. This requirement may pose practical difficulties when attempts are made to study contacts to heavily doped regions as often found in silicon junctions. Moreover, in some cases the surface dopant concentration is affected by metallurgical reactions that take place during contact fabrication. Such is the case with either the arsenic or the phosphorus surface concentration which is found to increase considerably during PtSi formation on a silicon substrate²⁸. When a non-uniform situation exists, such as in a multilayered structure, proper correction factors to the spreading resistance should be employed²⁹. Another complication is due to the fact that the two contacts are different in size. Thus, the stream lines are not expected to be parallel to each other. In such a case, the current will experience some bending and crowding beneath the interface. These effects are not accounted for in eqns. (8) and (9). Therefore, the identification of the R_i term in these equations with the true interface resistance may not be correct.

Two modifications to this version of the two-terminal resistor test structure were discussed by Berger¹⁹ and by Sinha³⁰. In Berger's approach an attempt is made to compare the value of the measured total resistance of the contact under study with that obtained from reference structures for which the R_i value is assumed to be negligible. In his scheme the contacts in the reference structure are identical in all respects with those in the structure being examined except for the fact that contact is made to a heavily doped region in an effort to eliminate the contribution due to the interface resistance. This then limits the usefulness of this method to contacts made to moderately doped semiconductors. Sinha's scheme was devised because of concerns related to parasitic contributions associated with this method of measure-

ment. In his two-terminal structure, the area of the contact in the reference system is made very large so as to minimize both of the contributions due to interface and spreading resistance. Parasitic contributions such as those due to the “probe resistances” are also believed to be eliminated.

Yet another “two-terminal” resistor method is that described by Ting and Chen³¹. In this method a special design is employed to enable sensing of the magnitude of the voltage drop at several locations in the contact region. The contact resistance is then evaluated by a numerical integration of the power dissipation law. Although this method is potentially more accurate than others, it is not practical for the small contact geometries encountered in VLSI technology.

3.2. The three-terminal resistor method

Although termed here the three-terminal resistor method, this method of contact resistance measurement is truly made up of two or more two-terminal “planar” resistors. It was first proposed by Shockley in 1964³² and has since attracted much attention and been used in many contact resistance studies. Two basic versions of this method exist. One version is made of many planar contacts on an implanted semiconductor bar, the various contacts usually being a fixed distance from each other. The total resistance between progressing pairs of contacts is measured and plotted as a function of the pair distance. The resulting function enables the determination of a suitable parameter known as the transfer length, from which the specific contact resistance may be estimated. This version of the three-terminal resistor method is known as the transfer length method (TLM). It has been employed by Yu³³ and discussed in detail by Hower *et al.*³⁴ and has since been widely used. More recent references to this method are those of Braslau²⁶ and Reeves and Harrison³⁵.

The version of the three-terminal resistor method that is depicted in Fig. 3(a) has attracted more theoretical and experimental attention, presumably owing to its simplicity. In this structure, three identical contacts are made to a semiconductor bar fabricated as before by implanting p-type impurities on n-type substrates or vice versa. This situation is devised to minimize non-linear contributions due to current spreading effects. As shown in Fig. 3(a) the three contacts of width W and length d are placed such that the distance $l_1 \neq l_2$. Thus three two-terminal “planar” resistors result (of resistance R_1 and R_2 , as shown in Fig. 3(a), and $R_3 = R_1 + R_2$). Assuming the contact resistance in all three contacts is the same, one may write

$$R_i = R_s \frac{l_i}{W} + 2R_c \quad (10)$$

where $i = 1, 2, 3$ and R_s ($\Omega/\square$) is the sheet resistance of the implanted region beneath the contact. Thus, in principle the value of R_c may be obtained by measuring the total resistance of any two of the three resistors. Solving for R_c , the expression reads

$$R_c = \frac{R_2 l_1 - R_1 l_2}{2(l_1 - l_2)} \quad (11)$$

This is indeed a simple result that promoted the use of this structure.

Much care, however, has to be exercised in analyzing the experimental data. The current in this “planar” device is depicted in Fig. 3(b), where the junction depth

is denoted by t . The current lines are parallel only between the two equipotential surfaces V_1 and V_2 (placed at their extreme locations). According to Kennedy and Murley³⁶, at the entrance to the contact window, a current crowding phenomenon occurs. As we shall see later on, this phenomenon results in a contact size dependence which must be taken into account. In addition, the total contact impedance is again made of several contributions. These include the sheet resistance of the material that is beneath the contact interface, the interface resistance and some interface capacitance. The equivalent circuit is shown in Fig. 3(c). It is thus clear that the values of the resistance as determined from eqn. (11) cannot be directly linked to the interface resistance.

In order to establish such a relation between R_c and R_i (or ρ_i) detailed theoretical investigations were undertaken by Murrmann and Widmann³⁷⁻³⁹, Berger^{40,41} and Chang⁴². The R_c analysis approach in all these studies is that known as the transmission line model. (Although this term strictly refers to the details of the current and voltage drop characteristics in the region of one particular contact as shown in Fig. 3(c), the name, abbreviated as TLM, has been attached to this three-terminal resistor method. Thus some confusion has resulted since, as

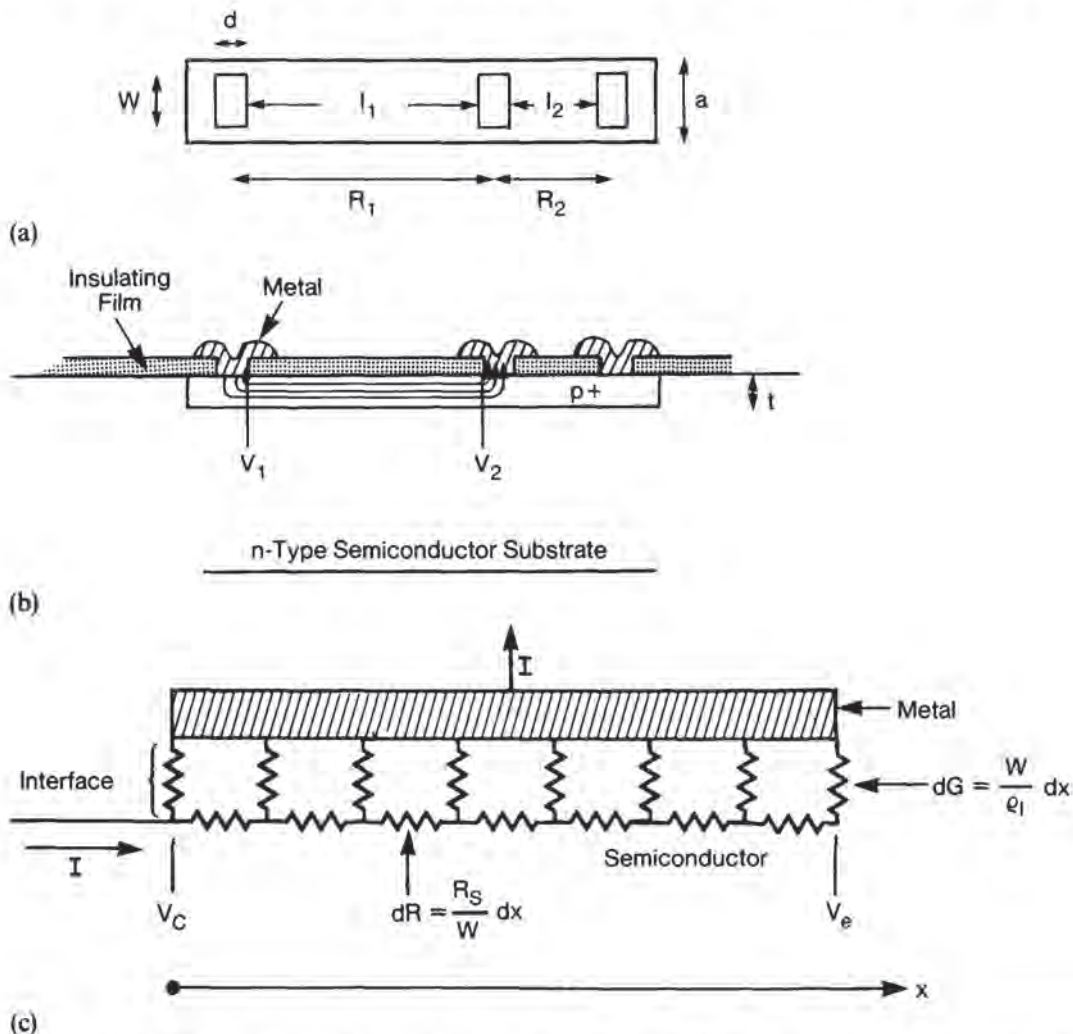


Fig. 3 (a), (b) The three-terminal resistor structure. V_1 and V_2 denote equipotential surfaces between which planes the current lines run parallel. The junction depth is given as t . (c) The transmission line model pertaining to one particular contact region and definitions of the various relevant quantities.

noted above, TLM also stands for the transfer length method.) The approach of Murrmann and Widmann was based on solving the differential equations that describe the transmission line^{34,38}, whereas Berger's⁴¹ approach was to solve the transmission line equations for the equivalent circuit of Fig. 3(c). The latter approach was also taken by Chang⁴² who found it necessary to modify the sheet resistance value in order to bring about an agreement between the experimental data and the theoretical results of the transmission line model. Chang justified the modification of the R_s value by describing the effects of metallurgical reactions that take place during the contact formation. While that is most probably the case for silicide contacts, it is somewhat difficult to justify in the case of aluminum contacts, as also questioned by Berger⁴¹. The original transmission line calculations also assumed that the three-terminal resistor is of vanishing thickness ($t = 0$) although its sheet resistance is finite. This unrealistic situation was also discussed by Berger who phenomenologically introduced a quantity which may be called the apparent specific interface resistance, which is supposed to account for the voltage drop over the semiconductor junction beneath the contact interface. A consideration of the voltage drop along the width of the contacts was suggested by Finetti *et al.*⁴³ This, however, turns out to be an unnecessary correction except for unrealistically wide contacts. In a recent publication, Marlow and Das⁴⁴ discussed the correction to the contact resistance due to the finite sheet resistance of the metallization. This may be of particular interest in cases involving relatively low conductance interconnect materials such as various metal silicides.

References 37–42 contain all the important results of the transmission line calculations. Essentially, these result in analytic expressions that relate the measured contact resistance (as obtained by means of eqn. (11)) with the sheet resistance, the specific interface resistance and the contact width and length parameters. Here we shall only quote two results that point to a major difficulty with this method of contact resistance determination. This difficulty is connected with the voltage drop measurement. While the current through the metal–semiconductor interface is easily measured, the assignment of the exact location for the voltage drop is less obvious. The measured voltage drop is defined as the difference between the potentials on two *suitably* chosen equipotential surfaces. The lack of a clear knowledge of where exactly in the contact region the voltage drop is being sensed (or where its average value is being measured) creates a major problem. Two obvious locations have been identified by Berger⁴¹. According to one approach the voltage drop is measured at the entrance to the contact region (V_e in Fig. 3(c)). This approach yields the following relation:

$$R_c = \frac{1}{W} (R_s \rho_l)^{1/2} \coth \left\{ d \left(\frac{R_s}{\rho_l} \right)^{1/2} \right\} \quad (12)$$

According to the other approach the voltage drop is sensed at the end of the contact opening (V_e in Fig. 3(c)). This then results in the following relation for the measured contact resistance:

$$R_c = \frac{1}{W} (R_s \rho_l)^{1/2} \left[\sinh \left\{ d \left(\frac{R_s}{\rho_l} \right)^{1/2} \right\} \right]^{-1} \quad (13)$$

Thus, these two approaches predict different dependences of R_c on the contact

length. Recent results on the size effect on contact resistance do not seem to support either of these two different results⁴⁵. We shall return to discuss the size effect in Section 5.

The inability to determine unambiguously the location at which the voltage drop is sensed is common to other methods of contact resistance determinations that utilize "planar" resistor structures. In Section 3.3 we shall see how this also affects the analysis of results for the four-terminal resistor structure. Beyond this, however, some problems exist with the three-terminal resistor structure that cast doubts on its usefulness for VLSI applications in which the ρ_c values are expected to be of the order of $100 \Omega \mu\text{m}^2$ and lower. We shall briefly discuss here the major difficulties.

(1) The quantities $R_1 l_2$ and $R_2 l_1$ in eqn. (11) are both much greater than the expected value of R_c and are of comparable numerical values. R_c is given in terms of their difference and hence it is difficult to see how, in cases of very low R_c values, it can be determined to any degree of accuracy. Of particular concern are errors made in measuring the resistor lengths l_1 and l_2 . In fact, in some cases⁴⁶ negative values for R_c result, presumably because of this problem.

(2) In deriving eqn. (11), an implicit assumption has been made that the contact resistances of all three contacts are identical. In reality, this of course need not be true as various surface defects and contaminations may alter the value of R_c from contact to contact. Indeed, in a recent study⁴⁷ we obtained values for R_c from individual contacts which differed by more than 200%. Thus, the practical validity of eqn. (11) in such cases is questionable.

(3) Inaccuracies may also exist in determining R_c in cases where $W \neq a$ (see Fig. 3). In such cases, lateral current spreading can introduce large errors since this is a non-linear effect and $l_1 \neq l_2$.

Thus, while the conventional three-terminal resistor method may have been adequate in cases of devices with large geometries, it is doubtful whether it can be of much use in VLSI technology where low values of R_c must be determined accurately.

3.3. The four-terminal Kelvin resistor

The main difficulties with the three-terminal resistor method of contact resistance determination have to do with the fact that a difference rather than an absolute value for V/I is derived. This situation is remedied by the four-terminal Kelvin resistor which involves only one single contact for the R_c measurement. The structure is shown in Fig. 4(a). It contains four landing metal pads that lie on an insulating film. Two of these are connected to an implanted bar of appropriate shape by means of large-area contacts. The other two pads contact the semiconductor surface at the contact opening (the filled square in Fig. 4(a)). Any two of these terminals which are not positioned diagonally with respect to each other may be used for passing current through the contact, while the other two terminals are simultaneously used to sense the voltage drop across the interface and the junction beneath it.

This geometry can also be modified so as to have the horizontal components of the field and stream lines perpendicular to each other. It is then possible to eliminate the contribution to the voltage drop associated with the horizontal component of the current in the contact region. This may eliminate any need to correct for the

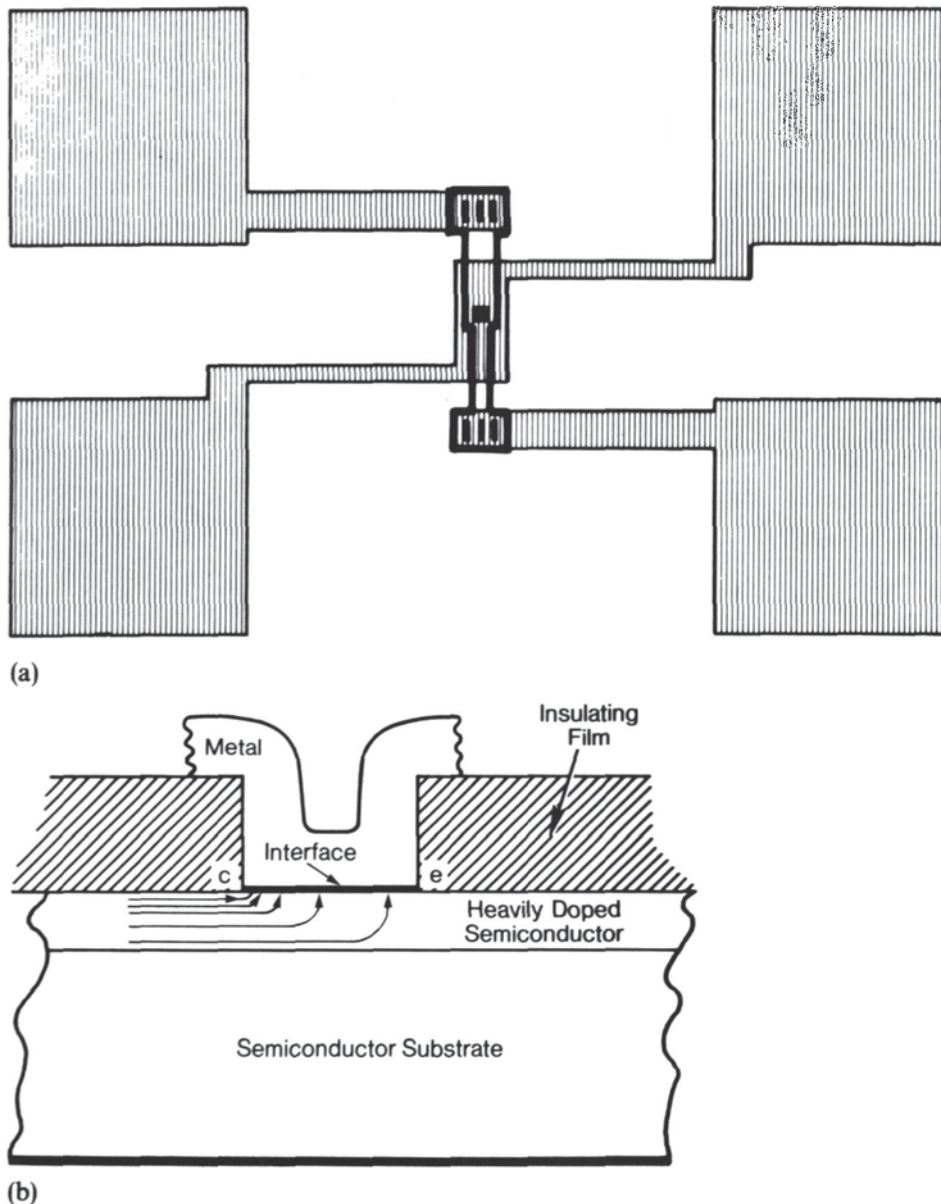


Fig. 4. (a) The four-terminal Kelvin resistor structure. The bold lines depict the implant bar area. The filled square is the actual contact and the other bold structures depict the contacts to the active area. The metal covers the shadowed area. (b) Illustration of how the current spreads and bends in the contact region underneath the interface.

voltage drop along the contact width. As seen in Fig. 4(a), the geometry of the implanted bar is such that contributions due to the lateral current spreading may be minimized, depending on the current direction.

Owing to the fact that the four-terminal resistor involves only one contact in the process of contact resistance measurement, there exist no practical limits to the value of R_c that can be measured. Indeed, in some cases we were able to obtain values of ρ_c (for $3\text{ }\mu\text{m} \times 3\text{ }\mu\text{m}$ contacts) which were as low as $1\text{ }\Omega\text{ }\mu\text{m}^2$ and lower. This feature of the four-terminal resistor is particularly important since with the advent of VLSI technology a need exists to measure small values for ρ_c accurately. As was the case for the three-terminal resistor, the four-terminal Kelvin resistor also does not yield the interface resistance directly. In fact, much the same “parasitic” contributions to the contact resistance exist here as well. These are mainly the contributions due to

current crowding effects³⁶ (shown in Fig. 4(b)) and the junction sheet resistivity. Thus the same transmission line equations may be employed, in principle, in an attempt to separate the various contributions.

The four-terminal Kelvin resistor mode of R_c determination does have one more major advantage over other existing methods. The type of square contacts shown in Fig. 4(a) are essentially those used in small aspect ratio field effect transistors. Hence the values of R_c as determined by this method of measurement, although made up of several contributions, are those which bear direct relevance to the contact resistances in real device contacts. Thus, even if no realistic theoretical models exist which would enable one to single out the contribution due to the interface resistance, the practical importance of the four-terminal resistor seems to be obvious.

In a sense, the study of McNeil⁴⁸ on metal-to-metal contacts is perhaps the first use made of the four-terminal Kelvin resistor in the context of semiconductor technology. In fact, McNeil did not even use all four terminals in his measurement set-up. Shih and Blum⁴⁹ seem to be the first to use this structure for evaluating metal-to-semiconductor contact resistance. Thereafter, only a limited number of studies that describe the four-terminal Kelvin resistor have appeared. One of these is that of Anderson and Rieth⁵⁰ and the other report belongs to Beuhler⁵¹. The interest in this method of contact resistance measurement has been renewed recently for reasons already mentioned above^{47, 52, 53}.

4. CONTACT RESISTANCE IN METAL-TO-SILICON SYSTEMS

Over the years many metallization systems have been studied in order to evaluate their suitability for silicon integrated circuit technology. To date the most widely used metal is aluminum and its alloys with silicon and copper. These alloys were introduced in order to solve such metallurgical failures as spiking⁵⁴ and electromigration. A spiking failure ends with shorting of the junction whereas voids in the metal line caused by electromigration result in open circuits. Several other hazards, however, still exist for devices fabricated utilizing aluminum metallizations. The barrier height of a newly formed Al/Si contact is very sensitive to the interface properties, *i.e.* to the surface preparation and the aluminum deposition conditions^{55, 56}. Significant aging effects are sometimes observed in the electrical characteristics of these contacts⁵⁷, and sintering can result in changes in the Al/Si barrier height owing to the dissolution of silicon in aluminum with subsequent silicon recrystallization at the interface on cooling⁵⁸⁻⁶⁰. Because of these and other problems such as the difficulty in patterning fine aluminum lines, aluminum as a single-metallization system may become obsolete for VLSI. However, for conventional integrated circuits with moderate junction depth of about 1–2 μm , aluminum is uniquely suited as a single-element metallization system. In such a level of integration, detrimental metallurgical effects are seldom observed and the contact area is large enough (of the order of 10–20 μm^2), so that the contact resistance is well within the desired range. Other factors contributed to the choice of aluminum as a metallization agent. It adheres well to both silicon and SiO_2 surfaces and is one of the better conductors available. It is also known to react with small amounts of SiO_2 , usually present as a native layer on the silicon surface when sintered at moderately low temperatures.

We have used the four-terminal Kelvin resistor structure to evaluate the contact resistance to both n^+ -Si and p^+ -Si using an alloy of Al-0.9%Si⁴⁷. Briefly, the average ρ_c values were found to be approximately $15 \Omega \mu\text{m}^2$ for contacts made to p^+ -Si and about $90 \Omega \mu\text{m}^2$ for contacts made to n^+ -Si. The surface dopant concentrations were $6 \times 10^{19} \text{ cm}^{-3}$ and $3 \times 10^{20} \text{ cm}^{-3}$ respectively. A fuller description of this study may be found in ref. 47. We have also used the four-terminal structure to study platinum silicide and molybdenum contacts to silicon.

Only a few studies on the contact resistance between platinum silicide and heavily doped silicon have been reported in the literature. An extensive study of the microstructural and electrical properties of thin PtSi films was carried out by Anderson and Rieth⁵⁰. In this study, a direct relation was established between the microstructural and electrical properties of the silicide film. Also, the effects due to various deposition parameters, and the dopant species and concentration were examined. Muta²⁵ studied the electrical properties of the Pt/n-Si system which was annealed at different temperatures in an H_2 ambient. Ohmic contacts were obtained when the arsenic bulk concentration exceeded $7 \times 10^{18} \text{ cm}^{-3}$. Values for the specific contact resistance ranged from 20 to $200 \Omega \mu\text{m}^2$, depending on the sintering temperature. These values are quoted for the highest dopant concentration used. Dopant concentrations lower than $7 \times 10^{18} \text{ cm}^{-3}$ were reported to yield nearly ideal Schottky barrier devices.

In our study of platinum silicide contacts^{52,61} several important parameters were checked. We observed an improvement in the contact resistance results when *in situ* heating and presputter etching were employed prior to the platinum deposition. Other parameters that were varied included the dopant concentration and the final metallization layer. As would be expected, the contact resistance was found to depend strongly on the dopant concentration. Because of lack of space we shall not discuss all these variables here. We shall merely list the best results that we have obtained. These were about $7 \Omega \mu\text{m}^2$ for the PtSi/ p^+ -Si system (for a surface dopant concentration N_s of $7 \times 10^{19} \text{ cm}^{-3}$) and about $4 \Omega \mu\text{m}^2$ for the PtSi/ n^+ -Si system ($N_s = 3 \times 10^{20} \text{ cm}^{-3}$). Similar results ($\rho_c \leq 10 \Omega \mu\text{m}^2$) were also obtained for direct molybdenum contacts to both p^+ -Si and n^+ -Si. Molybdenum contacts were also studied by Yanagawa *et al.*⁶² who quote a value of about $150 \Omega \mu\text{m}^2$ for ρ_c and by Mochizuki *et al.*⁶³ who obtained a value of about $70 \Omega \mu\text{m}^2$ in the case of low temperature (below 600°C) sintering.

In our studies of contact resistance, the I - V characteristics were linear in the range $-5 \text{ mA} \leq I < 5 \text{ mA}$. At such current levels, the current density in a small aspect contact would be rather high. This could then result in undesirable metallurgical effects. We have not witnessed any such phenomena in our studies. However, in these experiments the bias was applied for only a short time.

5. SIZE EFFECT ON CONTACT RESISTANCE

According to the scaling theory² the contact resistance is assumed to scale as k^{-2} , where k is known as the scaling factor. The scaling theory apparently assumes the measured contact resistance R_c to be identical with the interface resistance R_i . However, as we have seen, none of the measurement method truly yields a value for R_i . Instead, it is R_c which also includes various "parasitic" contributions that is

easily determined. Because no satisfactory theory capable of separating the various contributions to R_c seems to exist, it has become of interest to determine experimentally what sort of scaling rule R_c follows. Such a study also became timely because of concerns regarding the small geometries involved in VLSI technology. Our study involved square contacts whose size ranged from 0.8 to 10 μm . A full discussion of the results of this study will appear elsewhere⁴⁵. Here we limit ourselves to some essential features.

Figure 5 shows the data for PtSi contacts made to n^+ -Si with aluminum as a final metallization layer. These data were obtained from three different contact sizes: 1.5 $\mu\text{m} \times 1.5 \mu\text{m}$, 3 $\mu\text{m} \times 3 \mu\text{m}$ and 5 $\mu\text{m} \times 5 \mu\text{m}$. In Fig. 5(a) ρ_c as a function of W^2 is plotted. A clear trend to even lower ρ_c values with a further lowering of W is seen. In Fig. 5(b) R_c is plotted against W . The full curve describes average experimental results. The broken curve shows the expected behavior for R_i according to the scaling theory and assuming the value of R_c for $W = 5 \mu\text{m}$ as a basis for the calculation. It should be emphasized that such size effects become significant for low contact resistances. If care is not taken to process the contacts properly, surface contaminants and defects may be present at the interface. These would normally increase the interface resistance and cause the size effects to become less noticeable.

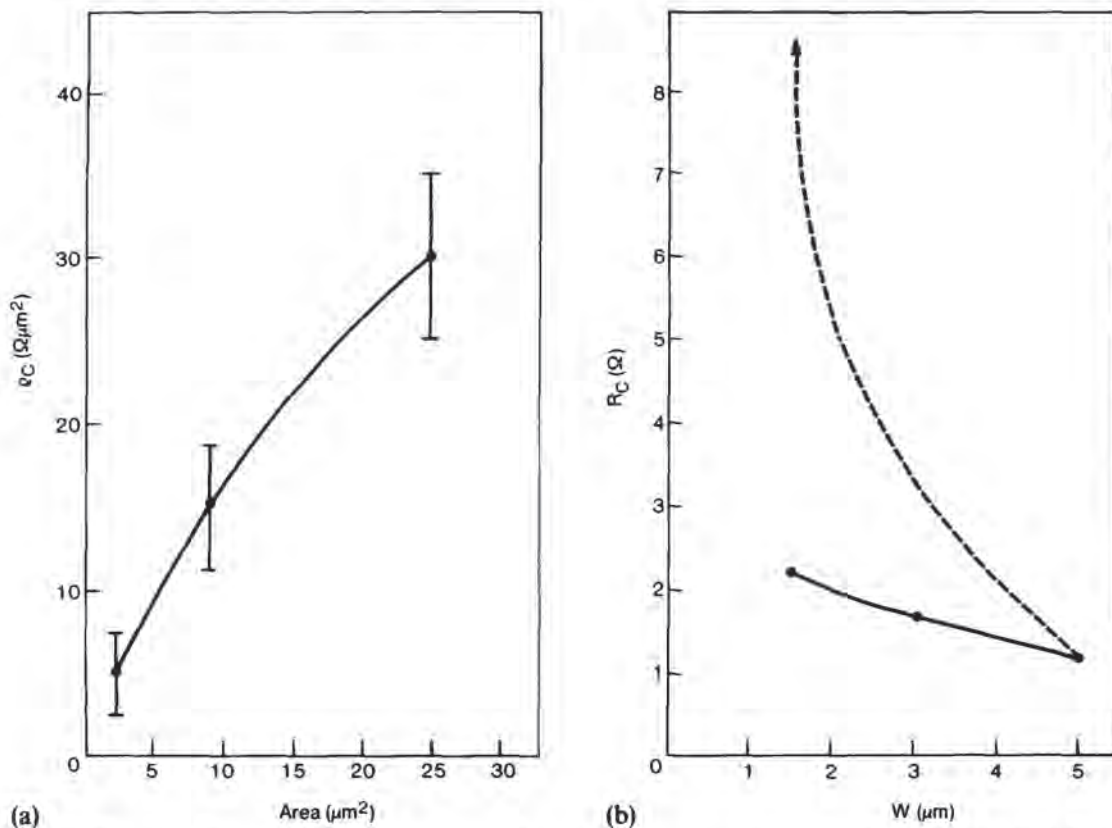


Fig. 5. The size effect on contact resistance as shown by the measured curves of (a) ρ_c vs. A and (b) R_c vs. W (---, expected behavior according to the scaling theory).

On the basis of these results two important conclusions can be made. First, it may be concluded that the scaling law for R_c may be substantially different from the quadratic law that, strictly speaking, applies only to R_i . Secondly, there seems to be no contact resistance problem associated with the envisaged submicron

geometries in future VLSI applications. Thus, the practical implications of the non-quadratic scaling of R_c may include less pressure for the development of alternative contact metallization systems for VLSI circuits. It may also suggest that revisions of estimates of achievable design rules be made.

6. SUMMARIZING REMARKS

The purpose of this presentation was to discuss several methods of metal-to-semiconductor contact resistance determination that are either widely used or hold promise for current needs. Common to all existing practical methods is the simplicity of the measurement scheme that yields "a resistance value". The analysis of this "resistance value", however, is not a trivial task and hence calls for much caution in discussing measured contact resistance values. Of all the resistor structures discussed here, we find the four-terminal Kelvin resistor mode of measurement to be the most satisfactory for two important reasons. It involves only one contact in the measurement; hence, an absolute value for R_c is obtained rather than a relative value as is the case in other methods. This then provides us with the ability to measure very small values of R_c accurately. Finally, the similarity of the contact measurement situation to that in real devices makes the values of R_c so determined of direct relevance.

The traditionally used terms of contact resistance R_c and specific contact resistance ρ_c , which through the years have been confused in more than one way, we have proposed to associate with the *experimentally measured quantities*. Thus, $R_c = V/I$ and $\rho_c = AV/I$. The theoretical equivalents of these, we have labeled R_i and ρ_i . Theoretically, it should be mentioned, the sole cause of the resistance is in the existence of an interface. The resistance-causing phenomena are assumed to be homogeneous over the contact area, and hence ρ_i is a constant which is independent of the contact size. As we have shown, recent experimental results indicate quite a different behavior for ρ_c . Fortunately, this happens to be in the desired direction for the emerging VLSI technology needs.

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