

Review on Methods for Trench MOSFET Gate Oxide Reliability and Switching Speed Improvement

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In high density vertical trench power double-diffused metal oxide semiconductor (DMOS), the trench width (CD) continually shrinks as driven by the market for low cost and longer battery lifetime. Subsequently, this imposes technical challenges to keep high breakdown voltage without affecting other performances such as gate charge and on-state resistance. This paper discusses some of the technical challenges faced and suggested solutions. The various methods to improve the trench oxide uniformity and trench corner profile are also presented through experimental data. Different methods to thicken the trench bottom oxide to reduce gate-to-drain capacitance (C_{gd}) and eliminate the oxide weak points are introduced. This paper also reviews advanced industrial developments to increase the device switching speed as well as breakdown voltage.

Introduction

Low on-state resistance ($r_{ds(on)}$), low gate charge for high switching speed, high drive current, high transduction and high breakdown are the main considerations in designing power MOSFETs. There are two main types of structural designs [1], [2]: lateral channel (the drain, gate, and source terminals are placed on the surface of a wafer) and vertical channel (the drain and source terminals are placed on the opposite sides of a wafer) designs. The former is suitable for process integration but not for obtaining high power ratings since the distance between source and drain must be large to obtain better voltage blocking capability. Figure 1 illustrates the vertical channel design variation [2]. VMOSFET is believed to be the first design to be commercialized in 1970's [3], but replaced by the DMOSFET due to the sharp tip at the bottom of V-groove degrading its breakdown voltage. Trenched DMOS, which emerged in 1990's, has a higher channel density which reduces the on-resistance as compared to the DMOSFET. For low voltage applications, trenched DMOS is preferred because of the very long gate widths that can be achieved in a given chip area at cell density above 30 million cells/inch² [4] and further improvement to 530 million cells/inch² [5].

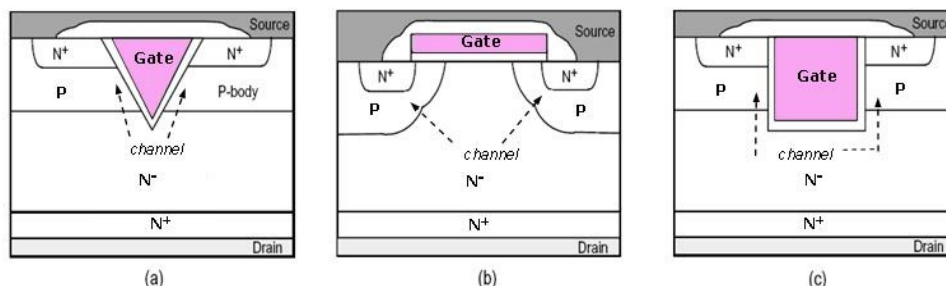


Figure 1. Three types of vertical channel structures, (a) VMOSFET, (b) DMOSFET or VDMOS, (c) UMOSFET or trenched DMOS used throughout in this paper.

Trenched DMOS is preferred over a planar structure because of its high cell density, enabling high drive current with low $r_{ds(on)}$ for a fixed space. In high density trenched DMOS, the trench width continually shrinks. Subsequently, this imposes technical challenges to keep high breakdown voltage without affecting other performances. The various methods to improve the trench oxide uniformity and trench corner profile are presented in this paper as well as different methods to thicken the trench bottom oxide. To have high switching speed, the C_{gd} is reduced by further increasing the trench bottom dielectric thickness or by novel split trenched gate methods reviewed in the last section.

Technical Challenges

Some technical challenges such as deep trench etching, corner rounding or gate oxide weak spots in deep trench, thinner gate oxide at trench bottom versus sidewall due to silicon crystallography and diffusion rate etc. are discussed in this section.

Deep Trench Etching and Convex Corner

The shift from DMOSFET to trenched DMOS required an advanced trench etch technology which was originally developed for DRAM. This challenge has been solved progressively by advanced reactive ion etch (RIE) technology as driven by the need of shallow trench isolation (STI). Ho et al [6] disclosed the technique in 1980 called the U-shaped MOSFET random access memory.

However, there is a challenge on gate oxide reliability due to the oxide thinning at the trench bottom convex corners. The oxide thinning is due to the stress increase following the volume expansion during conversion from Si to SiO_2 [7]. Scanning electron microscopy (SEM) images showed in Figure 2 illustrate the oxide thinning effect, before and after a furnace oxidation on the surface of a trench formed by RIE.

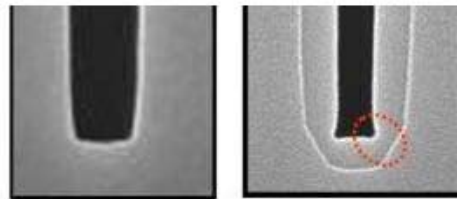


Figure 2. SEM images illustrates the trench profile before (left) and after oxidation (right)

Silicon Crystallography

Apart from the oxide thinning at the trench corners, the oxide thickness at the trench bottom is relatively lower than at the sidewall. In trenched DMOS, a wafer substrate with (100) crystal orientation is preferred due to the highest electron mobility that results in a smaller on-resistance. The oxidation rate on a (100) plane is lower than that on a (110) plane. Figure 3 demonstrates the crystallography effect.

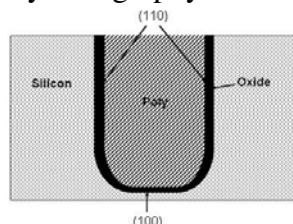


Figure 3. Schematic cross section of a trench showing thinner oxide at a (100) plane.

Restricted Oxidation Rate

It is speculated that the weak spots at trench corners are also due to the restricted thermal oxide growth, which is caused by the limited oxygen diffusion into the corner interface between insulator and sidewall substrate. The reason may explain the thinner oxide at the trench bottom on smaller trench width. The effect of restricted oxidation vanishes on the larger CD for which the non-uniformity of the thickness is solely due to the crystallography effect.

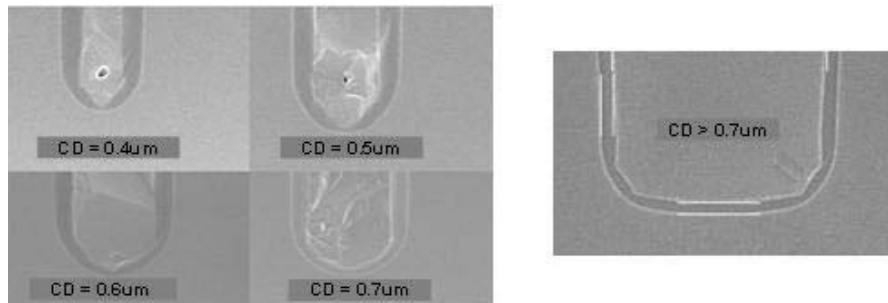


Figure 4. Trench bottom gate oxide thinning for various trench CD (left), reproduced from [8] and a more uniform thickness for larger CD (right).

Experimental Results

Double Sacrificial Oxidation before Gate Oxidation

After the RIE trench etch, a high temperature oxidation process, normally known as sacrificial oxidation (SACOX), is performed to remove the plasma damaged silicon layer to prepare a defect-free interface for subsequent trench gate oxidation. SACOX is also having an important task to round off the trench right-angled corners. This “rounding-off” SACOX has been studied intensively in [7], [8], and [9]. Some major factors to determine the oxide leakage and breakdown voltage from corner rounding includes: 1. Thickness of SACOX, 2. Oxidation temperature of SACOX, 3. Oxidation rate or diluted oxidizing ambient or H₂O concentration of SACOX, 4. Isotropic and anisotropic RIE, 5. Wet or dry etching before SACOX, and 6. Gate oxidation temperature.

In our experiment, we studied the two times SACOX (double SACOX) as the single SACOX is not enough to round off the convex corners for CD < 0.5um. Figure 5 compares the effect of single SACOX and double SACOX on the corner rounding performance for trench CD < 0.5um. The oxide thinning is still observed on the trench bottom corners using single SACOX.

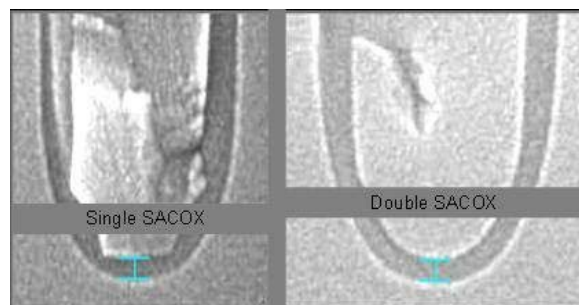


Figure 5. The trench bottom profile comparison of the single and double SACOX after gate oxidation and doped-polysilicon deposition.

Trench Bottom Implantation

Si oxidation rate can be enhanced or retarded by ion implantation at the trench bottom. It depends on the implant species, level of amorphisation, implant energy, dose. Inert gas such as Ar was implanted in the bottom of the trench to increase the gate oxidation rate [10]. Other species such as As, P, F can also enhance the oxidation rate but some electrical performance may be affected. Besides, ion implantation of oxygen has been suggested, followed by gate oxidation [11] or converted to silicon dioxide by high temperature anneal [12].

Advanced Methods Reviews

There are plenty of patents filed or issued on the methods to improve the trenched DMOS switching speed and breakdown voltage focusing on the trench area in addition to corner rounding and ion implantation. The methods vary from simple local oxidation of silicon (LOCOS) to a complex group of processes such as deposition, etch back, re-deposition. Table I shows two examples of how to increase the thickness of thermally-grown silicon dioxide at the bottom of the trench by the LOCOS method.

TABLE I. Thick Bottom Oxide from LOCOS

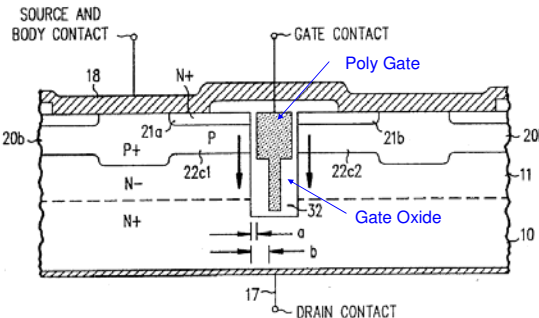
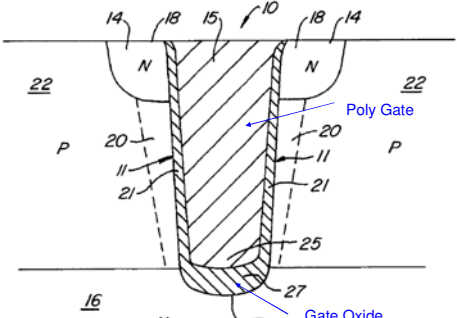
Source, drawings and description	
Blanchard et al. 1990 [13]  - Two distinct oxide thicknesses - LOCOS at sidewalls as well as bottom of the trench where are not protected by nitride layer. - Gate dielectric thickness "a" provides low device rdson and high device gain in the channel region. - Dielectric thickness "b" increases the field plate induced breakdown above the limit set by "a".	Hurst et al. 2002 [14]  - Self-aligned LOCOS at bottom of a trench. - The thicker dielectric layer at the bottom substantially reduces gate charge to reduce the Miller Capacitance effect, thereby increasing the efficiency of the semiconductor device.

Table II presents four examples of fabricating thick bottom oxide by deposition: 1. Chemical vapor deposition (CVD) of borophosphosilicate glass (BPSG), spin on glass (SOG) or polyimide [15] in the core surrounded by conductive polysilicon gate, 2. Selective CVD using TEOS [16], for example, the selectivity of TEOS depositing on trench bottom, silicon surface to barrier layer, silicon nitride is 5:1. 3. CVD oxide with composite dual gate layer [17] and 4. High density plasma (HDP) CVD oxide layer filling a tub-shaped trench etch at the bottom of a trench [18]. There are other novel methods invented as reported in [19], [20] and [21] which have some similarities with the examples showed in Table II. Table III shows two examples of split trench gate designs [22], [23] where the thick bottom oxide is replaced by polysilicon or a combination of polysilicon and thick bottom oxide.

TABLE II. Thick Bottom Oxide from Deposition

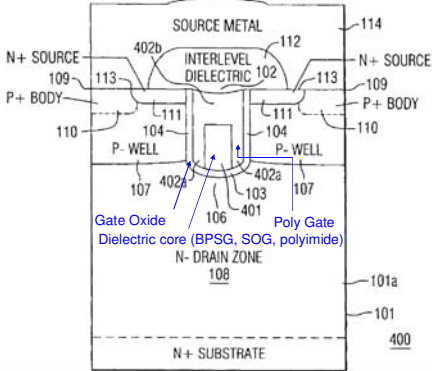
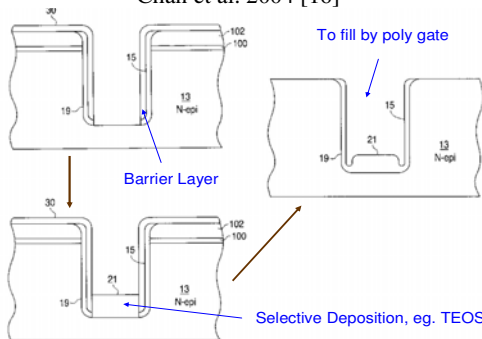
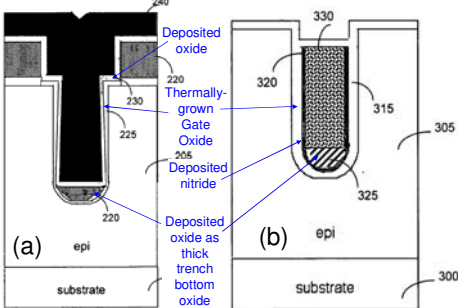
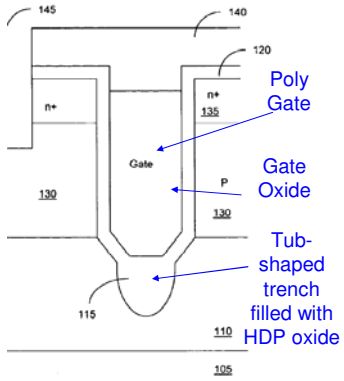
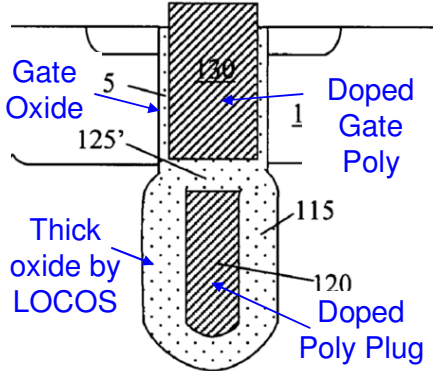
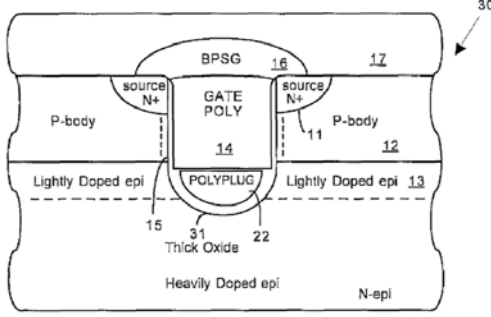
Source, drawings and description	
Hao et al. 2003 [15]	Chan et al. 2004 [16]
 Dielectric layer is deposited by CVD filling the “hole” surrounded by poly gate. The “hole” is centrally etched. Alternatively, the centrally disposed core extends upwardly from trench bottom to top surface.	 A thick insulating layer is deposited by CVD selectively in the bottom of the trench. The barrier layer is selected (e.g. silicon nitride or silicon dioxide) such that the thick insulating layer deposits in the bottom of the trench (e.g. TEOS) at a faster rate than on the barrier layer.
Hshieh et al. 2006 [17]	Hshieh et al. 2009 [18]
 Thick bottom oxide is formed by a combination of CVD nitride liner, CVD thick oxide, etch back etc. The trench gate dielectric consists of two layers, thermally-grown silicon dioxide as outer layer and CVD silicon dioxide or silicon nitride as inner layer encloses the poly gate.	 Thick bottom oxide is formed in a tub-shaped trench beneath the trenched gate instead of conventional flat or slightly convex trench bottom surface.

TABLE III Split Trenched Gate Techniques

Source, drawings and description	
Tai et al. 2008 [19]	Giles et al. 2009 [20]
 There are two conductive gate poly plugs. The thick oxide formed by LOCOS encompasses the first poly plug in the drain region. The trenched gate surrounded by the source region encompassed in the body region above the drain region.	 Thick oxide layer is grown on the sidewalls and bottom of the trench, depositing a polysilicon layer, etching the polysilicon layer to form the plug, etching the exposed portion of the thick oxide layer, growing a gate oxide layer and an oxide layer over the plug, and depositing and doping a polysilicon layer which serves as the gate electrode.

Conclusion

In this review paper, the technical challenges to keep high breakdown voltage focusing on the trench aspect have been discussed. From the simplest double sacrificial oxide method to the advanced double gate solution, the various methods to thicken the trench bottom oxide to reduce C_{gd} and eliminate the oxide weak points have been reviewed. In conclusion, the structural design and process flow for fabrication of trench DMOS is very much dependent on the foundry capability, manufacturing complexity and creativity on the selection of module processes especially etch and thin film engineering as well as the extent of improvement needed.

Acknowledgments

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