

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INERGY TECHNOLOGY, INC.,
Petitioner

v.

FORCE MOS TECHNOLOGY CO. LTD.,
Patent Owner

Inter Partes Review No. IPR2024-00094
U.S. Patent No. 7,812,409

DECLARATION OF DEAN NEIKIRK, PH.D.
IN SUPPORT OF PATENT OWNER'S RESPONSE

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I. INTRODUCTION

1. I have been retained by Patent Owner Force MOS Technology Co. Ltd. (“Patent Owner” or “ForceMOS”) in this *inter partes* review proceeding number IPR2024-00094 (“IPR”), filed by Petitioner Inergy Technology, Inc. (“Inergy” or “Petitioner”). I understand that this IPR proceeding involves U.S. Patent No. 7,812,409 (the ’409 patent) and that the challenged claims are claims 1-6 (the “Challenged Claims”).

2. I have been asked to provide my objective, independent analysis of the ’409 patent in view of the asserted prior art references cited in the Petition and to provide my opinion regarding the allegations in the Petition, as well as the supporting opinions of Dr. David Kuan-Yu Liu.

3. I have based my opinions on the information available to me as of the date of this declaration. I understand that additional information may become available after this declaration is submitted. If I become aware of additional information following my submission of this declaration I may, if I am permitted, offer additional opinions (including by amending and/or supplementing this declaration) taking into account such new information.

4. I am not currently, nor have I ever been, an employee of Force MOS. I received no compensation for this declaration beyond my normal hourly compensation based on my time actually spent working on this IPR. I will not

receive any added compensation based on the outcome of this IPR, any other IPR, or any other proceeding involving the '409 patent.

II. BACKGROUND AND QUALIFICATIONS

5. My qualifications are most accurately reflected in my curriculum vitae, which is Exhibit 2022. The following is a brief summary of some of my relevant experience and qualifications.

6. I have over 40 years of experience in electronic devices and systems, including the methods used to fabricate integrated circuits and devices.

7. I received a B.S. degree in 1979 in physics from Oklahoma State University, and an M.S. degree and a Ph.D. degree in 1981 and 1984, respectively, in applied physics from the California Institute of Technology.

8. Each of my academic degrees involved significant studies in solid state physics, semiconductor devices, electrical engineering, electronic systems, electromagnetics, optics, radio frequency systems, and antennas. For example, courses relating to these fields that I took include two years of study in electromagnetics and optics, one year of study in solid state and semiconductor physics, as well as four years of graduate research in electronic devices, antenna design, antenna fabrication, microwave systems, and optical systems. My Ph.D. thesis was on the design and fabrication of high frequency electromagnetic detectors and imaging arrays, including research on integrated-circuit fabrication, antennas,

sensors, and packaging. I designed and fabricated the first monolithic integrated-circuit imaging array for use at wavelengths in the far infrared (sometimes referred to as the terahertz) region of the electromagnetic spectrum. This research work required the fabrication, testing, and field placement of devices with many output channels, presenting a significant challenge (at that time) in packaging. I personally developed packages for my devices, and personally performed the packaging itself. At that time the most common method of connection made use of wirebonding, which I personally performed.

9. I am currently a Life Senior Member of the Institute of Electrical and Electronics Engineers (“IEEE”). From March 1991 to October 1994, I served as an Associate Editor for the IEEE publication called “IEEE Transactions on Education.” I also served as a member of the Editorial Board on the IEEE Transactions on Microwave Theory and Techniques in the 1990-2000 timeframe.

10. I have almost 40 years of experience on the faculty of the University of Texas at Austin. My work as a professor began in 1984, when I joined the University of Texas at Austin as an assistant professor. In 1988, I became an associate professor, and became a full professor in 1992.

11. My research over the last forty years has concentrated heavily in the areas of electromagnetics, microwave engineering, microelectronics, semiconductor devices, integrated circuit (IC) fabrication, and new sensors. This research work has

been funded by many agencies, focusing on the fabrication and modeling of semiconductor devices, electromagnetic devices and detectors, chemical sensors, temperature sensors, proximity sensors, and pressure sensors, as well as research on the high frequency properties of transmission lines, RF devices, and infrared to terahertz detectors for use in focal plane imaging arrays. My research related to the development of new chemical sensors (an “electronic taste” sensor) was selected for a commercialization venture between The University of Texas and two outside startup companies.

12. Over the years, I have also taught a variety of electrical engineering courses at the University of Texas. These include Integrated Circuit Fabrication, VLSI Fabrication Techniques, Ultra Large Scale Integrated Circuit Fabrication Techniques, Integrated Circuit Nanomanufacturing Techniques, Electromagnetics in Packaging, Simulation Methods in CAD/VLSI, Micro-Electromechanical Systems, Electromagnetic Engineering, and Microwave and Radio Frequency Engineering. I have also taught several continuing education courses in these fields.

13. In 1985, I established the Microelectronics Fabrication Teaching Laboratory at The University of Texas at Austin, which continues to this day to provide undergraduate and graduate students with hands-on experience in integrated circuit fabrication. I have taught many courses in integrated-circuit fabrication, microwave devices, integrated circuit packaging, electromagnetics, computer aided

design methods for circuit simulation, sensors of all sorts, and microelectromechanical systems.

14. I conducted research with students and research scientists in the Microelectromagnetics Research Group in the Microelectronics Research Center at The University of Texas at Austin for 37 years. For over ten years, I also served as the Graduate Advisor of the Department of Electrical and Computer Engineering at the University of Texas at Austin, as well as serving for over five years as an Associate Chairman of the Electrical and Computer Engineering Department at The University of Texas at Austin. I also served as Associate Dean of Graduate Studies from 2014 to 2021.

15. In addition to my work at The University of Texas at Austin, I have done part-time consulting work since 1984 as an independent consultant to the industry for technical projects and as a technical expert in legal cases. I am a senior member of the IEEE. Through my work on sensors, electronic systems, and innovations in other related fields, I have been named an inventor on 17 U.S. patents. These are summarized in my curriculum vitae.

16. As a result of my professional education and experience, I am qualified to render opinions in the areas of semiconductors and their fabrication, and in particular, the subject matter of the patents-in-suit.

III. COMPENSATION

17. I am being compensated as an expert witness in this case at my standard hourly rate in addition to out-of-pocket expenses. I have received no additional compensation for my work on this matter and my compensation does not depend, and has not ever depended in any way, on my opinion as expressed in this matter, in any testimony that I may give, or on the outcome of this matter. I am not and have never been employed by Force MOS. I have no financial stake in Force MOS, the ‘409 Patent, or the outcome of this IPR or any other matter involving the ‘409 Patent.

IV. MATERIALS CONSIDERED

18. In formulating my opinions, I have relied upon my training, knowledge and experience that are relevant to the ‘409 Patent. I have also considered the ‘409 Patent and its file history, Petition (“Pet.”) and attached exhibits, the Patent Owner preliminary response, the Board’s decision on institution, the asserted prior art references, and the declaration of Dr. Liu and the materials cited therein. In addition to the materials cited elsewhere in this declaration, I have also considered the following:

Exhibit No.	Description
2006	U.S. Patent No. US6700158B1 to Cao et al., “Trench corner protection for trench MOSFET”
2007	Excerpts of Webster’s Dictionary 3 rd . Ed.
2011	Claim Construction Order, Dkt. No. 132 from <i>Force Mos Technology Co., Ltd. v. ASUSTeK Computer, Inc.</i> , Case No. 2:22-cv-00460-JRG (E.D. Tex.)

2012	U.S. Patent No. 5,304,831 to Yilmaz et al., “Low on-resistance power MOS technology”
2013	U.S. Patent No. 6,867,083 to Iman et al., “Method of forming a body contact of a transistor and structure there”
2014	Excerpts of Lutz, Josef, et al. "Semiconductor power devices." 2018, ISBN 978-3-319-70917-8 (“Lutz”);
2015	Li, S., & Boyd, J. P. (2015). Approximation on non-tensor domains including squircles, Part III: Polynomial hyperinterpolation and radial basis function interpolation on Chebyshev-like grids and truncated uniform grids. <i>Journal of Computational Physics</i> , 281, 653–668. doi:10.1016/j.jcp.2014.10.035
2016	Maneuski, Dima, V. Gostilo, and A. Owens. "TCAD simulation studies of novel geometries for CZT ring-drift detectors." <i>Journal of Physics D: Applied Physics</i> 53.1 (2019): 015114
2017	Cohen, S. Simon. "Contact resistance and methods for its determination." <i>MRS Online Proceedings Library (OPL)</i> 18 (1982): 361.
2018	Excerpts from Semiconductor Glossary
2019	Ng, Hong Seng. "Review on Methods for Trench MOSFET Gate Oxide Reliability and Switching Speed Improvement." <i>ECS Transactions</i> 27.1 (2010): 21

V. UNDERSTANDING OF LEGAL PRINCIPLES

19. I am not an attorney. I have been asked to provide opinions on the validity of the Asserted Claims of the Patents-in-Suit from the perspective of a POSITA.

A. Claim Construction

20. I have been provided certain legal principles relating to the construction of patent claims. I understand that “claim construction” is the interpretation of the meaning of patent claims. I understand that words of a claim are generally given

their ordinary and customary meaning, which is the meaning the term or phrase would have to a person of ordinary skill in the art at the time of the invention. I understand that both intrinsic and extrinsic evidence can be used to assist in understanding the meaning of a claim. Intrinsic evidence includes the claim language, language in other claims of the patent, the specification, and the prosecution record. I further understand that, unless required by the claim language or specification, claims should generally not be limited to embodiments in the specification, including preferred embodiments. I understand that extrinsic evidence, which consists of all evidence external to the patent and prosecution history including expert and inventor testimony, dictionaries, and learned treatises, may also be relevant to claim construction.

B. Invalidity Based on Prior Art

21. I understand that each claim of an issued patent is presumed to be valid. A party challenging the validity of a patent claim must present clear and convincing evidence to overcome the presumption of validity.

1. Prior Art

22. I understand that a patent or other publication must first qualify as prior art before it can be used to invalidate a patent claim.

23. I understand that a U.S. or foreign patent qualifies as prior art to an asserted patent if the date of issuance of the patent is prior to the invention of the

asserted patent. I further understand that a printed publication, such as an article published in a magazine, academic journal, conference proceedings, or trade publication, or U.S. or foreign published patent application qualifies as prior art to an asserted patent if the date of publication is prior to the invention of the asserted patent.

24. I understand that a U.S. or foreign patent qualifies as prior art to an asserted patent if the date of issuance of the patent is more than one year before the priority date of the asserted patent. I further understand that a printed publication, such as an article published in a magazine, academic journal, conference proceedings, or trade publication, or U.S. or foreign published patent application constitutes prior art to an asserted patent if the publication occurs more than one year before the priority date of the asserted patent.

25. I understand that, absent an assertion by the patentee otherwise, the date of invention is the filing date of the patent. I understand that a U.S. patent qualifies as prior art to the asserted patent if the application for that patent was filed in the United States before the invention of the asserted patent.

26. I understand that a system or device qualifies as prior art to the asserted patent if it was known or used in the United States prior to the invention of the asserted patent. I further understand that a system or device qualifies as prior art to

the asserted patent if it was in public use or on sale in the United States more than one year prior to the priority date of the asserted patent.

27. I understand that if a device was used by others in this country before the date of the invention, or if it was in public use in this country more than one year before the effective date of application, the device qualifies as prior art. I understand that, under either scenario, for a non-patentee's use to qualify as prior art, the purported use must have been available to the public. I understand that the following factors may be helpful in analyzing whether there was a public use: (1) the nature of the activity that occurred in public; (2) the public access to and knowledge of the public use; and (3) whether there was any confidentiality obligation imposed on persons who observed the use. I further understand that where a non-patentee's public use puts all the claimed features of an invention in the public's possession, this cannot be negated by evidence that other, unclaimed aspects of the non-patentee's device were not publicly available. Conversely, I understand that for a non-patentee's uses to constitute prior art, that use must have placed each of the claimed features of an invention in the public's possession. And, I understand that a non-patentee's secret or confidential uses do not invalidate later-filed patents.

28. I understand that a patent claim may be anticipated where, before the invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it. I further understand that when the

non-patentee's invention's "inner workings" are the essence of the invention, it is those "inner workings" that must not be suppressed or concealed in order for the invention to constitute prior art.

29. I also understand that prior art can include work by a prior inventor if that prior inventor: (1) conceived of the claimed invention before the conception date of the patentee, (2) was reasonably diligent in reducing the invention to practice from just prior to the conception date of the patentee, and (3) has not abandoned, suppressed or concealed the invention.

30. I understand that to qualify as prior art, a reference must contain an enabling disclosure that allows one of ordinary skill to practice the claims without undue experimentation.

31. I understand that documents and materials that qualify as prior art can be used to invalidate a patent claim as anticipated or as obvious.

32. I understand that invalidity must be shown by clear and convincing evidence. Furthermore, I understand that clear and convincing evidence means that it is highly probable that the fact is true.

2. Anticipation

33. I understand that, pursuant to 35 U.S.C. § 102, a claim of a patent is invalid for anticipation if, among other things, any of the following is true: (i) the invention was known or used by others in this country, or patented or described in a

printed publication in this or a foreign country, before the invention thereof by the applicant for patent, (ii) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country more than one year prior to the date of the application for patent in the United States, or (iii) the invention was described in another's United States patent or published patent application which issued from a patent application filed in the United States before the invention by the applicant for patent.

34. I understand that, once the claims of a patent have been properly construed, the second step in determining anticipation of a patent claim requires a comparison of the properly construed claim language to the prior art on a limitation-by-limitation basis.

35. I understand that a prior art reference "anticipates" an asserted claim, and thus renders the claim invalid, if all elements of the claim are disclosed in that prior art reference, either expressly or inherently (i.e., necessarily present), arranged in the same way as in the claim. I understand that, for inherent anticipation, it is required that the missing descriptive material is necessarily present in the prior art reference.

36. I understand that to anticipate an asserted claim, an allegedly anticipatory prior art reference has to have an enabling disclosure. I understand an

enabling disclosure describes the claimed invention in sufficient detail to enable a person of ordinary skill in the art to carry out the claimed invention.

37. I understand that a patent is anticipated if, before such invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it.

38. A patent claim is also anticipated if there is clear and convincing proof that, more than one year before the priority date of the patent, the claimed invention was: in public use or on sale in the United States; patented anywhere in the world; or described in a printed publication anywhere in the world. This is called a statutory bar.

39. I have written this declaration with the understanding that anticipation must be shown by clear and convincing evidence. I understand that clear and convincing evidence means that it is highly probable that the fact is true.

3. Obviousness

40. I understand that even if a patent is not anticipated, it is still invalid pursuant to 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person of ordinary skill in the pertinent art (henceforth, a “POSITA”).

41. I understand that a POSITA provides a reference point from which the prior art and claimed invention should be viewed. This reference point prevents one from using his or her own insight or hindsight in deciding whether a claim is obvious.

42. I also understand that an obviousness determination includes the consideration of various factors such as (1) the scope and content of the prior art, (2) the differences between the prior art and the Asserted Claims, (3) the level of ordinary skill in the pertinent art, and (4) the existence of secondary considerations (also called objective indicia of non-obviousness).

43. I understand that the test of obviousness is whether the claimed invention, as a whole, would have been obvious to one of ordinary skill in the art as of the date of the invention in light of the prior art.

44. I understand that a claim is not proved obvious merely by demonstrating that each of the elements was independently known in the prior art. I understand that most, if not all, inventions rely on building blocks long since uncovered, and claimed discoveries, almost of necessity, will likely be combinations of what is already known. I understand that it is important to identify whether a reason existed at the time of the invention that would have prompted a person of ordinary skill in the art in the relevant field to combine the known elements in the way the claimed invention does. I understand that the use of hindsight must be avoided when considering whether the alleged invention would have been obvious

to the person of ordinary skill in the art. In assessing obviousness, I have been instructed to consider the distortion caused by hindsight bias, guard against slipping into the use of hindsight, be cautious of arguments that rely upon after-the-fact reasoning, and avoid the temptation to read into the prior art the teachings of the invention in issue.

45. I understand that secondary considerations of non-obviousness (also known as objective indicia of non-obviousness) may include: (1) a long felt but unsolved need; (2) commercial success; (3) unexpected results; (4) industry praise; (5) licensing; and (6) copying by others. I also understand that there must be a relationship or nexus between any such secondary considerations and the claimed invention. I further understand that contemporaneous and independent invention by others is a secondary consideration supporting an obviousness determination.

46. I understand that any secondary consideration must bear a nexus to the claimed invention. Where the offered secondary consideration actually results from something other than what is both claimed and novel in the claim, there is no nexus to the merits of the claimed invention. I further understand that the patentee bears the burden of demonstrating that the relevant secondary indicia is attributable to the claimed invention, as opposed to other economic and commercial factors unrelated to the technical quality of the patented subject matter. I understand that a nexus is presumed where the secondary considerations are tied to a particular product which:

(i) embodies the claimed invention and (ii) is coextensive with the claimed invention. In analyzing whether a product is coextensive with the claimed invention, I understand that there is no requirement for a perfect correspondence between the claims and the product, and that the presumption of a nexus can still apply when unclaimed features present in the product amount to nothing more than additional insignificant features.

47. I further understand that, as a safeguard against hindsight bias, all secondary considerations of non-obviousness must be considered prior to reaching an obviousness conclusion.

48. I understand that an obviousness evaluation can be based on a combination of multiple prior art references. I understand that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but other times the nexus linking two or more prior art references can be based on the ordinary understandings available to a POSITA. I further understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may be supplied by the direction of the marketplace.

49. It is further my understanding that a proper obviousness analysis focuses on what was known or obvious to a POSITA, not just the patentee. Accordingly, I understand that any need or problem known in the field of endeavor

at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

50. I understand that whether a prior art reference “teaches away” from the claimed invention is a fact to be considered in determining obviousness. I understand that it is improper to combine references where the references teach away from their combination. However, I understand that the nature of the teaching is highly relevant and must be weighed in substance – a known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use. Furthermore, I understand that the prior art’s mere disclosure of more than one alternative does not constitute a teaching away from any of those alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed.

51. For an obviousness combination, obviousness must be proven by clear and convincing evidence such that a POSITA at the time of the alleged invention would have had a reason (or reasons) for combining the teachings of those prior art references to achieve the claimed invention, and that same POSITA would have had a reasonable expectation of success from combining those teachings.

VI. LEVEL OF ORDINARY SKILL IN THE ART

52. My opinions herein are based from my standpoint of a person of ordinary skill in the art at the time of invention of the ‘409 Patent, which I refer herein as a “POSITA.”

53. I understand that, for the purposes of proceeding, the ‘409 Patent is entitled to a priority date no later than December 4, 2006, the filing date of the application leading to the ‘409 Patent (U.S. Pat. Appl. No. 11/633,366).

54. I understand that Petitioner and its expert Dr. Liu have proposed that a POSITA “would have earned a Master’s degree in electrical engineering, and at least two years of relevant work experience in the field of integrated circuit design and manufacturing.” Pet. at 13; Ex. 1003 ¶ 52.

55. I have applied Petitioner’s proposed level of skill for my analysis. At the relevant time frame, I was a person of more than ordinary skill in the art during the relevant timeframe. However, I worked with and managed many people who fit the characteristics of the POSITA, and I am familiar with their level of skill.

VII. BACKGROUND OF TRENCHED MOSFETS

56. The ‘409 Patent is directed to improvements in the field of trench MOSFETs. ‘409 Patent, Title, Abstract, 1:5-67. In connection with my analysis and opinions herein, I will provide a brief description of the background of Trenched MOSFETs. This background information is based on my knowledge and

experience, but such background information regarding MOSFETs, including trench MOSFETs can be found in various publications. *See, e.g.*, Baliga, B. Jayant, *Fundamentals of Power Semiconductor Devices*, 2019, ISBN 978-3-319-93988-9 (“Baliga Fundamentals”); Lutz, Josef, et al. “Semiconductor power devices.” 2018, ISBN 978-3-319-70917-8 (“Lutz”); R. K. Williams, et al. “The Trench Power MOSFET: Part I—History, Technology, and Prospects,” in *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 674-691, March 2017 (“Williams”).

57. There are two primary types of transistors. A transistor is a semiconductor device that can act as a switch or amplifier. The first is the Bipolar Junction Transistor (BJT) and the second is the Field Effect Transistor (FET). Transistors have three (or more) terminals—the outputs/inputs of the transistor—which typically include gate, source and drain terminals. In a transistor, changing the voltage of the gate terminal (or base current) allows varying the flow of charge (e.g., current) between the source (or emitter) and drain (or collector) (e.g., turning “on” or “off” the current flow). In a Field Effect Transistor (FET) the region of a transistor where charge can flow between the source and drain is called the “channel” region. In general, MOSFETs often offer faster switching speeds, lower conduction losses, and simpler drive circuitry compared to other types of transistors.

58. Pure semiconductor material (e.g., silicon) has a conductivity which is greater than insulators (e.g., oxides) but less than conductors (e.g., metals). However, the conductivity of regions of semiconductors can be increased by adding “doping.” Doping is the process of introducing impurities into semiconductor material (e.g., silicon) to affect its electrical properties. N-type semiconductors are created by doping a semiconductor with an electron donor element (e.g., phosphorus or arsenic). N refers to the negative charge of an electron. P-type semiconductors are created by doping a semiconductor with an electron acceptor element (e.g., boron or gallium). P refers to the positive charge of a hole—a hole is quasiparticle denoting the lack of an electron at a position where one could exist in an atom or atomic lattice.

59. Thus, N-type and P-type doping introduce additional charge carriers (e.g., electrons or holes) and permit designers of transistor devices to control the flow of charge. For example, at a junction of P-type and N-type semiconductor materials (a so called p-n junction), current can only readily pass in one direction when forward biased—i.e., electrons pass from the N-type to the P-type material (and notional “current” goes in the opposite direction since current is the direction of positive charge, and electrons are negatively charged). A number of conventions have been adopted in the industry for referring to different magnitudes of doping. N⁺ doping is used to refer to material which has been more highly doped with

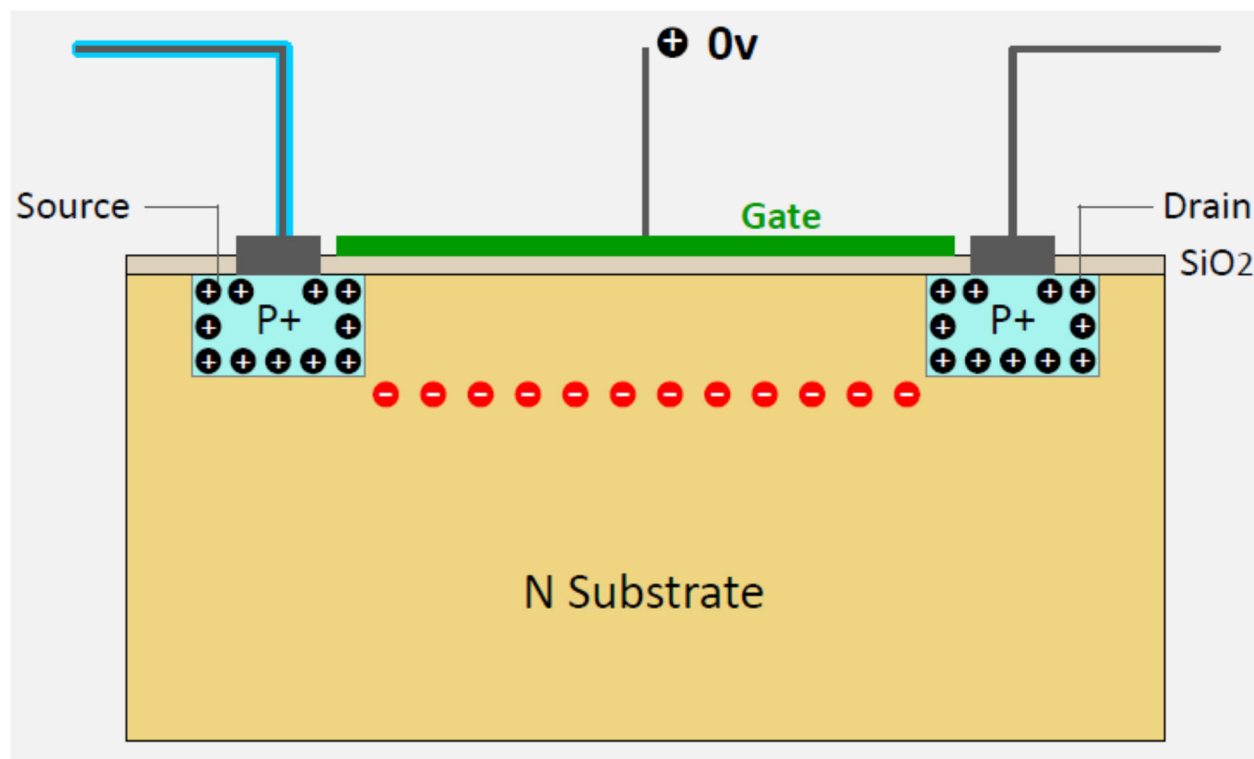
electron donor impurities than N-type doping, while N- doping is used to refer to material which is more lightly doped with electron donor impurities. Similarly, P+ doping is used to refer to material which has been more highly doped with electron acceptor impurities than P-type doping, while P- doping is used to refer to material which is more lightly doped with electron acceptor impurities.

60. The term “MOSFET” refers to a metal–oxide–semiconductor field-effect transistor. In MOSFETs, a gate (originally made of metal) is physically separated from the rest of the device via an insulative “oxide” layer (i.e., the “gate oxide”).¹ The voltage applied to the gate terminal controls the flow of charge in the channel region by using the “field effect”—i.e., the electric field created by the gate voltage attracts or repels charge carriers in or near the channel region. *Id.* In “N-Channel MOSFETs” the channel region charge carriers are electrons, while in “P-Channel MOSFETs,” the charge carriers are holes. *Id.* Some MOSFETs—called “depletion mode MOSFETs”—are designed so that charge will always flow in the channel unless a voltage is applied at the gate. Other MOSFETs—called “enhancement mode MOSFETs”—are designed so that charge will only flow in the

¹ Subsequent MOSFET devices have used different materials for the gate, particularly polysilicon—silicon crystal which is grown to be composed of many smaller crystals—as opposed to the monocrystalline silicon typically used for semiconductor devices. Despite no longer using metal for the gate, the term MOSFET has continued to be applied in the industry for such devices because they operate by the same mechanism as the original MOSFETs.

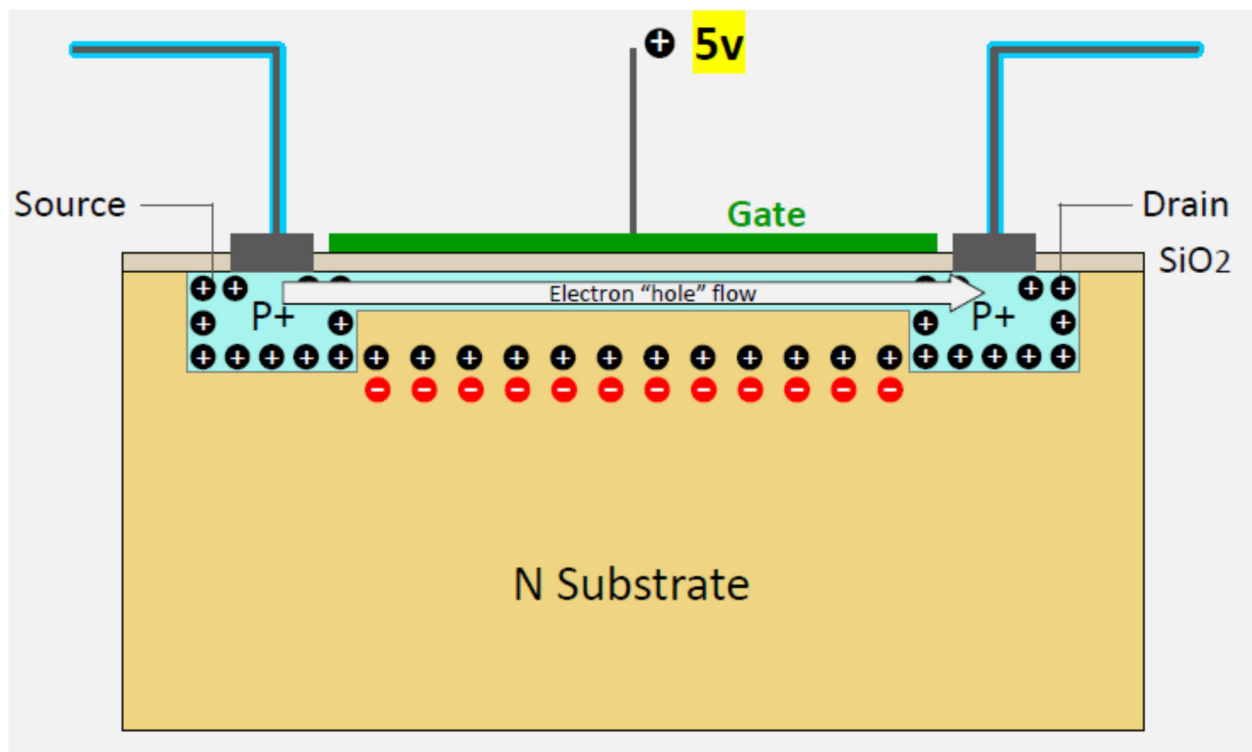
channel when a voltage is applied at the gate. The following exemplary figures depict the operation of a P-Channel enhancement mode MOSFET.

61. In the first figure, because this is a P-channel MOSFET, we have source and drain regions which are positively doped, to create a surplus of holes—positive charge carriers, whereas the body of the MOSFET has been negatively doped, creating a surplus of electrons—negative charge carriers. Because no voltage is applied to the gate terminal there is no change in the carriers in the N substrate, and hence charge flow is “blocked” by the p-n junctions formed between the source and substrate and the drain and substrate of this enhancement mode device.



62. In the next figure, we see that a voltage has been applied to the gate terminal. This repels electrons from the region below the gate, leaving behind

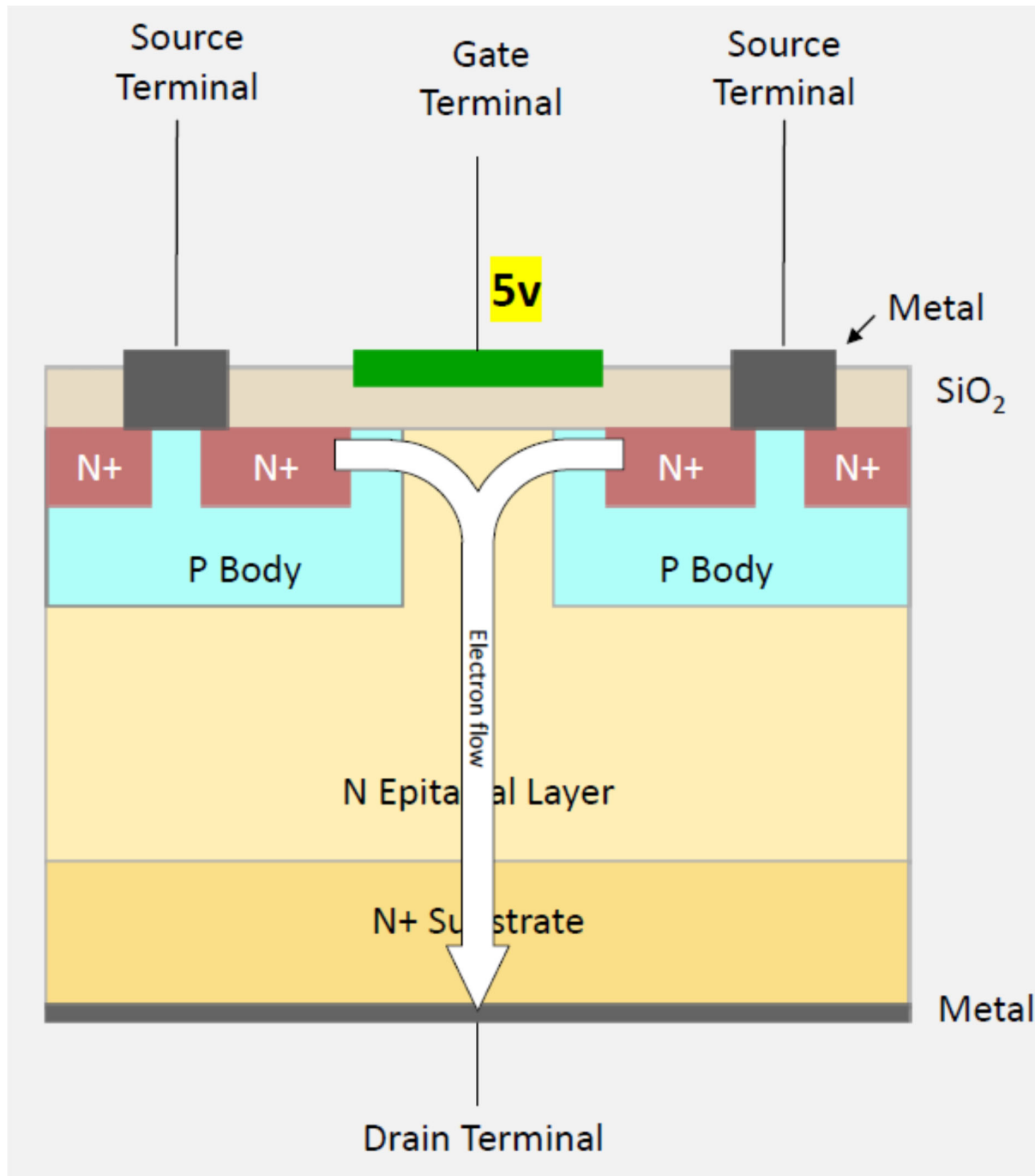
positive carriers and, as a result, below the channel region a depletion region (a region where substrate charge carriers have been forced away) is formed. Holes are attracted towards the gate into the channel region, creating a channel (also called an “inversion layer”) between the source and drain—a layer of holes near the gate between the two P⁺ regions. The channel carriers (holes) are the same as the carrier in the P⁺ source and drain regions. As a result, holes can flow (i.e., current) from source to drain.



63. If the gate voltage is removed, the device will return to its prior state (as illustrated in the first figure). Similar figures could illustrate the operation of N-Channel or depletion mode MOSFETs). For example, in an “N-Channel” MOSFET, the doping of each region would be reversed, and, electrons instead of holes would

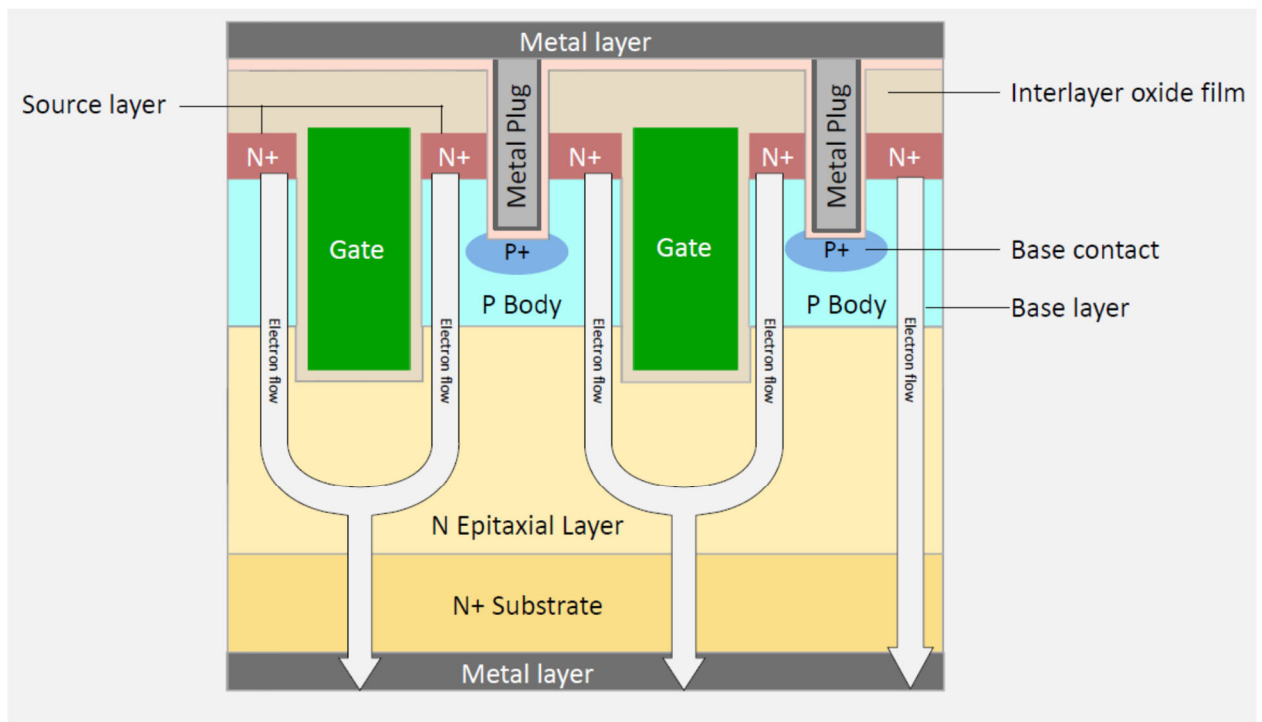
flow from source to drain when a channel is formed (and thus current would flow from drain to source). In a depletion-mode MOSFET, the channel region would typically have the same doping as the source and drain regions, and the channel would be present when there is no gate voltage, but the channel region would be depleted (preventing charge flow) when a voltage is applied to the gate. *Id.*

64. The above figures illustrate a lateral planar MOSFET, the original type of MOSFET—where the gate, source and drain are in a planar relationship, and the channel runs from source to drain along that plane. To increase the current carrying capability for devices such as power MOSFETs, other designs used vertical drain electrodes (i.e., with the source and gate electrodes on the top of the chip and the drain electrode on the bottom of the chip). By using a vertical drain, the MOSFET can increase density, improving current-handling capacity and reducing $R_{DS(on)}$ (discussed below). Note that in this device the channel is not formed in the “substrate” as it is in the lateral planar MOSFET, since the substrate is now part of the drain. The source and drain still must be doped oppositely from the channel region, which is often called the “body” in the vertical MOSFET. A MOSFET with a vertical drain configuration is illustrated in the following figure:



65. Trench MOSFETs present a further improvement on the vertical drain MOSFET, by including trenches for the gate material (e.g., gate trenches). As a result, the channels form vertically along the sides of the gates. Accordingly, a

trench gate MOSFET essentially makes a chip conduct the current vertically from one surface to the other, permitting packing millions of trenches on a chip. As a result, it allows for much smaller cell pitch (and hence higher cell density), thus providing further improved current-handling capacity and reduced $R_{DS(on)}$. The following figure illustrates a trench MOSFET also having source trenches filled with metal.



66. A number of properties are important to the function and performance of MOSFETs, particularly trench MOSFETs. One of the most important properties is on-state resistance, or $R_{DS(on)}$, which is the resistance when the MOSFET is in the ON state (i.e., charge flow is occurring). Subject to other constraints, MOSFET designers generally want to minimize $R_{DS(ON)}$ because such resistance results in

conduction losses, harming the efficiency of the device (e.g., everything else being equal, a higher $R_{DS(on)}$ will result in unwanted energy usage and heat generation). MOSFETs are often compared by on-resistance-area ($R_{DS(on)} \cdot A$), as generally the larger the chip size (surface area) of the MOSFET the smaller the ON resistance. Thus, a MOSFET design with a better on-resistance-area can fit a smaller $R_{DS(on)}$ in the same package size as a device with worse on-resistance area and a higher $R_{DS(on)}$. Thus, on-resistance-area is a way for comparing MOSFET designs independent of the particular package. *Id.* $R_{DS(on)}$ performance of a MOSFET can often be improved (i.e., lowered) by increasing device density.

67. Another important property of MOSFETs is called “threshold voltage” (“ V_{th} or $V_{GS(th)}$ ”), which is the minimum voltage at the gate where the device switches between the “ON” and “OFF” states (e.g. in an enhancement mode MOSFET, the voltage where the channel forms and meaningful charge flow can occur). The threshold voltage is between gate and “body”, but since the body is normally electrically connected to the source, the gate voltage is also usually given relative to the source. A high threshold voltage can be disadvantageous for a number of reasons. For example, if the design of a MOSFET has a threshold voltage which is too high, it can reduce switching speed, and even potentially render the MOSFET unusable for low-voltage situations by being above the supply voltage (e.g., the voltage of the device’s battery).

68. Another important property is referred to as “parasitic capacitance.” In particular, capacitance is the ability of a material to store an electrical charge. In the context of a MOSFET, particularly power MOSFETs, parasitic capacitance is important because it can result in switching losses—efficiency power losses that increase as switching speed increases. In essence, these effective capacitors within the MOSFET require energy to fill to allow the MOSFET to switch between OFF and ON states, but the energy in such capacitors is dissipated without useful activity when such state switching occurs. Unlike the conductive losses from higher RDS(on), parasitic capacitances are often made worse by increasing device density.

69. Another important property of MOSFETs are parasitic structures. Parasitic structures are interactions of parts of a MOSFET (e.g., doped regions) other than the desired operation of controlling the drain-to-source charge flow using gate voltage. In particular, the structure of MOSFETs often include multiple P-N and/or N-P junctions that can interact to form other transistors, particularly a parasitic “BJT” or bipolar junction transistor within a MOSFET. A BJT is a transistor formed by P-N-P or N-P-N arrangement of doped regions, where the amount of current supplied to the “base” terminal (physically connected to the middle doped region, e.g., the body in the vertical MOSFET) controls current flow between a collector on one end of the NPN/PNP and an emitter on the other end. *Id.*

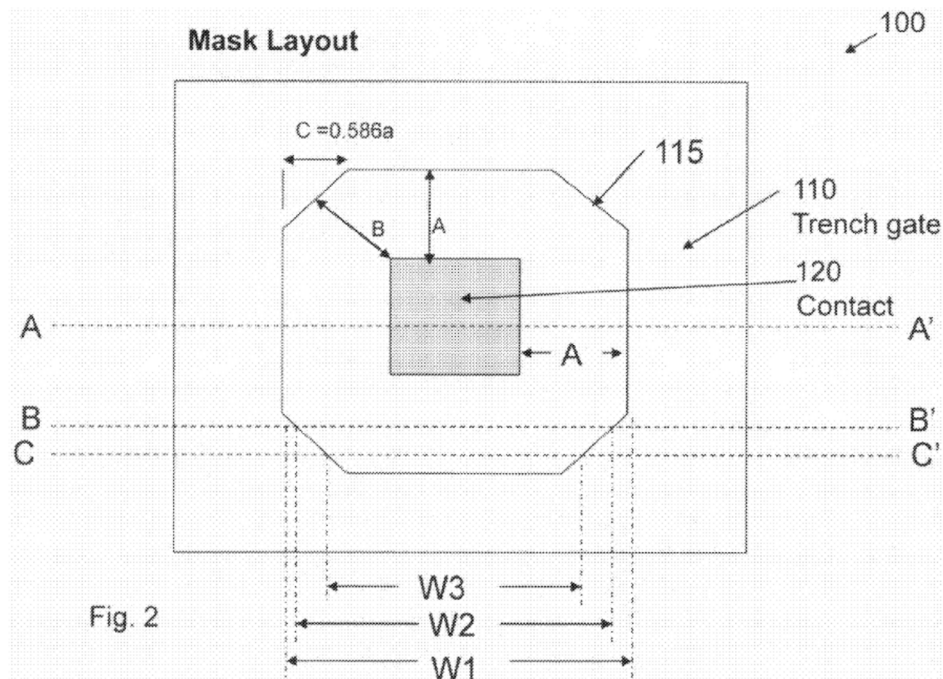
70. Related to the parasitic BJT is the phenomena of “avalanche breakdown” of a MOSFET. In the condition of avalanche breakdown, high drain-source voltages (e.g., transient voltages at turn-off that occur due to inductive loads or spike voltages) cause electrons to obtain sufficient kinetic energy to collide with atoms in the semiconductor lattice, ionizing those atoms to create holes and additional free electrons (i.e., impact ionization). Those released free electrons can, in turn, collide with other atoms in the lattice to create further holes and further free electrons, potentially resulting in an avalanching amount of charge flow. Breakdown voltage (BVDSS) refers to the reverse-bias drain to source voltage that will result in avalanche breakdown and avalanche current—even when the gate voltage would otherwise be in an “OFF” state and the channel is off. In this condition, referred to as the “breakdown region,” a small increase in drain-source voltage creates an exponential increase in current flow. In particular, when the drain-to-source voltage becomes high enough, the parasitic BJT (also called parasitic NPN) is turned on (i.e., a type of latch-up or short circuit), and a positive feedback mechanism of thermal runaway occurs where increasing temperature causes increasing current flow (even if VDSS is brought back under BVDSS). This can easily result in device destruction. Avalanche ruggedness is a property of MOSFETs that reflects the amount of avalanche current or avalanche energy a MOSFET can withstand prior to device destruction.

71. Each of these properties is important to the design and operation of a MOSFET, the applications a MOSFET is suitable for use in, and the operation of an electrical device using the MOSFET.

VIII. BACKGROUND OF THE '409 PATENT

72. The '409 patent is derived from U.S. Application Number 11/633,366, which was filed on December 24, 2006. The '409 Patent relates to trench MOSFETs with source contact trenches, where the layout of the trench gate surrounding the transistor cells as closed cells having truncated corners or rounded corners. '409 Patent, Abstract. The '409 Patent recognizes that prior art cell layouts for trench MOSFETs—which used conventional square shaped cells with square shaped contacts—had a problem. *Id.*, Fig. 1A. In particular, the problem of “parasitic bipolar NPN latch up”—a type of undesired current flow—was especially pronounced near the cells’ corners in the prior art devices. *Id.* at 1:15-20. The '409 Patent recognized that this problem was exacerbated by the significant variation in the distances between the contact and the gates in prior art, where the distances at the corners of the trench gate would be over 1.4 times farther from the source contact than the same measurement at the middle of the sides of the trench gate. *Id.*, Fig. 1A, 1:28-39. As a result, the non-uniform space between the square-shaped contact and the corners of the trench create weak points, resulting in low avalanche current and reduced device ruggedness. *Id.* at 1:45-57. The '409 Patent addressed this

problem by introducing an improved cell layout, having rounded or truncated corners to make the space between the trenched gate and the source contact more uniform, thereby enhancing device ruggedness. *Id.* at 2:3-7, Abstract, Figs. 2, 3. The embodiment of the invention with substantially square shaped closed cells with truncated corners is illustrated in Fig. 2:



Ex. 1001 ('409 Patent), Fig. 2

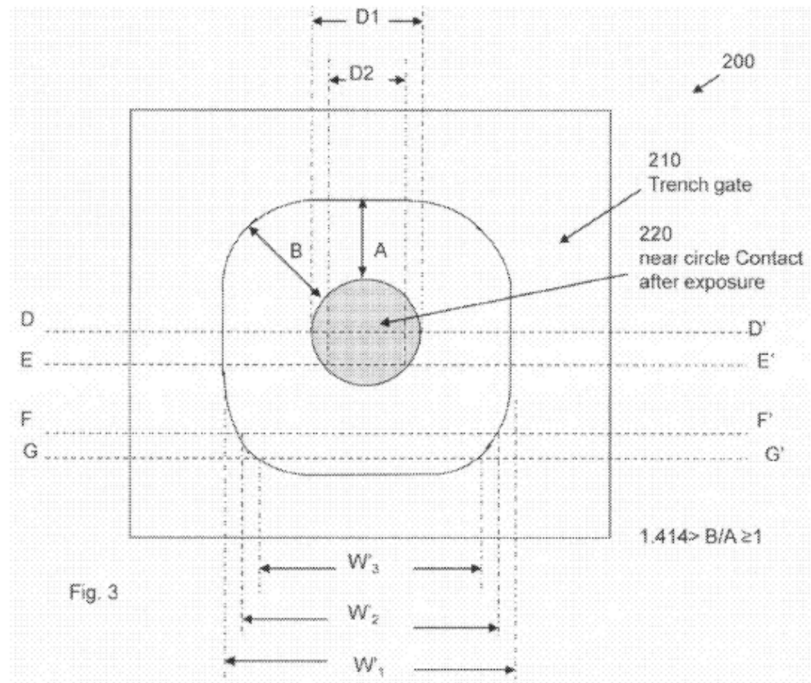
73. FIG. 2 illustrates a top view perspective of a closed cell configuration of a semiconductor power device of the '409 patent. The closed cell is surrounded by a trenched gate 110 having a truncated corner 115 such that the distance B between the truncated corners to the metal contact or a doped contact region 120 is substantially equal to the distance A between the edges of the contact region 120 to

the edges of the trenched gate. *Id.* at 3:34-39. That is, there is a uniform space between the surrounding trenched gate 110 and the metal contact or doped contact region 120. *Id.* at 3:39-40. Because the space is more uniform, device ruggedness is enhanced by eliminating the weak spots around the corners. *Id.* at 3:41-44, 4:15-17. Figs. 2A-2C illustrate cross-sections of the MOSFET of Fig. 2 at lines A-A', B-B' and C-C'.²

74. The '409 patent also discloses a manufacturing process that includes exposure through the mask such that the square contact becomes approximately circular shaped contact and truncated corners become smoother. *Id.* at 4:53-58. In that manufacturing process, truncated corners become rounded due to, at least, to resolution of 0.18-0.35 μm photolithography. *Id.* at 4:58-64. However, the '409 Patent does not assert that this is the only way to generate a MOSFET with closed cells having rounded corners. *Id.*

75. Fig. 3 of the '409 Patent illustrates a top-view perspective of an embodiment of a MOSFET with substantially square shaped closed cells having rounded corners:

² Fig. 2 also includes the text "Mask Layout." However, obviously a mask layout itself would not have cross-sections (i.e. as illustrated in Figs. 2A-2C). Rather, it is my opinion that the "Mask Layout" text simply indicates that the "truncated corner" embodiment of Fig. 2 uses a manufacturing process such that the cell structure of the final cell closely hews to the shape of the mask layout.



Ex. 1001 ('409 Patent), Fig. 3

Figures 3A-3D illustrate side-view cross-sections of the MOSFET of Fig. 3 at lines D-D', E-E', F-F' and G-G'.

IX. CLAIM CONSTRUCTION

A. “substantially square-shaped cells with rounded corners” ('409 Patent, cl. 1)

76. I understand that, in the preliminary response in this IPR, Patent Owner argued that “this term should receive its plain and ordinary meaning, *i.e.*: the cells have, from the top view perspective, largely or essentially the shape of a square (a shape that has four equal sides and four right angles) with all corners rounded (i.e. having a curved shape like a portion of a circle or oval).” Paper 6 at 4.

77. I understand that Petitioner and Dr. Liu propose that the term “rounded corners” be construed as “corners that are truncated by design and subsequently rounded by lithography.” Ex. 1003 ¶ 58.

78. I understand that, in the *Force MOS v. ASUSTek* district Court case, the Defendant proposed the same claim construction of “rounded corners” as Petitioner advances in this IPR. Ex. 2011 at 28. I understand that, in that case, Force MOS argued that “rounded corners” should be construed as “plain and ordinary meaning, i.e.: corners having a curved shape (i.e., like a portion of a circle or oval).”

79. I understand that, in its claim construction order in the *Force MOS v. ASUSTek* district Court case, the Court rejected Defendant’s proposed construction, and stated that:

Defendant incorrectly argues that the “rounded corners” must be truncated by design layout and then rounded. Contrary to Defendant’s argument, all of the cited portions are in passages that discuss the “process for manufacturing” or “manufacturing process.” ’409 Patent at 2:10–20, 4:53– 62. The Asserted Claim is an apparatus claim, and is not limited to products made by a particular process. ... Simply stated, the term “rounded corners” in Claim 1 is directed to what “rounded corners” are, not how the “rounded corners” were made.

Ex. 2011 at 30.

80. I understand that, in the Institution Decision in this IPR, the Board stated:

Based on the preliminary arguments and evidence, we disagree with Petitioner’s proposed construction requiring the corners to be

rounded via a particular process because it improperly imports a process of manufacture from the Specification into apparatus claims.

...

At this stage, we do not adopt Patent Owner’s proposed construction, which requires “all” corners being rounded from a “top view perspective.” The claims do not recite language directed to all corners, and we decline to import this particular embodiment into the claims based on the current record. At this stage, we need not resolve whether the corners need be rounded solely from a top view perspective because, as we discuss below, we preliminarily determine that the combination of Kobayashi and Hshieh teaches rounding from a top view perspective. See *infra* Section III.D.3. Rather, at this stage of the proceeding and on this record, we see no reason to determine that “substantially square-shaped cells with rounded corners” deviates from its ordinary and customary meaning, and we determine that, apart from our discussion above, no other claim construction analysis is necessary for our decision to institute an *inter partes* review. ... Thus, we preliminarily determine that the term does not include any process limitations and does not necessarily require all four corners to be rounded.

Paper 9 at 10-12.

81. In my opinion an express construction of “substantially square-shaped cells with rounded corners” is needed to address several issues in this IPR. In particular, in their anticipation ground over Kobayashi 196, Petitioner and Dr. Liu use their “truncated by design” construction to present a theory arguing that hexagon-shaped cells satisfy this limitation. Second, in their anticipation ground over Kobayashi 196, Petitioner and Dr. Liu alternatively argue that gate trench rounding of gate bottoms and openings—which is visible in the side view—satisfies this limitation. Third, in their obviousness grounds for Kobayashi 196 in view of

Hsieh, Petitioner and Dr. Liu argue that embodiments in Hsieh with two rounded or truncated corners motivate combining the references in the manner claimed. In my opinion, such theories are inconsistent with the appropriate construction of this term.

82. In my opinion, Force MOS is correct that “trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners” should receive its plain and ordinary meaning, *i.e.*: “the cells have, from the top view perspective, largely or essentially the shape of a square (a shape that has four equal sides and four right angles) with all corners rounded (i.e. having a curved shape like a portion of a circle or oval).”

83. First, I disagree with Petitioner’s construction that this term be construed as “corners that are truncated by design and subsequently rounded by lithography.” In my opinion, the term “rounded corners” has an established ordinary meaning in the field of semiconductors, and there is nothing that required deviating from that construction.

84. Moreover, the ’409 Patent discloses two distinct embodiments: cells with “truncated corner[s]” and cells with “rounded corner[s].” Ex. 1001 (’409 Patent) at 1:66-2:7. Figure 2 is an “improved cell layout” where the “trenched gate 100 [] has [] truncated corners.” *Id.* at 3:17, 3:32-35. Corresponding to that embodiment, claim 6 recites “said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with *truncated corners*.”

Id., cl. 6 (emphasis added). By contrast, Figure 3 is “another embodiment of this invention wherein a closed cell unit 200 of a MOSFET device includes trenched gate 210 ... and the trenched gate is formed with rounded corners 215.” *Id.* at 4:4-9. Similarly, claim 1 recites “trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with *rounded corners*.” *Id.*, cl. 1 (emphasis added). In my opinion, construing this term as proposed by Petitioner would conflate these distinct embodiments, and ignore the patentee’s intentional choice to recite claims with rounded corners (claim 2 and dependents) and a separate claim with truncated corners (claim 6).

85. I understand that, in support of their construction, Petitioner and its expert point to the ’409 Patent’s specification statement that “[t]he truncated corners are formed by design layout not process. It is by nature that truncated corners in layout becomes rounded after exposure due to resolution issue of 0.18~0.35 μm photolithography.” Ex. 1001 (’409 Patent) at 2:17-20; *see also id.* at 4:57-62; *see also id.* at 2:14-17, 2:58-60. However, those are passages that discuss the “process for manufacturing” or “manufacturing process.” Ex. 1001 (’409 Patent) at 2:10-20, 4:53-62. Dr. Liu also argues that “It was also well known in the art that the corners would become rounded as a natural or incidental result of lithography.” Ex. 1003 ¶ 56.

86. In my opinion, nothing in the specification of the ‘409 Patent indicates that the rounded corners of the invention can only be created by truncating corners in the design layout and subsequently rounding corners by photolithography. And, in my opinion, nothing in the language of claim 1 of the ‘409 Patent—which is an apparatus claim—would indicate to a POSITA that it is limited to products made by a particular process, as Petitioner proposes. Moreover, a POSITA would be well aware that rounded corners can be created in other ways. For example, rounded corners could be created by rounded corners in a mask design layout. A POSITA would also understand that rounded corners (or non-rounded corners) could be created from a mask without rounded/truncated corners by manipulating parts of the manufacturing process *after* mask design, such as: photolithography resolution, etch type for creating the trenches, the etch time and other etch parameters, the mask material, the exact shape of the mask, among other things.

87. Thus, to the extent that Dr. Liu is opining that Petitioner’s construction is necessary because some degree of rounded corners are inherent in *every* semiconductor device with etching created by photolithography, I disagree. As the prosecution history of the ‘409 Patent demonstrates (e.g. in the examiner’s application of the Pfirsch reference, Ex. 1002 at 237, 295, 302), as well as Dr. Liu’s own citation of the Hshieh reference (Ex. 1006 at 5:8), those of skill in the art understand that the plain and ordinary meaning of “rounded corners” in the field of

semiconductor design has a real meaning and is not something present in every semiconductor device that uses etching. That is, “rounded corners” means “corners having a curved shape (i.e., like a portion of a circle or oval). Ex. 2007 (dictionary definition of “round”, “rounded”) at 5.

88. Next, addressing the issue of “top view” versus “side view,” it is my opinion this limitation requires that the rounded corners be visible in the “top view.” In my opinion, this is essentially an issue of what structure in the claim must have the “rounded corners”—the cell (whose corners are only visible from the top view) or the trenched gate (whose bottom and opening corners are visible from the side view). The text of the language of claim 1 recites “A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein: said trenched gates surrounding said transistor cells as *closed cells constituting substantially square-shaped cells with rounded corners* ...” ‘409 Patent, cl. 1. Thus, the claim language itself is clear—it is the “closed cells” which must have rounded corners, not simply the trenched gates recited earlier in the claim.

89. That the “rounded corners” belong to the “closed cell” visible from the top view is also supported by the specification of the ‘409 Patent. Indeed, that the relevant view is the “top view” of the cell is demonstrated by the figures, which all

focus on the top view of the cell.³ Ex. 1001 ('409 Patent), Fig. 2, 3 (depicting top view of cells), at 1:20-1:33 (discussing “top view of a closed cell unit” of the prior art), at 3:32-34 (referring to “top view of a closed cell configuration of an improved semiconductor power device of this invention). In addition, all of the side view perspectives in the specification of the '409 Patent show an absence of rounding of the gate trench's bottoms or openings. *Id.*, Figs. 2A-2C, 3A-3D.

90. Moreover, the specification of the '409 Patent discloses that the primary purpose of the invention is improving device ruggedness by increasing the uniformity of the distances between the source contact and the gate trench. *Id.* at 1:18-57, 1:66-2:7; *see also id.* at 3:34-45, 3:55-4:3, 4:9-20, 4:33-51 (describing the preferred embodiments using various measurements of the top view perspective of Figures 2 and 3); *see also* Ex. 1002 ('409 File History) at 302, l. 29 (discussing “top view of closed cells” of the pending claims). That uniformity is demonstrated by the top view—i.e. comparing the top views of the embodiments of Figs. 2 and 3 to the top view of prior art Fig. 1A demonstrates that Figs. 2 and 3 have greater uniformity in the distance between source contact and gate trench. By contrast, a single side view perspective cannot demonstrate uniformity because it only shows

³ In particular, Figures 1A, 2, and 3 are cross-sectional top views because omit the overlaying source metal and interlayer oxide layers to permit view of the closed cell structure of the trench gates. *Compare* Ex. 1001 ('409 Patent), Fig. 1A (depicting gate trenches) *with* Fig. 1C (depicting “source metal” layer and inter oxide layer over gate trenches); *compare id.*, Fig. 2 *with* Figs. 2A-2D (same); *compare id.*, Fig. 3 *with* Figs. 3A-3D (same).

one cross-section of the cell. Moreover, that uniformity is not promoted by rounding the bottom corners or openings of trench gates visible from a side view—to the contrary it would make the distance between the gate and the source contact vary *more* (i.e. be less uniform), since the rounded bottom corners of the trench gates would be *further* away from the source contact than the middle of the sidewalls of the gate trenches, and the rounded openings of the trench gates would be *closer* to the source contact than the middle of the sidewalls of the gate trenches.

91. The idea that the plain and ordinary meaning of a MOSFET’s cell shape (also called the cell’s topology or layout) is defined from the top view perspective is also demonstrated by the file history of the ‘409 Patent and the references applied therein. For example, in the July 15, 2009 rejection, the examiner applied the Imam reference (U.S. Patent No. 6,867,083, Ex. 2013), stating that it discloses “a plurality of substantially square-shaped cells,” and citing to various figures in Imam, including figure 6. Ex. 1002 (‘409 File History) at 277. Imam itself refers to transistors in a “plurality of square shaped cells or plurality of cells” and states that it is illustrated in Fig. 6. Ex. 2013 (US6,867,083) at 5:35-39, Fig. 6. Fig. 6 of Imam illustrates that the square cells exist in the top view perspective. *Id.*, Fig. 6; Ex. 1002 at 279.

92. The idea that the plain and ordinary meaning of a MOSFET’s cell shape (aka topology or layout) is defined from the top view perspective is also

demonstrated by the Petitioner’s own asserted prior art references. For example, the Kobayashi patent states that:

“Referring to FIGS. 3A, 3B, 4A, and 4B, a UMOSFET chip may have various layouts of cells. In FIG. 3A, a plurality of square cells are arranged in a matrix. In FIG. 3B, the square cells are arranged in a matrix and the cells in adjacent lines are offset in position from each other. In FIG. 4A, a plurality of hexagonal cells are arranged. In FIG. 4B, a plurality of elongated cells are arranged in a column direction. As a matter of convenience, unit cells 101, 201, and 301 in each figure can be defined as structural units separated by trenches 106, 206, and 306 where gate electrodes are to be formed.”

Ex. 1005 at 6:25-35. Figs. 3A, 3B, 4A and 4B of Kobayashi are all *top view* perspectives. By contrast, when Kobayashi refers to rounding, it does not refer to the *cell’s* corners as being rounded, but rather refers to the “corners of each [gate] *trench* 6 at the bottom are rounded” and “In this event, corners of each *trench* 6 at an opening portion may also be rounded.” *Id.* at 7:57-60 (emphasis added). Thus, Kobayashi itself demonstrates that those in the field understand that a cell’s shape is defined from the *top view* perspective, and that the forms of rounding that can occur in the side view perspective are not rounding of the cell or its corners (but rather the gate trench). Other references in the field similarly show that cell shape is defined from the top view perspective. Ex. 2014 (Lutz) at 344-345 (depicting squares visible from top, and stating “cells are of square form and arranged in a square pattern”).

93. I also note that Petitioner’s position that rounding other than in the top view can read on this limitation is entirely inconsistent with its position that the rounding must be a result of “truncating” in the design layout followed by rounding by photolithography. In particular, side view rounding has nothing to do with truncation in design layout—the design layout (which is translated into the mask layout used for photolithography)—instead, it only controls the top view perspective since the light source used for photolithography creates a pattern on the top of the semiconductor.

94. Lastly, as to the issue of whether this limitation requires all or only some corners be rounded, it is my opinion that it requires that *all* corners of the substantially square shaped cell be rounded. As discussed above, the structure that has the “rounded corners” is the cell. Thus, it is clear from the claim language itself of “substantially square-shaped cells with rounded corners” that all corners are rounded. Nothing in that language conveys or suggests having some non-rounded corners. Indeed, the patentee could have readily used language indicating that less than all corners need be rounded (e.g. “with at least some rounded corners”). Moreover, the concept of a square with rounded corners consistently refers to a square with all corners being rounded. For example, another name for a substantially square shape with rounded corners is a “squircle.” For example, another name for a substantially square shape with rounded corners is a “squircle.” In definitions of

“squirele,” it is described as “a square *with slightly rounded corners.*” Ex. 2015 at 654. Such shapes are consistently depicted in the art as having all four corners rounded. *See e.g., id.*; Ex. 2016 at 3, Fig. 1 & caption. I am aware of no reference that uses the phrase “square with rounded corners” or “square shaped with rounded corners” to refer to a shape with some non-rounded corners.

95. Moreover, having all corners be rounded is required to achieve the ‘409 Patent’s purpose of increased uniformity of source contact to gate trench distance, discussed above. A cell that has fewer than all corners rounded would *decrease uniformity* rather than increase uniformity.

96. Thus, in my opinion, “trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners” should be construed as “Patent Owner argued that “this term should receive its plain and ordinary meaning, i.e., the cells have, from the top view perspective, largely or essentially the shape of a square (a shape that has four equal sides and four right angles) with all corners rounded (i.e., having a curved shape like a portion of a circle or oval).”

B. “substantially square-shaped cells with truncated corners” (‘409 Patent, cl. 6)

97. I understand that, in the preliminary response in this IPR, Patent Owner argued that “this term should receive its plain and ordinary meaning, *i.e.*: the cells have, from the top view perspective, largely or essentially the shape of a square (a

shape that has four equal sides and four right angles) with all corners truncated (i.e. being cut off).” Paper 6 at 9.

98. I understand that Petitioner and Dr. Liu propose that the term “truncated corners” be construed as “corners that are truncated by design layout.” Ex. 1003 ¶ 58.

99. I understand that in the Institution Decision in this IPR, the Board stated:

For reasons similar to those discussed above, we decline to adopt either of the parties’ proposed claim constructions. Rather, at this stage and on this record, we see no reason to determine that the term deviates from its ordinary and customary meaning, which does not include any process limitations and does not necessarily require all four corners to be truncated.

Paper 9 at 12.

100. It is my opinion that Patent Owner’s proposed construction of this term is correct, and that Petitioner’s proposed construction is incorrect. Indeed, all of the analysis applied above with respect to “rounded corners” applies to “truncated corners”. In particular, Petitioner’s construction is incorrect because there is nothing in apparatus claim 6 that indicates that this is limited to a particular process for making truncated corners. Indeed, Petitioner’s arguments are even weaker here since Petitioner argues that the manufacturing process causes truncated corners to become rounded. Neither Petitioner nor Dr. Liu explain how that can be reconciled in a way that makes the “truncated corners” limitation of claim 6 different from the

“rounded corners” limitation of claim 2 (i.e., they do not explain how the portions of the specification of the ‘409 Patent that they cite provides that “truncated corners” become rounded corners in claim 2 but somehow “truncated corners” do not become rounded in claim 6). Indeed, Dr. Liu suggests that the claimed “truncated corners” are in fact “rounded.” Ex. 1003 ¶ 60. In my opinion a POSITA would recognize that the intentional choice of reciting “rounded corners” in one independent claim and “truncated corners” in a different independent claim indicates that those limitations have different scopes (contrary to Dr. Liu’s argument).

101. And, like the “rounded corner” embodiment of Fig. 3 (discussed above), the truncated corner embodiment of Fig. 2 of the ‘409 Patent likewise is depicted and described from a top-view perspective. And, all the other reasons that a top-view perspective is required discussed with respect to “rounded corners,” apply equally to “truncated corners.”

102. And, like the discussion above concerning “rounded corners,” it is apparent from the claim language itself and the specification of the ‘409 Patent that all corners of the substantially square shaped cell must be truncated to satisfy this limitation. Indeed, if it did not, it would not satisfy the purpose of uniformity of distance between source contact and gate trench that is a primary focus of the ‘409 Patent. ‘409 Patent at 1:18-57, 1:66-2:7. Nor am I aware of any usage of the term

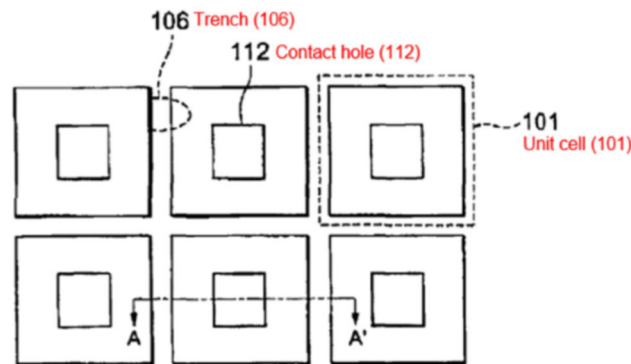
“square with truncated corners” to refer to a shape with fewer than all corners truncated.

X. THE CHALLENGED CLAIMS OF THE '409 PATENT ARE NOT ANTICIPATED AND ARE NOT RENDERED OBVIOUS

A. Overview of the Prior Art Relied Upon for the '409 Patent

1. U.S. Patent No. 6,888,196 (“Kobayashi 196”)

103. Kobayashi 196, entitled “Vertical MOSFET Reduced in Cell Size and Method of Producing the Same,” discloses conventional cell layouts such as square cells with square corners and square contacts. Ex. 1005, Fig. 3A.



Annotated version of Kobayashi’s Fig. 3A from Ex. 1003 ¶ 67

104. Although Kobayashi refers to “rounding,” it is directed to the rounding of the trenches’ opening and bottoms (which are visible in the side view), not the cells, which are visible in the top view. Ex. 1005 at 7:57-59. Indeed, Figure 6C, a sectional view (not a top view), clearly shows that it is the bottom of the trenches that is rounded and not the corner of the closed cell, which are visible from a top view:

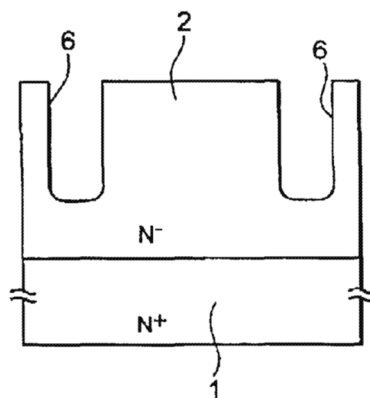
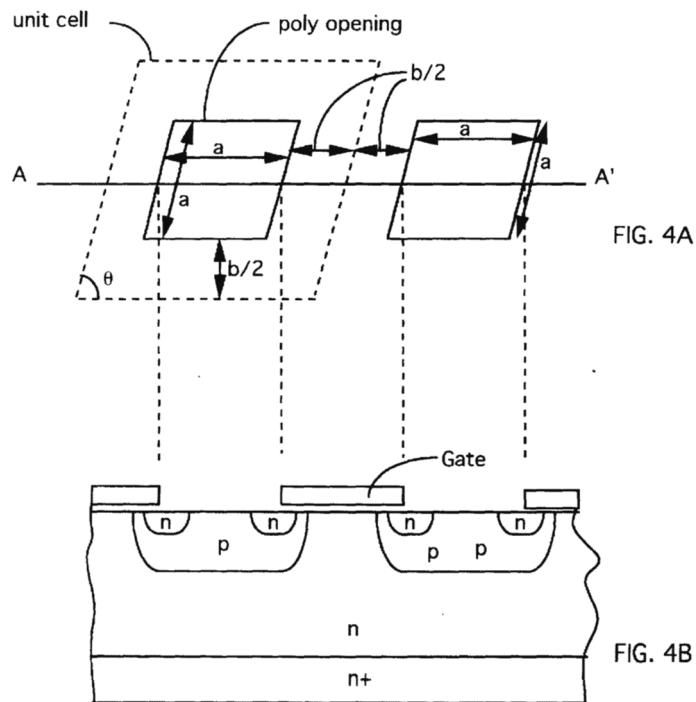


FIG.6C

2. U.S. Patent No. 5,763,914 (“Hshieh 914”)

105. Hshieh 914, entitled “Cell Topology for Power Transistors with Increase Packing Density,” discloses cell topology where packing density is increased by arranging cells as non-orthogonal parallelograms compared with that of conventional square cells. *See*, Ex. 1006 at 2:64-3:5, Figs. 4A, 4B. Hshieh is focused on the specific problems of its parallelogram configuration, disclosing rounding the two sharper corners of each nonorthogonal parallelogram, leaving two corners unrounded.



106. Unlike the '409 Patent which has both “trenched gates” and a “circular [source] trench contact,” most of Hshieh 914’s embodiments lack either of those. Ex. 1006 at 4B, 9D, 10B, 7:26-8:5. And Hshieh 914’s few embodiments that do have trench gates lack rounded or blunted corners. *Id.* And, all of Hshieh’s MOSFETs entirely lack trench source contacts. *Id.* By contrast, the claimed “circular trench contact” of the '409 Patent is a trench source contact because it is “filled with a contact metal plug” that is “connected to a source metal disposed on top of the circular trench contact.” Ex. 1001 ('409 Patent) cl. 1; *see also*, Figs. 2A, 3A (depicting “trench contact 120” connected to the “Source Metal” layer). In each embodiment of Hshieh 914, rather than having source metal connected to a metal-

filled trench penetrating into the semiconductor material's source and body regions, the source metal instead is in a planar relationship with the semiconductor material and contacts the semiconductor material through "source openings" in the oxide layer. Ex. 1006, Figs, 4B, 9D, 10B, 1:45-51, 3:38-42, 6:52-56, 7:2630, 7:56-60, cl. 21. Thus, not surprisingly, Hsieh 914's discussion of "rounding" is not concerned with problems relating to trenched source contacts. Rather, Hsieh 914 is concerned with the effect of the "three dimension diffusion effect" at the two sharper corners of Hsieh's non-orthogonal parallelograms. Ex. 1006 (Hsieh 914) at 5:3-17. Hsieh cites to Yilmaz (U.S. Patent No. 5,304,831, Ex. 2012) as explaining the three-dimensional diffusion effect. Ex. 1006 at 2:19-34.

3. Kikkawa

107. Petitioner relies on the article entitled "'A Quarter-Micrometer Interconnection Technology Using a TiN/Al-Si-Cu/TiN/Al-Si-Cu/TiN/Ti Multilayer Structure,'" by Kikkawa, T. et al, IEEE Transactions on Electron Devices, Vol. 40, No. 2 ("Kikkawa") as prior art in connection with claims 2 and 6. Claim 2 recites "a contact resistance reduction metal layer composed of a titanium (Ti) layer disposed above a top surface said contact metal plug and below a bottom surface of said source metal for reducing a contact resistance between said contact metal plug and said source metal." '409 Patent, cl. 2. Claim 6 recites, among other things, "said circular trench contact hole is filled with a metal plug composed of a Ti/TiN/W plug

to contact said source and body regions and said metal plug contacting a source metal disposed on top of said metal plug wherein said source metal layer composed of Ti/AlCu or Ti/AlSiCu all.” *Id.*, cl. 6.

108. Kikkawa is directed to “a TiN /Al-1 %Si-0.5%Cu/TiN / Al-1 %Si-0.5%Cu/TiN /Ti multilayer conductor” as “a quarter-micrometer interconnection for 256-Mb DRAM’s.” Ex. 1007 at 3. Notably, unlike the “trenched power device” of the ‘409 Patent (and recited in the preambles of claims 1 and 6), the DRAMs of Kikkawa refer to dynamic random access memory. Although at a high level, DRAMs contain MOS transistors, they are not power devices. Moreover, Kikkawa confirms that its interconnection structure was only tested in a non-functional mock-up of layered films, rather than any actual semiconductor having, for example, junctions of doped regions of semiconductor material. Ex. 1007 at 3 (describing construction of mockup under “Experiment) p. 7, Fig. 11 (showing mockup structure).

109. Kikkawa’s invention is directed specifically to a “layered conductor structure” for “quarter-micrometer interconnections” within DRAM. Ex. 1007 at 3. Kikkawa explains that aluminum conductors of prior art DRAM cells, had problems with stress-induced migration and electromigration, that its layered structure was intended to address. However, notably, Kikkawa is entirely silent as to “plugs.” A conductor (as that term is used in Kikkawa) is distinct from a plug, as a conductor

connects adjacent metal interconnect layers, whereas a plug is used for connecting a metal layer to the semiconductor material, and is typically deeper than a conductor. Moreover, Kikkawa only mentions structures using tungsten in the background discussion of other articles. Ex. 1007 at 3.

B. Claims 1, 3-5 Are Not Anticipated by Kobayashi 196

1. Claim 1

[1.a]. “said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;”

110. Kobayashi 196 does not disclose the claimed “cells constituting substantially square-shaped cells with rounded corners.” In particular, it is my opinion that Dr. Liu makes two flawed assertions for this limitation which I discuss in detail below.

111. First, Dr. Liu incorrectly points to the hexagonal cells in figure 4A of Kobayashi 196 as “square-shaped cells with truncated corners.” Ex. 1003, ¶ 68. But there is no support for such assertion. One, a POSITA would understand such hexagons to be hexagonal shaped cells, not substantially-square shaped cells. Squares have four sides, not six. Ex. 2007 at 6 (definition of square). Indeed, Kobayashi 196 itself classifies these cells as hexagonal: “[i]n FIG. 4A, a plurality of hexagonal cells are arranged.” Kobayashi 196 at 6:30-31. The “truncation” diagram that Dr. Liu and petitioner create to show how one could create a hexagon shape

from a square shape have no apparent factual basis, and, in any event, truncate far more than simply the corners of the theoretical square.

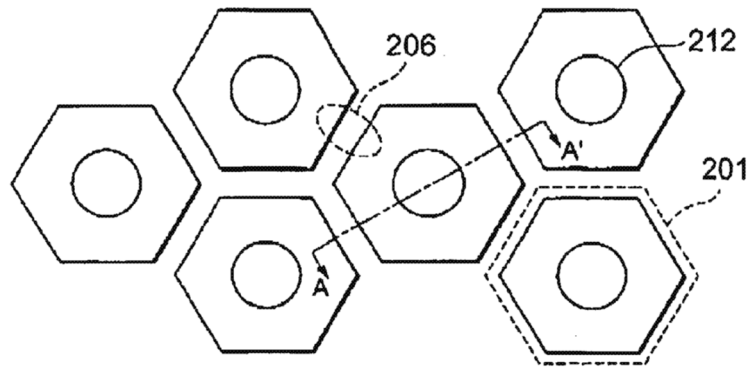


FIG. 4A

112. Second, in an apparently alternative theory, Dr. Liu incorrectly points to Kobayashi's disclosures of rounded trench bottoms and openings, visible in a side view, as the claimed "substantially square-shaped cells with rounded corners." Ex. 1003, ¶ 69. As discussed above, this argument is inconsistent with the appropriate construction of "substantially square-shaped cells with rounded corners," which requires that the *cells'* corners be rounded, not merely the *trench's* bottom or opening corners. And, as discussed, the cell's corners are visible in the top view, not the side view. This is plainly evident from the disclosures relating to Figure 3 of the '409 Patent—rounded corners 215 are only described and depicted as being present in the top-view perspective. '409 patent at Fig. 3, 4:4-13.

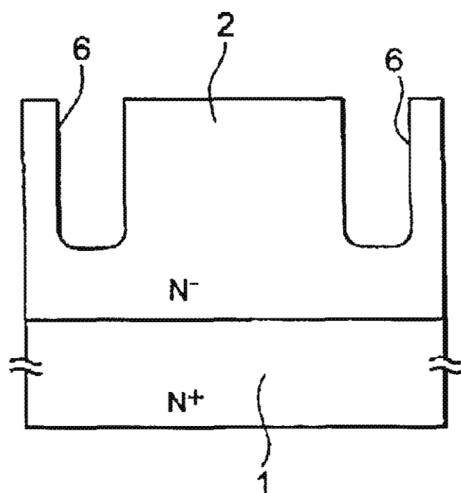
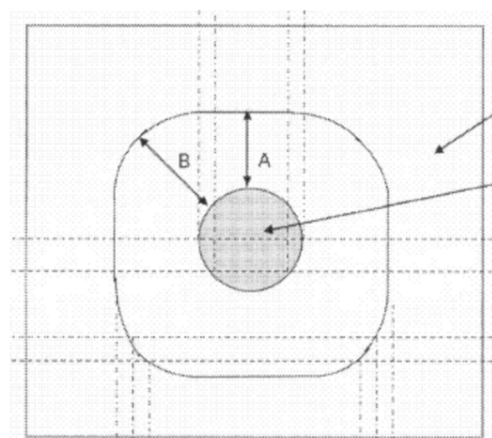


FIG. 6C

Kobayahi 196, Fig. 6C



'409 Patent, Fig. 3 (cropped)

113. Indeed, as discussed, the invention of the '409 patent solves the parasitic bipolar NPN latch up problem using the rounded cell corners as shown in figure 3 of the specification, not the rounded trench bottoms and openings as shown in figure 6C of Kobayashi 196. Solely rounding trench bottoms and openings would not serve the '409 Patent's goal of improving device ruggedness by improving the uniformity of the distance between the trenched gates and the source metal contact. '409 patent at 3:21-26.

114. Dr. Liu's argument is also inconsistent with the claim language, which recites "said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners." Viewed from the top-view perspective, the gate trenches plainly surround the transistor cells. '409 patent at Fig. 3, 2:45-47, 4:20-22 (depicting and describing that cell's source and

body regions surrounded by gates). But viewed from a side view perspective—as Dr. Liu’s alternative “rounded corner” theory requires—the gates do not surround the bottom of the cells’ source and body regions (which instead directly contact the N+ substrate layer). *Id.*, Figs. 2A-2D, 3A-3D. The same is true of Kobayashi’s Fig. 6C. That is, viewed from a side view, the gates do not “surround” the cell to form a square shape, as recited, and thus corners rounded in the side view are immaterial to limitation 1.a., which requires “substantially square-shaped cells with rounded corners.”

115. Also, as discussed above, Dr. Liu’s side view rounding theory is entirely inconsistent with Petitioner’s proposed construction of “rounded corners” requiring that the claimed rounding must be a result of “truncating” in the design layout followed by rounding by photolithography. In particular, such side view rounding has nothing to do with truncation in design layout. Ex. 1005 (Kobayashi) at 7:57-8:4 (describing the rounding as a result of “growing a sacrificial oxide film on a silicon surface in an oxygen atmosphere at about 1100° C. and thereafter removing the sacrificial oxide film by etching” or “heat treatment in a hydrogen atmosphere at about 950° C.”). The design layout (which is translated into the mask layout used for photolithography) only controls the top view perspective since the light source used for photolithography creates a pattern on the top of the semiconductor.

2. Claims 3-4

116. Claims 3-4 depend from claim 1, and therefore contain all of the limitations of claim 1. Because claim 1 is not anticipated (as discussed above), claims 3-4 are also not anticipated by Kobayashi.

3. Claims 5

117. Claim 5 depend from claim 1, and therefore contains all of the limitations of claim 1. Because claim 1 is not anticipated (as discussed above), claim 5 is also not anticipated by Kobayashi.

118. Moreover, claim 5 further recites “a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer.” Dr. Liu opines that this limitation is disclosed by Kobayashi because Kobayashi discloses *other measurements* (i.e. the source layer depth, P base layer depth, and gate trench width), and based on his analysis of the “apparent relative proportions of the MOSFET of Figure 5A.” Ex. 1003 ¶¶ 80-81. However, it is my understanding that, as a matter of law, a patent’s figures should not be used for measurements or precise proportions unless the patent states that the figures are to scale. Nothing in Kobayashi 196 states that its figures are to scale. Thus, it is my opinion that Dr. Liu’s analysis is improper, and fails to show that Kobayashi discloses claim 5.

C. Claims 2 and 6 Are Not Render Obvious by Kobayashi 196 in view of Kikkawa

1. Lack of Motivation to Combine

119. In my opinion, neither Petitioner nor Dr. Liu articulate an adequate motivation to combine Kikkawa and Kobayashi in the manner claimed in claims 2 and 6. In particular, they argue that they are in the same field of endeavor of each other and the ‘409 Patent. Ex. 1003 ¶ 98. However, in my opinion, the relevant field of endeavor for the ‘409 Patent and Kobayashi are trenched power MOSFETs. ‘409 Patent, Title, Abstract, 1:23-58, cls. 1, 6 (preamble), Ex. 1005 (Kobayashi) at Title, Abstract, 3:66-4:11. By contrast, as discussed above, Kikkawa is directed to improved conductors (components for connecting different metal interconnect layers) for DRAM. DRAM and Power MOSFETs, although both transistors, are very different types of semiconductor devices with different properties and pertinent design considerations. Petitioner’s argument is essentially the entire field of semiconductor design is a single field of endeavor, but it is my opinion that a POSITA would not understand the field of endeavor to be so broad.

120. Petitioner and Dr. Liu also argue that Kikkawa is pertinent to a problem solved by claims 2 and 6 of the ‘409 Patent. In particular, they point out that that the ‘409 Patent’s titanium layer is for “for reducing a contact resistance between said contact metal plug and said source metal” (as recited in claim 2). Ex. 1003 ¶ 99. But Kikkawa is not directed to reducing contact resistance, it is directed to a multi-

layer configuration of a conductor (having multiple titanium and aluminum layers) to reduce stress migration and electro migration. Ex. 1007 at 3 (investigating “a new layered conductor structure is investigated for quarter-micrometer interconnections”). Dr. Liu argues that reducing electro-migration and stress-migration would *eventually* reduce contact resistance if left on and used over an indeterminate period of time compared to a device also left on and used and which that suffered from electro-migration and stress-migration. Ex. 1003 ¶ 85.

121. However, in my opinion, Dr. Liu’s analysis is fundamentally flawed in numerous ways. Firstly, the capability of resisting electro-migration and stress-migration is distinct from *contact resistance*, which refers to the actual electrical resistance of the contact. Ex. 2017 (Cohen, S. Simon. "Contact resistance and methods for its determination." MRS Online Proceedings Library (OPL) 18 (1982): 361.) at 362 (“contact resistance then stands for the composite contributions [to resistance] originating at the interface and in the material underneath it.”); Ex. 2017 (semiconductor glossary) at 77 (“electromigration deleterious effect plaguing some metals, but in particular aluminum; physical motion of atoms away from the areas where current density is very high”). Moreover, the ‘409 Patents’ claims are directed to an apparatus, and thus “reduc[ed] contact resistance” is not appropriately measured by what *may* occur over an unspecified period of time if the device is used (e.g. if the device is allowed to operate under conditions and over a period of time

such that electromigration or stress-migration occurs). Rather, contact resistance is a property that can be measured from the contribution of the contact to resistance, regardless if the device is in on or off. Ex. 2017 at 367-374.

122. Moreover, Dr. Liu articulates no reason to believe that Kobayashi suffers from electro-migration or stress-migration that would benefit from combination to Kikkawa. *See also* Ex. 1005, Fig. 5A (element 16), 6:61-64, 9:30-33. In addition, Kikkawa does not state that simply having a single titanium layer (as Dr. Liu proposes in his combination) can reduce electro-migration and stress-migration. Instead, as discussed, Kikkawa identifies a particular, multi-layer conductor having multiple titanium and aluminum layers as theoretically having reduced electro-migration and stress-migration. Ex. 1007 at 3-4. Finally, Kikkawa provides no disclosure or suggestion for locating the titanium layer between a contact metal *plug* and a source metal of a MOSFET. And, as discussed, Kikkawa relates to *conductor* (i.e., for connecting distinct metal interconnect layers) in DRAM, not *plugs* (i.e. for connecting a metal layer to the active semiconductor material) in a MOSFET.

2. Claim 2

123. Claim 2 depends from claim 1, and thus contains all of the limitations of claim 1. Dr. Liu and Petitioner rely entirely on their arguments that Kobayashi 196 anticipates claim 1 in connection with their arguments that Kobayashi 196 in

view of Kikkawa renders obvious claim 2. Ex. 1003 ¶ 84. They make no argument that Kikkawa cures any of the deficiencies discussed above with respect to Kobayashi 196's failure to anticipate claim 1. Accordingly, Kobayashi 196 in view of Kikkawa fail to render claim 2 obvious for the same reasons discussed above for Kobayashi.

124. Additionally, as discussed above, neither Kikkawa nor Kobayashi disclose or suggest “a contact resistance reduction metal layer composed of a titanium (Ti) layer disposed above a top surface said contact metal plug and below a bottom surface of said source metal for reducing a contact resistance between said contact metal plug and said source metal” as recited in claim 2. In particular, as discussed, Kikkawa's structure is distinct from the structure recited in this claim (i.e. Kikkawa uses a repeated multi-layer structure and lacks plugs as claimed), and is directed to reducing electro-migration and stress-migration, not contact resistance. And, as discussed, a POSITA would not be motivated to combine Kikkawa and Kobayashi in the manner recited in claim 2.

3. Claim 6

- a) ***“said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with truncated corners;”***

125. Kobayashi 196 does not disclose the claimed “cells constituting substantially square-shaped cells with truncated corners.” In my opinion, Dr. Liu makes two flawed assertions for this limitation which I discuss in detail below.

126. Notably, although this limitation differs from limitation 1.a. of claim 1 by reciting “truncated corners” instead of “rounded corners,” Dr. Liu simply points to his analysis of limitation 1.a without any additional elaboration. Ex. 1003 ¶ 89. Thus, for all the same reasons I discuss above with respect to alleged anticipation of limitation 1.a by Kobayashi 196, Dr. Liu’s analysis of limitation 6.a likewise fails.

127. Indeed, applying the reasoning from Dr. Liu’s analysis of 1.a is even more problematic in a number of respects. Firstly, although one of Dr. Liu’s theories for limitation 1.a. relates to “trench corner rounding” of trench gate bottom corners and opening corners (Ex. 1003 ¶ 69)—visible only in a side view—Dr. Liu has no explanation how such “rounding” is anyway relevant to “truncated corners.” Ex. 1003 ¶ 89. As discussed above, the claimed “truncated corners,” like “rounded corners” are those of *closed cell*, not simply the trench gates, and the cell’s shape is defined from the *top view*. Moreover, even if the side view perspective is relevant, the cited portion of Kobayashi only discusses “rounded” corners, not “truncated”

corners. Ex. 1003 ¶ 69 (citing Ex. 1005 at 7:57-8:4). And such side view rounding has nothing to do with a design layout (if Petitioner’s construction of “truncated corners” is adopted), since the design layout only controls the features visible from at top view (i.e. where the photolithographic light source is located).

128. Dr. Liu’s “hexagon” theory also fails in this limitation. As discussed above in connection with “rounded corners” and limitation 1.a, Kobayashi’s hexagons are not “substantially square-shaped cells.” Ex. 1003 ¶ 68 (citing Ex. 1005, 6:3, Fig. 4A). Hexagons and squares are distinct topologies in the art, and hexagons (which have six sides) are not squares or substantially square shaped (as squares have four sides). Dr. Liu points to no evidence that anyone in the field refers to hexagons as squares (or substantially square shaped) with truncated corners. In my experience, I am aware of no one referring to hexagons as such.

b) 6[g]: “said circular trench contact hole is filled with a metal plug composed of a Ti/TiN/W plug to contact said source and body regions and said metal plug contacting a source metal disposed on top of said metal plug wherein said source metal layer composed of Ti/AlCu or Ti/AlSiCu alloys;”

129. As discussed above, neither Kikkawa nor Kobayashi disclose or suggest “said circular trench contact hole is filled with a metal plug composed of a Ti/TiN/W plug to contact said source and body regions and said metal plug contacting a source metal disposed on top of said metal plug wherein said source metal layer composed of Ti/AlCu or Ti/AlSiCu alloys.” In particular, as discussed,

Kikkawa's structure is distinct from the structure recited in this claim (i.e. Kikkawa uses a repeated multi-layer structure for conductors, rather than the plugs as claimed). Ex. 1007 at 3-4. And, as discussed, a POSITA would not be motivated to combine Kikkawa and Kobayashi in the manner recited in this limitation.

D. Claim 5 Is Not Rendered Obvious by Kobayashi 196 and the Knowledge of a POSITA

1. Lack of Motivation to Modify / Alter Kobayashi 196

130. Claim 5 depends from claim 1 and further recites “a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer.” Dr. Liu argues that this limitation would be obvious because “[a] POSITA would have understood that the diameter of the circular trench contact and the width as the trench 6 are substantially the same based relative proportions of the MOSFET of Figure 5A (annotated below)” and “Kobayashi teaches that the trench 6 can have a width less than 0.5 μm . Ex. 1003 ¶ 110. As discussed above, it is my understanding that, as a matter of law, a patent's figures should not be used for measurements or precise proportions unless the patent states that the figures are to scale. Nothing in Kobayashi 196 states that its figures are to scale. Thus, it is my opinion that Dr. Liu's analysis is improper.

131. Dr. Liu also argues that “a wider width [of the circular trench contact] would lead to wider total width of the unit cell for the Power MOSFET, and thus a larger unit cell area” which “would lead to less current drive and higher on resistance

per a given silicon area, making the device less economical to manufacture.” Ex. 1003 ¶ 112. Dr. Liu also notes that “wider source contact trench width in between the two gate trenches would dictate that the P+ base layer will be closer to its adjacent trench gate on both sides, and would lead to an increase of threshold voltage of the transistor due to the lateral diffusion of the P+ base layer.” *Id.* ¶ 113. Finally, Dr. Liu opines that a wider source contact trench would increase tungsten deposition time. *Id.* ¶ 114. Although there is generally a motivation to speed up the fabrication process, and to shrink feature sizes in the field of semiconductors, in my opinion, such reasons fail to articulate any reason why it would be obvious to use trench contacts with a diameter smaller than 1.0 micrometer. Moreover, Kobayashi already presents techniques for addressing the issue of the P+ base layer potentially increasing threshold voltage. Ex. 1005 at 5:44-49 (“the contact is formed to the depth different from the peak depth of the impurity concentration of the base layer” and “[t]hus, it is possible to suppress an influence upon a channel region by the impurity of the base contact layer formed at the bottom of the contact and to reduce the cell size without increasing V_t [i.e. threshold voltage].”) Thus, this is also not a reason for using circular trench contact smaller than 1.0 micrometer in diameter. Moreover, Dr. Liu fails to discuss any downsides of decreasing source contact diameter, i.e. greater difficulty in filling in Kobayashi’s plugs (especially where barrier layers are used, as in Kobayashi), and reduced current carrying ability of the

trenched source contacts. In short, in my opinion, Dr. Liu has failed to provide an explanation why a POSITA would be motivated to specifically try to use source contacts of the recited diameter, or why it would be predicate to do so.

2. Claim 5

132. Claim 5 depends from claim 1, and thus contains all of the limitations of claim 1. Dr. Liu and Petitioner rely entirely on their arguments that Kobayashi 196 anticipates claim 1 in connection with their arguments that Kobayashi 196 in view of Kikkawa renders obvious claim 52. Ex. 1003 ¶ 110. They make no argument that the knowledge of a POSITA cures any of the deficiencies discussed above with respect to Kobayashi 196's failure to anticipate claim 1. Accordingly, Kobayashi 196 in view of Kikkawa fail to render claim 5 obvious for the same reasons.

133. Additionally, claim 5 recites "a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer." Dr. Liu cites to no disclosure or suggestion in Kobayashi of such measurement.

E. Claims 1, 3-5 Are Not Rendered Obvious by Kobayashi 196 in View of Hsieh

1. Lack of Motivation to Combine

134. In Petitioner and Dr. Liu's motivation to combine analysis, they argue that:

“Kobayashi also discloses rounding corners of trenches in square cells. Ex. 1005, 7:57-8:4. In support of rounding the corners of the trenches in the square cells, Kobayashi cites to Sang-Gi Kim et al’s paper (Ex. 1012). In the cited paper, Kim et al discuss the benefits of trench corner rounding leading to higher breakdown voltage and lower leakage current—the same benefits discussed in the ’409 Patent. Ex. 1005, 7:57-8:4; Ex. 1012. Hsieh also discloses vulnerable punch-through weak points in the corners of square cell. Again this is due to an undesirable higher peak electric field being reached due to the same corner effect.”

Ex. 1003 ¶ 133.

135. In my opinion, this is conflating different types of rounding that occur in different places for different purposes, a problem which repeats throughout Dr. Liu’s analysis. *See, e.g.*, Ex. 1003 ¶ 135, 138, 140, 141 (conflating Kobayashi and Hsieh’s “rounding” and “corners” despite different rounding of different corners for different purposes).

136. As discussed, above in connection with Petitioner’s anticipation ground for claim 1 over Kobayashi 196, the passage at Ex. 1005 (Kobayashi 196), 7:57-8:4 does not discuss rounding of *cell* corners (i.e. rounding visible from the top view), but rather discusses rounding of the *trench bottom* and opening corners (i.e. rounding which is only visible from a side view cross-section). Similarly, the Kim reference also is addressed to side-view rounding of gate trench bottom and openings, not the rounding of corners of a closed cell. Ex. 1012 at 1, Fig. 1.

137. Unlike the rounding at issue in the ’409 Patent, or in Hsieh 914, the side-view rounding of gate trench corners at issue in Kobayashi 196 and Kim relate

primarily to gate “leakage.” Ex. 1012 at 1. In particular, in trench MOSFETs, the gate oxide can potentially become thinned in the corners. Ex. 2019 (Ng, Hong Seng. “Review on Methods for Trench MOSFET Gate Oxide Reliability and Switching Speed Improvement.” ECS Transactions 27.1 (2010): 21.) at 22. This is detrimental because the gate oxide is what prohibits direct current conduction from the gate to drain (in proper operation of a MOSFET the gate signal is intended to control source-to-drain charge flow via the field effect). At sufficient voltages, if the gate oxide is too thin, leakage can occur from the gate to the base layer via tunneling, resulting in unwanted power dissipation and potentially device destruction. *Id.* at 23; Ex. 2018 (semiconductor glossary) at 106 (“gate leakage a leakage current flowing across the MOS gate structure in the MOSFET; contributor to the possible overheating of the logic ICs.”).

138. Hsieh 914 uses rounding in a different way, and at a different place, and in a manner unrelated to the type and purpose of rounding in Kim and Kobayashi. In particular, Hsieh 914 is concerned with the three dimensional diffusion phenomenon, which causes short channel length in the corners of cells, particularly for Hsieh’s non-orthogonal parallelograms. Ex. 1006 at 2:19-34. I discuss the three-dimensional diffusion effect further below, but, suffice to say, that type of rounding is entirely unrelated to the side view trench corner bottom / opening rounding at issue in Kobayashi and Kim.

139. Moreover, in the ‘409 Patent, the purpose of rounded corners is to increase the uniformity of distance between the source contact and the gate. ‘409 Patent at 1:43-57, 2:3-7. Otherwise the corners form points where such distance is closer, resulting in weak points that occur at the four corners, resulting in low avalanche threshold and reduced device ruggedness due to the parasitic latch. *Id.*

140. Given the differences in the type and purpose of rounding at issue in Kim and Kobayashi from that at issue in Hsieh 914 and the ‘409 Patent, the discussion of “rounding” in Kim and Kobayashi would not motivate a POSITA to combine the rounding disclosed in Hsieh with Kobayashi 196.

141. Petitioner and Dr. Liu also argue that Hsieh 914 expressly teaches the benefits of rounding cell corners. Ex. 1003 ¶ 137. In particular, Petitioner and Dr. Liu argue that Hsieh “discloses the problems of vulnerable punch-through weak points in the corners of square cells, [which is] due to undesirable higher peak electric field being reached at the corners.” Pet. 57–58. They cite to Hsieh’s statement that “[i]n order to prevent the corner vulnerability where punch through weak points may be formed at the sharp corners due to a three-dimension diffusion effect . . . , the sharp corners [of the cells] can be either be blunted or rounded.” Ex. 1006, 5:3–8. However, in my opinion, as discussed further below, this analysis is incorrect for two major reasons. First, the entire limitation of claim 1 is “said trenched gates surrounding said transistor cells as closed cells constituting

substantially square-shaped cells with rounded corners” and Hsieh expressly teaches against square-shaped cells. Second, the “corner vulnerability” discussed in Hsieh—short channel length in corners resulting from the three dimensional diffusion phenomenon—is inapplicable to the structure of Kobayashi’s MOSFET. Each of these is discussed below.

142. It is my opinion that the disclosures of Hshieh 914 teach away from combining Hshieh 914 with Kobayashi 196 in the manner claimed (i.e. “trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners”). In particular, Hshieh 914 is directed to increasing the packing density of the cell topology of power transistors by using “*non-orthogonal parallelograms*.” Ex. 1006 (Hshieh 914), Abstract (emphasis added), 2:64-3:55, 4:32-5:2, Figs. 5A-5B, cls. 1, 8, 12, 21, 26, 30. By definition, non-orthogonal parallelograms are shapes which do not have right corners, and thus are not square shaped.

143. Hshieh specifically identifies square cell configurations as having disadvantageous packing densities that the invention is meant to overcome: “[t]he packing density of the transistor cell is improved with the parallelogram cell occupies less areas than *the regular square cell* having the same total channel width.” Ex. 1006 (Hshieh 914), Abstract (emphasis added); see also id. at 1:14-23 (identifying power MOSFETs having “cellular structure” with “square” topologies

as having increased “JFET resistance” and “on-resistance,” particularly as “cell size is reduced.”), Figs. 2C. By contrast, Hshieh touts its “non-orthogonal parallelogram” cell layout as providing “*packing density [that] is increased* with the same total channel width formed in a smaller cell area *when compared to that of square cells* as [] commonly used in the prior art such that the cell size can be further reduced without sacrificing the total channel width.” *Id.* at 2:64-3:5 (emphasis added).

144. It is my opinion that Dr. Liu mischaracterizes the respective problems that the '409 patent and the Hshieh 914 are trying to solve. Dr. Liu ignores important differences between the purposes of the “rounded” corners in Hshieh and the particular configuration of the '409 Patent having substantially square-shaped cells with rounded corners and a circular trench contact. The '409 Patent teaches that these two techniques address the problem of the prior art of non-uniform distances between trench gates and the source trench contact. In particular, as Figure 1C of the '409 Patent illustrates, the parasitic bipolar latch up problem that the patent is attempting to address originates in the P⁺ region at the bottom of the trenched source contact. '409 Patent at Fig. 1C, 1:42-45 (“The resistance R between the channel and the P⁺ region 25 is proportional to the space, i.e., the shortest distance between the metal contact region 15 and the trenched gates 20.”).

145. By contrast, Hshieh’s structure is fundamentally different. Nearly all of Hsieh’s disclosed embodiments lack trench gates. Ex. 1006, Figs. 6A-8B.

Indeed, none of the depicted or disclosed embodiments with rounded corners in Hsieh's specification have trench gates. *Compare* Ex. 1006, Figs. 6A-8B *with id.*; Figs. 10A, 10B (not depicting Figs. 10A and 10B as having rounded or blunted corners); *see also id.* at 3:58-4:28 (only describing Figs. 10A and 10B of having trenches).⁴ Moreover, all of Hshieh's embodiments entirely lack trenched source contacts. That is, unlike the '409 Patent which has both "trenched gates" and a "circular [source] trench contact," Hshieh only discloses embodiments with trenched gates without rounded corners and no trenched source contact. Ex. 1006 (Hshieh 914) at Fig. 4B, 9D, 10B, 7:26-8:5. In each of Hshieh's embodiments, rather than having source metal connected to a metal-filled trench penetrating into the semiconductor material's source and body regions, the source metal instead is in a planar relationship with the semiconductor material and contacts the semiconductor material through "source openings" in the oxide layer. *Id.* Figs, 4B, 9D, 10B, 1:45-51, 3:38-42, 6:52-56, 7:26-30, 7:56-60. Thus, not surprisingly, Hshieh's discussion of "rounding" is not concerned with problems relating to trenched source contacts. Rather, Hshieh is concerned with the effect of the "three dimension diffusion effect" at the two sharper corners of Hshieh's non-orthogonal parallelograms. *Id.*, 5:3-17.

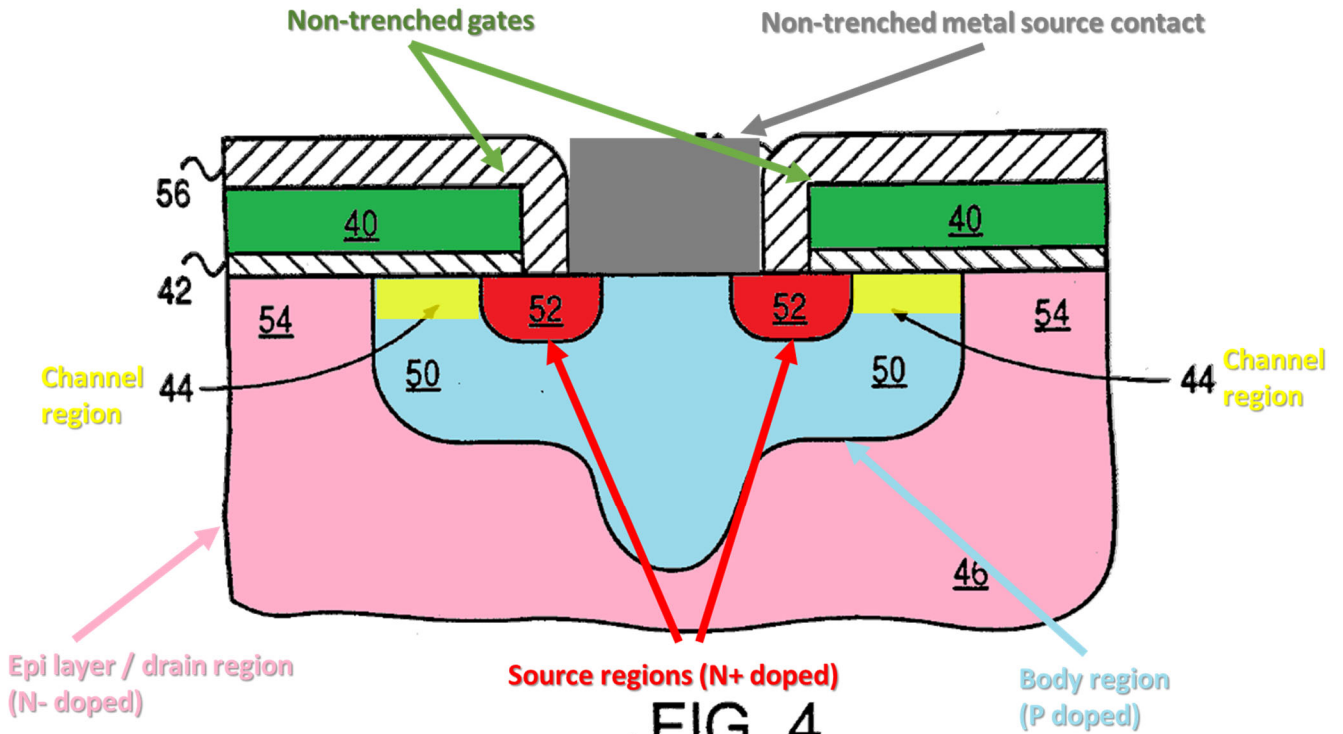
⁴ One claim of Hsieh does recite a trench gate with rounded corners. Ex. 1006, cl. 37. However, neither Hsieh itself, nor Petitioner, nor Dr. Liu, provide any explanation how rounded corners would be beneficial for a trench gate MOSFET.

Thus, Hsieh does not disclose or suggest that rounded or blunted corners are useful for a square topology.

146. Moreover, the “three dimensional diffusion phenomenon” is the specific motivation for using rounded or blunted corners in Hshieh—and is the only reason that Dr. Liu cites as motivation for combining Hshieh 914 with Kobayashi 196. Ex. 1003 ¶ 133 (citing 2:19-39). However, the three-dimensional diffusion problem identified by Hshieh 914 is inapplicable to the structure of Kobayashi 196’s MOSFET. In particular, as Hshieh 914 itself notes, the three dimensional diffusion phenomena arises in vertical draining double diffused MOSFETs (which Kobayashi is not). Ex. 1006 (Hshieh 914) at 1:36-55, 2:19-35, Fig. 1.

147. And, as the Yilmaz reference—which is discussed in the cited portion of Hshieh 914—discloses, the three dimensional diffusion phenomena becomes a problem in such MOSFETs because they rely on putting N⁺ source wells into P-doped bodies, such that the channel is largely horizontal/lateral, and charge flow only continues in the downward vertical direction (out the drain area) after the charge carriers leave the horizontal/lateral channel region. *Id.*; Ex. 2012 (Yilmaz) at 3:42-4:11, Figs. 3-4. Because the P-type dopants and doping process used in the body region of such MOSFETs have worse horizontal diffusion than the N-type doped source regions in the top-view corners of the cells, the result is that those cell corners have an excessively short channel length, which risks punch-through. *Id.* Yilmaz

does not actually provide a cross-section figure depicting the difference between the mid-cell cross-section of Fig. 4 and a short-channel cross section as would be found in the corners. However, the following annotated and modified versions of Fig. 4 of Yilmaz approximately depict this:



Ex. 2012 (Yilmaz), Figure 4 (annotated with colors, text and arrows),
showing cell cross-section outside of corners with standard length channel

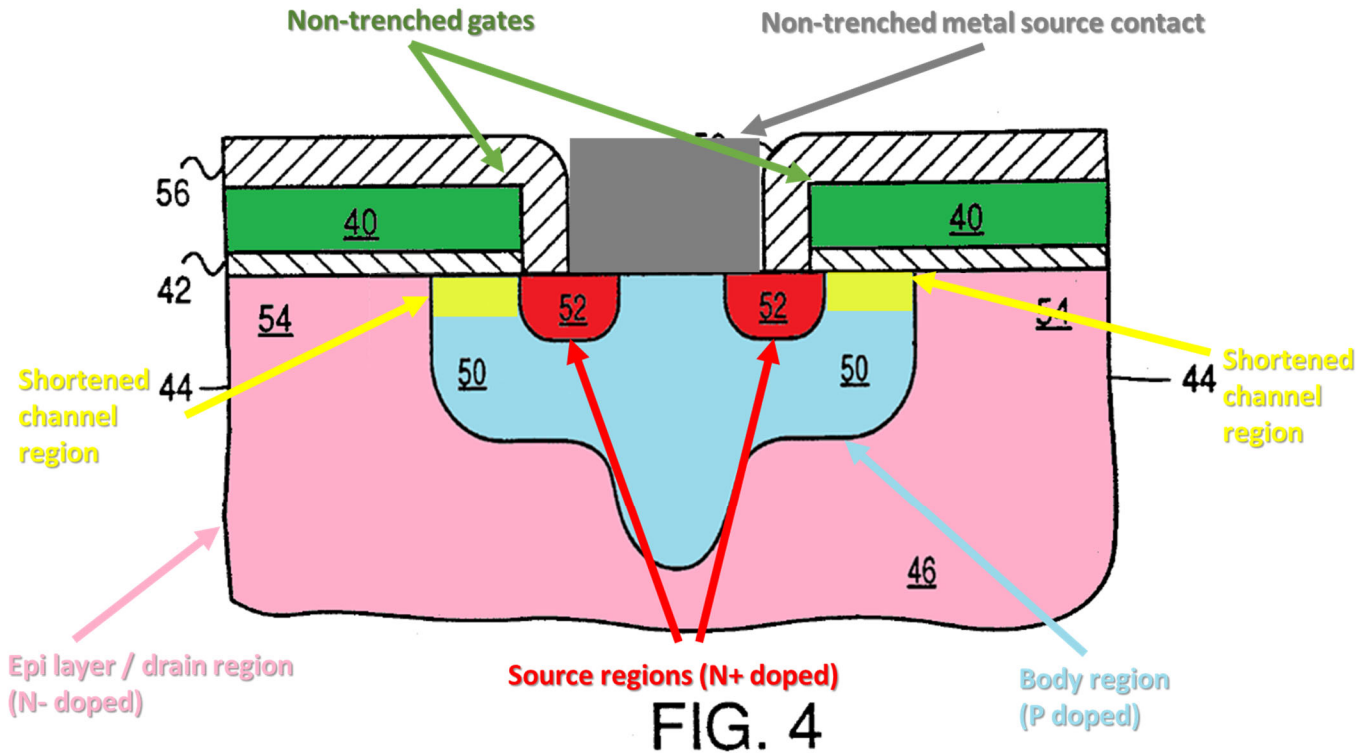


FIG. 4
Version of Ex. 2012 (Yilmaz), Fig. 4 (horizontally compressed cell; and annotated), showing mock-up of cross-section at cell corners with shortened channel length

148. As shown, in a double-diffused MOSFET such as Yilmaz (or Hsieh 914 Figs. 5A-9D), the channel (yellow) is horizontal, and is defined by the horizontal interface between the source region (red) and body region (light blue), and the horizontal interface between the body region (light blue) and the drain region (pink). Because of the reduced degree of diffusion of the p dopants that are used to create the p-doped body region at the corners, the result is a shortened channel length compared to the cross-section of the cell in the middle of the cell (and illustrated in the unmodified version of Fig. 4). Thus, Yilmaz (and Hsieh 914 by citing Yilmaz) discloses that using blunted corners reduces the three-dimensional diffusion problem in double diffused MOSFETs because the less-sharp corners allow the P-type

dopants to diffuse further horizontally, preventing the excessively short channel lengths of these horizontal channels in the corners. Ex. 2012 at 4:12-428; Ex. 1006 at 2:19-34.

149. However, Kobayashi 196 is a *trench*-gate and a *trench*-source MOSFET, not a horizontal/lateral gate and channel vertical-drain doubled diffused MOSFET. Kobayashi 196, Abstract, Fig. 5A. One of the defining characteristics of a trench-gate MOSFET is that the channel is in the *vertical* direction along the *trenched* gate. Ex. 2014 (Josef, et al. "Semiconductor power devices." 2018, ISBN 978-3-319-70917-8 at 345 (§ 9.2)); *see also* Ex. 1005 at 7:1-10, Fig. 5A. Thus, the differences in *horizontal* diffusion between P-type and N-type dopants are irrelevant to channel length of Kobayashi's *vertical* channel. Dr. Liu provides no explanation: (1) why he believes Kobayashi 196 has a shorter channel length in the top-view cell corners; or (2) why he believes the problem of three-dimensional diffusion shortening channel length identified in Hshieh 914 has any relevance to Kobayashi 196's structure. Indeed, because Kobayashi 196 has both source trenches and gate trenches, there are no horizontal/lateral boundaries between the source and body regions or the body and drain regions, only vertical/depth-wise boundaries. This is illustrated in the below annotated version of Fig. 5A of Kobayashi:

and describes the creation of the body layers and source layers as occurring without any photoresist mask within the cell region (i.e. any mask that would define horizontal boundaries between the source, body, or drain regions):

[P]atterning by photolithography is required in an area except a cell region. Subsequently, implantation of B (boron) or BF₂ (boron fluoride) ions and heat treatment in an oxygen atmosphere or a nitrogen atmosphere are carried out to form the P-type base layer 9 to the depth shallower than the trenches 6 ... [T]he N⁺-type source layer 10 is formed on the surface of the P-type base layer 9 by implantation of As ions and heat treatment in a nitrogen atmosphere.

Id. at 8:21-46, Fig. 7A. Because the channel length of Kobayashi's vertical channel is determined by the vertical depth of implantation and diffusion of the source layer and body region, the problem of the three dimensional diffusion phenomena—the differential rates of horizontal diffusion of P and N type dopants in corners—is irrelevant to the structure, design, or fabrication of Kobayashi 196's MOSFET. Accordingly, in my opinion, Dr. Liu has not identified any motivation to combine Hsieh 914's corner rounding/blunting that has any applicability to Kobayashi 196.

151. Even if Hsieh 914 had any applicability to Kobayashi 196, in my opinion, Dr. Liu does not articulate an adequate reason for selecting the *circular* contact embodiment of Kobayashi 196 with the *square* cell layout of Kobayashi 196 and the rounded corners of Hsieh 914. Indeed, the '409 Patent reflects the inventors' discovery of the novel benefits of increasing the uniformity of distance between the gate trenches and metal source contact in a trench-gate MOSFET with

trenched MOSFETs. Dr. Liu’s conclusion that a person of skill in the art would somehow happen upon a combination having more uniform source-contact to gate-trench distance, therefore, appears to be the result of arbitrary selection of various unrelated features of the two references.

2. Claims 1, 3-5

152. To the extent that Petitioner and Dr. Liu are relying on any of their anticipation theories for Kobayashi 196 (i.e. any rounding allegedly disclosed in Kobayashi rather than Hsieh) in connection with this ground, such theories fail for the same reasons discussed above in connection with Petitioner’s anticipation ground for limitation 1.a over Kobayashi 196 alone.

153. And, as discussed, a POSITA would not be motivated to combine Kobayashi 196 and Hsieh in the manner recited by limitation 1.a, as neither reference suggests or discloses “trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners.”

3. Claim-5

154. For claim 5 for the ground of Kobayashi 196 in View of Hsieh, Dr. Liu and Petitioner rely entirely on their arguments that claim 5 is anticipated by Kobayashi. Ex. 1003 ¶ 110. Thus, their arguments that claim 5 is rendered obvious by Kobayashi 196 in View of Hsieh fails for the same reasons discussed in connection with the ground for anticipation over Kobayashi 196.

F. Claims 2 and 6 Are Not Rendered Obvious by Kobayashi 196 in View of Hsieh and Kikkawa

1. Lack of Motivation to Combine

155. As discussed above in connection with Petitioner's and Dr. Liu's ground for obviousness of claim 1 over Kobayashi 196 in view of Hsieh, Petitioner's motivation to combine theory is flawed in numerous ways. Claims 2 and 6 depend on claim 1. Petitioner's and Dr. Liu's motivation to combine theory for this ground apparently relies on the motivation to combine theory for Kobayashi 196 in view of Hsieh, as neither Petitioner nor Dr. Liu provides any separate motivation to combine analysis for the combination of the three references together. Ex. 1003 ¶ 145. Accordingly, Petitioner's and Dr. Liu's motivation to combine arguments for this ground fail for the same reasons discussed above.

156. Additionally, as discussed above in connection with Petitioner's ground for obviousness of claim 2 and 6 over Kobayashi 196 in view of Kikkawa, Petitioner's and Dr. Liu's motivation to combine theory is flawed in numerous ways. Petitioner's and Dr. Liu's motivation to combine theory for this ground apparently relies on the motivation to combine theory for Kobayashi 196 in view of Kikkawa, as neither Petitioner nor Dr. Liu provides any separate motivation to combine analysis for the combination of the three references together. Ex. 1003 ¶ 145.

2. Claims 2 and 6

157. As discussed, a POSITA would not be motivated to combine Kobayashi 196 and Hsieh in the manner recited by limitation 1.a, and thus would not be motivated to combine Kobayashi 196, Hsieh, and Kikkawa in the manner claimed by claims 2 or 6.

158. And, as discussed, a POSITA would not be motivated to combine Kobayashi 196 and Kikkawa in the manner recited by claims 2 and 6, and thus would not be motivated to combine Kobayashi 196, Hsieh, and Kikkawa in the manner claimed by claims 2 or 6.

G. Claim 5 Is Not Rendered Obvious by Kobayashi 196 in View of Hsieh, Kikkawa, and the Background Knowledge of a POSITA

1. Lack of Motivation to Combine

159. As discussed above in connection with Petitioner's and Dr. Liu's ground for obviousness of claim 1 over Kobayashi 196 in view of Hsieh, Petitioner's motivation to combine theory is flawed in numerous ways. Claim 5 depends on claim 1. Petitioner's and Dr. Liu's motivation to combine theory for this ground apparently relies on the motivation to combine theory for Kobayashi 196 in view of Hsieh, as neither Petitioner nor Dr. Liu provides any separate motivation to combine analysis for the combination of the three references together with the background knowledge of a POSITA. Ex. 1003 ¶ 156. Accordingly, Petitioner's motivation to

combine arguments for this ground fail for the same reasons discussed above regarding claim 1 over Kobayashi 196 in view of Hsieh.

160. Additionally, as discussed above in connection with Petitioner's and Dr. Liu's ground for obviousness of claim 5 over Kobayashi 196 alone, Petitioner's and Dr. Liu's theory for motivation to modify Kobayashi 196 in the manner recited by claim 5 is flawed in numerous ways. Petitioner's and Dr. Liu's motivation to combine for claim 5 for this ground apparently relies on the motivation to combine theory for Kobayashi 196 alone, as neither Petitioner nor Dr. Liu provides any separate motivation to combine analysis for the combination of the three references together with the knowledge of a POSITA. Ex. 1003 ¶ 145. Accordingly, Petitioner's and Dr. Liu's motivation to combine arguments for this ground fail for the same reasons discussed above regarding claim 5 over Kobayashi 196 alone.

2. Claim 5

161. And, as discussed, a POSITA would not be motivated to combine Kobayashi 196 and Hsieh in the manner recited by limitation 1.a, and thus would not be motivated to combine Kobayashi 196, Hsieh, Kikkawa and the background knowledge of a POSITA in the manner claimed by claim 5.

162. And, as discussed, a POSITA would not be motivated to modify Kobayashi 196 based on the background knowledge of a POSITA in the manner

recited by claim 5, and thus would not be motivated to combine Kobayashi 196, Hsieh, and Kikkawa in the manner claimed by claim 5.

XI. CONCLUSION

163. I currently hold the opinions that I have expressed in this declaration. However, my analysis may continue, and I may acquire or receive additional information or insights that may result in revised or supplemental observations or opinions.

164. I understand this declaration will be used as evidence in a contested case before the PTAB.

165. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 or Title 18 of the United State Code, and that such willful false statements may jeopardize the validity of the '409 Patent..

I declare under penalty of perjury that the foregoing is true and correct.

Executed: September 12, 2024



Dr. Dean Neikirk