US007656244B2

(12) **United States Patent**
McCorquodale et al.

(10) **Patent No.: US 7,656,244 B2**
(45) **Date of Patent: *Feb. 2, 2010**

(54) **DISCRETE CLOCK GENERATOR AND TIMING/FREQUENCY REFERENCE**

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(73) Assignee: **Mobius Microsystems, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 5 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **12/036,165**

(22) Filed: **Feb. 22, 2008**

(65) **Prior Publication Data**

US 2008/0150645 A1 Jun. 26, 2008

Related U.S. Application Data

(63) Continuation of application No. 11/384,973, filed on Mar. 20, 2006, now Pat. No. 7,358,826, which is a continuation-in-part of application No. 11/232,407, filed on Sep. 20, 2005, now Pat. No. 7,456,699, and a continuation-in-part of application No. 11/084,962, filed on Mar. 21, 2005, now Pat. No. 7,227,423, and a continuation-in-part of application No. 11/085,372, filed on Mar. 21, 2005, now Pat. No. 7,227,424, said application No. 11/232,407 is a continuation-in-part of application No. 11/084,962, filed on Mar. 21, 2005, now Pat. No. 7,227,423, and a continuation-in-part of application No. 11/085,372, filed on Mar. 21, 2005, now Pat. No. 7,227,424.

(60) Provisional application No. 60/555,193, filed on Mar. 22, 2004.

(51) **Int. Cl.**
H03B 5/12 (2006.01)

(52) **U.S. Cl.** ..... **331/179**; 331/117 FE

(58) **Field of Classification Search** ..... 331/1 A, 331/2, 8, 10, 11, 16–18, 25, 36 C, 36 L, 57, 331/117 R, 117 FE, 117 D, 173, 175, 177 R, 331/177 V, 179, DIG. 2
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

7,227,423 B2 * 6/2007 McCorquodale et al. 331/179

* cited by examiner

Primary Examiner—David Mis
(74) *Attorney, Agent, or Firm*—Nancy R. Gamburd; Gamburd Law Group LLC

(57) **ABSTRACT**

In various embodiments, the invention provides a discrete clock generator and/or a timing and frequency reference using an LC-oscillator topology, having a frequency controller to control and provide a stable resonant frequency, which may then be provided to other, second circuitry such as a processor or controller. Frequency stability is provided over variations in a selected parameter such as temperature and fabrication process variations. The various apparatus embodiments include a sensor adapted to provide a signal in response to at least one parameter of a plurality of parameters; and a frequency controller adapted to modify the resonant frequency in response to the second signal. In exemplary embodiments, the sensor is implemented as a current source responsive to temperature fluctuations, and the frequency controller is implemented as a plurality of controlled reactance modules which are selectively couplable to the resonator or to one or more control voltages. The controlled reactance modules may include fixed or variable capacitances or inductances, and may be binary weighted. Arrays of resistive modules are also provided, to generate one or more control voltages.

53 Claims, 44 Drawing Sheets

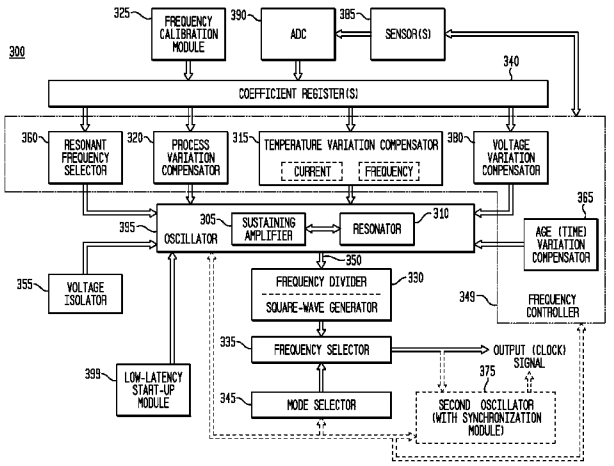


FIG. 1

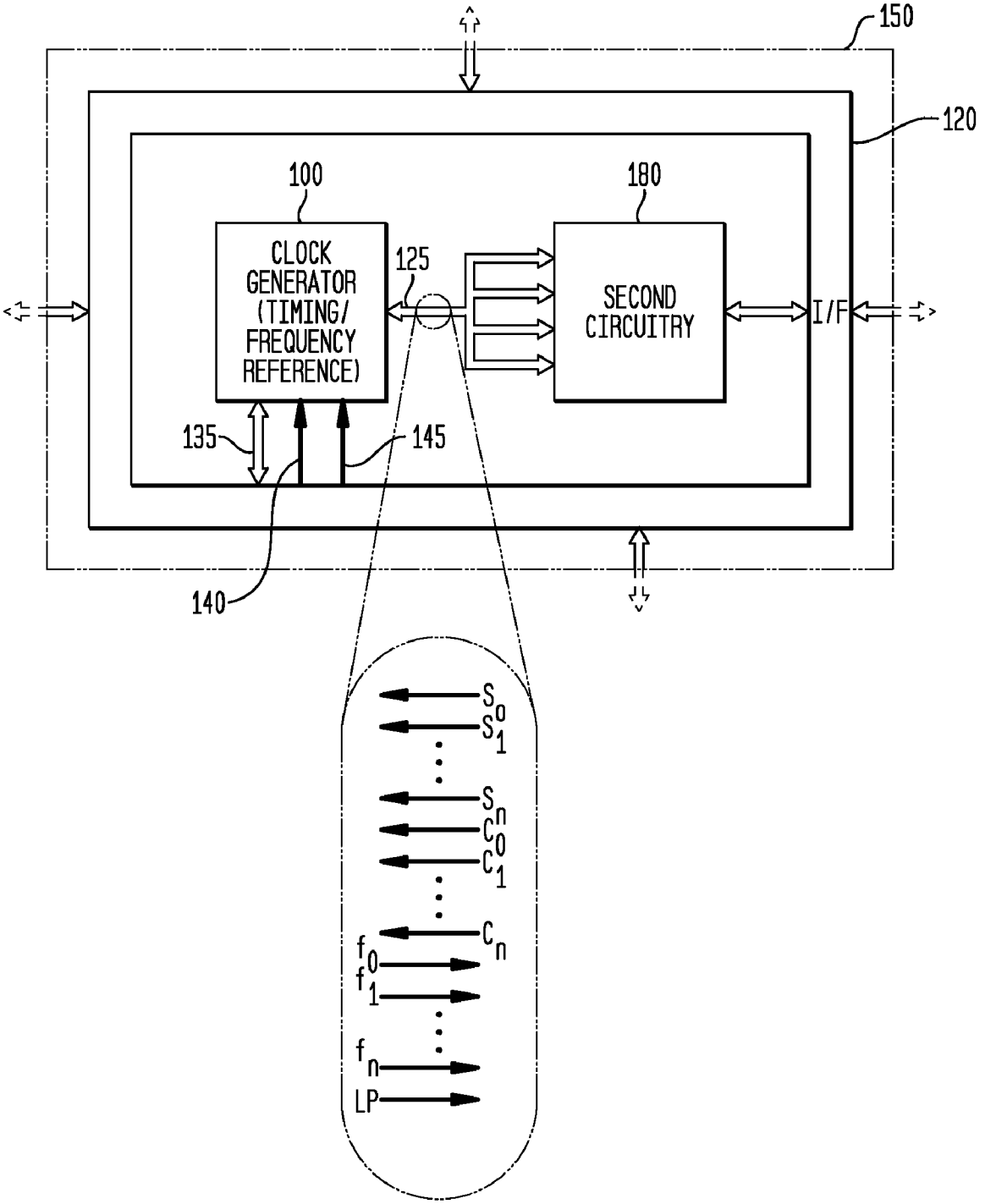
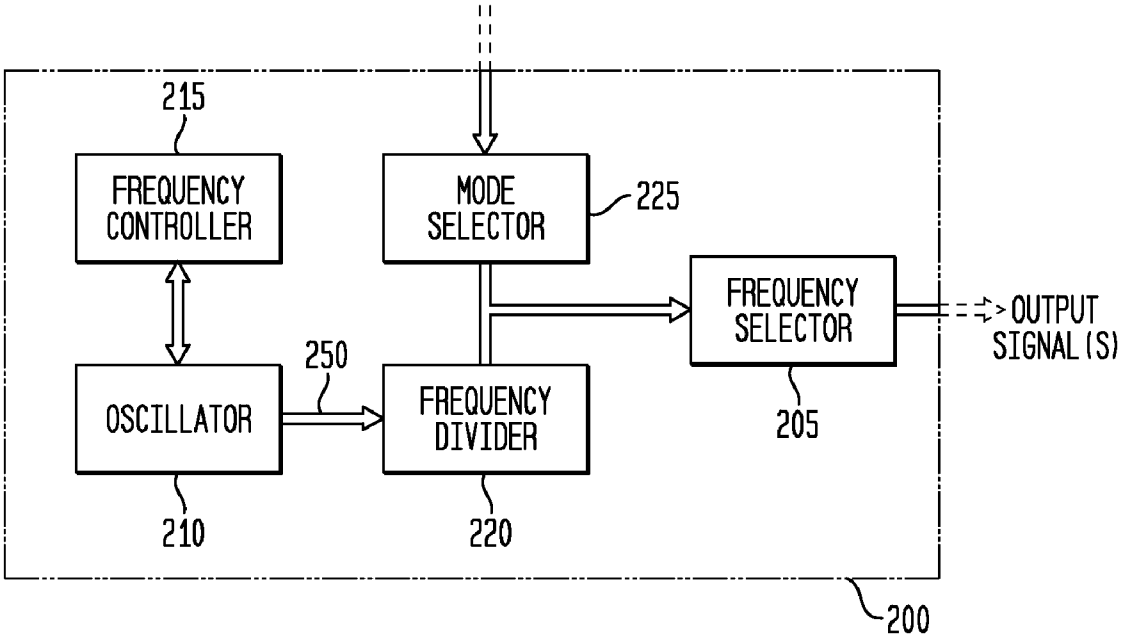

150
120
100
180
CLOCK GENERATOR (TIMING/ FREQUENCY REFERENCE)
125
SECOND CIRCUITRY
I/F
135
145
140
S_0
S_1
S_n
C_0
C_1
C_n
f_0
f_1
f_n
LP

FIG. 2


215
FREQUENCY CONTROLLER
MODE SELECTOR
225
FREQUENCY SELECTOR
OUTPUT SIGNAL(S)
250
OSCILLATOR
FREQUENCY DIVIDER
205
210
220
200

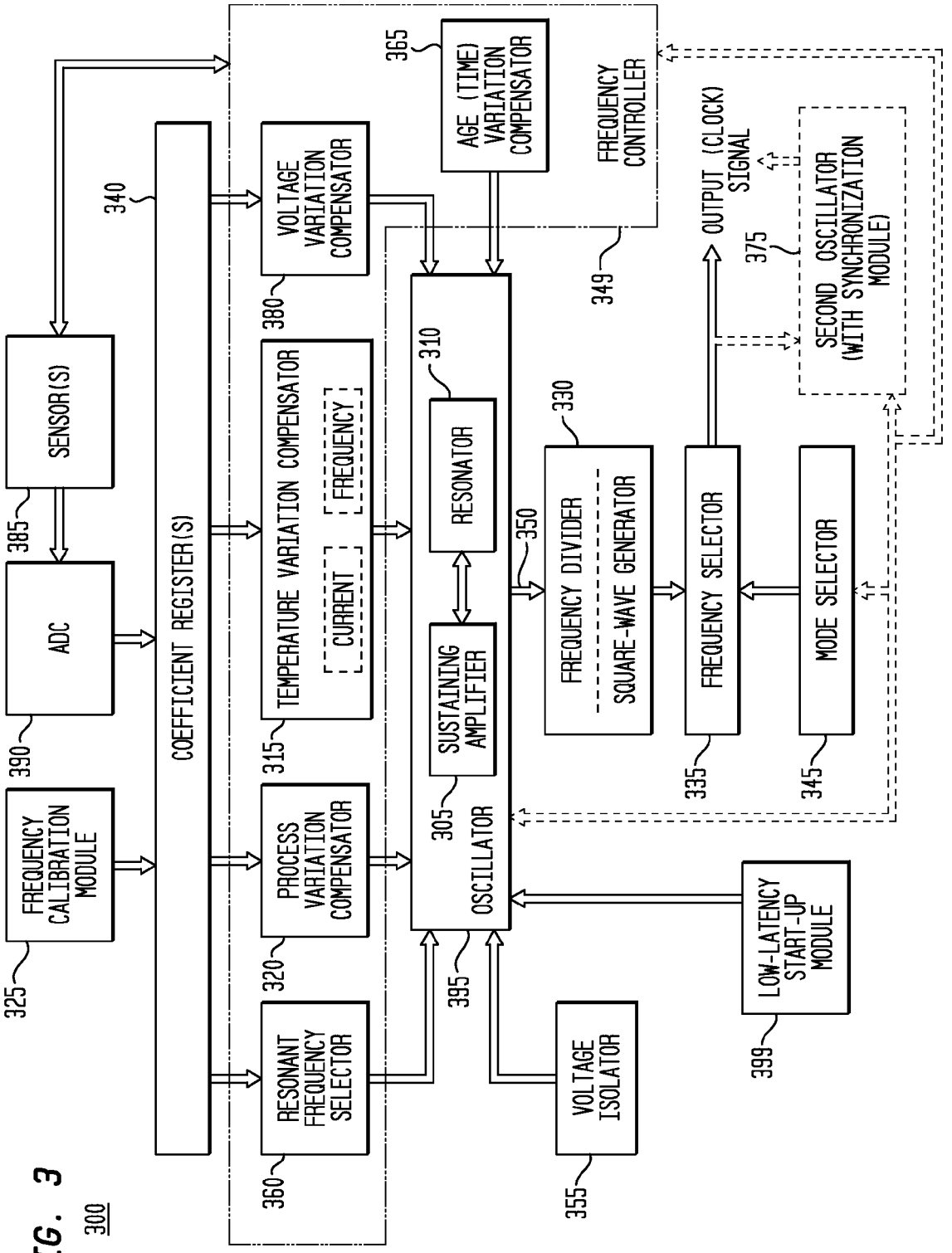

SENSOR(S)
385
ADC
390
FREQUENCY CALIBRATION MODULE
325
COEFFICIENT REGISTER(S)
340
VOLTAGE VARIATION COMPENSATOR
380
TEMPERATURE VARIATION COMPENSATOR
CURRENT
FREQUENCY
315
PROCESS VARIATION COMPENSATOR
320
RESONANT FREQUENCY SELECTOR
360
AGE (TIME) VARIATION COMPENSATOR
365
RESONATOR
310
SUSTAINING AMPLIFIER
305
OSCILLATOR
395
FREQUENCY CONTROLLER
349
FREQUENCY DIVIDER
SQUARE-WAVE GENERATOR
330
350
FREQUENCY SELECTOR
335
MODE SELECTOR
345
OUTPUT (CLOCK) SIGNAL
SECOND OSCILLATOR (WITH SYNCHRONIZATION MODULE)
375
VOLTAGE ISOLATOR
355
LOW-LATENCY START-UP MODULE
399

FIG. 3

300

FIG. 4

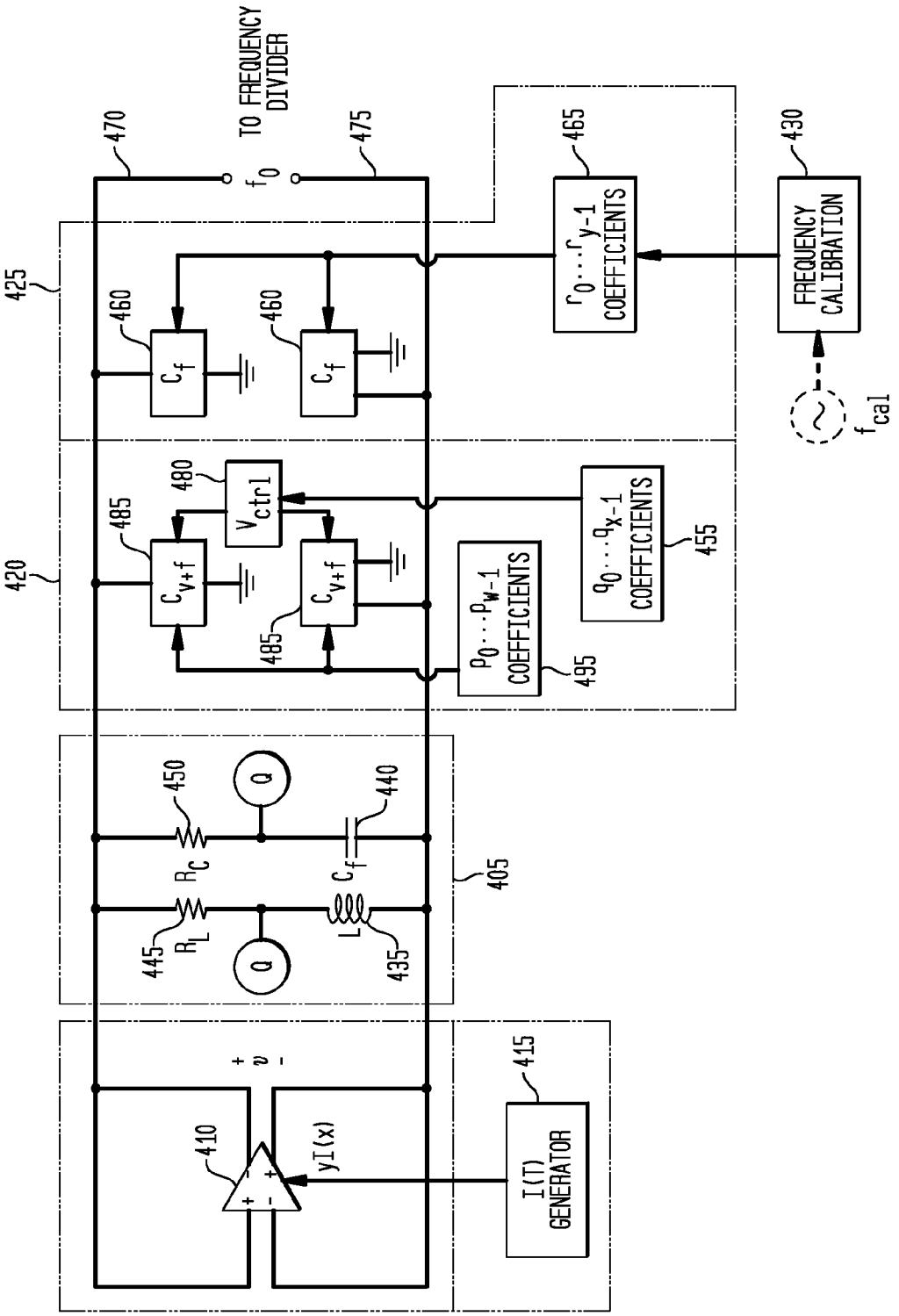

TO FREQUENCY DIVIDER
470
475
f_0
425
420
405
460
460
C_f
C_f
465
$r_0 \cdots r_{y-1}$ COEFFICIENTS
430
FREQUENCY CALIBRATION
f_{cal}
480
V_{ctrl}
485
485
C_{v+f}
C_{v+f}
$q_0 \cdots q_{x-1}$ COEFFICIENTS
455
$p_0 \cdots p_{w-1}$ COEFFICIENTS
495
450
440
Q
Q
R_C
C_f
445
R_L
L
435
410
yI(x)
415
I(T) GENERATOR

FIG. 5A

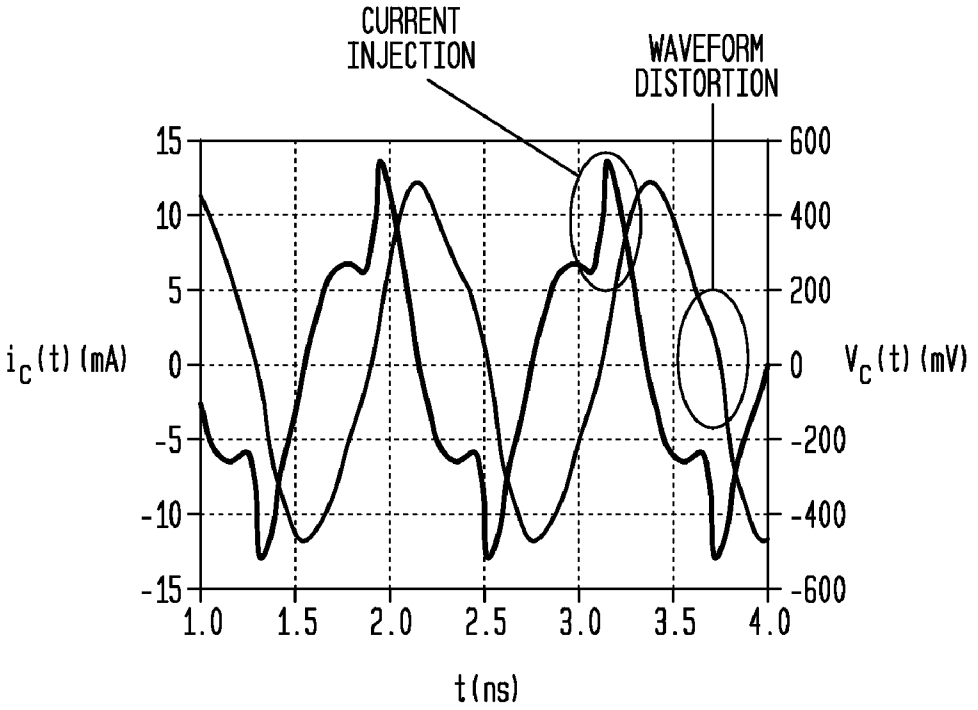
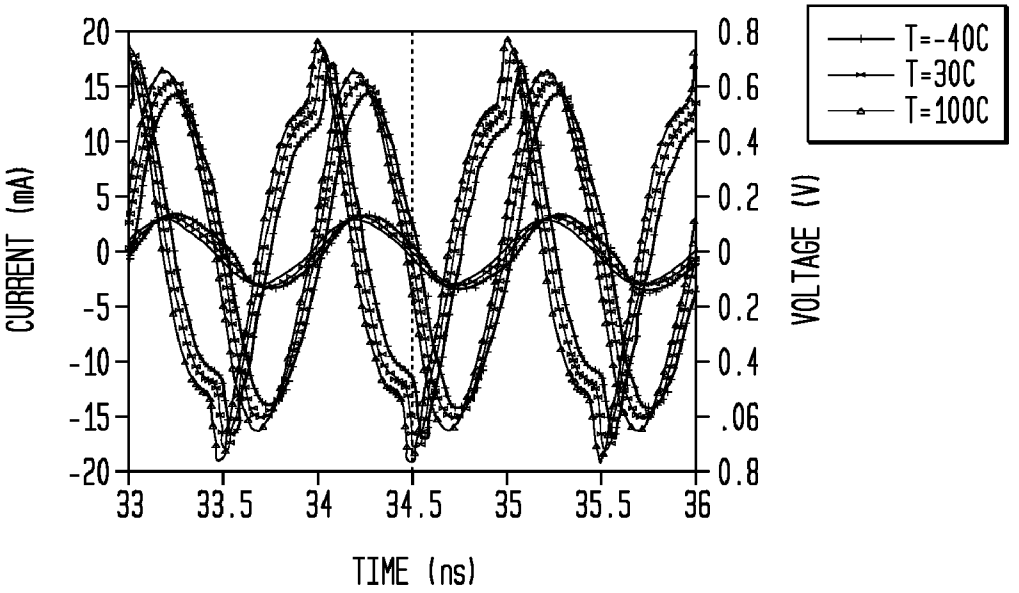


FIG. 5B



TEMPERATURE/BIAS DEPENDENCE

FIG. 5C

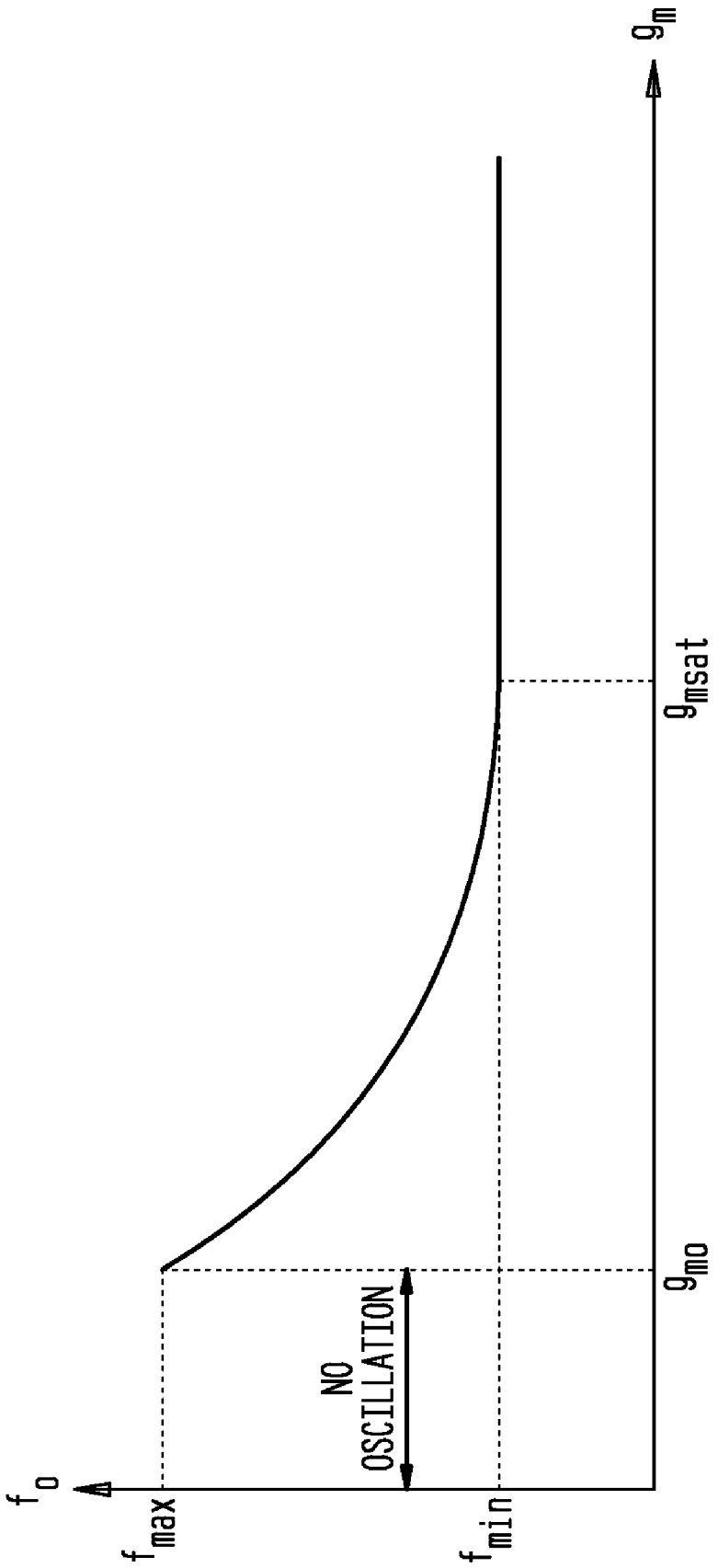


FIG. 6

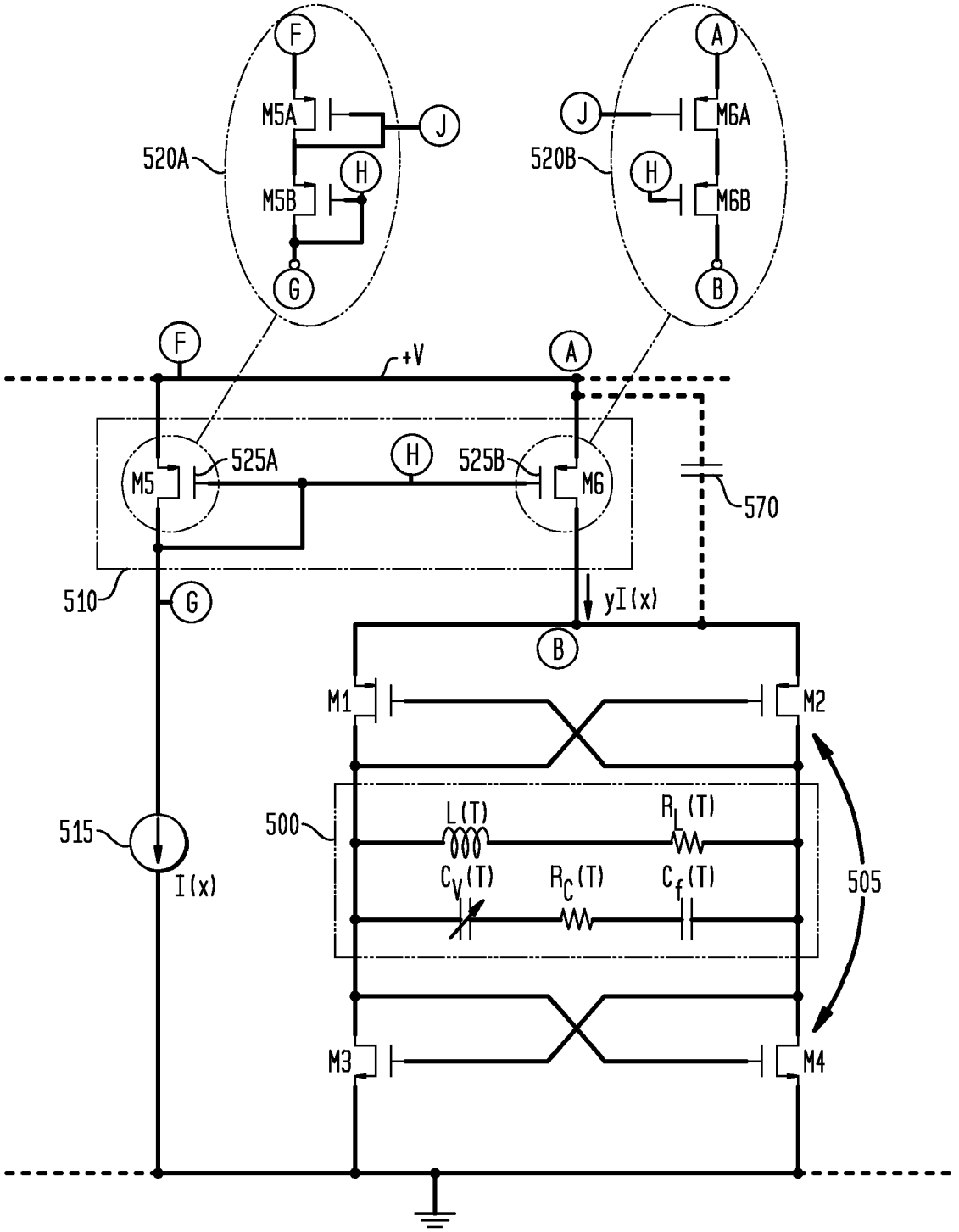

F
M5A
J
520A
H
M5B
G
A
J
M6A
520B
H
M6B
B
F
+V
A
525A
H
525B
M5
M6
570
510
G
yI(x)
B
M1
M2
515
500
L(T)
R_L(T)
I(x)
C_V(T)
R_C(T)
C_f(T)
505
M3
M4

FIG. 7A

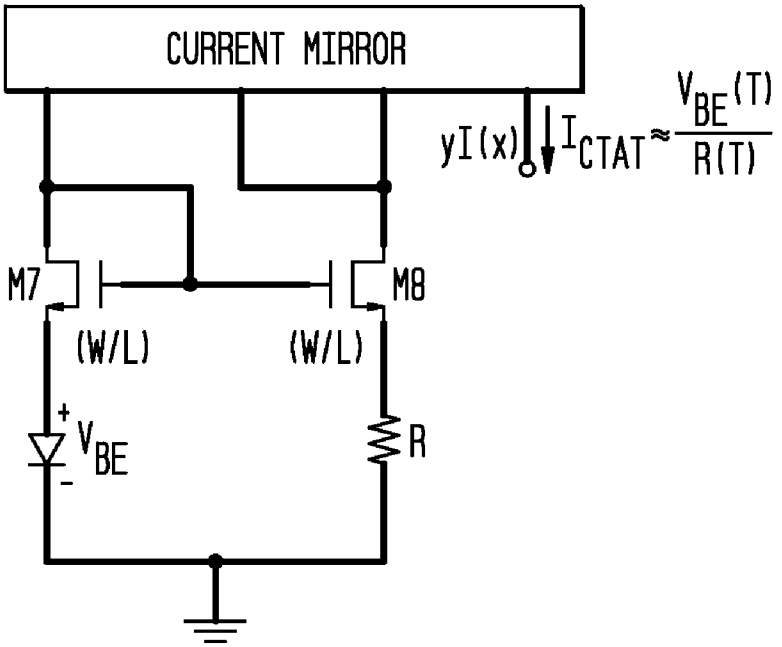

CURRENT MIRROR
yI(x)
$I_{CTAT} \approx \frac{V_{BE}(T)}{R(T)}$
M7
M8
(W/L)
(W/L)
+
V_{BE}
-
R

FIG. 7B

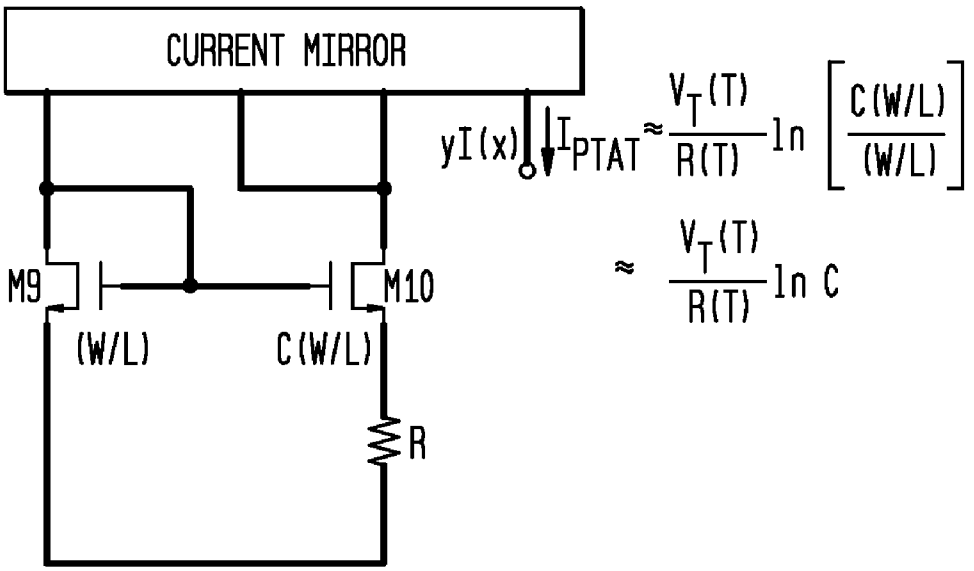

CURRENT MIRROR
yI(x)
$I_{PTAT} \approx \frac{V_T(T)}{R(T)} \ln \left[\frac{C(W/L)}{(W/L)} \right]$
$\approx \frac{V_T(T)}{R(T)} \ln C$
M9
M10
(W/L)
C(W/L)
R

FIG. 7C

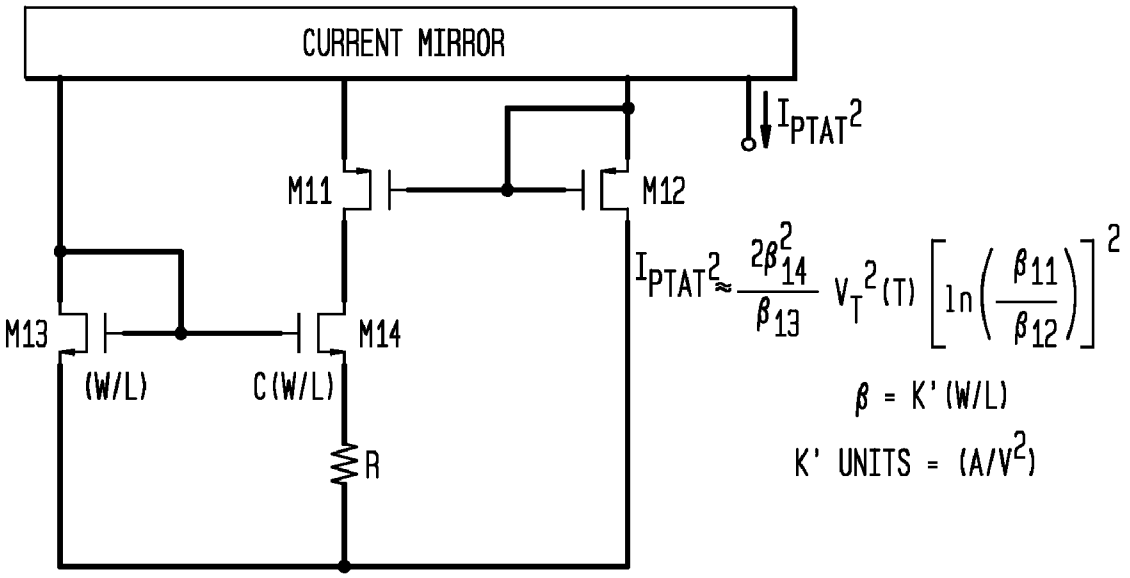

CURRENT MIRROR
I_{PTAT}^2
M11
M12
M13
M14
(W/L)
C(W/L)
R
$I_{PTAT}^2 \approx \frac{2\beta_{14}^2}{\beta_{13}} V_T^2(T) \left[\ln\left(\frac{\beta_{11}}{\beta_{12}}\right)\right]^2$
$\beta = K'(W/L)$
K' UNITS = (A/V^2)

FIG. 7D

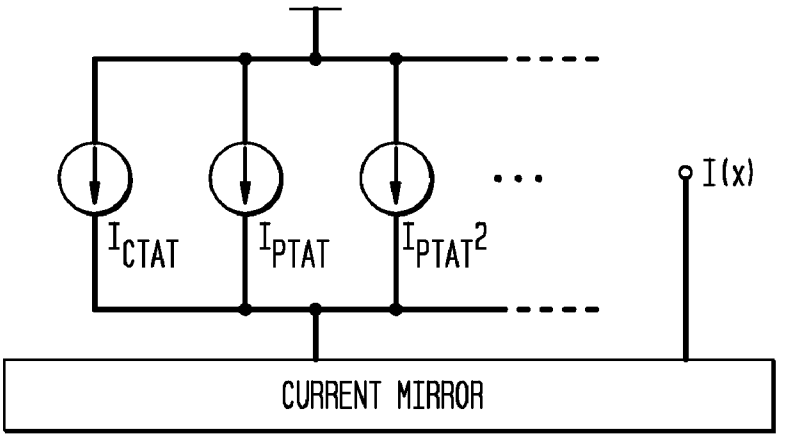

I_{CTAT}
I_{PTAT}
I_{PTAT}^2
I(x)
CURRENT MIRROR

FIG. 8

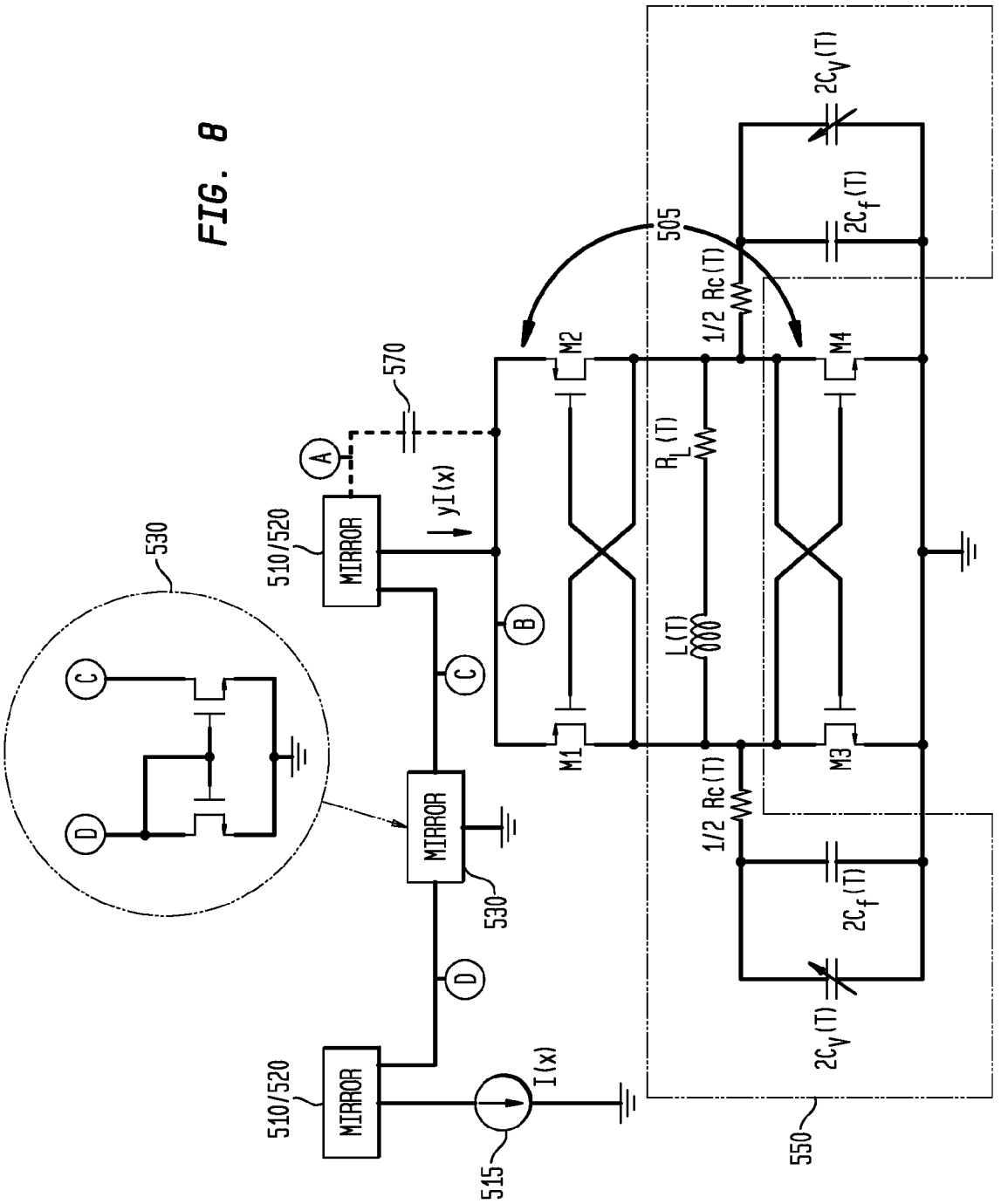

530
C
D
510/520
MIRROR
A
570
yI(x)
B
C
MIRROR
530
D
510/520
MIRROR
515
I(x)
M1
M2
M3
M4
505
1/2 Rc(T)
1/2 Rc(T)
$R_L(T)$
L(T)
$2C_V(T)$
$2C_f(T)$
$2C_f(T)$
$2C_V(T)$
550

FIG. 9

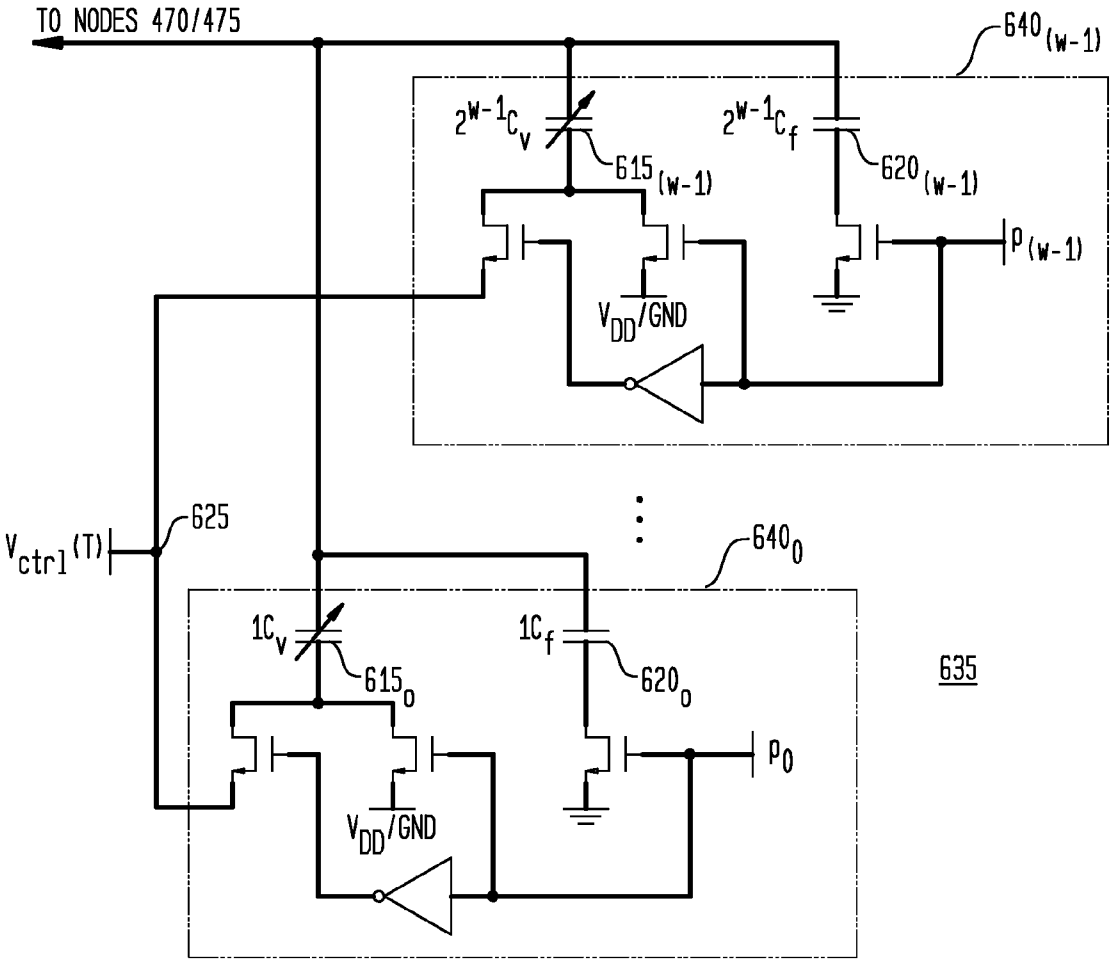

TO NODES 470/475
640(w-1)
2w-1Cv
615(w-1)
2w-1Cf
620(w-1)
P(w-1)
VDD/GND
Vctrl(T)
625
640o
1Cv
615o
1Cf
620o
635
Po
VDD/GND

FIG. 10

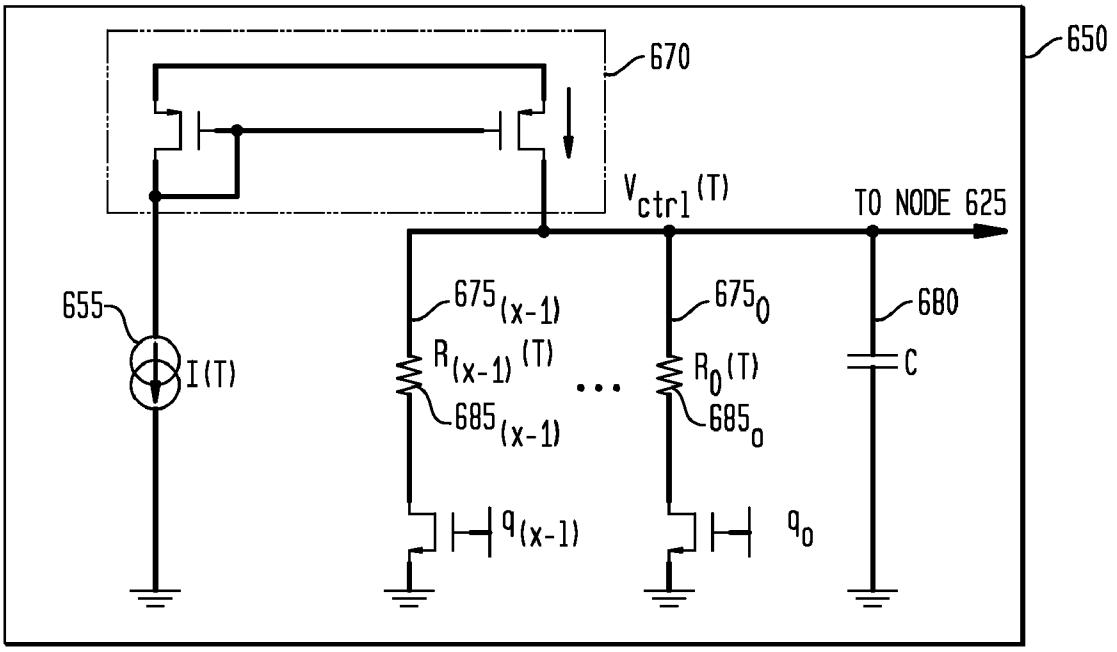

650
670
$V_{ctrl}(T)$
TO NODE 625
655
I(T)
$675_{(x-1)}$
$R_{(x-1)}(T)$
$685_{(x-1)}$
675_0
$R_0(T)$
685_0
680
C
$q_{(x-1)}$
q_0

FIG. 11

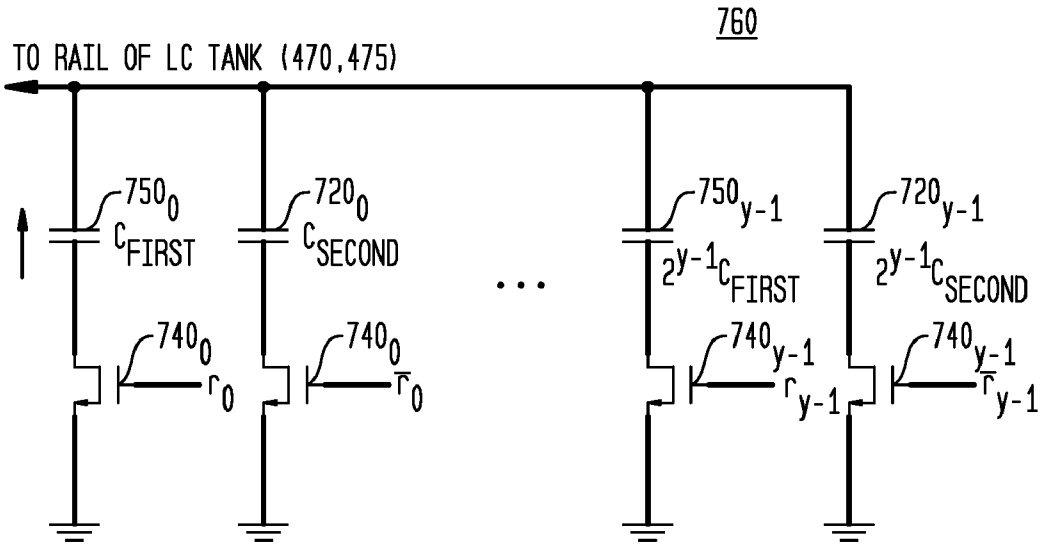

760
TO RAIL OF LC TANK (470,475)
750_0
C_{FIRST}
720_0
C_{SECOND}
750_{y-1}
$2^{y-1}C_{FIRST}$
720_{y-1}
$2^{y-1}C_{SECOND}$
740_0
r_0
740_0
$\bar{r}_0$
740_{y-1}
r_{y-1}
740_{y-1}
$\bar{r}_{y-1}$

FIG. 12

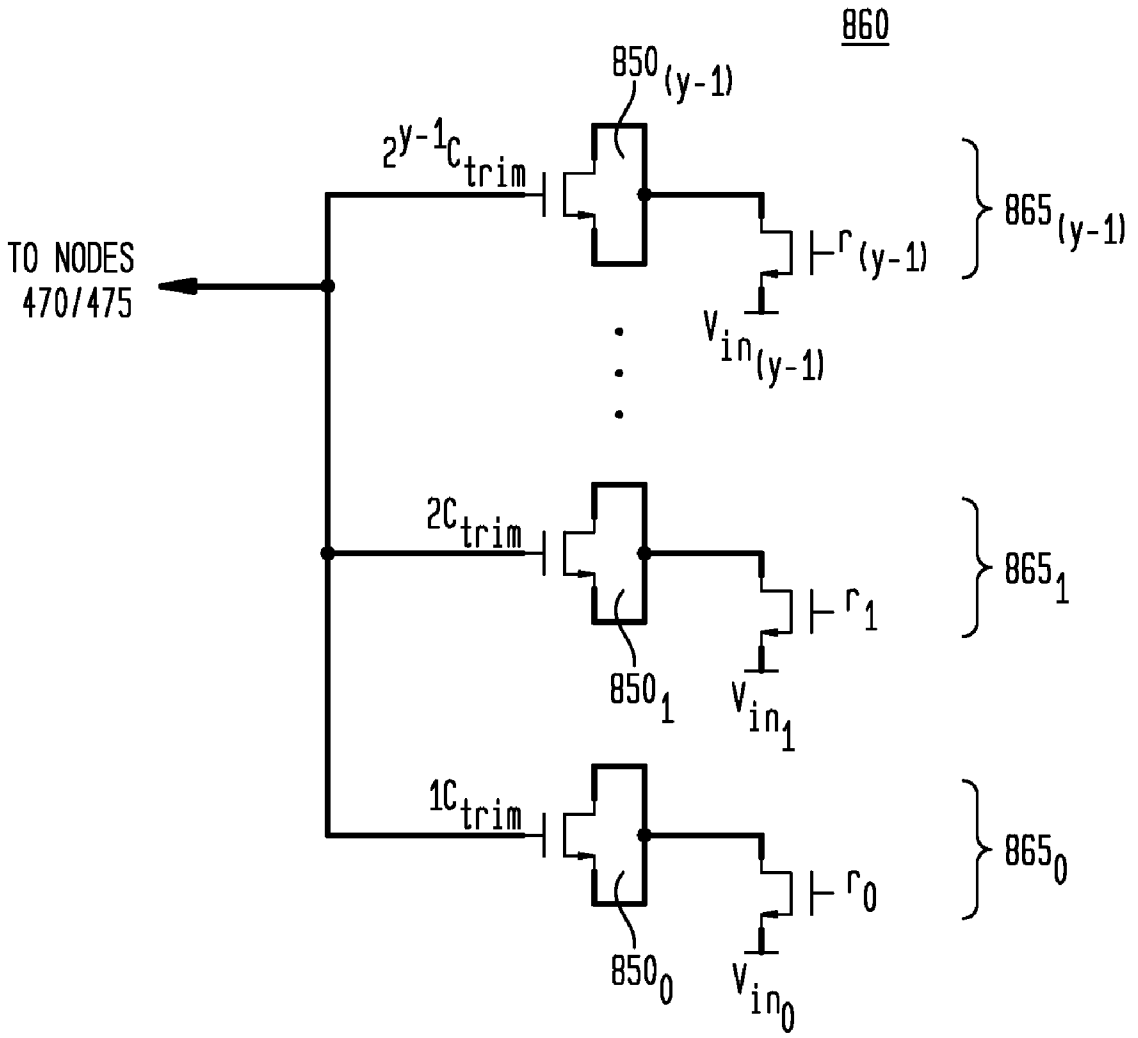

860
850(y-1)
2y-1Ctrim
TO NODES
470/475
r(y-1)
865(y-1)
Vin(y-1)
2Ctrim
r1
865 1
850 1
Vin1
1Ctrim
r0
865 0
850 0
Vin0

FIG. 13

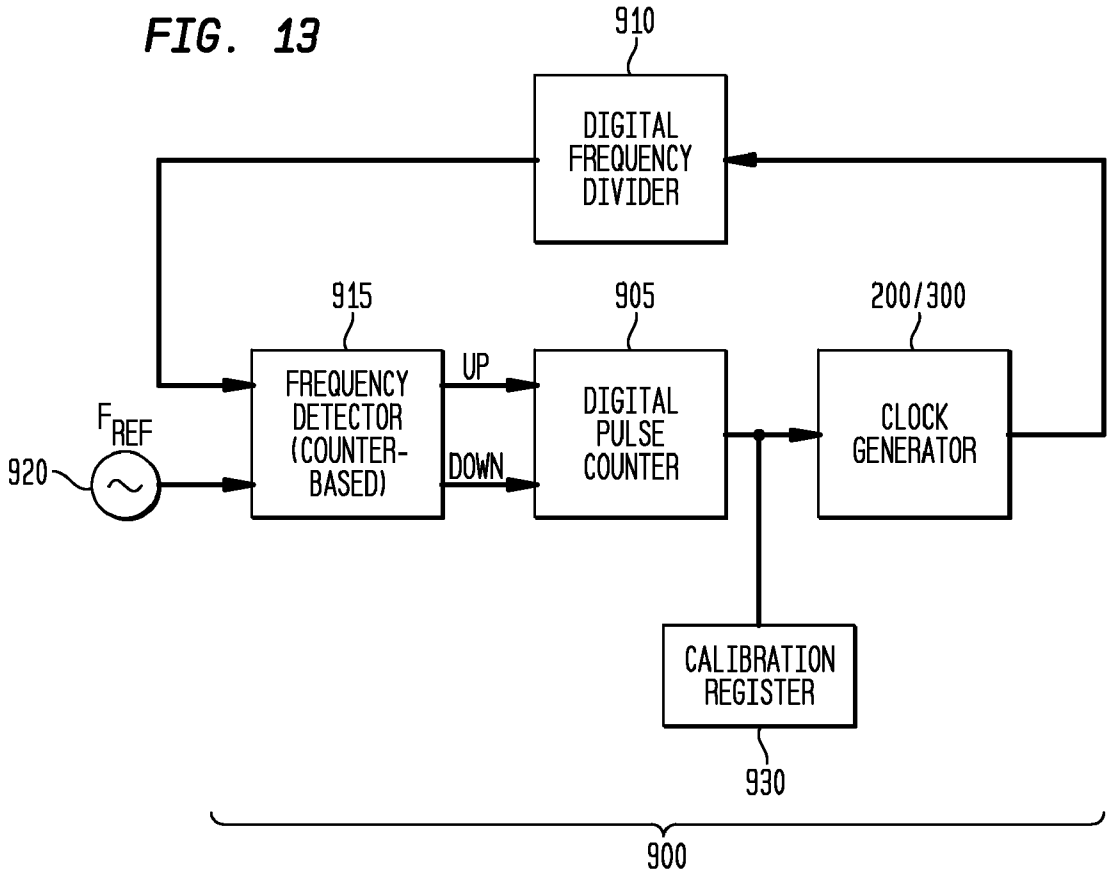

910
DIGITAL FREQUENCY DIVIDER
915
905
200/300
FREQUENCY DETECTOR (COUNTER-BASED)
UP
DOWN
DIGITAL PULSE COUNTER
CLOCK GENERATOR
F_{REF}
920
CALIBRATION REGISTER
930
900

FIG. 14

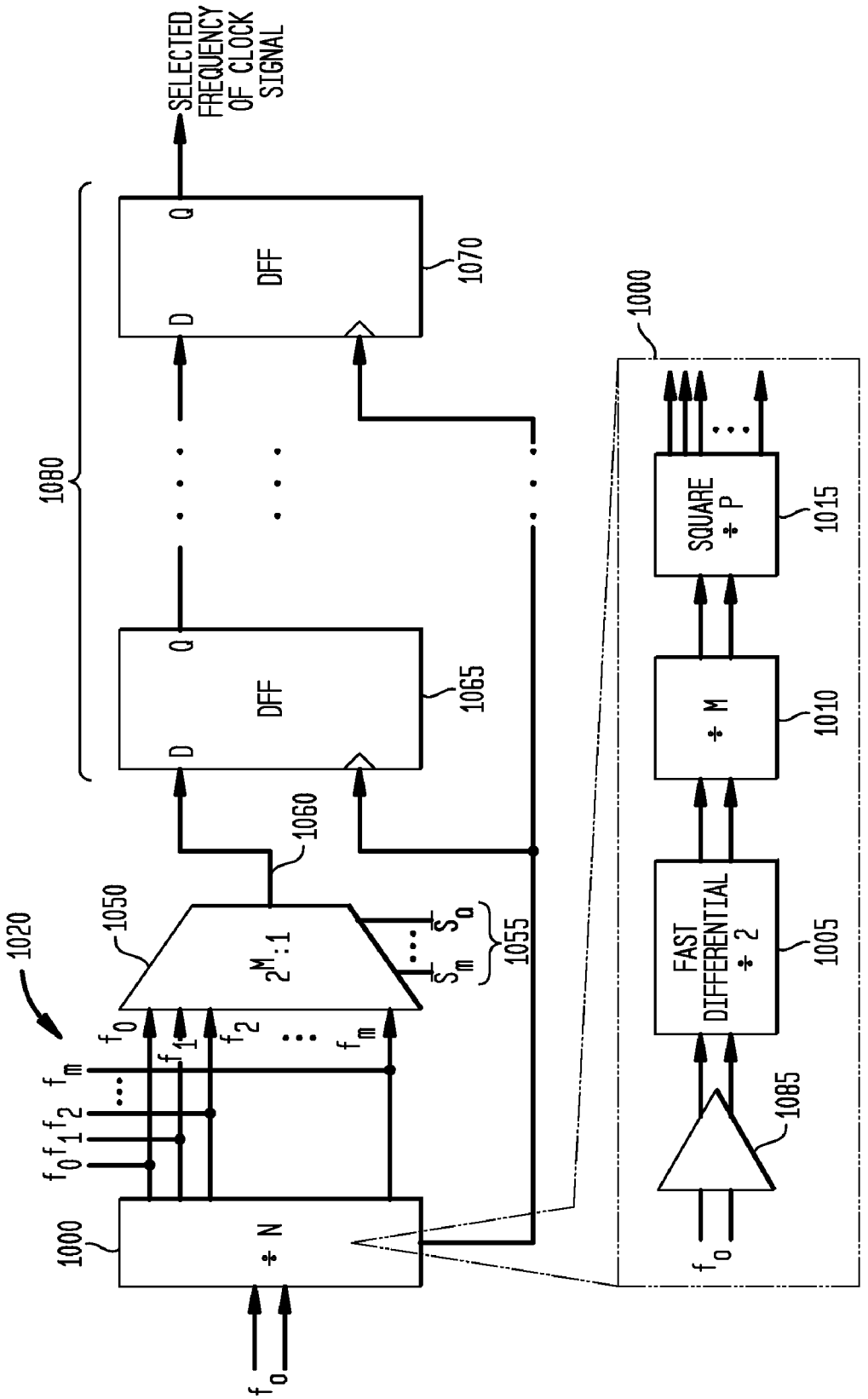

SELECTED FREQUENCY OF CLOCK SIGNAL
DFF
D
Q
1070
1080
DFF
D
Q
1065
1060
1050
$2^M:1$
S_m
S_0
1055
1020
f_0
f_1
f_2
f_m
1000
÷ N
f_0
1000
SQUARE ÷ P
1015
÷ M
1010
FAST DIFFERENTIAL ÷ 2
1005
1085
f_0

FIG. 15B

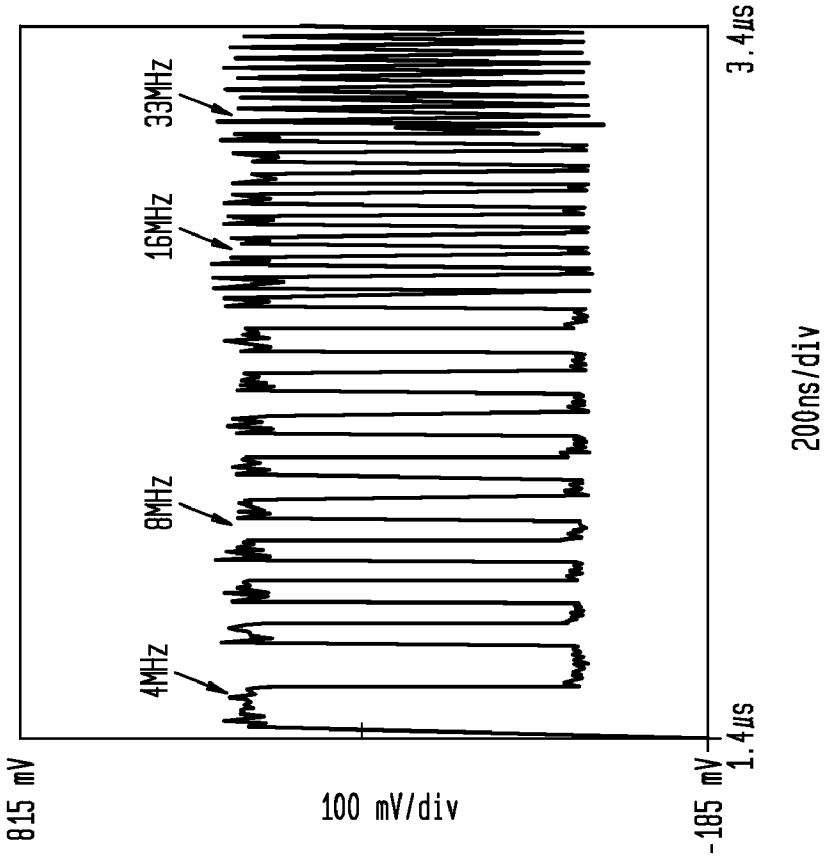


FIG. 15A

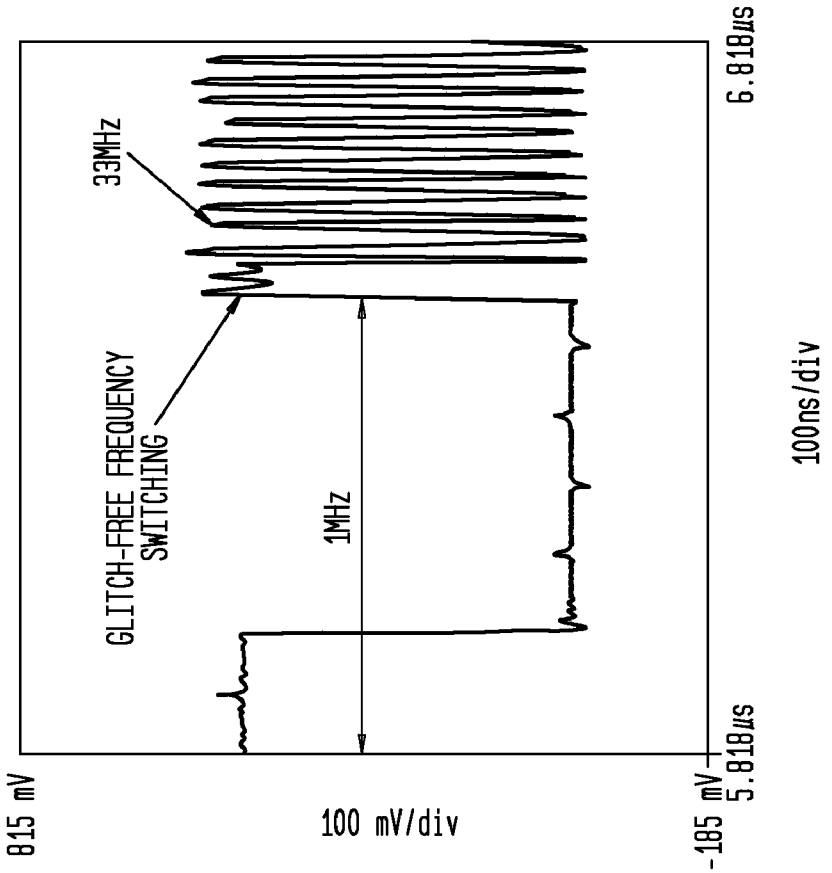


FIG. 16

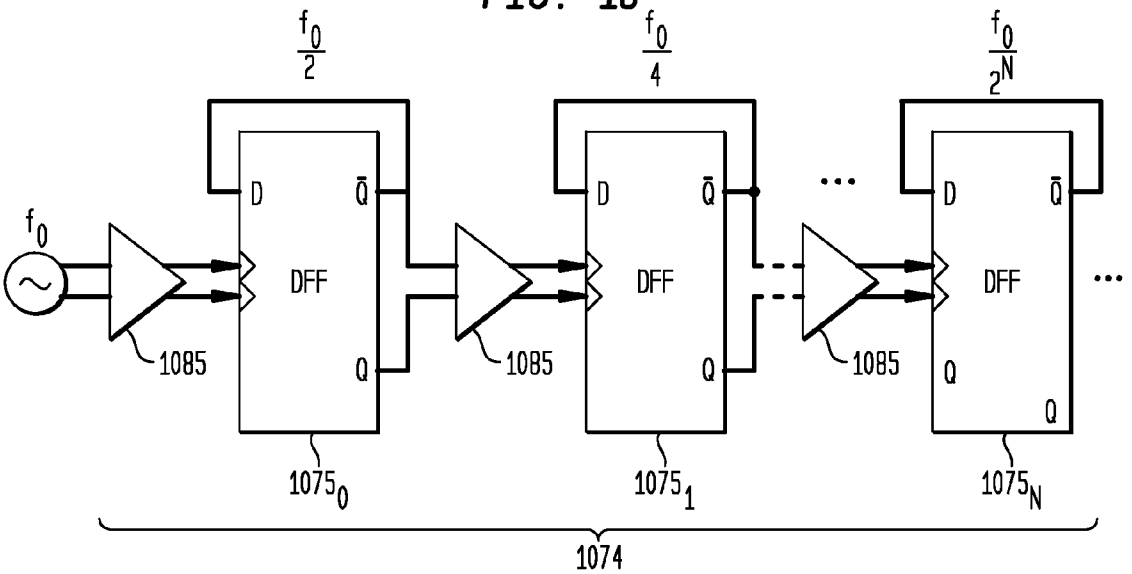


FIG. 17

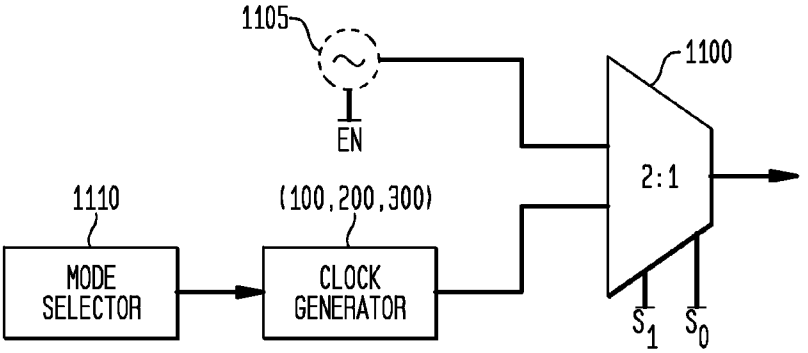


FIG. 18

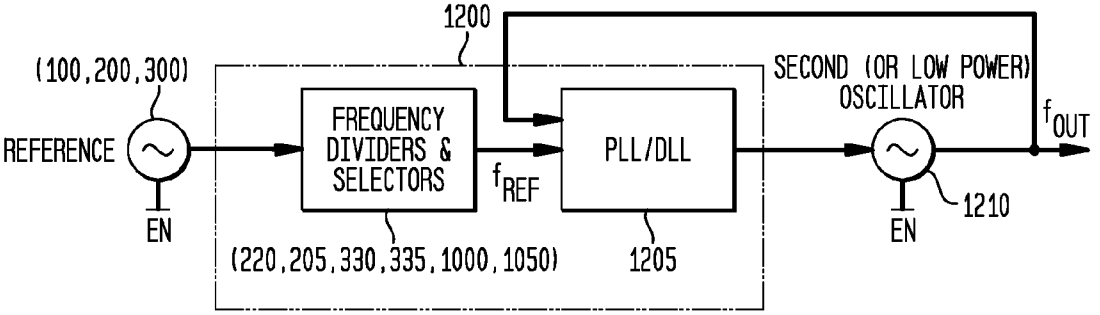


FIG. 19

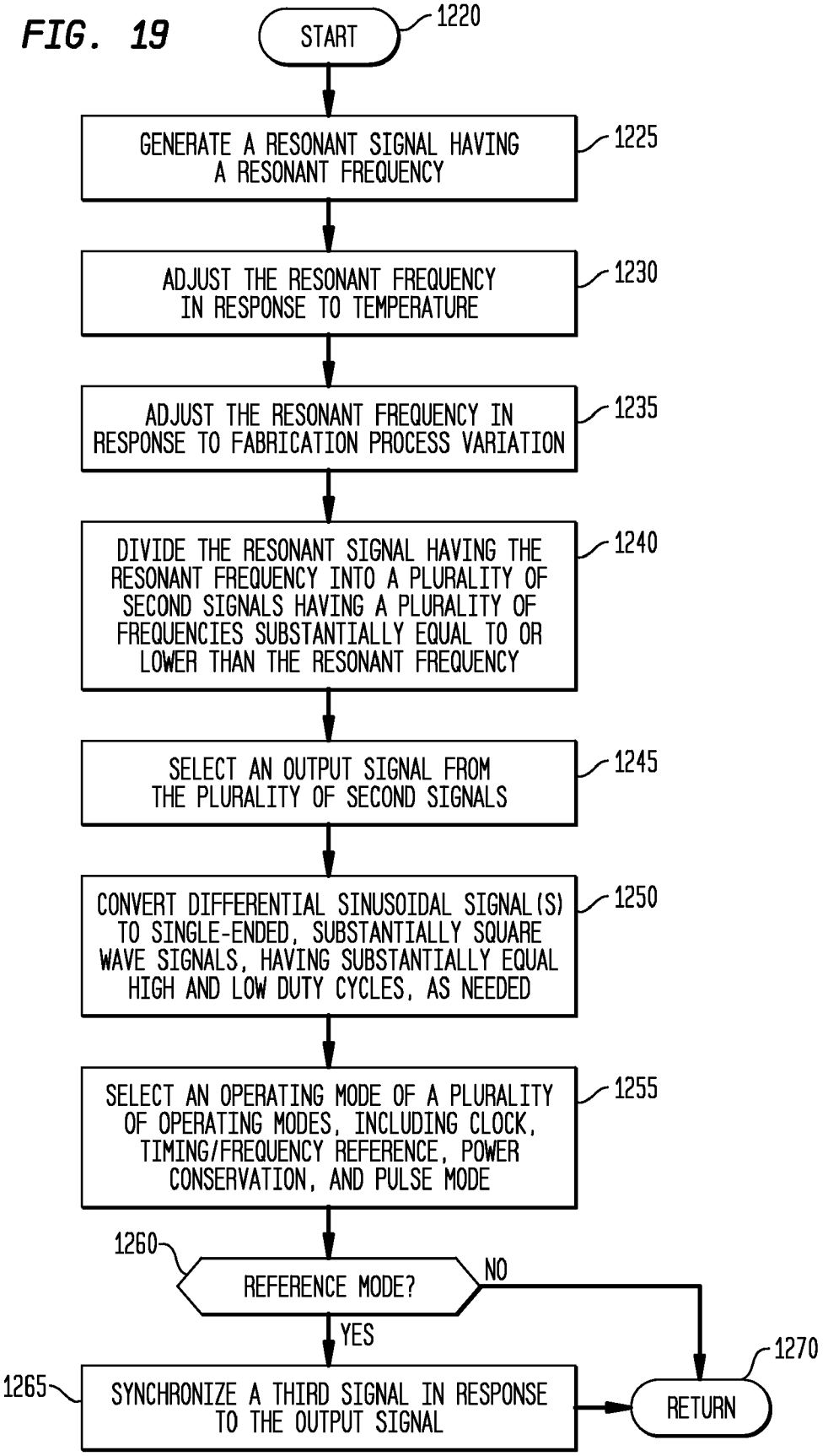

START
1220
GENERATE A RESONANT SIGNAL HAVING A RESONANT FREQUENCY
1225
ADJUST THE RESONANT FREQUENCY IN RESPONSE TO TEMPERATURE
1230
ADJUST THE RESONANT FREQUENCY IN RESPONSE TO FABRICATION PROCESS VARIATION
1235
DIVIDE THE RESONANT SIGNAL HAVING THE RESONANT FREQUENCY INTO A PLURALITY OF SECOND SIGNALS HAVING A PLURALITY OF FREQUENCIES SUBSTANTIALLY EQUAL TO OR LOWER THAN THE RESONANT FREQUENCY
1240
SELECT AN OUTPUT SIGNAL FROM THE PLURALITY OF SECOND SIGNALS
1245
CONVERT DIFFERENTIAL SINUSOIDAL SIGNAL(S) TO SINGLE-ENDED, SUBSTANTIALLY SQUARE WAVE SIGNALS, HAVING SUBSTANTIALLY EQUAL HIGH AND LOW DUTY CYCLES, AS NEEDED
1250
SELECT AN OPERATING MODE OF A PLURALITY OF OPERATING MODES, INCLUDING CLOCK, TIMING/FREQUENCY REFERENCE, POWER CONSERVATION, AND PULSE MODE
1255
1260
REFERENCE MODE?
NO
YES
1265
SYNCHRONIZE A THIRD SIGNAL IN RESPONSE TO THE OUTPUT SIGNAL
RETURN
1270

FIG. 20

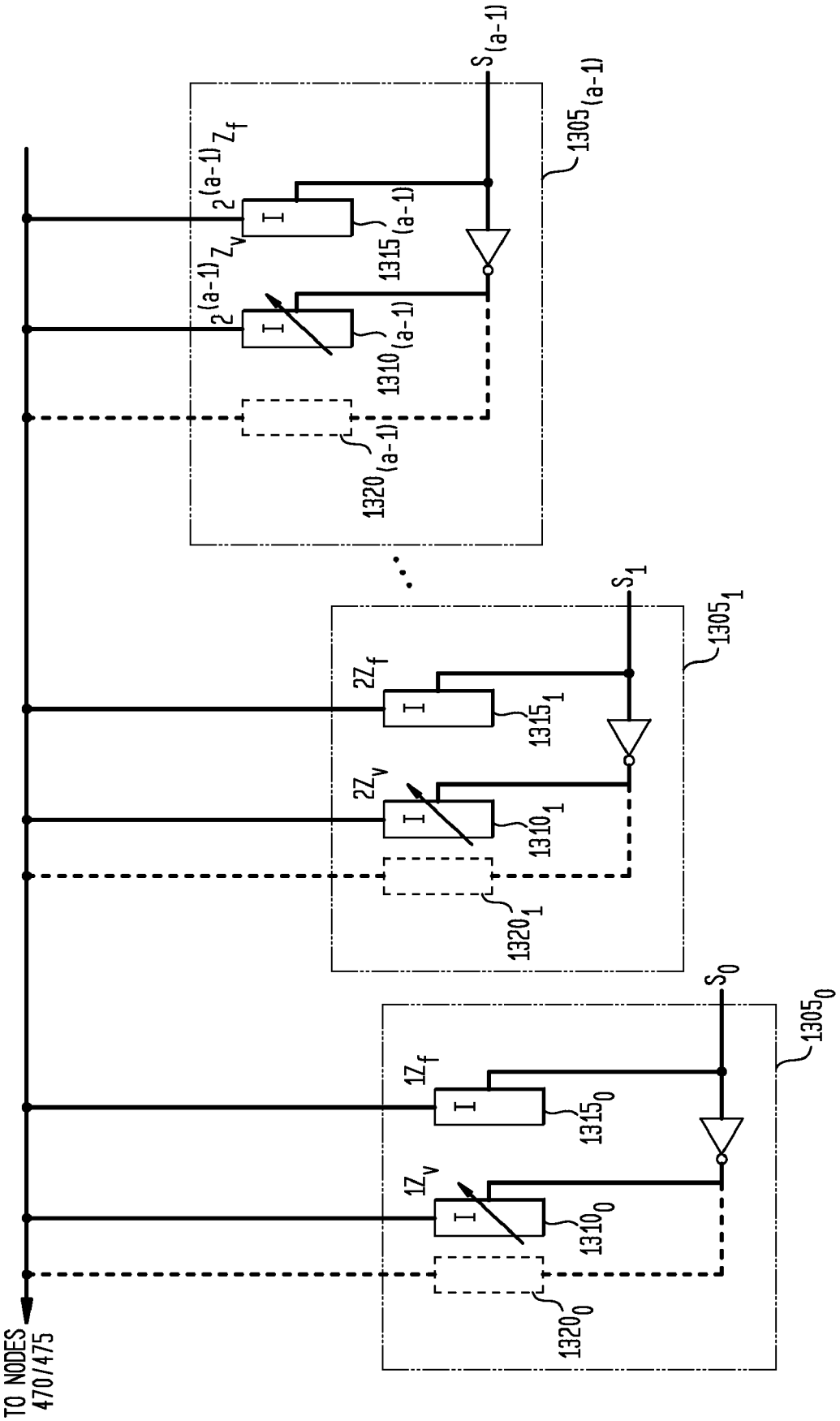
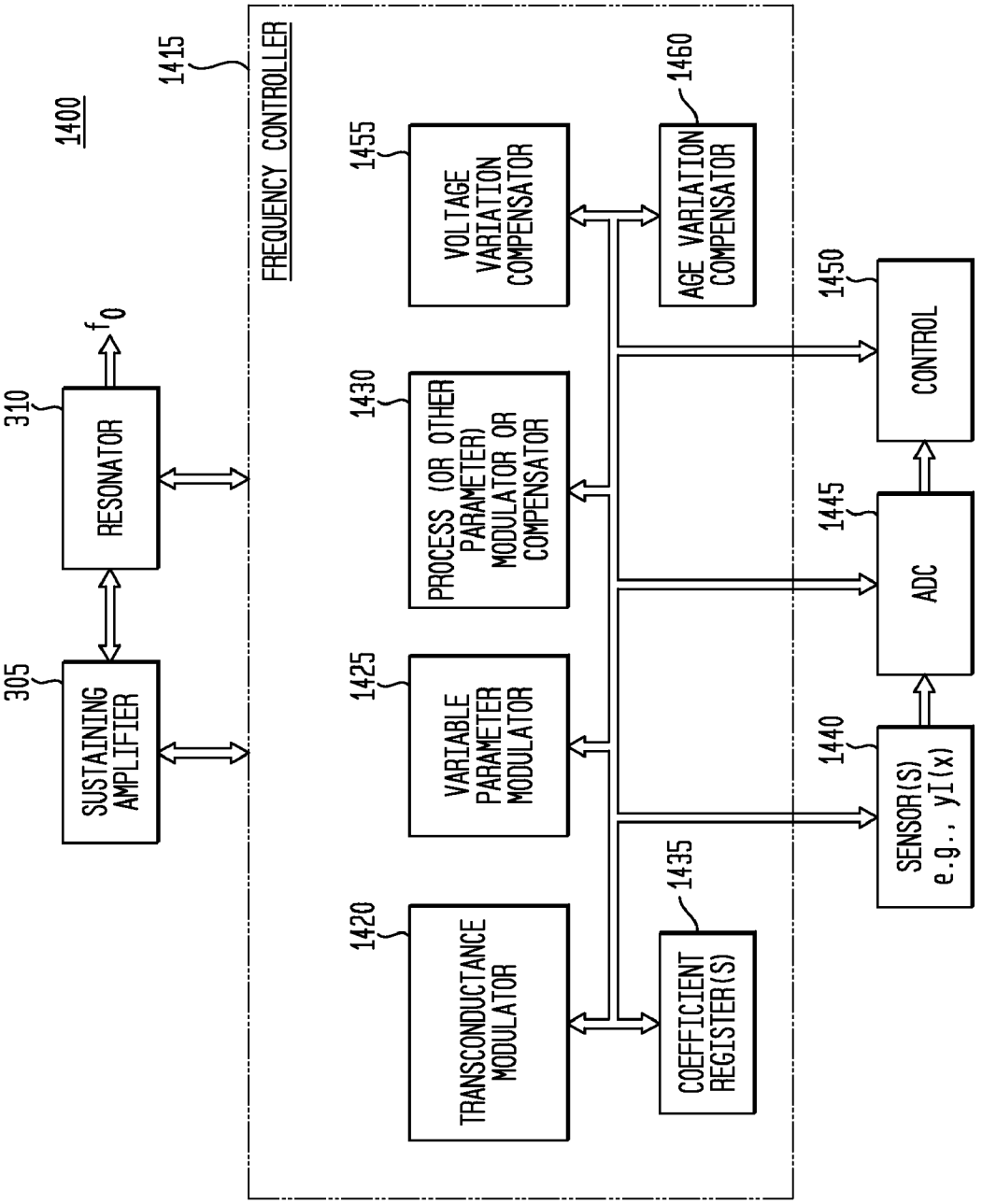

1300
TO NODES 470/475
$1Z_f$
$1Z_v$
1315_0
1310_0
1320_0
1305_0
S_0
$2Z_f$
$2Z_v$
1315_1
1310_1
1320_1
1305_1
S_1
$2^{(a-1)}Z_f$
$2^{(a-1)}Z_v$
$1315_{(a-1)}$
$1310_{(a-1)}$
$1320_{(a-1)}$
$1305_{(a-1)}$
$S_{(a-1)}$

FIG. 21


1400
1415
FREQUENCY CONTROLLER
310
RESONATOR
f_0
305
SUSTAINING AMPLIFIER
1455
VOLTAGE VARIATION COMPENSATOR
1460
AGE VARIATION COMPENSATOR
1430
PROCESS (OR OTHER PARAMETER) MODULATOR OR COMPENSATOR
1425
VARIABLE PARAMETER MODULATOR
1420
TRANSCONDUCTANCE MODULATOR
1435
COEFFICIENT REGISTER(S)
1450
CONTROL
1445
ADC
1440
SENSOR(S) e.g., yI(x)

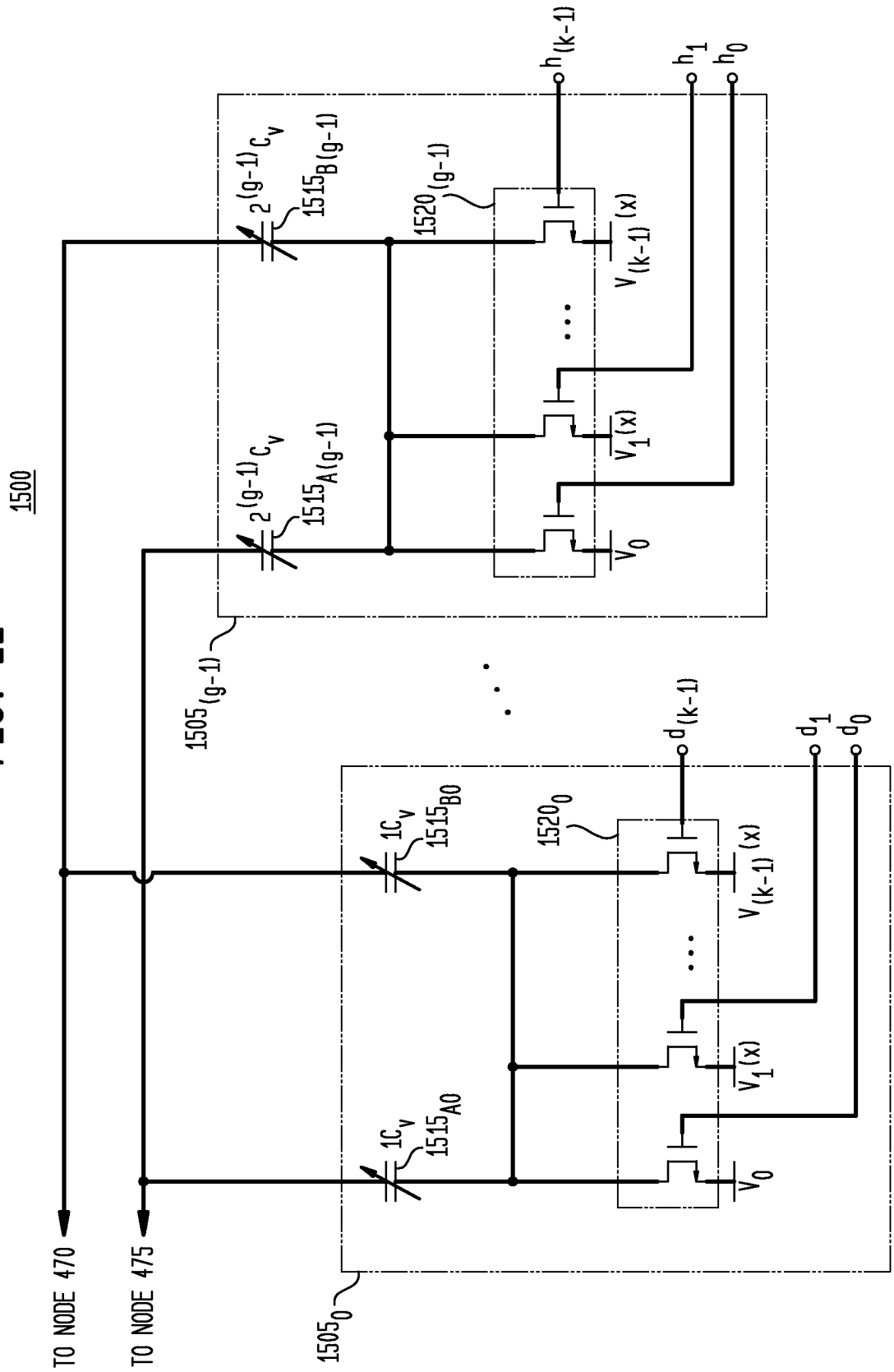

1500
TO NODE 470
TO NODE 475
1505_0
$1505_{(g-1)}$
1515_{A0}
1515_{B0}
$1515_{A(g-1)}$
$1515_{B(g-1)}$
1520_0
$1520_{(g-1)}$
$1C_V$
$2^{(g-1)}C_V$
V_0
$V_1(x)$
$V_{(k-1)}(x)$
d_0
d_1
$d_{(k-1)}$
h_0
h_1
$h_{(k-1)}$

FIG. 22

FIG. 23

1600

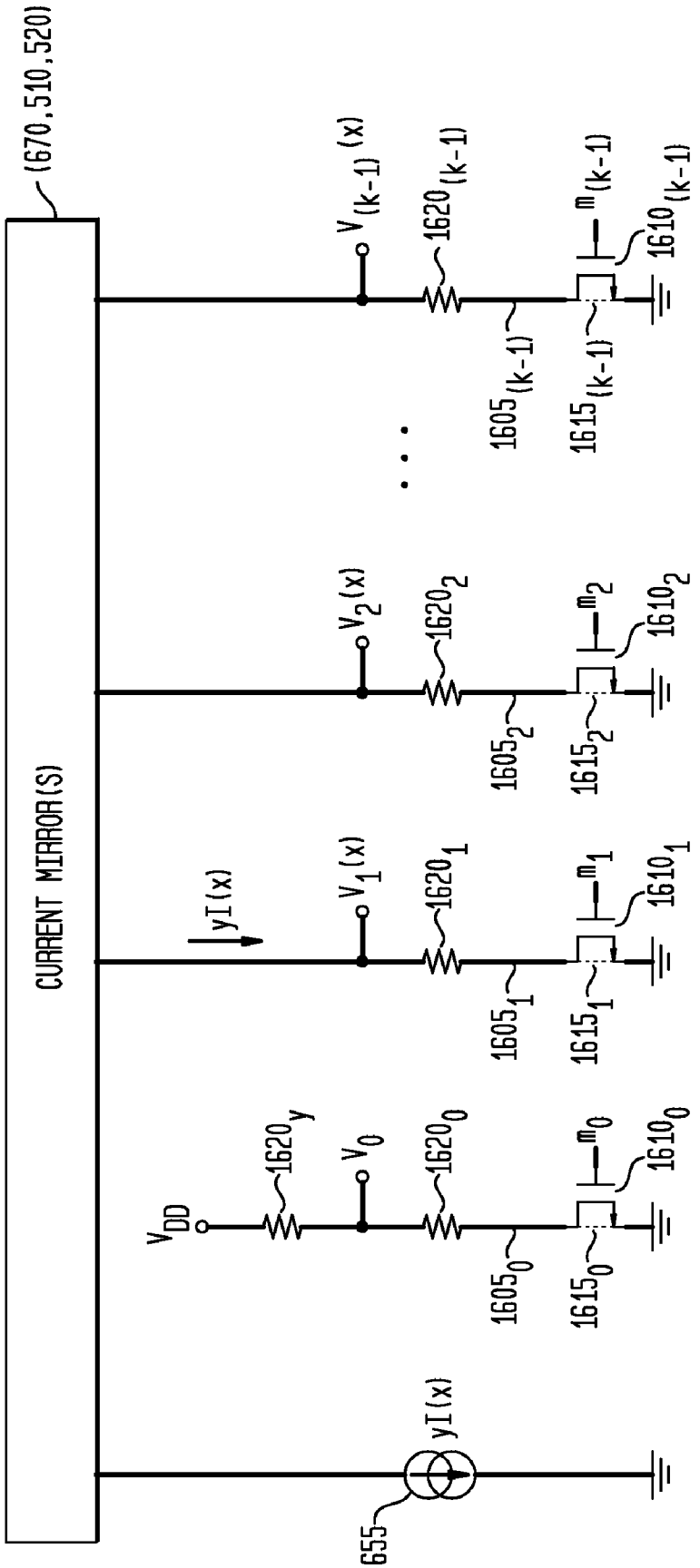

(670,510,520)
CURRENT MIRROR(S)
655
yI(x)
V_{DD}
1620_y
V_0
1620_0
1605_0
1615_0
m_0
1610_0
yI(x)
$V_1(x)$
1620_1
1605_1
1615_1
m_1
1610_1
$V_2(x)$
1620_2
1605_2
1615_2
m_2
1610_2
$V_{(k-1)}(x)$
$1620_{(k-1)}$
$1605_{(k-1)}$
$1615_{(k-1)}$
$m_{(k-1)}$
$1610_{(k-1)}$

FIG. 24

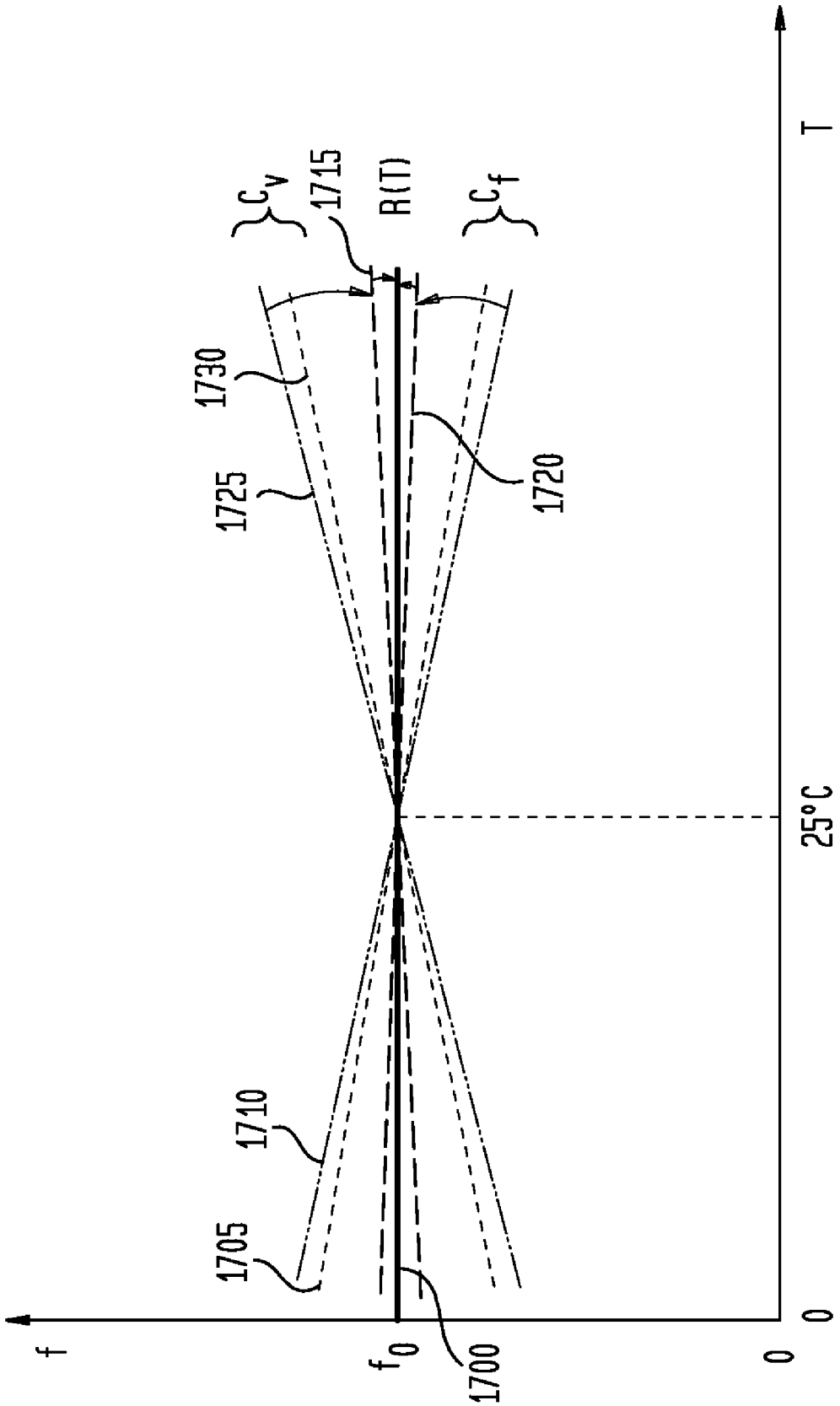
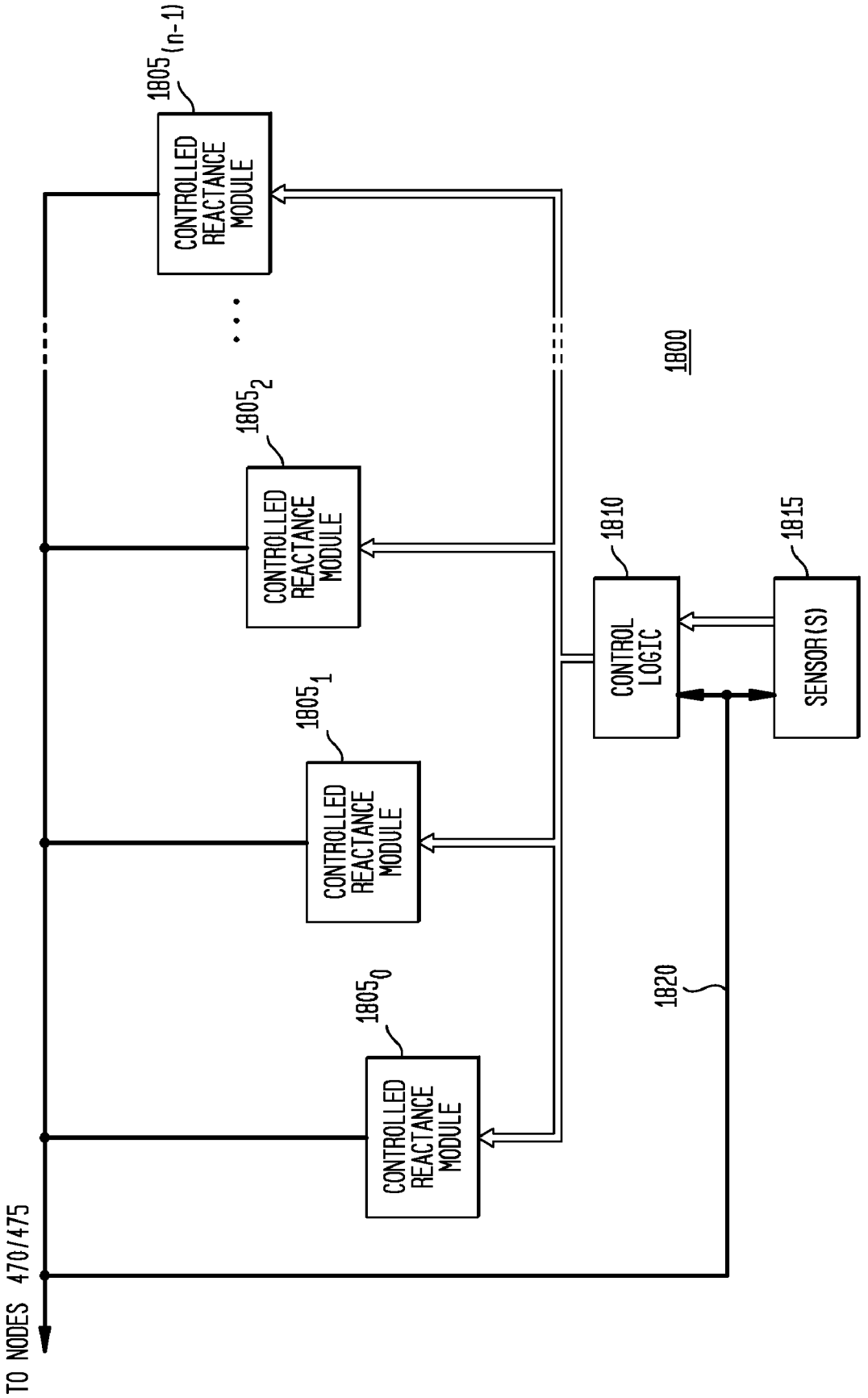


FIG. 25


1805(n-1)
CONTROLLED REACTANCE MODULE
1805 2
CONTROLLED REACTANCE MODULE
1805 1
CONTROLLED REACTANCE MODULE
1805 0
CONTROLLED REACTANCE MODULE
1810
CONTROL LOGIC
1815
SENSOR(S)
1800
1820
TO NODES 470/475

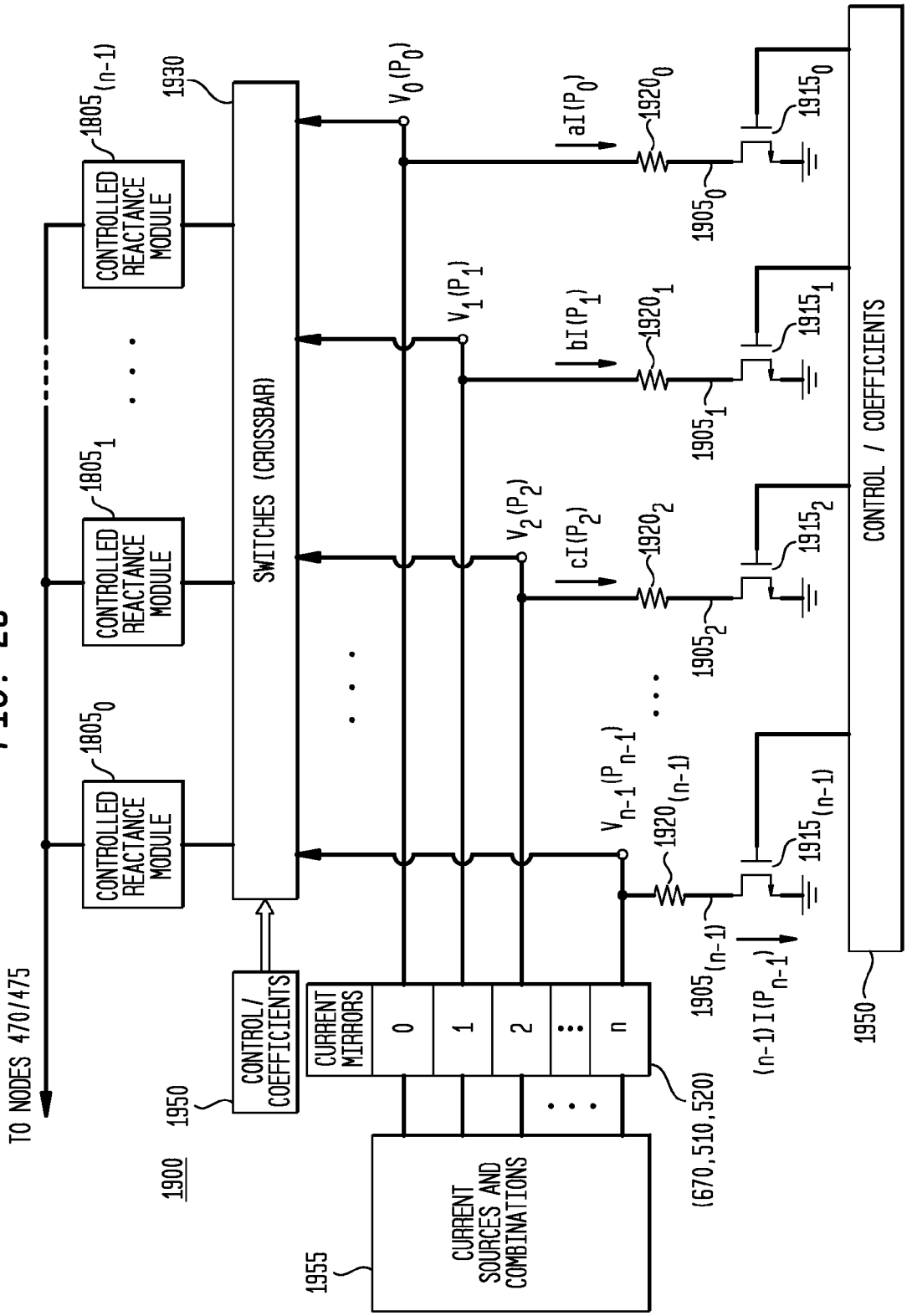

TO NODES 470/475
CONTROLLED REACTANCE MODULE
CONTROLLED REACTANCE MODULE
CONTROLLED REACTANCE MODULE
1805(n-1)
1805 1
1805 0
1930
SWITCHES (CROSSBAR)
CONTROL/ COEFFICIENTS
1950
1900
CURRENT MIRRORS
0
1
2
n
(670,510,520)
CURRENT SOURCES AND COMBINATIONS
1955
V0(P0)
V1(P1)
V2(P2)
Vn-1(Pn-1)
aI(P0)
bI(P1)
cI(P2)
(n-1)I(Pn-1)
1920 0
1920 1
1920 2
1920(n-1)
1905 0
1905 1
1905 2
1905(n-1)
1915 0
1915 1
1915 2
1915(n-1)
CONTROL / COEFFICIENTS
1950

FIG. 26

FIG. 27

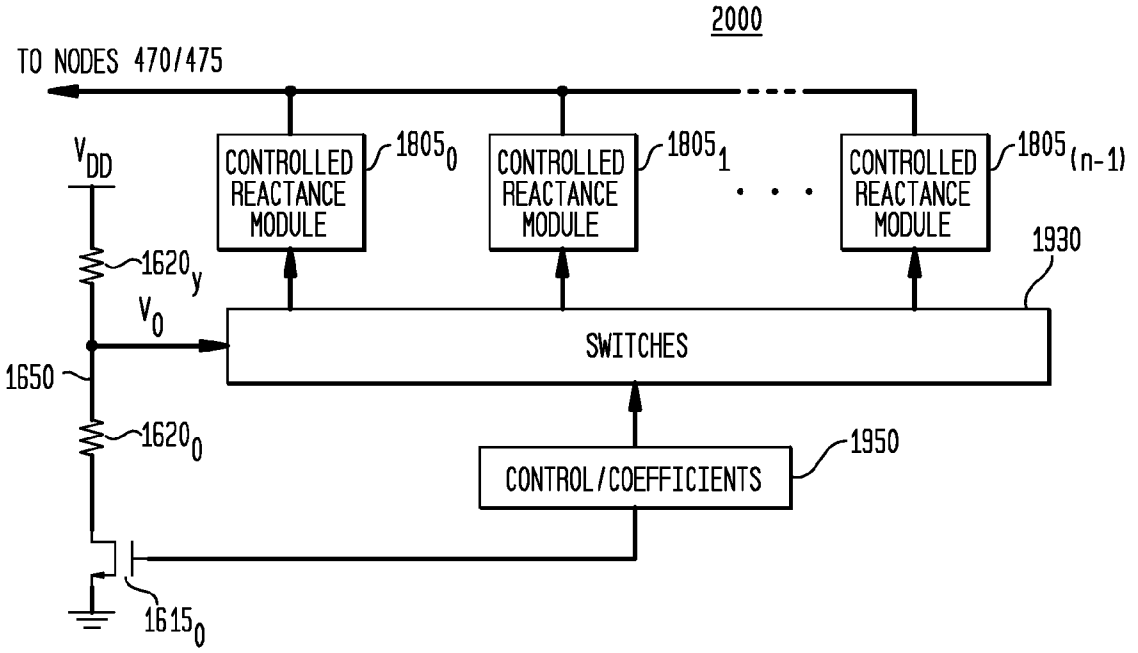

2000
TO NODES 470/475
V_{DD}
CONTROLLED REACTANCE MODULE
1805_0
CONTROLLED REACTANCE MODULE
1805_1
CONTROLLED REACTANCE MODULE
$1805_{(n-1)}$
1930
1620_y
V_0
SWITCHES
1650
1620_0
CONTROL/COEFFICIENTS
1950
1615_0

FIG. 28

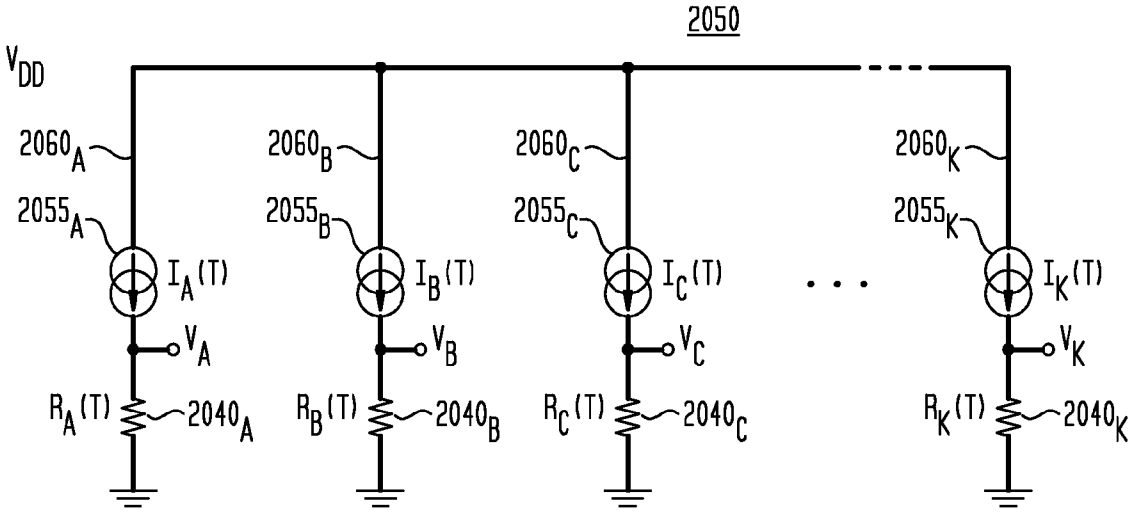

2050
VDD
2060A
2060B
2060C
2060K
2055A
2055B
2055C
2055K
IA(T)
IB(T)
IC(T)
IK(T)
VA
VB
VC
VK
RA(T)
RB(T)
RC(T)
RK(T)
2040A
2040B
2040C
2040K

FIG. 29

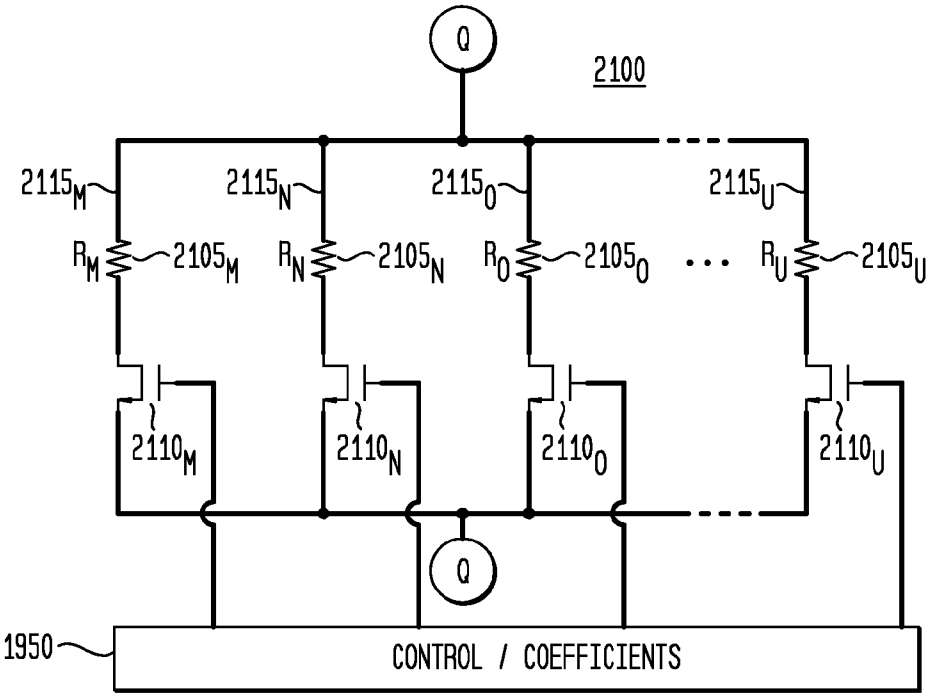
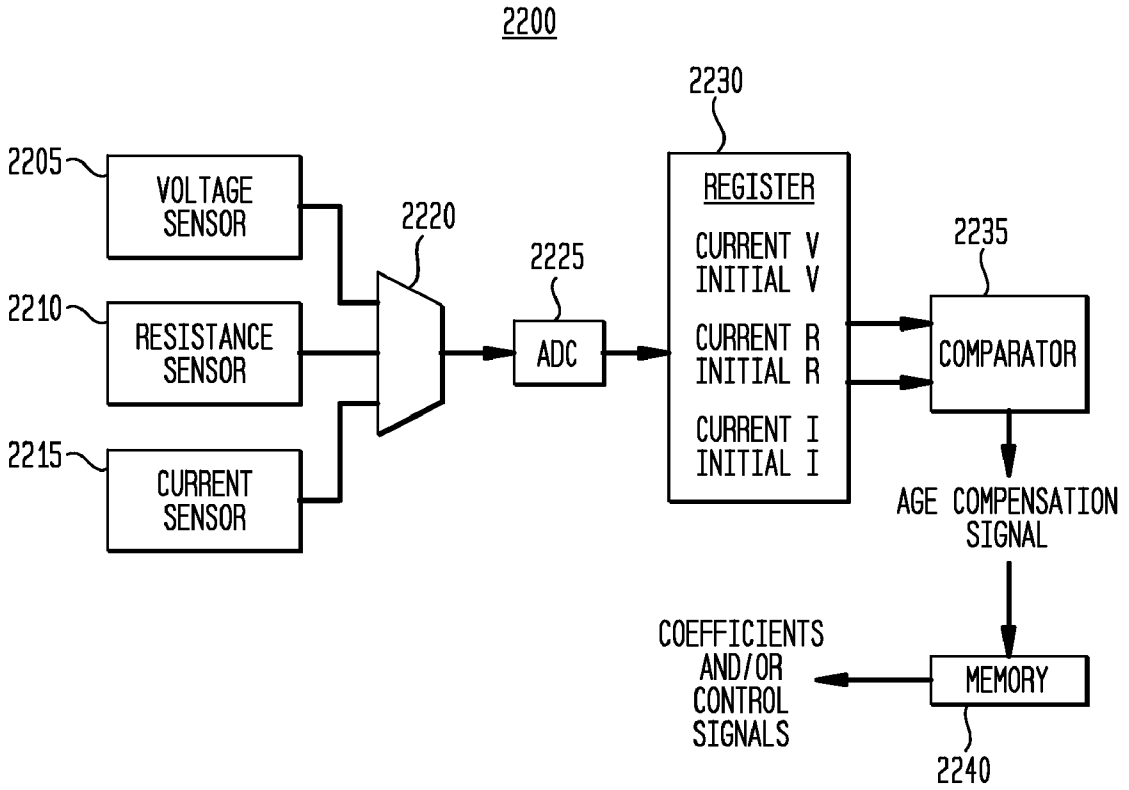

Q
2100
2115M
2115N
2115O
2115U
RM
RN
RO
RU
2105M
2105N
2105O
2105U
2110M
2110N
2110O
2110U
Q
1950
CONTROL / COEFFICIENTS

FIG. 30


2200
2205
VOLTAGE SENSOR
2210
RESISTANCE SENSOR
2215
CURRENT SENSOR
2220
2225
ADC
2230
REGISTER
CURRENT V
INITIAL V
CURRENT R
INITIAL R
CURRENT I
INITIAL I
2235
COMPARATOR
AGE COMPENSATION SIGNAL
MEMORY
2240
COEFFICIENTS AND/OR CONTROL SIGNALS

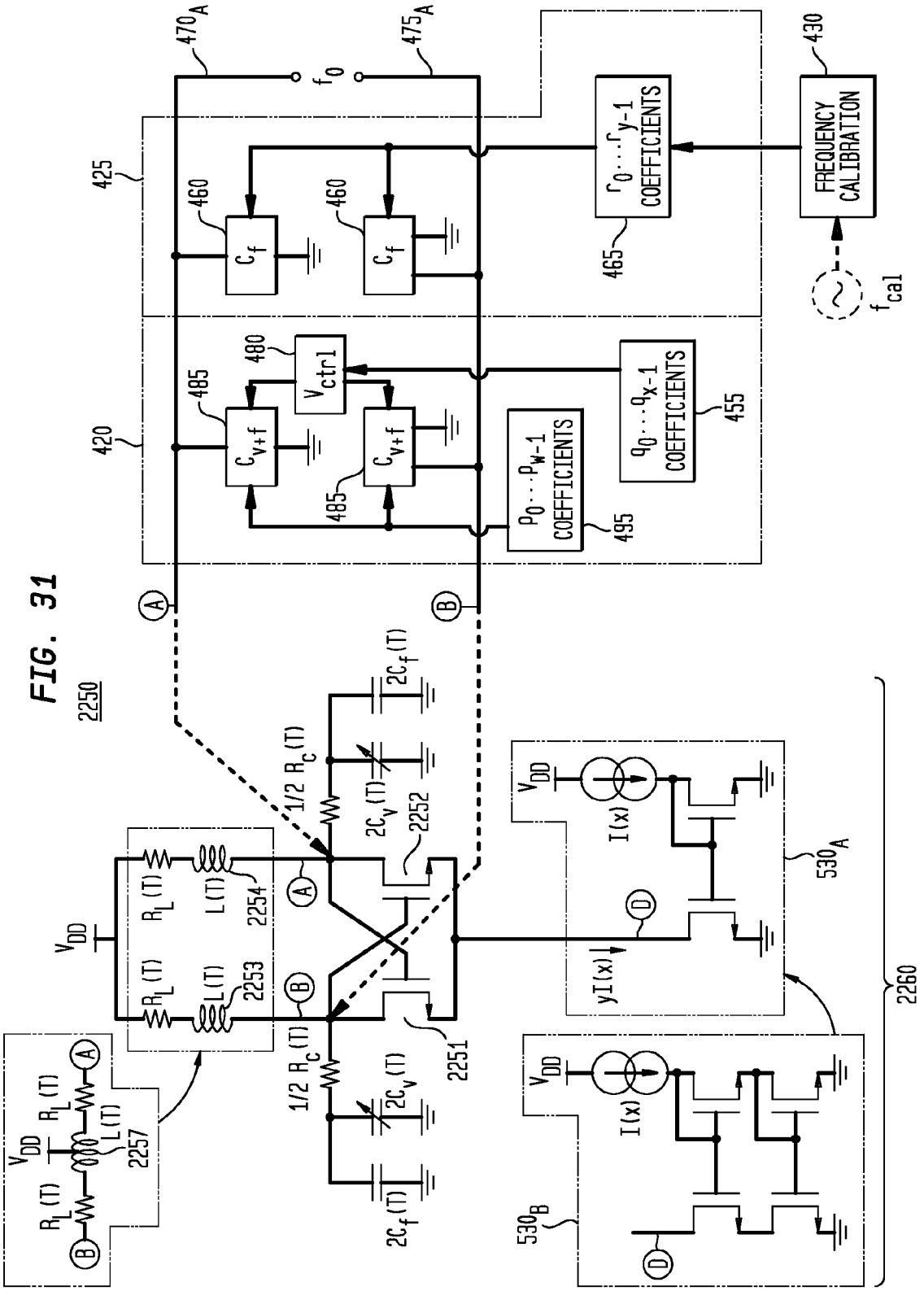
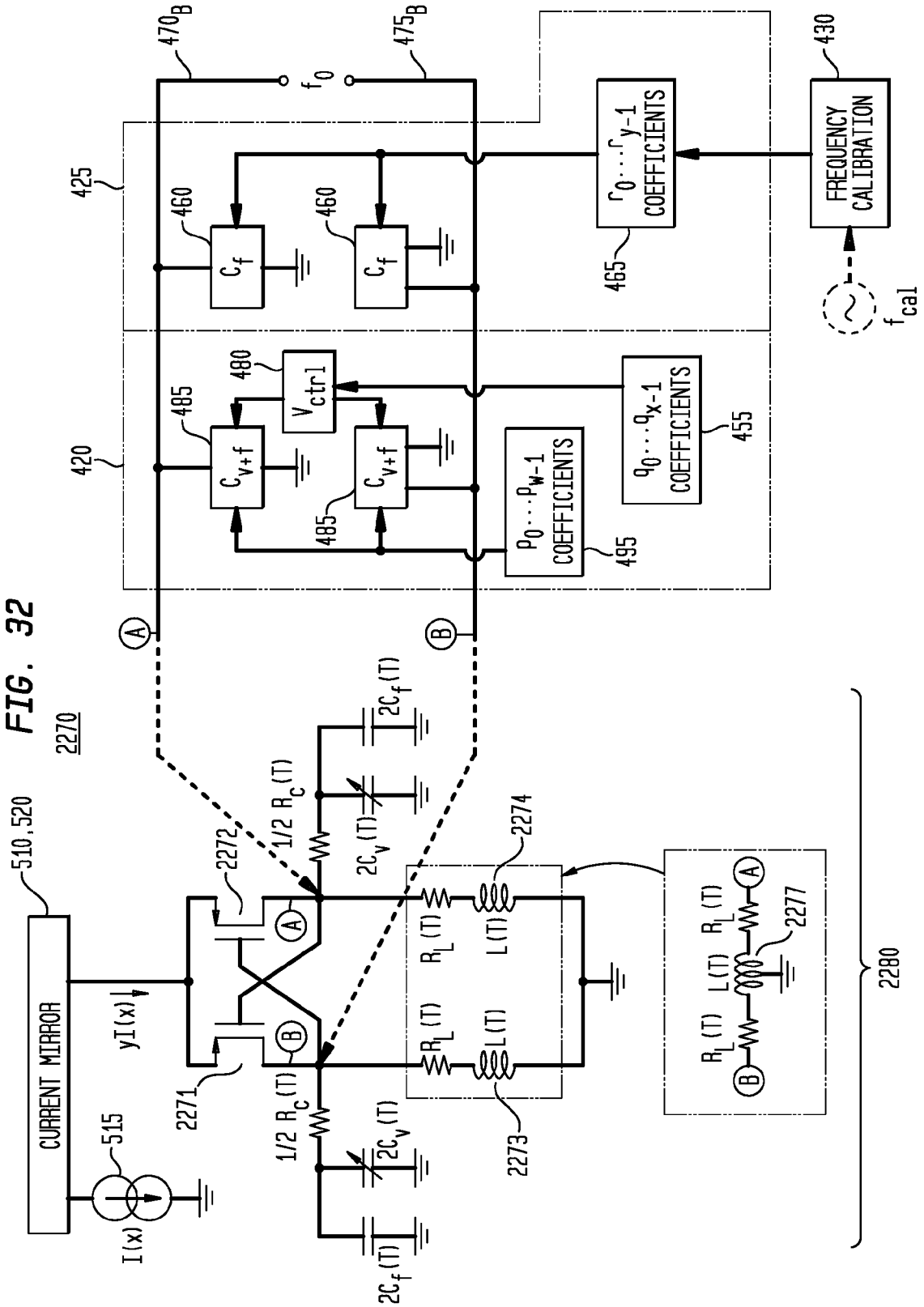

2250
470A
475A
f0
425
420
460
460
Cf
Cf
485
485
480
Vctrl
Cv+f
Cv+f
r0...ry-1 COEFFICIENTS
465
q0...qx-1 COEFFICIENTS
455
p0...pw-1 COEFFICIENTS
495
FREQUENCY CALIBRATION
430
fcal
A
B
VDD
RL(T)
L(T)
2254
2253
2257
1/2 Rc(T)
2Cv(T)
2Cf(T)
2252
2251
I(x)
yI(x)
D
530A
530B
2260

FIG. 31



CURRENT MIRROR
510,520
515
I(x)
yI(x)
2271
2272
2273
2274
2277
2280
1/2 R_C(T)
$2C_v$(T)
$2C_f$(T)
R_L(T)
L(T)
A
B
C_f
C_{v+f}
V_{ctrl}
$p_0 \cdots p_{w-1}$ COEFFICIENTS
$q_0 \cdots q_{x-1}$ COEFFICIENTS
$r_0 \cdots r_{y-1}$ COEFFICIENTS
FREQUENCY CALIBRATION
f_0
f_{cal}
420
425
430
455
460
465
470B
475B
480
485
495

FIG. 32

2270

FIG. 33

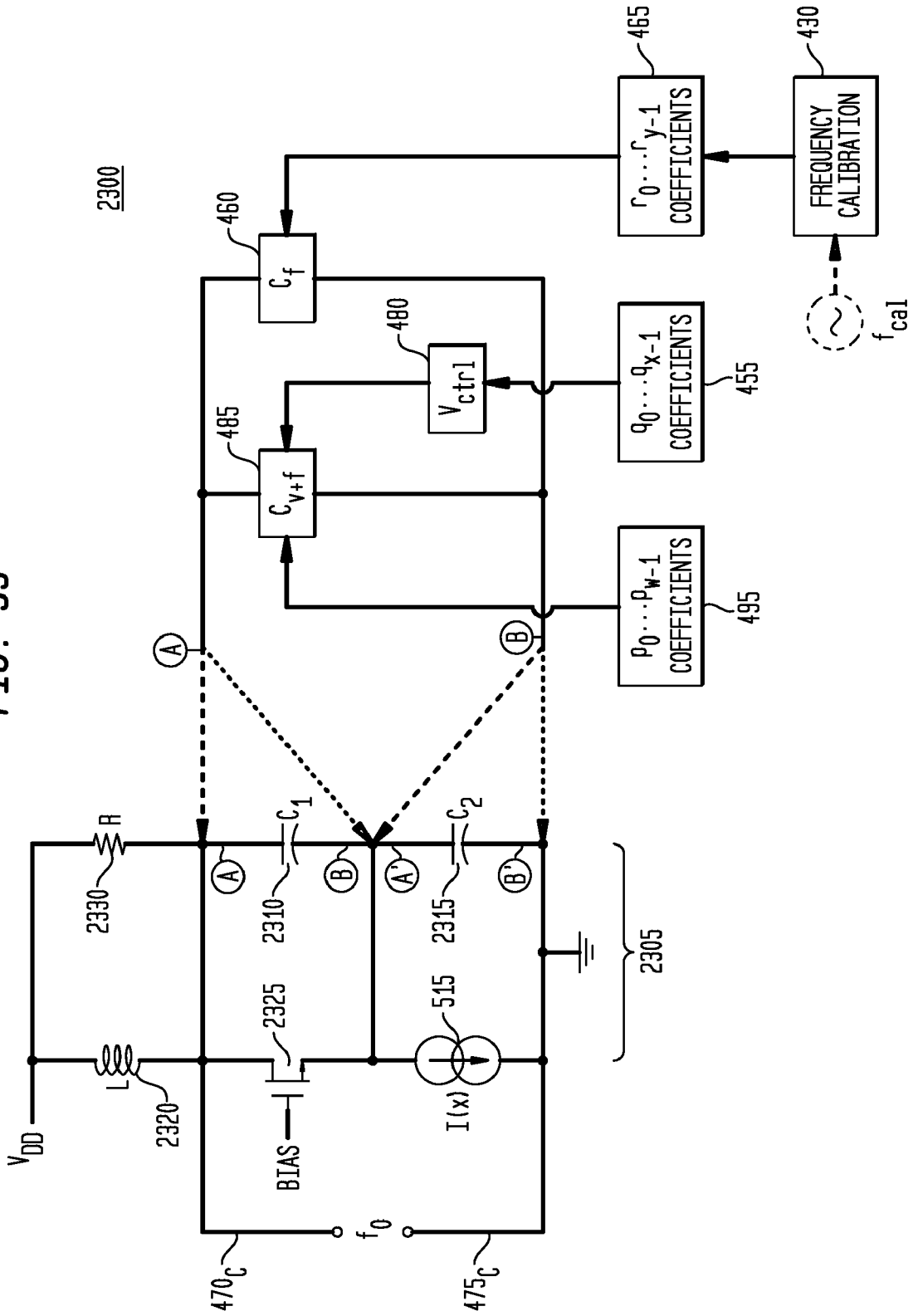

2300
V_{DD}
L
2320
R
2330
2325
BIAS
C_1
2310
C_2
2315
515
I(x)
2305
A
B
A'
B'
f_0
470_C
475_C
C_f
460
V_{ctrl}
480
C_{v+f}
485
$p_0 \cdots p_{w-1}$ COEFFICIENTS
495
$q_0 \cdots q_{x-1}$ COEFFICIENTS
455
$r_0 \cdots r_{y-1}$ COEFFICIENTS
465
FREQUENCY CALIBRATION
430
f_{cal}

FIG. 34

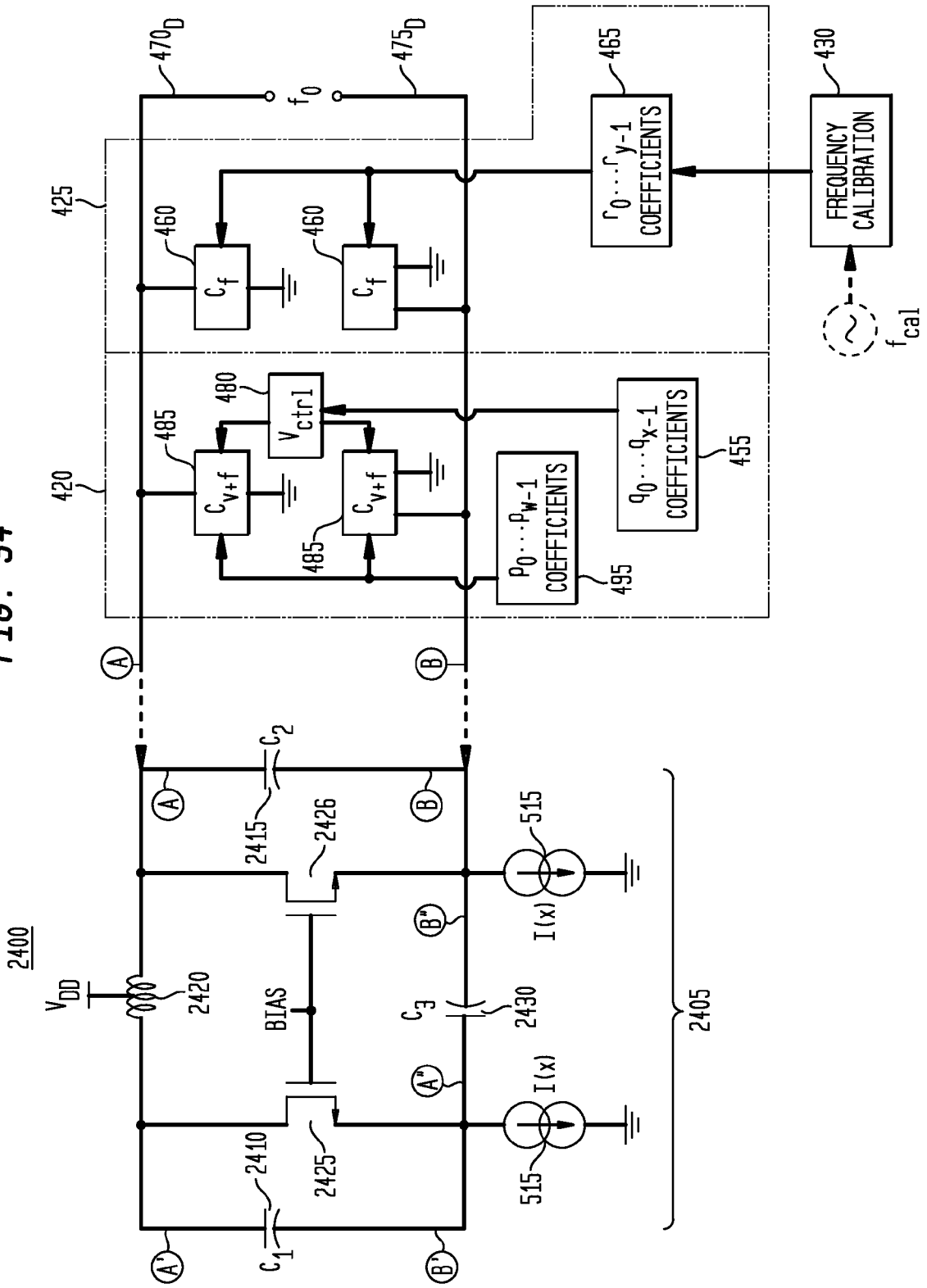

2400
V_{DD}
2420
BIAS
2410
2425
2415
2426
C_1
C_2
C_3
2430
515
I(x)
2405
A'
A
A"
B'
B
B"
420
425
C_{v+f}
485
480
V_{ctrl}
C_f
460
$p_0 \cdots p_{w-1}$ COEFFICIENTS
495
$q_0 \cdots q_{x-1}$ COEFFICIENTS
455
$r_0 \cdots r_{y-1}$ COEFFICIENTS
465
FREQUENCY CALIBRATION
430
f_{cal}
470_D
475_D
f_0

FIG. 35

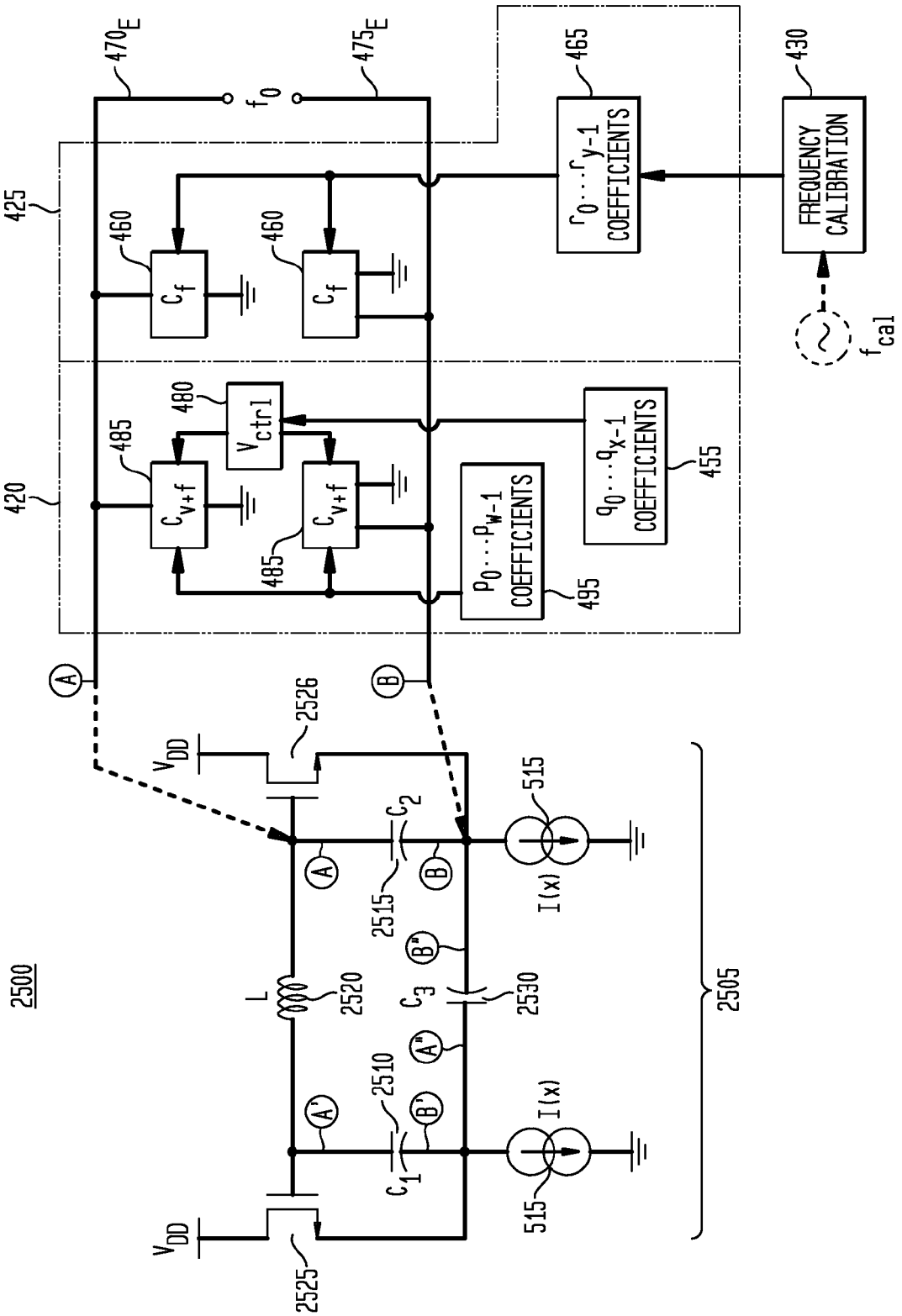

2500
V_{DD}
2525
2510
C_1
A'
B'
515
I(x)
L
2520
C_3
2530
A"
B"
2515
C_2
2526
A
B
2505
V_{DD}
C_{v+f}
485
V_{ctrl}
480
$p_0 \cdots p_{w-1}$ COEFFICIENTS
495
$q_0 \cdots q_{x-1}$ COEFFICIENTS
455
420
425
C_f
460
$r_0 \cdots r_{y-1}$ COEFFICIENTS
465
FREQUENCY CALIBRATION
430
f_{cal}
f_0
470_E
475_E

FIG. 36

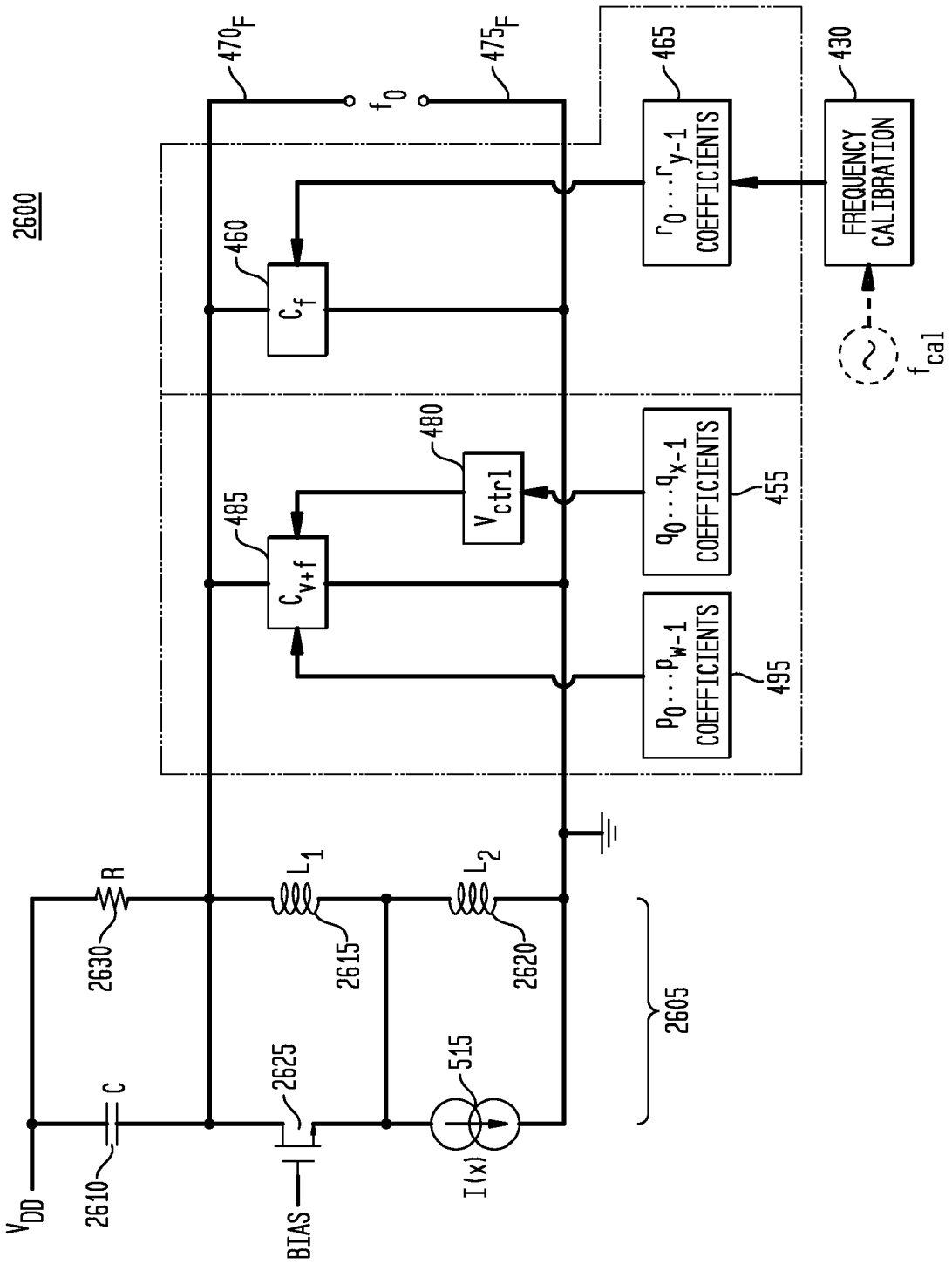

2600
470F
475F
f0
460
Cf
465
r0...ry-1
COEFFICIENTS
430
FREQUENCY
CALIBRATION
fcal
480
Vctrl
485
Cv+f
455
q0...qx-1
COEFFICIENTS
495
p0...pw-1
COEFFICIENTS
R
2630
L1
2615
L2
2620
2605
VDD
2610
C
2625
BIAS
515
I(x)

FIG. 37

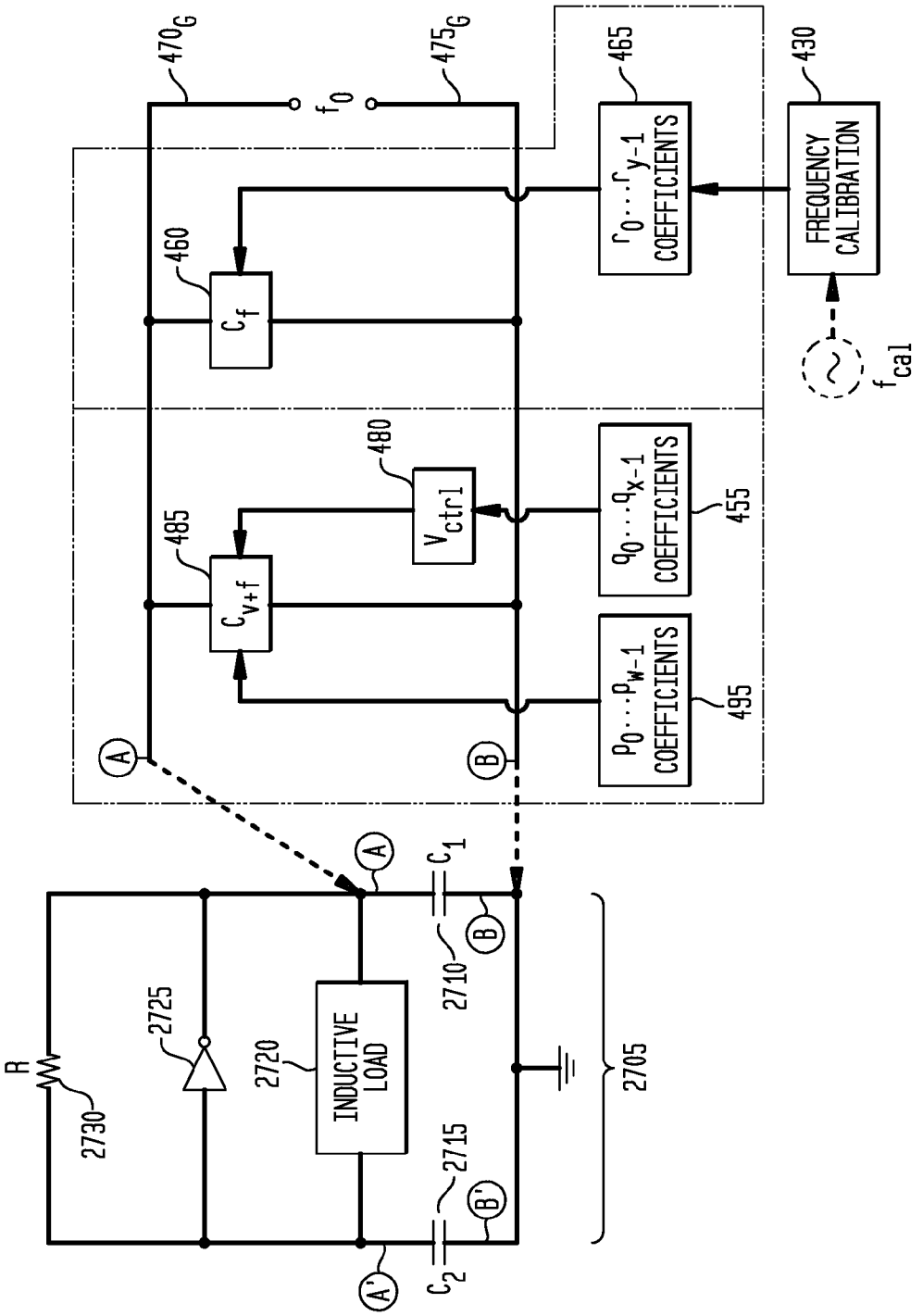
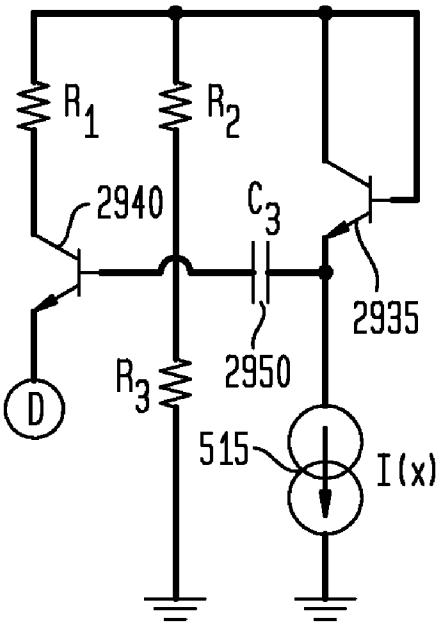
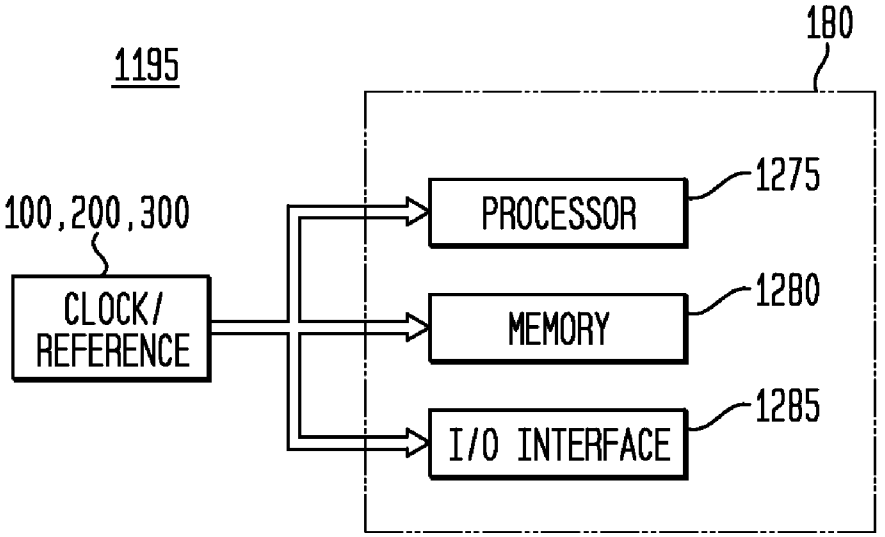

2700
470_G
475_G
f_0
465
430
$r_0 \cdots r_{y-1}$ COEFFICIENTS
FREQUENCY CALIBRATION
460
C_f
f_{cal}
480
V_{ctrl}
485
C_{v+f}
$q_0 \cdots q_{x-1}$ COEFFICIENTS
455
$p_0 \cdots p_{w-1}$ COEFFICIENTS
495
A
B
A
C_1
B
2710
R
2725
2720
INDUCTIVE LOAD
2730
2705
2715
B'
A'
C_2

FIG. 38



2910

FIG. 39



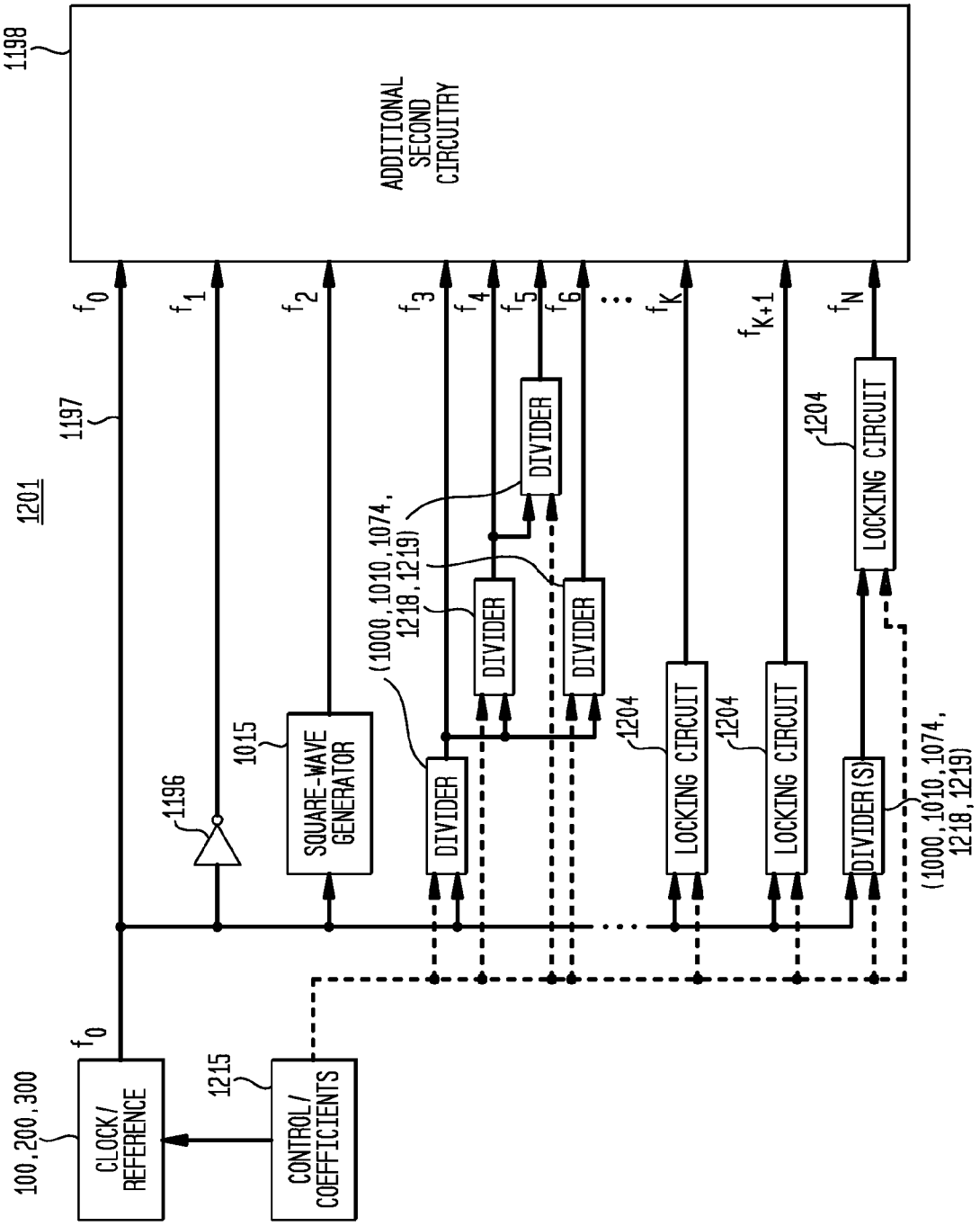

1198
ADDITIONAL SECOND CIRCUITRY
1201
1197
f_0
f_1
f_2
f_3
f_4
f_5
f_6
f_K
f_{K+1}
f_N
1196
1015
SQUARE-WAVE GENERATOR
DIVIDER
DIVIDER
DIVIDER
DIVIDER
(1000, 1010, 1074, 1218, 1219)
1204
LOCKING CIRCUIT
1204
LOCKING CIRCUIT
1204
LOCKING CIRCUIT
DIVIDER(S)
(1000, 1010, 1074, 1218, 1219)
100, 200, 300
CLOCK/ REFERENCE
f_0
1215
CONTROL/ COEFFICIENTS

FIG. 40

FIG. 41

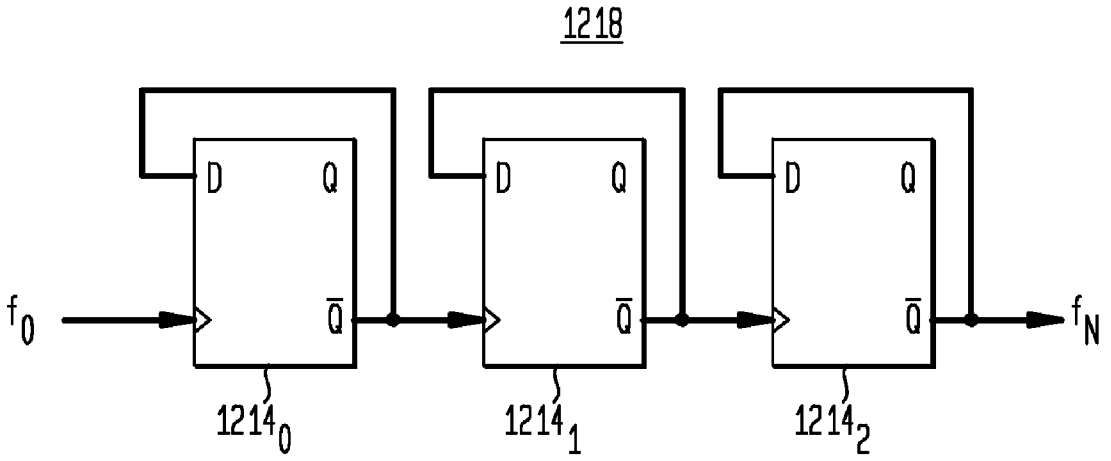

1218
D
Q
Q̄
f_0
f_N
1214_0
1214_1
1214_2

FIG. 42

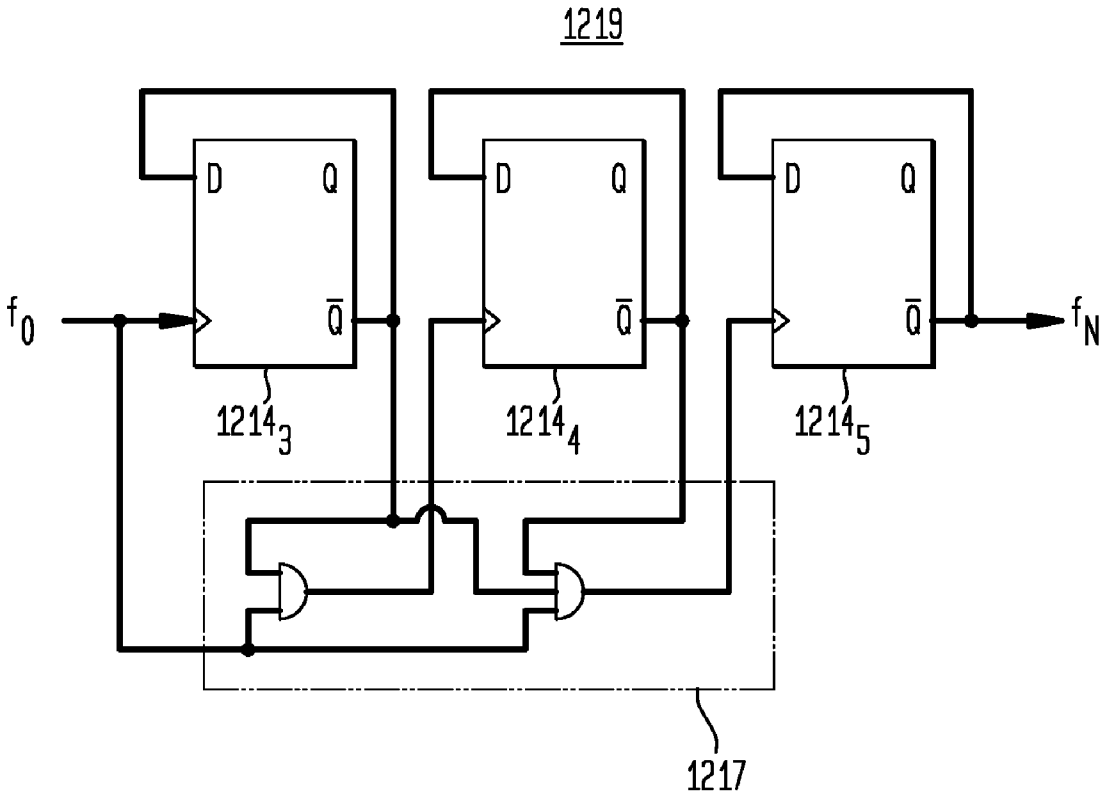
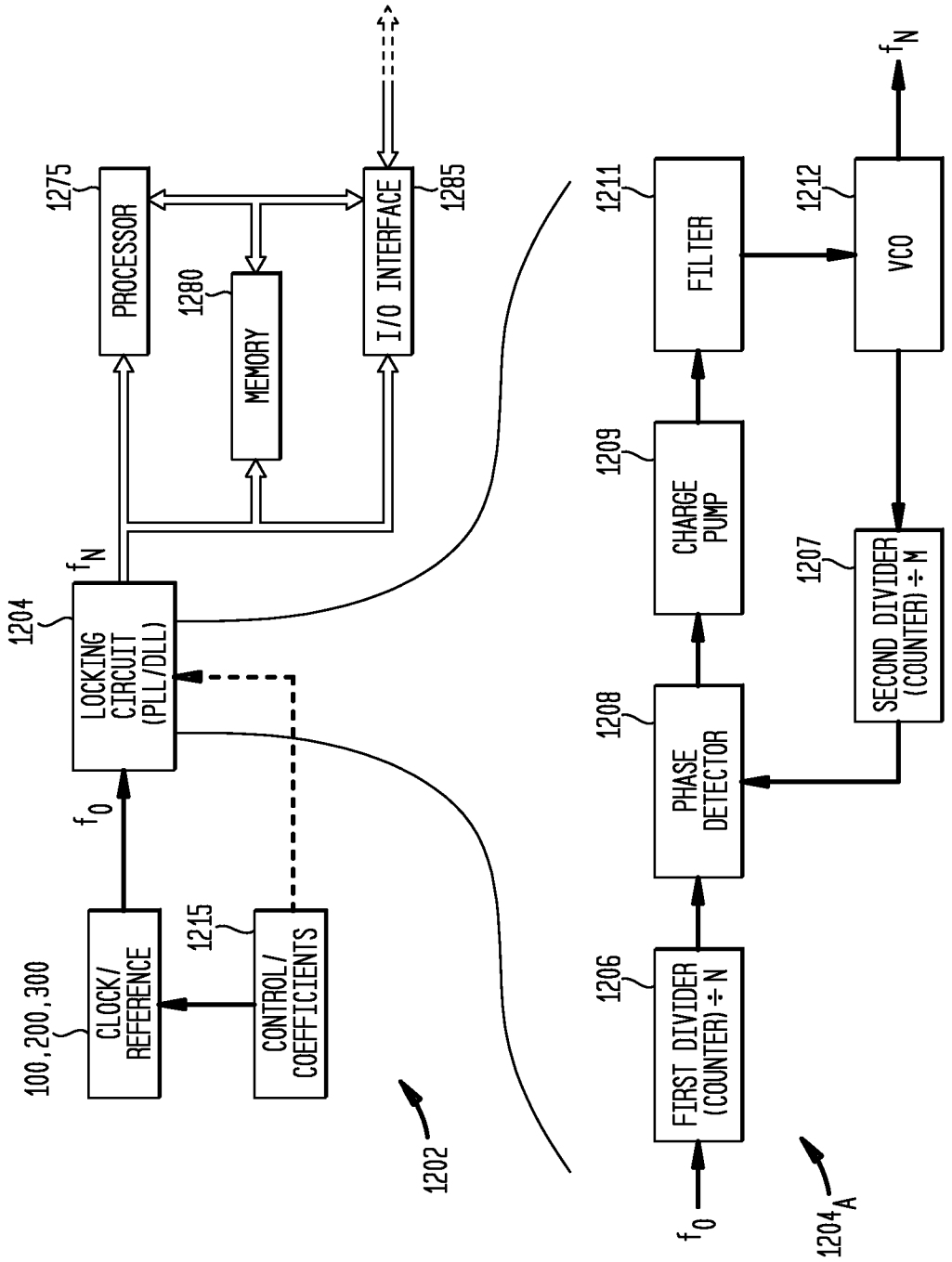

1219
D
Q
Q̄
f_0
f_N
1214_3
1214_4
1214_5
1217

FIG. 43


100,200,300
CLOCK/ REFERENCE
1215
CONTROL/ COEFFICIENTS
f_0
1204
LOCKING CIRCUIT (PLL/DLL)
f_N
1275
PROCESSOR
1280
MEMORY
1285
I/O INTERFACE
1202
1206
FIRST DIVIDER (COUNTER) ÷ N
1208
PHASE DETECTOR
1209
CHARGE PUMP
1211
FILTER
1212
VCO
1207
SECOND DIVIDER (COUNTER) ÷ M
f_0
f_N
1204_A

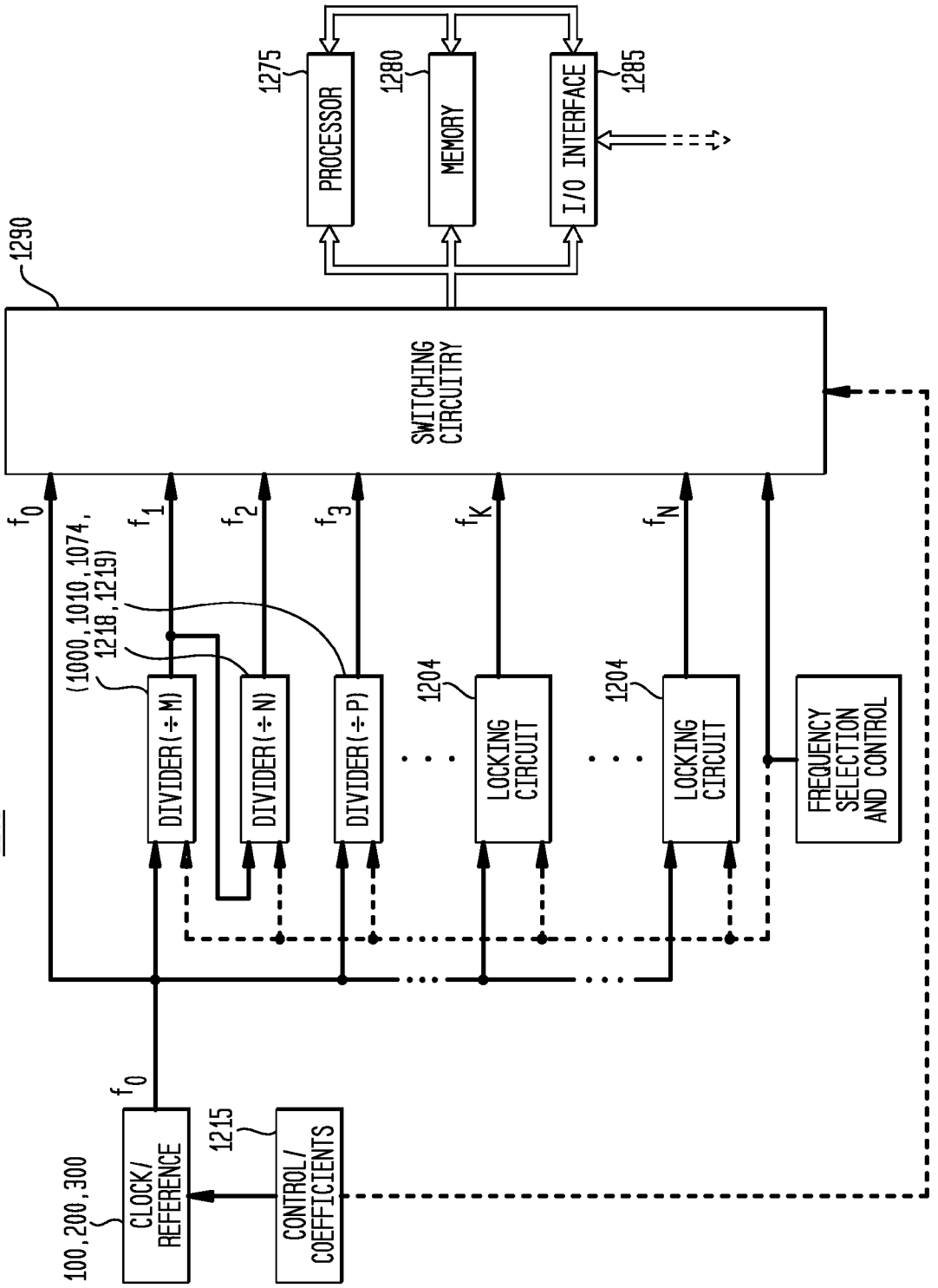

1203
1275
PROCESSOR
1280
MEMORY
1285
I/O INTERFACE
1290
SWITCHING CIRCUITRY
f_0
f_1
f_2
f_3
f_K
f_N
(1000, 1010, 1074, 1218, 1219)
DIVIDER (÷ M)
DIVIDER (÷ N)
DIVIDER (÷ P)
1204
LOCKING CIRCUIT
1204
LOCKING CIRCUIT
FREQUENCY SELECTION AND CONTROL
f_0
100, 200, 300
CLOCK/ REFERENCE
1215
CONTROL/ COEFFICIENTS

FIG. 44

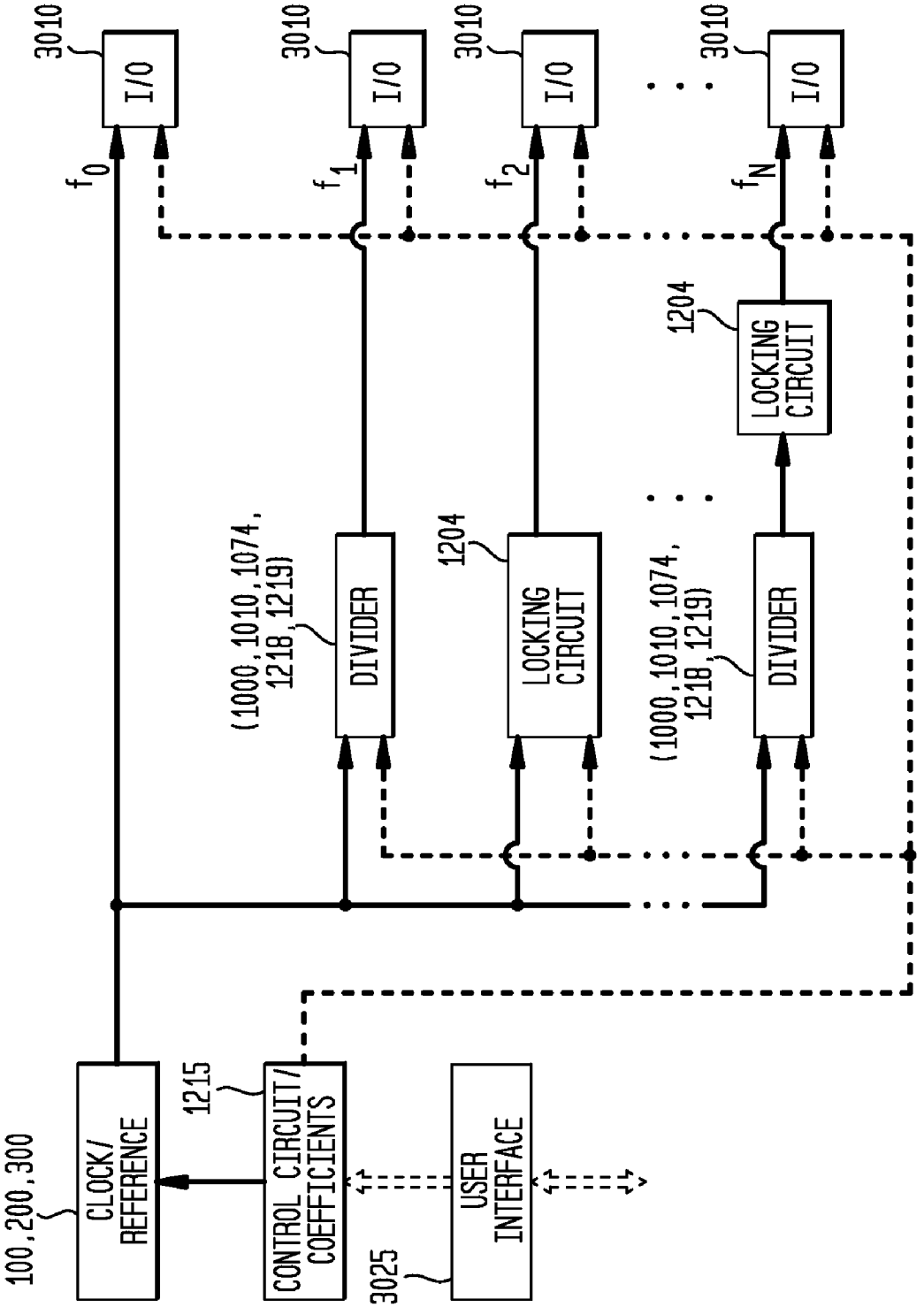

3000
3010
I/O
f_0
f_1
f_2
f_N
(1000,1010,1074,
1218,1219)
DIVIDER
1204
LOCKING
CIRCUIT
100,200,300
CLOCK/
REFERENCE
1215
CONTROL CIRCUIT/
COEFFICIENTS
3025
USER
INTERFACE

FIG. 45

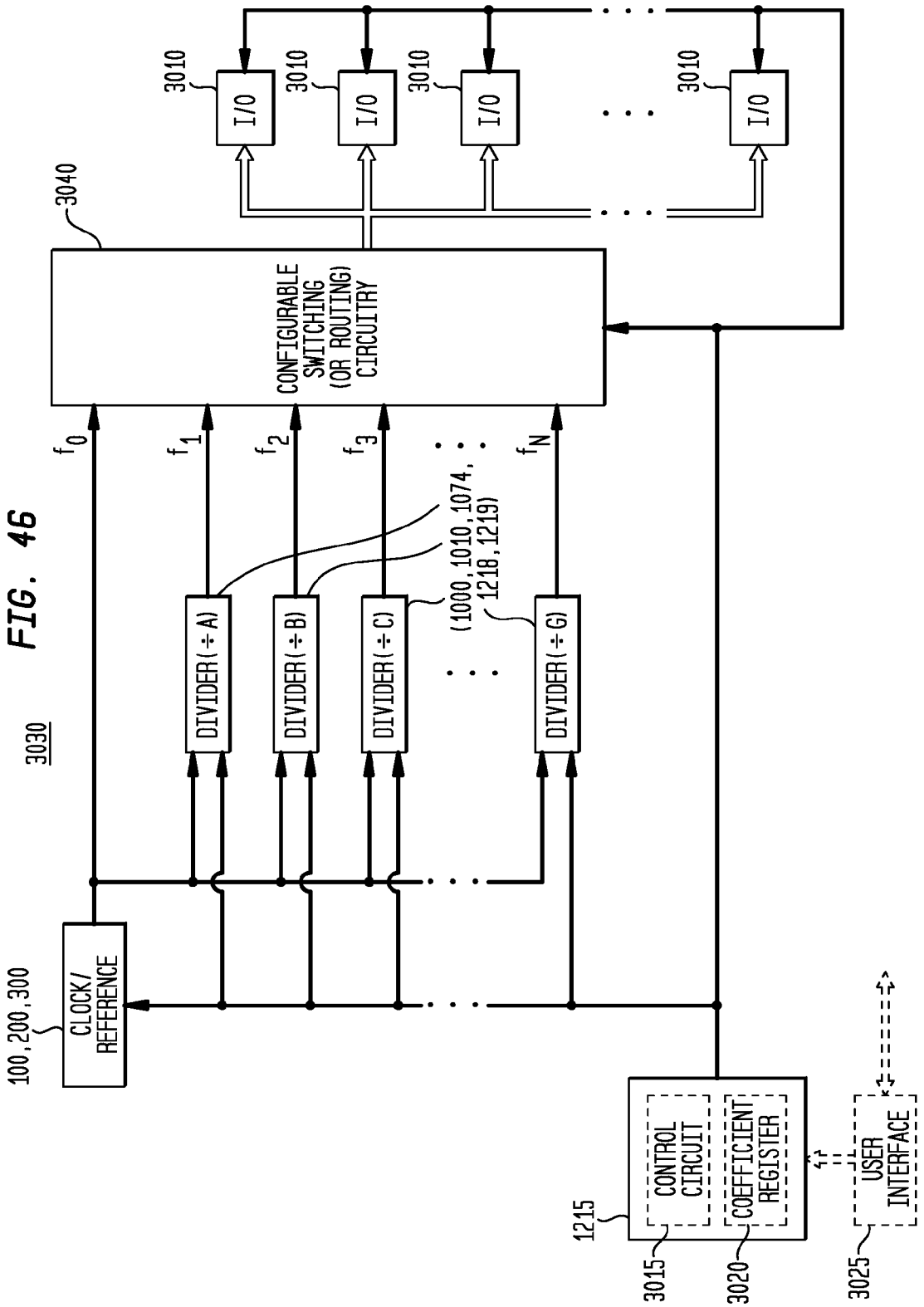

3010
I/O
3010
I/O
3010
I/O
3010
I/O
3040
CONFIGURABLE SWITCHING (OR ROUTING) CIRCUITRY
f_0
f_1
f_2
f_3
f_N
(1000, 1010, 1074, 1218, 1219)
DIVIDER(÷ A)
DIVIDER(÷ B)
DIVIDER(÷ C)
DIVIDER(÷ G)
3030
100, 200, 300
CLOCK/ REFERENCE
1215
CONTROL CIRCUIT
COEFFICIENT REGISTER
USER INTERFACE
3015
3020
3025

FIG. 46

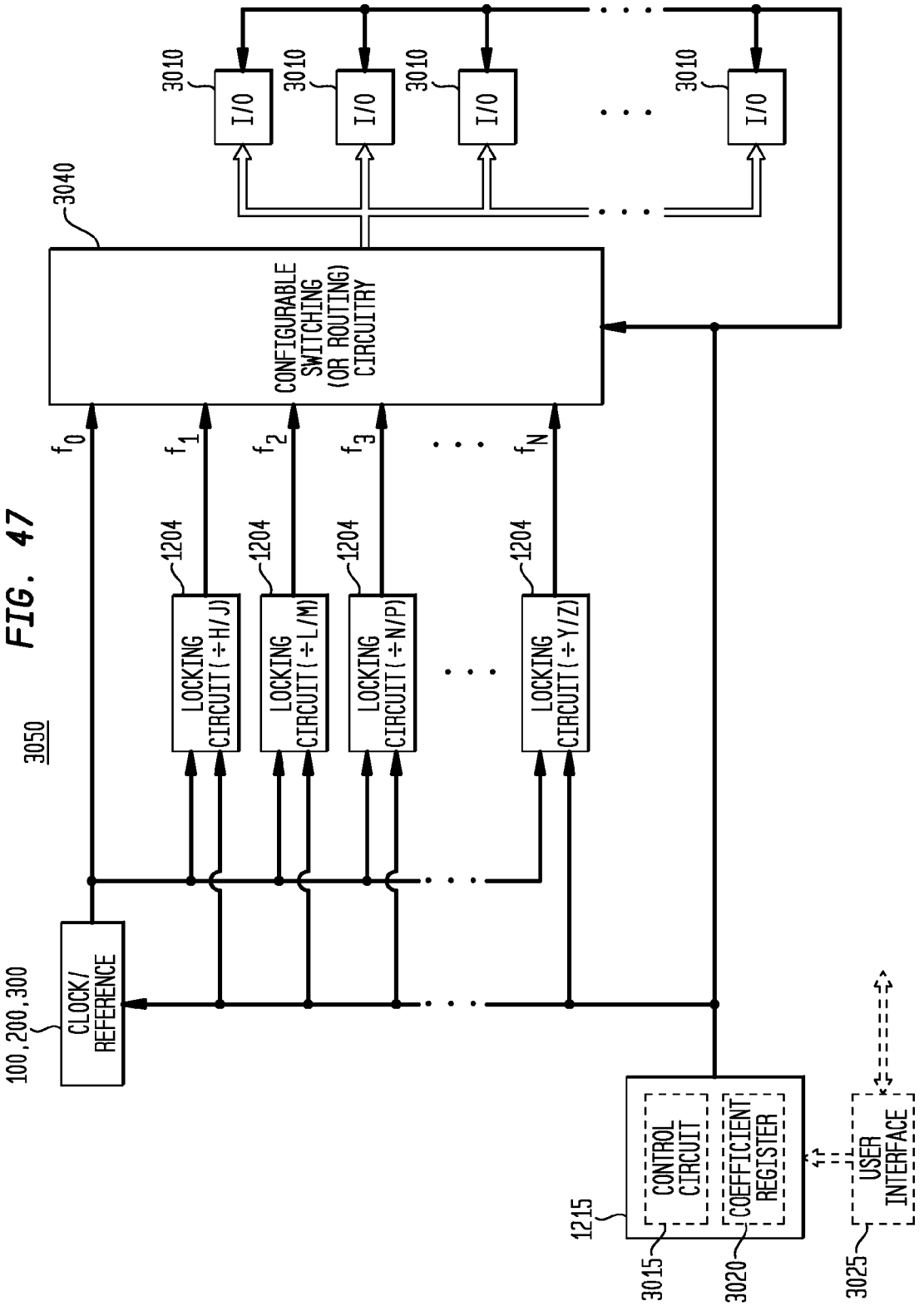

3010
I/O
3010
I/O
3010
I/O
3010
I/O
3040
CONFIGURABLE SWITCHING (OR ROUTING) CIRCUITRY
f_0
f_1
f_2
f_3
f_N
1204
LOCKING CIRCUIT (÷H/J)
1204
LOCKING CIRCUIT (÷L/M)
1204
LOCKING CIRCUIT (÷N/P)
1204
LOCKING CIRCUIT (÷Y/Z)
3050
100,200,300
CLOCK/ REFERENCE
1215
CONTROL CIRCUIT
COEFFICIENT REGISTER
USER INTERFACE
3015
3020
3025

FIG. 47

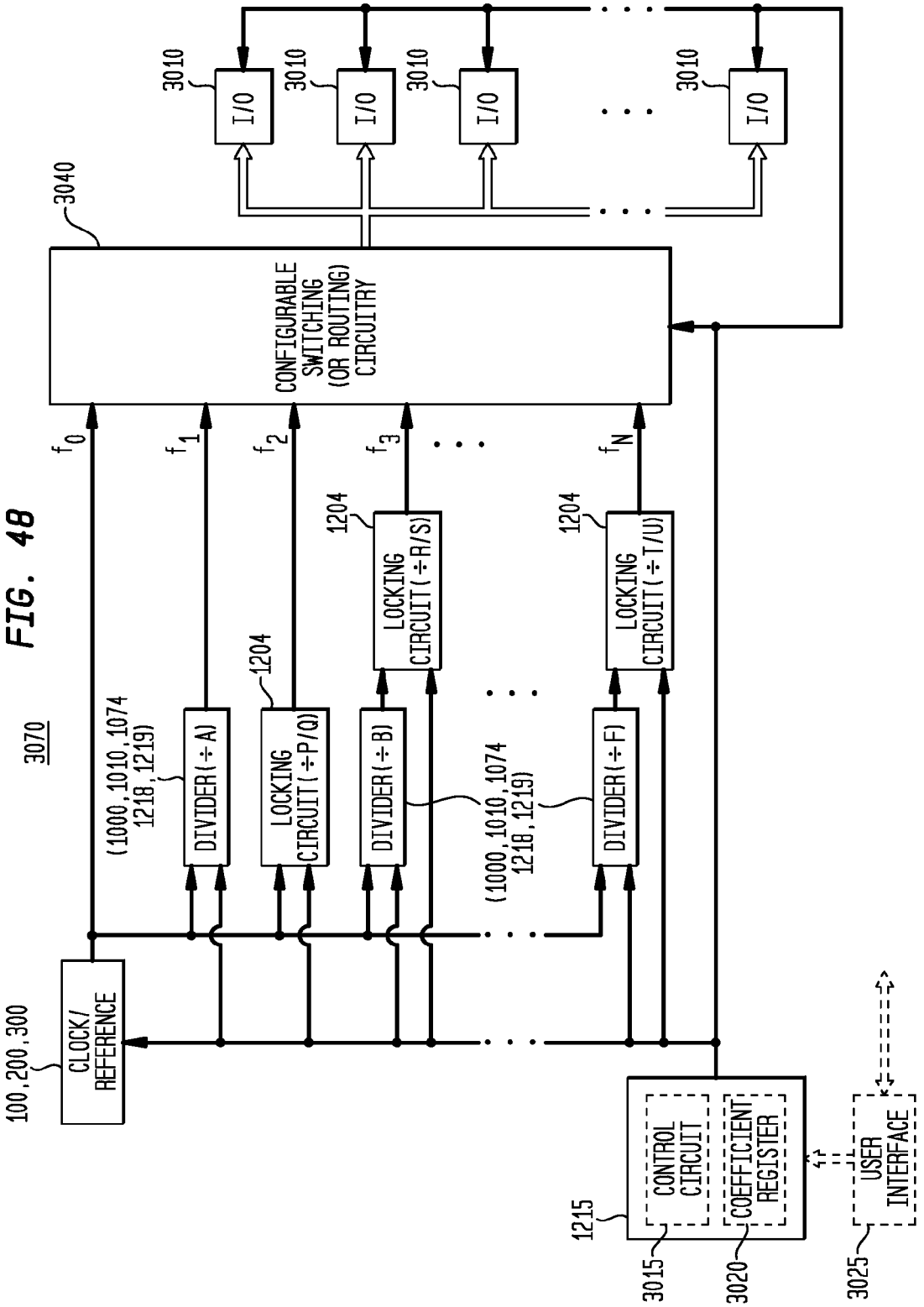

3010
I/O
3010
I/O
3010
I/O
3010
I/O
3040
CONFIGURABLE SWITCHING (OR ROUTING) CIRCUITRY
f_0
f_1
f_2
f_3
f_N
1204
LOCKING CIRCUIT(÷R/S)
1204
LOCKING CIRCUIT(÷T/U)
1204
LOCKING CIRCUIT(÷P/Q)
3070
(1000,1010,1074 1218,1219)
DIVIDER(÷A)
DIVIDER(÷B)
(1000,1010,1074 1218,1219)
DIVIDER(÷F)
100,200,300
CLOCK/ REFERENCE
1215
CONTROL CIRCUIT
COEFFICIENT REGISTER
USER INTERFACE
3015
3020
3025

FIG. 48

DISCRETE CLOCK GENERATOR AND TIMING/FREQUENCY REFERENCE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to and is a continuation of McCorquodale, Michael S. et al., U.S. patent application Ser. No. 11/384,973, filed Mar. 20, 2006, entitled "Discrete Clock Generator and Timing/Frequency Reference", which is commonly assigned herewith, the contents of all of which are incorporated herein in their entireties by reference, and with priority claimed for all commonly disclosed subject matter.

U.S. patent application Ser. No. 11/384,973, filed Mar. 20, 2006, claims priority to and is a continuation-in-part of McCorquodale, Michael S. et al., U.S. patent application Ser. No. 11/232,407, filed Sep. 20, 2005, entitled "Frequency Controller for a Monolithic Clock Generator and Timing/Frequency Reference", which is a continuation-in-part of and claims priority to McCorquodale, Michael S. et al., U.S. patent application Ser. No. 11/084,962, filed Mar. 21, 2005, entitled "Monolithic Clock Generator and Timing/Frequency Reference", now U.S. Pat. No. 7,227,423, which further claims priority to McCorquodale, Michael S. et al., U.S. Provisional Patent Application Ser. No. 60/555,193, filed Mar. 22, 2004, entitled "Monolithic and Top-Down Clock Synthesis with Micromachined Radio Frequency Reference", which are commonly assigned herewith, the contents of all of which are incorporated herein in their entireties by reference, and with priority claimed for all commonly disclosed subject matter.

U.S. patent application Ser. No. 11/384,973, filed Mar. 20, 2006, is also a continuation-in-part of and claims priority to McCorquodale, Michael S. et al., U.S. patent application Ser. No. 11/084,962, filed Mar. 21, 2005, entitled "Monolithic Clock Generator and Timing/Frequency Reference", now U.S. Pat. No. 7,227,423, which further claims priority to McCorquodale, Michael S. et al., U.S. Provisional Patent Application Ser. No. 60/555,193, filed Mar. 22, 2004, entitled "Monolithic and Top-Down Clock Synthesis with Micromachined Radio Frequency Reference", and is also related to and claims priority to McCorquodale, Michael S. et al., U.S. patent application Ser. No. 11/085,372, filed Mar. 21, 2005, entitled "Transconductance and Current Modulation for Resonant Frequency Control and Selection", now U.S. Pat. No. 7,227,424, which further claims priority to U.S. Provisional Patent Application Ser. No. 60/555,193, which are commonly assigned herewith, the contents of all of which are incorporated herein in their entireties by reference, and with priority claimed for all commonly disclosed subject matter.

FIELD OF THE INVENTION

The present invention, in general, relates to oscillation or clocking signal generation, and more particularly, relates to a discrete clock signal generator and timing/frequency reference which is free-running, self-referenced, accurate over fabrication process, voltage and temperature, has low jitter.

BACKGROUND OF THE INVENTION

Accurate clock generators or timing references have generally relied upon crystal oscillators, such as quartz oscillators, which provide a mechanical, resonant vibration at a particular frequency. The difficulty with such crystal oscillators is that they cannot be fabricated as part of the same integrated circuit ("IC") that is to be driven by their clock

signal. For example, microprocessors such as the Intel Pentium processor require a separate clock IC. As a consequence, virtually every circuit requiring an accurate clock signal requires an off-chip clock generator.

There are several consequences for such non-integrated solutions. For example, because such a processor must be connected through outside circuitry (such as on a printed circuit board (PCB)), power dissipation is comparatively increased. In applications which rely on a finite power supply, such as battery power in mobile communications, such additional power dissipation is detrimental.

In addition, such non-integrated solutions, by requiring an additional IC, increase space and area requirements, whether on the PCB or within the finished product, which is also detrimental in mobile environments. Moreover, such additional components increase manufacturing and production costs, as an additional IC must be fabricated and assembled with the primary circuitry (such as a microprocessor).

Other clock generators which have been produced as integrated circuits with other circuits are generally not sufficiently accurate, particularly over fabrication process, voltage, and temperature ("PVT") variations. For example, ring, relaxation and phase shift oscillators may provide a clock signal suitable for some low-sensitivity applications, but have been incapable of providing the higher accuracy required in more sophisticated electronics, such as in applications requiring significant processing capability or data communications. In addition, these clock generators or oscillators often exhibit considerable frequency drift, jitter, have a comparatively low Q-value, and are subject to other distortions from noise and other interference.

As a consequence, a need remains for a clock generator or timing reference which may be integrated monolithically with other circuitry, as a single IC, and which is highly accurate over PVT variations. Such a clock generator or timing reference should be free-running and self-referencing, and should not require locking or referencing to another reference signal. Such a clock generator or timing reference should exhibit minimal frequency drift and have comparatively low jitter, and should be suitable for applications requiring a highly accurate system clock. Such a clock generator or timing reference should also provide multiple operating modes, including a clock mode, a reference mode, a power conservation mode, and a pulsed mode. Lastly, such a clock generator or timing reference should provide for control over output frequency, to provide a stable and desired frequency in response to variation in ambient or junction temperature or variation in other parameters such as voltage, fabrication process, frequency, and age.

SUMMARY OF THE INVENTION

In various exemplary embodiments, the invention provides an apparatus which generates a frequency reference signal. The apparatus comprises a resonator, which may be implemented using one or more inductors and capacitors (as an "LC-tank"), a transconductance amplifier, a frequency controller and a temperature compensator for use in providing open-loop frequency control and selection for a low-jitter, free-running and self-referencing clock generator and/or a timing and frequency reference which is highly accurate over PVT and aging (time) variations and which can be integrated monolithically with other circuitry, to form a singular integrated circuit. No separate reference oscillator is required, and the exemplary embodiments are not phase-locked, delay-locked or otherwise locked to any other frequency reference. Instead, the exemplary embodiments may be utilized as such

a reference oscillator which generates a frequency reference signal, which may then be locked to by one or more phase-locked or delay-locked loops. Various exemplary embodiments of the invention include features for highly accurate frequency generation over fabrication process, voltage, and temperature ("PVT") variations. These features include frequency tuning and selection, and compensation for frequency variations which may be caused due to temperature and/or voltage fluctuations, fabrication process variations, and variations due to aging of the integrated circuitry.

The invention may be provided as a discrete integrated circuit which provides a clock signal or other frequency reference signal, which may then be combined with other integrated circuits for any user application. The inventive apparatus may be configured or programmed for frequency selection, signal selection, input/output ("I/O") selection, I/O pin selection, spread-spectrum selection, and other options. Several methods are provided for such configuration and programming, including mask programmability during IC design and fabrication, manufacturer or distributor programmability post-fabrication of the IC, and user programmability post-fabrication of the IC.

The invention also may be combined with other integrated circuits to form a singular component, typically provided in a single IC package. For example, the inventive clock generator and/or a timing and frequency reference may be combined with any other, second circuitry, of any kind or type, for any function or application, such as various processors, controllers, digital signal processors, and so on, to provide an integrated, free-running clock for the second circuitry which does not require synchronization or locking to an external reference such as a crystal oscillator.

For example and without limitation, the clock generator and/or a timing and frequency reference may be combined with any of the following types of processors: a microprocessor; a digital signal processor; a controller; a microcontroller; a universal serial bus (USB) controller; a Peripheral Component Interconnect (PCI) controller; a Peripheral Component Interconnect Express (PCI-e) controller; a Firewire controller; an AT Attachment (ATA) interface controller, an Integrated Drive Electronics (IDE) controller; a Small Computer Systems Interface (SCSI) controller; a television controller; a local area network (LAN) controller; an Ethernet controller; a video controller; an audio controller; a modem processor; an MPEG controller; a multimedia controller; a communication controller; a mobile communication controller; an IEEE 802.11 controller; a GSM controller; a GPRS controller; a PCS controller; an AMPS controller; a CDMA controller; a WCDMA controller; a spread spectrum controller; a wireless LAN controller; an IEEE 802.11 controller; a DSL controller; a T1 controller; a ISDN controller; or a cable modem controller. Innumerable other types of second circuitry for integration with the inventive clock generator and/or a timing and frequency reference are also within the scope of the invention.

For such exemplary embodiments, the clock generator and/or a timing and frequency reference provides a first reference signal having a first frequency f_0. The first reference signal may be utilized in any of a plurality of ways, such as: (1) utilized directly by second circuitry as a clocking or frequency reference signal; (2) provided to one or more square-wave generators or divider circuits, with the resulting substantially square or divided signal(s) provided as output (as one or more second reference signals at a selected frequency or frequencies (e.g., having frequencies f_0, f_1, f_2, through f_K), any one or more of which are then utilized by second circuitry as a clocking or frequency reference signal; (3) utilized for locking by a locking circuit, such as one or more phase-locked loops, delay-locked loops, or injection locking circuits, or by a combination of dividers and locking circuits, also to provide as output one or more second reference signals, at a selected frequency or frequencies (e.g., having frequencies f_{K+1}, f_{K+2}, through f_N), to second circuitry.

These one or more second reference signals can be switched, multiplexed or provided directly to any second circuitry, such as a processor, memory and input/output interface, as a clock or reference signal at a selected frequency. These signals may also be provided in any of a plurality of forms, such as single-ended, differential, phase-shifted, quadrature, including in inverted and/or non-inverted forms.

Frequency selection for any of the frequencies f_0, f_1, f_2, through f_N) may be provided in a plurality of ways, depending upon the selected embodiment. The frequency selection may occur as part of design and fabrication, such as through selection of the number and size of inductors and capacitors utilized in the LC oscillator of the clock generator and/or a timing and frequency reference. For example, the size(s) and/or shape(s) of the one or more inductors may be selected through a suitable metal layer mask, and capacitors may be sized for generation of particular frequencies or range of frequencies. Frequency selection also may occur post-fabrication, through the use of the various calibration and control coefficients or signals, discussed in greater detail below. In addition, frequency selection may be performed through the configuration of the one or more locking circuits, such as through selection of the divide ratio(s) through programmable counters in phase-locked loops, which may be as part of the design and fabrication of the IC, or may be programmed post-fabrication, also through use of calibration and control coefficients or signals, or by switching dividers in or out of the divide chain. Additional configuration methods are discussed in greater detail below.

Additional embodiments also provide for generating a plurality of frequency reference signals, whether sinusoidal or square-wave, such as for use as one or more clock signals or reference frequency sources. In exemplary embodiments, the clock/frequency reference of the invention is coupled to one or more phase-locked loops ("PLLs") or delay-locked loops ("DLLs), to provide a corresponding plurality of output reference signals at selected frequencies. Various exemplary embodiments may be configurable or programmable, through control signals or stored coefficients, such as to adjust the divide ratios of the PLLs or DLLs for corresponding frequency selection.

For applications potentially requiring a high Q value, low jitter and low phase noise, the resonator typically comprises one or more inductors and capacitors, forming one or more LC-tanks or LC resonators. In a first embodiment, a double-balanced, differential LC oscillator topology is utilized. In other exemplary embodiments, differential or single-ended LC oscillator topologies may be utilized, such as a differential n-MOS cross-coupled topology; a differential p-MOS cross-coupled topology; a single-ended Colpitts LC oscillator, a single-ended Hartley LC oscillator, a differential Colpitts LC oscillator (both common base and common collector versions), a differential Hartley LC oscillator (also both common base and common collector versions), a single-ended Pierce LC oscillator, a quadrature oscillator (e.g., formed from at least two double-balanced, differential LC oscillators). In any of these embodiments, an active inductor may be utilized in the LC oscillator or in the other reactive components. Any of these LC topologies may be implemented to be balanced, cross-coupled, differential, or single-ended, and may utilize any type of transistors, such as n-MOS, p-MOS, or BJT, for example. Additional LC oscillator topologies, now known or

which become known, are considered equivalent and within the scope of the present invention.

Exemplary embodiments of the present invention also provide several different levels and types of control. For example, both discrete and continuous control are provided, in real time, for control over output frequency of the free-running oscillator in light of such variations. In addition, such control is provided generally as an open-loop, without requiring or necessitating a feedback connection and without requiring continuous locking of the oscillator to another reference signal.

In addition, exemplary embodiments of the invention provide a clock generator and/or a timing and frequency reference having multiple operating modes, including modes such as a power conservation mode, a clock mode, a reference mode, and a pulsed mode. In addition, the various embodiments provide multiple output signals at different frequencies, and provide low-latency and glitch-free switching between these various signals.

Significantly, various exemplary embodiments of the invention generate a significantly and comparatively high frequency, such as in the hundreds of MHz and GHz range, which is then divided to a plurality of lower frequencies. Each such division by "N" (a rational number, as a ratio of integers) results in a significant noise reduction, with phase noise reduced by N and phase noise power reduced by N^2. As a consequence, exemplary embodiments of the invention result in significantly less relative period jitter than other oscillators that generate their output directly or through frequency multiplications.

Various apparatus embodiments include a resonator, an amplifier, and a frequency controller, which may include various components or modules such as a temperature compensator, a process variation compensator, a voltage isolator and/or voltage compensator, an age (time) variation compensator, a frequency divider, and a frequency selector. The resonator provides a first signal having a resonant frequency. A temperature compensator adjusts the resonant frequency in response to temperature, and the process variation compensator adjusts the resonant frequency in response to fabrication process variation. In addition, the various embodiments may also include a frequency divider to divide the first signal having the resonant frequency into a plurality of second signals having a corresponding plurality of frequencies which are substantially equal to or lower than the resonant frequency; and a frequency selector to provide an output signal from the plurality of second signals. The frequency selector may further include a glitch-suppressor. The output signal may be provided in any of various forms, such as differential or single-ended, and substantially square-wave or sinusoidal.

Exemplary embodiments of the present invention provide an apparatus for frequency control of an integrated, free-running harmonic oscillator, comprising a resonator adapted to provide a first signal having a resonant frequency; a sensor adapted to provide a second signal, such as a control voltage, in response to at least one parameter of a plurality of parameters; and a frequency controller coupled to the sensor and couplable to the resonator, with the frequency controller adapted to modify a reactance element coupled to the resonator in response to the second signal to modify the resonant frequency. The plurality of parameters are variable and comprise at least one of the following parameters: temperature, fabrication process, voltage, frequency, and age (i.e., elapsed time).

In the exemplary embodiments, the frequency controller is further adapted to modify an effective reactance or impedance element coupled to the resonator in response to the second signal, such as modifying a total capacitance of the resonator in response to the second signal, coupling to the resonator or decoupling from the resonator a fixed or variable capacitance, modifying an effective reactance of the resonator by varying or switching a varactor to a selected control voltage, or equivalently, modifying an inductance or resistance of the resonator in response to the second signal, such as by coupling to the resonator or decoupling from the resonator a fixed or variable inductance or resistance. In other embodiments, differentially weighted or sized reactances, such as variable capacitors (varactors), may be switched to or from the resonator, switched to or from a plurality of different, selectable control voltages, or both. For example, in selected embodiments, the reactance of one or more variable capacitors which are coupled to the resonator may be varied by switching the one or more variable capacitors to a selected control voltage, of a plurality of control voltages, resulting in differently or differentially-weighted effective reactances coupled to the resonator.

For example, a plurality of fixed capacitances (having different, binary weighted or otherwise differentially-weighted capacitances), may be coupled to the resonator to provide a discrete level of frequency control, and a varactor coupled to the resonator may be provided with a selected control voltage, of a plurality of control voltages, which varies in response to temperature, which may be utilized to maintain a constant frequency over such temperature fluctuations, and which provides a continuous level of frequency control. In addition, any of such control voltages may either vary in response to a selected parameter, such as temperature, or may be constant with respect to such a parameter. The differing weights of the various reactances utilized may be embodied in a plurality of forms, such as binary weighted, linearly weighted, or weighted utilizing any other desirable scheme, all of which are considered equivalent and within the scope of the present invention.

It should be noted that the terms "fixed" and "variable" are utilized as known in the art, with "fixed" being understood to mean configured generally to be non-varying with respect to a selected parameter, and "variable" meaning configured generally to be varying with respect to the selected parameter. For example, a fixed capacitor generally means that its capacitance does not vary as a function of an applied voltage, while a variable capacitor (varactor) will have a capacitance which does vary as a function of applied voltage. Both, however, may have and generally will have capacitances which vary as a function of fabrication process variation. In addition, a fixed capacitor may be formed as a varactor coupled to a constant voltage, for example. Similarly, components may be coupled to each other either directly or indirectly or, stated another way, operatively coupled or coupled via signal transmission. For example, one component may be coupled to a second component via a third component, such as through a switching arrangement, a divider, a multiplier, etc. Those of skill in the art will recognize these various circumstances and contexts, as illustrated and as discussed below, and what is meant when such terms are utilized.

In the exemplary embodiments, the frequency controller may further comprise: a coefficient register adapted to store a first plurality of coefficients; and a first array having a plurality of switchable capacitive modules coupled to the coefficient register and couplable to the resonator, each switchable capacitive module having a fixed capacitance and a variable capacitance, each switchable capacitive module responsive to a corresponding coefficient of the first plurality of coefficients to switch between the fixed capacitance and the variable capacitance and to switch each variable capacitance to a

control voltage. The plurality of switchable capacitive modules may be binary-weighted. The frequency controller may further comprise a second array having a plurality of switchable resistive modules coupled to the coefficient register and further having a capacitive module, the capacitive module and the plurality of switchable resistive modules further coupled to a node to provide the control voltage, with each switchable resistive module responsive to a corresponding coefficient of a second plurality of coefficients stored in the coefficient register to switch the switchable resistive module to the control voltage node. In selected embodiments, the sensor further comprises a current source responsive to temperature, wherein the current source is coupled through a current mirror to the second array to generate the control voltage across at least one switchable resistive module of the plurality of switchable resistive modules. Also in selected embodiments, the current source has at least one complementary to absolute temperature ("CTAT") configuration, proportional to absolute temperature ("PTAT") configuration, proportional to absolute temperature squared ("$PTAT^2$") configuration, or combinations of these configurations. In addition, each switchable resistive module of the plurality of switchable resistive modules has a different temperature response for a selected current.

In other exemplary embodiments, the sensor is a parameter (temperature, process, voltage, age, etc.) sensor and varies the second signal in response to variation of the selected parameter; for example, the sensor may be a temperature or voltage sensor and varies the second signal in response to temperature or voltage variation. The selected embodiments may also include an analog-to-digital converter coupled to the sensor to provide a digital output signal in response to the second signal, and a control logic block to convert the digital output signal to the first plurality of coefficients.

In other exemplary embodiments, the frequency controller further comprises a process variation compensator couplable to the resonator and adapted to modify the resonant frequency in response to a fabrication process parameter of the plurality of parameters. The process variation compensator may further comprise a coefficient register adapted to store a plurality of coefficients; and an array having a plurality of binary-weighted switchable capacitive modules coupled to the coefficient register and to the resonator, each switchable capacitive module having a first fixed capacitance and a second fixed capacitance, with each switchable capacitive module responsive to a corresponding coefficient of the plurality of coefficients to switch between the first fixed capacitance and the second fixed capacitance. In other exemplary embodiments, the process variation compensator may further comprise a coefficient register adapted to store a plurality of coefficients; and an array having a plurality of switchable variable capacitive modules coupled to the coefficient register and to the resonator, each switchable variable capacitive module responsive to a corresponding coefficient of the plurality of coefficients to switch between a first voltage and a second voltage, such as switching to a selected control voltage.

In other exemplary embodiments, frequency controller further comprises a coefficient register adapted to store a first plurality of coefficients; and a first array having a plurality of switchable, capacitive modules coupled to the coefficient register and couplable to the resonator, each switchable capacitive module having a variable capacitance, each switchable capacitive module responsive to a corresponding coefficient of the first plurality of coefficients to switch the variable capacitance to a selected control voltage of a plurality of control voltages. In other exemplary embodiments, the process variation compensator may further comprise a coefficient register adapted to store at least one coefficient; and at least one switchable variable capacitive module coupled to the coefficient register and to the resonator, which is responsive to the at least one coefficient to switch to a selected control voltage. The sensor may comprises a current source responsive to temperature, and the frequency controller may also include a second array having a plurality of resistive modules coupled through a current mirror to the current source, the plurality of resistive modules adapted to provide the plurality of control voltages, and wherein each resistive module of the plurality of resistive modules has a different response to temperature and is adapted to provide a corresponding control voltage, of the plurality of control voltages, in response to a current from the current source.

In other exemplary embodiments, an apparatus for frequency control of a resonator comprises a coefficient register adapted to store a first plurality of coefficients; and a first array having a plurality of switchable reactance or impedance modules coupled to the coefficient register and to the resonator, each switchable reactance module responsive to a corresponding coefficient of the first plurality of coefficients to switch a corresponding reactance to modify the resonant frequency. The corresponding reactance or impedance may be a fixed or variable inductance, a fixed or variable capacitance, a fixed or variable resistance, or any combination thereof. The corresponding reactance may be switched to the resonator or, when coupled to the resonator, may be switched to a control voltage, a power supply voltage or a ground potential, and the control voltage may be determined by a current source responsive to temperature. For example, the corresponding reactance is variable and is coupled to the resonator and switched to a selected control voltage of a plurality of control voltages. In selected embodiments, the first plurality of coefficients are calibrated or are determined by a sensor responsive to at least one parameter of a plurality of variable parameters, such as temperature, fabrication process, voltage, frequency and age.

In other exemplary embodiments, an apparatus for frequency control of an integrated, free-running harmonic oscillator comprises: a plurality of resistive modules adapted to generate a plurality of control voltages; a plurality of controlled reactance modules coupled to the harmonic oscillator; and a plurality of switches coupled to the plurality of resistive modules and to the plurality of controlled reactance modules, with the plurality of switches responsive to a control signal to couple a first control voltage of the plurality of control voltages to a first controlled reactance module of the plurality of controlled reactance modules to modify a resonant frequency of the harmonic oscillator.

As illustrated above, the apparatus may also include a current source coupled to the plurality of resistive modules, with the current source adapted to provide a parameter-dependent current to at least one resistive module of the plurality of resistive modules to generate at least one control voltage, of the plurality of control voltages, which is parameter-dependent. In other embodiments, the current source is adapted to provide a substantially parameter-independent current to at least one resistive module of the plurality of resistive modules to generate at least one control voltage, of the plurality of control voltages, which is substantially parameter-independent. Depending upon the exemplary embodiment, each switchable resistive module of the plurality of switchable resistive modules may have a different temperature response for a selected current. As a consequence, when the parameter is temperature, at least one control voltage of the plurality of control voltages is temperature-depen-

dent and at least one control voltage of the plurality of control voltages is substantially temperature-independent.

The exemplary apparatus may also comprise a coefficient register coupled to the plurality of switches and adapted to store a first plurality of coefficients, wherein the control signal is provided by at least one coefficient of the first plurality of coefficients. The plurality of controlled reactance modules may further comprise a plurality of differentially (e.g., binary) weighted fixed capacitances and variable capacitances, and wherein the plurality of switches are responsive to the first plurality of coefficients to couple a fixed capacitance to the harmonic oscillator and to couple a first control voltage of the plurality of control voltages to a variable capacitance coupled to the harmonic oscillator. The plurality of resistive modules may further comprise a plurality of switchable resistive modules coupled to the coefficient register and a capacitive module, the capacitive module and the plurality of switchable resistive modules further coupled to a node to provide the first control voltage, with each switchable resistive module responsive to a corresponding coefficient of a second plurality of coefficients stored in the coefficient register to switch the switchable resistive module to the control voltage node.

In exemplary embodiments, an analog-to-digital converter may be coupled to the plurality of switchable resistive modules to provide a digital output signal in response to the first control voltage, to, for example, convert a temperature-dependent current (as a sensor) to a digital form; and a control logic block to convert the digital output signal to the first plurality of coefficients or to the control signal.

Also in exemplary embodiments, the plurality of controlled reactance modules further comprise: a plurality of switchable capacitive modules coupled to the coefficient register and couplable to the harmonic oscillator, with each switchable capacitive module having a variable capacitance, and with each switchable capacitive module responsive to a corresponding coefficient of the first plurality of coefficients to switch the variable capacitance to a selected control voltage of the plurality of control voltages. Depending upon the embodiment, a current source which is responsive to a parameter of a plurality of variable parameters is coupled through a current mirror to the plurality of resistive modules; wherein each resistive module of the plurality of resistive modules has a different response to the parameter and is adapted to provide a corresponding control voltage, of the plurality of control voltages, in response to a current from the current source. Depending upon the embodiment, at least one control voltage of the plurality of control voltages is substantially parameter-dependent and at least one control voltage of the plurality of control voltages is substantially parameter-independent.

Also in exemplary embodiments, the plurality of controlled reactance modules further comprise: a plurality of differentially-weighted switchable capacitive modules coupled to the coefficient register and to the harmonic oscillator, each switchable capacitive module having a first fixed capacitance and a second fixed capacitance, each switchable capacitive module responsive to a corresponding coefficient of the plurality of coefficients to switch between the first fixed capacitance and the second fixed capacitance. In other embodiments, the plurality of controlled reactance modules further comprise: a plurality of switchable variable capacitive modules coupled to the coefficient register and to the harmonic oscillator, each switchable variable capacitive module responsive to a corresponding coefficient of the plurality of coefficients to switch between a first voltage and a second voltage of a plurality of control voltages. And in other embodiments, the plurality of controlled reactance modules further comprise: a plurality of switchable variable capacitive modules coupled to the coefficient register and to the harmonic oscillator, each switchable variable capacitive module responsive to a corresponding coefficient of the plurality of coefficients to switch to a selected control voltage of a plurality of control voltages, the plurality of control voltages comprising a plurality of different magnitude voltages, and wherein the selected control voltage is substantially constant over temperature variations.

Also in exemplary embodiments, the apparatus may further comprise: a plurality of switchable resistors responsive to a control signal to switch a corresponding resistance to the harmonic oscillator to modify the resonant frequency. The apparatus may include a voltage divider coupled to the plurality of controlled reactance modules and adapted to provide a selected control voltage responsive to voltage variations. In addition, an age variation compensator may be coupled to the resonator and adapted to compare a current value of a selected parameter of the plurality of parameters to an initial value of the selected parameter and to modify the resonant frequency in response to a difference between the current value and the initial value of the selected parameter.

Numerous other exemplary embodiments are illustrated and described in detail below, and include additional modulators and compensators for voltage variations and age (IC lifetime) variations.

The present invention may also include a mode selector coupled to the frequency selector, wherein the mode selector is adapted to provide a plurality of operating modes, which may be selected from a group comprising a clock mode, a timing and frequency reference mode, a power conservation mode, and a pulsed (or pulse) mode.

For a reference mode, the invention may also include a synchronization circuit coupled to the mode selector; and a controlled oscillator coupled to the synchronization circuit and adapted to provide a third signal; wherein in the timing and reference mode, the mode selector is further adapted to couple the output signal to the synchronization circuit to control timing and frequency of the third signal. Such a synchronization circuit may be a delay-locked loop, a phase-locked loop, or an injection locking circuit.

These and additional embodiments are discussed in greater detail below. Numerous other advantages and features of the present invention will become readily apparent from the following detailed description of the invention and the embodiments thereof, from the claims and from the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features and advantages of the present invention will be more readily appreciated upon reference to the following disclosure when considered in conjunction with the accompanying drawings and examples which form a portion of the specification, wherein like reference numerals are used to identify identical or similar components in the various views, in which:

FIG. **1** is a block diagram illustrating a first exemplary system embodiment in accordance with the teachings of the present invention.

FIG. **2** is a block diagram illustrating a first exemplary apparatus embodiment in accordance with the teachings of the present invention.

FIG. **3** is a block diagram illustrating a second exemplary apparatus embodiment in accordance with the teachings of the present invention.

FIG. **4** is a high-level schematic and block diagram illustrating exemplary frequency controller, oscillator and frequency calibration embodiments in accordance with the teachings of the present invention.

FIG. **5**A is an exemplary graph illustrating oscillator voltage waveform (frequency) distortion due to a harmonic content of current injected into an oscillator with a specific filter response.

FIG. **5**B is an exemplary graph illustrating oscillator voltage waveform (frequency) shown in FIG. **5**A as a function of temperature.

FIG. **5**C is an exemplary graph illustrating oscillator frequency as a function of the transconductance of a sustaining amplifier.

FIG. **6** is a circuit diagram illustrating first exemplary negative transconductance amplifier, temperature-responsive current generator (I(T)), and LC tank oscillator embodiments in accordance with the teachings of the present invention.

FIG. **7**A is a circuit diagram illustrating an exemplary temperature-responsive CTAT current generator in accordance with the teachings of the present invention.

FIG. **7**B is a circuit diagram illustrating an exemplary temperature-responsive PTAT current generator in accordance with the teachings of the present invention.

FIG. **7**C is a circuit diagram illustrating an exemplary temperature-responsive $PTAT^2$ current generator in accordance with the teachings of the present invention.

FIG. **7**D is a circuit diagram illustrating an exemplary selectable and scalable temperature-responsive current generator, with selected CTAT, PTAT, and $PTAT^2$ configurations, in accordance with the teachings of the present invention.

FIG. **8** is a circuit and block diagram illustrating second exemplary negative transconductance amplifier, temperature-responsive current generator (I(T)), and LC tank oscillator embodiments in accordance with the teachings of the present invention.

FIG. **9** is a circuit diagram illustrating an exemplary first controlled (or controllable) capacitance module utilized in a frequency-temperature compensation module in accordance with the teachings of the present invention.

FIG. **10** is a circuit diagram illustrating an exemplary first voltage control module utilized in a frequency-temperature compensation module in accordance with the teachings of the present invention.

FIG. **11** is a circuit diagram illustrating an exemplary first process variation compensation module in accordance with the teachings of the present invention.

FIG. **12** is a circuit diagram illustrating an exemplary second process variation compensation module in accordance with the teachings of the present invention.

FIG. **13** is a block diagram illustrating an exemplary frequency calibration module in accordance with the teachings of the present invention.

FIG. **14** is a block diagram illustrating an exemplary first frequency divider, square wave generator, asynchronous frequency selector and glitch suppression module in accordance with the teachings of the present invention.

FIG. **15** is a graphical diagram illustrating exemplary low latency frequency switching in accordance with the teachings of the present invention.

FIG. **16** is a block diagram illustrating an exemplary second frequency divider in accordance with the teachings of the present invention.

FIG. **17** is a block diagram illustrating an exemplary power mode selection module in accordance with the teachings of the present invention.

FIG. **18** is a block diagram illustrating an exemplary synchronization module for a second oscillator in accordance with the teachings of the present invention.

FIG. **19** is a flow diagram illustrating an exemplary method in accordance with the teachings of the present invention.

FIG. **20** is a block and circuit diagram illustrating an exemplary controlled impedance module utilized in a compensation module in accordance with the teachings of the present invention.

FIG. **21** is a block diagram illustrating a first exemplary frequency controller and apparatus in accordance with the teachings of the present invention.

FIG. **22** is a circuit diagram illustrating an exemplary second controlled capacitance module utilized in a frequency-temperature compensation module in accordance with the teachings of the present invention.

FIG. **23** is a circuit diagram illustrating an exemplary second voltage control module utilized in a frequency-temperature compensation module in accordance with the teachings of the present invention.

FIG. **24** is a graph illustrating exemplary frequency control in response to temperature variation in accordance with the teachings of the present invention.

FIG. **25** is a block diagram illustrating a second exemplary frequency controller and apparatus in accordance with the teachings of the present invention.

FIG. **26** is a circuit diagram illustrating an exemplary third controlled capacitance module and an exemplary third voltage control module utilized in a parameter compensation module in accordance with the teachings of the present invention.

FIG. **27** is a circuit and block diagram illustrating an exemplary voltage variation compensation module in accordance with the teachings of the present invention.

FIG. **28** is a circuit diagram illustrating an exemplary fourth voltage control module utilized in frequency and process compensation modules in accordance with the teachings of the present invention.

FIG. **29** is a circuit diagram illustrating an exemplary resistive control module in accordance with the teachings of the present invention.

FIG. **30** is a block diagram illustrating an exemplary age variation compensator in accordance with the teachings of the present invention.

FIG. **31** is a circuit diagram illustrating a third exemplary LC oscillator which may be utilized in accordance with the teachings of the present invention.

FIG. **32** is a circuit diagram illustrating a fourth exemplary LC oscillator which may be utilized in accordance with the teachings of the present invention.

FIG. **33** is a circuit diagram illustrating a fifth exemplary LC oscillator which may be utilized in accordance with the teachings of the present invention.

FIG. **34** is a circuit diagram illustrating a sixth exemplary LC oscillator which may be utilized in accordance with the teachings of the present invention.

FIG. **35** is a circuit diagram illustrating a seventh exemplary LC oscillator which may be utilized in accordance with the teachings of the present invention.

FIG. **36** is a circuit diagram illustrating an eighth exemplary LC oscillator which may be utilized in accordance with the teachings of the present invention.

FIG. **37** is a circuit diagram illustrating a ninth exemplary LC oscillator which may be utilized in accordance with the teachings of the present invention.

FIG. **38** is a block diagram illustrating an active inductor embodiment in accordance with the teachings of the present invention.

FIG. **39** is a block diagram illustrating a second exemplary system embodiment in accordance with the teachings of the present invention.

FIG. **40** is a block diagram illustrating a third exemplary system embodiment in accordance with the teachings of the present invention.

FIG. **41** is a block diagram illustrating a third exemplary frequency divider embodiment in accordance with the teachings of the present invention.

FIG. **42** is a block diagram illustrating a fourth exemplary frequency divider embodiment in accordance with the teachings of the present invention.

FIG. **43** is a block diagram illustrating a fourth exemplary system embodiment in accordance with the teachings of the present invention.

FIG. **44** is a block diagram illustrating a fifth exemplary system embodiment in accordance with the teachings of the present invention.

FIG. **45** is a block diagram illustrating an exemplary first discrete apparatus **3000** embodiment in accordance with the teachings of the present invention.

FIG. **46** is a block diagram illustrating an exemplary second discrete apparatus embodiment in accordance with the teachings of the present invention.

FIG. **47** is a block diagram illustrating an exemplary third discrete apparatus embodiment in accordance with the teachings of the present invention.

FIG. **48** is a block diagram illustrating an exemplary fourth discrete apparatus embodiment in accordance with the teachings of the present invention.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

While the present invention is susceptible of embodiment in many different forms, there are shown in the drawings and will be described herein in detail specific examples and embodiments thereof, with the understanding that the present disclosure is to be considered as an exemplification of the principles of the invention and is not intended to limit the invention to the specific examples and embodiments illustrated.

As indicated above, the various embodiments of the invention provide numerous advantages, including the ability to integrate a highly accurate (over PVT and age), low-jitter, free-running and self-referencing clock generator and/or a timing and frequency reference with other circuitry, such as illustrated in FIG. **1**. FIG. **1** is a block diagram illustrating an exemplary system embodiment **150** in accordance with the teachings of the present invention. As illustrated in FIG. **1**, the system **150** is a single integrated circuit, having a clock generator and/or timing/frequency reference **100** of the present invention integrated monolithically with other, or second, circuitry **180**, together with interface (I/F) (or input/output (I/O) circuitry) **120**. The interface **120** will generally provide power, such as from a power supply (not illustrated), ground, and other lines or busses to the clock generator **100**, such as for calibration and frequency selection. As illustrated, one or more output clock signals are provided on bus **125**, as a plurality of frequencies, such as a first frequency (f_0), a second frequency (f_1), and so on, through an $(n+1)^{th}$ frequency (f_n). In addition, a power conservation mode (or low power mode (LP)) is provided (also on bus **125**). The second circuitry **180** (or the I/F **120**) may also provide input into the clock generator **100**, such as through selection signals (S_0, S_1, through S_n), and one or more calibration signals (C_0, C_1, through C_n). Alternatively, the selection signals (S_0, S_1, through S_n) and one or more calibration signals (C_0, C_1, through C_n) may be provided directly to the clock generator **100** through the interface **120**, such as on bus **135**, along with power (on line **140**) and ground (on line **145**).

The clock generator and/or timing/frequency reference **100**, in addition to a low power mode, has additional modes discussed in greater detail below. For example, in a clock mode, the apparatus **100** will provide one or more clock signals, as output signals, to the second circuitry **180**. The second circuitry **180** may be any type or kind of circuitry, such as a microprocessor, a digital signal processor ("DSP"), a radio-frequency circuit, for example, or any other circuit which could utilize the one or more output clock signals. Also for example, in a timing or frequency reference mode, the output signal from the apparatus **100** may be a reference signal, such as a reference signal for synchronization for a second oscillator. As a consequence, the terminology clock generator and/or timing/frequency reference will be utilized interchangeably herein, with the understanding that the clock generator will also generally provide a square-wave signal, which may or may not be provided with a timing/frequency reference, which may utilize a substantially sinusoidal signal instead. In addition, as discussed in greater detail below, the various embodiments of the invention also provided a pulsed mode, in which the output signal from clock generator and/or timing/frequency reference **100** is provided in bursts or intervals, for increased instruction processing efficiency and lower power consumption, for example.

It should be noted that the various signals, voltages, parameter-independent current sources, and so on, are referred to as "substantially" sinusoidal or square-wave signals, substantially constant control voltages, or substantially parameter-independent voltages or currents, for example. This is to accommodate the various fluctuations, noise sources and other distortions introduced which may cause such signals, voltages or currents to differ in practice from the more ideal depictions found in textbooks. For example, as discussed in greater detail below, exemplary "substantially" square-wave signals are depicted in FIGS. **15**A and **15**B, and exhibit a variety of distortions, such as undershoots, overshoots, and other variations, and are nonetheless considered to be very high quality square-waves in practice.

Several important features of the present invention are in system **150**. First, a highly accurate, low-jitter, free-running and self-referencing clock generator **100** is integrated monolithically with other (second) circuitry **180**, to form a singular integrated circuit (system **150**). This is in sharp contrast with the prior art, in which a reference oscillator is used to provide a clock signal, such as a crystal reference oscillator, which cannot be integrated with other circuitry and is off-chip, as a second and separate device which must be connected through a circuit board to any additional circuitry. For example, in accordance with the present invention, the system **150**, including clock generator **100**, may be fabricated with other, second circuitry using conventional CMOS (complementary metal oxide semiconductor), BJT (bipolar junction transistor), BiCMOS (bipolar and CMOS), or other fabrication technologies utilized in modern IC manufacturing.

Second, no separate reference oscillator is required. Rather, in accordance with the invention, the clock generator **100** is self-referencing and free-running, such that it is not referenced to or locked to another signal, such as being synchronized in a phase locked loop ("PLL"), delay locked loop ("DLL"), or via injection locking to a reference signal, which

is typical of the prior art. Instead, the exemplary embodiments may be utilized as such a reference oscillator which generates a frequency reference signal, which may then be locked to by one or more phase-locked or delay-locked loops, for example.

Third, the clock generator **100** provides a plurality of output frequencies and a power conservation mode, such that frequencies may be switched with low latency and in a glitch-free manner. For example, second circuitry **180** may shift to a power conservation mode, such as a battery or lower frequency mode, and request (through selection signals) a lower clock frequency for minimizing power consumption, or request a low power clock signal to enter a sleep mode. As discussed in greater detail below, such frequency switching is provided with substantially negligible latency, with low latency introduced for glitch prevention (in proportion to the number of glitch prevention stages utilized), using a merely a handful of clock cycles, rather than the thousands of clock cycles required to change the output frequency from a PLL/DLL.

Additional embodiments also provide for generating a plurality of frequency reference signals, whether sinusoidal or square-wave, such as for use as one or more clock signals or reference frequency sources. In exemplary embodiments, the clock/frequency reference of the invention is coupled to one or more phase-locked loops ("PLLs") or delay-locked loops ("DLLs), to provide a corresponding plurality of output reference signals at selected frequencies. These exemplary embodiments are typically programmable, through control signals or stored coefficients, such as to adjust the divide ratios of the PLLs or DLLs for corresponding frequency selection.

In addition, given the significantly high available output frequencies of the clock generator and/or timing/frequency reference **100** discussed below, new operating modes are available. For example, clock start-up times are effectively or substantially negligible, allowing the clock generator and/or timing/frequency reference **100** to be repeatedly started and stopped, such as turned off entirely or to be pulsed for power conservation. For example, rather than running continuously as a clock, the clock generator and/or timing/frequency reference **100** can be operated in comparatively short, discrete intervals or bursts (i.e., pulsed), periodically or non-periodically, for instruction processing by a second circuit **180**, such as a processor. As discussed in greater detail below, with the rapid start-up time, such pulsed operation provides a power savings, as more instructions (million instructions per second or MIPS) are processed per milliwatt (mW) of power consumption. In addition, such a pulsed mode may also be utilized to periodically synchronize a second clock or oscillator, in addition to other uses. As a consequence, the clock generator and/or timing/frequency reference **100** (and the other embodiments discussed below) has a plurality of operating modes, including a clock mode, a timing and/or frequency reference mode, a power conservation mode, and a pulsed mode.

Fourth, as discussed in greater detail below, the clock generator and/or timing/frequency reference **100** includes features for highly accurate frequency generation over fabrication process, voltage, temperature ("PVT") and age variations. These features include frequency tuning and selection, and compensation for frequency variations which may be caused due to temperature and/or voltage fluctuations, fabrication process variations, and IC aging.

Fifth, the clock generator and/or timing/frequency reference **100** generates a significantly and comparatively high frequency, such as in the hundreds of MHz and GHz range, which is then divided to a plurality of lower frequencies. Each such division by "N" (a rational number, as a ratio of integers) results in a significant noise reduction, with phase noise reduced by N and phase noise power reduced by N^2. As a consequence, the clock generator of the present invention results in significantly less relative period jitter than available with other oscillators that generate their output directly or through frequency multiplication.

These features are illustrated in greater detail in FIG. **2**, which is a block diagram illustrating a first exemplary apparatus **200** embodiment, including a frequency controller **215** in accordance with the teachings of the present invention. As illustrated in FIG. **2**, the apparatus **200** is a clock generator and/or timing/frequency reference, providing one or more output signals, such as a clock or reference signal having any of a plurality of frequencies, selected using frequency selector **205**. The apparatus (or clock generator) **200** includes an oscillator **210** (having a resonant element), a frequency controller **215**, a frequency divider **220**, a mode selector **225**, and the frequency selector **205** mentioned above. In accordance with the invention, the oscillator **210** generates a signal having a comparatively high frequency, f_0. Due to PVT or age variations mentioned above, the frequency controller **215** is utilized to frequency select or tune the oscillator **210**, such that the oscillation frequency f_0 is selectable from a plurality of potential oscillation frequencies, i.e., the frequency controller **215** provides for output signals having frequencies which are accurate over PVT and age variations.

For example, given these PVT variations, the output frequency from an oscillator, such as oscillator **210**, may vary plus or minus 5%. For some applications, such as those utilizing ring oscillators, such frequency variability may be acceptable. In accordance with the present invention, however, greater accuracy for the clock generator **200** is desirable, particularly for more sensitive or complex applications, such as providing clock signals for integrated microprocessors, microcontrollers, digital signal processors, communication controllers, and so on. As a consequence, frequency controller **215** is utilized to adjust for these PVT variations, such that the output frequency from the oscillator is the selected or desired frequency f_0 with much less variance by several orders of magnitude, such as ±0.25% or less, and having a comparatively low-jitter.

Various exemplary embodiments of the frequency controller **215**, in accordance with the teachings of the present invention, are illustrated in detail below. For example, referring to FIG. **21**, which is a block diagram illustrating an exemplary frequency controller **1415** and apparatus **1400** in accordance with the teachings of the present invention, an oscillator (resonator **310** and sustaining amplifier **305**) provides a first output signal having a resonant frequency f_0. The exemplary frequency controller **1415** is coupled to the oscillator and modifies the resonant frequency f_0 in response to a second signal, such as a second signal provided by one or more sensors **1440**. The exemplary frequency controller **1415** comprises one of more of the following components: transconductance modulator **1420**, variable parameter modulator (or controller) **1425** (such as one or more of the controlled capacitance or controlled reactance modules discussed below), process (or other parameter) modulator (or compensator) **1430**, voltage compensator **1455**, coefficient register(s) **1435**, and potentially also an age variation compensator **1460**. Depending upon the selected embodiment, the frequency controller **1415** may also include one or more sensor(s) **1440**, analog-to-digital (A/D) converter ("ADC") **1445**, and control logic block **1450**. For example, a temperature-dependent current source, I(T) (or, more generally, yI(x)) generator **415** illustrated in FIG. **4** effectively functions as a temperature

sensor in accordance with the present invention, providing a corresponding output current which varies as a function of ambient or junction temperature. Such a temperature-dependent output current may be converted into a digital signal by A/D converter (ADC) **1445**, and utilized to provide corresponding coefficients (stored in registers **1435**) utilized by the various modulators or compensators **1420**, **1425**, **1430**, **1455** and **1460** of the frequency controller **1415**, to control the resonant (or output) frequency f_0 in light of various parameters, such as a variable operating temperature or variable fabrication processes. In other illustrated embodiments, such a temperature-dependent output current is provided directly (as a second signal, without intervening A/D conversion) to the various modulators, such as to transconductance modulator **1420** and to variable parameter modulator (or controller) **1425**. These modulators, in turn, modify the resonant frequency f_0 through, for example, modifying the current through the resonator **310** and sustaining amplifier **305**, or modifying the effective reactance or impedance (e.g., capacitance, inductance or resistance) coupled to and effectively forming part of the resonator **310**. For example, the effective reactance (or impedance) may be modified by coupling to or decoupling from the resonator **310** fixed or variable capacitances, or modifying the magnitudes of one or more reactances coupled to the resonator, such as by modifying a control voltage or other continuous control parameter.

In the various illustrated embodiments discussed below, the transconductance modulator **1420** and variable parameter modulator (or controller) **1425** are generally implemented to utilize a temperature parameter, such that a substantially stable resonant frequency f_0 is provided over variations in operating temperature. It will be understood by those of skill in the art that these modulators may be implemented to provide a substantially stable resonant frequency f_0 as a function or in response to other variable parameters, such as variations due to fabrication process, voltage variations, aging, and other frequency variations.

Referring again to FIG. **2**, to improve performance and decrease jitter (noise) and other interference, instead of generating a low frequency output and multiplying it up to a higher frequency, as is typically done using PLLs and DLLs, the present invention generates a comparatively high frequency output, f_0, which is then divided to one or more lower frequencies (f_1 through f_n), using frequency divider **220**. Clock signals having one or more of the plurality of frequencies from frequency divider **220** may then be selected, using frequency selector **205**. As indicated above, such frequency selection is provided glitch-free and with low latency, providing comparatively and significantly fast and glitch-free frequency switching. In addition, a plurality of operating modes are provided, using mode selector **225**.

FIG. **3** is a block diagram illustrating in greater detail a second exemplary apparatus embodiment, as clock generator and/or timing/frequency reference **300**, in accordance with the teachings of the present invention. Referring to FIG. **3**, clock generator and/or timing/frequency reference **300** comprises a resonator **310** and a sustaining amplifier **305** (forming an oscillator **395**), a temperature compensator (or modulator) **315**, a process variation compensator (or modulator) **320**, a frequency calibration module **325**, a voltage variation compensator (or modulator) **380**, an age (time) variation compensator (or modulator) **365**, one or more coefficient registers **340**, and depending on the selected embodiments, may also include a sensor(s) **385**, an analog-to-digital converter ("ADC") **390**, frequency divider and square wave generator **330**, a voltage isolator **355**, a resonant frequency selector **360**, an output frequency selector **335**, a mode selector **345**, and a low-latency start-up module **399**. The sustaining amplifier **305**, temperature compensator **315**, process variation compensator **320**, voltage isolator **355**, voltage variation compensator **380**, age variation compensator **365**, resonant frequency selector **360**, and frequency calibration module **325** are often included within a frequency controller, such as frequency controller **349** (or **215** or **1415**). Alternatively, the sustaining amplifier **305** and resonator **310** may be considered to comprise an oscillator **395**, with one or more of the various controller elements (e.g., temperature compensator **315**, process variation compensator **320**, voltage isolator **355**, voltage variation compensator **380**, age variation compensator **365**, resonant frequency selector **360**, sensor(s) **385**, ADC **390**, and frequency calibration module **325**) included within a frequency controller **349** (or **215** or **1415**). It should also be noted that the square-wave generator (of **330**) may not be needed in timing or frequency reference embodiments.

The resonator **310** may be any type of resonator which stores energy, such as an inductor (L) and a capacitor (C) coupled to form an LC-tank, where the LC-tank has a selected configuration of a plurality of LC-tank configurations, or is otherwise electrically or electromechanically equivalent to or otherwise typically represented in the art as an inductor coupled to a capacitor. Such an LC-resonator is illustrated as resonator **405** in FIG. **4**. In addition to LC resonators, other resonators are considered equivalent and within the scope of the present invention; for example, the resonator **310** may be a ceramic resonator, a mechanical resonator (e.g., XTAL), a microelectromechanical ("MEMS") resonator, or a film bulk acoustic resonator. In other cases, various resonators may be represented by electrical or electromechanical analogy as LC resonators, and are also within the scope of the present invention. In exemplary embodiments, an LC-tank has been utilized as a resonator, to provide for a high Q-value for a completely integrated solution.

The sustaining amplifier **305** provides for both start-up and sustaining amplification for the resonator **310**. The temperature compensator **315** provides frequency control for the resonator **310**, to adjust the oscillation frequency based on variations due to temperature. In selected embodiments, depending upon the degree of control desired or required, the temperature compensator **315** may include control over both current and frequency, as illustrated below for selected embodiments. For example, the temperature compensator **315** may comprise one or both of a transconductance modulator **1420** and variable parameter modulator **1425** of FIG. **21**, with both modulators **1420** and **1425** embodied to be responsive to temperature fluctuations. Similarly, the process variation compensator **320** provides frequency control for the resonator **310**, to adjust the oscillation frequency based on process variations inherent in semiconductor fabrication technologies, both process variations within a given foundry (e.g., batch or run variations, variations within a given wafer, and die-to-die variations within the same wafer) and process variations among different foundries and foundry processes (e.g., 130 nm and 90 nm processes)). Voltage variation compensator **380** may be utilized to maintain a stable output frequency over supply voltage variations and other voltage variations. Age variation compensator **365** may be utilized to maintain a stable output frequency as the IC ages, with corresponding variations in circuit elements occurring over time. Frequency calibration module **325** is utilized to fine-tune and select the desired output frequency, f_0, from among a plurality of oscillation frequencies which may occur in resonator **310**, i.e., to select the output frequency f_0 from a plurality of available or potential frequencies. In selected embodiments, coefficient registers **340** are utilized to store coefficient values

utilized in the various exemplary compensator and calibration embodiments, discussed in greater detail below.

As mentioned above, the frequency controller **349**, in selected embodiments, may also include one of more sensors **385** and analog-to-digital converter (ADC) **390**. In addition, many of the other compensators and modulators of the frequency controller include components which function as sensors, such as temperature-dependent current sources and other voltage variation detectors. In addition to being utilized to generate various pluralities of stored coefficients which provide control to various switching elements, to both switch controlled reactance modules (discussed below) to the resonator **310** (as a discrete form of control) and to vary the amount of effective reactance supplied by a coupled or switched reactance to the resonator **310** (a continuous form of control), the various sensors, compensators and modulators may also be utilized to provide other forms of continuous control over the resonant frequency of the resonator **310**. The various continuous outputs from sensors, current generators, control voltages, etc., as illustrated and discussed below, function as control signals within the scope of the present invention. For example, the various control voltages, which may vary with a selected parameter (e.g., temperature) or which may be constant with respect to a selected parameter, function as control signals which are used to modify corresponding magnitudes of controlled capacitance modules implemented using varactors.

In addition to the temperature and process compensation, voltage isolator **355** provides isolation from variations in voltage, such as from a power supply, and may be implemented separately or as part of other components, such as part of temperature compensator **315**. In addition to frequency adjustment for these PVT and age variations, the resonant frequency may also be selected independently through resonant frequency selector **360**, for obtaining a selected frequency from a range of available frequencies.

For clock signal generation, clock generator **300** utilizes a frequency divider (in module **330**) to convert the output oscillation frequency f_0 to a plurality of lower frequencies (f_1 through f_n) and to convert a substantially sinusoidal oscillation signal to a substantially square wave signal for clock applications, using a square wave generator (also in module **330**). Frequency selector **335** then provides for selection of one or more of the available output signals having the plurality of frequencies, and mode selector **345** may also provide for operating mode selection, such as providing a low power mode, a pulsed mode, a reference mode, and so on. Using these components, the clock generator **300** provides a plurality of highly accurate (over PVT), low jitter, and stable output frequencies, f_0, f_1 through f_n, with minimal to negligible frequency drift due to such PVT variations, thereby providing sufficient accuracy and stability for sensitive or complex applications, as mentioned above.

FIG. **4** is a high-level schematic and block diagram illustrating exemplary frequency controller, oscillator and frequency calibration embodiments in accordance with the teachings of the present invention. As illustrated in FIG. **4**, the resonator is embodied as a resonant LC tank **405**, and the frequency controller is embodied as several elements, a negative transconductance amplifier **410** (used to implement the sustaining amplifier), a temperature-responsive (or temperature-dependent) current generator I(T) (or, more generally, yI(x), as responsive to any such parameter "x") **415**, a temperature-responsive (or temperature-dependent) frequency (f_0 (T)) compensation module **420**, a process variation compensation module **425**, and may also include a frequency calibration module **430**. The various temperature-responsive or temperature-dependent modules **415** and **420** are sensitive to or responsive to temperature fluctuations, and provide corresponding adjustments, such that the resonant frequency is stable and accurate over these PVT and age variations.

The resonant LC tank **405** with a sustaining amplifier may be equally described as a harmonic oscillator or harmonic core, and all such variations are within the scope of the present invention. It should be noted that while the resonant LC tank **405** is an inductor **435** in parallel with a capacitor **440**, other circuit topologies are also known and equivalent to that illustrated, such as an inductance in series with a capacitance. Another such equivalent topology is illustrated in FIG. **8**. In addition, as indicated above, other types of resonators may be utilized and all are considered equivalent to the exemplary resonant LC tank illustrated herein. Moreover, as discussed in greater detail below, additional capacitances and/or inductances, both fixed and variable (and referred to more generally as impedances or reactances (or reactive elements)), are distributed in the various modules and effectively form part of the resonant LC tank **405** and are utilized as part of the frequency controller of the invention. In addition, corresponding resistances (resistive components of the various impedances) R_L **445** and R_C **450** are illustrated separately, but should be understood to be intrinsic to the inductor **435** and capacitor **440**, respectively, occurring as part of fabrication, and are not additional or separate components from the respective inductor **435** and capacitor **440**. Conversely, such additional or intrinsic (parasitic) resistances can also be included as part of compensation for PVT variations, as illustrated and discussed below with reference to FIG. **29**.

The inductor **435** and capacitor **440** of the resonant LC tank or oscillator **405** are sized to substantially or approximately provide the selected oscillation frequency, f_0, or range of oscillation frequencies around f_0. In addition, inductor **435** and capacitor **440** may be sized to have or to meet IC layout area requirements, with higher frequencies requiring less area. Those of skill in the art will recognize that $f_0 \approx \frac{1}{2\pi}\sqrt{LC}$, but only as a first order approximation because, as discussed below, other factors such as the impedances R_L and R_C, any additional resistors, along with temperature and process variations and other distortions, affect f_0, and may be included in second and third order approximations. For example, the inductor **435** and capacitor **440** may be sized to generate a resonant frequency in the 1-5 GHz range; in other embodiments, higher or lower frequencies may be desirable, and all such frequencies are within the scope of the invention. In addition, the inductor **435** and capacitor **440** may be fabricated using any semiconductor or other circuitry process technology, and may be CMOS-compatible, bipolar-junction transistor-compatible, for example, while in other embodiments, the inductor **435** and capacitor **440** may be fabricated using silicon-on-insulator (SOI), metal-insulator-metal (MiM), polysilicon-insulator-polysilicon (PiP), GaAs, strained-silicon, semiconductor heterojunction technologies, or MEMS-based (microelectromechanical) technologies, also for example and without limitation. It should be understood that all such implementations and embodiments are within the scope of the invention. In addition, other resonator and/or oscillator embodiments, in addition to or instead of the resonant LC tank **405**, may also be utilized and are also within the scope of the present invention. As used herein, "LC tank" will mean and refer to any and all inductor and capacitor circuit layouts, configurations or topologies which may provide oscillation, however embodied. It should be noted that the capability of the oscillator **405** to be fabricated using a conventional process, such as CMOS technology, allows the clock generator to be fabricated integrally and monolithically

with other circuitry, such as the second circuitry **180**, and provides a distinct advantage of the present invention.

In addition, the capacitance **440** illustrated in FIG. **4** is only a portion of the overall capacitance involved in the resonance and frequency determination of the resonant LC tank **405**, and is a fixed capacitance. In selected embodiments, this fixed capacitance may represent approximately 10% to 90% of the total capacitance ultimately utilized in the oscillator, as an example. Alternatively, the capacitance **440** may also be implemented as a variable capacitance, if desired. As discussed in greater detail below, the overall capacitance is distributed, such that additional fixed and variable capacitance is selectively included within the clock generator and/or timing/frequency reference **300**, and is provided, for example, by components of the frequency controller (**215**, **1415**), such as temperature-responsive frequency ($f_0(T)$) compensation module **420** and process variation compensation module **425**, to provide for both selecting the resonant frequency f_0 and to allow the resonant frequency f_0 to be substantially independent of both temperature and process variations.

In the selected embodiments, the inductance **435** has been fixed, but also could be implemented in a variable manner, or as a combination of fixed and variable inductances. As a consequence, those of skill in the art will recognize that the detailed discussions of fixed and variable capacitance, for both frequency tuning and temperature and process independence, pertain similarly to inductance choices. For example, different inductances could be switched in or out of the oscillator, to similarly provide tuning. In addition, a single inductor's inductance may also be modulated. As a consequence, all such inductance and capacitance variations are within the scope of the present invention, and are illustrated as switchable, variable and/or fixed reactive elements or components of the exemplary controlled impedance modules **1305** of FIG. **20** and the controlled reactance modules **1805** of FIGS. **25-27**.

Also as illustrated in FIG. **4**, the resonant LC tank **405** and resulting output signal, referred to as a first (output) signal at nodes or lines **470** and **475**, is a differential signal and provides common-mode rejection. Other configurations, including non-differential or other single-ended configurations are also within the scope of the present invention. For example, in single-ended configurations, only one instantiation of the various modules (e.g., **485**, **460**) would be required, rather than the use of two for a balanced configuration as illustrated. Similarly, other components and features discussed below, such as frequency dividers, would also have a single-ended rather than differential configuration. Such additional exemplary LC oscillators, both differential and single-ended, are discussed below with reference to FIGS. **31-37**, in addition to the differential LC oscillators illustrated in FIGS. **6** and **8**. In addition, various embodiments illustrated utilize MOSFET transistors (metal oxide semiconductor field effect transistors) in various forms (such as CMOS, accumulation-mode MOSFET ("AMOS"), inversion-mode MOSFET ("IMOS"), and so on); other implementations are also available, such as using bipolar junction transistors ("BJTs"), BiCMOS, etc. All such embodiments are considered equivalent and are within the scope of the present invention.

The negative transconductance amplifier **410** is selected to provide temperature compensation through transconductance (g_m) modulation and the on-resistance of its resistors. Transconductance (g_m) modulation may also be utilized independently in frequency selection. Another significant advantage of the present invention is the selection of a negative transconductance amplifier **410** to provide start-up and sustaining amplification, because both oscillation amplitude and frequency are affected by the transconductance of the sustaining amplifier, providing both amplitude modulation and frequency trimming (or tuning), in addition to providing temperature compensation. The negative transconductance amplifier **410** will inject current into the resonant LC tank **405** (and specifically onto the capacitor **440**) in response to a voltage "v" across the resonant LC tank **405**, as illustrated (across nodes **470** and **475**). That current injection, in turn, will change (and distort) the voltage waveform (as voltage is the integral of the current), resulting in a change or variation in frequency, generally in inverse proportion to the magnitude of the transconductance, g_m, as illustrated in FIG. **5**A. It should be noted that this transconductance is a negative value, as gain is provided to cancel the loss intrinsic to the resonant element. As a consequence, whenever "transconductance amplifier" is utilized herein, it should be understood to mean and to be merely an abbreviation for "negative transconductance amplifier". In turn, the transconductance is also a function of the bias current, substantially proportional (approximately) to the square root of the current (yI(x)) through the amplifier **410** (for MOSFETs), and substantially proportional (approximately) to the current (yI(x)) through the amplifier **410** (for BJTs), which is temperature-dependent, resulting in a waveform distortion which is both temperature and bias current dependent, as illustrated in FIG. **5**B. In addition, as illustrated in FIG. **5**C, the oscillation frequency is also related to and a function of the transconductance of the sustaining negative transconductance amplifier **410**, providing for oscillation frequency selection. Moreover, in addition to temperature dependence (as I(T)), the current can also vary as a function of other parameters or variables (so is referred to more generally as current I(x)), such as voltage or external tuning, and may also be amplified such as by a factor of "y" (as illustrated below); as a consequence, the current is referred to as "yI(x)".

As indicated above, more generally, such a variable current yI(x) may be utilized as or as part of a sensor, such as one or more sensors **1440** or transconductance modulator **1420** of FIG. **21** or sensors **1815** of FIG. **25**. For example, when such as variable current is provided by I(T) generator **415**, such that the current provided is a function of temperature (parameter or variable "x"=temperature parameter "T"), I(T) generator **415** thereby functions as a temperature sensor, and may be utilized as such in the exemplary embodiments, such as utilized by the frequency controller (**215**, **349**, **1415**) to adjust the resonant frequency f_0 in response to temperature fluctuations. For example, transconductance modulator **1420** of FIG. **21** may comprise such a temperature (or other parameter) responsive current source **415** (which also functions as a sensor **1440**), providing current to a sustaining amplifier **305**.

Significant inventive breakthroughs of the present invention include utilizing these potential distortions advantageously, to provide for frequency compensation in generating the selected f_0 value of the oscillator, and frequency modulation through modulation of the transconductance of the sustaining amplifier. As a consequence, and as discussed in greater detail below, the transconductance, first, may be modified or varied for frequency selection, and second, to compensate for such frequency variation due to temperature, voltage, fabrication process or aging, by modifying the current yI(x), generally on a real-time or near real-time basis. The selected frequency f_0, and its stability with respect to temperature variations, in accordance with the invention, may be determined through appropriate selection of the transconductance g_m and selection of I(T). Stated another way, in accordance with the present invention, the bias current is made temperature dependent, as I(T) (or, more generally, as

yI(x)), which in turn affects the transconductance g_m, which in turn affects the oscillation frequency f_0. This methodology may also be utilized for other variables, such as voltage fluctuations, process variation, or aging variation.

FIG. **6** is a circuit diagram illustrating exemplary negative transconductance amplifier (**410**), temperature-responsive current generator (I(T) **415**), and LC tank resonator (**405**) embodiments in accordance with the teachings of the present invention. As illustrated in FIG. **6**, a resonant LC tank **500** is coupled to a negative transconductance amplifier implemented as a complementary cross-coupled pair amplifier **505** (comprised of transistors M**1**, M**2**, M**3** and M**4**) which, in turn, is coupled through a voltage isolator **510** (implemented as current mirror (transistors **525**A and **525**B) and referred to interchangeably herein) to a temperature-responsive current generator (I(x)) **515**. The current mirror **510** (voltage isolator) may also be implemented in a cascode topology (**520**A and **520**B), such as to provide improved stability with variations in power supply and isolate the oscillator from the power supply (voltage isolation). The temperature-responsive current generator **515** may be implemented utilizing topologies such as CTAT (complementary to absolute temperature), PTAT (proportional to absolute temperature), or $PTAT^2$ (proportional to absolute temperature squared), as illustrated in FIGS. **7**A, **7**B and **7**C, respectively, and combinations of CTAT, PTAT, and $PTAT^2$, as illustrated in FIG. **7**D. In each case, the current I(T) (or yI(x)) injected into the negative transconductance amplifier (complementary cross-coupled pair amplifier) **505** has a temperature dependence, such as increasing current (PTAT and $PTAT^2$) or decreasing current (CTAT) as a function of increasing temperature, as illustrated. One or more combinations of these temperature-responsive current generators may also be implemented, as illustrated in FIG. **7**D, such as CTAT in parallel with PTAT, for example.

The selection of a particular temperature-responsive or temperature-dependent current generator is also a function of the fabrication process utilized; for example, CTAT may be utilized for a Taiwan Semiconductor (TSMC) fabrication process. More generally, as different fabricators utilize different materials, such as aluminum or copper, R_L typically varies, resulting in different temperature coefficients which, in turn, change the temperature coefficient of the oscillator, thereby requiring differences in I(T) compensation. Correspondingly, different ratios of CTAT, PTAT, and $PTAT^2$ compensation may be required to provide an effectively flat frequency response as a function of temperature. Not separately illustrated, the various temperature-responsive current generators illustrated in FIGS. **7**A, **7**B, **7**C and **7**D may include a start-up circuit. In addition, the transistors comprising the selected temperature-responsive current generator configuration may be biased differently, such as biased in strong inversion for CTAT (M**7** and M**8**) and $PTAT^2$ (M**13** and M**14**), and in subthreshold for PTAT (M**9** and M**10**) and $PTAT^2$ (M**11** and M**12**), for the exemplary topologies illustrated.

FIG. **8** is a circuit and block diagram illustrating additional exemplary negative transconductance amplifier, temperature-responsive (or temperature-dependent) current generator (I(T) or I(x)), and LC tank oscillator embodiments in accordance with the teachings of the present invention. As illustrated in FIG. **8**, the resonant LC tank **550** has a different topology than previously illustrated, but also is coupled to a negative transconductance amplifier implemented as a complementary cross-coupled pair amplifier **505** (transistors M**1**, M**2**, M**3** and M**4**) which, in turn, is coupled through a plurality of current mirrors **510** (or **520**) and **530** to a temperature-responsive (or temperature-dependent) current generator (I(T) or I(x)) **515**. As illustrated, the plurality of current mirrors are utilized to successively provide gain to and increase the current I(T) entering the negative transconductance amplifier **505** and resonant LC tank **550**. Often, the tail device in the current mirror (e.g., transistor M**6** in FIG. **6**) providing current into node B and which drives the negative transconductance amplifier is selected to be a PMOS device, and thus several stages of mirroring may be required (as shown) to provide a PMOS current mirror input to the g_m amplifier. PMOS is often selected because in modern CMOS processes, PMOS devices are often buried channel devices which are known to exhibit less flicker noise than equally sized and similarly biased NMOS devices. Reduced flicker noise in the tail device reduces the phase noise and jitter of the oscillator because flicker noise is upconverted around the oscillation frequency by the nonlinear active devices in the circuit.

As indicated above, the portion of the current mirror **510** or **520** (or other circuitry) sourcing current into the negative transconductance amplifier **505** should have a high impedance at its output to reduce power supply frequency drift, such as by using long transistor geometries and cascode configurations to increase output resistance, and provide significant stability at node B. In addition, a shunt capacitor **570** also may be employed to filter and thereby reduce flicker noise from the various tail devices.

Depending upon the selected application, the use of the negative transconductance amplifier **505** with its I(T) (or yI(x)) bias may provide sufficient frequency stability, such that the additional frequency controller components may not be necessary or desirable in that application. In other embodiments, however, additional accuracy and less frequency drift may be provided, using one or more of the components discussed in greater detail below.

In addition to providing a temperature-dependent current yI(x) (or I(T)), the various transistors M**1**, M**2**, M**3** and M**4** each have an associated resistance during conduction, which may also tend to cause frequency distortion and frequency drift during oscillation. In each half-cycle, either M**1** and M**4** or M**2** and M**3** are on and conducting. Such resistance is also temperature dependent. As a consequence, the transistors M**1**, M**2**, M**3** and M**4** should be adjusted in size (width and length) to also compensate for such frequency effects. It should be noted that the current injected into the resonant LC tank **405** must be sufficient to sustain oscillation (as illustrated in FIG. **5**C) and, as a consequence, will have a minimum value, which may limit the degree or capability of frequency control which can be readily implemented through the negative transconductance amplifier **410** (or **505**) and temperature-dependent current generator **415** (or **515**). As a consequence, I(T) and the transistor (M**1**, M**2**, M**3** and M**4**) sizing should be jointly selected to provide for oscillation start up, to accommodate maximum currents for power consumption constraints, and to fit into the selected IC area and layout. For example, the transconductance g_m may be selected to provide approximately sufficient current to ensure start up and sustain oscillation, with a frequency characteristic of decreasing frequency with increasing temperature, followed by sizing transistors M**1**, M**2**, M**3** and M**4** to be large enough to either make the frequency independent of temperature or increasing with increasing temperature, followed by fine-tuning the frequency-temperature relationship with appropriate selection of I(T). In selected modeled embodiments, this has resulted in frequency accuracy of approximately ±0.25% to 0.5% over PVT, which may be more than sufficient for many applications.

Referring again to FIG. **4**, additional compensation modules are also utilized as part of frequency controller (**215**, **349**,

1415) to provide greater control and accuracy over the resonant frequency f_0, such as for applications in which greater accuracy and less variance (or frequency drift) may be required, or where technologies do not allow the previous techniques to provide sufficient accuracy over PVT or age variations, such as to provide a frequency accuracy of approximately ±0.25% or better. In these circumstances, temperature-dependent (or temperature-responsive) frequency (f_0(T)) compensation module **420** may be utilized, such as the exemplary temperature-responsive frequency (f_0(T)) compensation module **420**. This module **420** may be implemented, for example, utilizing controlled (or controllable) capacitance modules **485**, with each coupled to a respective side or rail of the resonant LC tank **405** (lines **470** and **475**), and with each under common control, provided by a first plurality ("w") of switching coefficients (p_0 though $p_{(w-1)}$) (register **495**) and a voltage controller (V_{CTRL}) **480** providing a control voltage determined by a second plurality ("x") of switching coefficients (q_0 though $q_{(x-1)}$) (register **455**), with representative examples illustrated in FIGS. **9** and **10**. (The terms "controlled" and "controllable" are utilized interchangeably herein). Additional exemplary embodiments are illustrated in FIG. **20**, which illustrates an exemplary controlled impedance module **1300** utilized in a frequency-temperature compensation module, such as in place of or in addition to controlled (or controllable) capacitance modules **485** in module **420**; in FIG. **22**, which illustrates another variation of controlled capacitance modules **485**, as controlled capacitance modules **1500** with a plurality of temperature-dependent or other parameter-dependent control voltages (generated as illustrated FIG. **23** or **26**); in FIG. **25**, which illustrates a plurality of controlled reactance modules **1805** which are switched in or out (coupled to or uncoupled from the resonator) in response to control signals from control logic **1810** and sensor(s) **1815**, including feedback from the oscillator; in FIG. **26**, which illustrates a plurality of controlled reactance modules **1805** which are switched in or out and/or switched to a control voltage, in response to control signals (continuous) or coefficients (discrete); and in FIG. **27**, which illustrates a plurality of controlled reactance modules **1805** which are switched in response to control signals, for voltage variation compensation. There are several different types of switching available, such as coupling or uncoupling a reactance or impedance to the resonator, or switching coupled reactances or impedances to selected control voltages or other control signals, for example.

FIG. **9** is a circuit diagram illustrating an exemplary first controllable capacitance module **635** in accordance with the teachings of the present invention, which may be utilized as the controlled (or controllable) capacitance modules **485** in the frequency-temperature compensation module **420** (and attached to each side of the resonant LC tank **405** (nodes or lines **470** and **475**)). As illustrated, the controlled (or controllable) capacitance module **635** is comprised of a bank or array of a plurality (w) of switchable capacitive modules **640** of binary-weighted fixed capacitors (C_f) **620** and binary- or other differentially-weighted variable capacitors (varactors) (C_v) **615**. Any type of fixed capacitors **620** and variable capacitors (varactors) **615** may be utilized; in selected embodiments, the varactors **615** are AMOS (accumulation-mode MOSFET), IMOS (inversion-mode MOSFET), and/or junction/diode varactors. Each switchable capacitive module **640** has an identical circuit layout, and each differs by a binary weighted capacitance, with switchable capacitive module $\mathbf{640}_0$ having a capacitance of one unit, switchable capacitive module $\mathbf{640}_1$ having a capacitance of two units, and so on, with switchable capacitive module $\mathbf{640}_{(W-1)}$ having a capacitance of $2^{(w-1)}$ units, with each unit representing a particular capacitance magnitude or value (typically in femtofarads (fF) or picofarads (pF)). As mentioned above, other differential weighting schemes are equally applicable, such as linear or binary, and may also consist of providing such differential weighting by switching the reactance to a selected control voltage, thereby increasing or decreasing its effective reactance.

Within each switchable module **640**, each fixed and variable capacitance is initially equal, with the variable capacitance allowed to vary in response to the control voltage provided at node **625**. This control voltage, in turn, varies with temperature or another selected variable parameter, resulting in an overall or total capacitance provided by the controlled capacitance module **635** also varying as a function of temperature (or other parameter) and which, in turn, is utilized to vary the resonant frequency f_0. In other selected embodiments, any of a plurality of control voltages may be utilized, including static control voltages, to provide for other types of compensation, discussed below. Also within each switchable capacitive module **640**, either the fixed capacitance C_f or the variable capacitance C_v is switched into the circuit, not both, using switching coefficients p_0 though $p_{(w-1)}$. For example, in the selected embodiment, for a given or selected module **640**, when its corresponding "p" coefficient is a logic high (or high voltage), the corresponding fixed capacitance C_f is switched into the circuit and the corresponding variable capacitance C_v is switched out of the circuit (and coupled to a power rail voltage V_{DD} or ground (GND), depending whether the device is AMOS or IMOS, respectively, to avoid a floating node and to minimize the capacitance presented to the tank), and when its corresponding "p" coefficient is a logic low (or low voltage), the corresponding fixed capacitance C_f is switched out of the circuit and the corresponding variable capacitance C_v is switched into the circuit and coupled to the control voltage provided on node **625**.

In an exemplary embodiment, a total of eight switchable capacitive modules **640** (and corresponding first plurality of eight switching coefficients p_0 though P_7 have been implemented to provide 256 combinations of fixed and variable capacitances. As a result, significant control over oscillation frequency as a function of temperature variations is provided.

It should be noted, in this exemplary embodiment, by switching in or out the fixed capacitance C_f or the variable capacitance C_v, the ratio of fixed to variable changes and, correspondingly, the amount or degree of temperature-responsiveness of the controllable capacitance module **635**. For example, with increasing amounts of variable capacitance C_v, the controllable capacitance module **635** provides greater variability of capacitance in response to temperature (or other parameter), thereby adjusting the frequency response of the tank or other oscillator.

FIG. **10** is a circuit diagram illustrating an exemplary temperature dependent voltage control module **650** utilized to provide the control voltage in the controllable capacitance module **635** (of the frequency-temperature compensation module **420**) and as V_{CTRL} **480** (in FIG. **4**), in accordance with the teachings of the present invention. As illustrated, voltage control module **650** creates a temperature-dependent current I(T) (or more generally, a current I(x)), using current generator **655**, as previously discussed, using one or more combinations of PTAT, $PTAT^2$ and/or CTAT current generators, and may share the I(T) generator **415** utilized with the negative transconductance amplifier **410**, instead of providing a separate generator **655**. The temperature-dependent current I(T) (or I(x)) is mirrored through current mirror **670** to an array or bank of a plurality of switchable resistive modules or

branches **675** and a fixed capacitive module or branch **680**, all configured in parallel. In other exemplary embodiments, depending upon the parameter variation to be compensated, other control voltage generators discussed below may be utilized.

In other combinations, depending upon the selection and weighting of the PTAT, $PTAT^2$ and/or CTAT current generators, a temperature-independent current may also be generated. For example, a PTAT generator and a CTAT generator, sized to have equal magnitudes and opposite slopes, can be combined to create a current generator which provides a constant current over temperature fluctuations. Such a current generator, for example, can be utilized to provide a constant current source in the aging variation compensator illustrated in FIG. **30**. Those of skill in the art will recognize that other current sources may also be utilized, such as those which vary with power supply voltage, and may be utilized as corresponding voltage sensors.

The resistors **685** may be any type or combination of different types, such as diffusion resistors (p or n), polysilicon, metal resistors, salicide or unsalicide polysilicon resistors, or well resistors (p or n well), for example. Depending upon the type or combination of types of resistors selected, the resistors **685** generally will also have a corresponding temperature dependence (or responsiveness), providing a corresponding voltage variation across the selected resistor **685** as a function of temperature for a given current through the selected resistor **685**. For example, a diffusion resistor will generally have a high temperature coefficient (providing more voltage variation with temperature), while a polysilicon resistor will generally have a low temperature coefficient (providing less voltage variation with temperature), while a mix of a plurality of these different resistor types in series for a selected module **675** will provide a corresponding response in between these high and low response levels. Alternatively, the resistors **685** may be sized or weighted to provide different voltage levels as a function of a given current, such as a temperature-dependent current (e.g., I(T)), also thereby providing a corresponding voltage variation as a function of temperature for such a temperature-varying current.

Each switchable resistive module **675** is switched in or out of the voltage control module **650** by a corresponding "q" coefficient of a second plurality ("x") of switching coefficients q_0 though $q_{(x-1)}$. When switchable resistive module **675** is switched into the circuit (such as when its corresponding coefficient is a logic high or high voltage), the resulting voltage across its corresponding resistor **685** is also temperature-dependent, due to the temperature-dependent current I(T). In a selected embodiment, three switchable resistive modules **675** were utilized, providing 8 branch combinations. As a result, the control voltage provided to node **625** is also a function of temperature (or other parameter), thereby providing a temperature or other parameter dependence or sensitivity to the variable capacitors **615** in controllable capacitance module **635**. Other resistive modules which are more generally parameter-dependent, or which are temperature-independent, are discussed below with reference to FIGS. **23** and **26**, and FIG. **28**, respectively.

The first plurality of switching coefficients p_0 though $p_{(w-1)}$ and the second plurality of switching coefficients q_0 though $q_{(x-1)}$ may be determined post-fabrication by testing a representative IC having the clock generator of the present invention. Once a resonant frequency f_0 has been selected and/or calibrated for a given fabrication process (discussed below with reference to FIGS. **11** and **12**), the temperature (or other parameter) responsiveness of the oscillator is determined and adjusted, to provide a substantially constant selected resonant frequency f_0 for such variation in ambient or operating temperature (or other variable parameter). In the exemplary embodiments, the first plurality of switching coefficients p_0 though $p_{(w-1)}$ are determined first, by testing various combinations of coefficients, to provide a coarse level of adjustment, resulting in a substantially or mostly flat frequency response as a function of varying ambient temperature. As illustrated in FIG. **24**, more or less fixed capacitance C_f or variable capacitance C_v is switched into or out of the oscillator. For example, when the uncompensated frequency response of the oscillator to temperature variation is represented by lines **1705** or **1710**, additional variable capacitance C_v may be switched in, providing a coarse adjustment for the frequency response of the oscillator to approximately line **1715**. Conversely, also for example, when the uncompensated frequency response of the oscillator to temperature variation is represented by lines **1725** or **1730**, additional fixed capacitance C_f may be switched in, providing a coarse adjustment for the frequency response of the oscillator to approximately line **1720**.

The second plurality of switching coefficients q_0 though $q_{(x-1)}$ are then determined, also by testing various combinations of coefficients, to provide a finer level of adjustment, resulting in a substantially and significantly flat frequency response as a function of varying ambient temperature, illustrated in FIG. **24** as adjusting a partially compensated frequency response (lines **1715** or **1720**) to the substantially flat response of line **1700**, through selection of the temperature responsiveness of the various resistors **685**. The first and second pluralities of coefficients are then loaded into respective registers **495** and **455** in all of the ICs fabricated in the selected processing run (or batch). Depending on the fabrication processing, under other circumstances, it is possible that for higher accuracy, each IC may be separately calibrated. As result, in conjunction with the temperature compensation provided by the negative transconductance amplifier **410** and I(T) generator **415**, the overall frequency response of the clock generator is substantially independent of temperature fluctuations.

In other exemplary embodiments, the first plurality of switching coefficients p_0 though $p_{(w-1)}$ and the second plurality of switching coefficients q_0 though $q_{(x-1)}$ may also be determined and varied dynamically during operation of the oscillator, such as through sensor(s) **1440** and A/D converter **1445**, as illustrated in FIG. **21**, or through sensor(s) **1815** and control logic (or control loop) **1810** illustrated in FIG. **25**. In these alternative embodiments, the stored first and second pluralities of coefficients may be eliminated or bypassed, with corresponding voltages applied directly as control signals to the respective switching components as illustrated in FIGS. **9** and **10** (and, similarly, extended to the other pluralities of coefficients discussed below).

For example, as illustrated in FIG. **26**, as discussed in greater detail below, any of a plurality of current sources **1955** may be provided in various combinations to a plurality of resistive modules, to create a plurality of control voltages responsive to a selected parameter "P", which may be switched in any combinations to each of the plurality of controlled reactance modules **1805**, which may be embodied, for example, as controlled capacitance modules **1505** (FIG. **22**), to control the effective reactance of the resonator. In addition, any of a plurality of constant (temperature independent) control voltages may also be created, as illustrated in FIG. **28**. Moreover, other or additional types of current sources may be utilized, either to generate the control voltage or to provide sensor **385**, **1440** capability, such as those which may vary with the supply voltage VDD, or which are inde-

pendent of both supply voltage, temperature, and other parameters. Any of these control voltages may be utilized to provide continuous control in real time, in addition to discrete control, over parameter variations, such as temperature variations.

As a consequence, the overall capacitance provided to the resonant LC tank **405** is distributed into a combination of fixed and variable portions, with the variable portions responsive to provide temperature compensation and, therefore, control over the resonant frequency f_0. The more variable capacitance C_v which is switched into the circuit (controlled capacitor module **635**), the greater the frequency response to fluctuations in ambient temperature. As indicated above, both fixed and variable capacitors may be implemented using variable capacitors (varactors) coupled or switched, respectively, to substantially constant or variable voltages.

In addition to providing temperature compensation, it should be noted that a switched or controlled (or controllable) capacitance module **635** may also be utilized to select or tune the resonant frequency f_0. It will also be apparent to those of skill in the art that a switched or controllable capacitance module **635** may also be utilized to provide a frequency response to other parameter variations, such as fabrication process variations, frequency, and voltage fluctuations. In addition, as discussed below with reference to FIGS. **20** and **25-27**, a capacitance, an inductance, a resistance, or any other reactance or impedance element may be utilized in these various exemplary embodiments, providing a controlled reactance or impedance module to provide a selected frequency response to any of a plurality of variable parameters, such as temperature, voltage, fabrication process, or frequency.

FIG. **22** is a circuit diagram illustrating an exemplary second controlled capacitor module **1500** utilized (with module **1600** of FIG. **23**) (in lieu of or in addition to modules **485** and **480**) in a frequency-temperature compensation module **420**, or more generally, in a frequency controller **215**, **349**, **1415**, in accordance with the teachings of the present invention. The second controlled capacitance module **1500** operates similarly to the first controlled capacitance module **635**, but utilizes variable capacitances, instead of both fixed and variable, and utilizes a plurality of different control voltages, instead of a single control voltage. In addition, such variable capacitances are not coupled to or decoupled from the resonator (i.e., the variable capacitances are always coupled to the resonator), and instead are switched to different control voltages to control the frequency response as a function of a selected parameter such as temperature. Selected embodiments, moreover, may utilize as few as one module, and the differential weighting may be accomplished by switching to a selected control voltage of a plurality of control voltages.

Referring to FIG. **22**, the second controlled capacitor module **1500** utilizes at least one of a plurality ("g") of variable capacitance modules **1505**, each of which contains variable capacitances (C_v) $\mathbf{1515}_{AO}$ through $\mathbf{1515}_{B(g-1)}$ (illustrated in pairs A and B, corresponding to balanced coupling to node **475** or **470**, and illustrated with binary-weighting) which are switchable (through pluralities of transistors or other switches $\mathbf{1520}_0$ through $\mathbf{1520}_{(g-1)}$) to a selected control voltage of a plurality of control voltages V_0, $V_1(x)$, through $V_{(k-1)}(x)$, where control voltage V_0 is substantially static (substantially non-responsive to the selected parameter "x", such as temperature), while the remaining control voltages $V_1(x)$ through $V_{(k-1)}(x)$ are generally responsive or sensitive to the selected parameter "x", such as temperature. As illustrated, the backplates of each corresponding pair of variable capacitors **1515** (A and B) are coupled to each other (shorted together), and then connected via a switch to a selected control voltage. Each such pair of variable capacitances **1515** is switchable, through corresponding coefficients (illustrated as a fourth plurality of coefficients $d_0, d_1, \ldots d_{(k-1)}$ through $h_0, h_1, \ldots h_{(k-1)}$, such that each module **1505** may be switched separately and independently to any of the plurality of control voltages V_0, $V_1(x)$, through $V_{(k-1)}(x)$. As a consequence, these switchable modules may remain coupled to the resonator with the effective impedance (e.g., reactance) varied through switching to one or more control voltages.

FIG. **23** is a circuit diagram illustrating an exemplary second voltage control module **1600** utilized in a frequency-temperature compensation module in accordance with the teachings of the present invention. As illustrated in FIG. **23**, a parameter-sensitive or responsive current source **655** (such as any of the various CTAT, PTAT and $PTAT^2$ temperature sensitive current sources, and their combinations, previously discussed an illustrated in FIGS. **7A-7D**) is provided (through one or more current mirrors (e.g., **670**, **510**, **520**)) to an array or bank of a plurality "k−1" of resistive modules **1605** (illustrated as modules $\mathbf{1605}_0$, $\mathbf{1605}_1$, through $\mathbf{1605}_{(k-1)}$), each of which provides a separate or independent control voltage, $V_1(x)$, $V_2(x)$, through $V_{(k-1)}(x)$ which are provided to modules **1505** (of FIG. **22**). The various corresponding resistors $\mathbf{1620}_0$, $\mathbf{1620}_1$, through $\mathbf{1620}_{(k-1)}$ may be any of the types, sizes or weights previously discussed with reference to FIG. **10**, to provide any selected voltage response to a selected parameter, such as temperature. A static control voltage, V_0, as illustrated, may be generated utilizing any voltage divider coupled between the voltage supply rail V_{DD} and ground, with corresponding resistance magnitudes or values $\mathbf{1605}_0$ and $\mathbf{1605}_y$ selected to provide the desired static voltage level. In addition, generation of a plurality of different static or constant (i.e., temperature independent) voltages is illustrated in FIG. **28**, by combining different current sources having differently shaped currents in response to temperature (or another parameter) with different temperature-dependent resistors having complementary or opposing temperature responses, resulting in a plurality of control voltages having different magnitudes and substantially constant over temperature variations. Any of these various voltages may be utilized, as needed, as any of the various control voltages.

In the exemplary embodiments, each such control voltage of the plurality of control voltages is different, to provide a plurality of control voltages, each of which are differently responsive or shaped (i.e., provide different responses (response curves) as a function of variations in the selected parameter such as temperature), may respond to different parameters, and others which may be substantially constant with respect to a selected parameter. Depending upon the selected embodiment, the array or bank of resistive modules **1605** may be switchable (through corresponding transistors **1610** (illustrated as transistors $\mathbf{1610}_0$, $\mathbf{1610}_1$, through $\mathbf{1610}_{(k-1)}$), and thereby switched into or out of the array **1600**, or may be statically included (fixed connections **1615**, illustrated as dashed lines in FIG. **23**) to automatically generate a predetermined number of control voltages V_0, $V_1(x)$, through $V_{(k-1)}(x)$. Depending upon the selection of resistors **1620** (and/or transistors **1610**, if included), each of the various control voltages V_0, $V_1(x)$, through $V_{(k-1)}(x)$ will be different or otherwise provide a different response to the selected parameter or variable, such as a different temperature response.

Similarly, FIG. **26** is a circuit and block diagram illustrating an exemplary third voltage control module **1900** which may be utilized to provide control voltages to any of the various modules in accordance with the teachings of the

present invention. As illustrated in FIG. **26**, a plurality of parameter-sensitive or responsive current sources **1955** (such as any of the various CTAT, PTAT and $PTAT^2$ temperature sensitive current sources, and their combinations, previously discussed an illustrated in FIGS. **7**A-**7**D) is provided (through one or more current mirrors (e.g., 670, 510, 520)) to an array or bank of a plurality "n−1" of resistive modules **1905** (illustrated as modules $\mathbf{1905}_0$, $\mathbf{1905}_1$, through $\mathbf{1905}_{(n-1)}$). Each of the resistive modules **1905** provides a separate or independent control voltage, $V_0(P)$, $V_1(P)$, $V_2(P)$, through $V_{(n-1)}(P)$, creating a plurality of control voltages which are responsive or dependent upon the selected parameter "P", and which are provided to controlled reactance modules **1805**, controlled capacitance modules **1505** (of FIG. **22**), or any of the other modules utilizing one or more control voltages. The various corresponding resistors $\mathbf{1920}_0$, $\mathbf{1920}_1$, through $\mathbf{1920}_{(n-1)}$ may be any of the types, sizes or weights previously discussed, to provide any selected voltage response to a selected parameter. The selection of current source (or combination of current sources) and resistor size and type allows the shaping of the response of any desired control voltage to the selected parameter. In addition, any of the plurality of different static or constant (i.e., temperature independent) voltages illustrated in FIG. **28** also may be utilized, as needed, as any of the various control voltages for any of the modules discussed.

Depending upon the selected embodiment, the array or bank of resistive modules **1905** may be switchable (through corresponding transistors **1915** (illustrated as transistors $\mathbf{1915}_0$, $\mathbf{1915}_1$, through $\mathbf{1915}_{(n-1)}$), and thereby switched into or out of the array, dynamically or statically, to automatically generate a plurality of control voltages $V_0(P)$, $V_1(P)$, $V_2(P)$, through $V_{(n-1)}(P)$. Each of these different control voltages may then be switched (using switches **1930**, such as a full crossbar switch), in any combination, statically or dynamically, under the switching control of control signals and/or coefficients **1950**, to controlled reactance modules **1805**, which may be coupled to the resonator or which also may be switched into or out of the tank. As a consequence, any of these control voltages may be utilized to control the effective reactance of the resonator (oscillator), providing both discrete and continuous control of the resulting resonant frequency. For example, any of these parameter-dependent control voltages $V_0(P)$, $V_1(P)$, $V_2(P)$, through $V_{(n-1)}(P)$, or any of the substantially parameter-independent control voltages (FIG. **28**), may be provided to the controlled impedance modules **1305** or the controlled capacitance modules **1505** or **1805** to vary the effective capacitance provided to the resonator, providing frequency control over variations from any of a plurality of parameters.

Referring again to FIG. **22**, when each of these different control voltages V_0, $V_1(x)$, through $V_{(k-1)}(x)$, or more generally, $V_0(P)$, $V_1(P)$, $V_2(P)$, through $V_{(n-1)}(P)$, and any of the substantially constant control voltages, is available and switchable to the variable capacitances C_v **1515** in the variable capacitance modules **1505** through the fourth plurality of coefficients $d_0, d_1, \ldots d_{(k-1)}$ through $h_0, h_1, \ldots h_{(k-1)}$, a highly flexible, fine-tuned and highly controllable frequency response to the selected parameter (such as temperature) is provided to the resonator **405**, enabling highly accurate frequency control over the resonant frequency f_0. For example, variable capacitances $\mathbf{1515}_{A(g-1)}$ and $\mathbf{1515}_{B(g-1)}$ in module $\mathbf{1505}_{(g-1)}$ may be switched to control voltage $V_1(x)$ through parameter h_1 (or a corresponding dynamically applied voltage, as a control signal) being set to a logic high or high voltage with the remaining h parameters of the fourth plurality of parameters set to a logic low or low voltage, providing a first frequency response as a function of temperature or another selected parameter, while variable capacitances $\mathbf{1515}_{A0}$ and $\mathbf{1515}_{B0}$ in module $\mathbf{1505}_0$ may be switched to control voltage $V_{(k-1)}(x)$ through parameter $d_{(k-1)}$ (or a corresponding dynamically applied voltage, as another control signal) being set to a logic high or high voltage with the remaining d parameters of the fourth plurality of parameters set to a logic low or low voltage, providing a second frequency response as a function of temperature or another selected parameter, and so on. As discussed above, the fourth plurality of coefficients $d_0, d_1, \ldots d_{(k-1)}$ through $h_0, h_1, \ldots h_{(k-1)}$, also may be determined post-fabrication through testing one or more ICs, or may also be determined and varied dynamically during operation of the oscillator, such as through sensor(s) **1440** and A/D converter **1445**, as illustrated in FIG. **21**, or through sensor(s) **1815** and control logic (or control loop) **1810** illustrated in FIG. **25**. More generally, such control through either coefficients or control signals is illustrated in FIG. **26**, and can be utilized to provide either or both discrete or continuous frequency control as a function of any selected parameter, such as temperature, voltage, fabrication process, age, or frequency.

In addition, in lieu of stored coefficients for the first, second or fourth pluralities of coefficients, particularly when the corresponding values would be determined dynamically, as discussed above, corresponding voltages may be directly applied to the various switches (e.g., transistors **1520** or the switching transistors of modules **640** and **650**), as control signals, as mentioned above.

Referring again to FIG. **4**, another compensation module is also utilized to provide greater control and accuracy over the resonant frequency f_0, also for applications in which greater accuracy and less variance (or frequency drift) may be required, such as to provide a frequency accuracy of approximately ±0.25% or better over PVT. In these circumstances, a process variation compensation module **425** may be utilized, to provide control over the resonant frequency f_0 independently of fabrication process variations, such as the exemplary modules illustrated in FIGS. **11** and **12**. As indicated above, any of these various modules may include any impedance, reactance, or resistance, and be made responsive to any selected parameter, such as temperature, process variation, voltage variation, and frequency variation.

FIG. **11** is a circuit diagram illustrating an exemplary first process variation compensation module **760** in accordance with the teachings of the present invention. The first process variation compensation module **760** may be utilized as the process compensation modules **460** in FIG. **4**, with each module attached to a rail or side of the resonant LC tank **405** (lines or nodes **470** and **475**). In addition, each first process variation compensation module **760** is controlled by a third plurality ("y") of switching coefficients r_0 though $r_{(y-1)}$, stored in register **465**. The first process variation compensation module **760** provides an array of switchable capacitive modules having differentially-weighted (e.g., binary-weighted), first fixed capacitances **750**, for adjustment and selection of the resonant frequency f_0, by switching in or out a plurality of fixed capacitances **750**, through a corresponding plurality of switching transistors **740** (controlled by a corresponding "r" coefficient). Again, as each capacitance branch is switched in or out of the array or circuit **760**, the corresponding first fixed capacitance is added or subtracted from the total capacitance available for oscillation in the resonant LC tank, thereby changing the effective reactance and modulating the resonant frequency. The third plurality of switching coefficients r_0 though $r_{(y-1)}$ is also determined post-fabrication using test ICs, generally as an iterative process with the determinations of the first and second (or fourth) pluralities of

switching coefficients. This calibration is accomplished using the frequency calibration module (**325** or **430**) and a reference oscillator known to have a predetermined frequency. The determined "r" coefficients are then stored in the corresponding registers **465** of the ICs of that production or process batch. Alternatively, each IC may be calibrated separately, for example.

In addition to such calibration methods, the third plurality of switching coefficients r_0 though $r_{(y-1)}$ may also be determined using other methods, discussed below, such as using various voltage and current sensors to measure parameters or variables which reflect fabrication process parameters, such as transistor threshold voltages, resistance magnitudes or values of the tank, or absolute current levels produced by the various current sources. Such measured values may then be utilized to provide corresponding coefficients (the third plurality of switching coefficients r_0 though $r_{(y-1)}$) and/or control signals for corresponding frequency adjustment. For example, such measured or sensed values may be converted to digital values, which are then indexed to a lookup table in memory, which then provides stored values based on known values, or other calibrations or modeling.

To avoid additional frequency distortions, several additional features may be implemented with this first process variation compensation module **760**. First, to avoid additional frequency distortion, the on resistance of the MOS transistors **740** should be small, and therefore the transistors' width/length ratio is large. Second, large capacitances may be split into two branches, with two corresponding transistors **740** controlled by the same "r" coefficient. Third, to provide for the resonant LC tank to have a similar load under all conditions, when a first fixed capacitance **750** is switched in or out of the circuit **760**, a corresponding second fixed capacitance **720**, as a "dummy" capacitor (having a significantly smaller capacitance or the smallest size allowed by the design rules for the fabrication process), is correspondingly switched out of or into the circuit, based on the inverse of the corresponding "r" coefficient. As a consequence, approximately or substantially the same on resistance of the transistors **740** is always present, with only the amount of capacitance varied.

As an alternative to the use of the "dummy" capacitances, metal fuses or the like could be utilized instead of the transistors **740**. Metal fuses would be left intact to include the corresponding fixed capacitance **750**, and could be "blown" (open-circuited) to remove the corresponding fixed capacitance **750** from the resonant LC tank **405**.

FIG. **12** is a circuit diagram illustrating an exemplary second process variation compensation module **860** in accordance with the teachings of the present invention. The second process variation compensation module **860** may be utilized as the process compensation modules **460** in FIG. **4**, with each module attached to a rail or side (lines **470** and **475**) of the resonant LC tank **405**, instead of modules **760**. More generally, the second process variation compensation module **860** is utilized as part of frequency controller (**215**, **349** or **1415**), such as process (or other parameter) modulator or compensator **1430** (FIG. **21**). In addition, each second process variation compensation module **760** would also be controlled by a third plurality of switching coefficients r_0 though $r_{(y-1)}$ stored in register **465**. (Because of the different circuitry employed in each exemplary process variation compensation module **760** or **860**, however, the corresponding third pluralities of switching coefficients r_0 though $r_{(y-1)}$ generally would, of course, be different from each other.) In addition, such switching may be controlled through use of any control signals, discussed above.

It should be noted that FIG. **12** provides a varactor illustration different from those utilized in other Figures, in which a varactor **850** is represented by a MOS transistor, rather than as a capacitor with an arrow through it. Those of skill in the art will recognize that varactors are often AMOS or IMOS transistors, or more generally MOS transistors, such as those illustrated in FIG. **12**, and configured by shorting the transistor's source and drain. As a consequence, the other illustrated varactors may be consider to include, as potential embodiments, the AMOS or IMOS transistors as configured as in FIG. **12**. In addition, the varactors **850** may also be binary-weighted with respect to each other, or may use another differential weighting scheme.

The second process variation compensation module **860** has a similar structural concept, but additional notable differences from the first process variation compensation module **760**. The second process variation compensation module **860** provides an array or bank of a plurality of switchable variable capacitive modules **865**, without MOS switches/transistors, and hence the losses or loading through the MOS transistors are eliminated. Instead, the load appears as a low loss capacitance; such low loss also implies that the oscillator start-up power is less. In the second process variation compensation module **860**, a MOS varactor **850** is switched either to Vin, which may be any of the various pluralities of control voltages discussed above, to provide a corresponding capacitance level to the resonant LC tank **405**, or may be switched to ground or the power rail (voltage V_{DD}), thereby providing either the minimum capacitance or the maximum capacitance to the resonant LC tank **405** based upon the varactor **850** geometry. For AMOS, switched to voltage V_{DD} would provide minimum capacitance and switched to ground would provide maximum capacitance, while the opposite is the case for IMOS. Again, the second process variation compensation module **860** is comprised of an array of variable capacitances, as varactors **850**, for adjustment and selection of the resonant frequency f_0, by coupling or switching a selected varactor **850** to any of a plurality of control voltages (Vin), or to ground or V_{DD}, such as switching between a first voltage and a second voltage, through a corresponding "r" coefficient or through application of a corresponding control signal. In another alternative, instead of a plurality or an array, one varactor **850** may be utilized, with its effective reactance provided to the tank controlled by a selected control voltage.

As each capacitance branch is switched to a corresponding control voltage, ground or V_{DD}, the corresponding variable capacitance is added to or not included in the total capacitance available for oscillation in the resonant LC tank, thereby changing its effective reactance and modulating the resonant frequency. More particularly, for an AMOS implementation, coupling to V_{DD} (as V_{in}) provides lesser capacitance and coupling to ground (V_{in}=0) provides greater capacitance, with the opposite holding for an IMOS implementation, in which coupling to V_{DD} (as V_{in}) provides greater capacitance and coupling to ground (V_{in}=0) provides lesser capacitance, where it is assumed that the voltage on the rails of the LC tank (nodes or lines **470** and **475** of FIG. **4**) is between zero V and voltage V_{DD}, and significantly or substantially far from either voltage level. Coupling to voltages between V_{DD} and ground, such as many of the various control voltages, as Vin, will provide a corresponding, intermediate level of capacitance to the tank. The third plurality of switching coefficients r_0 though $r_{(y-1)}$ is also determined post-fabrication using test ICs, also generally as an iterative process with the determinations of the first and second pluralities of switching coefficients. The determined "r" coefficients are then stored in the corresponding registers **465** of the ICs of that production or

process batch. Again, individual ICs may also be calibrated and tested separately. In addition, any selected number of modules **850** may be controlled dynamically, to provide continuous frequency control during oscillator operation.

As indicated above, depending upon the type (AMOS or IMOS) of varactor, switching any of the variable capacitive modules **865** to V_{DD} or ground, as first and second voltage levels, results in the corresponding maximum capacitance or no (negligible) capacitance being included as effective capacitance for the resonator (LC tank). As mentioned above, however, other capacitance levels intermediate between such maxima and minima may also be generated, by switching the variable capacitive modules **865** to a corresponding control voltage. Utilizing a plurality of control voltages having different magnitudes, results in a corresponding capacitance of the variable capacitive modules **865** being added to (or subtracted from) the LC tank, thus changing its effective reactance and modulating the resonant frequency.

FIG. **28** is a circuit diagram illustrating an exemplary fourth voltage control module **2050** utilized in frequency, process and other parameter compensation modules in accordance with the teachings of the present invention. Referring to FIG. **28**, a plurality of substantially constant voltage modules **2060** (illustrated as $\mathbf{2066}_A$, $\mathbf{2060}_B$, $\mathbf{2060}_C$ through $\mathbf{2060}_K$) are utilized to create a corresponding plurality of control voltages which are substantially constant with respect to a selected parameter, such as temperature, and which have a corresponding plurality of different magnitudes, creating a plurality of control voltages V_A, V_B, V_C through V_K, which have different magnitudes. As illustrated, the plurality of different, substantially static or constant (i.e., temperature independent) voltages is created by combining different current sources **2055** (illustrated as current sources $\mathbf{2055}_A$, $\mathbf{2055}_B$, $\mathbf{2055}_C$ through $\mathbf{2055}_K$), each having different responses to temperature or another parameter (i.e., differently shaped currents in response to temperature (or another parameter)), with a corresponding plurality of resistors **2040** (illustrated as corresponding resistors $\mathbf{2040}_A$, $\mathbf{2040}_B$, $\mathbf{2040}_C$ through $\mathbf{2040}_K$), each of which have a temperature or other parameter-dependent response which is opposing or complementary to the corresponding current source **2055** of the particular module **2060**. Each corresponding current source **2055** and resistor **2040** is selected to have such opposing or complementary responses with the other, to effectively cancel the other's response to the selected parameter. For example, a current source **2055** is selected to have a particular combination of PTAT, CTAT or $CTAT^2$ current sources of appropriate magnitude, and a resistor **2040** is selected based on size, type, and so on, such that the resulting voltage is substantially constant over the parameter variations, e.g., temperature variations. Any of these various voltages may be utilized, as needed, as any of the various control voltages, such as to provide a corresponding Vin for the variable capacitive modules **865** illustrated in FIG. **12**, to adjust the effective capacitance (reactance) of the resonator and the resulting resonant frequency.

It should also be noted that the illustrated embodiments for modules such as temperature compensator **315** (or **410**, **415** and/or **420**) and process variation compensator **320** (or **425** and **460**), such as those illustrated in FIGS. **6-12**, may be utilized for other purposes. For example, the various illustrated embodiments for the compensator **315** (or **410**, **415** and/or **420**) may be made dependent upon process variation, rather than temperature. Similarly, the various illustrated embodiments for the compensator **320** (or **425** and **460**) may be made dependent upon temperature, rather than process variation. As a consequence, the embodiments for these and other modules should not be considered limited to the exemplary circuits and structures illustrated, as those of skill in the art will recognize additional and equivalent circuits and applications, all of which are within the scope of the invention.

As indicated above, the various illustrated controlled capacitance modules (**485**, **635**, **460**, **760**, **860**, **1501**) may be generalized to any reactance or impedance element, whether a capacitance, inductance, resistance, or combination of capacitance, inductance or resistance. An array or bank **1300** of such a plurality ("a") of switchable, controlled impedance (or reactance) modules **1305** are illustrated in FIG. **20**, and may be utilized within the frequency controller (**215**, **349**, **1400**) of the present invention, as any of the various modulators or compensators (**315**, **320**, **355**, **1420**, **1425**, **1430**). Each differently weighted, controlled reactance or impedance module **1305** (illustrated as $\mathbf{1305}_0$, $\mathbf{1305}_1$, through $\mathbf{1305}_{(a-1)}$) is comprised of one or more fixed reactances Z_f**1315**, variable reactances Z_v **1310**, or "dummy" reactances **1320**, which are switchable in response to a corresponding coefficient "s" of a fifth plurality of coefficients (s_0, s_1, through $s_{(a-1)}$). The array of controlled reactance or impedance modules **1305** generally may be implemented to operate as discussed above with respect to any of the various controlled capacitance modules, in any of the various embodiments. The fifth plurality of coefficients may be determined post-fabrication, or dynamically, as discussed above for the other sets of coefficients. In addition, depending upon the implementation, the various reactances or impedances may be switched in or out of the array **1300** or switched to various control voltages or ground, as previously illustrated, and may be utilized to provide a selected frequency response of the oscillator in response to any of a plurality of parameters, such as temperature variations, voltage fluctuations, fabrication process, or frequency.

Similarly, referring to FIG. **25**, an array or bank of a plurality "n" of switchable, controlled reactance modules **1805** are illustrated (as controlled reactance modules $\mathbf{1805}_0$ through $\mathbf{1805}_{(n-1)}$), and also may be utilized within the frequency controller (**215**, **1415**) of the present invention, as any of the various modulators or compensators (**315**, **320**, **355**, **1420**, **1425**, **1430**). These controlled reactance modules **1805** may also be binary, linearly, or otherwise differently weighted, and switched in or out of the various circuits, switched to one or more control voltages, or any combination thereof, and may be responsive to any selected parameter. The array of controlled reactance modules **1805** generally may be implemented to operate as discussed above with respect to any of the various controlled capacitance modules, in any of the various embodiments. Rather than being switched to the oscillator through a plurality of coefficients, in this exemplary embodiment, the controlled reactance modules **1805** are switched dynamically, through voltages or currents provided directly by sensors **1815** and control logic **1810**, with feedback provided (line or node **1820**), and which may be implemented as known in the art, or as illustrated above, with all such variations considered within the scope of the present invention. In addition, the reactance modules may be more considered more broadly, as impedance modules, with both a resistive and/or reactance aspect, such as utilizing the various resistors illustrated in FIG. **29**.

For example, such variations in the selected parameter may be determined in any of a plurality of ways previously discussed, such as through a temperature-sensitive current source, other temperature sensors, or any other type of sensor which is responsive to the selected parameter. For example, a sensor may comprise a voltage across a diode, providing a voltage output responsive to temperature. Referring to FIG. **21**, the output of such a sensor **1440** may be provided to A/D

converter **1445**, which provides a digital output indicative of the level of the sensed parameter, which may then be utilized as the corresponding coefficients (any of the pluralities of coefficients discussed above), or utilized to dynamically switch any of the various controlled reactance or impedance modules (e.g., **1305**, **1805**) or the various second controlled capacitance modules. Similarly, sensor **1815** output may be provided to control logic **1810**, which may also adjust the various reactances, either statically or dynamically, and with or without feedback from the resonator.

FIG. **27** is a circuit and block diagram illustrating an exemplary voltage variation compensation module **2000** in accordance with the teachings of the present invention, and may be utilized as a voltage variation compensator **380**, **1455** illustrated in FIGS. **3** and **21**. Referring to FIG. **27**, a switchable resistive module **1650** forms a voltage divider, using resistors $\mathbf{1620}_0$ and $\mathbf{1620}_y$, providing voltage V_0. In the event of fluctuations in the supply voltage (power rail) V_{DD}, voltage V_0 is correspondingly changed. As voltage V_0 can be switched (switches **1930**) (as discussed above) to any of the controlled reactance modules **1805**, under the control of control signals or coefficients **1950**, the effective capacitance to the tank is also varied, thereby modulating the resonant frequency. As a result, the resonant frequency may be controlled over such voltage fluctuations. Other implementations will be apparent based upon the other illustrated embodiments, and are also within the scope of the invention

As indicated above, the resonant frequency of the tank may also be modified by varying the resistance to the tank, in addition to the intrinsic or parasitic resistances R_L **445** and R_C**450** of FIG. **4**. FIG. **29** is a circuit diagram illustrating an exemplary resistive control module **2100** which may be utilized as or as part of any of the various frequency control module and the various frequency controllers in accordance with the teachings of the present invention. Such a resistive control module **2100** may be inserted into node Q in resonator **405** of FIG. **4**, in series with inductor **435** and R_L **445**, or in series with capacitor **440** and R_C**450**, or both. Each switchable resistive module **2115** (illustrated as the plurality of switchable resistive modules $\mathbf{2115}_M$, $\mathbf{2115}_N$, $\mathbf{2115}_O$ through $\mathbf{2115}_U$) has a differently weighted (such as a binary-weighted), resistor **2105** (illustrated as corresponding resistors $\mathbf{2105}_M$, $\mathbf{2105}_N$, $\mathbf{2105}_O$ through $\mathbf{2105}_U$), and is switchable in or out of the array or module **2100** through corresponding transistors or switches **2110** (illustrated as transistors $\mathbf{2110}_M$, $\mathbf{2110}_N$, $\mathbf{2110}_O$ through $\mathbf{2110}_U$), under the control of control signals and/or coefficients **1950**. As indicated above, such switching also provides another mechanism to control or modulate the resonant frequency of the resonator **405**, and may be a function of any selected parameter, or may be parameter independent, such as for resonant frequency selection.

FIG. **30** is a block diagram illustrating an exemplary age variation compensator **2200** in accordance with the teachings of the present invention. As illustrated in FIG. **30**, various sensors are utilized to measure a relevant parameter which is or may be affected by the passage of time, or which otherwise changes over the lifetime of an IC, such as a voltage sensor **2205** to measure a threshold voltage of a transistor, a resistance sensor **2210** to measure one or more resistance magnitudes or values of the tank, and/or a current sensor to measure absolute current levels produced by the various current sources. A selected measurement, at a given point in time is provided (via multiplexer **2220**) to ADC **2225**, for conversion into a digital value, which is stored in a register or other non-volatile memory **2230**. When the IC is first powered on or otherwise initialized, an initial measurement is stored in the register **2230**, to provide a basis for comparison for subsequent measurements. Subsequently, additional measurements may be performed, with the resulting values stored as corresponding current values in register **2230**, illustrated as current and initial values for voltage, resistance and current. For a given parameter, such as voltage, current and initial values may be read and compared, comparator **2235**, which then provides a corresponding age compensation signal proportional to any difference between the two values. Such difference values provided by the age compensation signal may then be utilized to provide corresponding coefficients and/or control signals for corresponding frequency adjustment. For example, such age compensation signals may be indexed to a lookup table in memory **2240**, which then provides stored values based on known values, or other calibrations or modeling of age affects, and provides for corresponding frequency adjustments using any of the various modulators and compensators discussed above.

As mentioned above, the clock generator and timing/frequency reference (**100**, **200**, **300**) of the present invention may utilizing a wide variety of oscillators. In exemplary embodiments, resonant LC oscillators are utilized to provide an output signal, as a first reference signal, having a comparatively higher Q, lower jitter, and decreased phase noise. Exemplary first and second differential LC oscillators have been discussed above with reference to FIGS. **4**, **6** and **8**. Additional types of resonant oscillators are also within the scope of the present invention, and exemplary LC oscillators are illustrated in and discussed below with reference to FIGS. **31-37**, with an active inductor illustrated in FIG. **38**. These additional exemplary LC oscillators and inductor types (passive or active) may be utilized equivalently to the LC oscillators previously discussed, and to illustrate their equivalent operation, are also illustrated in conjunction with exemplary frequency controller components previously described and illustrated in FIG. **4**, namely, compensation modules **420** and **425**. It should be understood that any of the other controller reactance modules, control voltage generators, frequency control, calibration, frequency selection, frequency division, and other components may also be utilized equivalently, in addition to those specifically illustrated in FIGS. **31-37**.

It should also be noted that the exemplary active inductor illustrated in FIG. **38**, or any other active inductor, may be substituted for any of the passive inductors illustrated in any of the topologies of any of the FIGS. **1-37**. Similarly, various topologies are illustrated using n-MOS or p-MOS transistors; any types of transistors may be utilized equivalently. Accordingly, use of any passive or active inductor, or any type of transistor, is considered equivalent and within the scope of the present invention.

The various LC oscillators illustrated below may provide either a differential or a single-ended first reference signal. The various compensation modules **420** and **425**, which may be implemented in a wide variety of ways as discussed above, as controlled reactance modules, may be combined with the various oscillators in a plurality of ways. First, the controlled reactance modules (illustrated as compensation modules **420** and **425**) may be coupled in parallel with any of the one or more illustrated capacitors. In many instances, multiple instances of the controlled reactance modules can be coupled to the illustrated LC oscillators. Consequently, the corresponding nodes for coupling are labeled as node "A" and node "B", to indicate the corresponding nodes for coupling to the given LC oscillator topology, with additional instances available for coupling illustrated as a corresponding node "A'" (A-prime) and node "B' " (B-prime) and/or corresponding node "A"" (A-double-prime) and node "B"" (B-double-

prime). Second, not separately illustrated in the various FIGS. **31-37**, the controlled reactance modules (illustrated as compensation modules **420** and **425**) may be utilized in lieu of and substitute for any of the one or more illustrated capacitors. Those of skill in the art will recognize innumerable other variations, all of which are considered equivalent and within the scope of the invention.

FIG. **31** is a circuit diagram illustrating a third exemplary LC oscillator **2260**, implemented with a differential n-MOS cross-coupled topology, which may be utilized in accordance with the teachings of the present invention, and is a variation of the LC oscillator illustrated in FIG. **8**. As illustrated, the apparatus **2250** comprises the third exemplary LC oscillator **2260**, having a differential n-MOS cross-coupled topology, and the frequency controller and frequency calibration modules (compensation modules **420** and **425**) previously discussed in the double-balanced configuration of FIG. **4**. The output frequency f_0 is obtained between nodes $\mathbf{470}_A$ and $\mathbf{475}_A$, which are equivalent to the nodes **470** and **475** previously discussed, and may be substituted as such for all references in the Figures and this specification.

The cross-coupled n-MOS transistors **2251** and **2251** are coupled through a current mirror **530**A (or **530**B), to a bias current, such as using the parameter-responsive current I(x) generator **515** (or **415**), also previously discussed or, alternatively, another fixed or variable current source. The frequency controller modules (**480**, **485** with coefficient registers **455** and **495**) and frequency calibration modules (**460** with coefficient register **465**) are coupled to the oscillator across nodes A and B as illustrated, and also operate as previously discussed. The inductors **2253** and **2254** (with illustrated resistances) may be replaced equivalently by the center-tap inductor **2257** (center-tap coupled to V_{DD}) and inserted between nodes A and B, as illustrated, and may be fixed or variable. In addition, the various capacitances may be implemented to be either fixed or variable, also as previously discussed, and are illustrated with both fixed and variable capacitors. In exemplary embodiments, the resistances may also be fixed or varying.

It will be apparent to those of skill in the art that a similar cross-coupled n-MOS version of the oscillator illustrated in FIG. **6** may be implemented similarly (by removing (replacing with short-circuits) the illustrated cross-coupled p-MOS transistors M**1** and M**2**).

FIG. **32** is a circuit diagram illustrating a fourth exemplary LC oscillator **2280**, implemented with a differential p-MOS cross-coupled topology, which may be utilized in accordance with the teachings of the present invention, and is also a variation of the LC oscillator illustrated in FIG. **8**. As illustrated, the apparatus **2270** comprises the fourth exemplary LC oscillator **2280**, having a differential p-MOS cross-coupled topology, and the frequency controller and frequency calibration modules (compensation modules **420** and **425**) previously discussed in the double-balanced configuration of FIG. **4**. The output frequency f_0 is obtained between nodes $\mathbf{470}_B$ and $\mathbf{475}_B$, which are also equivalent to the nodes **470** and **475** previously discussed, and may be substituted as such for all references in the Figures and this specification.

The cross-coupled p-MOS transistors **2271** and **2271** are coupled through a current mirror **510** (or **520**) to a bias current, such as using the parameter-responsive current I(x) generator **515** (or **415**), also previously discussed or, alternatively, another fixed or variable current source. The frequency controller modules (**480**, **485** with coefficient registers **455** and **495**) and frequency calibration modules (**460** with coefficient register **465**) are coupled to the oscillator across nodes A and B as illustrated, and also operate as previously discussed. The inductors **2273** and **2274** (with illustrated resistances) may be replaced equivalently by the center-tap inductor **2277** (center-tap coupled to ground) and inserted between nodes A and B, as illustrated, and may be fixed or variable. In addition, the various capacitances may be implemented to be either fixed or variable, also as previously discussed, and are illustrated with both fixed and variable capacitors. In exemplary embodiments, the resistances may also be fixed or varying.

Also, it will be apparent to those of skill in the art that a similar cross-coupled p-MOS version of the oscillator illustrated in FIG. **6** may be implemented similarly (by removing (replacing with short-circuits) the illustrated cross-coupled n-MOS transistors M**3** and M**4**).

FIG. **33** is a circuit diagram illustrating a fifth exemplary LC oscillator **2305**, having a single-ended Colpitts configuration (or topology), which may be utilized in accordance with the teachings of the present invention. As illustrated, the apparatus **2300** comprises the third exemplary LC oscillator **2305**, having a single-ended Colpitts configuration (or topology), and portions of the frequency controller and frequency calibration modules previously discussed (single-ended versions of compensation modules **420** and **425**). The frequency controller and frequency calibration modules (**485**, **460**) are coupled in parallel to either capacitor **2310** across nodes A and B as illustrated, or to capacitor **2315** across nodes A' and B' as illustrated, or both (separately in parallel to capacitor **2310** across nodes A and B and to capacitor **2315** across nodes A' and B'). The output frequency f_0 is obtained between nodes $\mathbf{470}_C$ and $\mathbf{475}_c$, which are equivalent to the nodes **470** and **475** previously discussed, and also may be substituted as such for all references in the Figures and this specification.

The transistor **2325** may be coupled to a fixed or varying bias voltage or to another circuit node (not separately illustrated). In addition, a bias current is also provided, such as using the parameter-responsive current I(x) generator **515**, also previously discussed or, alternatively, another fixed or variable current source. The frequency controller modules (**480**, **485** with coefficient registers **455** and **495**) and frequency calibration modules (**460** with coefficient register **465**) also operate as previously discussed. In addition, the various reactances (inductor **2320**, capacitors **2310** and **2315**) may be implemented to be either fixed or variable, also as previously discussed. In exemplary embodiments, the resistance **2330** may also be fixed or varying.

FIG. **34** is a circuit diagram illustrating a sixth exemplary LC oscillator, having a differential, common base Colpitts configuration (or topology), which may be utilized in accordance with the teachings of the present invention. As illustrated the apparatus **2400** comprises the sixth exemplary LC oscillator **2405**, having a differential, common base Colpitts configuration (or topology), and the frequency controller and frequency calibration modules previously discussed in the double-balanced configuration of FIG. **4**. The output frequency f_0 is obtained between nodes $\mathbf{470}_D$ and $\mathbf{475}_D$, which are also equivalent to the nodes **470** and **475** previously discussed, and may be substituted as such for all references in the Figures and this specification.

The transistors **2425** and **2426** may be coupled to a fixed or varying bias voltage. While illustrated using n-MOS transistors, transistors **2425** and **2426** also provide an example of equivalent use of bipolar junction transistors in the present invention. In addition, one or more bias currents are also provided, such as using the parameter-responsive current I(x) generator **515**, also previously discussed or, alternatively, one or more other fixed or variable current sources. The frequency controller modules (**480**, **485** with coefficient registers **455**

and **495**) and frequency calibration modules (**460** with coefficient register **465**) are coupled in parallel to capacitor **2415** across nodes A and B as illustrated, or in parallel to capacitor **2410** across nodes A' and B' as illustrated, or in parallel to capacitor **2430** across nodes A" and B" as illustrated, or in any combination of these three configurations, and also operate as previously discussed. In addition, the various reactances (inductor **2420**, capacitors **2410**, **2415** and **2430**) may be implemented to be either fixed or variable, also as previously discussed.

FIG. **35** is a circuit diagram illustrating a seventh exemplary LC oscillator **2405**, having a differential, common collector Colpitts configuration (or topology), which may be utilized in accordance with the teachings of the present invention. As illustrated, the apparatus **2400** comprises the seventh exemplary LC oscillator **2405**, having a differential, common collector Colpitts configuration (or topology), and the frequency controller and frequency calibration modules previously discussed in the double-balanced configuration of FIG. **4**. The output frequency f_0 is obtained between nodes $\mathbf{470}_E$ and $\mathbf{475}_E$, which are also equivalent to the nodes **470** and **475** previously discussed, and may be substituted as such for all references in the Figures and this specification.

One or more bias currents are provided, such as using the parameter-responsive current I(x) generator **515**, also previously discussed or, alternatively, one or more other fixed or variable current sources. The frequency controller modules (**480**, **485** with coefficient registers **455** and **495**) and frequency calibration modules (**460** with coefficient register **465**) are coupled in parallel to capacitor **2515** across nodes A and B as illustrated, or in parallel to capacitor **2510** across nodes A' and B' as illustrated, or in parallel to capacitor **2530** across nodes A" and B" as illustrated, or in any combination of these three configurations, and also operate as previously discussed. In addition, the various reactances (inductor **2520**, capacitors **2510**, **2515** and **2530**) may be implemented to be either fixed or variable, also as previously discussed.

FIG. **36** is a circuit diagram illustrating an eighth exemplary LC oscillator **2605**, having a single-ended Hartley configuration (or topology), which may be utilized in accordance with the teachings of the present invention. As illustrated, the apparatus **2600** comprises the eighth exemplary LC oscillator **2605**, having a single-ended Hartley configuration (or topology), and portions of the frequency controller and frequency calibration modules previously discussed. Also because the oscillator **2605** is single-ended rather than differential, the frequency controller and frequency calibration modules (**485**, **460**) are coupled to one rail (node $\mathbf{470}_F$) only, rather than having the double-balanced configuration of FIG. **4**. As illustrated, the output frequency f_0 is obtained between nodes $\mathbf{470}_F$, and $\mathbf{475}_F$, which also are equivalent to the nodes **470** and **475** previously discussed, and may be substituted as such for all references in the Figures and this specification. (In addition, while the frequency controller and frequency calibration modules (**485**, **460**) are illustrated between node $\mathbf{470}_F$, and a ground potential, on node $\mathbf{475}_F$, the frequency controller and frequency calibration modules (**485**, **460**) are also considered to be in parallel across capacitor **2610** between node $\mathbf{470}_F$ and V_{DD}, as equivalent to an AC ground.)

The transistor **2625** may be coupled to a fixed or varying bias voltage. In addition, a bias current is also provided, such as using the parameter-responsive current I(x) generator **515**, also previously discussed or, alternatively, another fixed or variable current source. The frequency controller modules (**480**, **485** with coefficient registers **455** and **495**) and frequency calibration modules (**460** with coefficient register **465**) also operate as previously discussed. In addition, the various reactances (inductors **2615** and **2620**, capacitor **2610**) may be implemented to be either fixed or variable, also as previously discussed. In exemplary embodiments, the resistance **2630** may also be fixed or varying.

Comparing FIGS. **33** and **36**, it will be apparent that the Hartley configuration may be derived from the Colpitts configuration by switching the capacitors for inductors, and switching the inductors for capacitors. Referring again to FIGS. **34** and **35**, as a consequence, it will be apparent to those of skill in the art that differential Hartley oscillator configurations, both common base and common collector, may be formed by switching capacitors and inductors in the illustrated differential Colpitts configurations. Accordingly, differential Hartley oscillator configurations are not illustrated separately.

FIG. **37** is a circuit diagram illustrating a ninth exemplary LC oscillator, having a single-ended Pierce configuration (or topology), which may be utilized in accordance with the teachings of the present invention. As illustrated, the apparatus **2700** comprises the ninth exemplary LC oscillator **2705**, having a single-ended Pierce configuration (or topology), and portions of the frequency controller and frequency calibration modules previously discussed. Also because the oscillator **2705** is single-ended rather than differential, the frequency controller and frequency calibration modules (**485**, **460**) are coupled to one rail (node $\mathbf{470}_G$) only, rather than having the double-balanced configuration of FIG. **4**. As illustrated, the output frequency f_0 is obtained between nodes $\mathbf{470}_G$ and $\mathbf{475}_G$, which also are equivalent to the nodes **470** and **475** previously discussed, and may be substituted as such for all references in the Figures and this specification. In addition, the frequency controller and frequency calibration modules (**485**, **460**) are coupled in parallel to either capacitor **2710** across nodes A and B as illustrated, or to capacitor **2715** across nodes A' and B' as illustrated, or both (separately in parallel to capacitor **2710** across nodes A and B and to capacitor **2715** across nodes A' and B').

The oscillator **2705** includes an inductive load **2720** which may be, for example, an inductor or an inductor in parallel with a capacitor (presenting an overall inductance), and may be implemented to be either fixed or variable, also as previously discussed. The inductive load **2705** is in parallel with an inverter **2725** and resistance **2730**. The frequency controller modules (**480**, **485** with coefficient registers **455** and **495**) and frequency calibration modules (**460** with coefficient register **465**) also operate as previously discussed. In addition, the various capacitances **2710** and **2715** may be implemented to be either fixed or variable, also as previously discussed. In exemplary embodiments, the resistance **2730** may also be fixed or varying.

It should be noted that any of the various LC oscillator topologies may be implemented to provide a quadrature configuration (or topology), which may be utilized with the frequency compensation (for temperature, process variation, and other parameter variation) in accordance with the teachings of the present invention. For example, two LC oscillators may be cross-coupled with each other (and appropriately configured with the frequency controller modules (**480**, **485** with coefficient registers **455** and **495**) and frequency calibration modules (**460** with coefficient register **465**) to provide a plurality of first reference signals having 90° phase relationships (at 0°, 90°, 180° and/or 270°).

FIG. **38** is a circuit diagram illustrating an exemplary active inductor **2910** configuration, which may be utilized in accordance with the teachings of the present invention. While the active inductor **2910** is illustrated using bipolar junction transistors, an equivalent circuit may be obtained using any type

of CMOS transistors. An active inductor **2910** may be utilized for any of the inductors or inductive loads of any of the LC oscillators described herein or their equivalents, and may provide a savings in IC area. The illustrated active inductor **2910** would generally be coupled to the other portions of an oscillator at node D. A bias current is also provided, such as using the parameter-responsive current I(x) generator **515**, also previously discussed or, alternatively, another fixed or variable current source. In addition, the active inductor **2910** is illustrated as an example and without limitation—other active inductor circuits may also be utilized equivalently, including with other types of transistors and circuit configurations.

Those of skill in the art will recognized that innumerable variations are available for the various exemplary LC oscillator embodiments illustrated above. For example, the various amplifiers may be implemented in a wide variety of ways, such as with p channel transistors only, n channel transistors only, or a combination of both p and n channel transistors as illustrated. In addition, the various amplifiers and current mirrors may have various circuit locations and configurations with respect to the various resonators. Singular or multiple inductor or capacitor variations may be utilized equivalently. The various topologies may be symmetrical or asymmetrical, complementary or non-complementary, or cross-coupled or non-cross-coupled, for example. All such variations are considered equivalent and within the scope of the present invention.

Referring again to FIG. **21**, the frequency controller **215**, **349**, **1415** of the present invention may comprise one or more of the following components: (1) a transconductance modulator **1410** (e.g. **410**, **415** and the embodiments illustrated in FIGS. **6-8**), which in the exemplary embodiments, may also include or be coupled to sustaining amplifier **305**; (2) a variable parameter modulator **1425**, to modulate the resonant frequency f_0 in response to any selected parameter, such as temperature, fabrication process variation, voltage variation, or frequency, such as the various controlled capacitance modules **485**, **635**, **1505** or controlled reactance modules **1305**, **1805**; (3) a process (or other parameter) modulator or compensator **1430**, such as process variation compensator **425**, **760**, **860**, or controlled reactance modules **1305**, **1805**; (4) a voltage variation compensator **380**, **1455**; and/or (5) an age (time) variation compensator (or modulator) **365**, **1460**. It will be observed by those of skill in the art that the various divisions between transconductance modulator **1410**, variable parameter modulator **1425**, or process (or other parameter) modulator or compensator **1430** or the other compensators and modulators are arbitrary and do not limit the scope of the present invention, as each may be made responsive to any of the parameters discussed above, and each may be utilized for any of the purposes discussed above (e.g., the variable parameter modulator **1425** may be utilized to compensate for fabrication process variations, etc., rather than temperature variations, for example). In addition, depending upon the selected implementation, one or more coefficient registers **1435** (e.g., 455, 465, 495) may be utilized to store any of the pluralities of coefficients discussed above. In alternative embodiments, such coefficients may not be needed, with switching voltages or currents applied directly, either statically or dynamically, as control signals.

Also in the exemplary embodiments, these various components may include a sensor **1440**, **1815** (e.g., yI(x) (or I(T)) generator **415**, **515**), or such as sensor may be provided as a separate component, such as a current source coupled to a diode as discussed above. Also, depending on the selected embodiment, and A/D converter **1445** and control logic **1450**, **1810**, to provide the selected frequency control.

In summary, the exemplary embodiments of the present invention provide an apparatus for frequency control of a resonator, with the resonator adapted to provide a first signal having a resonant frequency. The apparatus comprises a sensor (**1440**, **1815**) adapted to provide a second signal, such as a control voltage, in response to at least one parameter of a plurality of parameters; and a frequency controller (**215**, **1415**) coupled to the sensor and couplable to the resonator, with the frequency controller adapted to modify the resonant frequency in response to the second signal. The plurality of parameters are variable and comprise at least one of the following parameters: temperature, fabrication process, voltage, frequency, and age.

In the exemplary embodiments, the frequency controller is further adapted to modify a reactance or impedance element coupled to the resonator in response to the second signal, such as modifying a total capacitance of the resonator in response to the second signal (FIG. **9**), coupling to the resonator or decoupling from the resonator a fixed or variable capacitance (**635**), modifying the effective reactance of a varactor coupled to the resonator by switching the varactor to a selected control voltage, or equivalently, modifying an inductance of the resonator in response to the second signal, such as by coupling to the resonator or decoupling from the resonator a fixed or variable inductance, or modifying a resistance (or other impedance) of the resonator in response to the second signal, such as by coupling to the resonator or decoupling from the resonator a resistance.

In the exemplary embodiments, the frequency controller may further comprise: a coefficient register adapted to store a first plurality of coefficients; and a first array (**635**) having a plurality of switchable capacitive modules coupled to the coefficient register and couplable to the resonator, each switchable capacitive module having a fixed capacitance **615** and a variable capacitance **620**, each switchable capacitive module responsive to a corresponding coefficient of the first plurality of coefficients to switch between the fixed capacitance and the variable capacitance and to switch each variable capacitance to a control voltage. The plurality of switchable capacitive modules may be binary-weighted. The frequency controller may further comprise a second array **650** having a plurality of switchable resistive modules coupled to the coefficient register and further having a capacitive module, the capacitive module and the plurality of switchable resistive modules further coupled to a node **625** to provide the control voltage, with each switchable resistive module responsive to a corresponding coefficient of a second plurality of coefficients stored in the coefficient register to switch the switchable resistive module to the control voltage node **625**. In selected embodiments, the sensor further comprises a current source **655** responsive to temperature, wherein the current source is coupled through a current mirror **670** to the second array to generate the control voltage across at least one switchable resistive module of the plurality of switchable resistive modules. Also in selected embodiments, the current source has at least one CTAT, PTAT, or $PTAT^2$ configuration (FIGS. **7A-7D**). In addition, each switchable resistive module of the plurality of switchable resistive modules has a different temperature response for a selected current.

In other exemplary embodiments, the sensor is a temperature sensor and varies the second signal in response to temperature variation. The selected embodiments may also include an analog-to-digital converter **1445** coupled to the temperature sensor to provide a digital output signal in

response to the second signal, and a control logic block **1450** to convert the digital output signal to the first plurality of coefficients.

In other exemplary embodiments, the frequency controller further comprises a process variation compensator **320**, **425**, **760** or **860**, the process variation compensator couplable to the resonator and adapted to modify the resonant frequency in response to a fabrication process parameter of the plurality of parameters. The process variation compensator may further comprise a coefficient register adapted to store a plurality of coefficients; and an array **760** having a plurality of switchable capacitive modules coupled to the coefficient register and to the resonator, each switchable capacitive module having a first fixed capacitance **750** and a second fixed capacitance **720**, each switchable capacitive module responsive to a corresponding coefficient of the plurality of coefficients to switch between the first fixed capacitance and the second fixed capacitance. In other exemplary embodiments, the process variation compensator may further comprise a coefficient register adapted to store a plurality of coefficients; and an array **860** having a plurality of binary-weighted switchable variable capacitive modules **865** coupled to the coefficient register and to the resonator, each switchable variable capacitive module responsive to a corresponding coefficient of the plurality of coefficients to switch between a first voltage and a second voltage.

In other exemplary embodiments, a frequency controller further comprises a coefficient register adapted to store a first plurality of coefficients; and a first array **1500** having a plurality of switchable, binary-weighted capacitive modules **1505** coupled to the coefficient register and couplable to the resonator, each switchable capacitive module having a variable capacitance **1515**, each switchable capacitive module responsive to a corresponding coefficient of the first plurality of coefficients to switch (**1520**) the variable capacitance to a selected control voltage of a plurality of control voltages. The sensor may comprises a current source responsive to temperature, and the frequency controller may also include a second array **1600** having a plurality of resistive modules **1605** coupled through a current mirror (**670**, **510**, **520**) to the current source (**655**), the plurality of resistive modules adapted to provide the plurality of control voltages, and wherein each resistive module of the plurality of resistive modules has a different response to temperature and is adapted to provide a corresponding control voltage, of the plurality of control voltages, in response to a current from the current source.

In other exemplary embodiments, an apparatus for frequency control of a resonator comprises a coefficient register adapted to store a first plurality of coefficients; and a first array (**1300**, **1800**) having a plurality of switchable reactance modules (**1305**, **1805**) coupled to the coefficient register and to the resonator, each switchable reactance module responsive to a corresponding coefficient of the first plurality of coefficients to switch a corresponding reactance to the resonator to modify the resonant frequency. The corresponding reactance may be a fixed or variable inductance, a fixed or variable capacitance, or any combination thereof. The corresponding reactance may be switched between the resonator and a control voltage or a ground potential, and the control voltage may be determined by a current source responsive to temperature. For example, the corresponding reactance is variable and is switched between the resonator and a selected control voltage of a plurality of control voltages. In selected embodiments, the first plurality of coefficients are calibrated or are determined by a sensor responsive to at least one parameter of a plurality of variable parameters, such as temperature, fabrication process, voltage, and frequency.

In the exemplary embodiments, the plurality of switchable reactance modules may further comprise a plurality (**635**) of binary-weighted switchable capacitive modules **640**, each switchable capacitive module having a fixed capacitance and a variable capacitance, each switchable capacitive module responsive to a corresponding coefficient of the first plurality of coefficients to switch between the fixed capacitance and the variable capacitance and to switch each variable capacitance to a control voltage. The apparatus may also include a current source **655** responsive to temperature; and a second array having a plurality of switchable resistive modules **675** coupled to the coefficient register and selectively couplable to the current source, the second array further having a capacitive module **680**, the capacitive module and the plurality of switchable resistive modules further coupled to a node **625** to provide the control voltage, each switchable resistive module responsive to a corresponding coefficient of a second plurality of coefficients stored in the coefficient register to switch the switchable resistive module to the control voltage node, and wherein each switchable resistive module of the plurality of switchable resistive modules has a different temperature response for a selected current from the current source.

In other exemplary embodiments, the plurality of switchable reactance modules further comprise a plurality **1500** of binary-weighted switchable capacitive modules **1505**, each switchable capacitive module having a variable capacitance **1515**, each switchable capacitive module responsive to a corresponding coefficient of the first plurality of coefficients to switch (**1520**) the variable capacitance to a selected control voltage of a plurality of control voltages. The apparatus may also include a current source **655** responsive to temperature; and a second array having a plurality of resistive modules **1605** coupled through a current mirror (**670**, **510**, **520**) to the current source, the plurality of resistive modules adapted to provide the plurality of control voltages, and wherein each resistive module of the plurality of resistive modules has a different response to temperature and is adapted to provide a corresponding control voltage, of the plurality of control voltages, in response to a current from the current source.

In other exemplary embodiments, the plurality of switchable reactance modules may further comprise a plurality **760** of binary-weighted switchable capacitive modules coupled to the coefficient register and to the resonator, each switchable capacitive module having a first fixed capacitance **750** and a second fixed capacitance **720**, each switchable capacitive module responsive to a corresponding coefficient of the plurality of coefficients to switch between the first fixed capacitance and the second fixed capacitance. In other exemplary embodiments, the plurality of switchable reactance modules may further comprise a plurality **860** of binary-weighted switchable variable capacitive modules **865** coupled to the coefficient register and to the resonator, each switchable variable capacitive module responsive to a corresponding coefficient of the plurality of coefficients to switch between a first voltage and a second voltage.

In the exemplary embodiments, an apparatus in accordance with the teachings of the invention comprises a resonator **310**, **405** adapted to provide a first signal having a resonant frequency; and a temperature compensator **315** coupled to the resonator and adapted to modify the resonant frequency in response to temperature variation. The resonator is at least one of the following resonators: an inductor (L) and a capacitor (C) configured to form an LC-tank resonator; a ceramic resonator, a mechanical resonator, a microelectromechanical resonator, or a film bulk acoustic resonator. The apparatus may further comprise a negative transconductance amplifier **410** coupled to the resonator and to the temperature compen-

sator, wherein the temperature compensator is further adapted to modify a current through the negative transconductance amplifier in response to temperature variation. The temperature compensator may further comprises a current source **415**, **515**, **655** responsive to temperature variation.

In other exemplary embodiments, the temperature compensator further comprises: a current source **415**, **515**, **655** adapted to provide a current responsive to temperature variation; a coefficient register adapted to store a first plurality of coefficients; a plurality of resistive modules **675**, **1605** coupled to the resonator and the current source, at least one resistive module of the plurality of resistive modules adapted to provide a control voltage or a plurality of control voltages; and a plurality of switchable reactance modules (**1305**, **1805**, **635**, **1505**), coupled to the resonator and to the current source and selectively couplable to at least one resistive module of the plurality of resistive modules.

In other exemplary embodiments, the invention provides a frequency controller for frequency control of a resonator, comprising: a coefficient register adapted to store a first plurality of coefficients and a second plurality of coefficients; a current source **415**, **515**, **655** adapted to provide a current corresponding to a temperature; a first array having a plurality of switchable resistive modules **675**, **1605** coupled to the coefficient register and further having a capacitive module, the first array further coupled through a current mirror to the current source to create at least one control voltage across at least one switchable resistive module of the plurality of switchable resistive modules, each switchable resistive module responsive to a corresponding coefficient of the second plurality of coefficients to switch the switchable resistive module to provide the control voltage to a control voltage node; and a second array having a plurality of binary-weighted switchable capacitive modules **640** coupled to the coefficient register and to the resonator, each switchable capacitive module having a fixed capacitance and a variable capacitance, each switchable capacitive module responsive to a corresponding coefficient of the first plurality of coefficients to switch between the fixed capacitance and the variable capacitance and to switch each variable capacitance to the control voltage node.

Referring again to FIGS. **3** and **4**, the clock generator and/or timing/frequency reference (**100**, **200**, or **300**) may also include a frequency calibration module (**325** or **430**). This frequency calibration module is the subject of a separate patent application, but its high-level functionality is described briefly below. FIG. **13** is a high-level block diagram illustrating an exemplary frequency calibration module **900** (which may be utilized as module **325** or **430**) in accordance with the teachings of the present invention. The frequency calibration module **900** includes a digital frequency divider **910**, a counter-based frequency detector **915**, a digital pulse counter **905**, and a calibration register **930** (which also may be utilized as register **465**). Using a test IC, the output signal from the clock generator (**100**, **200** or **300**) is frequency divided (**910**) and compared with a known reference frequency **920** in frequency detector **915**. Depending upon whether the clock generator (**100**, **200** or **300**) is fast or slow with respect to the reference, down or up pulses are provided to the pulse counter **905**. Based upon those results, the third plurality of switching coefficients r_0 though $r_{(y-1)}$ is determined, and the clock generator (**100**, **200** or **300**) is calibrated to a selected reference frequency. Again, individual ICs may also be calibrated and tested separately.

Referring again to FIGS. **2**, **3** and **4**, it will be appreciated by those of skill in the art that a highly accurate over PVT, low jitter, free-running and self-referenced oscillator has been described, providing a differential, substantially sinusoidal signal having a selectable and tunable resonant frequency, f_0, available at nodes **470** and **475**. For many applications, this signal is sufficient, and may be utilized directly (and may be output on bus **125** or **135** of FIG. **1**, on line **250** of FIG. **2**, or on line **350** of FIG. **3**, or between the rails or lines **470** and **475** of FIG. **4**). For example, this signal may be utilized as a timing or frequency reference. In accordance with the present invention, additional applications are available, including clock generation (substantially square wave), frequency division, low-latency frequency switching, and mode selection, as described below.

FIG. **14** is a block diagram illustrating an exemplary first frequency divider and square wave generator **1000**, and an exemplary asynchronous frequency selector **1050**, with exemplary glitch suppression module **1080** in accordance with the teachings of the present invention. As indicated above, first frequency divider and square wave generator **1000** may be included in or comprise modules **220** and/or **330**, and frequency selector **1050** (with or without glitch suppression module **1080**) may be included in or comprise modules **205** and/or **335**.

Referring to FIG. **14**, the output signal from the oscillator, namely, a differential and substantially sinusoidal signal having a frequency f_0, such as output on line **250** of FIG. **2**, or line **350** of FIG. **3**, or between the rails or lines **470** and **475** of FIG. **4**, is input into frequency divider and square wave generator **1000**. The frequency of this substantially sinusoidal signal is divided by any one or more arbitrary values "N" into "m" different frequencies (including f_0, where appropriate), and converted to substantially square wave signals, resulting in a plurality of substantially square wave signals having m+1 different available frequencies, output on lines or bus **1020** as frequencies f_0, f_1, f_2, through f_m. Any of these substantially square wave signals having m+1 different available frequencies are selectable asynchronously through exemplary asynchronous frequency selector **1050** which, as illustrated, may be embodied as a multiplexer. The selection of any of these substantially square wave signals having m+1 different available frequencies may be accomplished through the plurality of selection lines (S_m through S_0) **1055**, providing a substantially square wave signal having the selected frequency, output on line **1060**.

As part of asynchronous frequency selection, glitch suppression is also provided by glitch suppression module **1080**, which may be embodied in a plurality of ways, including through the use of one or more exemplary D flip-flops ("DFFs") illustrated in FIG. **14**. A glitch could occur in an asynchronous frequency transition in which either a low state or a high state is not maintained for a sufficient period of time and may cause metastability in circuitry which is driven by the output clock signal. For example, an asynchronous frequency transition could result in a low state at a first frequency transitioning into a high state at a second frequency, at a point where the high state is about to transition back to a low state at the second frequency, resulting in a voltage spike or glitch. To avoid potential glitches from being provided as part of an output clock signal, the selected substantially square wave signal (having the selected frequency) is provided on line **1060** to a first DFF **1065** which provides a holding state; if a glitch should occur, it will be held until a clock edge triggering the DFF. To avoid the glitch occurring at the clock edge, the DFFs may be clocked at less than the maximum available frequency, or one or more additional DFFs (such as DFF **1070**) may be employed, as during the wait for another clock signal, the Q output from the DFF **1065** will have stabilized to either a first state (high or low) or a second state (low or high),

such as to either the power or ground rail. It has been shown by the inventors that 2 DFFs are sufficient, with additional DFFs potentially being added as may be desired, but with additional DFFs causing increased switching latency. While illustrated utilizing exemplary DFFs, other flip-flops or counters may be utilized, and those of skill in the art will recognize myriad other equivalent implementations which will achieve this result, and all such variations are within the scope of the invention.

Such exemplary low latency frequency switching in accordance with the teachings of the present invention is illustrated in FIG. **15**. FIG. **15** is also illustrative of "substantially" square waves of the present invention, which are typical of actual square waves utilized in various technologies, exhibiting reasonable variation, undershoots and overshoots at their respective high and low states (and not the perfect "flatness" of textbook examples). FIG. **15**, part A, illustrates asynchronous glitch-free switching from 1 MHz to 33 MHz, while part B illustrates measured glitch-free switching from 4 MHz to 8 MHz, then to 16 MHz, and then to 33 MHz.

Referring again to FIG. **14**, the frequency divider and square wave generator **1000** may be implemented in innumerable ways, such as differential or single-ended, with the illustrated divider being merely exemplary. As the output from the oscillator illustrated in FIG. **4** is differential (across lines or rails **470** and **475**), the first divider **1005** is also differential and provides complementary outputs, to present a substantially constant load to the oscillator and to maintain phase alignment, and is fast, to support high frequencies such as in the GHz range. In addition, it may be necessary or advisable to reject any relaxation mode oscillation of the first divider **1005**. The second divider **1010** may also be differential and provide any arbitrary frequency division (divide by "M"), such as dividing by an integer, a multiple of two, a rational number, or any other amount or number, etc. Topologies or configuration for such dividers are known in the art, and any such divider may be utilized. Such dividers, for example and without limitation, may be a sequence (multiple stages) of counters or flip-flops **1075**, such as those flip-flops illustrated in FIG. **16**, as a second, differential frequency divider **1074**, which provide frequency division in powers or multiples of 2, with the output of each stage providing a different frequency and further providing a clock signal for the next stage and also fed back to its own input, as illustrated. As illustrated, a plurality of frequencies are then available for output on lines or bus **1020**, such as $f_0/2$, $f_0/4$, and so on, through $f_0/2^N$. In addition, as illustrated, buffers **1085** may also be utilized, from the oscillator to the first divider **1005**, to provide sufficient voltage to drive the first divider **1005**, and also between second divider **1010** stages, to isolate state-dependent load variation which could also affect signal rise and fall times.

It should also be noted that the use of the various flip-flops has also provided a substantially square wave, as any substantially sinusoidal signal has been provided to clock a flip flop, whose output is then pulled to a high or low voltage. Other square wave generators may also be utilized, as known or becomes known in the art. In the illustrated embodiments, to maintain phase alignment, differential signals are maintained through the last division. Following the last frequency division, the plurality of signals (each having a different frequency) are then squared (in module **1015**) to provide substantially an evenly divided (e.g., 50:50) duty cycle, such that the time in which the signal is in a first (high) state is substantially equal to the time in which the signal is in a second (low) state.

FIG. **17** is a block diagram illustrating an exemplary mode selection module in accordance with the teachings of the present invention. There are circumstances in which a highly-accurate, high performance reference, such as a clock generator (**100**, **200** or **300**) of the invention, is unnecessary, such as in a low power, standby mode. In these circumstances, in accordance with the invention, either no clock output is provided, or a low power, reduced performance clock **1105** output is provided. For example, at comparatively low frequencies, a low performance ring oscillator may provide suitable performance with low power consumption. As illustrated in FIG. **17**, for these conditions, the output of the low power oscillator **1105** may be selected (through multiplexer **1100**), and provided as a clock output to other circuitry. At higher frequencies, however, such low performance oscillators consume considerably more power, typically significantly more than the oscillator of the present invention. There is typically a "break-even" point as a function of frequency, after which the clock generator (**100**, **200** or **300**) provides both higher performance and lower power consumption, and may be selected (through multiplexer **1100**), and provided as a clock output to other circuitry. As a consequence, the clock generator (**100**, **200** or **300**) may also be utilized to provide a low power mode.

In addition, using mode selector **1110**, other modes may be selected, such as a no power mode, rather than merely a low-frequency or sleep mode, as the clock generator (**100**, **200** or **300**) may be restarted comparatively rapidly, or a pulsed mode, in which the clock generator (**100**, **200** or **300**) is repeatedly stopped and restarted, periodically or non-periodically, in bursts or intervals. Various reference modes are discussed below.

In sharp contrast to the prior art, this pulsed clocking using the clock generator and/or timing/frequency reference (**100**, **200** or **300**) of the present invention provides power savings or conservation. While more power may be consumed during a given burst, as the clock has a comparatively high frequency, more instructions are processed in that interval, followed by no or limited power dissipation during the non-pulse or off interval, resulting in higher MIPS/mW compared to a continuously running clock. In contrast, due to the comparatively long start-up time and locking of prior art clocks, such pulsed clocking results in more power consumption and less efficiency in the prior art.

FIG. **18** is a block diagram illustrating an exemplary synchronization module **1200** for a second oscillator in accordance with the teachings of the present invention. As mentioned above, the clock generator and/or timing/frequency reference (**100**, **200** or **300**) may provide a reference mode to synchronize other oscillators or clocks, which may or may not be low power, such as second oscillator **1210** (e.g., ring, relaxation, or phase shift oscillators). An output signal from the clock generator and/or timing/frequency reference (**100**, **200** or **300**) is further frequency divided as needed to form a plurality of available reference frequencies, with a reference frequency selected from this plurality of frequencies. This may be accomplished using the modules discussed above, such as by using the existing frequency dividers (**220**, **330**, **1000**, for example), and then providing the reference signal from the frequency selector **1050** (or **205** or **335**). For example, referring to FIG. **3**, mode selector **345** may select a reference mode and provide the output reference signal from frequency selector **335** to a second oscillator (with synchronization module) **375**. A synchronization module, such as PLL or DLL **1205**, is then utilized to synchronize the output signal from the second oscillator **1210** to the reference signal provided by clock generator and/or timing/frequency reference (**100**, **200** or **300**). In addition to a mode of continuous synchronization, a pulsed-synchronization may also be pro-

vided, in which the clock generator and/or timing/frequency reference (**100**, **200** or **300**) provides a pulsed output, and synchronization occurs during the interval of these pulses, as a synchronization interval.

FIG. **19** is a flow diagram illustrating an exemplary method in accordance with the teachings of the present invention, and provides a useful summary. The method begins with start step **1220**, such as through clock generator and/or timing/frequency reference (**100**, **200** or **300**) start-up. It should be noted that while illustrated in FIG. **19** as consecutive steps, these steps may occur in any order, and generally may occur concurrently as the clock generator and/or timing/frequency reference (**100**, **200** or **300**) operates. Referring to FIG. **19**, a resonant signal having a resonant frequency is generated, step **1225**, such as through LC tank **405** or resonator **310**. The resonant frequency is adjusted in response to temperature, step **1230**, such as through a temperature compensator **315**, which adjusts current and frequency. The resonant frequency is adjusted in response to fabrication process variation, step **1235**, such as through process variation compensator **320**. As indicated above, step **1235** may be performed as a first calibration step, followed by the temperature adjustment of step **1230**. The resonant signal having the resonant frequency is divided into a plurality of second signals having a corresponding plurality of frequencies, in which the plurality of frequencies are substantially equal to or lower than the resonant frequency, step **1240**, such as through frequency divider **330** or **1000**). An output signal is selected from the plurality of second signals, step **1245**, such as through frequency selector **335** or **1050**, for example. Depending upon the selected embodiment or mode, the selected output signal may be provided directly, for example, as a reference signal.

In other embodiments, such as when the output signal is a differential rather than single-ended signal, and when the resonant signal is a substantially sinusoidal signal, the method continues with converting the differential, substantially sinusoidal signal to a single-ended, substantially square wave signal having a substantially equal high and low duty cycle, as needed, step **1250**, such as to generate a clock output signal using modules **330** or **1000**, for example. An operating mode is also selected from a plurality of operating modes, step **1255**, where the plurality of operating modes can be selected from a group comprising a clock mode, a timing and frequency reference mode, a power conservation mode, and a pulsed mode, for example, such as using mode selector **225** or **345**. When a reference mode is selected in step **1255**, in step **1260**, the method proceeds to step **1265**, to synchronize a third signal (e.g., from a second oscillator) in response to the output signal, such as illustrated in FIG. **18**. Following steps **1260** or **1265**, the method may end or repeat (continue) (such as with the clock generator and/or timing/frequency reference (**100**, **200** or **300**) running continuously), return step **1270**.

FIG. **39** is a block diagram illustrating a second exemplary system **1195** embodiment in accordance with the teachings of the present invention. As illustrated, the second exemplary system **1195** comprises a clock generator (timing/frequency reference) (**100**, **200**, **300**), as discussed above, and second circuitry **180**, of any type or kind, for any function, application, or purpose, such as a "processor" **1275** as illustrated and as defined below. The second circuitry **180** may also further comprise a memory **1280**, an interface **1285** for input and output ("I/O"), and other circuitry components for any selected application or function. The second exemplary system **1195** is typically embodied as a single integrated circuit, providing one or more first reference signals, as one or more system clocks or references, which is integrated with other components and which does not require any external reference or clock, such as a crystal oscillator reference. For example, the clock/reference (**100**, **200**, **300**) is free-running and is not and does not lock to any reference clock or signal, and instead provides a reference clock or signal to other, second circuitry **180**.

The second exemplary system **1195** also may be embodied as a plurality of integrated circuits, coupled through bonding wires within the same IC package. For example, the clock generator (timing/frequency reference) (**100**, **200**, **300**) may be embodied on a first IC, and the second circuitry **180** on a second IC, which are coupled to each other through one or more bonding wires, for the first IC (clock) to provide one or more first reference signals, as one or more system clocks or references, to the second IC (second circuitry **180**), providing a clock or reference as part of a single, packaged component which does not require any external reference or clock, such as a crystal oscillator reference.

As illustrated in FIG. **39**, in addition to the clock generator (timing/frequency reference) (**100**, **200**, **300**), the second exemplary system **1195** further comprises one or more types of second circuitry, such as one or more processors **1275**, and potentially also an I/O interface (or other I/O means) **1285** and a memory **1280**. Each of these components receives the one or more first reference signals, typically for use as one or more clocking signals. In the second exemplary system **1195**, the I/O interface **1285** may be implemented as known or may become known in the art, to provide data communication between, first, the processor **1275**, memory **1280**, and second, any channel, busses, input and output devices, mechanisms and media discussed herein (not separately illustrated), including wireless, optical or wireline, using any applicable standard, technology, or media, without limitation. For example, when the second exemplary system **1195** is utilized as a computer processor, the I/O interface **1285** is adapted to provide data communication to and from one or more busses, such as a PCI bus, a PCI-Express bus, a universal serial bus (USB1 or USB2), and so on. In addition, the I/O interface **1285** may provide an interface to any CD or disk drives, or an interface to a communication channel for communication via a network, to provide communication with any form of media or communication device, such as providing an Ethernet port, for example. Also for example, the I/O interface **1285** may provide all signaling and physical interface functions, such as impedance matching, data input and data output between external communication lines or channels (e.g., Ethernet, T1 or ISDN lines) coupled to a network, and internal server or computer communication busses (e.g., one of the various PCI or USB busses), for example and without limitation. In addition, depending upon the selected embodiment, the I/O interface **1285** (or the processor **1275**) may also be utilized to provide data link layer and media access control functionality.

The memory **1280** may be embodied in any number of forms, including within any computer or other machine-readable data storage medium, memory device or other storage or communication device for storage or communication of information such as computer-readable instructions, data structures, program modules or other data, currently known or which becomes available in the future, including, but not limited to, a magnetic hard drive, an optical drive, a magnetic disk or tape drive, a hard disk drive, other machine-readable storage or memory media such as a floppy disk, a CDROM, a CD-RW, digital versatile disk (DVD) or other optical memory, a memory integrated circuit ("IC"), or memory portion of an integrated circuit (such as the resident memory within a processor IC), whether volatile or non-volatile, whether removable or non-removable, including without

limitation RAM, FLASH, DRAM, SDRAM, SRAM, MRAM, FRAM, ROM, EPROM or E^2PROM, or any other type of memory, storage medium, or data storage apparatus or circuit, which is known or which becomes known, depending upon the selected embodiment. In addition, such computer readable media includes any form of communication media which embodies computer readable instructions, data structures, program modules or other data in a data signal or modulated signal, such as an electromagnetic or optical carrier wave or other transport mechanism, including any information delivery media, which may encode data or other information in a signal, wired or wirelessly, including electromagnetic, optical, acoustic, RF or infrared signals, and so on.

The second exemplary system **1195** further comprises one or more types of processing circuitry, such as one or more processors **1275**, which may be single- or multiple-core, may be general purpose or specialized, and which may be adapted to perform any type of functionality. As the term "processor" is used and defined herein, a processor **1275** may be any type or kind of circuitry, adapted to perform a function, application, or other purpose, of any type or kind, and may include use of a single integrated circuit ("IC"), or may include use of a plurality of integrated circuits or other components connected, arranged or grouped together, such as microprocessors, digital signal processors ("DSPs"), controllers or microcontrollers, parallel processors, multiple core processors, custom ICs, application specific integrated circuits ("ASICs"), field programmable gate arrays ("FPGAs"), adaptive computing ICs, associated memory (such as RAM, DRAM and ROM), and other ICs and components. As a consequence, as used herein, the term processor should be understood to equivalently mean and include a single IC, or arrangement of custom ICs, ASICs, processors, microprocessors, controllers, FPGAs, adaptive computing ICs, or some other grouping of integrated circuits which perform(s) any applicable function(s), with associated memory, such as microprocessor memory or additional RAM, DRAM, SDRAM, SRAM, MRAM, ROM, FLASH, EPROM or E^2PROM. A processor (such as processor **1275**), with its associated memory, may be adapted or configured (via programming, microcode, FPGA interconnection, or hard-wiring) to perform any functionality, as discussed below, associated with any selected application of the second exemplary system **1195** (or third, fourth or fifth exemplary systems discussed below). For example, any function or methodology may be programmed and stored, in a processor **1275** with its associated memory (and/or memory **1280**) and other equivalent components, as a set of program instructions or other code (or equivalent configuration or other program) for subsequent execution when the processor is operative (i.e., powered on and functioning). Equivalently, when the processor **1275** may implemented in whole or part as FPGAs, custom ICs and/or ASICs, the FPGAs, custom ICs or ASICs also may be designed, configured and/or hard-wired to implement any selected functionality or methodology. For example, the processor **1275** may implemented as an arrangement of microprocessors, DSPs and/or ASICs, collectively referred to as a "processor", which are respectively programmed, designed, adapted or configured to implement a selected function, such as a communication function, a data processing function, etc.

The processor **1275** may be implemented as, for example and without limitation, a microprocessor; a digital signal processor; a controller; a microcontroller; a universal serial bus (USB) controller; a Peripheral Component Interconnect (PCI) controller; a Peripheral Component Interconnect Express (PCI-e) controller; a Firewire controller; an AT Attachment (ATA) interface controller, an Integrated Drive Electronics (IDE) controller; a Small Computer Systems Interface (SCSI) controller. In other embodiments, the processor **1275** may be implemented to provide other forms of control functionality, such as a television controller; a local area network (LAN) or Ethernet controller; a video controller; an audio controller; a modem processor or controller; a cable modem controller or processor; a multimedia controller; an MPEG controller, e.g., MPEG-1, (Video CD, MP3), MPEG-2 (digital television, DVD), MPEG-4 (multimedia for fixed and mobile web applications), MPEG-7 (description and search of audio and visual content), MPEG-21 (multimedia framework). In other embodiments, when the clock/reference has been implemented to provide significant and stable frequency accuracy, the processor **1275** may be implemented to provide communications functionality, such as one or more communication controllers for mobile communication (a mobile communication controller; an IEEE 802.11 controller; a GSM controller; a GPRS controller; a PCS controller; an AMPS controller; a CDMA controller; a WCDMA controller; a spread spectrum controller; a wireless LAN controller; an IEEE 802.11 controller in its various forms, etc.), or non-mobile communication (e.g., a DSL controller; a T1 controller; a ISDN controller; or other multimedia or other communication controller.

Continuing with the above-example, selected frequencies may include 12, 30, 48 or 480 MHz for a USB controller (USB1 or USB2); 33 or 66 MHz for a PCI controller, or 6 MHz for a PCI-e controller, a Firewire controller, an ATA controller, or a SCSI controller; 10.7 MHz for a television controller; 50 MHz for a local area network (LAN) or Ethernet controller; 27 MHz or 54 MHz for a video controller; 24.576 MHz for an audio controller; 56.448 MHz for a modem processor; and other frequencies suitable for any of the various MPEG controllers or communications controllers mentioned above. Other frequencies are also selected based upon the application, such as appropriate GHz frequencies when the processor **1275** is utilized in a computer, for example.

The various frequencies, such as those illustrated above, may be determined in any of a plurality of ways, whether provided directly by the clock generator (timing/frequency reference) (**100**, **200**, **300**) as first frequency f_0 of the first reference signal, or as one or more second frequencies of one or more second reference signals (via the one or more dividers (**1000**, **1010**, **1074**, **1218**, **1219**) or locking circuits **1204** and other components discussed below). For example, the various frequencies may be determined as part of design and fabrication, or post-fabrication (such as through calibration and programming), or both. More particularly, the frequency selection may occur as part of design and fabrication, such as through selection of the number and size of inductors and capacitors utilized in the LC oscillator of the clock/reference (**100**, **200**, **300**). For example, the size(s) and/or shape(s) of the one or more inductors (e.g., **445**) may be selected through a suitable metal layer mask. As discussed above, frequency selection also may occur post-fabrication, through the use of the various calibration and control coefficients or signals discussed above. In addition, as discussed below, frequency selection may be performed through the configuration of the one or more locking circuits **1204** or dividers, such as through selection of the divide ratio(s) through programmable counters, which may be as part of the design and fabrication of the IC, or may be programmed post-fabrication, also through use of calibration and control coefficients or signals, or by switching dividers in or out of the divide chain.

In addition to the illustrated one or more processors **1275**, I/O interface **1285**, and memory **1280**, those of skill in the art will appreciate that the various exemplary systems may also include additional or different components, and generally will vary with the selected application. For example, different application may require additional circuits, such as different physical layer implementations in addition to that described for I/O interface **1285**, for example.

FIG. **40** is a block diagram illustrating a third exemplary system **1201** embodiment in accordance with the teachings of the present invention. As illustrated in FIG. **40**, the first reference signal having a first frequency (f_0) is provided either directly to a processor **1275** (as an example of second circuitry **180**) or to additional second circuitry illustrated as inverter **1196**, dividers (**1000**, **1074**, **1218** and/or **1219** (discussed below)), locking circuits **1204** (illustrated as locking circuit $\mathbf{1204}_1$, locking circuit $\mathbf{1204}_2$ through locking circuit $\mathbf{1204}_N$), and combinations or permutations of such dividers, locking circuits, etc. This additional second circuitry is adapted to receive the first reference signal having a first frequency (f_0) and to provide one or more corresponding second reference signals at selected frequencies, illustrated as frequencies f_1, f_2, through f_N and having any selected phase relationship (e.g., inverted, 90 degrees, quadrature, etc.).

The third exemplary system **1201** (and the various other exemplary embodiments discussed below provide for generating a plurality of reference signals, whether sinusoidal or square-wave, such as for use as one or more clock signals or frequency references. The clock/frequency reference (**100**, **200**, **300**) provides a first reference signal (having a first frequency f_0), and is coupled to one or more locking circuits **1204** such as phase-locked loops, delay-locked loops, injection locking circuits (illustrated as locking circuit $\mathbf{1204}_1$, locking circuit $\mathbf{1204}_2$, through locking circuit $\mathbf{1204}_N$), to provide a corresponding plurality of output signals at selected frequencies, illustrated as frequencies f_{K+1}, f_{K+2}, through f_N. Each locking circuit **1204** of the plurality of locking circuits **1204** has a corresponding divide ratio of a plurality of different divide ratios. In operation, each locking circuit **1204** is adapted to phase, delay or otherwise lock to the first reference signal provided by the clock/frequency reference (**100**, **200**, **300**), and to provide an output, second reference signal having an output frequency determined from the first frequency and the corresponding divide ratio. Each locking circuit **1204**, such as a PLL or DLL, may be implemented as known in the art, such as the illustrated PLL $\mathbf{1204}_A$ in FIG. **43** and discussed below.

In an exemplary embodiment, the frequencies of the second reference signals may be fixed, such as fixed at fabrication through wired or configured dividers or divide ratios, or variable, such as selected or programmed post-fabrication through control circuitry (or logic) or stored coefficients (**1215**) (block **1215**, which may be a register storing coefficients or other circuitry providing control signals), such as to adjust the divide ratios of the locking circuits **1204** for corresponding frequency selection, and as further discussed below. Any stored coefficients (**1215**) may also be part of the various frequency calibration and frequency control coefficients stored in registers **455**, **465** and **495**, as discussed above. As an option, a user input, such as for frequency selection, also may be provided through a user interface (not separately illustrated).

As discussed above with reference to FIGS. **14** (dividers **1000**, **1010**) and **16** (divider **1074** for a differential signal), the output signal from the oscillator of clock/frequency reference (**100**, **200**, **300**), as a first reference signal typically at a first frequency, also may be frequency divided to provide one or more second reference (or clock) signals having one or more selected, second frequencies. FIG. **41** is a block diagram illustrating a third exemplary frequency divider **1218** embodiment in accordance with the teachings of the present invention, for asynchronous frequency division. FIG. **42** is a block diagram illustrating a fourth exemplary frequency divider **1219** embodiment in accordance with the teachings of the present invention, for synchronous frequency division. As previously discussed, for these embodiments, each flip-flop (or counter) **1214** (illustrated as flip-flops $\mathbf{1214}_0$, $\mathbf{1214}_1$, through $\mathbf{1214}_5$) provides a frequency division by a factor of two or, when implemented as a counter, by whatever number maximum (terminal or ultimate) number to which the counter is adapted to count. FIG. **41** illustrates a configuration of the flip-flops (or counters) **1214** to provide asynchronous frequency division. FIG. **42** illustrates a configuration of the flip-flops (or counters) **1214**, with other gate logic (AND gates) **1217** to provide synchronous frequency division. In addition to the illustrated gate logic (AND gates) **1217**, any configuration of combinational logic, for example, may be utilized to provide the selected synchronization, with the gate logic (AND gates) **1217** being one example for the illustrated divide by 8 of FIG. **42**, and all such variations are within the scope of the invention.

Frequency dividers, such as the third exemplary frequency divider **1218** and the fourth exemplary frequency divider **1219**, may be coupled to the oscillator of the various clock generator (timing/frequency reference) (**100**, **200**, **300**) embodiments, providing one or more second reference signals having a corresponding plurality of second frequencies, illustrated as frequencies f_2, f_3, through f_K. Alternatively, frequency dividers such as the third exemplary frequency divider **1218** and the fourth exemplary frequency divider **1219**, may be part of a locking circuit **1204** (e.g., one or more phase-locked loops ("PLLs"), delay-locked loops ("DLLs"), or injection locking circuits) which is coupled to the oscillator of the various clock generator (timing/frequency reference) (**100**, **200**, **300**) embodiments. An exemplary locking circuit was illustrated as PLL **1205** in FIG. **18**. Such locking circuit embodiments are discussed below with reference to FIGS. **43** and **44**. In addition, the various dividers (**1000**, **1010**, **1074**, **1218**, **1219**) may also be coupled to one or more locking circuits **1204**, as illustrated in FIG. **40**.

Both asynchronous frequency division and synchronous frequency division, for providing one or more output signals having a selected frequency, are within the scope of the present invention. In addition, the frequency division may be switched between or among synchronous or asynchronous frequency division, at any point in the divide chain (i.e., the succession of coupled flip-flops (or counters) **1214** as illustrated). Such frequency division may be division by any number. The frequency division may be of either a single-ended or a differential clock or reference signal (e.g., as illustrated in FIGS. **14**, **16**, **41** and **42**). Innumerable other circuit topologies for frequency division will be apparent to those of skill in the art, and are considered equivalent, with all such variations are within the scope of the invention.

Continuing to refer to FIG. **40**, the third exemplary system **1201** may comprise the clock generator (timing/frequency reference) (**100**, **200**, **300**) and any one or more of the illustrated second circuitry, such as inverter **1196**, square-wave generator **1015**, a divider (**1000**, **1010**, **1074**, **1218**, **1219**), a locking circuit **1204**, or any of the various other types of second circuitry previously mentioned, such as one or more processors **1275**, memory **1280**, or I/O interface **1285**. For example, the third exemplary system **1201** may be implemented to include the direct provision (on line **1197**) of the

first reference signal having a first frequency (f_0) to additional second circuitry **1198** such as a processor **1275**, along with one or more dividers (**1000**, **1010**, **1074**, **1218**, **1219**) adapted to provide a plurality of second reference signals at lower frequencies, such as for power saving. Also for example, the third exemplary system **1201** may be implemented to include one or more locking circuits **1204** and/or one or more dividers (**1000**, **1010**, **1074**, **1218**, **1219**) coupled to locking circuits **1204**, to provide a plurality of second reference signals at any corresponding frequencies, such as based upon corresponding divide ratios (providing any rational multiple of the first frequency (f_0).

FIG. **43** is a block diagram illustrating a fourth exemplary system **1202** embodiment in accordance with the teachings of the present invention. The clock/frequency reference (**100**, **200**, **300**) provides a first reference signal (having a first frequency f_0), and is coupled to at least one locking circuit **1204** such as a phase-locked loop (PLL), a delay-locked loop (DLL), or an injection locking circuit, to provide a corresponding, second reference signal, such as a clock output signal at a selected frequency, illustrated as frequency f_N. (A fifth system embodiment with multiple locking circuit **1204** is discussed below with reference to FIG. **44**.) In operation, each locking circuit (such as PLL or DLL) **1204** is adapted to phase, delay or otherwise lock to the first reference signal provided by the clock/frequency reference (**100**, **200**, **300**), and to provide an output signal (as the second reference signal) having an output, second frequency determined from the first frequency and a corresponding divide ratio. Illustrated as a phase-locked loop embodiment for purposes of example and not limitation, a phase-locked loop $\mathbf{1204}_A$ (as a type of locking circuit **1204**) comprises a first divider (or multiplier) **1206** (e.g., ÷N) and a second divider (or multiplier) **1207** (e.g., ÷M), forming a corresponding divide ratio, to provide the second frequency f_N which is a rational multiple (M/N) of first frequency f_0. In the illustrated embodiment, the second divider **1207** effectively functions as a multiplier (dividing the output frequency f_N to a lower frequency to match and phase lock with f_0/N). Depending upon the selected embodiment, the output frequency of the second reference signal (e.g., f_N) may be any rational multiple of the first frequency f_0, whether higher or lower.

The locking circuit **1204**, when implemented as a phase-locked loop embodiment $\mathbf{1204}_A$, further comprises a phase detector **1208**, a charge pump **1209**, optionally filter **1211**, and a voltage-controlled oscillator ("VCO") **1212** (such as a second oscillator **1210** illustrated in FIG. **18**). The VCO **1212** provides the second reference signal having a second frequency f_N which is utilized as a clock or other reference by the processor **1275**, memory **1280**, and I/O interface **1285** in an integrated third system **1202** embodiment.

The clock/reference (**100**, **200**, **300**) is adapted to provide, as output, a first reference signal at a first frequency f_0, or in conjunction with divider or locking circuit **1204**, a second reference signal at a second frequency, illustrated as frequency f_N in FIG. **43**, or with a plurality of locking circuits **1204** or dividers, to provide output of a corresponding plurality of second reference signals having corresponding frequencies f_1, f_2, through f_N illustrated in FIG. **44**. As mentioned above, the frequency selection may occur as part of design and fabrication, such as through selection of the number and size of inductors and capacitors utilized in the LC oscillator of the clock/reference (**100**, **200**, **300**). For example, the size(s) and/or shape(s) of the one or more inductors (e.g., **445**) may be selected through a suitable metal layer mask. Frequency selection also may occur post-fabrication, through the use of the various calibration and control coefficients or signals discussed above. In addition, frequency selection may be performed through the configuration of the one or more locking circuits **1204** (PLL/DLLs), such as through selection of the divide ratio(s) through programmable counters, which may be as part of the design and fabrication of the IC, or may be programmed post-fabrication, also through use of calibration and control coefficients or signals, or by switching dividers in or out of the divide chain.

FIG. **44** is a block diagram illustrating a fifth exemplary system **1203** embodiment in accordance with the teachings of the present invention. The fifth exemplary system **1203** comprises the components previously discussed for the third system **1202** embodiment, namely, a clock/frequency reference (**100**, **200**, **300**), control logic or stored coefficients (**1215**), one or more processors **1275**, an I/O interface (or other I/O means) **1285**, and a memory **1280**. The fifth exemplary system **1203** further comprises a plurality of locking circuits **1204** and dividers (**1000**, **1010**, **1074**, **1218**, **1219**), such as phase-locked loops or delay-locked loops (or injection locking circuits) and synchronous or asynchronous dividers, respectively, to provide a corresponding plurality of second reference signals (clock or other reference signals) having a corresponding plurality of second frequencies, including of any type or shape (single-ended, differential, square-wave, sinusoidal, spread spectrum), illustrated as plurality of second reference signals having corresponding second frequencies f_1, f_2, f_3, f_K, through f_N. The plurality of second reference signals having corresponding frequencies f_1, f_2, f_3, f_K, through f_N, and potentially also the first reference signal having first frequency f_0, are provided to switching circuitry **1290**, for selection of one or more second reference signals to be provided to the one or more processors **1275**, I/O interface **1285**, and memory **1280**.

The switching circuitry **1290** may be controlled by the frequency selection and control logic circuitry **1295** and/or control logic or stored coefficients register (**1215**) (discussed above). For example, the control logic circuitry **1295** may provide one or more control signals to the switching circuitry **1290** which, in turn, is adapted to respond to the one or more control signals to switch a selected second reference signal, of the plurality of second reference signals, to the processor **1275** and the other components. Similarly, one or more stored coefficients (e.g., stored in a coefficient register **1215**) may be utilized to control the switching a selected second reference signal, of the plurality of second reference signals, to the processor **1275** and the other components, by controlling a gate voltage of a switching or pass-transistor, for example. In addition, the frequency selection and control logic circuitry **1295** may also be utilized to control the plurality of locking circuits **1204**, such as by programming the corresponding divide ratios. In exemplary embodiments, the switching circuitry **1290** is implemented to provide substantially glitch-free switching, and may be implemented through any type of switching fabric or matrix, such as through one or more multiplexers, pass-transistors, cross-bar switch, or other switching or configurable circuitry. Alternatively, the switching circuitry **1290** may be omitted, with a plurality of clock or reference signals, having different frequency or phase relationships, types or shapes (e.g., single-ended, differential, square-wave, sinusoidal, spread spectrum) provided directly to the one or more processors **1275**, I/O interface **1285**, and memory **1280**. In addition, the switching circuitry **1290** may be implemented through non-reconfigurable circuitry, such as through various fuse or other electrically programmable connections, ROM connections, or other one-time configurable linkages, for example. Innumerable variations on the

control of the selection of the one or more second reference signals, of the plurality of second reference signals, which are provided to the second processing circuitry such as the processor **1275**, memory **1280**, I/O interface **1285**, will be apparent to those of skill in the art, are considered equivalent and are within the scope of the present invention.

For example, the fifth exemplary system **1203** may be utilized to provide a plurality of clock or reference signals having any selected frequency and/or phase relationships, single-ended or differential, and square-wave or sinusoidal. Continuing with the example, a first, comparatively higher frequency signal may be provided to the one or more processors **1275**, an I/O interface **1285**, and memory **1280** for high performance when ample power is available. A second, comparatively lower frequency signal may be provided to the one or more processors **1275**, an I/O interface **1285**, and memory **1280** for power-saving performance when a power source may be limited, such as for a power reduction when the power supply is a battery. A third, comparatively lower frequency signal may be provided to the one or more processors **1275**, an I/O interface **1285**, and memory **1280** for more power-saving, such as for a sleep or hibernation mode. In addition to frequency determination through the selection of the number and size of inductors and capacitors utilized in the LC oscillator of the clock/reference (**100**, **200**, **300**), the frequency selection and control logic circuitry **1295** and/or control logic or stored coefficients (**1215**) may be programmed or calibrated to control the switching circuitry **1290** to provide any such corresponding clock or other second reference signals having frequencies f_1, f_2, through f_N.

Four exemplary discrete apparatus embodiments are illustrated in FIGS. **45-48**. Similarly to the other illustrated embodiments, these discrete apparatus embodiments are also adapted to operate without locking to an external reference signal, such as without locking to any type of crystal (XTAL) reference. In addition, any of these discrete apparatus embodiments may be provided in configurable or programmable forms, such as to provide selectable frequencies and output pins for the one or more second reference signals, or in non-configurable or non-programmable forms, such as to provide predetermined or otherwise fixed frequencies and output pins for the one or more second reference signals. For example, the discrete apparatus embodiments may be provided as a "standard" IC providing one or more clock signals at predetermined frequencies, or may be provided as a configurable IC for user selection of output frequencies, signal types, signal levels, etc. Such configuration and/or selection may occur as part of design and fabrication, such as through mask-programming of reactance sizes, amounts, and interconnections, or post-fabrication, such as through configuration and selection of interconnections, reactance switching, divide ratios, etc., as discussed in greater detail below. In addition, such configurability may be combined with the exemplary integrated embodiments discussed above.

FIG. **45** is a block diagram illustrating an exemplary first discrete apparatus **3000** embodiment in accordance with the teachings of the present invention, typically implemented as a discrete (i.e., single) integrated circuit. As illustrated in FIG. **45**, the first discrete apparatus **3000** comprises a clock/frequency reference (**100**, **200**, **300**), one or more dividers (**1000**, **1010**, **1074**, **1218**, or **1219**) and/or one or more locking circuits **1204**, which operate as previously discussed, and one or more input/output (I/O) interface circuits **3010**. In addition, as an option, the first discrete apparatus **3000** may further comprise control logic and/or stored coefficients register (**1215**) and a user interface **3025**. Not separately illustrated, the first discrete apparatus **3000** typically includes input for power and control signals, and may also include a voltage regulator.

The one or more locking circuits **1204** may be phase-locked loops or delay-locked loops (or injection locking circuits), and the one or more dividers (**1000**, **1010**, **1074**, **1218**, **1219**) (including any within the locking circuits **1204**) may be synchronous or asynchronous, single-ended or differential, as discussed above. The locking circuits **1204** and/or dividers (**1000**, **1010**, **1074**, **1218**, **1219**) may also be implemented to be configurable or non configurable. In this exemplary first discrete apparatus **3000** and the other exemplary discrete embodiments discussed below, the one or more dividers (**1000**, **1010**, **1074**, **1218**, or **1219**) and/or one or more locking circuits **1204** provide a corresponding plurality of second reference signals (clock or other reference signals) having a corresponding plurality of second frequencies, including of any type or shape (single-ended, differential, square-wave, sinusoidal, spread spectrum, etc.), illustrated as plurality of plurality of second reference signals having corresponding second frequencies f_1, f_2, through f_N. The plurality of second reference signals having corresponding frequencies f_1, f_2, through f_N, and potentially also the first reference signal having first frequency f_0, are provided directly to the corresponding plurality of I/O interfaces **3010**. (In addition, depending upon the number of divider and or locking circuits which are successively "chained", such as illustrated in FIGS. **45** and **48**, with one or more second reference signals occurring between the successive circuits, the resulting output (from the last of the successive divider or locking circuits) may be referred to as plurality of third reference signals having a corresponding plurality of third frequencies f_1, f_2, through f_N).

Similarly to the I/O interface **1285**, the I/O interface **3010** may be implemented as known or may become known in the art, to provide (output) communication of the first and/or second reference signals from the clock/frequency reference (**100**, **200**, **300**) and any of the various dividers (**1000**, **1010**, **1074**, **1218**, **1219**) and locking circuits **1204**, to any other device or structure (e.g., an off-chip device), such as, for example and without limitation, one or more IC input/output pins, or channels, busses, input and output devices, other circuitry, other I/O PADs, mechanisms and media discussed herein, including wireless, optical or wireline, using any applicable standard, technology, or media. For example, when first discrete apparatus **3000** is utilized to provide a clocking IC for a computer or communication system, the I/O interface **3010** is adapted to provide reference signal communication to (and potentially from) one or more conductive lines or wires on a printed circuit board (PCB), one or more busses, such as a PCI bus, a PCI-Express bus, a universal serial bus (USB1 or USB2), or one or more other ICs, such as when connected via IC bonding wires to another IC, and so on. In addition, the I/O interface **3010** may provide an interface to any other device or structure previously discussed.

For purposes of the present invention, while referred to as an I/O interface **3010**, the I/O interface **3010** is only required to provide output of the various first and/or second reference signals. Depending upon the selected embodiment, the I/O interface **3010** may also be implemented to accept various types of input. Similarly, in exemplary embodiments utilizing switchable or configurable connections (discussed below), the I/O interface **3010** may be implemented for both output and input functionality, with input signals correspondingly switched or routed to other parts of the IC, as part of I/O pin configuration, for example.

The I/O interface **3010** is utilized to provide any and/or all signaling and physical interface functions, such as impedance matching, signal transmission or other data output from the first discrete apparatus **3000** to any other device, and any other communication functionality suitable for any selected application. In the exemplary embodiment, the I/O interface **3010** may be implemented to be configurable or programmable, such as for selection of output signal levels (e.g., full voltage rail-to-full voltage rail, or fractional voltage rail-to-fractional voltage rail), selection of output signal types (e.g., single-ended or differential), and for changing or matching a load to be driven. In other exemplary embodiments, the I/O interface **3010** also may be implemented to be non configurable, such as to provide the one or more second reference signals at fixed or predetermined levels, types, and loads.

Such configurability or programmability is also applicable to other configurable or programmable components of the other illustrated, discrete embodiments, and such configurability and/or programmability may be provided through either or both the control circuit or logic and/or stored coefficients register (**1215**) and a user interface **3025**, and implemented as part of design and manufacture, or implemented post-fabrication by a manufacturer, distributor, or end user. (Implementation through control circuit or logic and/or stored coefficients register (**1215**) is illustrated using the dashed lines of FIG. **45**.) In addition, such configurability and/or programmability may be implemented utilizing any type of configurable, programmable, selection, switching or routing circuitry, discussed in detail below with respect to configurable switching or routing circuitry **3040** of FIGS. **46-48**. For example, such configuration and/or programming may be implemented using switches, fuses, laser trimming, pass-transistors, multiplexers, demultiplexers, FPGAs, other configurable logic, etc. The various configurations or programs may be one-time configurations, such as when implemented through fuse connections, mask programming, or static coefficients stored in ROM, or may be reconfigurable, such as through storing variable coefficients in non-volatile memory, such as FLASH or EPROM, for control of corresponding switches or multiplexers, for example.

In addition, configurability or programmability may be provided as part of the design and fabrication of the various embodiments. For example, as discussed above, various pluralities of coefficients or control signals are determined post-fabrication for selection of the first frequency of the first reference signal by calibration to another reference frequency signal, such as an external frequency reference. The first frequency also may be mask programmable through selection of a size (and/or amounts or numbers) of the reactances (inductor(s) and/or capacitors), through selection of a plurality of connections and/or interconnections of the plurality of switchable, controlled reactance modules, to connect or disconnect the various reactances for control of the first frequency, or selection of a plurality of sizes of the plurality of switchable, controlled reactance modules, through selection of the type of signal (such as single-ended or differential), for example. The first frequency is also configurable post-fabrication through selection of a plurality of connections or interconnections of the plurality of switchable, controlled reactance modules and the interconnections of the other various components.

Other configurations are also mask programmable or otherwise configurable or selectable as part of the IC fabrication process. For example, any of the various connections and interconnections between and among components may be programmed in any of the conductive layer masks. For example, a selection of the output location of one or more second reference signals may occur at any point in a divide or locking chain, and may be selected through corresponding selection of interconnections provided in a conductive mask layer. Continuing with the example, for design and fabrication configurability, the I/O interface **3010** may be configured through providing various interconnections (through conductive layer masks), such as to a selected driver or amplifier of a plurality of drivers or amplifiers, to provide a corresponding signal level, or through bonding to a selected potential or floating potential. In addition, any of the various process parameters and sizes may also be modified for programmability and/or configurability, such as through any of the various etches, doping, ion implantation, deposition, layer thicknesses, conductive choices (e.g., metal versus polysilicon), use of stressed or strained substrates such as strained silicon, and so on. Other methods and types of configurability and programmability will be apparent to those of skill in the art, are considered equivalent, and within the scope of the present invention.

Continuing to refer to FIG. **45**, spread-spectrum functionality may also be implemented in accordance with the present invention. For example and without limitation, spread-spectrum functionality may be implemented within the a clock/frequency reference (**100**, **200**, **300**), to vary the first frequency of the first reference signal over time, or within any of the various dividers (**1000**, **1010**, **1074**, **1218**, **1219**) or locking circuits **1204** to vary any of the second frequencies of the corresponding second reference signals over time. For example, a control circuit of (control logic and/or stored coefficients register (**1215**)) may be coupled to the plurality of switchable, controlled reactance modules, and adapted to provide a time-dependent switching of the plurality of switchable, controlled reactance modules to modify the first frequency and provide a spread-spectrum first reference signal having a plurality of different first frequencies over time. Also for example, a control circuit of (control logic and/or stored coefficients register (**1215**)) may be coupled to one or more of the locking circuits **1204**, with the control circuit adapted to provide a time-dependent variance of the divide ratio to provide a spread-spectrum second reference signal having a plurality of different, second frequencies over time. Continuing with the example, the various first and second dividers (**1206** and **1207**) (of a locking circuit **1204**), or any of the other divide circuits (**1000**, **1010**, **1074**, **1218**, **1219**), may be implemented as counters, with the control circuit adapted to modify the terminal or ultimate count upon which the counter provides an output signal, also to vary the one or more second reference signals to provide a spread-spectrum second reference signal having a plurality of different, second frequencies over time.

The various calibrations and configurations may be provided post-fabrication through a user interface **3025**. Such a user interface **3025** may be implemented to provide input to the various types of control circuitry (e.g., **3015**, **1810**) and/or coefficient registers (e.g., **455**, **465**, **495**, **1215**, **1950**, **3020**) for input of any selections or configurations. For example, the user interface **3025** may be coupled to a test bench or other computer interface, for automated input of such selections and configurations, as may be known or become known in the art, such as coupled to the various types of workstations or other equipment utilized for programming FPGAs, non-volatile memory, or other configurable logic.

FIG. **46** is a block diagram illustrating an exemplary second discrete apparatus **3030** embodiment in accordance with the teachings of the present invention. FIG. **47** is a block diagram illustrating an exemplary third discrete apparatus **3050** embodiment in accordance with the teachings of the

present invention. FIG. **48** is a block diagram illustrating an exemplary fourth discrete apparatus **3070** embodiment in accordance with the teachings of the present invention. The second discrete apparatus **3030** is implemented utilizing one or more dividers (**1000**, **1010**, **1074**, **1218**, **1219**), such as configurable counters. The third discrete apparatus **3050** is implemented utilizing one or more locking circuits **1204** (with configurable divide ratios, typically also implemented using configurable counters for incorporated first and second divide circuits). The fourth discrete apparatus **3070** is implemented utilizing both one or more dividers (**1000**, **1010**, **1074**, **1218**, **1219**), such as configurable counters, and one or more locking circuits **1204** (also with configurable divide ratios). In addition, the control circuit **3015** and coefficient register **3020** of the control circuit or logic and/or stored coefficients register (**1215**) are illustrated separately.

Instead of providing the various first reference signal and/or plurality of second reference signals directly to the corresponding I/O interfaces **3010** of the plurality of I/O interfaces **3010**, for these exemplary second, third and fourth discrete apparatus embodiments, the first reference signal and plurality of second reference signals are provided to configurable switching (or routing) circuitry **3040**. More particularly, the one or more dividers (**1000**, **1010**, **1074**, **1218**, or **1219**) and/or one or more locking circuits **1204** provide a corresponding plurality of second (or third) reference signals (clock or other reference signals) having a corresponding plurality of second (or third) frequencies, including of any type or shape (single-ended, differential, square-wave, sinusoidal, spread spectrum) (illustrated as plurality of plurality of second or third reference signals having corresponding second or third frequencies f_1, f_2, through f_N) to the configurable switching (or routing) circuitry **3040**, also with the first reference signal having first frequency f_0. In turn, the configurable switching (or routing) circuitry **3040** selectively switches or routes the first reference signal and plurality of second reference signals to selected I/O interfaces **3010** of the plurality of I/O interfaces **3010**. Such selective switching or routing also may be controlled through the control circuitry **3015** and/or coefficient register **3020** (of a control circuit/coefficient register **1215**), and also configured or programmed through the user interface **3025**.

The configurable switching (or routing) circuitry **3040** may be implemented utilizing any type of configurable, programmable, switching or routing circuitry. For example, such configuration and/or programming may be implemented using multiplexers, demultiplexers, switches, fuses, laser trimming, pass-transistors, FPGAs, or any other types of configurable logic or switching, etc. The various configurations or programs may be one-time configurations which provide a direct routing (direct interconnection) of signals, such as when implemented through mask connections, fuse connections or fixed coefficients stored in ROM, or may be reconfigurable, such as through storing variable coefficients in non-volatile memory, through state machines implemented in control circuitry and other types of control circuitry, for control of corresponding switches or multiplexers, for example. The selected switching or routing provided by the configurable switching (or routing) circuitry **3040** may be programmable or configurable as part of the fabrication process discussed above, such as through mask programmable connections, or may be determined post fabrication, such as through the control circuit or logic and/or stored coefficients register (**1215**) and user interface **3025**.

For example, a generic, flexible and/or adaptive integrated circuit containing the various exemplary embodiments may be designed (and fabricated) to support a wide range of first and second frequencies, as discussed above, such as through mask programmability. Post-fabrication, typically through the user interface **3025** or other mechanisms previously discussed, the selected apparatus (IC) may be calibrated to have a first reference signal at one or more first frequencies, such as through the determination of the various coefficients previously discussed (and stored in a coefficient register, such as one of the registers previously discussed or coefficient register **3020**). In addition, depending upon the selected embodiment, such calibration may provide one or more control signals.

Continuing with the example, also through the user interface **3025**, any of the various second and/or third frequencies may be selected, along with their output locations, levels, and types, for providing specific output frequencies and signal types from the otherwise generic or flexible IC. Also post-fabrication, any of the various configurations or programming discussed above may be implemented, through either the use of control signals (from control circuit **3015**) or coefficients (such as switching or control coefficients) (stored in coefficient register **3020**) and utilized to, for example, control switching or routing of the various first and second reference signals. In addition, through the user interface **3025**, the manufacturer, distributor or end user may also configure any of the switching (or routing) circuitry **3040** and other parameters previously discussed, such as the various divide ratios or terminal (ultimate) counts utilized by the various locking circuits **1204** or dividers (**1000**, **1010**, **1074**, **1218**, **1219**) for frequency selection of the one or more second (or third) reference signals, the selected configuration of the I/O interfaces **3010** (e.g., signal level, signal type), and with the configurable switching (or routing) circuitry **3040**, may provide for switching or routing of any selected first or second reference signal, having a corresponding, selected (and configurable) frequency, to any of the I/O interfaces **3010** of the plurality of I/O interfaces **3010**. This addition feature can be utilized, for example, for customized IC pin programming, to provide one or more selected clock signals at selected IC pins.

In summary, the present invention provides an integrated circuit comprising: an oscillator comprising an inductor and a capacitor, the oscillator adapted to provide a first reference signal having a first frequency, the oscillator further adapted to operate without locking to an external reference signal; a voltage controller adapted to provide a plurality of voltage control signals; a plurality of switchable, controlled reactance modules coupled to the oscillator and to the voltage controller, each reactance module of the plurality of reactance modules adapted to provide a selected reactance in response to a corresponding voltage control signal of the plurality of voltage control signals to modify the first frequency; and an output circuit adapted to provide an interface for external signal communication.

The exemplary integrated circuit may further comprise a divider circuit coupled to the oscillator, the divider circuit adapted to provide a second reference signal at a second frequency. A locking circuit may be coupled to the divider circuit and adapted to lock to the second reference signal and provide a third reference signal having a third frequency, with the third frequency determined from the second frequency and a divide ratio of the locking circuit. In addition, a control circuit may be coupled to the locking circuit, with the control circuit adapted to provide a time-dependent variance of the divide ratio to provide a spread-spectrum third reference signal having a plurality of different third frequencies over time. Alternatively, a control circuit may be coupled to the plurality of switchable, controlled reactance modules, with the control circuit adapted to provide a time-dependent switching of the

plurality of switchable, controlled reactance modules to provide a spread-spectrum first reference signal having a plurality of different first frequencies over time.

The output circuit may be configurable for selection of a signal type of a plurality of signal types of the second reference signal, the plurality of signal types comprising at least one of the following signal types: differential, single-ended, full voltage rail-to-full voltage rail, or fractional voltage rail-to-fractional voltage rail.

The exemplary integrated circuit may further comprise a plurality of locking circuits coupled to the divider circuit, the plurality of locking circuits adapted to lock to the second reference signal and provide a corresponding plurality of third reference signals having a plurality of corresponding third frequencies, each third frequency of the plurality of corresponding third frequencies determined from the second frequency and a divide ratio of the corresponding locking circuit of the plurality of locking circuits. Each locking circuit of the plurality of locking circuits may be one of the following locking circuits: a phase-locked loop, a delay-locked loop, or an injection locking circuit. In addition, each locking circuit of the plurality of locking circuits may be configurable for selection of the divide ratio.

The exemplary integrated circuit may further comprise a plurality of output circuits adapted to provide a corresponding plurality of output interfaces for signal communication; and first switching circuitry coupled to the plurality of locking circuits and to the plurality of output circuits, the first switching circuitry adapted to selectively switch a selected, third reference signal of the plurality of third reference signals to a selected output circuit of the plurality of output circuits. Control circuitry may be coupled to the plurality of output circuits and adapted to provide a control signal to a selected output circuit of the plurality of output circuits for selection of a signal type of a plurality of signal types of a corresponding third reference signal. Control circuitry may be coupled to the first switching circuitry and adapted to provide a control signal to the first switching circuitry to switch the selected, third reference signal to the selected output circuit.

Similarly, a coefficient register may be coupled to the first switching circuitry and adapted to provide a first control coefficient of a first plurality of control coefficients to the first switching circuitry to switch the selected, third reference signal to the selected output circuit. The coefficient register may be further coupled to the plurality of switchable, controlled reactance modules, the coefficient register adapted to store a second plurality of coefficients and to provide a corresponding coefficient of the second plurality of coefficients to control switching of a corresponding controlled reactance module to the oscillator. The second plurality of coefficients may be determined post-fabrication by calibration to an external signal providing a reference frequency. The exemplary integrated circuit may further comprise a user interface coupled to the coefficient register and adapted to provide a coefficient of the first plurality of coefficients or second plurality of coefficients to the coefficient register in response to user input.

The first switching circuitry may comprise, for example, a plurality of multiplexers and demultiplexers, or a plurality of pass-transistors, or a cross-bar switch.

The first frequency may be mask programmable through selection of a size of the inductor, or through selection of a plurality of connections of the plurality of switchable, controlled reactance modules, or through selection of a plurality of sizes of the plurality of switchable, controlled reactance modules. The first frequency may be configurable post-fabrication through selection of a plurality of connections of the plurality of switchable, controlled reactance modules.

Another exemplary integrated circuit embodiment may comprise: a harmonic oscillator comprising an inductor and a capacitor, the harmonic oscillator adapted to provide a first reference signal having a first frequency; a plurality of controlled reactance modules coupled to the harmonic oscillator, each reactance module of the plurality of reactance modules adapted to provide a selected reactance in response to a control voltage of a plurality of control voltages to modify the first frequency; a first coefficient register adapted to store a first plurality of switching coefficients; a first plurality of switches coupled to the plurality of controlled reactance modules, each switch of the first plurality of switches responsive to a corresponding switching coefficient of the first plurality of switching coefficients to couple a selected control voltage of the plurality of control voltages to a corresponding controlled reactance module; a first divider coupled to the harmonic oscillator, the first divider adapted to provide a second reference signal at a second frequency; and a plurality of locking circuits coupled to the first divider, the plurality of locking circuits adapted to lock to the second reference signal and provide a corresponding plurality of third reference signals having a plurality of corresponding third frequencies, each third frequency of the plurality of corresponding third frequencies determined from the second frequency and a divide ratio of the corresponding locking circuit of the plurality of locking circuits. The harmonic oscillator may be further adapted to operate without locking to an external reference signal.

Also in summary, another exemplary configurable integrated circuit embodiment may comprise: an oscillator comprising an inductor, a capacitor, and a transconductance amplifier, the oscillator adapted to provide a first reference signal having a first frequency, the oscillator further adapted to operate without locking to an external reference signal, the transconductance amplifier further comprising a variable current source adapted to provide a corresponding current in response to operating temperature; a voltage controller adapted to provide a plurality of voltage control signals; a plurality of switchable, controlled reactance modules coupled to the oscillator and to the voltage controller, each reactance module of the plurality of reactance modules adapted to provide a selected reactance in response to a corresponding voltage control signal of the plurality of voltage control signals to modify the first frequency; a first divider coupled to the harmonic oscillator, the first divider adapted to provide a second reference signal at a second frequency; and a plurality of configurable locking circuits coupled to the first divider, the plurality of locking circuits adapted to lock to the second reference signal and provide a corresponding plurality of third reference signals having a plurality of corresponding third frequencies, each third frequency of the plurality of corresponding third frequencies determined from the second frequency and a configurable divide ratio of the corresponding locking circuit of the plurality of locking circuits.

Also in summary, the present invention provides an integrated circuit, comprising: a resonator comprising an inductor and a capacitor, the resonator adapted to provide a first reference signal having a first frequency; a voltage controller adapted to provide a plurality of voltage control signals; a plurality of switchable, controlled reactance modules coupled to the resonator and to the voltage controller, each reactance module of the plurality of reactance modules adapted to provide a selected reactance in response to a corresponding voltage control signal of the plurality of voltage control signals to modify the first frequency; and a processor

coupled to the resonator. The IC may further comprise a locking circuit coupled to the resonator, the locking circuit adapted to lock to the first reference signal and provide a second reference signal having a second frequency which is a rational multiple of the first frequency; and wherein the processor is coupled through the locking circuit to the resonator, and is adapted to receive the second reference signal.

The first or second reference signals may be, for example, a square-wave clock signal. The processor may be any type of circuitry adapted to perform a function, for example, any one of the following types of processors: a microprocessor; a digital signal processor; a controller; a microcontroller; a universal serial bus (USB) controller; a Peripheral Component Interconnect (PCI) controller; a Peripheral Component Interconnect Express (PCI-e) controller; a Firewire controller; an AT Attachment (ATA) interface controller, an Integrated Drive Electronics (IDE) controller; a Small Computer Systems Interface (SCSI) controller; a television controller; a local area network (LAN) controller; an Ethernet controller; a video controller; an audio controller; a modem processor; an MPEG controller; a multimedia controller; a communication controller; a mobile communication controller; an IEEE 802.11 controller; a GSM controller; a GPRS controller; a PCS controller; an AMPS controller; a CDMA controller; a WCDMA controller; a spread spectrum controller; a wireless LAN controller; an IEEE 802.11 controller; a DSL controller; a T1 controller; a ISDN controller; or a cable modem controller. The integrated circuit may also further comprise: a memory coupled to the processor and further coupled to the locking circuit to receive the second reference signal; and an input/output interface coupled to the processor and further coupled to the locking circuit to receive the second reference signal. The locking circuitry may be one of the following locking circuits, for example: a phase-locked loop, a delay-locked loop, or an injection locking circuit.

In other exemplary embodiments, the integrated circuit further comprises a plurality of locking circuits coupled to the resonator, the plurality of locking circuits adapted to lock to the first reference signal and provide a corresponding plurality of second reference signals having a plurality of corresponding frequencies; and may also include switching circuitry coupled to the plurality of locking circuits and to the processor, the switching circuitry adapted to selectively couple the processor to the plurality of locking circuits by switching a selected, second reference signal of the corresponding plurality of second reference signals to the processor. The integrated circuit may further comprise: control circuitry coupled to the switching circuitry, the control circuitry adapted to provide a control signal to the switching circuitry to switch the selected, second reference signal to the processor; and/or a coefficient register coupled to the switching circuitry, the coefficient register adapted to provide a control coefficient to the switching circuitry to switch the selected, second reference signal to the processor. Each locking circuit of the plurality of locking circuits may further comprise a plurality of asynchronous or synchronous divider circuits, and the plurality of corresponding frequencies are determined by corresponding divide ratios of the plurality of divider circuits. The integrated circuit may further comprise a spread-spectrum generator coupled to the resonator or the locking circuitry, the spread-spectrum generator adapted to provide time-varying modulation of the first reference signal or the second reference signal.

In other exemplary embodiments, the integrated circuit may comprise: a harmonic oscillator comprising an inductor and a capacitor, the harmonic oscillator adapted to provide a first reference signal having a first frequency; a plurality of resistive modules adapted to generate a plurality of voltage control signals; a plurality of controlled reactance modules coupled to the harmonic oscillator and to the plurality of resistive modules, each reactance module of the plurality of reactance modules adapted to provide a selected reactance in response to a corresponding voltage control signal of the plurality of voltage control signals to modify the first frequency; a first coefficient register coupled to the plurality of switches, the first coefficient register adapted to store a first plurality of switching coefficients; a first plurality of switches coupled to the plurality of resistive modules and to the plurality of controlled reactance modules, each switch of the first plurality of switches responsive to a corresponding switching coefficient of the first plurality of switching coefficients to couple a selected control voltage of the plurality of control voltages to a corresponding controlled reactance module; a locking circuit operatively coupled to the harmonic oscillator, the locking circuit adapted to lock to the first reference signal and provide a second reference signal having a second frequency; and a processor operatively coupled to the locking circuit to receive the second reference signal.

This integrated circuit may further comprise: a plurality of locking circuits operatively coupled to the harmonic oscillator, the plurality of locking circuits adapted to lock to the first reference signal and provide a corresponding plurality of second reference signals having a plurality of corresponding frequencies; and a second plurality of switches coupled to the plurality of locking circuits and to the processor, the second plurality of switches adapted to switch a selected, second reference signal of the corresponding plurality of second reference signals to the processor. In addition, control circuitry may be coupled to the second plurality of switches, the control circuitry adapted to provide a control signal to the second plurality of switches to switch the selected, second reference signal to the processor. Alternatively a second coefficient register may be coupled to the second plurality of switches, the second coefficient register adapted to provide a control coefficient to the second plurality of switches to switch the selected, second reference signal to the processor.

In other exemplary embodiments, the integrated circuit comprises: a resonator comprising an inductor and a capacitor, the resonator adapted to provide a first reference signal having a first frequency; a sensor adapted to provide a second signal in response to operating temperature or fabrication process variation; a voltage controller adapted to provide a plurality of voltage control signals; a plurality of switchable, controlled reactance modules coupled to the resonator and to the voltage controller, each reactance module of the plurality of reactance modules adapted to provide a selected reactance in response to a corresponding voltage control signal of the plurality of voltage control signals to modify the first frequency; a plurality of locking circuits operatively coupled to the resonator, the plurality of locking circuits adapted to lock to the first reference signal and provide a corresponding plurality of second reference signals having a plurality of corresponding frequencies; a processor adapted to receive a selected, second reference signal of the plurality of second reference signals; and switching circuitry coupled to the plurality of locking circuits and to the processor, the switching circuitry adapted to switch the selected, second reference signal to the processor.

Also in summary, the present invention provides an apparatus comprising a resonator adapted to provide a first signal having a resonant frequency; an amplifier coupled to the resonator; and a frequency controller (coupled to the resonator) which is adapted to select a resonant frequency having a first frequency of a plurality of frequencies. The apparatus

also includes a frequency divider (coupled to the resonator) which is adapted to divide the first signal having the first frequency into a plurality of second signals having a corresponding plurality of frequencies, the plurality of frequencies substantially equal to or lower than the first frequency, such as by division by a rational number.

The first signal may be a differential signal or a single-ended signal. When the first signal is a differential signal, the frequency divider is further adapted to convert the differential signal to a single-ended signal. Similarly, when the first signal is a substantially sinusoidal signal, the frequency divider is further adapted to convert the substantially sinusoidal signal to a substantially square wave signal.

In various embodiments, the frequency divider may comprise a plurality of flip-flops or counters coupled successively in series, wherein an output of a selected flip-flop or counter is a frequency of a previous flip-flop or counter divided by two, or more generally, a plurality of dividers coupled successively in series, wherein an output of a successive divider is a lower frequency than the output of a previous divider. The plurality of dividers may be differential, single-ended, or differential and single-ended, such as differential followed by a final single-ended stage. The frequency divider may also include a square-wave generator adapted to convert the first signal into a substantially square-wave signal having a substantially equal high and low duty cycle.

The present invention may also include a frequency selector coupled to the frequency divider, and adapted to provide an output signal from the plurality of second signals. The frequency selector may further comprise a multiplexer and a glitch-suppressor.

The present invention may also include a mode selector coupled to the frequency selector, wherein the mode selector is adapted to provide a plurality of operating modes, which may be selected from a group comprising a clock mode, a timing and frequency reference mode, a power conservation mode, and a pulsed mode.

For a reference mode, the invention may also include a synchronization circuit coupled to the mode selector; and a controlled oscillator coupled to the synchronization circuit and adapted to provide a third signal; wherein in the timing and reference mode, the mode selector is further adapted to couple the output signal to the synchronization circuit to control timing and frequency of the third signal. Such a synchronization circuit may be a delay-locked loop, a phase-locked loop, or an injection locking circuit.

In selected embodiments, the amplifier may be a negative transconductance amplifier. The frequency controller may be further adapted to modify a current through the negative transconductance amplifier in response to temperature, and may comprise a current source responsive to temperature. Such a current source may have one or more configurations selected from a plurality of configurations, such as the plurality of configurations comprising CTAT, PTAT, and $PTAT^2$ configurations. In addition, the frequency controller may be further adapted to modify a current through the negative transconductance amplifier to select the resonant frequency, modify a transconductance of the negative transconductance amplifier to select the resonant frequency, or modify a current through the negative transconductance amplifier in response to a voltage. The frequency controller may also include a voltage isolator coupled to the resonator and adapted to substantially isolate the resonator from a voltage variation, and may comprises a current mirror, which may further have a cascode configuration. The frequency controller may be further adapted to modify a capacitance or an inductance of the resonator in response to fabrication process variation, temperature variation, or voltage variation.

The frequency controller may have various embodiments for these various functions, and may further comprise: a coefficient register adapted to store a first plurality of coefficients; and a first array having a plurality of switchable capacitive modules coupled to the coefficient register and to the resonator, each switchable capacitive module having a fixed capacitance and a variable capacitance, each switchable capacitive module responsive to a corresponding coefficient of the first plurality of coefficients to switch between the fixed capacitance and the variable capacitance and to switch each variable capacitance to a control voltage. The plurality of switchable capacitive modules may be binary-weighted, or have another weighting scheme. The frequency controller may also include a second array having a plurality of switchable resistive modules coupled to the coefficient register and further having a capacitive module, the capacitive module and the plurality of switchable resistive modules further coupled to a node to provide the control voltage, each switchable resistive module responsive to a corresponding coefficient of a second plurality of coefficients stored in the coefficient register to switch the switchable resistive module to the control voltage node; and a temperature-dependent current source coupled through a current mirror to the second array.

The frequency controller may also include a process variation compensator coupled to the resonator and adapted to modify the resonant frequency in response to fabrication process variation. In an exemplary embodiment, the process variation compensator may comprise: a coefficient register adapted to store a plurality of coefficients; and an array having a plurality of switchable capacitive modules coupled to the coefficient register and to the resonator, each switchable capacitive module having a first fixed capacitance and a second fixed capacitance, each switchable capacitive module responsive to a corresponding coefficient of the plurality of coefficients to switch between the first fixed capacitance and the second fixed capacitance. The plurality of switchable capacitive modules may be binary-weighted, or have another weighting scheme.

In another exemplary embodiment the process variation compensator may comprise: a coefficient register adapted to store a plurality of coefficients; and an array having a plurality of switchable variable capacitive modules coupled to the coefficient register and to the resonator, each switchable variable capacitive module responsive to a corresponding coefficient of the plurality of coefficients to switch between a first voltage and a second voltage. The plurality of switchable variable capacitive modules also may be binary-weighted, or have another weighting scheme.

The present invention may also include a frequency calibration module coupled to the frequency controller and adapted to modify the resonant frequency in response to a reference signal. For example, the frequency calibration module may include a frequency divider coupled to the frequency controller, the frequency divider adapted to convert an output signal derived from the first signal having the first frequency to a lower frequency to provide a divided signal; a frequency detector coupled to the frequency divider, the frequency detector adapted to compare the reference signal to the divided signal and provide one or more up signals or down signals; and a pulse counter coupled to the frequency detector, the pulse counter adapted to determine a difference between the one or more up signals or down signals as an indicator of a difference between the output signal and the reference signal.

The resonator used with the invention may comprise an inductor (L) and a capacitor (C) coupled to form an LC-tank, having a selected configuration of a plurality of LC-tank configurations, such as series, parallel and so on, and may include other components. In other embodiments, the resonator may be selected from a group comprising: a ceramic resonator, a mechanical resonator, a microelectromechanical resonator, and a film bulk acoustic resonator, or any other resonator which is electrically equivalent to an inductor (L) coupled to a capacitor (C).

For example, the resonator typically comprises one or more inductors and capacitors, forming one or more LC-tanks or LC resonators. In a first embodiment, a double-balanced, differential LC oscillator topology is utilized. In other exemplary embodiments, differential or single-ended LC oscillator topologies may be utilized, for example, a single-ended Colpitts LC oscillator, a single-ended Hartley LC oscillator, a differential Colpitts LC oscillator (both common base and common collector versions), a differential Hartley LC oscillator (also both common base and common collector versions), a single-ended Pierce LC oscillator, a quadrature oscillator (e.g., formed from at least two double-balanced, differential LC oscillators), or an active inductor LC oscillator (which may be implemented to be either differential or single-ended) Additional LC oscillator topologies, now known or which become known, are considered equivalent and within the scope of the present invention.

The apparatus of the invention may be utilized as a timing and frequency reference, or as a clock generator. In addition, the invention may also include a second oscillator (such as a ring, relaxation, or phase shift oscillator) providing a second oscillator output signal; and a mode selector coupled to the frequency controller and to the second oscillator, the mode selector adapted to switch to the second oscillator output signal to provide a power conservation mode. Additional operating modes may be provided by a mode selector coupled to the frequency controller, which may be adapted to periodically start and stop the resonator to provide a pulsed output signal, or adapted to selectively start and stop the resonator to provide a power conservation mode.

In another selected embodiment, the apparatus of the invention, comprises: a resonator adapted to provide a first signal having a resonant frequency; an amplifier coupled to the resonator; a temperature compensator coupled to the amplifier and to the resonator, the temperature compensator adapted to modify the resonant frequency in response to temperature; a process variation compensator coupled to the resonator, the process variation compensator adapted to modify the resonant frequency in response to fabrication process variation; a frequency divider coupled to the resonator, the frequency divider adapted to divide the first signal having the resonant frequency into a plurality of second signals having a corresponding plurality of frequencies, the plurality of frequencies substantially equal to or lower than the resonant frequency; and a frequency selector coupled to the frequency divider, the frequency selector adapted to provide an output signal from the plurality of second signals.

In another selected embodiment, the apparatus of the invention generates a clock signal, and comprises: an LC resonator adapted to provide a differential, substantially sinusoidal first signal having a resonant frequency; a negative transconductance amplifier coupled to the LC resonator; a temperature compensator coupled to the negative transconductance amplifier and to the LC resonator, the temperature compensator adapted to modify a current in the negative transconductance amplifier in response to temperature and further to modify a capacitance of the LC resonator in response to temperature; a process variation compensator coupled to the LC resonator, the process variation compensator adapted to modify the capacitance of the LC resonator in response to fabrication process variation; a frequency divider coupled to the resonator, the frequency divider adapted to convert and divide the first signal having the resonant frequency into a plurality of single-ended, substantially square-wave second signals having a corresponding plurality of frequencies, the plurality of frequencies substantially equal to or lower than the resonant frequency, and each second signal having a substantially equal high and low duty cycle; and a frequency selector coupled to the frequency divider, the frequency selector adapted to provide an output signal from the plurality of second signals.

From the foregoing, it will be observed that numerous variations and modifications may be effected without departing from the spirit and scope of the novel concept of the invention. It is to be understood that no limitation with respect to the specific methods and apparatus illustrated herein is intended or should be inferred. It is, of course, intended to cover by the appended claims all such modifications as fall within the scope of the claims.

It is claimed:

1. An integrated circuit comprising:

a reference oscillator comprising an inductor and a capacitor, the reference oscillator adapted to provide a first reference signal having a first frequency;

a plurality of controlled reactance modules coupled to the reference oscillator, each reactance module of the plurality of reactance modules adapted to provide a selected reactance in response to a control voltage to maintain the first frequency substantially constant in a first operating mode; and

an output circuit adapted to provide an output interface for signal communication.

2. The integrated circuit of claim **1**, further comprising:

a voltage controller coupled to the plurality of controlled reactance modules, the voltage controller adapted to provide the control voltage.

3. The integrated circuit of claim **1**, further comprising:

a control circuit coupled to the plurality of controlled reactance modules, the control circuit adapted to provide a time-dependent switching of the plurality of controlled reactance modules, in a second operating mode, to provide a spread-spectrum first reference signal having a plurality of different first frequencies over time.

4. The integrated circuit of claim **1**, further comprising:

a divider circuit coupled to the reference oscillator, the divider circuit adapted to provide a second reference signal at a second frequency.

5. The integrated circuit of claim **4**, further comprising:

a locking circuit coupled to the divider circuit and adapted to lock to the second reference signal and provide a third reference signal having a third frequency, the third frequency determined from the second frequency and a divide ratio of the locking circuit.

6. The integrated circuit of claim **5**, further comprising:

a control circuit coupled to the locking circuit, the control circuit adapted to provide a time-dependent variance of the divide ratio to provide a spread-spectrum third reference signal having a plurality of different third frequencies over time.

7. The integrated circuit of claim **4**, wherein the output circuit is configurable for selection of a signal type of a plurality of signal types of the second reference signal, the plurality of signal types comprising at least one of the follow-

ing signal types: differential, single-ended, full voltage rail-to-full voltage rail, or fractional voltage rail-to-fractional voltage rail.

8. The integrated circuit of claim **4**, further comprising:

a plurality of locking circuits coupled to the divider circuit, the plurality of locking circuits adapted to lock to the second reference signal and provide a corresponding plurality of third reference signals having a plurality of corresponding third frequencies, each third frequency of the plurality of corresponding third frequencies determined from the second frequency and a divide ratio of the corresponding locking circuit of the plurality of locking circuits.

9. The integrated circuit of claim **8**, wherein each locking circuit of the plurality of locking circuits is at least one of the following locking circuits: a phase-locked loop, a delay-locked loop, or an injection locking circuit.

10. The integrated circuit of claim **8**, wherein each locking circuit of the plurality of locking circuits is configurable for selection of the divide ratio.

11. The integrated circuit of claim **8**, further comprising:

a plurality of output circuits adapted to provide a corresponding plurality of output interfaces for signal communication; and

first switching circuitry coupled to the plurality of locking circuits and to the plurality of output circuits, the first switching circuitry adapted to selectively switch a selected, third reference signal of the plurality of third reference signals to a selected output circuit of the plurality of output circuits.

12. The integrated circuit of claim **11**, further comprising:

control circuitry coupled to the plurality of output circuits, the control circuitry adapted to provide a control signal to a selected output circuit of the plurality of output circuits for selection of a signal type of a plurality of signal types of a corresponding third reference signal, the plurality of signal types comprising at least one of the following signal types: differential, single-ended, full voltage rail-to-full voltage rail, or fractional voltage rail-to-fractional voltage rail.

13. The integrated circuit of claim **11**, further comprising:

control circuitry coupled to the first switching circuitry, the control circuitry adapted to provide a control signal to the first switching circuitry to switch the selected, third reference signal to the selected output circuit.

14. The integrated circuit of claim **11**, further comprising:

a coefficient register coupled to the first switching circuitry, the coefficient register adapted to provide a first control coefficient of a first plurality of control coefficients to the first switching circuitry to switch the selected, third reference signal to the selected output circuit.

15. The integrated circuit of claim **14**, wherein the coefficient register is further coupled to the plurality of controlled reactance modules, the coefficient register adapted to store a second plurality of coefficients and to provide a corresponding coefficient of the second plurality of coefficients to control a switching of a corresponding controlled reactance module to the oscillator.

16. The integrated circuit of claim **15**, further comprising:

a voltage controller coupled to the plurality of controlled reactance modules, the voltage controller adapted to provide the control voltage; and

wherein the plurality of controlled reactance modules further comprise:

a second plurality of switches coupled to the coefficient register; and

a plurality of variable capacitors correspondingly coupled to the second plurality of switches and to the voltage controller, the plurality of variable capacitors adapted to provide a selected capacitance in response to the control voltage.

17. The integrated circuit of claim **16**, wherein the plurality of controlled reactance modules further comprise:

a plurality of fixed capacitors correspondingly coupled to the second plurality of switches, the plurality of fixed capacitors adapted to provide a selected capacitance in response to a corresponding coefficient.

18. The integrated circuit of claim **15**, wherein the second plurality of coefficients is determined post-fabrication by calibration to an external signal providing a reference frequency.

19. The integrated circuit of claim **15**, further comprising:

a user interface coupled to the coefficient register, the user interface adapted to provide a coefficient of the first plurality of coefficients or second plurality of coefficients to the coefficient register in response to user input.

20. The integrated circuit of claim **11**, wherein the first switching circuitry comprises a plurality of multiplexers and demultiplexers, or a plurality of pass-transistors, or a cross-bar switch.

21. The integrated circuit of claim **1**, wherein the first frequency is mask programmable through selection of a size of the inductor, or through selection of a plurality of connections of the plurality of controlled reactance modules, or through selection of a plurality of sizes of the plurality of controlled reactance modules.

22. The integrated circuit of claim **1**, wherein the first frequency is configurable post-fabrication through selection of a plurality of connections of the plurality of controlled reactance modules.

23. The integrated circuit of claim **1**, wherein the oscillator has at least one configuration of the following configurations: a double-balanced, differential LC configuration; a differential n-MOS cross-coupled topology; a differential p-MOS cross-coupled topology; a single-ended Colpitts LC configuration; a single-ended Hartley LC configuration; a differential, common base Colpitts LC configuration; a differential, common collector Colpitts LC configuration; a differential, common base Hartley LC configuration; a differential, common collector Hartley LC configuration; a single-ended Pierce LC oscillator, or a quadrature LC oscillator configuration.

24. The integrated circuit of claim **1**, further comprising a variable current source, the variable current source adapted to provide a corresponding current in response to ambient or operating temperature.

25. An integrated circuit comprising:

a reference harmonic oscillator comprising an inductor and a capacitor, the harmonic oscillator adapted to provide a first reference signal having a first frequency;

a first plurality of controlled reactance modules coupled to the reference harmonic oscillator, each reactance module of the first plurality of reactance modules adapted to provide a selected reactance in response to a control voltage to maintain the first frequency substantially constant in a first operating mode;

a first coefficient register adapted to store a first plurality of switching coefficients;

a first plurality of switches coupled to the first plurality of controlled reactance modules, each switch of the first plurality of switches responsive to a corresponding switching coefficient of the first plurality of switching

coefficients to couple a control voltage to a corresponding controlled reactance module; and

a first divider coupled to the reference harmonic oscillator, the first divider adapted to provide a second reference signal at a second frequency.

26. The integrated circuit of claim **25**, wherein the reference harmonic oscillator is further adapted to provide the first reference signal without locking to an external reference signal.

27. The integrated circuit of claim **25**, further comprising:

a control circuit coupled to the first plurality of controlled reactance modules, the control circuit adapted to provide, in a second operating mode, a time-dependent switching of the plurality of control voltages to provide a spread-spectrum first reference signal having a plurality of different first frequencies over time.

28. The integrated circuit of claim **25**, further comprising:

a second plurality of switches coupled to the first plurality of controlled reactance modules, each switch of the second plurality of switches responsive to a control signal to couple a selected controlled reactance module to a ground or power voltage.

29. The integrated circuit of claim **25**, further comprising:

a second plurality of controlled reactance modules; and

a control circuit coupled to the second plurality of controlled reactance modules, the control circuit adapted to provide, in a second operating mode, a time-dependent switching of the second plurality of controlled reactance modules to the harmonic oscillator to provide a spread-spectrum first reference signal having a plurality of different first frequencies over time.

30. The integrated circuit of claim **25**, wherein the divider circuit is configurable for selection of a signal type of a plurality of signal types of the second reference signal, the plurality of signal types comprising at least one of the following signal types: differential, single-ended, full voltage rail-to-full voltage rail, or fractional voltage rail-to-fractional voltage rail.

31. The integrated circuit of claim **25**, further comprising:

a plurality of locking circuits coupled to the first divider, the plurality of locking circuits adapted to lock to the second reference signal and provide a corresponding plurality of third reference signals having a plurality of corresponding third frequencies, each third frequency of the plurality of corresponding third frequencies determined from the second frequency and a divide ratio of the corresponding locking circuit of the plurality of locking circuits.

32. The integrated circuit of claim **31**, further comprising:

a control circuit coupled to the plurality of locking circuits, the control circuit adapted to provide a time-dependent variance of the divide ratio of a first locking circuit of the plurality of locking circuits to provide a spread-spectrum third reference signal having a plurality of different third frequencies over time.

33. The integrated circuit of claim **31**, wherein each locking circuit of the plurality of locking circuits is at least one of the following locking circuits: a phase-locked loop, a delay-locked loop, or an injection locking circuit.

34. The integrated circuit of claim **31**, wherein each locking circuit of the plurality of locking circuits is configurable for selection of the divide ratio.

35. The integrated circuit of claim **31**, further comprising:

a plurality of output circuits; and

second switching circuitry coupled to the plurality of locking circuits and to the plurality of output circuits, the second switching circuitry adapted to selectively switch a selected, third reference signal of the plurality of third reference signals to a selected output circuit of the plurality of output circuits.

36. The integrated circuit of claim **35**, wherein each output circuit of the plurality of output circuits is configurable for selection of a signal level of a plurality of signal levels for output of a corresponding third reference signal of the plurality of third reference signals.

37. The integrated circuit of claim **35**, further comprising:

control circuitry coupled to the second switching circuitry, the control circuitry adapted to provide a control signal to the second switching circuitry to switch the selected, third reference signal to the selected output circuit.

38. The integrated circuit of claim **35**, further comprising:

a second coefficient register coupled to the second switching circuitry, the second coefficient register adapted to provide a control coefficient of a second plurality of control coefficients to the second switching circuitry to switch the selected, third reference signal to the selected output circuit.

39. The integrated circuit of claim **35**, wherein the second switching circuitry comprises a plurality of multiplexers and demultiplexers, or a plurality of pass-transistors, or a cross-bar switch.

40. The integrated circuit of claim **25**, wherein the first plurality of controlled reactance modules further comprise:

a plurality of variable capacitors, each variable capacitor of the plurality of variable capacitors adapted to provide a corresponding capacitance in response to the control voltage.

41. The integrated circuit of claim **40**, further comprising:

a second plurality of controlled reactance modules comprising a plurality of fixed capacitors, each fixed capacitor of the plurality of fixed capacitors adapted to provide a selected capacitance; and

a second plurality of switches coupled to the second plurality of controlled reactance modules, each switch of the second plurality of switches responsive to a corresponding switching coefficient of a second plurality of switching coefficients to couple a corresponding controlled reactance module of the second plurality of controlled reactance modules to the reference harmonic oscillator.

42. The integrated circuit of claim **41**, wherein the second plurality of switching coefficients is determined post-fabrication by calibration to a second reference frequency signal.

43. The integrated circuit of claim **41**, further comprising:

a user interface coupled to the first coefficient register, the user interface adapted to provide a coefficient of the first plurality of switching coefficients or second plurality of control coefficients to the first coefficient registers in response to user input.

44. The integrated circuit of claim **41**, wherein the first frequency is mask programmable through selection of a size of the inductor, through selection of a plurality of connections of the first and second pluralities of controlled reactance modules, or through selection of a plurality of sizes of the first and second pluralities of controlled reactance modules.

45. The integrated circuit of claim **41**, wherein the first frequency is configurable post-fabrication through selection of a plurality of connections of the first and second pluralities of controlled reactance modules.

46. The integrated circuit of claim **25**, wherein the reference harmonic oscillator has at least one configuration of the following configurations: a double-balanced, differential LC configuration; a differential n-MOS cross-coupled topology; a differential p-MOS cross-coupled topology; a single-ended Colpitts LC configuration; a single-ended Hartley LC configuration; a differential, common base Colpitts LC configuration; a differential, common collector Colpitts LC configuration; a differential, common base Hartley LC configuration;

a differential, common collector Hartley LC configuration; a single-ended Pierce LC oscillator, or a quadrature LC oscillator configuration.

47. The integrated circuit of claim **25**, further comprising:

a variable current source adapted to provide a corresponding current in response to ambient or operating temperature.

48. The integrated circuit of claim **47**, wherein the variable current source has at least one complementary to absolute temperature (CTAT) configuration, proportional to absolute temperature (PTAT) configuration, or proportional to absolute temperature squared ($PTAT^2$) configuration.

49. A configurable integrated circuit comprising:

a reference oscillator comprising an inductor, a capacitor, and an amplifier, the reference oscillator adapted to provide a first reference signal having a first frequency without locking to an external reference signal;

a voltage controller adapted to provide a control voltage;

a first plurality of controlled reactance modules coupled to the reference oscillator and to the voltage controller, each reactance module of the plurality of reactance modules adapted to provide a selected reactance in response to the control voltage to maintain the first frequency substantially constant in a first operating mode;

a first divider coupled to the reference oscillator, the first divider adapted to provide a second reference signal at a second frequency; and

a locking circuit coupled to the first divider, the locking circuit adapted to lock to the second reference signal and provide a third reference signal having a third frequency determined from the second frequency and a divide ratio of the locking circuit.

50. The configurable integrated circuit of claim **49**, further comprising:

a control circuit coupled to the locking circuit, the control circuit adapted to provide a time-dependent configuration of the divide ratio of the locking circuit to provide a spread-spectrum third reference signal having a plurality of different third frequencies over time.

51. The integrated circuit of claim **49**, further comprising:

a second plurality of controlled reactance modules;

a coefficient register coupled to the second plurality of controlled reactance modules, the coefficient register adapted to store a plurality of coefficients and to provide a corresponding coefficient to control switching of a corresponding controlled reactance module of the second plurality of controlled reactance modules to the reference oscillator.

52. The configurable integrated circuit of claim **49**, further comprising:

a control circuit coupled to the coefficient register, the control circuit adapted to provide, in a second operating mode, a time-dependent switching of the second plurality of controlled reactance modules to the reference oscillator to provide a spread-spectrum first reference signal having a plurality of different first frequencies over time.

53. The configurable integrated circuit of claim **49**, wherein the oscillator has at least one configuration of the following configurations: a double-balanced, differential LC configuration; a differential n-MOS cross-coupled topology; a differential p-MOS cross-coupled topology; a single-ended Colpitts LC configuration; a single-ended Hartley LC configuration; a differential, common base Colpitts LC configuration; a differential, common collector Colpitts LC configuration; a differential, common base Hartley LC configuration; a differential, common collector Hartley LC configuration; a single-ended Pierce LC oscillator, or a quadrature LC oscillator configuration.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,656,244 B2
APPLICATION NO. : 12/036165
DATED : February 2, 2010
INVENTOR(S) : McCorquodale et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Patent;
Column 1, Line 52: Please insert the following language before FIELD OF THE INVENTION:

--GOVERNMENT FUNDING

This invention was made with Government support under NSF Grant (EEC) 9986866 awarded by the National Science Foundation. The Government has certain rights in this invention.--

Signed and Sealed this
Ninth Day of October, 2012

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office