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ation and adoption of additional standardization. The lack of a centrally located point for monitoring and/or management always has been a criticism leveled at coax-based 802.3/Ethernet. The 10BASE-T hub-based star architecture removes this as an obstacle.

Due to the widespread adoption of hub-based topologies supporting Ethernet, Token Ring, and FDDI, the standardization of network-management information and its exchange also has received significant attention. Currently, the Simple Network Management Protocol (SNMP) is the de facto standard employed in Ethernet networks for the management of infrastructure components (e.g., bridges, routers, etc.) (16). Several standards organizations and network vendors have been working actively on the definition of standards to allow the management of repeaters, particularly 10BASE-T repeaters. This is described in more detail in the section, "Repeater Management."

Shrinking Ethernet Components

Integration at the Node

Since the initial 802.3/Ethernet standards are mature, integrated circuit technology to implement the primary end-station functions has been available for some time. The first complete Ethernet silicon solution, a three-chip set, was available from Advanced Micro Devices (AMD) in 1985, and consisted of a **controller** (containing the processor bus interface and MAC functions), a Manchester encoder/decoder (with the PLS function), and a coax transceiver (with the MAU function) (see Fig. 28). Subsequently, additional silicon vendors offered similar functions. However, the level of integration remained largely unchanged for three to four years, at which point several vendors offered the MAC/PLS functions as an integrated part. The primary obstacle to further integration was the inability to incorporate the AUJ functionality (see the "Isolation" portion of the "Technology Advantages of 10 BASE-T" section for additional details).

The advent of 10BASE-T significantly changed the potential for integration. Silicon vendors were able to resume the integration process, starting with the 10BASE-T transceiver function. The huge installed base of AUJ-compatible

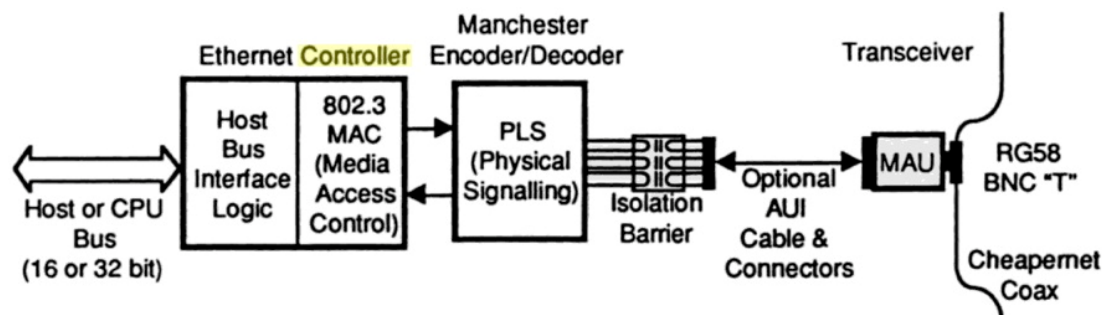


FIG. 28 Typical coaxial chip set for Ethernet node.

16- or 32-bit data and/or address paths. This primarily is due to the large variety of different system buses and CPU types employed in this market space, in which proprietary interfaces frequently are utilized to optimize for performance and/or cost. The system vendor typically embeds the additional interface logic within the system to customize the interface of the LAN controller to suit the specific host bus. However, integration is still of paramount importance, and silicon vendors have integrated the capabilities of the 10BASE-T transceiver with the controller and encoder/decoder functions, to provide a completely integrated, single-chip Ethernet device (see Fig. 30). Most implementations still retain the ability to provide a full 50-m AUI drive capability, providing a compatibility path for coax or fiber installations using an appropriate transceiver. Frequently, the capability to automatically sense the active network port (10BASE-T or AUI) also is provided.

Personal Computers

The commodity PC-compatible market largely has offered LAN connectivity as an add-in card option due to the cost and space associated with network chips and the lack of a predominant standard for office networking in the PC arena. This is by far the largest market segment for Ethernet chip sets. A typical add-in card consists of the LAN components (supporting thick, thin, or twisted-pair Ethernet) and the “glue” logic to interface to the appropriate adapter bus, of which the PC/AT® (commonly referred to as the Industry Standard Architecture [ISA]), EISA™ (Enhanced ISA), MCA™ (Micro Channel Architecture), and various Macintosh buses are the most prevalent.

Two distinct add-in card (or adapter) architectures are predominant, bus master or bus slave. Both types generally are nonintelligent. The use of node processors on the card, popular when bus and processor speeds were lower, is now rare in Ethernet applications, except in specialized areas in which some form of protocol processing is required (e.g., bridges and routers).

Bus mastership allows direct memory access (DMA) directly between the

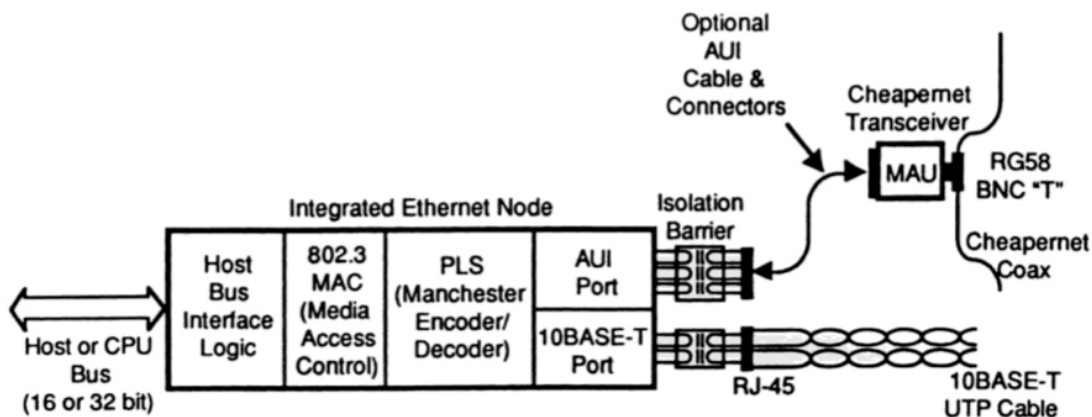


FIG. 30 Typical integrated 10BASE-T chip set for Ethernet node.

LAN controller and system memory, so no additional on-card shared memory is required. The **LAN controller** directly moves transmit data and receive data from and to the PC memory with no CPU intervention. The slave-memory approach provides memory on the adapter card for temporary packet storage, so the CPU writes packet data into this memory for the **LAN controller** to transmit and reads receive data from the memory after the **LAN controller** indicates a completed receive packet.

A good example of a bus-master design, as well as the integration process that has occurred in this area, is the Novell NE2100 and/or NE1500T products. This network card is suited ideally for desktop applications due to its high performance and low cost (no on-board memory).

As shown in the block diagram in Fig. 31, the card consists of the Ethernet **controller** (LANCE, Local Area Network **Controller** for Ethernet), the Manchester encoder/decoder (SIA, serial interface adapter), and the transceiver (coax TAP transceiver or TPEX, Twisted-Pair Ethernet Transceiver). The controller to PC/AT interface logic required some 13 additional ICs. Finally, the IEEE programmable read only memory (PROM) (which contains the unique 48-bit source address for the node) and the boot PROM (for remote start up in diskless workstation environments) are required.

With the submicron-level geometries that are available to mainstream silicon vendors and the fact that the 10BASE-T transceiver can be implemented in this technology, it now is possible to integrate virtually the entire add-in card into a single chip. Only those components that require custom programming (i.e., remote boot PROM and IEEE address PROM) need to remain external to the integrated Ethernet node silicon. The incorporation of the bus interface logic to provide a single-chip, bus-specific **LAN controller** offers the optimal level of

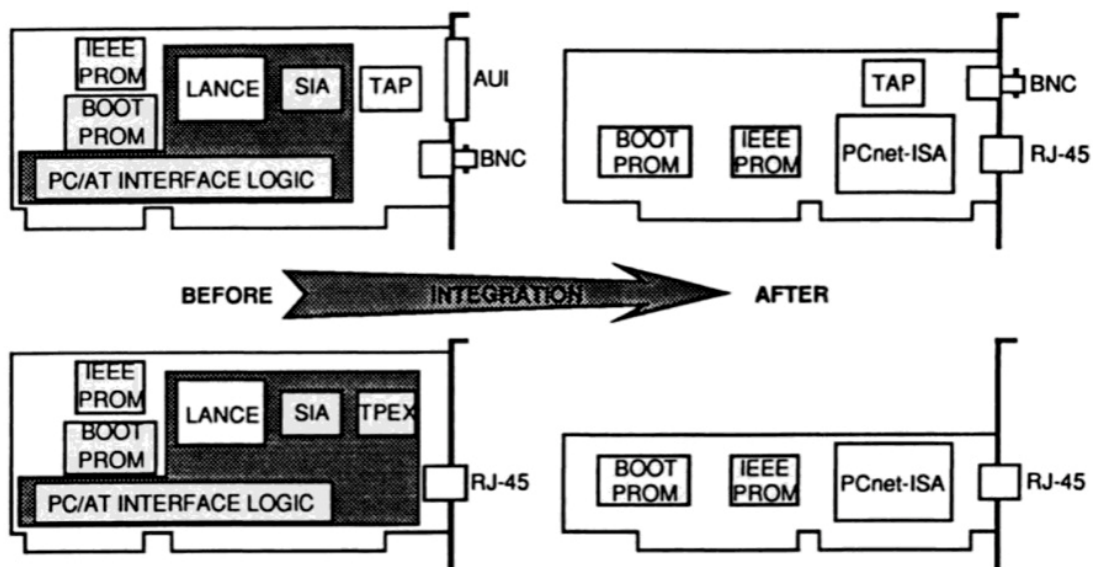


FIG. 31 Equivalent architectures for NE2100 (top) and NE1500T (bottom) (TAP = coax transceiver; TPEX = Twisted-Pair Ethernet Transceiver; PROM = programmable read only memory).