

PRABHAT MISHRA

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RESEARCH EXPERTISE

- **Validation and Verification** (formal verification, system-on-chip validation, test generation, post-silicon debug)
- **Cybersecurity** (hardware/firmware security, security verification, side-channel attacks, confidential computing)
- **Computer Architecture** (processor/memory design, reconfigurable architecture, on-chip communication)
- **Artificial Intelligence** (explainable AI, AI for cybersecurity, AI for VLSI CAD, AI for autonomous systems)
- **Embedded Systems** (compression, exploration, dynamic reconfiguration, energy-aware computing, real-time OS)
- **Quantum Computing** (quantum algorithms, quantum synthesis, quantum measurement, quantum steering)

EDUCATION

PhD	Information and Computer Science	University of California , Irvine, USA	2004
MTech	Computer and Information Technology	Indian Institute of Technology , Kharagpur	1996
BE	Computer Science and Engineering	Jadavpur University , Kolkata, India	1994

EMPLOYMENT

Since Aug 16, 2016	Professor	University of Florida , Gainesville, Florida, USA
Aug 2010 – Aug 2016	Associate Professor	University of Florida , Gainesville, Florida, USA
Jul 2004 – Aug 2010	Assistant Professor	University of Florida , Gainesville, Florida, USA
Dec 1998 – Jun 1999	Senior R&D Engineer	Synopsys , Bangalore, India
Jul 1997 – Dec 1998	Senior Software Engineer	Silicon Automation Systems , Bangalore, India
Feb 1996 – Jun 1997	Software Design Engineer	Texas Instruments , Bangalore, India

MAJOR AWARDS / ACHIEVEMENTS

- **AAAS Fellow**, American Association for the Advancement of Science (AAAS), 2023.
- **IEEE Fellow**, Institute of Electrical and Electronics Engineers (IEEE), 2021.
- **ACM Distinguished Scientist**, Association for Computing Machinery (ACM), 2016.
- **UF Research Foundation Professorship**, University of Florida (UF), 2020 – 2023, 2025 – 2028.
- **UF Doctoral Dissertation Mentoring Award**, University of Florida (UF), 2025.
- **UF Invention of the Year Award**, University of Florida (UF), 2024.
- **UF Preeminence Term Professorship**, University of Florida (UF), 2017 – 2022.
- **HWCOE Doctoral Dissertation Mentoring Award**, Herbert Wertheim College of Engineering, 2019, 2025.
- **IET Outstanding Editor Award**, Institute of Engineering and Technology (IET), 2019
- **CEDA Distinguished Lecturer**, IEEE Council of Electronic Design Automation (CEDA), 2023 – 2024.
- **ACM Distinguished Speaker**, Association for Computing Machinery (ACM), 2016
- **IBM Faculty Award**, IBM Corporation, 2015
- **Best Paper Award**, IEEE ISQED 2016, IEEE VLSI Design 2011, ACM/IEEE CODES+ISSS 2003.
- **NSF CAREER Award**, National Science Foundation (NSF), 2008.
- **UF International Educator of the Year**, University of Florida, 2007.
- **EDAA Outstanding Dissertation Award**, European Design and Automation Association (EDAA), 2004.

SUMMARY OF PUBLICATIONS

- **9 books, 35 book chapters, 13 Ph.D. dissertations, 5 M.S. theses, and 29 patents** (17 pending)
- **80 journal articles and 148 referred conference papers with 8060 citations and h-index of 48** [Google Scholar]

SUMMARY OF FUNDED PROJECTS

- **Overall: 30 grants** in the last **15 years** with a total value of **\$17,428,366** (my portion: **\$7,145,368**)
- **Annual Expenditures: 659,470** (2023-2024), **702,193** (2022-2023), **538,394** (2021-2022), **681,650** (2020-2021)

SUMMARY OF TEACHING CONTRIBUTIONS

- Developed and taught many large (**100 – 350**) undergraduate and graduate-level core courses, including computer organization, hardware modeling and verification, embedded systems, and computer architecture principles.
- The teaching evaluations (**4.3 – 4.8** out of **5**) are consistently higher than the department and college average.

RECENT PROFESSIONAL SERVICES

- **Chair**, ACM TRETs EiC Search Committee, ACM Trans. on Reconfigurable Technology and Systems, 2025.
- **Chair**, IEEE CEDA Fellow Evaluation Committee, IEEE Council of Electronic Design Automation, 2023–2025.
- **Chair**, IEEE Cohort (CEDA+NANO) Fellow Evaluation Committee, IEEE Council of Electronic Design Automation (CEDA) and IEEE Nanotechnology Council (NANO), 2023–2024.
- **Contributor**, NIST/SRC Microelectronics and Advanced Packaging Technologies (MAPT) Roadmap, 2023–25
- **Program Chair**, International Symposium on HW/SW Codesign and System Synthesis (CODES+ISSS), 2024.
- **Vice Program Chair**, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2024.
- **CEDA Distinguished Lecturer**, IEEE Council of Electronic Design Automation (CEDA), 2023 – 2024.
- **ACM Distinguished Speaker**, Association for Computing Machinery (ACM), 2016 – 2019
- **Associate Editor**, ACM Transactions on Embedded Computing Systems (TECS), 2021 - present.
- **Associate Editor**, ACM Transactions on Design Automation of Electronic Systems, 2012-2020, 2024 - present.
- **Associate Editor**, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015 – 2023.
- **Deputy Editor-in-Chief**, IET Computers & Digital Techniques (CDT), 2014 – 2018.
- **Program Chair**, International Conference on VLSI Design (VLSID), 2019.
- **General Chair**, Annual IoT Conference 2019 (IoT), 2019.

LAB/ALUMNI HIGHLIGHTS

- **Overall: 3 Postdocs, 17 Ph.D. dissertations, 5 MS theses, 5 Honors theses, and 40 undergraduate researchers**
- **Current Students: 6 Ph.D. students and 4 undergraduate (REU) researchers**
- **Former Ph.D. Students: 6** in academia (see below) and **7** in industry (e.g., senior architect at Nvidia)
 - Dr. Mingsong Chen, Tenured Full Professor, East China Normal University, China
 - Dr. Kanad Basu, Tenure-Track Assistant Professor, University of Texas at Dallas, USA
 - Dr. Farimah Farahmandi, Tenure-Track Assistant Professor, University of Florida, USA
 - Dr. Yangdi Lyu, Tenure-Track Assistant Professor, Hong Kong University of Science and Technology, China
 - Dr. Subodha Charles, Tenure-Track Assistant Professor, University of Moratuwa, Sri Lanka
 - Dr. Zhixin Pan, Tenure-Track Assistant Professor, Florida State University, USA.

SELECTED PUBLICATIONS

Books

- B9** Z. Pan and P. Mishra, *Explainable Artificial Intelligence for Cybersecurity*, ISBN: 978-3-031-46478-2, **Springer Nature**, 2023.
- B8** P. Mishra and S. Charles (editors), *Network-on-Chip Security and Privacy*, ISBN: 978-3-030-69130-1, **Springer**, 2021
- B7** F. Farahmandi, Y. Huang and P. Mishra, *System-on-Chip Security Validation and Verification*, ISBN: 978-3-030-30596-3, **Springer**, 2019.
- B6** P. Mishra and F. Farahmandi (editors), *Post-Silicon Validation and Debug*, ISBN: 978-3-319-98115-4, **Springer**, 2018.
- B5** P. Mishra, S. Bhunia, M. Tehranipoor (editors), *Hardware IP Security and Trust*, ISBN: 978-3-319-49024-3, **Springer**, January 2017.
- B4** M. Chen, X. Qin, H. Koo and P. Mishra, *System-Level Validation: High-Level Modeling and Directed Test Generation Techniques*, ISBN: 978-1-4614-1358-5, **Springer**, August 2012.
- B3** W. Wang, P. Mishra and S. Ranka, *Dynamic Reconfiguration in Real-Time Systems - Energy, Performance, Reliability and Thermal Perspectives*, ISBN: 978-1-4614-0277-0, **Springer**, July 2012.
- B2** P. Mishra and N. Dutt, Editors, “*Processor Description Languages: Applications and Methodologies*”, ISBN 978-0-12-3742872, **Morgan Kaufmann**, June 2008.
- B1** P. Mishra and N. Dutt, “*Functional Verification of Programmable Embedded Architectures: A Top-Down Approach*”, **Springer**, ISBN 0-387-26143-5, July 2005.

Journal Articles

- J80** S. Sanjaya, A. Jayasena and P. Mishra, Information Leakage through Physical Layer Supply Voltage Coupling Vulnerability, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)*, 2025.
- J79** A. Jayasena, R. Bachmann and P. Mishra, *CISELeaks: Information Leakage Assessment of Cryptographic Instruction Set Extension Prototypes*, *IEEE Transactions on Information Forensics & Security (TIFS)*, volume 20, pages 1551-1565, January 2025.
- J78** S. Sanjaya, H. Witharana, and P. Mishra, *Assertion-Based Validation using Clustering and Dynamic Refinement of Hardware Checkers*, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2024.
- J77** H. Weerasena and P. Mishra, *Revealing CNN Architectures via Side-Channel Analysis in Dataflow-based Inference Accelerators*, *ACM Transactions on Embedded Computing Systems (TECS)*, 2024.
- J76** H. Witharana, H. Weerasena and P. Mishra, *Formal Verification of Virtualization-based Trusted Execution Environments*, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, volume 43, issue 11, pages 4262-4273, November 2024.
- J75** H. Weerasena and P. Mishra, *Breaking On-Chip Communication Anonymity using Flow Correlation Attacks*, *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, volume 20, issue 4, pages 1-27, October 2024.
- J74** A. Jayasena and P. Mishra, *HIVE: Scalable Hardware-Firmware Co-Verification using Scenario-based Decomposition and Automated Hint Extraction*, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, volume 43, issue 10, pages 3278-3291, April 2024.
- J73** H. Witharana, A. Jayasena and P. Mishra, *Incremental Concolic Testing of Register-Transfer Level Designs*, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2024.

- J72** Z. Utt, D. Volya and P. Mishra, *Quantum Measurement Classification using Statistical Learning*, ACM Transactions on Quantum Computing (TQC), 2024.
- J71** Z. Pan and P. Mishra, *TD-Zero: Automatic Golden-Free Hardware Trojan Detection using Zero-Shot Learning*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), volume 43, issue 7, pages 1998-2011, July 2024.
- J70** D. Volya and P. Mishra, *State Preparation on Quantum Computers via Quantum Steering*, IEEE Transactions on Quantum Engineering (TQE), 2024.
- J69** A. Jayasena and P. Mishra, *Directed Test Generation for Hardware Validation: A Survey*, ACM Computing Surveys (CSUR), 2023
- J68** H. Weerasena and P. Mishra, *Security of Electrical, Optical and Wireless On-Chip Interconnects: A Survey*, ACM Transactions on Design Automation of Electronic Systems (TODAES), volume 29, issue 2, pages 1-41, February 2023.
- J67** A. Jayasena, E. Andrews and P. Mishra, *TVLA*: Test Vector Leakage Assessment on Hardware Implementations of Asymmetric Cryptography Algorithms*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI), volume 31, issue 9, pages 1269-1279, July 2023.
- J66** A. Jayasena and P. Mishra, *Scalable Detection of Hardware Trojans using ATPG-based Activation of Rare Events*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), volume 42, issue 12, pages 4450-4462, June 2023.
- J65** Z. Pan and P. Mishra, *AI Trojan Attack for Evading Machine Learning-based Detection of Hardware Trojans*, IEEE Transactions on Computers (TC), 2023.
- J64** M. Dey, M. Patra and P. Mishra, *Efficient Detection and Localization of DoS Attacks in Heterogeneous Vehicular Networks*, IEEE Transactions on Vehicular Technology (TVT), 2022.
- J63** A. Jayasena, B. Kumar, S. Charles, H. Witharana and P. Mishra, *Network-on-Chip Trust Validation using Security Assertions*, Springer Journal of Hardware and Systems Security (HASS), volume 6, pages 79-94, December 2022.
- J62** H. Witharana, A. Jayasena, A. Whigham and P. Mishra, *Automated Generation of Security Assertions for RTL Models*, ACM Journal on Emerging Technologies in Computing Systems (JETC), 2022.
- J61** C. Sudusinghe, S. Charles, S. Ahangama and P. Mishra, *Eavesdropping Attack Detection using Machine Learning in Network-on-Chip Architectures*, IEEE Design & Test (D&T), volume 39, issue 6, pages 28-38, August 2022.
- J60** Z. Pan and P. Mishra, *A Survey on Hardware Vulnerability Analysis using Machine Learning*, IEEE Access, volume 10, pages 49508 – 49527, 2022.
- J59** S. Charles, V. Bindschaedler and P. Mishra, *Digital Watermarking for Detecting Malicious Intellectual Property Cores in NoC Architectures*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, volume 30, issue 7, pages 952-965, July 2022.
- J58** Z. Pan, J. Sheldon and P. Mishra, *Hardware-Assisted Malware Detection and Localization using Explainable Machine Learning*, IEEE Transactions on Computers (TC), volume 71, issue 12, pages 3308-3321, February 2022.
- J57** P. Panigrahi, V. Sahithya, C. Karfa, and P. Mishra, *Secure Register Allocation for Trusted Code Generation*, IEEE Embedded Systems Letters (ESL), 2022.
- J56** H. Witharana, Y. Lyu, S. Charles and P. Mishra, *A Survey on Assertion-based Hardware Verification*, ACM Computing Surveys (CSUR), January 2022.

- J55** A. Das, J. Jose and P. Mishra, *Data Criticality in Multi-Threaded Applications: An Insight for Many-Core Systems*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 29(9), pages 1675-1679, 2021.
- J54** S. Charles and P. Mishra, A Survey of Network-on-Chip Security Attacks and Countermeasures, ACM Computing Surveys (CSUR), 54(5), article 101, pages 1-36, 2021.
- J53** H. Witharana, Y. Lyu and P. Mishra, *Directed Test Generation for Activation of Security Assertions in RTL Models*, ACM Transactions on Design Automation of Electronic Systems (TODAES), 26(4), article 26, pages 1-28, 2021.
- J52** Y. Lyu and P. Mishra, *MaxSense: Side-Channel Sensitivity Maximization for Trojan Detection using Statistical Test Patterns*, ACM Transactions on Design Automation of Electronic Systems (TODAES), 26(3), article 22, pages 1-21, 2021.
- J51** Y. Lyu and P. Mishra, *Scalable Activation of Rare Triggers in Hardware Trojans by Repeated Maximal Clique Sampling*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 40(7), pages 1287-1300, 2021.
- J50** S. Charles and P. Mishra, *Reconfigurable Network-on-Chip Security Architecture*, ACM Transactions on Design Automation of Electronic Systems (TODAES), 25(6), article 53, pages 1-25, 2020.
- J49** Y. Lyu and P. Mishra, *Scalable Concolic Testing of RTL Models*, IEEE Transactions on Computers (TC), 2020.
- J48** A. Sarkar, P. Mishra and T. Kahveci, *Data Perturbation and Recovery of Time Series Gene Expression Data*, IEEE/ACM Transactions on Computational Biology and Bioinformatics (TCBB), 2020.
- J47** S. Charles, Y. Lyu and P. Mishra, *Real-time Detection and Localization of Distributed DoS Attacks in NoC based SoCs*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2020.
- J46** S. Charles, A. Ahmed, U. Ogras and P. Mishra, *Efficient Cache Reconfiguration using Machine Learning in NoC-based Many-Core CMPs*, ACM Transactions on Design Automation of Electronic Systems, 2019.
- J45** A. Ahmed, Y. Huang and P. Mishra, *Cache Reconfiguration using Machine Learning for Vulnerability-aware Energy Optimization*, ACM Transactions on Embedded Computing Systems (TECS), 8(2), article 15, 2019.
- J44** F. Farahmandi and P. Mishra, *Automated Test Generation for Debugging Multiple Bugs in Arithmetic Circuits*, IEEE Transactions on Computers (TC), 68(2), pages 182-197, February 2019.
- J43** Y. Huang, S. Bhunia and P. Mishra, *Scalable Test Generation for Trojan Detection using Side Channel Analysis*, IEEE Transactions on Information Forensics & Security (TIFS), 13(11), pages 2746-2760, May 2018.
- J42** A. Nahiyan, F. Farahmandi, P. Mishra, D. Forte and M. Tehranipoor, *Security-aware FSM Design Flow for Identifying and Mitigating Vulnerabilities to Fault Attacks*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), May 2018.
- J41** Y. Huang and P. Mishra, *Vulnerability-aware Energy Optimization for Reconfigurable Caches in Multitasking Systems*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), May 2018.
- J40** Y. Lyu, X. Qin, M. Chen and P. Mishra, *Directed Test Generation for Validation of Cache Coherence Protocols*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), February 2018.
- J39** K. Rahmani and P. Mishra, *Feature-based Signal Selection for Post-silicon Debug using Machine Learning*, IEEE Transactions on Emerging Topics in Computing (TETC), December 2017.
- J38** Y. Lyu and P. Mishra, *A Survey of Side Channel Attacks on Caches and Countermeasures*, Springer Journal of Hardware and Systems Security (HASS), issue 2, pages 33-50, 2018.
- J37** X. Guo, R. Dutta, P. Mishra and Y. Jin, *Automatic Code Converter Enhanced PCH Framework for SoC Trust Verification*, IEEE Transactions on Very Large Scale Integration Systems, 25(12), 3390-3400, October 2017.

- J36** U. Gupta, C. Patil, G. Bhat, P. Mishra and U. Ogras, *DyPO: Dynamic Pareto Optimal Configuration Selection for Heterogeneous MpSoCs*, ACM Transactions on Embedded Computing Systems (TECS), 16(5), pages 123:1 – 123:20, October 2017.
- J35** P. Mishra, R. Morad, A. Ziv and S. Ray, *Post-silicon Validation in the SoC Era: A Tutorial Introduction*, IEEE Design & Test (D&T), 34(3), pages 1-25, June 2017.
- J34** Y. Huang and P. Mishra, *Trace Buffer Attack on the AES Cipher*, Springer Journal of Hardware and Systems Security (HASS), 1(1), pages 68-84, 2017.
- J33** K. Rahmani, S. Ray and P. Mishra, *Post-silicon Trace Signal Selection Using Machine Learning Techniques*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 25(2), 570-580, 2017.
- J32** M. Chen, X. Zhang, G. Pu, X. Fu and P. Mishra, *Efficient Resource Constrained Scheduling using Parallel Structure-Aware Pruning Techniques*, IEEE Transactions on Computers (TC), 65(7), pages 2059-2073, 2016.
- J31** K. Rahmani, S. Proch and P. Mishra, *Efficient Selection of Trace and Scan Signals for Post-Silicon Debug*, Accepted to appear in IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI), 2015.
- J30** M. Chen, X. Qin and P. Mishra, *Efficient Learning-Oriented Property Decomposition for Automated Generation of Directed Tests*, Springer Journal of Electronic Testing (JETTA), 2014
- J29** K. Basu and P. Mishra, *Restoration-Aware Trace Signal Selection for Post Silicon Validation*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI), 2012.
- J28** X. Qin, W. Wang and P. Mishra, *TCEC: Temperature- and Energy-Constrained Scheduling in Real-Time Multitasking Systems*, IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, 2012.
- J27** W. Wang, S. Ranka and P. Mishra, *Energy-Aware Dynamic Slack Allocation for Real-Time Multitasking Systems*, Elsevier Sustainable Computing: Informatics and Systems (SUSCOM), 2012.
- J26** K. Basu, C. Murthy and P. Mishra, *Bitmask aware Compression of NISC Control Words*, Elsevier Integration, the VLSI Journal (INTEGRATION), 2012.
- J25** X. Qin and P. Mishra, *Directed Test Generation for Validation of Multicore Architectures*, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2012.
- J24** H. Hajimiri, K. Rahmani and P. Mishra, *Compression-Aware Dynamic Cache Reconfiguration for Embedded Systems*, Elsevier Sustainable Computing: Informatics and Systems, 2012.
- J23** W. Wang, P. Mishra and A. Gordon-Ross, *Dynamic Cache Reconfiguration for Soft Real-Time Systems*, ACM Transactions on Embedded Computing Systems (TECS), volume 11, issue 2, article 28, July 2012.
- J22** M. Chen, P. Mishra and D. Kalita, *Automatic RTL Test Generation from SystemC TLM Specifications*, ACM Transactions on Embedded Computing Systems (TECS), 2011.
- J21** M. Chen and P. Mishra, *Property Learning Techniques for Efficient Generation of Directed Tests*, IEEE Transactions on Computers (TC), 2011.
- J20** W. Wang and P. Mishra, *System-Wide Leakage-Aware Energy Minimization using Dynamic Voltage Scaling and Cache Reconfiguration in Multitasking Systems*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI), volume 20, issue 5, pages 902 – 910, May 2012.
- J19** W. Wang and P. Mishra, *Dynamic Reconfiguration of Two-Level Cache Hierarchy in Real-Time Embedded Systems*, Journal of Low Power Electronics (JOLPE), 2011.
- J18** W. Wang, S. Ranka and P. Mishra, *Energy-Aware Dynamic Reconfiguration Algorithms for Real-Time Multitasking Systems*, Elsevier Sustainable Computing: Informatics and Systems(SUSCOM), 2010.
- J17** M. Chen, P. Mishra and D. Kalita, *Efficient Test Case Generation for Validation of UML Activity Diagrams*, Springer Design Automation for Embedded Systems (DAES), 2010.

- J16** M. Chen and P. Mishra, *Efficient Techniques for Directed Test Generation using Incremental Satisfiability*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2009.
- J15** X. Qin, C. Murthy and P. Mishra, Decoding-aware Compression of FPGA Bitstreams, IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI), 2009.
- J14** K. Basu and P. Mishra, “*Test-Data Compression using Application-Aware Bitmask and Dictionary Selection Methods*”, IEEE Transactions on Very Large Scale Integration Systems (TVLSI), volume 18, issue 9, pages 1277-1286, 2010.
- J13** X. Qin and P. Mishra, *A Universal Placement Technique of Compressed Instructions for Efficient Parallel Decompression*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), volume 28, no 8, pages 1224-1236, August 2009.
- J12** H. Koo and P. Mishra, Functional Test Generation using Design and Property Decomposition Techniques, ACM Transactions on Embedded Computing Systems (TECS), vol 8, no 4, article 32, July 2009.
- J11** S. Seong and P. Mishra, *Bitmask-Based Code Compression for Embedded Systems*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 27(4), pages 673-685, 2008.
- J10** P. Mishra and N. Dutt, *Specification-driven Directed Test Generation for Validation of Pipelined Processors*, ACM Transactions on Design Automation of Electronic Systems (TODAES), volume 13, no 3, 36 pages, Article 42, July 2008.
- J9** M. Reshadi, P. Mishra and N. Dutt, “*Hybrid Compiled Simulation: An Efficient Technique for Instruction-Set Architecture Simulation*”, ACM Transactions on Embedded Computing Systems, 8(3), April 2009.
- J8** P. Mishra, A. Shrivastava and N. Dutt, “*Architecture Description Language (ADL)-driven Software Toolkit Generation for Architectural Exploration of Programmable SOCs*”, ACM Transactions on Design Automation of Electronic Systems (TODAES), volume 11, no 3, pages 1-33, July 2006.
- J7** M. Reshadi, P. Mishra and N. Dutt, “*A Retargetable Framework for Instruction-Set Architecture Simulation*”, ACM Transactions on Embedded Computing Systems (TECS), 5(2), pages 431-452, 2006.
- J6** P. Mishra and N. Dutt, “*Architecture Description Languages for Programmable Embedded Systems*”, IEE Proceedings on Computers and Digital Techniques (CDT), 152(3), pages 285-297, May 2005.
- J5** P. Mishra, N. Dutt, N. Krishnamurthy and M. Abadir, “*A Methodology for Validation of Microprocessors using Symbolic Simulation*”, International Journal of Embedded Systems (IJES), 1(1/2), pages 14-22, 2005.
- J4** P. Mishra, N. Dutt, N. Krishnamurthy, and M. Abadir, “*A Top-Down Methodology for Validation of Microprocessors*”, IEEE Design & Test of Computers, 21(2), pages 122-131, March-April, 2004.
- J3** P. Mishra, N. Dutt, and H. Tomiyama, “*Towards Automatic Validation of Dynamic Behavior in Pipelined Processor Specifications*”, Kluwer Design Automation for Embedded Systems, 8(2), pages 249-265, 2003.
- J2** P. Mishra and N. Dutt, “*Modeling and Validation of Pipeline Specifications*”, ACM Transactions on Embedded Computing Systems (TECS), 3(1), pages 140-162, 2004.
- J1** P. Mishra, M. Mamidipaka, and N. Dutt, “*Processor-Memory Co-Exploration using an Architecture Description Language*”, ACM Transactions on Embedded Computing Systems, 3(1), pages 114-139, 2004.

Referred Conference Papers with Archival Proceedings

- C148** H. Weerasena and P. Mishra, *Traffic Analysis Attacks on Wireless NoC-based SoCs*, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2025.
- C147** H. Witharana, H. Weerasena and P. Mishra, *Security Assertions for Trusted Execution Environments*, Design Automation and Test in Europe (DATE), 2025.

- C146** P. Mishra, *Adversarial Assertions*, IEEE International Symposium on Quality Electronic Design (ISQED), 2025.
- C145** D. Volya and P. Mishra, *Quantum Benchmarking via Random Dynamical Quantum Maps*, IEEE International Conference on Quantum Computing and Engineering (QCE), 2024.
- C144** S. Sanjaya, D. Volya and P. Mishra, *Variational Quantum Algorithms via Measurement-Induced Passive Steering*, IEEE International Conference on Quantum Computing and Engineering (QCE), 2024.
- C143** D. Volya, A. Nikitin and P. Mishra, *Fast Quantum Process Tomography via Riemannian Gradient Descent*, IEEE International Conference on Quantum Computing and Engineering (QCE), 2024.
- C142** H. Witharana, H. Weerasena and P. Mishra, *Formal Verification of Virtualization-based Trusted Execution Environments*, ACM/IEEE International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES), 2024.
- C141** H. Witharana, D. Chatterjee and P. Mishra, *Verifying Memory Confidentiality and Integrity of Intel TDX Trusted Execution Environments*, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2024.
- C140** H. Weerasena and P. Mishra, *Lightweight Multicast Authentication in NoC-based SoCs*, IEEE International Symposium on Quality Electronic Design (ISQED), 2024.
- C139** A. Jayasena, R. Bachmann and P. Mishra, *EvilCS: An Evaluation of Information Leakage through Context Switching on Security Enclaves*, Design Automation and Test in Europe (DATE), 2024.
- C138** A. Jayasena and P. Mishra, *Design for Trust utilizing Rareness Reduction*, International Conference on VLSI Design (VLSID), 2024.
- C137** H. Witharana, D. Volya and P. Mishra, *QcAssert: Quantum Device Testing with Concurrent Assertions*, Asia and South Pacific Design Automation Conference (ASPDAC), 2024
- C136** D. Volya and P. Mishra, *Quantum Steering of Surface Error Correcting Codes*, IEEE International Conference on Quantum Computing and Engineering (QCE), 2023.
- C135** D. Volya, Z. Pan and P. Mishra, *Feedback Steering for Quantum State Preparation*, IEEE International Conference on Quantum Computing and Engineering (QCE), 2023
- C134** D. Volya, T. Zhang, N. Alam, M. Tehranipoor and P. Mishra, *Towards Secure Classical-Quantum Systems*, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2023.
- C133** H. Witharana, S. Sanjaya and P. Mishra, *Dynamic Refinement of Hardware Assertion Checkers*, Design Automation and Test in Europe (DATE), 2023.
- C132** Z. Utt, D. Volya and P. Mishra, *Quantum Measurement Discrimination using Cumulative Distribution Functions*, Design Automation and Test in Europe (DATE), 2023.
- C131** Z. Pan and P. Mishra, *Hardware Trojan Detection using Shapley Ensemble Boosting*, Asia and South Pacific Design Automation Conference (ASPDAC), 2023. **[Best Paper Nomination]**
- C130** D. Volya and P. Mishra, *Quantum Data Compression for Efficient Generation of Control Pulses*, Asia and South Pacific Design Automation Conference (ASPDAC), 2023.
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- P12** Prabhat Mishra, Zhixin Pan and Jennifer Sheldon, Hardware-Assisted Malware Detection using Explainable Machine Learning, U.S. Patent No. 11,829,475, November 28, 2023.
- P11** Prabhat Mishra, Subodha Charles and Vincent Bindschaedler, Securing On-Chip Communication using Digital Watermarking, U.S. Non-Provisional Patent Application Serial No. 17/525,176, filed November 12, 2021.
- P10** Prabhat Mishra and Yangdi Lyu, Delay-based Side-channel Analysis for Trojan Detection, U.S. Patent No. 11,580,265, February 14, 2023.
- P9** Prabhat Mishra and Subodha Charles, Reconfigurable Network-on-Chip Security Architecture, U.S. Utility Patent No. 11,593,298, February 28, 2023.
- P8** Subodha Charles and Prabhat Mishra, Lightweight and Trust-aware Routing in NoC based SoC Architectures, U.S. Patent No. 11,770,399, September 26, 2023.
- P7** Prabhat Mishra, Subodha Charles and Yangdi Lyu, Securing System-on-Chip using Incremental Cryptography, U.S. Patent No. 11,552,782, January 10, 2023.
- P6** Prabhat Mishra, Subodha Charles and Yangdi Lyu, Real-Time Detection and Localization of DoS Attacks in NoC based SoC Architectures, U.S. Patent No. 11,797,667, October 24, 2023.
- P5** Prabhat Mishra and Yangdi Lyu, Maximization of Side-Channel Sensitivity for Trojan Detection, U.S. Patent No. 11,579,185, February 14, 2023.
- P4** Prabhat Mishra and Yangdi Lyu, Trigger Activation by Repeated Maximal Clique Sampling, U.S. Patent No. 11,568,046, January 31, 2023.
- P3** Prabhat Mishra, Swarup Bhunia and Yuanwen Huang, MERS: Statistical Test Generation for Side-Channel Analysis Based Trojan Detection, U.S. Copyright Registration TXu 2-112-970, August 17, 2018.

- P2** Swarup Bhunia, Prabhat Mishra and Jonathan Cruz, Trojan Insertion Tool, US Patent 11,144,648, October 12, 2021.
- P1** Prabhat Mishra and Nikil Dutt, Functional Coverage driven Test Generation for Validation of Pipelined Processors, US Patent 7533294, May 12, 2009.

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- BC35** P. Mishra and S. Charles, *Trustworthy System-on-Chip Design using Secure On-Chip Communication Architectures*, Network-on-Chip Security and Privacy, P. Mishra and S. Charles (editors), Springer, 2021.
- BC34** S. Charles and P. Mishra, *Lightweight Encryption using Incremental Cryptography*, Network-on-Chip Security and Privacy, P. Mishra and S. Charles (editors), Springer, 2021.
- BC33** S. Charles and P. Mishra, *Trust-aware Routing in Network-on-Chip Architectures*, Network-on-Chip Security and Privacy, P. Mishra and S. Charles (editors), Springer, 2021.
- BC32** S. Charles and P. Mishra, *Lightweight Anonymous Routing for On-Chip Interconnects*, Network-on-Chip Security and Privacy, P. Mishra and S. Charles (editors), Springer, 2021.
- BC31** S. Charles and P. Mishra, *Real-time Detection and Localization of Denial-of-Service Attacks*, Network-on-Chip Security and Privacy, P. Mishra and S. Charles (editors), Springer, 2021.
- BC30** S. Charles and P. Mishra, *Securing On-Chip Communication using Digital Watermarking*, Network-on-Chip Security and Privacy, P. Mishra and S. Charles (editors), Springer, 2021.
- BC29** C. Sudusinghe, S. Charles and P. Mishra, *Network-on-Chip Attack Detection using Machine Learning*, Network-on-Chip Security and Privacy, P. Mishra and S. Charles (editors), Springer, 2021.
- BC28** M. Rajan, A. Das, J. Jose and P. Mishra, *Trojan-Aware Network-on-Chip Routing*, Network-on-Chip Security and Privacy, P. Mishra and S. Charles (editors), Springer, 2021.
- BC27** A. Jayasena, S. Charles and P. Mishra, *Network-on-Chip Security and Trust Verification*, Network-on-Chip Security and Privacy, P. Mishra and S. Charles (editors), Springer, 2021.
- BC26** P. Mishra and S. Charles, *The Future of Secure and Trustworthy Network-on-Chip Architectures*, Network-on-Chip Security and Privacy, P. Mishra and S. Charles (editors), Springer, 2021.
- BC25** A. Ahmed, F. Farahmandi, Y. Iskander and P. Mishra, *Security and Trust Verification of IoT SoCs*, Security and Fault Tolerance in Internet of Things, R. Chakraborty, J. Mathew and A. Vasilakos (editors), Springer, 2018.
- BC24** A. Ahmed, K. Rahmani and P. Mishra, *Post-Silicon Signal Selection using Machine Learning*, Post-Silicon Validation and Debug, P. Mishra and F. Farahmandi (editors), Springer, 2018.
- BC23** F. Farahmandi and P. Mishra, *Utilization of Debug Infrastructure for Post-Silicon Coverage Analysis*, Post-Silicon Validation and Debug, P. Mishra and F. Farahmandi (editors), Springer, 2018.
- BC22** F. Farahmandi and P. Mishra, *Observability-aware Directed Test Generation*, Post-Silicon Validation and Debug, P. Mishra and F. Farahmandi (editors), Springer, 2018.
- BC21** S. Charles and P. Mishra, *Network-on-Chip Validation and Debug*, Post-Silicon Validation and Debug, P. Mishra and F. Farahmandi (editors), Springer, 2018.
- BC20** Y. Lyu, Y. Huang and P. Mishra, *SoC Security versus Post-Silicon Debug Conflict*, Post-Silicon Validation and Debug, P. Mishra and F. Farahmandi (editors), Springer, 2018.
- BC19** F. Farahmandi and P. Mishra, *Post-Silicon SoC Validation Challenges*, Post-Silicon Validation and Debug, P. Mishra and F. Farahmandi (editors), Springer, 2018.

- BC18** F. Farahmandi and P. Mishra, *The Future of Post-Silicon Debug*, Post-Silicon Validation and Debug, P. Mishra and F. Farahmandi (editors), Springer, 2018.
- BC17** F. Farahmandi, Y. Huang and P. Mishra, *Formal Approaches to Hardware Trust Verification*, The Hardware Trojan War: Attacks, Myths, and Defenses, S. Bhunia and M. Tehranipoor (editors), Springer, 2017.
- BC16** P. Mishra, S. Bhunia and M. Tehranipoor, *Security and Trust Vulnerabilities in Third-party IPs*, Hardware IP Security and Trust, P. Mishra, S. Bhunia and M. Tehranipoor (editors), Springer, 2016.
- BC15** P. Mishra, S. Bhunia and M. Tehranipoor, *The future of Trustworthy SoC Design*, Hardware IP Security and Trust, P. Mishra, S. Bhunia and M. Tehranipoor (editors), Springer, 2016.
- BC14** Y. Huang and P. Mishra, *Malicious Parametric Variations*, Hardware IP Security and Trust, P. Mishra, S. Bhunia and M. Tehranipoor (editors), Springer, 2016.
- BC13** F. Farahmandi and P. Mishra, *Validation of IP Security and Trust*, Hardware IP Security and Trust: Design and Validation Perspectives, P. Mishra, S. Bhunia and M. Tehranipoor (editors), Springer, 2016.
- BC12** A. Chattopadhyay, N. Dutt, R. Leupers and P. Mishra, *Processor Modeling and Design Tools*, Electronic Design Automation for Integrated Circuits Handbook (Second Edition), L. Lavagno, I. Markov, G. Martin and L. Scheffer (editors), CRC Press, 2016.
- BC11** S. Ray, S. Bhunia and P. Mishra, *Security Validation in System-on-Chip*, Fundamentals of IP and SoC Security - Design, Verification and Debug, S. Bhunia, S. Ray and S. Sur-Kolay (editors), Springer, 2015.
- BC10** P. Mishra, *Computer Architecture*, Encyclopedia of Life Support Systems (EOLSS), United Nations Educational, Scientific and Cultural Organization (UNESCO), 2012
- BC9** W. Wang, X. Qin and P. Mishra, *Energy-Aware Dynamic Cache Reconfigurations and Voltage Scaling in Real-Time Systems*, Handbook of Energy-Aware and Green Computing, I. Ahmad and S. Ranka (editors), Chapman & Hall/CRC Press, 2011.
- BC8** N. Bandyopadhyay, K. Basu and P. Mishra, “*HMDES, ISDL and other Contemporary ADLs*”, in Processor Description Languages: Applications and Methodologies, Prabhat Mishra and Nikil Dutt (editors), Morgan Kaufmann Publishers, 2008.
- BC7** P. Mishra and A. Shrivastava, *ADL-driven Methodologies for Design Automation of Embedded Processors*, in Processor Description Languages: Applications and Methodologies, Prabhat Mishra and Nikil Dutt (editors), Morgan Kaufmann Publishers, 2008.
- BC6** P. Mishra and N. Dutt, *EXPRESSION: An ADL for Software Toolkit Generation, Exploration, and Validation of Programmable SOC Architectures*, in Processor Description Languages: Applications and Methodologies, Prabhat Mishra and Nikil Dutt (editors), Morgan Kaufmann Publishers, 2008.
- BC5** P. Mishra and N. Dutt, *Introduction to Architecture Description Languages*, in Processor Description Languages: Applications and Methodologies, Prabhat Mishra and Nikil Dutt (editors), Morgan Kaufmann Publishers, 2008.
- BC4** P. Mishra and N. Dutt, *Architecture Description Languages*, in Customizable and Configurable Embedded Processors”, Paolo Ienne and Rainer Leupers (editors), Morgan Kaufmann, 2006.
- BC3** P. Mishra and N. Dutt, *Processor Modeling and Design Tools*, in The EDA Handbook, G. Martin, L. Lavagno, and L. Scheffer (editors), CRC Press, 2005.
- BC2** P. Mishra and N. Dutt, *Architecture Description Languages for Programmable Embedded Systems*, in SOC: Next Generation Electronics, Bashir M. Al-Hashimi (editor), IEE Press, 2005.
- BC1** P. Mishra and N. Dutt, *Modeling and Verification of Pipelined Embedded Processors in the Presence of Hazards and Exceptions*, in Design and Analysis of Distributed Embedded Systems, Kluwer Academic Publishers, pages 81-90, 2002.

Non-Referred Publications (Magazine Articles, Guest Editorials, Informal Proceedings, etc.)

- M26** E. Andrews and P. Mishra, Explainable Metric Learning for Deflating Data Bias, SRC TECHCON, Austin, Texas, September 8-10, 2024.
- M25** L. Chang, Z. Pan and P. Mishra, Deflating Data Bias through Guided Diffusion, SRC TECHCON, Austin, Texas, September 10-12, 2023.
- M24** E. Andrews, Z. Pan and P. Mishra, Towards Accurate Measurement of Pretraining Bias, SRC TECHCON, Austin, Texas, September 10-12, 2023.
- M23** A. Jayasena and P. Mishra, Towards Formal Verification of Hardware-Firmware Implementations, SRC TECHCON, Austin, Texas, September 10-12, 2023.
- M22** H. Witharana and P. Mishra, Scalable Assertion-based Validation of Trusted Execution Environments, SRC TECHCON, Austin, Texas, September 10-12, 2023.
- M21** Z. Pan and P. Mishra, Hardware-based Acceleration of Explainable AI Models, GOMACTech Conference, San Diego, March 20-23, 2023.
- M20** D. Volya and P. Mishra, A Quantum Algorithm for Graph Clustering, GOMACTech Conference, San Diego, March 20-23, 2023.
- M19** Z. Utt, D. Volya and P. Mishra, Mitigation of Quantum Measurement Errors with Distribution-based Learning, GOMACTech Conference, San Diego, March 20-23, 2023.
- M18** H. Weerasena and P. Mishra, Preserving Confidentiality and Anonymity in NoC-based SoCs, GOMACTech Conference, San Diego, March 20-23, 2023.
- M17** A. Jayasena and P. Mishra, Efficient Activation of Stealthy Triggers in Hardware Trojans, GOMACTech Conference, San Diego, March 20-23, 2023.
- M16** K. Rani, E. Andrews, A. Jayasena and P. Mishra, Defending Elliptic Curve Cryptography against Laser Fault injection Attacks, GOMACTech Conference, San Diego, March 20-23, 2023.
- M15** H. Witharana and P. Mishra, Security validation of Trusted Execution Environments, GOMACTech Conference, San Diego, March 20-23, 2023.
- M14** H. Witharana and P. Mishra, Speculative Load Forwarding Attack on Modern Processors, SRC TECHCON, 2022.
- M13** A. Jayasena and P. Mishra, Network-on-Chip Trust Validation using Security Assertions, SRC TECHCON, 2022.
- M12** H. Witharana and P. Mishra, Automated Generation of Security Assertions for RTL Models, SRC TECHCON, 2021.
- M11** H. Witharana and P. Mishra, Directed Test Generation for Activation of Assertions in RTL Models, SRC TECHCON, 2020.
- M10** P. Mishra, D. Mukhopadhyay and S. Bhunia, Guest Editorial on Machine Intelligence for Security and Privacy Analytics, IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI), 2019.
- M9** P. Mishra, A. Shrivastava and P. Panda, Guest Editorial on Energy-efficient Computing for Embedded and IoT Devices, IET Computer & Digital Techniques (CDT), 2019.
- M8** P. Mishra, Towards Trust Validation of Hardware Intellectual Property (IP) Cores, Special session on New Directions in Hardware Security, International Conference on VLSI Design, 2016.
- M7** Z. Zilic, P. Mishra and S. Shukla, Special Section on System-Level Design and Validation of Heterogeneous Chip Multiprocessors, IEEE Transactions on Computers, 62(2), pages 209-210, 2013.

- M6** P. Mishra, Z. Zilic and S. Shukla, Guest Editors' Introduction: Multicore SoC Validation with Transaction-Level Models, IEEE Design & Test of Computers, May/June 2011.
- M5** S. Shukla, P. Mishra and Z. Zilic, A Brief History of Multiprocessors and EDA, IEEE Design & Test of Computers, May/June 2011.
- M4** Z. Zilic, P. Mishra and S. Shukla, Challenges of Rapidly Emerging Consumer Space Multiprocessors, IEEE Design & Test of Computers, May/June 2011.
- M3** P. Mishra, Guest Editorial, Journal of Electronic Testing, volume 26, number 2, pages 149-150, 2010.
- M2** P. Mishra, Guest Editor Introduction: Special Issue on Nano/Bio-Inspired Applications and Architectures, International Journal of Parallel Programming, volume 37, number 4, pages 343-344, 2009.
- M1** P. Mishra, "*Processor Validation - A Top-Down Approach*", IEEE Potentials, February-March, 29-33, 2005.

PROFESSIONAL SERVICES

Professional Association Memberships

1. **AAAS Fellow**, American Association for Advancement of Science (AAAS), 2023 - present.
2. **IEEE Fellow**, Institute of Electrical and Electronics Engineers (IEEE), 2021 – present.
3. **ACM Distinguished Scientist**, Association for Computing Machinery (ACM), 2015 - present.

Fellow Evaluation Committees

1. **Chair**, CEDA Fellow Evaluation Committee, IEEE Council of Electronic Design Automation, 2024, 2025.
2. **Chair**, CEDA+NANO Cohort Fellow Evaluation Committee, IEEE Council of Electronic Design Automation (CEDA) and IEEE Nanotechnology Council (NANO), 2024.
3. **Member**, IEEE CS Fellow Evaluation Committee, IEEE Computer Society (CS), 2022.
4. **Member**, CEDA Fellow Evaluation Committee, IEEE Council of Electronic Design Automation, 2022, 2023.

Technology Roadmap Initiatives

1. **Contributor**, NIST/SRC Microelectronics and Advanced Packaging Technologies Roadmap, 2024
2. **Contributor**, NIST/SRC Microelectronics and Advanced Packaging Technologies Roadmap, 2023

Distinguished Speaker Appointments

1. **CEDA Distinguished Lecturer**, IEEE Council of Electronic Design Automation (CEDA), 2023 – 2024.
2. **ACM Distinguished Speaker**, Association for Computing Machinery (ACM), 2016 – 2019.

Editorial Activity

1. **Chair**, Editor-in-Chief Search Committee, ACM Trans. on Reconfigurable Technology and Systems, 2025.
2. **Senior Associate Editor**, ACM Transactions on Design Automation of Electronic Systems, 2025 - present.
3. **Associate Editor**, ACM Transactions on Embedded Computing Systems (TECS), 2021 - present.
4. **Associate Editor**, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015-2023.
5. **Associate Editor**, ACM Transactions on Design Automation of Electronic Systems, 2012-2020, 2024 - present.
6. **Deputy Editor-in-Chief**, IET Computers & Digital Techniques (CDT), 2014 – 2018.
7. **Associate Editor**, Springer Journal of Electronic Testing (JETTA), 2012-2019.
8. **Associate Editor**, IEEE Design & Test, 2011-2015.

9. **Associate Editor**, IET Computer & Digital Techniques (CDT), 2012-2015.
10. **Associate Editor**, SIGDA e-Newsletter (eNews), 2012-2013.
11. **Guest Editor**, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, *Special Issue on “Machine Intelligence for Security and Privacy Analytics”*, 2019.
12. **Guest Editor**, IET Computers & Digital Techniques, *Special Issue on “Energy-efficient Computing for Embedded and IoT Devices”*, 2019.
13. **Guest Editor**, IEEE Design & Test of Computers, *Special Issue on “System-Level Design & Validation of Heterogeneous Chip Multiprocessors”*, 2011-2012.
14. **Guest Editor**, IEEE Transactions on Computers, *Special Issue on “Transaction-Level Validation of Multicore Architectures”*, 2010-2011.
15. **Guest Editor**, Springer Journal of Electronic Testing (JETTA), *Special Issue on “High-Level Design Validation and Test”*, 2009-2010.
16. **Guest Editor**, Springer International Journal of Parallel Programming (IJPP), *Special Issue on “Nano/Bio-Inspired Applications and Architectures”*, 2008-2009.
17. **Information Director**, ACM Transactions on Design Automation of Electronic Systems, 2004 - 2010.

Conference Organizing Committee

1. **Program Chair**, ACM/IEEE International Conference on Hardware-Software Co-Design and System Synthesis (CODES+ISSS), 2024, 2025.
2. **Vice Program Chair**, IEEE International Symposium on Hardware Oriented Security and Trust, 2025.
3. **Registration Chair**, IEEE International Symposium on Hardware Oriented Security and Trust, 2024.
4. **Special Sessions Chair**, Embedded Systems Week (ESWEEK), 2022.
5. **Exhibition Co-Chair**, IEEE International Symposium on Hardware Oriented Security and Trust, 2022.
6. **Tutorial Co-Chair**, *Simulation and Validation*, ACM/IEEE Design Automation and Test in Europe, 2021.
7. **Program Chair**, International Conference on VLSI Design (VLSID), 2019.
8. **General Chair**, Annual IoT Conference 2019 (IoT), 2019.
9. **Program Chair**, International Conference on Embedded Systems (ES), 2019.
10. **Subcommittee Chair**, Verification, Design Automation Conference (DAC), 2016.
11. **Tutorial Chair**, International Conference on VLSI Design (VLSI Design), 2016.
12. **Program Co-Chair**, IEEE International Symposium on Rapid System Prototyping (RSP), 2015.
13. **Track Chair**, Simulation and Validation, ACM/IEEE Design Automation and Test in Europe, 2015.
14. **Workshop Chair**, Embedded Systems Week (ESWEEK), 2014.
15. **Track Chair**, *System-level Design*, International Conference on VLSI Design (VLSI Design), 2014.
16. **Track Co-Chair**, *Simulation and Validation*, ACM/IEEE Design Automation and Test in Europe, 2014.
17. **Track Chair**, *Simulation, validation and verification*, ACM/IEEE International Conference on Hardware Software Co-Design and System Synthesis (CODES+ISSS), 2012.
18. **Track Chair**, *Application-Specific Architectures and Algorithms*, ACM/IEEE International Conference on Hardware-Software Co-Design and System Synthesis (CODES+ISSS), 2010.
19. **Track Chair**, *Verification and validation*, ACM/SIGDA Ph.D. Forum at DAC, 2010, 2011, 2012.
20. **Track Chair**, *Systems*, International Conference on Contemporary Computing (IC3), 2010.
21. **General Chair**, IEEE International High Level Design Validation and Test Workshop, 2010.

22. **Program Chair**, IEEE International High Level Design Validation and Test Workshop, 2009.
23. **Track Chair**, *Synthesis and Verification*, International Conference on VLSI Design, 2009.
24. **Publications Chair**, IEEE International High Level Design Validation and Test Workshop, 2008.

Technical Program Committee

1. ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2007–2015, 2017 - 2025.
2. IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2018, 2020-2025.
3. International Conference on Computer-Aided Design (ICCAD), 2011 – 2013, 2018-2020, 2024-2025.
4. ACM/IEEE Design Automation Conference (DAC), 2013-2016, 2018-2020.
5. International Conference on Post-Quantum Cryptography (PQCrypto), 2020.
6. IEEE International Conference on Computer Design (ICCD), 2019, 2020.
7. Design Automation and Test in Europe (DATE), 2006 – 2010, 2012 – 2015.
8. IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), 2013.
9. Asia and South Pacific Design Automation Conference (ASPDAC), 2010 – 2011.
10. International Conference on VLSI Design (VLSI Design), 2007 – present.
11. International Symposium on VLSI Design, Automation and Test (VLSI-DAT), 2011.
12. ACM Great Lakes Symposium on VLSI (GLSVLSI), 2009 – 2010, 2012.
13. IEEE Annual Symposium on VLSI (ISVLSI), 2009 – 2010.
14. IEEE International High Level Design Validation and Test Workshop (HLDVT), 2008 – 2012, 2017.
15. IEEE/IFIP International Conference on VLSI and System-on-Chip (VLSI-SoC), 2010.
16. IEEE International Symposium on Circuits and Systems (ISCAS), 2005 – 2007.
17. IFIP International Conference on Embedded and Ubiquitous Computing (EUC), 2007.
18. International Symposium on Parallel Architectures, Algorithms, and Networks (I-SPAN), 2007.

Session Chairs

1. IEEE/ACM Design Automation Conference (DAC), 2016, 2017, 2018, 2019, 2023.
2. ACM/IEEE/EDAA Design Automation and Test in Europe (DATE), 2020.
3. IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), 2013.
4. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2011.
5. International Conference on VLSI Design (VLSI Design), 2009, 2011, 2012, 2018.
6. ACM Great Lakes Symposium on VLSI (GLSVLSI), 2008, 2009.
7. IEEE International Symposium on VLSI (ISVLSI), 2009.
8. ACM/IEEE/IFIP International Conference on Hardware/Software Codesign and System Synthesis, 2008
9. IEEE International Workshop on Microprocessor Test and Verification (MTV), 2004
10. IEEE International High Level Design Validation and Test Workshop (HLDVT), 2004, 2007.

Reviewer of Scholarly Journals

1. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2007 – 2022.
2. IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2004 – 2022.
3. IEEE Transactions on Computers (TC), 2019 - 2022.

4. ACM Computing Surveys (CSUR), 2014.
5. ACM Transactions on Architecture and Code Optimization (TACO), 2004 – 2007.
6. ACM Transactions on Design Automation of Electronic Systems (TODAES), 2004 – 2008.
7. IEEE Design and Test of Computers (D&T), 2004 – 2010.
8. ACM Transactions on Embedded Computing Systems (TECS), 2004 – 2008.
9. IEEE Transactions on Computers (Computers), 2005 – 2007.
10. IEEE Transactions on Circuits and Systems II (TCAS-II), 2005 – 2007.
11. Springer Design Automation for Embedded Systems (DAES), 2004 – 2007.
12. Elsevier Journal of Parallel and Distributed Computing (JPDC), 2008.
13. Journal on Satisfiability, Boolean Modeling and Computation (JSAT), 2007.

Reviewer of Premier Conferences

1. ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis, 2000 – 2025.
2. IEEE/ACM Design Automation Conference (DAC), 2000 – 2020.
3. IEEE International Test Conference (ITC), 2010.
4. IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2018, 2020.
5. IEEE International Conference on Computer-Aided Design (ICCAD), 2000 – 2025.
6. Design Automation and Test in Europe (DATE), 2000 – 2007.
7. Asia and South Pacific Design Automation Conference (ASPDAC), 2000 – 2007, 2010.
8. International Conference on Compilers, Architectures, and Synthesis for Embedded Systems, 2000 – 2007.
9. IEEE International Conference on VLSI Design (VLSI), 2000 – 2019.
10. IEEE Asian Test Symposium (ATS), 2005.
11. IEEE International Symposium on Circuits and Systems (ISCAS), 2004 – 2007.

Offices Held

1. **President**, Indian Graduate Students' Association, University of California, Irvine, 1999.

Reviewer of Research Proposals

1. NSF Panels, National Science Foundation, 2009, 2010, 2014, 2015-2018, 2022-2025.
2. Deanship of Scientific Research, King Fahd University of Petroleum and Minerals, 2010, 2011, 2014.
3. Council of Physical Sciences, Netherlands Organization for Scientific Research (NWO), 2005.
4. Research Funding Program, University of Cyprus, 2022
5. Research Project Review, University of Sharjah, 2021.

INVITED KEYNOTES AND PRESENTATIONS

Keynote Speeches

- K9** P. Mishra, Explainable AI for Cybersecurity, Systems Day at Indian Institute of Science (IISc), Bengaluru, January 9, 2025.
- K8** P. Mishra, Design Automation for Quantum Computing, International Embedded Systems Symposium (IESS), Gainesville, Florida, October 15, 2024.

- K7** P. Mishra, Design Automation for Quantum Computing, International Workshop on Design Automation for Quantum Computing, IEEE Communications Society, Guwahati, India, July 1, 2024.
- K6** P. Mishra, Securing Hardware for Designing Trustworthy Systems, International Conference on Contemporary Computing (IC3), Noida, India, August 5, 2022. <https://www.ic3conf.net/IC3-2022/index.html>
- K5** P. Mishra, Design of Trustworthy Systems, ISEA International Conference on Security and Privacy, Guwahati, India, February 29, 2020. <https://event.iitg.ac.in/isap2020/>
- K4** P. Mishra, Securing Hardware for Designing Trustworthy Systems, Brazilian Symposium on Information and Computational Systems Security, São Paulo, Brazil, September 3, 2019. <https://sbseg2019.ime.usp.br/en/>
- K3** P. Mishra, Securing Hardware for Designing Trustworthy Systems, SPARC Workshop on Hardware Security (HSW), New Delhi, India, July 27, 2019. <https://www.iiitd.edu.in/noc/hsw/>
- K2** P. Mishra, System-on-Chip Design using Potentially Untrusted Third-Party IPs, ISEA Workshop on Advances in Hardware Security, Guwahati, India, May 24, 2019. https://www.iitg.ac.in/johnjose/isea_ahs.html
- K1** P. Mishra, Cruising the Landscape of System Validation: Dangers and Opportunities, IEEE International Symposium on VLSI Design and Test (VDATE), Coimbatore, India, July 18, 2014.

Panels

- P4** P. Mishra, W. Ruby (FortifyIQ), Trust and Verify: Overcoming costly and piecemeal approaches to pre-silicon side-channel attack vulnerability analysis and verification, ACM/IEEE Design Automation Conference (DAC), San Francisco, December 6, 2021.
- P3** P. Mishra, D. Bertozzi (Univ. of Ferrara), Sujay Deb (IIIT Delhi) and A. Ebrahimi (KTH RIT), Machine Learning and NoCs, International Workshop on Network on Chip Architectures (NoCArc), Athens, Greece, October 22, 2021.
- P2** P. Mishra, Panelist/member of the CCC Visioning Workshop on Extreme Scale Design Automation (ESDA 2014) organized by Computing Community Consortium (CCC) of Computing Research Association (CRA) and Special Interest Group on Design Automation (SIGDA) of Association for Computing Machinery (ACM), Tampa, February 21-22, 2014. <http://www.cra.org/ccc/visioning/visioning-activities/esda>
- P1** P. Mishra, S. Kumar (Freescale), E. Rentschler (Mentor Graphics), K. Reick (IBM), D. Sorin (Duke Univ.), Diagnosing Disaster: Getting to Post-Silicon, ACM/IEEE Design Automation Conference (DAC), San Francisco, June 5, 2014.

Special Sessions

- S4** Prabhat Mishra, Debjit Pal, and Graziano Pravadelli, Specifications mining in a world of generative AI: extensions, applications, and pitfalls, IEEE Design Automation and Test in Europe (DATE), March 31, 2025
- S3** Prabhat Mishra, Huiyang Zhou, Swaroop Ghosh and Samah Saeed, Noise-aware Quantum Synthesis and Compilation IEEE International Conference on Computer Design (ICCD), October 23-26, 2022
- S2** Prabhat Mishra, Susmita Sur-Kolay, Himanshu Thapliyal and Christopher J. Wood, Reliable Quantum Computing using Noisy Intermediate-Scale Quantum Systems, IEEE International Conference on Computer Design (ICCD), October 18-21, 2020.
- S1** Towards Trust Validation of Hardware Intellectual Property (IP) Cores, Special session on New Directions in Hardware Security, International Conference on VLSI Design, January 5, 2016.

Tutorials

- T13** Z. Pan and P. Mishra, Explainable AI for Cybersecurity, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), Washington DC, May 6, 2024.

- T12** P. Mishra and A. Shrivastava (University of Maryland), Hardware Security and Trust Verification, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), Washington DC, May 6, 2024.
- T11** P. Mishra and R. Wille (TU Munich), Design Automation for Quantum Computing, International Conference on VLSI Design, Kolkata, India, January 6-7, 2024.
- T10** D. Volya and P. Mishra, Quantum Noise Characterization and Mitigation Techniques, IEEE International Conference on Quantum Computing and Engineering (QCE), Bellevue, Washington, September 17, 2023.
- T9** P. Mishra, Hardware Security and Trust Validation, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), San Jose, California, May 1, 2023.
- T8** P. Mishra, Hardware Security and Trust Verification, Embedded Systems Week (ESWEEK), Shanghai, October 7, 2022.
- T7** D. Volya and P. Mishra, Quantum Noise Characterization and Mitigation for NISQ Systems, IEEE International Conference on Quantum Computing and Engineering (QCE), Broomfield, Colorado, September 18-23, 2022.
- T6** P. Mishra and S. Vasudevan, Hardware Trust Validation using Machine Learning and Formal Methods, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), Washington DC, June 27, 2022.
- T5** P. Mishra, Verification of Hardware IP Security and Trust, IACR Conference on Cryptographic Hardware and Embedded Systems (CHES), Pune, India, August 25, 2019.
- T4** P. Mishra and R. Chakraborty (IIT Kharagpur), Hardware Intellectual Property (IP) Security and Trust: Challenges and Solutions, International Conference on VLSI Design, January 7, 2018.
- T3** S. Kumar (NXP), J. Schumann (IBM), S. Singh (Intel), S. Menon (Intel), and P. Mishra, The Future of SoC System Validation & Debug. and Why You Should Care!, Design Automation Conference (DAC), 2017.
- T2** P. Mishra, S. Bhunia (Case Western), and S. Ravi (Texas Instruments), Validation and Debug of Security and Trust Issues in Embedded Systems, International Conference on VLSI Design, 2015.
- T1** P. Mishra, M. Fujita (Univ. of Tokyo), V. Singh (IIT Bombay), N. Tamarapalli (AMD), S. Kumar (Freescale) and R. Mittal (TI), Post-Silicon Validation, Debug and Diagnosis, International Conference on VLSI Design, January 6, 2013.

Invited Presentations

1. Securing Hardware for Designing Trustworthy Systems, Arizona State University, March 27, 2025.
2. Explainable AI for Cybersecurity, Indian Institute of Technology (IIT), Guwahati, March 10-21, 2025. I was the lead speaker for this two-week GIAN course, where I provided four-hour lectures each day.
3. Explainable AI for Cybersecurity, Computer Science Seminar, Texas Tech University, February 4, 2025.
4. Explainable AI for Cybersecurity, IISc Systems Day Workshop, Indian Institute of Science (IISc), January 9, 2025.
5. Securing Hardware for Designing Trustworthy Systems, International Conference on VLSI Design (VLSID), Bengaluru, January 7, 2025.
6. Quantum AI for Scientists and Engineers, KIAC Distinguished Seminar, Kotak IISc AI/ML Center (KIAC), Indian Institute of Science (IISc), January 6, 2025.
7. Design Automation for Quantum Computing, IEEE Computer Society Distinguished Seminar, Oregon Chapter, December 5, 2024.
8. Towards Secure Classical-Quantum Systems, Annual Quantum Computer Cybersecurity Symposium (QCCS), New Haven, Connecticut, October 25, 2024.
9. Security Verification of Trusted Execution Environments, Intel SRC GRC Executive Lecture, October 17, 2024.

10. Securing Hardware for Designing Trustworthy Systems, IEEE CEDA Distinguished Lecture, September 26, 2024.
11. Scalable Verification of Software and Hardware Implementations, MathWorks, Massachusetts, July 25, 2024.
12. Explainable AI for Cybersecurity, Indian Institute of Information Technology (IIIT), Guwahati, July 5, 2024.
13. Design Automation for Quantum Computing, Indian Institute of Technology (IIT), Guwahati, July 1-3, 2024. I was the lead speaker for this three-day workshop, where I provided three-hour lectures each day.
14. Securing Hardware for Designing Trustworthy Systems, Department of Electrical and Computer Engineering, Indian Institute of Engineering Science and Technology (IIST), Shibpur, June 26, 2024.
15. Design Automation for Noise-Resilient Quantum Computing, Institute of Engineering & Management, Kolkata, June 25, 2024.
16. Design Automation for Noise-Resilient Quantum Computing, St. Thomas' College of Engineering & Technology, Kolkata, May 14, 2024.
17. Design Automation for Quantum Computing, IEEE CEDA Distinguished Lecture, University of Illinois, Chicago, March 15, 2024.
18. Design Automation for Quantum Computing, ACMU Workshop on Computing Devices: VLSI and Beyond, Indian Statistical Institute, January 12, 2024.
19. Security Verification of Trusted Execution Environments, AMD Tech Talk, November 16, 2023.
20. Explainable AI for Cybersecurity, Interdisciplinary Workshop on Machine Learning for Cryptology (ML4Crypto), Indian Statistical Institute, Kolkata, November 8, 2023.
21. Design Automation for Quantum Computing, Quantum Computer Systems Lecture Series, October 7, 2023. <https://sites.nd.edu/quantum/quantum-computer-systems-qucs-lecture-series/>
22. Network-on-Chip Security and Privacy, IEEE CS Oregon Section Technical Seminar, June 29, 2023.
23. Network-on-Chip Security and Privacy, Raytheon Technologies Symposium, June 23, 2023.
24. Design, Verify and Validate for Security: An end-to-end Approach, Synopsys, March 14, 2023.
25. Securing Hardware for Designing Trustworthy Systems, Motorola Solutions Science Advisory Board Conference, March 9, 2023.
26. Secure and Smart Systems – AI, Quantum, and Edge Computing, L3Harris, February 20, 2023.
27. Securing Hardware for Designing Trustworthy Systems, Department of Electrical and Computer Engineering, University of Houston, February 20, 2023.
28. Noise-Resilient EDA for Quantum Computing, Ansys, February 9, 2023.
29. Securing Hardware for Designing Trustworthy Systems, Department of Electrical and Computer Engineering, Indian Institute of Engineering Science and Technology (IIST), Shibpur, January 6, 2023.
30. Noise-Resilient Quantum Computing, Indian Statistical Institute, January 5, 2023.
31. Noise-Resilient Quantum Computing, Department of Computer Science and Engineering, Jadavpur University, January 4, 2023.
32. Hardware Security and Trust Verification, IEEE CS Oregon Section Technical Seminar, March 31, 2022.
33. Hardware-Assisted Malware Detection using Explainable Machine Learning, Amazon, November 5, 2021.
34. Securing Hardware for Designing Trustworthy Systems, IEEE CS Oregon Section Technical Webinar, September 23, 2021.
35. Securing Hardware for Designing Trustworthy Systems, MIT Computer Science & Artificial Intelligence Lab (CSAIL), Massachusetts Institute of Technology (MIT), Cambridge, Massachusetts, August 3, 2021.

36. Validation of Embedded Systems, Department of Electronic and Telecommunication Engineering, University of Moratuwa, Sri Lanka, May 21, 2021.
37. Securing Hardware for Designing Trustworthy Systems, Tata Consultancy Services (TCS), Kolkata, India, May 11, 2021.
38. Advances in Hardware Security, Indian Institute of Technology (IIT), Guwahati, May 24-29, 2019. The workshop was attended by faculty members, Ph.D. students and researchers from premier academic institutions as well as companies across India. Please visit http://www.iitg.ac.in/johnjose/isea_ahs.html for further details.
39. Hardware-Software Co-Design and Co-Verification for Embedded and IoT Devices, Raytheon (Systems & Software Assurance Technology), October 15, 2020.
40. Design Automation of Embedded and Cyber-Physical Systems, University of São Paulo, Brazil, September 4, 2019.
41. Validation of Hardware Security and Trust, Arizona State University, Tempe, Arizona, November 1, 2018.
42. Validation of Hardware Security and Trust, Indian Institute of Technology (IIT) Kharagpur, July 10, 2018.
43. Validation of Hardware Security and Trust, Stanford University, June 25, 2018.
44. Validation of Hardware Security and Trust, University of South Florida, Tampa, March 9, 2018.
45. Validation and Debug in the Context of Hardware Security, Indian Institute of Technology (IIT) Kharagpur, India, July 2017.
46. SAT-based Bounded Model Checking, Cisco, September 14, 2016.
47. Validation of Hardware Security and Trust, Texas A&M University, College Station, Texas, October 14, 2016.
48. Validation of Hardware Security and Trust, Indian Institute of Technology, Mumbai, India, August 11, 2016.
49. Validation of Hardware Security and Trust, Indian Institute of Technology (IIT Kharagpur), Mumbai, India, August 1, 2016.
50. Towards Trust Validation of Hardware Intellectual Property (IP) Cores, Special session on hardware security, International Conference on VLSI Design, 2016.
51. Design Automation of Embedded Systems, Heritage Institute of Technology, Kolkata, India, Aug. 14, 2015.
52. Design Automation of Embedded Systems, Indian Institute of Engineering, Science and Technology, Shibpur, India, August 12, 2015.
53. Energy-aware Computing – Dynamic Reconfiguration in Real-Time Systems. Indian Statistical Institute, Kolkata, India, August 5, 2015.
54. P. Mishra, Post-Silicon Validation and Debug. Indian Institute of Technology, Kharagpur, Dec. 22, 2014.
55. “Reconfigurable Computing in Memory for Improving Energy Efficiency and Reliability of Embedded Systems”, Workshop on Highly-Reliable Power-Efficient Embedded Designs (HARSH), February 16, 2014. http://researcher.watson.ibm.com/researcher/view_project.php?id=5152
56. “Energy-Aware Dynamic Reconfigurations in Real-Time Embedded Systems”, Intel Symposium on Power-Efficient Computing, Haifa, October 2, 2013. http://workshop.ee.technion.ac.il/index.php?EVT_SysID=195
57. “System-level Validation of Multicore SoCs”, IBM Research, Haifa, October 1, 2013.
58. Technical University of Munich, Germany. Scheduling-Aware Dynamic Reconfigurations, March 2010.
59. Indian Institute of Technology (IIT), Kharagpur. Code Compression for Embedded Systems, April 2008.
60. Calcutta University, India. Design Automation of Embedded Systems, December 2006.

61. AMD, Bangalore, India. Functional Validation of Programmable Architectures, Dec 2006.
62. NXP (Philips) Semiconductors, India. Functional Validation of Embedded Systems, Nov 2006.
63. Intel, Bangalore, India. Functional Validation of Programmable Architectures, July 2006.
64. Indian Institute of Technology, Kharagpur. Top-Down Validation of Embedded Systems, June 2005.
65. Indian Institute of Technology, Delhi. Language-driven Validation of Embedded Architectures, June 2005.
66. Indian Institute of Technology, Kanpur. Validation of Programmable Architectures, June 2005.
67. Indian Institute of Technology, Bombay. Top-Down Validation of Programmable Architectures, June 2005.
68. Indian Institute of Science, Bangalore. Validation of Programmable Embedded Architectures, June 2005.
69. Intel, Arizona. Test Generation using Architecture Description Languages, November 2005.

Ph.D. ADVISEES (Chair)

1. **Heon-Mo Koo**, Ph.D., December 2007.
Dissertation: Coverage-directed Test Generation for Validation of Pipelined Processors
Employment: **Video Codec Architect**, Platform Architecture, **Apple**, USA.
Major Awards: KUSCO-KSEA Scholarship 2007, Korean Graduate Student Award 2006.
2. **Mingsong Chen**, Ph.D., August 2010.
Dissertation: Coverage-directed Test Generation for Validation of Pipelined Processors
Employment: **Professor**, East China Normal University, China.
Major Awards: **Best Paper Nominations**, VLSI Design 2013, and VLSI Design 2010.
3. **Weixun Wang**, Ph.D., August 2011.
Dissertation: Dynamic Reconfiguration in Real-Time Embedded Systems
Employment: **Engineering Leader**, *Stripe*, USA.
4. **Xiaoke Qin**, Ph.D., May 2012.
Dissertation: System-Level Validation of Multicore Architectures
Employment: **Senior Architect**, Nvidia, USA
Major Awards: **Best Paper Nomination**, Design Automation and Test in Europe (DATE), 2012.
5. **Kanad Basu**, Observability Enhancement Techniques for Post-Silicon Validation and Debug, August 2012.
Employment: **Assistant Professor**, University of Texas at Dallas, USA
Major Awards: **NSF CAREER Award**, **Best Paper Award** (VLSID 2021).
6. **Kamran Rahmani**, Ph.D., April 2017.
Dissertation: Scalable Signal Selection for Post-Silicon Debug
Employment: **Head of Engineering**, Asana, USA
7. **Yuanwen Huang**, Ph.D., June 2017.
Dissertation: System-on-Chip Vulnerability Analysis and Mitigation Techniques
Employment: **Software Engineer**, Google, USA
Major Awards: **Best Paper Award**, International Symposium on Quality Electronic Design, 2016.
8. **Farimah Farhamandi**, Ph. D., May 2018.
Dissertation: Formal Verification of Hardware Security and Trust
Employment: **Walden Rhines Endowed Professor for Hardware Security**, University of Florida, USA
Major Awards: **NSF CAREER Award**, 2024; **UF Outstanding Assistant Professor Award**, 2024

9. **Yangdi Lyu**, Ph.D., May 2020.
Dissertation: Test Generation for System-on-Chip Security Validation
Employment: **Assistant Professor**, Hong Kong University of Science and Technology, China
Major Awards: **Best Paper Nomination**, DATE 2019; SIGDA Best Ph.D. Forum Award, ASPDAC 2020
10. **Subodha Charles**, Ph.D., December 2020
Dissertation: Design of Secure and Trustworthy Network-on-Chip Architectures
Employment: **Assistant Professor**, University of Moratuwa, Sri Lanka
Major Awards: HWCoe Outstanding Achievement Award, 2020
11. **Zhixin Pan**, Ph.D., December 2022
Dissertation: Securing Computer Systems against Malicious Attacks using Machine Learning
Employment: **Assistant Professor**, Florida State University, USA
Major Awards: **EDAA Outstanding Dissertation Award**, 2024; Best Paper Nomination, ASPDAC, 2023.
12. **Hasini Witharana**, Ph.D., July 2024
Dissertation: Design of Trustworthy Systems using Security Assertions
Employment: **Security Scientist**, Intel, USA
13. **Daniel Volya**, Ph.D., July 2024
Dissertation: Steering Quantum Computers as Open Quantum Systems
Employment: **Quantum Scientist**, HRL Labs, USA
14. **Aruna Jayasena**, Ph.D., July 2025
Dissertation: Hardware-Firmware Security Co-Verification
15. **Hansika Weerasena**, Ph.D., July 2025
Dissertation: Network-on-Chip Security and Privacy
16. **Sahan Sanjaya**, Ph.D., December 2026 (tentative)
Dissertation: Side-Channel Analysis
17. **Emma Andrews**, Ph.D., December 2026 (tentative)
Dissertation: Quantum AI
18. **Dakshina Tharindu**, Ph.D., December 2029 (tentative)
Dissertation: Trustworthy AI Hardware
19. **Dumindu Bandara**, Ph.D., December 2029 (tentative)
Dissertation: Semantic Transfer

M.S. ADVISEES (Chair)

1. **Sudhi Proch**, M.S., April 2014.
Thesis: Directed Test Generation for Hybrid Systems
Employment: **AMS Verification Lead**, Texas Instruments, USA.
2. **Prateek Thakyal**, M.S., April 2014.
Thesis: Layout-aware Signal Selection for Post-Silicon Debug
Employment: Intel, USA.
3. **Seok-won Seong**, M.S., March 2006.
Thesis: Dictionary-Based Code Compression Techniques using Bitmasks
Employment: **Senior Engineer**, Innovium Inc, USA.

4. **Chetan Murthy**, M.S., December 2008.

Thesis: Decoding-Aware Compression Techniques for Reconfigurable Systems

Employment: Principal Engineer, Juniper Networks, USA.

5. **Kartik Shrivastava**, M.S., August 2010.

Thesis: Code Compression and Encryption in Embedded Systems

Employment: ASIC Engineer, NVIDIA, Bangalore, India.

UNDERGRADUATE HONORS THESIS (Chair)

1. Lydia Chung, Design and Validation of Hardware Cryptographic Modules, spring 2025.
2. Zachery Utt, Quantum Measurement Discrimination using Cumulative Distribution Functions, spring 2023
3. Miranda Overstreet, Robustness Metrics for Evasion Attacks on Neural Networks, spring 2020
4. Jennifer Sheldon, Malware Detection Using Hardware Trace Analysis, spring 2020
5. Jonathan Cruz, Hardware Trojan Detection using ATPG and Model Checking, spring 2017
6. David Nash, Use of Similarity in Dictionary Selection for Bitmask-based Code Compression, fall 2007

UNDERGRADUATE RESEARCH ADVISING (Chair)

1. Jorge Ramirez, Undergraduate Engineering Research, spring 2025.
2. Oscar Rodas, Undergraduate Engineering Research, fall 2024 – spring 2025.
3. Matthew Randall, Undergraduate Engineering Research, fall 2024 – spring 2025.
4. Andrey Nikitin, NSF Research Experience for Undergraduates (REU), fall 2023 – summer 2024.
5. Xiaoguo Jia, NSF Research Experience for Undergraduates (REU), summer 2024 – fall 2024.
6. Edward Guthrie, NSF Research Experience for Undergraduates (REU), summer 2024.
7. Diego Santos Gonzalez, NSF Research Experience for Undergraduates (REU), summer 2024.
8. Emmett Kogan, NSF Research Experience for Undergraduates (REU), summer 2023.
9. Richard Bachmann, NSF Research Experience for Undergraduates (REU), spring 2023 – fall 2023.
10. Lydia Chung, NSF Research Experience for Undergraduates (REU), fall 2022 – fall 2024.
11. Laura Chang, NSF Research Experience for Undergraduates (REU), summer 2022 – spring 2024.
12. Zachery Utt, NSF Research Experience for Undergraduates (REU), spring 2022 – spring 2023.
13. Christina Kohlbeck, NSF Research Experience for Undergraduates (REU), spring 2022.
14. Dylan Ferris, NSF Research Experience for Undergraduates (REU), spring 2021 – summer 2022.
15. Nathaniel Strand, NSF Research Experience for Undergraduates (REU), spring 2021 – fall 2021.
16. Andrew Whigham, NSF Research Experience for Undergraduates (REU), spring 2020 – fall 2021.
17. Rohil Tuli, NSF Research Experience for Undergraduates (REU), spring 2020 – fall 2021.
18. Courtney Cross, NSF Research Experience for Undergraduates (REU), Spring 2021 (OPS summer 2021).
19. Irelis Suarez, NSF Research Experience for Undergraduates (REU), Fall 2020.
20. Stephen Butler, NSF Research Experience for Undergraduates (REU), spring 2018 – spring 2019, fall 2020.

21. Maxwell Rosenzweig, NSF Research Experience for Undergraduates (REU), summer 2020 – current.
22. Jennifer Sheldon, NSF Research Experience for Undergraduates (REU), spring 2020.
23. Miranda Overstreet, NSF Research Experience for Undergraduates (REU), summer 2019 – spring 2020.
24. Megan Logan, NSF Research Experience for Undergraduates (REU), spring 2018 – spring 2019.
25. Meredith Agens, NSF Research Experience for Undergraduates (REU), spring 2018.
26. Amy DeVries, NSF Research Experience for Undergraduates (REU), fall 2017.
27. Alexander Rumak, NSF Research Experience for Undergraduates (REU), fall 2017.
28. Nathan Barnavon, NSF Research Experience for Undergraduates (REU), fall 2017.
29. Nikhil Venkatesh, NSF Research Experience for Undergraduates (REU), fall 2017 – spring 2018.
30. John Barta, NSF Research Experience for Undergraduates (REU), spring 2017.
31. Kevin Barta, NSF Research Experience for Undergraduates (REU), spring 2017.
32. James Safko, NSF Research Experience for Undergraduates (REU), spring 2017.
33. John Zoldos, NSF Research Experience for Undergraduates (REU), spring 2017.
34. Lisbeth Cardoso, NSF Research Experience for Undergraduates (REU), spring 2016 – fall 2016.
35. Jonathan Cruz, NSF Research Experience for Undergraduates (REU), spring 2016 – spring 2017.
36. Mai Tran, NSF Research Experience for Undergraduates (REU), 2016.
37. Ryan Blanchard, NSF Research Experience for Undergraduates (REU), spring 2016 – fall 2016.
38. Rachel Johnson, NSF Research Experience for Undergraduates (REU), fall 2014 – summer 2015.
39. Emre Ozgener, NSF Research Experience for Undergraduates (REU), spring 2015 – spring 2016.
40. Leslie Richardson, Research Experience for Undergraduates (REU), 2015.
41. David Weinberg, Undergraduate Research, spring 2012.
42. Leon Rogers, NSF Research Experience for Undergraduates (REU), summer 2011.
43. Cumpase Lawrence III, NSF Research Experience for Undergraduates (REU), summer 2009.
44. Cris Rivero, NSF Research Experience for Undergraduates (REU), summer 2008.
45. David Nash, Honors Thesis, fall 2007.

UNIVERSITY MINORITY MENTOR PROGRAM (Mentor)

1. Carolina Chau, Intended Major in English, 2014-2015.
2. Niel Wingfield, Intended Major in Computer Engineering, 2014-2015.
3. Pavel Blinov, Intended Major in Computer Engineering, 2013-2014.
4. Sageetha Matchanikal, Intended Major in Computer Science, 2013-2014.
5. Rainer Ledesma, Intended Major in Computer Science, 2012-2013.
6. James Birdsong, Intended Major in Computer Engineering, 2012-2013.
7. Daniel Rodriguez, Intended Major in Biochemistry, 2011-2012.

8. Catherine Phan, Intended Major in Biochemistry, 2011-2012.
9. Leanne Dumeny, Intended Major in Biochemistry, 2011-2012.
10. Danielle Everett, Intended Major in Computer Science, College of Engineering, 2010 – 2011.
11. Arthriya Sukswan, Intended Major in Civil Engineering, College of Engineering, 2010 – 2011.
12. Lazaro Sanchez, Intended Major in Computer Engineering, College of Engineering, 2009 – 2010.
13. Jenilyn Enriquez, Intended Major in Computer Engineering, College of Engineering, 2009 – 2010.
14. Jackie Campuzano, Intended Major in Decision and Information Science, College of Business, 2008– 09.
15. Josue Mazariegos, Intended Major in Computer Engineering, College of Engineering, 2008 – 2009.

UNIVERSITY/DEPARTMENTAL SERVICES

University-Level Services

1. Member, Shared Infrastructure Advisory Committee, UF Information Technology, 2011 – 2012.
2. Mentor, University Minority Mentor Program (UMMP), 2008 – 2011.

College-Level Services

1. Chair, HWCOE Honors and Awards Committee, 2021 – 2022.
2. Member, HWCOE Honors and Awards Committee, 2015 – 2021.
3. Steering Committee Member, Interdisciplinary Strategic Planning (Energy), 2009 – 2010
4. Member, Computer Engineering (CpE) Curriculum Committee, 2013 – 2014.
5. Chair, ABET Committee (Computer Engineering), 2013-2015.

Departmental Services

1. Chair, CISE Faculty Recruitment Committee, 2022 – 2024.
2. Chair, Instructional Faculty Search Committee, 2023 – 2024.
3. Chair, CISE Scholarships and Awards Committee, 2015 – 2022.
4. Member, CISE Steering Committee, 2019-2021.
5. Member, CISE Faculty Search Committee, 2021-2022.
6. Member, Graduate Admissions Committee, 2005-2011, 2015-2019.
7. Chair, CISE ABET Coordination Committee, 2013 – 2014.
3. Member, CISE Curriculum Committee, 2013 – 2014.
4. Member, CISE Scholarships and Awards Committee, 2005-2011.
5. Member, CISE Colloquium Committee, 2005-2011.
6. CISE Commencement Representative, 2004-2006, 2022-2023.

SERVICE TO SCHOOLS

1. **Judge**, Florida Junior Science, Engineering, and Humanities Symposium, January 30, 2017.
2. **Judge**, Florida Junior Science, Engineering, and Humanities Symposium, January 26, 2015.
3. **Judge**, Alachua Regional Science and Engineering Fair, 2010, 2012.
4. **Judge**, Ft. Clarke Middle School Science Fair, December 07, 2011.

COURSES TAUGHT

University of Florida, USA

Introduction to Computer Organization	CDA 3101 (undergraduate core course)	2011 – 2022
Computer Architecture Principles	CDA 5155 (graduate core course)	2005 – 2025
Computer Architecture	CDA 4102 (undergraduate elective)	2005 – 2025
Embedded Systems	CDA 5636 (graduate elective)	2006 – 2025
Embedded Systems	CDA 4630 (undergraduate elective)	2006 – 2025
Hardware Modeling and Verification	CIS 6930 (graduate special topics)	2005

Indian Institute of Science, Bangalore, India

Embedded Systems: Theory, Modeling and Verification	Graduate core course	2006
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SUMMARY OF RESEARCH FUNDING

Title of Grant	Agency	Role	Duration	Total Funding	My Portion
Few-shot In-context Learning for Robust Semantic Transfer Using Multi-modal Foundation Models and Formal Methods	DARPA	PI	08/24 – 07/26	\$1,980,000	\$564,664
Symbolic and Statistical Evaluation of Firmware Security Vulnerabilities	SRC	PI	01/25 – 12/27	\$315,000	\$315,000
Automated Data Augmentation for Deflating Data Bias	SRC	PI	01/23 – 12/25	\$255,000	\$255,000
Compositional Security Verification of Trusted Execution Environments	SRC	PI	10/22 – 09/25	\$270,000	\$270,000
Measurement-induced Steering of Variational Quantum Algorithms	DARPA	PI	01/24 – 12/24	\$215,162	\$215,162
Automatic Implementation of Secure Silicon	DARPA	co-PI	01/20 – 09/24	\$7,828,268	\$1,200,671
Design-for-Debug Architecture for Post-Silicon Security Validation (including supplements)	NSF	PI	10/19 – 9/24	\$597,727	\$597,727
Trustworthy System-on-Chip Design using Secure On-Chip Communication Architecture	NSF	PI	10/19 – 9/24	\$579,970	\$579,970
Scalable Validation of System-on-Chip Vulnerabilities using Security Assertions	SRC	PI	01/20 – 12/22	\$255,000	\$255,000
Effective Utilization of Assertions for SoC Trust Validation	Edaptive	PI	01/20-09/21	\$425,000	\$425,000
MEST: MicroElectronics Security Training	AFOSR	co-PI	04/19 – 04/21	\$905,155	\$27,580
Defending against Adversarial Attacks on Deep Learning Systems	FC2	PI	01/19 – 12/19	\$75,000	\$37,500
Test Generation for Side Channel Analysis	Raytheon	PI	01/18 – 12/18	\$100,000	\$55,000

SoC Verification using Security Assertions	Cisco	PI	05/18 – 04/19	\$100,000	\$100,000
UF Informatics Institute Fellowship	UFII	PI	08/16 – 07/18	\$31,899	\$31,899
Robust Authentication of Embedded Systems with Intrinsic Identifiers	Harris	PI	01/16 – 12/16	\$40,000	\$20,000
Verification of IP Security and Trust	Cisco	PI	01/16 – 12/17	\$200,000	\$105,000
GAANN: Computer Systems Security	ED	PI	10/15 – 09/18	\$590,556	\$295,278
Dynamic Reconfiguration for Adaptive Computing in Heterogeneous SoCs	NSF	PI	10/15 – 09/18	\$499,710	\$260,000
IBM Faculty Award	IBM	PI	10/15 – 09/17	\$25,000	\$25,000
DURIP: Developing Research Capability in Cyber-Physical Systems	ARO	co-PI	08/15 – 07/16	\$199,919	\$40,000
IPTrust: A Comprehensive Framework for IP Integrity Validation	NSF	PI	10/14 – 09/17	\$349,333	\$146,000
IPTrust: A Comprehensive Framework for IP Integrity Validation	SRC	PI	10/14 – 09/17	\$161,667	\$75,000
Automated Techniques for Efficient Post-Silicon Validation and Debug	NSF	PI	08/12 – 07/16	\$474,000	\$474,000
Automated Techniques for Post-Silicon Validation and Debug	Intel	PI	05/11 – 05/12	\$35,000	\$35,000
Multi-Element & Multi-Objective Optimization for Task Allocation in Multicore Processors	NSF	co-PI	08/09 – 07/13	\$270,000	\$104,917
Lossless Data Compression and Decompression in Embedded Systems	NSF	PI	08/09 – 07/12	\$100,000	\$100,000
A Multi-Objective Optimization Approach for Allocating Tasks to Multicore Processors	SRC	co-PI	08/09 – 07/12	\$30,000	\$15,000
New Directions for Functional Verification of Multicore Architectures	NSF	PI	06/08 – 05/14	\$400,000	\$400,000
SystemC Transaction Level Modeling for Design and Validation of SoCs	Intel	PI	11/06 – 08/09	\$120,000	\$120,000
TOTAL				\$17,428,366	\$7,145,368

NSF: National Science Foundation

ED: US Department of Education

UFII: UF Informatics Institute

FC2: Florida Center for Cybersecurity

DARPA: Defense Advanced Research Projects Agency

SRC: Semiconductor Research Corporation

Intel: Intel Corporation

Harris: Harris Endowment Fund

AFOSR: Air Force Office of Scientific Research

ARO: Army Research Office

IBM: IBM Corporation

Cisco: Cisco Systems