

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DELTA ELECTRONICS, INC.
Petitioners,

v.

VICOR CORPORATION
Patent Owner

Case IPR2024-00134

U.S. Patent No. 10,199,950

PETITION FOR *INTER PARTES* REVIEW

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	OVERVIEW OF CHALLENGE AND RELIEF REQUESTED	2
A.	37 C.F.R. §42.104(b)(1): Claims for Which IPR Is Requested	2
B.	37 C.F.R. §42.104(b)(2): Grounds for Challenge	2
C.	37 C.F.R. §42.104(b)(3): Claim Construction	4
D.	37 C.F.R. §42.104(b)(4): How the Claims Are Unpatentable	4
E.	37 C.F.R. §42.104(b)(5): Evidence Supporting Challenge	4
III.	OVERVIEW OF THE '950 PATENT	5
A.	Specification and Claims	5
B.	Summary of the Prosecution History	6
C.	Person of Ordinary Skill In The Art	7
IV.	OVERVIEW OF THE PRIOR ART	7
A.	Huang (Ex. 1005)	7
B.	Liu (Ex. 1006)	10
C.	The '481 Patent (Ex. 1007)	12
D.	Lee (Ex. 1008)	15
V.	SPECIFIC GROUNDS FOR PETITION UNDER 37 C.F.R. § 42.104(B)	16
A.	Ground I: Claims 1, 5-7, 9, 13-16, and 19, 21-40 Are Obvious Over Huang	16
1.	Claim 1	16
2.	Claim 5	25
3.	Claim 6	31
4.	Claim 7	31
5.	Claim 9	32

6.	Claim 13	32
7.	Claim 14	32
8.	Claim 15	33
9.	Claim 16	33
10.	Claim 19	34
11.	Claim 21	34
12.	Claim 22	34
13.	Claim 23	36
14.	Claim 24	36
15.	Claim 25	36
16.	Claim 26	38
17.	Claim 27	38
18.	Claim 28	38
19.	Claim 29	39
20.	Claim 30	39
21.	Claim 31	39
22.	Claim 32	40
23.	Claim 33	41
24.	Claim 34	41
25.	Claim 35	41
26.	Claim 36	41
27.	Claim 37	42
28.	Claim 38	42
29.	Claim 39	44
30.	Claim 40	45
B.	Ground II: Claims 5, 13, 21, 25-27, and 34 Are Obvious Over Huang In View Of The '481 Patent	45
1.	Motivation to Combine	45
2.	Claim 5	47
3.	Claim 13	48
4.	Claim 21	49
5.	Claim 25	49
6.	Claim 26	49
7.	Claim 27	49
8.	Claim 34	49
C.	Grounds III and IV: Claims 1, 5-7, 14-16, 19, and 21-40 Are Obvious Over Huang, Alone Or In Combination With The '481 Patent, In View Of Lee	49

Petition for *Inter Partes* Review of U.S. Patent No. 10,199,950

1.	Motivation to Combine	49
2.	Claim 1	53
3.	Claim 5	56
4.	Claim 6	57
5.	Claim 7	57
6.	Claim 14	58
7.	Claim 15	58
8.	Claim 16	58
9.	Claim 19	59
10.	Claim 21	59
11.	Claim 22	59
12.	Claim 23	60
13.	Claim 24	60
14.	Claims 25-28	60
15.	Claim 29	60
16.	Claim 30	61
17.	Claim 31	61
18.	Claim 32	61
19.	Claim 33	62
20.	Claims 34-39	62
21.	Claim 40	62
D.	Ground V: Claims 1, 2, 6-10, 14-17, 19, 22-33, 35-37, and 39-40 Are Obvious Over Liu	63
1.	Claim 1	63
2.	Claim 2	75
3.	Claim 6	76
4.	Claim 7	76
5.	Claim 8	76
6.	Claim 9	77
7.	Claim 10	78
8.	Claim 14	78
9.	Claim 15	78
10.	Claim 16	78
11.	Claim 17	78
12.	Claim 19	79
13.	Claim 22	79
14.	Claim 23	83
15.	Claim 24	83

16.	Claim 25	83
17.	Claim 26	87
18.	Claim 27	87
19.	Claim 28	87
20.	Claim 29	87
21.	Claim 30	88
22.	Claim 31	88
23.	Claim 32	89
24.	Claim 33	89
25.	Claim 35	90
26.	Claim 36	90
27.	Claim 37	90
28.	Claim 39	90
29.	Claim 40	90
E.	Ground VI: Claims 1, 2, 6-8, 10, 14-17, 19, 22-33, 35-37, and 39-40 Are Obvious Over Liu In View Of Lee	90
1.	Motivation to Combine	90
2.	Claim 1	93
3.	Claim 2	97
4.	Claim 6	98
5.	Claim 7	98
6.	Claim 8 and 10	99
7.	Claim 14	99
8.	Claim 15	99
9.	Claim 16	99
10.	Claim 17	100
11.	Claim 19	100
12.	Claim 22	100
13.	Claim 23	100
14.	Claim 24	101
15.	Claims 25-28	101
16.	Claim 29	101
17.	Claim 30	101
18.	Claim 31	102
19.	Claim 32	102
20.	Claim 33	103
21.	Claims 35-37, 39	103
22.	Claim 40	103

VI.	SECONDARY CONSIDERATIONS	104
VII.	NO JUSTIFICATION FOR DISCRETIONARY DENIAL	104
VIII.	MANDATORY NOTICES	106
A.	Real Party in Interest Under 37 C.F.R. § 42.8(b)(1).....	106
B.	Related Matters.....	107
C.	Lead and Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)	107
IX.	PAYMENT OF FEES UNDER 37 C.F.R. § 42.103	109
X.	GROUND FOR STANDING UNDER 37 C.F.R. § 42.104(A)	109
XI.	CONCLUSION.....	110

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>Apple Inc. v. Fintiv, Inc.</i> , IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020)	104, 105, 106
<i>Certain Power Converter Modules and Computing Systems Containing the Same</i> , Inv. No. 337-TA-1370, USITC Order No. 8 (Sep. 25, 2023)	105, 107
<i>CommScope Techs. LLC v. Dali Wireless, Inc.</i> , IPR2022-01242, Paper 23 (Feb. 27, 2023)	105
<i>Roku, Inc. v. Universal Electronics Inc.</i> , IPR2021-00263, Paper 19 (P.T.A.B. Feb. 8, 2023)	104
<i>Vicor Corp. v. Delta Electronics, Inc.</i> , 2:23-CV-00323-JRG-RSP, Dkt. 35 (E.D. Tex. Aug. 22, 2023)	105
<i>Vicor Corporation v. Delta Electronics, Inc. et al.</i> , 2-23-cv-00323 (E.D. Tex.)	107
Other Authorities	
Director Vidal, Memorandum, “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation,” 5–7 (June 21, 2022)	104, 106

LIST OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 10,199,950
1002	Certified File History of U.S. Patent No. 10,199,950
1003	Declaration of Douglas Hopkins
1004	<i>Curriculum Vitae</i> of Douglas Hopkins
1005	Daocheng Huang et al., <i>Novel Non-isolated LLC Resonant Converters</i> , 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC) (Feb. 2012) (“Huang”)
1006	U.S. Patent No. 7,307,857 to Yan-Fei Liu and Sheng Ye (“Liu”)
1007	U.S. Patent No. 9,166,481 to Patrizio Vinciarelli and Sergey Luzanov (“the ’481 Patent”)
1008	Fred C. Lee et al., <i>Design Challenges for Distributed Power Systems</i> , Asian Power Electronics Journal, Vol. 1, No. 1 (Aug. 2007)
1009	Declaration of Dr. Sylvia Hall-Ellis, Ph.D.
1010	Excerpt from Vicor’s October 16, 2023 Supplemental Response to Respondents’ Interrogatory No. 10, in Inv. No. 337-1370, <i>Certain Power Convert Modules and Computing Systems Containing the Same</i>

Petitioner Delta Electronics, Inc. (“Delta” or “Petitioner”) requests *inter partes* review (“IPR”) of claims 1, 2, 5-10, 13-17, 19, and 21-40 (the “Challenged Claims”) of U.S. Patent No. 10,199,950 (Ex. 1001, “the ’950 Patent”).

I. INTRODUCTION

The ’950 Patent claims nothing more than a power converter comprising a non-isolated LLC resonant converter. Such systems were known in the art at the time of the purported invention, as evidenced by the explicit disclosures in the Huang and Liu prior art references discussed below. Despite the claimed technology being well-known, neither Huang nor Liu were of record and the ’950 Patent sailed through prosecution with only a single office action, despite 10 requests for continued examination/amendments after final action and 5 claim amendments after the first notice of allowance.

The ’950 Patent issued from an application filed on July 2, 2013. Ex. 1001, Cover. But non-isolated LLC resonant converters were known in the art long before that date. Huang disclosed a variety of full- and half-bridge non-isolated LLC resonant converters as early as March 9, 2012. Ex. 1005; Ex. 1009, ¶¶39-45, 48. Even earlier than that, in December 2007, Liu disclosed dozens of DC-DC converters, many of them non-isolated and/or resonant. *See generally* Ex. 1006. Both Huang and Liu derived their non-isolated converters from existing isolated converters by connecting the primary side and secondary side circuits of the

isolated converters in series: just as the '950 Patent claims. Yet Vicor filed its patent over a year after Huang and almost *seven* years after Liu, claiming nothing more than an isolated converter made non-isolated by connecting its primary side and secondary side circuits in series—just as Liu and Huang describe—without disclosing either Huang or Liu, or any of the other references discussed in this Petition, to the Patent Office—despite citing over *twelve hundred* other references. See Ex. 1001, Cover-page 17.

Accordingly, Petitioners respectfully request that *inter partes* review of the '950 Patent be instituted and that claims, 1, 2, 5-10, 13-17, 19, and 21-40 be cancelled as unpatentable pursuant to 35 U.S.C. § 318(b). This Petition demonstrates that there is a reasonable likelihood that at least one of the Challenged Claims is unpatentable as obvious.

II. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

A. 37 C.F.R. §42.104(b)(1): Claims for Which IPR Is Requested

Petitioners challenge the patentability of claims 1, 2, 5-10, 13-17, 19, and 21-40 of the '950 Patent and request that they be cancelled.

B. 37 C.F.R. §42.104(b)(2): Grounds for Challenge

The claims are challenged based on the following references, none of which were considered by the Examiner during prosecution. The '950 Patent is subject to AIA law, as the patent's earliest claimed priority date is July 2, 2013.

- **Huang** - Huang is a conference paper from the 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC) held February 5-9, 2012. It was published by at least March 9, 2012. Ex. 1009, ¶¶39-45, 48. Accordingly, Huang qualifies as prior art under at least 35 U.S.C. §102(a)(1).

- **Liu** - Liu is a U.S. patent filed on August 16, 2006 and issued as U.S. Patent 7,307,857 on December 11, 2007. Accordingly, Huang qualifies as prior art under at least 35 U.S.C. §102(a)(1).

- **The '481 Patent** – The '481 Patent is a U.S. patent filed on March 1, 2013 and issued as U.S. Patent No. 9,166,481 on October 20, 2015. The '481 Patent names as inventors Patrizio Vinciarelli and Sergey Luzanov. Accordingly, the '481 Patent qualifies as prior art under at least 35 U.S.C. §102(a)(2).

- **Lee** – Lee is a paper published in the Asian Power Electronics Journal no later than August 31, 2007. Ex. 1009, ¶¶46-48. Accordingly, Lee qualifies as prior art under at least 35 U.S.C. §102(a)(1).

Petitioners request cancellation of the Challenged Claims as unpatentable under post-AIA 35 U.S.C. §§ 102 and 103. The specific grounds are set forth below and are supported by the declaration of Dr. Douglas Charles Hopkins (Ex. 1003).

Ground	Basis	Claims	Proposed Statutory Rejection
I	§ 103	1, 5-7, 9, 13-16, and 19, 21-	Obvious over Huang

		40	
II	§ 103	5, 13, 21, 25-27, and 34	Obvious over Huang In View Of The '481 Patent
III	§ 103	1, 5-7, 14-16, and 19, 21-40	Obvious over Huang In View Of Lee
IV	§ 103	5, 13, 21, 25-27, and 34	Obvious over Huang In View Of The '481 Patent And Lee
V	§ 103	1, 2, 6-10, 14-17, 19, 22-33, 35-37, and 39-40	Obvious over Liu
VI	§ 103	1, 2, 6-8, 10, 14-17, 19, 22-33, 35-37, and 39-40	Obvious over Liu in view of Lee

C. 37 C.F.R. §42.104(b)(3): Claim Construction

For the purposes of this Petition, all terms should be given their plain and ordinary meaning. 37 C.F.R. §42.104(b)(3). Petitioner reserves the right to later address the construction of any terms, if necessary.

D. 37 C.F.R. §42.104(b)(4): How the Claims Are Unpatentable

A detailed explanation of how the Challenged Claims are unpatentable is provided below in Section V.

E. 37 C.F.R. §42.104(b)(5): Evidence Supporting Challenge

A list of exhibits is provided at the beginning of this Petition. The relevance of this evidence and the specific portions supporting the challenge are provided

below in Section V. Petitioners submit the declaration of Dr. Douglas Charles Hopkins (Ex. 1003) in support of this Petition. 37 C.F.R. §1.68.

III. OVERVIEW OF THE '950 PATENT

The '950 Patent issued on February 5, 2019 from U.S. Application No. 13/933,252, filed on July 12, 2013. Ex. 1001, Cover. The '950 Patent only claims priority to its own application. *Id.*

A. Specification and Claims

The '950 Patent describes and claims DC-DC power/bus converters including “an input circuit and output circuit” wherein the converter “is adapted to convert power from the input circuit to the output circuit at a substantially fixed voltage transformation ratio” and wherein the “input circuit and at least a portion of the output circuit are connected in series across the source.” Ex. 1001, Abstract. The converter comprises an inductive component and one or more power switches in either the input circuit, the output circuit, or both. *See, e.g., id.*, claim 1. A charge flowing in the inductive component charges and discharges capacitances in the converter so that a voltage across one or more of the switches is reduced prior to turning on said one or more switches. *Id.* Also claimed is a power distribution bus containing such a converter and “a plurality of regulators” connected to the output of the converter and the input of a load. *Id.* The '950 Patent does not identify or claim to solve any particular problem in the art, and discusses nothing

more than obvious and well-known DC-DC power/bus converter functionality and structure. *See* Ex. 1003, ¶34.

B. Summary of the Prosecution History

Application No. 13/933,252 was filed on July 12, 2013. Ex. 1002, Cover. The pending claims were rejected once, as obvious and anticipated by U.S. Patent Application No. 2008/0211304 to Farrington et al. (“Farrington”). *Id.*, 77-83. The applicant distinguished the pending claims on the basis that Farrington did not disclose an “input of the bus converter and at least a portion of the output circuit of the bus converter are connected in series across the source.” *Id.*, 99-100. Instead, Farrington disclosed an output circuit that is galvanically isolated from the source because “the input circuit is connected to the output circuit via magnetic coupling between the primary winding 309 and the secondary windings 210 and 211 of the isolation transformer.” *Id.*, 100. On the same basis, the applicant argued that Farrington did not disclose “the primary and secondary transformer winding are galvanically connected in series, wherein the bus converter is configured to provide power to a power distribution bus that is not galvanically isolated from the source.” *Id.*, 103.

The claims were thereafter allowed. *See* Ex. 1002, 114. The applicant filed numerous requests for continued examination/amendments after allowance, amending the specification (*id.*, 139-142), adding hundreds of prior art references

Petition for *Inter Partes* Review of U.S. Patent No. 10,199,950

to the record (*id.*, 147-205, 359-421, 588-598, 776-780), and amending existing claims or adding new claims (*id.*, 517-529, 546-555, 561-570, 623-669). Each time the application was allowed without rejection. *Id.*, 298, 450, 539, 558-560, 580-582, 610, 674, 793. The issue notification was finally entered on January 16, 2019, and the '950 Patent issued on February 5, 2019. *Id.*, 811.

C. Person of Ordinary Skill In The Art

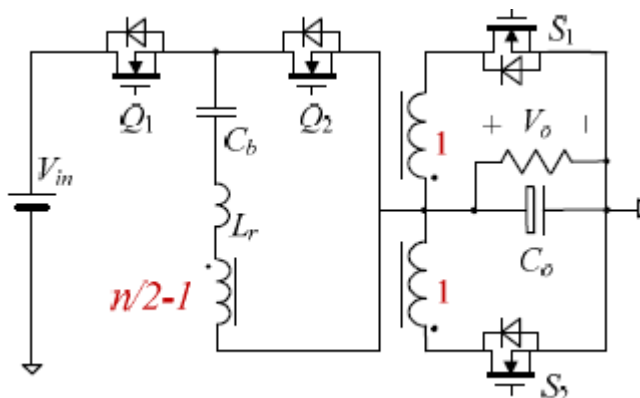
A person of ordinary skill in the art (“POSITA”) at the time of the '950 Patent would have at least a Master’s degree in electrical engineering and two or more years of work experience relating to power electronics and the design of switching power converters, with more experience potentially substituting for education or vice versa. Ex. 1003, ¶29; Ex. 1009, ¶¶35-38; Ex. 1010, 80.

IV. OVERVIEW OF THE PRIOR ART

A. Huang (Ex. 1005)

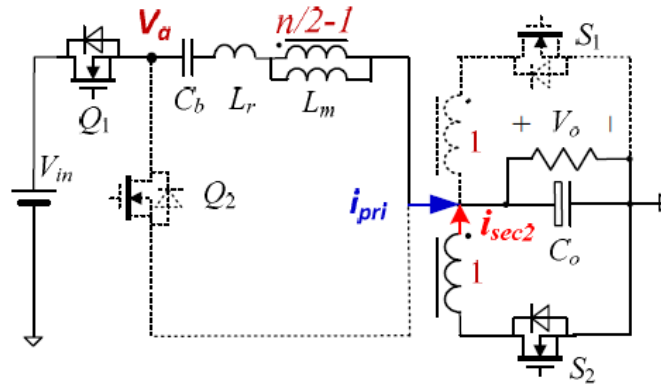
Huang is a conference paper entitled “Novel Non-isolated LLC Resonant Converters.” Ex. 1005. It was published by at least March 9, 2012. Ex. 1009, ¶¶39-45, 48. It was presented at the 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC) in February 2012. None of the named inventors or Patent Owner are listed as co-authors of Huang. Huang proposes “novel non-isolated LLC resonant converters” that can achieve zero voltage switching, reduce the number of turns in the transformer, and reduce the current through the secondary transformer winding. Ex. 1005, 1373.

One of these topologies is a half-bridge, non-isolated resonant converter depicted in Figure 12(b):



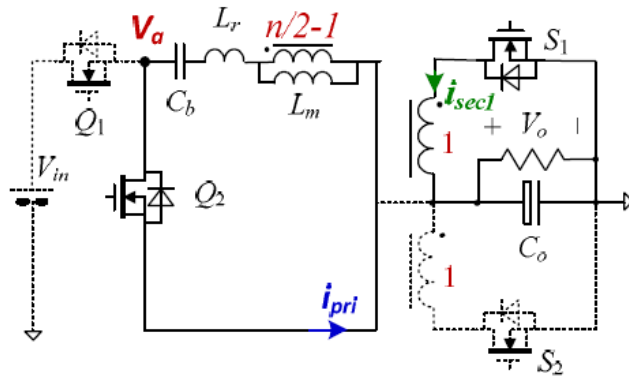
Id., Figure 12(b). Huang's converters are capable of zero-voltage switching. *Id.*, 1373. Zero-voltage switching, in which switches are not turned on/closed until the voltage across the body diode of the switch is zero or near-zero, allows for operation at a higher frequency and higher input voltages without sacrificing efficiency. Ex. 1003, ¶42.

Figures 14(a) and 14(b) depict equivalent circuits for the operation of Huang's Figure 12(b) converter at two different time intervals. *Id.*, 1378. During t_1 to t_2 , the current is delivered from the source to the resonant tank and the transformer (Q_1 is closed/on and Q_2 is open/off).



(a) t_1-t_2

Ex. 1005, Figure 14(a), 1378; Ex. 1003, ¶43. During t_2 to t_3 , the remaining power stored in the resonant tank is transferred to the transformer with current flowing in the opposing direction as in time t_1 to t_2 (Q_1 is open/off and Q_2 is closed/on).



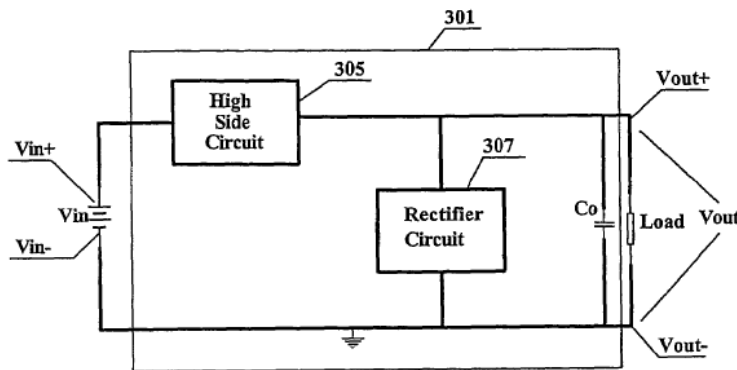
(b) t_2-t_3

Ex. 1005, Figure 14(b), 1378; Ex. 1003, ¶44. Zero-voltage switching occurs between these two time periods as well as directly after t_2 to t_3 . Ex. 1003, ¶45. During zero-voltage switching, current from the LLC tank (which includes the transformer primary winding, inductor L_r , and capacitor C_b) flows through the antiparallel diode of the switch (e.g., Q_2 between t_1 to t_2 and t_2 to t_3 , Q_1 after t_2 to t_3) which causes the voltage across the transistor to drop until it reaches a value close

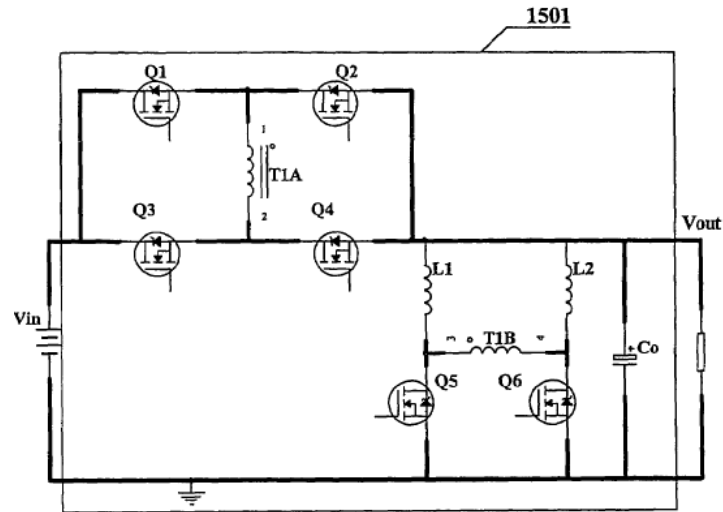
to zero (limited by the small voltage drop of the diode). *Id.* Because this occurs when both gate signals are low, i.e., the switches are both off/open, by the time the circuit transitions from both switches being off to one being on, the voltage across the transistor of the switch to be turned on is close to zero. *Id.*

B. Liu (Ex. 1006)

Liu is a United States patent that was filed on August 16, 2006 and issued on December 11, 2007. Ex. 1006, Cover. Liu claims priority to a provisional application filed on December 9, 2002. *Id.* Liu discloses two high-level converter topologies, one shown in Figure 3 comprising a high-side circuit, rectifier circuit, and output capacitor:

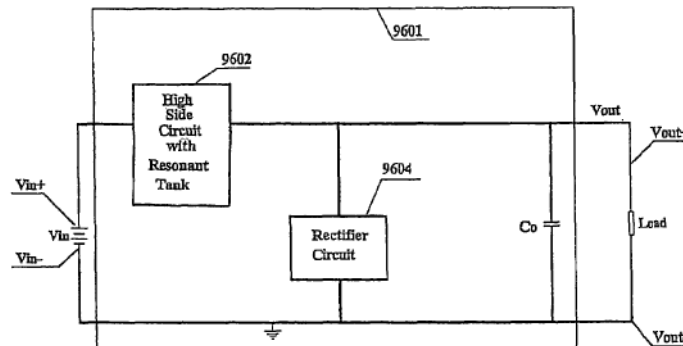


Ex. 1006, Figure 3. Figure 15 is a specific embodiment of the configuration shown in Figure 3, comprising a full-bridge high-side circuit comprising primary switches that control the flow of current through the transformer primary winding and a half-bridge rectifier circuit with two switches controlling the flow of current through the transformer secondary winding and two inductors L1 and L2:



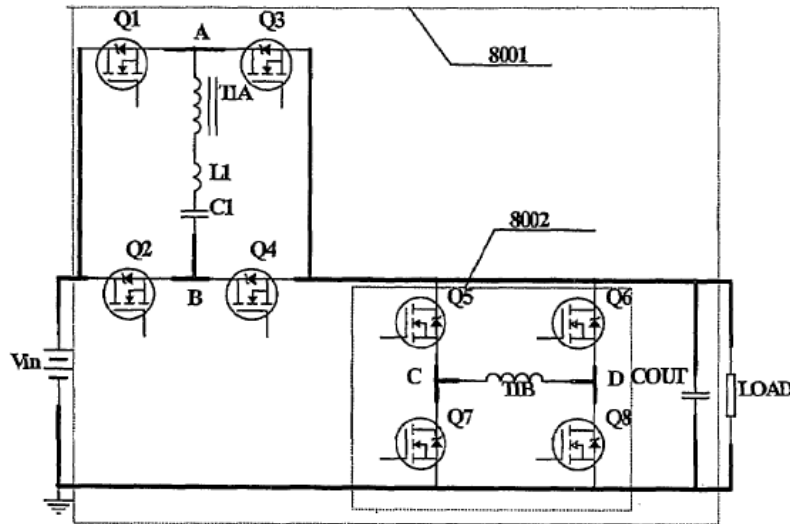
Ex. 1006, Figure 15, 16:16-18:16.

The second topology disclosed by Liu and depicted in Figure 68A is similar to Figure 3 except the high-side circuit includes a resonant tank:



Ex. 1006, Figure 68A. Figure 80 is a specific embodiment of the configuration shown in Figure 68A, comprising a full-bridge high-side circuit with four primary switches that control the flow of current through an LLC series resonant tank including the transformer primary winding T1A, inductor L1, and capacitor C1. *Id.*, Figure 80, 32:53-33:7. It further comprises a full-bridge rectifier circuit with

four primary switches that control the flow of current through the transformer secondary winding T1B. *Id.*



Id., Figure 80

Liu discloses that its converter topologies are advantageously capable of zero voltage switching among other efficiencies. Ex. 1006, 18:21-31, 36:20-33. Zero-voltage switching operates by lowering the voltage across a switch's antiparallel/body diode to zero or near-zero before turning the switch on or closing the switch by, for example, reversing current direction in the transformer windings. Ex. 1003, ¶51.

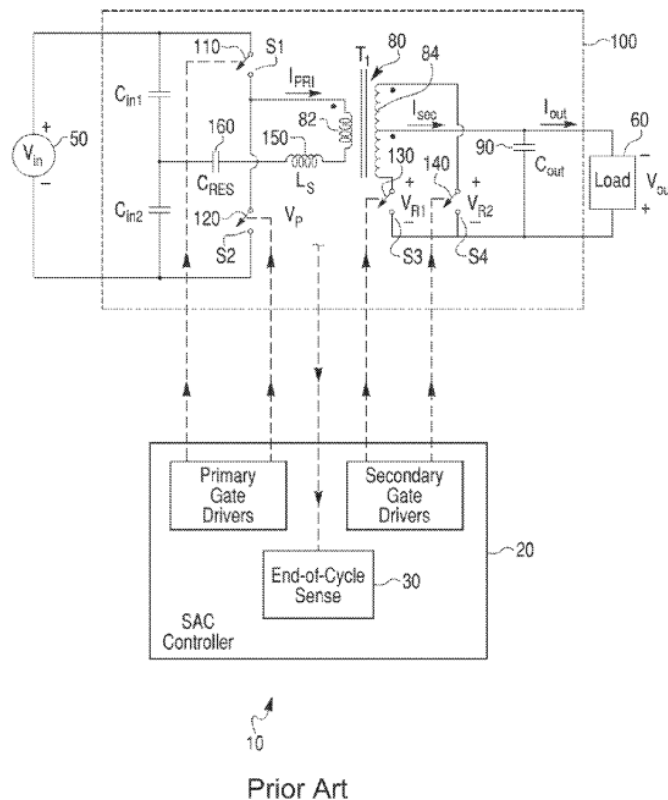
C. The '481 Patent (Ex. 1007)

The '481 Patent relates to a method for “digital control of resonant zero-current and zero-voltage switching resonant power converters.” Ex. 1007, 1:6-9. The specification describes one implementation of the invention as “a method of

synchronously operating a power converter in a series of converter operating cycles includes providing an oscillator for generating clock signals at an oscillator frequency and generating timing control signals for each of a plurality of events based upon the clock signals in a standard converter operating cycle having a standard operating period and frequency. The timing and control signals may turn a primary switch ON and OFF at times when essentially zero voltage is impressed across and essentially zero resonant current is flowing in the primary switch and turn a secondary switch ON and OFF at times when essentially zero current is flowing in and essentially zero voltage is impressed across the secondary switch.” *Id.* 2:26-41.

The '481 Patent explains that resonant power converters with zero-current and zero voltage switching capabilities were known in the art at the time of invention (the '481 Patent was filed on March 14, 2013). *See* Ex. 1007, 1:13-2:7; Figure 1. The '481 Patent claims to have invented a digital controller to replace the prior art controller, though states that the circuitry of the claimed digital controller is “essentially the same as” the prior art controller. *Id.*, 4:29-35. Thus, both the prior art controller and the claimed digital controller “control[] the turning ON and OFF of switches within the power conversion circuitry” to control the timing of power transfer and energy recycling intervals. *Id.*, 1:22-59. “Each converter operating cycle comprises two power transfer intervals of equal length and two

energy recycling intervals of equal length.... Each power transfer interval is substantially equal to one-half of the characteristic period[.]” *Id.*, 1:47-53; *see also id.*, 8:22-26 (normal converter operation may be defined by power transfer intervals being one half of the characteristic resonant period). During a power transfer interval, primary switches (e.g., S1 in the figure below) are closed which causes a flow of resonant current in the transformer primary winding, *i.e.*, power is transferred from the input of the circuit to the output via the transformer. *Id.*, 1:22-47.

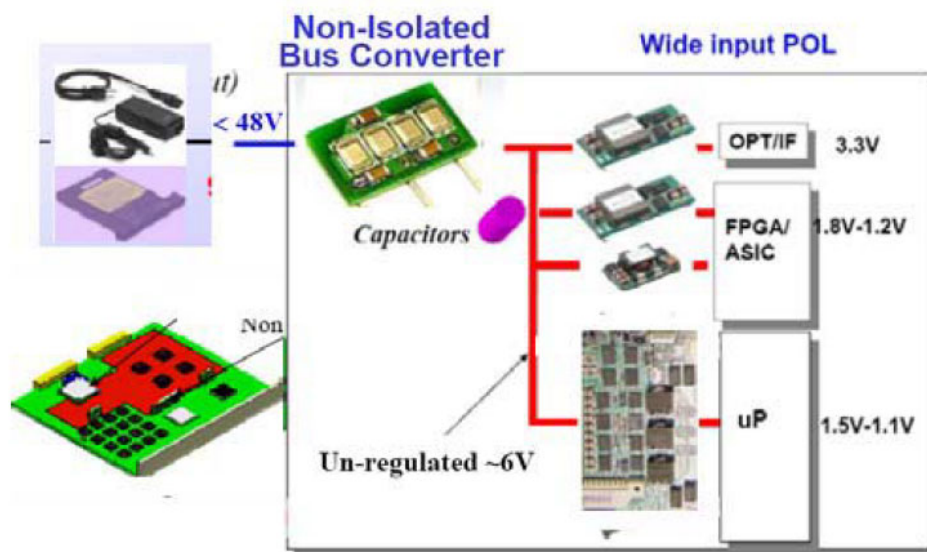


Id., Figure 1.

D. Lee (Ex. 1008)

Lee is an article entitled “Design Challenges for Distributer Power Systems” published in the Asian Power Electronics Journal, Volume 1, No. 1. Ex. 1008, 1. It was published no later than August 31, 2007. Ex. 1009, ¶¶46-48. None of the named inventors or Patent Owner are listed as co-authors of Lee.

Lee discusses technological advancements, challenges, and opportunities for development in distributed power systems. Ex. 1008, 1. One specific proposal is a non-isolated intermediate bus architecture, depicted below. *Id.*, 12, Figure 43. This architecture includes a non-isolated bus converter designed to minimize switching losses and body diode losses at high switching frequencies and increase circuit efficiency. *Id.*, 11-12.



Ex. 1008, Figure 43.

V. SPECIFIC GROUNDS FOR PETITION UNDER 37 C.F.R. § 42.104(B)

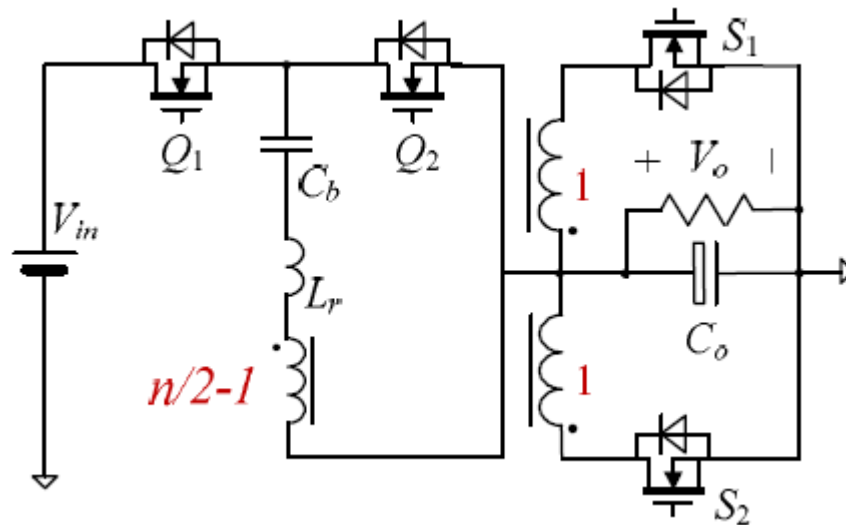
A. Ground I: Claims 1, 5-7, 9, 13-16, and 19, 21-40 Are Obvious Over Huang

1. Claim 1

a. Limitation 1(a)

b. Limitation 1(b)

Huang discloses various non-isolated LLC resonant converters, both full- and half-bridge (e.g., Ex. 1005, Figs. 2, 6, 7, 8, 12), including the half-bridge converter depicted in Figure 12(b):



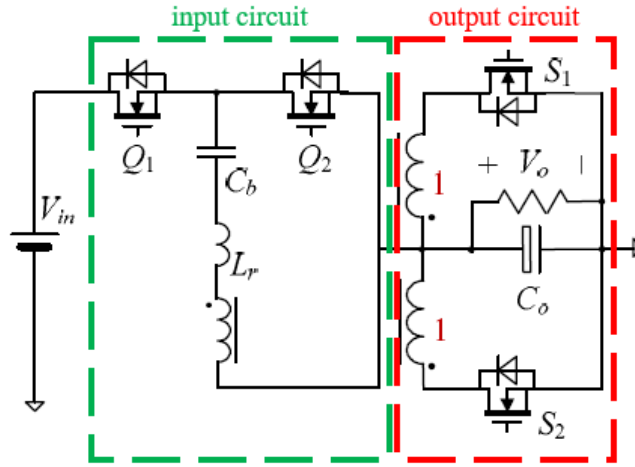
Id., Figure 12(b). Figure 12(b)'s converter "receive[s] power from a power distribution system comprising a source for providing power at a DC source voltage V_S " indicated by " V_{in} " ("voltage in") on the left. Ex. 1003, ¶61. Huang makes clear that this source is a DC source: when explaining the problem to be addressed, Huang notes the benefits and detriments of existing DC-DC converters

and then proposes an alternative solution. Ex. 1005, 1373. The converter prototype made to verify the proposals made in Huang was a DC-DC converter. *Id.*, 1379. DC-DC converters receive and output DC voltage. Ex. 1003, ¶61.

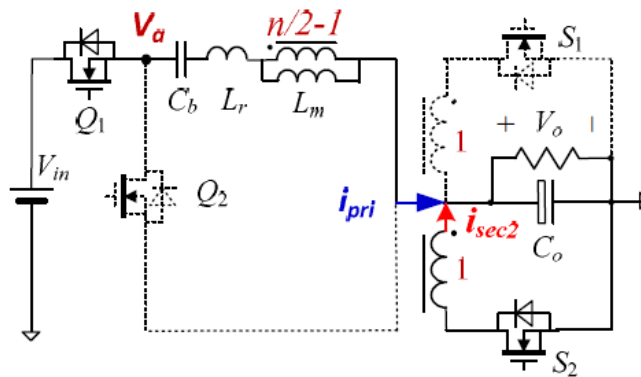
c. Limitation I(c)

As the '950 Patent acknowledges, the Intermediate Bus Architecture (“IBA”) was known in the art at the time of invention. Ex. 1001, 1:13-35 (describing IBA configuration as prior art). The IBA included a bus converter that included, for example, a DC transformer to provide voltage transformation, *e.g.*, a DC-DC converter such as that disclosed by Huang. *Id.*; Ex. 1005, Figure 12(b). A POSITA would have known that a bus converter is or contains a power converter. Ex. 1003, ¶63. A POSITA would also have known, where the input and output of the converter both need to be DC, to use a DC-DC converter such as Huang’s as the bus converter or part of the bus converter because the input to the converter is DC and the electronics downstream from the converter also use DC. *Id.*, ¶64. A POSITA would have also known that, in the case of IBA, the bus converter should both be efficient and low cost. *Id.*, ¶65. Huang’s converter increases efficiency by, for example, achieving zero voltage switching, low turn off loss for switches, reduction in transformer turns, and reduction of current through transformer secondary windings. *See* Ex. 1005, 1373. Huang would thus be an attractive option to a POSITA seeking a high efficiency converter. Ex. 1003, ¶65.

Huang's Figure 12(b) converter converts power from the input circuit to the output circuit, which are indicated in green and red, respectively:



Ex. 1005, Figure 12(b) (annotations added). The input voltage to the input circuit, V_{IN} , is the input voltage to the converter less the output voltage: $V_{in} - V_o$. Ex. 1003, ¶67. This can be seen in Figure 14(a), which depicts an equivalent circuit of Figure 12(b) when switches Q_2 and S_1 are off (open), and Q_1 and S_2 are on (closed):



Ex. 1005, Figure 14(a); Ex. 1003, ¶67. The output circuit then produces an output voltage, V_o , referred to in the claim as V_{OUT} . *Id.*

The power conversion is performed at a substantially fixed voltage transformation ratio that can be represented as $K_{DC}=V_{OUT}/V_{IN}$. Preliminarily, Huang discloses that the switching frequency of its converter may be at the resonant frequency. Ex. 1005, 1378. In LLC converters, the impedance of the resonant tank is zero when the switching frequency is at the resonant frequency. Ex. 1003, ¶68. Because the impedance of the resonant tank is zero, the voltage gain is fixed for all load conditions. *Id.* Thus, the transformation ratio, which is the voltage gain, is fixed and only affected by the transformer turns ratio when the switching frequency is at the resonant frequency. *Id.*; Ex. 1001, 4:57-60 (“The voltage gain or voltage transformation ratio of a system is defined generally herein is the ratio of its output voltage to its input voltage at a specified current such as an output current.”). The transformer turns ratio is physically fixed in the circuit and, therefore, the transformation ratio is likewise fixed. Ex. 1003, ¶68.

This can also be demonstrated mathematically. In the circuit of Figure 12(b), the voltage transformation ratio is $K_{DC} = \frac{V_{OUT}}{V_{IN}} = \frac{V_o}{V_{in}-V_o}$. Ex. 1003, ¶69. The ratio value can be represented in terms of the transformer turns ratio and is therefore fixed because the turns in a transformer are fixed for a circuit. *Id.* Specifically, Huang notes that the transformer turns ratio of the Figure 12(b) circuit, which for clarity will be referred to as K_t herein, is $\frac{(V_{in}/2)-V_o}{V_o}$. Ex. 1005, 1378. Using the

voltage transformation ratio and the transformer turns ratio, we can see that the voltage transformation ratio is equal to $\frac{1}{(2K_t+1)}$.

$$K_t = \frac{(V_{in}/2)-V_o}{V_o}$$

Multiply both sides by two: $2K_t = \frac{V_{in}-2V_o}{V_o}$

Add one to both sides: $2K_t + 1 = \frac{V_{in}-2V_o+V_o}{V_o}$

Simplify: $2K_t + 1 = \frac{V_{in}-V_o}{V_o}$

Transpose: $\frac{1}{2K_t+1} = \frac{V_o}{V_{in}-V_o}$

Substitute: $\frac{1}{2K_t+1} = K_{DC}$

Ex. 1003, ¶70. Therefore, the converter shown in Figure 12(b) of Huang is adapted to convert power from the input circuit to the output circuit at the fixed voltage transformation ratio $\frac{1}{(2k_t+1)}$, where k_t is the transformer turns ratio $\frac{(V_{in}/2)-V_o}{V_o}$. Ex. 1003, ¶71.

d. Limitation I(d)

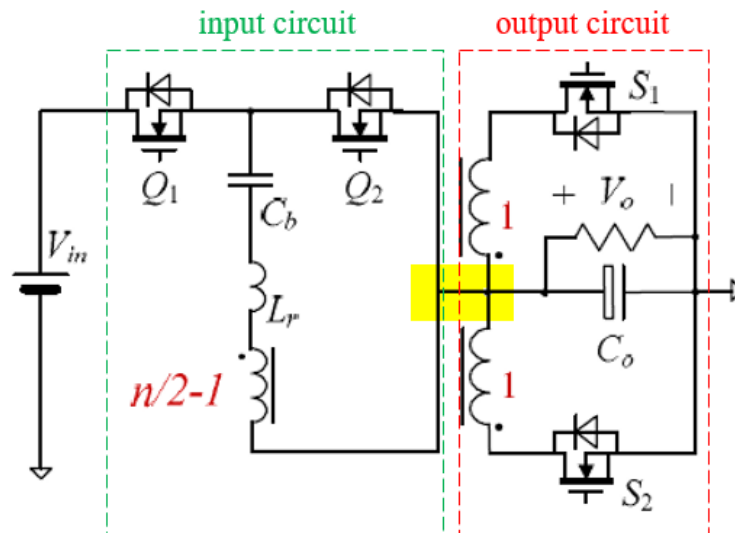
Huang discloses the area of application for its disclosed invention as point-of-load and voltage regulator converters for use in processors. Ex. 1005, 1373. A POSITA would have understood Huang's Figure 12(b)'s output to be connected to a power distribution bus to distribute power from the output circuit, as this is the purpose of such converters. Ex. 1003, ¶72.

e. Limitation 1(e)

The '950 Patent explains that the use of IBA, wherein a bus converter supplies power to one or more down-stream regulators, was known at the time of invention. Ex. 1001, 1:13-35, Figure 1. In this configuration, the input of the regulators is attached to a power distribution bus to which the output of the bus converter is also attached, such that the regulators are receiving power from the output of the bus converter. *Id.* The regulators would then provide regulated power/voltage to their respective loads. *Id.* A POSITA would have further known that regulators would be separated by a distance from the bus converter. Ex. 1003, ¶73.

f. Limitation 1(f)

A series connection between the input circuit and the output circuit is shown in Figure 12(b), highlighted in yellow below.

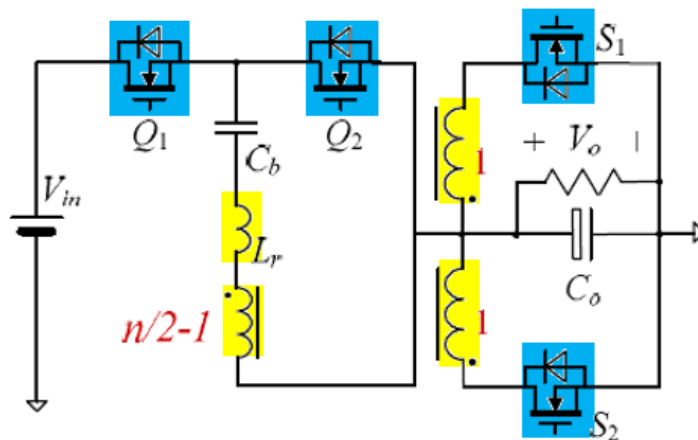


Ex. 1005, Figure 12(b) (annotations added). Galvanic connection refers to whether there is direct electrical charge connection between functional sections of the system, *i.e.*, the input and output circuit. Ex. 1003, ¶75. Because the input circuit and output circuit are serially connected and non-isolated, they are galvanically connected. *Id.*

Further, as discussed above, the voltage V_{IN} applied to the input circuit is $V_{in} - V_o$, where V_{in} is the DC source voltage V_s . In other words, the voltage applied to the input circuit is equal to the DC source voltage V_s less the output voltage V_{OUT} . Ex. 1003, ¶76. Thus, the input voltage V_{IN} is equal to the DC source voltage V_s minus a number N times the output voltage V_{OUT} , where N is exactly 1. *Id.*

g. Limitation I(g)

Huang discloses that both the input circuit and output circuit of the converter depicted in Figure 12(b) have inductive components, namely the resonant inductor (L_r) and the transformer highlighted in yellow in the image below. Huang's input circuit and output circuit also both comprise power switches, highlighted in blue below.

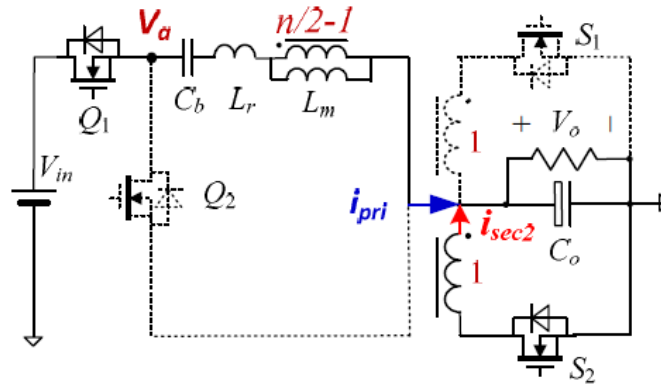


Ex. 1005, Figure 12(b) (annotations added); Ex. 1003, ¶77.

h. Limitation 1(h)

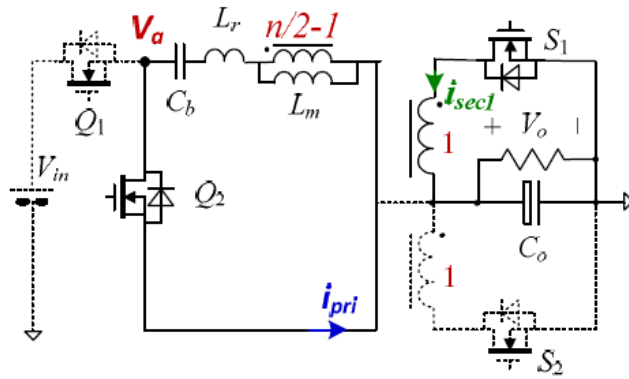
When switching occurs when the current is approximately zero, that is called zero-current switching; when switching occurs when the voltage is low, that is called zero-voltage switching. Ex. 1003, ¶78. As Huang notes, LLC resonant converters, such as the one depicted in Figure 12(b), can achieve both zero-voltage switching and zero-current switching. Ex. 1005, 1373, 1379.

Figures 14(a) and 14(b) depict equivalent circuits for the operation of the converter of Figure 12(b) at two different time intervals. *Id.*, 1378. During t_1 to t_2 , the current is delivered from the source to the resonant tank and the transformer (Q_1 is closed/on and Q_2 is open/off).



(a) t_1-t_2

Ex. 1005, Figure 14(a), 1378; Ex. 1003, ¶79. During t_2 to t_3 , the remaining power stored in the resonant tank is transferred to the transformer with current flowing in the opposing direction as in time t_1 to t_2 (Q_1 is open/off and Q_2 is closed/on).



(b) t_2-t_3

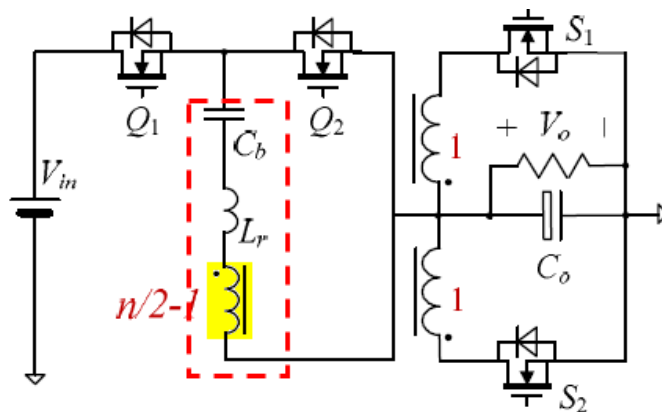
Ex. 1005, Figure 14(b), 1378; Ex. 1003, ¶80. Zero-voltage switching occurs between these two time periods as well as directly after t_2 to t_3 . Ex. 1003, ¶81. During zero-voltage switching, current from the LLC tank (which includes the transformer primary winding) flows through the antiparallel diode of the switch (e.g., Q_2 between t_1 to t_2 and t_2 to t_3 , Q_1 after t_2 to t_3) which causes the voltage across the transistor to drop until it reaches a value close to zero (limited by the

small voltage drop of the diode). *Id.* Because this occurs when both gate signals are low, i.e., the switches are both off/open, by the time the circuit transitions from both switches being off to one being on, the voltage across the transistor is close to zero. *Id.*

2. Claim 5

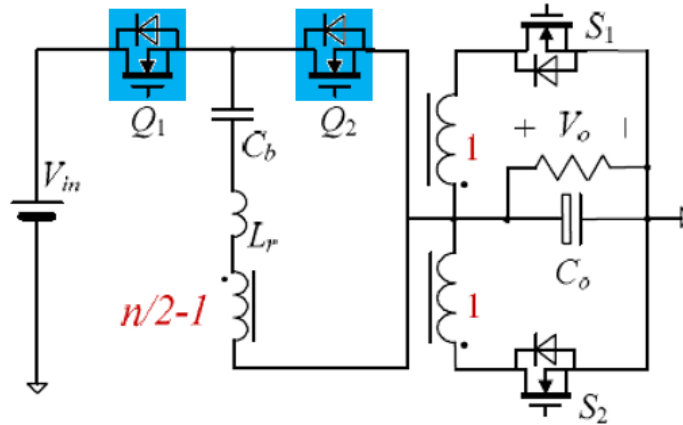
a. *Limitation 5(a)*

Huang renders obvious claim 1. §V.A.1, *supra*. The transformer in Figure 12(b) is highlighted in yellow below, and the resonant circuit of which it is a part is outlined in red:

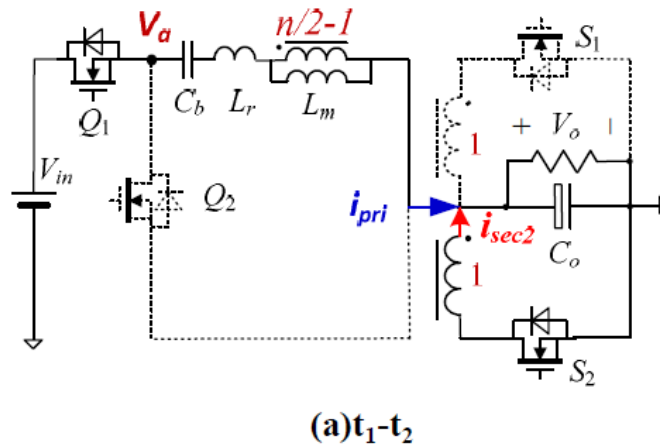


Ex. 1005, Figure 12(b) (annotations added); Ex. 1003, ¶84. Resonant converters, like Figure 12(b), are circuits made up of inductors and capacitors that oscillate at a specific frequency, called the resonant frequency. Ex. 1003, ¶85. Thus, by virtue of disclosing that the converter depicted in Figure 12(b) is an LLC resonant converter, Huang discloses that its resonant circuit has a characteristic resonant frequency and period. *Id.*

The input circuit of the converter depicted in Figure 12(b) comprises two primary switches that are connected to drive the resonant circuit, highlighted blue in the image below.

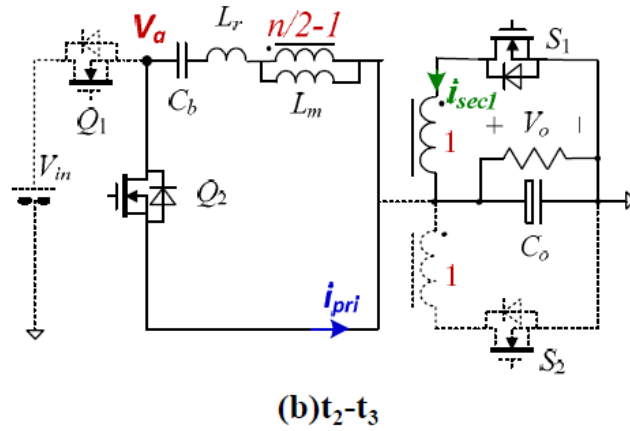


Ex. 1005, Figure 12(b) (annotations added); Ex. 1003, ¶86. As discussed above, the switches drive the resonant circuit: When Q_1 is closed/on and Q_2 is open/off, current is delivered from the source to the resonant tank and the transformer, as shown in Figure 14(a):



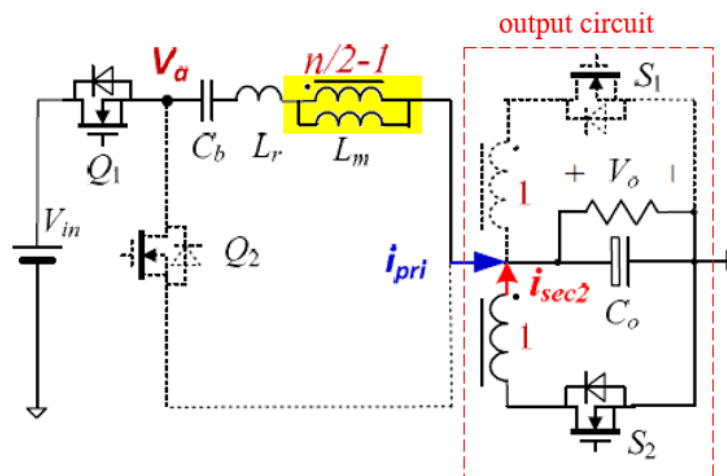
Ex. 1005, Figure 14(a), 1378; Ex. 1003, ¶87. When Q_1 is open/off and Q_2 is closed/on, the remaining power stored in the resonant tank is transferred to the

transformer with current flowing in the opposing direction as when Q_1 is closed/on and Q_2 is open/off, as shown in Figure 14(b).



Ex. 1005, Figure 14(b), 1378; Ex. 1003, ¶88.

As can also be seen in Figure 14(a), where the solid lines indicate active portions of the circuit, the output circuit (outlined with red dashed lines) receives power from the transformer (highlighted in yellow):

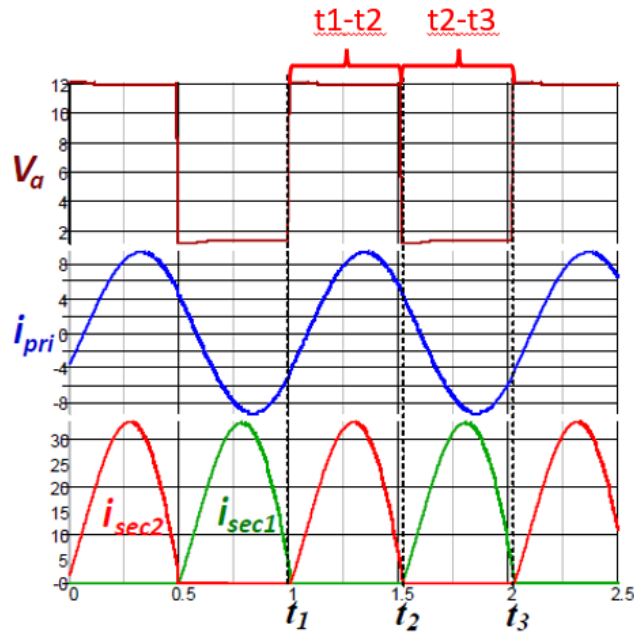


Ex. 1005, Figure 14(a), 1378; Ex. 1003, ¶89.

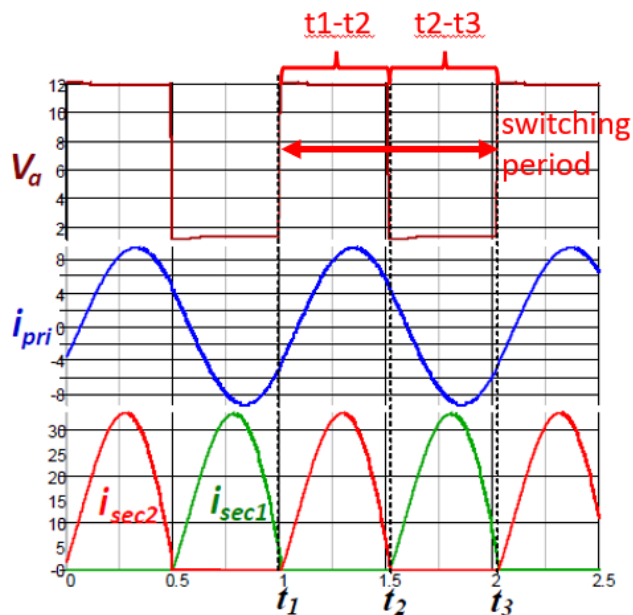
b. Limitation 5(b)

As discussed above, the converter depicted in Figure 12(b) operates in converter operating cycles where (1) at time t_1 to t_2 Q_1 is closed/on and Q_2 is open/off and current is delivered from the source to the resonant tank and the transformer, (2) Q_1 and Q_2 are both open/off and current flows through the body diode of Q_2 causing the voltage across the transistor to drop until it reaches a value close to zero, (3) at time t_2 to t_3 Q_1 is open/off and Q_2 is closed/on and the remaining power stored in the resonant tank is transferred to the transformer with current flowing in the opposing direction as in time t_1 to t_2 , and (4) Q_1 and Q_2 are both open/off and current flows through the body diode of Q_1 causing the voltage across the transistor to drop until it reaches a value close to zero. Ex. 1005, Figs. 14(a), 14(b), 1378; Ex. 1003, ¶90. Steps (1) and (3) above are power transfer intervals because current/power is being transferred between components of the circuit. Ex. 1003, ¶90. Further, a POSITA would have known that the opening and closing of Q_1 and Q_2 was operated by a switch controller. *Id.*

Huang further discloses that these power transfer intervals are of essentially equal duration, each less than the characteristic resonant period. Ex. 1003, ¶91. The durations of these intervals are shown in Figure 14(c), demonstrating that they are essentially the same length (half of a time unit):

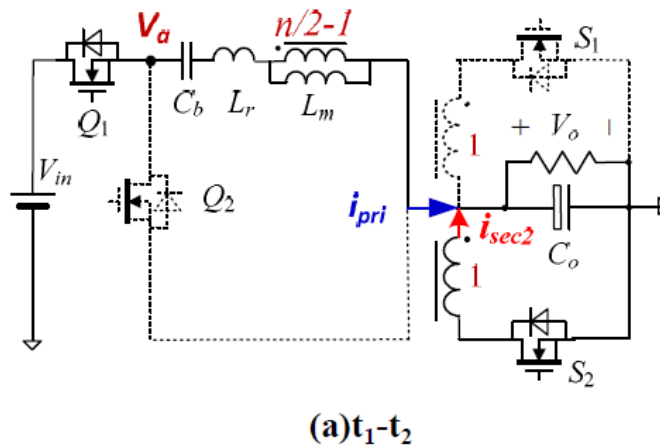


Ex. 1005, Figures 14(c) (annotations added), 1378; Ex. 1003, ¶91. The interval across which all the above steps are performed is the switching period. Ex. 1003, ¶92. For Huang's Figure 12(b) converter, the period is t_1 to t_3 (steps 2 and 4 are essentially instantaneous). *Id.*



Ex. 1005, Figure 14(c) (annotations added), 1378; Ex. 1003, ¶92. In describing the operation of the Figure 12(b) converter, Huang discloses that the switching frequency for the converter is at or above the resonant frequency. Ex. 1005, 1378. It is a known property that the switching frequency is the inverse of the switching period, and the resonant frequency is the inverse of the resonant period. Ex. 1003, ¶93. Thus, Huang's disclosure that the switching frequency of the Figure 12(b) converter may be at or above the resonant frequency, the switching period of Huang is equal to or less than the resonant period. *Id.* Because each power transfer interval is shown by Huang to be about half of the switching period (which is itself equal to or less than the resonant period) each power transfer interval is also less than the resonant period. *Id.*

During the converter operating cycle, when switch Q_1 is closed/on, power is transferred from the input to the output via the transformer, as can be seen in Figure 14(a):



Ex. 1005, Figure 14(a), 1378; Ex. 1003, ¶94.

3. Claim 6

Huang renders obvious claim 1. §V.A.1, *supra*. As the '950 Patent itself explains, IBA was known in the art at the time of invention. Ex. 1001, 1:13-35. IBA included a bus converter that included, for example, a DC-DC converter such as that disclosed by Huang. *Id.*; Ex. 1005, Figure 12(b). As discussed above, a POSITA would have known to use a DC-DC converter such as Huang's where the input to the converter and output of the converter are both DC. *See* §V.A.1.c. Moreover, it was known that bus converters would comprise self-contained assemblies adapted to be installed as units into, for example, computing systems. *Id.*; Ex. 1003, ¶95.

4. Claim 7

Huang renders obvious claim 1. §V.A.1, *supra*. Further, it was known that bus converters and regulators could be assembled onto a circuit board with one another. Ex. 1003, ¶96. And, as claimed in claim 1, it was known that regulators would provide power to a load. *Id.* When the regulator was mounted to the same circuit board as the bus converter, rather than the same circuit board as the load itself, the regulator would necessarily provide power to the integrated circuit as the load. *Id.*

5. Claim 9

a. Limitation 9(a)

b. Limitation 9(b)

See §§V.A.1.b, V.A.1.c, supra.

c. Limitation 9(c)

See §V.A.1.f, supra.

d. Limitation 9(d)

See §V.A.1.g, supra.

e. Limitation 9(e)

See §V.A.1.h, supra.

6. Claim 13

a. Limitation 13(a)

See §§V.A.5, V.A.2.a, supra.

b. Limitation 13(b)

See §V.A.2.b, supra.

7. Claim 14

Huang renders obvious claim 9. §V.A.5, *supra*. As the '950 Patent itself acknowledges, IBA was known in the art at the time of invention. Ex. 1001, 1:13-35 (describing IBA configuration as prior art). IBA included a bus converter that included, for example, a DC transformer to provide voltage transformation, *e.g.*, a DC-DC converter such as that disclosed by Huang. *Id.*; Ex. 1005, Figure 12(b). A

POSITA would have known that a DC-DC converter like that disclosed in Huang may be used alone or as part of a bus converter. Ex. 1003, ¶103. A POSITA would have further known that bus converters were commonly provided in self-contained assemblies to be installed into computing system as a unit. *Id.*

8. Claim 15

See §§V.A.5, V.A.1.d, V.A.1.e, V.A.4, *supra*.

9. Claim 16

a. Limitation 16(a)

b. Limitation 16(b)

See §§V.A.1.b, V.A.1.c, *supra*.

c. Limitation 16(c)

See §V.A.1.d, *supra*.

d. Limitation 16(d)

See §V.A.1.e, *supra*.

e. Limitation 16(e)

See §V.A.1.f, *supra*.

f. Limitation 16(f)

See §V.A.1.g, *supra*.

g. Limitation 16(g)

See §V.A.1.h, *supra*.

10. Claim 19

See §§V.A.9, V.A.3, *supra*.

11. Claim 21

a. Limitation 21(a)

See §§V.A.9, V.A.2.a, *supra*.

b. Limitation 21(b)

See §V.A.2.b, *supra*.

12. Claim 22

a. Limitation 22(a): An apparatus comprising:

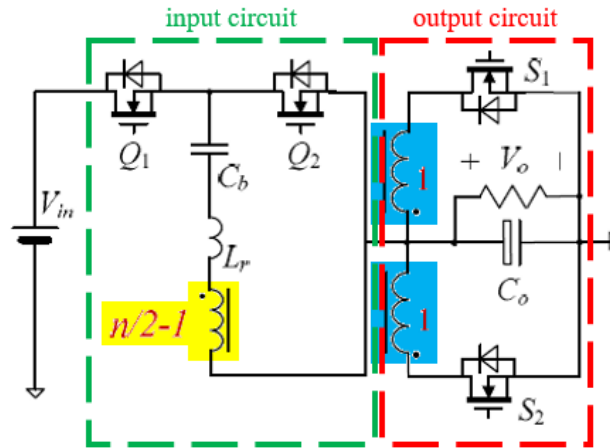
b. Limitation 22(b)

Huang renders obvious this claim limitation for the same reasons discussed above for claim element 1(b). *See* §V.A.1.b, *supra*. As the '950 Patent acknowledges, IBA was known in the art at the time of invention. Ex. 1001, 1:13-35 (describing IBA configuration as prior art); Ex. 1003, ¶114.

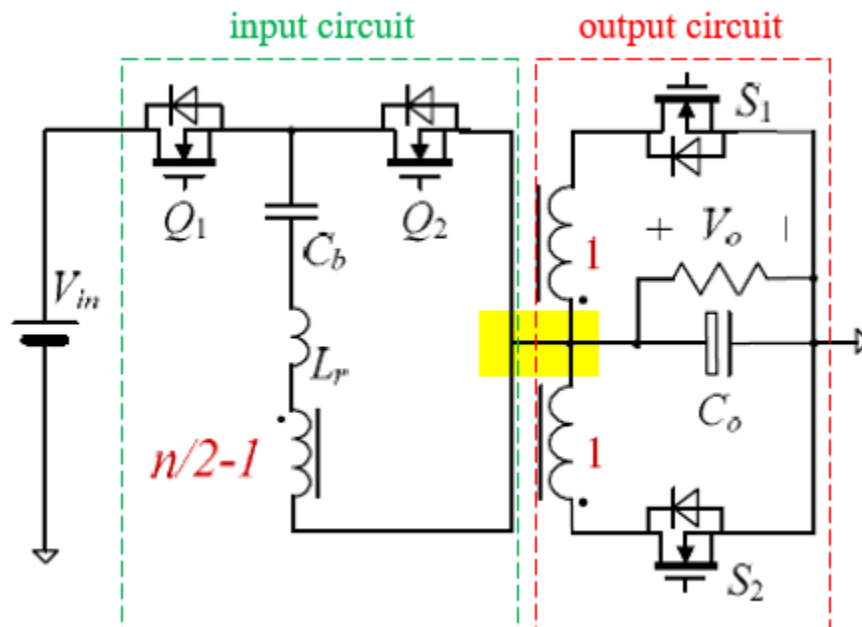
c. Limitation 22(c)

As discussed above, a POSITA would have known that Huang's Figure 12(b) converter could be used as part of a bus converter and would have been motivated to do so due to the efficiencies gained by Huang's converter. §V.A.1.c, *supra*. Huang's input and output circuits are outlined in green and red, respectively, below. Huang's primary transformer winding within the input circuit

is highlighted in yellow while the secondary windings within the output circuit are highlighted in blue.



Ex. 1003, Figure 12(b) (annotations added); Ex. 1003, ¶116. Further, the input and output circuits are galvanically connected in series, as can be seen by the direct connection between them (yellow):



Ex. 1003, Figure 12(b) (annotations added); Ex. 1003, ¶117. Huang's Figure 12(b) converter is therefore also configured to provide power to a power distribution bus that is not galvanically isolated from the source because it does not provide galvanic isolation between the source (V_{in}) and the power provided to the power distribution bus (V_o).. Ex. 1003, ¶118.

d. Limitation 22(d)

See §V.A.1.e, supra.

13. Claim 23

a. Limitation 23(a)

See §§V.A.12, V.A.1.c, supra.

b. Limitation 23(b)

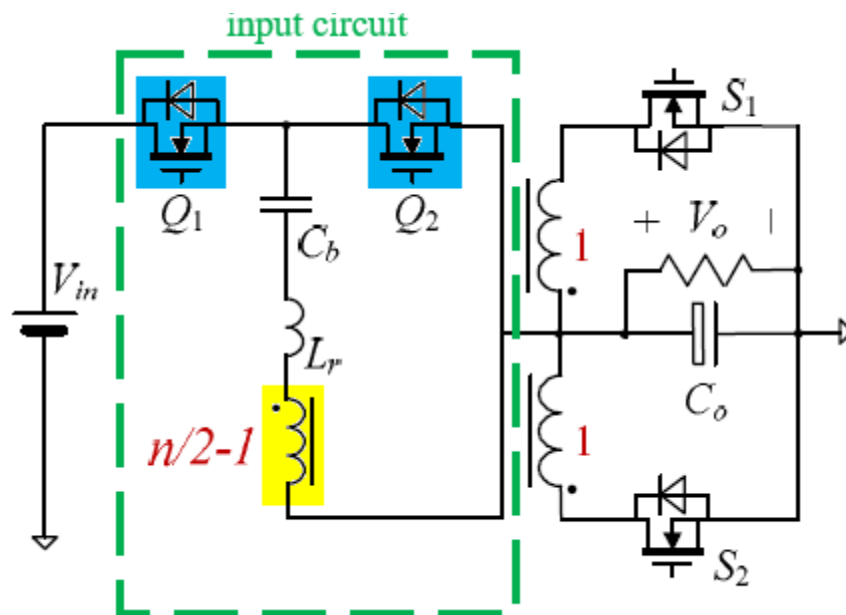
See §V.A.1.f, supra.

14. Claim 24

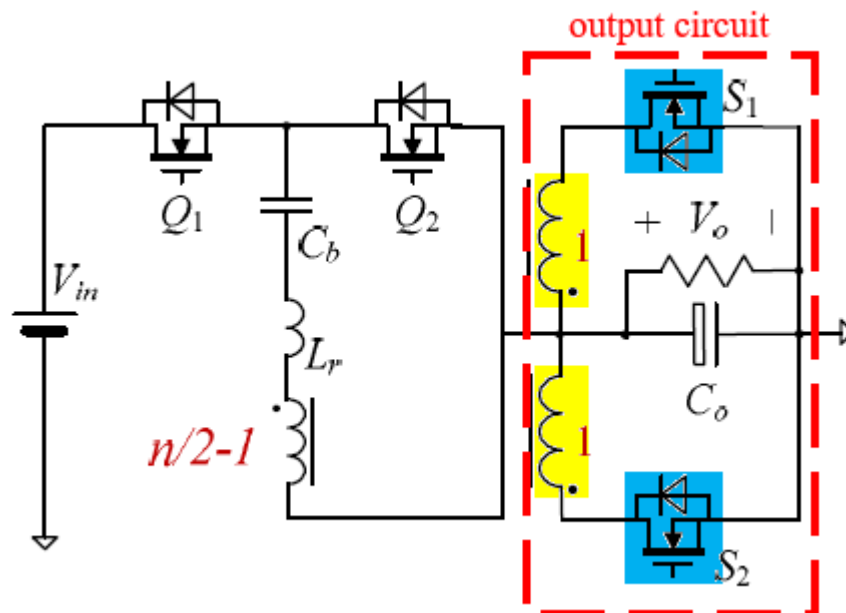
Huang renders obvious claim 22. Huang renders obvious this claim limitation for the same reasons discussed above for claim 6. *See §§V.A.12, V.A.3, supra.*

15. Claim 25

Huang renders obvious claim 1. §V.A.1, *supra*. Below, Huang's input circuit is outlined in green, with the primary winding highlighted in yellow and the primary switches connected to the primary winding highlighted in blue:

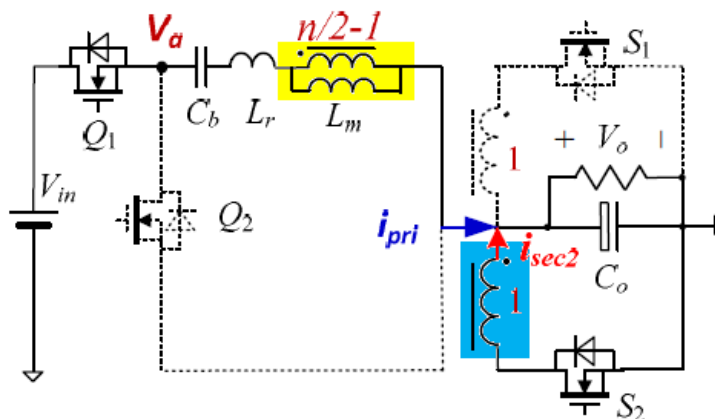


Ex. 1005, Figure 12(b) (annotations added); Ex. 1003, ¶123. Huang's output circuit is outlined in red below, with the secondary winding highlighted in yellow and the secondary switches connected to the secondary winding highlighted in blue:



Ex. 1005, Figure 12(b) (annotations added); Ex. 1003, ¶124.

As discussed in detail above, a switch controller operates the primary and secondary switches in a series of operating cycles, each comprising two power transfer intervals. §V.A.2.b, *supra*. During the converter operating cycle when switch Q_1 is closed/on, the primary winding (yellow) is connected in series to the secondary winding (blue), as can be seen in Figure 14(a):



Ex. 1005, Figure 14(a) (annotations added), 1378; Ex. 1003, ¶125.

16. Claim 26

See §§V.A.5, V.A.15, supra.

17. Claim 27

See §§V.A.9, V.A.15, supra.

18. Claim 28

See §§V.A.1, V.A.1.h, supra.

19. Claim 29

a. Limitation 29(a)

b. Limitation 29(b)

See §V.A.1.b, supra.

c. Limitation 29(c)

See §V.A.1.c, supra.

d. Limitation 29(d)

See §V.A.1.d, supra.

e. Limitation 29(e)

See §V.A.1.e, supra.

f. Limitation 29(f)

See §V.A.1.f, supra.

g. Limitation 29(g)

See §V.A.1.g, supra.

h. Limitation 29(h)

See §V.A.1.h, supra.

20. Claim 30

See §§V.A.19, V.A.1.h, supra.

21. Claim 31

a. Limitation 31(a)

b. Limitation 31(b)

See §V.A.1.b, supra.

c. Limitation 31(c)

See §V.A.1.c, supra.

d. Limitation 31(d)

See §V.A.1.d, supra.

e. Limitation 31(e)

See §V.A.1.e, supra.

f. Limitation 31(f)

See §V.A.1.c, supra.

g. Limitation 31(g)

See §V.A.1.f, supra.

22. Claim 32

a. Element 32(a)

b. Element 32(b)

See §V.A.1.b, supra.

c. Element 32(c)

See §V.A.1.c, supra.

d. Element 32(d)

See §V.A.1.d, supra.

e. Element 32(e)

See §V.A.1.e, supra.

f. Element 32(f)

See §V.A.1.c, supra.

g. Element 32(g)

See §V.A.1.f, supra.

23. Claim 33

a. Limitation 33(a)

b. Limitation 33(b)

See §V.A.1.c, supra.

c. Limitation 33(c)

See §V.A.1.f, supra.

d. Limitation 33(d)

See §V.A.1.g, supra.

e. Limitation 33(e)

See §V.A.1.h, supra.

24. Claim 34

a. Limitation 34(a)

See §§V.A.23, V.A.2.a, supra.

b. Limitation 34(b)

See §V.A.2.b, supra.

25. Claim 35

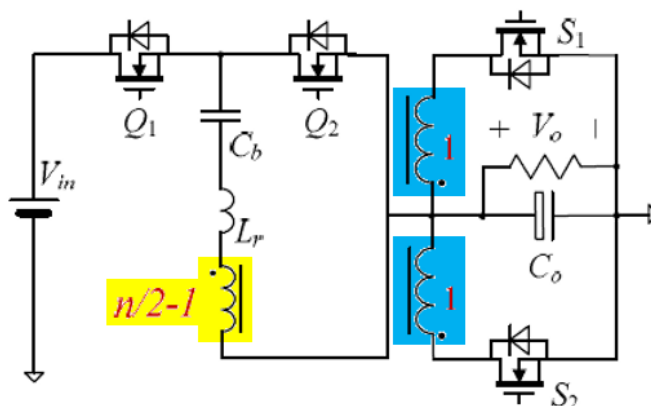
Huang renders obvious claim 33. Huang renders obvious this claim for the same reasons discussed above for claim 28. *See §§V.A.23, V.A.18, supra.*

26. Claim 36

See §§V.A.23, V.A.1.f, supra.

27. Claim 37

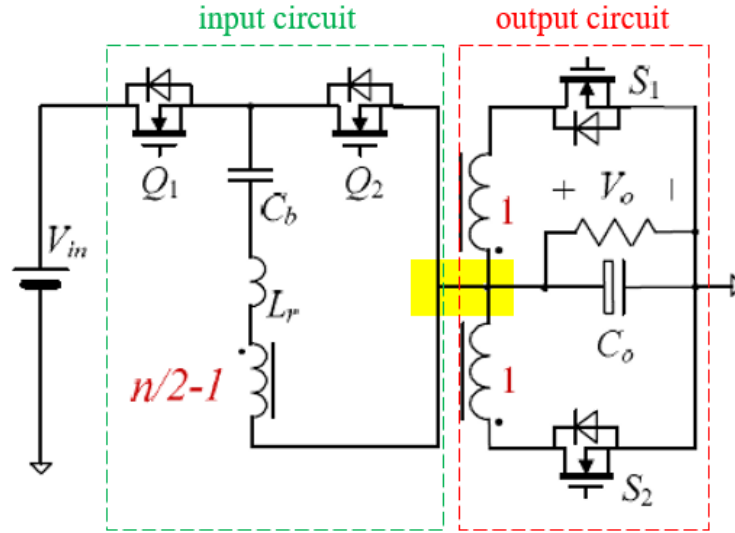
Huang renders obvious claim 33. §V.A.23, *supra*. The input circuit of Huang's Figure 12(b) converter comprises a first transformer winding having a first number of turns, $\frac{n}{2} - 1$ (yellow), and two second windings each having one turn (blue).



Ex. 1005, Figure 12(b) (annotations added); Ex. 1003, ¶157. As discussed above, the voltage transformation ratio is a function of the transformer turns ratio, which is the ratio of the number of turns of the second winding to the number of turns of the first winding. §V.A.1.c, *supra*; Ex. 1003, ¶158.

28. Claim 38

Huang renders obvious claim 37. §V.A.27, *supra*. A series connection between the input circuit and the output circuit is shown in Figure 12(b), highlighted in yellow below.



Ex. 1005, Figure 12(b) (annotations added); Ex. 1003, ¶159. Galvanic connection refers to whether there is direct electrical charge connection between functional sections of the system, *i.e.*, the input and output circuit. Ex. 1003, ¶160. Because the input circuit and output circuit are serially connected and non-isolated, they are galvanically connected. *Id.*

As discussed above, using the voltage transformation ratio ($K_{DC} = \frac{V_{OUT}}{V_{IN}} = \frac{V_o}{V_{in}-V_o}$) and the transformer turns ratio provided by Huang ($K_t = \frac{(V_{in}/2)-V_o}{V_o}$), one can derive that $K_{DC} = \frac{1}{2K_t+1}$. See §V.A.1.c, *supra*; Ex. 1003, ¶161. The voltage applied to the transformer primary winding is equal to the transformer turns ratio multiplied by the voltage applied to the transformer secondary winding. Ex. 1003, ¶162. Here, we know the voltage applied to the transformer secondary winding is

V_{OUT} . *Id.* Thus, the voltage across the transformer primary winding, V_{PRI} is equal to $K_t * V_{OUT}$. *Id.*

Using the fact that $K_{DC} = \frac{1}{2K_t+1}$ and $K_{DC} = \frac{V_{OUT}}{V_{IN}}$, one knows that $\frac{V_{OUT}}{V_{IN}} = \frac{1}{2K_t+1}$. Ex. 1003, ¶163. Using this relation, we can show that $V_{PRI} = K_t * V_{OUT} =$

$V_{IN} - (K_t + 1) * V_{OUT}$:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{2K_t+1}.$$

Cross multiply:

$$V_{IN} = (2K_t + 1) * V_{OUT}$$

Multiply out right side:

$$V_{IN} = 2K_t V_{OUT} + V_{OUT}$$

Subtract $K_t V_{OUT}$ from both sides:

$$V_{IN} - K_t V_{OUT} = K_t V_{OUT} + V_{OUT}$$

Subtract V_{OUT} from both sides:

$$V_{IN} - K_t V_{OUT} - V_{OUT} = K_t V_{OUT}$$

Simplify by factoring out V_{OUT}

$$V_{IN} - (K_t + 1) * V_{OUT} = K_t V_{OUT}$$

Id. Thus, the voltage applied to the first winding, V_{PRI} or $K_t * V_{OUT}$, is approximately equal to the absolute value of the input voltage, V_{IN} , minus a number N times the absolute value of the output voltage V_{OUT} , where N is $K_t + 1$. Ex. 1003, ¶164. $K_t + 1$ is greater than 1 because the transformer turns ratio must be a positive number. *Id.*

29. Claim 39

See §§V.A.12, V.A.1.g, V.A.1.h, *supra*.

30. Claim 40

See §V.A.4, *supra*.

B. Ground II: Claims 5, 13, 21, 25-27, and 34 Are Obvious Over Huang In View Of The '481 Patent

1. Motivation to Combine

A POSITA would have been motivated to combine Huang and the '481 Patent. Ex. 1003, ¶167-170. Huang discloses a variety of novel, non-isolated LLC DC-DC resonant converters that can achieve zero voltage switching, low turn off loss for switches, reduction in transformer turns, and reduction of current through transformer secondary windings. *See* Ex. 1005, 1373. The '481 Patent is directed to a method for “digital control of resonant zero-current and zero-voltage switching resonant power converters,” such as the resonant circuits disclosed in Huang. *See* Ex. 1007, 1:6-9.

Modifying the resonant converter disclosed in Huang to utilize the digital control circuitry disclosed in the '481 Patent would have been obvious to a POSITA. *First*, as the '481 Patent states, prior art power converters using resonant processes to efficiently transfer energy from an input source to a load (e.g., the converters disclosed in Huang) were known to include controllers to control “the turning ON and OFF of switches within the power conversion circuitry.” Ex. 1007, 1:13-25. It would have been obvious to a POSITA to try using the digital control circuitry described in the '481 Patent with the converters disclosed in Huang: there

were a limited number of controller types compatible with resonant circuits, and a POSITA would have had a reasonable expectation of success in using the '481 Patent's circuitry with the converters disclosed in Huang. Ex. 1003, ¶168. Indeed, the '481 Patent confirms that its disclosed digital power conversion circuitry is “essentially the same” as what existed in the prior art. Ex. 1007, 4:29-35.

Second, a POSITA would have specifically been interested in enhancing efficiency in light of Huang's focus on improving existing converter design to reduce switching and transformer losses. *See, e.g.*, Ex. 1005, 1373. Both Huang and the '481 Patent indicate that a motivation to implement their disclosed inventions is to improve the efficiency of existing circuit design. *See, e.g., id.*; Ex. 1007, 7:29-35. Thus, a POSITA would have been counseled to improve the efficiency of the circuit design in other ways, such as including digital control circuitry to improve the energy efficiency of the converter. *See* Ex. 1003, ¶169.

Third, use of the digital control circuitry in the '481 Patent with the resonant converters disclosed in Huang would have involved mere substitution of one known element (existing control circuitry) for another (the specific digital control circuitry disclosed in the '481 Patent) to obtain predictable results (the efficient control of the resonant converter). Ex. 1003, ¶170. A POSITA would have recognized using the circuitry disclosed in the '481 Patent to be an easy

modification or addition to make to Huang's converters using standard techniques known in the art. *Id.*

2. Claim 5

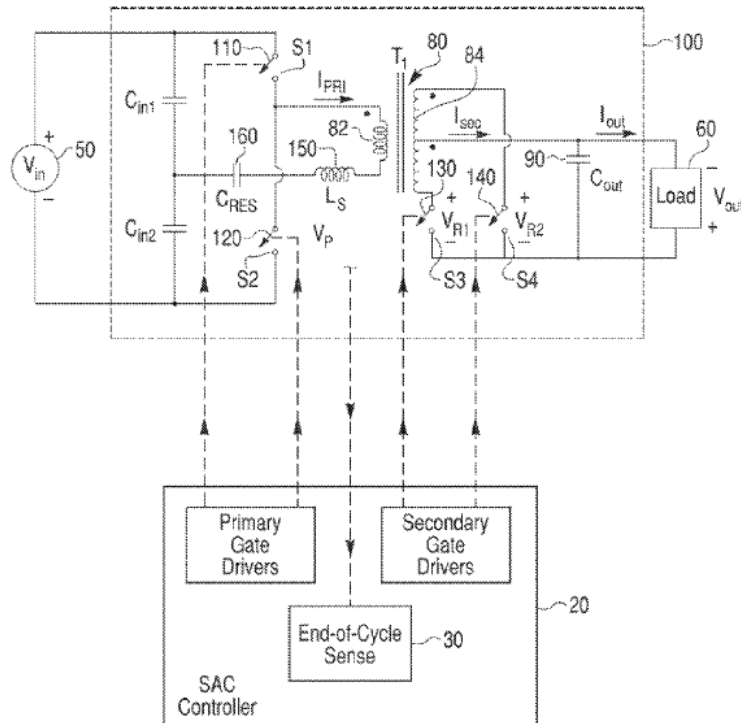
a. Limitation 5(a)

Huang in view of the '481 Patent renders this limitation obvious for the reasons discussed above. §§V.A.1, V.A.2.a. The '481 Patent further discloses that the resonant circuit including the transformer that the disclosed circuitry is intended to control comprises a characteristic resonant frequency and period. *See, e.g.,* Ex. 1007, 1:32-36, 4:29-45, 6:21-24, claim 1.

b. Limitation 5(b)

Huang modified to operate with the control circuitry disclosed by the '481 Patent renders this limitation obvious. Ex. 1003, ¶172. Specifically, the '481 Patent discloses a “method of synchronously operating a power converter in a series of converter operating cycles.” Ex. 1007, Abstract. The switch controller “controls the turning ON and OFF of switches within the power conversion circuitry” to control the timing of power transfer and energy recycling intervals. *Id.*, 1:22-59. “Each converter operating cycle comprises two power transfer intervals of equal length and two energy recycling intervals of equal length.... Each power transfer interval is substantially equal to one-half of the characteristic period” *Id.*, 1:47-53; *see also id.*, 8:22-26 (normal converter operation may be defined by power transfer intervals being one half of the characteristic resonant period). During a power

transfer interval, primary switches (e.g., S1 in the figure below) are closed which causes a flow of resonant current in the transformer primary winding, *i.e.*, power is transferred from the input of the circuit to the output via the transformer. *Id.*, 1:22-47.



Ex. 1007, Figure 1 (prior art).

3. Claim 13

a. *Limitation 13(a)*

See §§V.A.5, V.A.2.a, V.B.2.a.

b. *Limitation 13(b)*

See §§V.A.2.b, V.B.2.b.

4. Claim 21

a. Limitation 21(a)

See §§V.A.9, V.A.2.a, V.B.2.a.

b. Limitation 21(b)

See §§V.A.2.b, V.B.2.b.

5. Claim 25

See §§V.A.1, V.A.15, V.A.2, V.B.2.

6. Claim 26

See §§V.A.5, V.A.16, V.A.2, V.B.2.

7. Claim 27

See §§V.A.9, V.A.17, V.A.2, V.B.2.

8. Claim 34

a. Limitation 34(a)

See §§V.A.23, V.A.24, V.A.2.a, V.B.2.a.

b. Limitation 34(b)

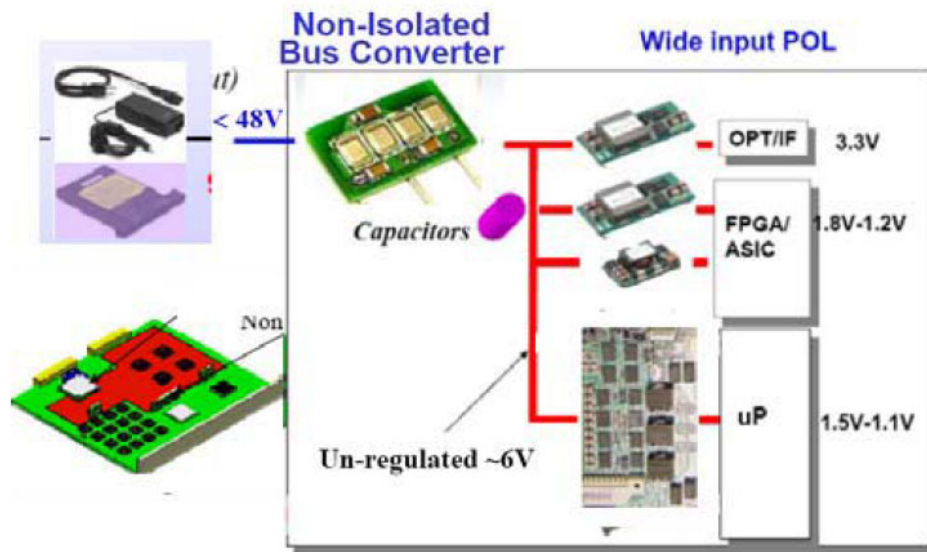
See §§V.A.2.b, V.B.2.b.

C. Grounds III and IV: Claims 1, 5-7, 14-16, 19, and 21-40 Are Obvious Over Huang, Alone Or In Combination With The '481 Patent, In View Of Lee

1. Motivation to Combine

A POSITA would have been motivated to combine Huang, alone or in combination with the '481 Patent, and Lee. Ex. 1003, ¶182-187. Huang discloses a variety of novel, non-isolated LLC DC-DC resonant converters that can achieve

zero voltage switching, low turn off loss for switches, reduction in transformer turns, and reduction of current through transformer secondary windings. *See* Ex. 1005, 1373. Lee discusses design challenges and opportunities for a variety of power supply applications including DC-DC converters. Ex. 1008, 1. Opportunities discussed include cost savings, performance improvements, and chip size. *Id.* One specific proposal is a non-isolated intermediate bus architecture, depicted below. *Id.*, 12, Figure 43. This architecture includes a non-isolated bus converter designed to minimize switching losses and body diode losses at high switching frequencies and increase circuit efficiency. *Id.*, 11-12.



Ex. 1008, Figure 43. Lee discloses using a “voltage divider” DC-DC converter that can achieve high power density and “ultra-high efficiency in the whole load range with capability to handle over load conditions” as the non-isolated bus converter in Lee’s architecture. *Id.* at 12.

It would have been obvious to a POSITA to use the resonant converters disclosed in Huang, as is or as modified by the '481 Patent, in the intermediate bus architecture disclosed in Lee in place of Lee's "voltage divider." Ex. 1003, ¶184. **First**, a POSITA would understand that the "non-isolated bus converter" of Lee's proposed architecture is a power converting circuit that could take many forms, including the DC-DC converter disclosed by Huang. *Id.* **Second**, Huang contemplates the use of its converters in point-of-load (POL) and voltage regulator applications where high power density and high efficiency are desired. Ex. 1005, 1373. It would have been obvious to a POSITA to try Huang's high power density and high efficiency converters as the non-isolated bus converter in the non-isolated intermediate bus architecture proposed by Lee in place of Lee's DC-DC "voltage divider": there were limited options for non-isolated converters, and Huang's non-isolated LLC resonant converters were specifically designed for the same purpose as Lee's voltage divider, namely, increasing overall circuit efficiency. *Compare* Ex. 1005, 1373, 1378-79, *with* Ex. 1008, 12; Ex. 1003, ¶185. A POSITA would have had a reasonable expectation of success in using Huang's converters in the intermediate bus architecture disclosed in Lee because, as shown in Lee Figure 43, it was contemplated that the non-isolated bus converter would be a modular, and thus replaceable, component.

Third, a POSITA would have specifically been interested in enhancing efficiency in light of both Lee and Huang's focus on improving existing converter design to reduce switching and transformer losses. *See, e.g.*, Ex. 1005, 1373; Ex. 1008, 11-12. Both Huang and Lee indicate that a motivation to implement their disclosed inventions is to improve the efficiency of existing circuit design. *See, e.g., id.* Thus, a POSITA would be counseled to improve the efficiency of the circuit design in other ways, such as including Huang's improved converters in Lee's improved architecture design to improve the overall power conversion efficiency. *See* Ex. 1003, ¶186.

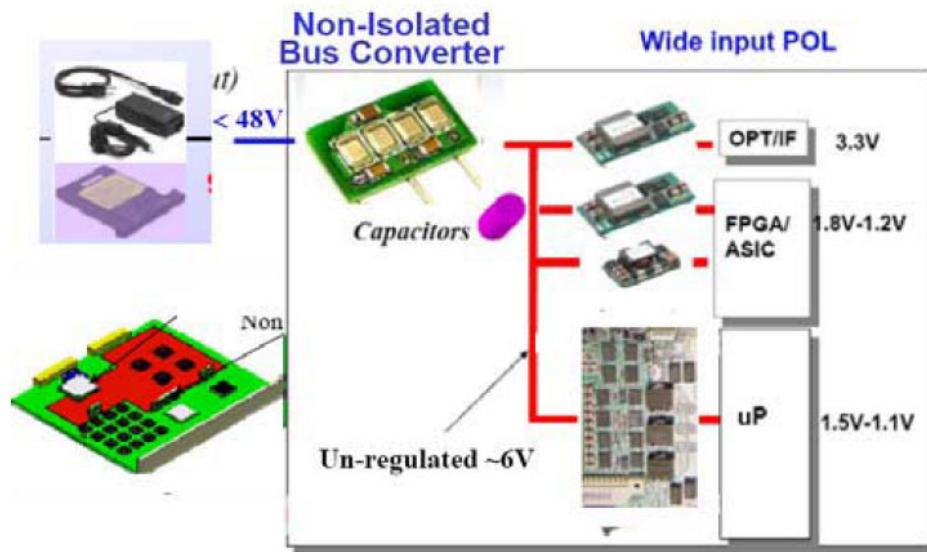
Fourth, use of Lee's intermediate bus architecture with the resonant converters disclosed in Huang would have involved mere substitution of one known element (Lee's "voltage divider" as the non-isolated bus converter shown in Figure 43) for another (Huang's non-isolated LLC resonant converters as the non-isolated bus converter) to obtain predictable results (more efficient power conversion). Ex. 1003, ¶187. A POSITA would have recognized using Huang's Figure 12(b) converter to be an easy modification to make to Lee's intermediate bus architecture using standard techniques known in the art. *Id.*

2. **Claim 1**

a. *Limitation 1(a)*

b. *Limitation 1(b)*

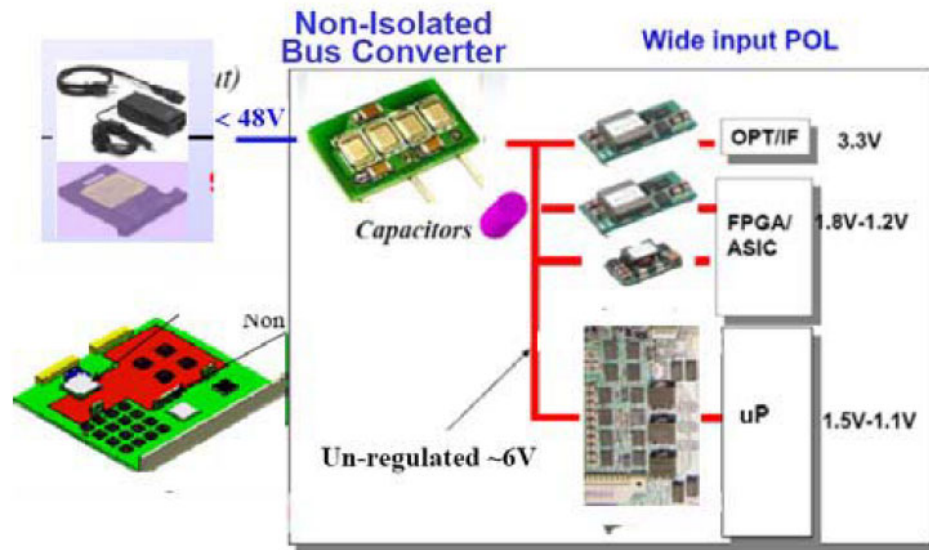
Lee's proposed intermediate bus architecture (a power distribution system) includes a 48V DC source voltage:



Ex. 1008, Figure 43; *see also id.*, 11-12 (“voltage divider” disclosed by Lee as a non-isolated bus converter is a DC-DC converter); Ex. 1003, ¶188. Huang likewise discloses this claim limitation. *See* §V.A.1.b.

c. *Limitation 1(c)*

As discussed above, Huang's Figure 12(b) converter would operate as the non-isolated bus converter Lee's intermediate bus architecture in the combination of Huang and Lee. Ex. 1003, ¶190; §V.C.1.

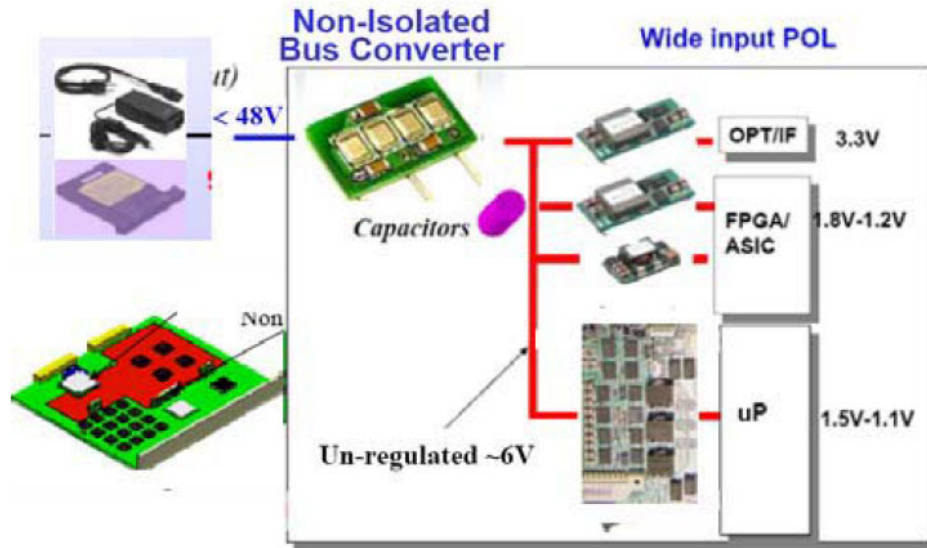


Ex. 1008, Figure 43. Huang's converter comprises the remainder of this limitation.

See §V.A.1.c.

d. Limitation 1(d)

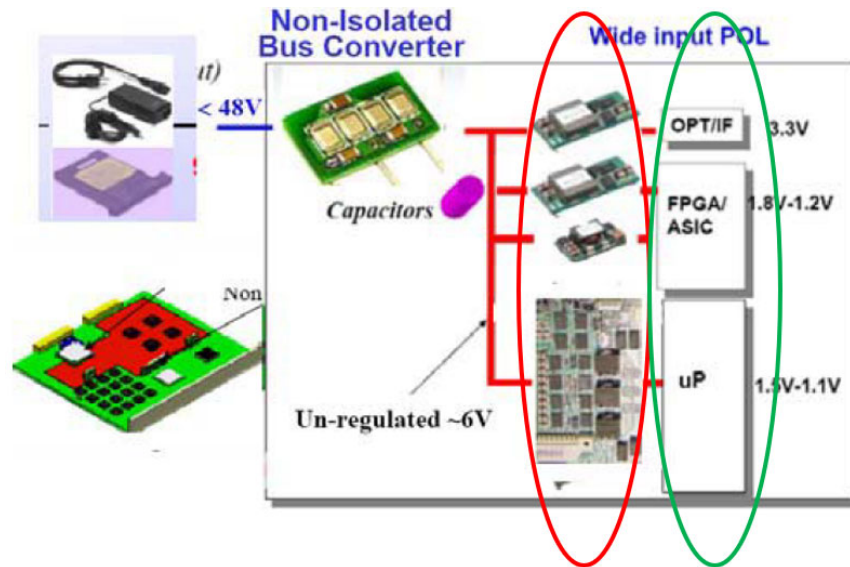
Lee's intermediate bus architecture includes a power distribution bus (red lines in figure below) connected to distribute power from the output circuit of the non-isolated bus converter (Huang's Figure 12(b) converter in the combination) at the output voltage V_{OUT} . See Ex. 1008, Figure 43; §V.A.1.d; Ex. 1003, ¶192.



Ex. 1008, Figure 43.

e. Limitation 1(e)

Lee's intermediate bus architecture includes a plurality of regulators, each regulator comprising an input connected to receive power from the output circuit of the bus converter (Huang's Figure 12(b) converter in the combination) and an output connected to supply power to a load. Ex. 1008, 11-12; Ex. 1003, ¶193. The circuits circled in red below are the regulators, what Lee refers to as "wide input POLs," or point-of-load DC-DC converters. Ex. 1008, 8, 11-12. The white boxes circled in green are the loads; for example, the center load is an FPGA or ASIC, two types of integrated circuits that are ordinarily off-the-shelf components. *Id.*; Ex. 1003, ¶193.



Ex. 1008, Figure 43 (annotations added). A POSITA would have recognized the regulators to be distanced from the bus converter for a number of reasons including at least because the bus converter is a separate component from the POL DC-DC converters and the POL DC-DC converters would have been part of the circuit boards comprising the loads themselves (i.e., the POL converters were local to the load, not the bus converter). Ex. 1003, ¶194.

f. Limitation I(f)

See §V.A.1.f.

g. Limitation I(g)

See §V.A.1.g.

h. Limitation I(h)

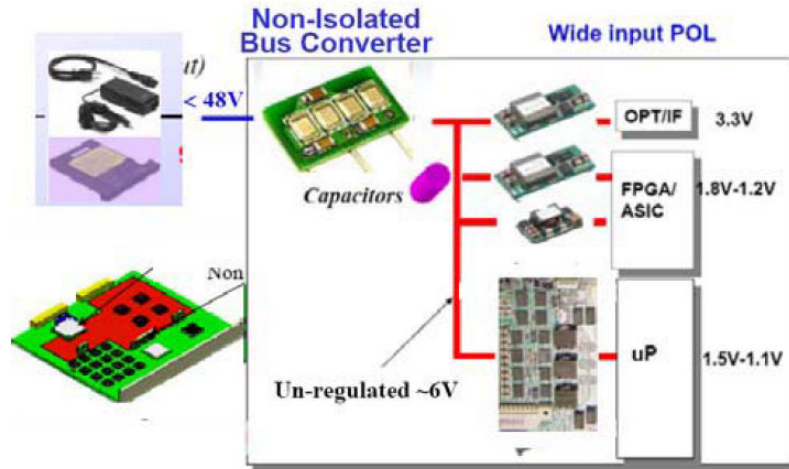
See §V.A.1.h.

3. Claim 5

See §§V.A.1, V.A.2, V.B.2, V.C.2.

4. Claim 6

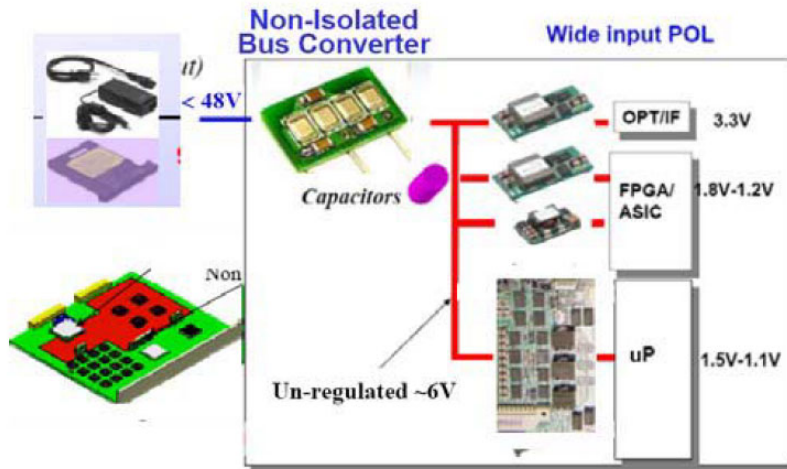
As seen in Figure 43 of Lee, the non-isolated bus converter of the proposed intermediate bus architecture is a self-contained assembly adapted to be installed as a unit:



Ex. 1008, Figure 43; Ex. 1003, ¶198.

5. Claim 7

As seen in Figure 43 of Lee, the non-isolated bus converter and the regulators are assembled to circuit boards in the proposed intermediate bus architecture:



Ex. 1008, Figure 43. At least one regulator in Lee is configured to supply power to an integrated circuit; specifically, the regulators are shown connected to an FPGA or ASIC, which is a type of integrated circuit. Ex. 1003, ¶199-200.

6. Claim 14

See §§V.A.3, V.A.5, V.C.4.

7. Claim 15

See §§V.A.4, V.A.5, V.A.1.e, V.C.2.e, V.C.5.

8. Claim 16

a. Limitation 16(a)

b. Limitation 16(b)

See §§V.A.1.b, V.A.1.c, V.C.2.b, V.C.2.c.

c. Limitation 16(c)

See §§V.A.1.d, V.C.2.d.

d. Limitation 16(d)

See §§V.A.1.e, V.C.2.e.

e. Limitation 16(e)

See §§V.A.1.f, V.C.2.f.

f. Limitation 16(f)

See §§V.A.1.g, V.C.2.g.

g. Limitation 16(g)

See §§V.A.1.h, V.C.2.h.

9. Claim 19

See §§V.A.9, V.A.3, V.C.9, V.C.4.

10. Claim 21

a. Limitation 21(a)

See §§V.A.9, V.A.2.a, V.A.11, V.B.2.a, V.B.4, V.C.8, V.C.3.a.

b. Limitation 21(b)

See §§V.A.2.b, V.B.2.b, V.C.3.

11. Claim 22

a. Limitation 22(a)

b. Limitation 22(b)

See §§V.A.1.b, V.A.12.b, V.C.2.b.

c. Limitation 22(c)

See §§V.A.1.c, V.A.12.c, V.C.2.c.

d. Limitation 22(d)

See §§V.A.1.e, V.A.12.e, V.C.2.e.

12. Claim 23

See §V.A.13.

13. Claim 24

See §§V.A.3, V.A.12, V.C.4, V.C.11.

14. Claims 25-28

See §§V.A.1, V.A.5, V.A.9, V.A.15-18, V.B.5-7, V.C.2, V.C.8.

15. Claim 29

a. Limitation 29(a)

b. Limitation 29(b)

See §§V.A.1.b, V.C.2.b.

c. Limitation 29(c)

See §§V.A.1.c, V.C.2.c.

d. Limitation 29(d)

See §§V.A.1.d, V.C.2.d.

e. Limitation 29(e)

See §§V.A.1.e, V.C.2.e.

f. Limitation 29(f)

See §§V.A.1.f, V.C.2.f.

g. Limitation 29(g)

See §§V.A.1.g, V.C.2.g.

h. Limitation 29(h)

See §§V.A.1.h, V.C.2.h.

16. Claim 30

See §V.A.20.

17. Claim 31

a. Limitation 31(a)

b. Limitation 31(b)

See §§V.A.1.b, V.C.2.b.

c. Limitation 31(c)

See §§V.A.1.c, V.C.2.c.

d. Limitation 31(d)

See §§V.A.1.d, V.C.2.d.

e. Limitation 31(e)

See §§V.A.1.e, V.C.2.e.

f. Limitation 31(f)

See §§V.A.1.c, V.C.2.c.

g. Limitation 31(g)

See §§V.A.1.f, V.C.2.f.

18. Claim 32

a. Limitation 32(a)

b. Limitation 32(b)

See §§V.A.1.b, V.C.2.b.

c. Limitation 32(c)

See §§V.A.1.c, V.C.2.c.

d. Limitation 32(d)

See §§V.A.1.d, V.C.2.d.

e. Limitation 32(e)

See §§V.A.1.e, V.C.2.e.

f. Limitation 32(f)

See §§V.A.1.c, V.C.2.c.

g. Limitation 32(g)

See §§V.A.1.f, V.C.2.f.

19. Claim 33

a. Limitation 33(a)

b. Limitation 33(b)

See §§V.A.1.c, V.C.2.c.

c. Limitation 33(c)

See §§V.A.1.f, V.C.2.f.

d. Limitation 33(d)

See §§V.A.1.g, V.C.2.g.

e. Limitation 33(e)

See §§V.A.1.h, V.C.2.h.

20. Claims 34-39

See §§V.A.24-29, V.B.8.

21. Claim 40

See §§V.A.4, V.C.5.

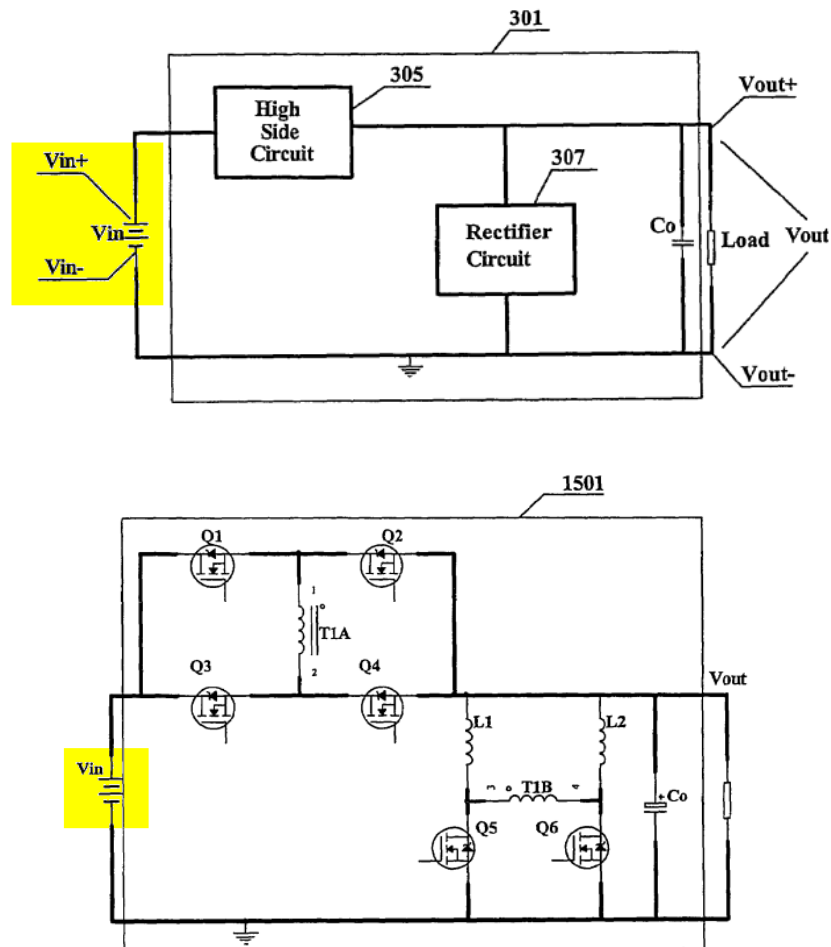
D. Ground V: Claims 1, 2, 6-10, 14-17, 19, 22-33, 35-37, and 39-40 Are Obvious Over Liu

1. Claim 1

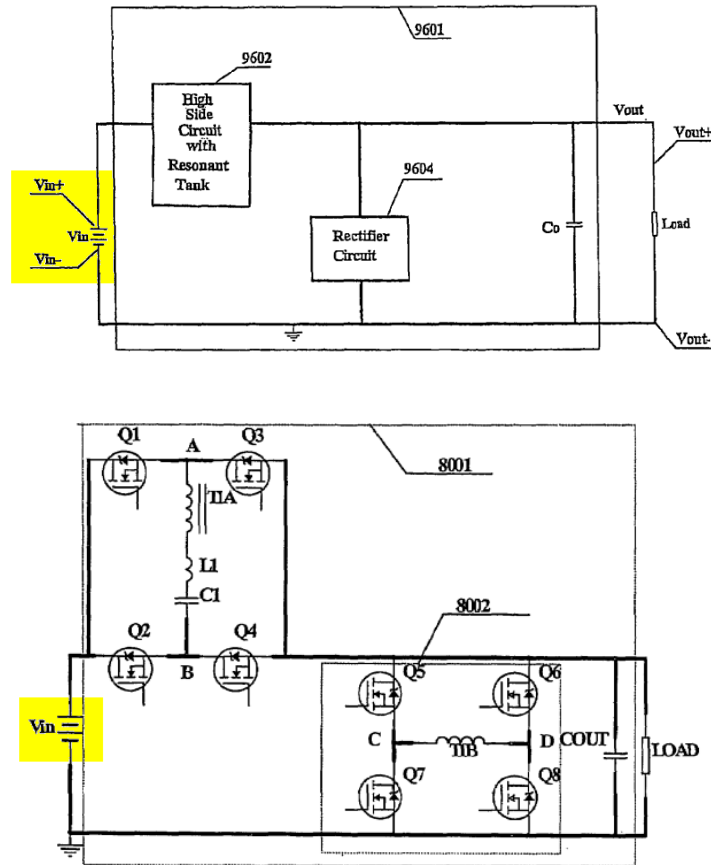
a. *Limitation 1(a)*

b. *Limitation 1(b)*

Liu discloses a variety of DC-DC converters, all of which receive as input a DC source voltage V_{in} . A first generalized embodiment of these converters is provided in Figure 3, of which Figure 15 is a particular embodiment:



Ex. 1006, Figures 3, 15 (annotation added). A second generalized embodiment of the disclosed converters is provided in Figure 68A, of which Figure 80 is a particular embodiment:

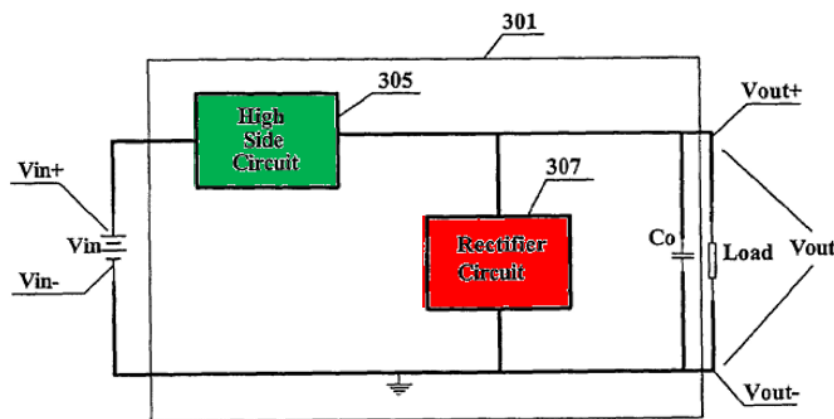


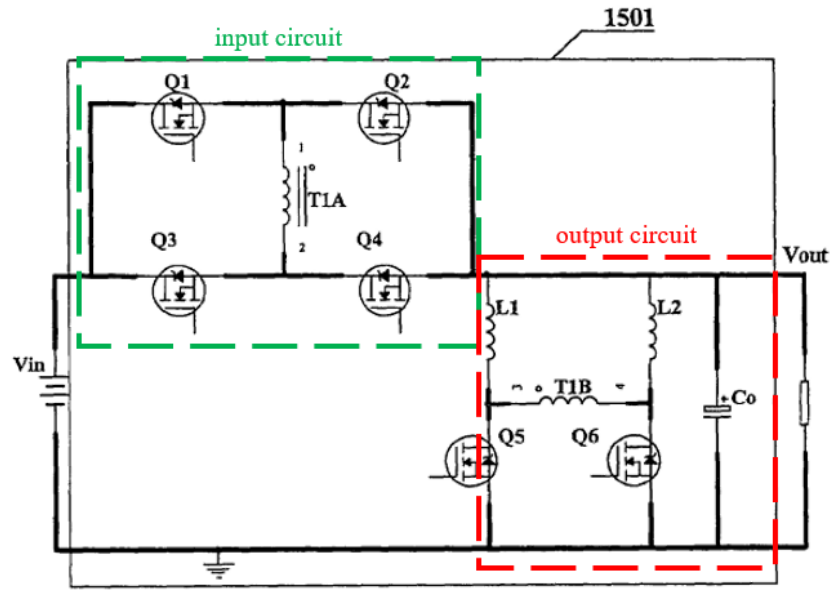
Id., Figures 68A, 80 (annotation added). Liu describes the input voltage as DC. *See, e.g.*, Ex. 1006, 2:64-3:2; 6:63-65. A POSITA would have known this DC source to have come from a power distribution system comprising the source. Ex. 1003, ¶243-245.

c. Limitation 1(c)

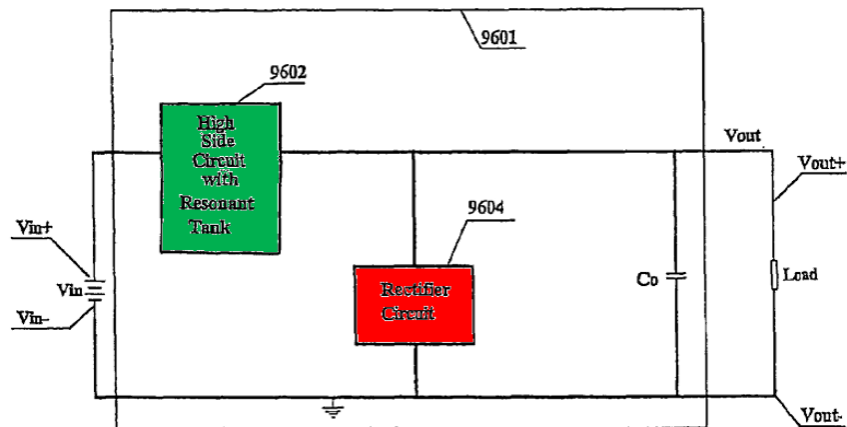
As the '950 Patent itself acknowledges, IBA was known in the art at the time of invention. Ex. 1001, 1:13-35. IBA included a bus converter that included, for example, a DC-DC converter such as that disclosed by Liu. *Id.*; Ex. 1006, Figs. 3, 15, 68A, 80. A POSITA would have known, where the input and output of the converter both need to be DC, to use a DC-DC converter such as Liu's as the bus converter or part of the bus converter because the input to the converter is DC and the electronics downstream from the converter also use DC. Ex. 1003, ¶246. A POSITA would have also known that, in the case of IBA, the bus converter should both be efficient and low cost. *Id.* Liu's converters increase efficiency by, for example, achieving zero voltage switching. *See* Ex. 1006, 36:20-33. Liu's converters would thus be an attractive option to a POSITA. Ex. 1003, ¶247.

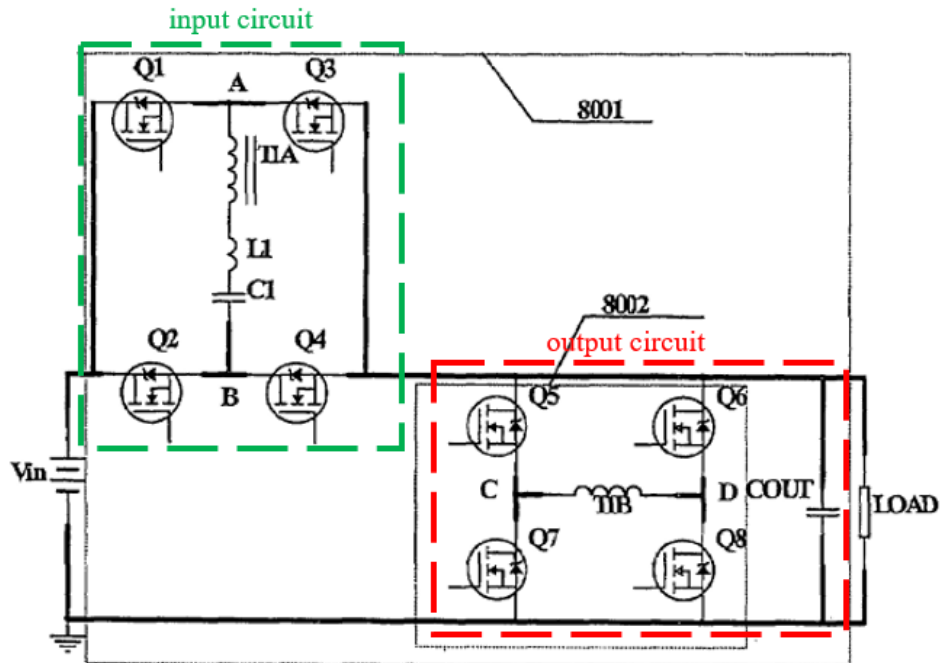
The converters embodying the Figure 3 configuration convert power from the input circuit to the output circuit, which are indicated in green and red, respectively:





Ex. 1006, Figures 3, 15 (annotations added). The converters embodying the Figure 68A configuration likewise convert power from the input circuit to the output circuit, which are indicated in green and red, respectively:





Id., Figures 68A, 80 (annotations added). The output circuit produces an output voltage, V_{out} , referred to in the claim as V_{OUT} . Ex. 1003, ¶248-250. *Id* The input voltage to the input circuit, V_{IN} , is the input voltage to the converter less the output voltage: $V_{in} - V_{out}$.

The power conversion is performed at a substantially fixed voltage transformation ratio that can be represented as $K_{DC} = V_{OUT}/V_{IN}$. In the circuits of Figures 15 and 80, the voltage transformation ratio is $K_{DC} = \frac{V_{out}}{V_{in} - V_{out}}$. Ex. 1003, ¶250. Further, the values of V_{out} and V_{in} can be represented in terms of the transformer turns ratio. See Ex. 1006, 17:5-15, 18:36-46; Ex. 1003, ¶151. For example, Liu discloses that the relationship between V_{out} and V_{in} for Figure 15 is shown in the equation $V_{out} = \frac{V_{in} * N * D}{(2 + N * D)}$ where N is the transformer turns ratio and D

is the total duty cycle. Ex. 1006, 18:36-46. Using this equation, we can derive K_{DC} based on the transformer turns ratio and total duty cycle:

$$V_{out} = \frac{V_{in} * N * D}{(2 + N * D)}$$

Multiply by $(2 + N * D)$: $(2 + N * D) * V_{out} = V_{in} * N * D$

Multiply out left side: $2 * V_{out} + N * D * V_{out} = V_{in} * N * D$

Subtract $N * D * V_{out}$: $2 * V_{out} = V_{in} * N * D - N * D * V_{out}$

Simplify right side: $2 * V_{out} = N * D (V_{in} - V_{out})$

Divide by $V_{in} - V_{out}$: $\frac{2 * V_{out}}{V_{in} - V_{out}} = N * D$

Divide by 2: $\frac{V_{out}}{V_{in} - V_{out}} = \frac{N * D}{2}$

Substitute: $K_{DC} = \frac{N * D}{2}$

Ex. 1003, ¶251. For a duty cycle of 50%, which Liu describes as desirable because it optimizes performance of the converter (*see* Ex. 1006, 17:5-15), the voltage transformation ratio becomes $K_{DC} = \frac{0.5 * N}{2}$, which can be simplified to $K_{DC} = \frac{N}{4}$.

Ex. 1003, ¶252. Thus, K_{DC} is fixed. *Id.*

The circuit depicted in Figure 80 is a series resonant LLC circuit. When the switching frequency of the circuit depicted in Figure 80 is at the resonant frequency, the voltage across the primary winding (as well as inductor L1 and capacitor C1) is $V_{in} - V_{out}$. Ex. 1003, ¶253. The voltage across the secondary winding is equivalent to V_{out} . *Id.* The turns ratio of a transformer is equal to the

voltage across the secondary winding divided by the voltage across the primary winding. *Id.* Therefore, the turns ratio of the transformer, N , in Figure 80 is

$\frac{V_{out}}{V_{in}-V_{out}}$. The voltage transformation ratio of the circuit shown in Figure 80 is

$K_{DC} = \frac{V_{out}}{V_{in}-V_{out}}$. *Id.* Thus, $K_{DC} = N$ and is therefore fixed by the physical

transformer turns ratio N . *Id.*

d. Limitation I(d)

Liu discloses an area of application for its disclosed converters as computing applications, more specifically as part of the power distribution bus taking AC voltage from a wall outlet, converting the AC to DC, and then converting the DC voltage to lower voltages required by, for example, CPUs. Ex. 1006, 1:21-48. A POSITA would have understood output of the DC-DC converters disclosed in Liu to be connected to the power distribution bus to distribute power from the output circuit, as this is the purpose of such converters. Ex. 1003, ¶254.

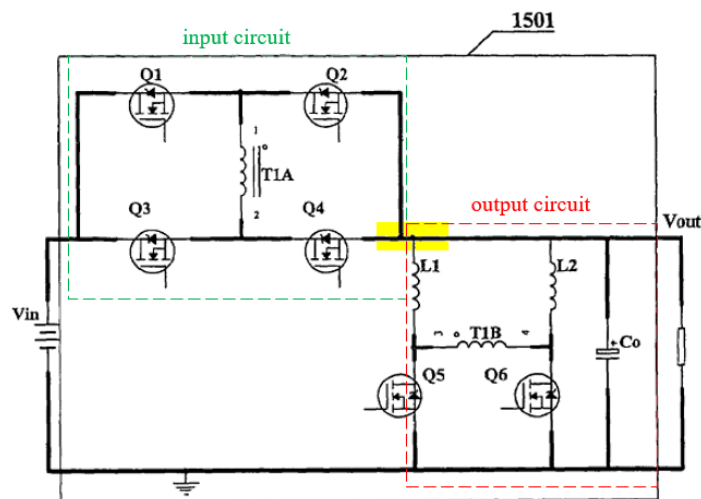
e. Limitation I(e)

The '950 Patent acknowledges that the use of an IBA, wherein a bus converter supplies power to one or more down-stream regulators, was known at the time of invention. Ex. 1001, 1:13-35, Figure 1. In this configuration, the input of the regulators is attached to a power distribution bus to which the output of the bus converter is also attached, such that the regulators are receiving power from the output of the bus converter. *Id.* The regulators would then provide regulated

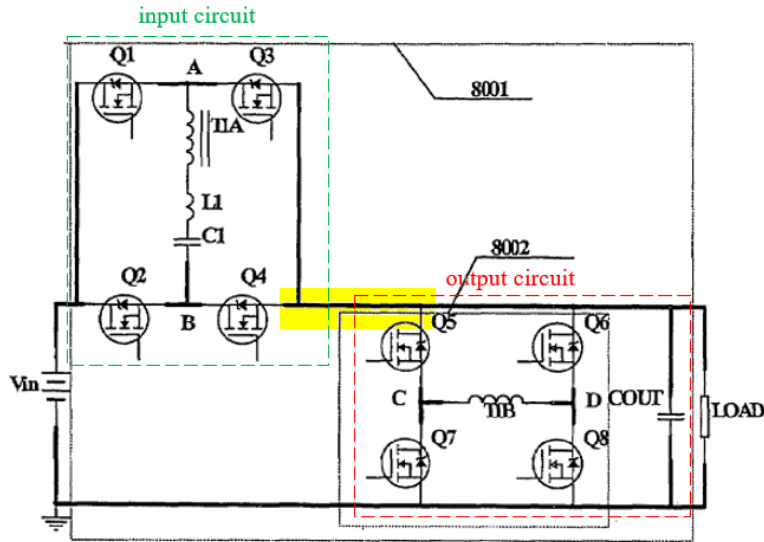
power/voltage to their respective loads. *Id.* A POSITA would have further known that regulators would be separated by a distance from the bus converter. Ex. 1003, ¶255.

f. Limitation 1(f)

A series connection between the input circuit (green) and the output circuit (red) in Figure 15 of Liu is highlighted in yellow below:



Ex. 1006, Figure 15 (annotations added). A series connection between the input circuit (green) and the output circuit (red) in Figure 80 of Liu is highlighted in yellow below:

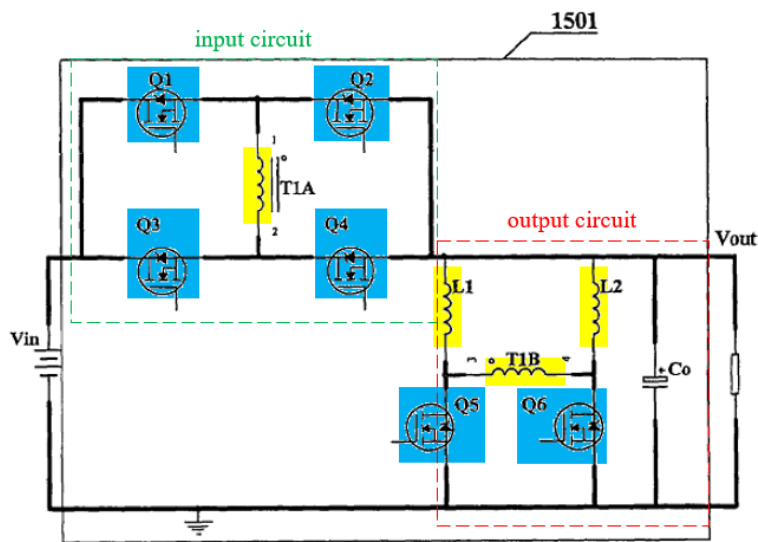


Ex. 1006, Figure 80 (annotations added). Galvanic connection refers to whether there is a direct electrical charge connection between functional sections of the system, *i.e.*, the input and output circuit. Ex. 1003, ¶256-258. Because the input circuit and output circuit are serially connected and non-isolated, they are galvanically connected. *Id.*

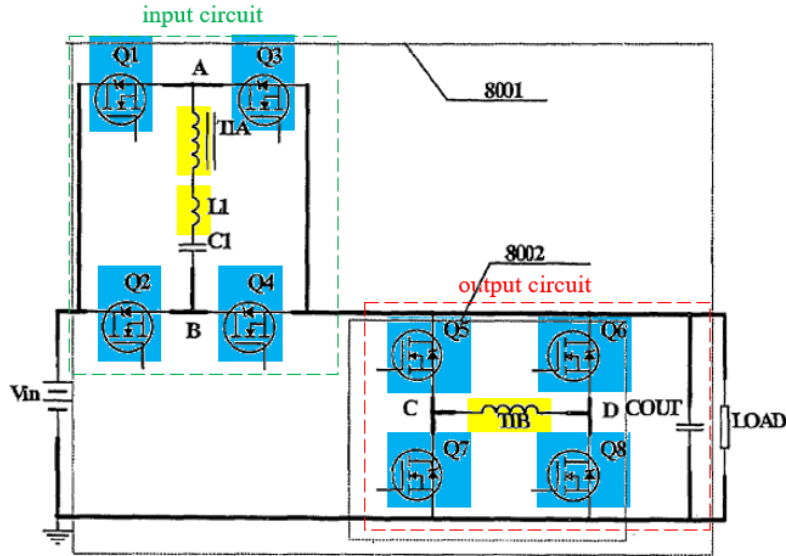
Further, as discussed above, the voltage V_{IN} applied to the input circuit is $V_{in} - V_{out}$, where V_{in} is the DC source voltage V_S . In other words, the voltage applied to the input circuit is equal to the DC source voltage V_S less the output voltage V_{OUT} . Ex. 1003, ¶259. Thus, the input voltage V_{IN} is equal to the DC source voltage V_S minus a number N times the output voltage V_{OUT} , where N is exactly 1. *Id.*

g. Limitation I(g)

Liu discloses that both the input circuit and output circuit of the converter depicted in Figure 15 have inductive components, namely primary transformer winding T1A in the input circuit and secondary transformer winding T1B and inductors L1 and L2 in the output circuit, all highlighted in yellow below. The input and output circuits also comprise power switches, highlighted in blue.



Ex. 1006, Figure 15 (annotations added), 16:18-44; Ex. 1003, ¶260. Both the input circuit and output circuit of Figure 80 also have inductive components, namely primary transformer winding T1A and inductor L1 in the input circuit and secondary transformer winding T1B in the output circuit, all highlighted in yellow below. The input and output circuits also comprise power switches, highlighted in blue.



Ex. 1006, Figure 80 (annotations added), 32:55-33:7; Ex. 1003, ¶261.

h. Limitation 1(h)

Like Huang, Liu discloses that an advantage of its converters is that they can operate in zero voltage switching mode. Ex. 1006, 18:20-31, 36:30-33. As a POSITA would understand, zero voltage switching means that the switches turn on once the voltage across them reaches near zero. Ex. 1003, ¶262. With respect to the converter shown in Figure 15, Liu specifically notes that ZVS “for Q1, Q2, Q3, and Q4 can be achieved by *the leakage inductance of the transformer T1* and by the load current” by using phase-shift PWM control, such as the phase-shift PWM control gate drive scheme depicted in Figure 20. Ex. 1006, 18:24-28 (emphasis added). Using these phase-shift PWM controls, there is a time when Q1 will be turned off while Q4 is still on. Ex. 1003, ¶262. At this time, the current reflected from the secondary side (i.e., the current flowing through the primary winding)

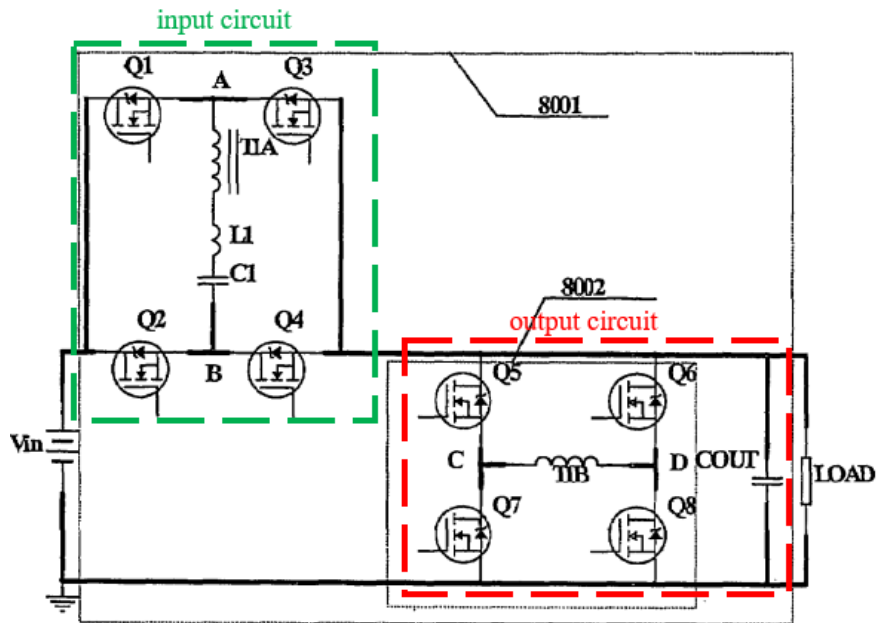
charges the capacitance of Q1. *Id.* At the same time, the antiparallel diode of the off-switch, Q2, provides a path for the current which in turn discharges the capacitance of Q2, reducing the voltage across Q2 to near zero. *Id.* Q2 is then turned on, achieving zero voltage turn on. *Id.* After Q2 is turned on, and while Q5 is still on, the secondary side of the transformer is shorted, causing the primary and secondary sides of the transformer to be decoupled, i.e., electrical energy is prevented from transferring between the windings of the transformer. *Id.* Q4 is then turned off, and switch Q2 is still on. *Id.* In this configuration, the leakage inductance of the transformer will charge the capacitance of Q4 and discharge the capacitance of Q3, reducing the voltage across Q3 to near zero. Q3 is then turned on, achieving zero voltage turn on. *Id.*

With respect to the converter shown in Figure 80, a POSITA would have known that ZVS would be achieved using the resonant tank in the high-side circuit. Ex. 1003, ¶263. Specifically, when switches are off, the resonant tank (including the transformer) resonates. This traverses the voltage across the off switches from zero to their peak, and then back down again to zero. *Id.* The off switches are then turned on, when their voltage is near zero. *Id.*

Thus, the transformers in both Liu's Figure 15 and 80 circuits charges and discharges capacitances in the bus converter reducing a voltage across said one or more switches prior to turning ON said one or more switches.

2. Claim 2

Liu renders obvious claim 1. §V.D.1, *supra*. As can be seen below, the input and output circuits of Liu's Figure 80 embodiment comprise full-bridge circuits, which can be seen in their use of four switches each.



Ex. 1006, Figure 80 (annotations added); Ex. 1003, ¶265. The input circuit comprises transformer primary winding $T1A$, and the output circuit has transformer secondary winding $T1B$. *Id.* $T1A$ and $T1B$ each have a number of turns. *See, e.g.*, 17:5-15 (noting possibility of 2 turns in secondary winding and 3 in primary). As discussed above, the the voltage transformation ratio is a function of a ratio of the first number of turns to the second number of turns, N . §V.D.1.c, *supra*; Ex. 1003, ¶266.

3. Claim 6

Liu renders obvious claim 1. §V.D.1, *supra*. As the '950 Patent itself acknowledges, IBA was known in the art at the time of invention. Ex. 1001, 1:13-35. IBA included a bus converter that included, for example, a DC-DC converter such as that disclosed by Liu. *Id.*; Ex. 1005, Figure 12(b). As previously discussed, a POSITA would have known that a DC-DC converter such as Liu's may be used alone or as part of a bus converter. §§V.D.1.c, V.D.1.d; Ex. 1003, ¶267. Moreover, it was known that bus converters would comprise self-contained assemblies adapted to be installed as units into computing systems. *Id.*

4. Claim 7

Liu renders obvious claim 1. §V.D.1, *supra*. Further, it was known that bus converters and regulators could be assembled onto a circuit board with one another. Ex. 1003, ¶268. And, as claimed in claim 1, it was known that regulators would provide power to a load. *Id.* When the regulator was mounted to the same circuit board as the bus converter, rather than the same circuit board as the load itself, the regulator would necessarily provide power to the integrated circuit as the load. *Id.*

5. Claim 8

Liu renders obvious claim 1. §V.D.1, *supra*. Liu discloses that a snubber circuit may be added to the output circuit (rectifier circuit) to reduce power dissipation. Ex. 1006, 15:24-26. A POSITA would be aware that snubber circuits

act as protection by limiting or stopping voltage spikes. Ex. 1003, ¶269. For example, a snubber circuit may switch voltage amplitude and the rate of its rise, thereby reducing the total power dissipation. *Id.* Snubber circuits operate by *clamping* the voltage spikes. *Id.* Therefore, a POSITA would have understood Liu to disclose connecting a snubber circuit to prevent the output voltage from exceeding a predetermined level. *Id.* Alternatively, a POSITA would have known that the switch controller could be used to monitor the output voltage and, e.g., turn on one synchronous rectifier transistor to short the output capacitor gathering the leakage current or otherwise switch the circuit to prevent the output voltage from exceeding a predetermined level. In this case, the controller is operating as a “clamp circuit.” *Id.*

6. Claim 9

a. Limitation 9(a)

b. Limitation 9(b)

See §§V.D.1.b, V.D.1.c, supra.

c. Limitation 9(c)

See §V.D.1.f, supra.

d. Limitation 9(d)

See §V.D.1.g, supra.

e. Limitation 9(e)

See §V.D.1.h, supra.

7. Claim 10

See §§V.D.6, V.D.2, *supra*.

8. Claim 14

See §§V.D.6, V.D.3, *supra*.

9. Claim 15

See §§V.D.1.d, V.D.1.e, V.D.4, V.D.6, *supra*.

10. Claim 16

a. Limitation 16(a)

b. Limitation 16(b)

See §§V.D.1.b, V.D.1.c, *supra*.

c. Limitation 16(c)

See §V.D.1.d, *supra*.

d. Limitation 16(d)

See §V.D.1.e, *supra*.

e. Limitation 16(e)

See §V.D.1.f, *supra*.

f. Limitation 16(f)

See §V.D.1.g, *supra*.

g. Limitation 16(g)

See §V.D.1.h, *supra*.

11. Claim 17

See §§V.D.2, V.D.10, *supra*.

12. Claim 19

See §§V.D.3, V.D.10, *supra*.

13. Claim 22

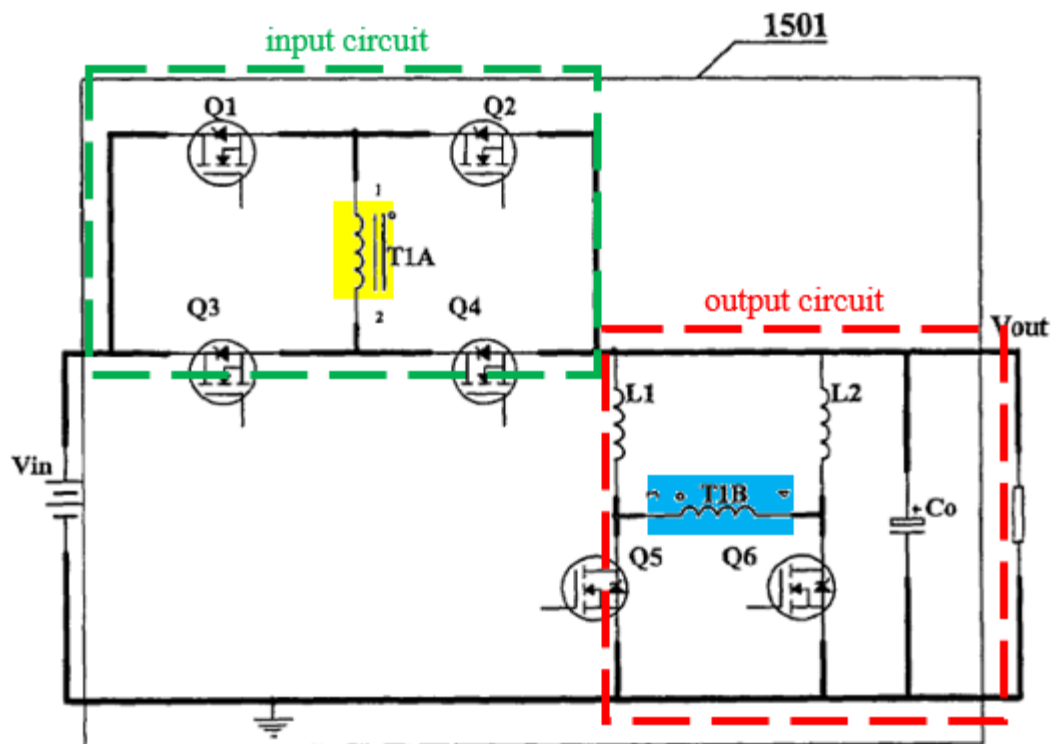
a. Limitation 22(a)

b. Limitation 22(b)

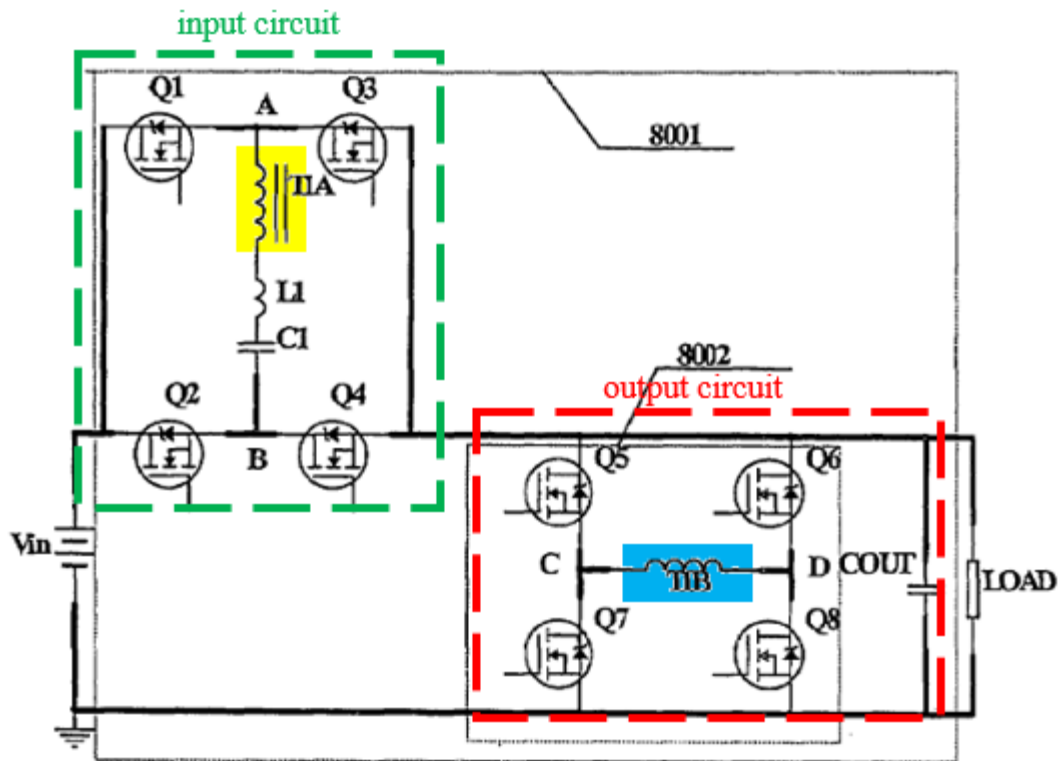
Liu renders obvious this claim limitation for the same reasons discussed above for claim element 1(b). *See* §V.D.1.b, *supra*. As the '950 Patent acknowledges, IBA was known in the art at the time of invention. Ex. 1001, 1:13-35 (describing IBA configuration as prior art); Ex. 1003, ¶285.

c. Limitation 22(c)

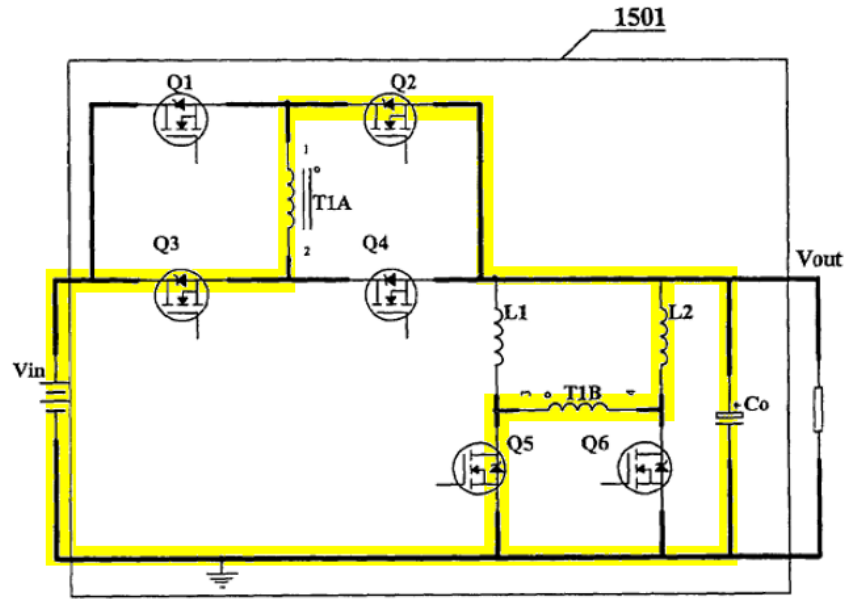
As discussed above, a POSITA would have known that Liu's converters could be used as part of a bus converter. §V.D.1.c, *supra*. The input and output circuits are outlined in green and red, respectively, for both the Figure 15 and Figure 80 embodiments of Liu below. The primary transformer winding within the input circuit is highlighted in yellow while the secondary winding is highlighted in blue.



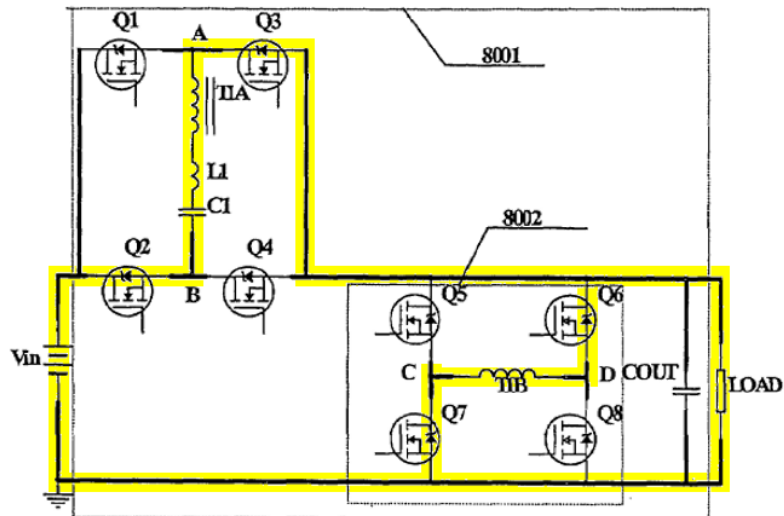
Ex. 1006, Figure 15 (annotations added).



Ex. 1006, Figure 80 (annotations added). Further, the input and output circuits are galvanically connected in series, as can be seen by the direct connection between them (yellow):



Ex. 1006, Figure 15 (annotations added).



Ex. 1006, Figure 80 (annotations added). Liu's Figure 15 and Figure 80 converters are therefore also configured to provide power to a power distribution bus that is not galvanically isolated from the source because they do not provide galvanic

isolation between the source (V_{in}) and the power provided to the power distribution bus (V_o). Ex. 1003, ¶287-289.

d. Limitation 22(d)

See §V.D.1.e, supra.

14. Claim 23

a. Limitation 23(a)

See §§V.D.13, V.D.1.c, supra.

b. Limitation 23(b)

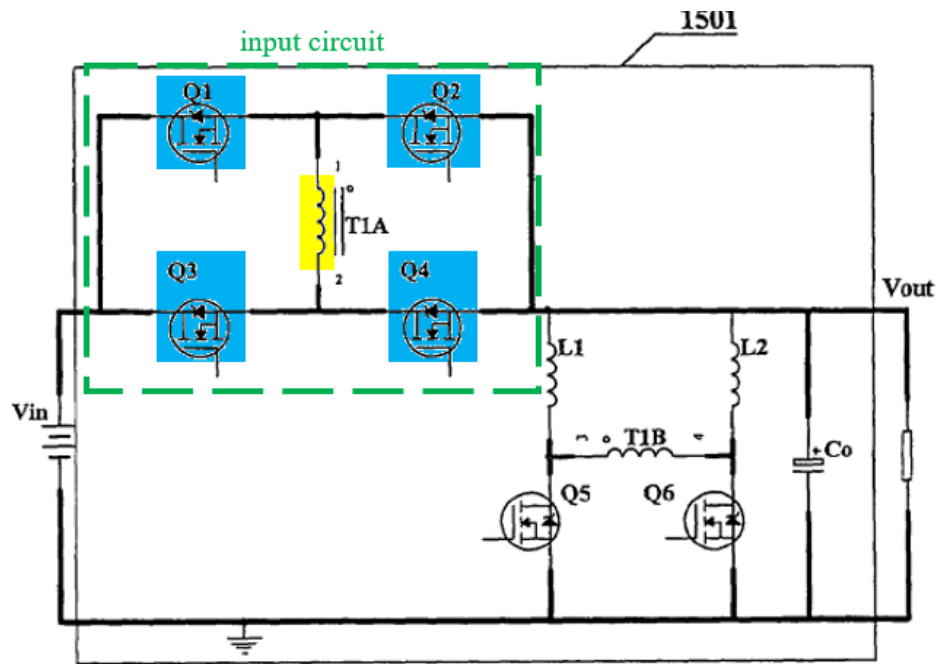
See §V.D.1.f, supra.

15. Claim 24

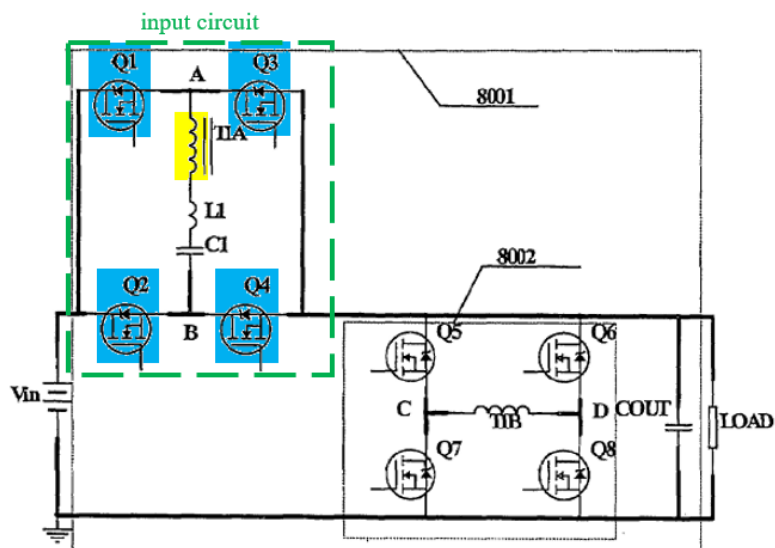
See §§V.D.13, V.D.3, supra.

16. Claim 25

Liu renders obvious claim 1. §V.D.1, *supra*. Below, the input circuits of Liu's Figure 15 and Figure 80 embodiments are outlined in green, with the transformer primary winding highlighted in yellow and the primary switches connected to the transformer primary winding highlighted in blue:

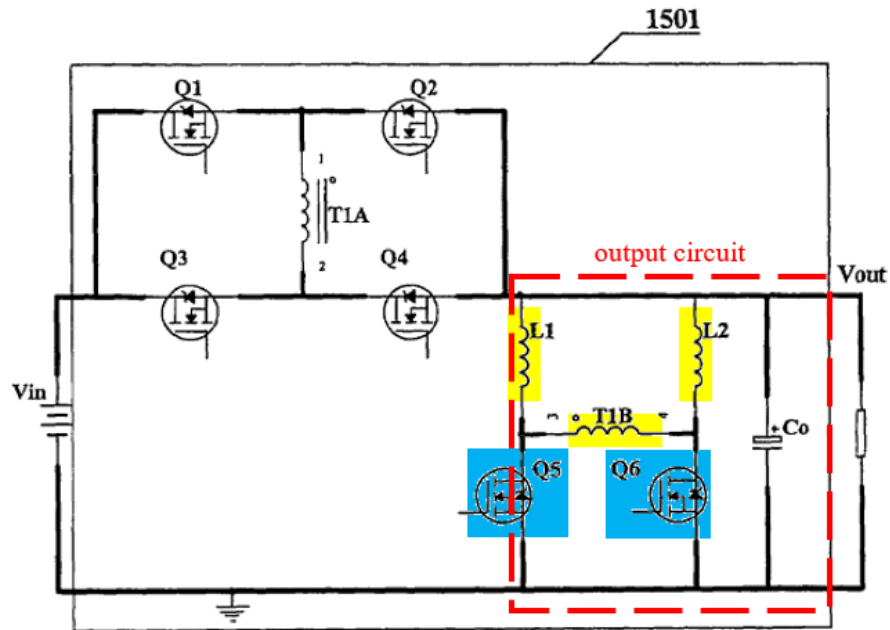


Ex. 1006, Figure 15 (annotations added).

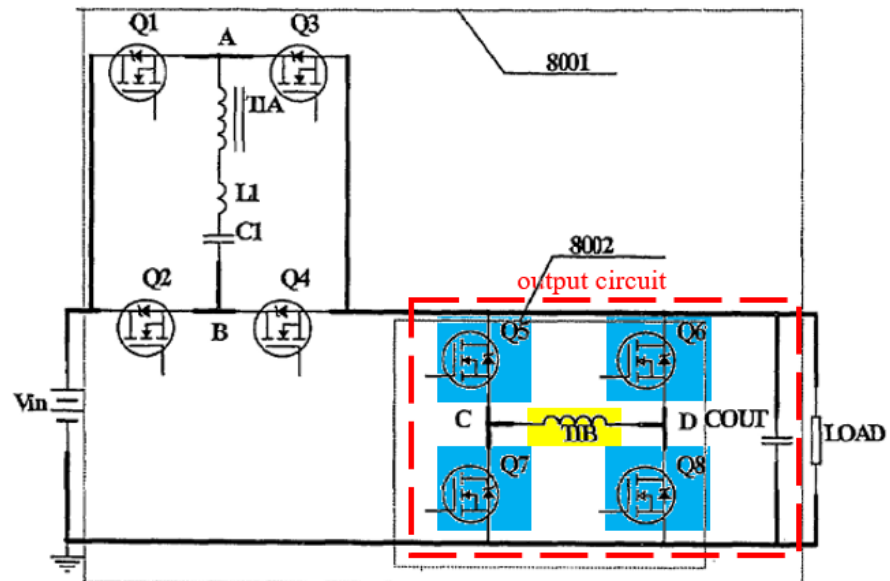


Ex. 1006, Figure 80 (annotations added); Ex. 1003, ¶294. The output circuits are outlined in red below, with the transformer secondary windings highlighted in

yellow and the secondary switches connected to the secondary winding highlighted in blue:

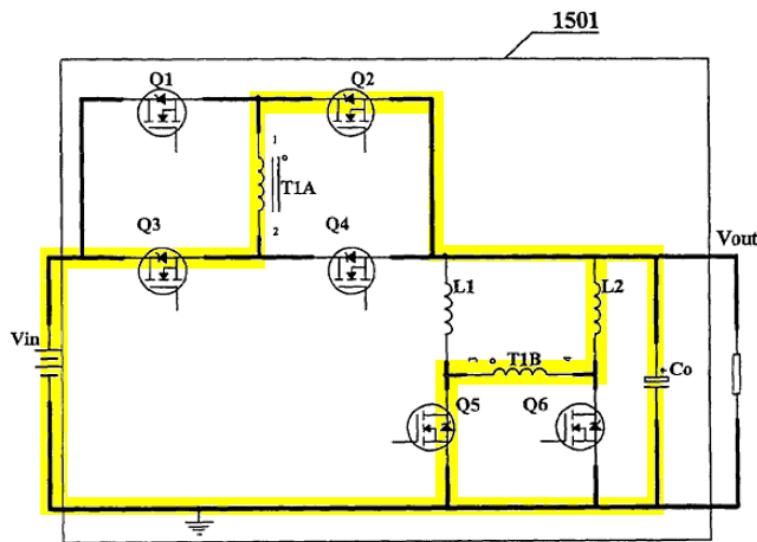


Ex. 1006, Figure 15 (annotations added).

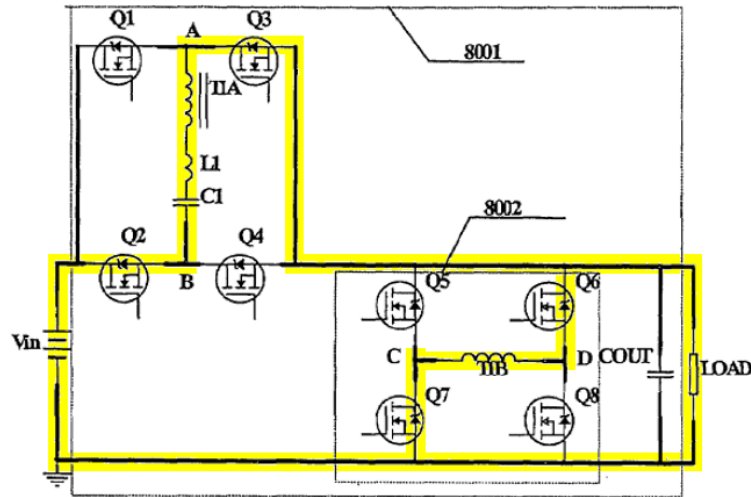


Ex. 1006, Figure 80 (annotations added); Ex. 1003, ¶295.

As discussed in detail above, the primary and secondary switches are operated (i.e., switched on or off, closed or open). §V.D.1.h. A POSITA would have understood that operation of the switches and converter would require a controller. Ex. 1003, ¶296. In Figure 15, the primary and secondary windings are connected in series when either of Q1, Q4, and Q6 or Q2, Q3, and Q5 are on/closed. *Id.* In Figure 80, the primary and secondary windings are connected in series when either of Q1, Q4, Q5, and Q8 or Q2, Q3, Q6, and Q7 are on/closed. *Id.*



Ex. 1006, Figure 15 (annotations added).



Ex. 1006, Figure 80 (annotations added).

17. **Claim 26**

See §§V.D.6, V.D.16, *supra*.

18. **Claim 27**

See §§V.D.10, V.D.16, *supra*.

19. **Claim 28**

See §§V.D.1, V.D.1.h, *supra*.

20. **Claim 29**

a. *Limitation 29(a)*

b. *Limitation 29(b)*

See §V.D.1.b, *supra*.

c. *Limitation 29(c)*

See §V.D.1.c, *supra*.

d. Limitation 29(d)

See §V.D.1.d, supra.

e. Limitation 29(e)

See §V.D.1.e, supra.

f. Limitation 29(f)

See §V.D.1.f, supra.

g. Limitation 29(g)

See §V.D.1.g, supra.

h. Limitation 29(h)

See §V.D.1.h, supra.

21. Claim 30

See §§V.D.20, V.D.1.h, supra.

22. Claim 31

a. Limitation 31(a)

b. Limitation 31(b)

See §V.D.1.b, supra.

c. Limitation 31(c)

See §V.D.1.c, supra.

d. Limitation 31(d)

See §V.D.1.d, supra.

e. Limitation 31(e)

See §V.D.1.e, supra.

f. Limitation 31(f)

See §V.D.1.c, supra.

g. Limitation 31(g)

See §V.D.1.f, supra.

23. Claim 32

a. Limitation 32(a)

b. Limitation 32(b)

See §V.D.1.b, supra.

c. Limitation 32(c)

See §V.D.1.c, supra.

d. Limitation 32(d)

See §V.D.1.d, supra.

e. Limitation 32(e)

See §V.D.1.e, supra.

f. Limitation 32(f)

See §V.D.1.c, supra.

g. Limitation 32(g)

See §V.D.1.f, supra.

24. Claim 33

a. Limitation 33(a)

b. Limitation 33(b)

See §V.D.1.c, supra.

c. Limitation 33(c)

See §V.D.1.f, *supra*.

d. Limitation 33(d)

See §V.D.1.g, *supra*.

e. Limitation 33(e)

See §V.D.1.h, *supra*.

25. Claim 35

See §§V.D.24, V.D.19, *supra*.

26. Claim 36

See §§V.D.24, V.D.1.f, *supra*.

27. Claim 37

See §§V.D.24, V.D.2, *supra*.

28. Claim 39

See §§V.D.13, V.D.1.g, V.D.1.h, *supra*.

29. Claim 40

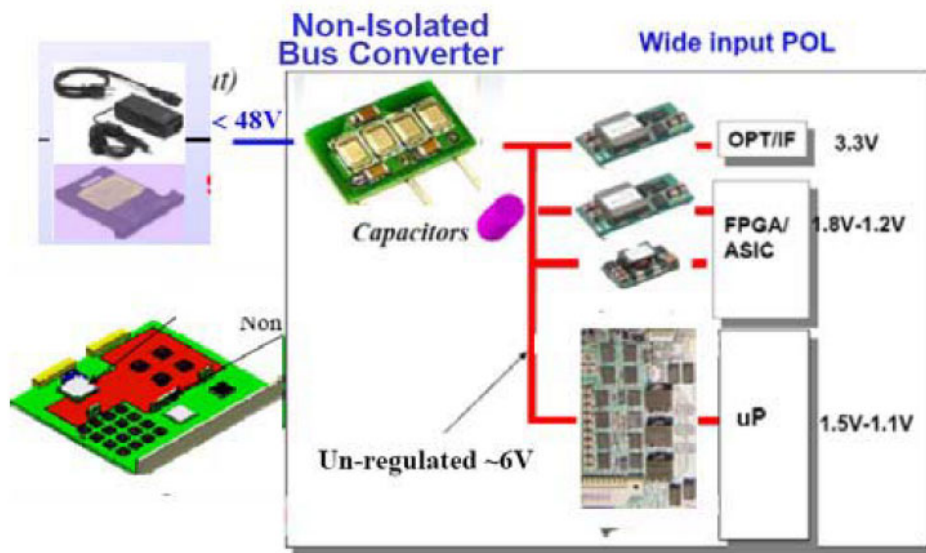
See §§V.D.13, V.D.4, *supra*.

**E. Ground VI: Claims 1, 2, 6-8, 10, 14-17, 19, 22-33, 35-37, and 39-40
Are Obvious Over Liu In View Of Lee**

1. Motivation to Combine

A POSITA would have been motivated to combine Liu and Lee. Ex. 1003, ¶¶329-334. Liu discloses a variety of DC-DC converters that can achieve zero voltage switching and other efficiencies. *See* Ex. 1006, 36:20-33. Lee discusses

design challenges and opportunities for a variety of power supply applications, including DC-DC converters. Ex. 1008, 1. Opportunities discussed include cost savings, performance improvements, and chip size. *Id.* One specific proposal is a non-isolated intermediate bus architecture, depicted below. *Id.*, 12, Figure 43. This architecture includes a non-isolated bus converter designed to minimize switching losses and body diode losses at high switching frequencies and increase circuit efficiency. *Id.*, 11-12.



Ex. 1008, Figure 43. Lee discloses using a “voltage divider” DC-DC converter that can achieve high power density and “ultra-high efficiency in the whole load range with capability to handle over load conditions” as the non-isolated bus converter in Lee’s architecture. *Id.* at 12.

It would have been obvious to a POSITA to use the DC-DC converters disclosed in Liu in the intermediate bus architecture disclosed in Lee. Ex. 1003,

¶331. **First**, a POSITA would understand that the “non-isolated bus converter” of Lee’s proposed architecture is a power converting circuit that could take many forms, including the DC-DC converter disclosed by Liu. *Id.* **Second**, Liu contemplates the use of its converters in, for example, personal computer applications. *See, e.g.*, Ex. 1006, 1:37-47, 13:3-6. It would have been obvious to a POSITA to try Liu’s higher efficiency converters as the non-isolated bus converters in the non-isolated intermediate bus architecture proposed by Lee in place of Lee’s DC-DC “voltage divider”: there were limited options for non-isolated converters, and Liu’s non-isolated DC-DC converters were specifically designed for the same purpose as Lee’s voltage divider, i.e., to improve operating efficiency. Ex. 1006, 36:20-33; Ex. 1008, 12; Ex. 1003, ¶332. A POSITA would have had a reasonable expectation of success in using Liu’s converters in the intermediate bus architecture disclosed in Lee because, as shown in Lee Figure 43, it was contemplated that the non-isolated bus converter would be a modular, and thus replaceable, component.

Third, a POSITA would have specifically been interested in enhancing efficiency in light of Both Lee and Liu’s focus on improving existing converter design to reduce switching and transformer losses. *See, e.g.*, Ex. 1006, 36:20-33; Ex. 1008, 11-12. Both Liu and Lee indicate that a motivation to implement their disclosed inventions is to improve the efficiency of existing circuit design. *See,*

e.g., id. Thus, a POSITA would be counseled to improve the efficiency of the circuit design in other ways, such as including Liu’s improved converters in Lee’s improved architecture design to improve the overall power conversion efficiency. *See* Ex. 1003, ¶333.

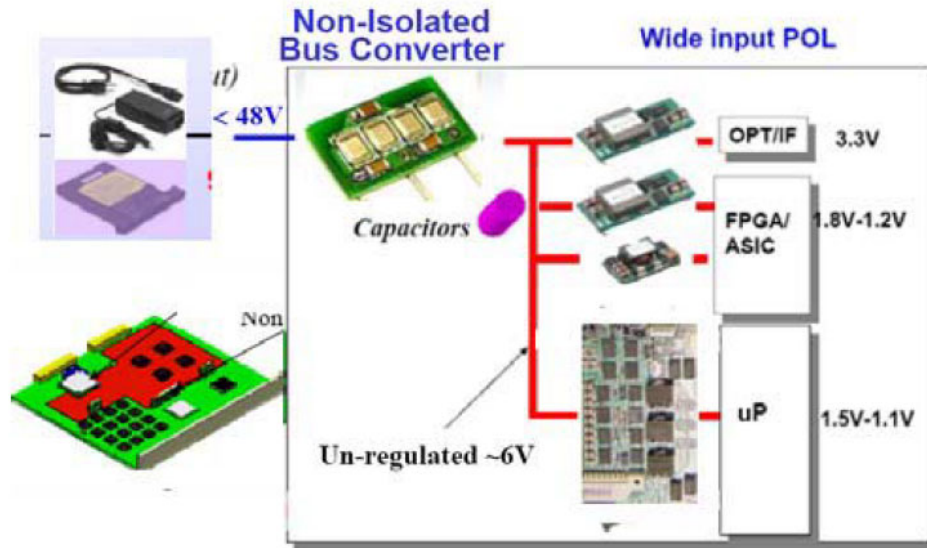
Fourth, use of Lee’s intermediate bus architecture with the DC-DC converters disclosed in Liu would have involved mere substitution of one known element (Lee’s “voltage divider” as the non-isolated bus converter shown in Figure 43) for another (Liu’s DC-DC converters as the non-isolated bus converter) to obtain predictable results (more efficient power conversion). Ex. 1003, ¶334. A POSITA would have recognized using the Liu’s converters to be an easy modification to make to Lee’s intermediate bus architecture using standard techniques known in the art. *Id.*

2. Claim 1

a. Limitation 1(a)

b. Limitation 1(b)

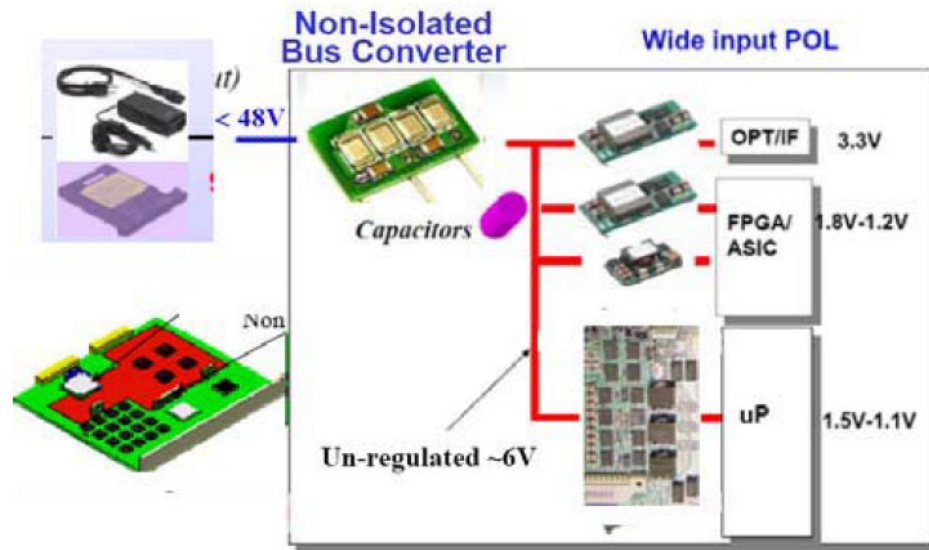
Lee’s proposed intermediate bus architecture (a power distribution system) includes a 48V DC source voltage:



Ex. 1008, Figure 43; *see also id.*, 11-12 (voltage divider disclosed by Lee as a non-isolated bus converter is a DC-DC converter); Ex. 1003, ¶335. Liu likewise discloses this claim limitation. *See* §V.D.1.b.

c. Limitation 1(c)

Liu's Figure 15 and 80 converters would operate as the non-isolated bus converter Lee's intermediate bus architecture in the combination of Liu and Lee. Ex. 1003, ¶337. Lee discloses that the non-isolated bus converter is unregulated, meaning that the transformation ratio of the converter is fixed. Ex. 1008, Figure 43; Ex. 1003, ¶337. When Liu's non-isolated converter is substituted into Lee's architecture as the bus converter, the transformation ratio (V_{OUT}/V_S) is therefore fixed. *Id.* Because for Liu's converters $V_{IN}=V_S-V_{OUT}$, V_{OUT}/V_{IN} is necessarily also fixed as it depends on other fixed values. *Id.*

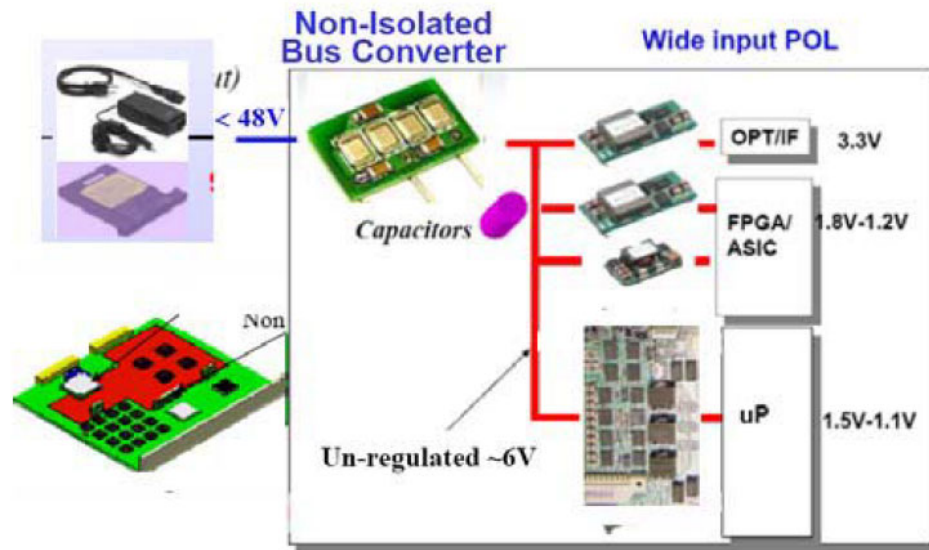


Ex. 1008, Figure 43. Huang's converter comprises the remainder of this limitation.

See §V.D.1.c.

d. Limitation 1(d)

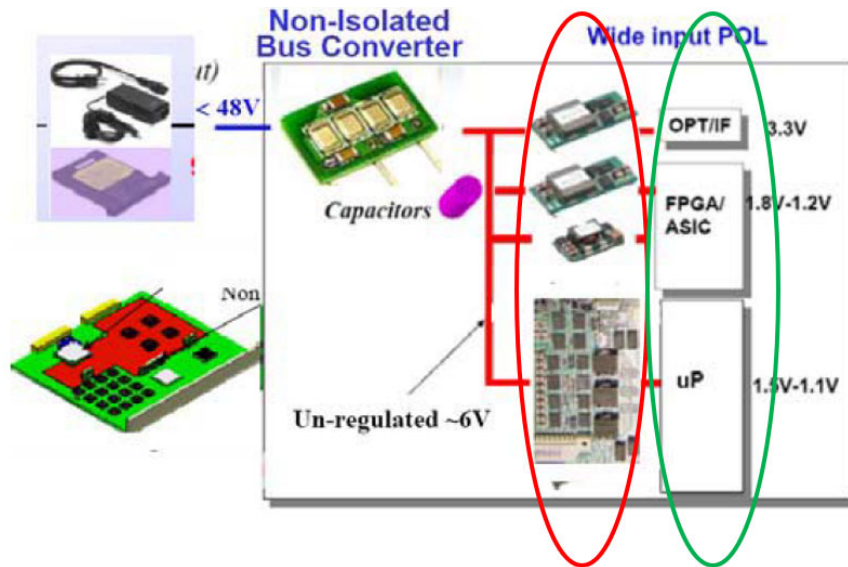
Lee's intermediate bus architecture includes a power distribution bus (red lines in figure below) connected to distribute power from the output circuit of the non-isolated bus converter (Liu's Figure 15 or 80 converter) at the output voltage V_{OUT} . See Ex. 1008, Figure 43; §V.D.1.d.



Ex. 1008, Figure 43; Ex. 1003, ¶339.

e. Limitation 1(e)

Lee's intermediate bus architecture includes a plurality of regulators, each regulator comprising an input connected to receive power from the output circuit of the bus converter and an output connected to supply power to a load. Ex. 1008, 11-12; Ex. 1003, ¶340. The circuits circled in red below are the regulators, what Lee refers to as "wide input POLs," or point-of-load DC-DC converters. Ex. 1008, 8, 11-12. The white boxes circled in green are the loads; for example, the center load is an FPGA or ASIC, two types of integrated circuits that ordinarily are off-the-shelf components. *Id.*; Ex. 1003, ¶340.



Ex. 1008, Figure 43 (annotations added). A POSITA would have recognized the regulators to be distanced from the bus converter for a number of reasons including at least because the bus converter is a separate component from the POL DC-DC converters and the POL DC-DC converters would have been part of the circuit boards comprising the loads themselves (i.e., the POL converters were local to the load, not the bus converter). Ex. 1003, ¶341.

f. Limitation 1(f)

See §V.D.1.f (claim 1(f)).

g. Limitation 1(g)

See §V.D.1.g (claim 1(g)).

h. Limitation 1(h)

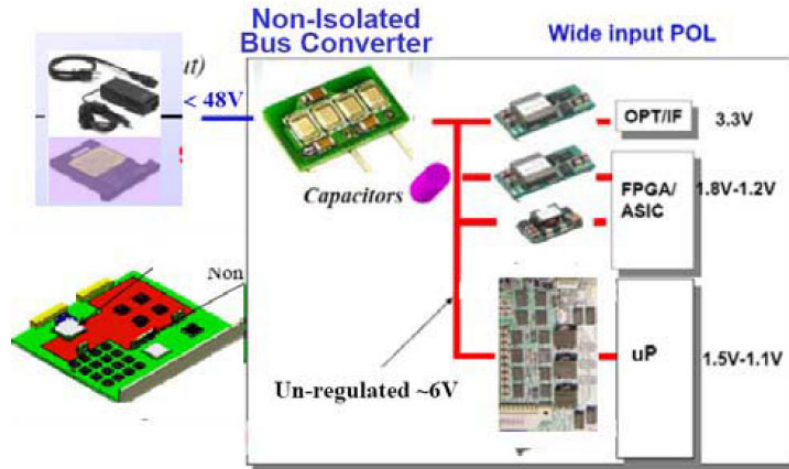
See §V.D.1.h (claim 1(h)).

3. Claim 2

See §V.D.2 (claim 2).

4. Claim 6

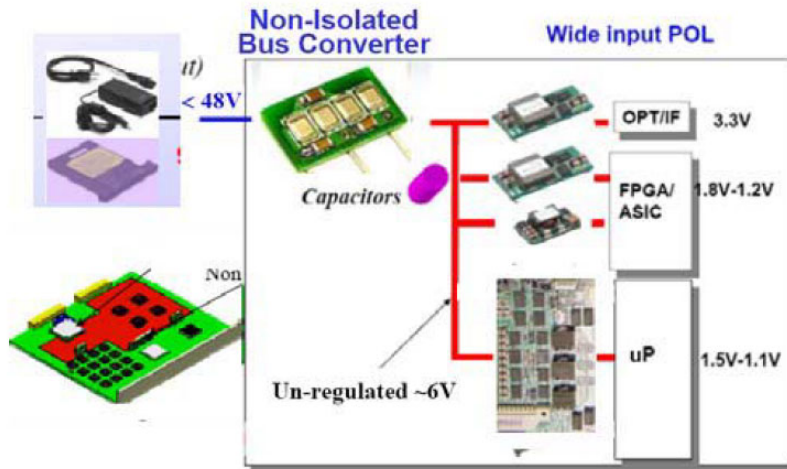
As seen in Figure 43 of Lee, the non-isolated bus converter of the proposed intermediate bus architecture is a self-contained assembly adapted to be installed as a unit:



Ex. 1008, Figure 43; Ex. 1003, ¶346.

5. Claim 7

As seen in Figure 43 of Lee, the non-isolated bus converter and the regulators are assembled to circuit boards in the proposed intermediate bus architecture:



Ex. 1008, Figure 43. At least one regulator in Lee is configured to supply power to an integrated circuit; specifically, the regulators are shown connected to an FPGA or ASIC, which is a type of integrated circuit. Ex. 1003, ¶347-348.

6. Claim 8 and 10

See §§V.D.5, V.D.7.

7. Claim 14

See §§V.D.6, V.E.3.

8. Claim 15

See §§V.D.1.e, V.D.4, V.D.6, V.D.9, V.E.2.e, V.E.5.

9. Claim 16

a. Limitation 16(a)

b. Limitation 16(b)

See §§V.E.2.b, V.E.2.c.

c. Limitation 16(c)

See §§V.D.1.d, V.E.2.d.

d. Limitation 16(d)

See §§V.D.1.e, V.E.2.e.

e. Limitation 16(e)

See §§V.D.1.f, V.E.2.f.

f. Limitation 16(f)

See §§V.D.1.g, V.E.2.g.

g. Limitation 16(g)

See §§V.D.1.h, V.E.2.h.

10. Claim 17

See §§V.D.10, V.D.11, V.E.9.

11. Claim 19

See §§V.D.10, V.D.12, V.E.9, V.E.4.

12. Claim 22

a. Limitation 22(a)

b. Limitation 22(b)

See §§V.D.1.b, V.D.13.b, V.E.2.b.

c. Limitation 22(c)

See §§V.D.1.c, V.D.13.c, V.E.2.c.

d. Limitation 22(d)

See §§V.D.1.e, V.D.13.e, V.E.2.e.

13. Claim 23

See §§V.D.13, V.D.1.c, V.D.1.f, V.E.12, V.E.2.c, V.E.2.f.

14. Claim 24

See §§V.D.3, V.D.13, V.E.12, V.E.4.

15. Claims 25-28

See §§V.D.16-19 (claims 25-28).

16. Claim 29

a. Limitation 29(a)

b. Limitation 29(b)

See §§V.D.1.b, V.E.2.b.

c. Limitation 29(c)

See §§V.D.1.c, V.E.2.c.

d. Limitation 29(d)

See §§V.D.1.d, V.E.2.d.

e. Limitation 29(e)

See §§V.D.1.e, V.E.2.e.

f. Limitation 29(f)

See §§V.D.1.f, V.E.2.f.

g. Limitation 29(g)

See §§V.D.1.g, V.E.2.g.

h. Limitation 29(h)

See §§V.D.1.h, V.E.2.h.

17. Claim 30

See §§V.D.20, V.D.21, V.E.16.

18. Claim 31

a. Limitation 31(a)

b. Limitation 31(b)

See §§V.D.1.b, V.E.2.b.

c. Limitation 31(c)

See §§V.D.1.c, V.E.2.c.

d. Limitation 31(d)

See §§V.D.1.d, V.E.2.d.

e. Limitation 31(e)

See §§V.D.1.e, V.E.2.e.

f. Limitation 31(f)

See §§V.D.1.c, V.E.2.c.

g. Limitation 31(g)

See §§V.D.1.f, V.E.2.f.

19. Claim 32

a. Limitation 32(a)

b. Limitation 32(b)

See §§V.D.1.b, V.E.2.b.

c. Limitation 32(c)

See §§V.D.1.c, V.E.2.c.

d. Limitation 32(d)

See §§V.D.1.d, V.E.2.d.

e. Limitation 32(e)

See §§V.D.1.e, V.E.2.e.

f. Limitation 32(f)

See §§V.D.1.c, V.E.2.c.

g. Limitation 32(g)

See §§V.D.1.f, V.E.2.f.

20. Claim 33

a. Limitation 33(a)

b. Limitation 33(b)

See §§V.D.1.c, V.E.2.c.

c. Limitation 33(c)

See §§V.D.1.f, V.E.2.f.

d. Limitation 33(d)

See §§V.D.1.g, V.E.2.g.

e. Limitation 33(e)

See §§V.D.1.h, V.E.2.h.

21. Claims 35-37, 39

See §§V.D.24, V.D.25-27, V.D.28, V.E.20.

22. Claim 40

See §§V.D.4, V.D.13, V.E.5, V.E.12, V.E.5.

VI. SECONDARY CONSIDERATIONS

There are no secondary considerations of non-obviousness with a provable nexus to the claimed invention of the '950 Patent. Ex. 1003, ¶393. Contrary to Patent Owner's allegations, Petitioner did not copy Patent Owner's power converters, and there is no evidence that any purported success or praise of Patent Owner or its power converters is related to the technology claimed in the '950 Patent.

VII. NO JUSTIFICATION FOR DISCRETIONARY DENIAL

The Board should decline to exercise its discretion to deny institution of this Petition. On June 21, 2022, the USPTO issued a memorandum in which the Director clarified that "[t]he PTAB will not discretionarily deny petitions based on applying *Fintiv*¹ to a parallel ITC proceeding." See Director Vidal, Memorandum, "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation," 5–7 (June 21, 2022) ("Guidance Memo"). This Guidance Memo is followed by the Board and should be applied here because, as noted in Section VIII.B below, the '481 Patent is part of a parallel ITC proceeding and the related district court proceeding has been stayed. *Id.*; see also *Roku, Inc. v. Universal Electronics Inc.*, IPR2021-00263, Paper 19 at 7-9 (P.T.A.B. Feb. 8, 2023).

¹ *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential) ("*Fintiv*").

Furthermore, even applying *Fintiv* in view of the related district court case, discretionary denial is not warranted. *Factor 1* weighs against discretionary denial because a stay of the district court case has been granted “until the resolution of [the ITC proceedings] becomes final, including any appeals and until the Commission proceedings are no longer subject to judicial review.” *Vicor Corp. v. Delta Electronics, Inc.*, 2:23-CV-00323-JRG-RSP, Dkt. 35 (Stay Order) (E.D. Tex. Aug. 22, 2023). Because the target date for completion of the ITC investigation is not until February 3, 2025,² and factoring in potential appeals, the district court stay would likely extend through the duration of this proceeding, if instituted.

Given the district court stay under Factor 1, *Factors 2–4* favor not denying institution (no trial date has been set; there is little investment in the case by the district court and parties; and little overlap, other than the ’481 patent itself, between issues raised between the Petition and district court case). *Factor 5* favors against denial because Petitioner is a defendant in the district court proceeding *along with eight (8) other parties*, as noted in Section VIII.B. *Fintiv*, 13–14. As for Factor 6, even if the Board determines that the other *Fintiv* factors favor discretionary denial, the Board must also consider whether the Petition presents

² *Certain Power Converter Modules and Computing Systems Containing the Same*, Inv. No. 337-TA-1370, USITC Order No. 8 (Setting the Procedural Schedule) (Sep. 25, 2023).

compelling merits. *CommScope Techs. LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 at 5 (Feb. 27, 2023) (precedential).

Here, *Fintiv* factors 1 through 5 weigh in favor of not denying institution. Further still, each ground in the Petition presents compelling evidence of unpatentability, and none of the references presented in this Petition were before the Examiner during prosecution. Given the objectives of IPRs, the Board must decline to exercise its discretion to deny institution. Guidance Memo at 4–5.

VIII. MANDATORY NOTICES

As set forth below and pursuant to 37 C.F.R. § 42.8(a)(1), the following mandatory notices are provided as part of this Petition.

A. Real Party in Interest Under 37 C.F.R. § 42.8(b)(1)

Delta Electronics, Inc.; Delta Electronics (Americas), Ltd.; Delta Electronics (USA), Inc.; Cyntec Co., Ltd.; Delta Electronics (Thailand) Public Company Limited; and DET Logistics (USA) Corporation are the real parties-in-interest.³

³ The following entities are not real parties-in-interest, but are being disclosed for transparency because they have also been, or may be, named as respondents in the related ITC investigation referenced in subsection B: Hon Hai Precision Industry Co. Ltd.; Foxconn Industrial Internet Co. Ltd.; FII USA Inc.; Ingrasys Technology Inc.; Ingrasys Technology USA Inc.; Quanta Computer, Inc.;

B. Related Matters

On July 12, 2023, Vicor Corporation filed two complaints alleging infringement of the '950 Patent by Petitioners and others: (1) *Power Converter Modules and Computing Systems Containing the Same*; Inv. No. 337-TA-3688, and (2) *Vicor Corporation v. Delta Electronics, Inc. et al.*, 2-23-cv-00323 (E.D. Tex.).

C. Lead and Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Pursuant to 37 C.F.R. § 42.8(b)(3), Petitioner provides the following designation of counsel:

Quanta Computer USA Inc.; Quanta Cloud Technology, Inc.; Quanta Cloud Technology USA LLC; QCH, Inc.

Lead Counsel	Back-Up Counsel
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Petitioner concurrently submits a Power of Attorney, 37 C.F.R. §42.10(b), and consents to electronic service directed to the following email address: 950_IPR_Delta@kirkland.com.

IX. PAYMENT OF FEES UNDER 37 C.F.R. § 42.103

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R. § 42.15(a)(1) for this Petition to Deposit Account No. 506092, consistent with the requested review of 34 claims. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition to be charged to the above-referenced deposit account.

X. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.104(A)

Petitioner certifies that the '950 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the claims on the grounds identified in this Petition. Petitioner certifies: (1) Petitioner is not the owner of the '950 Patent; (2) Petitioner (or any real party-in-interest) has not filed a civil action challenging the validity of any claim of the '950 Patent; (3) Petitioner files this Petition within one year of the date they was served with a complaint asserting infringement of the '950 Patent; (4) estoppel provisions of 35 U.S.C. §315(e)(1) do not prohibit this IPR; and (5) this Petition is filed after the '950 Patent was granted.

XI. CONCLUSION

Petitioner requests institution of an IPR and cancellation of the Challenged Claims.

Dated: November 2, 2023

Respectfully submitted,

/s/ Russell E. Levine

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APPENDIX OF CHALLENGED CLAIMS

Limitation	Claim Language
1(a)	An apparatus comprising:
1(b)	a power distribution system comprising a source for providing power at a DC source voltage V_S ;
1(c)	a bus converter comprising an input circuit and an output circuit, the bus converter being adapted to convert power from the input circuit to the output circuit at a substantially fixed voltage transformation ratio, K_{DC} , at an output current, wherein an input voltage V_{IN} is applied to the input circuit and an output voltage V_{OUT} is produced by the output of the bus converter, and wherein the substantially fixed voltage transformation ratio can be represented as $K_{DC}=V_{OUT}/V_{IN}$;
1(d)	a power distribution bus connected to distribute power from the output circuit of the bus converter at the output voltage V_{OUT} ; and
1(e)	a plurality of regulators, wherein each regulator comprises a regulator input connected to the power distribution bus to receive power from the output circuit of the bus converter and a regulator output connected to supply power to a respective load, the plurality of regulators each being separated by a distance from the bus converter;
1(f)	wherein the input circuit of the bus converter and at least a portion of the output circuit of the bus converter are galvanically connected in series across the source such that an absolute value of the input voltage V_{IN} applied to the input circuit is approximately equal to the absolute value of the DC source voltage V_S minus a number N times the absolute value of the output voltage V_{OUT} , where N is at least 1;
1(g)	wherein the bus converter comprises an inductive component and one or more power switches in the input circuit, the output circuit, or both; and
1(h)	wherein a current flowing in the inductive component charges and discharges capacitances in the bus converter reducing a voltage across said one or more switches prior to turning ON said one or more switches.
2	The apparatus of claim 1, wherein both the input circuit and the output circuit comprise full-bridge circuits, wherein the

	input circuit comprises a winding having a first number of turns, wherein the output circuit comprises a winding having a second number of turns, and wherein the voltage transformation ratio is a function of a ratio of the first number of turns to the second number of turns.
5(a)	The apparatus of claim 1, wherein the bus converter comprises: a transformer, and a resonant circuit including the transformer having a characteristic resonant frequency and period, the input circuit including two or more primary switches connected to drive the resonant circuit and the output circuit being connected to receive power from the transformer; and
5(b)	a switch controller adapted to operate the primary switches in a series of converter operating cycles, each converter operating cycle characterized by two power transfer intervals of essentially equal duration each interval having a duration less than the characteristics resonant period, during which one or more of the primary switches are ON and power is transferred from the input to the output via the transformer.
6	The apparatus of claim 1, wherein the bus converter is a self-contained assembly adapted to be installed as a unit.
7	The apparatus of claim 1, further comprising a circuit board, wherein the bus converter and at least one regulator are assembled to the circuit board, and the regulator is configured to supply power to an integrated circuit.
9(a)	An apparatus comprising:
9(b)	a power converter comprising an input circuit and an output circuit, wherein the power converter is configured to receive power from a power distribution system comprising a source for providing power at a DC source voltage V_S , the power converter being adapted to convert power from the input circuit to the output circuit at a substantially fixed voltage transformation ratio, K_{DC} , at an output current, wherein an input voltage V_{IN} is applied to the input circuit and an output voltage V_{OUT} is produced by the output of the power converter, and wherein the substantially fixed voltage transformation ratio can be represented as $K_{DC}=V_{OUT}/V_{IN}$, wherein the power converter further comprises:
9(c)	a series connection between the input circuit of the power

	converter and at least a portion of the output circuit of the power converter across the source, such that an absolute value of the input voltage V_{IN} applied to the input circuit is approximately equal to the absolute value of the DC source voltage V_S minus a number N times the absolute value of the output voltage V_{OUT} , where N is at least 1
9(d)	wherein the power converter comprises an inductive component and one or more power switches in the input circuit, the output circuit, or both; and
9(e)	wherein a current flowing in the inductive component charges and discharges capacitances in the power converter reducing a voltage across said one or more switches prior to turning ON said one or more switches.
10	The apparatus of claim 9, wherein both the input circuit and the output circuit comprise full-bridge circuits, wherein the input circuit comprises a winding having a first number of turns, wherein the output circuit comprises a winding having a second number of turns, and wherein the voltage transformation ratio is a function of a ratio of the first number of turns to the second number of turns.
13(a)	The apparatus of claim 9, wherein the power converter comprises: a transformer, and a resonant circuit including the transformer having a characteristic resonant frequency and period, the input circuit including two or more primary switches connected to drive the resonant circuit and the output circuit being connected to receive power from the transformer; and
13(b)	a switch controller adapted to operate the primary switches in a series of converter operating cycles, each converter operating cycle characterized by two power transfer intervals of essentially equal duration each interval having a duration less than the characteristics resonant period, during which one or more of the primary switches are ON and power is transferred from the input to the output via the transformer.
14	The apparatus of claim 9, wherein the power converter is part of a bus converter that is a self-contained assembly adapted to be installed as a unit.
15	The apparatus of claim 9, further comprising a circuit board, and wherein the power converter is configured to supply

	power to a plurality of regulators over a power distribution bus, the regulators disposed at a distance to the power converter, and wherein at least one of the regulators is assembled to the circuit board and configured to supply power to an integrated circuit.
16(a)	An apparatus comprising:
16(b)	a bus converter comprising an input circuit and an output circuit, wherein the bus converter is configured to receive power from a power distribution system comprising a source for providing power at a DC source voltage V_S , the bus converter being adapted to convert power from the input circuit to the output circuit at a substantially fixed voltage transformation ratio, K_{DC} , at an output current, wherein an input voltage V_{IN} is applied to the input circuit and an output voltage V_{OUT} is produced by the output of the bus converter, and wherein the substantially fixed voltage transformation ratio can be represented as $K_{DC}=V_{OUT}/V_{IN}$;
16(c)	a power distribution bus connected to distribute power from the output circuit of the bus converter at the output voltage V_{OUT} ; and
16(d)	a plurality of regulators, wherein each regulator comprises a regulator input connected to the power distribution bus to receive power from the output circuit of the bus converter and a regulator output connected to supply power to a respective load, the plurality of regulators each being separated by a distance from the bus converter;
16(e)	wherein the input circuit of the bus converter and at least a portion of the output circuit of the bus converter are connected in series across the source such that an absolute value of the input voltage V_{IN} applied to the input circuit is approximately equal to the absolute value of the DC source voltage V_S minus a number N times the absolute value of the output voltage V_{OUT} , where N is at least 1;
16(f)	wherein the bus converter comprises an inductive component and one or more power switches in the input circuit, the output circuit, or both; and
16(g)	wherein a current flowing in the inductive component charges and discharges capacitances in the bus converter reducing a voltage across said one or more switches prior to turning ON

	said one or more switches.
19	The apparatus of claim 16, wherein the bus converter is a self-contained assembly adapted to be installed as a unit.
21(a)	The apparatus of claim 16, wherein the bus converter comprises: a transformer, and a resonant circuit including the transformer having a characteristic resonant frequency and period, the input circuit including two or more primary switches connected to drive the resonant circuit and the output circuit being connected to receive power from the transformer; and
21(b)	a switch controller adapted to operate the primary switches in a series of converter operating cycles, each converter operating cycle characterized by two power transfer intervals of essentially equal duration each interval having a duration less than the characteristics resonant period, during which one or more of the primary switches are ON and power is transferred from the input to the output via the transformer.
22(a)	An apparatus comprising:
22(b)	an intermediate bus architecture power distribution system for an electrical system comprising a source for providing power at a DC source voltage;
22(c)	a circuit board comprising a bus converter, the bus converter comprising an input circuit, the input circuit comprising a primary transformer winding, the bus converter further comprising an output circuit, the output circuit comprising a secondary transformer winding, wherein the primary and secondary transformer windings are galvanically connected in series, and wherein the bus converter is configured to provide power to a power distribution bus that is not galvanically isolated from the source; and
22(d)	the circuit board further comprising a plurality of regulators, wherein each regulator comprises a regulator input connected to the power distribution bus to receive power from the output circuit of the bus converter and a regulator output connected to supply power to a respective load, the plurality of regulators each being separated by a distance from the bus converter.
23(a)	The apparatus of claim 22, wherein the bus converter is adapted to convert power from the input circuit to the output circuit at a substantially fixed voltage transformation ratio,

	K_{DC} , at an output current, wherein an input voltage V_{IN} is applied to the input circuit and an output voltage V_{OUT} is produced by the output of the bus converter, and wherein the substantially fixed voltage transformation ratio can be represented as $K_{DC}=V_{OUT}/V_{IN}$; and
23(b)	wherein the input circuit of the bus converter and at least a portion of the output circuit of the bus converter are connected such that an absolute value of the input voltage V_{IN} applied to the input circuit is approximately equal to the absolute value of the DC source voltage V_S minus a number N times the absolute value of the output voltage V_{OUT} , where N is at least 1.
24	The apparatus of claim 22, wherein the bus converter is a self-contained assembly adapted to be installed as a unit.
25	The apparatus of claim 1 wherein the input circuit comprises a primary winding and switches connected to the primary winding, the output circuit comprises a secondary winding and secondary switches connected to the secondary winding, and a controller for operating the switches in a series of converter operating cycles, wherein the primary and secondary windings are connected in series during at least a portion of each converter operating cycle.
26	The apparatus of claim 9 wherein the input circuit comprises a primary winding and switches connected to the primary winding, the output circuit comprises a secondary winding and secondary switches connected to the secondary winding, and a controller for operating the switches in a series of converter operating cycles, wherein the primary and secondary windings are connected in series during at least a portion of each converter operating cycle.
27	The apparatus of claim 16 wherein the input circuit comprises a primary winding and switches connected to the primary winding, the output circuit comprises a secondary winding and secondary switches connected to the secondary winding, and a controller for operating the switches in a series of converter operating cycles, wherein the primary and secondary windings are connected in series during at least a portion of each converter operating cycle.
28	The apparatus of claim 1 wherein the voltage across said one or more power switches is reduced to essentially zero volts prior to turning ON said one or more switches.

29(a)	An apparatus comprising:
29(b)	a power distribution system comprising a source for providing power at a DC source voltage V_S ;
29(c)	a bus converter comprising an input circuit and an output circuit, the bus converter being adapted to convert power from the input circuit to the output circuit at a substantially fixed voltage transformation ratio, K_{DC} , at an output current, wherein an input voltage V_{IN} is applied to the input circuit and an output voltage V_{OUT} is produced by the output of the bus converter, and wherein the substantially fixed voltage transformation ratio can be represented as $K_{DC}=V_{OUT}/V_{IN}$;
29(d)	a power distribution bus connected to distribute power from the output circuit of the bus converter at the output voltage V_{OUT} ; and
29(e)	a plurality of regulators, wherein each regulator comprises a regulator input connected to the power distribution bus to receive power from the output circuit of the bus converter and a regulator output connected to supply power to a respective load, the plurality of regulators each being separated by a distance from the bus converter;
29(f)	wherein the input circuit of the bus converter and the output circuit of the bus converter are galvanically connected; and
29(g)	wherein the bus converter comprises an inductive component and one or more switches in the input circuit or output circuit or both; and
29(h)	where in a current flowing in the inductive component charges and discharges capacitances in the converter reducing a voltage across said one or more switches prior to turning ON said one or more switches.
30	The apparatus of claim 29 wherein the voltage across one or more switches is reduced to essentially zero volts prior to turning ON said one or more switches.
31(a)	An apparatus comprising:
31(b)	a power distribution system comprising a source for providing power at a DC source voltage V_S ;
31(c)	a bus converter comprising an input circuit and an output circuit, the bus converter being adapted to convert power from the input circuit to the output circuit at a substantially fixed voltage transformation ratio, K_{DC} , at an output current, wherein

	an input voltage V_{IN} is applied to the input circuit and an output voltage V_{OUT} is produced by the output of the bus converter, and wherein the substantially fixed voltage transformation ratio can be represented as $K_{DC}=V_{OUT}/V_{IN}$;
31(d)	a power distribution bus connected to distribute power from the output circuit of the bus converter at the output voltage V_{OUT} ; and
31(e)	a plurality of regulators, wherein each regulator comprises a regulator input connected to the power distribution bus to receive power from the output circuit of the bus converter and a regulator output connected to supply power to a respective load, the plurality of regulators each being separated by a distance from the bus converter;
31(f)	wherein the input circuit comprises a winding having a first number of turns, wherein the output circuit comprises a winding having a second number of turns, and wherein the voltage transformation ratio is a function of a ratio of the first number of turns to the second number of turns; and
31(g)	wherein the input circuit of the bus converter and at least a portion of the output circuit of the bus converter are connected in series across the source such that an absolute value of the input voltage V_{IN} applied to the input circuit is approximately equal to the absolute value of the DC source voltage V_S minus a number N times the absolute value of the output voltage V_{OUT} , where N is at least 1.
32(a)	An apparatus comprising:
32(b)	a power distribution system comprising a source for providing power at a DC source voltage V_S ;
32(c)	a bus converter comprising an input circuit and an output circuit, the bus converter being adapted to convert power from the input circuit to the output circuit at a substantially fixed voltage transformation ratio, K_{DC} , at an output current, wherein an input voltage V_{IN} is applied to the input circuit and an output voltage V_{OUT} is produced by the output of the bus converter, and wherein the substantially fixed voltage transformation ratio can be represented as $K_{DC}=V_{OUT}/V_{IN}$;
32(d)	a power distribution bus connected to distribute power from the output circuit of the bus converter at the output voltage V_{OUT} ; and

32(e)	a plurality of regulators, wherein each regulator comprises a regulator input connected to the power distribution bus to receive power from the output circuit of the bus converter and a regulator output connected to supply power to a respective load, the plurality of regulators each being separated by a distance from the bus converter;
32(f)	wherein the input circuit comprises a winding having a first number of turns, wherein the output circuit comprises a winding having a second number of turns, and wherein the voltage transformation ratio is a function of a ratio of the first number of turns to the second number of turns; and
32(g)	wherein the input circuit of the bus converter and the output circuit of the bus converter are galvanically connected.
33(a)	An apparatus comprising:
33(b)	a bus converter comprising an input circuit and an output circuit, the bus converter being adapted to convert power from the input circuit to the output circuit at a substantially fixed voltage transformation ratio, K_{DC} , at an output current, wherein an input voltage V_{IN} is applied to the input circuit and an output voltage V_{OUT} is produced by the output of the bus converter, and wherein the substantially fixed voltage transformation ratio can be represented as $K_{DC}=V_{OUT}/V_{IN}$;
33(c)	wherein the input circuit of the bus converter and the output circuit of the bus converter are galvanically connected; and
33(d)	wherein the bus converter comprises an inductive component and one or more power switches in the input circuit or output circuit or both; and
33(e)	wherein a current flowing in the inductive component charges and discharges capacitances in the converter reducing a voltage across said one or more switches prior to turn ON said one or more switches.
34(a)	The apparatus of claim 33, wherein the bus converter comprises: a transformer, and a resonant circuit including the transformer having a characteristic resonant frequency and period, the input circuit including two or more primary switches connected to drive the resonant circuit and the output circuit being connected to receive power from the transformer; and
34(b)	a switch controller adapted to operate the primary switches in a

	series of converter operating cycles, each converter operating cycle characterized by two power transfer intervals of essentially equal duration each interval having a duration less than the characteristics resonant period, during which one or more of the primary switches are ON and power is transferred from the input to the output via the transformer.
35	The apparatus of claim 33 wherein the voltage across said one or more switches is reduced to essentially zero volts prior to turn ON of said one or more switches.
36	The apparatus of claim 33 wherein the input circuit of the bus converter and at least a portion of the output circuit of the bus converter are connected in series across the source such that an absolute value of the input voltage V_{IN} applied to the input circuit is approximately equal to the absolute value of the DC source voltage V_S minus a number N times the absolute value of the output voltage V_{OUT} , where N is at least 1.
37	The apparatus of claim 33, wherein the input circuit comprises a first winding having a first number of turns, wherein the output circuit comprises a second winding having a second number of turns, and wherein the voltage transformation ratio is a function of a ratio of the first number of turns to the second number of turns.
38	The apparatus of claim 37, wherein at least a portion of the input circuit of the bus converter is connected in series with at least a portion of the output circuit of the bus converter such that an absolute value of a voltage applied to the first winding is approximately equal to the absolute value of the input voltage, V_{IN} , minus a number N times the absolute value of the output voltage V_{OUT} , where N is at least 1.
39	The apparatus of claim 22 wherein the bus converter comprises an inductive component and one or more power switches in the input circuit, the output circuit, or both, and wherein a current flowing in the inductive component charges and discharges capacitances in the bus converter reducing a voltage across said one or more switches prior to turning ON said one or more switches.
40	The apparatus of claim 22 wherein at least one of the regulators is assembled to the circuit board and configured to supply power to an integrated circuit.

CERTIFICATE OF COMPLIANCE

This Petition complies with the type-volume limitations as mandated in 37 C.F.R. § 42.24, totaling 13,611 words. Counsel has relied upon the word count feature provided by Microsoft Word.

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Counsel for Petitioners

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that a copy of the foregoing document with accompanying Exhibits 1001-1010, as listed in Petitioners' Exhibit List on pages viii of this document, was caused to be served by Federal Express, costs prepaid, to Patent Owner at the following address of record:

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/s/ Russell E. Levine
Russell Levine, P.C.