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Design Challenges for Distributed Power Systems

Fred C. Lee¹, Ming Xu², Shuo Wang³ and Bing Lu⁴

Abstract – Remarkable progresses have been made over the past decade in power conversion technologies, including advanced power semiconductor devices, power management ICs, innovative circuit topologies, and packaging and integrated system solutions. These technological advancements have been manifested in a wide range of products and applications with ever increasing performances, efficiency, and power density. This paper highlights some of the challenges and opportunities of power conversion technologies in the Distributed Power System (DPS) for computer, telecommunication and network products. Topics techniques to mitigate the detrimental effects of filter/converter parasitics; impacts of the operating frequency of PFC to the size and weight of EMI filter; power conversion architecture and potential simplification; high-frequency high-density AC/DC and DC/DC topologies and designs; bus converters; as well as non-isolated point-of-load converters.

I. INTRODUCTION

Widespread use of the interest and telecommunication requires infrastructure support using a more sophisticated, high-quality and reliable “power network” that naturally takes the form of distribute power generation, distribution and regulation. Such a system is expected to achieve fully controllable, fully reconfigurable, autonomous platforms and customized for ever changing applications. It is envisioned that these advanced systems will be required to provide on demand power from a required source, and required load at any rate and in any desired form. A typical distributed power system (DPS) as shown in Fig. 1, is configured to be scalable and adaptable to ever changing power requirements of computers and telecommunication equipment and systems. The front-end AC/DC converter is a standardized module with the paralleling capability to convert the AC voltage source into the 48V DC voltage bus. This DC bus voltage is often distributed via a back-plane into various circuit boards in a form of plug-in modules, or “circuit packs” in the telephone jargon, with additional point-of-load DC/DC modules locally supplying the need power levels at the appropriate voltages to the end users.

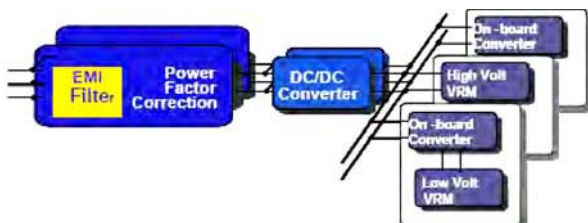


Fig 1: Distributed power system

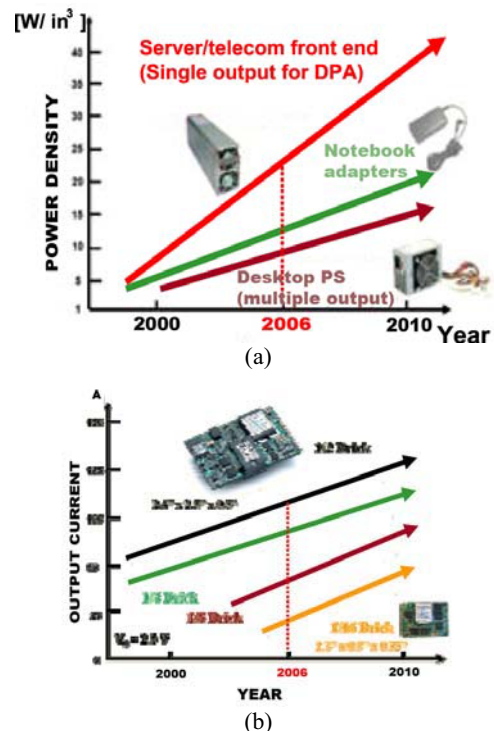


Fig.2: Power density roadmap
(a) AC/DC converters, (b) DC/DC converters

With ever increasing in functionality and shrinking in size and weight of all forms of computer and telecommunication equipment, it is essential to pack the advanced power hungry processors onto each circuit boards together with the high quality customized and miniaturized power. The aggressive power density targets for AC/DC converters and DC/DC modules, as shown in Fig. 2[1], respectively were met in the past decade and perhaps in the foreseeable future. The typical real estate utilization of the state-of-the-art 3kW 1U telecom AC/DC with 25W/inch³ is shown in Fig. 3. From this picture, it can be easily seen that EMI filter, PFC inductor and bulk capacitors and magnetic in the DC/DC converter represent the major portion of the system.

With rapidly growing computer, telecommunication, and internet technologies and applications, power supplies, other than demanding for higher power density, must achieve higher power conversion efficiency, especially for energy saving.

In the following sections, design challenges and opportunities for EMI filter, front-end AC/DC, board mounted DC/DC will be presented. More distributed power architecture with potential cost saving and performance improvements is proposed. At the meantime, system packaging and integration technologies leading to further improvement of power density and performances are discussed.

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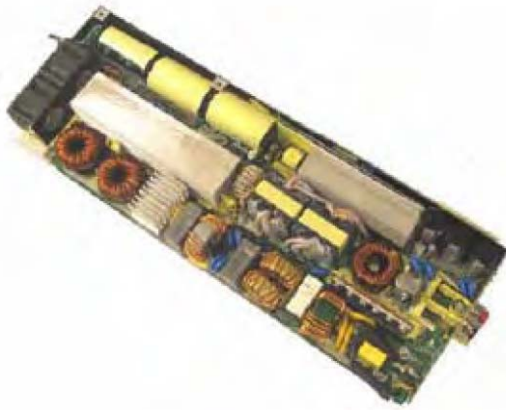


Fig.3: State-of-the-art front-end converter layout

II. EMI FILTER DESIGN CONSIDERATIONS AND CHALLENGES

In power electronics applications, electromagnetic (EMI) filter is a necessary interface between the power line and power conversion equipment, such as AC/DC and DC/DC converters operating in high frequency switching mode. They generate conducted switching noise with a spectrum that ranges from the designed switching frequency up to 30MHz. EMI standards, such as EN55022 class A, specify the frequency range (150kHz-30MHz) and noise limits which all power supplies must meet. In order to satisfy the frequency range (150kHz-30MHz) and noise limits which all power supplies must meet. In order to satisfy these EMI standards, one or two stages of EMI filters are usually employed. A typical one-stage EMI filter used in power supplies is shown in Fig. 4.

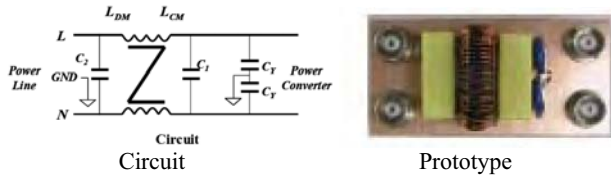
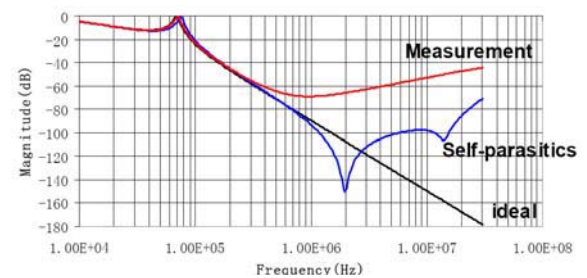


Fig. 4: One-stage EMI filter under investigation

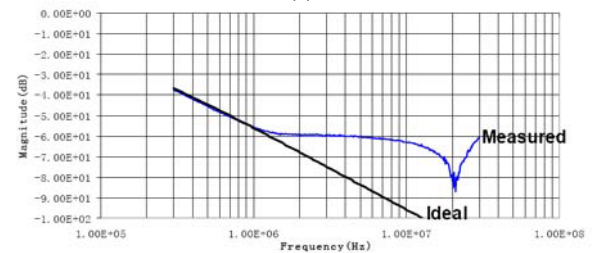
Due to the self- and mutual parasitics, the EMI filters do not work as well as expected at high frequencies (HF). Fig. 5(a) compares three DM insertion voltage gain curves, the curve that represents filter with ideal components, the curve that includes components together with their associated self parasitics and parasitics due to the coupling of electric field or electromagnetic field referred to as mutual parasitics. It is shown that the self parasitics make DM filter's HF performance much worse than that of an ideal filter; however, the mutual parasitics finally determines filter's HF performance. For CM filter performance shown in Fig. 5 (b), the self parasitics, especially the winding capacitance (EPC) of inductors degrades significantly the filter high frequency performances. Investigation [2, 3] shows the mutual coupling (mutual inductance) between inductor and trace loops, between inductor and capacitor, between two capacitors significantly affect differential mode (DM) EMI filter's high frequency performances. Equivalent series inductance (ESL) of capacitors also plays the role on the filter performances. The equivalent parallel capacitance (EPC), i.e. winding capacitance, of the inductor is a key

factor detrimental to CM filter's high frequency performances [8]. These parasitics must be minimized to improve EMI filter's ability to attenuate high frequency noises.

The mutual inductance between inductor and trace loops can be easily reduced by reducing the loop areas. One simple method to minimize the coupling between the inductor and capacitors is to rotate the inductor winding by 90° as shown in Fig. 6 [3]. In so doing, the mutual inductance can be reduced by as high as 92% (89.3nH vs. 7.5nH). To reduce the mutual inductance between two capacitors, one simple method is simply to arrange physically the two capacitors to be perpendicular [4]. In this manner, the coupling between the two capacitors can be reduced by 66% as shown in the measurement result. An even better method is to place a $1/3$ turn in parallel with one of the capacitor as shown in Fig. 7 [7].



(a)



(b)

Fig. 5: Comparison of insertion voltage gains: (a) Differential Mode (DM) and (b) Common Mode (CM).

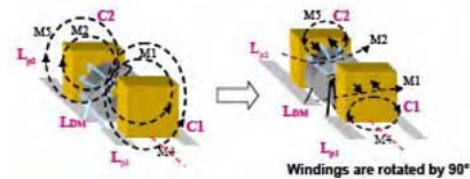


Fig 6: Reducing the mutual inductance between the inductor and capacitor

In Fig. 7, the magnetic flux linking C_2 also links cancellation turn, so the mutual inductance between two capacitors is cancelled. A 92.3% reduction (439pH vs. 19pH) is achieved in the measurement. The suggested methods illustrated in Fig. 6 and Fig. 7 can be employed at the same time to achieve even better results. Fig. 9 shows the measured insertion voltage gains with these proposed methods and compared them with the original EMI filter without incorporating any suggested methods for improvement.

Fig. 8 shows that the combination of methods suggested in Fig. 6 and Fig. 7 gives best result. A 40dB improvement achieved at 30MHz. It is well known that capacitor behaves like an inductor at high frequencies after the series resonant frequency between the capacitance and the

ESL. For a $0.47\mu\text{F}/400\text{V}$ film capacitor, the measured series resonant frequency is around 2MHz, which means this capacitor behaves like an inductor beyond 2MHz. For an electrolytic capacitor ($220\mu\text{F}/250\text{V}$), the measured series resonant frequency is even below 100kHz. If this electrolytic capacitor is used as a bulk capacitor for a converter with switching frequency above 100kHz, the capacitor actually works like an inductor even for the fundamental component of the switching waveform.

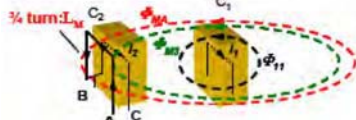


Fig. 7: Integrating cancellation turn with capacitor to cancel mutual inductance between two capacitors

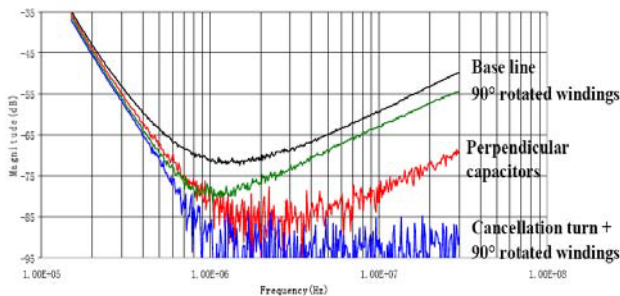


Fig. 8: Comparison of filter performance

Wang and Lee [9] further proposed a method to cancel the ESL of capacitors so as to significantly improve capacitor filtering performance at high frequencies. The idea is shown in Fig. 9.

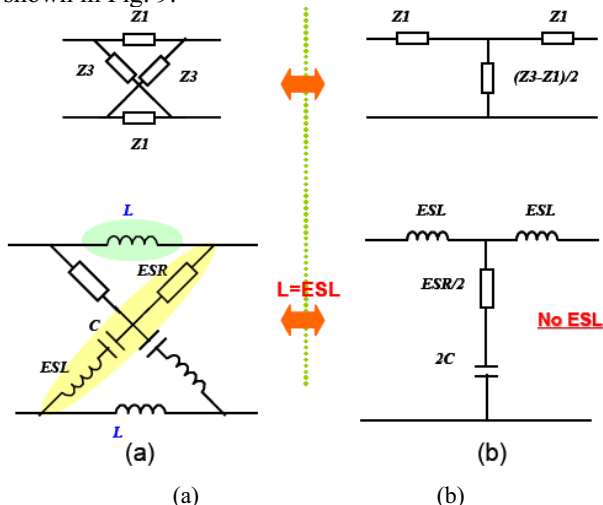


Fig. 9: Illustrating the idea of ESL cancellation: (a) network with cancellation inductor and (b) the equivalent network without ESL

Fig. 9 shows that the two networks on the top are equivalent. If two capacitors are diagonally connected and the inductor L is chosen with a value equal to the ESL of the two capacitors, from ESL as shown in the bottom diagram. In the proposed concept, the L can be implemented with the PCB trace inductance. Fig. 10 shows the measured insertion voltage gains with and without ESL cancellation. It shown that after ESL is canceled, the film capacitor performance is improved significantly above 3MHz and a 27dB improvement is achieved at 30MHz when compared with two paralleled capacitors. For electrolytic capacitors, a 27dB improvement at 30MHz also demonstrated and

performance improvement above 150 kHz is also noted. The performance improvement for both film and electrolytic capacitors is further verified in [9] by measuring the EMI noise of a converter using a noise separator [6] ad a spectrum analyzer.

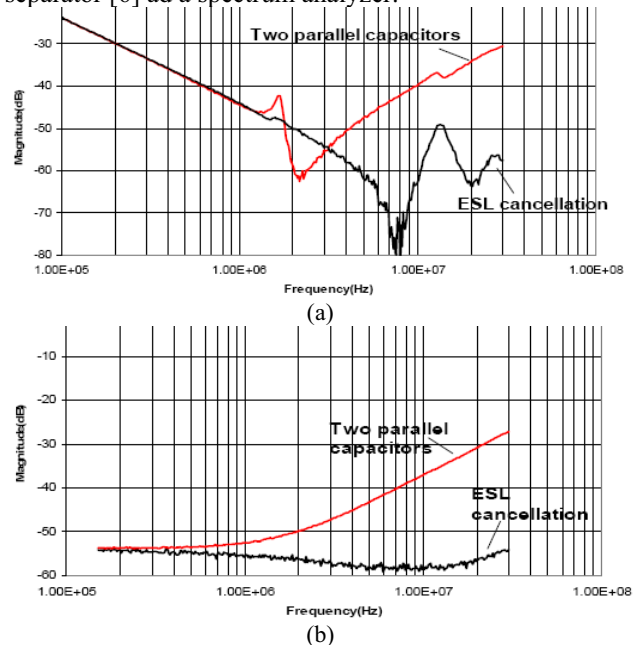


Fig. 10: Comparison of capacitor performance: (a) film ($0.47\mu\text{F}/400\text{V}$) and (b) electrolytic ($220\mu\text{F}/250\text{V}$)

The method for cancellation of winding capacitance EPC of an inductor was proposed recently [10, 11]. Fig. 11 shows models for DM inductors and CM inductors taking into consideration of EPR and EPC. Fig. 12 shows the ideas of winding capacitance cancellation.

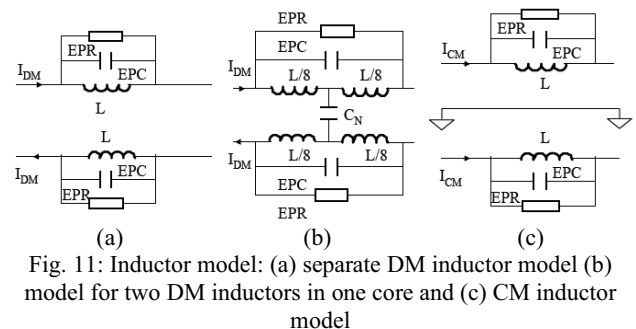


Fig. 11: Inductor model: (a) separate DM inductor model (b) model for two DM inductors in one core and (c) CM inductor model

If the two DM inductors are separated, i.e. not on one core, the parasitic model can be shown in Fig. 11(a). If two DM inductors are on one core then there is equivalent parasitic capacitance C_N between two inductors as shown in Fig. 11(b), since the permittivity of the core would be relatively high and the distance between two inductor windings are relatively close. For CM inductor the model is shown in Fig. 11(c).

In order to cancel the winding capacitance of DM inductors, two extra small capacitors are needed. For separate DM inductors, two small capacitors with values equal to EPC are diagonally connected to two inductors as shown in Fig. 12(a). The cancellation mechanism can be explained by network equivalence as well as mutual capacitance theory developed in [10]. For combined DM inductors, since two windings are on the same core, the effect of C_N can be equivalent to a negative capacitor with

value of $C_N/2$ in parallel with each inductor [10, 11]. If the equivalent negative capacitance is smaller than original EPC, then the total winding capacitance is still positive. Two small capacitors with values of $EPC - C_N/2$ can be diagonally connected to two inductors to cancel it. This is shown in Fig. 12(b). However, if the total winding capacitance is negative, then two small capacitors with values of $C_N/2 - EPC$ should be parallel with two DM inductors. Ironically, in order to cancel the winding capacitance, external capacitors are needed in parallel with windings. This is shown in Fig. 12(c).

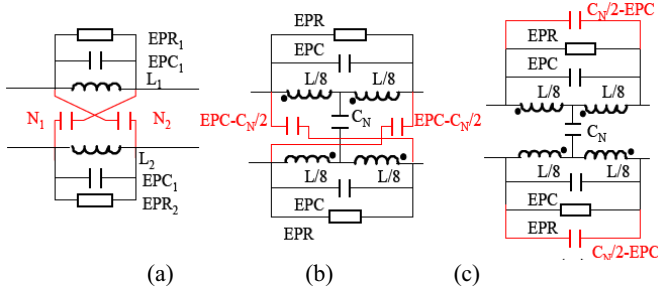


Fig. 12: Winding capacitance cancellation for DM inductors: (a) separate DM inductor, (b) Two DM inductors on one core when equivalent winding capacitance is positive and (c) Two DM inductors on one core when equivalent winding capacitance is negative

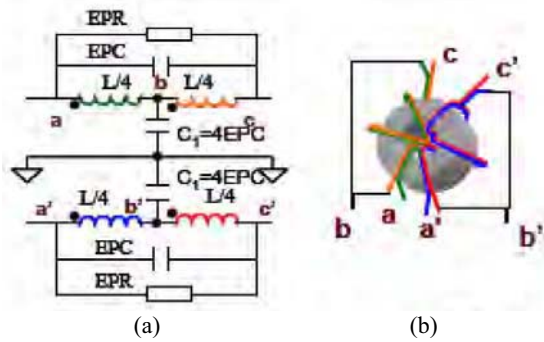


Fig. 13: The cancellation of winding capacitance for CM inductor: (a) Cancellation idea and (b) Proposed bifilar winding structure

For CM inductors, the method proposed for DM inductors can also be applied if a winding is allowed in ground path. If the winding is not desirable on ground path, the method proposed in [4] can be considered. For the method in [4], the coupling coefficient between two half windings of one side must be as high as 0.9999, which is possible to be realized in an integrated inductor structure. However, for a conventional discrete CM inductor winding structure, the coupling coefficient is around 0.99. Therefore, the idea cannot be applied, since a resonance between the leakage of two winding halves and the cancellation capacitor can cause high frequency noises.

A bifilar winding structure, which is not used in conventional CM inductors due to large EPC, is proposed for high coupling coefficient. Because two winding halves are almost in the same position, the coupling coefficient is very high. The measured value is 0.99995. Although EPC is enlarged, the EPC cancellation techniques can be employed and the performance improved.

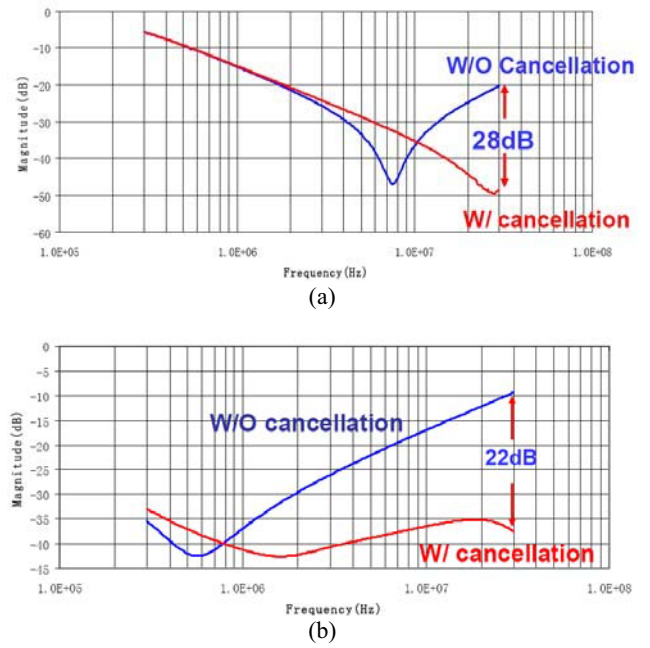


Fig. 14: Improvement on inductor impedance: (a) DM inductor and (b) CM inductor

Fig. 14 (a) and (b) show the measured impedance of the filter inductor. Impedance at high frequencies is significantly reduced for both DM and CM inductors due to winding capacitance cancellation. Both DM and CM inductor filtering performance is improved by more than 20dB. More elaborated EMI noise measurements on the proposed EPC cancellation techniques when applied to a power converter were reported in [10, 11] with significant improvements shown.

In this section, various techniques for cancellation of both mutual parasitics and self-parasitics are introduced. A much better understanding of the basic nature of EMI noises had led to development of in the practice. Continuous research in this area will eventually lead to an understanding and development of this subject matter as a branch of science in stead of art or “magic” as it is often referred to.

III. HIGH FREQUENCY HIGH DENSITY FRONT-END AC/DC

For the front-end AC/DC converters, normally they are implemented by two-stage approach. The first stage is the power factor correction (PFC) stage, which is able to provide power factor correction function and a constant voltage for the DC/DC stage input. The second stage is the DC/DC stage, which gives a regulated output voltage for the load. For the PFC stage, the single switch continuous current mode (CCM) PFC is the most widely used topology because of its simplicity and smaller EMI filter. For the whole front-end converter, the EMI noise major comes from the PFC stage. The differential mode and common mode EMI noise models for the single switch CCM PFC circuit have been derived and verified by CPES. Based on the derived EMI noise model, the switching frequency impact on the EMI filter design of the PFC circuit is analyzed. The switching frequency selection guideline is given based on the analysis.

A. Benefits from High Frequency PFC

Based on the filter attenuation requirement, we are able to develop the relationship between the corner-frequency of the filter and the switching frequencies of the converter, as shown in Fig. 15(a) [13~15]. In these curves, the zigzag nature of the curve is caused by the EMI standard which specifies the regulation requirement beginning at 150kHz.

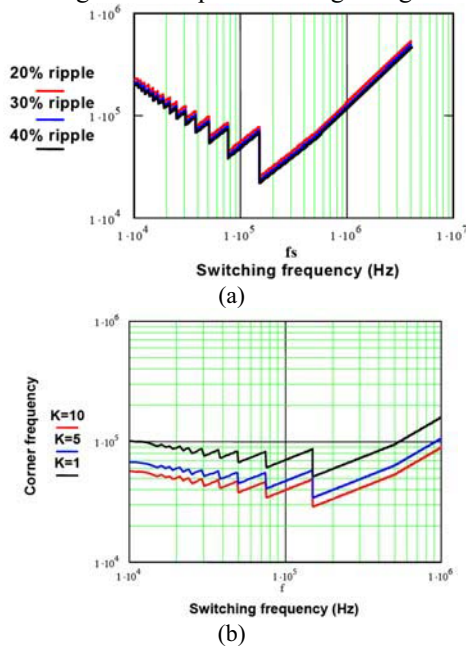


Fig. 15: Filter corner frequency vs. switching frequency: (a) Differential Mode (b) Common Mode

Those vertical jumps at frequencies representing the various sub-harmonics of 150kHz, such as 50kHz, 75kHz, etc. When the switching frequency is slightly lower than those frequencies, the corner frequency of the DM filter is much higher. Beyond 150kHz, the filter corner frequency will continue to increase as the switching frequency increase. From the curves, it can be seen that when the switching frequency is roughly higher than 400-500 kHz, the corner frequency of the DM filter will be higher than all the previous peaks. As it is known, higher the corner frequency means smaller the EMI filter size. Therefore, one can observe that the size reduction of the DM filter is achieved only if the switching frequency is higher than 400-500kHz, in comparison with that at 150kHz.

Similar observation can be made for the CM filter. From Fig. 15(b), it can be seen that irrespective to what K value is (where K is related to the circuit parasitic, the switching speed of the MOSFET and the output voltage of the PFC circuit.), when the switching frequency is higher than 400kHz, the size of CM filter will be smaller than that previously achieved at 150kHz. Further increasing of the switching frequency will continue to reduce filter size.

From the previous analysis, we can conclude that the switching frequency has great impacts on the EMI filter design. Since the EMI spec begins at 150kHz, certain frequency range should be avoided. Clearly, there is no filter size reduction achieved when the switching frequency is chosen between 150-400kHz. Since the new generation of power devices, such as CoolMOS and SiC, enable the PFC circuit to operate at a much higher switching frequency. It is possible to contemplating a switching frequency higher than 400kHz. To illustrate this

point, two CCM PFC circuits were built, one operated at 100kHz and the other at 400kHz. Two EMI filters were designed, respectively to meet the EMI standard EN55022 Class B. As shown in Fig. 16, both of the converters can meet the standard at the low frequency range. For the two different EMI filter and boost inductor, we can see that 34% and 55% volume reduction is achieved respectively by pushing the switching frequency from 100kHz to 400kHz. The excessive noises at high frequencies are due to parasitics of the EMI filter as discussed in the previous section. The problem can be solved by using the suggested techniques, grounding and shielding technologies.

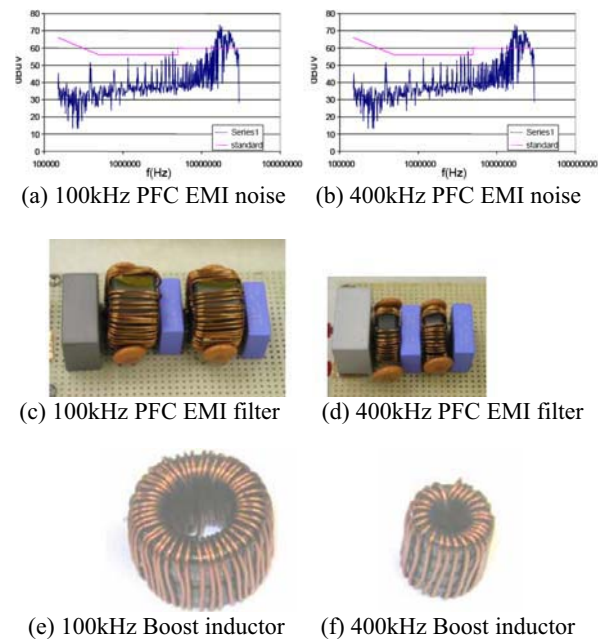
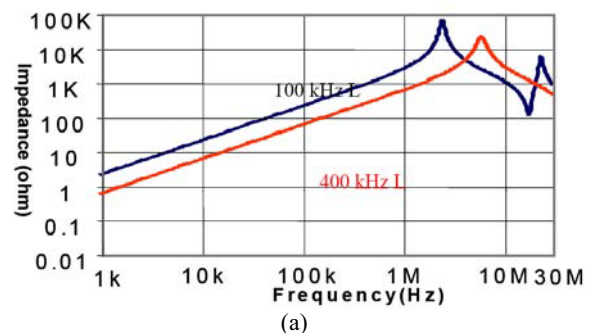


Fig. 16: EMI noise after filtering and EMI filter size comparison

In Fig. 17(a), the impedances of the boost inductors when designed for 100kHz PFC, there is a resonant valley at the frequency about 17MHz. At this frequency, the impedance of the boost inductor is small. Therefore, the EMI noise at corresponding frequency is high, which can be seen in Fig. 17(b) [15, 16]. But for the 400kHz boost inductor, the resonant valley is pushed beyond 30MHz, as discussed in the previous section; the filter ability to attenuate high frequency noises is compromised with the presence of parasitics. Therefore, it is important to eliminate the high frequency noise peaks. From the experimental results, we can clearly see that the benefit brought by pushing the switching frequency higher.



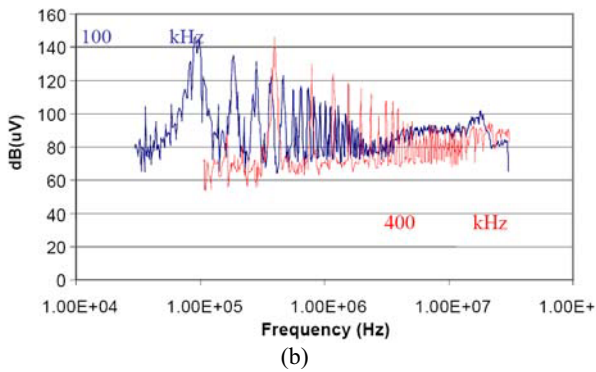


Fig.17: Comparison between two boost inductors for different switching frequencies: (a) Impedance, (b) EMI noise

To get high switching frequency for PFC, CPES has evaluated different devices, CoolMOSTM and SiC diode enable much higher efficiency and higher frequency [17]. A 1kW CCM PFC using CoolMOS TM and SiC diode running at 400 kHz is demonstrated. It shows that by using the CoolMOSTM and SiC diode, the 400kHz CCM PFC can achieve the similar efficiency by using conventional devices at 100kHz switching frequency, as shown in Fig. 18.

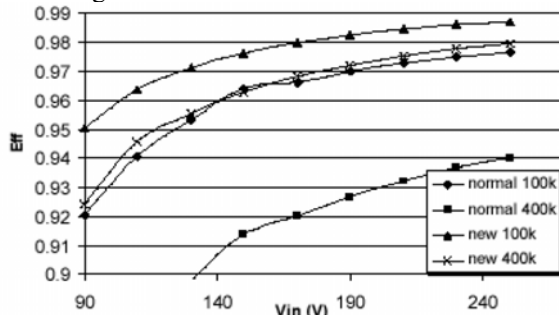


Fig. 18: Efficiency comparison between different PFC designs
Normal: IRFP460 + RHRP860, New: CoolMOS + SiC diode

B. High frequency DC/Converter

To achieve high power density for the front-end AC/DC converters, increased switching frequency is desired. However, its effectiveness is limited by the large holdup capacitors. For the telecom and computer applications, system is required to maintain a regulated output voltage with full power for 20ms after AC input is lost. Therefore, bulky capacitors are employed to provide the needed energy during holdup time. The size of the selected bulk capacitors will directly impact the input voltage range of the down stream DC/DC converter, thus its conversion efficiency and power rating. To reduce the holdup time capacitors and improve converter power density, it is essential to select an appropriate converter topology that can achieve high efficiency with wide input voltage range, especially high efficiency at 400V input [18~20].

For conventional PWM DC/DC converters, a maximum duty cycle is designed for the minimum input (say, 300V) which occurs when the AC input power is lost. Consequently, the given circuit will operate at a smaller duty cycle when the input voltage is at around 400V. Thus, to realize a wide input range, it is inevitable that the converter efficiency is suffered at the nominal input of 400V. Fig. 19 demonstrates the efficiency of an asymmetrical half-bridge (AHB) optimally designed for a

fixed input voltage at 400V. The circuit can achieve 94.5% efficiency. When the same circuit is designed to operate at 300V to 400V input range, the converter efficiency can only achieve 92% at 400V [20].

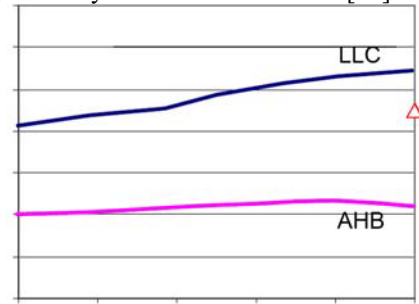


Fig. 19: Efficiency of AHB and LLC converters

Instead of using PWM converters, certain class of resonant converters such as the LLC resonant converter as shown in Fig. 20(a) is able to operate with a wide input range without compromising circuit efficiency at the desired operating voltage, i.e. at 400V. Because the magnetizing inductor participates in resonant, converter voltage gain characteristic is change, as shown in Fig. 20(b).

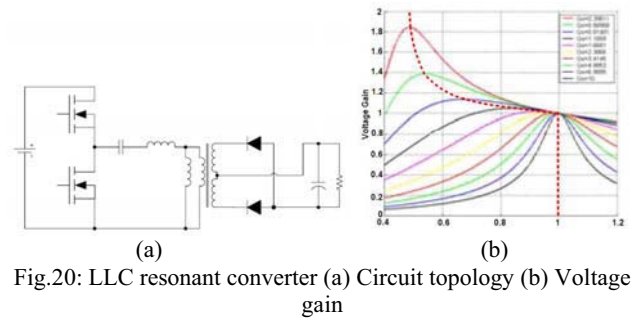


Fig.20: LLC resonant converter (a) Circuit topology (b) Voltage gain

The LLC converter can achieve a voltage conversion ratio either higher or lower than unity. Moreover, the zero voltage switching (ZVS) can be achieved with switching frequency both lower and higher than the series resonant frequency determined by L_r and C_r . By choosing a suitable transformer turns-ratio, the converter can be targeted to operate right on top of the resonant frequency with optimal efficiency at normal operation condition, i.e. 400V input. During holdup time, input voltage drops, and LLC resonant converter reduces its switching frequency and increase voltage gain to maintain regulated output voltage. Although LLC converter operates far away from the resonant point during the holdup time which means the circuit is less efficient, it only lasts for 20ms and will not cause extra thermal problem. Because LLC converter can operate at resonant frequency during normal operation condition, the circuit is operated at the most efficient point and its efficiency could be much higher in comparison with AHB or other PWM topologies. As shown in Fig. 19, with 200kHz switching, LLC could achieve 2 to 3% efficiency improvement over that of AHB. Moreover, LLC resonant is operated with ZVS turn-on and relatively small turn-off current. These properties make switching losses at the primary side switches very small. Besides, the secondary side diodes are also operated with ZCS thus reduces the diode reverse recovery loss. The much reduced switching losses enable LLC resonant converter to operate at much higher switching frequencies while maintaining high efficiency. A proto-type 1MHz LLC was developed with 94.5% efficiency at 1kW output. The

efficiency of LLC resonant converter for different switching frequency is shown in Fig. 21. As shown in Fig. 22(b), 1MHz LLC achieves $76\text{W}/\text{in}^3$ power density [20, 22].

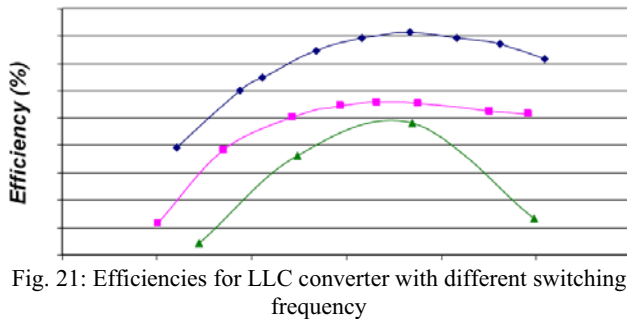


Fig. 21: Efficiencies for LLC converter with different switching frequency



Fig. 22: Comparison among different DC/DC converter designs: (a) 200 kHz AHB, $12\text{W}/\text{in}^3$ (b) 1MHz LLC, $76\text{W}/\text{in}^3$

C. High density front-end AC/DC via IPeMs

Although higher density is achieved at higher frequency, some fundamental limitations prevent further improvement in power density. For example, the parasitic inductance in the switch commutation loop hampers the switching speed and causes more switching losses. Large voltage stresses appear on switching devices due to large parasitic inductance, which compromises reliability. The parasitic junction capacitances between high voltage transition points to the earth ground increases the common mode noise. Moreover, the parasitic components brought by the interconnection of the electrical layout played a negative role in the system electromagnetic interference noise (EMI) if it is not treated carefully.

The front-end AC/DC converters are essentially custom designed and manufactured using discrete parts, which high labor content and high cost. To address the aforementioned performance issues and cost, the integrated power electronics module (IPEM) concept was proposed by Center of Power Electronics Systems (CPES). The IPEM concept is to explore the integration of discrete power devices to the extend that it is technologically practical and economically feasible. To this end, the active power semiconductor devices, with its associated drivers, protection circuits, sensors and controller are integrated together in the form of modular building block here referred to as active IPEM. Similarly, the passive power components such as inductors, capacitors and power transformers are integrated together into a Passive IPEM. One apparent benefit of integration is the size reduction. The integration of the switching devices together with their associated gate driver circuit, invariably will reduce parasitics associated with interconnects, thus resulting in smaller switching losses and voltage stresses. By integrating inductors, capacitors, together with power transformer, passive component size can be greatly reduced. Moreover, due to the integration,

circuit component number can be greatly reduced. The assembly of such modules could be automated thus reduce labor content. Furthermore, by perfecting the process of integration, IPEMs can become standard building blocks to facilitate system integration. Therefore, the reliability, product cycle time and cost can be significantly reduced [23, 24].

To demonstrate the benefits of the IPEM concept under the system level, two 1kW front-end AC/DC converters were built using exactly the same topologies, one using discrete devices and the other one using IPEMs. As shown in Fig. 1 and 23, the system is constructed by the two stages: PFC stage and DC/DC stage. For the PFC stage, a 400kHz single switch PFC using CoolMOS and SiC diode were chosen to reduce the boost inductor and EMI filter. The Asymmetrical Half Bridge operating at 200kHz was used for the DC/DC stage. The converters are designed for the universal input line 90V~264V, and the power rating is de-rated to 600W when operated below 150V input. Two converters are shown in Fig. 23.

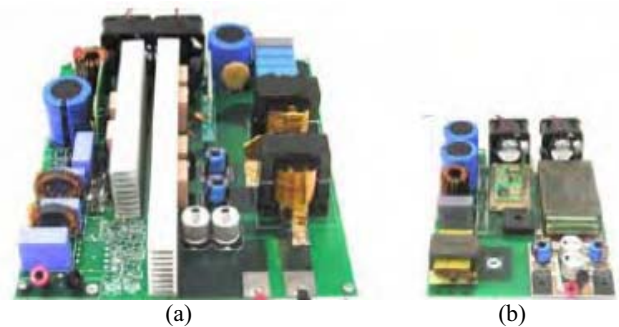


Fig. 23: Comparison among different DC/DC converter designs: (a) 200 kHz AHB, $12\text{W}/\text{in}^3$, (b) 1MHz LLC, $76\text{W}/\text{in}^3$

The discrete components have been replaced by the Active and Passive IPEMs. Through integration, density and form factor of the active and passive devices are much improved. Therefore, the power density at the system level is improved significantly. As for the discrete approach, the power density is $7.5\text{W}/\text{in}^3$, and for the IPEM-based converter, the power density is $11.4\text{W}/\text{in}^3$ and still has the room for improvement.

By replacing the discrete active and passive devices into the IPEMs, the number of components of the systems can be reduced from several hundreds part to about 20-30 parts. Not only the system power density has been improved, the system electrical performance has been improved as well. The system efficiency increases more than 2% at the high line voltage range, and more than 3% at 90V. Since the conduction losses are roughly the same for the same operation condition, the major improvement lies on the switching loss reduction by minimizing the circuit parasitics.

At the same time, due to the smaller parasitic inductance on critical path of the converter, less voltage stress is achieved. For the discrete PFC switch, when switch turn off occurs at 7Amp, the device voltage overshoot is 123V. But when the discrete components are replaced with an active IPEM, the voltage over-shoot is reduced to 72V even at 10Amp.

IV. HIGH FREQUENCY HIGH CURRENT DENSITY BOARDMOUNTED ISOLATED DC/DC CONVERTERS

With rapidly growing computer and telecommunication applications, the point-of-load (POL) DC/DC module is becoming smaller and smaller, from non-isolated POL to isolated 1/4 brick to 1/8 brick and even to 1/16 brick, and in the mean time, with continuous increasing in current demand and decreasing in output voltage. High power density and high efficiency are demanded by the customers. Design engineers, now a day are facing challenges in all fronts, including higher operating frequencies with reduced switching losses, conduction losses, body diode losses and even the gate driver losses; innovative packaging and thermal management; EMI and EMC containment and reduction.

This section will introduce two examples of circuit means of achieving higher operating frequencies and in the same time, higher efficiencies. These goals are realized by simultaneously reducing the primary side switching losses and conduction losses as well as the secondary side synchronous rectifier body diode conduction losses, reverse recovery losses, drive losses, and conduction losses.

A. Single Stage isolated DC/DC:

A.1 State-of-the-art:

Fig. 24(a) shows a typical PWM hard-switching 48V input DC/DC topology. To get faster dynamic performance and higher power density, higher switching frequency is desired. However, as shown in Fig. 24(c), efficiency will suffer a lot at higher switching frequency mainly due to the switching loss, driving loss and SR body diode conduction loss. By far, the soft switching technique is a well-known approach to reduce the switching loss effectively. Therefore, Fig. 24(b) shows the state-of-the-art 48V DC/DC for server processor (power pod), running at 300 KHz by employing phase-shift full bridge ZVS topology. Its efficiency can be seen in Figure 30(b).

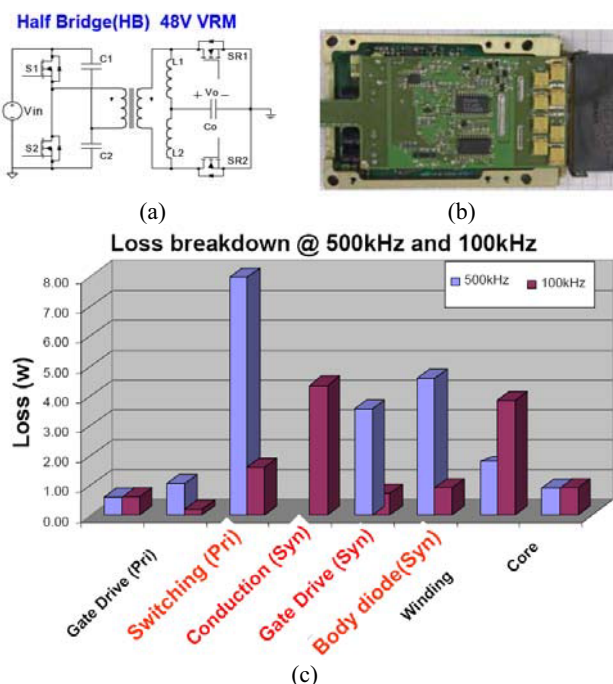


Fig. 24: State-of-the-art power pod in server

In the conventional synchronous rectifier, the dead time is necessary, accompanying with the body diode conduction loss and reverse recovery loss due to the current through the body diode during the dead time. There are some precise timing control driving ICs to reduce the body diode conduction loss. However, they cannot effectively solve the body diode reverse recovery problem. And also, they are expensive and noise sensitive.

A.2 Self-Driven ZVS Full-Bridge DC/DC and Magnetic Integration:

The self-driven technique has been widely used in the industry practice due to their simplicity and low cost. However, for bridge-type symmetrical converters, implementation of self-driven capability is difficult because of the inherent dead time period. One possible solution is the level-shifted self-driven concept [25]. However, the proposed approach has several drawbacks: (a) Ringing occurs at the gate signal because the signal is coming from the main power transformer and severe ringing is coupled from the power stage, (b) there is extra body diode conduction loss, and (c) there is large amount of conduction loss due to the low driving voltage during dead time. These issues prevent the level-shifted self-driven concept from being used in high frequency applications.

In order to overcome these issues, a self-driven ZVS full bridge (FB) was proposed [26, 27]. The power stage is shown in Fig. 25. By simply rearranging the control strategy, it becomes very suitable for self-driven capability as well as achieving ZVS. It was further demonstrated that the self driven scheme can save driving loss and body diode conduction loss and is very suitable for high-frequency applications where high power density is required.

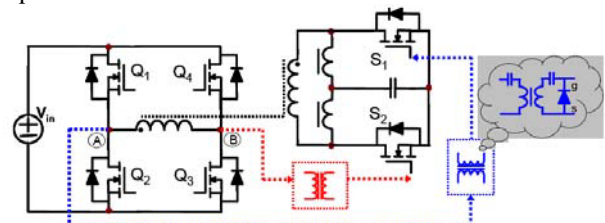


Fig.25: Conceptual diagram of the proposed self-driven ZVS full-bridge DC/DC converter

A 1MHz prototype picture shown in Fig. 26(a) was built to verify this self-driven concept. Fig. 26(b) shows the efficiency comparison. Including the driver loss, the proposed self-driven ZVS full-bridge can achieve 81.7% efficiency.

There is an efficiency improvement of 4.7% as compared with the conventional phase-shifted full-bridge with an external driver.

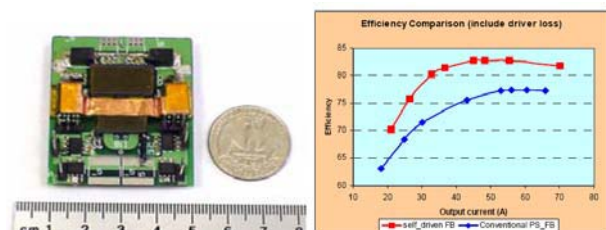


Fig. 26: (a) Hardware of the proposed DC/DC, (b) Efficiency comparison

However, this topology requires a total of 3 discrete transformers, one main power transformer and two synchronous rectifier gate drive transformers, thus increasing the number of passive components. Further work has been done to integrate all of the three magnetic components and two output inductors into a single core as shown in Fig. 27 [28]. This fully integrated magnetic has been adopted in a 1.2V/70A 1/8 brick prototype with 87% overall efficiency at 600kHz switching frequency. Comparing to the state-of-the-art 1/8 brick product, it can deliver 40% more output current while having 2% higher efficiency.

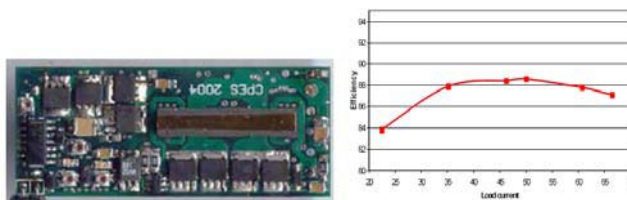


Fig. 27: 600 kHz 1.2V/70A 1/8 brick hardware and measured efficiency

Generally, the gate driving loss can be reduced by the combination of the ZVS technique and Self-driven technique. As an example, the proposed self-driven ZVS full-bridge has the following advantages: (a) soft switching for primary switches; (b) clean gate signal and no level-shifting during dead time; (c) reduced gate driving loss; and (d) reduced body diode conduction loss. The experimental results verify that this topology is very promising in high-frequency applications. Furthermore, the proposed self-driven method can be applied to any bridge and non-bridge topologies employing complementary control.

A.3. Current Tripler Concept and Magnetic Integration

For low-voltage and high-current applications, the secondary-side device switching and conduction losses have a major impact on system efficiency. To reduce the conduction loss in the secondary side, one solution is to reduce the on resistances of the synchronous rectifiers and the transformer winding resistance. This can be realized by paralleling more synchronous rectifier switches (SRs) and enlarging the window area of the transformer. The drawbacks of this solution are the higher cost, larger gate driver loss and larger footprint.

Other than reducing the $R_{ds(on)}$ of the synchronous rectifier, proper secondary-side topologies should be selected to reduce the RMS current through the SRs. There are three major secondary-side topologies: forward rectifier, center tapped rectifier and current-doubler rectifier. Among these three topologies, the current-doubler rectifier is the most suitable for high-current, low-voltage applications. Because of its simpler transformer structure and halved inductor currents and transformer secondary currents, the current-doubler topology offers lower conduction losses than the conventional center tapped topology [29].

The reason for the lower RMS current of the current-doubler rectifier is that during the freewheeling period (when there is no input-output energy transfer), both SR switches can conduct simultaneously to share the load

current. As a result, the total rectifier conduction loss during the freewheeling period is reduced. To further reducing the conduction losses for higher current applications, often times, current-doubler with more semiconductor devices in parallel and distributed magnetics are used to reduce the transformer winding losses. However, those solutions have their limitations:

- Increased cost,
- Larger footprint and lower power density,
- More devices mean greater driver loss.

Recently, a novel current-Tripler topology was proposed, as shown in Fig. 28. The proposed topology can easily achieve ZVS for all MOSFETs, therefore switching loss is significantly reduced [30]. Through magnetic integration shown in Fig. 29, a three phase high frequency transformer can be used to greatly simplify the circuit.

Compared with the conventional current doubler, the proposed current Tripler can reduce the SR conduction loss and transformer winding loss by 20% and 12.5% respectively.

A 300kHz prototype was developed to demonstrate the concept. Comparing to the typical industry design with the same spec and switching frequency, proposed current-Tripler DC/DC converter can achieve 45% footprint reduction and 4% higher efficiency, as shown in Fig. 30.

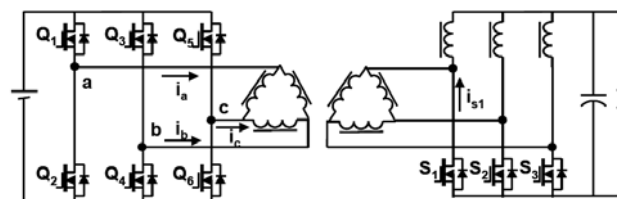


Fig. 28: Proposed Zero-Voltage-Switch current-Tripler DC/DC converter

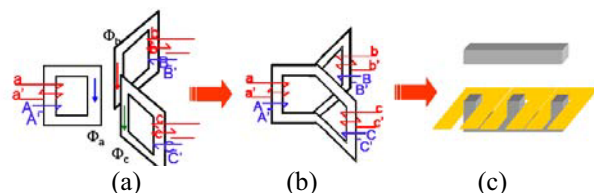


Fig. 29: Implementation by three discrete cores

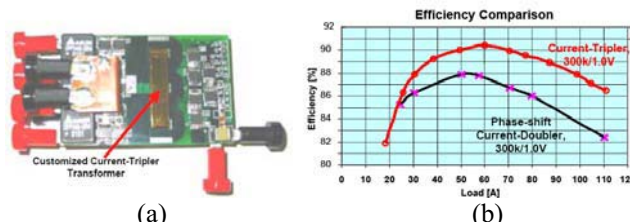


Fig. 30: (a) 300 kHz hardware of the proposed ZVS current tripler, (b) Efficiency comparison with state-of-the-art

B. Two-Stage isolated DC/DC

The 48V input DC/DC for high-end server and telecom applications requires higher voltage devices on the primary side and a transformer for isolation. To get fast dynamic response and regulation performance, the PWM type power conversion is preferred, whereas the efficiency and switching frequency is limited by the presence of the leakage inductances of the transformer. In order to achieve acceptable efficiency, lower switching frequencies,

around 200~300 KHz, are normally adopted. Thus the size of the transformer and its passive components are bulky and the transient responses are slow. Excessive output capacitors are necessary to satisfy the dynamic transient requirement. In general, the isolated 48V DC/DC is normally customized design with higher cost, while its footprint and power density are significantly lower than that of the non-isolated POL converters.

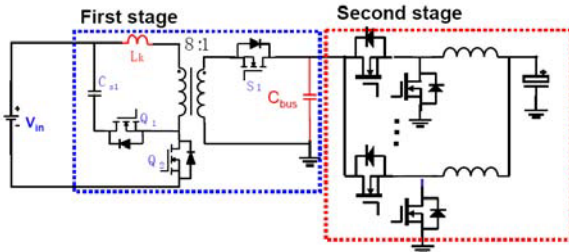


Fig. 31: Proposed two-stage solution

To leverage the 48V isolated DC/DC with standard high frequency non-isolated POL converter techniques, a superior two-stage approach was proposed [31], as shown in Fig. 31. The first stage utilizes a simple inductorless “DC/DC transformer operating at 1MHz switching frequency by adopting the resonant switching to minimize switching losses. The second stage employs the multiphase buck capable of operating at multi-Mega Hertz, taking advantage of the already established infrastructure for low-voltage POL converters. Fig. 32 shows the two-stage prototype for the 48V power pod used in the server. Due to the MHz switching frequency in the second stage, the passive components can be greatly reduced. Table I lists the comparison between the CPES two-stage prototype and the industry single stage practice in Fig. 24(b). Based on the reduction of passive components, the power density of the power pod can be increased to around 150%. It is also apparent that since the output capacitors are significantly reduced, the two-stage approach is less costly than the single-stage approach. This architecture has been quickly adopted by the industry and used in the current products.



Fig. 32: 130W two-stage power pod prototype for server

Table 1: The Comparison between Single-stage and two-stage

	Switching frequency	Transformer	Inductor	Capacitor
Industry Practice	300kHz	Philips EI32	2 Philips EI22 (customized)	15*1mF Tantalum
CPES Prototype	1 st stage: 300kHz, 2 nd stage: 1MHz	Philips EI22	4 Vishay IHLP-5050FD 150nH	4*270uF ESRE
Volume Reduction		54%	90%	75%

C. Intermediate Bus Architecture (IBA) and Bus Converter

With the proliferation of low-voltage, high-current microprocessors/DSPs and high-voltage analog devices on a single circuit board, the number of different voltages encountered has mushroomed. All these voltages share a common ground so that it is unnecessary to use an isolated transformer for each of these loads, respectively.

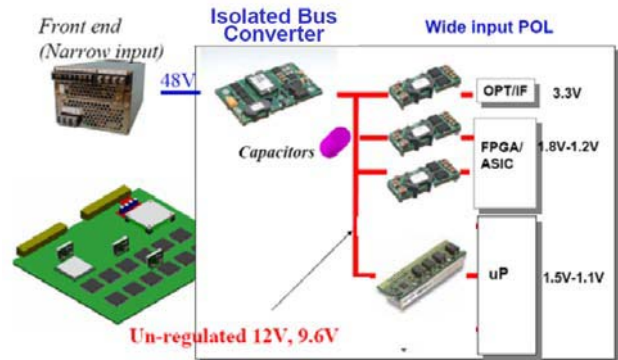


Fig. 33: Two-stage architecture—IBA

Therefore, the two-stage concept aforementioned was extended to the sub-system level, as shown in Fig. 33, in which an isolated bus converter steps down the 48V to an intermediate bus voltage to feed all the non-isolated point-of-load converters (POL) in the same board. This concept has been adopted by industry and is becoming a mainstream for high-end server and telecommunication applications, because it is more cost-effective, more flexible in terms of system structure. To minimize the size and cost of these bus converters, CPES proposed inductorless bus converter family with ZVZCS switching behavior through the resonant between the transformer leakage inductor and output capacitor [32]. These proposed topologies can double the power capability compared with state-of-the-art products. As an example, Fig. 34(a) shows the full-bridge version of the proposed inductorless bus converter family. Fig. 34(b) and (c) shows the 800 kHz 500W bus converter prototype with 96% efficiency at full load.

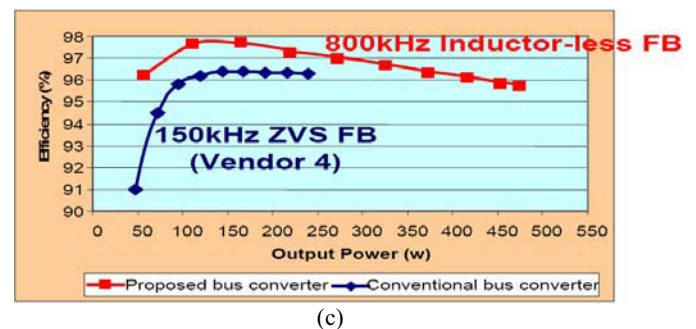
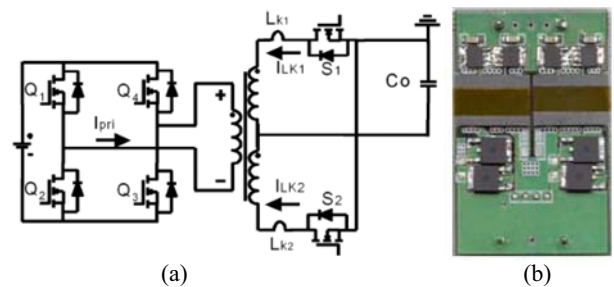


Fig. 34: Proposed inductor-less resonant FB DC/DC transformer

V. HIGH FREQUENCY HIGH CURRENT DENSITY NON-ISOLATED POINT-OF-LOAD (POL) CONVERTERS -- VRS

In 1997, CPES proposed a multi-phase buck converter, as shown in Fig. 35, for the INTEL Pentium processor. This concept was quickly adopted by the industry. The VR is designed to operate at around 300kHz and the control bandwidth is around 50kHz. It is well known that the switching frequency can be increased to reduce the output capacitance. However, the efficiency of today's single stage suffers at higher switching frequencies. As shown in Fig. 36, the major loss factors are the switching losses and the body diode losses.

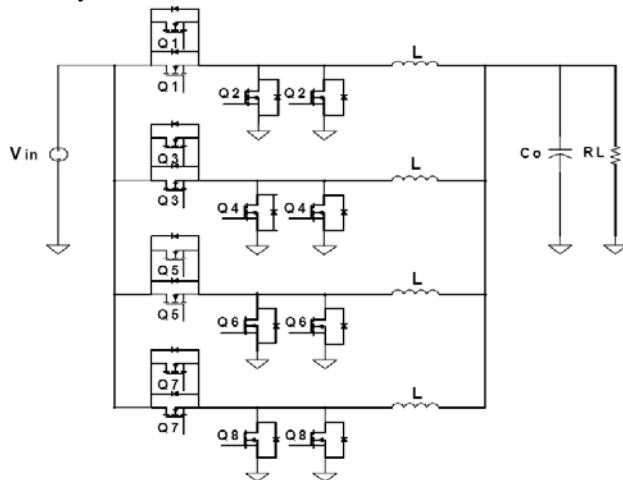


Fig. 35: State-of-the-art VR solution: Multi-phase Buck

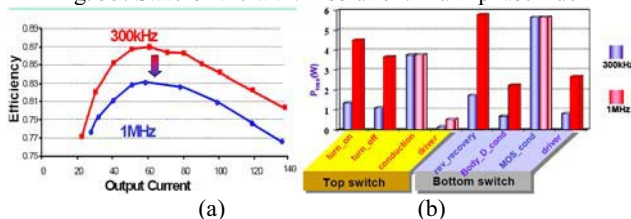


Fig. 36: Issues of single stage 12V VR at higher switching frequency, (a) Efficiencies, (b) Loss breakdown comparison

A. 1MHz ZVS Self-Driven Single-stage VRs

From the loss breakdown in Fig. 36, the major factors affecting circuit efficiency at 1MHz are switching loss, body diode losses and gate driving loss.

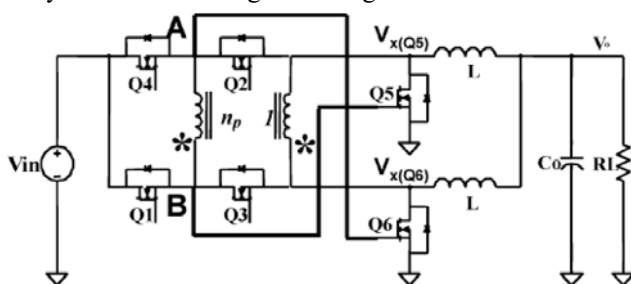


Fig. 37: Proposed ZVS self-driven full bridge Buck

To minimize the aforementioned high frequency losses, a novel self-driven dc/dc converter for non-isolated 12-V VR was proposed, as shown in Fig. 37 [33]. ZVS was realized for all the MOSFETs. By adding a transformer, the proposed topology extends its duty cycle so that both the switching loss and body diode reverse recovery loss are further reduced. This innovative self-driven concept eliminates the need for synchronous rectifier drivers which saves cost and driver loss. In addition, self-driven scheme

reduces the body diode conduction losses. Furthermore, the magnetic integration has been realized to merge the output inductor into the transformer to further reduced the size. All of these benefits have been demonstrated in a 1MHz 100A 1U 12V VRM prototype shown in Fig. 38(a). Compared to the conventional Buck design, the proposed topology can elevate the efficiency by 6% at 1MHz switching frequency with the same active component setup, as shown in Fig. 38(b).

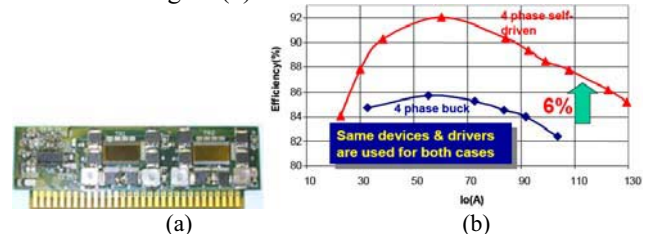


Fig. 38: Demonstration of the proposed DC/DC in 1U 100A 12V VRM (a) Hardware, (b) Efficiency comparison

Though the proposed self-driven topology is compelling, the duty cycle loss induced by the transformer leakage inductor is one inherent limitation for higher than 1 MHz operation. Theoretical analysis reveals that the gain of this topology is diminishing with switching frequency increasing beyond 1MHz.

Thereby, a two-stage approach shown in Fig. 39 is proposed in [34]. The first stage can be designed at relatively low switching frequency to step down the input voltage from 12V to around 5V. With the lower input voltage, the switching losses and reverse recovery losses of the second stage, which are proportional to the input voltage, are dramatically reduced. Therefore, it was demonstrated that the second stage switching frequency can be pushed to 2MHz to achieve 350kHz bandwidth at 83% efficiency [34, 35]. The prototype in Fig. 40 clearly shows that the two-stage approach can eliminate the output electrolytic capacitor entirely together with a 2% efficiency improvement over the single stage solution. This is achieved with a switching frequency is 4 times higher than the single stage counterpart.

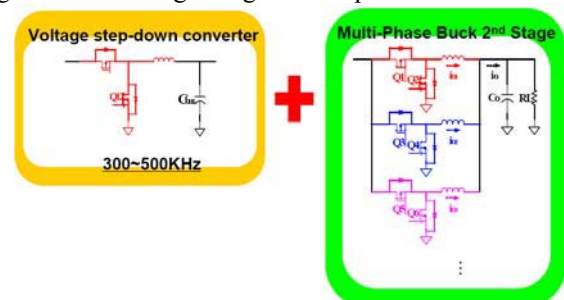


Fig. 39: The structure of the two-stage approach in [34]

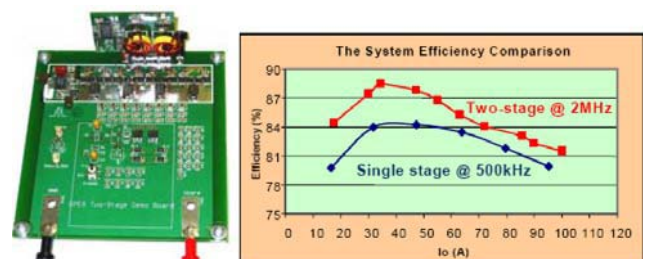


Fig. 40: Demonstration of the two-stage 12V VR (a) Hardware, (b) efficiency comparison

The conventional Buck converter was employed for the first stage initially, as shown in Fig. 39. It was designed to run at low switching frequency, e.g. 200-300 kHz, to attain high efficiency. However, this low switching frequency makes the first stage relatively large in size. Subsequently, a magneticless DC/DC converter was developed by adopting the switching capacitor technology [36]. Because no magnetic component is required, it can substantially boost the power density of the first stage up to $1\text{ kW}/\text{inch}^3$. The proposed first stage with fixed 2:1 conversion ratio is essentially serves as a voltage divider. It can achieve 98% efficiency with 12V or even higher input voltage. Fig. 41 shows the comparison between the buck and voltage divider designs for the first stage.

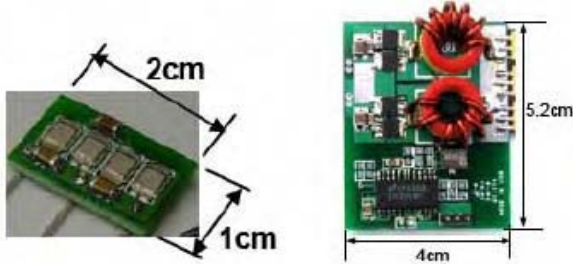


Fig. 41: Size comparison between voltage divider and Buck

Other than high power density, the proposed voltage divider can achieve ultra-high efficiency in the whole load range with capability to handle over load conditions. By adapting the switching frequency to the load, 98~99% efficiency in whole load range has been demonstrated in a 70W prototype design as shown in Fig. 42. Even with 100% overload, the circuit can maintain 95.5% efficiency.

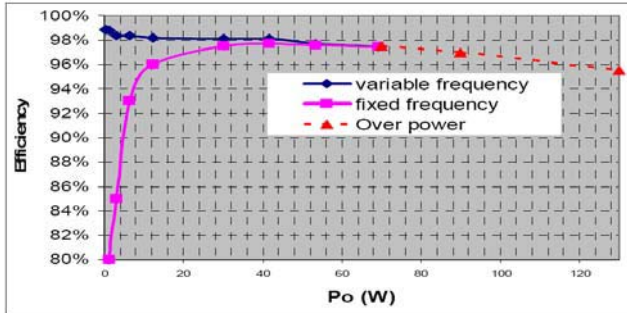


Fig. 42: Experimental efficiencies of 70W prototype

B. Non-isolated System Two-stage Architecture:

By extending this two-stage approach into system level, the non-isolated IBA structure is proposed, as shown in Fig. 43, in which the voltage divider is used as the non-isolated bus converter. This architecture has been investigated for the laptop with the configuration shown in Fig. 44 [37].

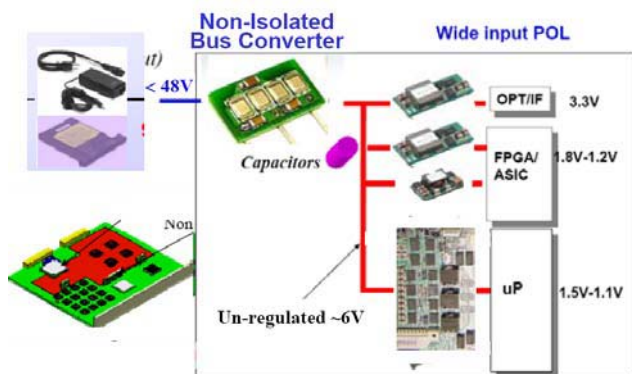


Fig. 43: Proposed non-isolated system two-stage architecture

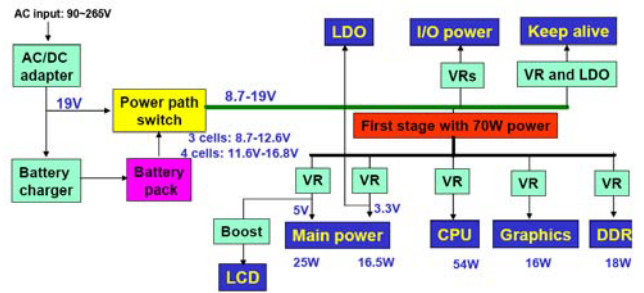


Fig. 44: Proposed system two-stage power architecture for laptop

Detailed analysis and experimental results have demonstrated that this architecture can achieve 45% total inductor size reduction, 35% total capacitor size reduction and 7% total cost reduction for major VRs inside the laptop. Furthermore, the proposed two-stage architecture can improve the light load efficiency for all down-stream VRs, which is critical to the battery life of the laptop. As an example, Fig. 45 shows 1~2% efficiency gain on the CPU VR at half load power and below.

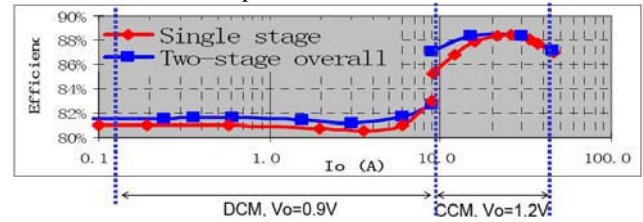


Fig. 45: Efficiency improvement from two-stage on CPU VR

VI. CONCLUSION

This paper provides an overview of some of the important design challenges and opportunities for power supplies, specifically using the example of a generic distributed power system for computer server, telecom and network applications. First, the effects of mutual and self-parasitics of the filter capacitors and inductors on the performance of EMI filter are presented. Techniques for cancellation of both mutual parasitics and self-parasitics are introduced. Specifically, mutual coupling between inductors and capacitors as well as coupling between two capacitors can be minimized.

Among the self-parasitics, the ESL of capacitors and the winding capacitance of the filter inductors are identified most detrimental to both DM and CM noises. The unwanted effects of self-parasitic can be neutralized by circuit means. The proposed technologies are proven by theory and verified by experiments. It is demonstrated that, EMI filter's HF performance can be greatly improved by applying proposed methods in practice.

To achieve higher power density of front-end converter, it is essential to using high switching frequency techniques to reduce passive component size. In the PFC stage, it is found that the impact of switching frequency to EMI filter size reduction is realized when the switching frequency is pushed beyond 400 kHz. The switching frequency between 150kHz to 400kHz should be avoid since the EMI filter size could be even larger than that at 70kHz due to the EMI regulation that specifies noise level from 150 kHz to 30MHz.

Besides the reduction on EMI filter and PFC inductor, it is

essential to reduce the size of bulk capacitor for hold up time requirement. It is found that the LLC resonant converter offer special advantage for this application. It can work with wide input range without sacrificing the conversion efficiency at the normal operation condition. Furthermore, smaller switching loss allows LLC converter to operate at considerably higher switching frequency while maintaining high efficiency. A prototype LLC converter operated at 1 MHz was demonstrated with 76W/in³ power density.

System power density was further improved by means of integration using IPEM concept. Modular and integrated approach makes the system layout easy and manufacturing process more automated. Furthermore, it was shown that circuit interconnect parasitics were significantly reduced, thus further improving converter efficiency and reducing components stresses.

Products in the area of isolated and non-isolated point-of-load converters are fiercely competitive. The major driving forces are cost, efficiency and power density. Design challenges for high-frequency, high-density POLs involve innovative circuit means of reducing the primary side switching losses and conduction losses as well as the secondary side synchronous rectifier body diode conduction losses, reverse recovery losses, drive losses, and conduction losses. Packaging and thermal management are equally important. Some of the important recent developments are presented. A novel zero-voltage switching (ZVS) current-Tripler converter was presented which offers great advantages compared with the popular current double configuration especially for low voltage and high current applications. A novel self-driven ZVS full bridge topology was introduced with significant saving of driver losses, switching losses, and body diode losses for isolated and non-isolated DC/DC converters. One of the potential applications is for powering the next generation of microprocessors. Prototype hardware is demonstrated operating at 1MHz 12V with an efficiency 6% above the comparable multi-phase Buck topology used in today's VRM design. Other than the topological innovations, CPES also proposed two-stage power architectures to further improve the system performance for isolated and non-isolated applications. Prototypes were developed to demonstrate significant improvements in efficiency, power density as well as potential cost saving compared to the state-of-the-art.

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