

Petition for *Inter Partes* Review of U.S. Patent No. 9,166,481

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DELTA ELECTRONICS, INC.

Petitioner,

v.

VICOR CORPORATION,

Patent Owner.

Case IPR2024-00187

U.S. PATENT NO. 9,166,481

PETITION FOR *INTER PARTES* REVIEW

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Exhibit No.	Description
1001	U.S. Patent No. 9,166,481 (the “’481 Patent”)
1002	Certified File History of the ’481 Patent
1003	Declaration of Dr. Douglas Hopkins
1004	<i>Curriculum Vitae</i> of Dr. Douglas Hopkins
1005	Brent McDonald and Dave Freeman, <i>Design and Optimization of a High-Performance LLC Converter</i> , 2012 Texas Instruments Power Supply Design Seminar (“McDonald”)
1006	Texas Instruments UCD3138 Data Manual – Highly Integrated Digital Controller for Isolated Power, March 2012 revision (“TI UCD3138”)
1007	JP Patent No. 2012-34522 (“Shimada”)
1008	Certified Translation for JP Patent No. 2012-34522 (“Shimada”)
1009	U.S. Patent No. 6,984,965 (“Vinciarelli”)
1010	U.S. Patent No. 8,243,473 (“Chen”)
1011	S. Pan and P.K. Jain, <i>Secondary Side Adaptive Digital Controlled Series Resonant DC-DC Converters for Low Voltage High Current Applications</i> , 2008 IEEE Power Electronics Specialists Conference, IEEE 2008 (“Pan”)
1012	U.S. Patent No. 6,370,050 (“Peng”)
1013	U.S. Patent Application Publication No. 2006/0220938 (“Leung”)
1014	U.S. Patent No. 7,428,159 (“Leung 159”)
1015	U.S. Patent No. 7,855,905 (“Leung ’905”)
1016	Declaration of Dr. Sylvia Hall-Ellis
1017	Excerpt from Vicor’s October 16, 2023 Supplemental Response to Respondents’ Interrogatory No. 10, in Inv. No. 337-1370, <i>Certain Power Convert Modules and Computing Systems Containing the Same</i>
1018	Texas Instruments UCD3040 Data Sheet – Digital Power Controllers, November 2010 revision (“TI UCD3040”)
1019	Microchip AN1336 Datasheet – DC/DC LLC Reference Design Using the dsPIC DSC, 2010 (“AN1336”)

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Exhibit No.	Description
1020	Microchip dsPIC33FJ06GS101 Datasheet – 16-bit Digital Signal Controllers, Revision F, January 2012 (“dsPIC33FJ06GS101”)
1021	Registration Website for 2012 Texas Instruments Power Supply Design Seminar

Petitioner Delta Electronics, Inc. (“Delta”) requests *inter partes* review (“IPR”) of claims 1, 22, and 31-35 (the “Challenged Claims”) of U.S. Patent No. 9,166,481 (Ex. 1001, “the ’481 Patent”).

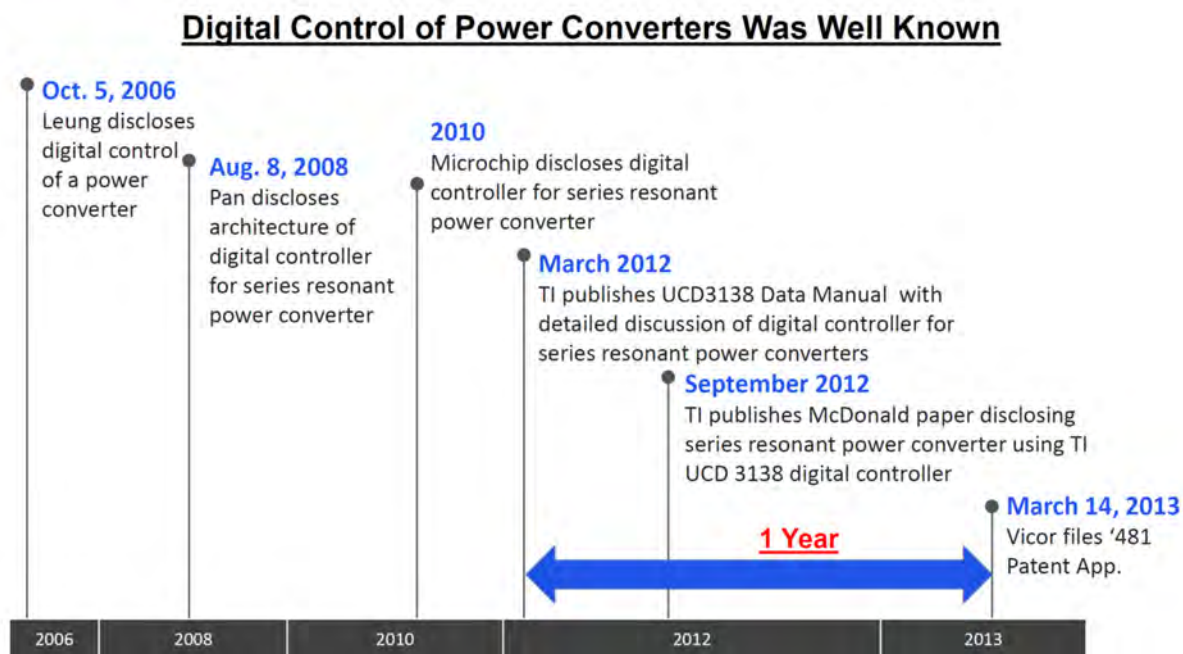
I. INTRODUCTION

The ’481 Patent is directed to a method for digital control of a resonant power converter. Ex. 1001, 1:6-9, 20:41-67 (claim 1). None of the prior art presented in this Petition (other than the applicant admitted prior art) have been considered by the Examiner. Ex. 1001, Cover; Ex. 1002. Despite their significance and relevance, none of these references were cited by the applicant or the Examiner during prosecution of the ’481 Patent. Simply stated, there was no prior art before the Examiner relating to digital control of resonant power converters.

At the time of the alleged invention of the ’481 Patent, though, digital control of power converters was well known in the art. Leung disclosed digital control of a power converter as early as **2006**. Ex. 1013, Cover (showing a patent application publication date of October 5, 2006). In **2008**, Pan disclosed the architecture of a digital controller for a series resonant power converter. Ex. 1011, 711; Ex. 1016, ¶¶ 39-45. In **2010**, Microchip published its AN1336 datasheet discussing series resonant power converters that use Microchip’s dsPIC digital controllers. Ex. 1019, 1. In **2012**, Texas Instruments published its TI UCD3138 data manual with detailed discussion of a digital controller for series resonant power converters (Ex. 1006,

Cover). Also, in **2012** TI published a paper, McDonald, disclosing a high-performance LLC resonant power converter that uses the TI UCD3138 digital controller. Ex. 1005, Cover; Ex. 1016, ¶¶ 46-49.

In March 2013, almost a year after the publications by Texas Instruments, and seven years after Leung's disclosure of digital control of a power converter, Vicor filed its patent application, the title of which was "Digital Control of Resonant Power Converters." The timeline below shows visually the prior art landscape that the Examiner could not see, much less evaluate, during prosecution of the '481 Patent application.



Vicor did not disclose any of the aforementioned prior references or the other references discussed in this Petition. The references disclosed by Vicor consisted primarily of Vicor's own patents relating to power converters. But, the references

disclosed by Vicor, and the few cited by the Examiner, did not address the digital control features of the purported invention. As indicated in the prior art references cited in this Petition, and as shown in the timeline above, digital control features were known in the art long before Vicor filed the application for the '481 Patent.

The prosecution of the '481 Patent was very limited, and the Challenged Claims issued without any rejection. After the application filing in March 2013, the Applicant submitted an Information Disclosure Statement ("IDS") on July 1, 2013 containing five references (two of which were Vicor patents with the same inventor as the '481 Patent). On July 29, 2014, the Applicant submitted a second IDS containing five references (all of which were Vicor patents and again all with the same inventor as the '481 Patent). The first and only Office Action was sent on April 23, 2015, allowing all 35 claims and stating that none of the prior art of record showed the claimed limitations—quoting the sole independent claim 1. The Office Action included a Notice of References Cited, containing five additional references beyond the ten identified in Vicor's IDS submissions, but none of these references disclosed digital control of power converters. A Notice of Allowance was sent on July 15, 2015, and the '481 Patent issued on October 20, 2015.

During prosecution, the Examiner did not have any digital control prior art before him, much less the art relied upon in this Petition. A review of the Examiner's prior art search history from the Office Action reveals no search terms related to

digital control of power converters, despite this being the title of the patent application and the crux of the alleged “invention.” The limited prior art searching and cursory nature of the overall prosecution of the ’481 Patent renders this a textbook case for *inter partes* review.

Accordingly, Petitioner respectfully requests that *inter partes* review of the ’481 Patent be instituted and that claims 1, 22, and 31-35 be cancelled as unpatentable pursuant to 35 U.S.C. § 318(b). This Petition demonstrates that there is a reasonable likelihood that at least one of the Challenged Claims is unpatentable as obvious.

II. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

A. 37 C.F.R. §42.104(b)(1): Claims for Which IPR Is Requested

Petitioner challenges the patentability of claims 1, 22, and 31-35 (the “Challenged Claims”) of the ’481 Patent and request that they be canceled.

B. 37 C.F.R. §42.104(b)(2): Grounds for Challenge

The claims are challenged based on the following references, none of which were considered by the Examiner during prosecution. The ’481 Patent is subject to pre-AIA law,¹ as the patent was filed on March 14, 2013.

¹ All citations in this Petition to 35 U.S.C. §§102 and 103 are to the pre-AIA law.

- **McDonald (Ex. 1005):** McDonald is a paper from the 2012 Texas Instruments Power Supply Design Seminar held on September 25, 2012. Ex. 1016, ¶¶ 46-49. It was publicly available at least by September 25, 2012. *Id.*, ¶ 48-49; Ex. 1021. Accordingly, McDonald qualifies as prior art under 35 U.S.C. § 102(a).

- **TI UCD3138 (Ex. 1006):** TI UCD3138 is a data manual from Texas Instruments for the UCD3138 Highly Integrated Digital Controller for Isolated Power, published in March 2012. Accordingly, TI UCD3138 qualifies as prior art under 35 U.S.C. § 102(a).

- **Shimada (Ex. 1007 (original), Ex. 1008 (certified translation)):** Shimada is a Japanese patent issued on February 16, 2012. Accordingly, Shimada qualifies as prior art under 35 U.S.C. § 102(b).

- **Chen (Ex. 1010):** Chen is a U.S. patent filed on October 26, 2009 and issued on August 14, 2012. Accordingly, Chen qualifies as prior art under 35 U.S.C. § 102(e).

- **Pan (Ex. 1011):** Pan is a conference paper from the 2008 IEEE Power Electronics Specialists Conference held June 15-19, 2008. Ex. 1016, ¶ 39. It was publicly available no later than August 8, 2008. *Id.*, ¶¶ 40, 45. Accordingly, Pan qualifies as prior art under 35 U.S.C. § 102(b).

- **Peng (Ex. 1012):** Peng is a U.S. patent issued on April 9, 2002. Accordingly, Peng qualifies as prior art under 35 U.S.C. § 102(b).

- **Leung (Ex. 1013):** Leung is a U.S. patent application filed March 31, 2005 and published October 5, 2006. Accordingly, Leung qualifies as prior art under 35 U.S.C. § 102(b).

- **TI UCD3040 (Ex. 1018):** TI UCD3040 is a datasheet from Texas Instruments for the UCD3040, UCD3028, and UCD3020 Digital Power Controllers, published in November 2010. Accordingly, TI UCD3138 qualifies as prior art under 35 U.S.C. § 102(b).

- **AN1336 (Ex. 1019):** AN1336 is datasheet from Microchip of the AN1336 DC/DC LLC Reference Design Using the dsPIC DSC, published in 2010. Accordingly, AN1336 qualifies as prior art under 35 U.S.C. § 102(b).

- **dsPIC33FJ06GS101 (Ex. 1020):** dsPIC33FJ06GS101 is a datasheet from Microchip of the dsPIC33FJ06GS101 Digital Signal Controller (DSC), published in January 2012. Accordingly, dsPIC33FJ06GS101 qualifies as prior art under 35 U.S.C. § 102(b).

- **AAPA (Exs. 1001, 1009):** The '481 Patent discloses numerous instances of Applicant Admitted Prior Art ("AAPA") related to zero voltage and zero current switching. The Patent Office's updated guidance on treatment of AAPA in *inter partes* review confirms that AAPA can be used "in combination with reliance on one or more prior art patents or printed publications" and in that case "those admissions do not form the basis of the ground and must be considered by the Board in its

patentability analysis.” See Director Vidal Memorandum, “Updated Guidance on the Treatment of Statements of the Applicant in the Challenged Patent in Inter Partes Reviews Under § 311,” 3 (June 9, 2022).

Petitioner requests cancellation of the Challenged Claims on the following grounds:

Ground	Basis	Claims	Proposed Statutory Rejection
I	§ 103	1, 22, 31-35	Obvious over McDonald in view of TI UCD3138
II	§ 103	1, 22	Obvious over Shimada in view of AAPA
III	§ 103	1, 22	Obvious over Chen in view of AAPA
IV	§ 103	1, 22, 31-35	Obvious over Pan in view of TI UCD3138 (or, alternatively, in view of TI UCD3040) and AAPA
V	§ 103	1, 22, 31-35	Obvious over Peng in view of TI UCD3138 (or, alternatively, in view of TI UCD3040) and AAPA
VI	§ 103	1, 22	Obvious over Leung in view of AAPA
VII	§ 103	1, 22	Obvious over AN1336 in view of dsPIC33FJ06GS101 and AAPA

C. 37 C.F.R. § 42.104(b)(3): Claim Construction

For purposes of this Petition, all terms should be given their plain and ordinary meaning. 37 C.F.R. § 42.104(b)(3). Petitioner reserves the right to later address the construction of any claim terms, if necessary.

D. 37 C.F.R. § 42.104(b)(4): How the Claims Are Unpatentable

A detailed explanation of how the Challenged Claims are unpatentable is provided below in Section VI.

E. 37 C.F.R. § 42.104(b)(5): Evidence Supporting Challenge

A list of exhibits is provided at the beginning of this Petition. The relevance of this evidence and the specific portions supporting this challenge are provided below in Section VI. Petitioner submits the declaration of Dr. Douglas Hopkins (Ex. 1003) in support of this Petition. 37 C.F.R. § 1.68.

III. OVERVIEW OF THE '481 PATENT

A. Priority Date

The '481 Patent issued on October 20, 2015 from U.S. Application 13/830,262 filed on March 14, 2013. Ex. 1001, Cover. The '481 Patent does not claim priority to any earlier applications, and thus, on its face, claims priority to March 14, 2013. Patent Owner has contended in a parallel ITC proceeding that the '481 Patent was conceived in April 2010. Petitioner asserts that Patent Owner is not entitled to that earlier priority date, and reserves the right to challenge that priority date in this IPR proceeding should Patent Owner raise it. In any event, the obviousness analysis presented herein for Grounds II-VII would not change regardless of which priority date applies, and for Ground I applies the March 14, 2013 priority date.

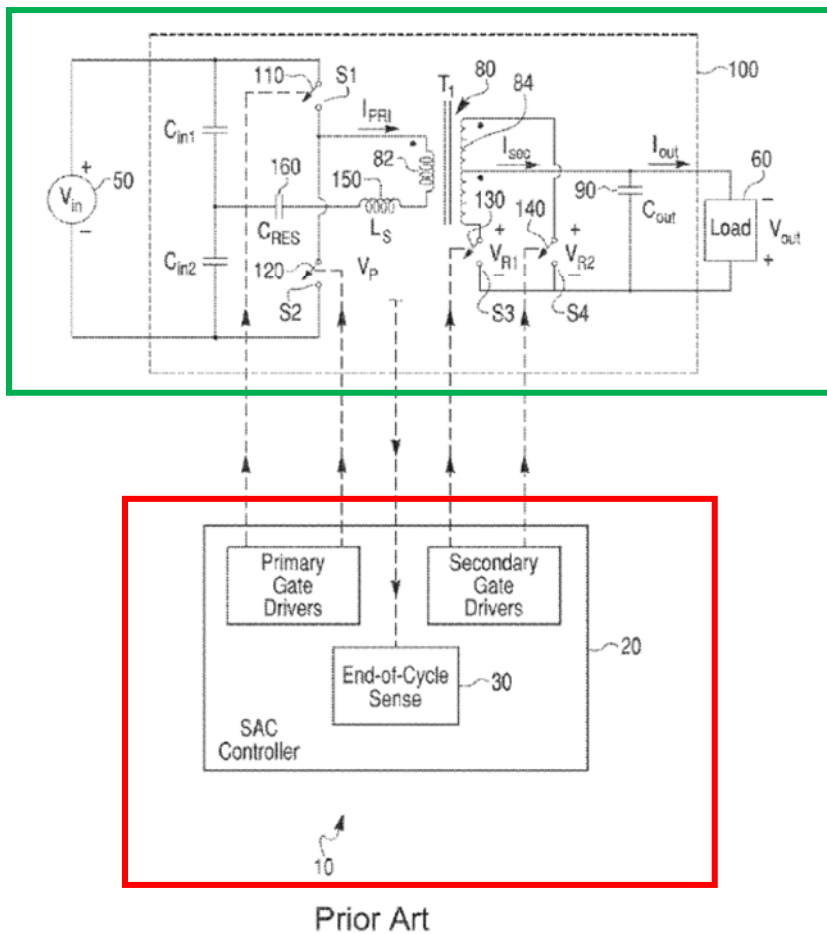
B. Specification and Claims

The '481 Patent is directed to a method for digital control of a resonant power converter. Ex. 1001, Abstract. More specifically, the patent relates to a method for “digital control of resonant zero-current and zero-voltage switching resonant power converters.” *Id.* 1:6-9. The specification describes one implementation of the invention as “a method of synchronously operating a power converter in a series of converter operating cycles includes providing an oscillator for generating clock signals at an oscillator frequency and generating timing control signals for each of a plurality of events based upon the clock signals in a standard converter operating cycle having a standard operating period and frequency. The timing and control signals may turn a primary switch ON and OFF at times when essentially zero voltage is impressed across and essentially zero resonant current is flowing in the primary switch and turn a secondary switch ON and OFF at times when essentially zero current is flowing in and essentially zero voltage is impressed across the secondary switch. The oscillator frequency may be preset and the timing of the timing control signals for one or more selected events may be set independently of other timing control signals and events.” *Id.* 2:26-41. That description is the essence of claim 1 of the '481 Patent, which is the sole independent claim in the patent. *Id.*, Claim 1.

The '481 Patent admits that resonant power converters with zero-current and

zero voltage switching were known in the art at the time of filing. Indeed, the converter and controller configuration in Figure 1 below is labeled as “Prior Art” in the '481 Patent and is described as a “block diagram of a half-bridge sine amplitude converter 10” that “comprises SAC power conversion circuitry 100 . . . and a SAC controller 20 which controls the turning ON and OFF of the switches within the power conversion circuitry 100.” Ex. 1001, 1:20-25; Fig. 1.

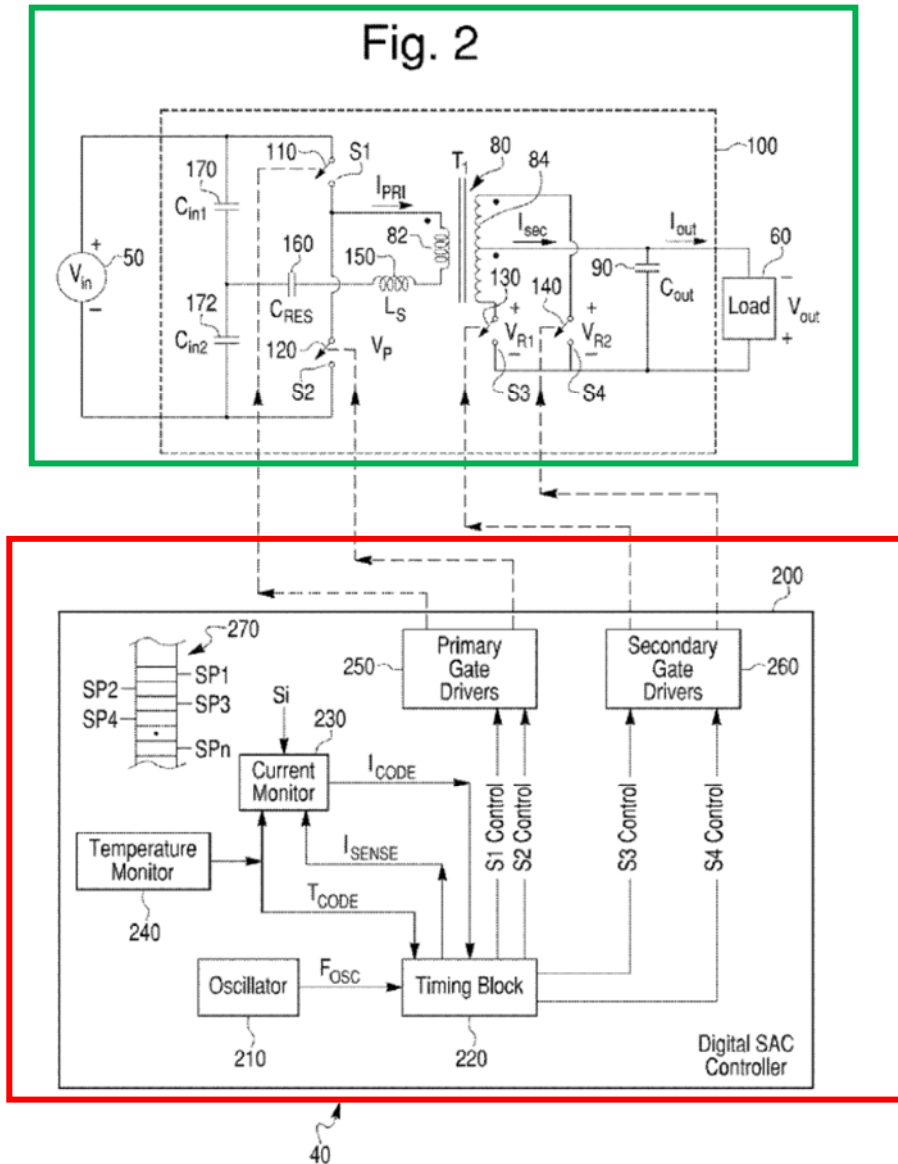
Fig. 1



Ex. 1001, Fig. 1 (“Prior Art”).² The green box in Figure 1 represents the prior art “SAC power conversion circuitry 100”, and the red box represents the prior art “SAC controller 20 which controls the turning ON and OFF of the switches within the power conversion circuitry 100”. *Id.* 1:20-25. The ’481 Patent further admits that the prior art was capable of performing zero-voltage switching (“ZVS”) and zero-current switching (“ZCS”). *Id.* 1:13-2:7.

The purported “invention” of the ’481 Patent replaced the conventional SAC controller 20 of Figure 1 with a digital SAC controller 200 of Figure 2, shown below.

² All colors and colored annotations to figures added.



Ex. 1001, Fig. 2. Indeed, the '481 Patent confirms that "the SAC power conversion circuitry 100 shown in Fig. 2 is essentially the same as shown in Fig. 1." *Id.* 4:29-35. A comparison of the SAC power conversion circuitry 100 (green boxes) in both Figure 1 (admitted prior art) and Figure 2 ('481 Patent) confirms that they are identical. The '481 Patent goes on to describe the operation of digital SAC controller 200, but as will be discussed in Section VI below, use of a digital controller to control

zero-voltage and zero-current switching in a resonant power converter was well known at the time of the '481 Patent's priority date, and the prior art references described in that section render the Challenged Claims of the '481 Patent unpatentable.

C. Prosecution History

The prosecution of the '481 Patent did not address any of the prior art relied on in this Petition (other than the AAPA). Ex. 1002. Indeed, the prosecution was very limited, and the Challenged Claims issued without any rejection. *Id.* After the application filing in March 2013, the Applicant submitted an Information Disclosure Statement ("IDS") on July 1, 2013 containing five references (two of which were Vicor patents). *Id.*, 7/01/2013 Response. On July 29, 2014, the Applicant submitted a second IDS containing five references (all of which were Vicor patents). *Id.*, 7/29/2014 IDS. The first and only Office Action was sent on April 23, 2015, allowing all 35 claims and stating that "none of the prior art of record taken alone or in combination shows" the claimed limitations. *Id.*, 4/23/2015 Office Action. The Office Action included a Notice of References Cited, containing five additional references beyond the 10 identified in the IDS submissions. *Id.* A Notice of Allowance was sent on July 15, 2015, and the '481 Patent issued on October 20, 2015.

IV. PERSON OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) at the time of the ’481 Patent (whether that date is March 14, 2013 or April 2010) would have at least a Master’s degree in electrical engineering and two or more years of work experience relating to power electronics and the design and control of switching power converters, with more experience potentially substituting for education, or vice-versa. Ex. 1017, 79; Ex. 1003, ¶ 29.

V. SUMMARY OF THE PRIOR ART

A. McDonald (Ex. 1005)

McDonald is a paper from the 2012 Texas Instruments Power Supply Design Seminar entitled “Design and Optimization of a High Performance LLC Converter.” Ex. 1005, Cover. The paper was publicly available by September 25, 2012. Ex. 1016, ¶¶ 46-49; Ex. 1021.

McDonald discusses the design of a resonant LLC converter that uses a digital controller to control the primary and secondary switches of the converter, including at zero voltage and zero current switching conditions. Ex. 1005, Abstract, 5-3, Fig. 1; Ex. 1003, ¶ 41. Figure 1 of McDonald “illustrates the basic schematic for a half-bridge LLC power stage as well as the critical operating variables in the system.” Ex. 1005, 5-3.

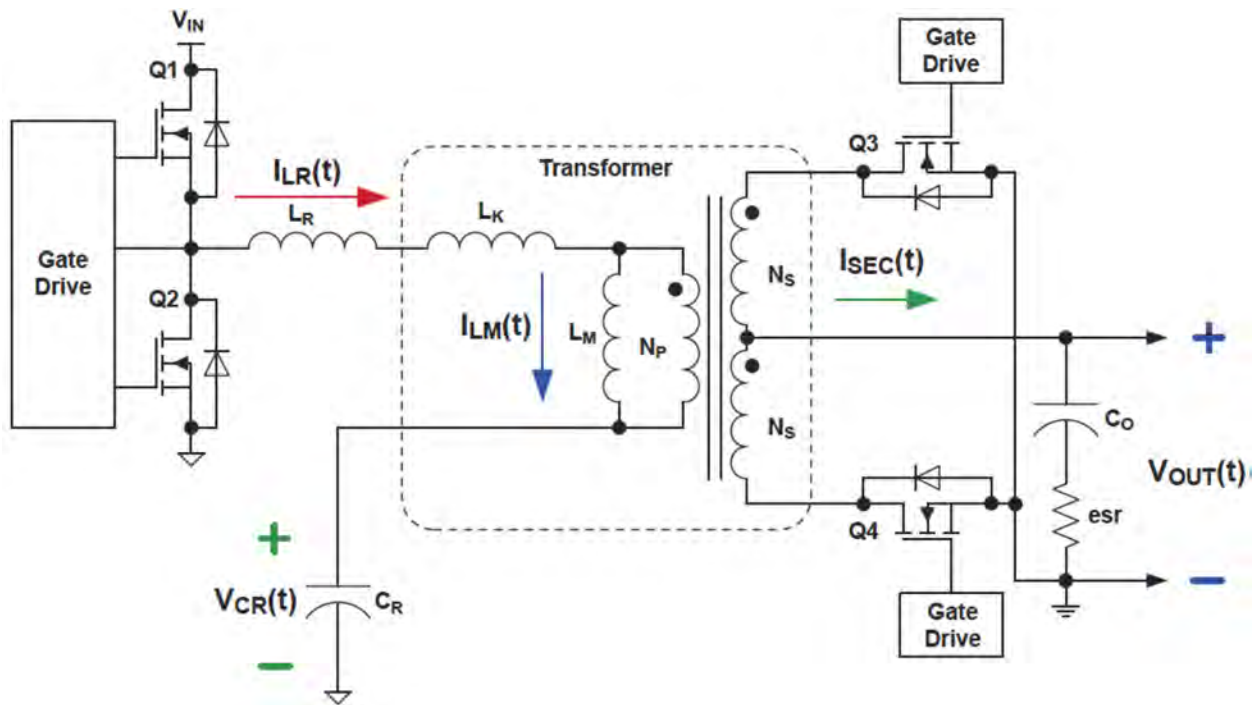


Figure 1 – Basic LLC schematic.

Ex. 1005, Figure 1. The resonant LLC converter shown in Figure 1 of McDonald contains: two primary side MOSFET switches (Q1 and Q2); two secondary side MOSFET switches (Q3 and Q4); a resonant tank on the primary side depicted by two inductors (L_R and L_M) and a capacitor (C_R); a transformer; and gate drive circuitry (Gate Drive) for controlling the converter. *Id.*; Ex. 1003, ¶ 42.

McDonald explicitly states that the converter depicted therein uses “a Texas Instruments UCD3138 digital controller” to facilitate “easy optimization and evaluation of the various control features” discussed. Ex. 1005, 5-22. The TI UCD3138 digital controller is discussed in greater detail below as another prior art reference in this Petition. This digital controller contains an oscillator for generating

clock signals for the controller, and also generates the various timing signals to control the switching of the switches in the resonant power converter. Ex. 1003, ¶ 43.

B. TI UCD3138 (Ex. 1006)

TI UCD3138 is a Texas Instruments data manual for the UCD3138 Highly Integrated Digital Controller for Isolated Power, published in March 2012. Ex. 1006, Cover. The manual discusses that the UCD3138 is a digital power supply controller that is “suitable for a wide variety of power conversion applications. Ex. 1006, 7.

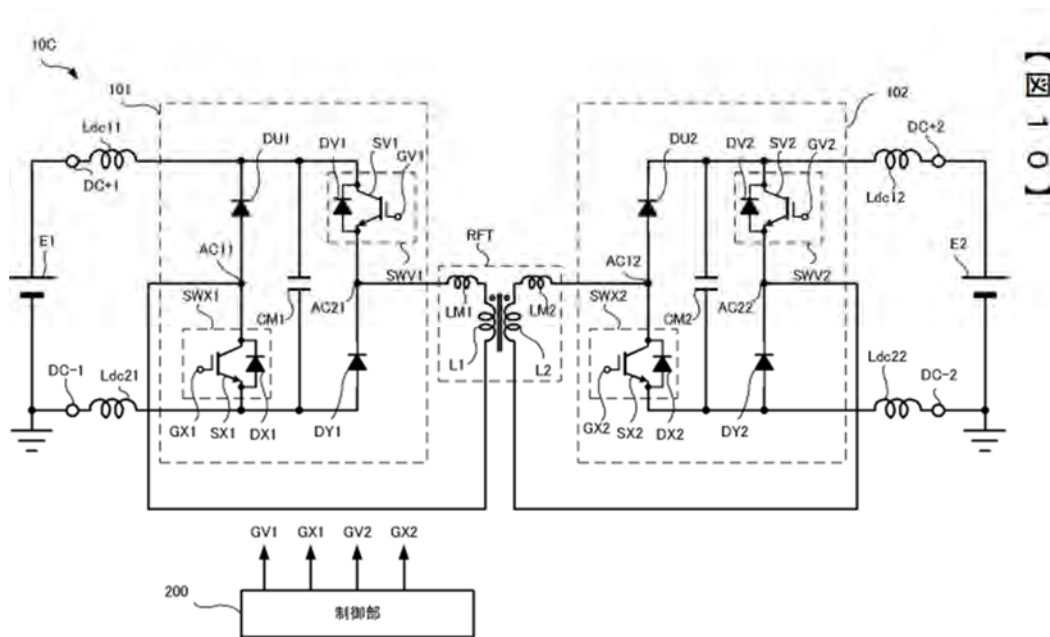
The manual also discusses that specific power management peripherals have been added to the controller to allow for a variety of operating features, including “LLC and phase shifted full bridge mode switching,” which refers to zero voltage and zero current switching. *Id.*; Ex. 1003, ¶ 45. The manual states that the device’s “topology support has been optimized” for a variety of configurations, including “LLC half bridge and full bridge.” Ex. 1006, 7.

C. Shimada (Ex. 1007 (original), Ex. 1008 (certified translation))

Shimada is a Japanese patent issued on February 16, 2012, entitled “Current-Fed Series Resonance DC/DC Converter and Power Conversion Control Method.” Ex. 1008, Cover. Shimada discusses a series resonant converter that “can supply bi-directional DC power and soft switching with simple control regardless of the output

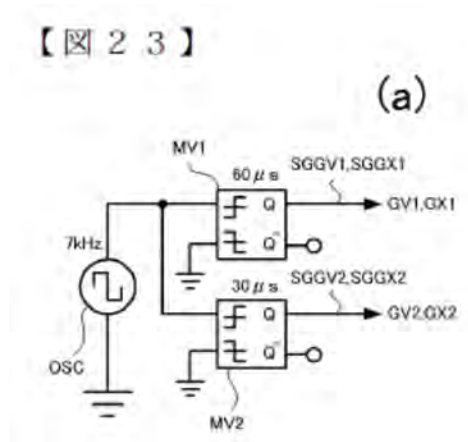
voltage of the power supply.” *Id.*, Abstract.

Figure 10 of Shimada (below) depicts a converter with: two primary side switches (SWV1 and SWX1); two secondary side switches (SWV2 and SWX2); a resonant tank circuit on the primary side; a transformer (RFT); and a digital control unit (200) for controlling the converter.



Ex. 1007, Fig. 10.

The digital control unit (200) of Shimada is depicted in Figure 23(a) (below) and includes an oscillator (OSC) for generating clock signals at a preset oscillatory frequency of 7kHz.

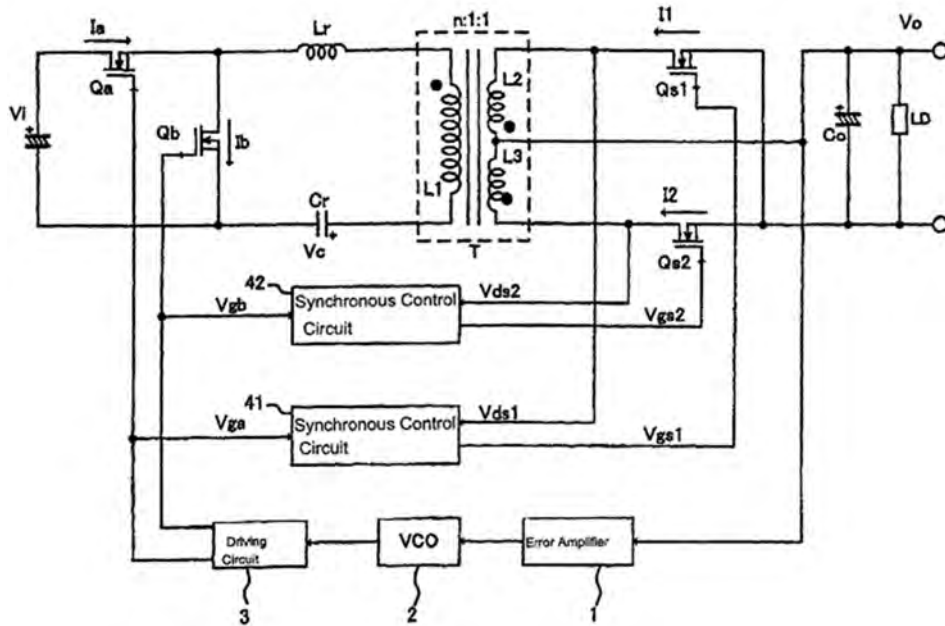


Id., Fig. 23(a); Ex. 1008, ¶ [0137].

D. Chen (Ex. 1010)

Chen is a U.S. patent issued on August 14, 2012, entitled “Switching Power Supply Device and Switching Power Supply Control Circuit.” Ex. 1010, Cover. Chen discusses a series resonant switching power supply device that utilizes a synchronous control circuit for controlling the primary and secondary switches of the power supply device. *Id.*, Abstract, 7:23-34.

Figure 1 of Chen (below) depicts a power supply converter with: two primary side MOSFET switches (Qa and Qb); two secondary side MOSFET switches (Qs1 and Qs2); a resonant circuit on the primary side (Lr, Cr); a transformer (T); and control circuitry for controlling the converter. The control circuitry includes an oscillator (VCO), a gate drive circuit (Driving Circuit), and control signals (Vga, Vgb, Vgs1, and Vgs2) for controlling the switches in the converter.

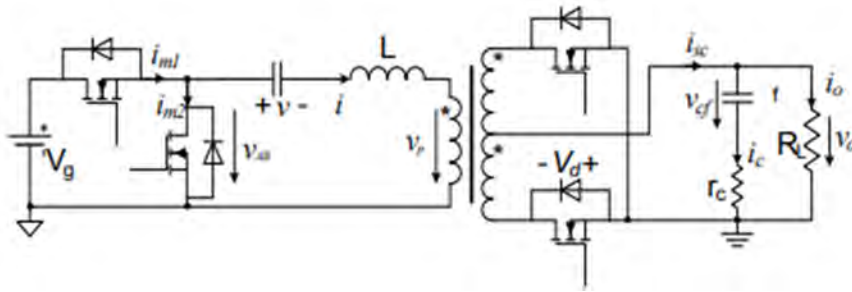


Ex. 1010, Fig. 1.

E. Pan (Ex. 1011)

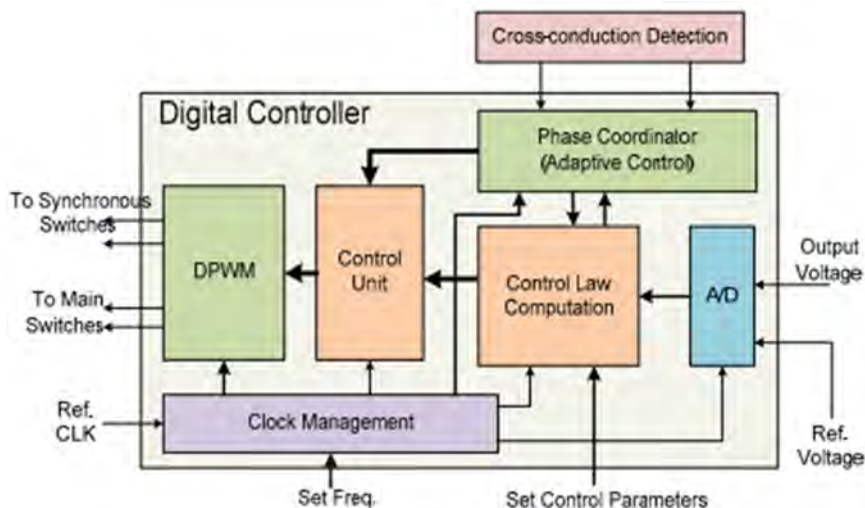
Pan is a conference paper from the 2008 IEEE Power Electronics Specialists Conference entitled “Secondary-side Adaptive Digital Controlled Series Resonant DC-DC Converters for Low Voltage High Current Applications.” Ex. 1011, Cover. The conference was held on June 15-19, 2008, and the paper was published no later than August 8, 2008. Ex. 1016, ¶ 39-45.

Pan describes a series resonant converter that utilizes a digital controller for controlling the primary and secondary switches of the converter. Ex. 1011, § II, Fig. 1, Fig. 11. Figure 1 of Pan (below) shows a series resonant converter with: two primary side MOSFET switches (M1 and M2); two secondary side MOSFET switches (S1 and S2); a resonant circuit on the primary side; and a transformer.



Ex. 1011, Fig. 1, 712. Regarding the converter, Pan also states that “[t]he main stage on the primary side of the transformer could be either half bridge or full bridge with L-C series resonant tank” and that “[t]he main switches (M1 & M2) operate in complementary mode against input voltage variations. The rectifier switches (S1 & S2) operate in PWM control mode against load variations.” *Id.* 712.

Pan’s Figure 11 shows the architecture of the digital controller used to control the series resonant converter.



Ex. 1011, Fig. 11. The digital controller includes a control unit, a digital pulse width modulator (DPWM), and clock management. *Id.*

F. Peng (Ex. 1012)

Peng is a U.S. patent issued on April 9, 2002, entitled “Isolated and Soft-Switched Power Converter.” Ex. 1012, Cover. Peng discusses a soft-switched power converter with resonant tank circuits on either side of an isolation transformer. *Id.*, Abstract. Peng’s Figure 6 (below) depicts a power converter with: primary side MOSFET switches (S1 and S2), secondary side switches (S3 and S4), a transformer (104), and resonant tank circuits on the primary side and secondary sides of the transformer.

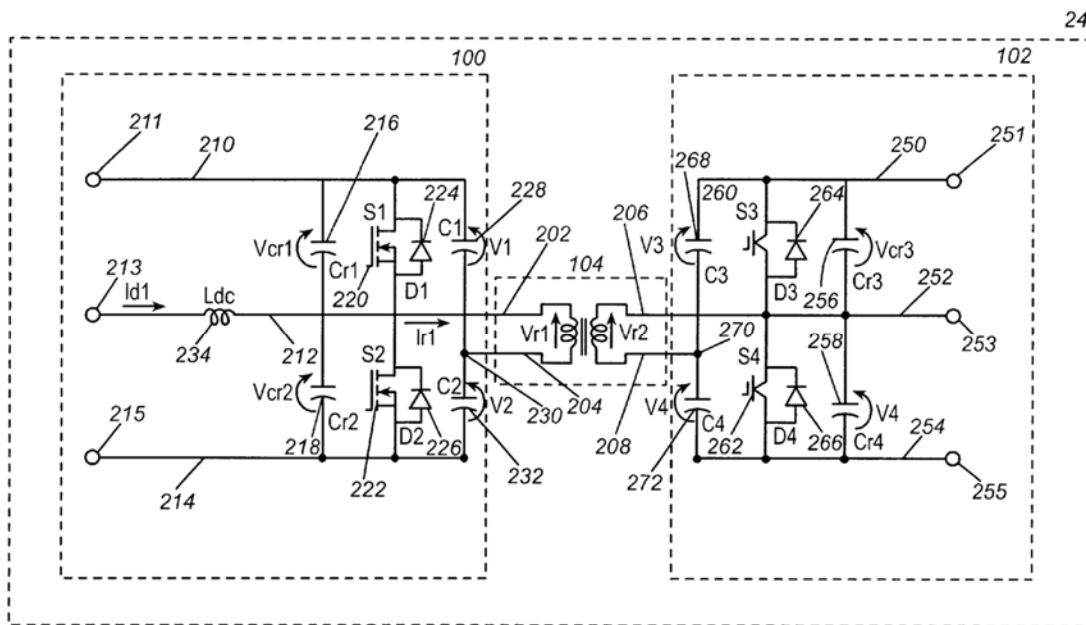


FIG. 6

Ex. 1012, Fig. 6.

Peng’s Figure 5 (below) is a block diagram of the power converter, which shows the switching controller (160) for controlling the primary and secondary switches. Peng notes that “[m]any suitable computing stations and circuits may

serve as the switching controller 160, including personal computers, workstations, minicomputers, application-specific digital/analog integrated circuits, and so forth.”

Id., 14:54-58.

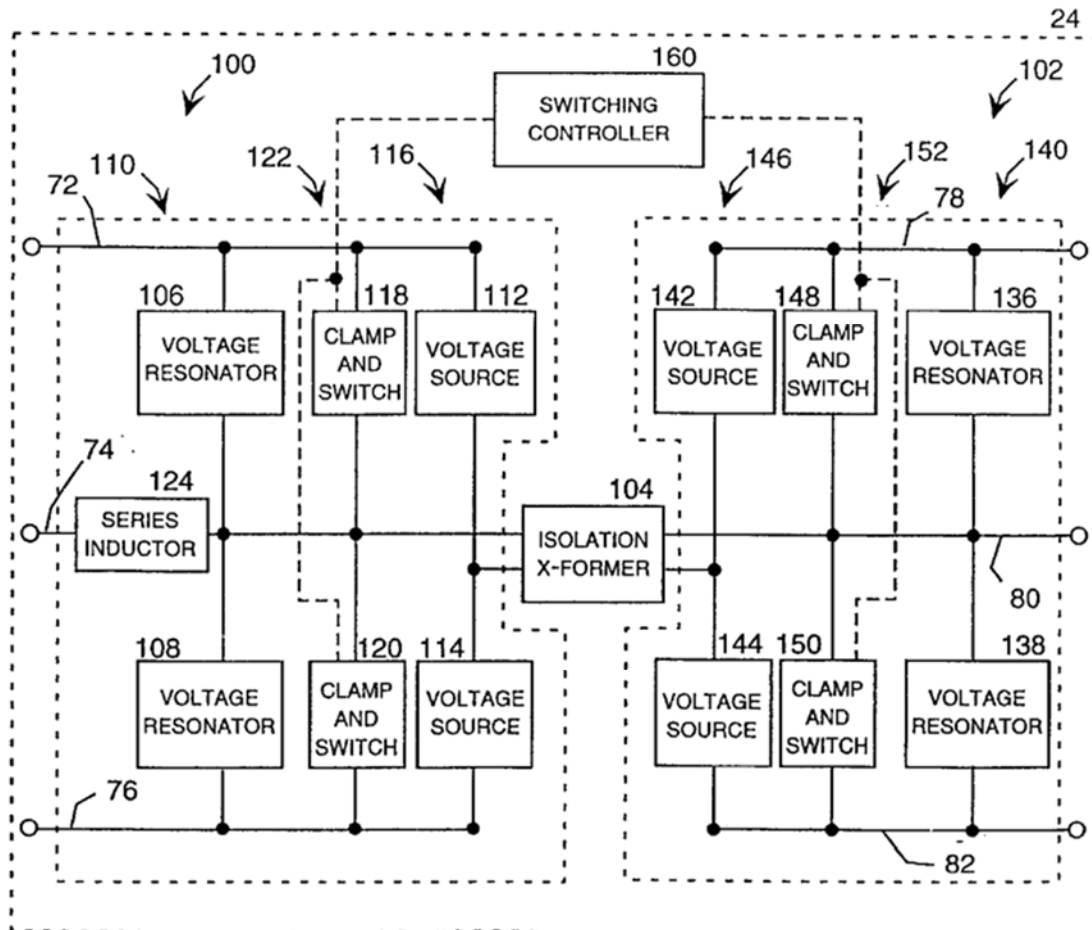


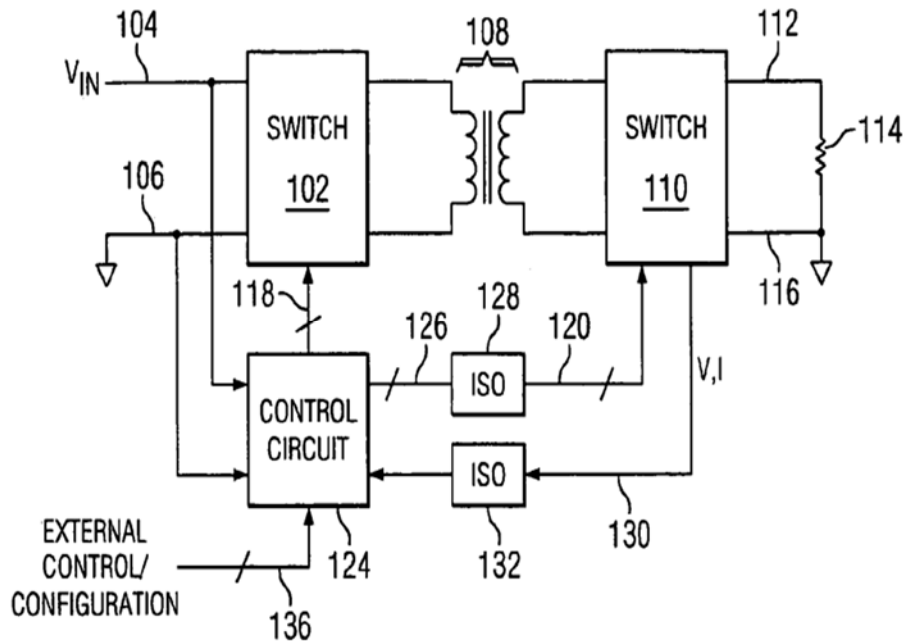
FIG. 5

Ex. 1012, Fig. 5.

G. Leung (Ex. 1013)

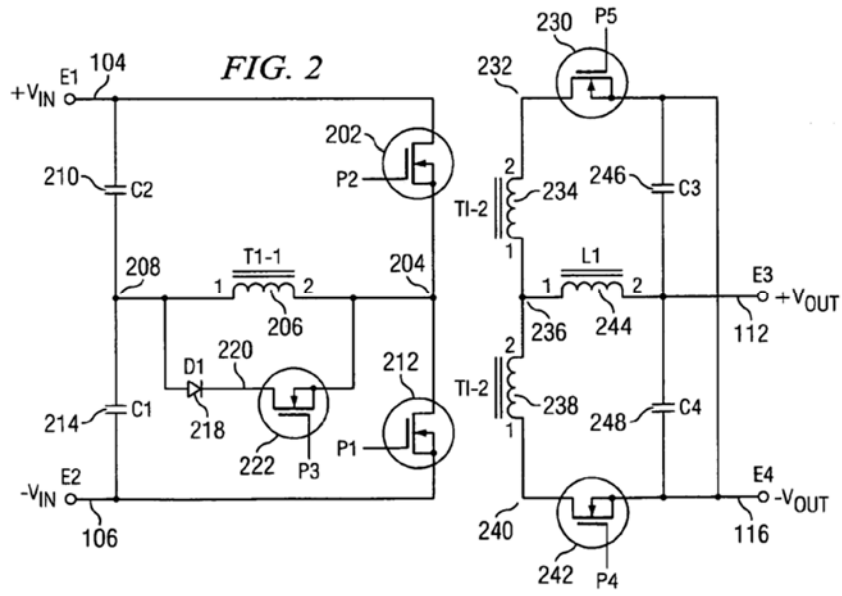
Leung is a U.S. patent application filed March 31, 2005 and published October 5, 2006, entitled “Digital PWM Controller.” Ex. 1013, Cover. Leung issued as U.S. Patent No. 7, 428,159 on September 23, 2008. *Id.*, Ex. 1014, Cover.

Figure 1 of Leung (below) shows a power converter with: a primary switch group (102), a secondary switch group (110); a transformer (108); and a digital control circuit (124).



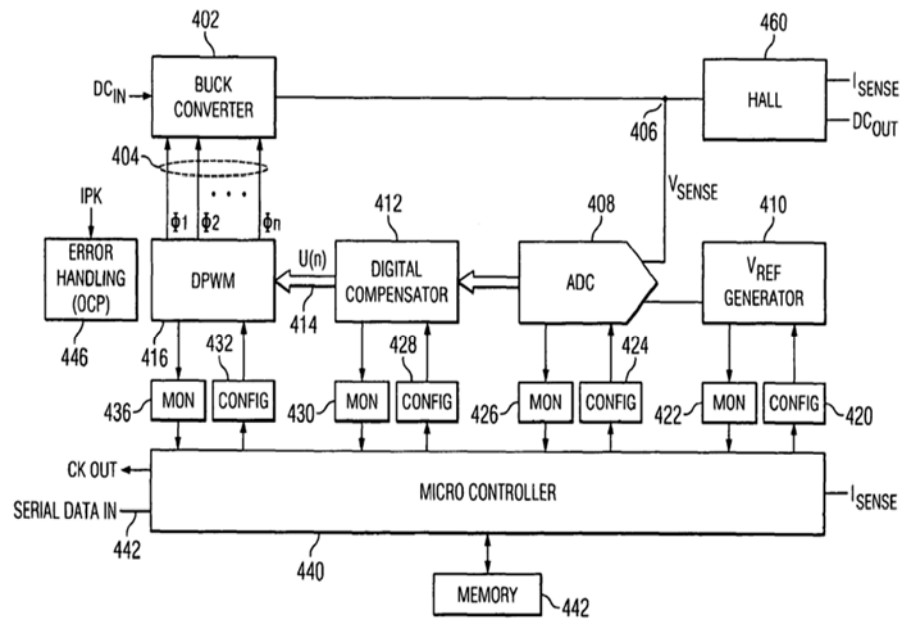
Ex. 1013, Fig. 1

Figure 2 of Leung (below) shows a more detailed schematic diagram of the primary switch group (102), the secondary switch group (110), and the isolation transformer (108).



Ex. 1013, Fig. 2

Figure 4 of Leung (below) shows a block diagram of the digital controller 124 in Figure 1.



Ex. 1013, Fig. 4.

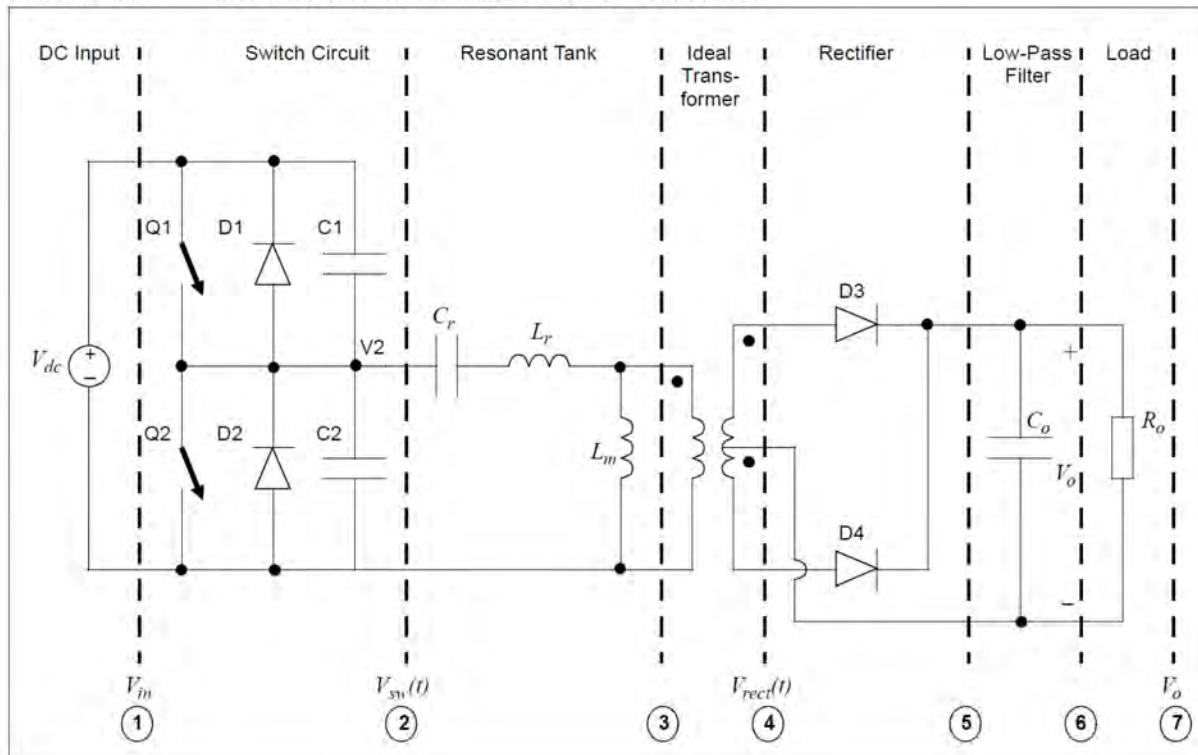
H. TI UCD3040 (Ex. 1018)

TI UCD3040 is a Texas Instruments datasheet for the UCD3040, UCD3028, and UCD3020 Digital Power Controllers, published in November 2010. Ex. 1018, 1. The datasheet discusses that UCD3040 is suitable for “isolated AC/DC and DC/DC power supplies.” *Id.* The datasheet also discusses that it supports a wide range of topologies, including “ half-bridge, phase-shifted full bridge, active clamp, and resonant LLC.” *Id.* at 2.

I. AN1336 (Ex. 1019)

AN1336 is Microchip datasheet for the AN1336 DC/DC LLC Reference Design Using the dsPIC DSC, published in 2010. Ex. 1019, 1. The datasheet discusses LLC resonant converters and control thereof using Microchip’s dsPIC digital signal controllers. *Id.* Ex. 1003, ¶¶ 63-65.

FIGURE 10: LLC CIRCUIT COMPONENTS AND SECTIONS



Ex. 1019, Figure 10.

J. dsPIC33FJ06GS101 (Ex. 1020)

dsPIC33FJ06GS101 is a Microchip datasheet for the dsPIC33FJ06GS101 Digital Signal Controller, published in January 2012. Ex. 1020, 374 (“Revision F (January 2012)”). The datasheet discusses that it provides high-speed PWM “with independent timing” and an internal oscillator. *Id.*, 1.

K. AAPA (Exs. 1001, 1009)

The '481 Patent discloses multiple instances of AAPA related to zero voltage and zero current switching. Ex. 1003, ¶¶ 67-70.

VI. SPECIFIC GROUNDS FOR PETITION

A. Ground I: Obvious over McDonald in view of TI UCD3138

McDonald (Ex. 1005) combined with TI UCD3138 (Ex. 1006) renders obvious claims 1, 22, and 31-35 of the '481 Patent. A POSITA would have been motivated to combine McDonald with TI UCD3138 because McDonald explicitly states that the converter depicted therein uses “a Texas Instruments UCD3138 digital controller” to facilitate “easy optimization and evaluation of the various control features.” Ex. 1005, 5-22. A POSITA would therefore have understood and expected that TI UCD3138 and its teachings could be used as the digital controller for the converter disclosed in McDonald. Ex. 1003, ¶¶ 72-73.

1. Claim 1

a. Limitation 1[a]³

To the extent the preamble is limiting, McDonald teaches it. Ex. 1003, ¶¶ 74-75. McDonald teaches a method of synchronously operating a half-bridge power converter, where the converter has at least one primary switch that drives a resonant circuit, at least one secondary switch, and a transformer. Ex. 1005, 5-3 (“Figure 1 illustrates the basic schematic for a half-bridge LLC power stage as well as the

³ See Appendix of Challenged Claims at the end of this Petition for corresponding claim language of each claim limitation.

critical operating variables in the system.”). McDonald’s Figure 1 (below) shows a half-bridge converter with primary switches Q1 and Q2 (blue), a resonant circuit (LLC) on the primary side (with a resonant frequency and period) consisting of inductor L_R , inductor L_M , and capacitor C_R , secondary switches Q3 and Q4 (pink), and a transformer (yellow).

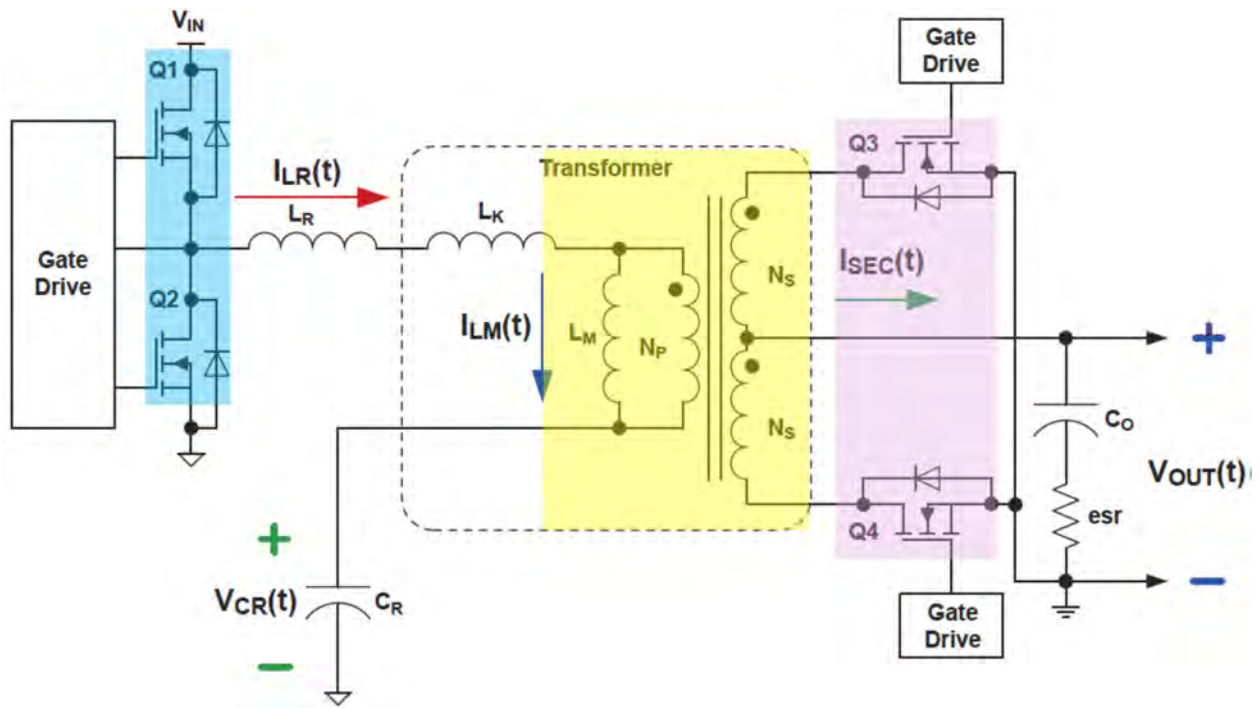


Figure 1 – Basic LLC schematic.

Ex. 1005, Fig. 1.

b. Limitation 1[b]

McDonald in combination with TI-UCD3138 (hereinafter, “McDonald-TI UCD3138”) renders this limitation obvious. Ex. 1003, ¶¶ 76-78. Figure 1 of McDonald (below) shows that the switches Q1, Q2, Q3, and Q4 are controlled by a

Gate Drive controller (shown in red).

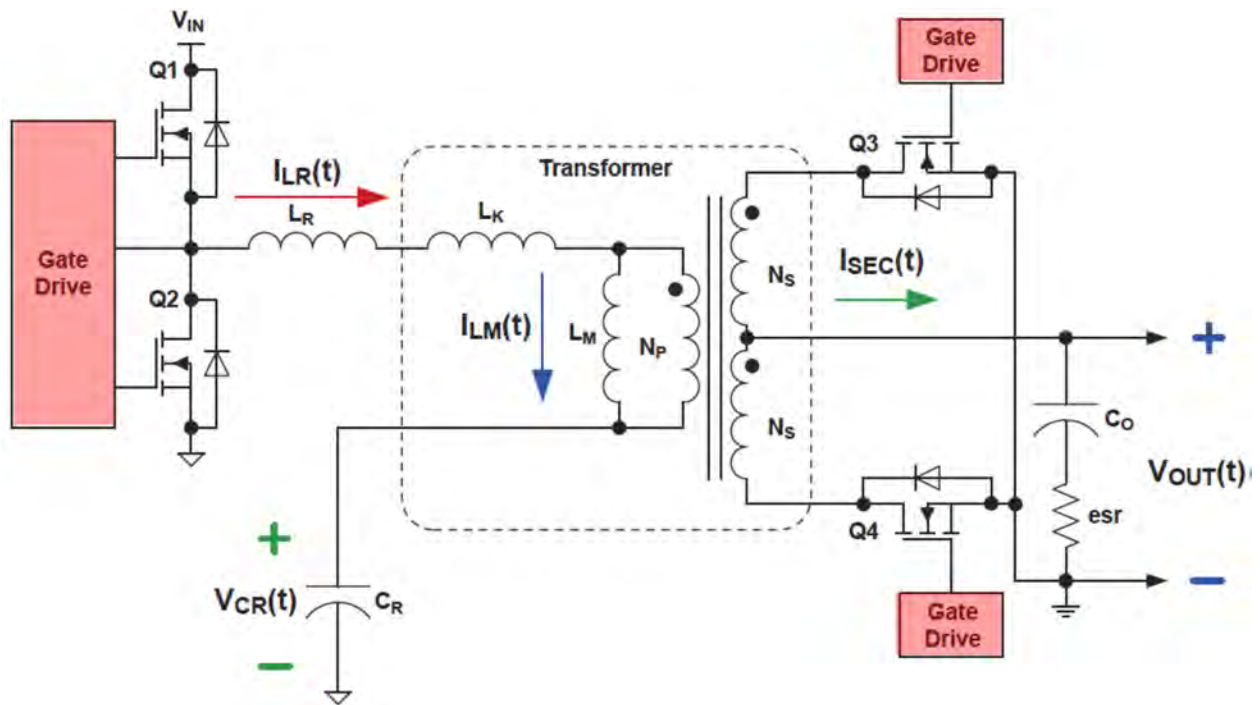
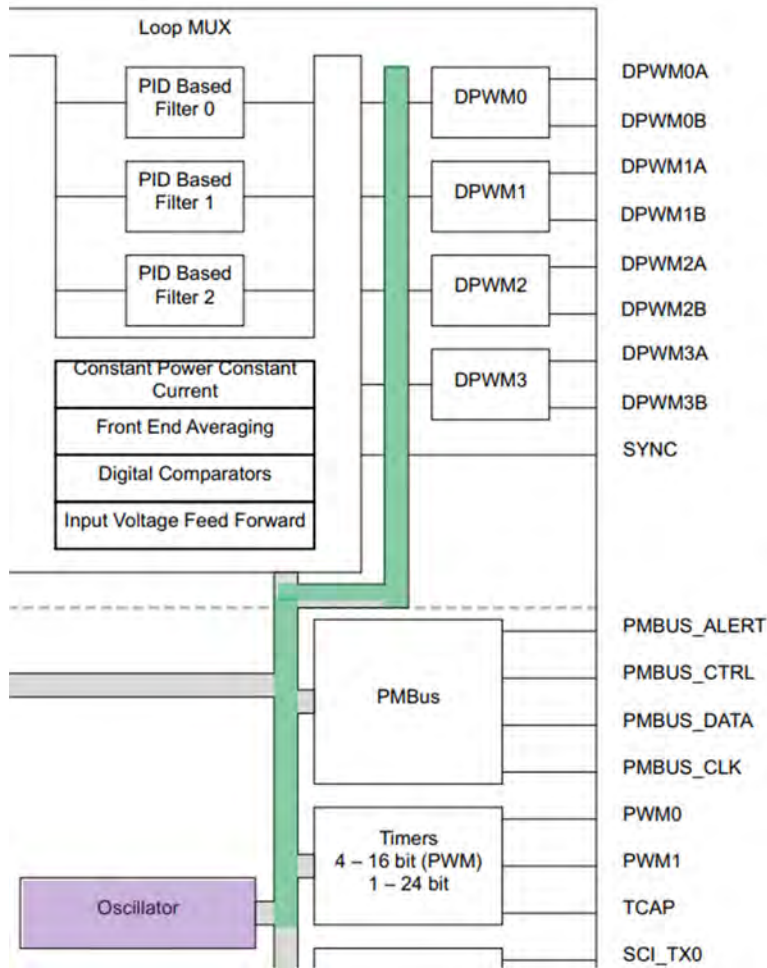


Figure 1 – Basic LLC schematic.

Ex. 1005, Figure 1. As noted above, McDonald also states that its converter uses “a Texas Instruments UCD3138 digital controller” to facilitate “easy optimization and evaluation of the various control features.” Ex. 1005, 5-22. Thus, TI UCD3138 controls the Gate Drives in McDonald. Ex. 1003, ¶ 76.

TI UCD3138 discloses an oscillator with an oscillator frequency that generates clock signals. Ex. 1006, 9 (Fig. 2.4), 17. Figure 2.4 of TI UCD3138 (below) shows an Oscillator (purple) that generates several clock signals (green).



Ex. 1006, Fig. 2.4. The oscillator in TI UCD3138 has an internal oscillator frequency $f_{(PCLK)}$ with a typical frequency of 250 MHz. *Id.*, 17. TI UCD3138 further discloses that its oscillator generates clock signals.

4.4.1.4 High Resolution DPWM

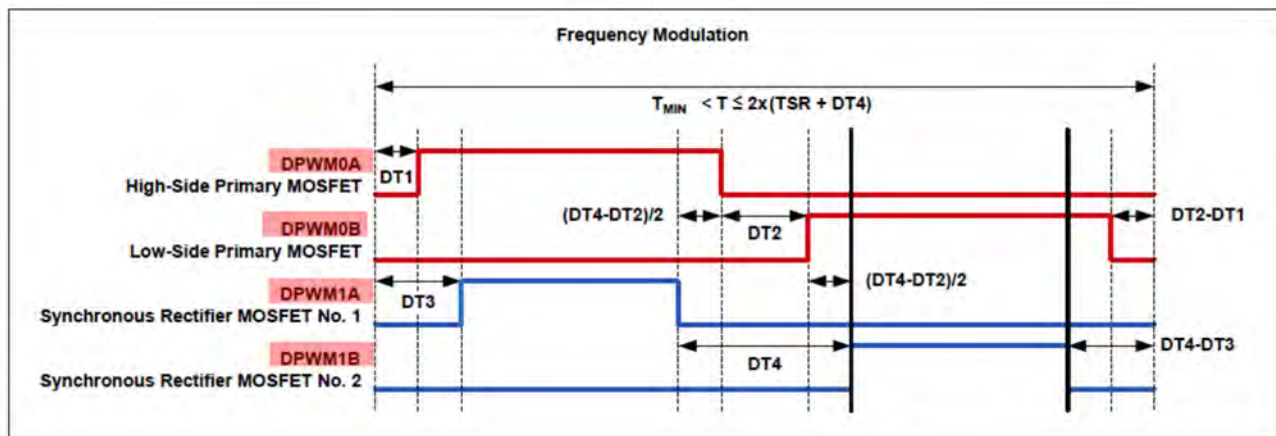
Unlike conventional PWM controllers where the frequency of the clock dictates the maximum resolution of PWM edges, the UCD3138 DPWM can generate waveforms with resolutions as small as 250 ps. This is 16 times the resolution of the clock driving the DPWM module.

This is achieved by providing the DPWM mechanism with 16 phase shifted clock signals of 250 MHz each. The high resolution section of DPWM can be enabled or disabled, also the resolution can be defined in several steps between 4ns to 250ps. This is done by setting the values of PWM_HR_MULTI_OUT_EN, HIRES_SCALE and ALL_PHASE_CLK_ENA inside the DPWM Control Register 1. See the Power Peripherals programmer's manual for details.

Id., 30.

c. Limitation 1[c]

McDonald-TI UCD3138 renders this limitation obvious. Ex. 1003, ¶¶ 79-81. Figure 25 of McDonald (below) shows that timing control signals DPWM0A, DPWM0B, DPWM1A, and DPWM1B (highlighted in red) control both the primary switches (High-Side Primary MOSFET and Low-Side Primary MOSFET) and the secondary switches (Synchronous Rectifier MOSFET No. 1 and Synchronous Rectifier MOSFET No. 2).



Ex. 1005, Figure 25; *Id.*, 5-17 (“Figure 25 illustrate the exact timing relationships between the primary-side MOSFET control signals and the synchronous-rectifier control signals.”).

TI UCD3138 also teaches that each DPWM can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28. When combined with McDonald, the timing control signals are based on clock signals in the resonant converter operating cycle, having a resonant period and frequency. Ex. 1005, 5-4 (“the operating frequency is exactly equal to the dominant frequency of the resonant tank.”); Ex. 1003, ¶ 81.

d. Limitation 1[d]

McDonald-TI UCD3138 renders this limitation obvious. Ex. 1003, ¶¶ 82-85. McDonald teaches that primary switches Q1 and Q2 turn on and off with zero voltage switching. Ex. 1005, 5-3 (“Figure 2 illustrates how this system achieves zero voltage switching (ZVS) on Q1 and Q2. . . . State 1 shows that V_{DS} of Q2 is charged all the way to V_{in} , with the inductor current flowing through the channel of Q1. When Q1 turns off, the current that was flowing through Q1’s channel diverts

and flows through the two capacitors, as shown in state 2.⁴ This state continues until the V_{DS} of Q2 has dropped low enough to forward-bias the diode across Q2. At this point operation transitions to state 3. Now the system is free to turn on Q2 with a near zero voltage, thus achieving the so-called ZVS, as shown in state 4.”)

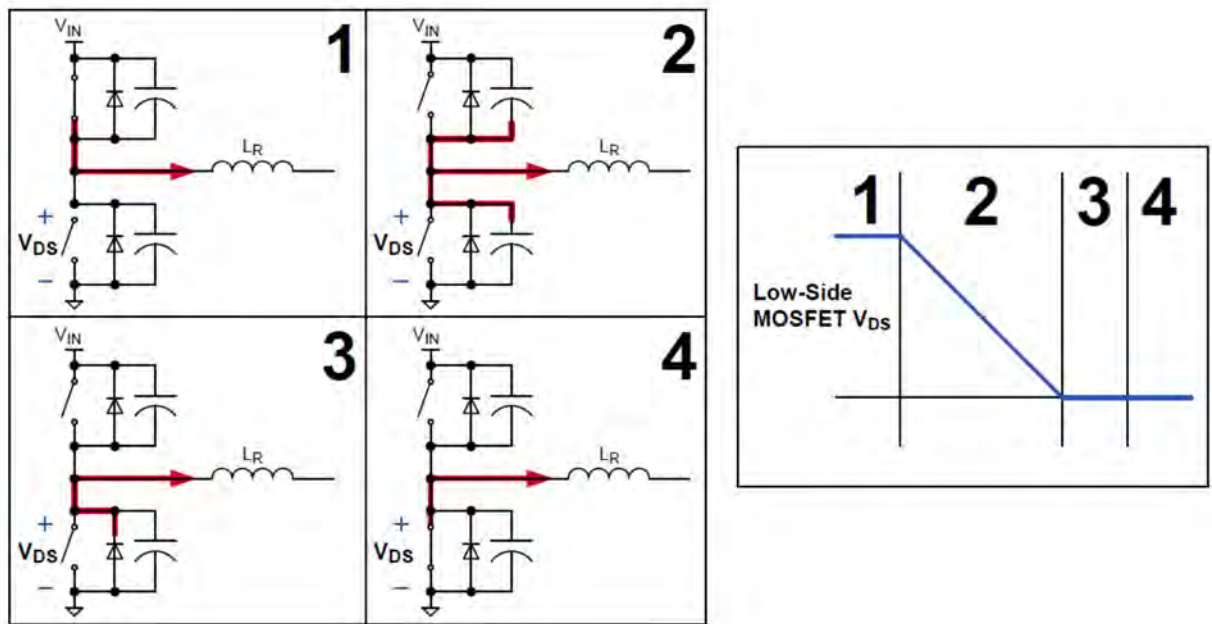


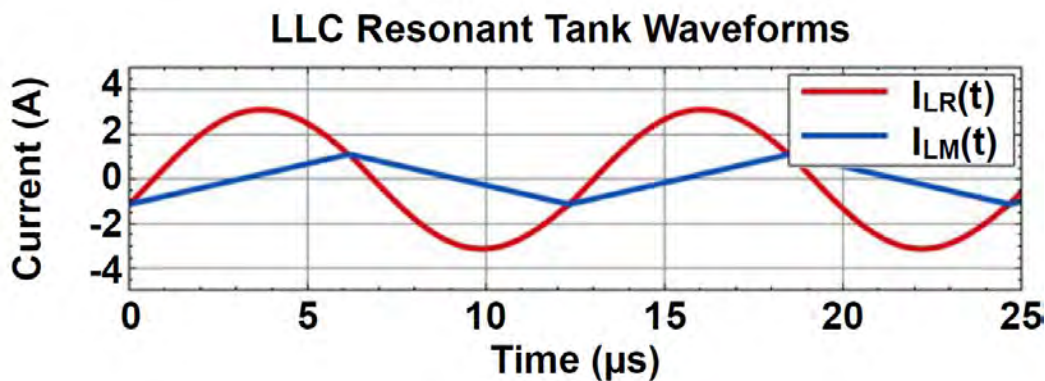
Figure 2 – Zero voltage switching.

Ex. 1005, 5-4.

McDonald also teaches that primary switches Q1 and Q2 turn on and off when zero resonant current is flowing in the switch. Ex. 1003, ¶ 83. McDonald shows a primary winding current I_{LR} , which is equal to the primary magnetizing current I_{LM}

⁴ The V_{DS} of Q2 remains at V_{in} and thus Q1 has turned off with essentially zero voltage impressed across it.

plus the resonant current I_{RES} ; meaning $I_{LR} = I_{LM} + I_{RES}$.⁵ *Id.* Thus, the resonant current is equal to the primary winding current minus the primary magnetizing current ($I_{RES} = I_{LR} - I_{LM}$), and the resonant current is zero when the primary winding current I_{LR} and primary magnetizing current I_{LM} are equal. *Id.* Figure 3 of McDonald (below) shows that the resonant current is zero at the points where I_{LR} (red) and I_{LM} (blue) are the same (i.e. at the minimum and maximum points of blue waveform I_{LM}). *Id.* ¶ 84.



Ex. 1005, Figure 3. McDonald also teaches that primary switches Q1 and Q2 generate a square wave, which produces the triangular-shaped magnetizing current I_{LM} in Figure 3.

⁵ This is the same equation disclosed in the '481 Patent, which states that "Fig. 3B shows the primary winding current, comprising both the resonant current (solid line) and the primary magnetizing current (dashed line)." Ex. 1001, 6:24-27.

To visualize this, recognize that Q1 and Q2 generate a square wave at the input to L_R . This square wave is filtered to produce a sine wave in $I_{LR}(t)$. The voltages across $L_R + L_K$ and C_R are 180 degrees out of phase and equal and opposite in magnitude. These voltages cancel out one another and produce a square wave voltage across L_M . This square wave produces the triangular-shaped current $I_{LM}(t)$ shown in Figure 3.

The input voltage is now reduced so that the system control effort changes the frequency to something below the resonant frequency, as defined by Equation 2.

$$f_x < \frac{1}{2\pi\sqrt{(L_x + L_K)C_R}} \quad (2)$$

Ex. 1005, 5-5. This means that the switches are switching on and off at the minimum and maximum points of the magnetizing current I_{LM} (blue waveform), and as discussed above there is zero resonant current at these points. Ex. 1003, ¶ 85.

e. Limitation 1[e]

McDonald-TI UCD3138 renders this limitation obvious. Ex. 1003, ¶¶ 86-88. McDonald discloses that secondary switches Q3 and Q4 turn on and off with zero current switching. Ex. 1005, 5-5 (“In Figures 3 and 4, notice that the current through Q3 and Q4 naturally decays to 0 A, providing zero current switching (ZCS) for these devices.”) Figure 29 of McDonald (below) also shows zero current turn on and off of the secondary switches Q3 and Q4 because the secondary current I_{SEC} starts at zero and ends at zero. Ex. 1003, ¶ 87.

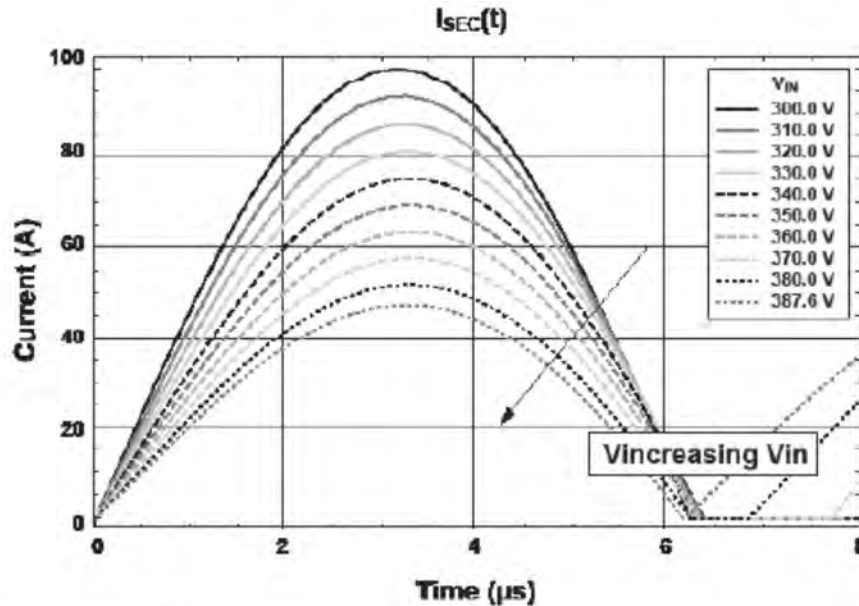


Figure 29 – Synchronous rectifier current and input voltage.

Ex. 1005, 5-19.

McDonald also discloses that secondary switches Q3 and Q4 turn on and off with zero voltage switching. Ex. 1005, 5-21 (“Figures 32, 33 and 34 illustrate this feature in action. . . . Notice that in all cases, the body-diode conduction time across the synchronous rectifiers is very close to minimum.”); Ex. 1003, ¶ 88. A POSITA would understand that MOSFET switches inherently achieve zero voltage at turn off because when a MOSFET switch is on it has zero volts across it, and in the short time it takes to turn off, the voltage does not change significantly because the inherent capacitance of the device mitigates fast changes in voltages. *Id.*

f. Limitation 1[f]

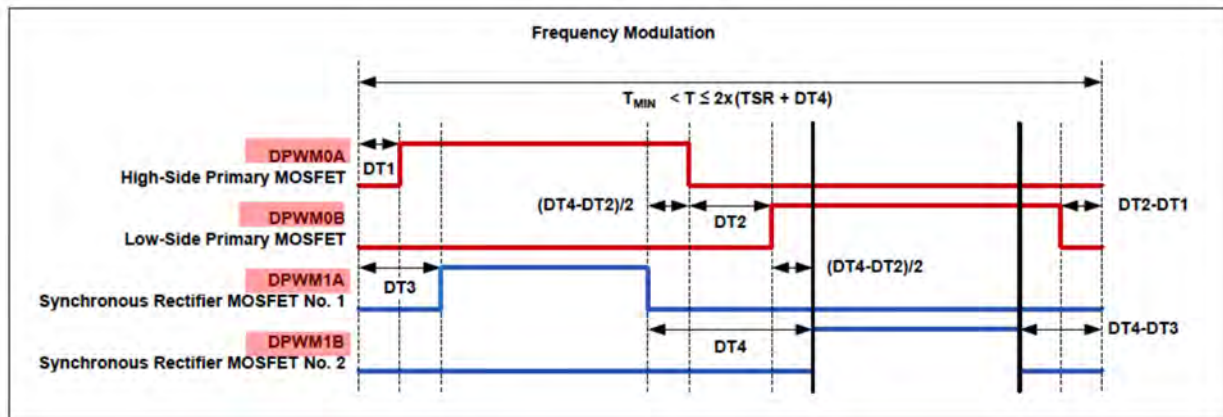
McDonald-TI UCD3138 renders this limitation obvious. Ex. 1003, ¶ 89. The oscillator in TI UCD3138 has an internal oscillator frequency $f_{(PCLK)}$ that is preset,

having a typical frequency of 250 MHz. Ex. 1006, 17.

g. Limitation 1[g]

McDonald-TI UCD3138 renders this limitation obvious. Ex. 1003, ¶¶ 90-92.

McDonald's Figure 25 (below) shows that the timing of the timing control signals DPWM0A, DPWM0B, DPWM1A, and DPWM1B are set independently.



Ex. 1005, 5-18; Ex. 1003, ¶ 90.

TI UCD3138 also discloses that timing of the timing control signals are independent.

4.4.1.2 DPWM Module

The DPWM module represents one complete PWM channel with 2 independent outputs, A and B. Multiple DPWM modules within the UCD3138 system can be configured to support all key power topologies. DPWM modules can be used as independent PWM outputs, each controlling one power supply output voltage rail. It can also be used as a synchronized PWM—with user selectable phase shift between the PWM channels to control power supply outputs with multiphase or interleaved PWM configurations.

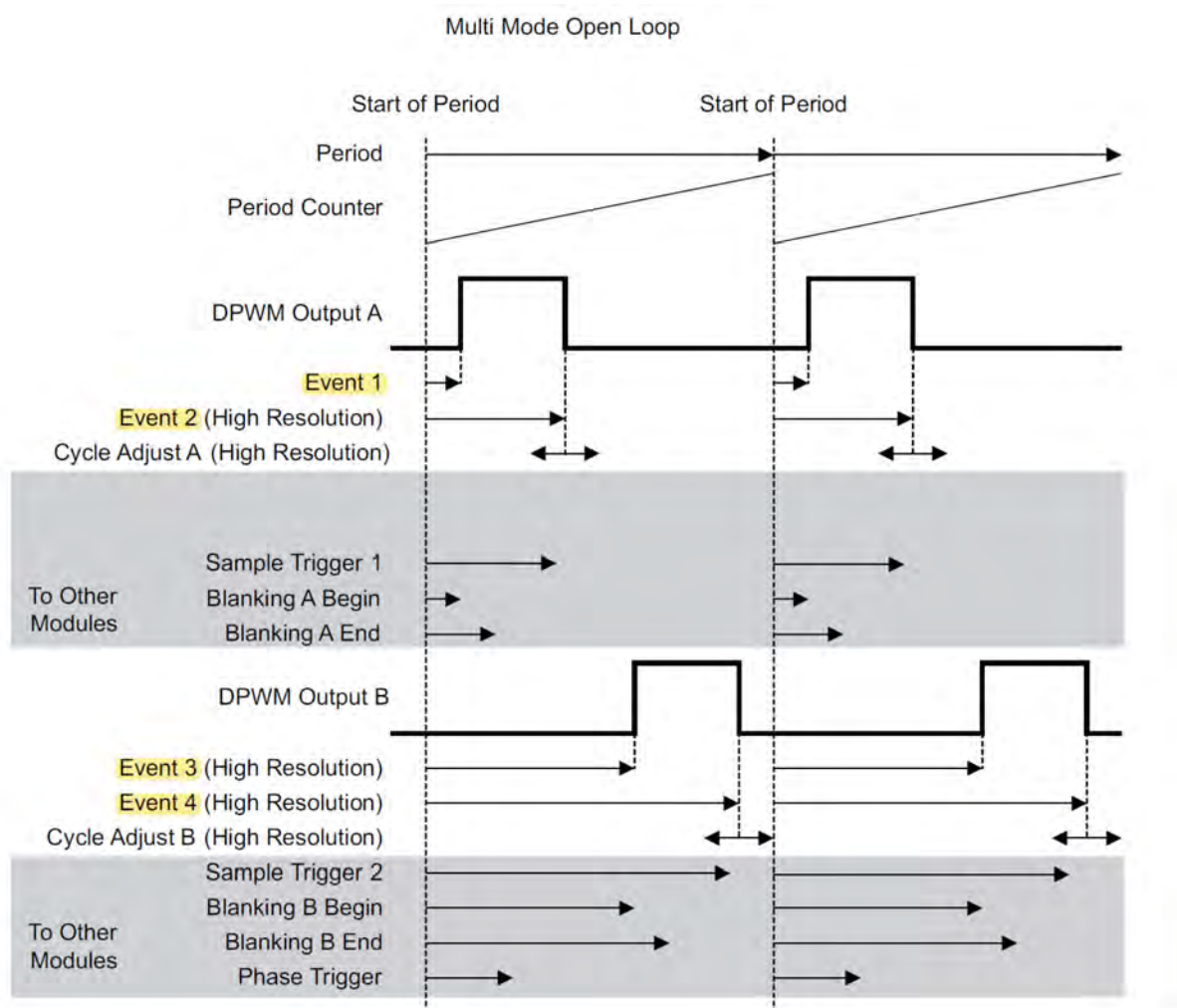
Ex. 1006, 27. TI UCD3138 further teaches that the timing of the timing control signals for various events are independent of each other, by indicating that each DPWM can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28. The Multi-Mode Open Loop figure (below) shows that Events 1-4 are not dependent on the timing of each other or other events. Ex. 1003, ¶ 92.



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
 DPWM A Falling Edge = Event 2 + Cycle Adjust A
 DPWM B Rising Edge = Event 3
 DPWM B Falling Edge = Event 4 + Cycle Adjust B
 Phase Trigger = Phase Trigger Register value

Ex. 1006, 29.

2. Claim 22

a. Limitation 22[a]

See § VI.A.1 above.

b. Limitation 22[b]

McDonald-TI UCD3138 renders this limitation obvious. Ex. 1003, ¶¶ 94-96.

Figure 1 of McDonald (below) shows use of Gate Drive circuits (red), which are controlled by TI UCD3138, to control the switches Q1, Q2, Q3, and Q4. *Id.*

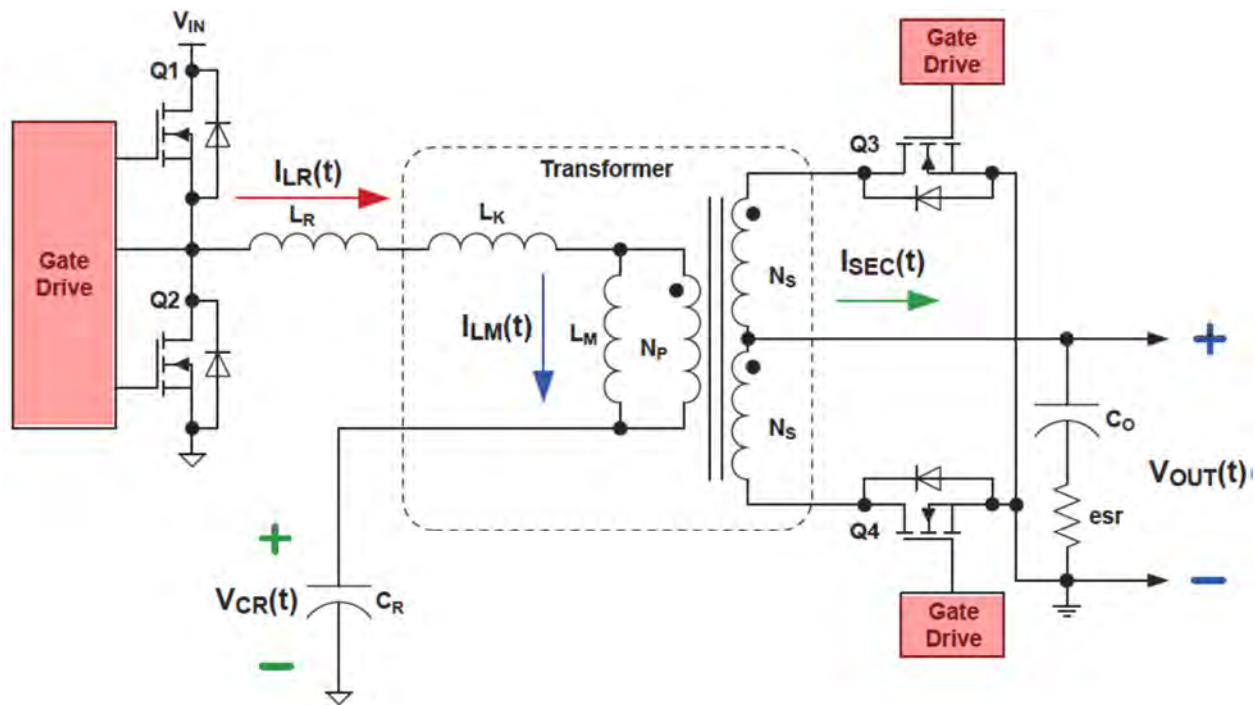
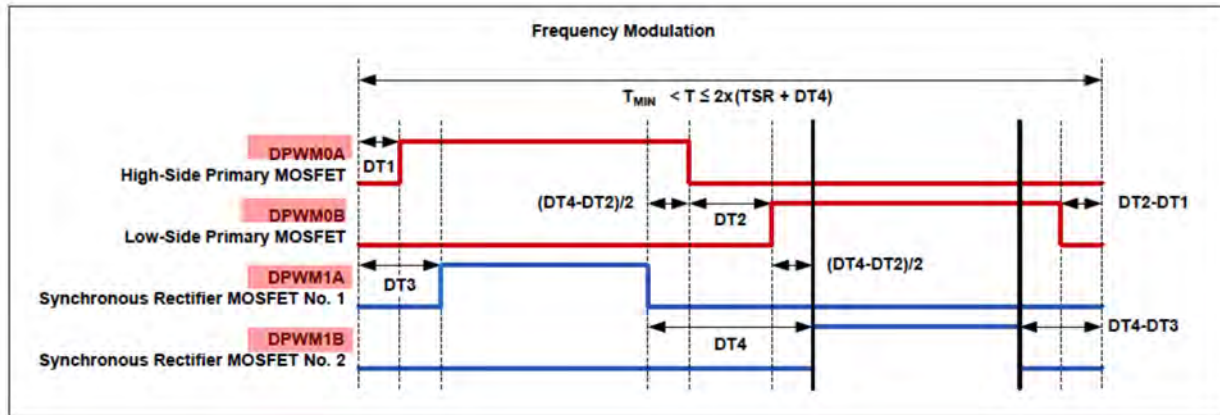


Figure 1 – Basic LLC schematic.

Ex. 1005, Figure 1.

Figure 25 of McDonald (below) further shows use of timing control signals DPWM0A, DPWM0B, DPWM1A, and DPWM1B (highlighted in red) to control both the primary switches Q1 and Q2 (High-Side Primary MOSFET and Low-Side Primary MOSFET) and the secondary switches Q3 and Q4 (Synchronous Rectifier MOSFET No. 1 and Synchronous Rectifier MOSFET No. 2).



Ex. 1005, 5-18.

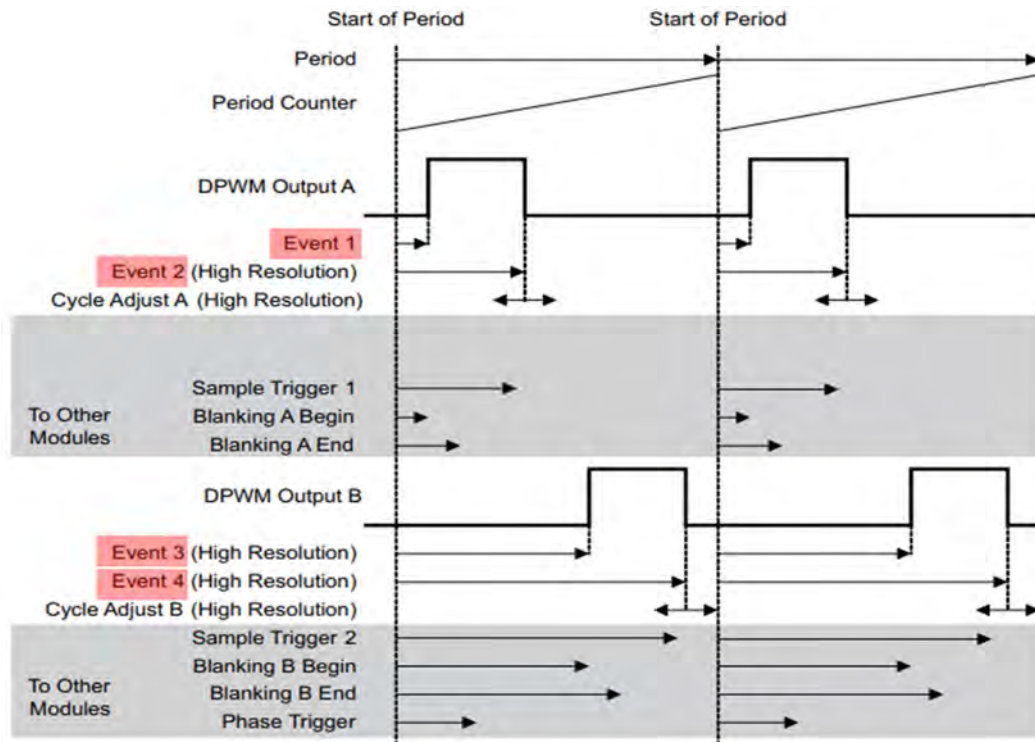
TI UCD3138 further shows that each timing control signal DPWM can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.



Ex. 1006, 29 (showing timing signals for different events).

3. Claim 31

a. Limitation 31[a]

See § VI.A.1.

b. Limitation 31[b]

McDonald-TI UCD3138 renders this limitation obvious. Ex. 1003, ¶ 98. TI UCD3138 teaches that the DPWM's control of the various timing events involves counting the clock signals from the oscillator.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

c. Limitation 31[c]

McDonald-TI UCD3138 renders this limitation obvious. Ex. 1003, ¶ 99. TI UCD3138 teaches that the DPWM sets a count threshold for each event.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

d. Limitation 31[d]

McDonald-TI UCD 3138 renders this limitation obvious. Ex. 1003, ¶ 100. TI UCD3138 teaches that the DPWM generates timing control signals for each event when the counting matches the count threshold.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

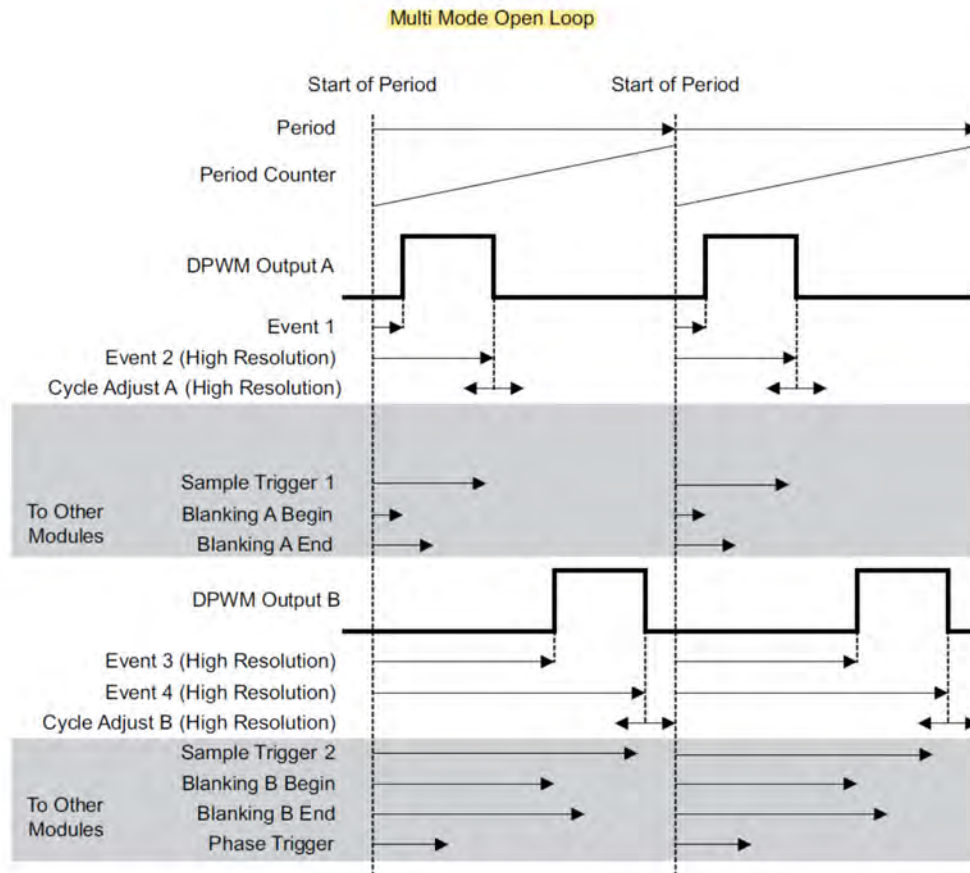
Basic comparisons between the programmed registers and the DPWM counter can create the desired edge placements in the DPWM. High resolution edge capability is available on Events 2, 3 and 4.

Ex. 1006, 28. *See also id.*, 31, 4.5 DPWM Modes of Operation (“... The DPWM logic causes transitions in many digital signals when the period counter hits the target value for that signal.”).

4. Claim 32

McDonald-TI UCD3138 renders this limitation obvious. Ex. 1003, ¶ 101; *see* § VI.A.3 above. TI UCD3138 contains a Multi-Mode Open Loop figure (below), stating that the DPWM is controlled entirely by its own registers and not by the filter

output.



Events which change with DPWM mode:

DPWMA Rising Edge = Event 1
 DPWMA Falling Edge = Event 2 + Cycle Adjust A
 DPWM B Rising Edge = Event 3
 DPWM B Falling Edge = Event 4 + Cycle Adjust B
 Phase Trigger = Phase Trigger Register value

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

The drawing above is for multi-mode, open loop. Open loop means that the DPWM is controlled entirely by its own registers, not by the filter output. In other words, the power supply control loop is not closed.

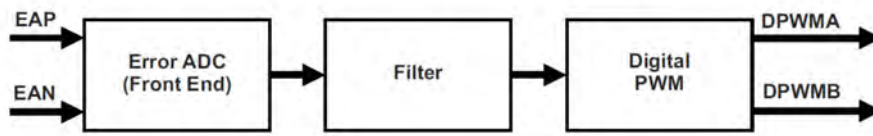
Ex. 1006, 29.

5. Claim 33

McDonald-TI UCD3138 renders this limitation obvious. Ex. 1003, ¶ 102; see § VI.A.3 above. McDonald teaches adjusting the oscillator and timing events with

feedback from measurements in the power train. Ex. 1005, 5-19 (“Traditionally, you can solve this problem by using some kind of current sensing circuitry to determine when the synchronous rectifier should be on and off.”). TI UCD3138 also teaches this limitation of adjusting timing events with feedback provided by the Filter.

These can be connected in many different combinations, with multiple filters and DPWMs. They are capable of supporting functions like input voltage feed forward, current mode control, and constant current/constant power, etc.. The simplest configuration is shown in the following figure:



Ex. 1006, 26.

6. Claim 34

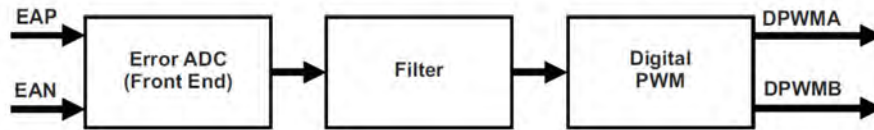
McDonald-TI UCD3138 renders this limitation obvious. Ex. 1003, ¶ 103; *see* § VI.A.4 above. TI UCD3138 teaches use of firmware data for performing certain measurements, and firmware is set during the manufacturing process. Ex. 1006, 22, 4.2 Memory (“Within the UCD31xx architecture, there is a 1024x32-bit Boot ROM that contains the initial firmware startup routines for PMBUS communication and non-volatile (FLASH) memory download. This boot ROM is executed after power-up-reset checks if there is a valid FLASH program written.”).

7. Claim 35

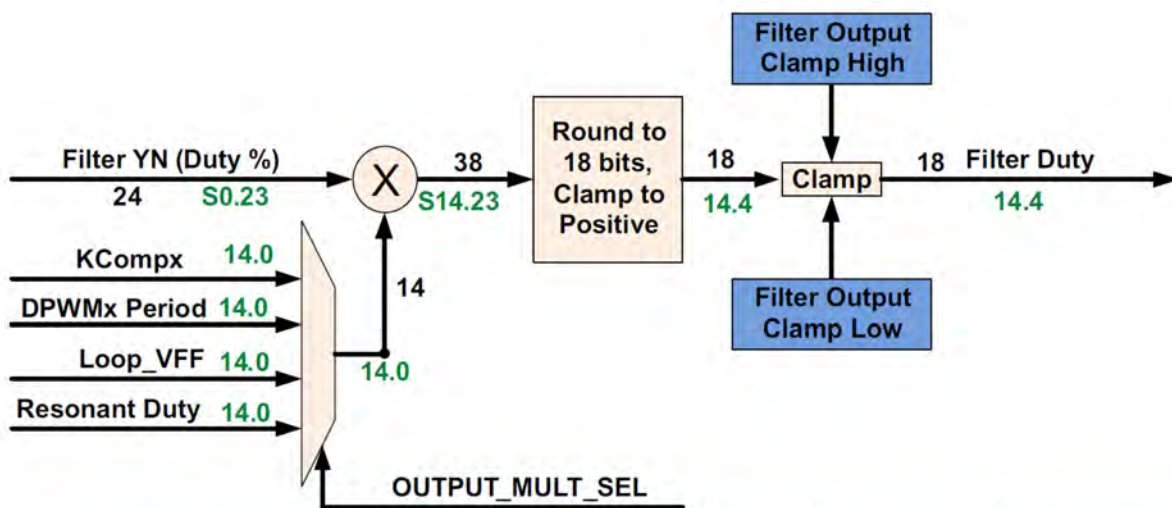
McDonald-TI UCD3138 renders this limitation obvious. Ex. 1003, ¶ 104; *see* § VI.A.4 above. TI UCD3138 teaches that the measurements and adjustments are performed during operation of the device as part of a closed-loop feedback system,

where the Filter provides the feedback.

These can be connected in many different combinations, with multiple filters and DPWMs. They are capable of supporting functions like input voltage feed forward, current mode control, and constant current/constant power, etc.. The simplest configuration is shown in the following figure:



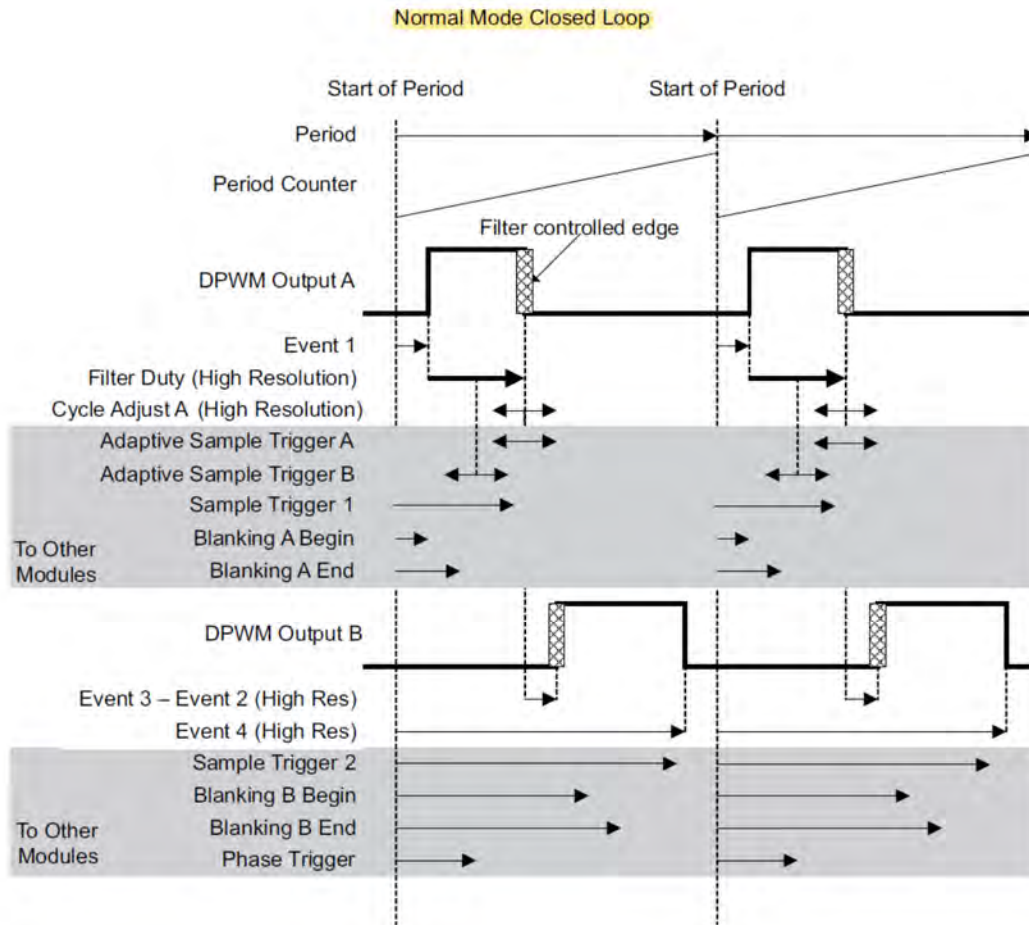
Ex. 1006, 26.



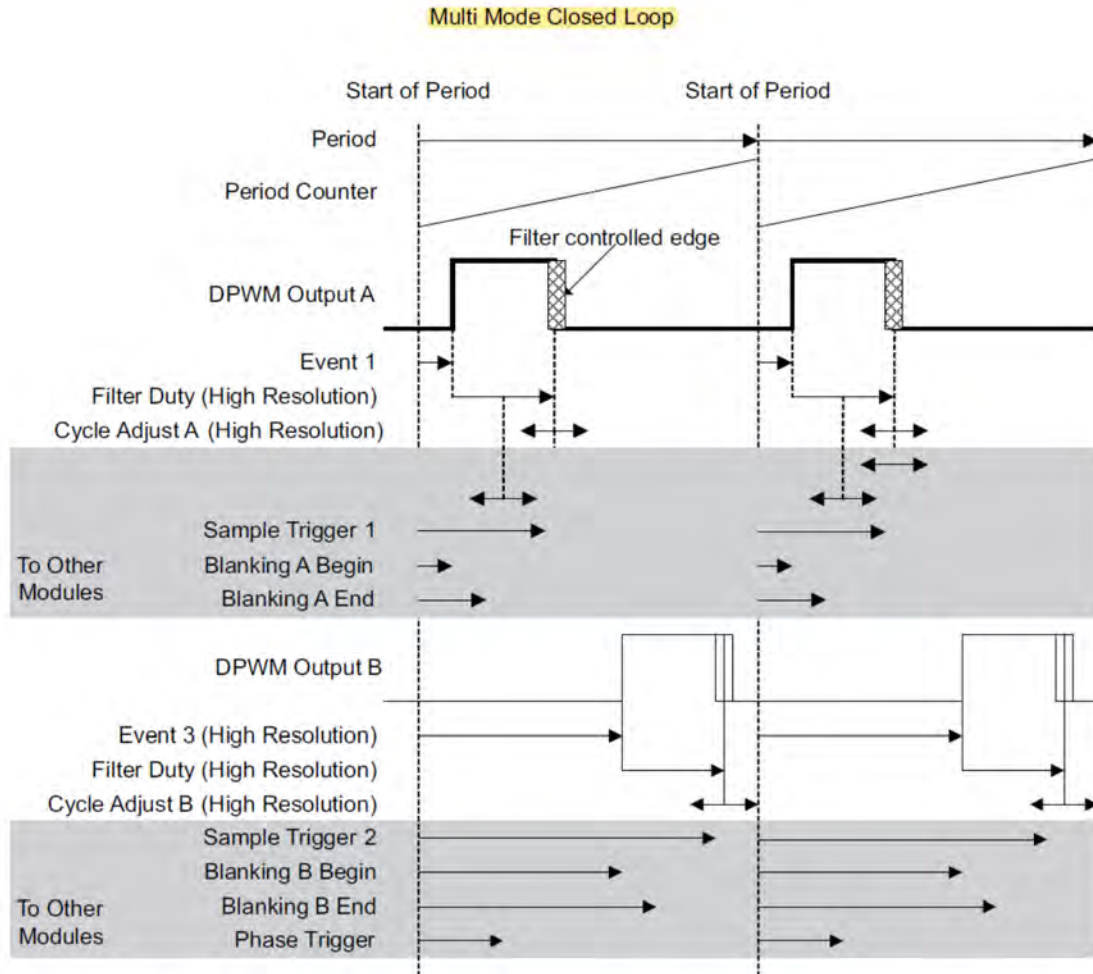
This permits the filter output to be multiplied by a variety of correction factors to match the DPWM Period, to provide for Voltage Feed Forward, or for other purposes. After this, there is another clamp. For resonant mode, the filter can be used to generate both period and duty cycle.

Ex. 1006, 46.

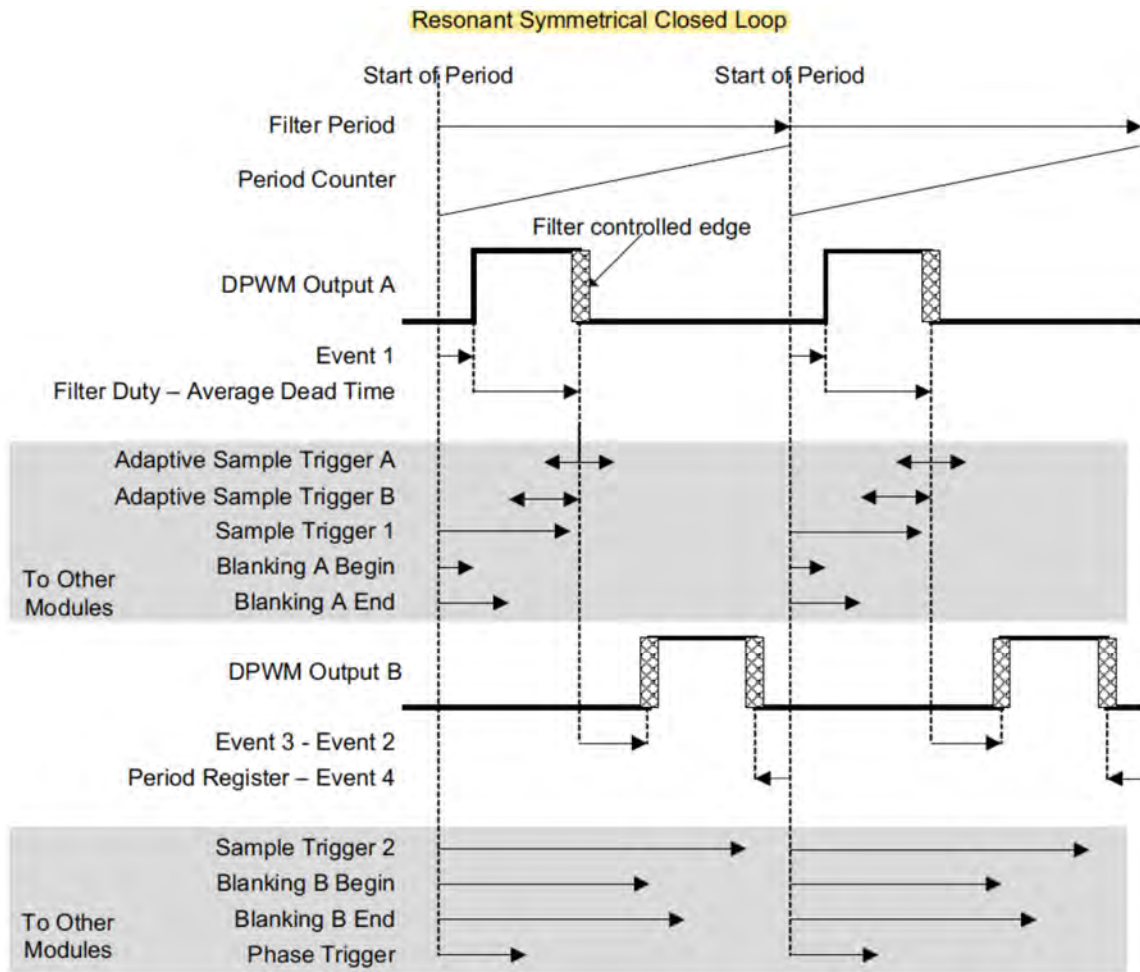
TI UCD3138 also has several figures disclosing closed loop operation.



Id., 32.



Id., 34.



Id., 36. See also, *Id.*, 37, 39.

B. Ground II: Obvious over Shimada in view of AAPA.

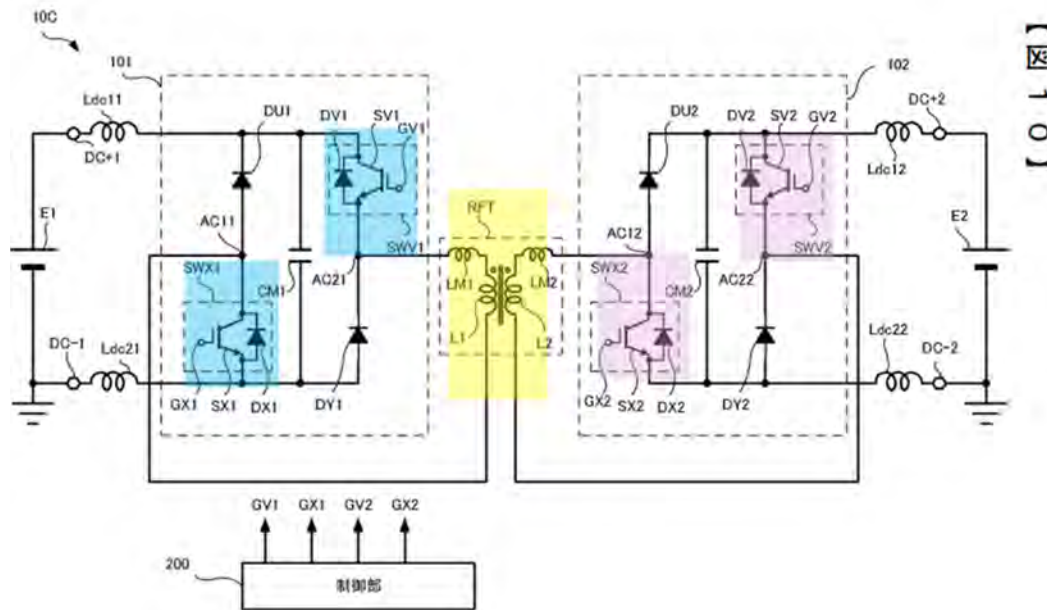
Shimada (Exs. 1007-1008) combined with the AAPA renders obvious claims 1, and 22 of the '481 Patent. A POSITA would have been motivated to combine Shimada with the AAPA for purposes of zero current and zero voltage switching because both are related to resonant converters, and Shimada contemplates zero current and zero voltage switching, which the AAPA explicitly teaches. Ex. 1003, ¶ 107. Thus, a POSITA would have understood and expected that the AAPA's

teachings, which were generally known in the prior art, would apply to Shimada's resonant converter, and would have looked to the AAPA for additional details related to zero current and zero voltage switching. *Id.*

1. Claim 1

a. Limitation 1[a]

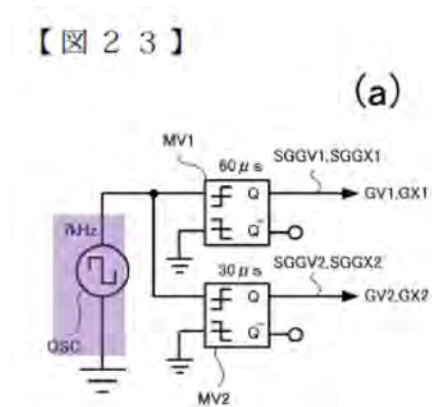
To the extent the preamble is limiting, Shimada teaches it. Shimada teaches a method of synchronously operating a half-bridge power converter, where the converter has at least one primary switch that drives a resonant circuit, at least one secondary switch, and a transformer. Exs. 1007-1008, [0012], Fig. 10. Figure 10 of Shimada (below) shows a half-bridge converter having primary switches SWV1 and SWX1 (blue), a resonant circuit (LLC) on the primary side (with a resonant frequency and period) consisting of inductor L_{dc11} , inductor L_{dc21} , and capacitor C_{M1} , secondary switches SWV2 and SWX2 (pink), and a transformer RFT (yellow).



Exs. 1007-1008, Fig. 10; Ex. 1003, ¶¶ 108-109.

b. Limitation 1[b]

Shimada teaches an oscillator OSC for generating clock signals at an oscillator frequency f_1 . Exs. 1007-1008, [0137] (“Fig. 23(a) shows a control circuit that outputs gate signals SGGV1, SGGX1, SGGV2, and SGGX2 of the DC-DC converter using the one-directional MERS described above. This circuit is equipped with an oscillator OSC [in purple below] and one-shot multivibrators MV1 and MV2. The oscillator OSC outputs clock pulses with a frequency 7kHz (frequency f_1).”).



Exs. 1007-1008, Fig. 23(a).

c. Limitation 1[c]

Shimada teaches that controller 200 generates timing control signals (gate signals) to control the primary and secondary switches. Ex. 1003, ¶ 111, Exs. 1007-1008, [0031] (stating that control unit 200 generates gate signals).

(0031)

Before the start of operation, the control unit 200 outputs all of the gate signals SGGV1, SGGX1, SGGV2, and SGGX2 as off signals and repeats the next cycle C1 on the basis of the pre-stored times d1 and d2 and the frequency f1 in response to a user instruction, for example.

In the cycle C1, the control unit 200 simultaneously switches all of the gate signals SGGV1, SGGX1, SGGV2, and SGGX2 from the off signal to the on signal. Then, time d2 after switching to the on signals, the gate signals SGGV2 and SGGX2 are switched from on signals to off signals, and then after another time (d1-d2) elapses, the gate signals SGGV1 and SGGX1 are switched from the on signals to the off signals.

The control unit 200 repeats this cycle C1 at the frequency f1.

Exs. 1007-1008, [0031]. The converter in Shimada inherently operates at the resonant period and frequency to achieve ZVS and ZCS. Ex. 1003, ¶ 112.

d. Limitation 1[d]

Shimada in combination with the AAPA (hereinafter, “Shimada-AAPA”) renders this limitation obvious. Ex. 1003, ¶¶ 113-115. Shimada teaches zero voltage and zero current switching on the primary switches.

(0127)

As can be seen from FIG. 20A to 20C, when switching the gate signals from the on signal to the off signal, the capacitor voltage of that MERS is almost zero, and when switching the gate signals from the off signal to the on signal, the current flowing in the inductor L_m is almost zero. Therefore, the switching of each switch is at zero voltage or zero current, and soft switching is achieved with both high and low charges per time.

Exs. 1007-1008, [0127].

The AAPA further teaches that zero voltage and zero current switching can be used to turn the primary switches on and off. For example, the AAPA teaches turning on (closing) a primary switch (S1) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32. It also teaches turning off (opening) a primary switch S1 “when the sinusoidal current flow completes half-cycle, and the current I_{pri} returns substantially to zero” and “the voltages across switches S2-120 and S4-140 decline toward zero.” *Id.*, 1:36-43.

e. Limitation 1[e]

Shimada-AAPA renders this limitation obvious. Ex. 1003, ¶¶ 116-120. Shimada teaches zero voltage and zero current switching on the secondary switches.

(0127)

As can be seen from FIG. 20A to 20C, when switching the gate signals from the on signal to the off signal, the capacitor voltage of that MERS is almost zero, and when switching the gate signals from the off signal to the on signal, the current flowing in the inductor L_m is almost zero. Therefore, the switching of each switch is at zero voltage or zero current, and soft switching is achieved with both high and low charges per time.

Exs. 1007-1008, [0127].

The AAPA teaches that zero voltage and zero current switching can be used to turn the secondary switches on and off. For example, the AAPA discloses that “the VTM may include secondary switches turned on and off essentially at times of

zero voltage to rectify power from the transformer. The VTM may include secondary switches on and off essentially at times of zero current to rectify power from the transformer.” Ex. 1009, 9:25-29.⁶ The AAPA also discloses turning on (closing) a secondary switch (S3) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32. The AAPA further discloses that “the voltage across one or more of the switches may be monitored to establish the timing of a zero-voltage switching or zero-current switching event.” *Id.* 1:66-2:3.

f. Limitation 1[f]

Shimada teaches the oscillator frequency f_1 is preset. Exs. 1007-1008, [0137] (“The oscillator OSC outputs clock pulses with the frequency 7kHz (frequency f_1).”).

g. Limitation 1[g]

Shimada teaches that timing of the timing control signals (gate signals) are independent. Ex. 1003, ¶¶ 122-123; Exs. 1007-1008, [0028]-[0029].

⁶ Incorporated by reference within the '481 Patent. Ex. 1001, 1:17-20.

(0028)

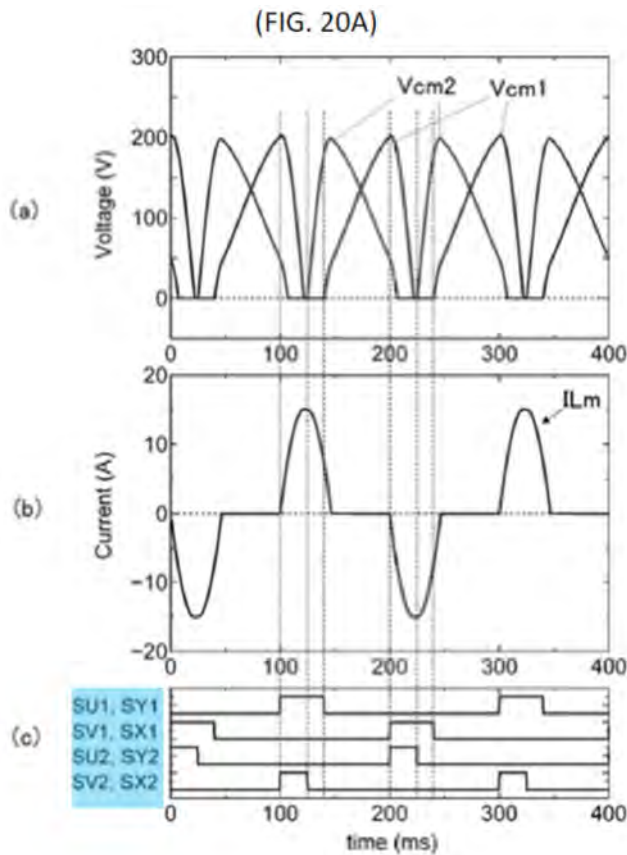
The control unit 200 is configured from a computer provided with, for example, a processor such as a central processing unit (CPU) and a memory device such as a random access memory (RAM) or a read only memory (ROM).

The control unit 200 uses the processor to read and execute, for example, a program stored in advance in the memory device, and by repeating the processing described below, e.g., the cycle described below, supplies the gate signals SGGV1, SGGX1, SGGV2, and SGGX2 to the gates GV1, GX1, GV2, and GX2, respectively.

(0029)

Each gate signal indicates on or off for a semiconductor switch provided with a gate to which the gate signal is supplied. For example, a gate signal that indicates on (on signal) has a voltage high enough to turn on the semiconductor switch (high level voltage), and a gate signal that indicates off (off signal) has a voltage low enough to turn off the semiconductor switch (low level voltage).

Ex. 1008, [0028]-[0029]. Figure 20A also shows independent timing signals (blue) for various events.



Ex. 1008, Fig. 20A.

2. Claim 22

a. Limitation 22[a]

See § VI.B.1.

b. Limitation 22[b]

Shimada teaches this limitation. Ex. 1003, ¶ 125. Shimada states that “Fig. 23(b) shows a control circuit that outputs gate signals SGGU1, SGGV1, SGGX1, SGGYI, SGGU2, SGGV2, SGGX2, AND SGGY2 of the DC/DC converter using the bidirectional MERS described above. The circuit is equipped with one-shot multivibrators MU1 and MU2 in addition to the control section 200 described in FIG. 23(a). . . . The one-shot multivibrator MU1 responds to the rising clock pulse output by the oscillator OSC by switching the off signal to the on signal, holding the on signal for 60 microsecond, and then switching to the off signal. . . . The one-shot multivibrator MU2 responds to the rising clock pulse output by the oscillator OSC, switches the off signal to the on signal, holds the on signal for 30 microseconds, and then switches to the off signal.”). Exs. 1007-1008, [0138].

C. Ground III: Obvious over Chen in view of AAPA

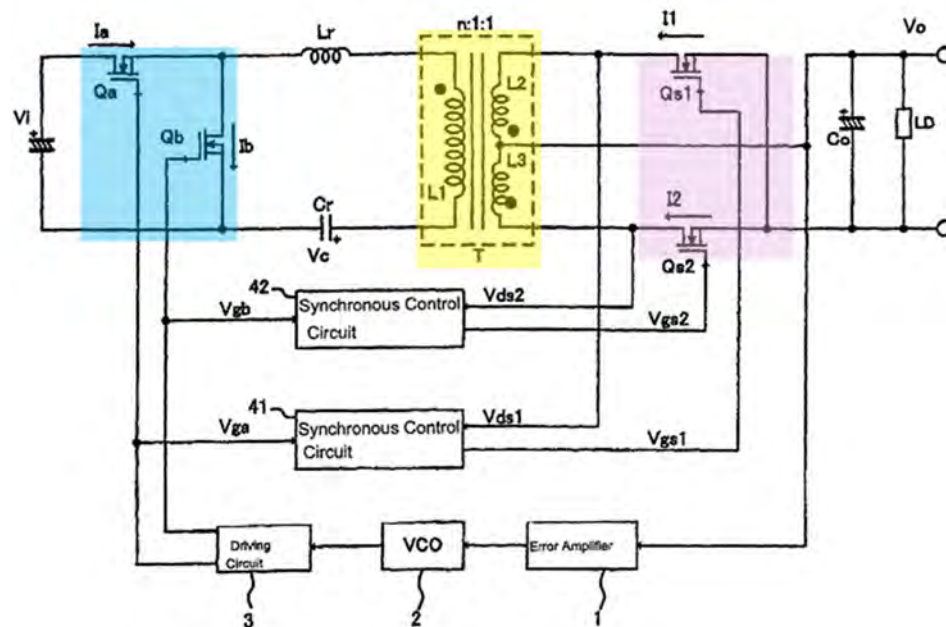
Chen (Ex. 1010) combined with the AAPA renders obvious claims 1, and 22 of the '481 Patent. A POSITA would have been motivated to combine Chen with the AAPA for purposes of zero current and zero voltage switching because both are related to resonant converters, and Chen contemplates zero current and zero voltage switching, which the AAPA explicitly teaches. Ex. 1003, ¶ 127. Thus, a POSITA would have understood and expected that the AAPA's teachings, which were generally known in the prior art, would apply to Chen's resonant converter, and

would have looked to the AAPA for additional details related to zero current and zero voltage switching. *Id.*

1. Claim 1

a. Limitation 1[a]

To the extent the preamble is limiting, Chen teaches it. Chen teaches a method of synchronously operating a half-bridge power converter, where the converter has at least one primary switch that drives a resonant circuit, at least one secondary switch, and a transformer. Ex. 1010, 9:25-28 (“MOSFETs Qa, Qb are main switching elements which switch the current path to the series resonance circuit by switching in alternation on the primary side of the transformer T”); *Id.*, 9:43-47 (“The other end of secondary windings L2 and tertiary windings L3 are connected, via synchronous rectification MOSFETs Qs1 and Qs2 respectively, to the other ends on the ground side of the output capacitor Co and the load LD.”). Figure 1 of Chen (below) shows a half-bridge converter having primary MOSFET switches Qa and Qb (blue), a resonant circuit on the primary side (with a resonant frequency and period) consisting of inductor L_r and capacitor C_r , secondary switches Qs1 and Qs2 (pink), and a transformer T (yellow). Ex. 1003, 128-129.

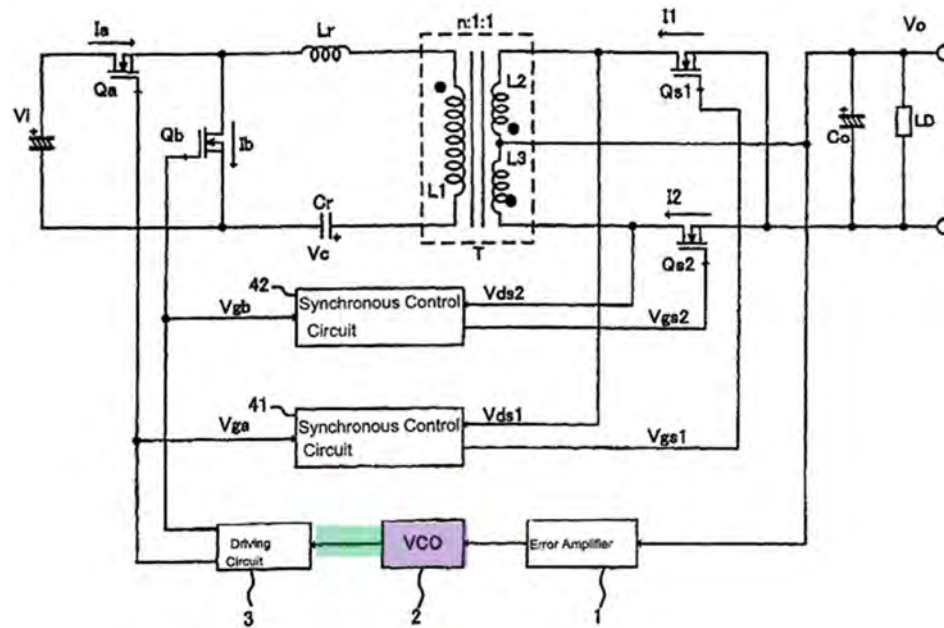


Ex. 1010, Fig. 1.

b. Limitation 1[b]

Chen teaches an oscillator VCO for generating clock signals at an oscillator frequency. Ex. 1003, ¶130. Figure 1 of Chen (below) shows oscillator VCO (purple), which inherently generates clock signals (green) at the oscillator frequency.

Id.



Ex. 1010, Fig. 1.

c. Limitation 1[c]

Chen teaches this limitation. Ex. 1003, ¶ 131. Chen teaches that the Driving Circuit generates timing control signals (gate signals and synchronous driving signals) to control primary switches Qa and Qb and secondary switches Qs1 and Qs2.

The output voltage V_O supplied to the load LD is fed back 55
to the driving circuit 3 of the MOSFETs Qa, Qb via the error
amplifier 1 and a VCO (voltage controlled oscillator circuit)
2. Here, gate signals Vga, Vgb which are turned on and off in
alternation with prescribed timing are generated in the driving
circuit 3, and the currents Ia, Ib of the MOSFETs Qa, Qb are 60
controlled so as to flow in the directions of the arrows with
prescribed timing. The current Ib flows in the direction oppo-
site the arrow depending on operating conditions. Here, the
output frequency of the VCO 2 is changed to be higher when
it is judged from the output of the error amplifier 1 that the 65
output voltage V_O is higher than a preset voltage, or that the
load LD is a light load. Conversely, when it is judged that the

Ex. 1010, 9:58-62; *Id.*, 10:10-14 (“And, synchronous driving signals Vgs1, Vgs2
which control the on periods of the synchronous rectification MOSFETs Qs1, Qs2
are output from these synchronous control circuits 41, 42 respectively.”); *Id.* Fig. 1.
The converter in Chen inherently operates at the resonant period and frequency to
achieve ZCS. Ex. 1003, ¶ 132.

d. Limitation 1[d]

Chen in combination with the AAPA (hereinafter, “Chen-AAPA”) renders
this limitation obvious. Ex. 1003, ¶¶ 133-135. Chen discusses zero current
switching on the secondary switches. Ex. 1010, 5:51-63 (“When the secondary
current Is decreases and becomes zero . . . Then, the comparison signal Vdsc is
inverted, the MOSFET is turned off By this means, the comparison signal Vdsc
is again inverted, the MOSFET is again turned on . . .”).

The AAPA further teaches that zero voltage and zero current switching can be

used to turn the primary switches on and off. For example, the AAPA discloses turning on (closing) a primary switch (S1) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32. It also discloses turning off (opening) a primary switch S1 “when the sinusoidal current flow completes half-cycle, and the current I_{pri} returns substantially to zero” and “the voltages across switches S2-120 and S4-140 decline toward zero.” *Id.*, 1:36-43.

e. Limitation 1[e]

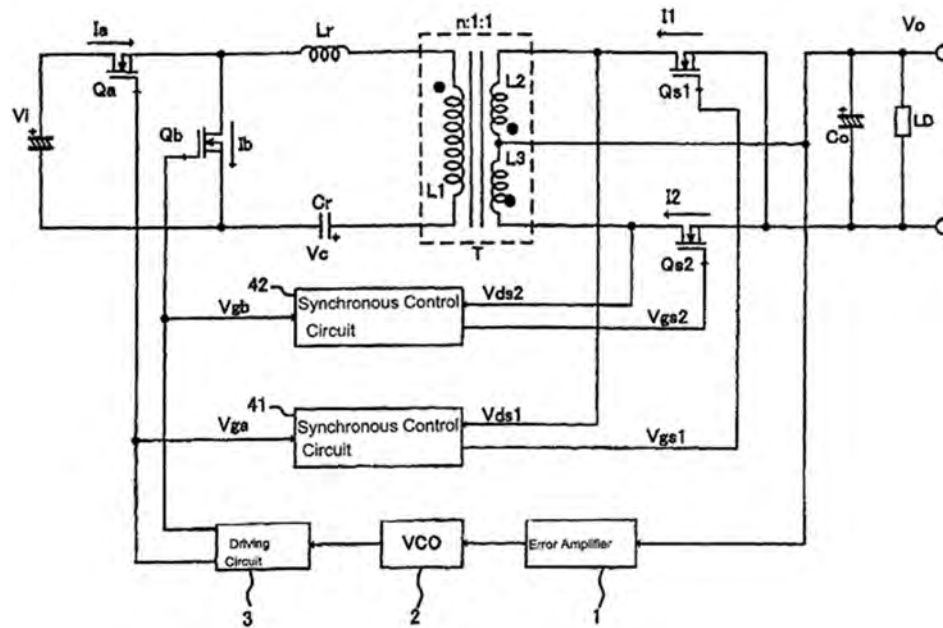
Chen-AAPA renders this limitation obvious. Ex. 1003, ¶¶ 136-139. The AAPA teaches that zero voltage and zero current switching can be used to turn the secondary switches on and off. For example, the AAPA teaches that “the VTM may include secondary switches turned on and off essentially at times of zero voltage to rectify power from the transformer. The VTM may include secondary switches on and off essentially at times of zero current to rectify power from the transformer.” Ex. 1009, 9:25-29. The AAPA also teaches turning on (closing) a secondary switch (S3) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32. The AAPA further teaches that “the voltage across one or more of the switches may be monitored to establish the timing of a zero-voltage switching or zero-current switching event.” *Id.* 1:66-2:3.

f. Limitation 1[f]

Chen teaches the oscillator frequency from VCO has 2 preset frequencies, a higher frequency and a lower frequency, depending on conditions from the error amplifier. Ex. 1003, ¶ 140; Ex. 1010, 9:64-10:5 (“Here, the output frequency of the VCO 2 is changed to be higher when it is judged from the output of the error amplifier 1 that the output voltage V_o is higher than a preset voltage, or that the load LD is a light load. Conversely, when it is judged that the output voltage V_o is lower than the preset voltage, or that the load LD is heavy, the VCO 2 functions to the lower output frequency.”).

g. Limitation 1[g]

Chen teaches that the timing of the timing control signals for the secondary switches (synchronous driving signals V_{gs1} and V_{gs2}) are independent of the timing control signals of the primary switches. Ex. 1010, 10:15-18 (“As explained below, these synchronous driving signals V_{gs1} , V_{gs2} turn on the MOSFETs Q_{s1} , Q_{s2} respectively synchronized to the slower timing among the on timing of the MOSFETs Q_a , Q_b .”). Figure 1 of Chen (below) further shows that synchronous driving signals V_{gs1} and V_{gs2} are output from Synchronous Control Circuits 41 and 42, which makes them independent of gate signals V_{ga} and V_{gb} which are generated directly by the Driving Circuit 3. Ex. 1003, ¶¶ 141-142.



Ex. 1010, Fig. 1.

2. Claim 22

a. Limitation 22[a]

See § VI.C.1.

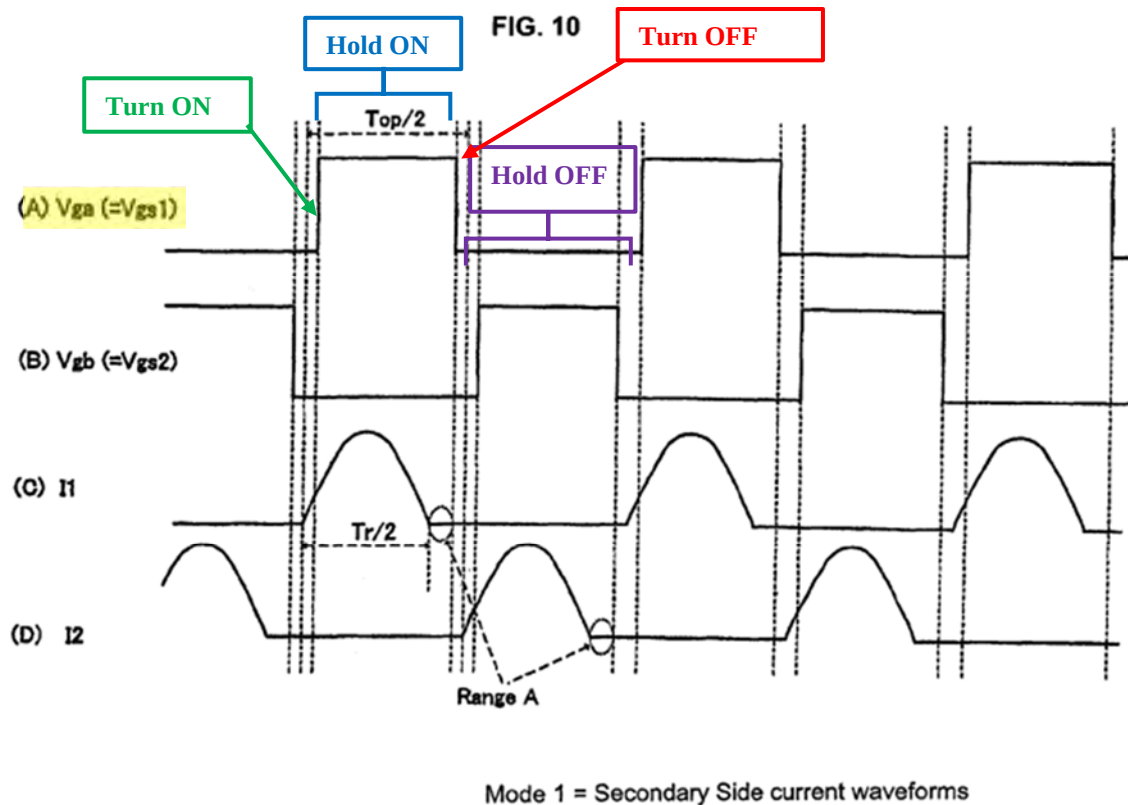
b. Limitation 22[b]

Chen teaches this limitation. Ex. 1003, ¶¶ 144-147. Chen states that “gate signals Vga, Vgb which are turned on and off in alternation with prescribed timing are generated in the Driving Circuit 3, and the currents Ia, Ib of the MOSFETs Qa, Qb are controlled so as to follow in the directions of the arrows with prescribed timing.” Ex. 1010, 9:58-62. Chen also teaches that the Driving Circuit 3 generates synchronous driving signals Vgs1, Vgs2 to control on and off periods of the synchronous rectification MOSFETs Qs1, Qs2.

5 Synchronous control circuits **41** and **42**, to which the gate signals V_{ga} and V_{gb} generated by the driving circuit **3** are respectively input, are provided in the switching power supply device. These synchronous control circuits **41**, **42** further take as inputs the cross-terminal voltage signals V_{ds1} , V_{ds1} across the sources and drains of the synchronous rectification MOSFETs Q_{s1} , Q_{s2} . And, synchronous driving signals V_{gs1} , V_{gs2} which control the on periods of the synchronous rectification MOSFETs Q_{s1} , Q_{s2} are output from these synchronous control circuits **41**, **42** respectively. As explained below, these synchronous driving signals V_{gs1} , V_{gs2} turn on 15 the MOSFETs Q_{s1} , Q_{s2} respectively synchronized to the slower timing among the on timing of the MOSFETs Q_a , Q_b , or the conduction timing of the internal diodes D_s (see FIG. 2) detected from the cross-terminal voltage signals V_{ds1} , V_{ds2} 20 of the MOSFETs Q_{s1} , Q_{s2} . Hence in this switching power

Id., 10:4-16.

Chen further discloses that “in the first operating mode (Mode 1), the synchronous driving signal V_{gs} turns off the MOSFET Q_s in synchronization with the earlier timing among the turn-off timing of the gate signal V_{gp} . . . Further, in the second and fifth operating modes (Modes 2 and 5), the synchronous driving signal V_{gs} turns on the MOSFET Q_s in synchronization with the later timing among the timing with which the maximum on-width signal T_{mot} indicates the on state” *Id.*, 16:5-23. The timing waveform for V_{gs} in Figure 10 of Chen (below) shows that in addition to turning the MOSFET switches on (green) and off (red), they can also hold the MOSFETs on (blue) and hold the MOSFETs off (purple). Ex. 1003, ¶¶ 146-147.



Ex. 1010, Fig. 10.

D. Ground IV: Obvious over Pan in view of TI UCD3138 (or, in the alternative, TI UCD3040) and AAPA

Pan (Ex. 1011) combined with TI UCD3138 (Ex. 1006) (or, alternatively, TI UCD3040 (Ex. 1018))⁷ and further combined with the AAPA renders obvious claims 1, 22, and 31-35 of the '481 Patent. A POSITA would have been motivated to combine Pan with TI UCD3138 or TI UCD3040 because Pan discloses a digital

⁷ Petitioner presents TI UCD3040 as an alternative to TI UCD3138, in the event that Patent Owner argues and the Board finds that the '481 Patent is entitled to a priority date earlier than the March 14, 2013 filing date.

controller that includes a control unit, a digital PWM (DPWM), and clock management. Ex. 1011, 716, Fig. 11. TI UCD3138 and TI UCD3040 are both digital controllers that have all of the features of the digital controller in Pan, including DPWM. TI UCD3138 states that its “Topology support has been optimized for . . . LLC half bridge and full bridge” converters. Ex. 1006, 7. TI UCD3040 states that it supports “half-bridge, phase-shifted full bridge, active clamp, and resonant LLC” converters. Ex. 1018, 2. Pan discloses a series resonant converter that can be either half bridge or full bridge. Ex. 1011, 712 (“Series resonant DC/DC converters with constant switching frequency control are utilized. The main stage on the primary side of the transformer could be either half bridge or full bridge with L-C series resonant tank.”) This presents a POSITA with further motivation to combine. Ex. 1003, ¶¶ 149-150.

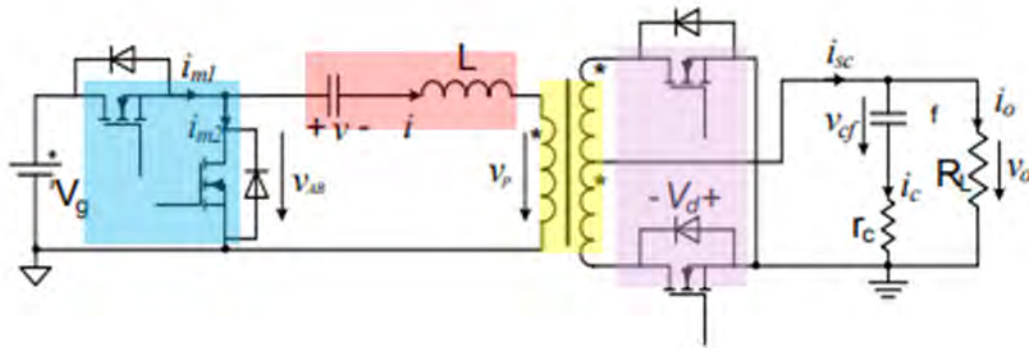
A POSITA would also have been motivated to combine Pan with the AAPA for purposes of zero current and zero voltage switching because both are related to resonant converters, and Pan contemplates zero current and zero voltage switching, which the AAPA explicitly teaches. Ex. 1003, ¶ 151. A POSITA would therefore have understood and expected that the AAPA’s teachings, which were generally known in the prior art, would apply to Pan’s resonant converter, and would have looked to the AAPA for additional details related to zero current and zero voltage switching. *Id.* TI UCD3138 also relates to resonant converters and contemplates

zero current and zero voltage switching by referencing “LLC and phase shifted full bridge mode switching.” Ex. 1006, 7. Similarly, TI UCD3040 discusses resonant LLC converters and contemplates zero current and zero voltage switching. Ex. 1018, 2; Ex. 1003, ¶ 151.

1. Claim 1

a. Limitation 1[a]

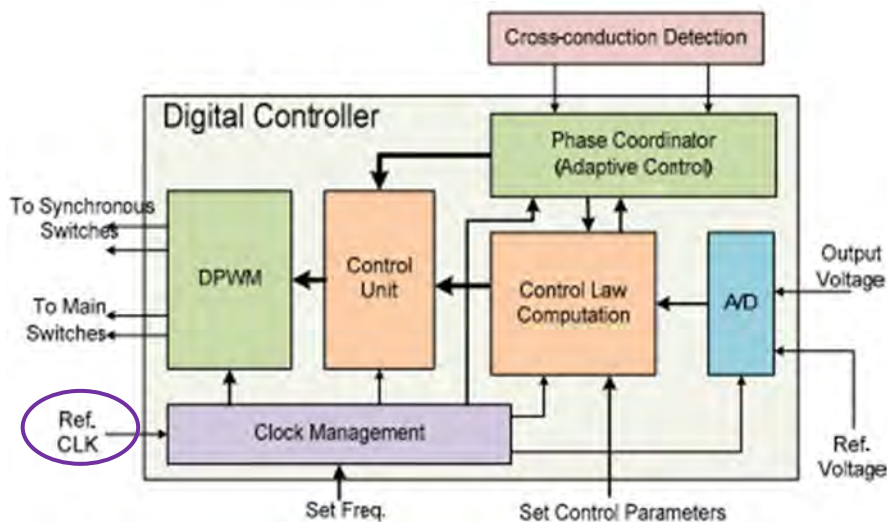
To the extent the preamble is limiting, Pan teaches it. Ex. 1003, ¶¶ 152-153. Pan teaches a method of synchronously operating a half-bridge power converter, where the converter has at least one primary switch that drives a resonant circuit, at least one secondary switch, and a transformer. Ex. 1011, 712 (“The main switches (M_1 & M_2) operate in complementary mode against input voltage variations. The rectifier switches (S_1 & S_2) operate in PWM control mode against load variations.”); *Id.* (“Series resonant DC/DC converters with constant switching frequency control are utilized. The main stage on the primary side of the transformer could be either half bridge or full bridge with L-C series resonant tank.”). Figure 1 of Pan (below) shows a half-bridge converter having primary MOSFET switches M_1 & M_2 (blue), a resonant circuit on the primary side (with a resonant frequency and period) consisting of inductor L and a capacitor (red), secondary MOSFET switches S_1 & S_2 (in pink), and a transformer (yellow).



Ex. 1011, Figure 1.

b. Limitation 1[b]

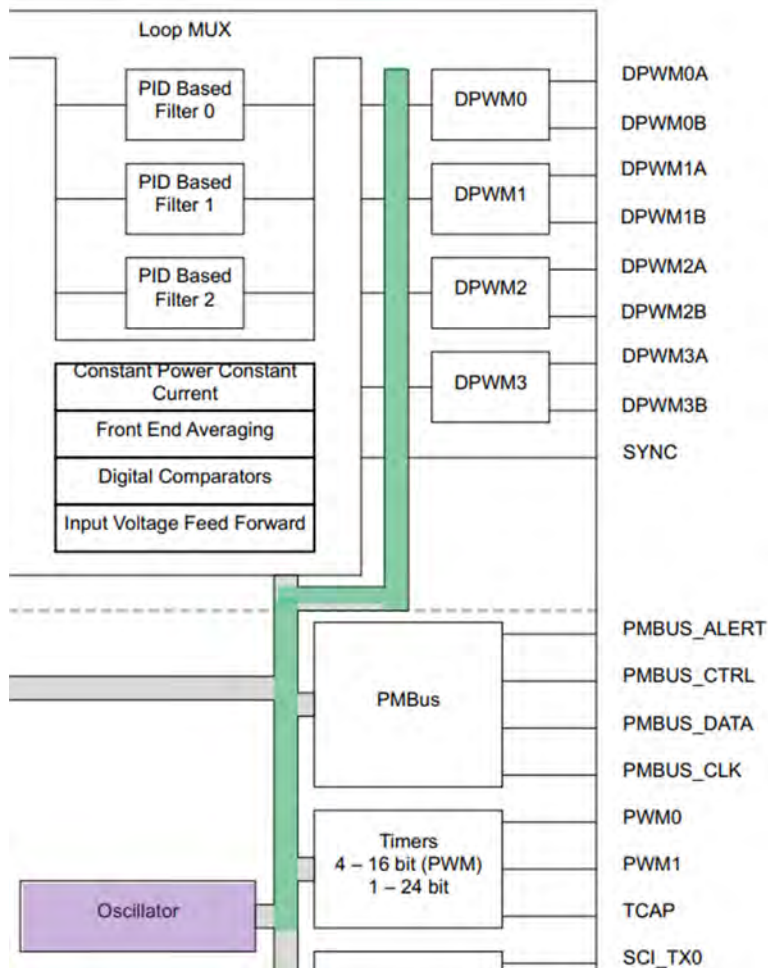
Pan in combination with the TI UCD3138 (hereinafter, “Pan-TI UCD3138”) (or, alternatively, Pan in combination with TI UCD3040, “Pan-TI UCD3040”) renders this limitation obvious. Ex. 1003, ¶¶ 154-157. Figure 11 of Pan (below) teaches an oscillator (Ref. CLK) for generating clock signals at an oscillator frequency.



Ex. 1011, Figure 11.

TI UCD3138 also discloses an oscillator with an oscillator frequency that

generates clock signals. Ex. 1006, 9 (Fig. 2.4), 17. Figure 2.4 of TI UCD3138 (below) shows an Oscillator (purple) that generates several clock signals (green).



Ex. 1006, 9. The oscillator in TI UCD3138 has an internal oscillator frequency $f_{(PCLK)}$, having a typical frequency of 250 MHz. *Id.*, 17. TI UCD3138 also teaches that its oscillator generates clock signals.

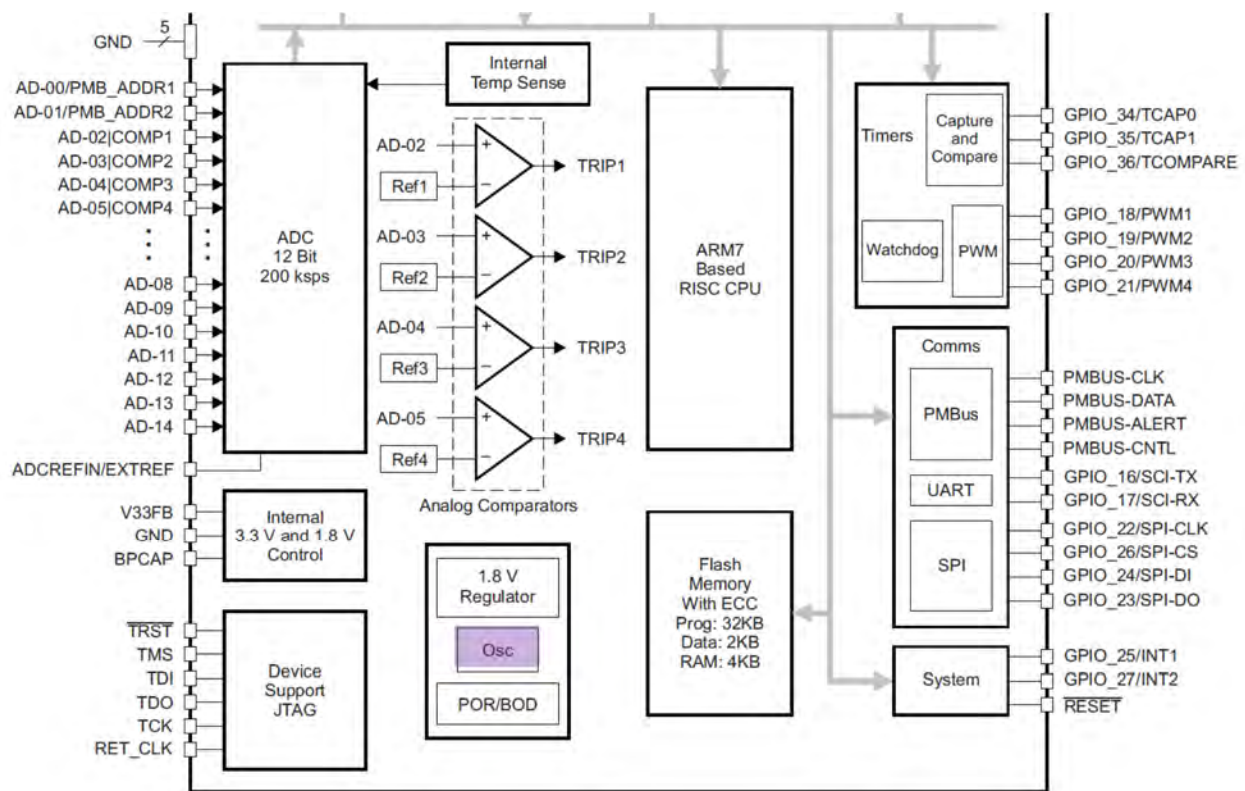
4.4.1.4 High Resolution DPWM

Unlike conventional PWM controllers where the frequency of the clock dictates the maximum resolution of PWM edges, the UCD3138 DPWM can generate waveforms with resolutions as small as 250 ps. This is 16 times the resolution of the clock driving the DPWM module.

This is achieved by providing the DPWM mechanism with 16 phase shifted clock signals of 250 MHz each. The high resolution section of DPWM can be enabled or disabled, also the resolution can be defined in several steps between 4ns to 250ps. This is done by setting the values of PWM_HR_MULTI_OUT_EN, HIRES_SCALE and ALL_PHASE_CLK_ENA inside the DPWM Control Register 1. See the Power Peripherals programmer's manual for details.

Id., 30.

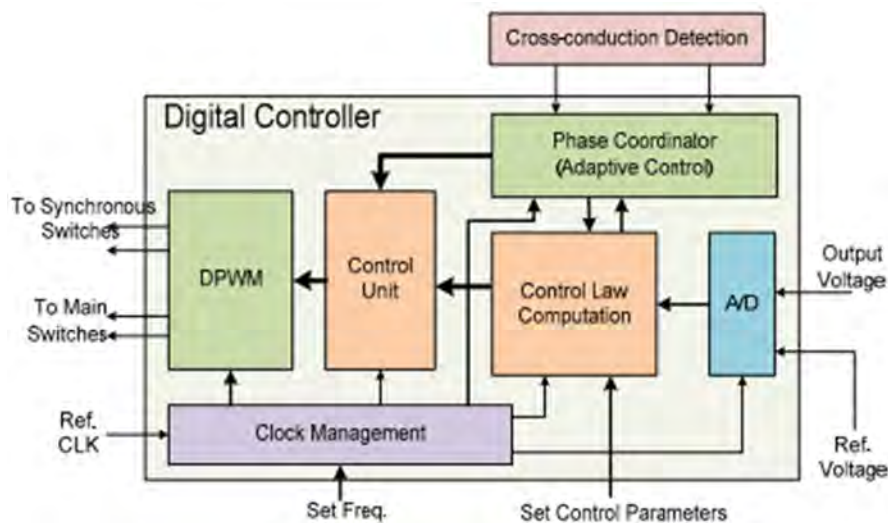
TI UCD3040 also discloses an oscillator with an oscillator frequency that generates clock signals. Ex. 1018, 4, 18. The figure below shows an oscillator OSC (purple).



Ex. 1018, 4. The oscillator in TI UCD3040 has an internal oscillator frequency $f_{(PCLK)}$ of 250 MHz. *Id.*, 18.

c. Limitation 1[c]

Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶¶ 158-160. Figure 11 of Pan (below) shows use of timing control signals (DPWM) to control both the primary switches (Main Switches) and the secondary switches (Synchronous Switches).



Ex. 1011, Figure 11.

TI UCD3138 and TI UCD3040 both teach that each DPWM can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31. The converter in Pan inherently operates at the resonant period and frequency to achieve ZVS and ZCS. Ex. 1003, ¶ 160.

d. Limitation 1[d]

Pan in combination with the AAPA (hereinafter, “Pan-AAPA”) renders this limitation obvious. Ex. 1003, ¶¶ 161-163. Pan discusses zero voltage switching on

the primary switches. Ex. 1011, 712 (“At t_3 , M_2 is turned on to achieve zero voltage switching (ZVS)”); *Id.*, 713 (“At t_8 , M_1 is turned on to achieve zero voltage switching (ZVS)”).

The AAPA further teaches that zero voltage and zero current switching can be used to turn the primary switches on and off. For example, the AAPA teaches turning on (closing) a primary switch (S1) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32. It also teaches turning off (opening) a primary switch S1 “when the sinusoidal current flow completes half-cycle, and the current I_{pri} returns substantially to zero” and “the voltages across switches S2-120 and S4-140 decline toward zero.” *Id.*, 1:36-43.

e. Limitation 1[e]

Pan-AAPA renders this limitation obvious. Ex. 1003, ¶¶ 164-168. Pan discusses the switching of the secondary switches when the resonant current is near zero. Ex. 1011, 713 (“At t_5 , the resonant current i is going across zero. Current through the body diode of S_2 is diminished to zero.”); *Id.* (“At t_0 , the resonant current i goes across zero. Current through the body diode of S_1 is diminished to zero.”).

The AAPA also teaches that zero voltage and zero current switching can be used to turn the secondary switches on and off. For example, the AAPA teaches that “the VTM may include secondary switches turned on and off essentially at times of

zero voltage to rectify power from the transformer. The VTM may include secondary switches on and off essentially at times of zero current to rectify power from the transformer.” Ex. 1009, 9:25-29. The AAPA also teaches turning on (closing) a secondary switch (S3) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32. The AAPA further teaches that “the voltage across one or more of the switches may be monitored to establish the timing of a zero-voltage switching or zero-current switching event.” *Id.* 1:66-2:3.

f. Limitation 1[f]

Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶¶ 169-171. Figure 11 of Pan shows that the frequency of the oscillator (Ref. CLK) can be preset to a set frequency. Ex. 1011, Figure 11. In addition, the oscillator in TI UCD3138 has an internal oscillator frequency $f_{(PCLK)}$ that is preset, having a typical frequency of 250 MHz. Ex. 1006, 17. Similarly, the oscillator in TI UCD3040 has a preset oscillator frequency $f_{(PCLK)}$ of 250 MHz. Ex. 1018, 18.

g. Limitation 1[g]

Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶¶ 172-174. TI UCD3138 and TI UCD3040 each disclose that timing of the timing control signals are independent.

4.4.1.2 DPWM Module

The DPWM module represents one complete PWM channel with 2 independent outputs, A and B. Multiple DPWM modules within the UCD3138 system can be configured to support all key power topologies. DPWM modules can be used as independent PWM outputs, each controlling one power supply output voltage rail. It can also be used as a synchronized PWM—with user selectable phase shift between the PWM channels to control power supply outputs with multiphase or interleaved PWM configurations.

Ex. 1006, 27.

DPWM Module

Programmers' Reference Manual: UCD30xx Fusion Digital Power Peripherals Programmer's Manual

The DPWM module represents one complete DPWM channel with two independent outputs, A and B. Multiple DPWM modules within the UCD30xx system can be configured to support all key power topologies. DPWM modules can be used as independent DPWM outputs, each controlling one power-supply output-voltage rail. A DPWM module can also be used as a synchronized DPWM, with user-selectable phase shift between the DPWM channels, in order to control power-supply outputs with multiphase or interleaved DPWM configurations.

Ex. 1018, 30.

TI UCD3138 and TI UCD3040 further disclose that the timing of the timing control signals for various events are independent of each other, by indicating that each DPWM can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28-29.

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

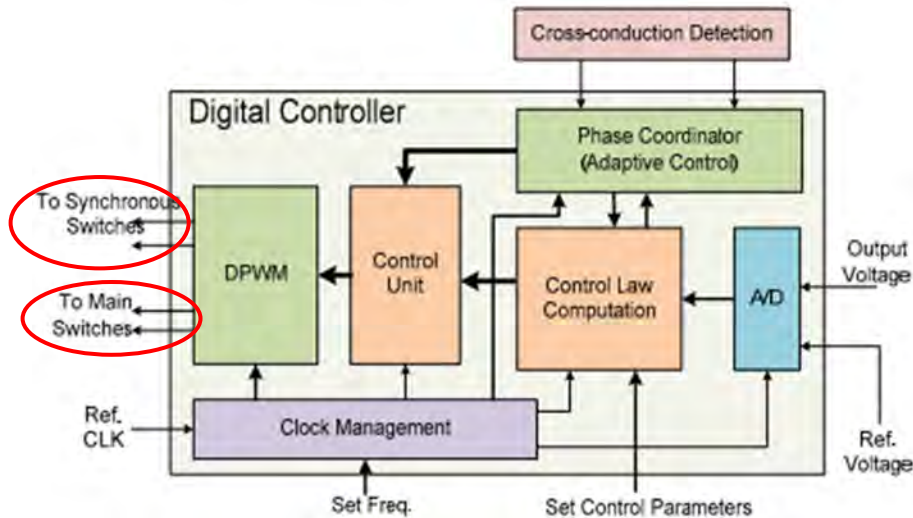
2. Claim 22

a. Limitation 22[a]

See §V1.D.1.

b. Limitation 22[b]

Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶¶ 176-177. Figure 11 of Pan (below) teaches use of a gate drive circuit (Control Unit) to generate timing control signals (DPWM) to control the primary (Main) and secondary (Synchronous) switches.



Ex. 1011, Figure 11.

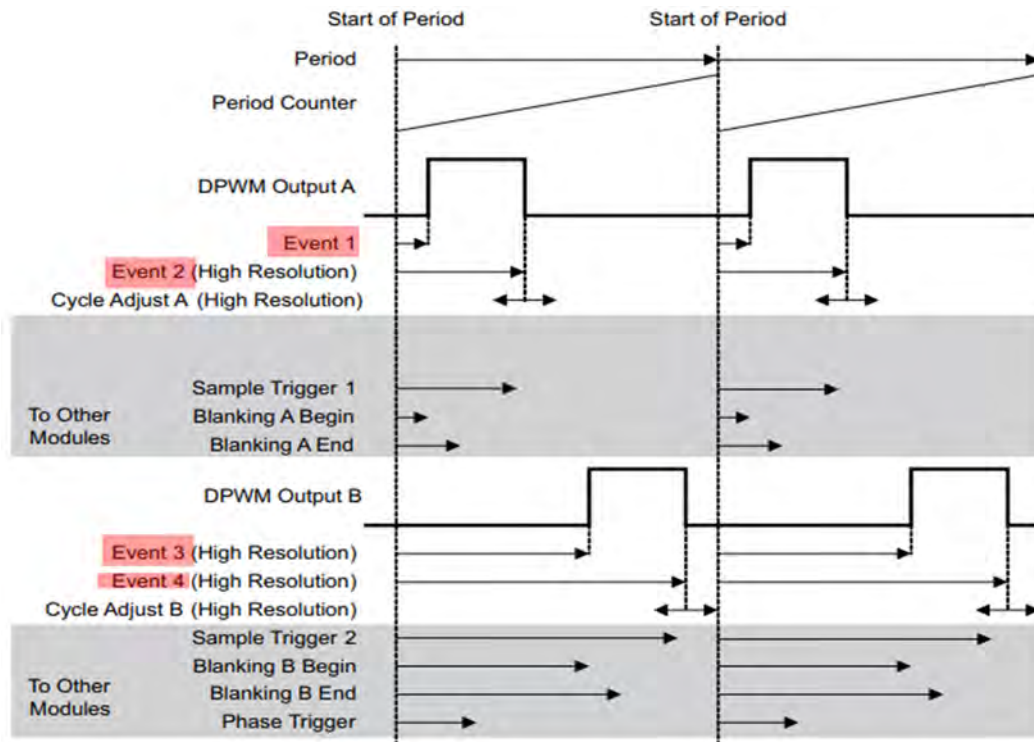
TI UCD3138 and TI UCD3040 both disclose that each timing control signal DPWM can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.



Ex. 1006, 30 (showing timing signals for different events).

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

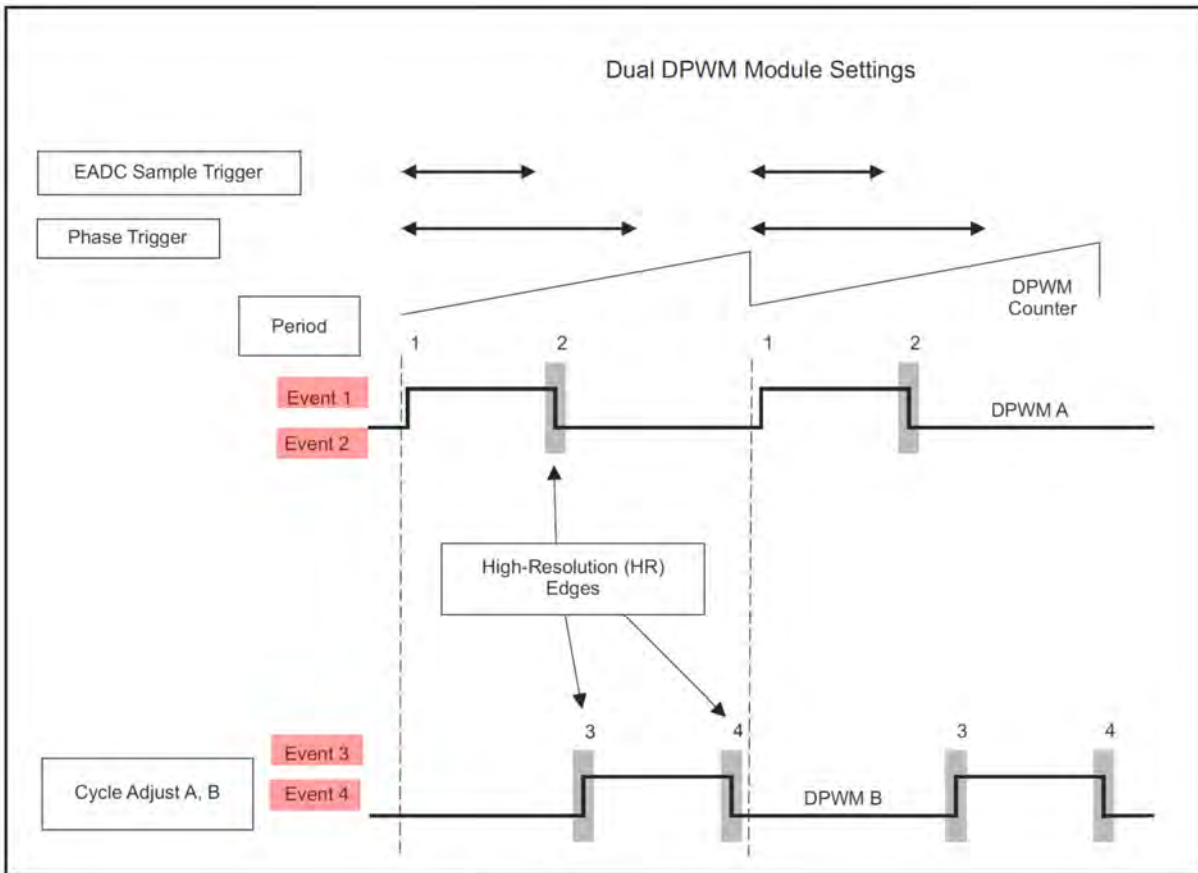


Figure 7. DPWM Events

Id., 32 (showing timing signals for different events).

3. Claim 31

a. Limitation 31[a]

See § V1.D.1.

b. Limitation 31[b]

Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶ 179. TI UCD3138 and TIUCD3040 both teach that the DPWM's control of the various timing events involves counting the clock signals from the oscillator.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

c. Limitation 31[c]

Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶ 180. TI UCD3138 and TI UCD3040 both teach that the DPWM sets a count threshold for each event.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

d. Limitation 31[d]

Pan-TI UCD 3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶ 181. TI UCD3138 and TI UCD3040 both teach that the DPWM generates timing control signals for each event when the counting matches

the count threshold.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28. *See also id.*, 32, 4.5 DPWM Modes of Operation (“... The DPWM logic causes transitions in many digital signals when the period counter hits the target value for that signal.”).

DPWM Events

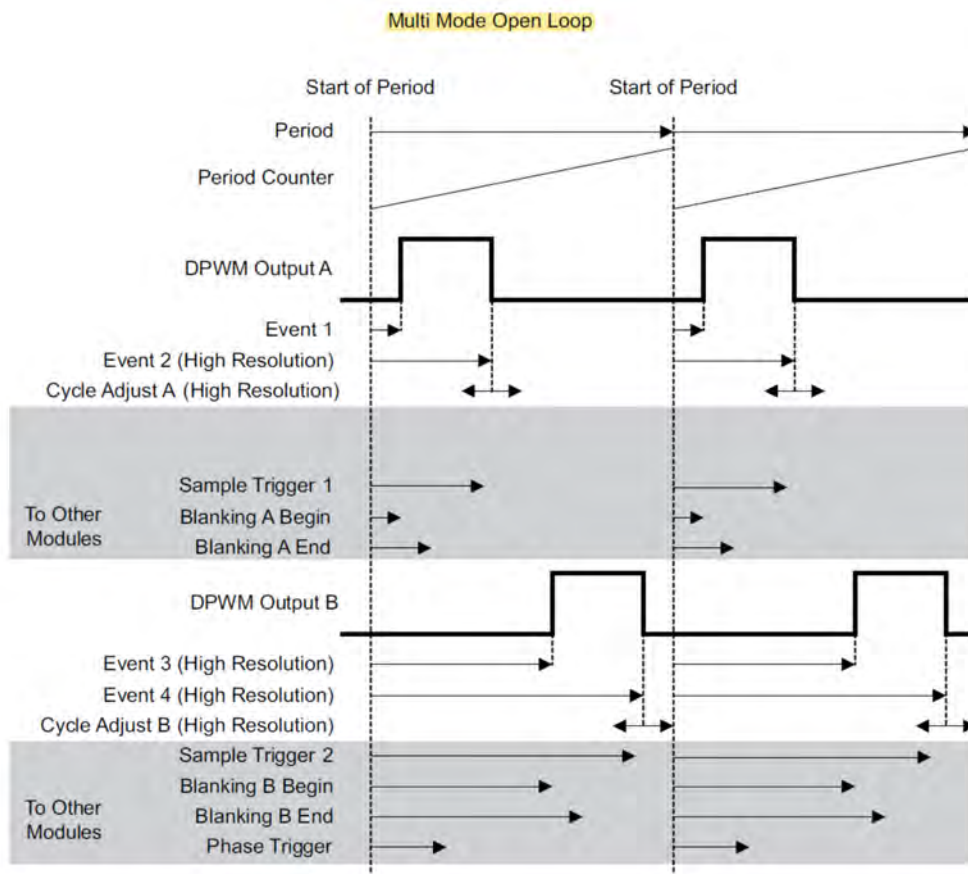
Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

4. Claim 32

Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶¶ 182-183; see § VI.D.3. TI UCD3138 shows a Multi-Mode Open Loop figure (below), stating that the DPWM is controlled entirely by its own registers and not by the filter output.



Events which change with DPWM mode:

DPWMA Rising Edge = Event 1
 DPWMA Falling Edge = Event 2 + Cycle Adjust A
 DPWM B Rising Edge = Event 3
 DPWM B Falling Edge = Event 4 + Cycle Adjust B
 Phase Trigger = Phase Trigger Register value

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

The drawing above is for multi-mode, open loop. Open loop means that the DPWM is controlled entirely by its own registers, not by the filter output. In other words, the power supply control loop is not closed.

Ex. 1006, 29. TI UCD3140 also discloses an open-loop mode (below).

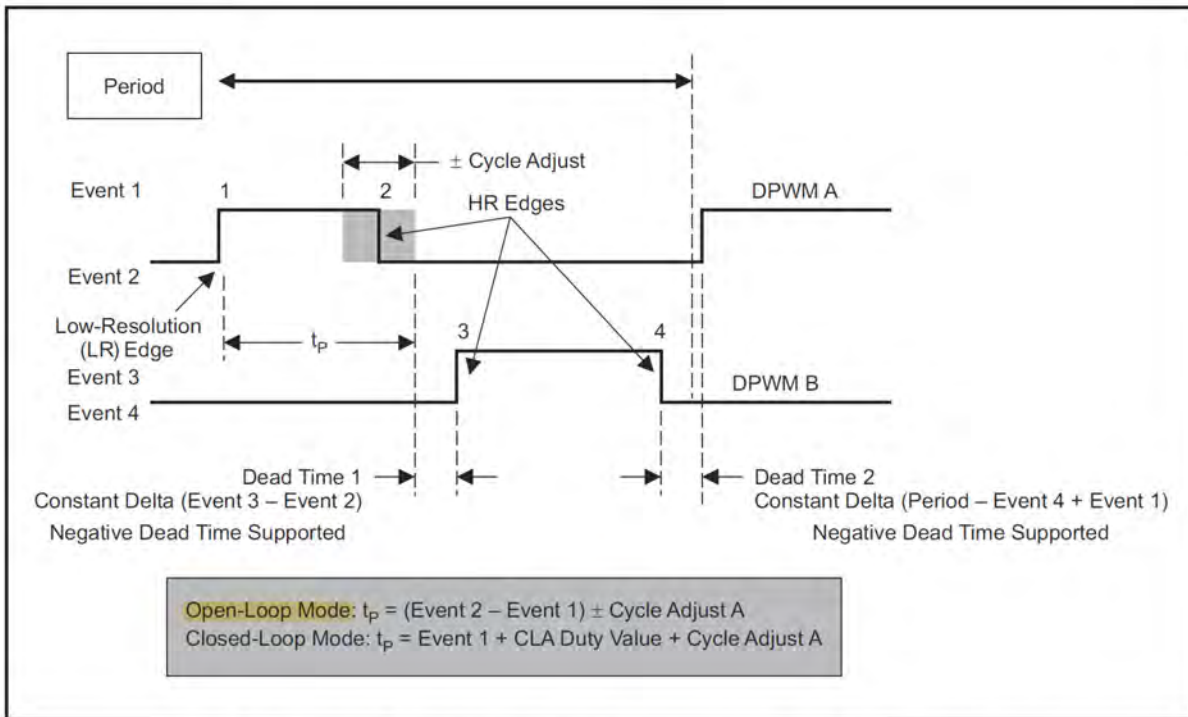


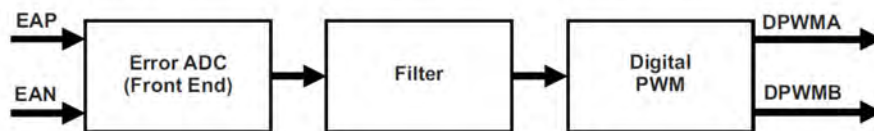
Figure 8. Normal Mode (Duty-Ratio Control) – DPWM Timing Diagram

Ex. 1018, 34.

5. Claim 33

Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶¶ 184-185; *see* § VI.D.3 above. TI UCD3138 teaches this limitation of adjusting timing events with feedback provided by the Filter.

These can be connected in many different combinations, with multiple filters and DPWMs. They are capable of supporting functions like input voltage feed forward, current mode control, and constant current/constant power, etc.. The simplest configuration is shown in the following figure:



Ex. 1006, 26. TI UCD3040 also teaches this limitation of adjusting timing events with feedback provided by the compensator.

PERIPHERALS

Fusion Digital Power Peripherals

At the core of the UCD30xx controller are its four Fusion Digital Power peripherals (FDPP). Each FDPP can be configured to drive from one to eight DPWM outputs. Each FDPP consists of a differential input error ADC (EADC), a hardware-accelerated digital three-pole/three-zero (3p/3z) compensator, and a digital PWM module.

Ex. 1018, 25.

6. Claim 34

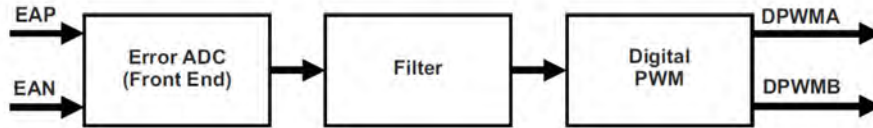
Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶ 186; *see* § VI.D.4. TI UCD3138 and TI UCD3040 both teach use of firmware data for certain measurements, and firmware is set during the manufacturing process. Ex. 1006, 22, 4.2 Memory (“Within the UCD31xx architecture, there is a 1024x32-bit Boot ROM that contains the initial firmware startup routines for PMBUS communication and non-volatile (FLASH) memory download. This boot ROM is executed after power-up-reset checks if there is a valid FLASH program written.”); Ex. 1018, 20, Memory (same quoted language but for UCD30xx).

7. Claim 35

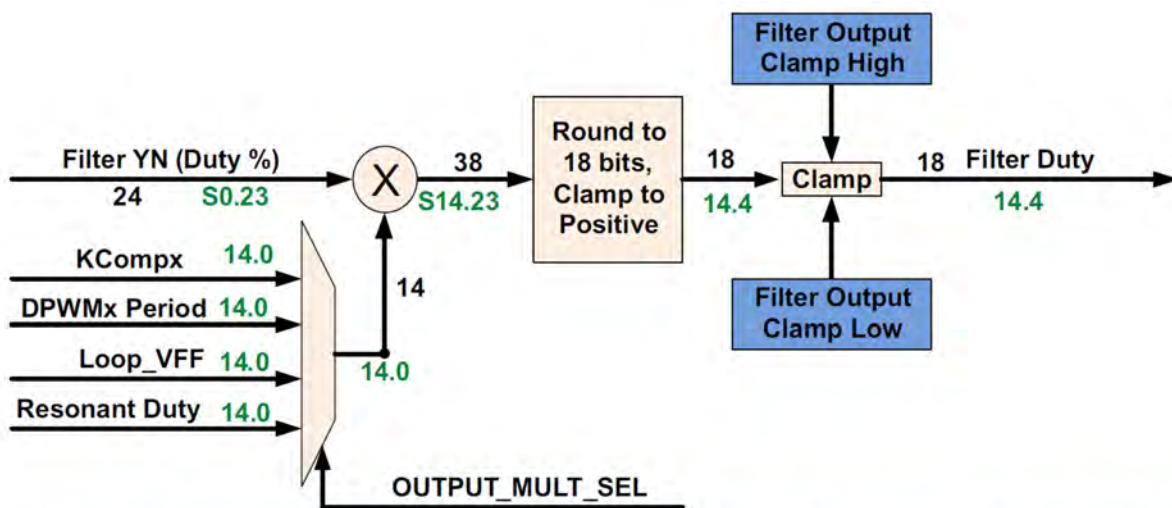
Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶¶ 187-188; *see* § VI.D.4. Pan Figure 11 teaches this closed-loop feedback during operation. Ex. 1003, ¶ 187. TI UCD3138 also teaches that the measurements and adjustments are performed during operation of the device as part

of a closed-loop feedback system, where the Filter provides the feedback.

These can be connected in many different combinations, with multiple filters and DPWMs. They are capable of supporting functions like input voltage feed forward, current mode control, and constant current/constant power, etc.. The simplest configuration is shown in the following figure:



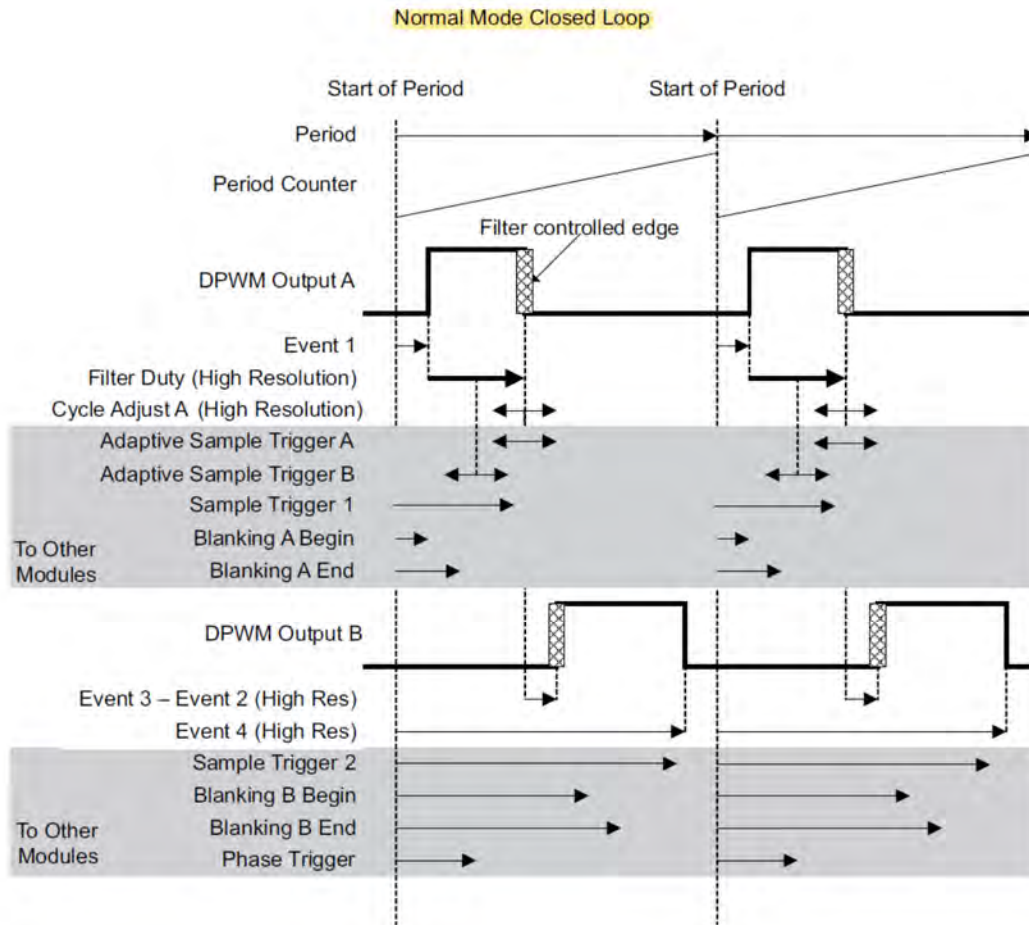
Ex. 1006, 26.



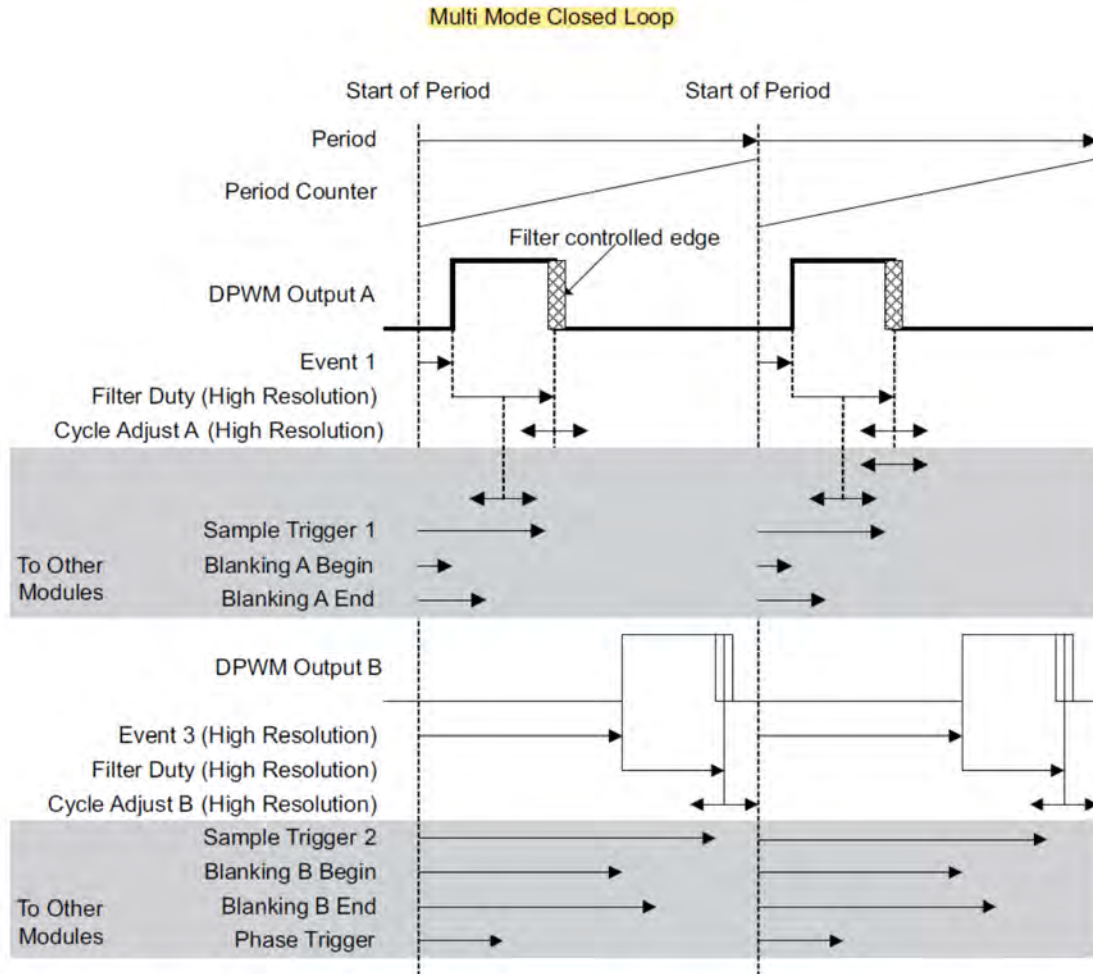
This permits the filter output to be multiplied by a variety of correction factors to match the DPWM Period, to provide for Voltage Feed Forward, or for other purposes. After this, there is another clamp. For resonant mode, the filter can be used to generate both period and duty cycle.

Ex. 1006, 46.

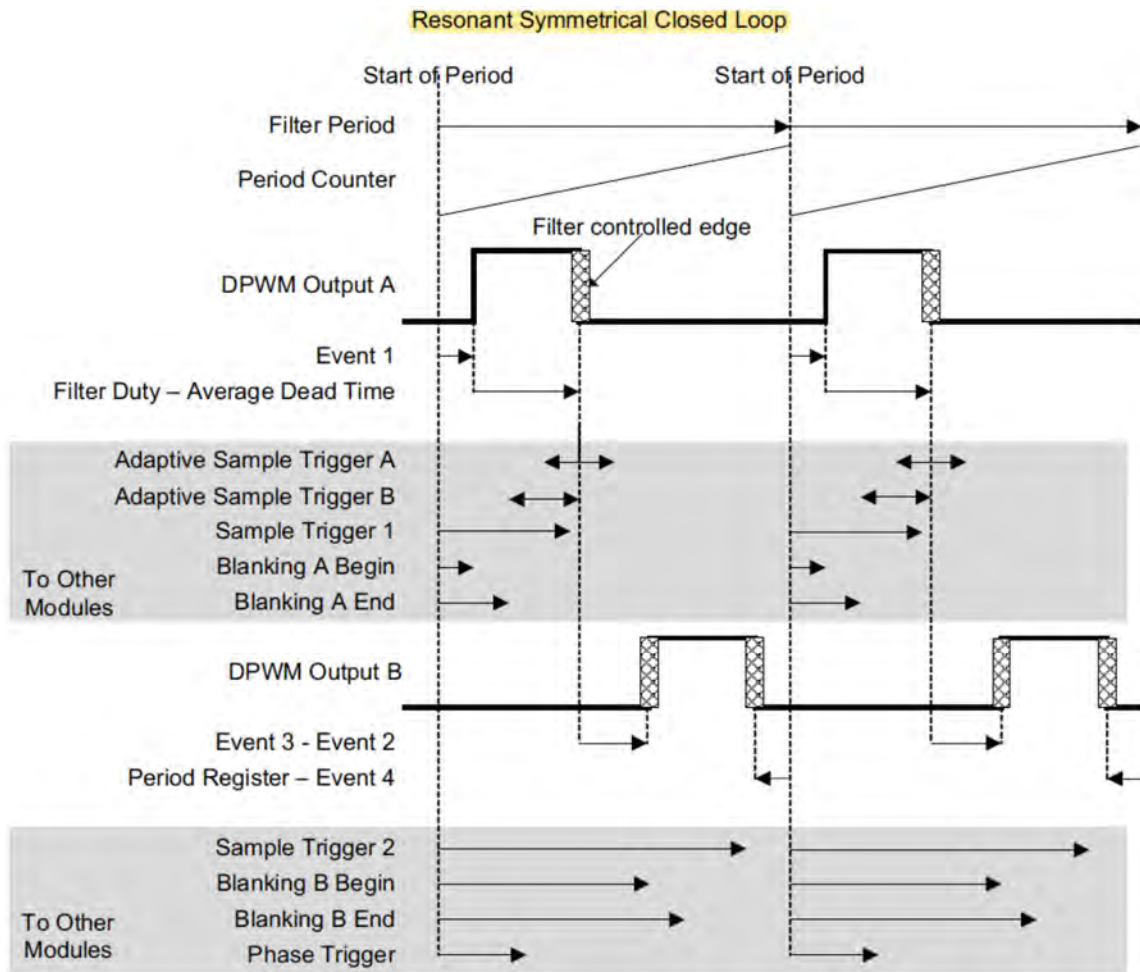
TI UCD3138 also has several figures disclosing closed loop operation.



Id., 32.



Id., 34.



Id., 36. See also, *Id.*, 37, 39.

Similarly, TI UCD3040 also teaches that the measurements and adjustments are performed during operation of the device as part of a closed-loop feedback system, with the compensator providing the feedback.

PERIPHERALS

Fusion Digital Power Peripherals

At the core of the UCD30xx controller are its four Fusion Digital Power peripherals (FDPP). Each FDPP can be configured to drive from one to eight DPWM outputs. Each FDPP consists of a differential input error ADC (EADC), a hardware-accelerated digital three-pole/three-zero (3p/3z) compensator, and a digital PWM module.

Ex. 1018, 25. TI UCD3140 also has several figures disclosing closed loop operation.

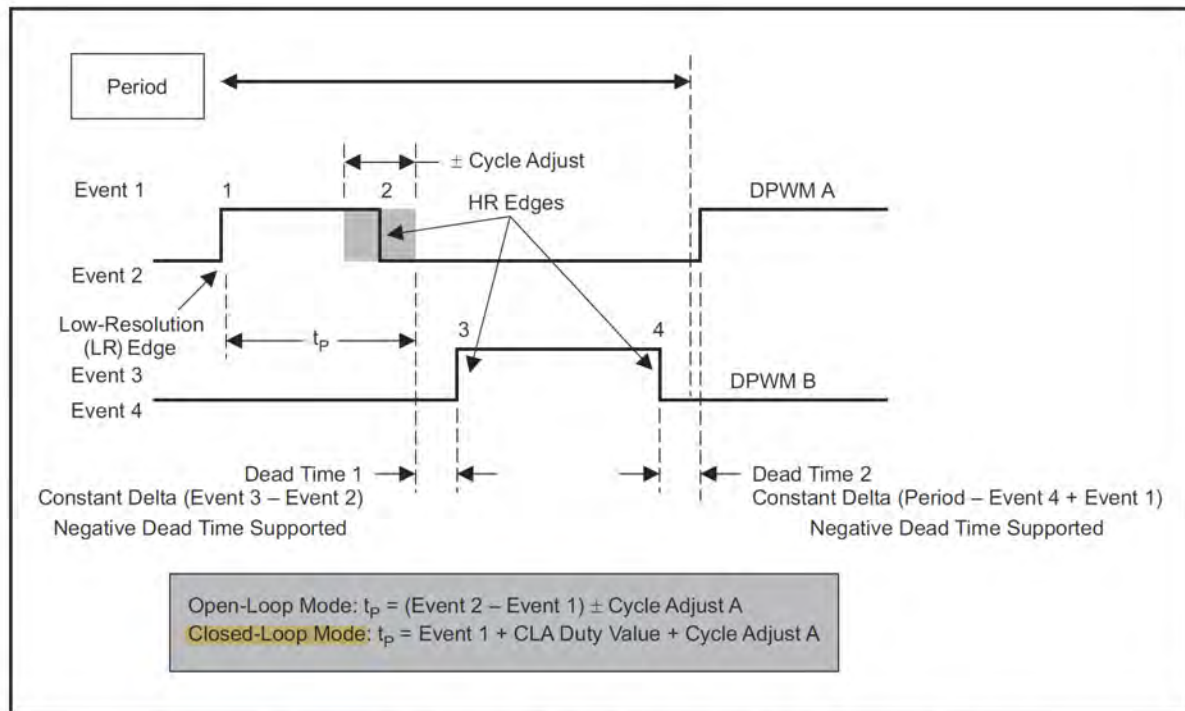


Figure 8. Normal Mode (Duty-Ratio Control) – DPWM Timing Diagram

Ex. 1018, 34.

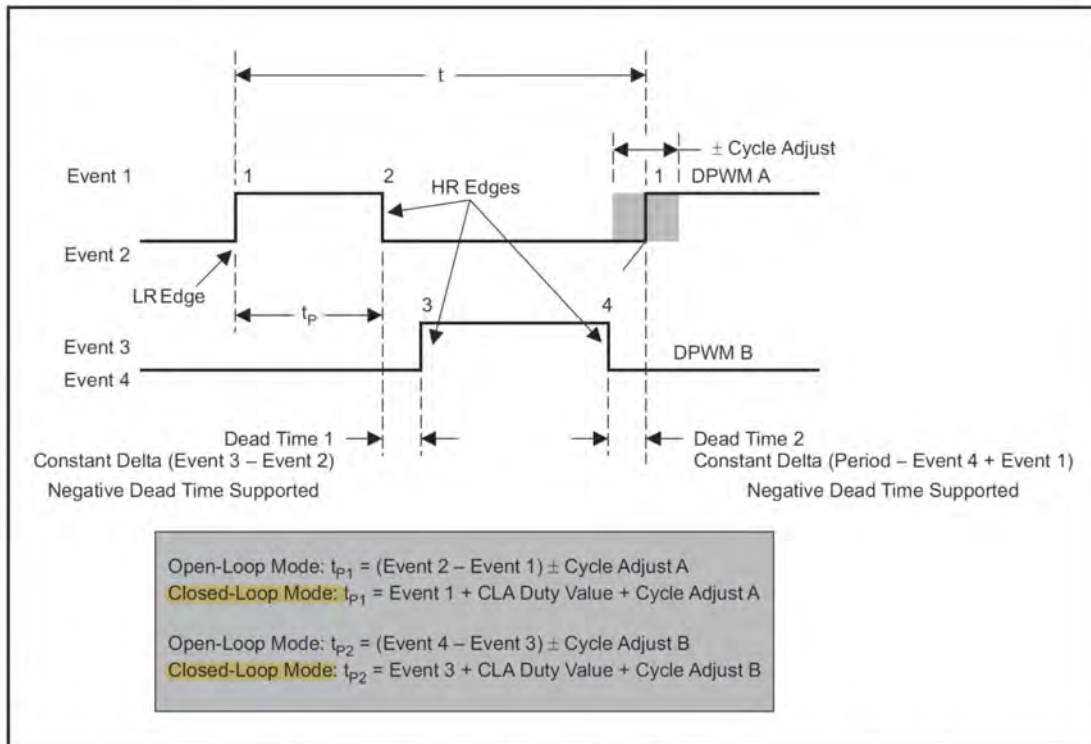


Figure 10. Resonance Mode (Constant-On Duty Ratio With Variable Period) – DPWM Timing Diagram

Id., 36.

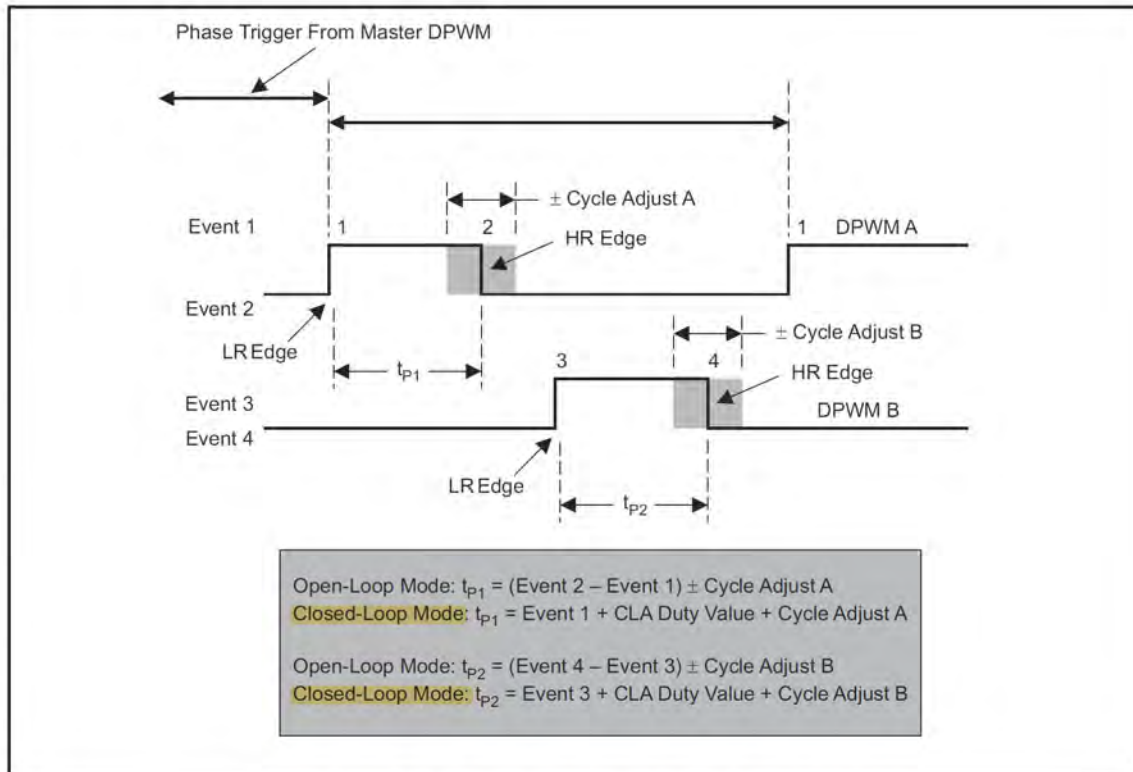


Figure 11. Multi-Output Mode – DPWM Timing Diagram

Id., 37.

E. Ground V: Obvious over Peng in view of TI UCD3138 (or, in the alternative, TI UCD3040) and AAPA

Peng (Ex. 1011) combined with TI UCD3138 (Ex. 1006) (or, alternatively, TI UCD3040 (Ex. 1018)) and further combined with the AAPA renders obvious claims 1, 22, and 31-35 of the '481 Patent. A POSITA would have been motivated to combine Peng with TI UCD3138 or TI UCD3040 because Peng explicitly states that “[m]any suitable computing stations and circuits may serve as the switching controller 160, including . . . application-specific digital/analog integrated circuits.” Ex. 1012, 14:54-58. TI UCD3138 and TI UCD3040 are both digital controllers as

described in Peng. TI UCD3138 states that its “Topology support has been optimized for . . . LLC half bridge and full bridge” converters. Ex. 1006, 7. TI UCD3040 states that it supports “half-bridge, phase-shifted full bridge, active clamp, and resonant LLC” converters. Ex. 1018, 2. Peng discloses a series resonant LCC half-bridge converter. Ex. 1012, Fig. 6, 16:10-15. This presents a POSITA with further motivation to combine. Ex. 1003, ¶ 193.

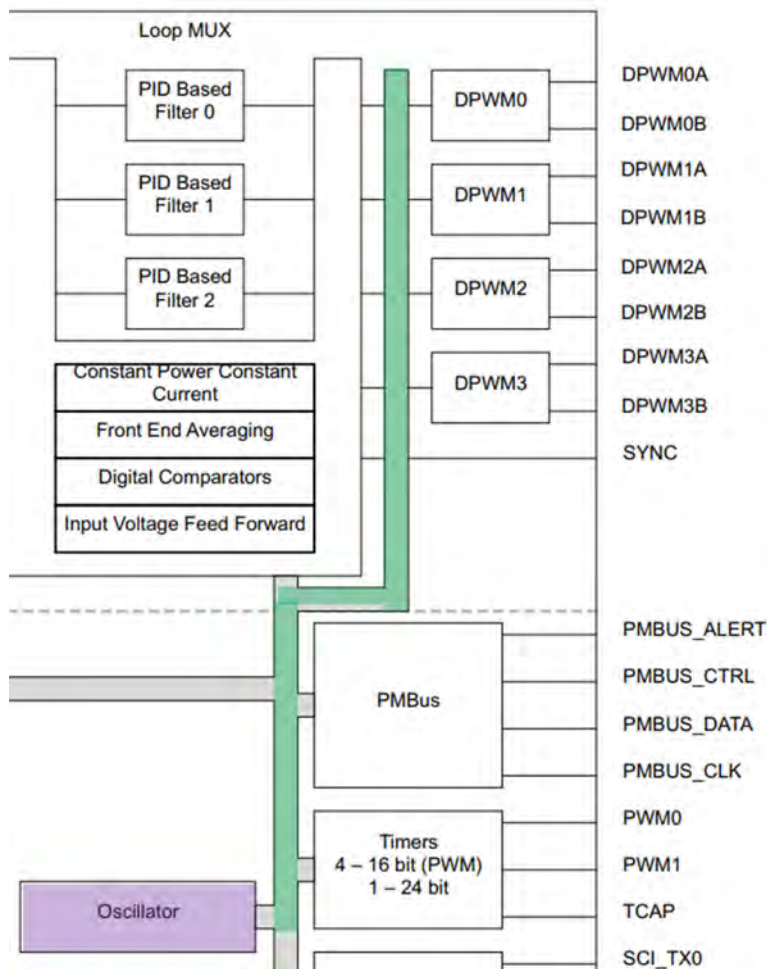
A POSITA would also have been motivated to combine Peng with the AAPA for purposes of zero current and zero voltage switching because both are related to resonant converters, and Peng contemplates zero current and zero voltage switching (Ex. 1012, 16:23-29), which the AAPA explicitly teaches. Ex. 1003, ¶ 194. A POSITA would therefore have understood and expected that the AAPA’s teachings, which were generally known in the prior art, would apply to Peng’s resonant converter, and would have looked to the AAPA for additional details related to zero current and zero voltage switching. *Id.* TI UCD3138 also relates to resonant converters and contemplates zero current and zero voltage switching. *Id.*; Ex. 1006, 7. Similarly, TI UCD3040 discusses resonant LLC converters and contemplates zero current and zero voltage switching. Ex. 1003, ¶ 194, Ex. 1018, 2.

1. Claim 1

a. Limitation 1[a]

To the extent the preamble is limiting, Peng teaches it. Ex. 1003, ¶¶ 195-196.

its switching controller 160 can be implemented using a digital integrated circuit. Ex. 1012, 14:54-58. TI UCD3138 is such a circuit, and discloses an oscillator with an oscillator frequency that generates clock signals. Ex. 1006, 9 (Fig. 2.4), 17. Figure 2.4 of TI UCD3138 (below) shows an Oscillator (purple) that generates several clock signals (green).



Ex. 1006, 9. The oscillator in TI UCD3138 has an internal oscillator frequency $f_{(PCLK)}$, having a typical frequency of 250 MHz. *Id.*, 17. TI UCD3138 also teaches that its oscillator generates clock signals.

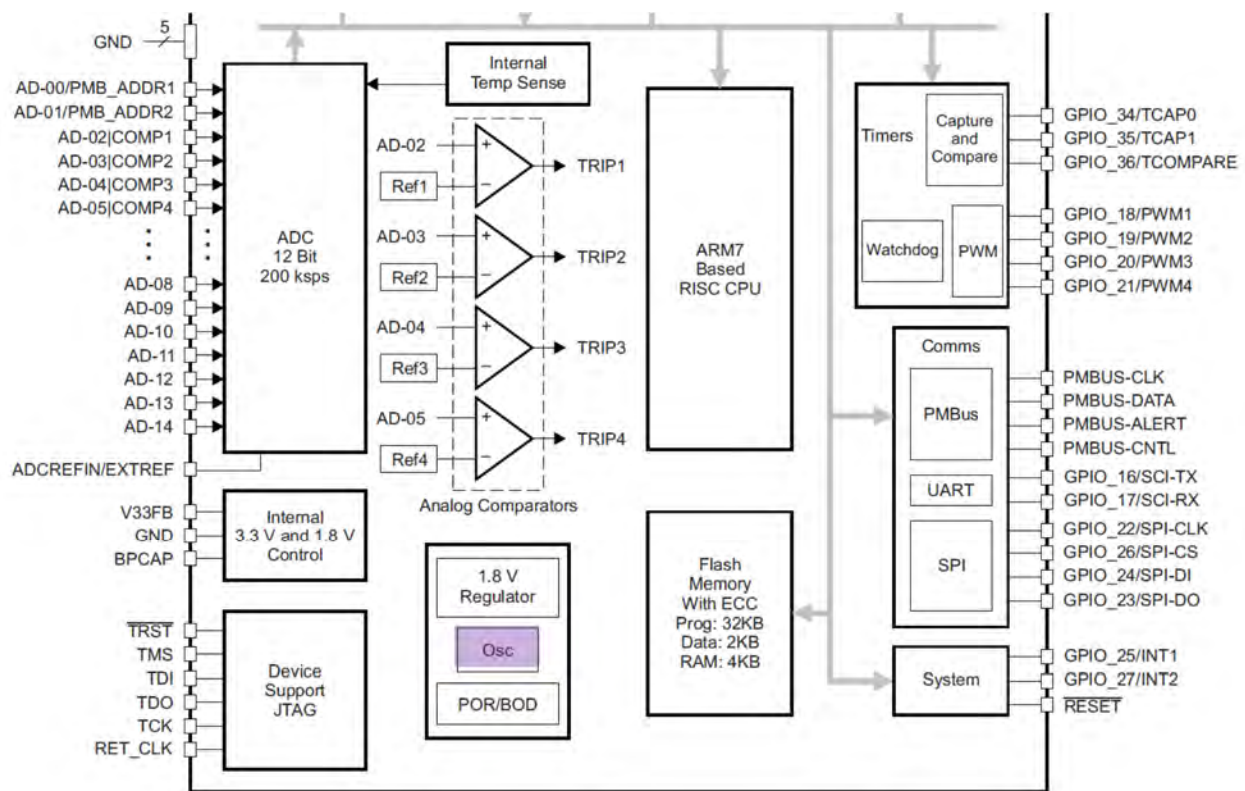
4.4.1.4 High Resolution DPWM

Unlike conventional PWM controllers where the frequency of the clock dictates the maximum resolution of PWM edges, the UCD3138 DPWM can generate waveforms with resolutions as small as 250 ps. This is 16 times the resolution of the clock driving the DPWM module.

This is achieved by providing the DPWM mechanism with 16 phase shifted clock signals of 250 MHz each. The high resolution section of DPWM can be enabled or disabled, also the resolution can be defined in several steps between 4ns to 250ps. This is done by setting the values of PWM_HR_MULTI_OUT_EN, HIRES_SCALE and ALL_PHASE_CLK_ENA inside the DPWM Control Register 1. See the Power Peripherals programmer's manual for details.

Id., 30.

TI UCD3040 also discloses an oscillator with an oscillator frequency that generates clock signals. Ex. 1018, 4, 18. The figure below shows an oscillator OSC (purple).



Ex. 1018, 4. The oscillator in TI UCD3040 has an internal oscillator frequency $f_{(PCLK)}$ of 250 MHz. *Id.*, 18.

c. Limitation 1[c]

Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶¶ 201-202. Peng teaches use of a switching controller 160 to generate gating signals to control the switching elements. Ex. 1012, 14:37-42; Fig. 5. As previously noted, TI UCD3138 and TI UCD3040 are both digital controllers that can be used in Peng's switching controller 160, and both teach that each DPWM can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31. The converter in Peng inherently operates at the resonant period and frequency to achieve ZVS and ZCS. Ex. 1003, ¶ 202.

d. Limitation 1[d]

Peng in combination with the AAPA (hereinafter, “Peng-AAPA”) renders this limitation obvious. Ex. 1003, ¶¶ 203-205. Peng discusses zero voltage and zero current switching on the primary switches. Ex. 1012, 16:27-29 (“The switches S1 and S2 are zero-voltage turn-off and zero-current zero-voltage turn-on.”).

The AAPA further teaches that zero voltage and zero current switching can be used to turn the primary switches on and off. For example, the AAPA discloses turning on (closing) a primary switch (S1) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32. It also discloses turning off (opening) a primary switch S1 “when the sinusoidal current flow completes half-cycle, and the

current I_{pri} returns substantially to zero” and “the voltages across switches S2-120 and S4-140 decline toward zero.” *Id.*, 1:36-43.

e. Limitation 1[e]

Peng-AAPA renders this limitation obvious. Ex. 1003, ¶¶ 206-210. Peng discusses achieving soft-switching of its switches, which a POSITA understands is turning devices on and off at zero or nearly zero voltage or current. Ex. 1012, 14:37-42; Ex. 1003, ¶ 206. The AAPA also teaches that zero voltage and zero current switching can be used to turn the secondary switches on and off. For example, the AAPA discloses that “the VTM may include secondary switches turned on and off essentially at times of zero voltage to rectify power from the transformer. The VTM may include secondary switches on and off essentially at times of zero current to rectify power from the transformer.” Ex. 1009, 9:25-29. The AAPA also teaches turning on (closing) a secondary switch (S3) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32. The AAPA further discloses that “the voltage across one or more of the switches may be monitored to establish the timing of a zero-voltage switching or zero-current switching event.” *Id.* 1:66-2:3.

f. Limitation 1[f]

Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶¶ 211-212. Peng teaches that the oscillator frequency

in the switching controller can be preset to “a single resonant frequency.” Ex. 1012, 26:38-45. In addition, the oscillator in TI UCD3138 has an internal oscillator frequency $f_{(PCLK)}$ that is preset, having a typical frequency of 250 MHz. Ex. 1006, 17. Similarly, the oscillator in TI UCD3040 has a preset oscillator frequency $f_{(PCLK)}$ of 250 MHz. Ex. 1018, 18.

g. Limitation 1[g]

Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶¶ 213-215. TI UCD3138 and TI UCD3040 both teach that timing of the timing control signals are independent.

4.4.1.2 DPWM Module

The DPWM module represents one complete PWM channel with 2 independent outputs, A and B. Multiple DPWM modules within the UCD3138 system can be configured to support all key power topologies. DPWM modules can be used as independent PWM outputs, each controlling one power supply output voltage rail. It can also be used as a synchronized PWM—with user selectable phase shift between the PWM channels to control power supply outputs with multiphase or interleaved PWM configurations.

Ex. 1006, 27.

DPWM Module

Programmers' Reference Manual: UCD30xx Fusion Digital Power Peripherals Programmer's Manual

The DPWM module represents one complete DPWM channel with two independent outputs, A and B. Multiple DPWM modules within the UCD30xx system can be configured to support all key power topologies. DPWM modules can be used as independent DPWM outputs, each controlling one power-supply output-voltage rail. A DPWM module can also be used as a synchronized DPWM, with user-selectable phase shift between the DPWM channels, in order to control power-supply outputs with multiphase or interleaved DPWM configurations.

Ex. 1018, 30.

TI UCD3138 and TI UCD3040 both further teach that the timing of the timing control signals for various events are independent of each other, by indicating that each DPWM can control different unrelated timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28-29.

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

2. Claim 22

a. Limitation 22[a]

See § VI.E.1.

b. Limitation 22[b]

Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this

limitation obvious. Ex. 1003, ¶¶ 217-218. Peng teaches that its switching converter 160 is used for “gating the switching elements” and includes “a circuit to generate a proper gating sequence to achieve soft switching and output power (or voltage) control.” Ex. 1012, 14:37-42.

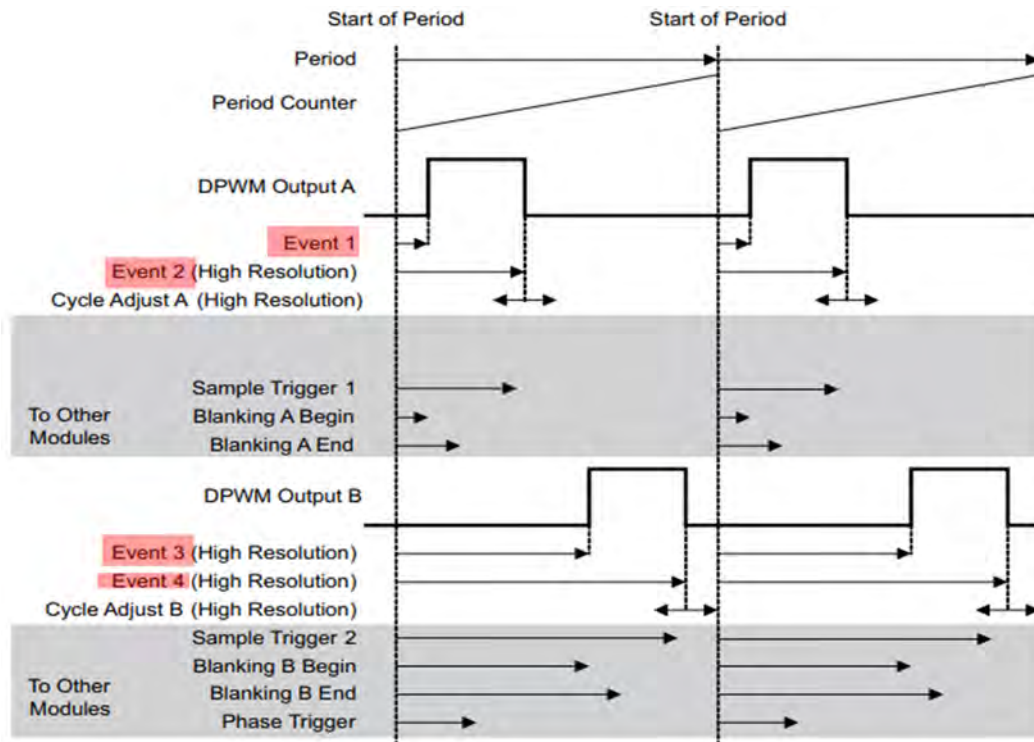
TI UCD3138 and TI UCD3040 both teach that each DPWM timing control signal can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.



Ex. 1006, 29 (showing timing signals for different events).

DPWM Events

Each DPWM can control the following timing events:

1. **Sample trigger count** – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. **Phase trigger count** – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. **Period** – Low-resolution switching-period count (count of PCLK cycles)
4. **Event 1** – Count offset for rising DPWM A event (count of PCLK cycles)
5. **Event 2** – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. **Event 3** – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. **Event 4** – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. **Cycle adjust** – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

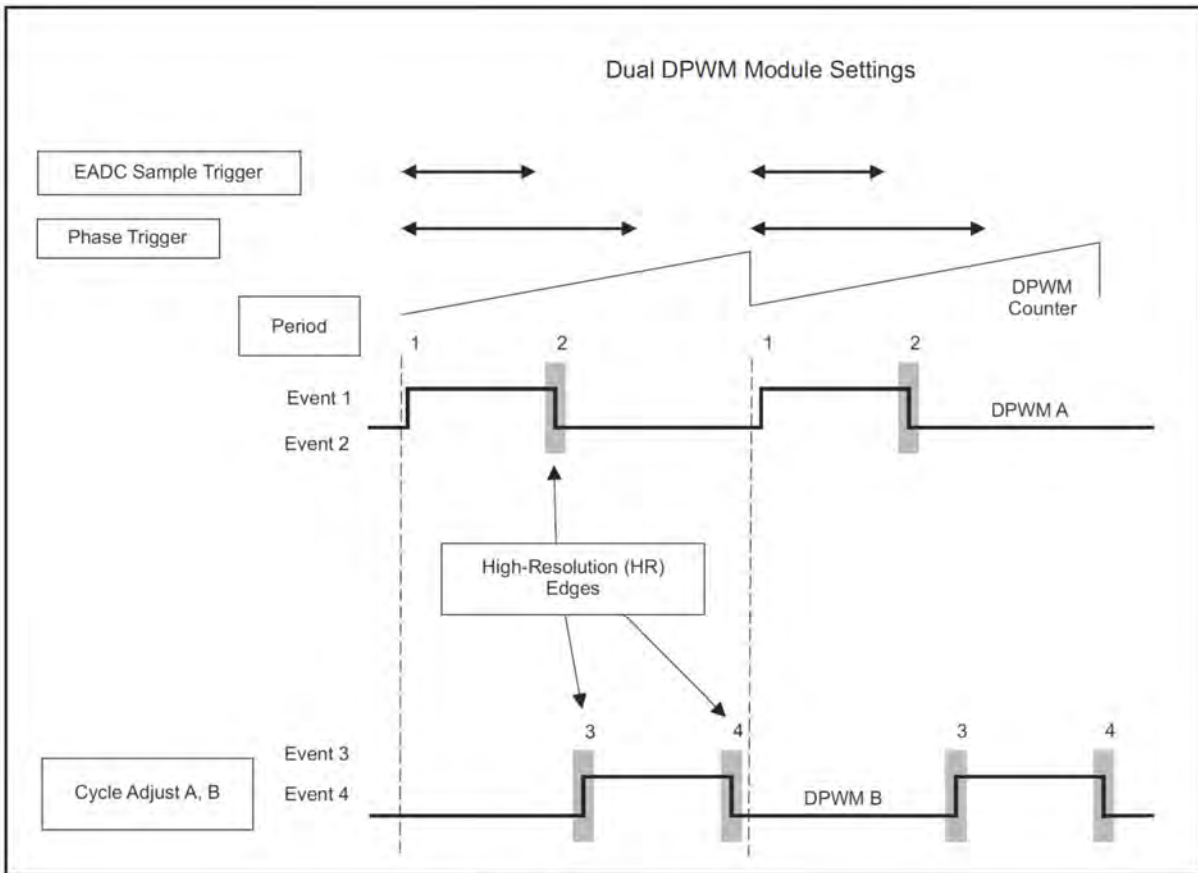


Figure 7. DPWM Events

Ex. 1018, 32 (showing timing signals for different events).

3. Claim 31

a. Limitation 31[a]

See § VI.E.1.

b. Limitation 31[b]

Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶ 220; see § VI.D.3.b.

c. Limitation 31[c]

Peng-TI UCD3138 (or alternatively Peng-TI UCD3040) renders this

limitation obvious. Ex. 1003, ¶ 221; *see* § VI.D.3.c.

d. Limitation 31[d]

Peng-TI UCD3138 (or alternatively Peng-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶ 222; *see* § VI.D.3.d.

4. Claim 32:

Peng-TI UCD3138 (or alternatively Peng-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶¶ 223-224; *see* § VI.D.4.a.

5. Claim 33

Peng-TI UCD3138 (or alternatively Peng-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶¶ 225-226; *see* § VI.D.5.a.

6. Claim 34

Peng-TI UCD3138 (or alternatively Peng-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶ 227; *see* § VI.D.6.a.

7. Claim 35

Peng-TI UCD3138 (or alternatively Peng-TI UCD3040) renders this limitation obvious. Ex. 1003, ¶¶ 228-231; *see* § VI.D.7.a.

F. Ground VI: Obvious over Leung in view of AAPA

Leung (Ex. 1013) combined with the AAPA renders obvious claims 1 and 22 of the '481 Patent. A POSITA would have been motivated to combine Leung with the AAPA for purposes of zero current and zero voltage switching because both are related to half-bridge converters, and zero current and zero voltage switching was

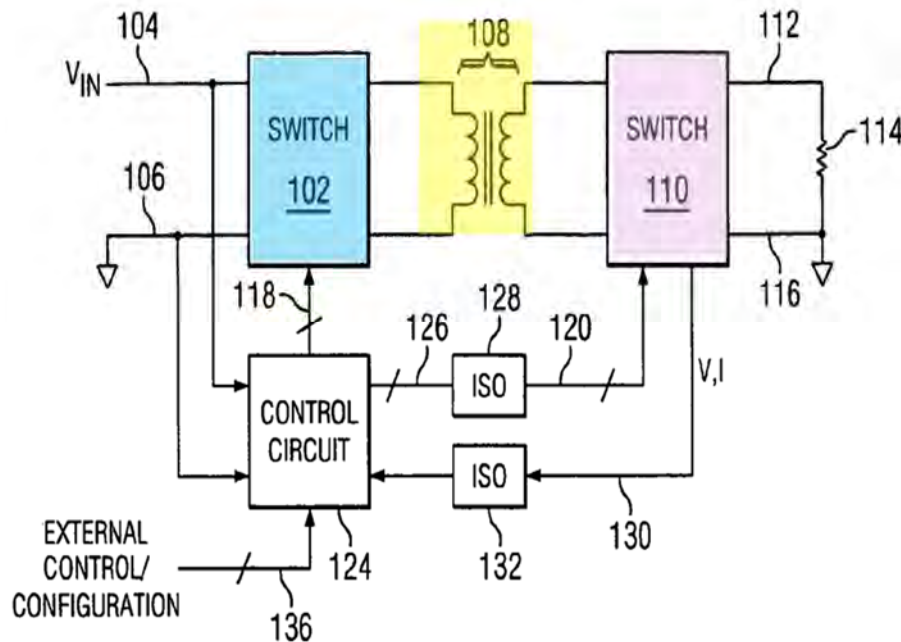
well known in the art, which the AAPA explicitly teaches. Ex. 1003, ¶ 233. A POSITA would therefore have understood and expected that the AAPA's teachings, which were generally known in the prior art, would apply to Leung's half-bridge converters, and would have looked to the AAPA for additional details related to zero current and zero voltage switching. *Id.*

1. Claim 1

a. Limitation 1[a]

To the extent the preamble is limiting, Leung in combination with the AAPA (hereinafter, "Leung-AAPA") renders this limitation obvious. Ex. 1003, ¶¶ 234-235. Leung teaches a method of synchronously operating a half-bridge power converter, where the converter has at least one primary switch, at least one secondary switch, and a transformer. Ex. 1013, [0062]. The AAPA makes clear that resonant half-bridge converters were well known in the prior art (Ex. 1001, 1:13-59, Fig. 1), and a POSITA would have known that a resonant circuit could be added the Leung's half-bridge converter, which would provide a resonant frequency and period. Ex. 1003, ¶¶ 234-235.

Figure 1 of Leung (below) shows a half-bridge converter having a primary switch group 102 (in blue), a secondary switch group 110 (in pink), and a transformer 108 (in yellow).



Ex. 1013, Fig.1

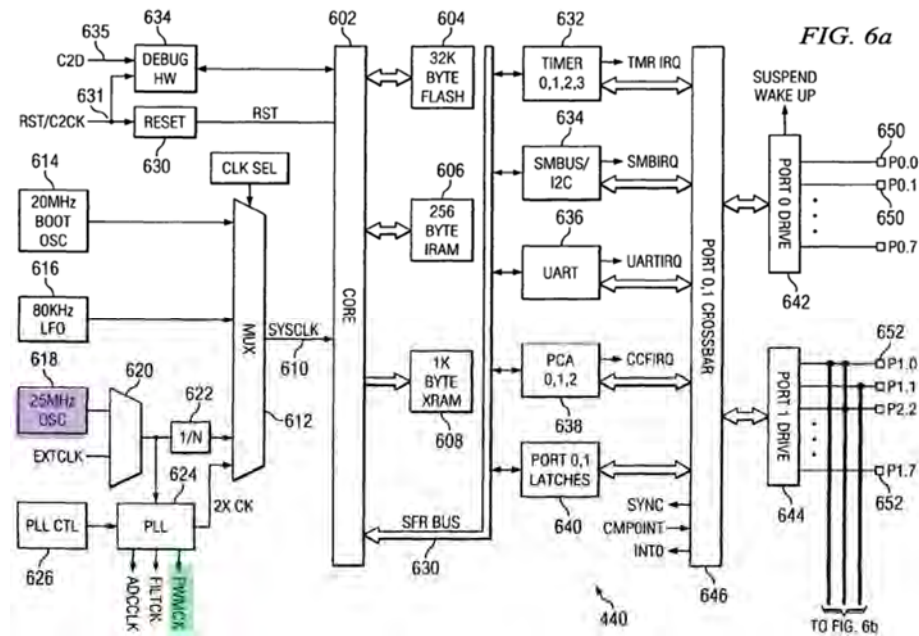
b. Limitation 1[b]

Leung teaches an oscillator OSC for generating clock signals at an oscillator frequency.

clock, if necessary. Additionally, an external clock is input to the other input of multiplexer 620, such that either the internally generated 25 MHz clock can be utilized or an external clock can be utilized. A phase lock loop 624 is provided which is controlled by a PLL control block 626 and this utilizes the 25 MHz clock 618 as a reference and then multiplies this clock up to as high as 400 kHz. This provides an output to one end of the multiplexer 612 for selection as the SYSCLK. This PLL 624 is operable to generate the other clocks associated with the operation of a digital controller, the clock for the DPWM 416, PWMCK, the filter clock, FILTCLK, and the ADC clock, ADCCLK. This will be described hereinbelow.

[0083] The core 602 is also operable to receive a Reset signal on a block 630, which is operable to generate a reset when it is not in a debug operating mode. In a debug

Ex. 1013, [0082].



Id., Fig. 6a (oscillator shown in purple, and clock signals shown in green).

c. Limitation 1[c]

Leung-AAPA teaches that the digital controller generates timing control signals (switching phases 404) from the DPWM to control the primary and secondary switches. Ex. 1003, ¶ 237; Ex. 1013, [0071]-[0072].

Digital Controller—Overall

[0071] Referring now to FIG. 4, there is illustrated a block diagram of the digital controller 124 of FIG. 1. As described hereinabove, the switching converter is generally realized with a half bridge converter, but a simpler buck converter 402 is illustrated in this figure. This requires a plurality of phases 404 for controlling the switches internal to the buck

converter 402. This will allow a DC input voltage to be converted to a DC output voltage on output 406. The digital controller senses the output voltage on the output 406 as a sense voltage, V_{SENSE} , and inputs this to one input of a differential analog-to-digital converter (ADC) 408. The other input of the ADC 408 is connected to an analog or reference voltage generated by a V_{REF} generator 410 that, as will be described hereinbelow, comprises a digital-to-analog converter (DAC).

Ex. 1013, [0071].

[0072] The output of the ADC 408 is a digital output that represents the difference between the analog output voltage on the DC output 406 and the “set point” generated by V_{REF} generator 410. The output of the V_{REF} generator 410 is typically the desired output voltage. As such, the operation of the control loop at regulation will typically result in a “0” output from the ADC 408. As will be described hereinbelow, this is the “0” code for the ADC 408. This is input to a digital compensator 412, which is operable to provide some phase lead in the loop. The buck converter 402 is comprised of a combination of a series inductor and shunt capacitor that forms an LC network, which provides a phase lag of 180° . The control loop will typically be provided by a negative feedback loop and will result in an additional negative phase shift of 180° . If the loop were allowed to operate in this manner, this would result in a 0° total phase change which would be an unstable loop. As such, the digital compensator 412 provides some phase lead to stabilize the loop. The output of digital compensator 412 provides the digital control value $u(n)$ on a digital output bus 414 for input to a digital pulse width modulator (DPWM) 416. This provides the various clock signals which provide the switching phases 404 to the buck converter 402 (or to a half bridge converter described herein above).

Id. at [0072].

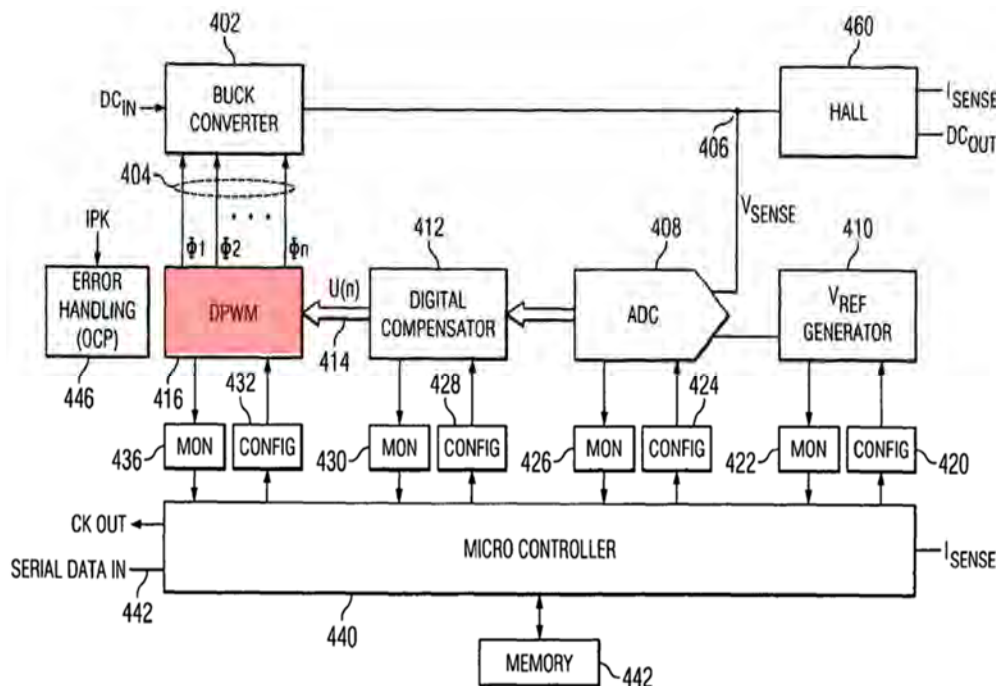


FIG. 4

Id., Fig. 4 (showing switching phases 404 (in red) coming from DPWM). The converter in Leung-AAPA inherently operates at the resonant period and frequency to achieve ZVS and ZCS. Ex. 1003, ¶ 237.

d. Limitation 1[d]

Leung-AAPA renders this limitation obvious. Ex. 1003, ¶¶ 238-239. Leung discusses that the digital control circuit 124 “is operable to control the operation of the primary switch group 102 and the secondary switch group 110. Ex. 1013, [0063].

The AAPA teaches that zero voltage and zero current switching can be used to turn the primary switches on and off. For example, the AAPA discloses turning on (closing) a primary switch (S1) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32. It also discloses turning off (opening) a primary switch S1 “when the sinusoidal current flow completes half-cycle, and the current I_{pri} returns substantially to zero” and “the voltages across switches S2-120 and S4-140 decline toward zero.” *Id.*, 1:36-43.

e. Limitation 1[e]

Leung-AAPA renders this limitation obvious. Ex. 1003, ¶¶ 240-243. The AAPA teaches that zero voltage and zero current switching can be used to turn the secondary switches on and off. For example, the AAPA teaches that “the VTM may include secondary switches turned on and off essentially at times of zero voltage to

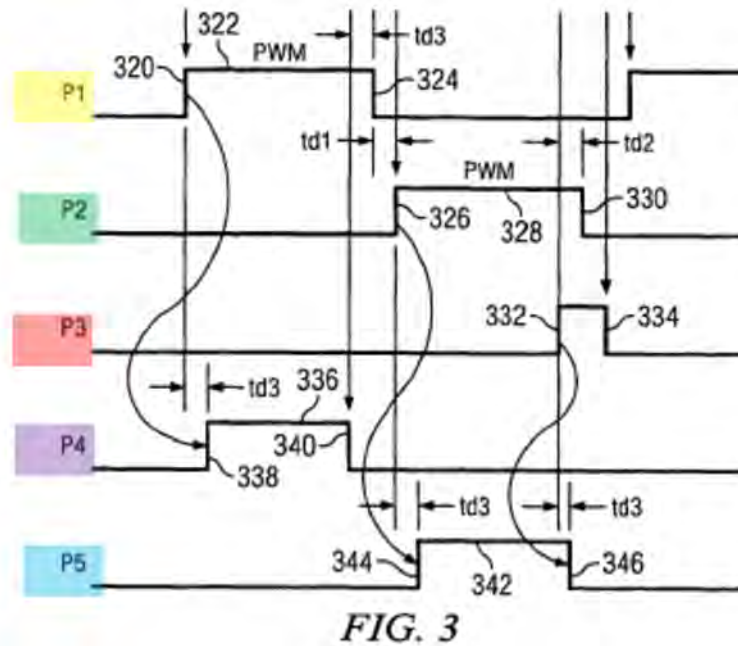
rectify power from the transformer. The VTM may include secondary switches on and off essentially at times of zero current to rectify power from the transformer.” Ex. 1009, 9:25-29. The AAPA also teaches turning on (closing) a secondary switch (S3) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32. The AAPA further teaches that “the voltage across one or more of the switches may be monitored to establish the timing of a zero-voltage switching or zero-current switching event.” *Id.* 1:66-2:3.

f. Limitation 1[f]

Leung teaches the frequency of oscillator OSC is preset at 25 MHz. Ex. 1013, [0082] (“The 25 MHz oscillator is the primary oscillator at the operating frequency of the core 602.”).

g. Limitation 1[g]

Leung teaches that timing of the timing control signals (switching phases 404) are independent. Ex. 1013, [0068] (“Referring now to Fig. 3, there is illustrated a timing diagram for generating the switching pulses to operate the switch of Fig. 2.”). As shown in Figure 3 of Leung (below), each timing pulse P1-P5 correlate to various switching transistors, and are all different, which ensures independent timing control signals. Ex. 1003, ¶ 245.



Ex. 1013, Fig. 3.

2. Claim 22

a. Limitation 22[a]

See § VI.F.1.

b. Limitation 22[b]

Leung teaches this limitation. Ex. 1003, ¶¶ 246. Leung teaches that the DPWM generates timing control signals (switching phases 404) based on clock signals to control the converter switches.

[0072] The output of the ADC 408 is a digital output that represents the difference between the analog output voltage on the DC output 406 and the “set point” generated by V_{REF} generator 410. The output of the V_{REF} generator 410 is typically the desired output voltage. As such, the operation of the control loop at regulation will typically result in a “0” output from the ADC 408. As will be described hereinbelow, this is the “0” code for the ADC 408. This is input to a digital compensator 412, which is operable to provide some phase lead in the loop. The buck converter 402 is comprised of a combination of a series inductor and shunt capacitor that forms an LC network, which provides a phase lag of 180° . The control loop will typically be provided by a negative feedback loop and will result in an additional negative phase shift of 180° . If the loop were allowed to operate in this manner, this would result in a 0° total phase change which would be an unstable loop. As such, the digital compensator 412 provides some phase lead to stabilize the loop. The output of digital compensator 412 provides the digital control value $u(n)$ on a digital output bus 414 for input to a digital pulse width modulator (DPWM) 416. This provides the various clock signals which provide the switching phases 404 to the buck converter 402 (or to a half bridge converter described herein above).

Ex. 1013, [0072].

[0139] Referring now to FIG. 34, there is illustrated a general block diagram of the DPWM 416. As noted hereinabove, the DPWM 416 is a state machine that is operable to generate up to six phases for use in driving external drivers that will control switches on the switching power converter. Each of these phases will be defined by a leading edge and a trailing edge, either leading or trailing edge being rising or falling. Either the $u(n)$ signal from the digital

See also, *id.*, [0139] (further describing switching phases 404).

G. Ground VII: Obvious over AN1336 in view of dsPIC33FJ06GS101 and AAPA

AN1336 (Ex. 1019) combined with dsPIC33FJ06GS101 (Ex. 1020) and further combined with the AAPA renders obvious claims 1 and 22 of the '481 Patent.

A POSITA would have been motivated to combine AN1336 with dsPIC33FJ06GS101 because AN1336 explicitly states that its converter “permits the implementation of control” using Microchip’s dsPIC DSC devices. Ex. 1019, 1. A POSITA would also have been motivated to combine AN1336 with the AAPA for purposes of zero current and zero voltage switching because both are related to half-bridge resonant converters, and AN1336 contemplates zero current and zero voltage switching, which the AAPA explicitly teaches. Ex. 1003, ¶¶ 248-249. A POSITA would therefore have understood and expected that the AAPA’s teachings, which were generally known in the prior art, would apply to AN1336’s resonant converters, and would have looked to the AAPA for additional details related to zero current and zero voltage switching. *Id.*

1. Claim 1

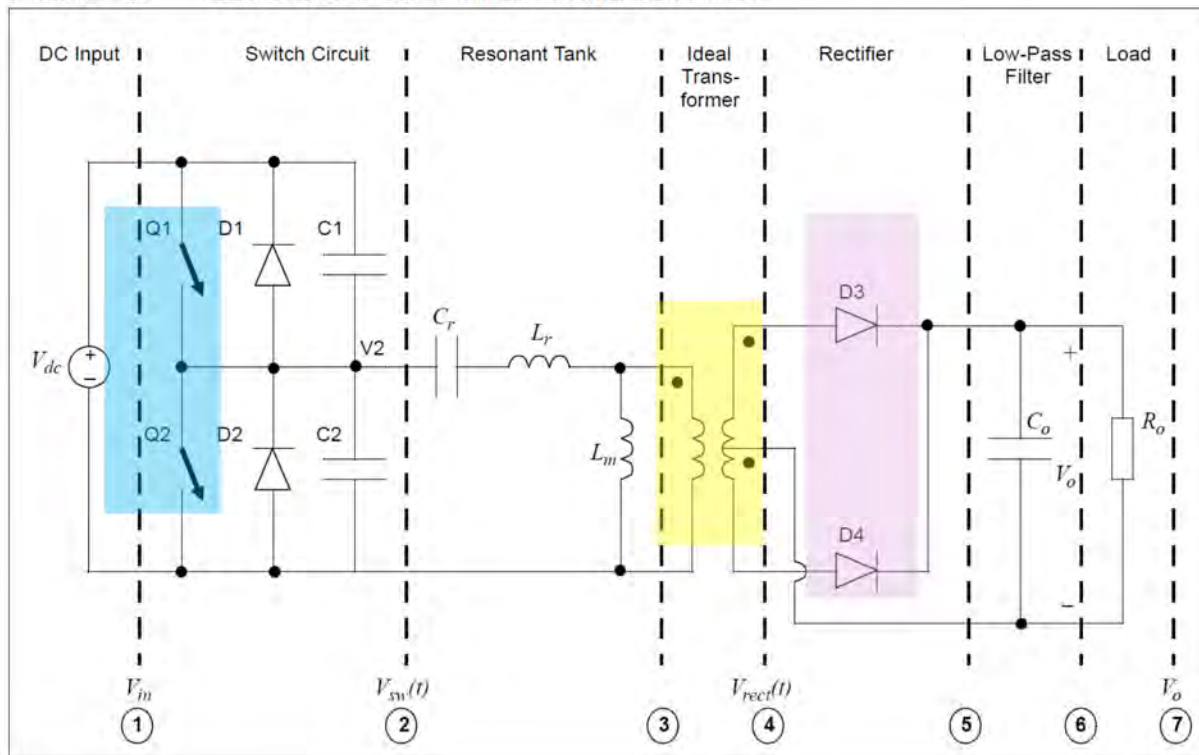
a. Limitation 1[a]

To the extent the preamble is limiting, AN1336 discloses this limitation. Ex. 1003, ¶¶ 250-252. AN1336 teaches a method of synchronously operating a half-bridge power converter, where the converter has at least one primary switch that drives a resonant circuit, at least one secondary switch, and a transformer. Ex. 1019, 8.

Figure 10 of AN1336 (below) shows a half-bridge converter having primary switches Q1 and Q2 (in blue), a resonant circuit (LLC) on the primary side (with a

resonant frequency and period) consisting of inductor L_r , inductor L_m , and capacitor C_r , secondary switches $D3$ and $D4$ (in pink), and a transformer (in yellow). The text describing Figure 10 also notes that “a diode-based full-wave rectifier is shown” but that “[a] number of different topologies can be used” including a “synchronous rectifier” which would consist of MOSFETs. *Id.*

FIGURE 10: LLC CIRCUIT COMPONENTS AND SECTIONS

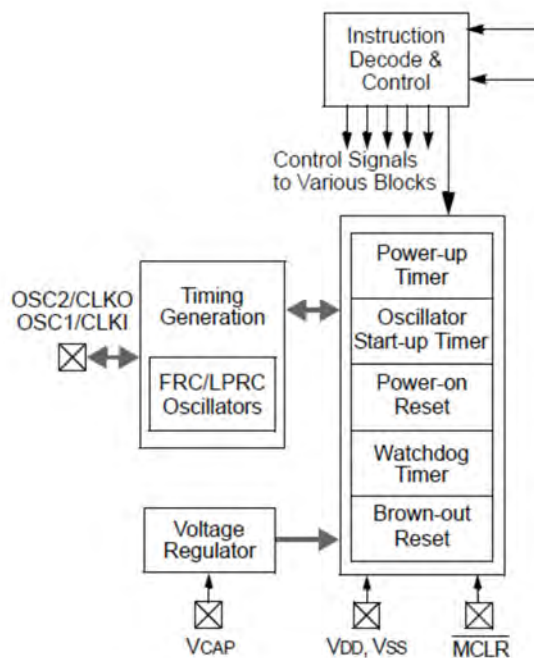


Ex. 1019, Fig. 10.

b. Limitation 1[b]

AN1336 in combination with dsPIC33FJ06GS101 (hereinafter “AN1336-dsPIC33FJ06GS101”) renders this limitation obvious. Ex. 1003, ¶ 253. Figure 1-1 of dsPIC33FJ06GS101 (below) discloses an oscillator (OSC1 or OSC2) for

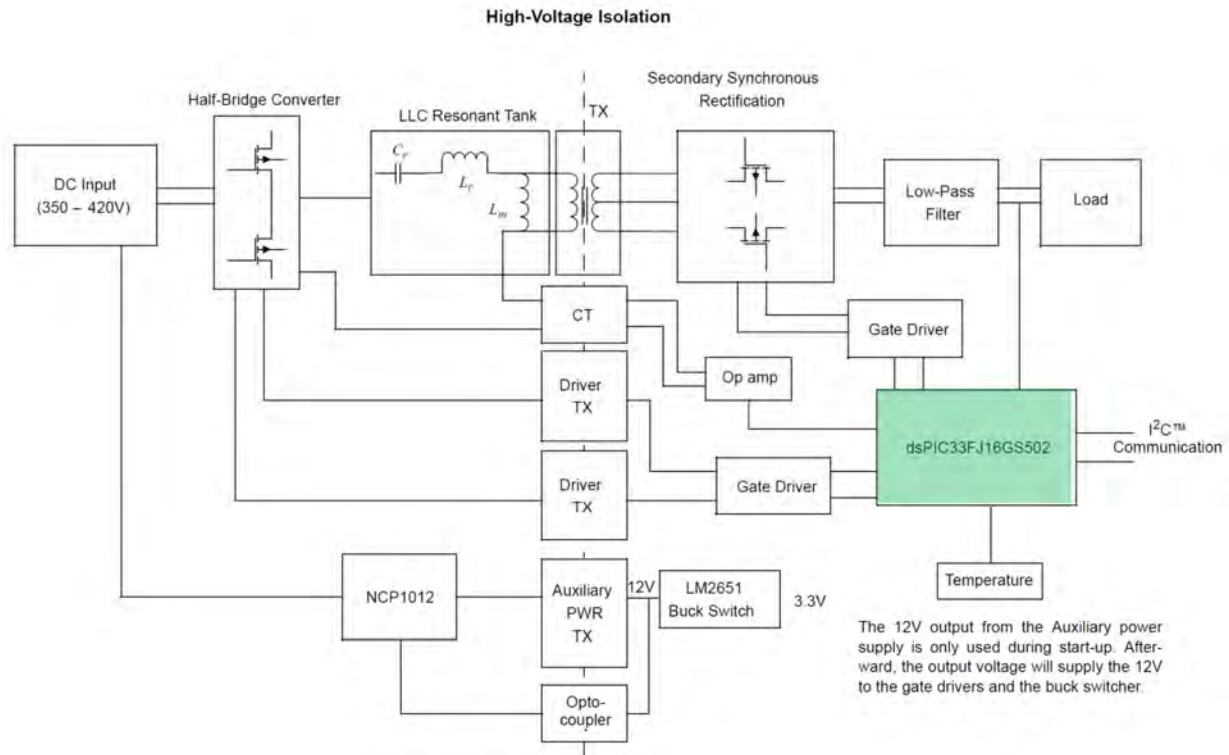
generating clock signals at an oscillator frequency.



Ex. 1020, 6 (Fig. 1-1). *See also, id.*, 133 (“The oscillator system provides external and internal oscillator options as clock sources.”).

c. Limitation 1[c]

AN1336-dsPIC33FJ06GS101 renders this limitation obvious. Ex. 1003, ¶¶ 254-256. Figure 46 of AN1336 (below) shows a dsPIC controller (in green) that generates timing control signals to control the primary and secondary switches of the converter.



Ex. 1019, 36 (Fig. 46). In addition, dsPIC33FJ06GS101 teaches that its timing control signals (PWM outputs) can control different timing events (“The high-speed PWM module incorporates . . . individual time base and duty cycle for each of the eight PWM outputs.”). Ex. 1020, 195. The converter in AN1336 operates at a resonant frequency and period. Ex. 1019, 28 (“This section describes the operation of the LLC converter at resonance, which is when the MOSFETs are operated at the same frequency as the resonant frequency.”); Ex. 1003, ¶ 256.

d. Limitation 1[d]

AN1336 in combination with the AAPA (hereinafter “AN1336-AAPA”) renders this limitation obvious. Ex. 1003, ¶¶ 257-259. AN1336 teaches that the primary switches turn on and off with zero voltage switching.

B.6 Zero Voltage Switching

Due to the phase shift between the resonant tank current and voltage the half-bridge MOSFETs are able to switch without any turn on losses. Figure B-9 and Figure B-10 demonstrate zero voltage switching on the low-side MOSFET.

Ex. 1019, 59; *id.* 59-60 (Figs. B-9, B-10).

In addition, the AAPA teaches that zero voltage and zero current switching can be used to turn the primary switches on and off. For example, the AAPA teaches turning on (closing) a primary switch (S1) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32. It also teaches turning off (opening) a primary switch S1 “when the sinusoidal current flow completes half-cycle, and the current I_{pri} returns substantially to zero” and “the voltages across switches S2-120 and S4-140 decline toward zero.” *Id.*, 1:36-43.

e. Limitation 1[e]

AN1336-AAPA renders this limitation obvious. Ex. 1003, ¶¶ 260-264. AN1336 teaches that the secondary switches turn on and off with zero current switching.

B.7 Zero Current Switching

Figure B-11 demonstrates zero current switching on the secondary rectifier. As the MOSFET current becomes zero the MOSFETs Drain-to-Source Voltage begins to rise. This eliminates any turn-off losses.

Ex. 1019, 61. *See also, id.* (Fig. B-11).

In addition, the AAPA teaches that zero voltage and zero current switching can be used to turn the secondary switches on and off. For example, the AAPA teaches that “the VTM may include secondary switches turned on and off essentially at times of zero voltage to rectify power from the transformer. The VTM may include secondary switches on and off essentially at times of zero current to rectify power from the transformer.” Ex. 1009, 9:25-29. The AAPA also teaches turning on (closing) a secondary switch (S3) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32. The AAPA further discloses that “the voltage across one or more of the switches may be monitored to establish the timing of a zero-voltage switching or zero-current switching event.” *Id.* 1:66-2:3.

f. Limitation 1[f]

AN1336-dsPIC33FJ06GS101 renders this limitation obvious. Ex. 1003, ¶ 265. dsPIC33FJ06GS101 teaches that the primary oscillator has a frequency “in the range of 10 MHz to 40 MHz,” which can be preset by the user. Ex. 1020, 134.

g. Limitation 1[g]

AN1336-dsPIC33FJ06GS101 renders this limitation obvious. Ex. 1003, ¶ 266. dsPIC33FJ06GS101 teaches that the timing of its timing control signals (PWM outputs) are set independently of other timing control signals. Ex. 1020, 195 (“The high-speed PWM module incorporates . . . individual time base and duty cycle for each of the eight PWM outputs.”); *id.* (“Independent fault/current-limit inputs for each of the eight PWM outputs.”); *id.*, 1 (“Up to four PWM pairs with independent timing.”).

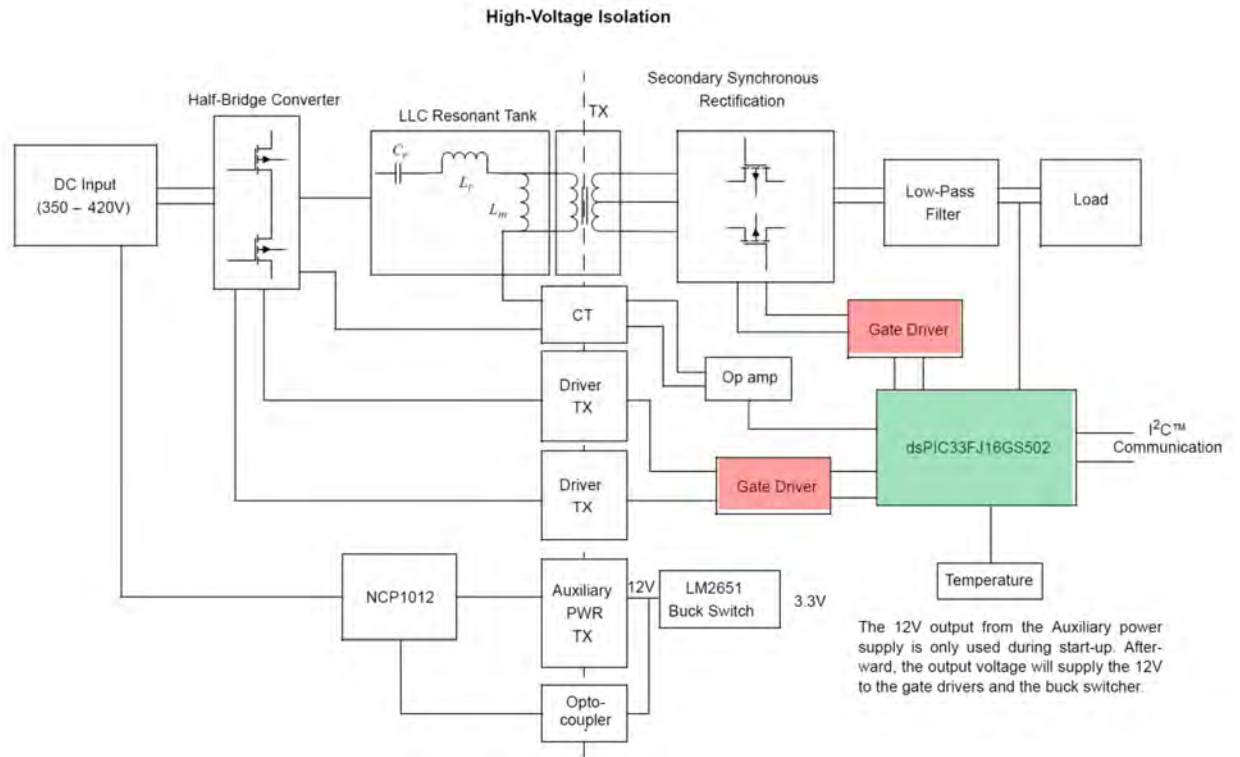
2. Claim 22

a. Limitation 22[a]

See § VI.G.1.

b. Limitation 22[b]

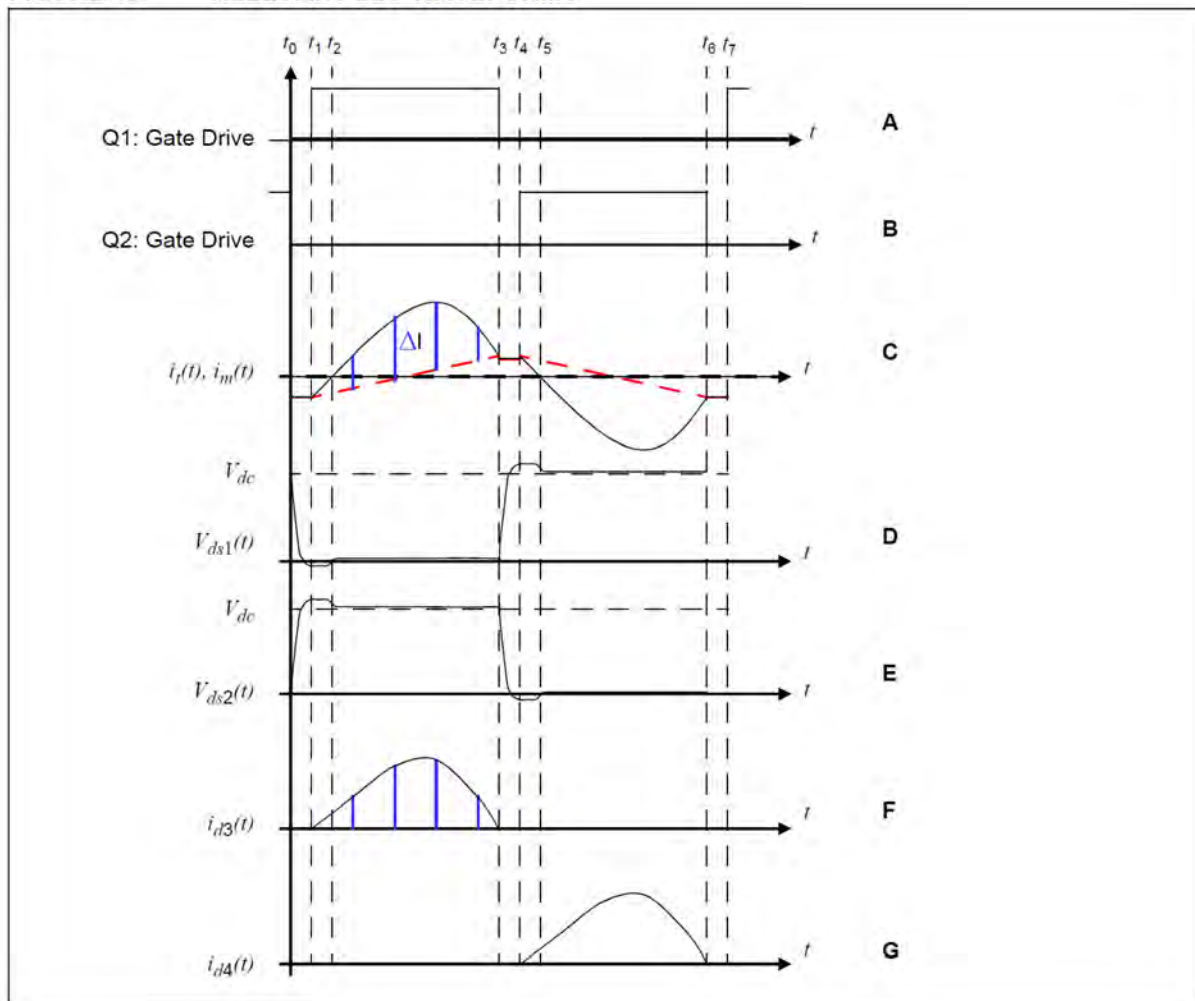
AN1336-dsPIC33FJ06GS101 renders this limitation obvious. Ex. 1003, ¶¶ 267-269. Figure 46 of AN1336 (below) teaches a dsPIC digital controller (green) that controls Gate Drive circuits (red) for operating the primary and secondary switches of the converter.



Ex. 1019, 36 (Fig. 46).

Figure 43 (below) shows waveforms of the converter circuit at resonance, including the various claimed transitions. Ex. 1003, ¶ 268

FIGURE 43: RELEVANT LLC WAVEFORMS



Ex. 1019, 32 (Fig. 43); Figs. 37-42.

In addition, dsPIC33FJ06GS101 teaches that the PWM module generates timing control signals (PWM outputs) to control the converter switches. Ex. 1020, 195 (“The high-speed PWM module incorporates . . . individual time base and duty cycle for each of the eight PWM outputs.”).

VII. SECONDARY CONSIDERATIONS

There are no secondary considerations of non-obviousness with a provable

nexus to the claimed invention of the '481 Patent. Ex. 1003, ¶ 270. Contrary to Patent Owner's allegations, Petitioner did not copy Patent Owner's power converters, and there is no evidence that any purported success or praise of Patent Owner or its power converters is related to the technology claimed in the '481 Patent.

VIII. NO JUSTIFICATION FOR DISCRETIONARY DENIAL

The Board should decline to exercise its discretion to deny institution of this Petition. On June 21, 2022, the USPTO issued a memorandum in which the Director clarified that "[t]he PTAB will not discretionarily deny petitions based on applying *Fintiv*⁸ to a parallel ITC proceeding." See Director Vidal, Memorandum, "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation," 5–7 (June 21, 2022) ("Guidance Memo"). This Guidance Memo is followed by the Board and should be applied here because, as noted in Section IX.B below, the '481 Patent is part of a parallel ITC proceeding and the related district court proceeding has been stayed. *Id.*; see also *Roku, Inc. v. Universal Electronics Inc.*, IPR2021-00263, Paper 19 at 7-9 (P.T.A.B. Feb. 8, 2023).

Furthermore, even applying *Fintiv* in view of the district court case, discretionary denial is unwarranted. *Factor 1* weighs against discretionary denial

⁸ *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential) ("*Fintiv*").

because the district court case is stayed “until the resolution of [the ITC proceedings] becomes final, including any appeals and until the Commission proceedings are no longer subject to judicial review.” *Vicor Corp. v. Delta Electronics, Inc.*, 2:23-CV-00323-JRG-RSP, Dkt. 35 (Stay Order) (E.D. Tex. Aug. 22, 2023). Because the target date for completion of the ITC investigation is not until February 3, 2025,⁹ and factoring in potential appeals, the district court stay would likely extend through the duration of this proceeding, if instituted.

Given the district court stay under Factor 1, *Factors 2–4* favor not denying institution (no trial date has been set; there is little investment in the case by the district court and parties; and little overlap, other than the ’481 patent itself, between issues raised between the Petition and district court case). *Factor 5* favors against denial because Petitioner is a defendant in the district court proceeding *along with eight (8) other parties*, as noted in Section IX.B. *Fintiv*, 13–14. Under Factor 6, even if the Board determines that the other *Fintiv* factors favor discretionary denial, the Board must also consider whether the Petition presents compelling merits. *CommScope Techs. LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 at 5 (Feb. 27, 2023) (precedential).

⁹ *Certain Power Converter Modules and Computing Systems Containing the Same*, Inv. No. 337-TA-1370, USITC Order No. 8 (Sep. 25, 2023).

Here, *Fintiv* Factors 1 through 5 weigh in favor of not denying institution. Further still, each ground in the Petition presents compelling evidence of unpatentability, and none of the references in this Petition were before the Examiner during prosecution. Given the objectives of IPRs, the Board must decline to exercise discretionary denial. Guidance Memo at 4–5.

IX. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1)

A. 37 C.F.R. § 42.8(b)(1): Real Party-in-Interest

Delta Electronics, Inc.; Delta Electronics (Americas), Ltd.; Delta Electronics (USA), Inc.; Cyntec Co., Ltd.; Delta Electronics (Thailand) Public Company Limited; and DET Logistics (USA) Corporation are the real parties-in-interest.¹⁰

B. 37 C.F.R. § 42.8(b)(2): Related Matters

The '481 Patent is the subject of ITC Investigation No. 337-TA-1370, filed

¹⁰ The following entities are not real parties-in-interest, but are being disclosed for transparency because they have also been, or may be, named as respondents in the related ITC investigation referenced in subsection B: Hon Hai Precision Industry Co. Ltd.; Foxconn Industrial Internet Co. Ltd.; FII USA Inc.; Ingrasys Technology Inc.; Ingrasys Technology USA Inc.; Quanta Computer, Inc.; Quanta Computer USA Inc.; Quanta Cloud Technology, Inc.; Quanta Cloud Technology USA LLC; QCH, Inc.

July 12, 2023 and instituted on August 15, 2023. The '481 Patent is also the subject of Civil Action No. 2:23-CV-00323-JRG-RSP in the Eastern District of Texas, filed July 12, 2023, which was stayed on August 22, 2023 pending resolution of the ITC Investigation, including any appeals.¹¹

¹¹ In addition to Petitioner, Delta Electronics, Inc., the following entities are defendants in the district court case: Delta Electronics (Americas), Ltd., Cyntec Co., Ltd., Delta Electronics (USA) Inc., Hon Hai Precision Industry Co. Ltd. d/b/a Foxconn Technology Group, Foxconn Industrial Internet Co. Ltd., Ingrasys Technology Inc., Quanta Computer Inc., and Quanta Cloud Technology Inc.

C. 37 C.F.R. § 42.8(b)(3) and (4): Counsel and Service Information

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Delta concurrently submits a Power of Attorney, 37 C.F.R. §42.10(b), and consents to electronic service directed to the following email address: 481_IPR_Delta@kirkland.com.

X. PAYMENT OF FEES UNDER 37 C.F.R. §42.103

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. 506092. Review of 7 claims is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition to be charged to the above-referenced deposit account.

XI. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies that the '481 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR of the Challenged Claims on the grounds identified herein. Petitioner certifies: (1) Petitioner is not the owner of the '481 Patent; (2) Petitioner (or any real party-in-interest) has not filed a civil action challenging the validity of any claim of the '481 Patent; (3) Petitioner filed this Petition within one year of the date it was served with a complaint asserting infringement of the '481 Patent; (4) estoppel provisions of 35 U.S.C. §315(e)(1) do not prohibit this IPR; and (5) this Petition is filed after the '481 Patent was granted.

XII. CONCLUSION

Petitioner requests institution of an IPR and cancellation of the Challenged Claims.

Dated: November 13, 2023

Respectfully submitted,

/s/ Russell E. Levine

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Attorneys for Petitioner

APPENDIX OF CHALLENGED CLAIMS

Claim Limitation	Claim Language
1[a]	A method of synchronously operating a power converter in a series of converter operating cycles the converter having at least one primary switch to drive a resonant power train and at least one secondary switch, the resonant power train including a transformer and having a characteristic resonant frequency and period, the method comprising:
1[b]	providing an oscillator for generating clock signals at an oscillator frequency;
1[c]	generating timing control signals for each of a plurality of events based upon the clock signals in a (A) standard converter operating cycle, having a standard operating period and frequency, to:
1[d]	(i) turn the at least one primary switch ON and OFF at times when essentially zero voltage is impressed across the respective at least one primary switch and essentially zero resonant current is flowing in the respective at least one primary switch; and
1[e]	(ii) turn the at least one secondary switch ON and OFF at times when essentially zero current is flowing in the respective at least one secondary switch and essentially zero voltage is impressed across the respective at least one secondary switch; and
1[f]	wherein the oscillator frequency is preset, and
1[g]	the timing of the timing control signals for one or more selected events may be set independently of other timing control signals and events.
22[a]	The method of claim 1 further comprising
22[b]	providing a gate drive circuit for operating selected switches in the converter and generating timing control signals based upon the clock signals to (a) initiate a transition of the selected switches

Claim Limitation	Claim Language
	from ON to OFF or OFF to ON, (b) hold the selected switches ON, and (c) hold the selected switches OFF.
31[a]	The method of claim 1 wherein the generating timing control signals based upon the clock signals further comprises:
31[b]	counting the clock signals from the oscillator;
31[c]	setting a count threshold for each event;
31[d]	generating the respective timing control signal for each event as the counting matches the respective count threshold.
32	The method of claim 31 wherein the oscillator and timing events are open-loop with respect to the power train.
33	The method of claim 31 wherein the oscillator or timing events are adjusted with feedback from measurements in the power train.
34	The method of claim 33 wherein the measurements and adjustments are performed during the manufacturing process
35	The method of claim 33 wherein the measurements and adjustments are performed during operation as part of a closed-loop feedback system.

CERTIFICATION OF COMPLIANCE

The undersigned certifies that the foregoing Petition complies with the type-volume limitations as mandated in 37 C.F.R. § 42.24, totaling 13,914 words. Counsel has relied upon the word count feature provided by Microsoft Word. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Dated: November 13, 2023

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CERTIFICATE OF SERVICE ON PATENT OWNER

Pursuant to 37 C.F.R. §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that a copy of the foregoing document with accompanying Exhibits 1001-1021, as listed in Petitioner's Exhibit List on pages vii-viii of this document, was caused to be served by Federal Express, costs prepaid, to Patent Owner at the following address of record:

112754 – Foley & Lardner LLP
3000 K Street N.W., Suite 600
Washington, DC 20007

Dated: November 13, 2023

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