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Design and Optimization of a High-Performance LLC Converter

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Design and Optimization of a High-Performance LLC Converter

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Abstract

In this paper, you will learn how to optimize the design of a resonant DC/DC converter using two inductors, LL, and a capacitor, C, known as an LLC converter. Our discussion will include a general background to make the topology easier to understand, a detailed transformer model and characterization procedure, and solutions to several common performance limitations. These solutions are rooted in pulse-width modulation (PWM) control enhancements to optimize performance during startup, short circuit, synchronous rectification and light load.

I. Introduction

High efficiency and high-performance power delivery are important to both power-supply design houses as well as the end users of these power supplies [1][7]. In some cases, the total efficiency of the power supply is required to be 96 percent (see Table 1), while simultaneously maintaining a high power factor and low total harmonic distortion [1].

Requirements like this are putting significant pressure on the DC/DC stage to deliver efficiency in excess of 96 percent in order to make up for losses in the power-factor-correction stage. Resonant LLC converters are receiving significant attention due to their ability to achieve these high efficiencies. Unfortunately, the implementation of many traditional high-performance features are not well understood for this topology. In addition, experience has shown that these features are also more difficult to implement even when they are understood.

In this paper, we will address three problem areas associated with resonant LLC converters – fundamental operation, resonant tank design and pulse-width modulation (PWM) methods for optimized performance – and provide detailed design insight as well as practical solutions to overcome associated challenges.

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80 PLUS Certification	115-V Internal Nonredundant				230-V Internal Redundant			
% of Rated Load	10%	20%	50%	100%	10%	20%	50%	100%
80 PLUS	–	80%	80%	80%	N/A			
80 PLUS Bronze	–	82%	85%	82%	–	81%	85%	81%
80 PLUS Silver	–	85%	88%	85%	–	85%	89%	85%
80 PLUS Gold	–	87%	90%	87%	–	88%	92%	88%
80 PLUS Platinum	–	90%	92%	89%	–	90%	94%	91%
80 PLUS Titanium	–	–	–	–	90%	94%	96%	91%

Table 1 – 80 Plus certification requirements.

II. LLC Converter Overview

Historically, buck-derived topologies have dominated the landscape of high-performance DC/DC converters: topologies include buck, push-pull, forward, half-bridge, full-bridge, phase-shifted full-bridge, etc. These circuits offer an intuitive venue for designers to work in.

Fundamentally, a buck converter works by creating a high-frequency square wave that runs through a low-pass filter to generate a DC output voltage. This low-pass filter usually comprises an inductor and capacitor, creating a classic second-order two-pole rolloff.

Controlling the output voltage is most often achieved by operating this square wave with a constant frequency-variable duty cycle (although other types of control exist). This kind of intuitive converter operation is not as easily extended to an LLC converter, however.

A. Fundamental Operation of an LLC Converter

Let's start with a brief overview of this converter and its salient operating states. Figure 1 illustrates the basic schematic for a half-bridge LLC power stage as well as the critical operating variables in the system. The output voltage is commonly controlled by using a fixed duty cycle (e.g., 50 percent) and a variable frequency. We'll discuss this further in section II-C.

Figure 2 illustrates how this system achieves zero voltage-switching (ZVS) on Q1 and Q2. In this figure, both Q1 and Q2 are modeled as ideal switches in parallel with a capacitor and diode. The node connecting Q1 and Q2 is driven by an inductor. This inductor behaves, conceptually, as a current source during the transition time.

State 1 shows that the V_{DS} of Q2 is charged all the way to V_{IN}, with the inductor current flowing through the channel of Q1. When Q1 turns off, the current that was flowing through Q1's channel diverts and flows through the two capacitors, as shown in state 2. This state continues until the V_{DS} of Q2 has dropped low enough to forward-bias the diode across Q2. At this point operation transitions to state 3. Now the system is free to turn on Q2 with a near zero voltage, thus achieving the so-called ZVS, as shown in state 4.

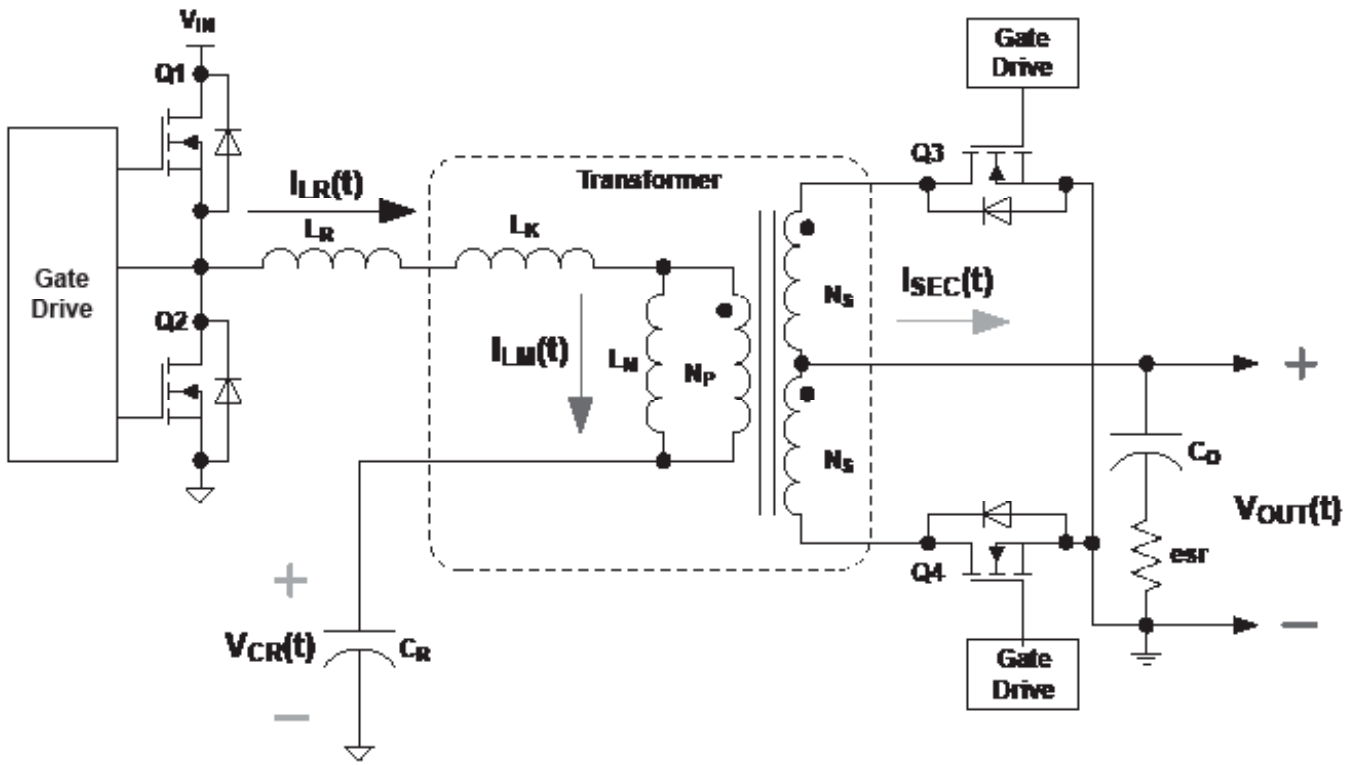

Figure 1 – Basic LLC schematic.

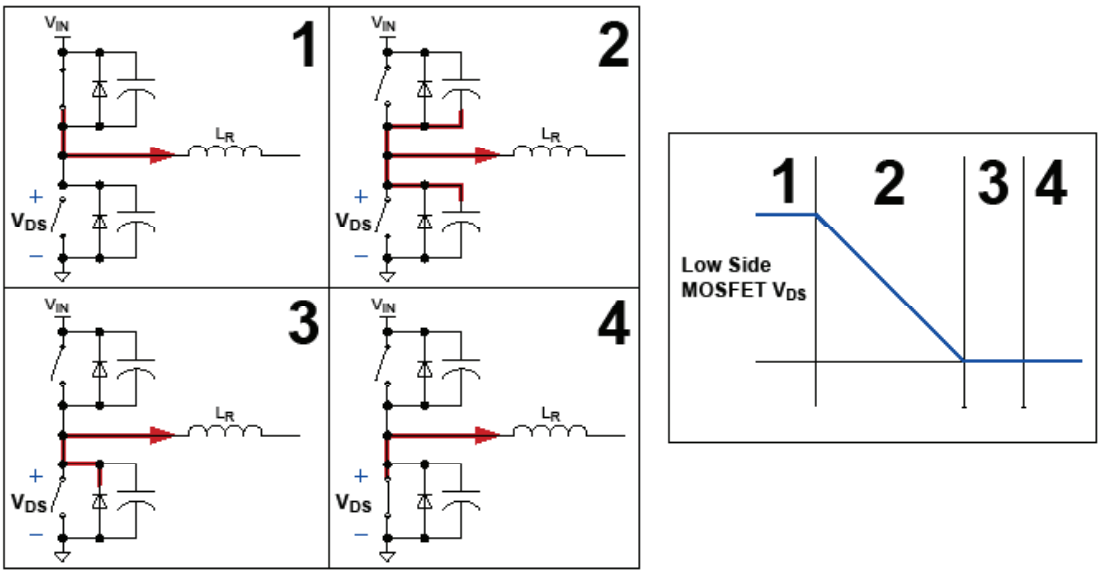

Figure 2 – Zero voltage switching.

B. Piecewise Linear Operating States

A buck converter has two fundamental operating modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM). CCM occurs when the inductor current changes continuously throughout the switching cycle. DCM occurs at light loads when the inductor current is clamped at 0 A, preventing any further reduction in the current.

Critical conduction occurs when the inductor current touches 0 A for an instant; this is the boundary between CCM and DCM. Additional modes are possible based on the type of rectification employed; however, these are the most common.

We can identify similar modes in an LLC converter. Figure 3 shows the operation at the boundary between two of the most common operating modes of the converter. The waveform names match those of Figure 1.

In Figure 2, the input voltage has been varied so that the system control effort (the operating frequency) is exactly equal to the dominant frequency of the resonant tank.

$$f_r = \frac{1}{2\pi\sqrt{(L_R + L_M)C_R}} \tag{1}$$

Notice, at this operating point, $I_{LR}(t)$ and $V_{CR}(t)$ are sine waves; $V_{OUT}(t)$ ripple and $I_{SEC}(t)$ are rectified sine waves, and $I_{LM}(t)$ is a triangle wave. This represents the simplest operating mode of the converter.

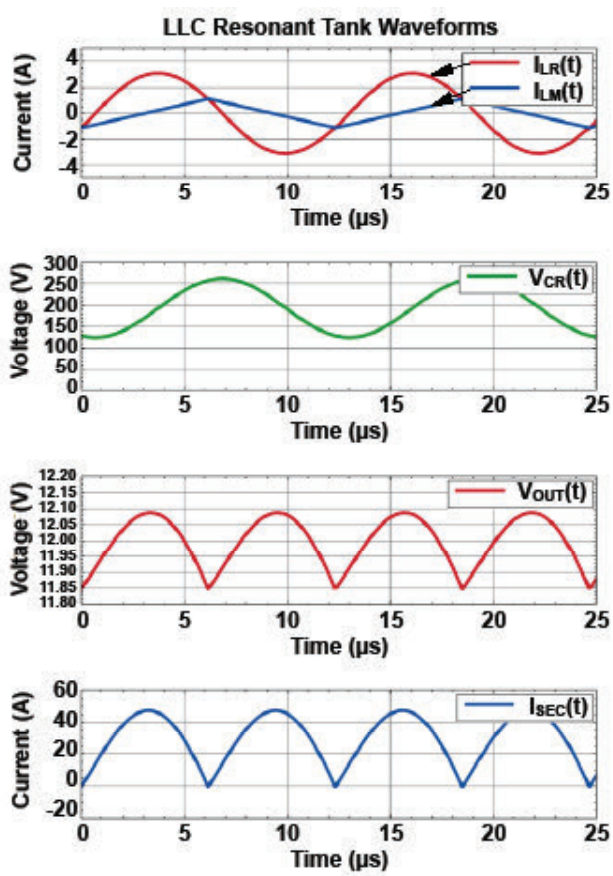

Figure 3 – Operation at resonance; V_{IN} = 387.6 V.

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To visualize this, recognize that Q1 and Q2 generate a square wave at the input to L_R. This square wave is filtered to produce a sine wave in $I_{LR}(t)$. The voltages across $L_R + L_K$ and C_R are 180 degrees out of phase and equal and opposite in magnitude. These voltages cancel out one another and produce a square wave voltage across L_M. This square wave produces the triangular-shaped current $I_{LM}(t)$ shown in Figure 3.

The input voltage is now reduced so that the system control effort changes the frequency to something below the resonant frequency, as defined by Equation 2.

$$f_s < \frac{1}{2\pi\sqrt{(L_R + L_K)C_R}} \qquad (2)$$

Figure 4 illustrates the waveforms for the condition of Equation 2. Most of the sinusoidal nature of the waveforms in Figure 3 are preserved; the exception to this is introduced by the dead time between the conduction of Q3 and Q4 as shown by $I_{SEC}(t)$. This dead time is produced when $I_{LR}(t)$ becomes equal to $I_{LM}(t)$, reducing the order of the tank by one.

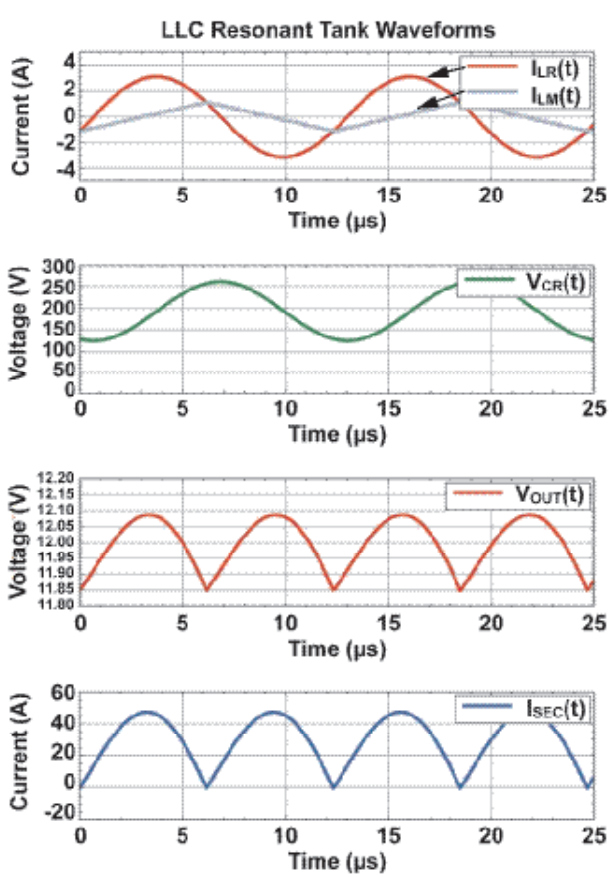

Figure 4 – Operation below resonance; V_{IN} = 370 V.

The input voltage is now increased so that the system control effort changes the frequency to something above resonance.

$$f_s > \frac{1}{2\pi\sqrt{(L_R + L_K)C_R}} \qquad (3)$$

Figure 5 illustrates the waveforms for the condition of Equation 3. More distortion is now present in the waveforms, making the sinusoidal characteristics less pronounced. In this case, the primary MOSFETs Q1 and Q2 are switched before $I_{LR}(t)$ is equal to $I_{LM}(t)$. This does not affect the ZVS on Q1 and Q2; however, it does change the switching characteristics of Q3 and Q4.

In Figures 3 and 4, notice that the current through Q3 and Q4 naturally decays to 0 A, providing zero current switching (ZCS) for these devices. In this case, switching Q1 and Q2 – prior to Q3 and Q4 reaching zero current – results in the loss of ZCS for these devices.

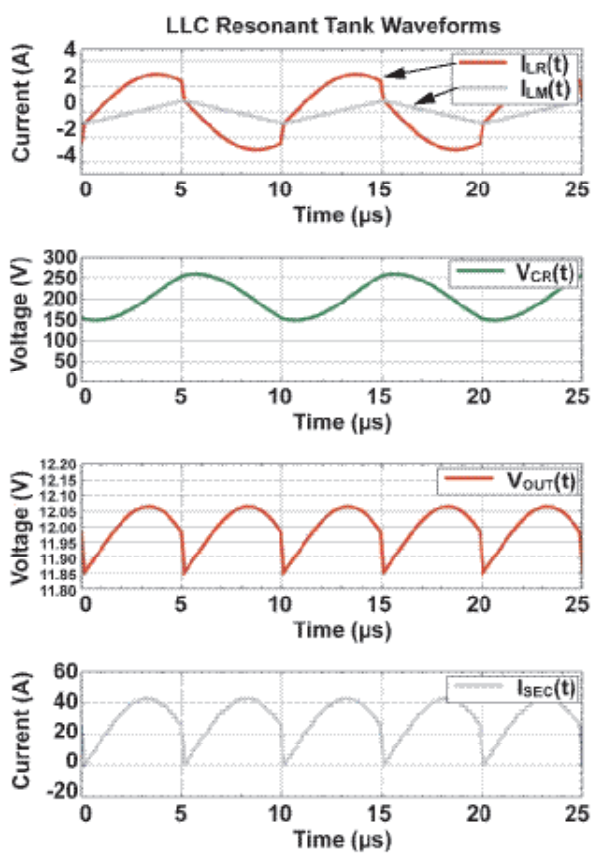

Figure 5 – Operating above resonance; V_{IN} = 410 V.

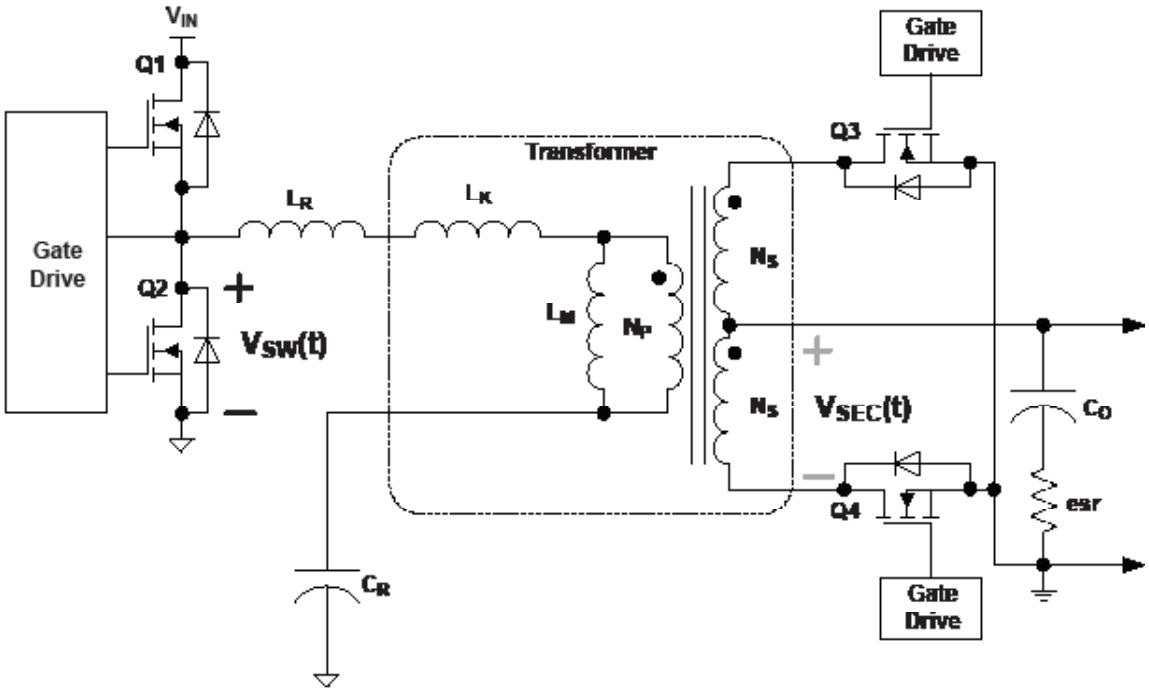

Figure 6 – Sinusoidal approximation schematic.

C. Sinusoidal Approximation

We can simplify this concept significantly by exploiting the sinusoidal nature of the system waveforms. Figure 6 shows the same schematic as Figure 1, but with the addition of two labeled variables.

Figure 7 plots what these waveforms look like when operation is at resonance, as defined by Equation 1 and Figure 3. Assuming that the bulk of the energy is transferred through the fundamental components of these square waves, these waveforms can be simplified to the sinusoidal curves overlaid on each plot in Figure 7.

You can calculate the amplitude of these sine waves using a Fourier series expansion with the closed form result shown in the legend entry for each plot in Figure 7. Utilizing these sinusoidal relationships and the RMS values of these signals results in the simplified schematic shown in Figure 8.

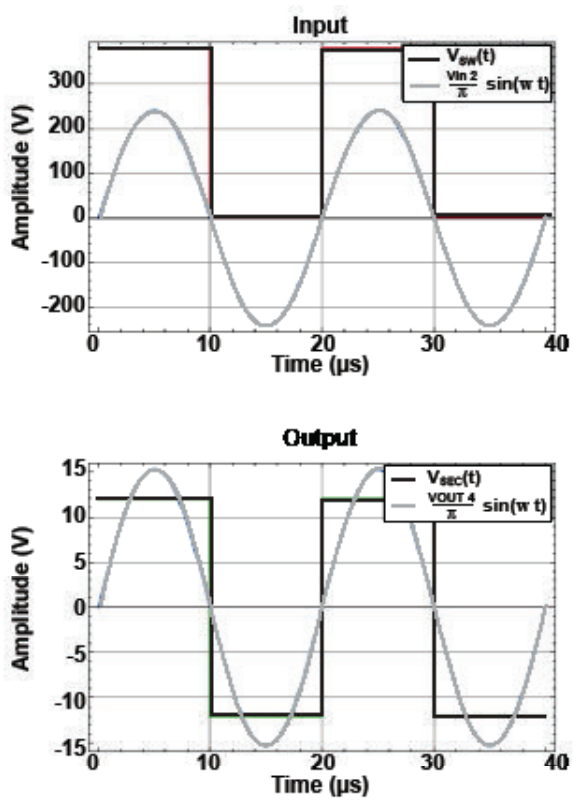

Figure 7 – Sinusoidal approximation assumptions.

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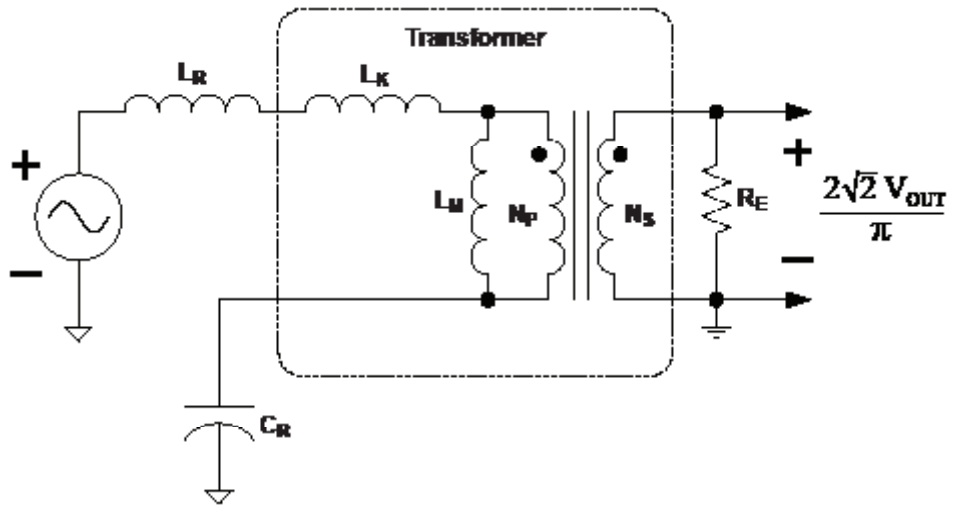

Figure 8 – Sinusoidal approximation equivalent circuit.

The only item that remains is to define an equivalent load resistance, R_E, such that the same power is delivered to the load for the DC output voltage as it is for the AC output voltage. This equivalence is quantified by Equation 4.

$$\frac{V_{OUT}^2}{R_O} = \frac{8 \times V_{OUT}^2}{\pi^2 \times R_E} \tag{4}$$

Solving Equation 4 for R_E results in Equation 5.

$$R_E = \frac{8 R_O}{\pi^2} \tag{5}$$

A similar relationship can be derived for the gain of the system at resonance, Q, as shown in Equation 6.

$$Q_E = \frac{1}{R_E} \frac{N_S^2}{N_P^2} \sqrt{\frac{L_R + L_K}{C_R}} \tag{6}$$

You can generate a plot – using linear system theory, the relationships of Equations 5 and 6 and the circuit of Figure 8 – illustrating the operating point vs. the system control effort. Figure 9 shows this relationship for a variety of load currents.

For convenience, the two resonant frequencies of the tank are marked with vertical lines and labeled with equations. The steady-state operating point of the system at nominal input voltage is marked with a black dot. In addition, the y-axis has been normalized by a factor of two – which accounts for the fact that this is a half-bridge topology – and the transformer turns ratio.

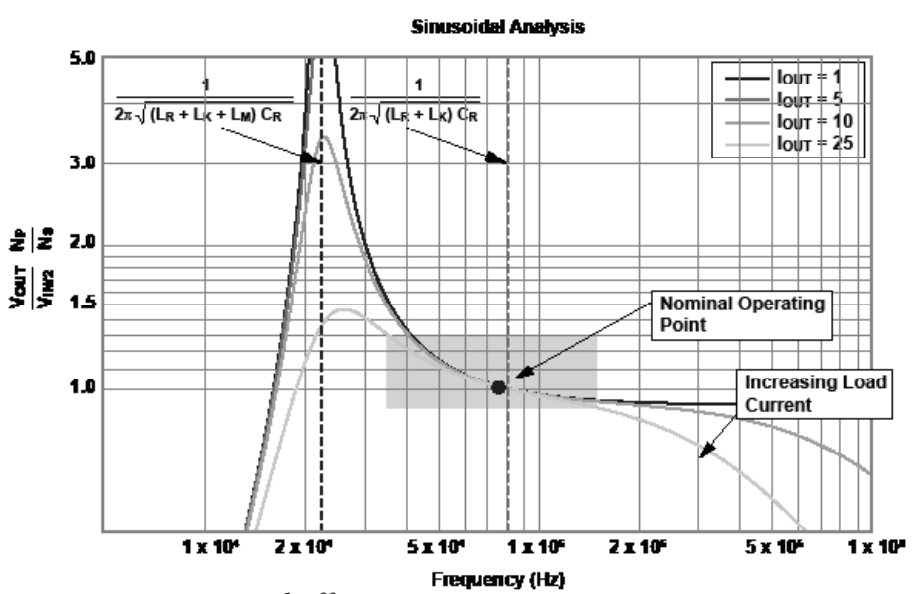

Figure 9 – Operating point vs. control effort.

If you were to plot this same relationship for a buck-derived topology operating in CCM, the x-axis control effort would be replaced with duty cycle and the first-order curve would simply be a straight line independent of load. The LLC case is quite different. The curves are load-dependent and non-monotonic. Under normal circumstances, a non-monotonic relationship like this is disastrous for a control loop. You can address this by constraining the operating frequency to a range where the curves are monotonic, as shown by the gray box. The boundary conditions for this box are chosen based on the required operating points of the system (such as what output and input voltages are required) and the component operational limits (switching losses and volt-second limits on transformers, for example).

This method is an extremely useful approximation for determining the DC operating point near the resonant frequency. As the operation deviates from this frequency, more error is introduced into the approximation. Yet this method is still useful as a starting point for the design and provides considerable insight into operation at many different frequencies.

Time-domain simulation is required for more accurate results, however, and the method provides no insight into the small-signal behavior of the system. Reference [2] provides extensive details on how to apply and use this method to the design of LLC converters.

III. Transformer Modeling and Design

At the heart of the LLC converter is the resonant tank, and central to the resonant tank is the transformer itself. In order to properly utilize this topology, it is of utmost importance to have a transformer model that preserves the salient features of the converter operation. Such a model needs to capture the significant AC and DC system operating characteristics and should also be easy to characterize and use. In this section, we'll present just such a model and discuss the design impacts to the LLC converter.

A. Previous Models

Figure 10 shows the schematic for the classic mutual-inductance coupled-inductor model.

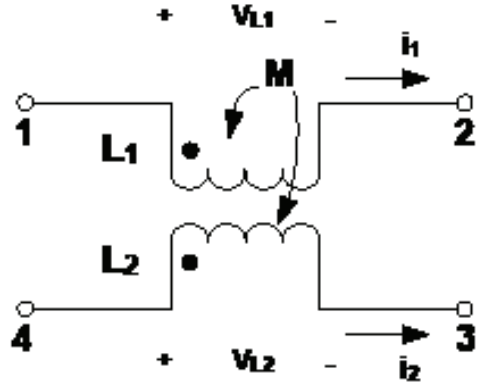

Figure 10 – Mutual inductance model.

Equations 7 and 8 exactly describe the behavior of this model.

$$V_{L1} = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt} \tag{7}$$

$$V_{L2} = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt} \tag{8}$$

Mathematically, this model can be easily extended to any number of windings; however, it is very mathematically oriented and thus it is difficult to derive any intuition from it. A better alternative is the so-called leakage-inductance model shown in Figure 11.

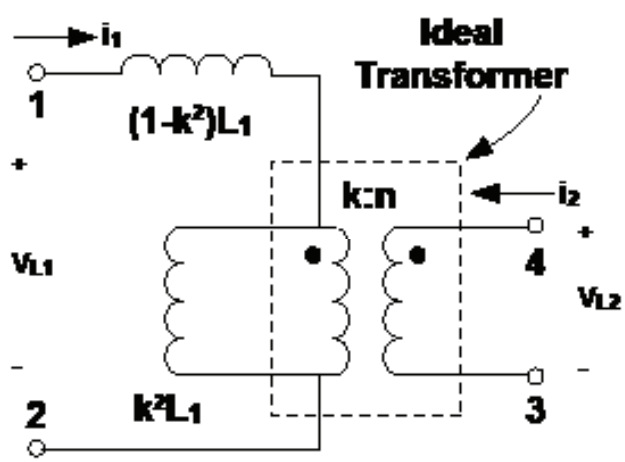

Figure 11 – Leakage-inductance model.

Using Equations 9 to 12, you can see an exact equivalence between the mutual-inductance model and the leakage-inductance model.

$$n = \sqrt{\frac{L_2}{L_1}} \tag{9}$$

$$k = \frac{M}{\sqrt{L_2 L_1}} \tag{10}$$

$$L_k = (1 - k_2) L_1 \tag{11}$$

$$L_M = k^2 L_1 \tag{12}$$

The parameters of the leakage-inductance model are easy to measure, with conventional lab equipment making it easy to characterize. This simplicity also brings with it considerable physical insight to both transformer construction and behavior.

B. Proposed Model

Figure 12 shows the schematic for a three-winding leakage-inductance model known as the cantilever model. The transformers shown in the schematic are ideal, and each has a unique turns ratio. There is also a magnetizing inductance and an individual leakage-inductance term between each winding.

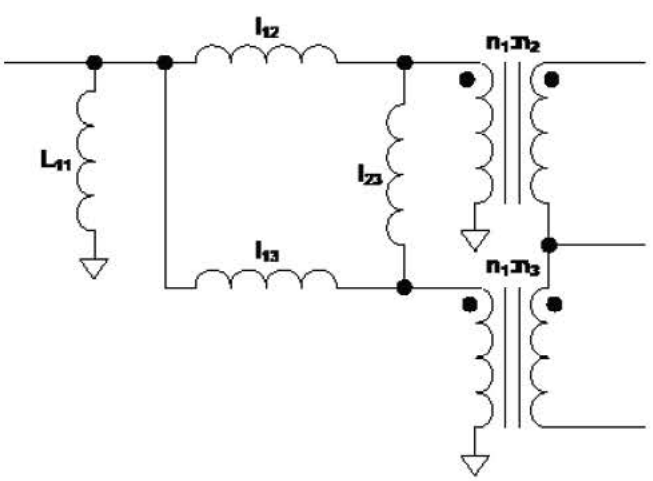

Figure 12 – Cantilever model.

As we will show later, this model requires the winding resistances to capture all of the salient features of the converter operation over frequency. Figure 13 shows a modification to this model that includes these resistances.

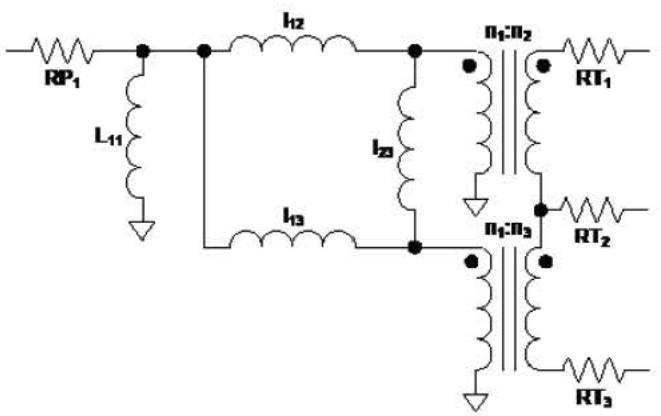

Figure 13 – Extended cantilever model.

C. Resistance Characterization

The resistance is easily characterized by using the DC winding resistance. At first glance, this may appear to be an unreasonable assumption for those familiar with the additional losses due to skin and proximity effect. It turns out that the sinusoidal nature of the LLC converter significantly reduces the high-frequency harmonics normally encountered in PWM converters. The validity of this assumption will be validated with test data in section III-E.

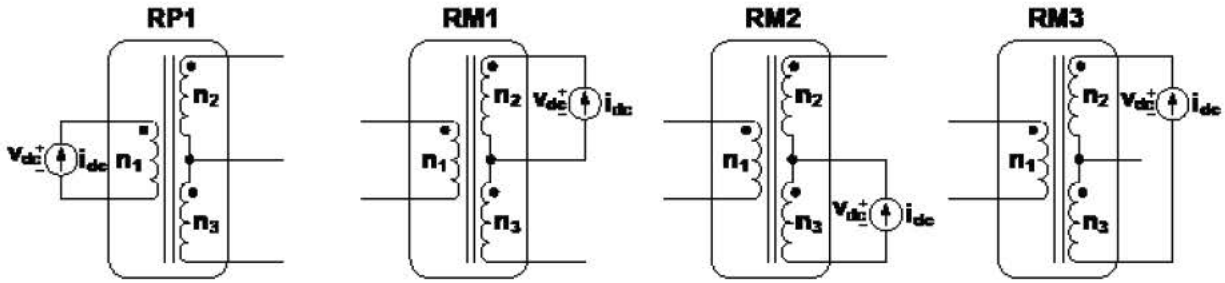

Figure 14 – Resistance characterization.

Figure 14 illustrates a series of measurements that can easily characterize the DC resistance terms of the model of Figure 13. In each case, the current source represents a precision resistance meter.

You can use Equations 13, 14 and 15 to easily convert these values to the model parameters shown in Figure 13.

$$RT1 - \frac{1}{2}(RM1 \quad RM2 + RM3) \tag{13}$$

$$RT2 - \frac{1}{2}(RM1 + RM2 \quad RM3) \tag{14}$$

$$RT3 - \frac{1}{2}(\ RM1 + RM2 + RM3) \tag{15}$$

D. Inductance Characterization

We will cover two methods for characterizing model-inductance parameters. The direct method offers a mathematically simple solution at the expense of more complex measurement methods. In contrast, the indirect method is mathematically complex; however, the measurements are intuitive, accurate and easy to perform.

i. Direct Method

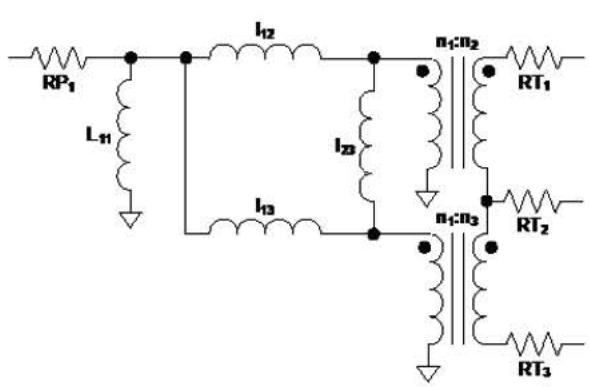

Figure 15 – Direct measurement method.

Figure 15 illustrates the measurement of l_{12}. In this case, both tertiary windings are shorted, a voltage stimulus is applied to the primary, and the resulting current is measured on the n_2 winding. If the shorts applied to the tertiary windings are sufficiently low to guarantee that no current flows through l_{23}, then the measurement of i_{ac} will be equal to the current through l_{12} transformed by turns ratio. Mathematically, this is expressed as Equation 16.

$$l_{12} = \frac{V_{ac}(s)n_1}{i_{ac}(s)n_2 s} \tag{16}$$

Where:

$s = j2\pi f$

f = excitation frequency

You can follow a similar procedure to obtain measurements for l_{13} and l_{23}, resulting in Equations 17 and 18.

$$l_{13} = \frac{V_{ac}(s)n_1}{i_{ac}(s)n_3 s} \tag{17}$$

$$l_{23} = \frac{V_{ac}(s)n_1^2}{i_{ac}(s)n_2 n_3 s} \tag{18}$$

Although mathematically and conceptually simple, the practical implementation of accurate measurements is difficult. First, conventional impedance analyzers are constructed to inject and measure at the same node. But in this case, the injection node and one of the measurement nodes occurs at the same place, while the current measurement occurs at a remote location. While this is technically feasible, it is not convenient. In

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addition, this method only works well if the short can be made sufficiently small to guarantee that no current flows through l_{23}. In practice, any real-world short is going to introduce some inductance into the circuit.

Figure 16 shows how the inductance of this short will modify the measured value of l_{12}. It only takes 25 nH (approximately 1 inch of wire) of inductance to cause a 30 percent error in the measured value of l_{12}.

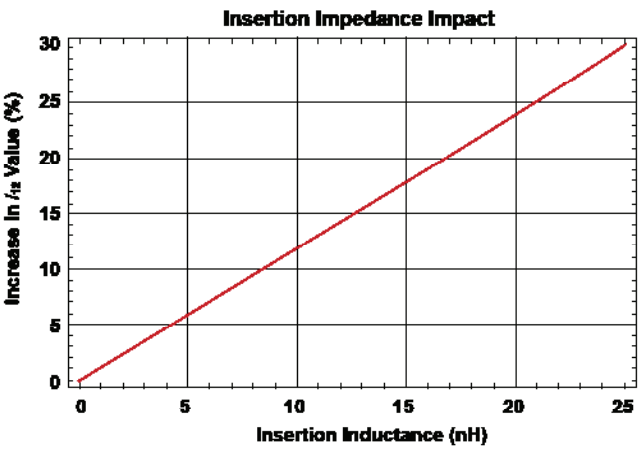

Figure 16 – Direct measurement insertion impedance.

ii. Indirect Method

In the indirect method, an intermediate set of inductances are measured and subsequently translated into the model parameters using linear algebra. Figure 17 illustrates the measurement of the intermediate inductance parameter L_{K2}. A short is placed across n_2; a signal is then injected and measured on the primary. The location of the injection and measurement is the same node, making it easy to use more conventional lab equipment to make the measurement. And because there is no need to measure a current through the shorted node, it is possible to make a lower-impedance short.

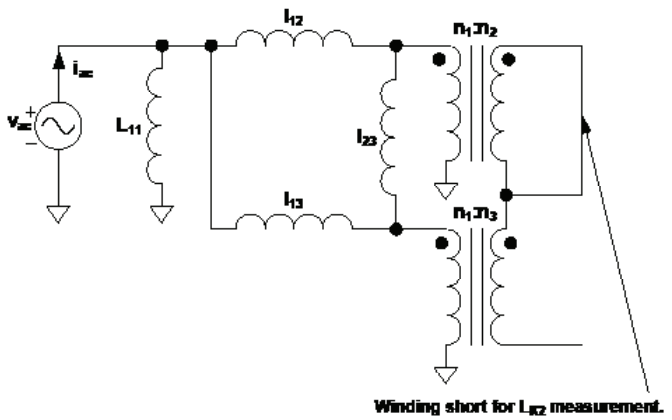

Figure 17 – Indirect measurement method.

In the case of the direct measurement, additional room is needed to account for the current measurement. The only real downside of the indirect technique is that the resulting measurements are not that useful all by themselves. They must be transformed into the model parameters by using Equations 19, 20 and 21.

Although these equations are complex, the benefit they bring to practical and accurate measurement techniques is significant.

$$l_{12} = \frac{-\sqrt{L11^2\ LK1^2\ (L11-LK2)\ (L11-LK3)\ (LK1-LK2)\ (LK1-LK3)} + \cdots + L11^2\ LK1(LK1-LK3) + L11LK1LK2\ (LK3-LK1)}{(L11-LK1)\ (L11-LK2)\ (LK1-LK3)} \tag{19}$$

$$l_{13} = \frac{-\sqrt{L11^2\ LK1^2\ (L11-LK2)\ (L11-LK3)\ (LK1-LK2)\ (LK1-LK3)} + \cdots + L11^2\ LK1(LK1-LK2) + L11LK1LK3\ (LK2-LK1)}{(L11-LK1)\ (L11-LK3)\ (LK1-LK2)} \tag{20}$$

$$l_{23} = \frac{\begin{array}{c}(L11(L11^3(-LK1)(LK1(LK2+LK3)-2LK2LK3)+\cdots \\ +L11((LK2+LK3)\sqrt{L11^2\ LK1^2\ (L11-LK2)\ (L11-LK3)\ (LK1-LK2)\ (LK1-LK3)} \\ +LK1^2(-LK2)\ LK3\ (LK2+LK3)+2LK1LK2^2LK3^2)+\cdots \\ -2LK2LK3\sqrt{L11^2LK1^2(L11-LK2)\ (L11-LK3)\ (LK1-LK2)\ (LK1-LK3)}+\cdots \\ +L11^2\ LK1(LK2+LK3)\ (LK1(LK2+LK3)-2LK2LK3)))\end{array}}{((L11-LK1)\ (L11-LK2)\ (L11-LK3)\ (L11(LK1(LK2+LK3)-LK2LK3)-LK1LK2]} \tag{21}$$

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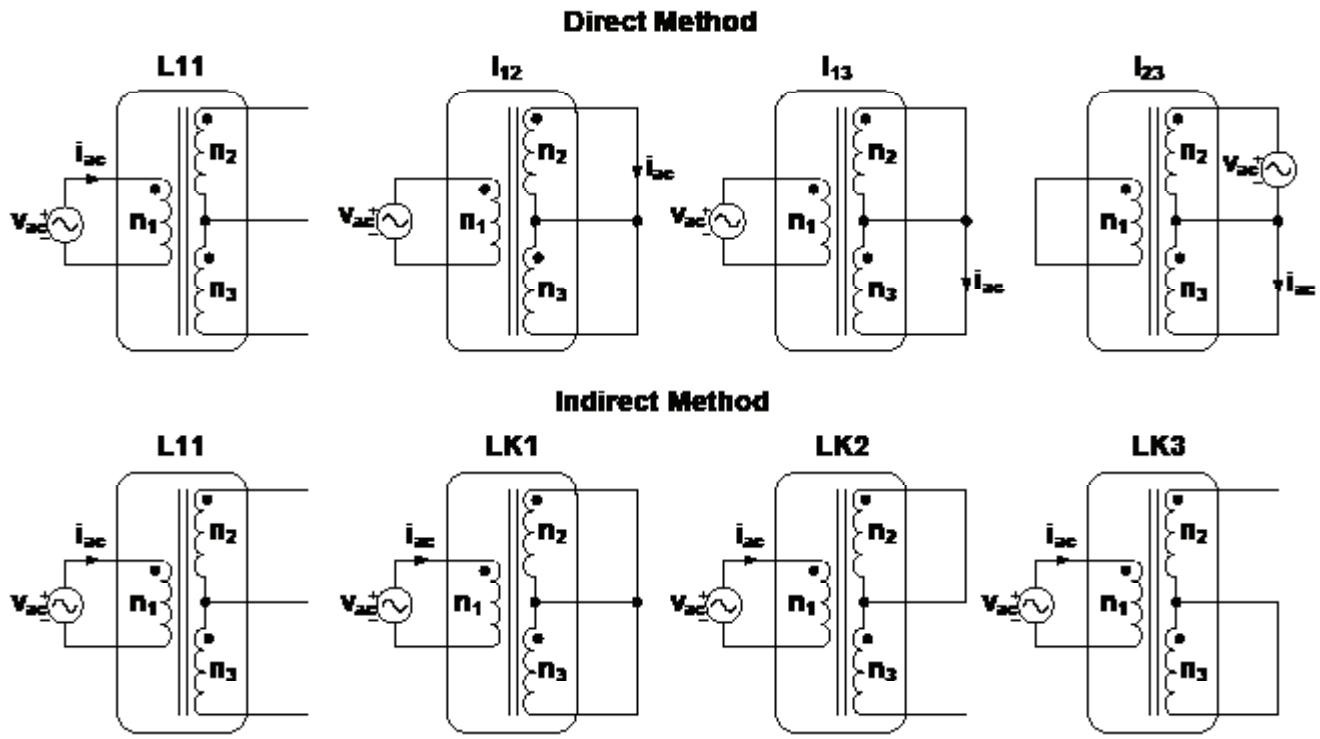

Figure 18 – Complete inductance measurement setup.

Figure 18 illustrates the complete setup for all of the inductance measurements using the direct and indirect methods.

E. Model Validation

We characterized an actual transformer using the indirect method. The resulting model parameters are shown in Table 2. It is important to recognize that the values in this table represent model parameters and do not by themselves necessarily have any intuitive meaning; it is only when the parameters are taken together that they are significant.

For example, notice that RT_2 is a negative number. By itself, a negative resistance does not make sense in this context. However, RT_2 only conducts current when in series with either RT_1 or RT_3. In those cases, the sum of $RT_1 + RT_2$ and $RT_2 + RT_3$ is always positive, restoring the model intuition.

LLC Extended Cantilever Model Parameters	
L_{11}	570 µH
n_1	32
n_2	2
n_3	2
RP_1	122.5 mΩ
RT_1	2.6 mΩ
RT_2	-415 µΩ
RT_3	2.5 mΩ
l_{12}	19.7 µH
l_{13}	16.8 µH
l_{23}	25.9 µH

Table 2 – Cantilever model numerical example.

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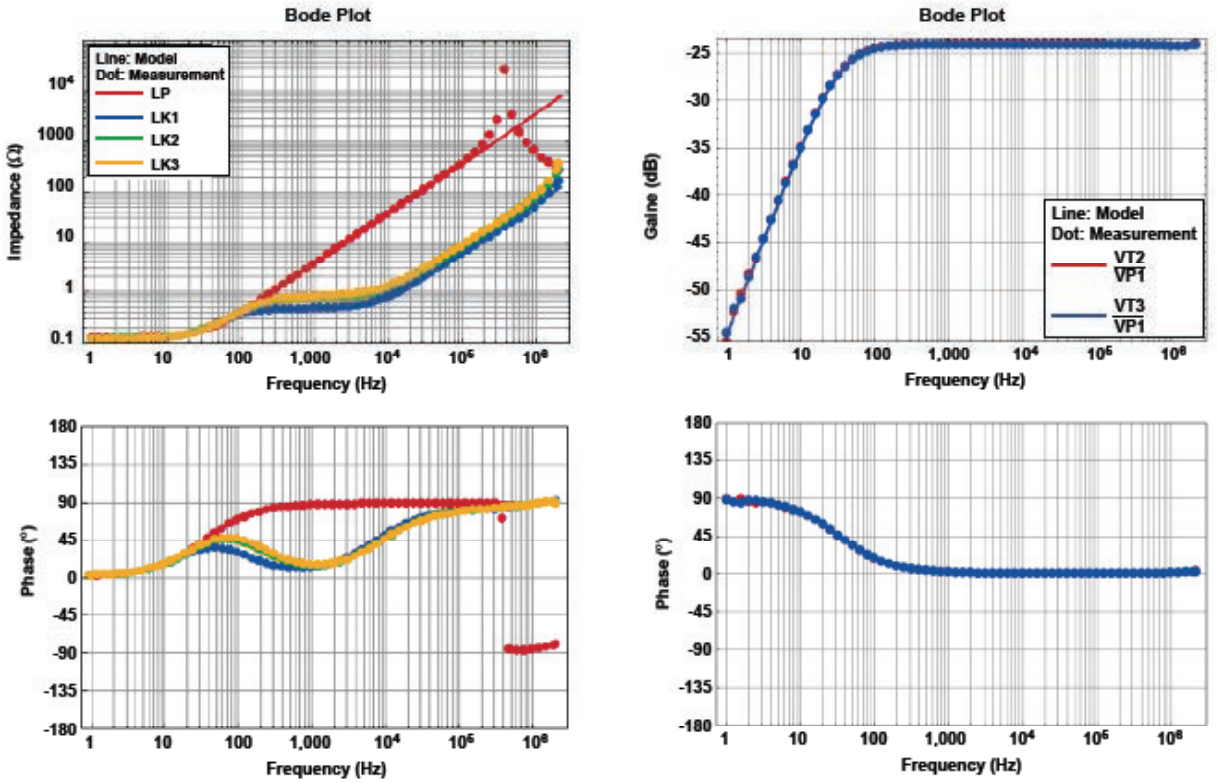

Figure 19 – Model results vs. measurement.

Figure 19 shows the measured results of the indirect method compared to the model. The plots on the left are the various inductance impedance measurements, while the plots on the right are the effective primary to secondary turns ratios.

In general the correlation is very good; however, there is one obvious discrepancy: the resonance at ~300 kHz. This is the result of the parasitic capacitance of the transformer in parallel with the capacitance of the measurement probes. This capacitance is estimated – via a curve fit – and included in the model plot in Figure 20.

The remaining poles and zeros in the plots of Figure 19 are due to the interaction of the inductance and resistance terms. In the previous section, the model resistances were characterized using the DC assumption. Given the very close correlation between model and measurement over a wide frequency range in Figure 19, this assumption appears well-justified.

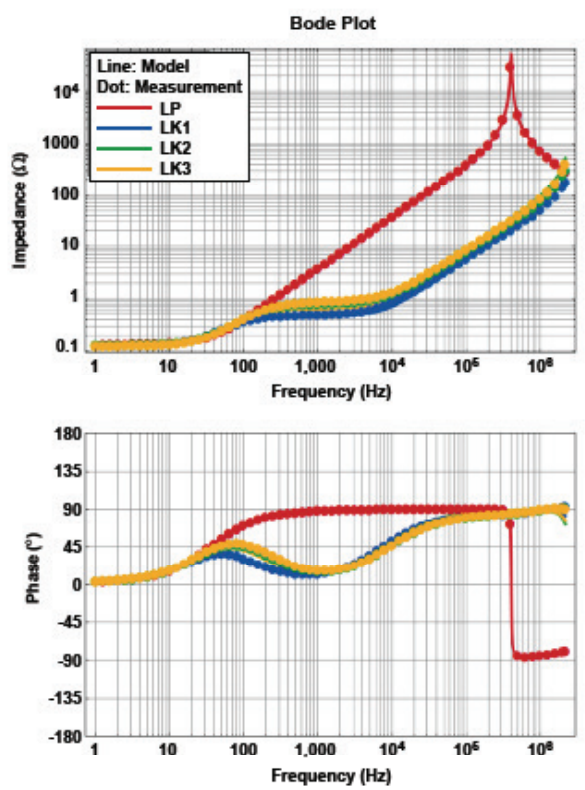

Figure 20 – Measurement and model results with capacitance.

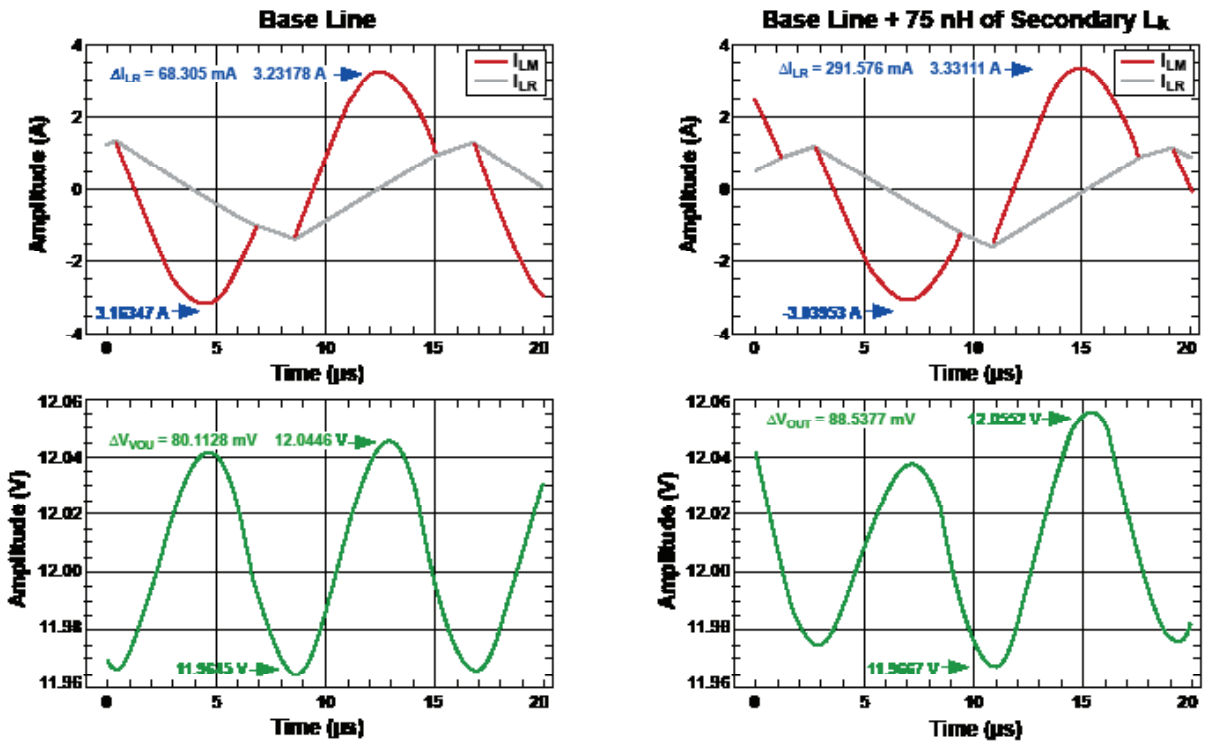

Figure 21 – Large-signal impact of leakage.

F. Design Impacts

Given the need for a series-inductance term in the LLC converter to regulate the output, it is generally acknowledged that some primary to secondary leakage inductance is beneficial to the system. In fact, if this inductance is properly sized, it can even eliminate the need for an external inductor.

Although this leakage term is valuable, leakage between the tertiary windings can be problematic to the design. Adverse effects can be introduced that compromise power-supply performance, including higher-voltage synchronous rectifiers, increased RMS currents, larger-output ripple voltage, and the potential to alter the steady-state and small-signal operating characteristics.

Figure 21 illustrates part of the impact of this leakage. The plots on the left show the resonant inductor current and the output voltage ripple for the transformer characterized by the data in Table 2. In general, the waveforms are very symmetric, having minimal ripple and RMS current values. The plots on the right show the results with an additional 75 nH of inductance introduced between the two tertiary windings. This inductance increases the output ripple voltage by approximately 10 percent.

We can make several additional observations directly from the model shown previously in Figure 13.

- $l_{23} = 0\,H$
  - No additional synchronous rectifier stress
  - Everything is symmetrical – minimal ripple and RMS currents
- $(\infty\,H > l_{23} > 0\,H) \wedge (l_{12} = l_{13})$
  - Synchronous rectifier voltage stresses can still be significant
  - Everything is symmetrical – minimal ripple and RMS currents
- $l_{23} \rightarrow \infty\,H$ – Worse case
  - Maximum stress on the synchronous rectifiers
  - Ripple
  - $l_{12} = l_{13}$, symmetrical – minimal ripple and RMS currents
  - $l_{12} > l_{13}$, asymmetrical
  - $l_{12} < l_{13}$, asymmetrical

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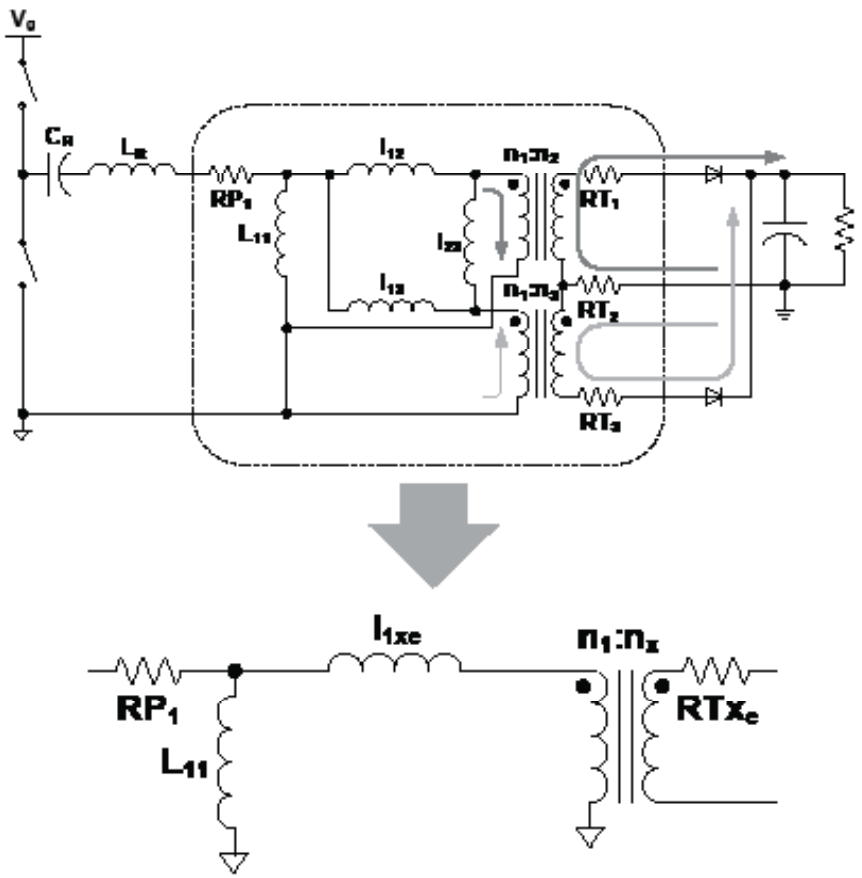

Figure 22 – Piecewise linear transformer model.

If you neglect the MOSFET and rectifier transition times, it's possible to make a significant conceptual and computational simplification to the model. Since only one of the secondary rectifiers conducts at a time, the transformer model can be simplified into two piecewise linear models for each diode conduction state. Figure 22 shows this transformation.

The piecewise linear model has the equivalent values shown in Equations 22 to 25.

$$l_{12e} = l_{12} \parallel (l_{13} + l_{23}) \tag{22}$$

$$l_{13e} = (l_{12} + l_{23}) \parallel l_{13} \tag{23}$$

$$R_{T1e} = R_{T1} + R_{T2} \tag{24}$$

$$R_{T2e} = R_{T2} + R_{T3} \tag{25}$$

This information can be further analyzed to directly calculate the resonant period of each half-cycle of conduction, as shown by Equations 26 and 27.

$$f_{c1} \approx \frac{1}{2\pi\sqrt{(L_R - l_{12e})C_R}} \tag{26}$$

$$f_{c2} \approx \frac{1}{2\pi\sqrt{(L_R - l_{13e})C_R}} \tag{27}$$

G. Design Considerations

As a final step in the transformer analysis, you must consider how these leakage inductances function relative to winding placement. Figure 23 shows a simple transformer bobbin and cross-section. In this example, the primary is constructed of round copper wire in the center of the structure. There are two tertiary windings constructed of copper foil. In all cases, each individual wire represents a single turn on the transformer.

To the right of the bobbin and wire cross-section is an expanded view of the transformer windings while conducting current. A dot indicates that current is flowing out of the page, while an "x" indicates that current is flowing into the page. In this example, the dark gray tertiary is conducting.

The magnetomotive force (MMF) drawing in the upper-right corner illustrates the leakage inductance that exists between layers. This plot is generated by drawing a box that starts in the center of the windings and expands outward. The sum of the current inside of this box is equal to the MMF at that particular location.

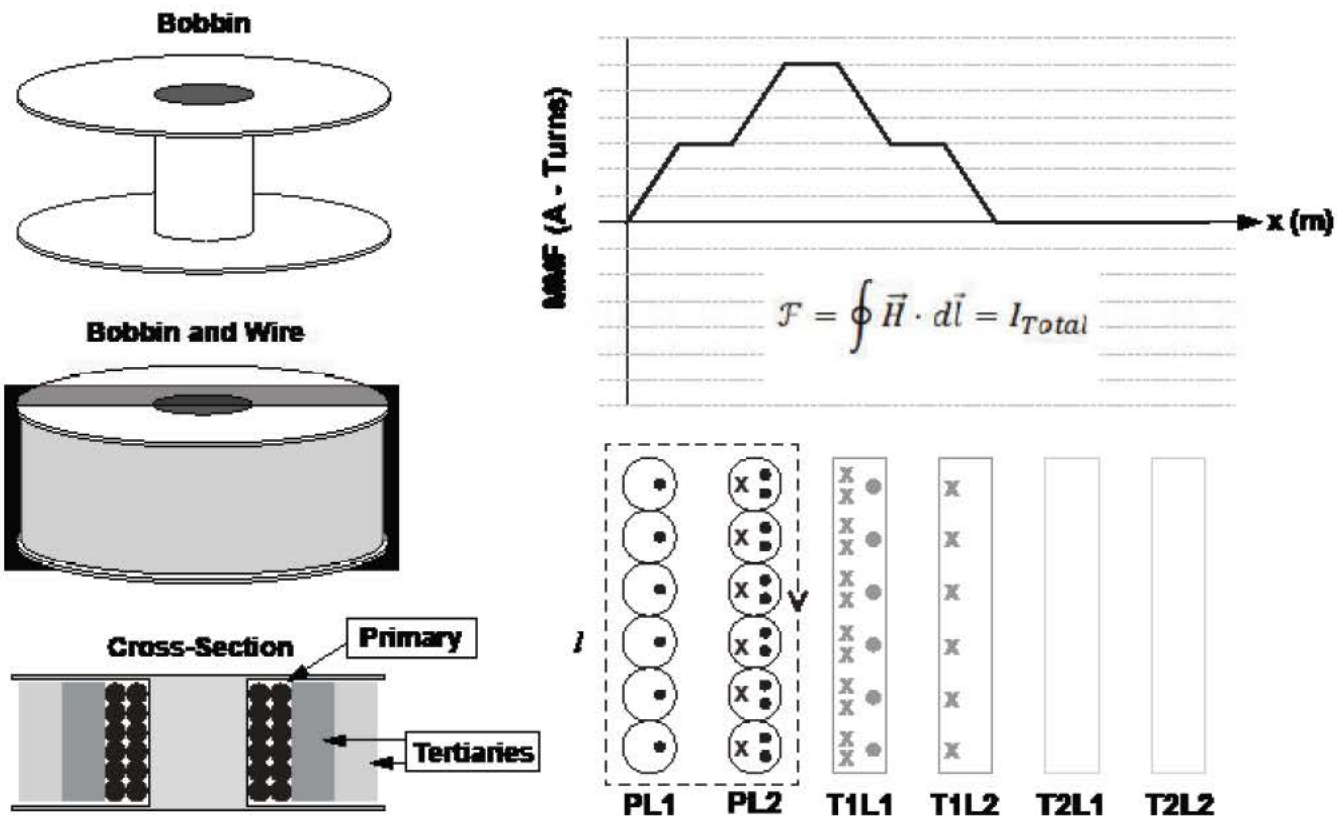

Figure 23 – Transformer winding analysis.

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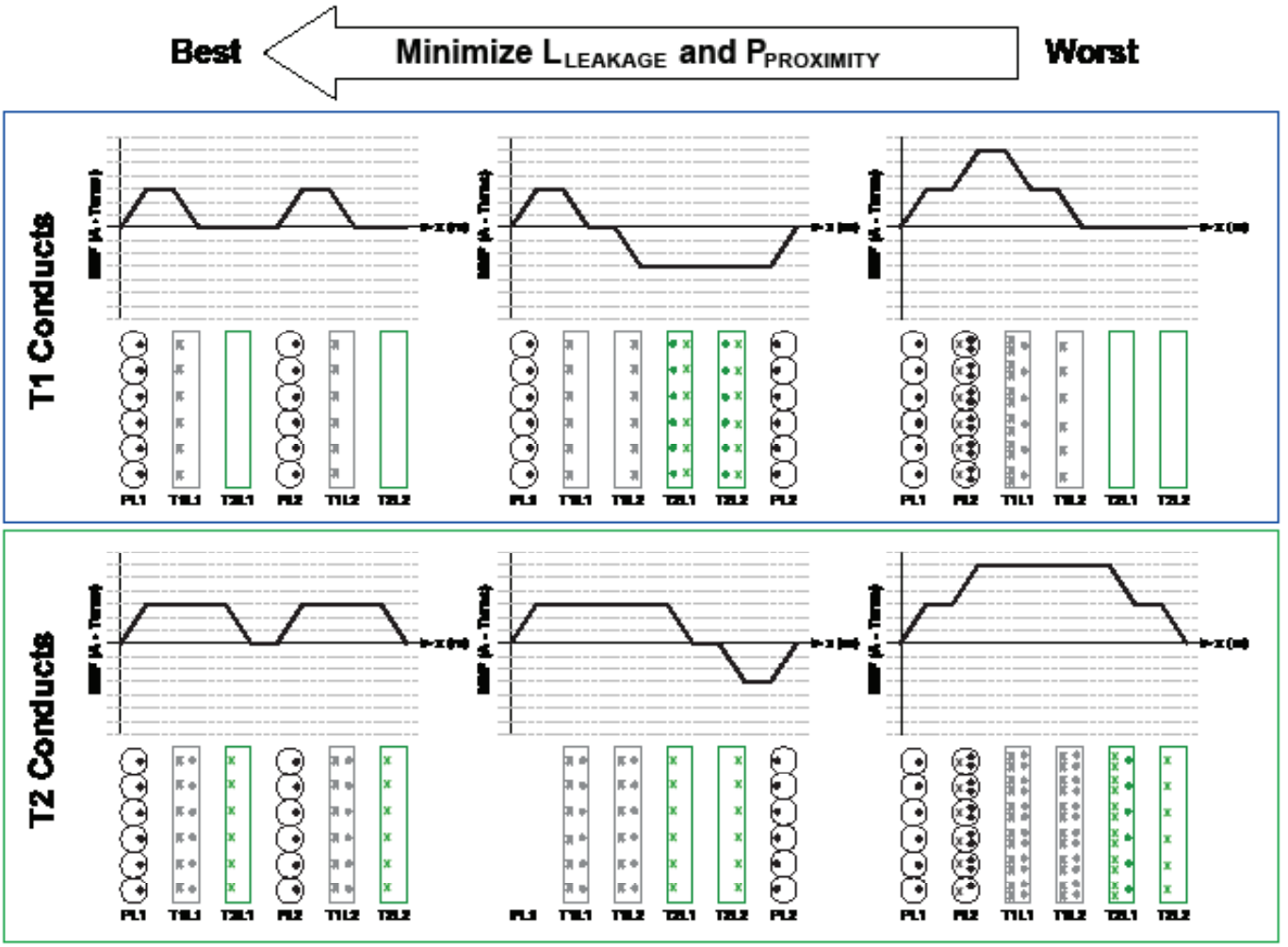

Figure 24 – Transformer winding strategy.

Figure 24 applies this same analysis to three different interleaving strategies for conduction in both T1 and T2. When the windings are fully interleaved, the area under the MMF functions is minimized. It is also important to note that the MMF levels are not the same when T1 conducts versus T2. Minimizing the MMF results in lower leakage and reduced losses due to proximity effect.

IV. PWM Methods for Optimized Performance

A. Problem No. 1: High fs

While an LLC converter offers a variety of advantages, there are several performance features that are more difficult to achieve than when designing with its buck-derived counterparts. First, requirements for light load, high input voltage or low output voltage require the converter to operate at high switching frequencies (see Figure 9 for details). These operating points can introduce additional switching losses; introduce regulation problems [5]; make soft start difficult; and even prevent operation in constant current, constant power or short circuit.

The fundamentals of steady-state operation were covered in section II-A. In this context, Figure 25 illustrates the exact timing relationships between the primary-side MOSFET control signals and the synchronous-rectifier control signals.

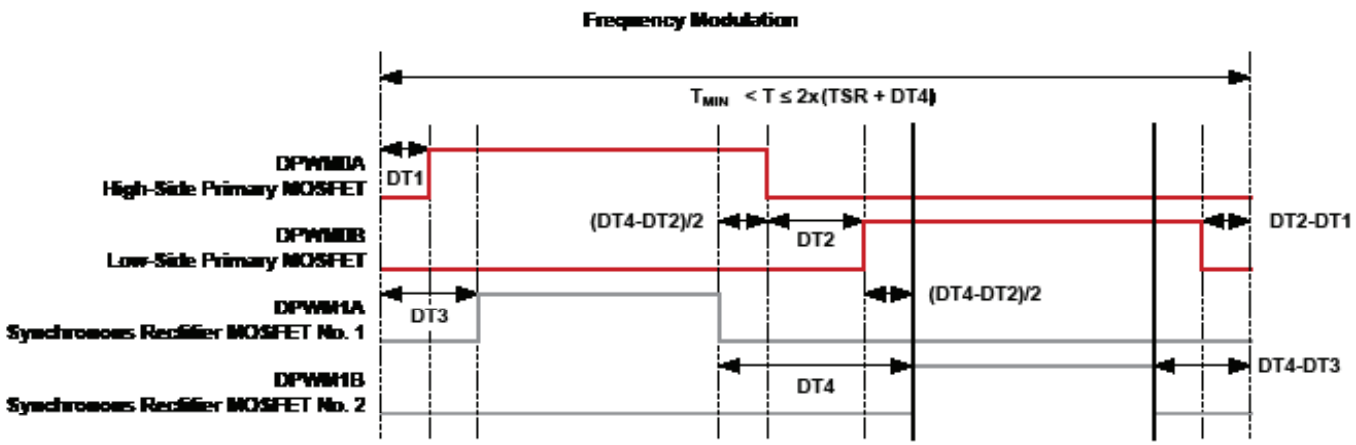

Figure 25 – Frequency modulation.

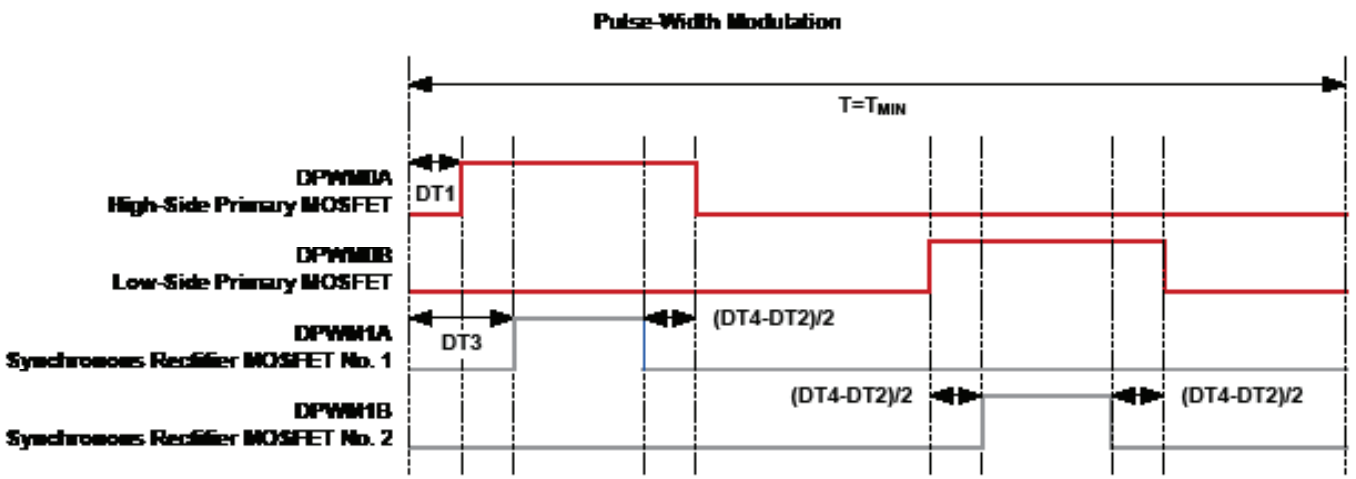

Figure 26 – Pulse-width modulation.

As an alternative to continuing to raise the switching frequency, it is possible to seamlessly switch modulation from frequency to pulse width. The PWM control signals are shown in Figure 26.

Notice that when the FM control frequency is equal to the PWM frequency, these waveforms are identical. This facilitates a perfectly smooth handoff between FM and PWM operation. Figure 27 illustrates this handoff during a typically soft start cycle. Notice the smooth, monotonic output voltage through the entire operation.

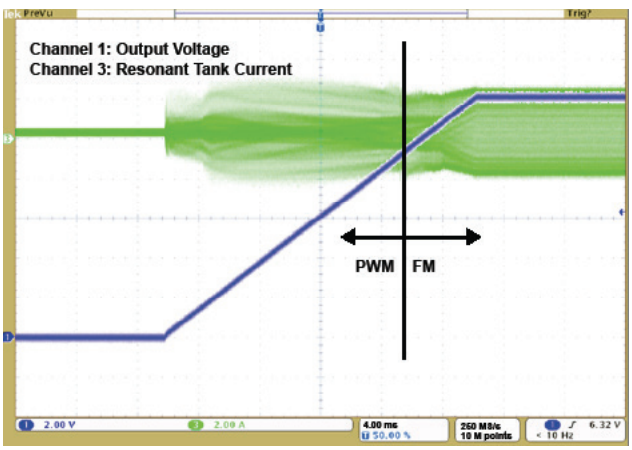

Figure 27 – Soft start.

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As another example, consider overload operation where the control transitions from constant voltage to constant power and constant current. Figure 28 shows the measured output voltage of the converter as it transitions through these three operating regions.

B. Problem No. 2: Synchronous Rectification

A second challenge is synchronous rectification. The timing of a properly diode-emulated synchronous rectifier does not follow the primary MOSFET control signal. Traditionally, you can solve this problem by using some kind of current-sensing circuitry to determine when the synchronous rectifier should be on and off. As an alternative, a programmable pulse-width clamp is placed on the synchronous-rectifier pulse width. If the width of this pulse is approximately equal to one-half the natural resonant period, you will get a very good approximation of an emulated diode. Figures 29 and 30 illustrate this relationship for a variety of input-voltage and load-current conditions.

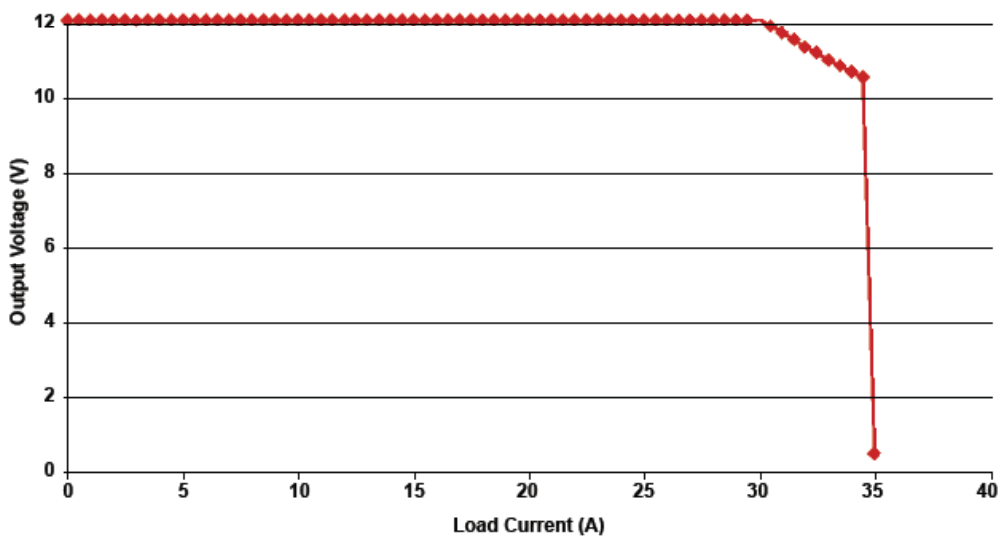

Figure 28 – Constant current constant power.

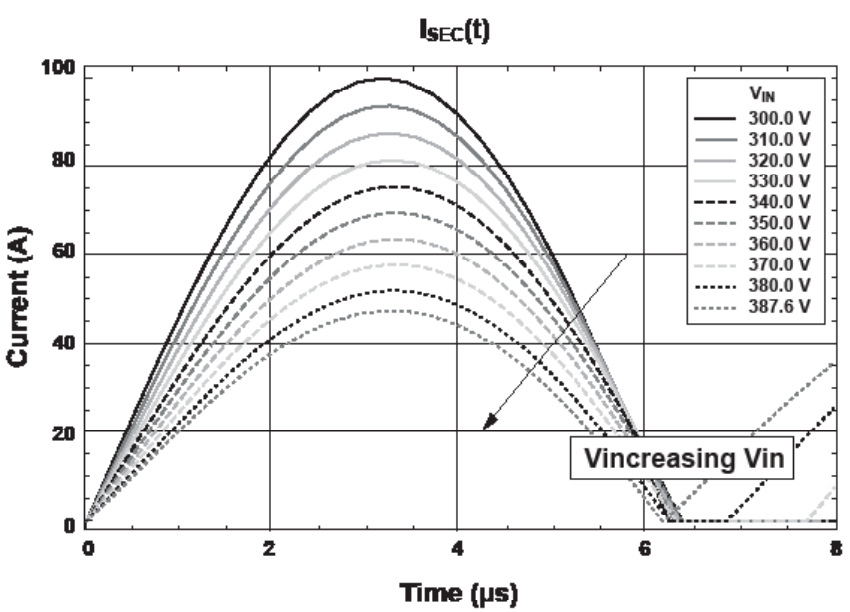

Figure 29 – Synchronous rectifier current and input voltage.

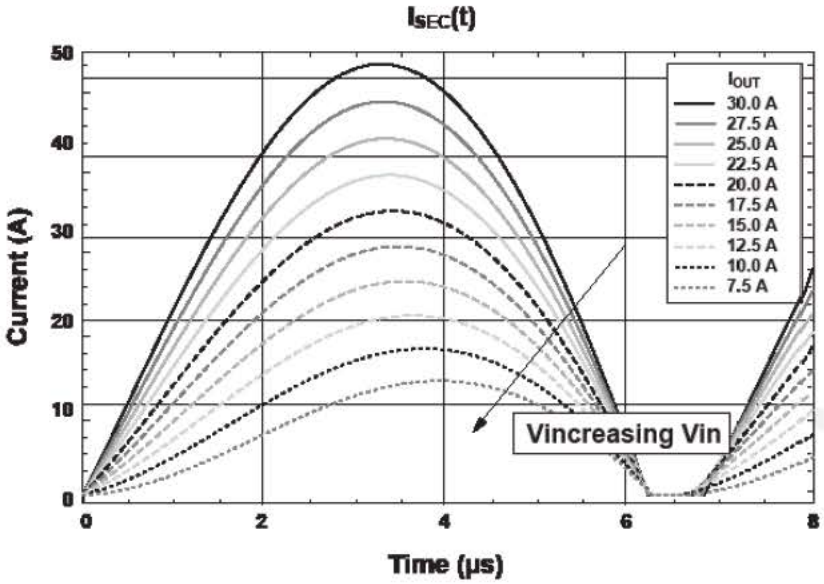

Figure 30 – Synchronous rectifier current and load current.

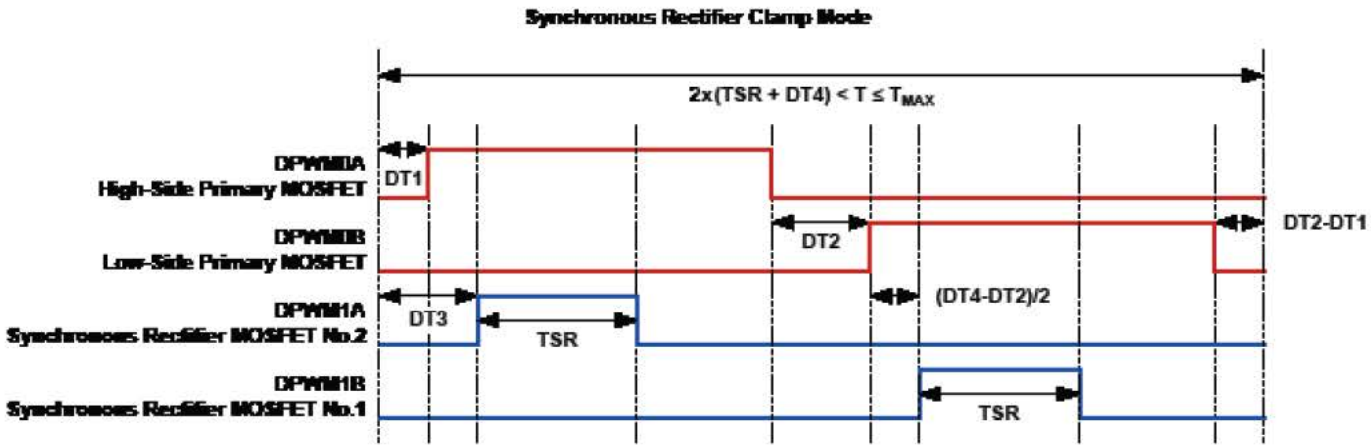

Figure 31 – Synchronous rectifier clamp mode.

Figure 31 illustrates the MOSFET control signals for this operating mode. The synchronous rectifiers simply follow the primary MOSFET signal (minus dead times) until the pulse width is longer than the preprogrammed clamp value. Once this happens, frequency adjustments continue to occur on all channels; however, only the primary MOSFET control signals maintain their duty-cycle ratio of ~50 percent.

Figures 32, 33 and 34 illustrate this feature in action. Using the schematic in Figure 1 as a reference, the following legend applies to all three plots:

Channel 1: Q3 V_{DS}
Channel 2: Q4 V_{DS}
Channel 3: I_{LR}
Channel 4: Q2 V_{DS}

Notice that in all cases, the body-diode conduction time across the synchronous rectifiers is very close to the minimum.

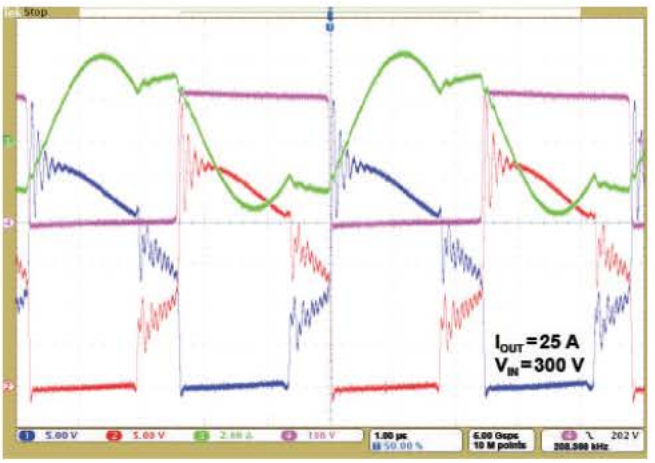

Figure 32 – V_{IN} = 300 V, I_{OUT} = 25 A.

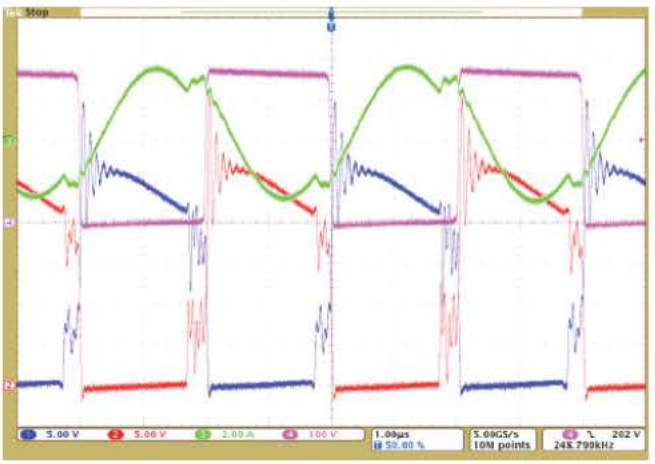

Figure 33 – V_{IN} = 350 V, I_{OUT} = 25 A.

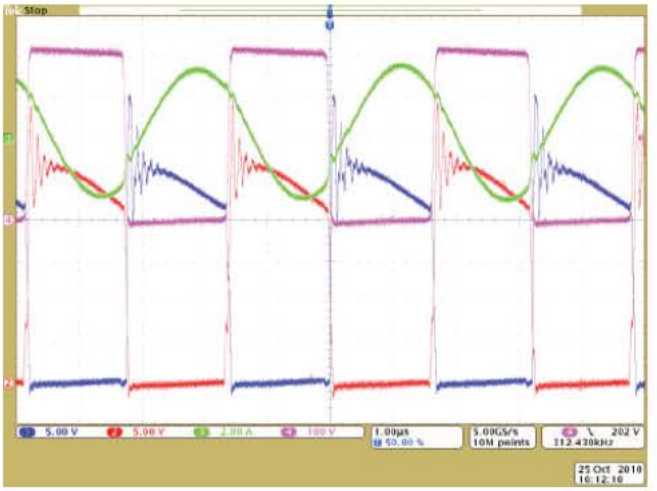

Figure 34 – V_{IN} = 400 V, I_{OUT} = 25 A.

C. Problem No. 3: Light Load Efficiency

Lastly, light load losses can become prohibitive due to the high switching frequency required to maintain regulation at low output currents. Figure 35 shows the power losses as a function of load current. The triangle represents the energy saved by employing a burst-mode algorithm to turn the MOSFET control signals on and off at a lower frequency.

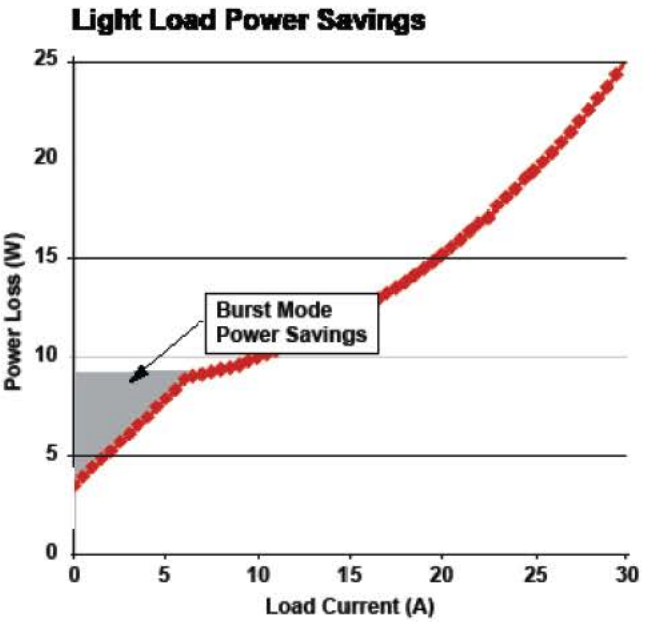

Figure 35 – Burst-mode power savings.

Figure 36 illustrates the algorithm. The compensator control effort is used as a crude indication of the load current. When this signal drops below a programmed threshold (labeled "Turn Off Threshold"), all of the MOSFET control signals are turned off. When it rises above a second programmed threshold (labeled "Turn On Threshold"), they turn on again.

Since the compensator control effort is only a crude representation of the load, some additional adjustment of the on/off thresholds is necessary as the input voltage varies.

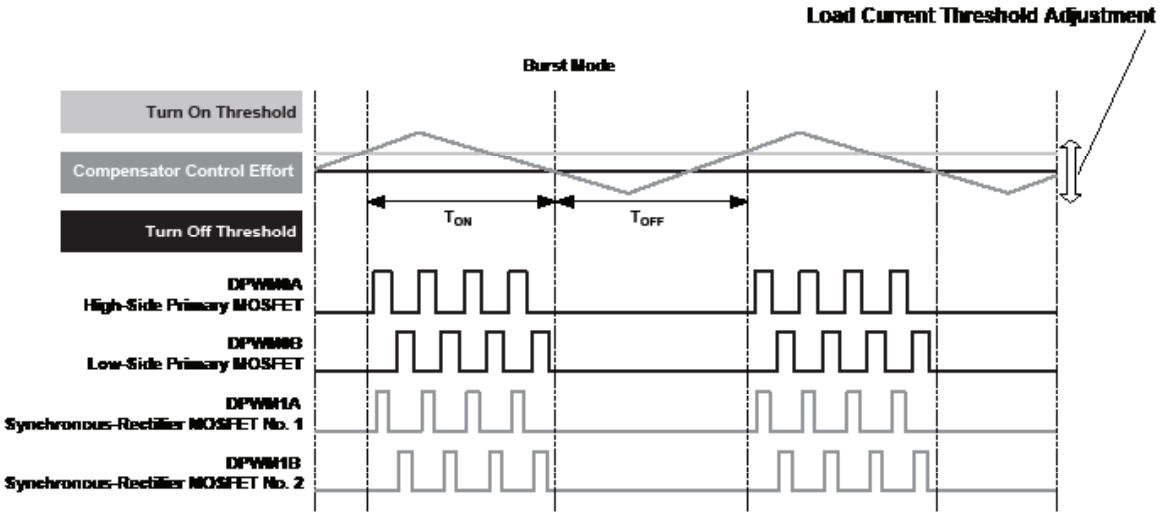

Figure 36 – Burst-mode algorithm

V. Conclusion

Figure 37 shows a picture of the completed evaluation module (EVM), while Figure 38 shows the corresponding efficiency of this converter.

Figure 37 – LLC EVM.

This EVM incorporates all of the features described in this paper, enabling a solution that provides competitive efficiency while maintaining the classic high-performance features designers are accustomed to using in buck-derived topologies.

The heart of this system uses a Texas Instruments UCD3138 digital controller. This facilitated easy optimization and evaluation of the various control features discussed in Section IV. The digital core of the UCD3138 also provided an efficient solution to the mode-switching problems while maintaining a minimum component count.

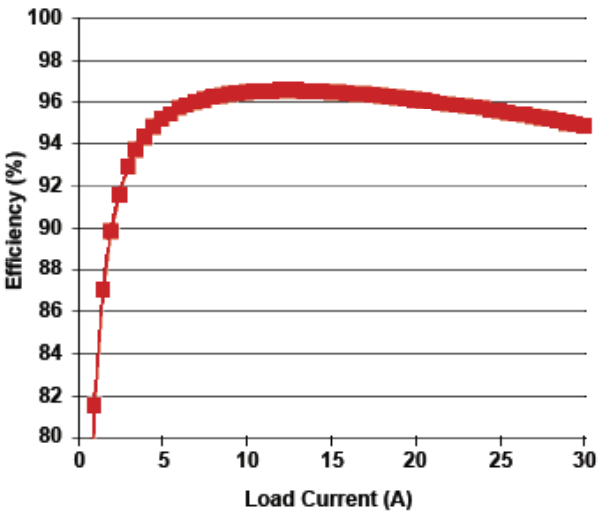

Figure 38 – LLC EVM efficiency.

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