

Voltage Divider and its Application in the Two-stage Power Architecture

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Abstract –An ultra-high power density DC/DC converter with fixed conversion ratio is proposed for the two-stage power architecture in the area of power management for the processor based power systems, including server, desktop, laptop, and other battery powered portable applications. Without the magnetic component inside, its power density has been scaled up by an order over the conventional approach. In addition, it also features the capability of holding ultra-high efficiency within whole load range, which is promising to the battery life extension in the laptop. 1kw/inch³ power density and 98% efficiency have been demonstrated in 120W and 60W DC/DC prototypes designed for two-stage VRs.

I. INTRODUCTION

Future generation microprocessors are expected to operate at much lower voltages (0.7-1V), to draw much higher currents (130A as shown in Fig.1) with high di/dt dynamic characteristics (20A/ns). Accordingly, voltage regulator (VR) will have to meet increasing challenges such as higher conversion efficiency, tighter voltage tolerances, and faster transient responses.

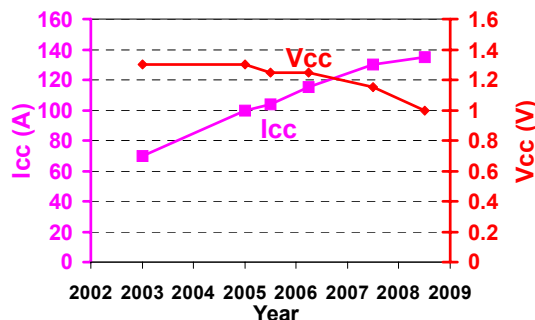


Figure 1. The microprocessor voltage and current roadmap

Current power management solution can no longer satisfy the future requirements. The excessive interconnect parasitics between the VR and the CPU limits the transient performance and efficiency. Furthermore, the limited control bandwidth of the VR is compromised with increasing usage of output capacitors for energy storage. Without fundamental change of

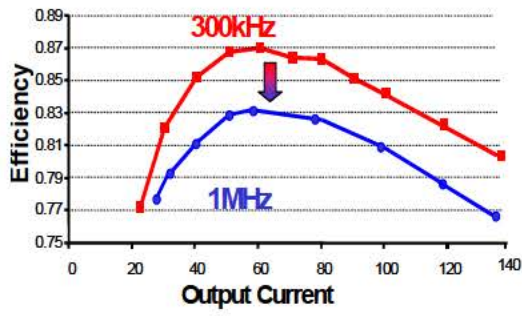
today's power delivery architecture, it is expected that the output capacitors will increase drastically [1].

To reduce the excessive usage of capacitors, the bandwidth of the VR must be increased. Assuming $f_c = 1/6 \cdot f_s$, when the switching frequency of VR is increased to 1.2MHz, the bulk capacitors could be switched from aluminum electrolytic capacitor to ceramic without added cost, yet with much smaller footprint. At 2MHz switching frequency (350kHz bandwidth), the bulk capacitors can be completely eliminated, which means a 30% of cost reduction of VR and smaller foot-print on the real estate of motherboard [1].

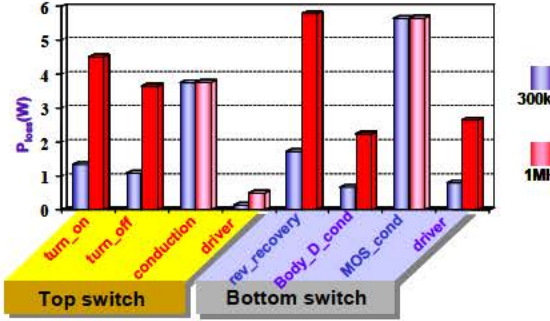
The state-of-the-art VR design is based on the single stage multi-phase buck converter. The VR is operated at around 300KHz and the control bandwidth is designed around 50KHz. According to the aforementioned discussion, the switching frequency should be increased to reduce the output capacitance. However, the efficiency of today's single stage suffers at higher switching frequencies as shown in Figure 2(a). The major loss factors are the switching losses and the body diode losses (shown in Figure 2(b)). If the input voltage of the multi-phase VR is operated as a low voltage, the VR efficiency can be improved. A two-stage approach shown in Figure 3 is proposed in [2]. The first stage can be designed at relatively low switching frequency to step down the input voltage from 12V to around 5V. With the lower input voltage, the switching loss and reverse recovery loss of the second stage, which are proportional to the input voltage, are dramatically reduced. Therefore, it was demonstrated that the second stage switching frequency can be pushed to 2MHz to achieve 350kHz bandwidth at 83% efficiency [2]. This two-stage concept can also be applied into the laptop for efficiency improvement and output capacitor reduction [3].

Buck converter was proposed for the first stage initially, as shown in Figure 3. It is assigned to run at low switching frequency, e.g. couple hundred KHz, to attain high efficiency. However, this low switching frequency makes the first stage in large size and counteracts the real estate saving from the high frequency second stage. Figure 4 shows two different VR designs in the two-stage approach. One is the version for desktop or laptop, the other is the VRM version for server. It can be easily seen that the first stage has the similar size as the second stage. Detailed analysis reveals that two-stage approach with the first stage structure in Figure 3 can not bring us too

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(a) Much lower efficiency at 1MHz



(b) Loss breakdown comparison

Figure 2. The suffered efficiency of single stage 12V VR at higher switching frequency

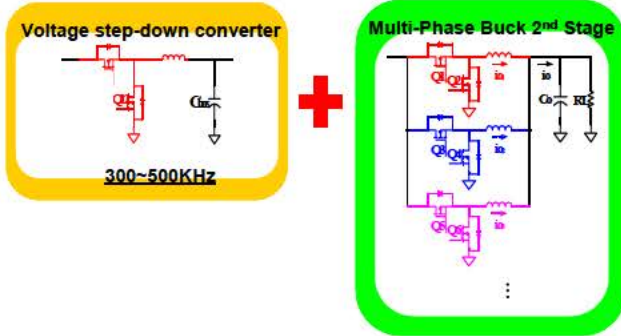


Figure 3. The structure of the two-stage approach in [2]

much benefit on the overall size reduction. This issue obstructs the two-stage approach from those density-sensitive applications, such as the laptop VR or VRM for server.

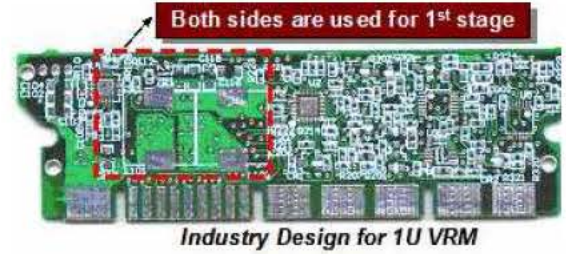
To solve this issue, a magnetic-less DC/DC converter is developed. Because no magnetic component is required, it can substantially boost the power density of the first stage. Furthermore, by leaving the voltage regulation to the second stage, proposed DC/DC converter for the first stage with fixed 2:1 conversion ratio, named Voltage Divider, can achieve as high as 98% efficiency with 12V or even higher input voltage in whole load range.

II. PROPOSED VOLTAGE DIVIDER AND OPERATION PRINCIPLE

Figure 5 shows the circuit diagram and control strategy of proposed voltage divider. Its operation principle is sketched below intuitively:



(a) 120W two-stage VR for desktop



Industry Design for 1U VRM

(b) 130W two-stage VRM for server

Figure 4. Two VR designs with two-stage approach

During $t_0 \sim t_1$: Q_1 and Q_3 are off, and Q_2 and Q_4 are on. Load current I_o charges the top capacitor C_1 and discharges the bottom capacitor C_3 and the flying capacitor C_2 .

During $t_1 \sim t_2$: Q_1 and Q_3 are turned on, and Q_2 and Q_4 are turned off. C_2 is paralleled with C_1 through Q_1 and Q_3 . Due to their voltage discrepancy, surge current occurs in the loop comprising Q_1 , Q_3 , C_1 and C_2 . Some charges are transferred from C_1 to C_2 . The voltage difference and loop impedance determine the amplitude of the surge current, which balances the voltages of C_1 and C_2 .

During $t_2 \sim t_3$: Q_2 and Q_4 are off, and Q_1 and Q_3 are on. Load current I_o charges the top capacitor C_1 and the flying capacitor C_2 while continuously discharging the bottom capacitor C_3 .

During $t_3 \sim t_4$: Q_2 and Q_4 are turned on, and Q_1 and Q_3 are turned off. C_2 is put back with C_3 through Q_2 and Q_4 . Due to their voltage discrepancy, surge current occurs in the loop comprising Q_2 , Q_4 , C_2 and C_3 . Some charges (or certain energy) brought from C_1 by C_2 are transferred to C_3 . As preceding explanation, this energy transferring induces a surge current which makes the voltage across C_2 and C_3 equal.

Comparing to the Buck DC/DC converter, the proposed circuit has following advantages in terms of efficiency:

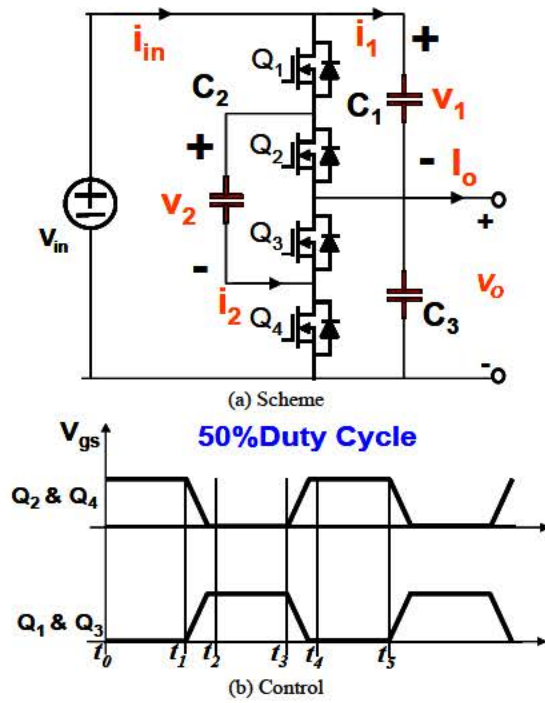


Figure 5. Proposed voltage divider and its control

1. Unlike Buck converter, turn-on loss of this circuit is independent upon the switching speed of the device but the voltage different between two capacitors being paralleled.
2. All switches can be turned off in zero voltage condition as long as the voltages of two capacitors have been balanced before they are separated by the switches' turn-off.
3. No body diode conduction losses. Because there is no inductor as well as its current freewheeling, the body diode of device will not conduct during the dead time which is normally reserved in the gate driver to avoid the short-through among the switches in the totem-pole structure.

It should be mentioned that, due to feature (1) and (2), there is no stringent parasitic requirement and excessive demand on gate driving for the devices. As a result, we can use cheap devices and drivers (or driving transformers) to lower down the cost.

III. DESIGN GUIDELINE FOR THE PROPOSED VOLTAGE DIVIDER

1. Circuit analysis

Assume the ESR for all capacitors is much lower than the on resistance of MOSFET.

RMS current on C_2 can be derived as:

$$I_{2RMS} = C_2 \sqrt{B^2 + \frac{4AB(e^{-T_s/(2\tau)} - 1) - \frac{A^2}{\tau}(e^{-T_s/\tau} - 1)}{T_s}} \quad (1)$$

where, T_s is switching period and A,B,C are:

$$A = \frac{I_o T_s}{2C_2} - \frac{I_o T_s}{2(C_1 + C_2 + C_3)} \frac{e^{-T_s/(2\tau)} - 1}{e^{-T_s/(2\tau)} - 1}$$

$$B = \frac{I_o}{C_1 + C_2 + C_3}$$

$$\tau = R \cdot \frac{(C_1 + C_3)C_2}{C_1 + C_2 + C_3} \quad (2)$$

where, $R = 2R_{dson}$. R_{dson} is the on resistance of each MOSFET.

RMS current on each MOSFET is:

$$I_{QRMS} = I_{2RMS} / \sqrt{2} \quad (3)$$

To normalize Eq.(1), we define:

$$I_{2N} = I_{2RMS} / I_o$$

$$\tau_N = \tau / T_s$$

$$k_N = C_2 / (C_1 + C_3) \quad (4)$$

Substitute (4) into (1), the normalized RMS current on C_2 can be expressed as:

$$I_{2N} = \sqrt{\frac{k_N(2+k_N)}{(1+k_N)^2} + \frac{[0.5/(1+k_N)]^2}{\tau_N} \frac{e^{-1/\tau_N} - 1}{(e^{-0.5/\tau_N} - 1)^2}} \quad (5)$$

Because the average current of C_1 and C_3 are zero, output DC current has to be equal to the sum of the currents of Q_2 and Q_3 . It can be easily seen that the current of C_2 is rectified by Q_2 and Q_3 as the DC output current. Therefore,

$$|I_2|_{avg} = I_o \quad (6)$$

Due to the charge balance of C_2 , the positive area of the current of C_2 should be equal to its negative area. With Equation (6), the average amplitude of either positive or negative current pulse should be I_o . It is known Q_1 conducts the positive current pulse of C_2 in 50% duty cycle, so the average input current should be:

$$I_{in} = I_o / 2 \quad (7)$$

Based on the conservation of energy, the output voltage can be calculated with:

$$V_o = \frac{V_{in}}{2} - \frac{I_{2rms}^2 R + P_{sw}}{I_o} \quad (8)$$

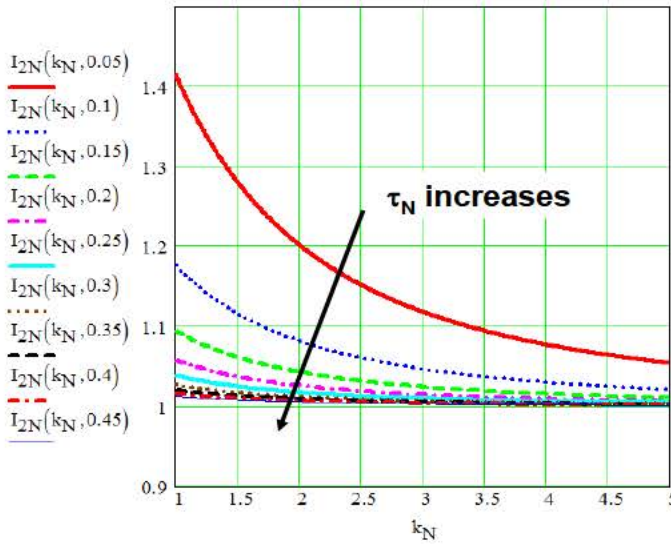
where, P_{sw} is the total switching related loss, which could be controlled to tiny level by appropriate capacitor design [4].

2. Selection on C_1 , C_2 and C_3

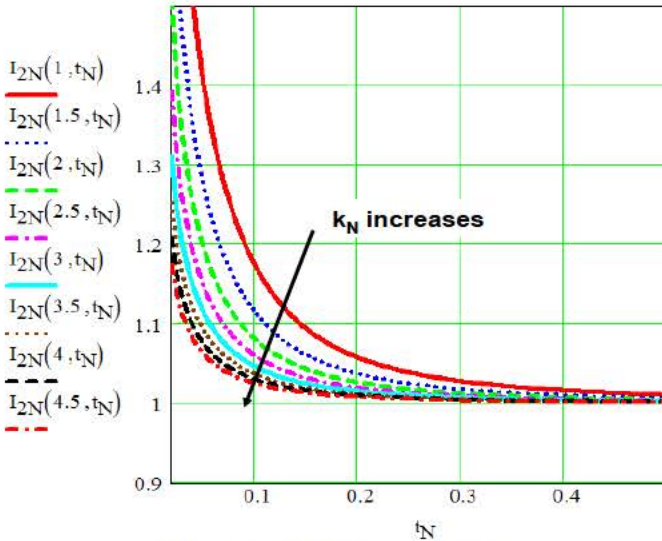
Since the switching related losses of the proposed voltage divide can be small enough to be ignored, MOSFET conduction losses are the only concern for the efficiency in this section. Equation (3) clearly shows that the RMS current on C_2 determines the conduction losses. From Equation (5), Figure 5 and Figure 6 show the relationship of I_{2N} with k_N and τ_N . It is clearly shown that either larger k_N or larger τ_N leads to lower RMS current. If k_N and τ_N are determined, C_2 and C_1+C_3 can be determined as follows:

$$C_2 = \frac{\tau_N(k_N+1)T_s}{R}$$

$$C_1 + C_3 = \frac{\tau_N(k_N+1)T_s}{k_N R} \quad (9)$$



(a) Normalized C_2 RMS current I_{2N} vs. k_N



(b) Normalized C_2 RMS current I_{2N} vs. τ_N

Figure 6. RMS current vs. k_N and τ_N

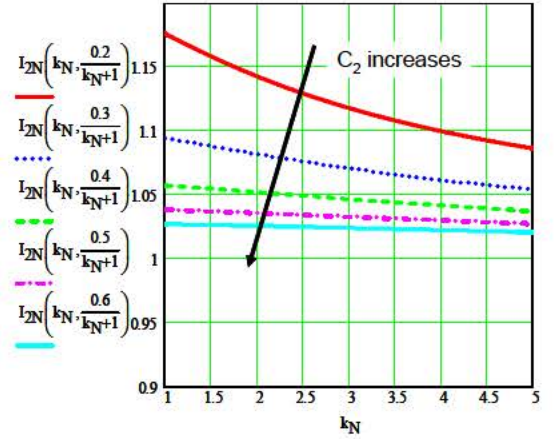


Figure 7. RMS current vs. k_N for different C_2

From Equation (9), both of k_N and τ_N are preferred to be large, whereas large k_N and τ_N require large capacitors for C_1 through C_3 , large footprint and high cost as well. The trade-off between the RMS current of C_2 and total capacitance can be done in two ways: one is large k_N and low τ_N , the other is low k_N and large τ_N . Both of them can set the RMS current in the vicinity of the minimum value.

Given a $(k_N+1)*\tau_N$, C_2 can be determined by Equation (9). Figure 7 clearly shows how the RMS current C_2 is impacted by k_N for a given C_2 . Large C_2 can greatly diminish the effect of the k_N on the RMS current. Consequently, C_2 is proposed to be designed firstly with large enough capacitance for high efficiency. After that, C_1+C_3 can be determined with other considerations.

Normally C_1 and C_3 can be selected with the consideration of output voltage ripple and input AC current. Figure 8(a) shows an example of the influence of the C_1+C_3 on the output voltage ripple. A proper C_1+C_3 should be selected to meet the ripple requirement. Figure 8(b) shows an example of the influence of C_1 on the input AC RMS current. An optimal C_1 will give the lowest input AC current.

For better understanding, a design example is shown as below.

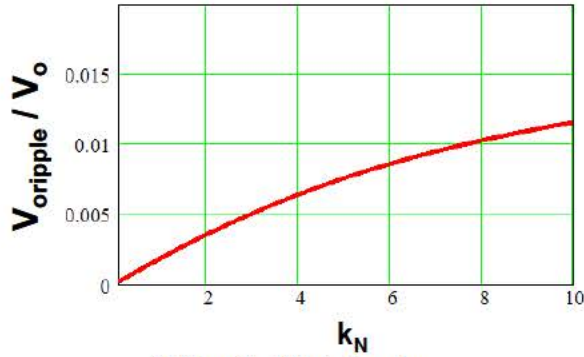
Circuit configuration: $V_{in}=12V$, $I_{omax}=10A$, $R=5m\Omega$ (Device: Si7858ADP), $f_s=350kHz$.

Firstly, $k_N=1.2$, $\tau_N=0.15$ are determined to achieve low RMS current and output ripple. From Equation (9), C_2 is equal to $130\mu F$, and C_1+C_3 is $90\mu F$. To achieve the lowest input AC current, $C_1=45\mu F$. Then $C_3=45\mu F$

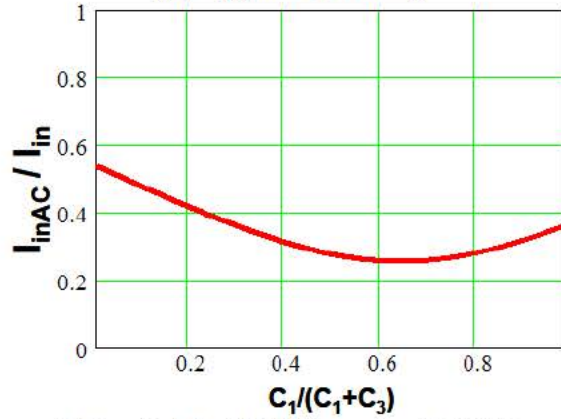
Finally the RMS current on each capacitor should be checked to decide how many capacitors must be paralleled to satisfy the current rating requirement of each capacitor. Based on calculation, the maximum RMS current for the three capacitors are:

$$I_{1RMS} = 3A, I_{2RMS} = 11A, I_{3RMS} = 3A$$

Generally, the low ESR capacitors such as Multi-layer ceramic capacitor (MLCC) are preferred for the proposed voltage divider, which can reduce the power losses on the capacitors. Each 22 μ F TDK ceramic capacitor has 2A RMS current capability. Two paralleled 22 μ F capacitors are used for C1 or C3. For C2, six paralleled 22 μ F capacitors are needed.



(a) Normalized Vo ripple vs. k_N
 $((k_N+1)\tau_N=0.35, I_o=12A)$



(b) Normalized Input AC RMS current vs. $C_1/(C_1+C_3)$
 $(k_N=1.2, \tau_N=0.14, I_o=12A, I_{in}=6A)$

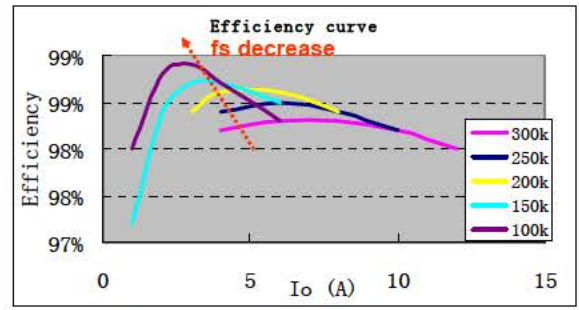
Fig. 8. Output ripple and input AC current vs. C_1 and C_3

IV. LIGHT LOAD EFFICIENCY AND GATE DRIVING METHOD

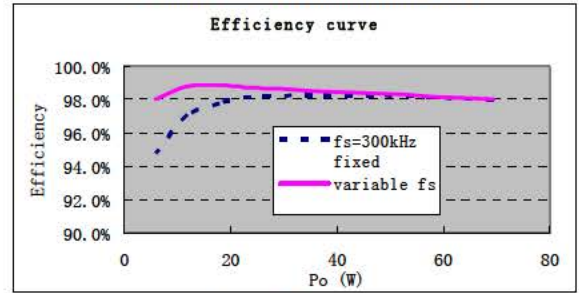
1. Light load efficiency

After the capacitor design is finished, τ and k_N are determined. Then $\tau_N = \tau/T_s = \tau \cdot f_s$ is proportional to the switching frequency. Figure 6 shows the lower τ_N , the higher C_2 RMS current. It means, for a given load current, lower frequency means higher conduction loss. So at heavy load, higher frequency is needed. However, lower frequency also leads to lower gate driver loss, which normally is dominant loss at light load. Thus, lowering down switching frequency at light load can improve light load efficiency of the proposed voltage divider. Figure 9(a) shows a batch of efficiency curves at different frequencies. If peak efficiency points of those curves are connected, an optimal efficiency curve can be achieved by varying the switching frequency respecting the load current, as shown in Figure 9(b).

2. Gate driving method

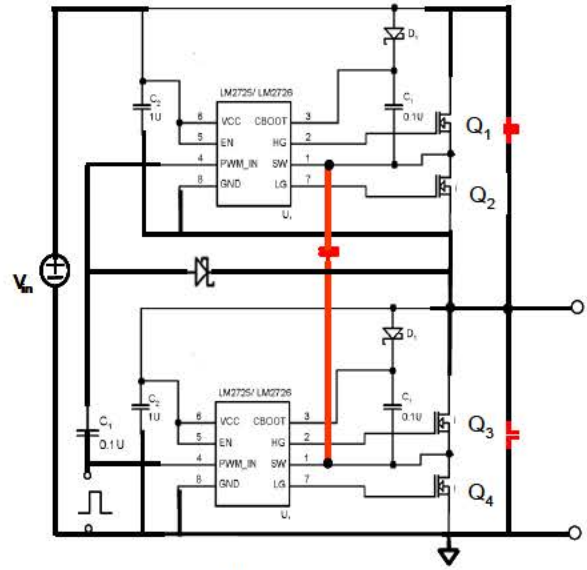


(a) Efficiency vs. I_o for different frequency

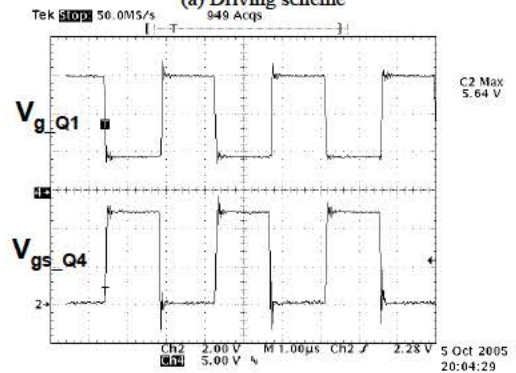


(b) Boost light load efficiency by lowering down f_s at light load

Fig. 9. Light load efficiency improvement for proposed VD



(a) Driving scheme



(b) Tested gate signals

Figure 10. Proposed gate driving for VD

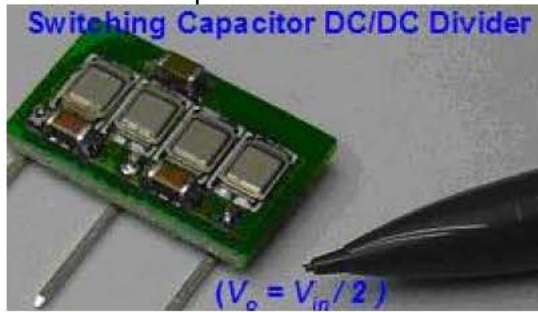
As aforementioned, there is no stringent demand on gate driving for the devices. As a result, the cost effective way of driving the devices is to use driving transformer. In low voltage applications, the commercial boost trap gate driver IC can be utilized for concise circuitry. Figure 10(a) shows the driving schematic. Two gate driver IC are used to drive the four MOSFETs. A boost trap scheme is used to get the PWM input signal for the upper two MOSFETs. The voltage on C_1 and C_3 can also be utilized as the voltage source of the gate driver respectively. Figure 10(b) shown the test gate signals for the proposed gate driving at $V_{in}=12V$ and $I_o=10A$. It shows the proposed gate driving works very well.

V. EXPERIMENTAL RESULTS

Two prototypes have been built. One is 12V input with 6V/20A output for desktop application. The other one is 12~16V input with 6~8V/8A output for laptop application. Both of the prototypes have achieved $1kw/inch^3$ power density. As an example, table 1 gives the component parameters. Different voltage rating devices are evaluated for this voltage divider.

Table 1. Parameters in the 60W Voltage Divider prototype:

Switching frequency	350KHz
Capacitance of C1, C2 and C3	C1, C3: 2 22uF MLCC/TDK C2: 6 22uF MLCC/TDK
Switches, Q1~Q4	30V device: Vishay SI7886ADP, 20V device: Vishay Si4864, 12V device: Vishay SI7858ADP
Driver	2x LM2726, National Semiconductor



(a) Prototype of 60W voltage divider

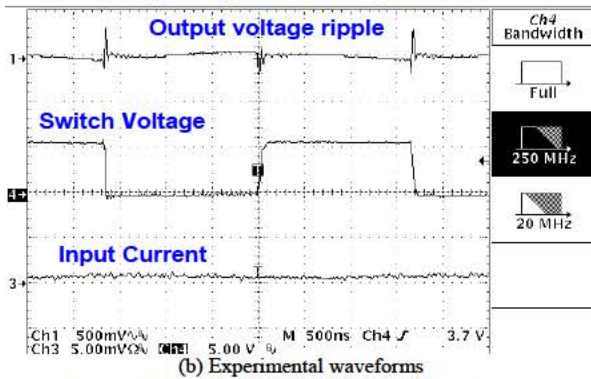
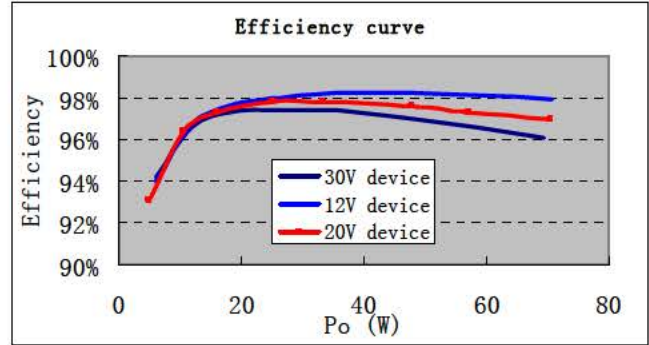
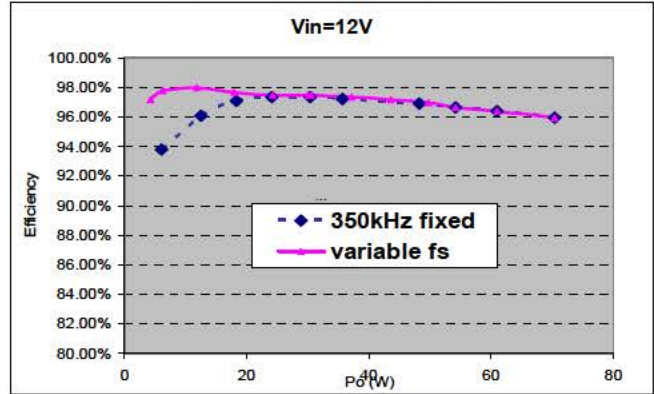


Figure 11. Prototype and experimental waveforms

Figure 11 shows the 60W prototype and its experimental waveforms. A pen is put aside in contrast with. The overall efficiencies and light load efficiency are given in Figure 12. It can be seen that lower voltage rating device can achieve higher efficiency. Figure13 compares the voltage divider with conventional Buck converter. The power density of the voltage divider is as high as $1kw/inch^3$, which is ten times of the conventional buck shown in the right hand side.



(a) Efficiencies with different devices



(b) Efficiencies with variable frequency

Figure 12. Experimental efficiencies

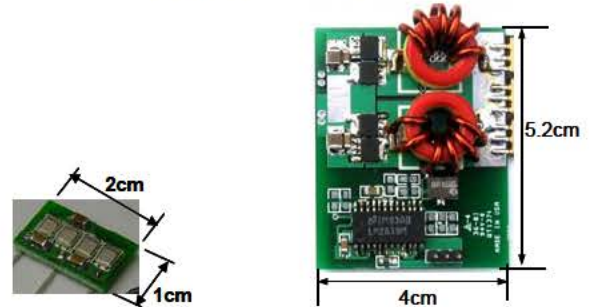


Figure 13. Size comparison between voltage divider and Buck

VI. CONCLUSION

A Voltage Divider DC/DC converter is proposed. Its ultra-high power density and efficiency in all load range make it promising to the two-stage power architecture. Theoretical analysis has been validated by the experiments. $1kw/inch^3$ power density and 98% efficiency have been realized in hardware.

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