RESONANT CONVERTERS: TOPOLOGIES, DYNAMIC MODELING AND CONTROL

By

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Malik Elsammany Elbuluk

Submitted to the Department of Electrical Engineering and Computer Science on September 22,1986 in partial fulfillment of the requirements for the degree of Doctor of Science in Electrical Engineering

ABSTRACT

Recent interest in high frequency resonant converters has prompted this exploration of aspects that have not previously been studied carefully. More specifically, this thesis examines possible methods for deriving resonant converter topologies and show how to develop dynamic models for converter behavior, demonstrates the design and implementation of control schemes based on these models.

Systematic methodologies for deriving resonant converter topologies are proposed. These allow the synthesis of existing and new converters. One method proposes a switching cell from which some basic topologies are derived. A second method uses the structural symmetry of resonant converters to derive other topologies. Duality is used to complete the set of resonant converter topologies obtained by the first two methods. Relationships between dual converters are discussed, drawing attention to the sort of implementation differences that arise.

Sampled-data models to describe the dynamics large signals and of small perturbations away from a cyclic steady state are developed. Associated transfer functions are obtained. Application of the model is illustrated by correlating the analysis with simulation results obtained for a series resonant dc-dc converter. The modeling technique used has also been generalized to include other power electronic circuits.

A discrete microprocessor-based controller designed using the above dynamic model has been built and tested on a simulation of a series resonant dc-dc converter, set up on MIT's Parity Simulator. The control methods implemented are state feedback and periodic output feedback, each designed to achieve a specified set of closed-loop poles. Two implementations of the controller have been tested, one using the the Parity Simulator Generalized Controller and the other using a Compupro microcomputer.

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Page 002

DEDICATED

TO

MY FAMILY

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Exhibit 1014
Page 004

TABLE OF CONTENTS

page

ABSTRACT 1

ACKNOWLEDGMENTS 2

LIST OF FIGURES 5

CHAPTER I : INTRODUCTION

(1) Background 10
(2) Goals Of This Thesis 11
(3) Thesis Overview 12

CHAPTER II : OVERVIEW OF RESONANT CONVERTERS

(1) Introduction 14
(2) Resonant Converters: Structure and Modes of Operation
  (A) Structure 15
  (B) Modes of Operation 24
(3) Conventional Resonant Converters
  (A) Voltage-fed resonant converters: overview 26
    (i) High power, high frequency applications 27
    (ii) Low power, high frequency applications 33
  (B) Current-fed resonant converters: overview 36
(4) Problems Presented by Conventional Converters
  (A) Limitation of thyristor turn-off time 39
  (B) Modification using time-sharing techniques
    (i) Time-sharing subunits..... 40
    (ii) Time-sharing techniques 43
      (a) Multi-winding transformer technique 45
      (b) Series-commutating capacitor technique .. 48
(5) Summary and Conclusions 48

CHAPTER III: SYNTHESIS OF RESONANT CONVERTERS

(1) Introduction 51
(2) Derivation of the Basic Topologies 51
  (A) The asymmetric topology 55
  (B) The symmetric topologies 57
  (C) Types of resonant loads 64
  (D) Power flow and switch implementation 69
(3) Parameters of Voltage-fed Converters
  (A) Series topologies 72
  (B) Parallel topologies 74
(4) Symmetry Derived Topologies 77
(5) Duality Considerations 87
(6) Current-fed Resonant Converters 91
(7) Summary and Conclusions 94

Appendix 3A: Synthesis of Power Converters using Linear Network Theory 96

InductEV, Inc.
Exhibit 1014
Page 005

CHAPTER IV: DYNAMIC MODELING OF RESONANT CONVERTERS

(1) Introduction 112
(2) Overview of Modeling in Power Electronics 112
(3) The Motivation to Model Resonant Converters 114
(4) Contribution of This Chapter 117
(5) The Voltage-Fed Series Resonant Converter
  (A) Description of the basic operation 118
  (B) Dynamic modeling
    (i) The state-space description 121
    (ii) Nonlinear large-signal sampled-data model 124
      (a) Half-cycle versus full-cycle model 127
    (iii) The cyclic steady state 130
    (iv) The perturbed state and the small-signal sampled-data model 131
    (v) Eigenvalues and frequency domain expressions 136
    (vi) Perturbation in the switching frequency 137
    (vii) Generalization of the model to other power electronic circuits 137
  (6) Results and discussion
    (A) Effects of the parity simulator parasitics 137
    (B) Results 138
  (7) Other Related Issues
    (A) Sensitivity analysis 143
    (B) Automatability 144

Appendix 4A Determination of the Steady State of the Series Resonant Converter 147

CHAPTER V : CONTROL OF RESONANT CONVERTERS

(1) Introduction 153
(2) Feedback Gain Calculation
  (A) State feedback 155
  (B) Periodic output feedback 157
(3) Effects of the Computer Delay 159
(4) Control Implementation 160
  (A) Parity simulator generalized controller 162
    (i) State feedback 164
    (ii) Periodic output feedback 167
  (B) Compupro microcomputer 168
(5) Results and Discussions
  (A) State feedback
    (i) Using the generalized controller 172
    (ii) Using the compupro 180
  (B) Periodic output feedback 181

CHAPTER VI : SUMMARY AND DIRECTIONS FOR FURTHER WORK

(1) Summary 187
(2) Suggestions for Further Work 190

REFERENCES 191

InductEV, Inc.
Exhibit 1014
Page 006

LIST OF FIGURES

Figure		Page
2-1	A series voltage-fed resonant converter and its impedance-frequency characteristics	16
2-2	A parallel voltage-fed resonant converter and its admittance-frequency characteristics	17
2-3	Symmetric Half bridge and asymmetric configurations of a resonant converter	18
2-4	Half bridge connection using a single source	20
2-5	Types of resonant load presented in the literature	21
2-6	Types of switch used in resonant converters	22
2-7	A tree diagram showing resonant converter types	23
2-8	Voltage-fed, half bridge, unidirectional switch, series load inverter analyzed by Thompson [5]	28
2-9	Voltage-fed, half bridge, bidirectional current switch inverter analyzed by Mapham [17]	28
2-10	Voltage-fed, full bridge, bidirectional current switch, series load inverter analyzed by Revankar and Karade [8]	30
2-11	Voltage-fed, full bridge, unidirectional switch resonant inverters	31
2-12	Modified voltage-fed, full bridge, series load inverter analyzed by Viet-son et al [15]	32
2-13	Voltage-fed series resonant dc-dc converter	34
2-14	Voltage-fed parallel resonant dc-dc converter	35
2-15	Current-fed, full bridge, unidirectional switch, parallel load inverter analyzed by Revenkar and Gadag [6]	36
2-16	Current-fed, full bridge, unidirectional switch, series-parallel load inverter analyzed in [7]	37
2-17	A high-frequency inverter, fed from the ac mains without the use of dc-link analyzed by Havas et al.	39
2-18	Current-fed, full bridge, series-parallel load, time-sharing inverter and its corresponding conventional inverter	41
2-19	Comparison of thyristor turn-off time for time-sharing and conventional converters (simulation results)	42

InductEV, Inc.
Exhibit 1014
Page 007

2-20	Time-sharing inverter subunits	44
2-21	A three-stage, four terminal, voltage-fed time-sharing inverter using multi-winding transformer technique [5]	45
2-22	A five stage, voltage-fed, time-sharing inverter using multi-winding transformer technique [39]	47
3-1	The parts of a resonant converter	52
3-2	Waveforms of the voltage V_L of Fig. 3-1	53
3-3	A switching cell for developing resonant converter topologies	54
3-4	The asymmetric voltage-fed topology	56
3-5	Full bridge voltage-fed topology	58
3-6	Voltage-fed topologies using two sources and two switching cells	59
3-7	Symmetric topology using two voltage sources	60
3-8	Half bridge voltage-fed topology	61
3-9	Symmetric half bridge topology with load voltage shown in Fig. 3-2d	62
3-10	Formation of a symmetric waveform from asymmetric waveforms	63
3-11	Basic types of resonant loads	65
3-12a	A series half bridge topology	66
3-12b	A parallel half bridge topology	67
3-13	Cascaded higher order loads	68
3-14	Voltage and current waveforms of a switch in a series voltage-fed converter	70
3-15	Switch implementation of the asymmetric topology	71
3-16	Series voltage-fed resonant circuit	72
3-17	Voltage-fed parallel resonant loads	75
3-18	Graphs of the impedance of the loads of Fig. 3-17	76
3-19	Series resonant circuit	78

InductEV, Inc.
Exhibit 1014
Page 008

3-20	Voltage-fed series resonant topologies derived using symmetry	79
3-21	Divided-inductor asymmetric and full bridge topologies	80
3-22	Half bridge topology obtained by applying symmetry about an inductor and a resistor in a series load	81
3-23	Symmetry derived half bridge series topologies obtained when a switch is placed across the capacitor	82
3-24	divided-inductor, divided-capacitor series topology	83
3-25	Parallel resonant circuits used for deriving voltage-fed parallel topologies using symmetry	84
3-26	Half bridge voltage-fed topologies with bidirectional power flow	85
3-27	Symmetry derived parallel topologies	86
3-28	Divided capacitor parallel voltage-fed topology	87
3-29	Voltage-fed series resonant topology with bidirectional current switch	89
3-30	Current-fed parallel resonant topology with bidirectional voltage switch	90
3-31	Voltage-fed parallel topologies and their duals	92
3A-1	Entries of the F matrix for a series resonant circuit	105
3A-2	Possible proper networks for a series resonant converter	105
3A-3	Entries of the F matrix that satisfy parallel resonant networks	108
3A-4	Circuit realizations of Fig. 3A-3	110
4-1	A voltage-fed series resonant converter	114
4-2	Response of the rectified inductor current (i_o) to a step change in the switching frequency for a resistive load	116
4-3	Response of i_o to a step change in the switching frequency for a voltage source load	116
4-4	Large-signal response of the series resonant converter (voltage source load	117
4-5	State variables waveforms for the series resonant converter of Fig. 4-1	119

InductEV, Inc.
Exhibit 1014
Page 009

4-6	The switching configurations for a series resonant converter during a complete switching cycle	123
4-7	Change of waveforms from sampling every cycle to sampling every half cycle	128
4-8	Perturbed and steady state waveforms of the inductor current	132
4-9	Nominal and perturbed states of a resonant converter over a half cycle	135
4-10	The series resonant converter circuit including the parasitic resistors in the simulator	139
4-11	Results of the small-signal model for the series resonant converter of Fig. 4-10, when V_o = 0.0 V	139
4-12	Response of the output current i_o to a 5% step in the switching frequency	140
4-13	Results of the small-signal model for the series resonant converter of Fig. 4-10, when V_o = 5.0 V	141
4-14	Locus of the poles as V_o is varied	142
4A-1	Circuit diagram for the switching configurations of the series resonant converter	149
4A-2	Phase-plane of the inductor and capacitor voltages over a complete switching cycle	150
5-1	The series resonant dc-dc converter	160
5-2	Waveforms of the state variables for the series resonant converter of Fig. 5-1	162
5-3	A block diagram of the closed-loop control of the series resonant converter using the generalized controller	165
5-4	State feedback implementations without a delay block using the generalized controller	166
5-5	Generalized controller implementation of the periodic output feedback	167
5-6	A block diagram of the state feedback control using the Compupro microcomputer	168
5-7	The A/D connections	170
5-8	The D/A connections	171

InductEV, Inc.
Exhibit 1014
Page 010

5-9	Open-loop response of of the output current to a 5% step change in f_s	175
5-10	Closed-loop response of the output current using a second order model and including a delay of one cycle	176
5-11	Closed-loop response of i_o using a third-order model	177
5-12	Closed-loop response of the output current using the generalized controller with a third-order model	178
5-13	Sampling and control instants	179
5-14	Closed-loop response of the output current using a second-order model without a cycle delay	179
5-15	Open-loop response of the output current to a 5% step in the switching frequency	183
5-16	State feedback response using the Compupro microcomputer	184
5-17	Periodic output feedback response of the output current using the generalized controller	185
5-18	Periodic Output feedback using the Compupro microcomputer	186

InductEV, Inc.
Exhibit 1014
Page 011

CHAPTER I

INTRODUCTION

(1) Background

Resonant converters have been used since the days of vacuum tubes [1] - [4]. The development of semiconductor power switches, such as transistors and thyristors, has led to better performance than was possible with vacuum tubes [5] - [51]. In the past two decades, resonant converters have normally been associated with thyristor converters. This is because the resonant load can be used to commutate the thyristor, thereby eliminating the need for an additional commutation circuit. The application of resonant converters, using tubes or thyristors, has until recently been limited to high power areas such as:

(i) ultrasonic cleaning, welding and mixing equipment using either magnetostrictive or electrostrictive transducers,

(ii) induction heating and melting,

(iii) VHF radio transmitters.

Advances in technology, design and manufacturing of the power semiconductor switches have reduced switching losses and increased speed. In particular, the advent of the power MOSFET has made high frequency switching (100 kHz or higher) increasingly attractive to circuit designers. In recent years considerable progress has been made in the design of high frequency resonant converters, using power MOSFETS. New applications have evolved, such as resonant dc-dc converters in power supplies for computers, telephone equipment or battery chargers.

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Exhibit 1014
Page 012

Many types of resonant converters have been treated in the literature [1]-[51]. The analysis and development of these converters have focused on two areas:

(i) Analyzing a specific converter and deriving design nomograms using some normalized parameters such as: the output power range, frequency range, distortion factor on output voltage and current, efficiency, voltage and current ratings of circuit components, and weight and size of the converter [1] - [37].

(ii) Overcoming the limitations of the thyristor turn-off time at high frequency. In this area, thyristor inverter circuits have been modified to perform at frequencies higher than those set by the thyristor turn-off time. Many authors have successfully applied the technique of time-sharing to some conventional thyristor power inverters and developed new time-sharing inverter technology to overcome the operating limitations of thyristor turn-off time [38]-[51].

(2) <u>Goals of this thesis</u>

The purpose of this thesis is to explore three areas that have not been studied carefully in the field of resonant converters. These are the areas of topology, dynamic modeling and control. Most of the previous work done in these areas has focused on switching dc-dc converters rather than resonant converters[55] - [59].

In the area of topology, there is a need to establish some methodologies to systematically develop resonant converter topologies. Such a need arises because of the lossness of existing classifications of resonant converters. This thesis begins an effort towards such a

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Exhibit 1014
Page 013

classification.

In the area of dynamic modeling of resonant converters, very little work has been done. King and Stuart [78] have considered large signal modeling of a series resonant converter. De Haan has analyzed the dynamics of an integral pulse module for a series resonant converter [79]. Dynamic modeling of resonant converters has also been treated in the work of Vorperian [72]. Our work has been carried out independently of these, and has addressed dynamic models of general circuits as well, see [61].

Dynamic models are necessary in the design of feedback controllers for resonant converters. Digital control schemes based on a sampled-data model are designed implemented and tested. The effects of computational delay in digital controller on the closed loop dynamics are also investigated.

(3) Thesis Outline

Chapter II presents an overview of resonant converters. The structure and modes of operation of a resonant converter are first duscussed. An overview of conventional resonant converters that have been presented in the literature is then given. Some of the limitations presented by conventional resonant converters are noted. In particular, the limitation imposed by the thyristor turn-off time at high frequency operation is discussed, and some of the techniques, such as time-sharing inverters, used to overcome this limitation are presented.

Chapter III presents three methodologies that may be used to synthesize resonant converter topologies. The first methodology defines a switching cell from which the basic resonant converter topologies are derived. These basic topologies are the asymmetric topology, the

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Page 014

symmetric full bridge and symmetric half bridge topologies. The second methodology explores the symmetry structure of a resonant converter to show how some existing and new topologies may be generated. The third methodology uses duality to derive other topologies and examines some of the relationships between dual converters. Some of the factors that enter this examination are the types of switch and modes of operation in dual converters.

Chapter IV addresses the issue of dynamic modeling of resonant converters. Some simulation results, obtained using the MIT Parity Simulator [69] and providing motivation to study the dynamics of resonant converters are discussed. Mathematical models that describe both the large-signal dynamics and the dynamics of small perturbations about cyclic steady state operation are developed. Some of the analytical results obtained are compared with the simulation results. Issues such as numeric and symbolic analysis, their automatability, and computation of sensitivity to circuit parameters are also discussed.

Chapter V discusses the closed loop control of resonant converters. In particular, the methods of state feedback and periodic output feedback are used with the model obtained in Chapter IV to control a series resonant dc-dc converter. The control is implemented in two ways. One uses the Parity Simulator generalized controller [80] and the other uses a Compupro microcomputer. Experimental results are presented.

Chapter VI gives a summary, conclusions and suggested future work.

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Page 015

CHAPTER II

OVERVIEW OF RESONANT CONVERTERS

(1) Introduction

In this chapter we shall describe resonant converters and give a summary of the categories into which research on resonant converters has fallen. We shall also define topics where more research needs to be done.

Research on resonant converters has focused on the development of thyristor inverters to supply high power at high frequency for induction heating, ultrasonic cleaning and welding, and low frequency radio transmitters. More recently, there is an increasing use of resonant converters in low power, high frequency applications, such as dc-dc power supplies. The thyristor has been used more than other switching devices in high power applications. There are two main reasons for this. First, the thyristor can handle high power, when compared with other switching devices. Secondly, since the thyristor turns off when its current goes to zero, the principle of natural commutation on which many resonant converters work turns off the thyristor without the need for an additional commutation circuit.

The analysis and development of resonant converters have emphasized two areas:

(i) Deriving design equations using some normalized parameters such as output power range, frequency of operation, converter efficiency and rating of components [1]-[37].

(ii) Overcoming the limitation imposed by the thyristor turn-off time at high frequencies by modifying resonant converters to perform at frequencies higher than those set by the thyristor

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Page 016

turn-off time [38] - [50].

Research in the first area has been mainly on single-stage resonant converters (conventional resonant converters). Research in the second area has led to the development of multi-stage resonant converters (time-sharing resonant converters). This chapter will discuss these two areas in detail, and will conclude with directions for further research.

(2) Resonant Converters: Structure and Modes of Operation

(A) Structure

Resonant converters (or inverters) are switched power circuits that generate nearly sinusoidal output voltages and currents from a dc supply. Typically, switches connect either a constant voltage across a series resonant load or a constant current through a parallel resonant load, as Fig. 2-1a shows. The switches S_1 and S_2 operate alternately at a switching frequency f_s, one pair closing the instant the other opens. In voltage-fed inverters, the switches experience square waves of constant amplitude voltage, and pass half sine waves of current. The impedance of the combined series resonant load as a function of the switching frequency are shown in Fig. 2-1b. This impedance is minimum when the switching frequency is equal to the resonant frequency $f_r(=1/(2\pi\sqrt{LC})$. At this point the LC filter has zero impedance, and the total impedance is equal to the load resistance. By varying the switching frequency about the resonant frequency, the LC filter will not have zero impedance, and depending on the ratio (f_s/f_r) it looks either like a small capacitor or a small inductor. This additional impedance will divide the input voltage between the LC filter and the load resistor. Therefore by varying the ratio (f_s/f_r) the output load voltage can be

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Exhibit 1014
Page 017

controlled. Similar discussion applies for a parallel resonant load with an input current source. Typical structure for a current-fed converter is shown in Fig. 2-2. The switches pass square waves of constant amplitude current and experience half sine waves of voltage. Again, the ratio (f_s/f_r) is used to control the output current.

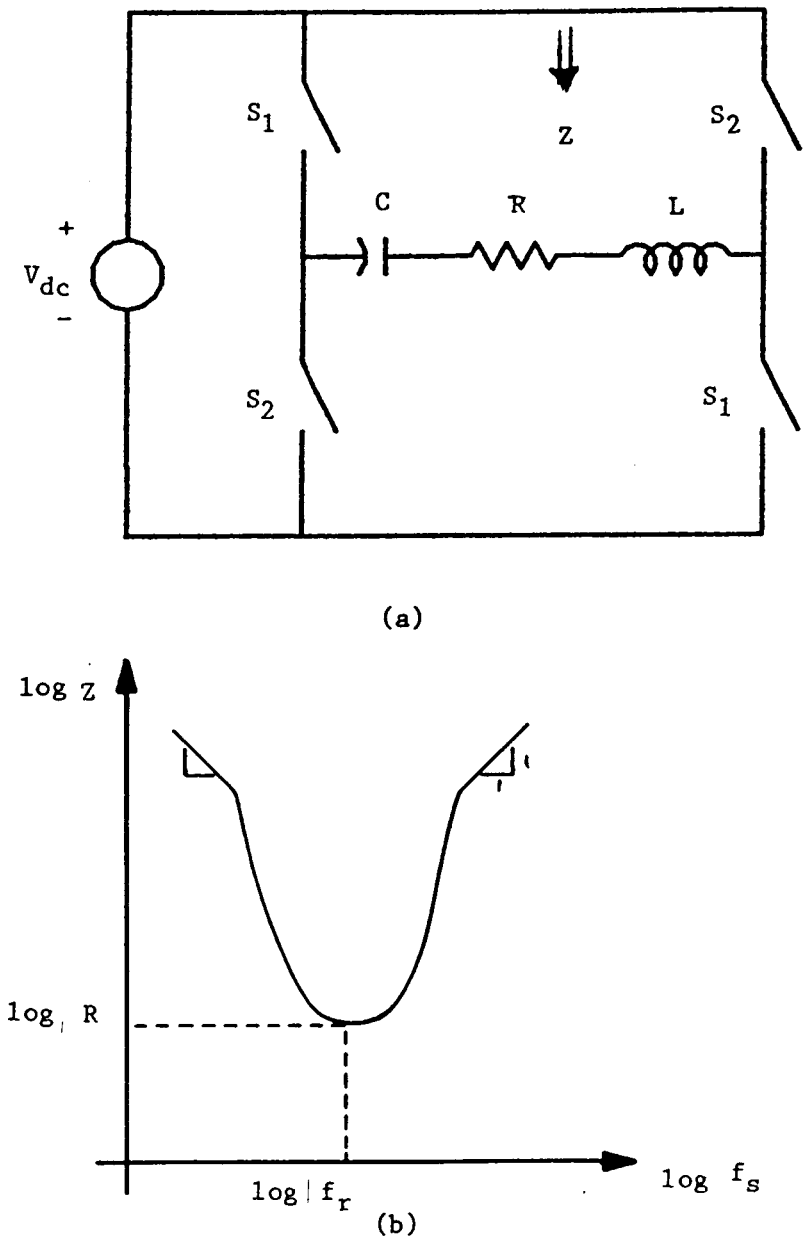

Fig. 2-1 A series voltage-fed resonant converter and its impedance-frequency characteristics

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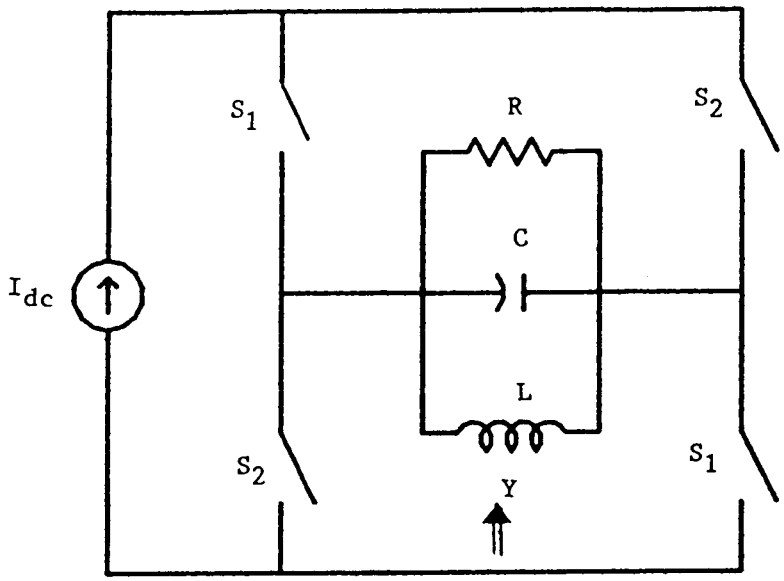
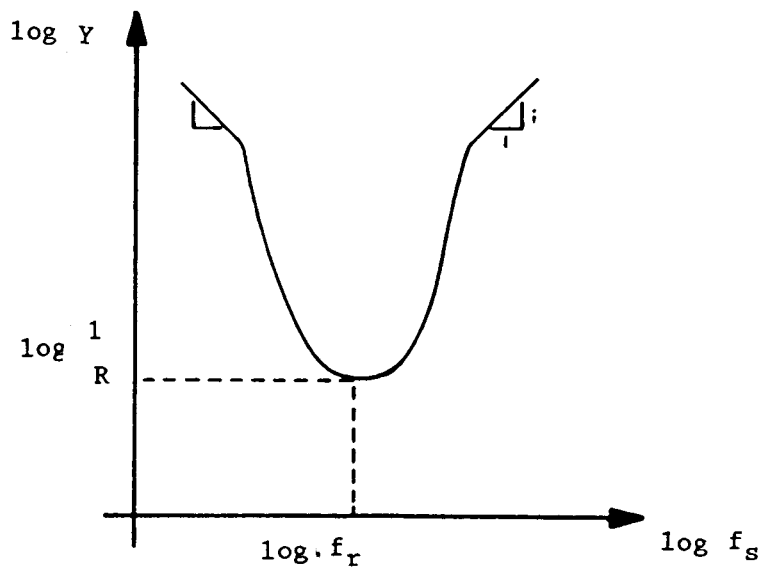
Exhibit 1014
Page 018



(a)



(b)

Fig. 2-2 A parallel current-fed resonant converter and its admittance-frequency characteristics

A resonant converter usually has three parts : a source, a load (including the resonant tank circuit) and switches. The source can be either a voltage or a current source. It connects to the load in either a symmetric configuration or asymmetric configuration.

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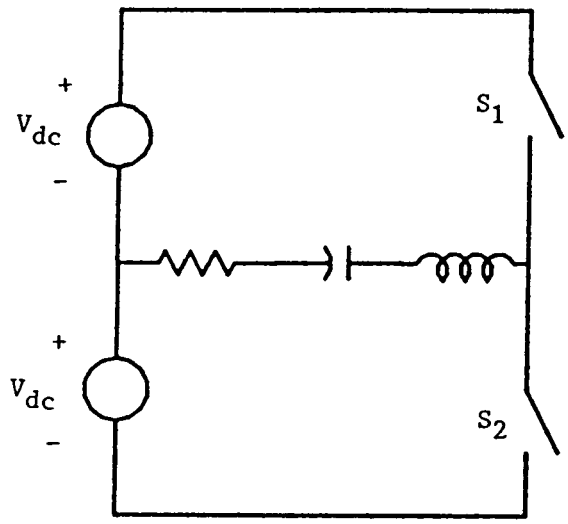
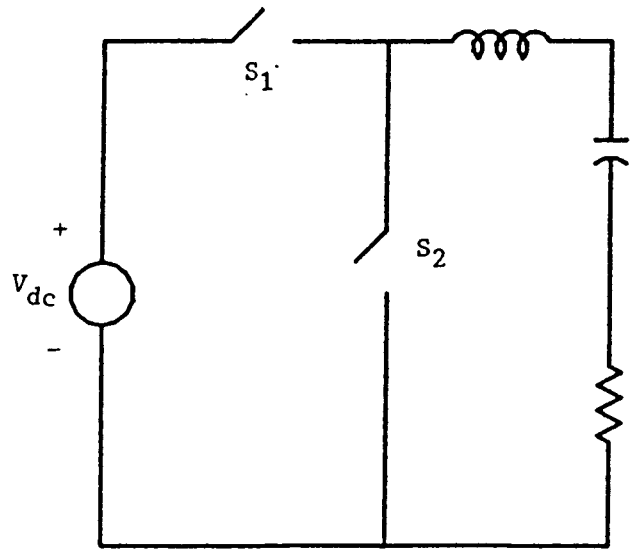
Page 019

The symmetric configuration can be either a full bridge [8](a single source connected to the load via four switches) or a half bridge (two sources connected to the load via two switches). The converters shown in Figs. 2-1 and 2-2 are both full bridge connections. Fig. 2-3a shows a half bridge configuration and Fig. 2-3b shows an asymmetric configuration.



(a) Half bridge connection



(b) Asymmetric connection

Fig. 2-3 Symmetric half bridge and asymmetric configurations of a resonant converter

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Page 020

The two voltage sources in the half bridge connection can be obtained by using: two independent sources [17]; a single source split by two capacitors, in case of a voltage source; or a divided-inductor in case of a current source [5]. The capacitors that split the voltage source and the inductor that splits the current source are sometimes used as part of the tuned circuit.

Fig. 2-4 shows two half bridge connections using a single source. The voltage, current and hence the energy storage and rating of the capacitors in Fig. 2-4a is different from that in Fig. 2-3a.

Three types of loads, usually associated with thyristor inverters for induction heating, are commonly considered in the literature: a series-compensated (s.c) load [5], a parallel-compensated (p.c) load [9], or a combined series-parallel-compensated (s.p.c) load [10]. Fig. 2-5 shows the three types. The "series" and "parallel" refer to the way the tuning capacitor is connected to the tuning inductor. The word "compensated" is introduced because capacitors are usually used with induction heating loads, which are usually inductive, to improve the power factor. There is confusion in the literature as to the use of the labels series and parallel. Some authors use these to refer to the way the switch is connected, while others use them to define the resonant load type. It is hoped that the discussion of resonant converter topologies in Chapter III will clarify the terminology.

The switch connections commonly considered are of two types: a basic switch (a thyristor, a transistor or a power MOSFET)[5],[12], and a reverse switch (any of the above switches with an anti-parallel diode across it)[8],[14],[17].

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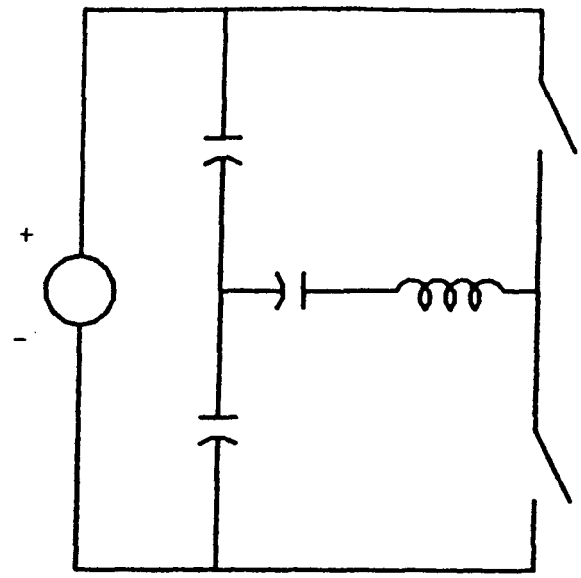
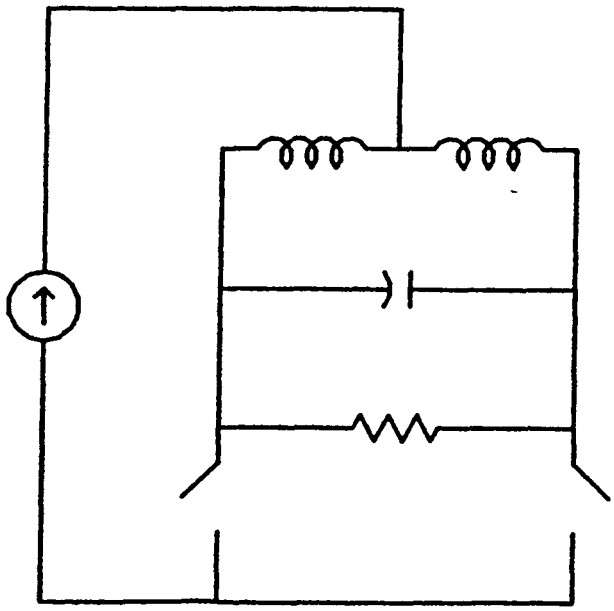
Page 021



(a) Divided-capacitor connection



(b) Divider-inductor connection

Fig. 2-4 Half bridge connections using a single source

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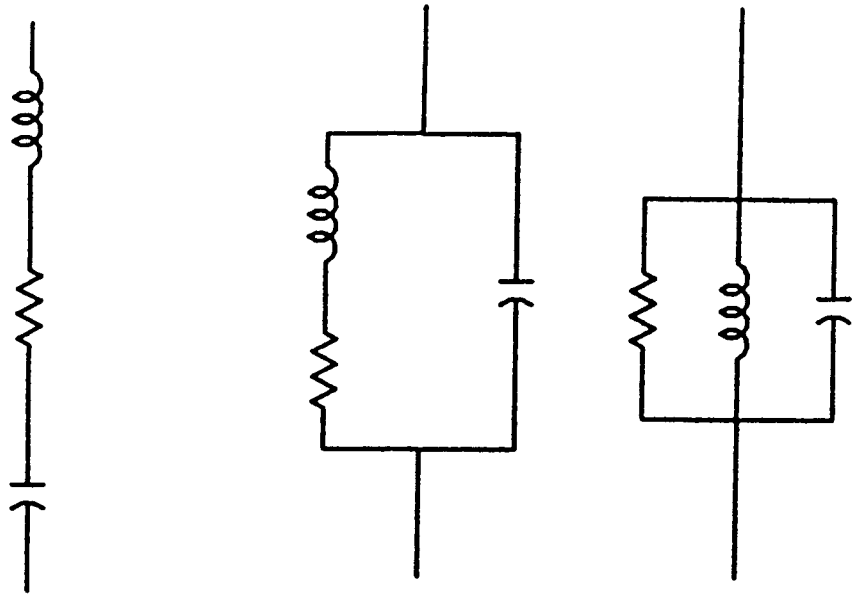
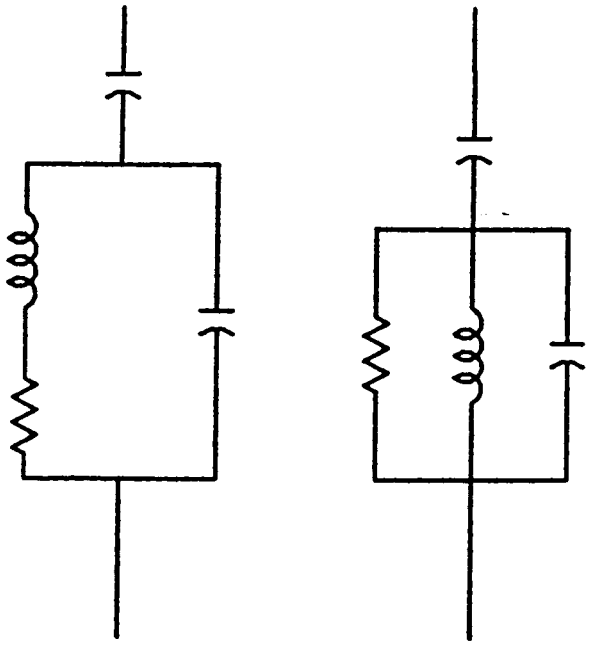
Exhibit 1014
Page 022



(a) S. C. load

(b) P. C. load

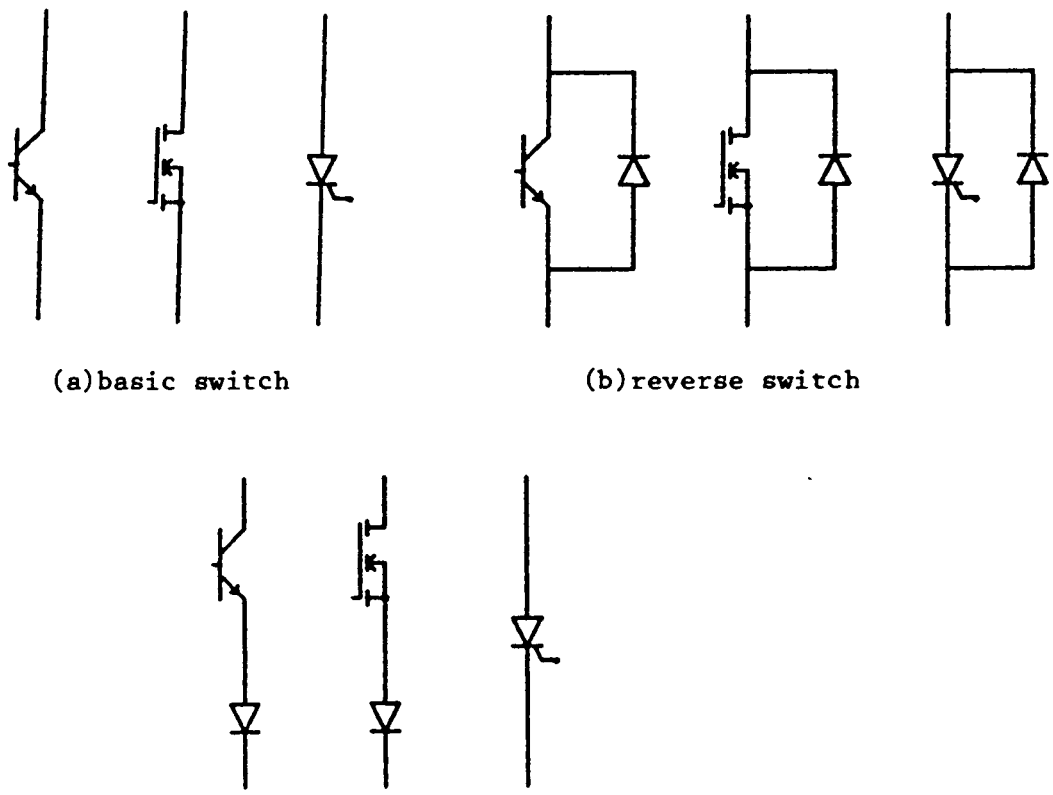


(c) S. P. C. load

Fig. 2-5 Types of resonant load presented in the literature

InductEV, Inc.
Exhibit 1014
Page 023

Fig. 2-6 shows the two types of switch. Better names for these switch connections are unidirectional current switch (for the basic switch) and bidirectional current switch (for the reverse switch). This allows a complete definition of switch types by introducing a bidirectional voltage switch [16] (the dual of the reverse switch of Fig. 2-6b), as shown in Fig. 2-6c. A diode is added in series with either a bipolar or a power MOSFET to support negative voltage. Thyristors are two of types: one type supports bidirectional voltage and no series diode is needed; the other type is designed so that it only supports a small negative voltage and therefore a series diode is needed for bidirectional voltage.



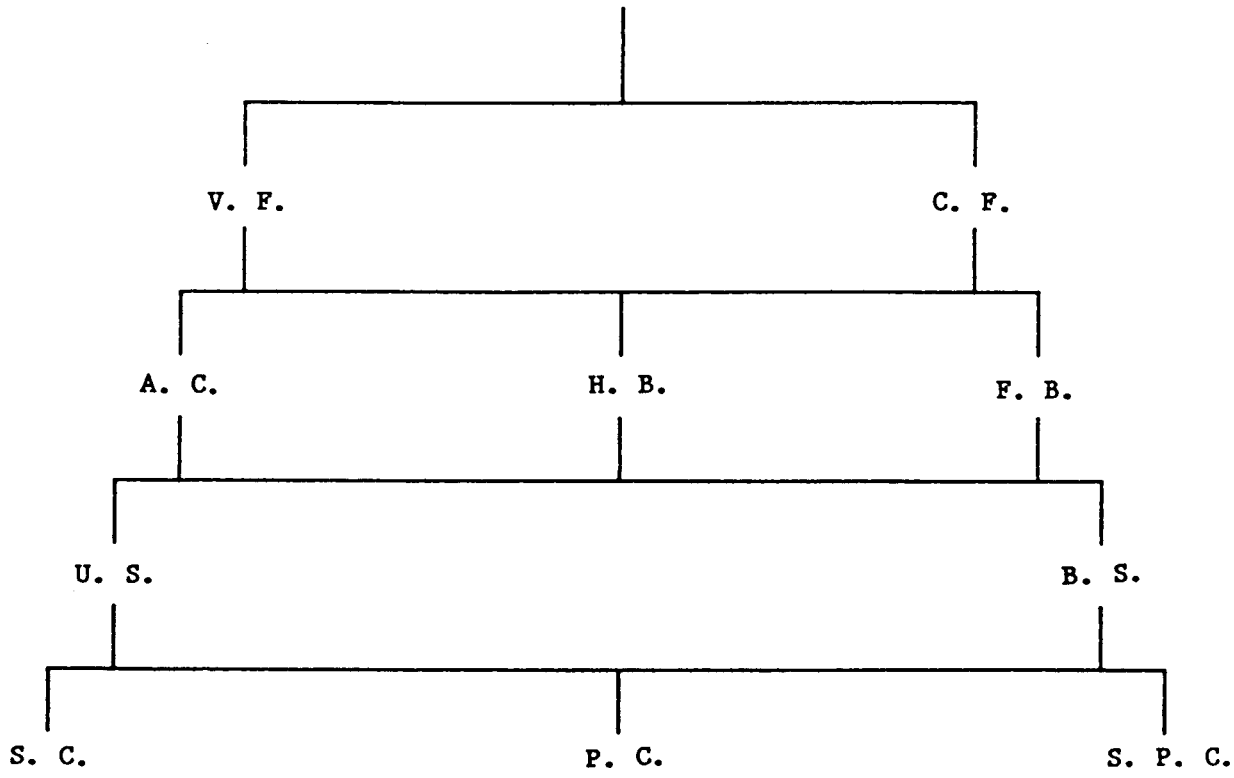
(a)basic switch (b)reverse switch

(c) Bidirectional voltage switch

Fig. 2-6 Types of switch used in resonant converters

InductEV, Inc.
Exhibit 1014
Page 024

These classifications of source, load and switch form a basis for categorizing or naming the different resonant converters that have been discussed in the literature. Fig. 2-7 lays out a summary of the classifications that we have discussed. These topologies will be discussed further when we discuss the synthesis of resonant converters in Chapter III.



V. F. = Voltage Fed
A. C. = Asymmetric connection
H. B. = Half Bridge
B. S. = Bidirectional Switch
P. C. = Parallel Compensated

C. F. = Current Fed
F. B. = Full Bridge
U. S. = Unidirectional Switch
S. C. = Series Compensated
S. P. C. = Series Parallel Compensated

Fig. 2-7 A tree diagram showing resonant converter types

InductEV, Inc.
Exhibit 1014
Page 025

(B) Modes of Operation

The mode of operation of a converter is its switching sequence or the switching configurations that occur during a switching cycle. These depend on the load and the ratio of the switch drive frequency (f_s) to the resonant frequency (f_r). Depending on this ratio, the no load operation has one of the following modes [12]:

(i) Natural commutation (discontinuous) mode, when $(f_s/f_r) < 1$ for a unidirectional current switch inverter and $(f_s/f_r) < (1/2)$ for a bidirectional current switch inverter. In this mode the switches are naturally commutated.

(ii) Critical commutation mode, when $(f_s/f_r) = 1$ for a unidirectional current switch inverter and $(f_s/f_r) = (1/2)$ for a bidirectional current switch inverter. This mode of operation makes the boundary between the natural commutation mode and the overlapping mode.

(iii) Overlapping (continuous) mode, where $(f_s/f_r) > 1$ for a basic switch inverter and $(f_s/f_r) > (1/2)$ for a bidirectional current switch inverter. In this mode the switches are commutated either by forced commutation or by an external commutation circuit.

(3) Conventional Resonant Converters

The name conventional converter (or inverter) applies to any of the structures given in Fig. 2-7. The term "conventional" is used to differentiate single-stage resonant converters from their corresponding multistage "time-sharing" converters. In the coming sections we shall discuss the different conventional resonant converters presented in the

InductEV, Inc.
Exhibit 1014
Page 026

literature. We shall consider the work done on voltage-fed converters first, and then discuss current-fed resonant converters. The basic operation of these converters will not be described, but the main features of each converter will be presented. Finally we shall discuss some of the limitations of conventional resonant converters. More specifically, the limitation imposed by the thyristor turn-off time on the operating frequency of conventional resonant converters will be discussed. This leads us to a discussion of time-sharing techniques that modify conventional converters to operate at a frequency higher than that set by the turn-off time of a thyristor.

Research on conventional resonant converters emphasizes the following areas:

(i) Analysis of steady state operation. Investigators analyze a specific converter and derive the equations for the allowable operating range of output power and frequency, allowable thyristor turn-off time and stresses, rating and design of components (capacitors, inductors, etc) as a function of the ratio (f_s/f_r) and the Q-factor or the characteristic impedance of the resonant tank circuit [1]-[15]. Each author has analyzed a specific converter and solved the state equations to obtain the steady state operation of the converter. Each analysis has its own normalized parameters and uses certain assumptions and approximations regarding ideality and nonideality of components, presence of certain parasitics or assumption of high Q.

(ii) Development of new converter topologies. An existing converter is modified to obtain better load characteristics, or new

InductEV, Inc.
Exhibit 1014
Page 027

devices are used in an existing converter [16]-[23]. We shall discuss in a later section how such modifications of existing converters may be carried out.

(iii) Design of protective circuits, development of starting methods or digital timing circuits for controlling the switches [24]-[27].

(iv) Analysis of dc-dc resonant converters [28]-[34].

(v) Reduction of weight, size and cost of equipment [35].

(vi) Design of off-line ac-ac resonant converters, where a high frequency output voltage is obtained directly from the 60 Hz line without the need for a rectifier stage [36], [37].

The following two sections give a detailed literature review of work on voltage-fed and current-fed converters.

(A) Voltage-fed resonant converters

The literature on voltage-fed converters can be divided into two application areas. The first deals with high power (on the order of hundreds of kilowatts), high frequency (10 kHz - 100 kHz) applications such as induction heating, ultrasonic cleaning and low frequency radio transmitters. These are mainly thyristor inverters. The second deals with low power (a few watts to one kilowatt), high frequency (100 kHz or higher) applications such as resonant dc-dc converters (power supplies for computers, telephone equipment or battery chargers). The devices used here are mostly bipolar power transistors and power MOSFETs. Most of the research done on resonant converters in the 1960's and early 1970's was in the first area. Work in the second area has increased recently because of the development of fully controlled switches that can operate in the megahertz range. The next two subsections review

InductEV, Inc.
Exhibit 1014
Page 028

some resonant converters that have been presented in the literature and discuss some of the issues studied in the research on each of them.

(i) High power, high frequency applications

Most of the research done on voltage-fed inverters falls into the first of the above areas [1]-[15]. The switch used in these inverters is generally a thyristor , and the mode of operation analyzed is usually the natural commutation mode. Issues presented in the analysis of each inverter generally fall into the calculation of the turn-off time and the voltage and current ratings of the thyristor and/or the ratings of the tuning elements for certain power and frequency specifications.

Fig. 2-8 shows a voltage-fed, half bridge, unidirectional switch inverter with a series compensated load. Thompson [5] has analyzed this inverter and compared it with the asymmetric inverter of Fig. 2-2. In his analysis, he shows that using two inductors in this inverter gives better performance than using a single inductor in the topology of Fig. 2-2. The use of two inductors reduces the delay between the firing instant of the thyristors, and lowers their dv/dt. The ratings of the devices do not increase. Also, in this inverter, the capacitors provide both a split source and a resonant action. Thompson has also analyzed the effect of coupling the two inductors. He shows that the turn-off time of the thyristor increases as the coupling is increased, and the size and cost of the core are increased; however, increasing coupling increases the voltage rating on the thyristor.

Mapham [17] points out that the inverter analyzed by Thompson has poor regulation and exhibits commutation failure at light loads, and is very sensitive to reactive loads. Mapham suggested an inverter, shown in Fig. 2-9, that overcomes these limitations.

InductEV, Inc.
Exhibit 1014
Page 029

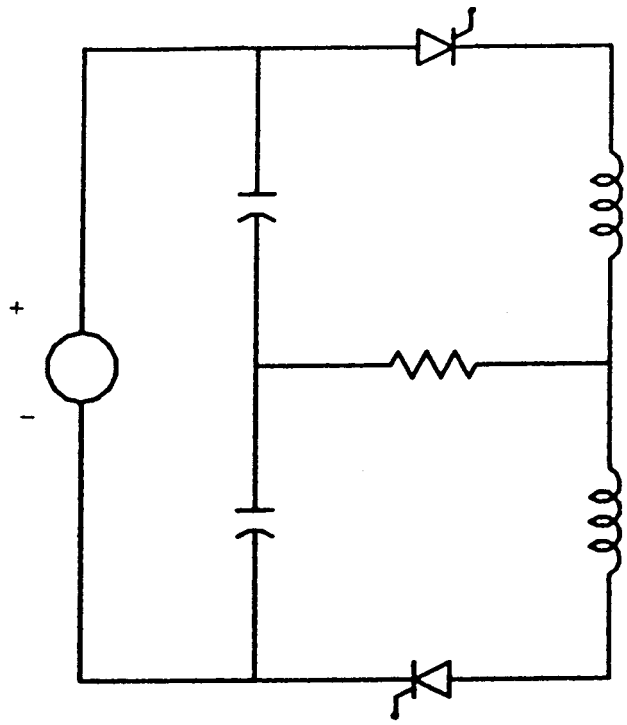


Fig. 2-8 Voltage-fed, half bridge, unidirectional switch, series load inverter analyzed by Thompson [5]

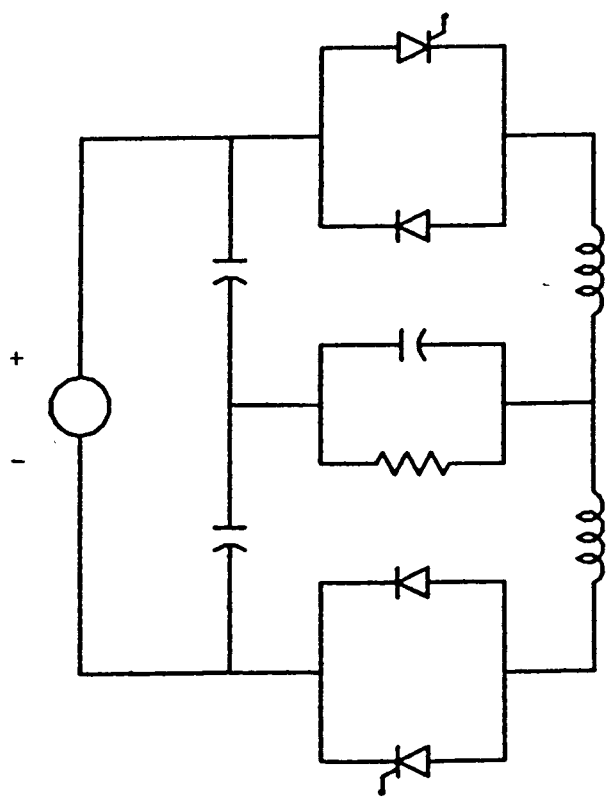


Fig. 2-9 Voltage-fed, half bridge, bidirectional current switch inverter analyzed by Mapham [17]

InductEV, Inc.
Exhibit 1014
Page 030

The capacitors across the source, in the Mapham inverter, are used only to obtain a split supply, and they are made very large compared to the resonant capacitor (across the resistor). The inverter uses a bidirectional current switch. The reverse voltage across the thyristor is equal to the forward voltage drop of the diode (on the order of one volt). Therefore, the thyristor need not to support a large reverse voltage. In fact, a new semiconductor device known as the Asymmetrical Silicon Controlled Rectifier (ASCR) [23] can be effectively used. The device is manufactured to be faster than a normal SCR by sacrificing reverse blocking voltage for speed. Hence the Mapham inverter not only has good regulation, but also can operate at a higher frequency than that of a basic switch inverter.

Revankar and Karade [8] have analyzed the voltage-fed, full bridge, bidirectional switch, series compensated load inverter, shown in Fig. 2-10. Their analysis shows that the inverter has a larger operating range of Q than the basic switch inverter. It also shows that the voltage across the tuning capacitor is higher for this inverter than for its dual current-fed inverter presented by Revankar and Gadag [6] (which will be discussed in the current-fed inverters section), a result that has also been reported by Kasturi [18].

Roda and Revankar [9]-[10] have analyzed the voltage-fed, full bridge, unidirectional switch inverter for both parallel and series-parallel tuned loads. Fig. 2-11 shows the two inverters. The analysis considers the operation of the inverters in the critical and the natural commutation modes. The equivalent load circuit for the inverter is designed to be capacitive at the operating frequency and a series-tuning inductor (L_d) is added in series with the dc supply.

InductEV, Inc.
Exhibit 1014
Page 031

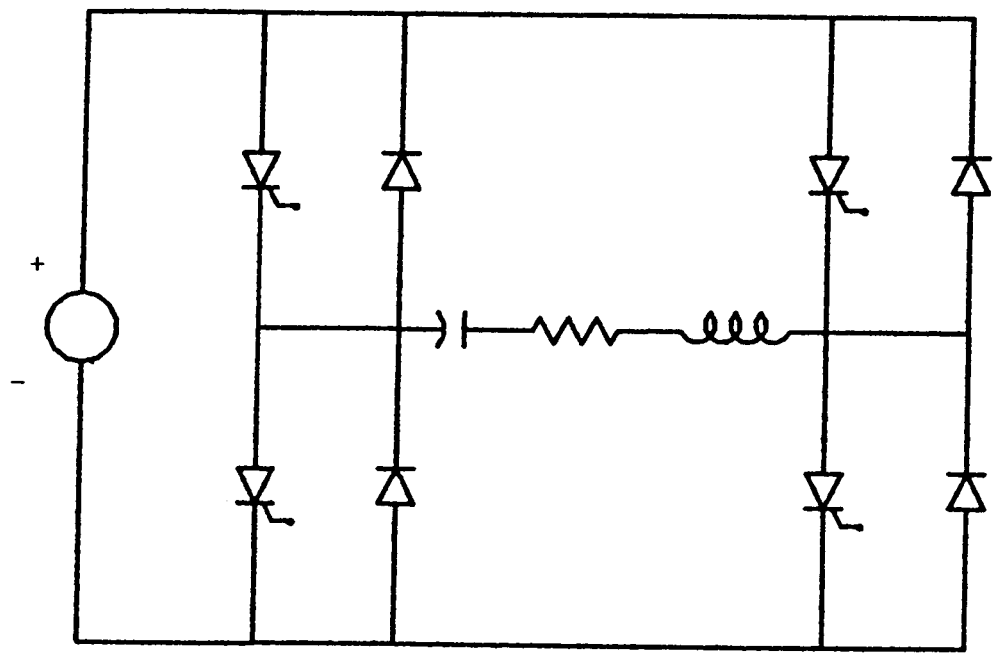


Fig. 2-10 Voltage-fed, full bridge, bidirectional current switch, series load inverter analyzed by Revankar and Karade [8]

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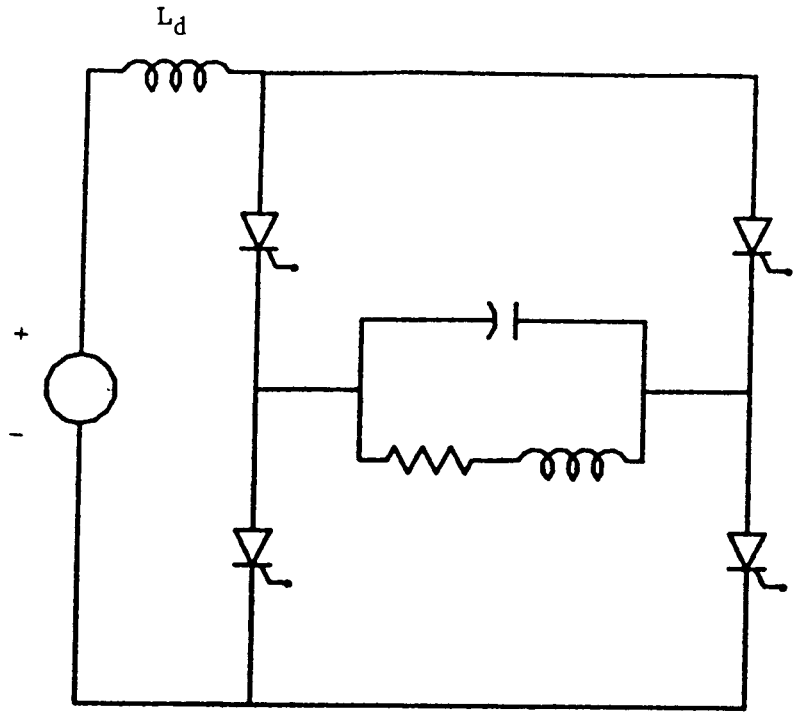
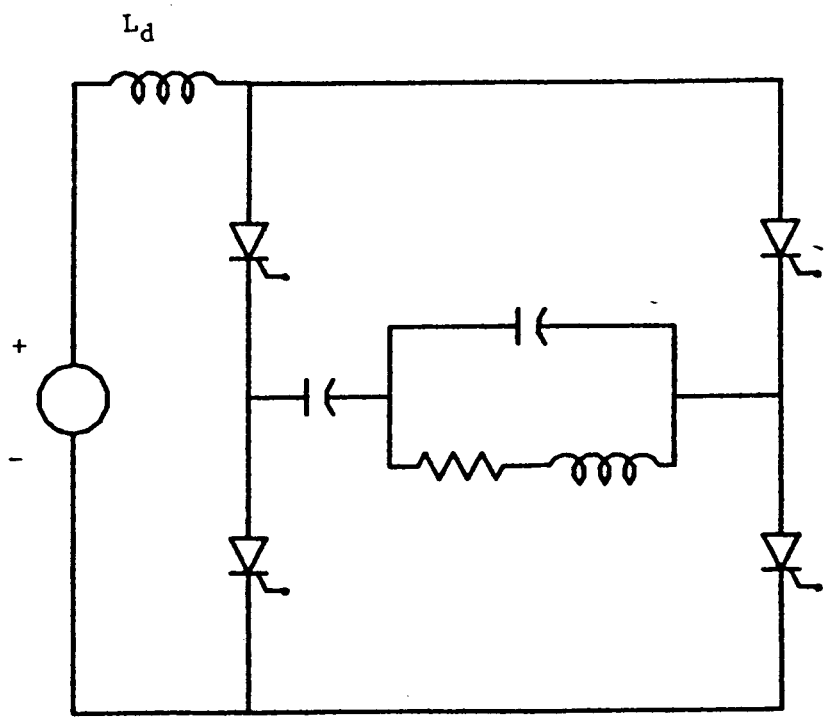
Exhibit 1014
Page 032



(a) P. C. load



(b) S. P. C. load

Fig. 2-11 Voltage-fed, full-bridge, unidirectional switch resonant inverters

InductEV, Inc.
Exhibit 1014
Page 033

There have been some attempts to modify certain inverter topologies and compare performance of the original inverter with its modification. Viet-son et al. [15] suggested the modification in Fig. 2-12 of the series load inverter of Fig. 2-8 discussed earlier by Thompson [5].

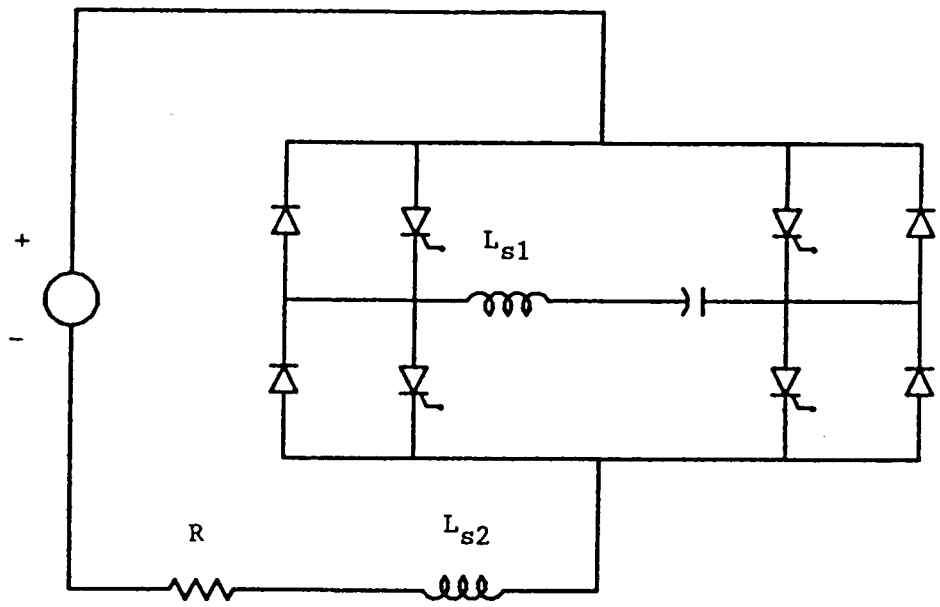


Fig 2-12 Modified, voltage-fed, full bridge series load inverter analyzed by Viet-Son et al [15]

The load R is put outside the bridge, and the inductor LS2 is added to control the dv/dt on the thyristor. More specifically their results show that the ratio $(L_{s2}/(L_{s1}+L_{s2}))$ can be chosen to make the dv/dt of this inverter lower than that of a bridge inverter with the load connected inside the bridge. One disadvantage of this inverter is the increase in the number of reactive components and the size of the inverter.

InductEV, Inc.
Exhibit 1014
Page 034

Nakaoka et al. [12]-[14] have analyzed the voltage-fed, half bridge, series load inverter for unidirectional and bidirectional current switch. They compare the two inverters in overlapping commutation mode. The maximum voltage and current of the thyristor in a the bidirectional current switch inverter are lower than those of the unidirectional switch inverter even if the load is shorted. Moreover, the initial rate of change of the thyristor current (di/dt) for the bidirectional current switch inverter does not vary over a wide range of load and frequency, and the thyristor commutation time margin is higher than that of the unidirectional switch.

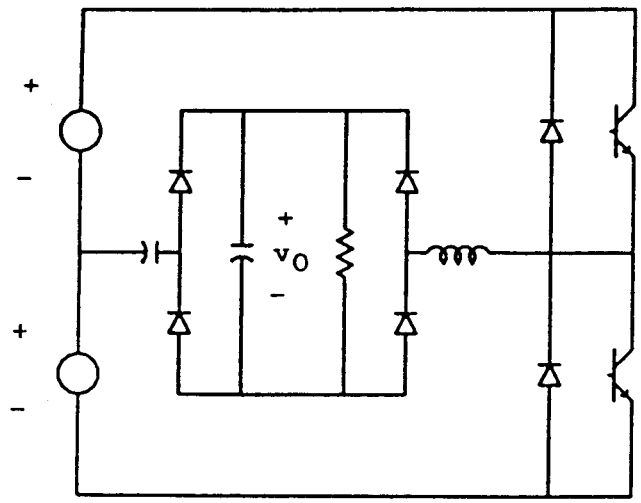
(ii) Low power, high frequency applications

One recent application of resonant converters at low power and high frequency is dc-dc converters. In this area high power is typically not needed, and the switches mostly used are bipolar power transistors and power MOSFETs. This application has attracted many researchers, driven by the development in the manufacturing of power devices that can switch at frequencies in the megahertz range. Operation at such high frequencies reduces the size and weight of the converter considerably, since the values of the resonant tank circuit components vary inversely with the resonant frequency.

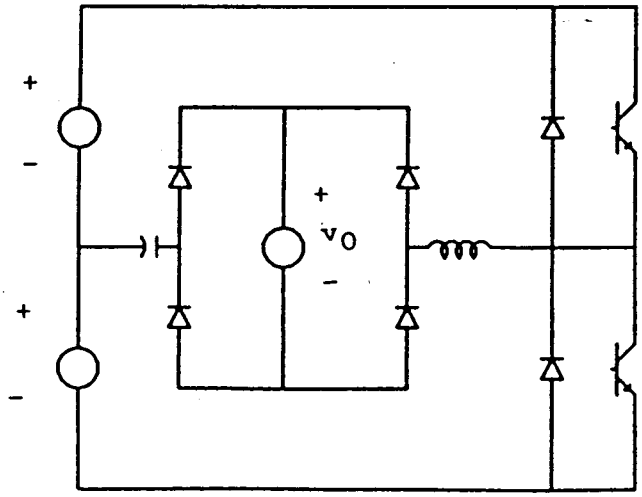
Two voltage-fed resonant dc-dc converters have been analyzed in some detail in the literature: the series [28]-[33] and parallel [34], [62], [77] resonant converters shown in Fig. 2-13 and 2-14 respectively. In the series resonant converter the inductor current is rectified, and the output of the rectifier approximates a voltage source. In the parallel converter the capacitor voltage is rectified and load on the output of the rectifier approximates a current source. In the analysis

InductEV, Inc.
Exhibit 1014
Page 035

the authors of the above papers have developed static models for the converters. The emphasis is on finding the variation of the conversion ratio (ratio of the output voltage to the input voltage) as a function of f_s/f_r. Such a function is very complicated to find when compared with the analysis of switching dc-dc converters [33]. Dynamic modeling of the two converters has been discussed in [62] and [72].



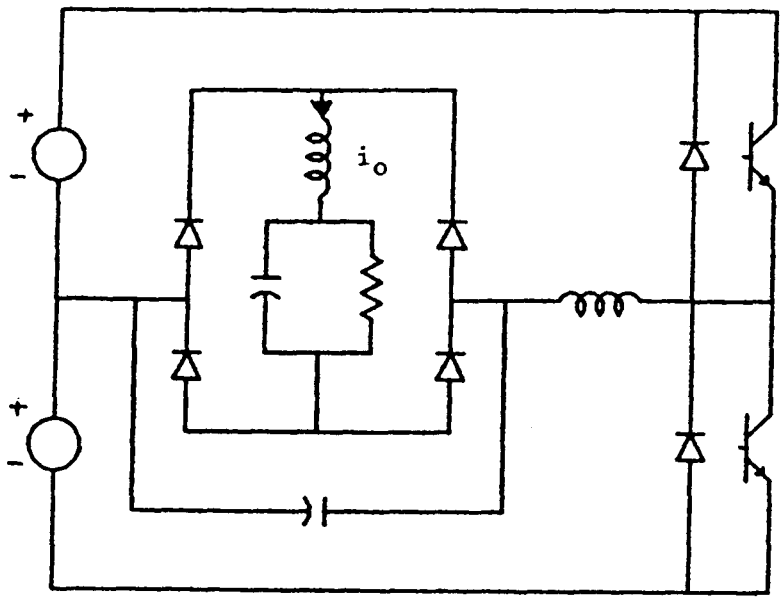
(a) Real component circuit



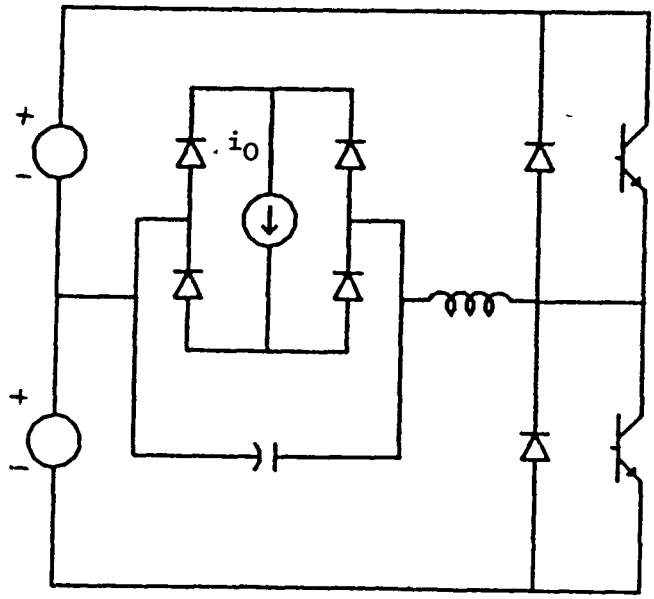
(b) Idealized component circuit

Fig. 2-13 Voltage-fed series resonant dc-dc converter

InductEV, Inc.
Exhibit 1014
Page 036



(a) Real component circuit



(b) Idealized component circuit

Fig. 2-14 Voltage-fed parallel resonant dc-dc converter

InductEV, Inc.
Exhibit 1014
Page 037

(B) Current-fed resonant converters

Current-fed resonant converters have been analyzed by some authors for the same applications that we considered when discussing voltage-fed resonant inverters (mostly induction heating applications). A true current source is difficult to build, but it can be approximated by a voltage source in series with a large smoothing inductor.

Revankar and Gadag [6] have analyzed the current-fed, full bridge, unidirectional current switch inverter for a parallel compensated load, as shown in Fig. 2-15.

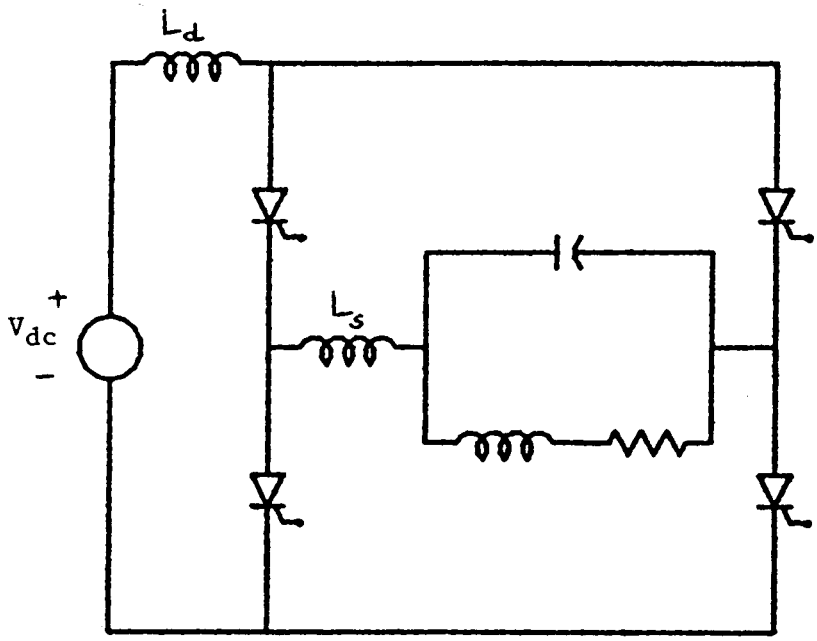


Fig. 2-15 Current-fed, full bridge, unidirectional switch, parallel load inverter analyzed by Revankar and Gadag [6]

As mentioned earlier, the voltage source V_{dc} and the inductance L_d are used to realize a current source. The inductor L_s represents a parasitic inductance with the load. This inverter is the dual of the inverter analyzed earlier by Thompson [5], and it would have been better if the analysis done by the authors of [6] had included a comparison of

InductEV, Inc.
Exhibit 1014
Page 038

the two inverters. For instance, they have shown that the thyristor turn-off time decreases with an increase in the load Q factor, a result opposite to what Thompson found. Such a result is valuable when considering duality relationships between inverters. Revankar and Gadag [7] have also analyzed the above current-fed inverter for a series-parallel compensated load, shown in Fig. 2-16. They have shown that the thyristor turn off time increases as the series capacitance (C_s) decreases. This effect allows the inverter to operate at a higher frequency than is possible with the parallel load, but it increases the maximum voltage across the thyristor.

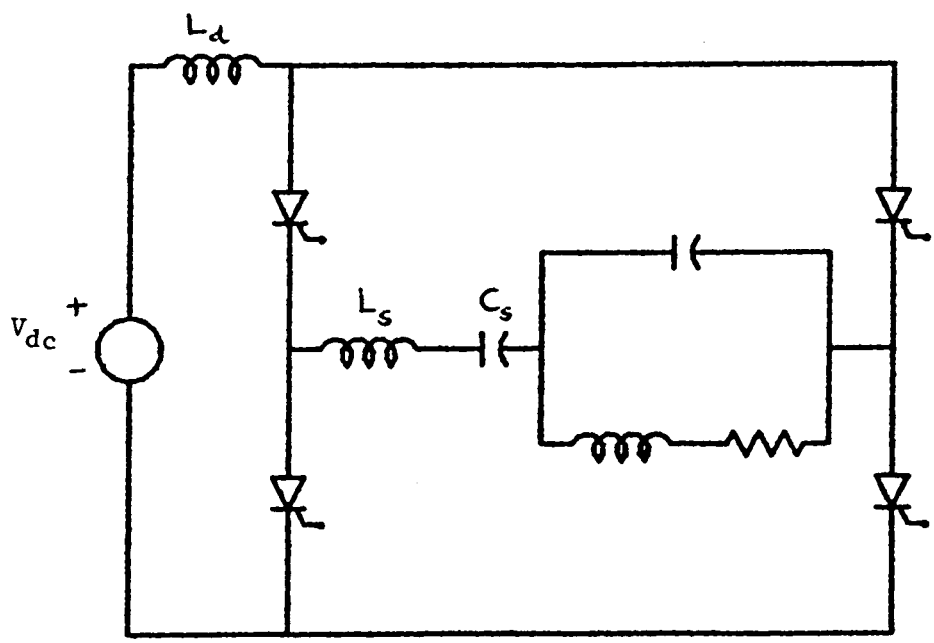


Fig. 2-16 Current-fed, full bridge, unidirectional switch, series-parallel compensated load inverter analyzed in [7]

Pelley [26] has discussed starting methods, and developed timing control for the current-fed, full bridge, unidirectional switch inverters for the parallel compensated load (Fig. 2-15) and the series parallel compensated loads (Fig. 2-16). His results show that the

InductEV, Inc.
Exhibit 1014
Page 039

series capacitor in the series parallel load is capable of providing sufficient commutation for the thyristor. Therefore an inverter with a series parallel compensated load is easier to start than the one with a parallel load. The timing control that he presented is an open loop control and not based on any detailed dynamic model.

So far we have considered resonant converters as dc-ac or dc-dc converters. There have been a few attempts to convert three phase power at 60 Hz directly to a single phase at higher frequency without the use of a dc link. For example, Havas et al. [25] have designed and built a 100 kW (700-1000 Hz) inverter that has an efficiency greater than 90% at unity power factor. The circuit diagram of the inverter is shown in Fig. 2-17. It is not clear whether or not the elimination of the dc link results in a reduction in weight and size of the converter, as the inverter needs an input filter and six switches. More work needs to be done in this area.

Another topic that has only been explored to a limited extent is the use of duality to expose relationships between dual converters. Kassakian [16] applied duality to the voltage-fed inverter analyzed by Mapham [17] and developed a current-fed inverter. A comparative study of the Kassakian and Mapham inverters is presented in [19], where it is shown that the implementation and application constraints on the two inverters prevent them from being practical duals.

InductEV, Inc.
Exhibit 1014
Page 040

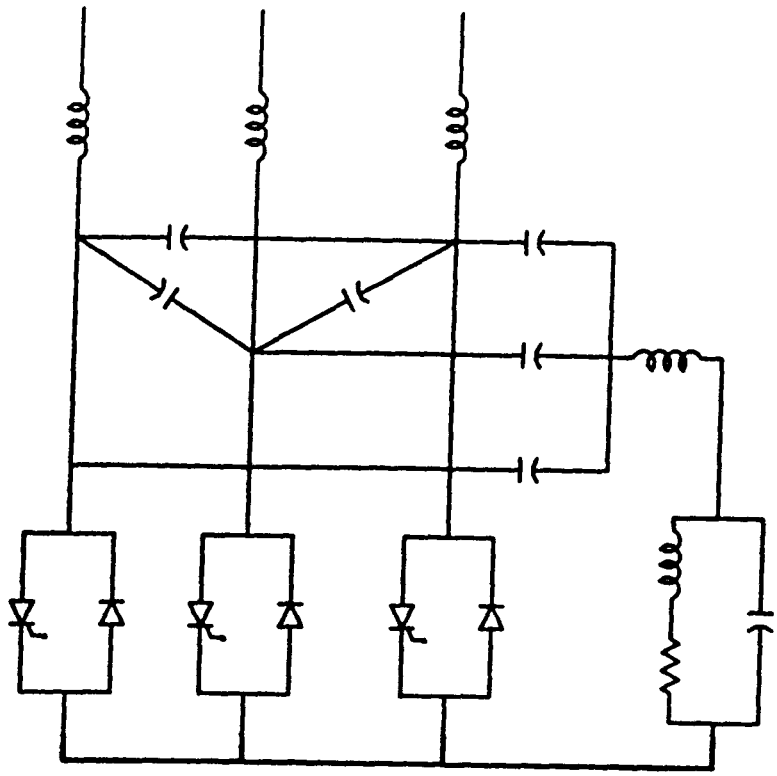


Fig. 2-17 A high frequency inverter fed from the ac mains without the use of a dc link as analyzed by Havas et al.[25]

(4) Problems Presented by Resonant Converters

(A) Limitation of the thyristor turn-off time

The thyristor has been used successfully as a switch in high frequency (up to 20 kHz), high power converters. However, its turn-off time limits the maximum operating frequency of the converter [39]. The allowed thyristor turn-off time is limited to some fraction (usually about one-fifth) of a half cycle. Therefore, a converter employing a thyristor with 20 microseconds turn-off time cannot run above a frequency of 5 kHz [39].

InductEV, Inc.
Exhibit 1014
Page 041

Two methods increase the allowable turn-off time in conventional thyristor-inverters. One uses asymmetrical thyristors, devices that have been made fast by sacrificing their reverse blocking capability [23]. The second method uses a commutating capacitor in series with the tank circuit (used only in current-fed inverters, see Fig. 2-16) [7],[10],[11].

Higher frequencies have also been achieved using a technique called time-sharing which will be discussed in the next section.

(B) Modification using time-sharing-techniques

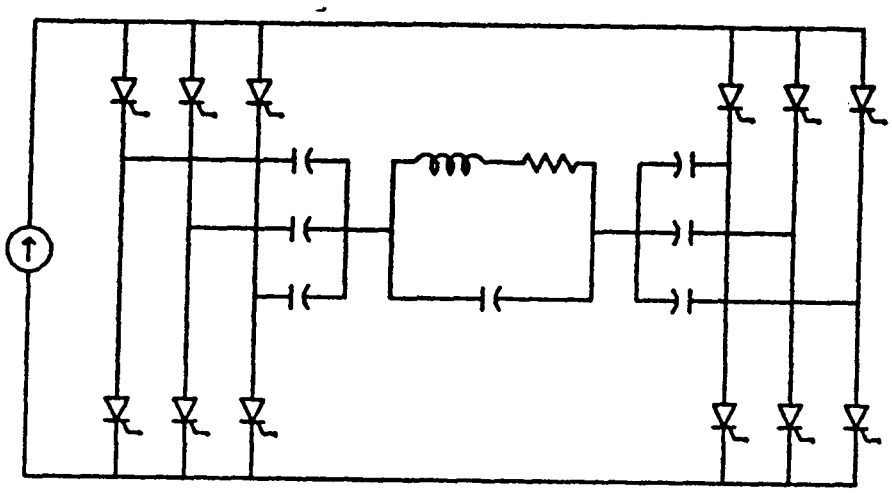
A time-sharing resonant inverter circuit (sometimes referred to as the sequential inverter) consists of parallel connected multiple stages of conventional inverters with a common load. The fundamental frequency of each subunit is a submultiple of the inverter output frequency.

Many authors have successfully applied the technique of time-sharing systems to some conventional thyristor inverters and developed new time-sharing inverter topologies to overcome the operating limitations of the thyristor turn-off time [37]-[51].

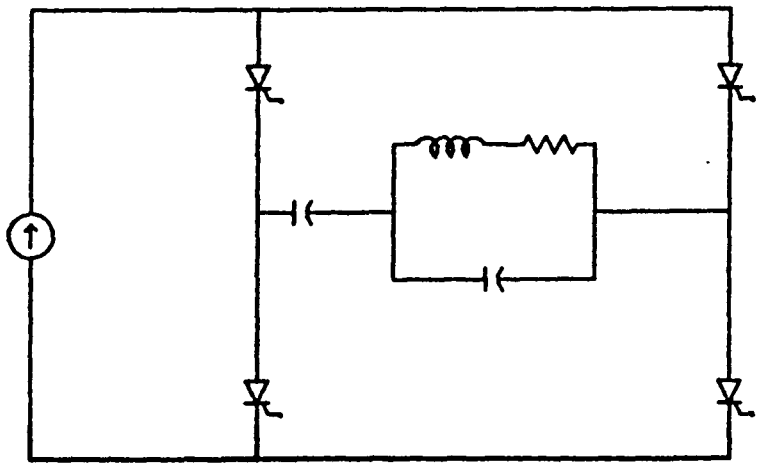
The following example can be used to illustrate the principle of time-sharing. Consider the series commutated capacitor time-sharing inverter shown in Fig. 2-18a. The inverter consists of three stages of the conventional current source inverter that has been analyzed by Revankar and Gadag [7] (Fig. 2-18b). Fig 2-19 shows the thyristor voltage waveforms for the two inverters when they are operated at the same power level and output frequency. The switching frequency of the thyristors in the conventional inverter is three times higher than that of the time-sharing inverter, so the turn-off margin for a time-sharing inverter is higher than that of a conventional inverter. The allowable

InductEV, Inc.
Exhibit 1014
Page 042

inverter is higher than that of a conventional inverter. The allowable thyristor turn-off time (duration of the negative voltage) for the time-sharing inverter above is about six times that of the conventional inverter.



(a) Time-sharing inverter (3 stages)



(b) Conventional inverter

Fig. 2-18 Current-fed, full bridge, series-parallel load, time-sharing inverter and its corresponding conventional inverter

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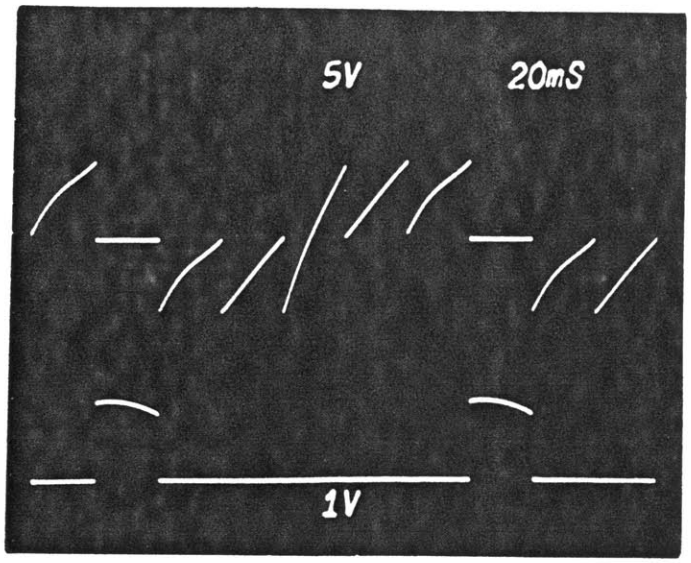
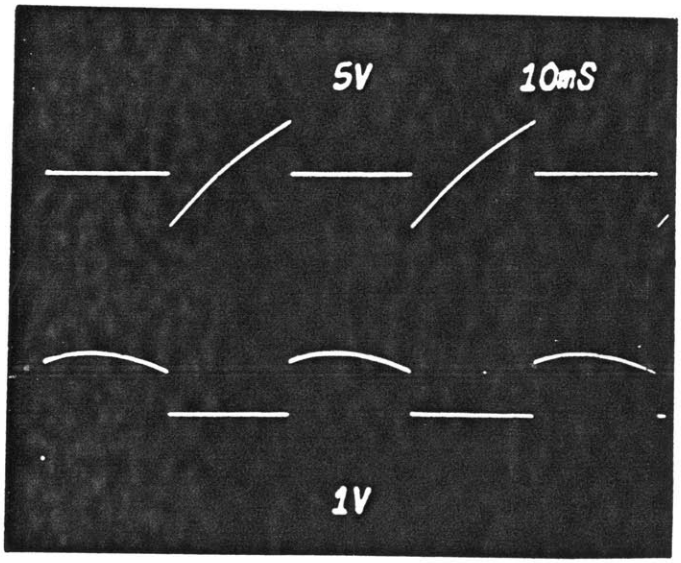
Exhibit 1014
Page 043



(a) Time-sharing inverter (3 stages)



(b) Conventional inverter

For both inverters:
upper trace :thyristor voltage lower trace : thyristor current

Fig. 2-19 Comparison of thyristor turn-off time for time-sharing and conventional inverters (simulation results)

InductEV, Inc.
Exhibit 1014
Page 044

(i) Time-sharing inverter subunits

Time-sharing subunits are circuits that are used to build time-sharing inverters. An attempt to classify these subunits has been made by Nakaoka et al. They divide the subunits into three types, as follows [49].

(i) Four-terminal switching coupling assemblies. These are combinations of subinverters composed of a switched capacitor and a reactor [44], [46], [47], [49].

(ii) Three-terminal switching coupling assemblies. These are combinations of multiple three terminal switched-capacitor with/without a reactor or a transformer [40]-[42], [49], [51].

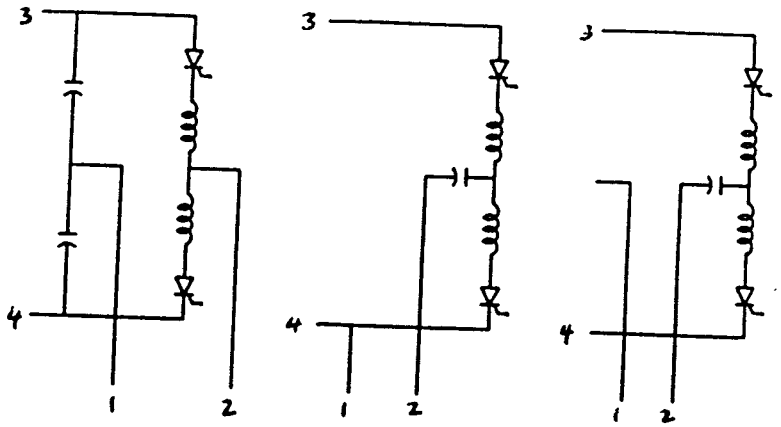
(iii) Two-terminal sub-chopper coupling type. These are combinations of multiple sub-choppers composed of two terminal switched capacitors with/without a reactor [49], [50].

Examples of the three types are shown in Fig. 2-20. The authors do not show what principles yield these subunits. In other words, it is not shown by the authors that the subunits they derived give all the possible or reasonable combinations of switches and reactive elements.

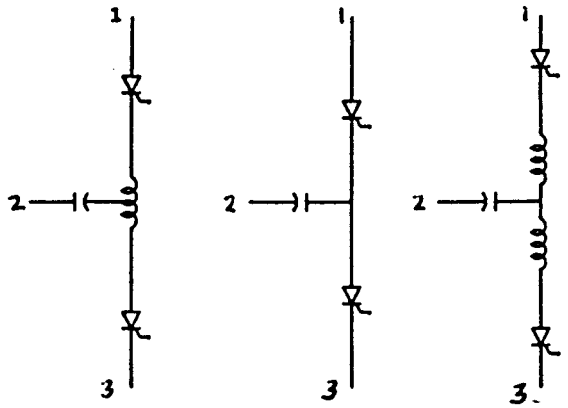
(ii) Time-sharing techniques

The development of time-sharing inverters has focused on new techniques of time-sharing. These techniques have used either a multi-winding transformer, or a commutating capacitor in series with the load, or a hybrid of the two. The two methods are illustrated by examples given below.

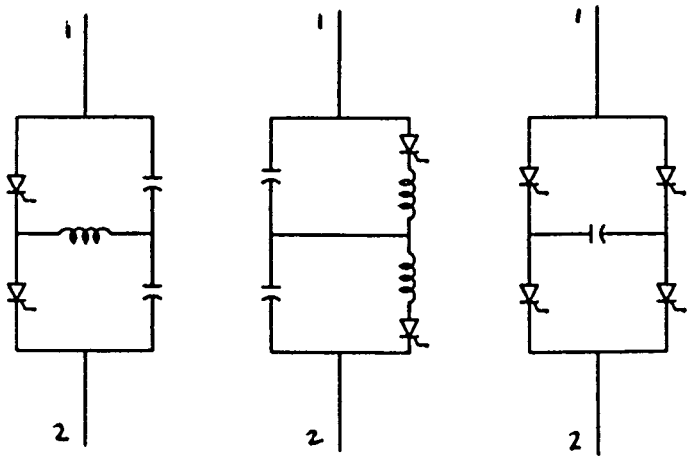
InductEV, Inc.
Exhibit 1014
Page 045



(a) Four-terminal time-sharing subunits



(b) Three-terminal time-sharing subunits



(c) Two terminals time-sharing subunits

Fig. 2-20 Time-sharing inverter subunits

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Exhibit 1014
Page 046

(a) Multi-winding transformer technique

This technique can best be illustrated by two examples of time-sharing inverters that have been presented in the literature. Thompson [38] has analyzed a four terminal time-sharing version of the conventional inverter he analyzed in [5]. Fig. 2-21. shows the time sharing inverter and its waveforms.

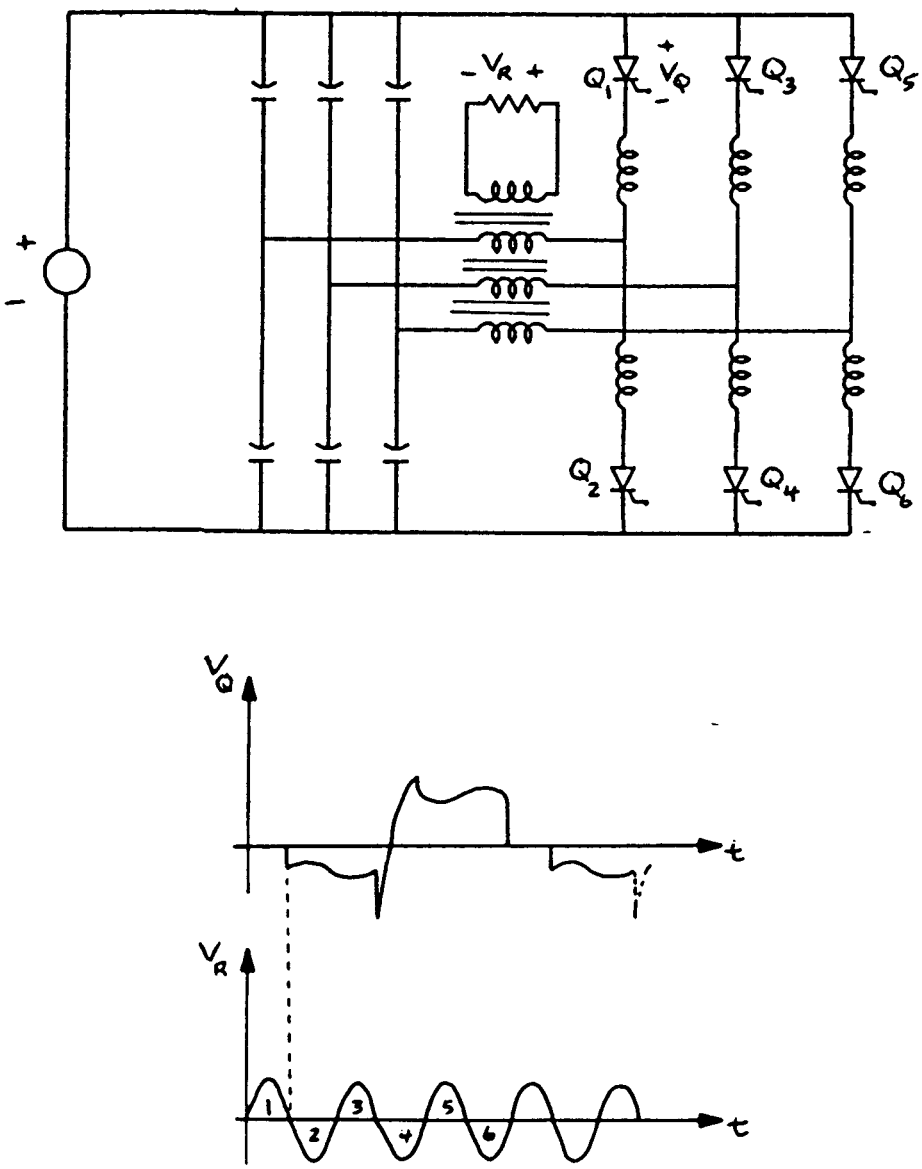

Fig. 2.21 A three-stage, four terminal, voltage-fed, time-sharing inverter using Multi-winding transformer technique [5]

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Exhibit 1014
Page 047

The inverter uses a transformer with three primaries and a common secondary. The thyristors labelled Q1 through Q6 are turned on in the order that they are numbered. The upper waveform shows the voltage across each thyristor, and the lower waveform shows the voltage across the load resistance R. The frequency of the load voltage is three times the frequency of the scr voltage. The change of polarity in the secondary voltage, when reflected to the primary, helps to extend the allowable turn-off time. In this case a turn-off time of two and a half cycles of the output frequency is achieved. Thompson reported that with the addition of a fourth stage a turn-off time of three and half cycles is achieved. Consequently the time-sharing inverter can be operated at a frequency three or four times higher than the frequency of the conventional inverter.

Another inverter that uses the multi-winding transformer technique is shown in Fig. 2-22 [39]. The switch used is a thyristor, but the symbol used for it is old and is no longer used. It is not changed here because the figure is a copy of the one used in [39]. With five stages, the turn-off time is improved by an order of magnitude or more, over that of a single stage inverter. A longer turn off time could be obtained by adding more stages. However, the output power decreases, as shown in the Table of Fig. 2-22.

An example of a current-fed inverter that uses the multi-winding transformer technique was presented by Shioya [44]. However the operating frequency range of the inverter was not presented. The inverter uses the same principles and structure as the voltage-fed inverter presented by Mapham [39]. A comparison of the two inverters would be of interest.

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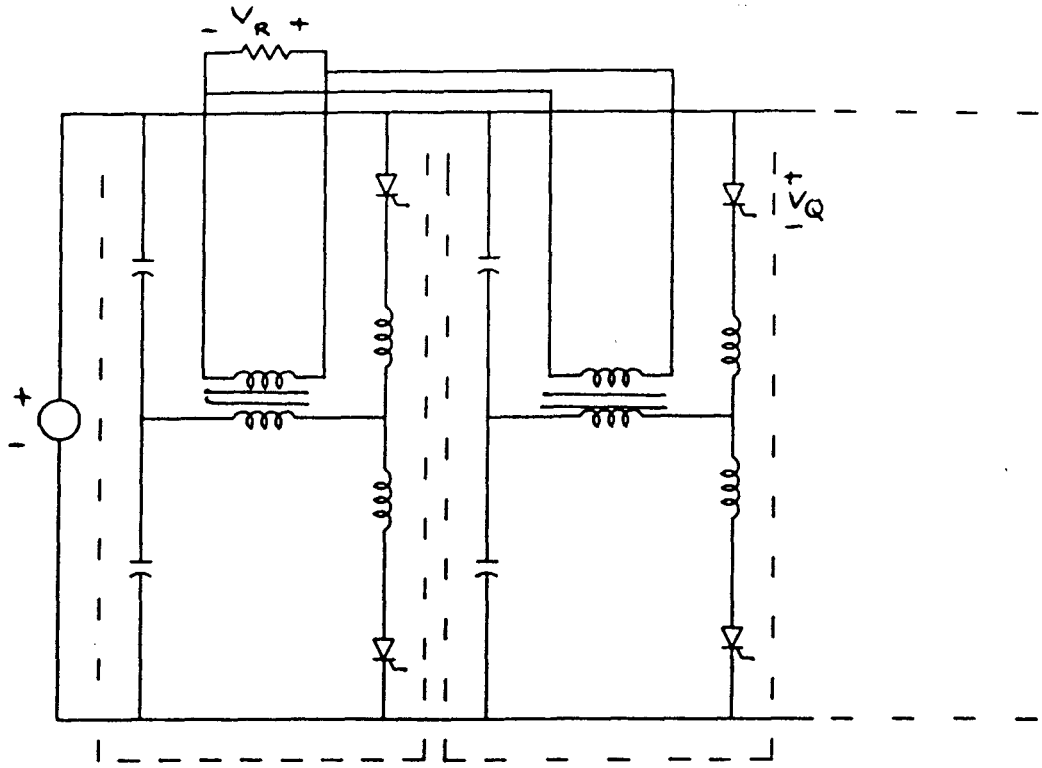
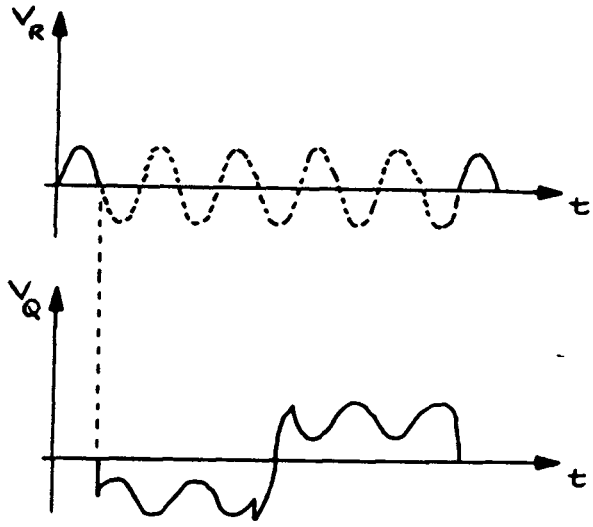
Exhibit 1014
Page 048





Frequency in kHz	Power in kw
10	30
20	23
30	19
40	16
70	10
100	7

Fig. 2-22 A five stage voltage-fed, time-sharing inverter using multi-winding transformer technique [39].

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Exhibit 1014
Page 049

(b) Series-commutated capacitor technique

Another technique used in time-sharing is the series commutated capacitor method. Fig. 2-18, shown earlier, is an example of the series commutated capacitor time-sharing inverter. The inverter has been discussed by many authors [42], [45], [50].

Time-sharing inverters that use a combination of the multi-winding transformer and series commutated capacitor techniques have been presented in [40].

(5) Summary and Conclusions

To summarize this literature review, most analyses of resonant converters have focused on solving the periodic steady state of the inverter to find the frequency and power ranges as functions of load parameters such as the Q-factor or the characteristic impedance. Also, improvement in frequency range has been achieved through modifying conventional inverter topologies using time-sharing techniques.

In the area of conventional resonant converters, the work that needs to done can be summarized by the following two points:

(i) There is a need to develop systematic methods for deriving resonant converter topologies. This will help to link the whole set of existing topologies together and aid the exploration of new topologies.

(ii) There is a need to study the dynamics of resonant converters. This will help in deriving mathematical models that will describe exactly the dynamics of these converters under varying operating conditions and enable the design of feedback compensators for improving the dynamic response of resonant converters.

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Exhibit 1014
Page 050

In the area of time-sharing inverters, some work remains to be done on the following topics:

(i) complete the analysis of other time-sharing inverters that have not been considered so far;

(ii) compare device and component ratings of time-sharing inverters and their corresponding conventional inverters;

(iii) compare different time-sharing inverter structures with respect to component ratings, operating frequency and power ranges;

(iv) determine the limitations on frequency and power of some conventional or time-sharing inverters using other new power switching devices, such as reverse-conducting thyristors (RCT), gate-turn off devices (GTO), static induction thyristors or transistors (SITH or SIT), gate assisted turn-off thyristor (GATT); Some applications of these device are in [49], [50].

The purpose of this thesis is to explore areas of conventional resonant converters that have not been studied before. In particular, we focus on the synthesis of resonant converters, their dynamic modeling, and their control.

There has been no attempt in the literature to derive conventional converter topologies in a systematic way. We need to develop whole classes of possible resonant converter topologies. This could eventually lead to the discovery of new converters. We shall discuss this in detail in Chapter III.

Until recently, the dynamic modeling of resonant converters has not been considered in the literature. Vorperian has obtained dynamic models for the series and parallel resonant converters of Figs. 2-13 and

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Exhibit 1014
Page 051

2-14 [62], [72]. The increased use of resonant converters prompts a need to develop dynamic models. Such models help in designing closed loop controllers for resonant converters. The results of some simulation experiments, using the Parity Simulator [69] to study the dynamics of the series resonant converter of Fig. 2-13, drew our attention to the necessity of exploring the dynamics of resonant converters. The dynamic modeling of resonant converters, together with the results of tests on the series resonant converter, are presented in Chapter IV. Results of feedback control of a resonant converter using the model developed in chapter IV will be discussed in Chapter V.

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Exhibit 1014
Page 052

CHAPTER III

SYNTHESIS OF RESONANT CONVERTERS

(1) Introduction

In the past decade several new resonant converter topologies have been developed [7], [15] - [16], [20] - [23]. It is natural to ask whether there are still further topologies for resonant converters, and how they are related to the existing ones. To answer this question, general laws and concepts that underlie the converter topologies need to be established, as the classification of resonant converter topologies is at present very loose. In this chapter we shall discuss some of the methodologies that can help in a systematic development of resonant converter topologies. In Section 2 we shall develop a switching cell from which the basic resonant converter topologies are derived. In Section 3 the symmetry properties of resonant converter topologies are used to derive other topologies. In Section 4 we shall derive additional resonant converter topologies using duality relationships, and contrast aspects of dual converters.

(2) Derivation of the Basic Topologies

A resonant converter can be divided into three parts: an input source, a switching network, and a resonant load that includes the resonant tank circuit (reactive elements) and a single resistor across which the output variable (voltage or current) is defined. Fig. 3-1 shows the three parts. We are assuming that the three parts can be separated from each other. Although this separation is not possible in some cases, using it here will allow us to suggest a switching cell from which three basic configurations are derived.

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Page 053

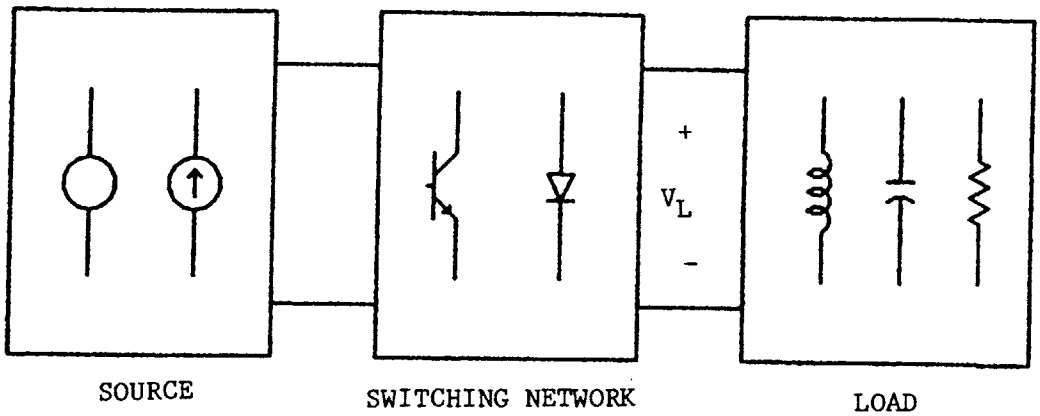

Fig. 3-1 The parts of a resonant converter parts

Now we need to derive the switching network that connects the source to the load, and develop the possible resonant loads that can act as the load in Fig. 3-1. Although we shall use a voltage source, the procedure when a current source is used is similar. If we assume the switching network contains only ideal switches, then the voltage V_L, across the resonant load, in Fig. 3-1, can have one of three values: V_{dc}, zero or $-V_{dc}$. The waveforms of V_L depend on the state of the switches and the order in which they are turned on and off during the switching cycle. For example, if a converter has two switching configurations during a switching cycle, then the possible waveforms for V_L are those shown in Fig. 3-2. In each case the voltage is a square wave which may or may not have a dc component. The waveform of Fig 3-2a has a positive dc component and in Fig. 3-2b the dc component is negative. When V_{dc} is symmetrically applied to the load, V_L will have no dc component, as shown in Fig. 3-2c. T_s is the period with which the

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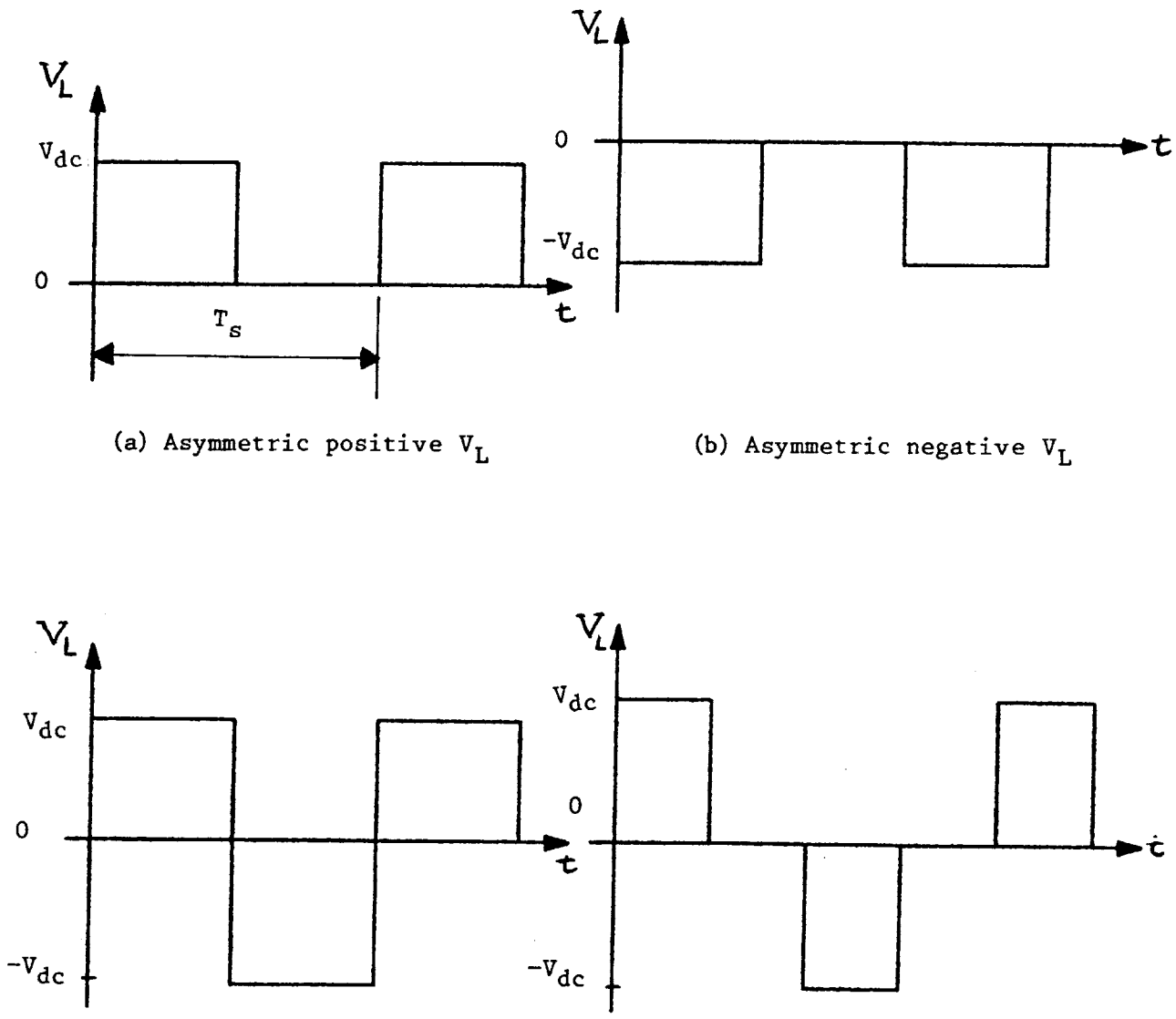
Page 054

switching network goes through a complete cycle. In this case there are two switching configurations during a switching cycle. Symmetric waveforms that have intervals of zero voltage across the load are possible as shown in Fig. 3-2d.



(a) Asymmetric positive V_L

(b) Asymmetric negative V_L

(c) Symmetric V_L

(d) Symmetric V_L with intervals of zero

Fig. 3-2 Waveforms of the voltage V_L of Fig. 3-1

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Exhibit 1014
Page 055

Fig. 3-3 shows a switching cell that can be used to obtain the waveforms of Fig. 3-2 or any combination of them, and Table 3-1 shows the switch combinations that give the waveforms of V_L.

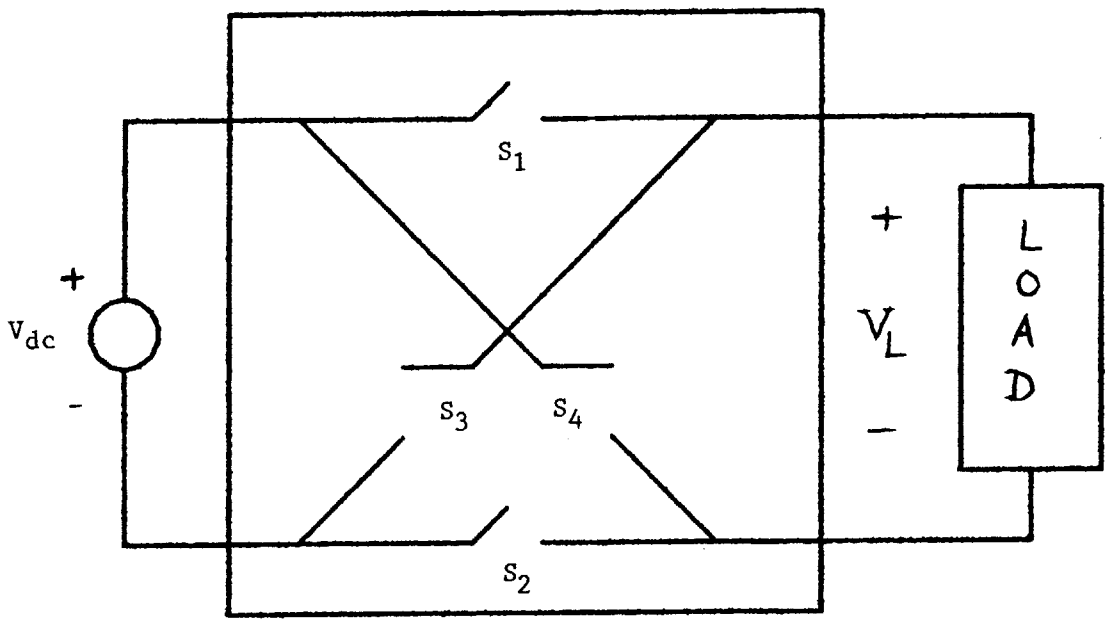

Fig. 3-3 A switching cell for deriving resonant converter topologies

V_L	Switch combinations and state
+ V_{dc}	(a) S_1 and S_2 closed and S_3 and S_4 open
0	Either (b) S_2 and S_3 open and S_1 and S_4 closed
	Or (c) S_2 and S_3 closed and S_1 and S_2 open
- V_{dc}	(d) S_1 and S_2 open and S_3 and S_4 closed

Table 3-1 Switch combinations for the waveforms of V_L of Fig. 3-4

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Exhibit 1014
Page 056

We next need to find the topologies that combine the waveforms of Fig. 3-2 with the switch combinations of Table 3-1. There are two basic converter structures that can be developed. In the first one the dc input voltage is asymmetrically applied to the load, or V_L takes the waveforms in Fig. 3-2 a or b. The resulting topology will be referred to as the **asymmetric topology**. In this topology there is always a dc offset voltage across the load. In the second one the input dc voltage is symmetrically applied to the load, or V_L takes the waveforms of Fig. 3-2c or d. In this case there is no net dc voltage across the load. This topology will be referred to as the **symmetric topology**.

(A) The asymmetric topology

Now let us synthesize the topology for which V_L has the waveforms of Fig. 3-2a and b. In Fig. 3-2a we have a positive voltage V_{dc} during one half of the switching cycle and zero voltage during the other half. In this case the dc component of the voltage across the load is positive and equal to half of the input dc voltage. From Table 3-1 there is one switch combination that gives a V_L of $+V_{dc}$, and two switch combinations that give zero voltage across the load. Therefore two topologies can be synthesized to generate the waveforms in Fig. 3-2a These are shown in Fig. 3-4. Although the topologies are obtained through different switch implementations, they should not be considered as different topologies.

Topology 1 is synthesized by switch combinations **a** and **b** of Table 3-1. The switch S_1 is not shown in the topology because it is closed during both modes, and therefore represented by a short circuit and no switch is needed for S_1. Also S_3 is not shown because it off all the time and is represented by an open circuit or completely eliminated from

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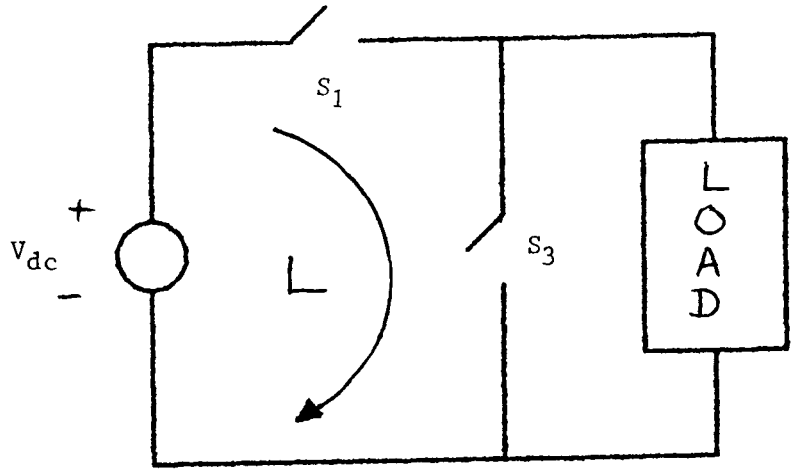
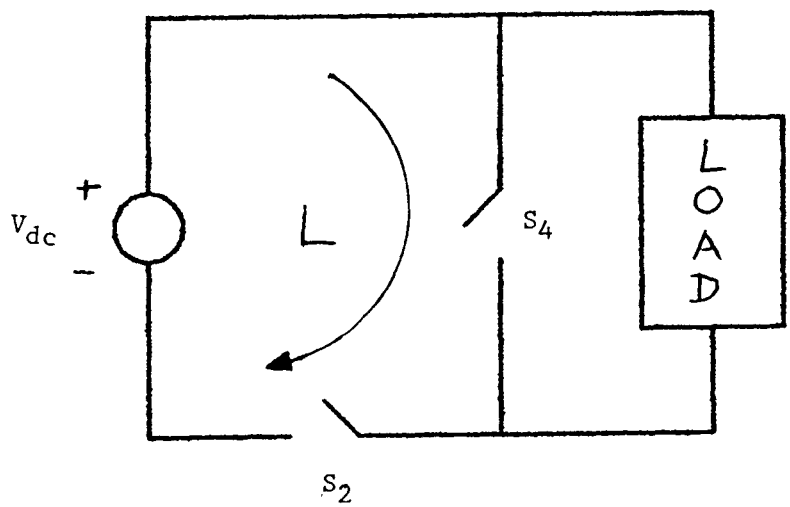
Exhibit 1014
Page 057



(a) Topology 1



(b) Topology 2

Fig. 3-4 The asymmetric voltage-fed topology

the circuit. Therefore we need only two switches S_2 and S_4.

Similarly Topology 2 is synthesized by the switch combinations **a** and **c** of Table 3-1. In this case S_2 is closed during both modes, and it is represented by a short circuit. Therefore only S_1 and S_3 are needed. In the two topologies the switches S_1 and S_2 only differ in their

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Exhibit 1014
Page 058

positions in the loop L, and they will have the same voltage and current waveforms. Therefore the circuit operation for the two topologies is identical, and they should not be considered as different topologies. The position of the switches S_1 and S_2 is an implementation issue which has an effect on the drive circuit that controls each of them, as will be clear when we discuss the implementation of the switch.

The asymmetric topology can also be synthesized from the waveforms of Fig. 3-4b, where V_L is either negative or zero. From Table 3-1 there is one switch combination that gives a negative V_L, and two switch combinations that give zero V_L. Two topologies can be realized using these switch combinations. The two resulting topologies are the same as those of Fig. 3-4, except for the obvious interchange of the switches in series and parallel with the load. Again one can go through the same arguments as in the previous paragraph and show that the two topologies are not different, and therefore the above the topologies formed by using different switch combinations, for both asymmetrical positive or negative waveforms, all represent the same topology. The different switch positions only affect the switch control circuit.

(B) <u>The symmetric topologies</u>

Symmetric topologies are derived from waveforms that have the dc input voltage symmetrically applied to the resonant load. Assuming two switching configurations per cycle, V_L has the waveform of Fig. 3-2c. This waveform can be achieved using switch combinations **a** and **d** of Table 3-1. The resulting topology is shown in Fig. 3-5. It uses four switches in a bridge connection, and will be referred to as the **<u>full bridge topology</u>**.

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Exhibit 1014
Page 059

The full bridge topology can also be synthesized from the waveforms of Fig. 3-2d, where there are switching intervals where the load voltage is zero. This can be obtained turning on either the upper two switches (S_1 and S_2) or the lower switches (S_3 and S_4) in Fig. 3-5 . Variation of the interval of zero voltage across the load is another way of controlling the power delivered to the load.

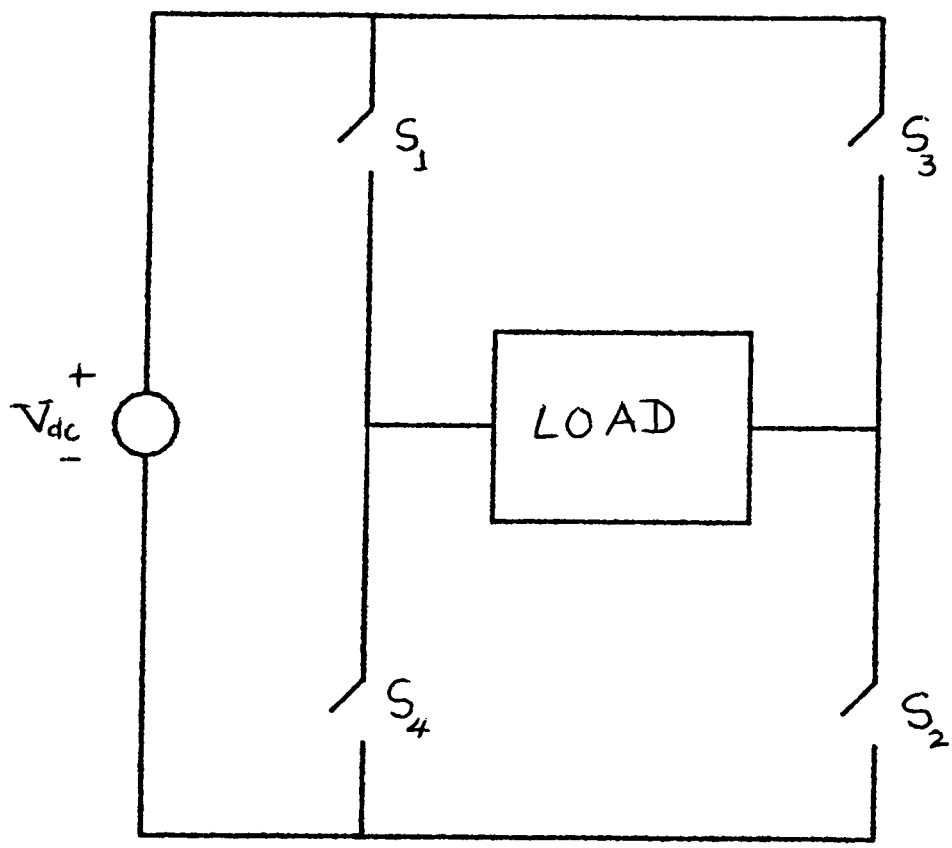

Fig. 3-5 Full bridge voltage-fed topology

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Exhibit 1014
Page 060

A symmetric square wave voltage across the resonant load can also be obtained by using two voltages connected to a common load via two switching cells, as shown in Fig. 3-6.

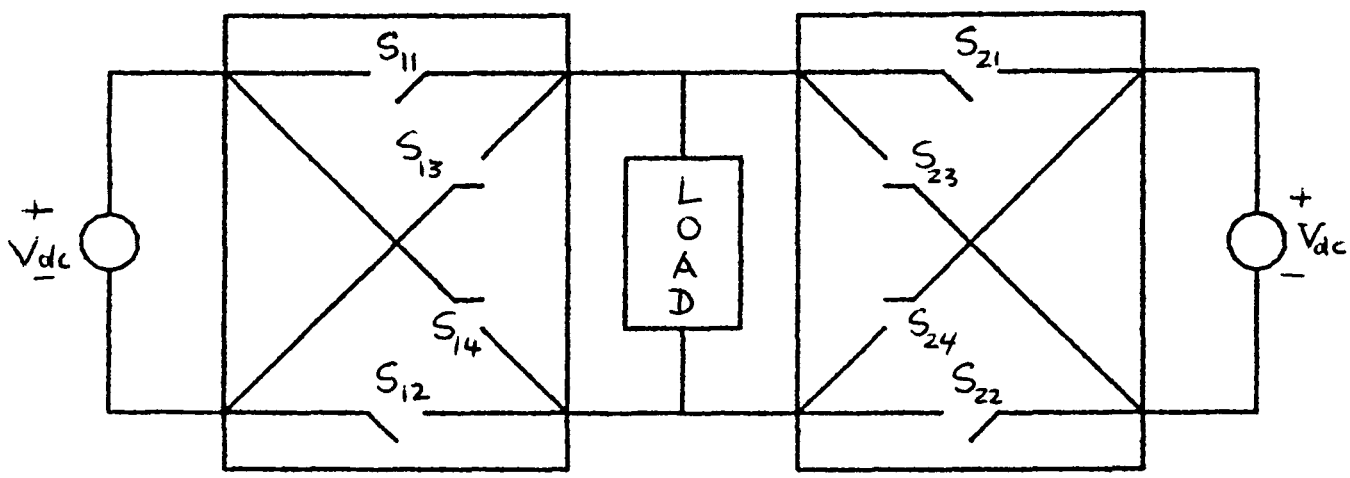

Fig. 3-6 Voltage-fed topologies using two sources and two switching cells

There are two numbers associated with each switch. The first number refers to the switching cell, and the second number refers to the switch number in the cell. From Table 3-1, the switch combination **a** (S_1 and S_2 closed) is used when the voltage across the load is $+V_{dc}$, and switch combination **d** (S_3 and S_4 closed) is used when the voltage across the load is $-V_{dc}$. The resulting topology is shown in Fig. 3-7.

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Exhibit 1014
Page 061

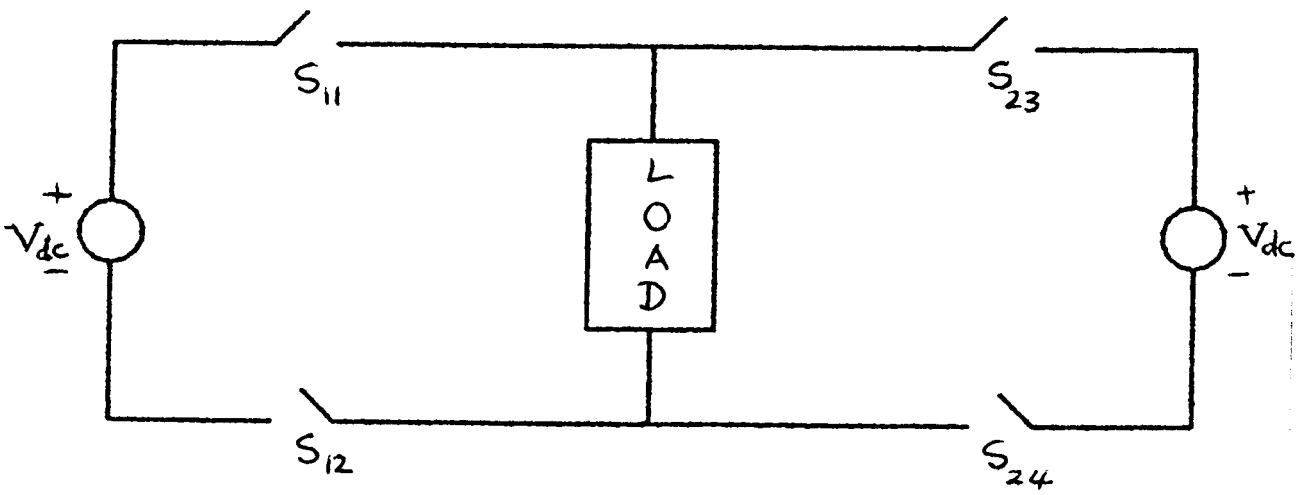

Fig. 3-7 Symmetric topology using two voltage sources

The switches S_{11} and S_{12}, in Fig. 3-8, are connected in series in the same loop. Therefore they can be combined in one switch. Likewise switches S_{23} and S_{24} are connected in series in the same loop, and they can be combined in one switch. Depending on which switch is eliminated in each loop there are four switch implementations for this topology, but four configurations differ only in the control circuit that drive the switches. They should thus be considered as one topology, the one shown in Fig. 3-8a. The resulting symmetric topology differs from the full bridge topology in that it uses two voltage sources and two switches instead of one voltage source and four switches. This topology will be referred to as the **half bridge topology**. This topology is sometimes implemented with one voltage source and two equal capacitors, as shown in Fig. 3-8b.

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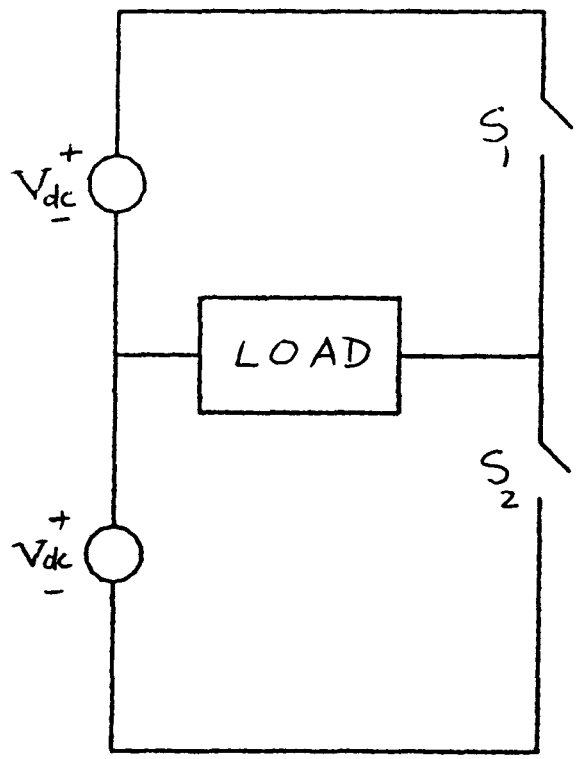
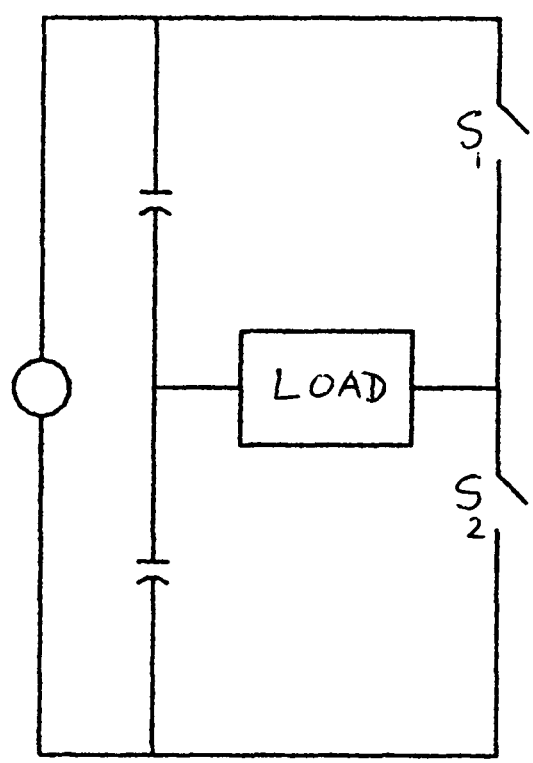
Page 062



(a) Using voltage two sources



(b) Using one voltage source

Fig. 3-8 Half bridge voltage-fed topology

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Exhibit 1014
Page 063

A half bridge topology with a load voltage corresponding to Fig. 3-2d, where there is are intervals of zero voltage across the load, is shown in Fig. 3-9.

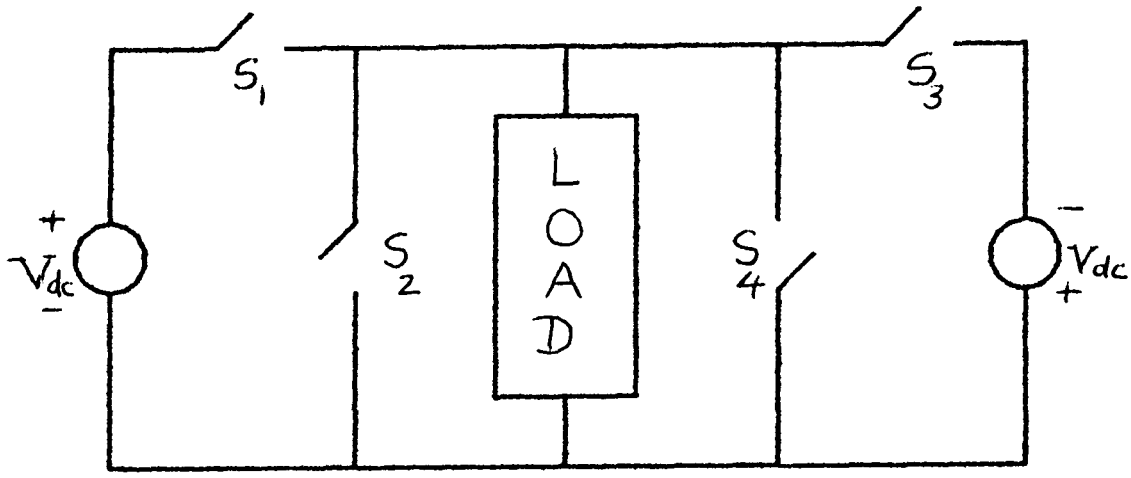

Fig. 3-9 Symmetric half bridge topology
with load voltage shown in Fig. 3-2d

The half bridge topology shown in Fig. 3-9 can be considered as two asymmetric converters connected to a common load. One asymmetric converter has the waveforms of Fig. 3-2a, and the other has the waveforms of Fig. 3-2b. If one of these waveforms is shifted by some angle $\emptyset^{\circ}$ with respect to the other, their sum will give the symmetric waveform of Fig. 3-2d. The three waveforms are also shown in Fig. 3-10. The phase shift angle $\emptyset$ can be varied from 0 to 180°. If the phase shift between the two waveforms is 180°, their sum would be equal to the symmetric waveform of Fig. 3-2c.

The switches connected in parallel with the load, in Fig. 3-9, are used only if zero voltage is needed across the load. This occurs when the phase shift between the added asymmetric waveforms is different from

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Exhibit 1014
Page 064

180°. When the phase shift is 180° the voltage across the load will never be zero and the switches in parallel with the load will be open all the times. In this case the resulting topology is essentially the same as the half-bridge topologies shown in Fig. 3-8.

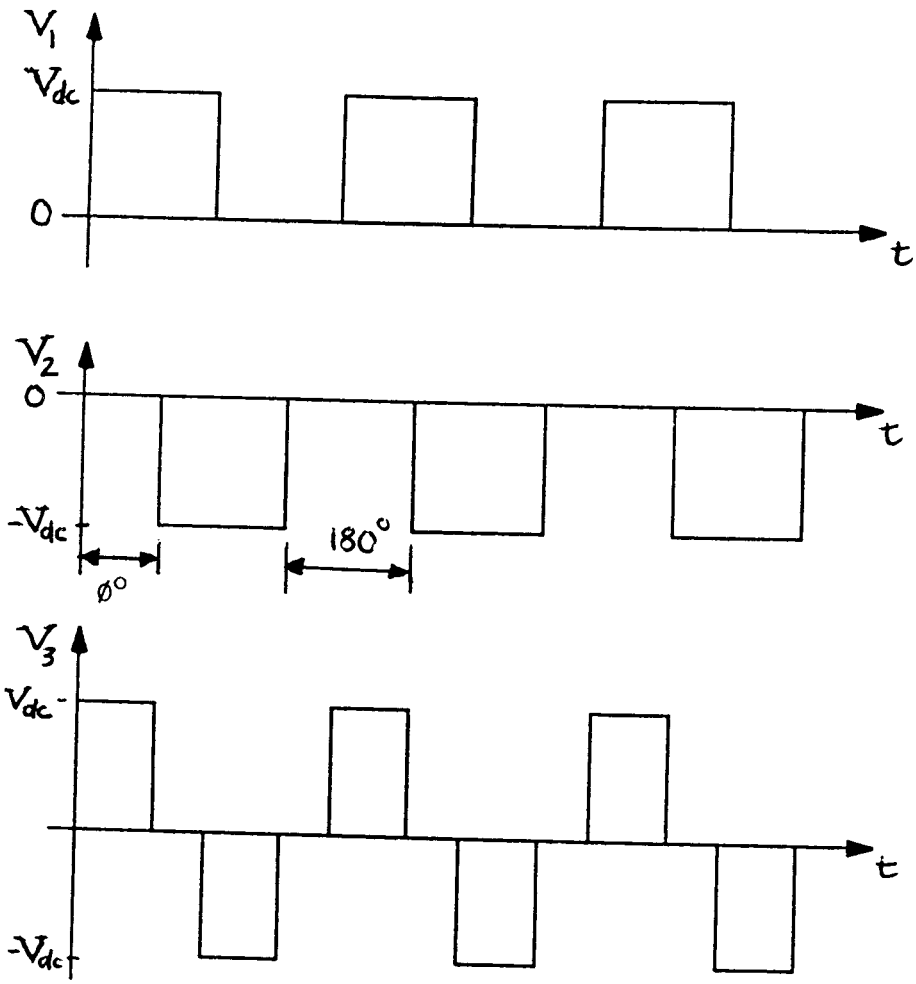

Fig. 3-10 Formation of a symmetric waveform from asymmetric waveforms

The variation of the phase shift from 0° to 180° is another way of controlling the power delivered to the resonant load from zero to full power. In this case the converter can operate at constant switching frequency, and hence a fixed ratio of the switching to the resonant frequency.

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Exhibit 1014
Page 065

We conclude this section by a few comparisons among the three basic topologies that we have derived. For the same dc input voltage, the switch voltage ratings of the half bridge are twice those of a full bridge, but they deliver the same power. Compared with the asymmetric topology, for the same value of the applied input voltage and load, the bridge topology delivers twice the power of the asymmetrical topology. The switch voltage and current ratings are the same for both topologies.

The topological relationships between the asymmetric topology, the full bridge topology and the half bridge topology are now obvious. One needs only to derive one topology, and the other topologies can be derived automatically using the trade off between the number of switches and the number of voltage sources, together with the symmetry relationships.

(C) Types of resonant loads

In this section we shall develop the kind of loads that can be used in the load block in Fig. 3-1. We will assume that the load consists of a single resistor, a single inductor and a single capacitor. There are then two basic types of load: the three components can be connected to form either a series resonant circuit or a parallel resonant circuit. The definition of a series or parallel load depends on the driving source. To illustrate this, let us consider the resonant circuits in Fig. 3-11. If each voltage source is replaced by a short circuit, and each current source is replaced by an open circuit, the resulting circuit will have the passive elements either connected in series (Fig. 3-11a) or in parallel (Fig. 3-11b).

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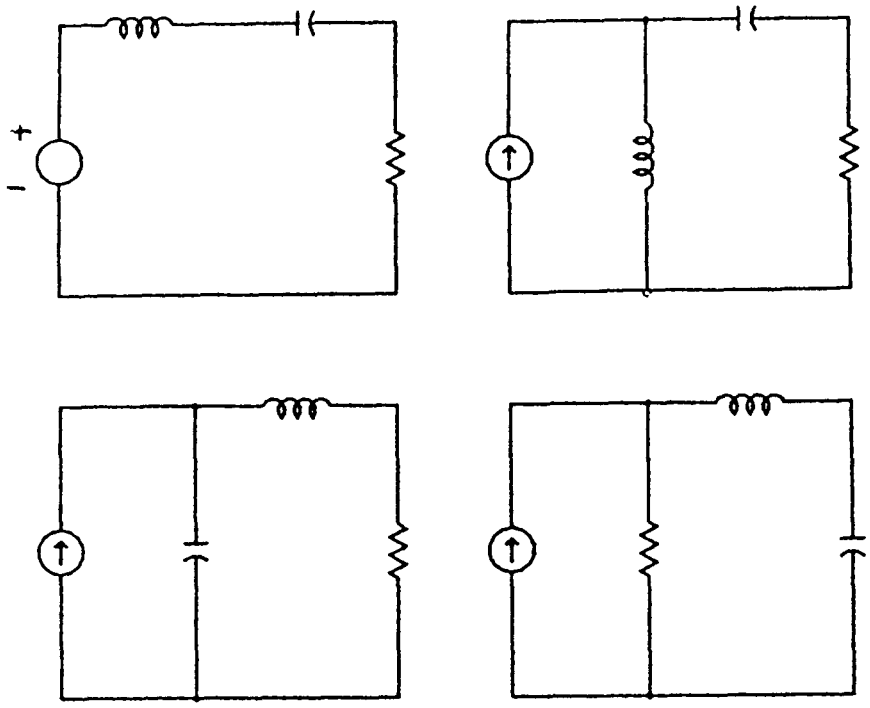
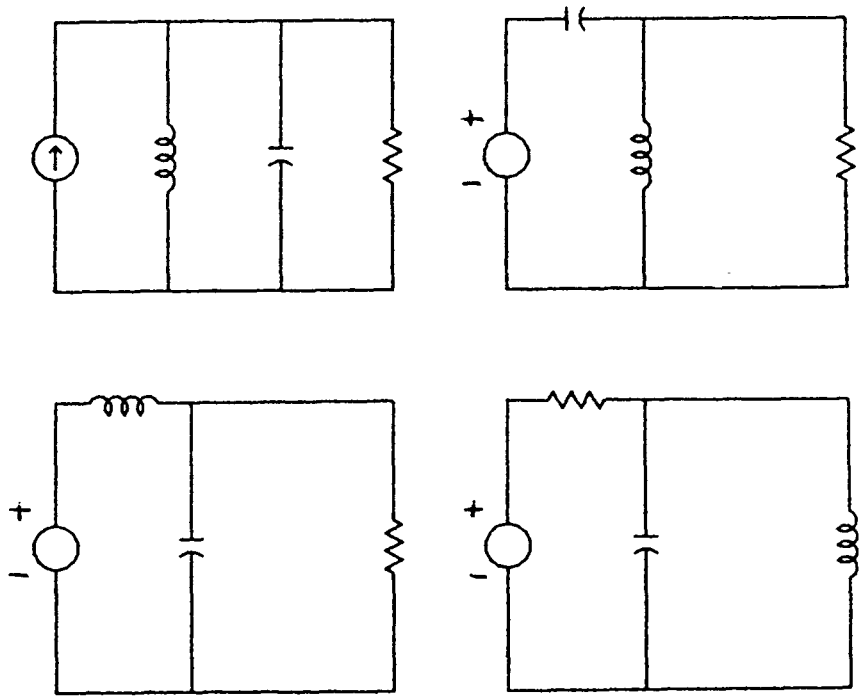
Exhibit 1014
Page 066



(a) Series loads



(b) Parallel loads

Fig. 3-11 Basic types of a resonant load

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Exhibit 1014
Page 067

We shall use the load type as a criterion for classifying the types of resonant converter topologies : the series converter topologies (when the load is a series resonant circuit) and the parallel converter topologies (when the load is a parallel resonant circuit). There are cases, as we shall see later, where the load is a combination of the two basic types.

For a voltage-fed converter there are three parallel loads and one series load, and for a current source there are three series loads and one parallel load. Fig. 3-12 shows examples of series and parallel half bridge voltage-fed topologies.

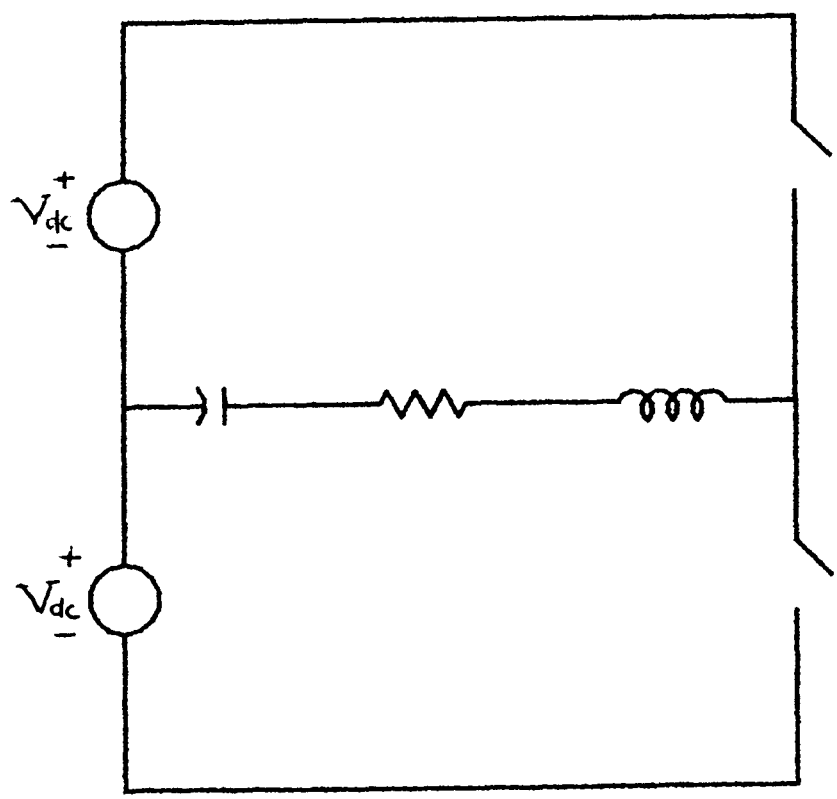

Fig. 3-12a A series half bridge topology

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Exhibit 1014
Page 068

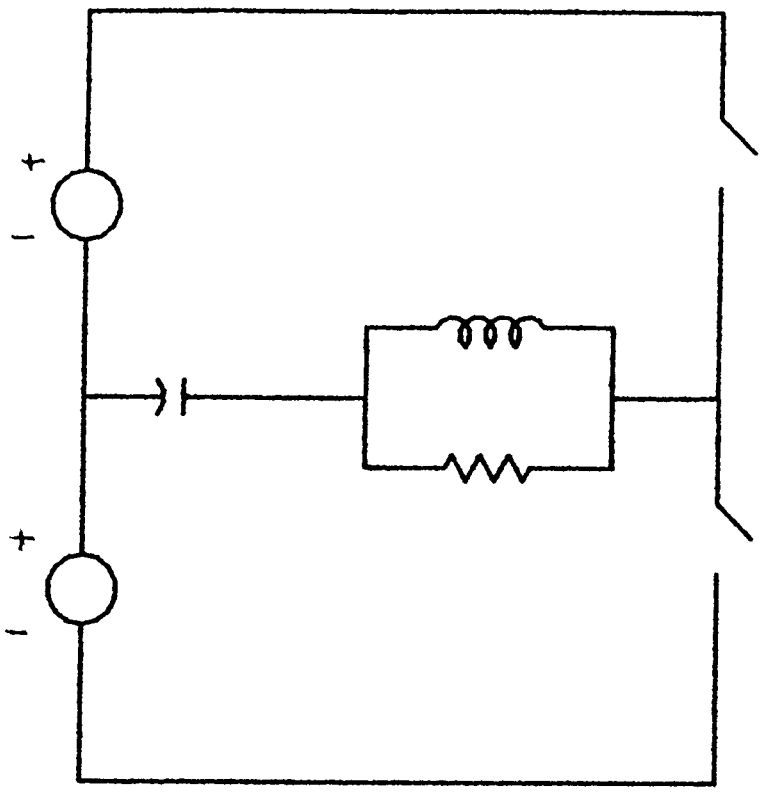

Fig. 3-12b A Parallel half bridge topology

A derivation of the basic resonant circuits using linear network theory is described in Appendix 3A. The loads that result from this analysis are also the series and parallel loads that are derived in this section.

Resonant converters with higher order filtering can also be developed. One systematic way to construct these filters using the basic series and parallel loads is to cascade the basic loads, by replacing the resistor in one load by another load. Examples of these cascaded loads are shown in Fig. 3-13.

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Exhibit 1014
Page 069

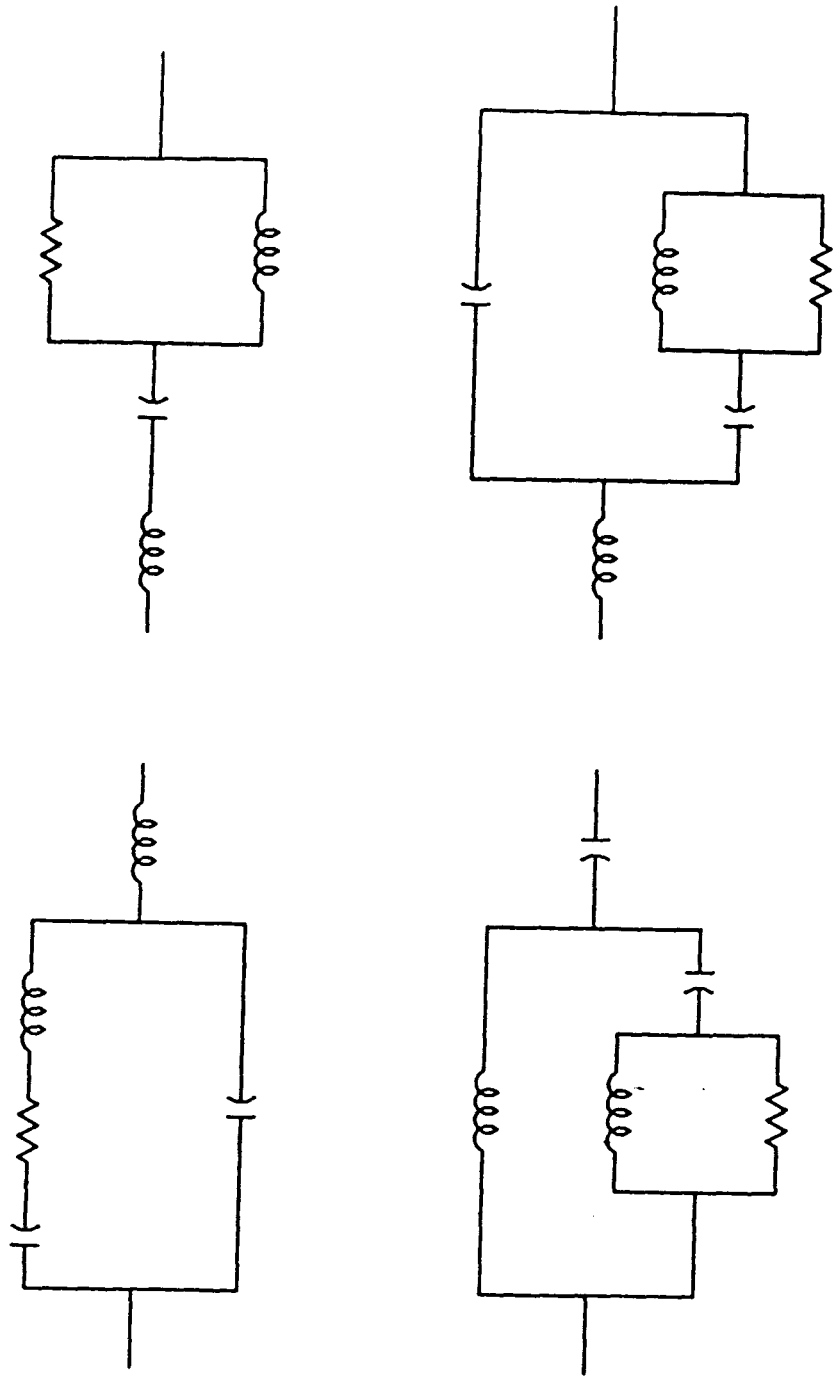

Fig. 3-13 Cascaded higher-order loads

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Exhibit 1014
Page 070

(D) Power flow and implementation of the switch

The direction of current in the switch is determined by the ratio of the switching frequency to the resonant frequency. If the impedance of the resonant circuit at the switching frequency is capacitive, the load current leads the load voltage. If the impedance of the resonant circuit at the switching frequency is inductive, the load current lags the load voltage. It is only when the switching frequency is equal to the resonant frequency that the resonant circuit impedance is resistive and the power factor is unity. Fig 3-14 shows the switch voltage and current, for a voltage-fed converter applied to a series load, as the switching frequency is varied. Whenever the switch is operated at a frequency different from the resonant frequency, the switch has to carry a bidirectional current. A unidirectional current switch can only be used when the switching frequency is equal to the resonant frequency. In other words, we can determine the switch type by considering the instantaneous power flow. Power can be delivered from the dc voltage to the load or vice-versa. In this case the input dc voltage can source or sink current, and a bidirectional switch is needed. If power flows from the dc voltage to the load all the time, then a unidirectional current switch is needed.

Fig. 3-15 shows the switch implementation for the asymmetric topology for both unidirectional and bidirectional power flow. For unidirectional power flow the switches have to be fully controlled (e.g. a transistor or a MOSFET). If diodes are used the dc source will be shorted, and hence no power will be delivered to the resonant load. An npn transistor will be used to represent a fully controlled switch throughout this chapter. In the case of bidirectional power flow, the

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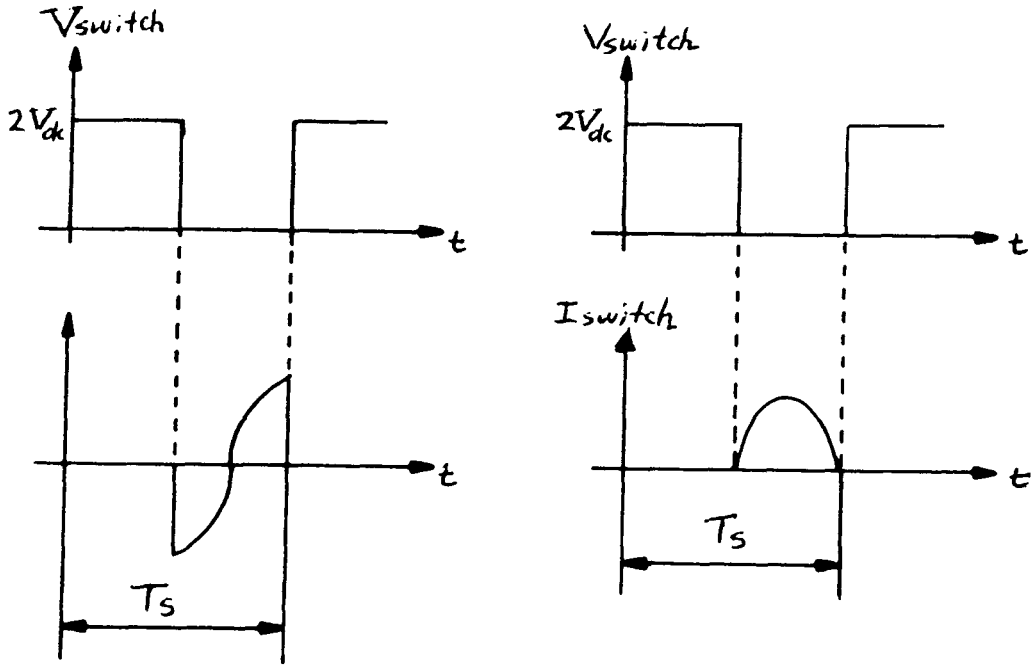
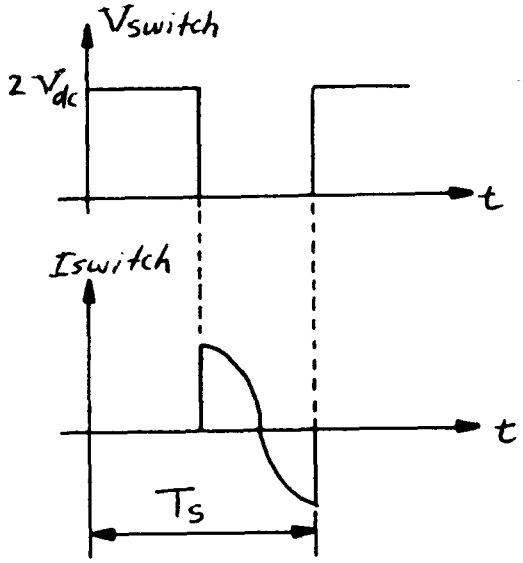
Exhibit 1014
Page 071

switch can be realized by a controlled switch with an antiparallel diode. The diode automatically conducts whenever the load voltage exceeds the input dc voltage.



(a) $f_s < f_r$ (b) $f_s = f_r$



(c) $f_s > f_r$

Fig. 3-14 Voltage and current waveforms of a switch in a series voltage-fed resonant converter

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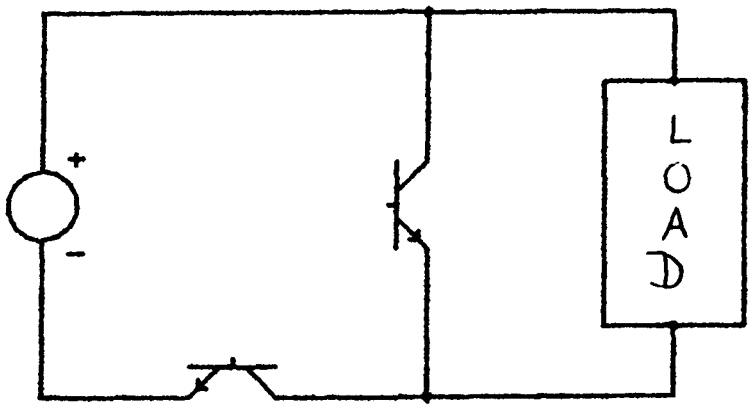
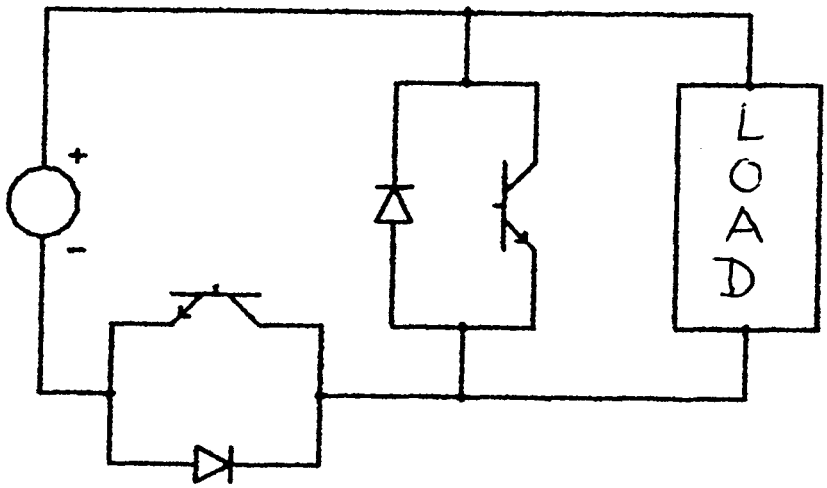
Exhibit 1014
Page 072



(a) unidirectional power flow



(b) bidirectional power flow

Fig. 3-15 Switch imlementations of the asymmetric topology

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Exhibit 1014
Page 073

(3) Parameters of Voltage-fed Resonant Converters

(A) Series topologies

In this is section and the following one we shall identify the parameters of the series and parallel voltage-fed topologies. As stated earlier, a resonant converter is characterized by its resonant frequency f_r, its quality-factor Q and its characteristic impedance Z_o. In this section we shall define these parameters for the series converter topologies.

A series voltage-fed topology has a series resonant circuit connected to a voltage source in each of its switching configurations, as shown in Fig. 3-16.

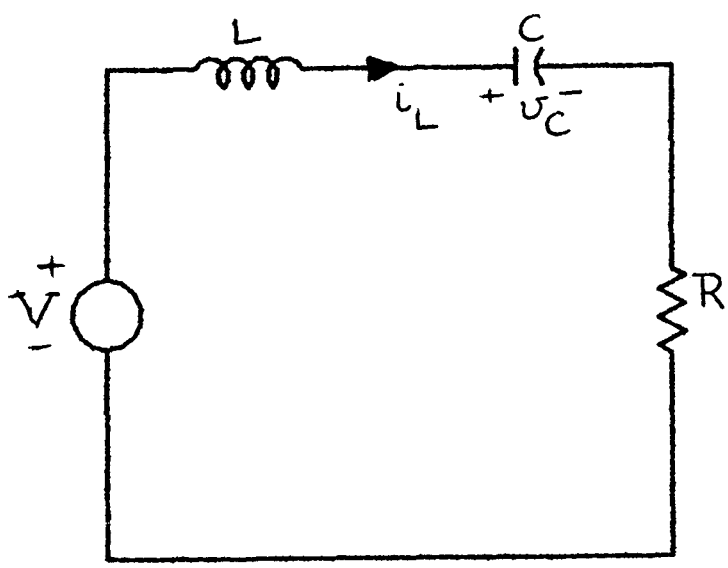

Fig. 3-16 A series voltage-fed resonant circuit

The circuit waveforms are those of an oscillatory underdamped second order system. Such a system is characterized by the second order differential equation below:

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Exhibit 1014
Page 074

$$\frac{d^2 x}{d t^2} + 2a \frac{d x}{d t} + w_r^2 x = K_x V \qquad (3.1)$$

where

x = a state variable such as inductor current or capacitor voltage

a = damping factor

w_r = resonant angular frequency = $2 f_r$

K_x = A constant for the state variable x

The Q-factor of such a circuit is defined as:

$$Q = \frac{w_r}{2 a} \qquad (3.2)$$

The frequency natural of oscillation w_d is not exactly at the resonant frequency, differing from it by an amount that depends on the value of the damping factor a and it is given by:

$$w_d = \sqrt{w_r^2 - a^2} \qquad (3.3)$$

If the state variables in the series resonant circuit are chosen to be the inductor current (i_L) and the capacitor voltage (v_C), then the differential equation for the inductor current is

$$\frac{d^2 i_L}{d t^2} + \frac{R}{L} \frac{d i_L}{d t} + \frac{i_L}{L C} = 0 \qquad (3.4)$$

and the differential equation for the capacitor voltage is

$$\frac{d^2 v_C}{d t^2} + \frac{R}{L} \frac{d v_C}{d t} + \frac{v_C}{L C} = \frac{V}{L C} \qquad (3.5)$$

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Exhibit 1014
Page 075

Comparing equations (3.4) and (3.5) with equation (3.1) we get

$$2a = \frac{R}{L} \tag{3.6a}$$

$$w_r = \frac{1}{\sqrt{L\,C}} \tag{3.6b}$$

$$K_i = 0 \quad , \quad K_v = \frac{1}{L\,C} \tag{3.6c}$$

and

$$Q = \frac{w_r}{2\,a} = \frac{L}{R\sqrt{LC}} = \frac{Z_o}{R} \tag{3.6d}$$

where $Z_o = \sqrt{L/C}$ = characteristic impedance of a resonant circuit

(B) <u>Parallel topologies</u>

When deriving the voltage-fed parallel converters, there are three possible resonant loads that should be considered, as shown in Fig. 3-17. When the voltage source is replaced by a short-circuit, the resulting circuits are identical, with the three elements of the resonant circuit connected in parallel. To differentiate between the three loads, we refer to them as types A, B and C.

In all three cases, the differential equation for i_L is

$$\frac{d^2 i_L}{d\,t^2} + \frac{1}{R\,C}\frac{d\,i_L}{d\,t} + \frac{1}{L\,C}\,i_L = f_i(V,R,L,C) \tag{3.7}$$

and the differential equation for v_C is

$$\frac{d^2\,v_C}{d\,t^2} + \frac{1}{R\,C}\frac{d\,v_C}{d\,t} + \frac{v_C}{L\,C} = g_i(V,R,L,C) \tag{3.8}$$

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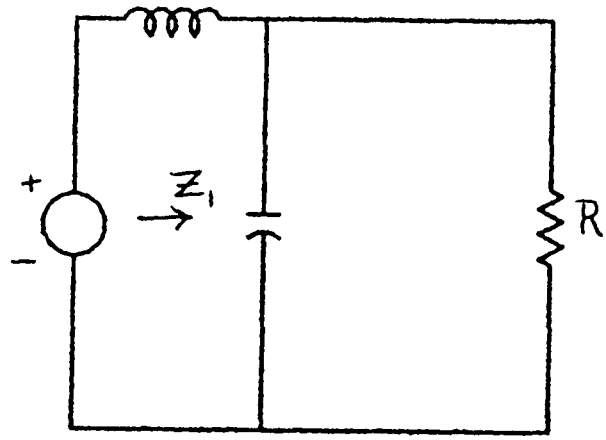
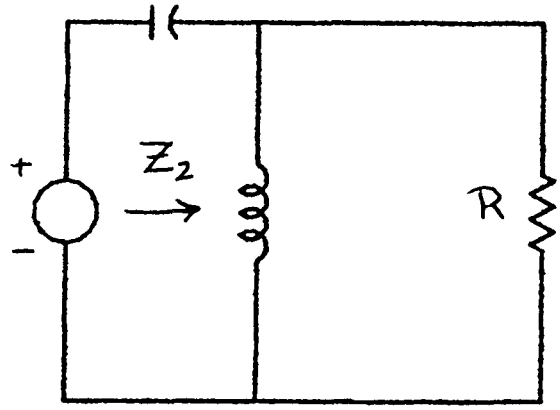
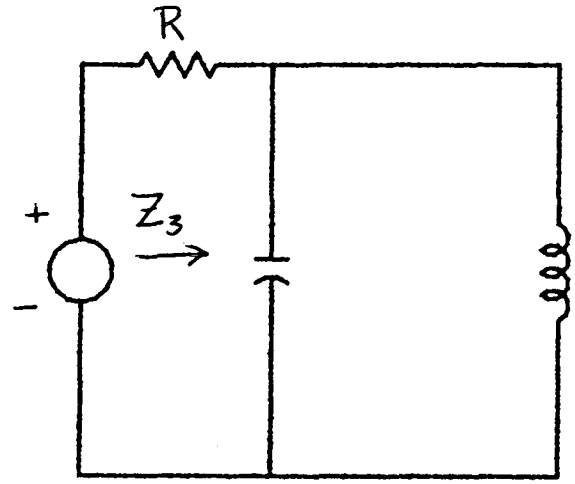
Exhibit 1014
Page 076



Type A





Type B Type C

Fig. 3-17 Voltage-fed parallel resonant loads

The right hand sides of equations (3.7) and (3.8) are different from one type to another. The subscript i on the functions $f_i(..)$ and $g_i(..)$ indexes type of the load. Also, the impedance $Z_i(s)$ seen by the source is also different in each case. The respective impedances as functions of frequency are shown in Fig. 3-18.

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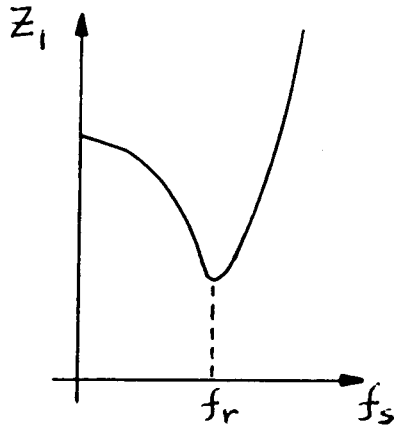
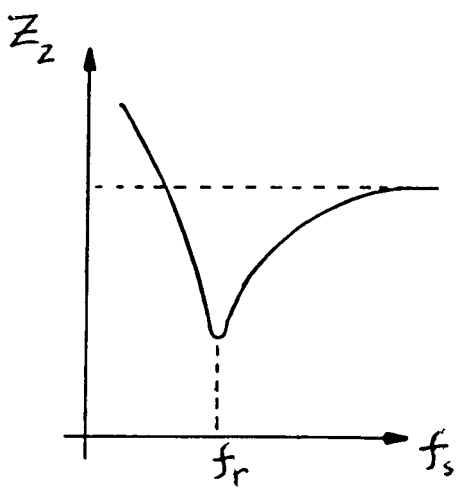
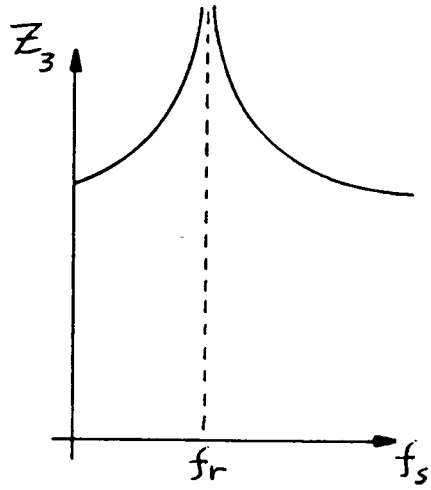
Exhibit 1014
Page 077



Type A





Type B

Type C

Fig. 3-18 Graphs of the impedance of the loads of Fig. 3-17

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Exhibit 1014
Page 078

Now comparing equations (3.7) and (3.8) with (3.1) we get

$$2a = \frac{1}{R\ C} \tag{3.9a}$$

$$w_r = \frac{1}{\sqrt{L\ C}} \tag{3.9b}$$

$$K_i = \frac{1}{R\ L\ C} \tag{3.9c}$$

$$K_v = \frac{1}{L\ C} \tag{3.9d}$$

and

$$Q = \frac{w_r}{2\ a} = \frac{R\ C}{\sqrt{LC}} = \frac{R}{Z_o} \tag{3.9e}$$

(4) Symmetry Derived Topologies

In this section we shall explore some topological symmetry properties to derive other resonant converter topologies. The half bridge topology (see Fig. 3-9) is symmetrically inverted about the load. In other words the load in Fig. 3-9 acts as a line of symmetry. All the components of the converter below the load are reflected about the load with their polarity being reversed. We shall refer to this reversed reflection as an **inverted mirror.** The motivation behind the use of an inverted mirror is that it starts with a circuit that cannot work as a resonant converter by itself, and changes it to a converting circuit. If the load is a single resistor, then the common branch between the two halves should always include that resistor and perhaps other components of the resonant load, but not the voltage source. Also, for power to be converted from dc to ac, a capacitor should not be placed in series with

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Exhibit 1014
Page 079

the voltage source, because a capacitor cannot have a dc current through it. Similarly, an inductor should not be placed in parallel with a current source.

Consider the series resonant circuit of Fig. 3-19. If we place the resistor, the inductor and the capacitor in the common branch, then by drawing an inverted mirror of this circuit we get the half bridge series inverter of Fig. 3-20a. If we place the resistor and the capacitor in the common branch, we obtain a half bridge inverter with two inductors, as shown in Fig. 3-20b. Thompson [5] referred to the topology in Fig. 3-20b as the twin choke converter[38]. We shall refer to it here as the **divided-inductor topology**.

We shall mention at this point that half bridge resonant converters obtained using symmetry also have asymmetric and full bridge topologies. For example, the divided-inductor asymmetric and full bridge topologies are shown in Fig. 3-21.

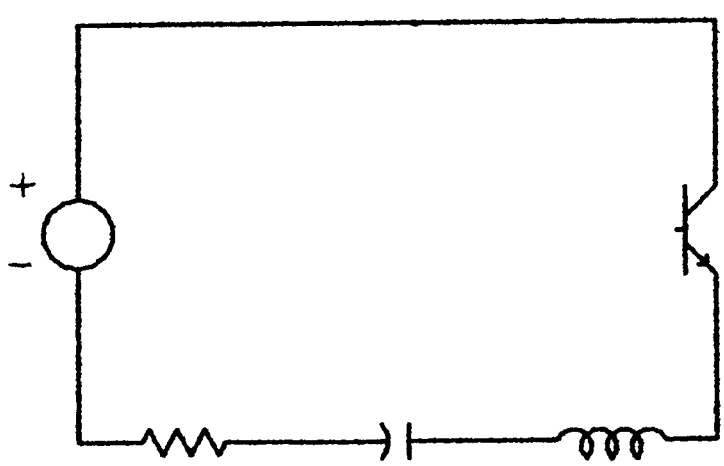

Fig. 3-19 Series resonant circuit

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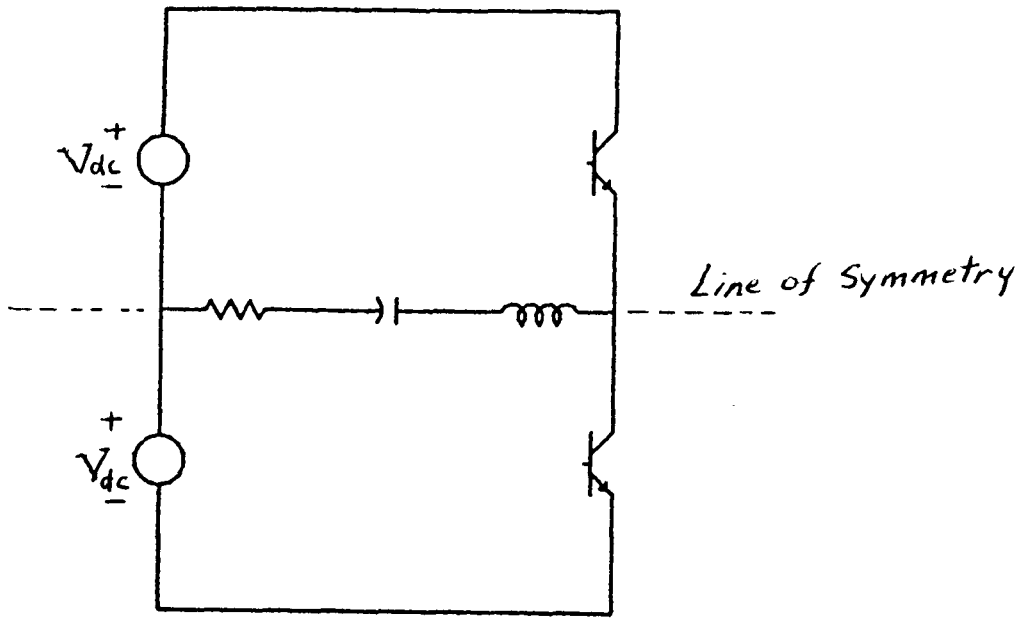
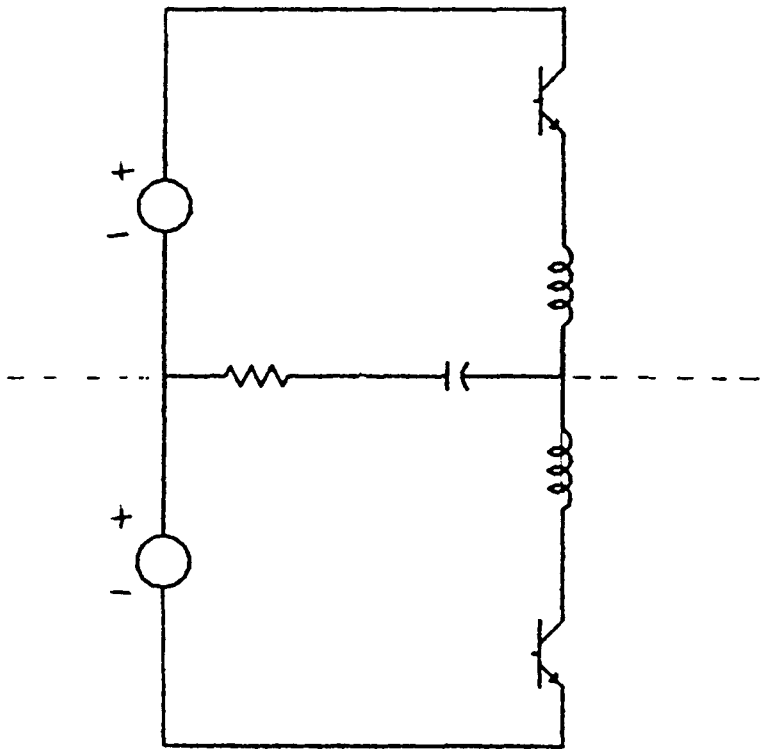
Exhibit 1014
Page 080



(a) Half-bridge topology



(b) Divided-inductor half bridge topology

Fig. 3-20 Voltage-fed series resonant topologies derived using symmetry

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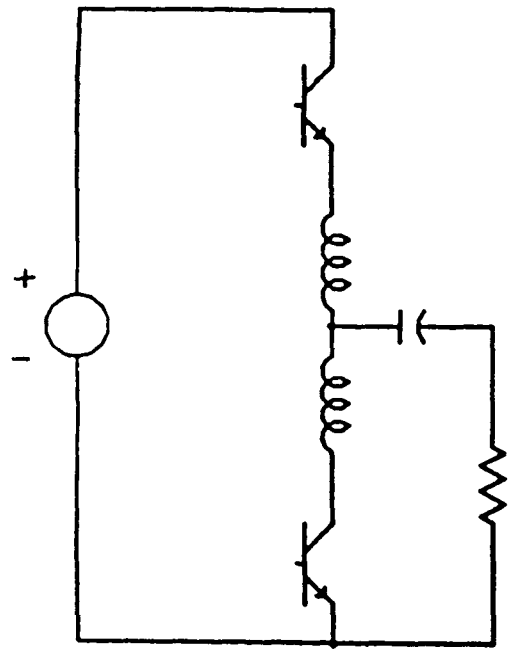
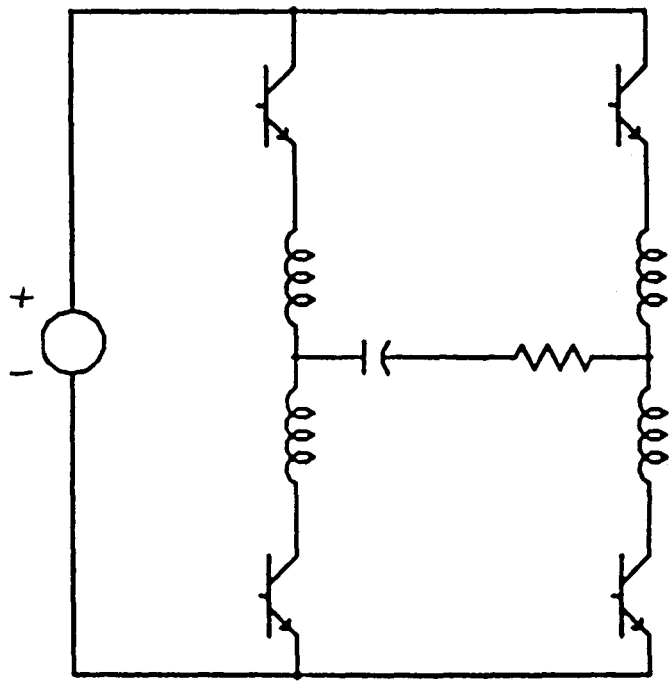
Exhibit 1014
Page 081



(a) Asymmetric topology



(b) Full bridge topology

Fig. 3-21 Divided-inductor asymmetric and full bridge topologies

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Exhibit 1014
Page 082

If the inductor and the resistor in Fig. 3-19 are placed in the common branch and symmetry is applied, the resulting topology is shown in Fig. 3-22. Such a topology cannot work as a resonant converter. This is because, the capacitor is in series with the voltage source and blocks any dc current, and hence no power is delivered from the dc source to the resonant circuit.

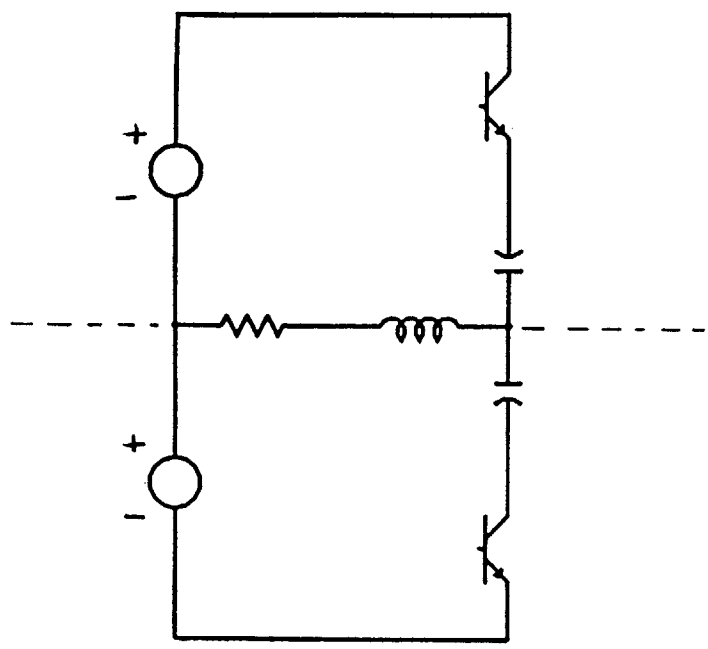

Fig. 3-22 Half bridge topology obtained by applying symmetry about an inductor and a resistor in a series load

The above topologies are derived from a series resonant circuit that results when the switch is turned on (closed). A series resonant circuit can also result when the switch is turned off (open). That is the case when the switch is placed in parallel with one of the resonant load elements. For example, if we place the switch in parallel with the capacitor and apply symmetry, we obtain the two topologies shown in Fig. 3-23. The constraint on this converter is that the switch should only be turned on when the capacitor voltage is zero.

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Exhibit 1014
Page 083

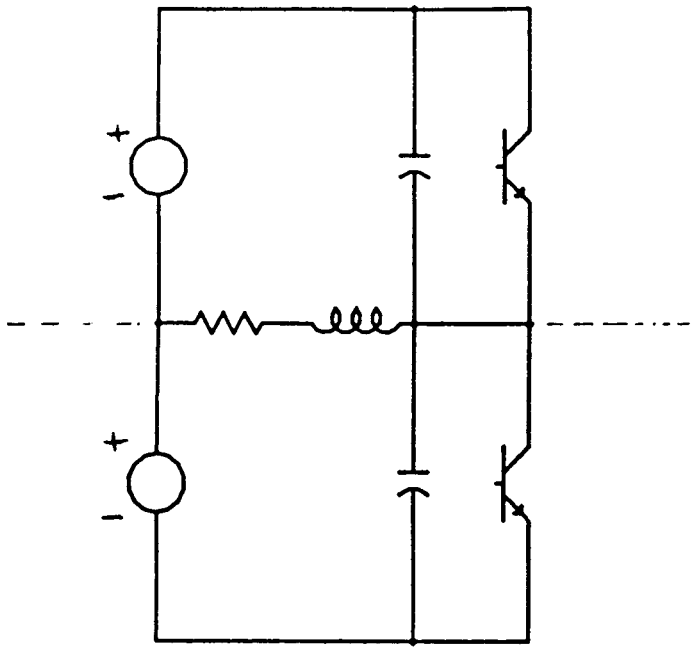

Fig. 3-23 Symmetry derived half bridge series topologies obtained when the switch is placed in parallel with the capacitor

Fig. 3-24 gives the resonant converter topology when both the capacitor and the inductor are split. when the inductor is split we shall call it, as before, the divided-inductor topology, and when the capacitor is split we shall call it the **divided capacitor topology**.

If the switch is placed in parallel with the inductor, the resulting topologies will have two inductors connected across a voltage source which will force the inductor current to build indefinitely. Therefore the resulting topology will not work as a resonant converter. This is analogous to the case when the switch is put in series with the capacitor. The two cases are duals, i.e the switch in series with a capacitor is the dual of a switch in parallel with an inductor.

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Exhibit 1014
Page 084

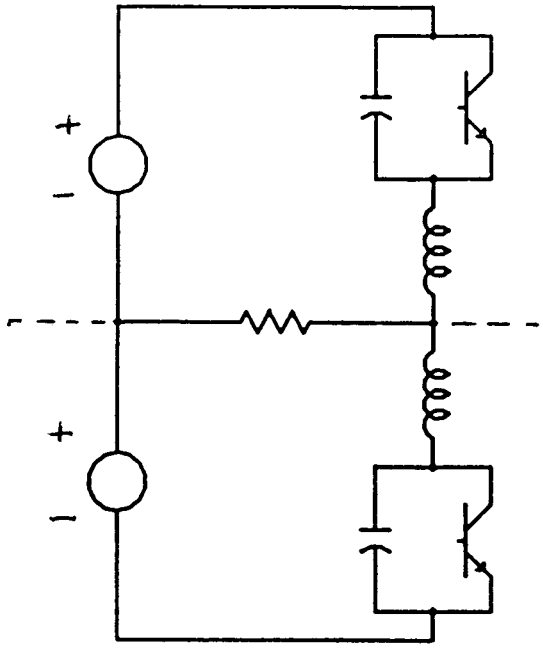

Fig. 3-24 Divided-inductor, divided-capacitor series topology

We can also use topological symmetry to derive parallel voltage-fed resonant converters in the same way we did for the series resonant converters. The three basic circuits to be used are shown in Fig. 3-25.

If the load in each circuit is put on the symmetry line, the resulting topologies are the half bridge configurations derived earlier, and shown in Fig. 3-26.

If the resistor is put on the symmetry line, the derived converters are shown in Fig. 3-27. Topology 2 cannot work as a resonant converter because the capacitors will block the dc current, and hence no dc power will be delivered. Topology 1 is a divided-inductor parallel resonant converter, and it can be extended by coupling [5], or uncoupling the inductors [17]. If the switch is placed across the capacitor, then the topology that results from applying symmetry is shown in Fig. 3-28.

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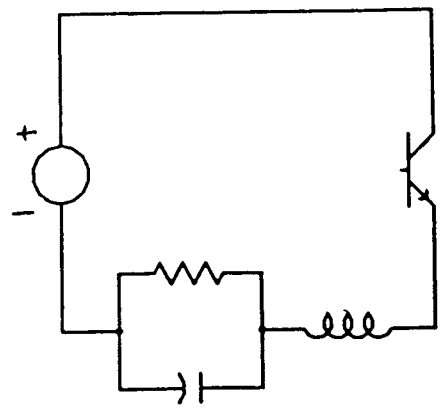
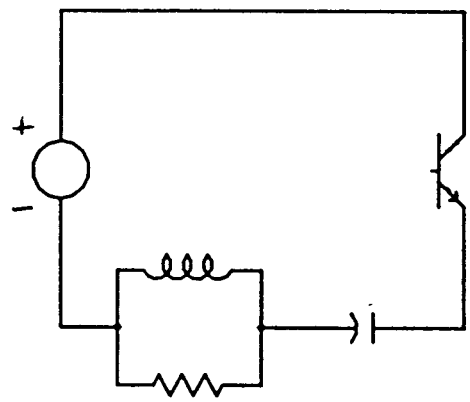
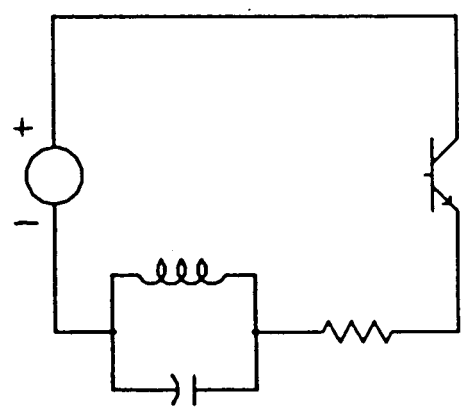
Exhibit 1014
Page 085



(a)



(b)



(c)

Fig. 3-25 Parallel resonant circuits used for deriving voltage-fed parallel topologies using symmetry

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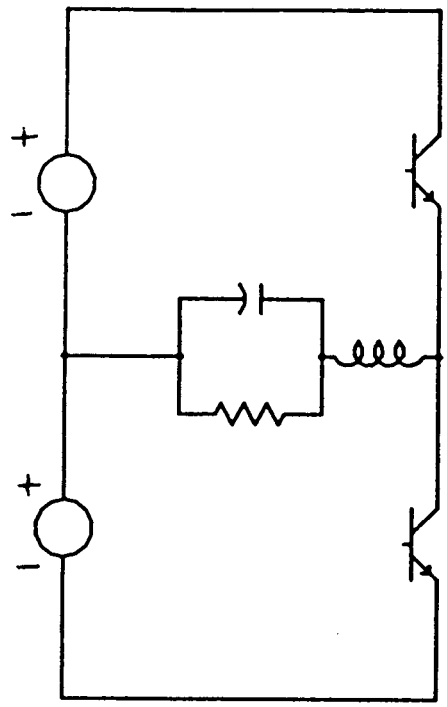
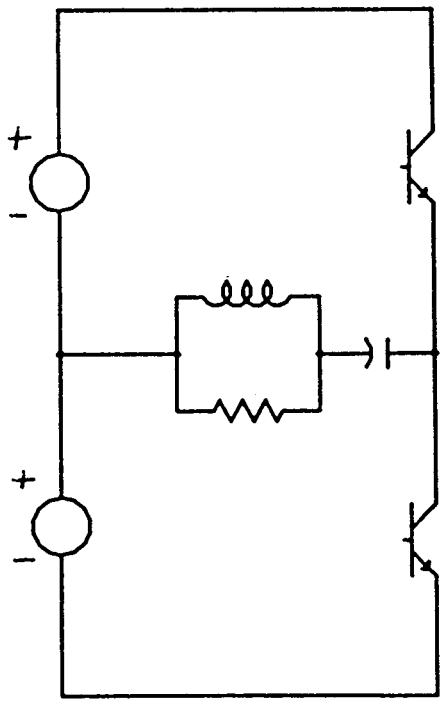
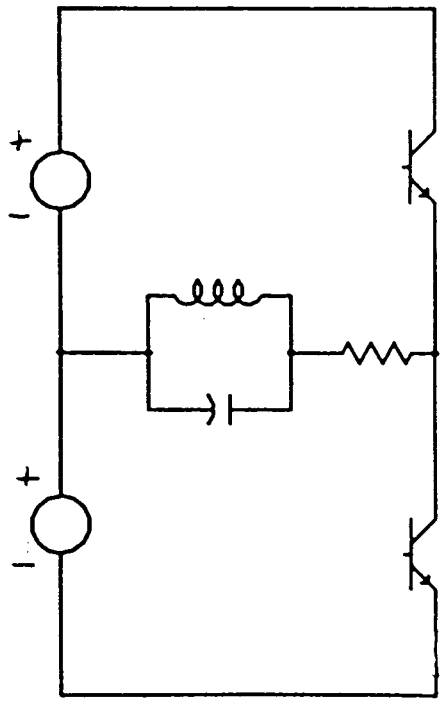
Exhibit 1014
Page 086



Topology 1



Topology 2



Topology 3

Fig. 3-26 Half bridge voltage-fed parallel topologies with bidirectional power flow

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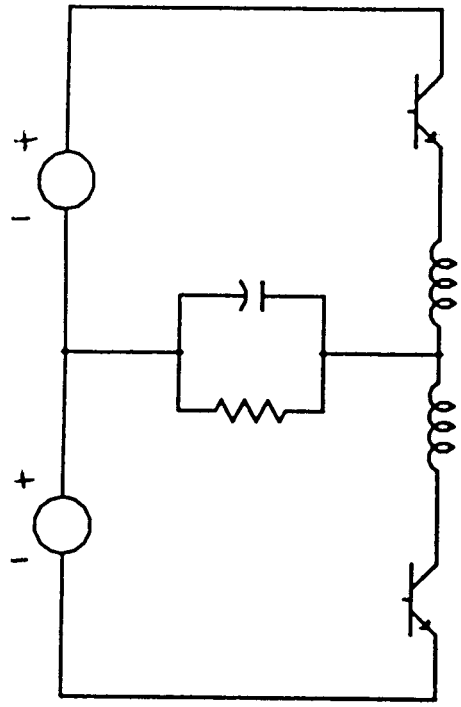
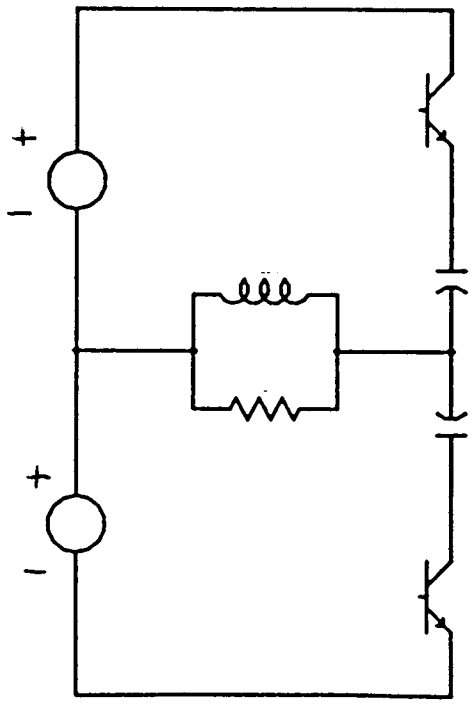
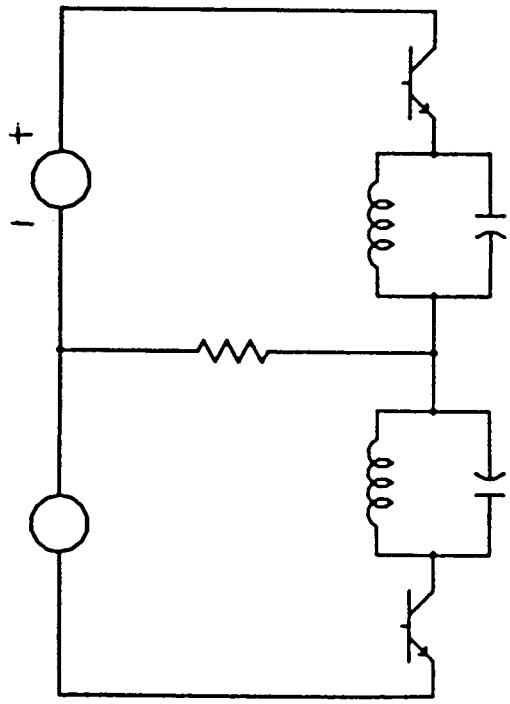
Exhibit 1014
Page 087



Topology 1





Topology 2

Topology 3

Fig. 3-27 Symmetry derived parallel topologies

InductEV, Inc.
Exhibit 1014
Page 088

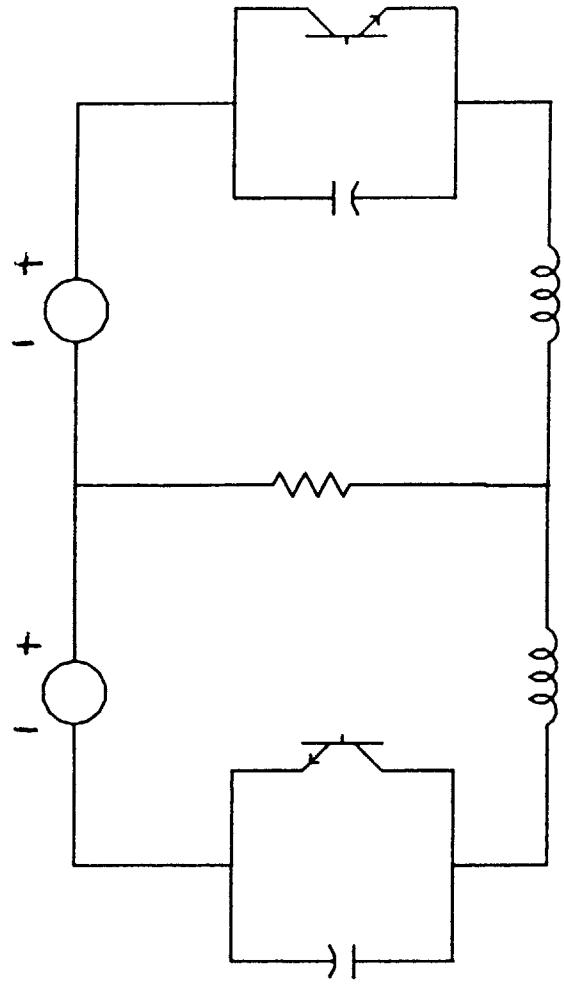


Fig. 3-28 Divided capacitor parallel voltage-fed topology

(5) Duality Considerations

Duality is a very useful link between power converters. It can yield new converter topologies as well as significantly improve understanding of the relationships between converters and their equivalent models [56]. Note that the type of switch and the modes of operation can differ between dual converters. It should also be noted that a converter that is dual to a given one may have some practical differences from the original [19].

InductEV, Inc.
Exhibit 1014
Page 089

In this section we shall give a brief review of dual networks. In the next section we shall use duality in combination with the set of voltage-fed topologies derived in the previous sections to generate current-fed resonant converter topologies. We shall also discuss some duality considerations governing dual resonant converters.

Principles of duality have also been discussed in [74] and [56]. Table 3-2 gives a summary of the duality relationships among electrical components and connections.

Element or connection	Dual elements or connection
Voltage Source	Current Source
Inductor	Capacitor
Resistance	Conductance
Impedance	Admittance
Open Switch	Closed Switch
Series	Parallel
Tree	Cotree
Node	Mesh
Loop	Cutset
ON	OFF
Short circuit	Open circuit

Table 3-2 Circuit elements, connections and their duals

Let us give an example of how to generate the dual of a network and discuss the operation of dual networks. Consider the bidirectional half bridge voltage-fed series resonant topology shown in Fig. 3-29. To obtain the dual of this topology we put a node inside each mesh and a

InductEV, Inc.
Exhibit 1014
Page 090

node outside the circuit. Now draw arcs between these nodes, one arc through each element of the original circuit. The elements on these arcs are the duals of the ones they cut. These connections are shown in Fig. 3-30a and the resulting dual topology is shown in Fig. 3-30b. The dual topology is a bidirectional half bridge current-fed parallel topology. The bidirectional current switch transforms into a bidirectional voltage switch. The implementation of a bidirectional voltage switch comprises a controlled switch (a power transistor) with a series diode connected to support the negative voltage. The switch implementation in dual networks is an important issue and we will consider it further in the next section. The switching configuration obtained by closing a switch in a converter corresponds to the switching configuration obtained when the switch is open in the dual converter.

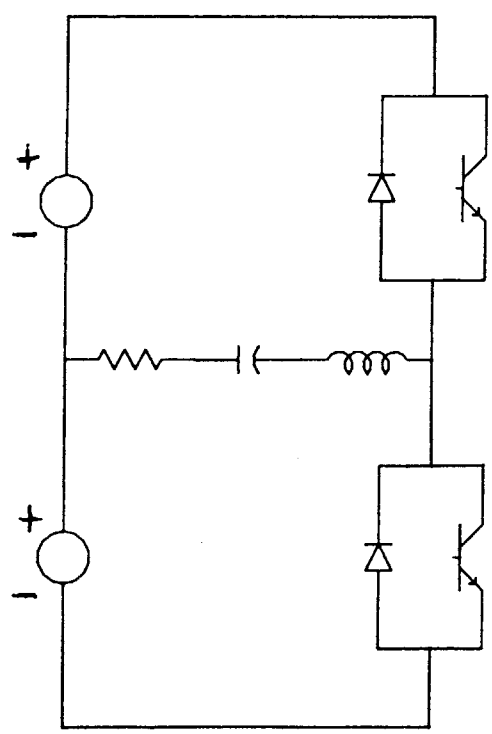
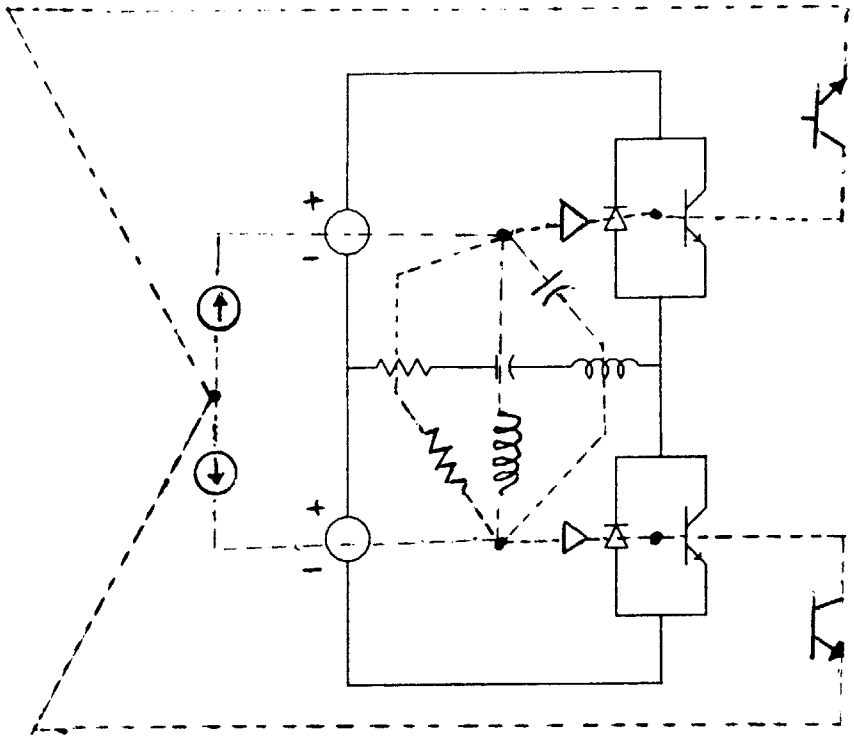
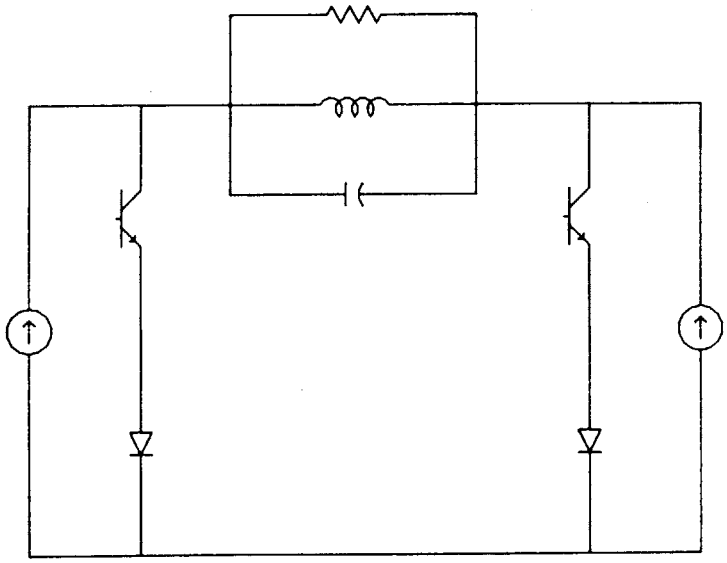


Fig. 3-29 Voltage-fed series topology with a bidirectional current switch

InductEV, Inc.
Exhibit 1014
Page 091



(a) Use of duality in Fig. 3-29



(b) Dual topology of Fig. 3-29

Fig. 3-30 Current-fed parallel resonant topology with bidirectional voltage switch

InductEV, Inc.
Exhibit 1014
Page 092

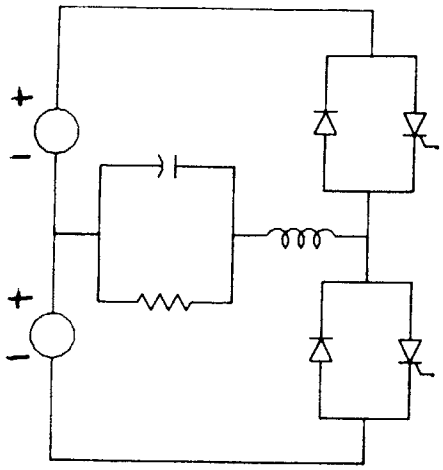
(6) Current-fed Resonant Converters

In the literature on resonant converters, a few current-fed topologies and their corresponding dual voltage-fed topologies have been presented. Examples of these converters are [5] and [8], [18] and [6], [16] and [17]. Except for [16], [17], the duality link has not been used. For example, in [18] two topologies that are duals of each other are analyzed separately for comparing the capacitor voltage. Instead, the comparison could have been obtained by analyzing one topology, and determining from its inductor current the capacitor voltage of the dual topology.

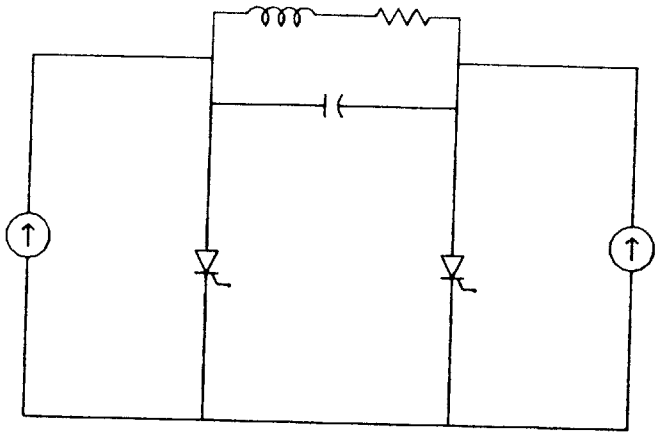
Having synthesized voltage-fed converters, one can by duality obtain the set of current-fed converters. For example, the derivation of parallel current-fed resonant converters will be the same as that of series voltage-fed converters, with all the terminology used in voltage-fed converters replaced by the dual terminology from Table 3-2. Similarly, the derivation of the series current-fed resonant topologies will be the same as that of the parallel voltage-fed resonant topologies. Rather than retracing the steps used in the derivation of the voltage-fed converters, we shall give in this section a discussion of the duality relationships between current-fed and voltage-fed converters.

The switching cell for deriving current-fed topologies is the same as that used for deriving voltage-fed topologies, with the source being a current source and the switches being normally closed rather than open. There loads for the current-fed topologies, are shown earlier in Fig. 3-11 . The switch implementation and the modes of operation can best be illustrated by the four converters shown in Fig. 3-31.

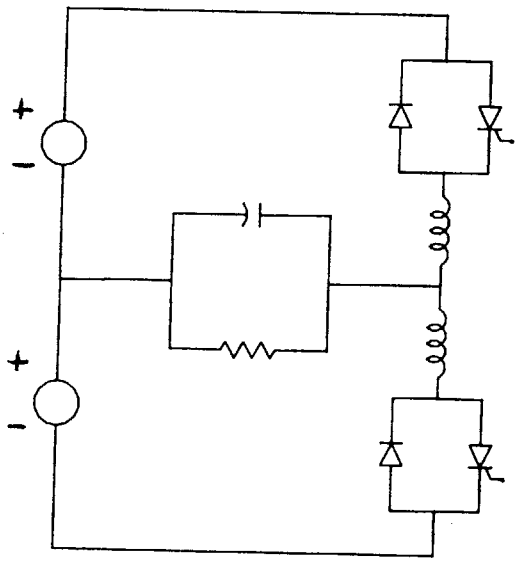
InductEV, Inc.
Exhibit 1014
Page 093



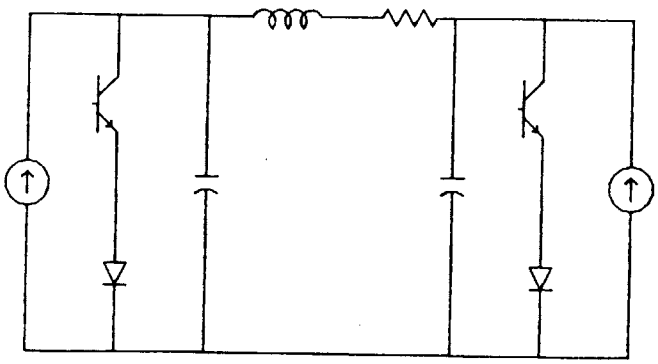
Topology A



Topology B



Topology C



Topology D

Fig. 3-31 Two voltage-fed parallel topologies and their duals

InductEV, Inc.
Exhibit 1014
Page 094

Topologies A and C are half bridge voltage-fed parallel converters with bidirectional current switches. Topologies B and D are their respective dual current-fed series converters. Topology A has been analyzed by Kasturi [18]. Topology C has been analyzed by Mapham [17], and Topology B has been analyzed by Kassakian [16] and [19]. Topology D is obtained by applying duality to Topology C, and its corresponding full bridge topology has been analyzed by Revankar and Gadag [7]. The following comparison gives insight into the similarities and differences that dual topologies can exhibit.

(i) The switches in Topologies A and C have to carry bidirectional currents, while the switches in B and D have to support bidirectional voltages.

(ii) Thyristors can be used in Topologies A and C with no additional commutation circuit needed. Commutation of the thyristors can either be natural or forced, depending on whether the switching frequency is below or above the resonant frequency. In Topology B, thyristors can be used, but they can only be turned off by forced commutation for a certain range of the switching frequency. Also, since the thyristor is a bidirectional voltage switch, only two switches are needed in Topology B, as compared to four switches in Topology A.

(iii) Topology C, which is a divided-inductor version of Topology A, can only operate at switching frequencies less than the resonant frequency, but it has better switch stresses (di/dt, dv/dt) than Topology A. Thyristors can be used in Topology C, and they are commutated naturally. In the dual current-fed Topology D, the switch is changed from a thyristor to a

InductEV, Inc.
Exhibit 1014
Page 095

transistor, and the operating switching frequency is higher than the resonant frequency. If thyristors are to be used, then an additional commutation circuit will be needed. Since a thyristor usually can handle a larger amount of power, then power handling capability of Topology B is larger than that of Topology D.

(iv) Topology C uses two inductors and one capacitor, while Topology D has two capacitors and one inductor. Capacitors can in general be lighter and closer to ideal than inductors, so one might argue that Topology D is better in this respect.

(v) If a transformer is used to isolate the load, then in Topologies A and C a transformer with large magnetizing inductance and a small leakage is needed. On the other hand, a transformer with high leakage inductance is needed to isolate the load in Topologies B and D.

Depending on the load and input characteristics, one has a choice between four converters that are topologically the same but different in characteristics.

(7) Summary and Conclusions

In this chapter we have explored three methodologies that may be used to synthesize resonant converter topologies. In the first method a switching cell is developed and the basic resonant converter topologies are derived from it. These are the asymmetric, the symmetric full bridge and the symmetric half bridge topologies. The different switch implementations and types of load (series, parallel and combination of these) are discussed. This a gives clearer picture of

InductEV, Inc.
Exhibit 1014
Page 096

inter-relationships among the resonant converter topologies presented in Chapter II.

The second method uses the symmetrical structure of resonant converters to derive other topologies. The symmetry derived topologies are: the divided-inductor topology, obtained by splitting the resonant load inductor; the divided-capacitor topology, obtained by splitting the resonant load capacitor; and topologies obtained by combinations of the preceding two.

The third method uses duality, which completes the set of resonant converter topologies by deriving the dual topologies of those derived by the first two methods. Also, it is shown that the comparison of dual converters can be of great help in choosing a converter that suits the load and input source characteristics.

InductEV, Inc.
Exhibit 1014
Page 097

APPENDIX 3A

SYNTHESIS OF RESONANT CONVERTERS USING LINEAR NETWORK THEORY

(1) Introduction

In power electronics, two methods have been used to synthesize power converter topologies. One method employs linear network theory to generate the set of switching dc-dc converter topologies [55], and the other uses duality to define the relationships among dc-dc converters [56]. In this appendix we shall explore the use of the first method.

Section 2 gives a review of the use of linear network theory for deriving the state equations for LTI systems. In Section 3 we shall discuss the use of the material of Section 2 in the synthesis of power converters. In particular we shall go over some of the work of Erickson [55] which uses linear network theory to synthesize switching dc-dc converters. In Section 4 we shall show how the Erickson approach can be used to synthesize resonant converters.

(2) State Equations Formulation of Linear Networks

The generality of the state variable method of system representation makes it applicable to a wide class of power converters. An additional advantage of the approach is that it is systematic and easy to adopt for computer simulation. The state representation of a system can be expressed in vector form as n first order differential equations as follows :

$$\frac{d\,\mathbf{x}}{d\,t} = \mathbf{x}^{\bullet} = \mathbf{A}\,\mathbf{x} + \mathbf{B}\,\mathbf{u} \qquad (3A.1)$$

where $\mathbf{x}$ is a vector of n state variables, $\mathbf{u}$ is a vector of m inputs and $\mathbf{A}$ and $\mathbf{B}$ are coefficient matrices of suitable dimensions. Although the

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Exhibit 1014
Page 098

choice of the state variables is not unique, it is common in linear network theory to choose inductor currents and capacitor voltages.

Methods for state equations formulation of linear network models exist and are well explained in many text books [52]-[56]. The method that we shall use to derive resonant converter topologies is explained in [52], and we shall briefly discuss it in this section. The method is developed for a certain class of linear networks known as 'proper networks' (networks that are composed of only lumped two-terminal elements and contain no capacitor-only loops or inductor-only cutsets). The network should contain only simple branches, i.e, branches containing only one element. The network can be divided into two parts: a proper tree (a subgraph that contains all the voltage sources, all the capacitors and possibly some resistors, but no inductors and no current sources), and a cotree which contains all the independent current sources, all inductors and possibly some resistors. The linearly independent Kirchoff's laws for the voltages and currents in the network can be written as:

$$i_v + F_{vr}\, i_r + F_{vl}\, i_l + F_{vi}\, i_i = 0 \qquad (3A.2a)$$

$$i_c + F_{cr}\, i_r + F_{cl}\, i_l + F_{ci}\, i_i = 0 \qquad (3A.2b)$$

$$i_g + F_{gr}\, i_r + F_{gl}\, i_l + F_{gi}\, i_i = 0 \qquad (3A.2c)$$

$$v_r - F_{vr}^T\, v_v - F_{cr}^T\, v_c - F_{gr}^T\, v_g = 0 \qquad (3A.2d)$$

$$v_l - F_{vl}^T\, v_v - F_{cl}^T\, v_c - F_{gl}^T\, v_g = 0 \qquad (3A.2e)$$

$$v_i - F_{vi}^T\, v_v - F_{ci}^T\, v_c - F_{gi}^T\, v_g = 0 \qquad (3A.2f)$$

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Exhibit 1014
Page 099

where:

v_v, i_v = voltage and current vectors of independent voltage sources

v_c, i_c = voltage and current vectors of network capacitors

v_g, i_g = voltage and current vectors of tree branch resistors

v_r, i_r = voltage and current vectors of cotree chord resistors

v_l, i_l = voltage and current vectors of network inductors

v_i, i_i = voltage and current vectors of independent current sources

F_{vr}, F_{vl}, F_{vi}, F_{cr}, F_{cl}, F_{ci}, F_{gr}, F_{gl} and F_{gi} are matrices which describe the connection between the network components. The superscript T denotes the transpose of a vector or a matrix. The entries of each F matrix can be either +1, 0 or -1 depending on the interconnections of the elements of the network.

The branch voltage current relationships (VCR) are given by:

$$v_r = R_r i_r \tag{3A.3a}$$

$$v_l = L\,(di_l/dt) \tag{3A.3b}$$

$$i_c = C\,(dv_c/dt) \tag{3A.3c}$$

$$i_g = G_g v_g \tag{3A.3d}$$

where

R_r and G_g are diagonal positive definite matrices containing cotree chord resistances and tree branch conductances respectively.

L is a symmetrical positive definite matrix whose diagonal elements are the self inductances and the off-diagonal elements are the mutual inductances of the network.

C is a diagonal positive definite matrix containing the network capacitances.

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Exhibit 1014
Page 100

Combining equations (3A.2) and (3A.3) gives the state equations of the network

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \begin{bmatrix} i_1 \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} H_{11} & H_{1c} \\ H_{c1} & H_{cc} \end{bmatrix} \begin{bmatrix} i_1 \\ v_c \end{bmatrix}$$

$$+ \begin{bmatrix} H_{1v} & H_{1i} \\ H_{cv} & H_{ci} \end{bmatrix} \begin{bmatrix} v_v \\ i_i \end{bmatrix} \qquad (3A.4a)$$

where

$$H_{11} = -F_{g1}^T G^{-1} F_{g1} \qquad (3A.4b)$$

$$G = G_g + F_{gr} R_r^{-1} F_{gr}^T \qquad (3A.4c)$$

$$H_{cc} = -F_{cr} R^{-1} F_{cr}^T \qquad (3A.4d)$$

$$R = R_r + F_{gr}^T G_g^{-1} F_{gr} \qquad (3A.4e)$$

$$H_{1c} = F_{c1}^T - F_{g1}^T G^{-1} F_{gr} R_r^{-1} F_{cr}^T \qquad (3A.4f)$$

$$H_{c1} = -F_{c1} + F_{cr} R^{-1} F_{gr}^T G_g^{-1} F_{g1} \qquad (3A.4g)$$

$$H_{1v} = F_{v1}^T - F_{g1}^T G^{-1} F_{gr} R_r^{-1} F_{vr}^T \qquad (3A.4h)$$

$$H_{cv} = -F_{cr} R^{-1} F_{vr}^T \qquad (3A.4i)$$

$$H_{1i} = -F_{g1}^T G^{-1} F_{gi} \qquad (3A.4j)$$

$$H_{ci} = -F_{ci} + F_{cr} R^{-1} F_{gr}^T G_g^{-1} F_{gi} \qquad (3A.4k)$$

(3) Synthesis of Power Converters using Linear Network Theory

Power converters are switched linear networks, where each switching configuration is an LTI system represented by equation (3.3). Given that the entries of each F matrix of a proper network can be either +1,

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Exhibit 1014
Page 101

0 or -1, and there are i elements in a tree and j elements in a cotree (i,j = 1, 2, 3, ...), then there are 3*i*j number of possible F_{ij}'s and 3^{ij} number of proper networks that can be constructed using different combinations of F_{ij}. For example if a tree of a proper network has 3 elements (say a capacitor, a resistor and a voltage source), and its cotree has 2 elements (say an inductor and a current source) then there are 18 possible different F entries, and 243 possible proper networks. The number of proper networks becomes large as the number of elements in a proper network increases.

To use these proper networks for realizing a certain power converter (e.g dc-dc, rectifiers,resonant converters,...etc) we need to develop a systematic reduction procedure by which we can extract, from all the existing proper networks, those that can characterize the converter. First we eliminate redundant networks (networks that are topologicaly the same) and non-realizable networks (networks that cannot be constructed because they violate certain electrical laws such as KVL and KCL). Second, the features of the power converter are used to further reduce these networks. For example, in dc-dc converters the load resistance is always bypassed by a filter capacitance, which makes F_{vr} equal to zero. This is because the load is not directly connected to an independent voltage source. Having determined all the possible switching configurations of a converter, switches are then introduced, depending on the number of switching configurations of the converter, to combine different networks to obtain the possible set of converter topologies.

InductEV, Inc.
Exhibit 1014
Page 102

Erickson [55] has used the above method to generate the possible set of dc-dc converter topologies. Although his application is for dc-dc converters, the procedure can also be applied in the synthesis of other types of power converters. The complexity of the synthesis procedure depends on the number of reactive elements and the number of switching configurations that the converter has during a switching cycle.

(4) Synthesis of Resonant Converters

Resonant converter topologies can be synthesized using the above approach. The possible parameters that can be used when synthesizing resonant converters are:

(i) The resonant frequency (f_r) which is important, when related to the switch drive frequency, in determining the input-to-output conversion ratio and the number of switching configurations during a cycle.

(ii) The Q-factor of a resonant converter which is an important parameter in designing the converter and in determining the conversion ratio.

(iii) The characteristic impedance of the resonant circuit.

In this section we shall synthesize resonant converters that have only one source, one capacitor, one inductor and one resistor. For a proper network, the resistor can be either in the tree or in the cotree. When we use a voltage source, if the resistor is part of the tree, the resulting network, as we shall see, is a series resonant circuit, and hence resonant converters obtained from combining configurations of this proper network will be referred to as the **series resonant converters.**

InductEV, Inc.
Exhibit 1014
Page 103

When the resistor is taken as part of the cotree, the resulting proper network is a parallel resonant circuit, and hence resonant converters obtained by combining the configurations of this proper network will be referred to as **parallel resonant converters**. The dual is true when a current source is used.

(A) Series resonant converters

In this section we shall treat the resistor as a part of the tree. Since we are considering only voltage sources, then all the F matrix entries that are related to a current source (e.g F_{ci}, F_{vi}, F_{gi}) are equal to zero. Similarly, R being a tree resistor will make the following simplifications

$$F_{cr} = F_{vr} = F_{gr} = 0 \tag{3A.5a}$$

$$H_{cc} = H_{cv} = 0 \tag{3A.5b}$$

$$H_{11} = -F_{g1}^{2} G_{g} \tag{3A.5c}$$

$$H_{1c} = F_{c1} \tag{3A.5d}$$

$$H_{c1} = -F_{c1} \tag{3A.5e}$$

$$H_{1v} = F_{v1} \tag{3A.5f}$$

Let us define $G_g^{-1} = R$ (R is the load resistance in a resonant converter) and $v_v = V$. Using these definitions and substituting (3A.5) in (3A.4) give

$$\begin{bmatrix} L\dfrac{di_1}{dt} \\ C\dfrac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -F_{g1}^{2} R & F_{c1} \\ -F_{c1} & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ v_c \end{bmatrix} + \begin{bmatrix} F_{v1} \\ 0 \end{bmatrix} V \tag{3A.6}$$

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Exhibit 1014
Page 104

Since we have 3 elements in the tree and one element in the cotree, then there are 27 possible proper networks that we can construct by interconnection of these elements. Our task now is to extract from these networks those that can be used in a series resonant converter. As we have defined in chapter II, a resonant converter converts dc power to ac sinusoidal power. Therefore one feature of the proper networks needed is that each of them to have sinusoidal voltages and currents. The differential equation in each of the state variables should be a second order of the form

$$\frac{d^2 x}{d t^2} + 2a \frac{d x}{d t} + w_r^2 x = K_x V \qquad (3A.7a)$$

Where

a = damping factor

w_r = resonant angular frequency = 2 f_r

K_x = A constant for the state variable x_i

The Q-factor of such a circuit is defined as:

$$Q = \frac{w_r}{2 a} \qquad (3A.7b)$$

The differential equation for the inductor current, obtained from (3A.6), is

$$\frac{d^2 i_1}{d t^2} + \frac{F_{g1}^2 R}{L} \frac{d i_1}{d t} + \frac{F_{c1}^2 i_1}{L C} = 0 \qquad (3A.8a)$$

and the differential equation for the capacitor voltage is

$$\frac{d^2 v_c}{d t^2} + \frac{F_{g1}^2 R}{L} \frac{d v_c}{d t} + \frac{F_{c1}^2 v_c}{L C} = \frac{-F_{c1} F_{v1}}{L C} \qquad (3A.8b)$$

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Exhibit 1014
Page 105

Comparing equations (3A.8) with equation (3A.7) we get

$$2a = \frac{F_{g1}^{2} R}{L} \tag{3A.9a}$$

$$w_r = \frac{F_{c1}}{\sqrt{L\ C}} \tag{3A.9b}$$

$$K_i = 0 \quad , \quad K_v = \frac{-F_{c1}\ F_{v1}}{L\ C} \tag{3A.9c}$$

and

$$Q = \frac{w_r}{2\ a} = \frac{F_{c1}}{F_{g1}^{2}} \frac{L}{R\ /LC} = \frac{Z_o\ F_{c1}}{R\ F_{g1}^{2}} \tag{3A.9d}$$

where $Z_o = \sqrt{L/C}$ = characteristic impedance of a resonant circuit

From these equations the possible values of the F matrix entries are

$$F_{c1}^{2} = 1 \longrightarrow F_{c1} = \pm 1 \tag{3A.10a}$$

$$F_{g1}^{2} = 1 \longrightarrow F_{g1} = \pm 1 \tag{3A.10b}$$

$$F_{v1} = 0,\ 1 \text{ or } -1 \tag{3A.10c}$$

For a positive Q we need F_{c1} to be positive, and for a finite Q we exclude F_{g1} from being zero. Also we will choose F_{g1} to be +1, since F_{g1} being -1 will give a redundant network. Finally it makes sense that F_{v1} to be 0, 1 or -1 because the resonant circuit can have either a positive voltage, a negative voltage or a zero voltage applied to it. The F entries that satisfy the conditions of a series resonant circuit are given in Fig. 3A-1, and the resultant proper networks are given in Fig. 3A-2. One can argue that the proper networks obtained by F_{v1} being +1 and -1 are redundant, but physically the two networks play different

InductEV, Inc.
Exhibit 1014
Page 106

roles in terms of energy or power flow. That is to say, if we assume a resonant converter with two configurations, a square wave voltage should be applied across the resonant circuit. If the voltage source in each of the three networks is set to zero, the elements are connected in series, hence the name series converter.

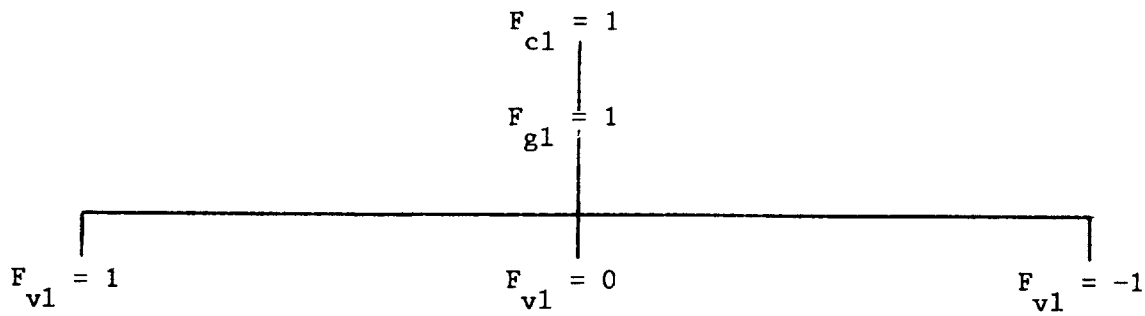

Fig. 3A-1 Entries of the F matrix for a series resonant circuit

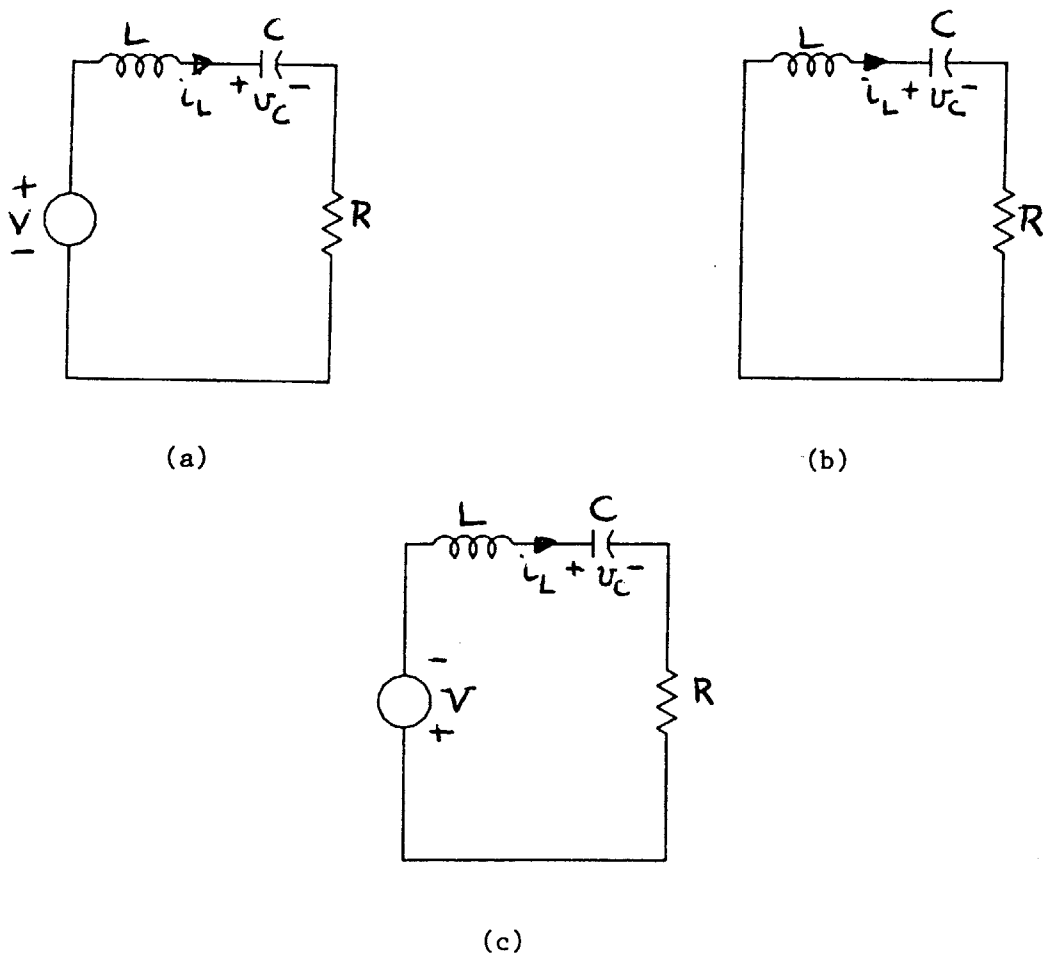

Fig. 3A-2 Possible proper networks for a series resonant converter

InductEV, Inc.
Exhibit 1014
Page 107

(i) Combining proper networks and switches

In this section we want to look at the possible ways of combining the proper networks that make series resonant circuits, as shown in Fig. 3A-2, with switches to generate the possible set of series voltage-fed resonant converters. We shall assume that the resonant converter that we want to synthesize has two modes, i.e there are two switching configurations during a cycle. Therefore we need to combine every two proper networks in Fig. 3A-2 with switches to form a resonant converter. Except for the load resistance, the elements of the combined networks can be chosen to be common to the two networks or separate. If we choose all the elements to be common, we obtain the resonant converter series topologies.

If the voltage sources are kept separate, then the resulting topology is obtained by combining networks (a) and (c) which is the series half bridge topology.

If the separate inductors are used, the resulting converters are the asymmetric and full bridge divided-inductor topologies, and if separate voltage sources and inductors are used, then the resulting topology is the half bridge divided-inductor topology.

With the switch placed in parallel with the capacitor, the possible topologies are the divided-capacitor topology with or without a divided-inductor.

(B) Parallel resonant converters

Parallel resonant converters are realized by networks combined of the same elements discussed in the previous section, except that the resistor will be part of the cotree rather than the tree of the proper network. In this case the F matrix entries associated with the tree

InductEV, Inc.
Exhibit 1014
Page 108

conductance are zero, and the entries of the H matrix in (3A.4) are:

$$H_{11} = 0 \tag{3A.11a}$$

$$H_{cc} = - F_{cr}^{2}/R \tag{3A.11b}$$

$$H_{c1} = - F_{c1} = - H_{1c} \tag{3A.11c}$$

$$H_{cv} = - F_{cr} F_{vr}/R \tag{3A.11d}$$

$$H_{1v} = F_{v1} \tag{3A.11e}$$

The differential equation in i_1 is

$$\frac{d^2 i_1}{d t^2} + \frac{F_{cr}^2}{C R} \frac{d i_1}{d t} + \frac{F_{c1}^2}{L C} i_L = \frac{F_{cr}^2 F_{v1} - F_{cr} F_{vr}}{L C} V \tag{3A.12a}$$

and the differential equation in v_c is

$$\frac{d^2 v_c}{d t^2} + \frac{F_{cr}^2}{C R} \frac{d v_c}{d t} + \frac{F_{c1}^2}{L C} v_c = \frac{- F_{vr}}{L C} V \tag{3A.12b}$$

Now comparing equations (3A.12) and (3A.7) we get

$$2a = \frac{F_{cr}^2}{R C} \tag{3A.13a}$$

$$w_r = \frac{F_{c1}}{\sqrt{L C}} \tag{3A.13b}$$

$$K_v = \frac{1}{L C} \tag{3A.13c}$$

and

$$Q = \frac{w_r}{2 a} = \frac{F_{c1}}{F_{cr}^2} \frac{R C}{\sqrt{LC}} = \frac{R F_{c1}}{Z_o F_{cr}^2} \tag{3A.13d}$$

InductEV, Inc.
Exhibit 1014
Page 109

In this case we have two tree elements and two cotree elements. Therefore there are 81 proper networks that we can construct. We want to find those networks that represent a resonant circuit. The features of a resonant circuit as seen from equation (3A.13) gives the following F entries

$$F_{cr}^{2} = 1 \longrightarrow F_{cr} = \pm 1 \qquad (3A.14a)$$

$$F_{cl}^{2} = 1 \longrightarrow F_{cl} = \pm 1 \qquad (3A.14b)$$

$$F_{vl} = 0,\ 1 \text{ or } -1 \qquad (3A.14c)$$

$$F_{vr} = 0,\ 1 \text{ or } -1 \qquad (3A.14d)$$

Choosing F_{cr} and F_{cl} to be 1 or -1 does not alter equation (3.12a). Therefore one choice gives a proper network that we can use, the other choice is redundant. For a positive Q we want F_{cl} to be 1, and for a finite Q we exclude F_{cr} from being zero. Also we can argue that F_{vl} and F_{vr} can be 1 and -1 for the same reasoning we gave in series resonant converters. Another way to look at it is that F_{vl} and F_{vr} are active entries, while F_{cl} and F_{cr} are passive entries. The final choice of F entries is given in Fig. 3A-3.

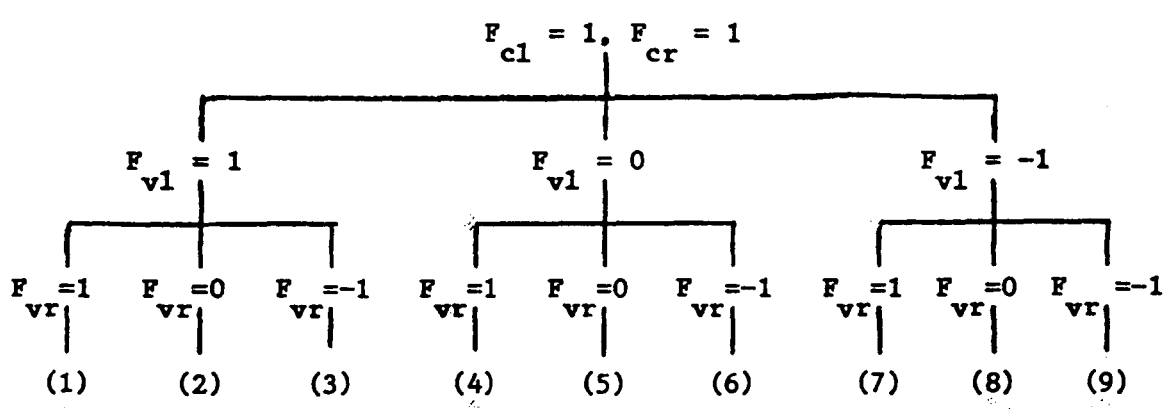

Fig. 3A-3 F entries that satisfy parallel resonant networks

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Exhibit 1014
Page 110

The state equations for the nine realizations of Fig. 3A-3 are given below:

(1)

$$L\frac{di}{dt} = v + V$$

$$C\frac{dv}{dt} = -i - \frac{v + V}{R}$$

(2)

$$L\frac{di}{dt} = v + V$$

$$C\frac{dv}{dt} = -i - \frac{v}{R}$$

(3)

$$L\frac{di}{dt} = v + V$$

$$C\frac{dv}{dt} = -i + \frac{V - v}{R}$$

(4)

$$L\frac{di}{dt} = v$$

$$C\frac{dv}{dt} = -i - \frac{v + V}{R}$$

(5)

$$L\frac{di}{dt} = v$$

$$C\frac{dv}{dt} = -i - \frac{v}{R}$$

(6)

$$L\frac{di}{dt} = v$$

$$C\frac{dv}{dt} = -i + \frac{V - v}{R}$$

(7)

$$L\frac{di}{dt} = v - V$$

$$C\frac{dv}{dt} = -i - \frac{v + V}{R}$$

(8)

$$L\frac{di}{dt} = v - V$$

$$C\frac{dv}{dt} = -i - \frac{v}{R}$$

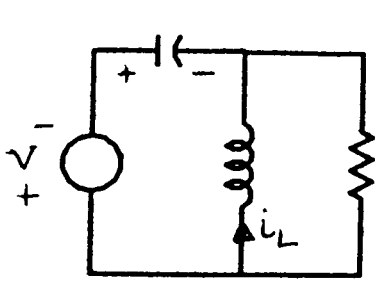
(9)

$$L\frac{di}{dt} = v - V$$

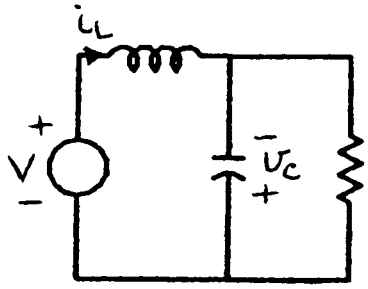
$$C\frac{dv}{dt} = -i + \frac{V - v}{R}$$

The nine networks that realize the above equations are given in Fig. 3A-4. Some of the networks are nonrealizable, because the KVL and KCL equations can not be satisfied simultaneously. In the absence of the voltage source all the elements are connected in parallel. This why we name resonant converters derived from the above 9 networks as parallel resonant converters.

InductEV, Inc.
Exhibit 1014
Page 111



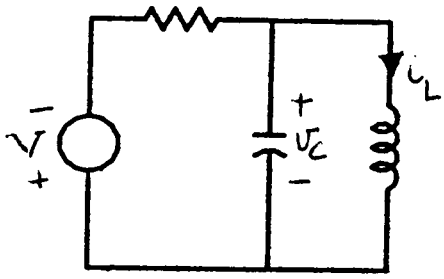
(1)



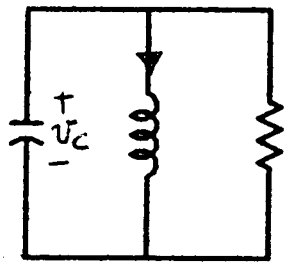
(2)

Non-realizable

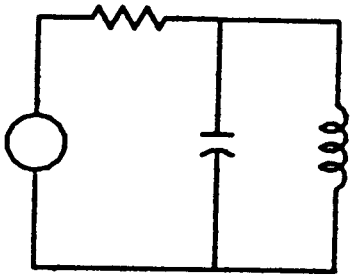
(3)



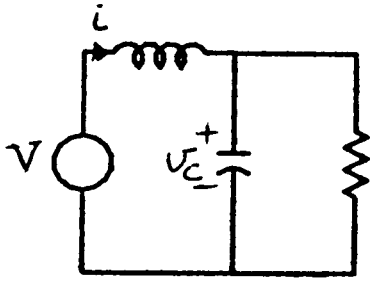
(4)



(5)



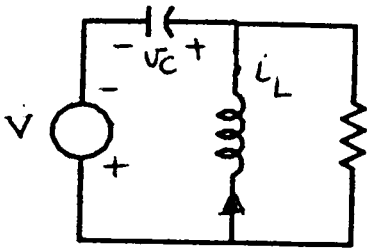
(6)



Nonrealizable

(7)

(8)



(9)

Fig. 3A-4 Circuit realizations of Fig. 3A-3

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Exhibit 1014
Page 112

(i) Combining networks and switches

Now we want to combine the networks of Fig. 3A-4 with switches to obtain parallel resonant converter topologies. We will follow the same procedure used for obtaining the series resonant converter topologies. We shall assume two configurations per switching cycle. If all the elements of the proper network are common to both configurations, we obtain the asymmetric and full bridge parallel topologies. If separate voltage sources are used the resulting topologies are the half bridge topologies. If we separate inductors are used, with one voltage source, one capacitor and one resistor the resulting topologies are the divided-inductor asymmetric and full bridge topologies. If separate inductors and voltage sources are used, the resulting topology is the divided-inductor half bridge topology.

All of the above topologies have been derived in chapter III. The switch implementation procedure is the same as we discussed before. For unidirectional power flow the switch is realized by controlled switch, and for bidirectional power flow the switch is realized by a control switch with anti-parallel diode. The topologies are obtained using a voltage source, but a current source could be used as well, by choosing a current source in equation (3A.4a). In this case the resonant converters obtained will be the duals of converters derived from the voltage source case.

InductEV, Inc.
Exhibit 1014
Page 113

CHAPTER IV

DYNAMIC MODELING OF RESONANT CONVERTERS

(1) Introduction

This chapter discusses the dynamic modeling of resonant converters. Section 2 gives a description of the modeling problem in power electronics and presents some of the modeling approaches available in the literature. Section 3 discusses the problem of dynamic modeling of resonant converters and describes some results that motivated us to model them. Section 4 presents a small-signal sampled-data model that we have developed for resonant converters. The model is illustrated using a voltage-fed series resonant converter. In Section 5 we shall discuss the results obtained from the dynamic model of the series resonant converter and compare them with the results obtained from the Parity Simulator [69].

(2) Overview of Modeling in Power Electronics

This section addresses the problem of modeling power electronic circuits, and gives a brief review of the different modeling approaches that have been developed in the literature.

Due to the nonlinear switching behavior of power converters, it is difficult to determine the characteristics and assess the stability of systems that use such converters. A model would help in the design and control of these converters. Two kinds of models are used: static and dynamic. A static model gives the analysis of the steady state, and helps designers develop equations for the converter's operating characteristics and component ratings. A dynamic model (at least a small-signal) is essential in determining the stability of a converter, and in designing feedback compensators. This chapter investigates the

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Exhibit 1014
Page 114

problem of dynamic modeling of power converters.

Methods of developing dynamic models for power converters range from discrete z-domain or continuous s-domain descriptions in terms of classical control block diagrams, to electrical equivalent circuit descriptions of linearized converter models (see [57] and references therein). The following sections outline some previous work on both continuous-time and discrete-time modeling of power electronic circuits.

Modeling of power converters in the literature has largely being devoted to certain categories of circuits: switched dc-dc converters and controlled-rectifiers. Special emphasis has been given to switched dc-dc converters. This is because there are some natural approximations of switched dc-dc converters that make them easy to model. One key approximation is the replacement of instantaneous signals by their averaged values.

In the area of dc-dc converters, approximate continuous-time dynamic models are developed using averaging techniques. The most famous of these techniques is the state space averaging approach developed by Middlebrook and C'uk [58], and Brocket and Wood [76]. It is a straightforward, general automatable technique [63]. Other models of dc-dc converters have been less general or less easy to obtain.

In the area of controlled rectifiers, a continuous-time model has been developed using Laplace transforms [57]. Although the model is exact in determining the dynamics of controlled-rectifiers, the algebra used to develop it is quite involved [75].

InductEV, Inc.
Exhibit 1014
Page 115

Many authors have also developed linearized discrete-time models for dc-dc converters (see [59] and references therein). Discrete-time models for controlled-rectifiers have been developed in [60].

(3) The Motivation to Model Resonant Converters

Our interest in dynamic modeling of resonant converters was partially sparked by [33], which deals with the static characteristics of a voltage-fed series resonant converter. Further motivation was provided by some initial work that we did to study the dynamics of resonant converters, using the MIT's Parity Simulator [69]. In this section, we shall only describe these results, and in a later section we shall analyze them. We looked at the dynamics of the series resonant converter shown in Fig. 4-1.

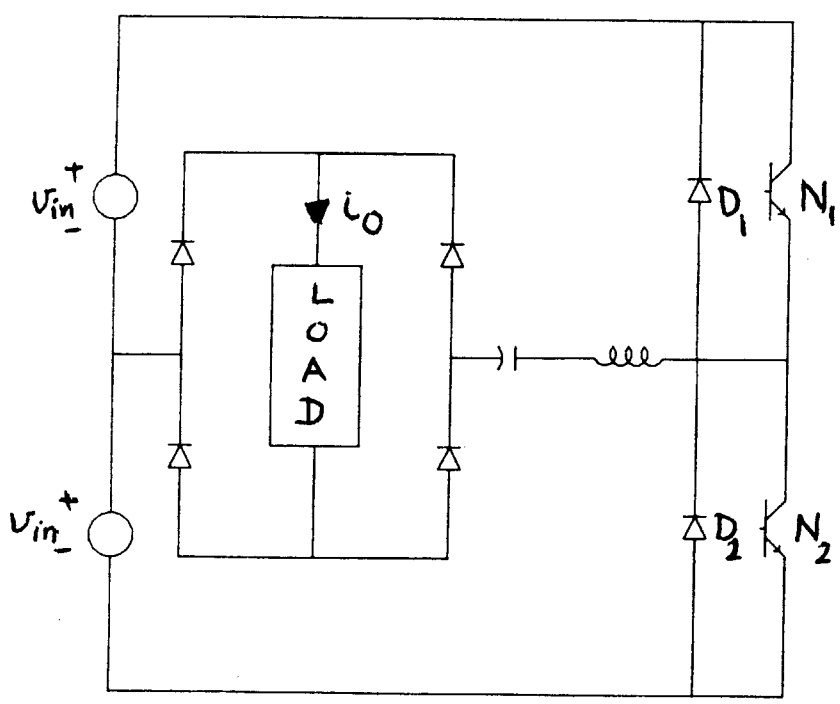

Fig. 4-1 A voltage-fed series resonant converter

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Exhibit 1014
Page 116

The actual converter circuit parameters are:

$L = 197$ uH $\qquad C = 100$ nF

$V_{in} = 14$ V $\qquad f_s = 40$ kHz

The elements in the Parity Simulator are designed using electronic analog and digital components such as operational amplifiers, comparators, .. etc. The voltage and current handling capabilities of these components are ± 10 V and ± 10 mA respectively. Also, the Simulator operating frequency range is 0.01 - 100 Hz. Therefore the voltage, current and frequency of the actual circuit should be scaled down to be within the limits of the Simulator. The scale factors we have chosen are:

Voltage scale factor = VSC = 0.1

Current Scale factor = ISC = 0.001

Frequency Scale factor = FSC = 2.5×10^{-4}

Fig. 4-2 shows the response of the load current, i_o, to a step change of 20% in the switch drive frequency f_s, when the load on the rectifier side is a 10 ohm resistor. Because of the damping by the load resistance, the response is well behaved.

When the resistance is replaced by a voltage source, the response has a second order appearance, as Fig. 4-3 shows. One interesting result observed from the response is that the frequency of ringing of the envelope is much lower than the switching frequency. Another observation to notice from Fig. 4-3b is the kick in the opposite direction to the steady state, which raises the question of the existence of a right half plane zero in the continuous-time small-signal transfer function.

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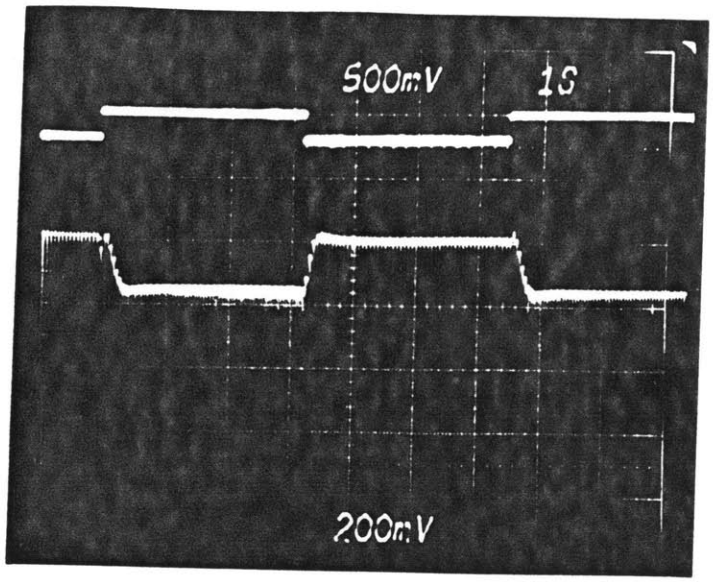
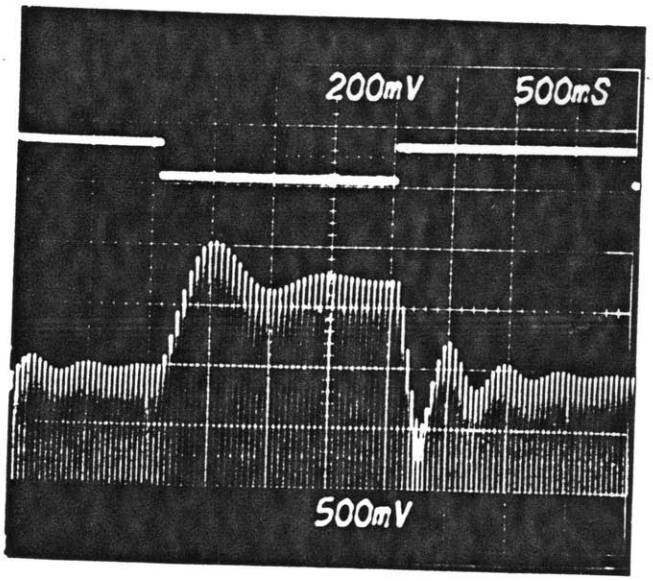
Exhibit 1014
Page 117



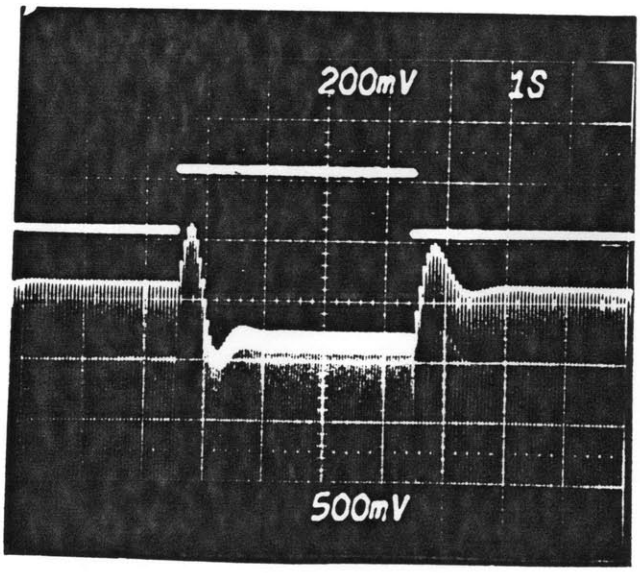
Load resistance = 10 ohm

Fig. 4-2 Response of the rectified inductor current (i_o) to a step change in the switching frequency for a resistive load



5% step in f_s

(a) V_o = 0.2V



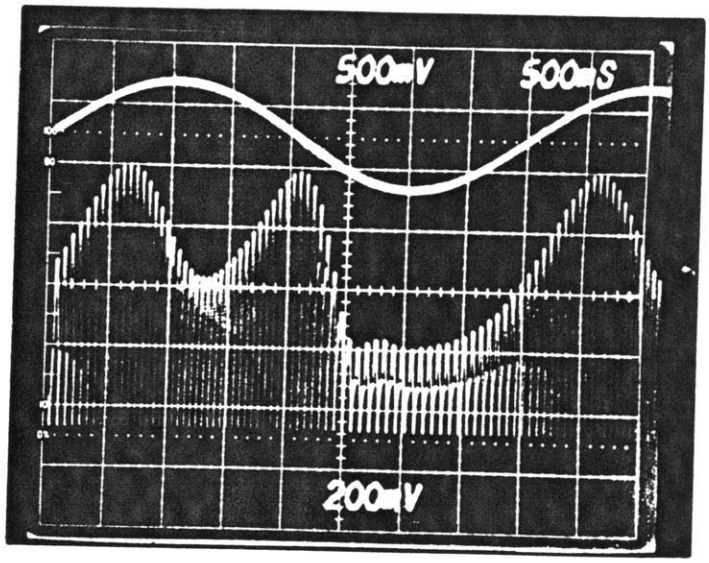
20% step in f_s

(b) V_o = 5.0 V

Fig. 4-3 Response of i_o to a step change in the switching frequency for a voltage source load

InductEV, Inc.
Exhibit 1014
Page 118

Fig. 4-4 shows the behavior of the rectified inductor current i_o when the load is a voltage source, and the frequency undergoes large sinusoidal variations (as opposed to the smaller step changes of Figs. 4-2 and 4-3). Note the highly nonlinear response.



Upper trace: switching frequency
Lower trace: rectified inductor current, i_o

Fig. 4-4 Large-signal response of the series resonant converter (voltage source load)

(4) Contributions of This Chapter

The above results draw attention to the necessity of modeling the dynamics of resonant converters. Prior work in resonant converters gives little guidance to describe the above dynamics. In this thesis, a contribution is made towards understanding the dynamics of resonant converters. Sampled-data models to describe the dynamics of both large-signal and small perturbations away from a cyclic steady state, due to a change in either the supply input (voltage or current) or the switching

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Exhibit 1014
Page 119

frequency, are developed. The models also allow the direct calculation of the sensitivity of the steady state of a converter to circuit parameter variations. The modeling approach is illustrated using the above series resonant converter, but the procedure can be used to model other types of resonant converters as well. Although the steps we follow in developing the dynamic model have been used in the literature for modeling other specific circuits, they are developed here in a systematic way that generalizes to include other power electronic circuits, such as resonant converters, where the sampling instant is the primary control [61]

Dynamic modeling of resonant converters, and the results obtained for a series resonant converter, constitute the rest of this chapter. In Section 5 we shall give a description of the steady state operation of the series resonant converter, and develop the small-signal sampled-data model for it. In Section 6 we present the results obtained from the small-signal model and compare them with the results obtained from the Parity Simulator. Section 7 discusses the sensitivity calculations and automatability of the converter analysis.

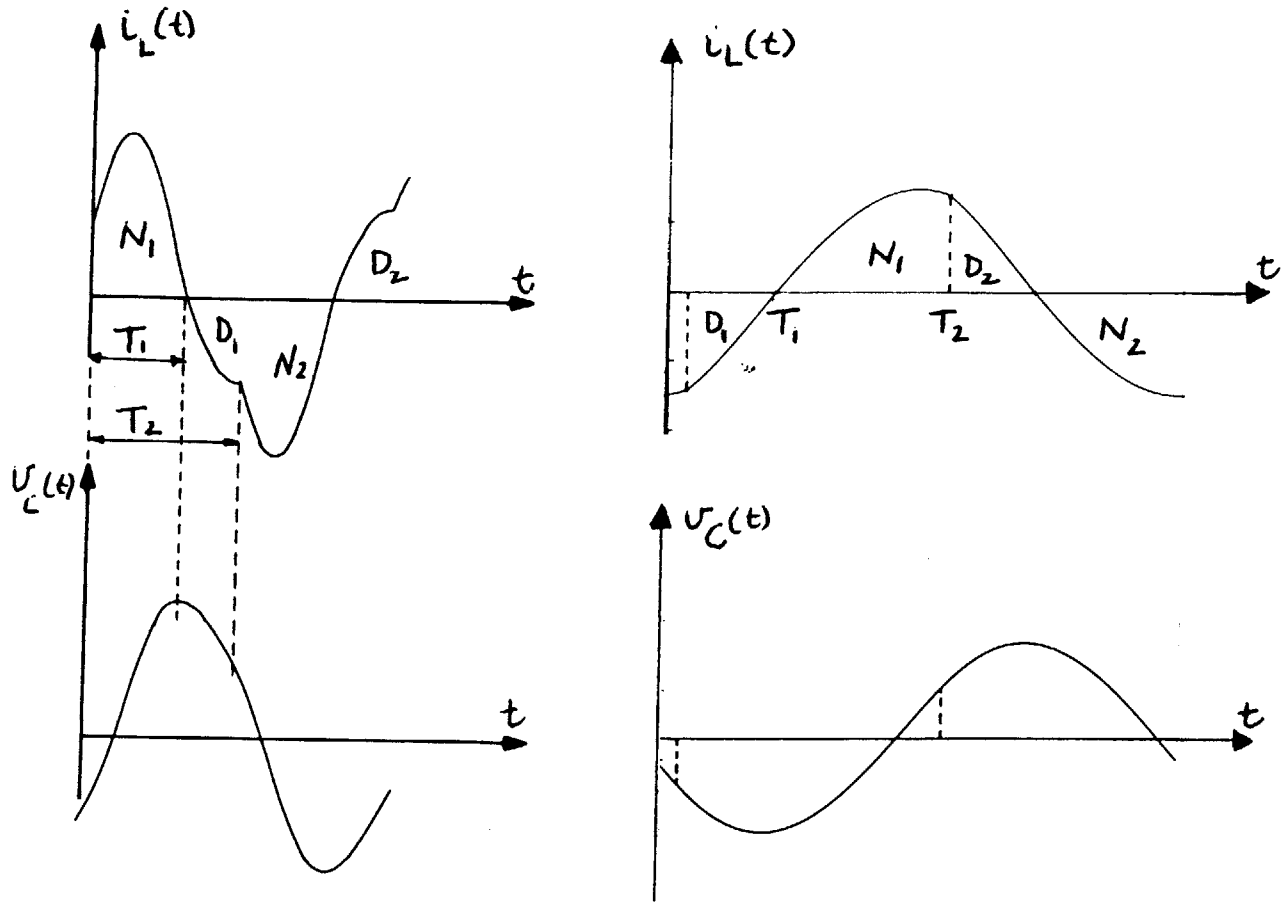
(5) The Voltage-Fed Series Resonant Converter

(A) Description of the basic operation

Many authors have analyzed the steady state operation of the voltage-fed series resonant converter of Fig. 4-1, in both the continuous and discontinuous conduction modes[28]- [33]. In this section the basic features of the operation of this converter are given. For a detailed description and analysis of this converter, the reader is referred to Stuart [32] and Vorperian [33].

InductEV, Inc.
Exhibit 1014
Page 120

The transistor/diode pairs N_1/D_1 and N_2/D_2 function as switches that cause the voltage V_{in} from the split dc source to be applied with alternating polarities across the series combination of the inductor L, the capacitor C and the diode bridge. The dc voltage source V_o in the bridge constitutes the load, and aids or opposes V_{in}, depending on the polarity of the inductor current $i_L(t)$. The waveforms of the inductor current $i_L(t)$ and the capacitor voltage $v_C(t)$ over a cycle of operation are shown in Fig. 4-5.



(a) $f_s < f_r$ (b) $f_s > f_r$

Fig. 4-5 State variables waveforms for the series resonant converter of Fig. 4-1

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Exhibit 1014
Page 121

The conducting order of the switches depends on the ratio of the switching frequency f_s to the resonant frequency f_r (= 1//LC). When this ratio is greater than 1, the conducting order is (D_1, N_1, D_2, N_2), as shown in Fig. 4-6a. As soon as N_2 is turned off (and N_1 turned on), marking the end of a cycle (e.g. the k-th cycle), D_1 begins to conduct, marking the beginning of the (k+1)-th cycle. D_1 eventually turns off at the transition time T_1, when its current $i_L(t)$ reaches the threshold value of 0, and N_1 begins to conduct. At time T_2 , N_1 is turned off (and N_2 turned on), marking the end of half the cycle and causing D_2 to begin conducting. The ensuing half cycle repeats the pattern of the half cycle before it.

For f_s less than f_r, the conducting order is (N_1, D_1, N_2, D_2), as shown in Fig. 4-6b. D_2 is turned off by turning on N_1, marking the end of the k-th cycle and the beginning of the (k+1)-th cycle. At the transition time T_1, N_1 turns off when its current i_L reaches the threshold value of 0, and D_1 turns on. At time T_2, D_1 is turned off by turning on N_2 and the next half cycle repeats. In this mode of operation thyristors can be used, and they are commutated naturally.

The conduction time T_1 is determined by the initial values of the inductor current and the capacitor voltage. The time T_2 is half the switching period and is controlled externally.

The switching frequency (or, equivalently, the switching period) is the primary control variable for such circuits [32],[33]. The magnitude of the steady-state response of the series LC pair, and hence the rectified load current i_o in the steady state, is clearly related to how much the switching frequency differs from the resonant frequency.

InductEV, Inc.
Exhibit 1014
Page 122

(B) Dynamic modeling

(i) The state-space description

As shown in Fig. 4-5, the series converter goes through four switch configurations every cycle. Each configuration in the (k+1)-th cycle has a linear time-invariant (LTI) state-space description of the form:

$$\frac{d\,\mathbf{x}(t)}{d\,t} = \mathbf{A}_{k,i}\,\mathbf{x}(t) + \mathbf{B}_{k,i}\,\mathbf{u}(t) \qquad (4.1)$$

$$i = 1,\ 2,\ 3,\ 4 \quad \text{and} \quad t_k + T_{k,i} < t < t_k + T_{k,i+1}$$

where:

$\mathbf{x}(t)$ = state variable vector. The capacitor voltage and the inductor current are the natural state variables.

$\mathbf{u}(t)$ = the vector of independent sources. When the load is resistive, this vector contains only the input voltage V_{in}, and when the load is a voltage source this vector has two components, which are the input voltage V_{in} and the output voltage V_o.

$\mathbf{A}_{k,i}$ and $\mathbf{B}_{k,i}$ are coefficient matrices.

t_k = the end of the k-th cycle and the beginning of the (k+1)-th cycle

$T_{k,i}$ = time from the beginning of the cycle till the end of the i-th switch configuration. Therefore $T_{k,0} = 0$, $T_{k,1} = T_1$ and $T_{k,2} = T_2$ = half the switching period.

Let us consider the operation of the series converter with the load being a voltage source, in the continuous conduction mode, and for f_s greater than f_r. The four switching configurations are shown in Fig. 4- 6. The state vector $\mathbf{x}(t)$ is:

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Exhibit 1014
Page 123

$$\mathbf{x}(t) = \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} = \begin{bmatrix} v_C(t) \\ i_L(t) \end{bmatrix} \tag{4.2}$$

The vector $\mathbf{u}(t)$ is:

$$\mathbf{u}(t) = \begin{bmatrix} V_{in}(t) \\ V_o(t) \end{bmatrix} \tag{4.3}$$

The matrix $\mathbf{A}_{k,i}$ is the same for each of the four configurations and is given by:

$$\mathbf{A}_{k,i} = \begin{bmatrix} 0 & 1/C \\ -1/L & 0 \end{bmatrix} \tag{4.4a}$$

and the matrix $\mathbf{B}_{k,i}$ is given by:

$$\mathbf{B}_{k,1} = -\mathbf{B}_{k,3} = \begin{bmatrix} 0 & 0 \\ -1/L & 1/L \end{bmatrix}, \tag{4.4b}$$

$$\mathbf{B}_{k,2} = -\mathbf{B}_{k,4} = \begin{bmatrix} 0 & 0 \\ 1/L & -1/L \end{bmatrix} \tag{4.4c}$$

InductEV, Inc.
Exhibit 1014
Page 124

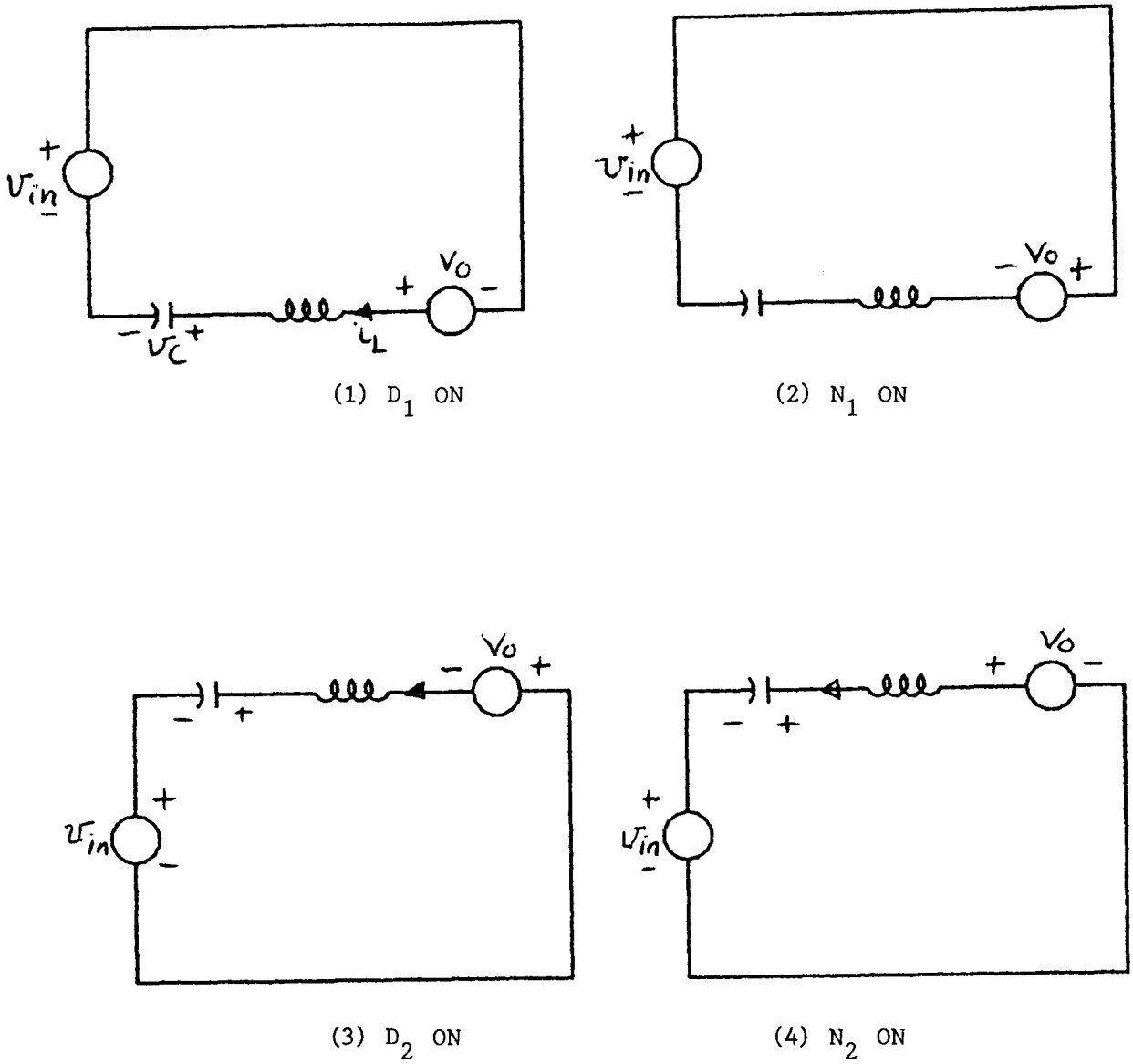

Fig. 4-6 The switching configurations for a series resonant converter during a complete switching cycle

Configurations 3 (D_2 conduction time) and 4 (N_2 conduction time) have the same matrices as configurations 1 (D_1 conduction time) and 2 (N_1 conduction time) respectively, except for a reversal of sign in the **B** matrices. This gives the circuit a half-cycle symmetry. That is to

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Exhibit 1014
Page 125

say, in the second half of each cycle, the transformed vector $-x(t)$ satisfies the same set of equations that $x(t)$ did in the first half-cycle. This symmetry property can be used to analyze the converter with equations written over only half the switching cycle instead of a full cycle.

For simplicity we shall, unless necessary, omit the subscript k. The solution of equation (4.1) will be:

$$x(t_k+T_{i+1}) = \phi_i(T_i, T_{i+1})\, x(t_k+T_i) + D_i(T_i, T_{i+1})u(t) \tag{4.5}$$

where:

$$\phi_i(t_i) = e^{(A_i t_i)}$$

$$D_i(T_i, T_{i+1}) = \int_{T_i}^{T_{i+1}} e^{(A_i t)} dt\,(B_i)$$

and

$$t_i = T_{i+1} - T_i$$

(ii) Nonlinear large-signal sampled-data model

The state vector $x(t)$ is continuous across each change in the switch configuration. The final state in one configuration is the initial state in the next. Therefore a discrete-time large signal model that describes the state $x(t_{k+1})$ at the end of the (k+1)-th cycle in terms of the state $x(t_k)$, the source waveforms and the transition times can be obtained by combining the four state transition equations expressed by (4.5), and given by the form below:

$$x(t_{V+1}) = f(x(t_k), P_k, T_k) \tag{4.6}$$

InductEV, Inc.
Exhibit 1014
Page 126

where:

$$\mathbf{T}_k = \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \end{bmatrix} \tag{4.7}$$

and

$$\mathbf{P}_k = \begin{bmatrix} V_{in} \\ V_o \\ L \\ C \\ T_2 \\ T_4 \end{bmatrix} \tag{4.8}$$

$\mathbf{T}_k$ is a vector of all the state transition times T_i's. These times are of two types: <u>directly controlled</u> and <u>indirectly controlled</u> transition times. The directly controlled transition times are T_2 and T_4. These times are controlled by an external action, namely turning on the appropriate transistor in the circuit of Fig. 4-1. The indirectly controlled transition times are T_1 and T_3. Those are times that depend on the state trajectories of the system, specifically when the inductor current goes to zero and turns off the diode that is on. These latter transition times are determined by the threshold conditions:

$$i_L(t_k+T_1) = 0 \tag{4.9a}$$

$$i_L(t_k+T_3) = 0 \tag{4.9b}$$

$\mathbf{p}_k$ is a vector of <u>controlling parameters</u>. These include the circuit parameters and the directly controlled transition times T_2 and T_4. The directly controlled parameters are common to **T** and **P**. T_2 is the second

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Exhibit 1014
Page 127

element of **T** and the fifth element of **P**. This relation can be expressed by the the following threshold condition:

$$\mathbf{T}[2] - \mathbf{p}[5] = 0 \tag{4.10a}$$

Similarly, T_4 is the forth element of **T** and the sixth element of **P**, and this relation gives the threshold condition:

$$\mathbf{T}[4] - \mathbf{p}[6] = 0 \tag{4.10b}$$

These two conditions, together with the conditions in equations (4.9) can be written as a 4x1 vector **c**, given below:

$$\mathbf{c}(\mathbf{x}(t_k), \mathbf{P}_k, \mathbf{T}_k) = \mathbf{0} \tag{4.11}$$

Equations (4.6) and (4.11) give the large-signal sampled-data model of the converter. It in fact follows from (4.5) that these equations actually have the form:

$$\mathbf{x}(t_{k+1}) = \mathbf{F}(\mathbf{T}_k, \mathbf{P}_k)\ \mathbf{x}(t_k) + \mathbf{G}(\mathbf{T}_k, \mathbf{P}_k) \tag{4.12a}$$

$$\mathbf{C}(\mathbf{T}_k, \mathbf{P}_k)\ \mathbf{x}(t_k) + \mathbf{D}(\mathbf{T}_k, \mathbf{P}_k) = \mathbf{0} \tag{4.12b}$$

Also, equations for the large-signal model of other variables, such as the peak or the average of the output current (rectified inductor current) can be written as an output equation of the form:

$$\mathbf{y}(k) = \mathbf{H}(\mathbf{x}(t_k, \mathbf{T}_k, \mathbf{P}_k) \tag{4.13}$$

where the vector **y**(k) contains contains variable calculated during the k-th cycle.

InductEV, Inc.
Exhibit 1014
Page 128

(a) Half-cycle versus full-cycle model

In this section we shall explore the symmetry properties of the state variables waveforms, shown earlier in Fig. 4-5, for the series resonant converter. These waveforms exhibit a half cycle symmetry which we shall use to obtain the large-signal model of equations (4.12). Fig. 4-7 shows the steady state waveform of the inductor current, and a transformed waveform of it which will allow us to obtain a model over a half cycle. The odd half cycles of Fig. 4-7b are the same as their corresponding half cycles in Fig. 4-7a, while the even half cycles are the negative of their corresponding waveforms. A similar discussion applies for the waveform of the capacitor voltage. Now, we need to develop a transformation matrix that will give a large signal model developed over a half cycle.

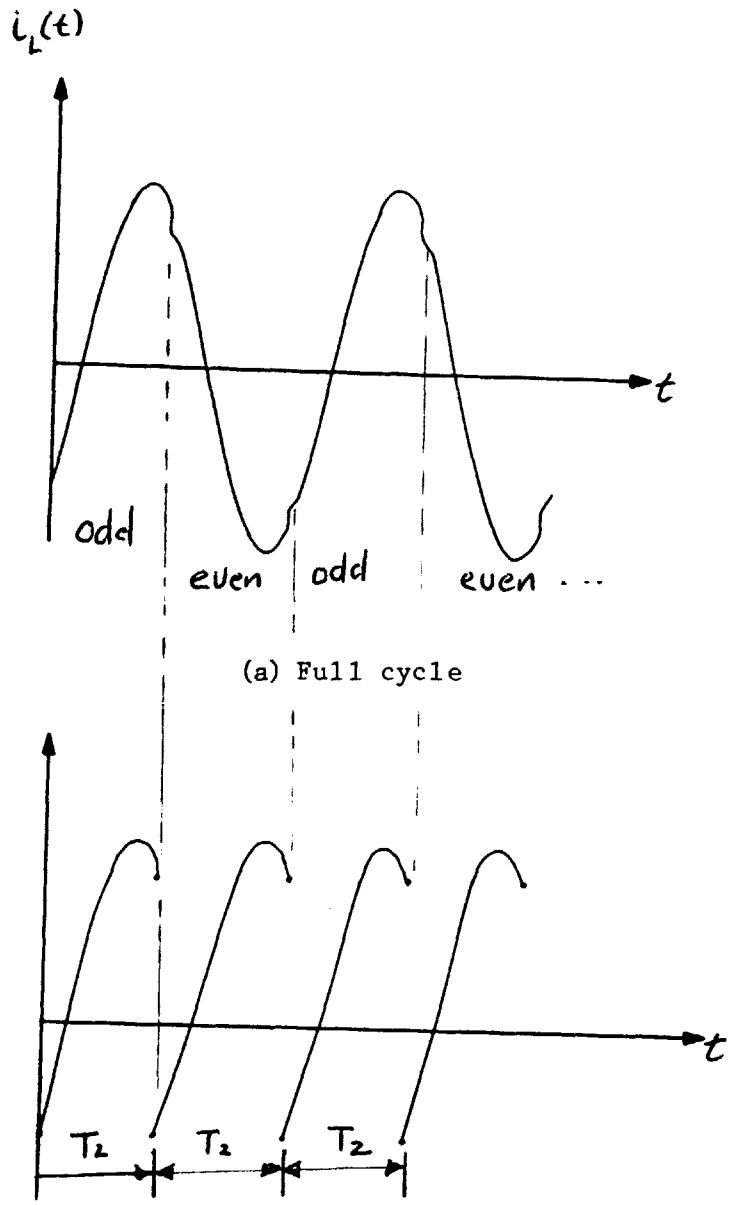
The equation for the state variables over the first half of each cycle (odd half cycle) is the same as equation (4.12), except that **F**(T,P) and **G**(T, P), which will be abbreviated as **F** and **G** respectively, are calculated over a half cycle, as given below:

$$\mathbf{F} = \begin{bmatrix} \cos(w_r T_2) & z_o \sin(w_r T_2) \\ -[\sin(w_r T_2)/z_0] & \cos(w_r T_2) \end{bmatrix}, \qquad (4.14a)$$

and

$$\mathbf{G} = \begin{bmatrix} V_1[\cos(w_r(T_2-T_1)-\cos(w_r T_2)] + V_2[1 - \cos(w_r(T_2-T_1))] \\ V_1[\sin(w_r T_2)-\sin(w_r(T_2-T_1)]/z_o + V_2[\sin(w_r(T_2-T_1))] \end{bmatrix}, \qquad (4.14b)$$

InductEV, Inc.
Exhibit 1014
Page 129



(a) Full cycle

(b) Half cycle

Fig. 4-7 Change of waveforms from sampling every cycle to sampling every half cycle

InductEV, Inc.
Exhibit 1014
Page 130

where:

$$V_1 = V_{in} + V_o, \quad V_2 = V_{in} - V_o, \quad w_r = 1//LC \text{ and } z_o = /L/C \qquad (4\text{-}14c)$$

The threshold condition, corresponding to equation (4.9a) is

$$\begin{aligned} i_L(t_k + T_1) &= c(\mathbf{W}\,\mathbf{x}(T_2),\ \mathbf{P},\ T_1) \\ &= [-(1/z_o)\sin(w_r T_1) \quad \cos(w_r T_1)]\mathbf{x}(t_k) \\ &\quad + [V_1 \sin(w_r T_1)]/z_o \end{aligned} \qquad (4\text{-}15)$$

Equations (4.12) for the second half-cycle (even half cycle) can be written using the one obtained for the odd half-cycle together with the symmetry of the wave forms, as follows:

$$\mathbf{W}\,\mathbf{x}(t_{k+1}) = \mathbf{W}\,\mathbf{F}\,\mathbf{x}(t_k+T_2) + \mathbf{W}\,\mathbf{G} \qquad (4.16a)$$

$$W[2,2]\ i_L(t_k + T_3) = \mathbf{W}\,c(\mathbf{W}\,\mathbf{x}(T_2),\ \mathbf{P},\ T_1) \qquad (4.16b)$$

where $\mathbf{W} = -I$ and is the transformation that was referred to earlier. $\mathbf{W}[2,2] = -1$, and it is the diagonal element in the second row and second column of $\mathbf{W}$.

With this transformation, a sampled-data large-signal model can be formed by sampling $\mathbf{x}(t_{k-1})$ and $\mathbf{W}\mathbf{x}(t_{k-1} + T_2)$ of Fig. 4-7. In other words, we sample $\mathbf{x}$ at the beginning of each odd half-cycle, and $\mathbf{W}\mathbf{x}$ at the beginning of each even half-cycle. In this case the sampled-data large-signal model is given by the following equation:

$$\mathbf{s}_{i+1} = \mathbf{W}\,\mathbf{F}\,\mathbf{s}_i + \mathbf{W}\,\mathbf{G} \qquad (4.17)$$

where:

$\mathbf{s}_{2k} = \mathbf{x}(t_k)$ and $\mathbf{s}_k = \mathbf{W}\,\mathbf{x}(t_{k-1} + T_2)$, $\mathbf{F}$ and $\mathbf{G}$ given as in equation (4.14).

InductEV, Inc.
Exhibit 1014
Page 131

The above discussion was based on the analysis over a half-cycle. Since the controlling parameters vary once per cycle, we can extend the half-cycle model to a full-cycle model by applying equation (4.16a) twice in succession. Using the fact that $\mathbf{W}^2 = \mathbf{I}$, and with $\mathbf{F}$ and $\mathbf{G}$ as defined by equation (4.14), we get

$$\mathbf{x}(t_{k+1}) = \mathbf{F}^2\, \mathbf{x}(t_k) + [\mathbf{F} - \mathbf{I}]\mathbf{G} \tag{4.18}$$

<u>An alternative approach</u> is to carry the calculations of $\mathbf{F}$ and $\mathbf{G}$ of equation (4.12) for a full cycle.

(iii) <u>The cyclic steady state</u>

The steady state solution of the circuit is found by solving either equation (4.6) or (4.12) along with (4.11) for some given constant $\mathbf{P}$. The model given by (4.12) is nonlinear because the period T_1 (the diode conduction time) is dependent on the state variables at the beginning of each half cycle, and, also, depends on the control variable T_2 which is buried in $\mathbf{F}$ and $\mathbf{G}$, as is evident from the threshold condition (4.9). Let the steady state values of the variables of equation (4.6) - (4.8) be defined as follows:

$$\begin{aligned}
&T_2 = T_S = \text{Sampling period},\\
&T_1 = T_1^*,\\
&\mathbf{P} = \mathbf{P}^*,\\
&\mathbf{x}(t_k) = \mathbf{x}(t_{k+1}) = \mathbf{X}\ ,\\
&t_k = kT_S\ ,\\
&t_{k+1} + T_2 = (k+1)T_S
\end{aligned} \tag{4.19}$$

InductEV, Inc.
Exhibit 1014
Page 132

The steady state values corresponding to equations (4.12) and (4.15) satisfy

$$\mathbf{X} = \mathbf{F}(T_1^*, \mathbf{P}^*)\ \mathbf{X} + \mathbf{G}(T_1^*, \mathbf{P}^*) \tag{4.20}$$

and

$$i_L(kT_S + T_1^*) = c(\mathbf{X}, T_1^*, \mathbf{P}^*) \tag{4.21}$$

For fixed values of the parameters of $\mathbf{P}$ and a switching period T_S, we need to determine the indirectly controlled T_1^* and the state vector $\mathbf{X}$. Two approaches are used to determine the steady state values. The first is an iterative approach which uses the Newton-Raphson method to numerically solve equations (4.20) and (4.21). Equation (4.20) is solved for some assumed value of T_1. The calculated $\mathbf{X}$ and the assumed T_1 are then substituted in (4.21). If (4.21) is not satisfied, then T_1 is updated using the Newton-Raphson correction, and the iteration continues till convegence is achieved.

The second approach is noniterative, and uses the phase plane method. It exploits the fact that for each switch configuration, the equation relating the inductor current and the capacitor voltage is the equation of a circle in the phase plane of i_L versus v_C. Simple equations can then be written to solve for the steady state values of T_1 and $\mathbf{X}$. The two methods are discussed in detail in Appendix 4A.

(iv) <u>The perturbed state and the small-signal sampled-data model</u>

In deriving the small signal model for the resonant converter, assume the state variables undergo small perturbations about the cyclic steady state solution of (4.20). For example, Fig. 4-8 shows the waveforms of the steady and perturbed inductor current. Denote the perturbations as follows:

InductEV, Inc.
Exhibit 1014
Page 133

$$\mathbf{x}_k = \mathbf{x}(t_k + \Delta_k) - \mathbf{X},$$

$$q_k = \mathbf{P} - \mathbf{P}^*,$$

$$t_1 = T_1 - T_1^*,$$

$$t_s = T_2 - T_S,$$

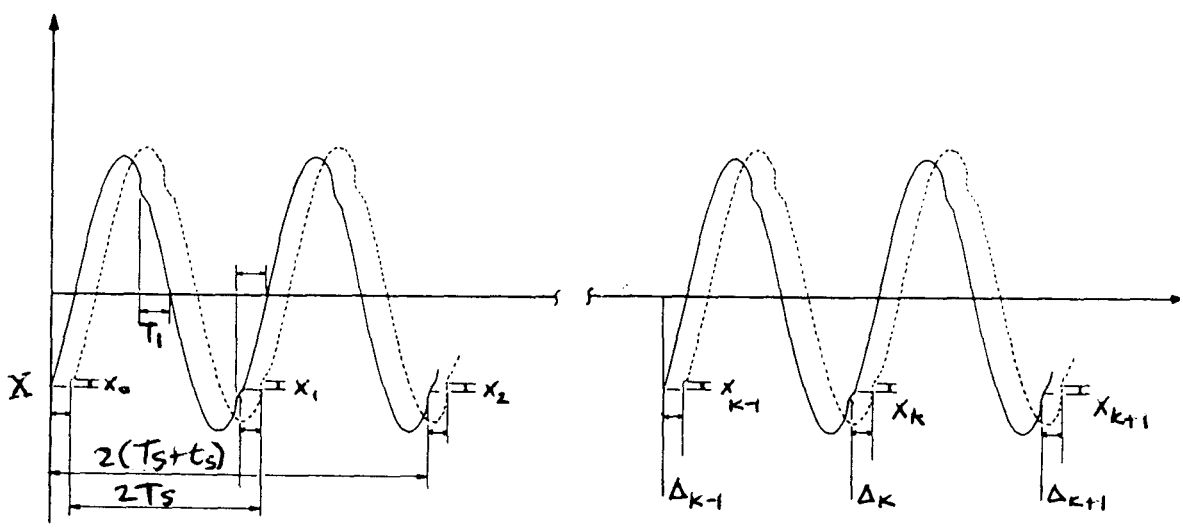


Fig. 4-8 Perturbed and steady state waveforms of the inductor current

Equations (4 16) for the large signal, obtained over a half cycle, also hold for the perturbed states, so that

$$\mathbf{x}[(k+1)T_S + \Delta_{k+1}] = \mathbf{F}(T_1^* + t_1, \mathbf{P}^* + \mathbf{q})\, \mathbf{x}(kT_S + \Delta_k) + \mathbf{G}(T_1^* + t_1, \mathbf{P} + \mathbf{q}) \qquad (4.23)$$

InductEV, Inc.
Exhibit 1014
Page 134

and

$$i_L(kT_S + \Delta_k + T_1^* + t_1) = c(x(kT_S+\Delta_k),\ T_1^* + t_1,\ P + q) = 0 \qquad (4.24)$$

Now expanding (4.23) and (4.24) in a Taylor series about the steady state values, retaining only the first-order terms, and abbreviating F(.., ..,) and G(.., ..,) by F and G respectively, we get

$$x[(k+1)T_S+\Delta_{k+1}] = [F + (\partial F/\partial P)q + (\partial F/\partial T_1)t_1]\ x(kT_S+\Delta_k)$$
$$+ G(T_1,\ P) + (\partial G/\partial P)q + (\partial G/\partial T_1)t_1 \qquad (4.25)$$

and

$$i_L(kT_S+\Delta_k+T_1^*+t_1) = c(X,\ T_1^*,\ P^*) + (\partial c/\partial X)\ x_k$$
$$+ (\partial c/\partial P)q + (\partial c/\partial T_1)t_1 = 0 \qquad (4.26)$$

All of the above partial derivatives are calculated at the cyclic steady state defined by equation (4.19). Now subtracting the steady state of equations (4.20) and (4.21) from equations (4.25) and (4.26) we get:

$$x((k+1)T_S+\Delta_{k+1}) - X = F\ [x(kT_S+\Delta_k) - X] + [(\partial F/\partial P)q + (\partial F/\partial T_1)t_1](X+x_k)$$
$$+ (\partial G/\partial P)q + (\partial G/\partial T_1)t_1 \qquad (4.27)$$

and

$$(\partial c/\partial X)x_k + (\partial c/\partial P)q + (\partial c/\partial T_1)t_1 = 0 \qquad (4.28)$$

Since T_1 depends on X and P, the perturbation t_1 should be eliminated from (4.27). This can be done by obtaining t_1 in terms of q and x_k using (4.28), and substituting into (4.28). We then get the following equation:

$$x_{k+1} = F\ x_k + [(\partial F/\partial P)X]q + (\partial G/\partial P)q$$
$$- (\partial c/\partial T_1)^{-1}\{(\partial G/\partial T_1)[(\partial c/\partial\ X)\ x_k + (\partial c/\partial P)q]$$
$$+ (\partial F/\partial T_1)X[(\partial c/\partial\ X)\ x_k + (\partial c/\partial P)q]\} \qquad (4.29)$$

InductEV, Inc.
Exhibit 1014
Page 135

or

$$x_{k+1} = [F - (\partial c/\partial T_1)^{-1} [\partial G/\partial T_1 + (\partial F/\partial T_1)X](\partial c/\partial X)x_k$$
$$+ [(\partial F/\partial P)X + (\partial G/\partial P)$$
$$- (\partial c/\partial T_1)^{-1}(\partial G/\partial T_1 + (\partial F/\partial T_1)X)(\partial c/\partial P)]q \qquad (4.30)$$

Now we can write equation (4.30) in the form:

$$x_{k+1} = A\, x_k + Bq_k \qquad (4.31)$$

where:

$$A = [F - (\partial c/\partial T_1)^{-1} [\partial G/\partial T_1 + (\partial F/\partial T_1)X](\partial c/\partial X)$$

and

$$B = [(\partial F/\partial P)X + (\partial G/\partial P)$$
$$- (\partial c/\partial T_1)^{-1}(\partial G/\partial T_1 + (\partial F/\partial T_1)X)(\partial c/\partial P)] \qquad (4.32)$$

Equation (4.31), which gives the relation between two successive perturbations, constitutes a sampled-data model for the series resonant converter's dynamics response to small perturbations in the switching period, the input voltage, the output voltage or the circuit parameters.

If T_2 (time at which transistors are turned on and off) is the only control variable, in P, that is varied from one half cycle to the other, then the nominal switching instant (steady state switching instant) and the actual switching instant are different by some amount Δ, as shown in Fig. 4-9. Although the sampling instant varies from the nominal switching instant, these variations are not troublesome if

$$\Delta_k = \sum_{j=1}^{k} t_{j,s} \qquad (4.33)$$

is small compared with the nominal switching period T_S,

where:

$t_{j,s}$ is the perturbation in the duration of the j-th switching cycle.

InductEV, Inc.
Exhibit 1014
Page 136

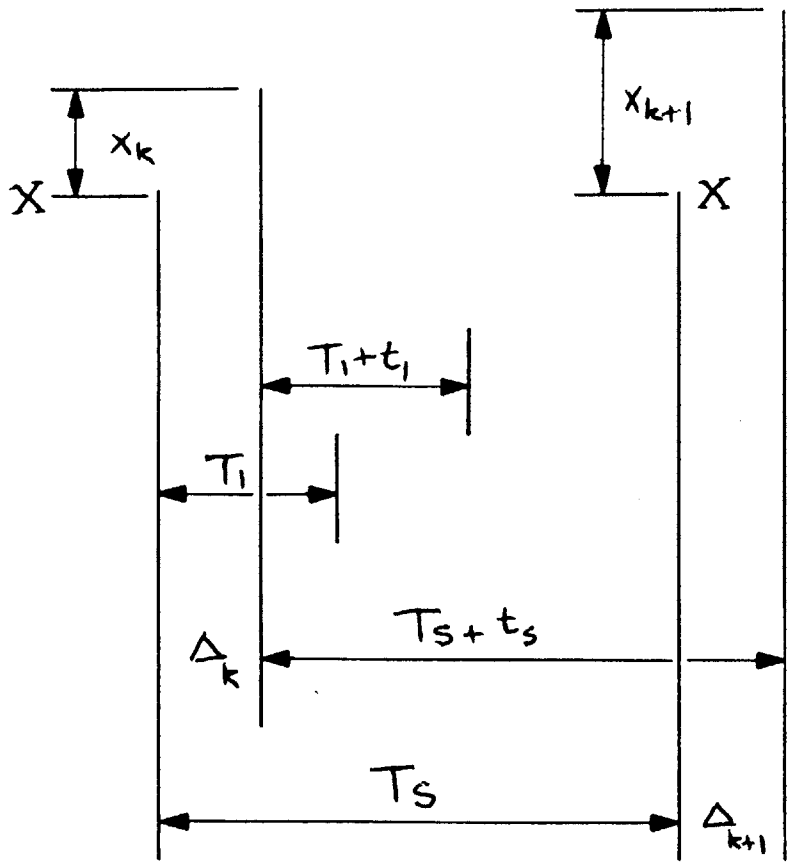


Fig. 4-9 Nominal and perturbed states of a resonant converter over a half cycle

The matrix **A** of (4.32) consists of two parts, when the load is a voltage source. One is the **F** matrix calculated in (4.14), and the other is a term that includes the dependence of the indirectly controlled transition times (T_1) on the state trajectory. In the case where the load is resistive, the **F** and the **G** matrices of (4.14) are no longer dependent on T_1. This is because the configurations for the transistor conduction time and the diode conduction time are the same. In other words, the matrices $\mathbf{A}_{k,i}$ and $\mathbf{B}_{k,i}$ of equation (4.1) are the same for the diode and the transistor conduction times. Therefore the **A** of the small-signal model is equal to the **F** matrix of (4.14). Hence, the frequency of the response of the converter state variables to a step change in the switching frequency, or to any other control parameter, for

InductEV, Inc.
Exhibit 1014
Page 137

a resistive load, is the damped resonant frequency of the circuit.

With the **A** and the **B** matrices calculated over a half-cycle (i.e using the half-cycle large-signal model of (4.31)), the small signal model can be formed by sampling the perturbation $\mathbf{x}_k$ at the beginning of each odd half-cycle and $\mathbf{W}\mathbf{x}_{k+1}$ at the beginning of each even half-cycle. The small-signal model over a half cycle is then given by:

$$\mathbf{s}_{i+1} = \mathbf{W}\,\mathbf{A}\,\mathbf{s}_i + \mathbf{W}\,\mathbf{B}\,\mathbf{q}_i \tag{4.34}$$

with $\mathbf{s}_i$ and $\mathbf{x}_i$ related, as before, by equation (4.17).

The model over a full-cycle can be found by a similar discussion to the one for the large-signal model. If the controlling parameters vary once per cycle, the half cycle model can be extended to a full cycle model by applying equation (4.31) twice in succession. The small signal model over a full-cycle then becomes

$$\mathbf{x}_{k+1} = \mathbf{A}^2\,\mathbf{x}_k + [\mathbf{A} - \mathbf{I}]\mathbf{B}\mathbf{q}_k \tag{4.35}$$

(v) <u>Eigenvalues and frequency-domain expressions</u>

Equations (4.34) or (4.35) give the time-domain representation of the perturbed system. To find the frequency-domain representation, we take the z-transform of (4.34) which gives:

$$\mathbf{S}(z) = (z\mathbf{I} - \mathbf{W}\mathbf{A})^{-1}\mathbf{W}\mathbf{B}\,\mathbf{Q}(z) \tag{4.36}$$

This gives the transfer function $(z\mathbf{I} - \mathbf{W}\mathbf{A})^{-1}\mathbf{W}\mathbf{B}$, from which the poles and zeros of the system are determined. Bode-plots and root loci as a function of any of the circuit parameters can then be computed. The poles of the system transfer function, for the half cycle model, are the eigenvalues of the matrix **W A**. For the full-cycle model of equation

InductEV, Inc.
Exhibit 1014
Page 138

(4.35), the poles of the transfer function are the eigenvalues of the matrix A^2.

(vi) Perturbation in the switching frequency

If the interest is to develop a dynamic model of the the response to perturbations in the switching frequency instead of in the switching period, we use the fact that the steady state switching frequency (F_S) is related to the switching period (T_S) by the following equation:

$$T_S = 1/2F_S \tag{4.37}$$

and the perturbations t_s and f_s in T_S and F_S respectively are therefore related by the following equation:

$$t_s = \frac{\partial T_S}{\partial F_S} f_s = -\frac{1}{2F_S^2} f_s \tag{4.38}$$

(vii) Generalization of the model to other power electronic circuits

The sampled-data small-signal model developed for the series resonant converter has been generalized to other power electronic circuits. The procedure is described in [61].

(6) Results and Discussion

In this section we shall present some of the results of the sampled-data small-signal model for the series resonant converter. Results obtained from the mathematical model will be compared with those obtained using the Parity Simulator.

(A) Effects of the parity simulator parasitic elements

There are some nonidealities of the Simulator components that will contribute to the discrepancy between the theoratical and experimental

InductEV, Inc.
Exhibit 1014
Page 139

results. For stability reasons, each element in the Parity Simulator has a resistance of 5.0 ohms in series with it. The inductor model also has a parallel resistance, the value of which depends on the value of the inductance. These appear in the simulated circuit after they are multiplied by the impedance scale factor. It is found that these resistors have an effect on the value of the steady state point of the series resonant converter. The parameters of the converter circuit and the scale factors, as given earlier, are:

$L = 1.94E-6$ H $\quad C = 1.0E-7$ F

$V_{in} = 14V \quad F_S = 40$ kHz

fsc = 2.5E-4 $\quad$ isc = 0.001 $\quad$ vsc = 0.1

With these element values and scale factors, each element has a resistor of 0.2 ohms in series with it. The parallel resistor across the inductor is 1880 ohm. In each switch configuration there are seven elements connected in series, so the total series resistance becomes 1.4 ohms. The modified circuit is shown in Fig. 4-10.

(B) <u>Results</u>

The results obtained from the mathematical model agree with those obtained using the Parity simulator. Given in Fig. 4-11 is a printout of the results of the mathematical model obtained for the dynamics of the series converter, when the output voltage V_o is zero. The frequency of response of the output current (the rectified inductor current) in this case is 4.172 kHz. This frequency equals the difference between the switching frequency (40 kHz) and the resonant frequency (35.586 kHz).

InductEV, Inc.
Exhibit 1014
Page 140

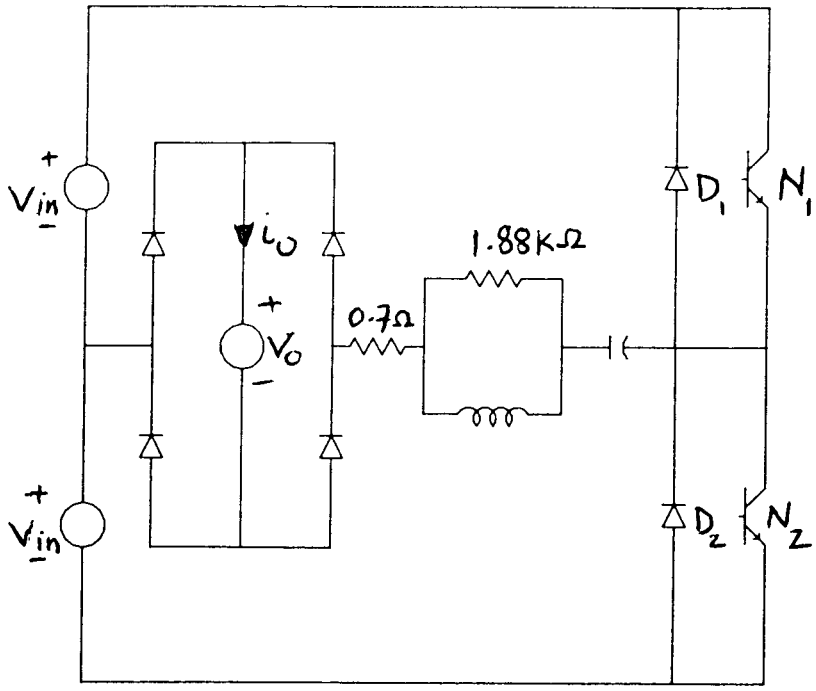


Fig. 4-10 The series resonant converter circuit including the parasitic resistors on the simulator

```
Steady state results are:
-------------------------

ILO  = -1.8070047870E+00
VCO  = -1.9054185812E+01
T1   =  5.2257566028E-06

  The simulation results (using full period):-
  --------------------------------------------

THE F MATRIX
[  6.8048438620E-01          1.1787618525E-02]
[                                             ]
[ -2.3405727626E+01          6.8639919314E-01]
[                                             ]

THE G MATRIX
[ -2.4483847438E+04]
[                   ]
[ -1.7252606594E+07]

THE POLES OF THE SYSTEM IN THE Z-PLANE ARE
z1  =   6.8344178967E-01 +j   5.2525140867E-01
z2  =   6.8344178967E-01 -j   5.2525140867E-01

THE CORRESPONDING POLES ON THE S-PLANE ARE
s1  =  -5.9416766921E+03 +j   2.6210425399E+04
s2  =  -5.9416766921E+03 -j   2.6210425399E+04
wn  =   2.6875452024E+04        zeta =   2.2108192587E-01
fn  =   4.2773610374E+03          fd  =   4.1715187627E+03

THE ZERO OF THE INDUCTOR CURRENT IN THE Z-PLANE IS
zi  =   -7.6197767702E+00

THE ZERO OF THE CAPACITOR VOLTAGE IN THE Z-PLANE IS
zv  =    7.1370036787E-01
```

Fig. 4-11 Results of the small-signal model for the series resonant converter of Fig. 4-10, when V_o = 0.0 V

InductEV, Inc.
Exhibit 1014
Page 141

The response obtained from the Parity Simulator is shown in Fig. 4-12. The frequency of oscillation of the response of the output current is voltage about 1.11 Hz. When this frequency is divided by the frequency scale factor (2.5 E-4), to get the frequency on the actual circuit, it is found that the frequency of the response is 4.44 kHz which agrees well with the results obtained from the model.

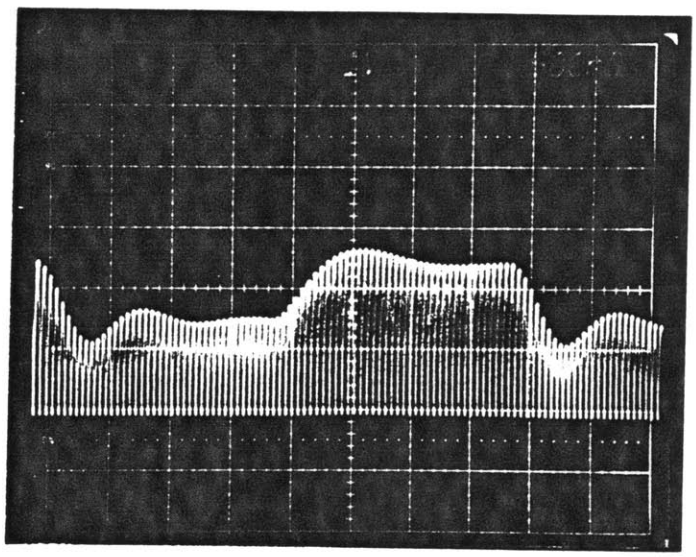


Fig. 4-12 Response of the output current i_o to a 5% step in the switching frequency

Another example of the match between the results of the model and those of the Simulator may be seen when V_o is equal to 5.0 V. As stated in the simulation shown in Section 3, the response from the Parity Simulator has a kick in the opposite direction of the steady state. This raises the question of the existence of a right half-plane zero. Fig. 4-13 shows the model results when V_o is 5.0 V. The zero of the inductor current transfer function in the z-domain is at z = 1.527 which is to the right of +1 and therefore corresponds to a right half-plane zero.

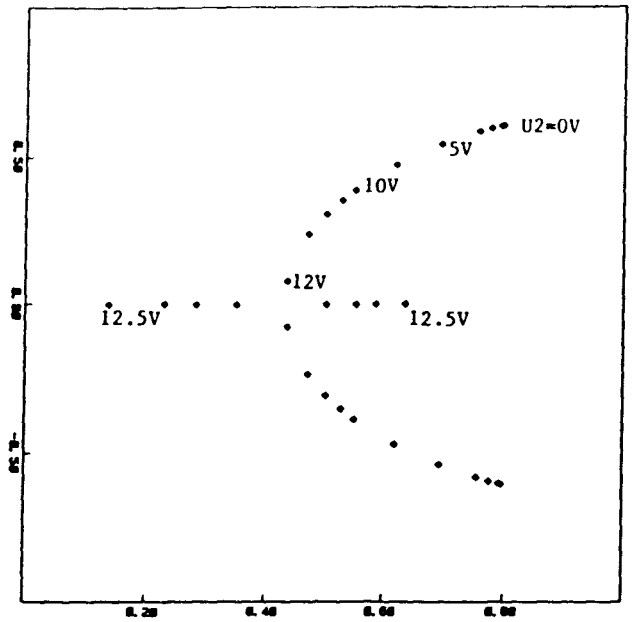
InductEV, Inc.
Exhibit 1014
Page 142

```
Steady state results are:

ILO  = -1.3297899039E+00
VCO  = -3.4490986178E+01
T1   =  3.6971288654E-06

  The simulation results (using half period):-

THE F MATRIX
[  8.4357604604E-01          7.5445676481E-03]
[                                             ]
[ -1.0173781722E+01          7.9954598063E-01]
[                                             ]

THE G MATRIX
[  1.3874283337E+05]
[                  ]
[ -1.3387629348E+07]

THE POLES OF THE SYSTEM IN THE Z-PLANE ARE
z1  =   8.2156101334E-01 +j   2.7617408057E-01
z2  =   8.2156101334E-01 -j   2.7617408057E-01

THE CORRESPONDING POLES ON THE S-PLANE ARE
s1  =  -1.1441490560E+04 +j   2.5943227899E+04
s2  =  -1.1441490560E+04 -j   2.5943227899E+04
wn  =   2.8354166890E+04          zeta =   4.0352060438E-01
fn  =   4.5127058178E+03           fd  =   4.1289929598E+03

THE ZERO OF THE INDUCTOR CURRENT IN THE Z-PLANE IS
zi  =    1.5275394403E+00

THE ZERO OF THE CAPACITOR VOLTAGE IN THE Z-PLANE IS
zv  =    7.3813995534E-01
```

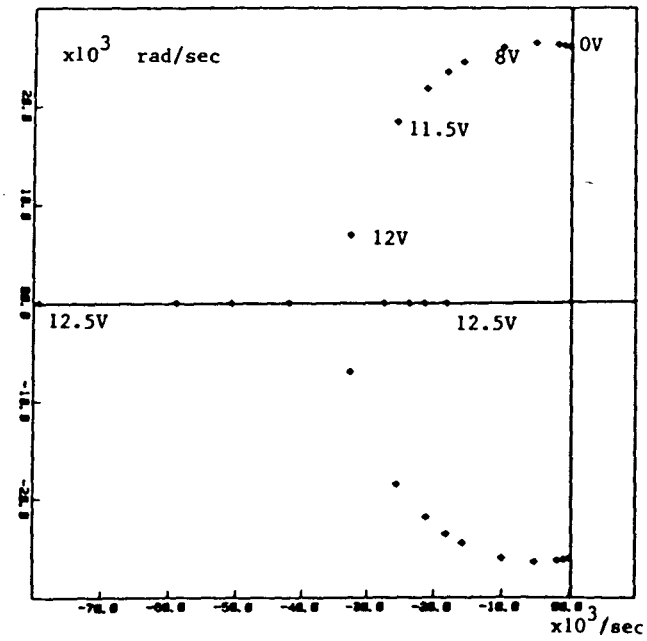
Fig. 4-13 Results of the small-signal model for the series resonant converter of Fig. 4-10, when V_o = 5.0 V

Fig. 4-14a shows the locus of natural frequencies or poles (which are just the eigenvalues of A^2) for the discrete-time system of (4.35) as the load voltage V_o varies. Mapping these back to "equivalent" continuous-time poles, using the transformation $z = e^{sT_S}$, we get Fig. 4-14b. For small values of V_o the poles are lightly damped and at the difference between the switching and resonant frequencies. It is essentially at this difference frequency that the envelope of the resonant current is observed to ring in response to a small step change in the switching frequency, as discussed earlier for the case of V_o = 0.

InductEV, Inc.
Exhibit 1014
Page 143



(a) Discrete-time poles



(b) "Equivalent" continuous-time poles

Fig. 4-14 Locus of the poles as V_o is varied

InductEV, Inc.
Exhibit 1014
Page 144

(7) Other Related Issues

The dynamic model obtained for the series converter allows the calculation of the sensitivity of the steady state to parameter variations. It also makes the automatabilty of the analysis of such converters feasible. The two issues are discussed in the following sections.

(A) Sensitivity Analysis

It is important to know the effects of component and control parameter variations on both the steady state and the dynamic behavior. Sensitivity calculations can be derived directly from the expressions developed for the dynamic model of a converter. For example, to find the effect a system parameter on the system Dehavior, the parameter is included as a control parameter P[i] of the vector P_k. To find the expression for the sensitivity, assume that we want the sensitivity of X[j] with respect to the control parameter P[i]. Then the normalized sensitivity is defined as:

$$S^{P[i]}_{X[j]} = (\Delta X[j]/X[j])/(\Delta P[i]/P[i]) \qquad (4.39)$$

X[j] and P[i] are the steady state values, and given in (4.19). Now Δ X[j]/ΔP[i] is the element determined by the j-th row and the the i-th column of the Jacobian [ΔX/ΔP], which can be obtained from (4.31) as:

$$[\Delta X/\Delta P] = -(I - A)^{-1}B \qquad (4.40)$$

where A and B are as defined in equation (4.32). This shows that the partial derivative matrices of F, G and c with respect to X, P and T that have been calculated for the sampled-data model can be used to determine the sensitivity.

InductEV, Inc.
Exhibit 1014
Page 145

(B) Automatability

Computer programs capable of determining transient and steady state responses of large linear networks are available. These programs solve the circuit equations from a simple description of the circuit topology and components. Some of these programs solve the circuit equations symbolically, while others use numerical techniques. The symbolic techniques obtain relations among circuit parameters, irrespective of any numerical values, while the numerical methods need numerical values to start various computational procedures. Symbolic analysis can provide greater insight into the problem and its solution; furthermore, solving the problem for a new choice of parameter values usually involves only substitution and evaluation, rather than starting the analysis again from scratch.

In the area of power converters, some of these techniques have been successfully used to automate the analysis dc-dc converters, using state-space-averaged models [63]. The key steps to automatically obtaining a general sampled-data model may follow steps similar to [59], where symbolical as well as numerical possibilities are discussed.

Symbolic automation

The use of digital computers in designing power converters has been limited to numerical computations. However there is a growing availability of programs such as MACSYMA [64] and SMP [65] to obtain symbolic solutions of circuits. Such programs are attractive to consider for use in automated model derivation and analysis. MACSYMA (Project MAC's SYmbolic MAnipulation Program) is a computer package developed over many years by the Mathlab Group at MIT. The program, written in LISP, is capable of performing symbolic as well as numerical

InductEV, Inc.
Exhibit 1014
Page 146

mathematical manipulations. We have used this program to derive a small signal sampled-data model for the series resonant converter. All the computations involved, starting from the state-space description of equation (4.1) and going via the sampled-data descriptions (4.12) and (4.15) to the small signal model given by (4.32) are carried out using MACSYMA, yielding a symbolic model for the converter. Thus, each time a new values for the converter parameters are given, the new model is determined by simple substitution for the symbols after the new cyclic steady state has been calculated numerically from (4.19). Matrix exponentials and their associated integrals, as well as partial derivatives and other results are obtained symbolically. In addition, plotting and numerical computations can be carried out using MACSYMA. Although the computations are done interactively, MACSYMA can also be run in a batch mode. Therefore, essentially all the steps needed for automated symbolic derivation of the general sampled-data model are available. Other examples of use symbolic analysis of circuits can be found in [53] and [54].

Numerical automation

As pointed out earlier, a lot of programs that numerically determine the behavior of power converters are available. For instance, most of the numerical programs used in [63] for automating dc-dc converter models can be used in the automation of our general sampled data model. Programs for numerically obtaining the state equations from a circuit description exist and have been discussed in many text books [53], [54], [68]. Many routines have been written to numerically calculate matrix exponentials and their integrals [66], [67].

InductEV, Inc.
Exhibit 1014
Page 147

Computation of the perturbations and derivation of the small signal model as well as eigenvalues and frequency response are very much the same as those used in [63].

InductEV, Inc.
Exhibit 1014
Page 148

APPENDIX 4A

SOLUTION OF THE STEADY STATE FOR THE SERIES RESONANT CONVERTER

(1) Introduction

In this appendix we will discuss two methods for solving the steady state nonlinear equations of the series resonant converter discussed in chapter IV. The first is the Newton-Raphson iterative method, and the second is a noniterative method that uses phase plane techniques.

The state variable vector $\mathbf{x}(t)$, as defined in Chapter IV, has the inductor current $i_L(t)$ and the capacitor voltage $v_C(t)$. The steady state is defined by the periodic or cyclic operation, as:

$$\mathbf{x}(2T_s) = \mathbf{x}(0) = -\mathbf{x}(T_s) = \mathbf{X} \tag{4A.1}$$

where T_s is defined as half the switching period, and the minus sign is because of the half-cycle symmetry of the waveforms of the state variables.

The nonlinear equation relating the state vector $\mathbf{X}$ to the circuit parameters $\mathbf{P}$ and the indirectly controlled transit time T_1 can be written as:

$$\mathbf{X} = f(\mathbf{X}, \mathbf{P}, T_1) \tag{4A.2}$$

This equation is nonlinear because the transit time T_1 depends on the state $\mathbf{X}$ and control vector $\mathbf{P}$. Two methods have been used, and will be described in the following sections.

(2) The Iterative Solution (Newton-Raphson Method)

The dependance of T_1 on $\mathbf{X}$ is given by the threshold condition that the inductor current, which is also the diode current, vanishes at the end of the transit time T_1, and is given by the equation below:

InductEV, Inc.
Exhibit 1014
Page 149

$$i_L(T_1) = c(X, P, T_1) \qquad (4A.3)$$

This threshold equation (4A.3) together with the nonlinear equation (4A.2) can be used in an iterative numerical method to solve for the steady state values of X and T_1. The Newton-Raphson method has been used, and the steps of the solution are given below:

(i) Assume a value for T_1 (A better guess should be less than T_s).

(ii) Calculate the value of X using equations (4A.2).

(iii) Substitute the calculated values of (ii) and T_1 in equation (4A.3). If the result is zero then the assumed T_1 and the calculated X are the required steady state values.

(iv) If the result of (iii) is not zero, then update T_1 as follows:

$$T_1)_{new} = T_1)_{old} - \frac{i_L(t_k + T_1)_{old})}{DEN} \qquad (4A-4)$$

$$\text{where} \quad DEN = \frac{\partial i_L}{\partial T_1} + \frac{\partial i_L}{\partial V_C}\frac{\partial V_C}{\partial T_1} + \frac{\partial i_L}{\partial I_L}\frac{\partial I_L}{\partial T_1}$$

$$\text{and} \qquad i_L = i_L(t_k + T_1)$$

(v) Repeat steps (ii) through (iv) until (4A.3) is satisfied.

(3) <u>Non-iterative method (The Phase Plane method)</u>

It turns out that for the case of the series resonant converter, a non-iterative method can be used to find steady state. The solution of each state equation for the converter can be represented by an arc of a circle in a phase plain of $i_L(t)$ vs. $v_C(t)$. To illustrate this consider

InductEV, Inc.
Exhibit 1014
Page 150

the circuit of Fig. 4A-1 which represents any of the four switching configurations. The only variation in this circuit is that polarity of the output voltage v_0 changes, depending on which switch is conducting.

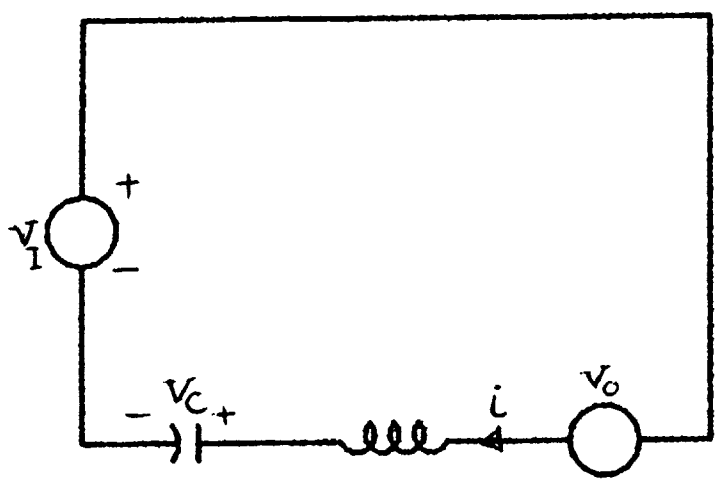


Fig. 4A-1 Circuit diagram for the switching configurations of the series resonant converter

KVL for the circuit can be written as:

$$v_C + v_L = (v_I \pm v_0) \tag{4A.4a}$$

with,

$$i_L = C\, dv_C/dt \tag{4A.4b}$$

$$v_L = L\, di_L/dt \tag{4A.4c}$$

Therefore

$$v_C + LC \frac{d^2 v_C}{dt^2} = (v_I \pm v_0) \tag{4A.5a}$$

multiplying (4A.5.a) by dv_C/dt gives

$$v_C \frac{d\, v_C}{d\, t} + L\, C \frac{d\, v_C}{d\, t} \frac{d^2\, v_C}{d\, t^2} = (v_I \pm v_0) \frac{d\, v_C}{d\, t} \tag{4A.5b}$$

InductEV, Inc.
Exhibit 1014
Page 151

which can be written as

$$v_C \, dv_C + (LC/2) \, d(i_L/C)^2 = (v_I \pm v_O) \, dv_C \qquad (4A.5c)$$

If $z_o = /L/C$ and $v' = i_L \, z_o$ then (4A.5.c) becomes

$$v_C \, dv_C + (1/2) \, d \, v' = (v_I \pm v_O) \, dv_C \qquad (4A.6)$$

integrating (4A.6) gives:

$$v_C^2 + v'^2 = 2(v_I \pm v_O) \, v_C + K \qquad (4A.7)$$

which can be written as:

$$(v_C + V_1)^2 + v'^2 = D^2 \qquad \text{with } V_1 = v_I + v_O \qquad (4A.8a)$$

OR

$$(v_C + V_2)^2 + v'^2 = Q^2 \qquad \text{with } V_2 = v_I + v_O \qquad (4A.8b)$$

K, Q and D are constants.

The phase plane of v' vs v_C is shown on Fig. 4A-2.

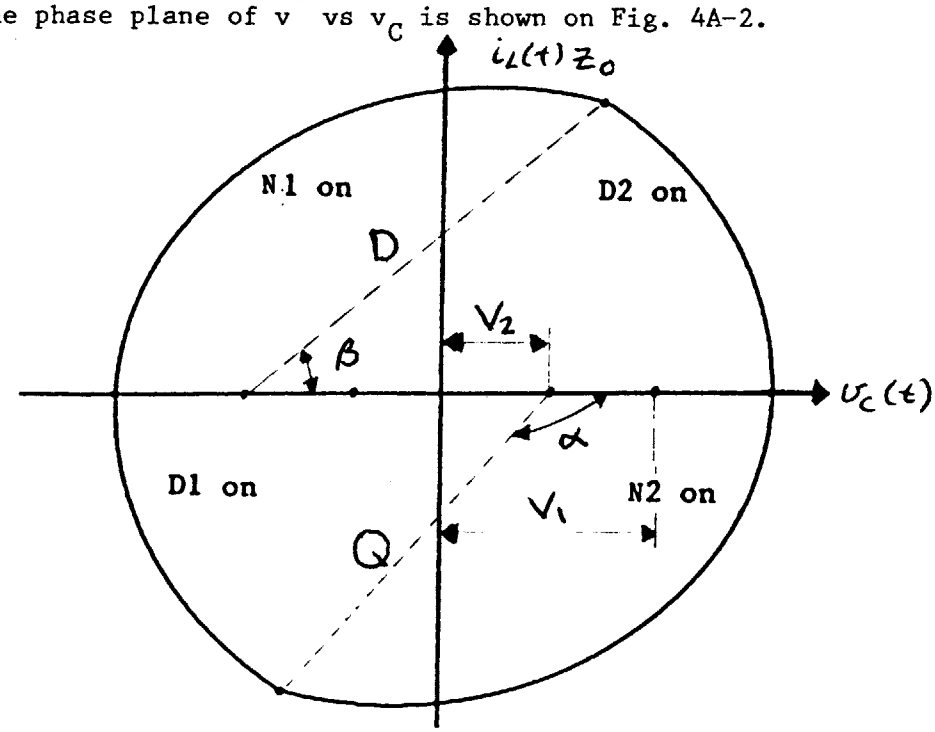


Fig. 4A-2 Phase plane of the inductor and the capacitor voltages over a complete switching cycle

InductEV, Inc.
Exhibit 1014
Page 152

Equations can be written from this phase plane and can be solved for the steady state V_C, I_L and T_1 as follows:

$$V_2 + Qe^{j\alpha} = -V_1 + De^{j\beta} \tag{4A.9}$$

Symmetry gives:

$$-V_2 + Q = -V_1 + D \tag{4A.10}$$

Diode conduction time + transistor conduction time = T_s

$$\text{or } (\pi - \alpha) + \beta = W_r T_s \tag{4A.11}$$

Equation (4A.9) gives

$$2 v_I = De^{j\alpha} - Qe^{j\beta} \tag{4A.12}$$

Equation (4A.10) gives:

$$2 v_0 = D - Q \tag{4A.13}$$

Substituting from (4A.11) and (4A.13) in (4A.12) gives

$$2 v_I = D e^{j(W_r T_s - \pi + \alpha)} - (D - 2v_0)e^{j\alpha} \tag{4A.14}$$

Equating the real parts of (4A.14) gives

$$(2 v_I)^2 = [(D \cos(W_r T_s - \pi) - (D-2v_0)]^2 + D^2 \sin^2 (W_r T_s - \pi)$$

which gives the following quadratic equation in D:

$$D^2 - 2v_0 D - V_1 V_2/\cos^2(W_r T_s) = 0 \tag{4A.15a}$$

which can be solved for D as:

$$D = v_0 + v_0^2 + V_1 V_2/\cos^2(W_r T_s) \tag{4A.15b}$$

InductEV, Inc.
Exhibit 1014
Page 153

$$Q = D - 2\ v_0 \tag{4A.15c}$$

$$\alpha = -\tan^{-1}\left(\frac{D \sin(W_r T_s - \pi)}{-D\ (1 + \cos W_r T_s) + 2\ v_0}\right) \tag{4A.15d}$$

$$\beta = \pi - \alpha \tag{4A.15e}$$

The steady state values are given by:

$$T_1 = (\beta / W_r) \tag{4A.16a}$$

$$V_C = B + Q \cos\alpha \tag{4A.16b}$$

$$I_L = Q \sin\alpha / z_o \tag{4A.16c}$$

This phase plane method in addition to giving the exact steady state solution, it saves a lot of computational time compared to the iterative method. It may also applicable to all dc-dc resonant converter. It can also be of potential for the studying the large signal response of the converter.

InductEV, Inc.
Exhibit 1014
Page 154

CHAPTER V

CONTROL OF RESONANT CONVERTERS

(1) Introduction

The ability to characterize a resonant converter by a dynamic model, using results of the previous chapter, makes the control system synthesis for the converter possible. Ways to better control the converter through feedback loops can be developed by examining different controllers in the context of the model.

The essential control task is to implement a control algorithm that generates the control signals to the converter based on measured output signals from the converter. The controller must also generate the control signals fast enough to retain control of the plant. Therefore, speed can be a severe limitation on the controller for systems with dynamics at high frequency. The use of microprocessors as a replacement for conventional analog controllers, to implement discrete controllers, therefore has advantages and limitations. The advantages are flexibility, programmability and the ability to handle other supplementary functions like start up and protection. On the other hand, since the controller must operate in real time, there is a speed limitation when controlling a very high speed system.

In resonant converters one usually controls the output voltage or current by varying the ratio f_s/f_r. In the past, designers have used the static characteristics of the converter (dc gain) to control the switching frequency. Such a controller can lead to stability problems. A dynamic model such as the one developed in Chapter IV is useful in determining the exact transfer function of the converter, which allows a

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Exhibit 1014
Page 155

circuit designer to apply all the simple techniques of linear network and control theory such as Bode plots and root locus construction to intelligently design feedback loops. In addition, it allows comparison of the dynamics of different resonant converters and choice of the most suitable one.

The goal of this chapter is to investigate some of the above issues. In particular, the goal is to design a feedback system based on the model developed in Chapter IV, and determine some of the limitations of the controller when microprocessors are used. A model operating at low frequency, specifically MIT's Parity Simulator [69], is used to study these limitations. Also, theoretical calculations of the delays caused by the controller will be made to determine the limitations on the speed of the controller.

We shall consider the application of the closed loop pole placement method in the design of a computer based control system for a series resonant converter. The purpose of the controller is to reduce the error in the converter output current by dynamic control of the switching frequency. This goal is accomplished by placing the closed loop poles of the transfer function from the switching frequency to the output current well inside the unit circle in the z-plane.

Section 2 of the chapter describes the control laws that we used, namely full state feedback and periodically varying output feedback. In Section 3 the problem of computer control and the effect of the computer delay on the dynamics of a feedback system are addressed. Section 4 describes two approaches used to implement the controller. One uses the Parity Simulator Generalized Controller [80], and the other uses a Compupro microcomputer. Section 5 discusses the control results.

InductEV, Inc.
Exhibit 1014
Page 156

(2) Calculation of Feedback Gains

In this section we present the design of a feedback system based on the state space model of a dynamic system. The technique we use is the pole assignment or pole placement technique. The design results in the assignment of the poles of a closed loop transfer function (zeros of the characteristic equation) to desired locations. This method will be applied to two control laws: state feedback and periodic output feedback.

Consider the discrete linear time invariant (DLTI) dynamical equation:

$$\mathbf{x}(k+1) = \mathbf{A}\mathbf{x}(k) + \mathbf{b}u(k) \tag{5.1a}$$

$$y(k) = \mathbf{c}\mathbf{x}(k) \tag{5.1b}$$

In this case we assume a single input, single output system with n state variables. Equation (5.1) is the same as the sampled-data equation developed in Chapter IV for the dynamics of the series resonant converter. To arbitrarily place the poles of the closed loop transfer function, we have to assume that the system is controllable (see definition of controllability in [70] or [75].

(A) State feedback gain calculation

Given the system in equation (5.1), under the state feedback operation corresponds to generating the control input u(k) by the relationship

$$u(k) = -\mathbf{F}\mathbf{x}(k) \tag{5.2a}$$

where

$$\mathbf{F} = [F_1 \quad F_2 \; .... \quad F_n] \tag{5.2b}$$

InductEV, Inc.
Exhibit 1014
Page 157

Then (5.1a) can be written as

$$\mathbf{x}(k + 1) = (\mathbf{A} - \mathbf{bF})\mathbf{x}(k) \tag{5.2c}$$

If we choose the desired closed loop poles locations at

$$z = z_1, z_2, \ldots\ldots\ldots\ldots, z_n \tag{5.3}$$

Then the system characteristic polynomial is

$$\begin{aligned} P_c(z) &= \det(z\mathbf{I} - \mathbf{A} + \mathbf{bF}) \\ &= (z - z_1)(z - z_2) \ldots\ldots(z - z_n) \end{aligned} \tag{5.4}$$

In this equation there are n unknowns F_1, F_2, ..., F_n, and n known coefficients in the right-hand side polynomial. We can solve for the unknown gains by equating coefficients in (5.4).

As an example, let us consider a second order system. The characteristic equation can be written as:

$$P_c(z) = \begin{bmatrix} z - a_{11} + b_1 F_1 & -a_{12} + b_1 F_2 \\ -a_{21} + b_2 F_1 & z - a_{22} + b_2 F_2 \end{bmatrix}$$

$$\begin{aligned} &= z^2 - q_1 z - q_2 \\ &= z^2 - (z_1 + z_2) z + z_1 z_2 \end{aligned}$$

where

$$q_1 = -(b_1 F_1 - a_{11}) - (b_2 F_2 - a_{22}) = z_1 + z_2 \tag{5.5a}$$

$$\begin{aligned} q_2 &= (b_1 F_2 - a_{12})(b_2 F_1 - a_{21}) - (b_1 F_1 - a_{11})(b_2 F_2 - a_{22}) \\ &= - z_1 z_2 \end{aligned} \tag{5.5b}$$

Equation (5.5) can be used to solve for F_1 and F_2. The procedure of matching coefficients becomes difficult for a system higher than a

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Exhibit 1014
Page 158

second order system. A procedure that greatly simplify the calculation of the gain matrix **F** is given in in [70] and [75].

(B) Periodic output feedback

Output feedback with time varying gain and the associated problems of stabilization and arbitrary closed loop pole assignment have received some attention in the literature, see [71], [73] and references therein. Such a feedback system is in principle more flexible than output feedback with a constant gain. The stability and eigenvalue assignment have been investigated for a linear, time invariant, second order discrete system with periodic feedback. It has been shown that with two-periodic output feedback gain, the system can have both the closed loop poles at the origin, and with three-periodic output feedback the poles can be placed anywhere inside the unit circle [71]. It is not known whether such results can be achieved practically. In this section we will consider the theory behind periodic output feedback and present some experimental results in Section 5.

Let us consider the discrete system of equation (5.1). When N-periodic output feedback of the form

$$u(k) = F(k)\, y(k), \quad F(k) = F(k+N), \text{ and } F(k) \text{ is real,} \tag{5.6}$$

is introduced, the closed-loop system is described by

$$\mathbf{x}(k+1) = (\mathbf{A} + \mathbf{b}\, F(k)\mathbf{c})\, \mathbf{x}(k) = \mathbf{A}(k)\, \mathbf{x}(k) \tag{5.7a}$$

$$y(k) = \mathbf{c}\, \mathbf{x}(k) \tag{5.7b}$$

The system described by equations (5.7) is a linear periodic discrete system because

InductEV, Inc.
Exhibit 1014
Page 159

$$\mathbf{A}(k) = \mathbf{A}(k+N) \tag{5.8}$$

The system dynamics is determined by the eigenvalues of the state transition matrix $\mathbf{A}_c$, over one period, given by

$$\mathbf{A}_c = \mathbf{A}(N-1+k)\ \mathbf{A}(N-2+k)\ \ldots\ \mathbf{A}(k) \tag{5.9}$$

$$= (\mathbf{A} + \mathbf{b}F(N-1+k)\mathbf{c})(\mathbf{A} + \mathbf{b}F(N-2+k)\mathbf{c})\ldots.(\mathbf{A} + \mathbf{b}F(k)\mathbf{c}) \tag{5.10}$$

If we choose the closed-loop poles locations at

$$z = z_1,\ z_2,\ \ldots\ldots\ldots,\ z_n,$$

then the system characteristic polynomial becomes

$$P_c(z) = (z - z_1)(z - z_2)\ \ldots.\ (z - z_n) = \det(zI - \mathbf{A}_c) \tag{5.11}$$

It has been shown that for arbitrary assignment of the eigenvalues, the period N must be greater than or equal to the number of state variables n [71]. For N equal to n, the gains can be solved for by equating the coefficients in equation (5.11). For N > n, we can choose (N - n) gains arbitrarily, and the remaining n gains can be found by matching the coefficients in equation (5.11).

As stated earlier, most of the existing analysis of periodic output feedback has concentrated on the analysis of second order systems. It has been that shown with two gains, a dead beat (both of the closed loop poles at the origin) can be achieved. With three gains the poles can be arbitrarily chosen inside the unit circle. Our results have shown that for a third order system, with a period equal to 3, the poles cannot be arbitrarily chosen inside the unit circle. Moreover, the gains values are very sensitive to changes in the specified closed loop poles.

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Exhibit 1014
Page 160

(3) Effects of the Computer Delay

The application of the feedback control laws discussed in Section 2, in a computer-based system would require an on line computation of the input in equations (5.2a) and (5.6). The difficulty with such a design is that there is a restriction imposed by the finite computational delay inherent in any computer-based control system, so that it may be impossible to have u(k) depend on $\mathbf{x}(k)$ or y(k). To model this computational delay, define a delayed input v(k) as

$$v(k) = u(k+1) \tag{5.12}$$

The original plant dynamics in equation (5.1) is then augmented to include the computational delay, and the new system becomes

$$\begin{bmatrix} \mathbf{x}(k) \\ \\ u(k+1) \end{bmatrix} = \begin{bmatrix} \mathbf{A} & \mathbf{b} \\ \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \mathbf{x}(k) \\ \\ u(k) \end{bmatrix} + \begin{bmatrix} \mathbf{0} \\ \\ 1 \end{bmatrix} v(k) \tag{5.13}$$

which has (n+1) states. The state feedback control law then becomes

$$v(k) = \mathbf{F}\,\mathbf{x}(k) + F_{n+1}\,u(k) \tag{5.14a}$$

$$u(k) = \mathbf{F}\,\mathbf{x}(k-1) + F_{n+1}\,u(k-1) \tag{5.14b}$$

where $\mathbf{F}$ is as defined in equation (5.2a). The pole placement method discussed earlier can now be used to determine the gains.

In cases where the calculation time is small compared to the sampling period, the computer delay can be ignored. Some experimental results demonstrating the effect of including or ignoring the computer delay will be presented in Section 5.

InductEV, Inc.
Exhibit 1014
Page 161

(4) Control Implementation

A computer-based control system has been used to control a Parity Simulator model of the series resonant converter shown in Fig. 5-1.

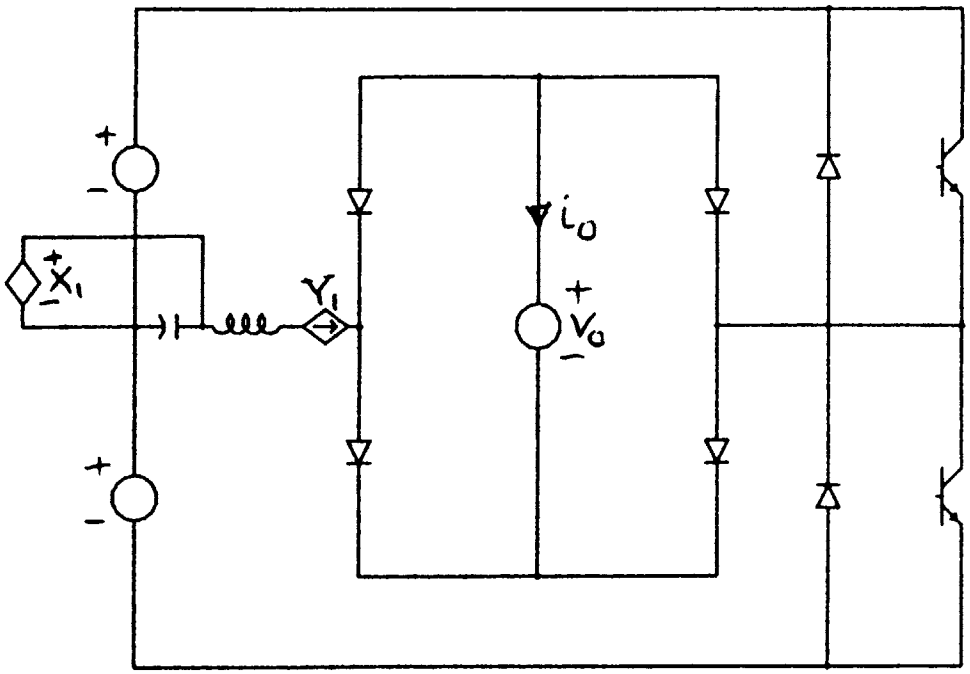

Fig. 5-1 The series resonant dc-dc converter

The parameter values for the series resonant converter are:

$L = 197$ uH $\qquad C = 100$ nF

$V_{in} = 14$ V $\qquad V_o = 5.0$ V

$f_s = 40$ kHz

and the simulator scale factors are:

vsc = voltage scale factor = 0.1

isc = current scale factor = 0.002

fsc = frequency scale factor = 2.5e-4

The simulator model is slowed down by the factor fsc. The objective here is to test the control algorithm; speeding up the hardware is left for a later development.

InductEV, Inc.
Exhibit 1014
Page 162

The state variables are the inductor current $i_L(t)$ and the capacitor voltage $v_C(t)$. The output is the rectified inductor current i_o. The input is the drive frequency f_s which controls the transistors N_1 and N_2. The waveforms of the state variables for one switching period are shown in Fig. 5-2. The goal is to control the output current i_o by changing the switching frequency f_s. Recall that the linear sampled-data model we obtained in Chapter IV describes small perturbations away from the steady state operation. The controller therefore samples the output or the state variables once every cycle, and compares the sampled values with the steady state values. The error is fed back through a gain and added to the reference switching frequency. The open loop **A** and **b** matrices of the dynamics of the converter, due to small changes in the switching frequency, are:

$$\mathbf{A} = \begin{bmatrix} 0.635 & 0.0124 \\ -16.72 & 0.563 \end{bmatrix} \qquad \mathbf{b} = \begin{bmatrix} -2.42e-5 \\ 0.004 \end{bmatrix} \tag{5.15}$$

If we are to use the model developed in Chapter IV, the sampling instant in the waveforms of Fig-5-2 is corresponding to the start of conduction of the diode D_1. Controlling the state variables at these points implies the control of any other point in the cycle, because the other points in the cycle are related to the sampled points by the auxiliary variables equations defined in Chapter IV. For example, the average or the peak of the waveforms can be considered as auxiliary outputs that are function of the state variables. The small signal transfer functions the switching frequency to such auxiliary outputs have the same poles but different zeros.

InductEV, Inc.
Exhibit 1014
Page 163

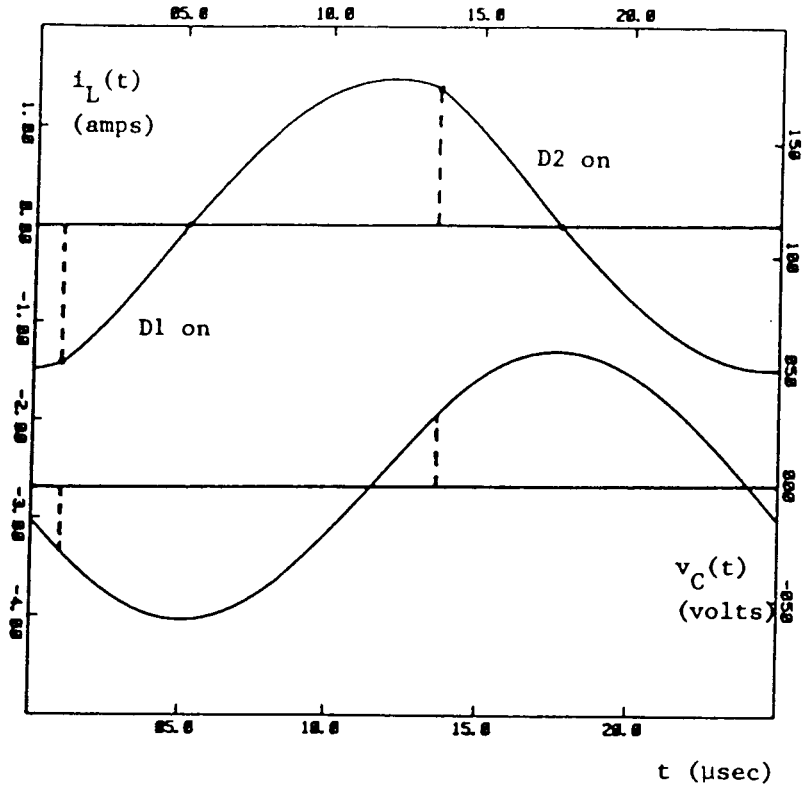

Fig. 5-2 Waveforms of the state variables of the series resonant converter in Fig. 5-1

The controller has been implemented in two ways: On the Parity Simulator Generalized Controller [80] and on a Compupro microcomputer. In the following subsections we shall discuss each implementation and in Section 5 we shall present some of the corresponding results.

(A) <u>The parity simulator generalized controller</u>

A generalized controller has been constructed for use with the Parity Simulator. The purpose of the controller is to allow the user of the Parity Simulator to design the control-system portion of a circuit under evaluation by way of digital simulation rather than by other means, such as breadboarding a hardware controller. Implementations of basic control blocks such as integrators, differentiators, gains and

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Exhibit 1014
Page 164

summers have been included. Twenty one functions are available to the user. These functions, together with the time to execute each of them on the the present IBM PC-XT implementation, are given in Table 5-2. They can be combined to implement a variety of control strategies.

Control Function	Execution Time (μsec)
Analog Input	86
Analog Output	75
Angle-to-voltage Converter	30
Digital Input	7
Digital Output	5
Comparator w/ hysterisis	45
Dead Band	30
Differentiator	82
Divider	24
Gain	25
High-pass Filter (single-pole)	82
Integrator	100
Limiter	40
Logic-controlled Switch	10
Look-up & Interpolate	
Low-pass Filter (single-pole)	80
Multiplier	24
Summing Junction (1 input)	30
Summing Junction (2 inputs)	40
Summing Junction (3 inputs)	50
Time Delay	40
Voltage Reference	no run-time penalty

Table 5-2 Generalized controller functions

The hardware of the controller consists of an IBM microcomputer attached to the simulator via a panel interface card cage. A compiler has been written for the controller. This computer program generates an assembly language source file containing the necessary instructions for the microcomputer to perform the control simulation specified by the user.

InductEV, Inc.
Exhibit 1014
Page 165

Signals from the Parity Simulator are connected to the controller input terminals. These signals are processed by the control computer during each sampling period of the controller. The control-block functions performed by the controller are specified by the user. The control signals generated at the controller output are connected to functions on the simulator panel such as pulse-width modulated (PWM) gate drives and frequency generators. The controller has the capability of sampling and generating up to 8 analog signals and 8 digital signals. The generalized controller has been used to implement both state and output feedbacks to control the series resonant converter.

(i) State feedback

A block diagram showing the connections of the Parity Simulator and its generalized controller for the control of the series resonant dc-dc converter are shown in Fig. 5-3. The inductor current i_L and the capacitor voltage v_C are available to the controller through the sensors Y_1 and X_1 respectively. The signals are connected to two analog inputs of the Generalized Controller. Each analog input has a scaling factor associated with it. These gains are chosen to be the inverse of the current and voltage scale factors (isc and vsc) in the Simulator. Therefore the outputs of controller analog inputs correspond to the actual circuit currents and voltages.

The signals are then sampled synchronously with the turn-off of N_2, when D_1 starts to conduct. The sampled signals are connected to summing junctions where the steady-state operating operating values ILR and VCR are subtracted. The outputs of the summing junctions correspond to the sampled errors in the inductor current $i_{Le}(k)$ and the capacitor voltage $v_{Ce}(k)$. These errors are multiplied by their respective gains k_i and

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Exhibit 1014
Page 166

k_v, calculated from the state feedback control design. They are then summed with the correction error in the input switching frequency $f_{se}(k)$ times a gain k_f, see (5.14). The output of the summing becomes the correction in the input frequency $f_{se}(k+1)$ at the next cycle, which is the reason for including the delay element in Fig. 5-3. In this case we are using a third order model, namely the second order system of the series converter augmented by the computer delay.

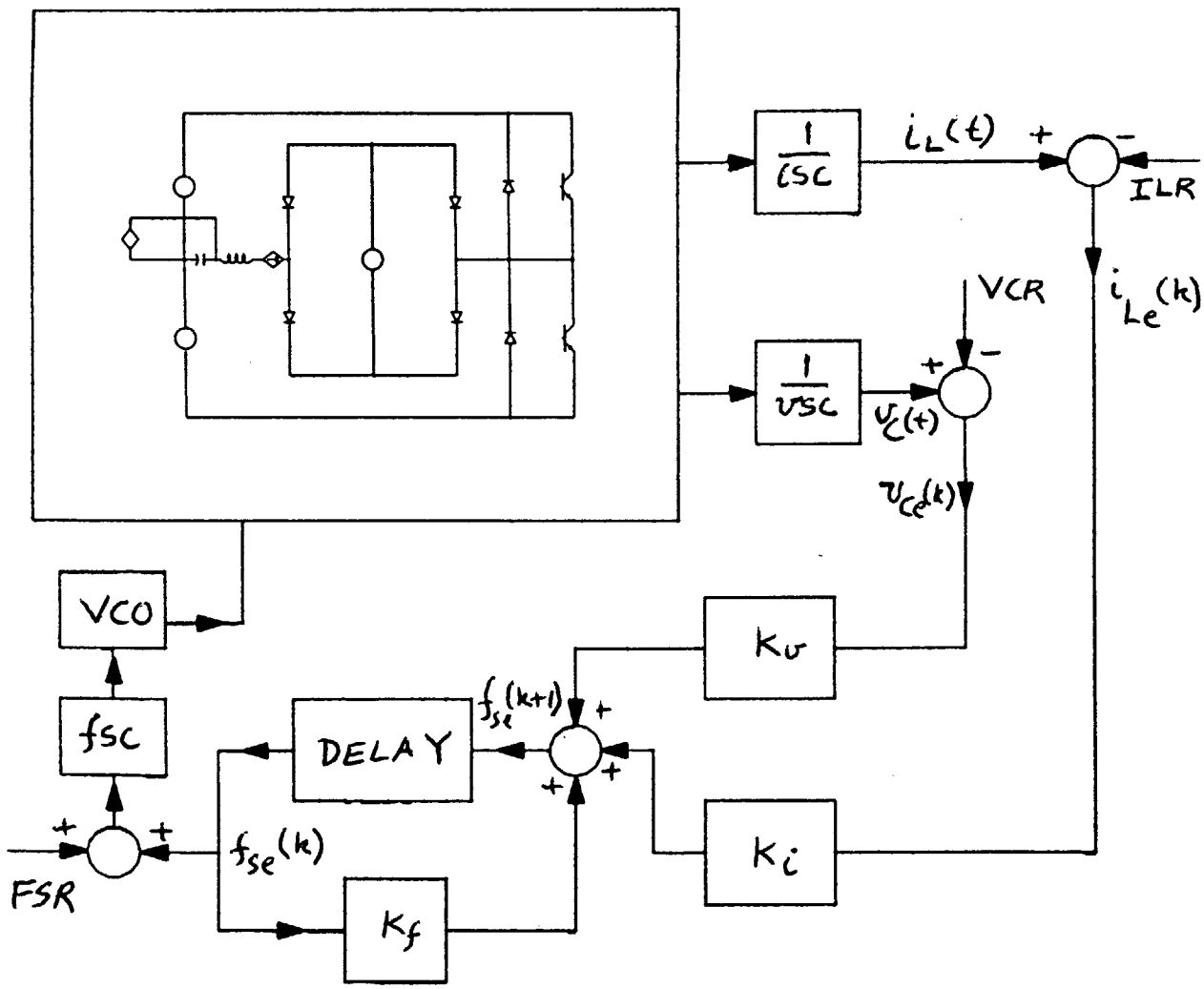

Fig. 5-3 A block diagram of the closed-loop control of the series resonant converter using the generalized controller

InductEV, Inc.
Exhibit 1014
Page 167

The control correction signal $f_{se}(k)$ is added at another summing junction to the reference switching frequency FSR. The output of the summing junction is a voltage proportional to the switching frequency. It is multiplied by a gain that equals the ratio of the frequency scale factor (fsc) to the voltage scale factor (vsc) of the Parity Simulator. This is then fed into the input of a VCO built in the simulator to give the required switching frequency.

If the computer delay is small comapred to the sampling period, one can ignore it and the block diagram of Fig. 5-3 can be redrawn as in Fig. 5-4. This implementation corresponds to a state feedback for a second order system.

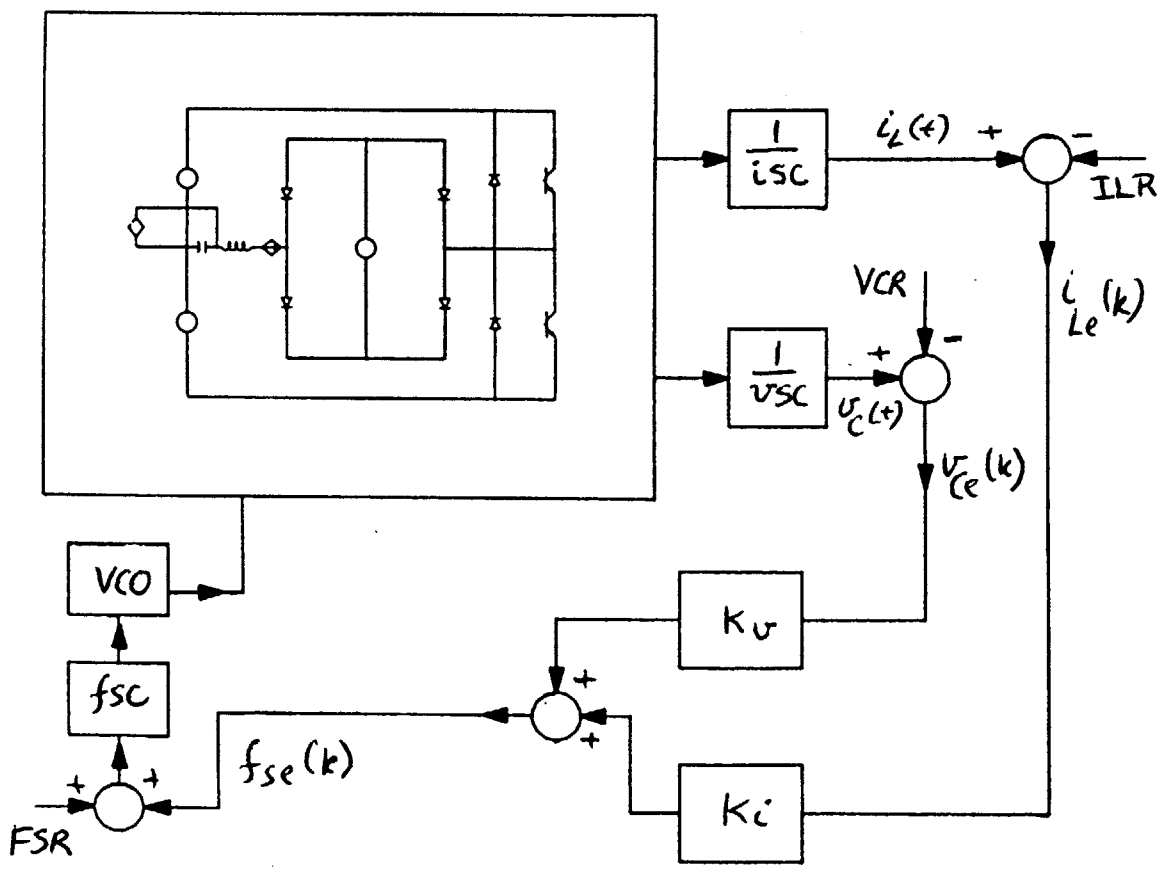

Fig. 5-4 State feedback implementation without a delay block using the generalized controller

InductEV, Inc.
Exhibit 1014
Page 168

(ii) Periodic output feedback

Fig. 5-5 shows the implementation of the periodic output feedback using the Generalized Controller. This block diagram differs from Figs. 5-3 and 5-4 in that only the inductor current is fed back. This is because the output current i_o that we want to control is equal to the rectified inductor current. The error in the inductor current is multiplied by a variable gain K(k). The switching from one gain to another is implemented by a software counter function whose cycle is equal to the period of the feedback (which we have picked to be 2 for a system without the computer delay and 3 for a system with the computer delay).

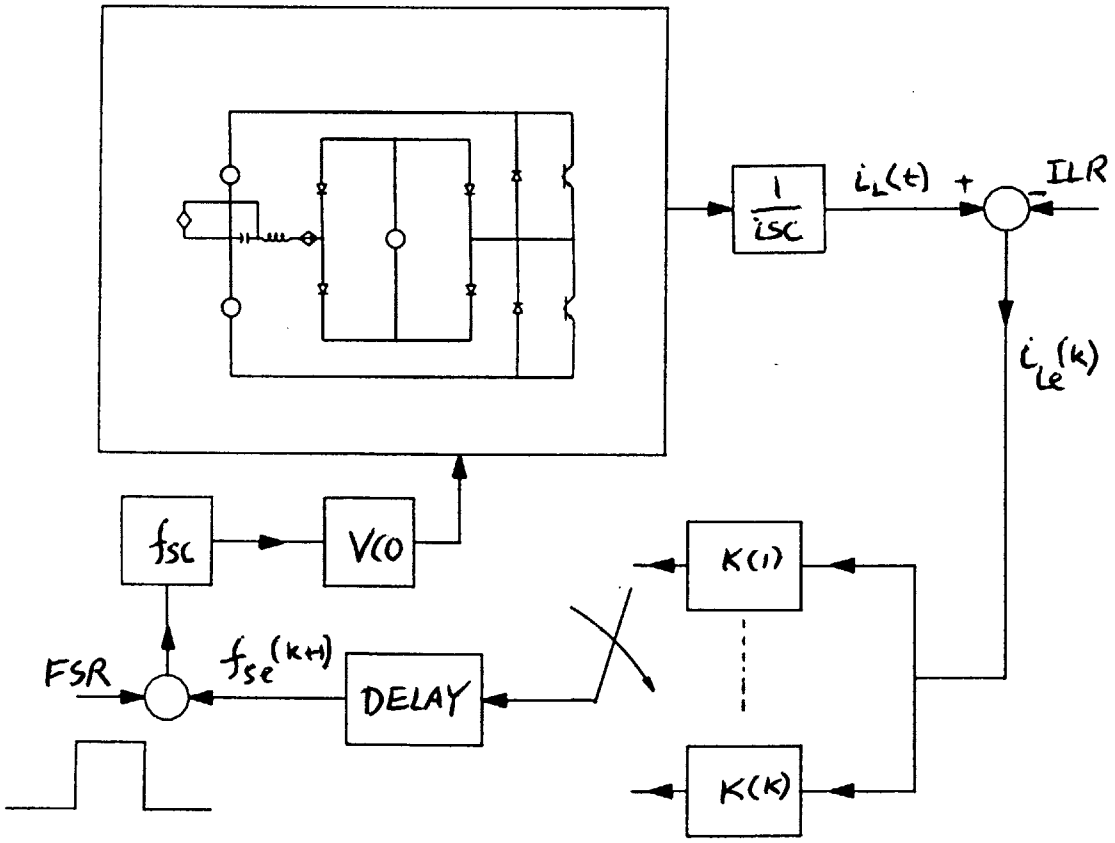

Fig. 5-5 Generalized controller implementation of the periodic output feedback

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Exhibit 1014
Page 169

(B) <u>The compupro microcomputer</u>

The two control laws have also been implemented using a Compupro microcomputer. This implementation is the same as the generalized controller, except that its software is written using the C language, and the circuit that interfaces the computer with the Parity Simulator is built externally, whereas in the Generalized Controller the software is written in assembly language and the interface circuit is built into the computer. Fig. 5-6 shows a block diagram of the Compupro implementation of the state feedback.

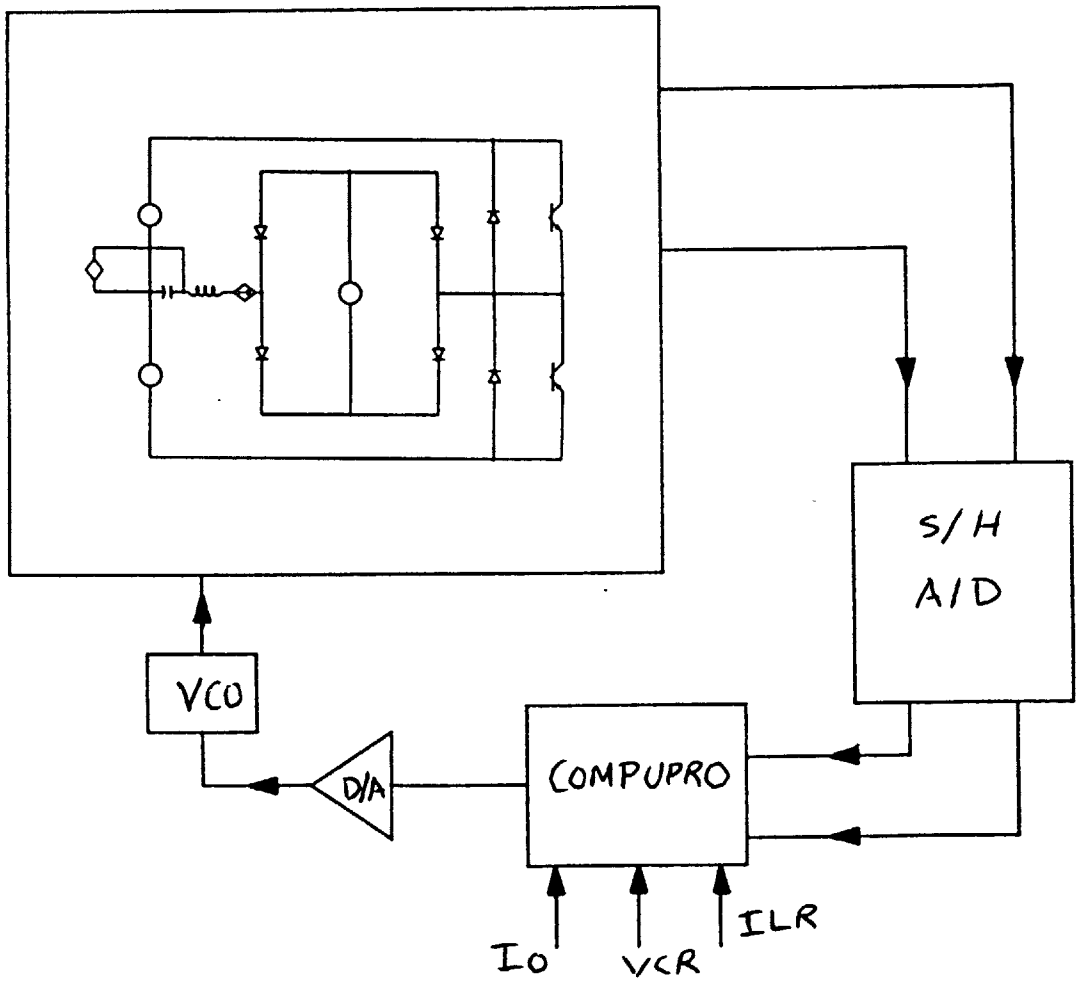

Fig. 5-6 A block diagram of the state feedback control using the Compupro microcomputer

InductEV, Inc.
Exhibit 1014
Page 170

The state variables are sampled and fed into an analog-to-digital circuit (A/D). The data output of the A/D is entered into the Compupro microcomputer, using three input/output (I/O) ports which are also used to control the interface circuit. The software performs the following functions :

(i) It subtracts the sampled state variables from their corresponding steady state values.

(ii) It multiplies the errors in the state variables by their corresponding gains, and adds them to obtain the control correction to the switching frequency.

(iii) It adds the frequency correction calculated above to the reference switching frequency, and loads the result through the I/O ports to the input of the digital-to-analog converter (D/A) which gives an output voltage proportional to the commanded switching frequency.

The circuits showing the connections of the A/D and the D/A interfaces are shown in Figs. 5-7 and 5-8 respectively. The computer I/O ports are labelled 128, 129, and 130. Signals to the input of the A/D are obtained from the output of the analog multiplexer AD7501 whose inputs are selected by a 3 bit control signal from the microcomputer. The synch pulse is used to synchronize the Compupro and the Parity Simulator. This pulse occurs at the sampling instant when the diode D_1 of Fig. 5-2 starts conducting. The comparator LM311 is used to generate a step change in the reference switching frequency.

The implementation of the periodic output feedback control, using the Compupro, is the same as explained in the case of periodic output feedback using the generalized controller.

InductEV, Inc.
Exhibit 1014
Page 171

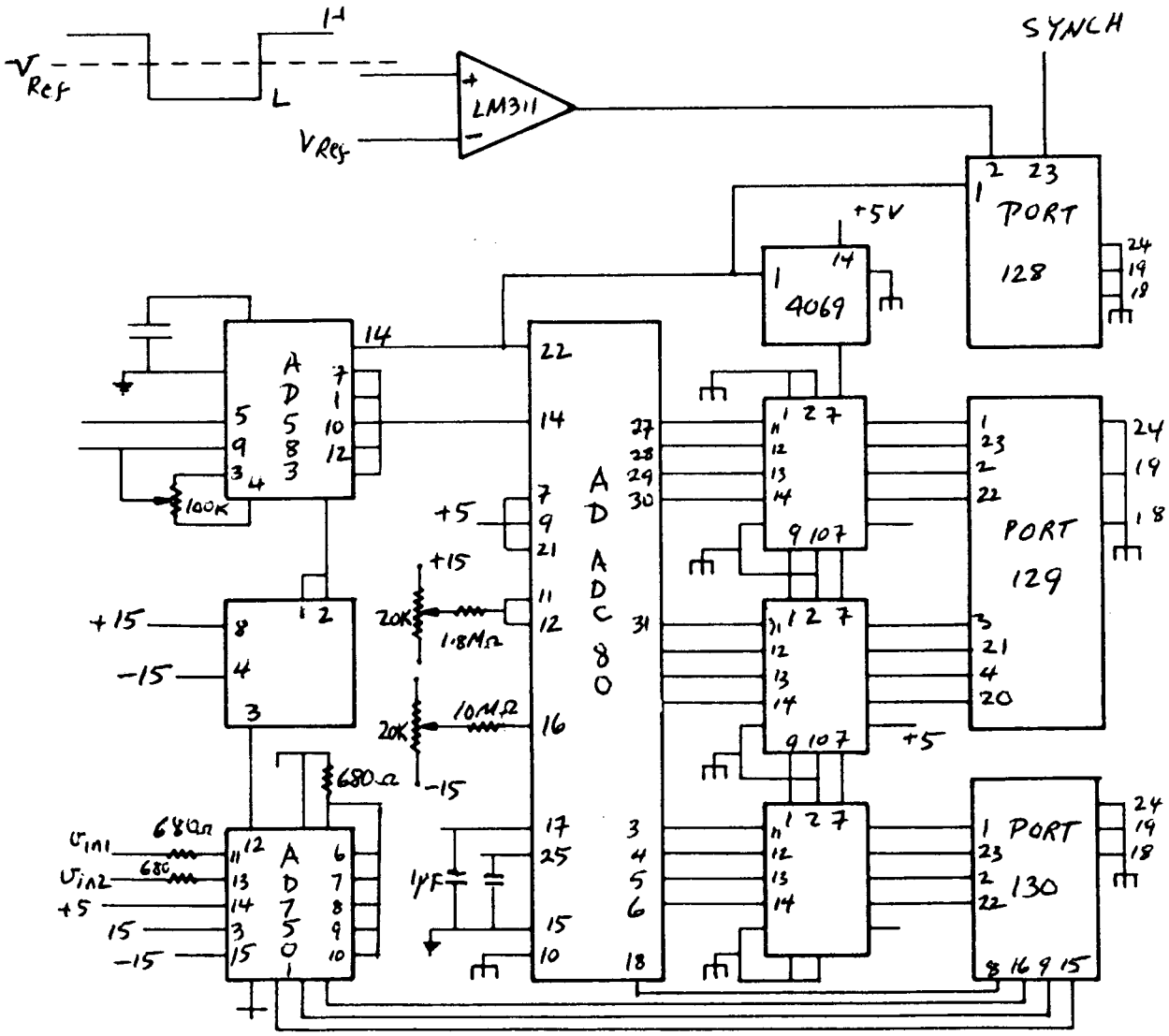

Fig. 5-7 The A/D connections

InductEV, Inc.
Exhibit 1014
Page 172

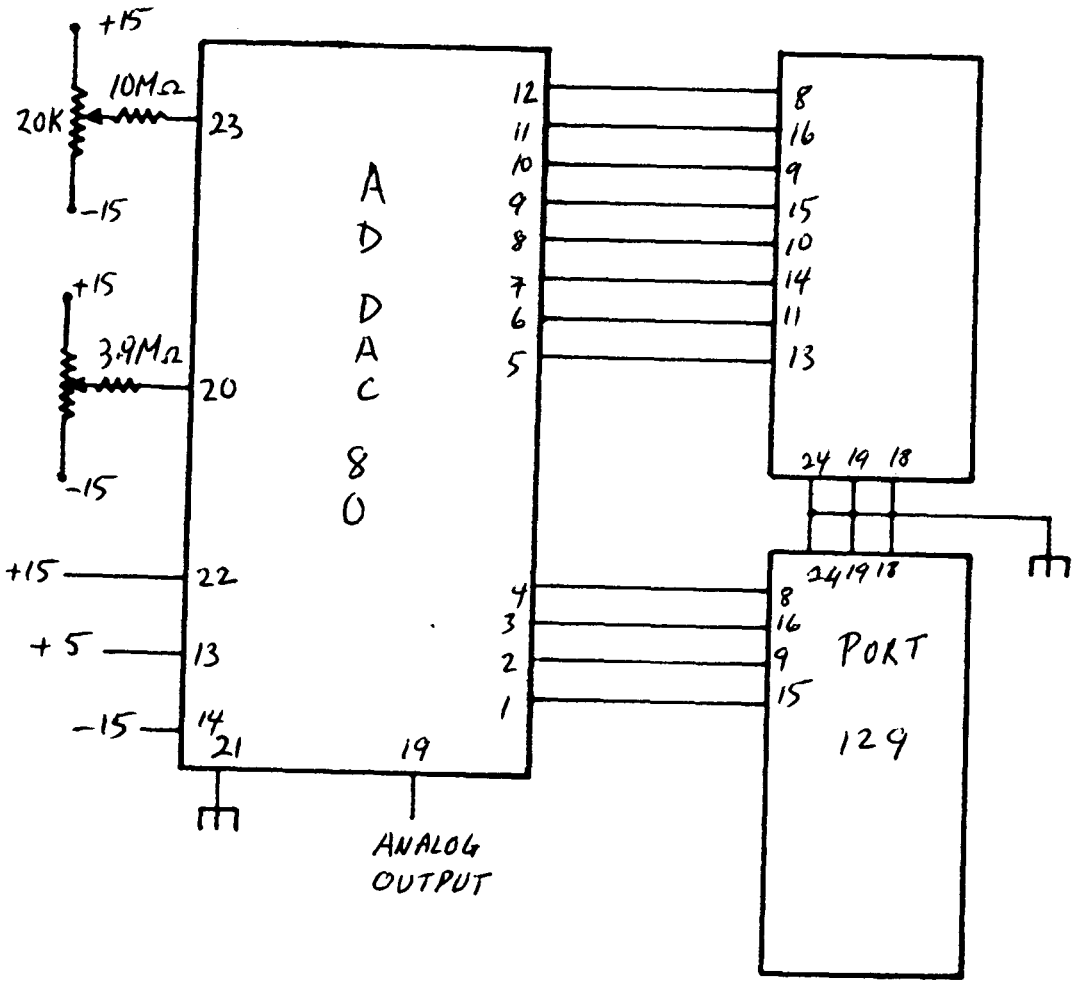

Fig. 5-8 The D/A connections

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Exhibit 1014
Page 173

(5) Results and Discussions

In this section, experimental results obtained from the above described implementations are described. We shall first present the results obtained for state feedback control using the generalized controller and the Compupro. Secondly we shall present the results of the periodic output feedback.

(A) State feedback

(i) Using the parity simulator generalized controller

For the series converter circuit, with the parameters specified earlier, the implementation of the state feedback has been done with and without the computer delay.

Fig. 5-9a shows the open loop response of the output current to a 5% step changes in the reference switching frequency, and in Fig. 5-9b the same step response is shown when the input is fed from the controller rather than from the simulator. The open loop output current response with the input frequency fed from the controller has some irregularities. This could be related either to quantitization error or some noise in the controller. The upward transition of the response is different from the downward transition, because the response depends on the operating point of the converter. The downward transition correspond to the 40 kHz switching frequency.

The closed loop is first implemented with a control delay of one sampling cycle, but with state feedback designed assuming no delay, i.e using the second order model. The system is designed to have closed loop poles at $z = 0.2 \pm j0.2$. The gains required are $k_i = 1169.3$ and $k_v = -192.4$. The response to 5% step changes in the switching frequency is shown in Fig. 5-10a. The response is close to unstable at a

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Exhibit 1014
Page 174

frequency equal to one-fifth the switching frequency. This is a very interesting result that demonstrates the importance of the modeling computer delay.

To ensure that the instability is due to ignoring the effect of the computer delay, the two gains above with a third gain k_f of zero are used in the augmented third order model (5.13), (5.14) that takes computer delay into account. The closed loop eigenvalues of the system are found to be at: $z = 0.316 \pm j0.943$ and $z = 0.476$. The complex conjugate pair lies virtually on the unit circle, and at an angle of almost exactly $\pm 2\pi/5$, which correlate excellently with the observed behavior. A numerically simulated discrete time step response for the third order model, obtained using the MATRIX X program, is shown in Fig. 5-10b. The frequency of oscillation is equal to five samples, which also agrees with what is found experimentally.

The experiment is now repeated with a state feedback designed using the more accurate third order model that includes the effect of the computer delay. The gains are calculated to yield closed loop poles at $z = 0.2$ and $z = 0.2 \pm j0.2$. Fig. 5-11 shows the response of the output current to 5% change in the reference switching frequency. The response is now very stable compared to what is seen Fig. 5-9a. This result again demonstrates the importance of modeling the computer delay. When we ignore the computer delay, we obtain a response worse than the open loop response, and when we take the computer delay into account, we obtain a closed loop response that is much better than the open loop response.

A numerical simulation of the step response using MATRIX X is again used to quantitatively the experimental results, see Fig. 511b. There

InductEV, Inc.
Exhibit 1014
Page 175

is one difference between the two results: the MATRIX X simulations track the point at which a diode turns ON (the point that is described by the model and sampled by the controller), and the ones obtained on the simulator give the response of the peak of the output current. The two transfer functions to the two responses have the same poles, but different zeros. This means that the diode turn-on point has the same general dynamic behavior as the peak of the output current waveform, but for example the initial kick in the response in Fig. 3-11b is opposite to that of the response in the peak (corresponding to the fact that the transfer function governing the former response has a zero to the right of $z = 1$ while the other one does not).

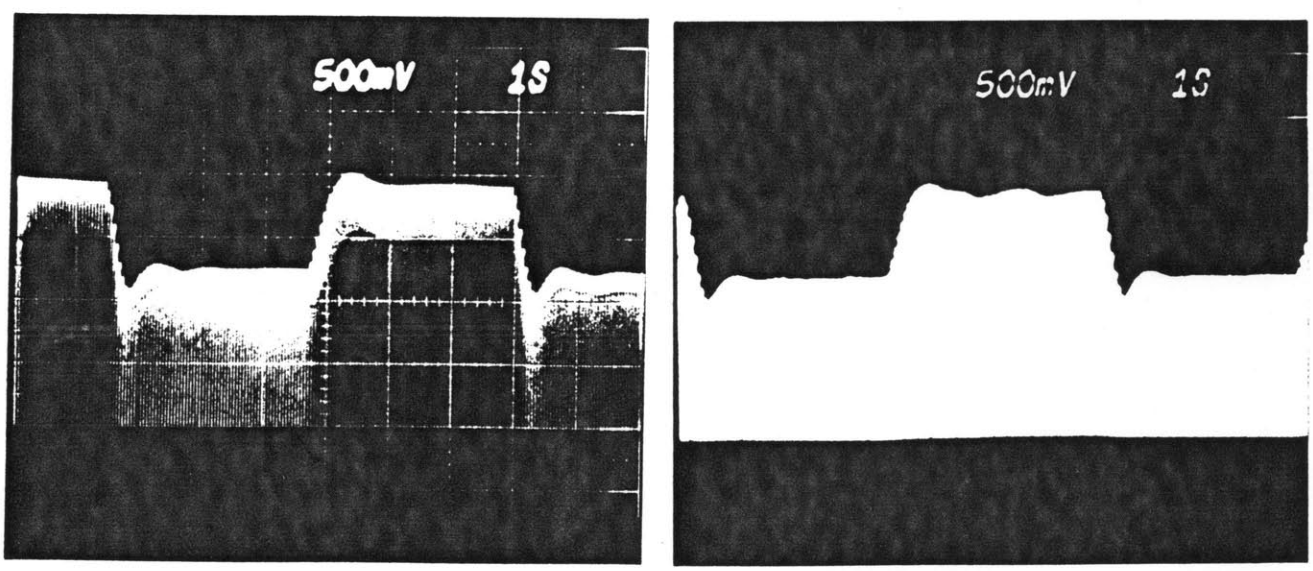
Responses for other closed loop locations are shown in Figs. 5-12. The response in Fig. 5-12a are for closed loop locations at $z = 0.2$, $z = 0.3 \pm j0.3$, and the response in Fig. 5-12b the three closed loop are all at $z = 0.1$

Now the experiment is repeated with the cycle delay in the control removed from the implementation, so that the second order model now is applicable. The difference between this experiment and the previous ones is illustrated by Fig. 5-13. In Fig. 5-13a, which corresponds to the earlier experiments, the control instant (i.e the instant to turn off a transistor) is determined from the computation made in the previous cycle. In Fig. 5-13b, which correspond to this experiment, the control instant is determined from computations made on the same cycle. The closed loop poles are placed at $z = 0.2 \pm j\ 0.2$. The response corresponding to 5% step changes in the switching frequency is shown in Fig. 5-14. It is a stable response, but the steady state value of the output current is different from that of Fig. 5-9a, though the step

InductEV, Inc.
Exhibit 1014
Page 176

change is the same in both cases. The reason is that the computer calculation time is subtract from the switching period obtained by the feedback calculations, and since the switching period (or frequency) controls the output current, a change in its value will affect the value of the output current.

One observation to be seen in the response of Fig. 5-14 is that the steady state value for the step change i_o is different from that of Fig. 5-9a. This due to the fact that the instant at which a transistor is turned off is advanced by an amount equals to the computational time. This affects the final value of switching frequency which affects the steady state value of the output current.



(a) f_s obtained from the Simulator

(b) f_s obtained from the generalized controller

Fig. 5-9 Open-loop response of the output current to a 5% step change in f_s

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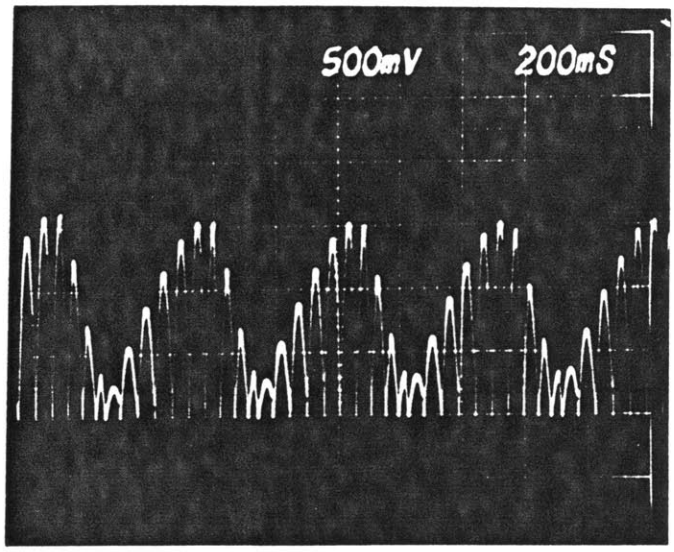
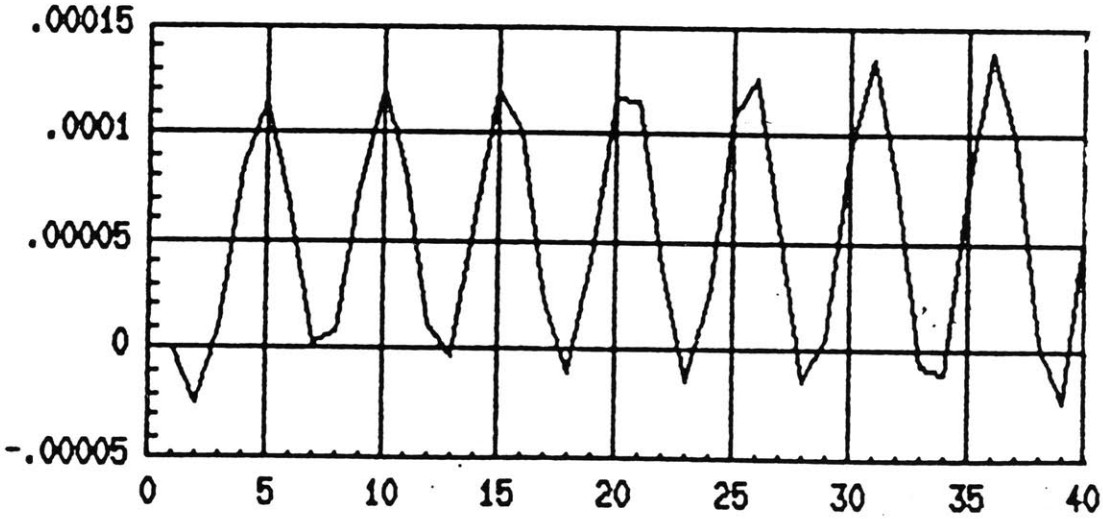
Exhibit 1014
Page 177



(a) f_s fed from the generalized controller



(b) MATRIX X simulation

poles at $0.2 \pm j0.2$

Fig. 5-10 Closed loop response of the output current using a second-order model and including a delay of one cycle

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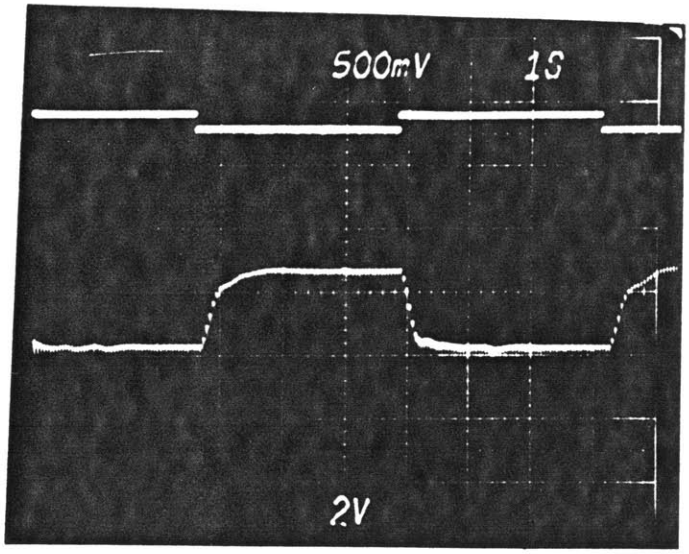
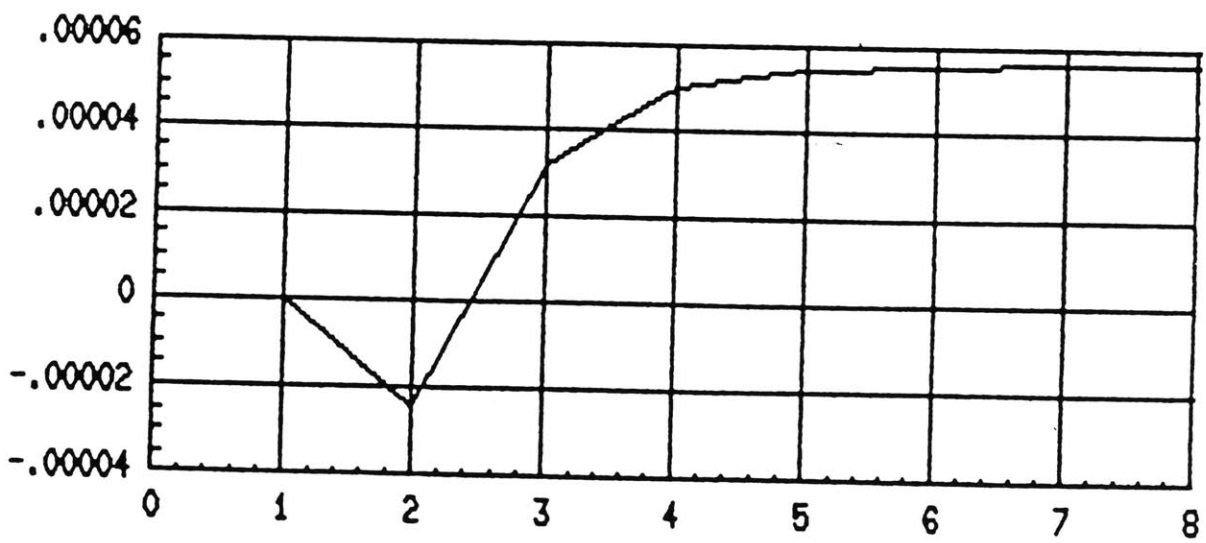
Exhibit 1014
Page 178



Upper trace: switching frequency (fsc = 2.5×10^{-4}, VCO scale is 10Hz/V)
Lower trace: output current i_o

(a) f_s fed from the generalized controller

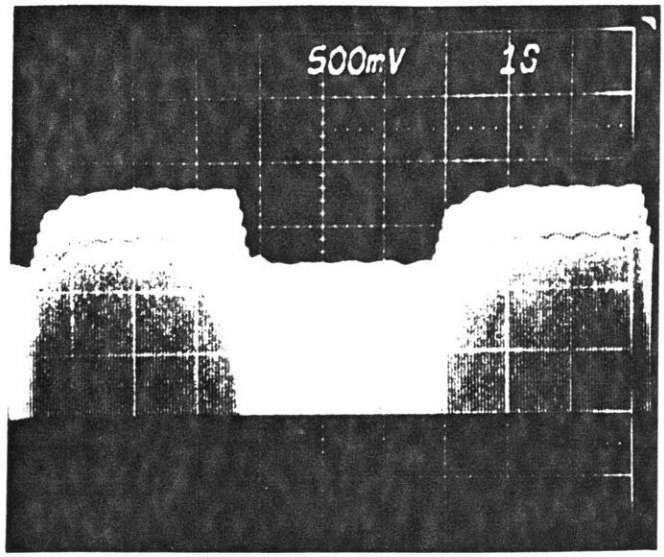


(b) MATRIX X simulation

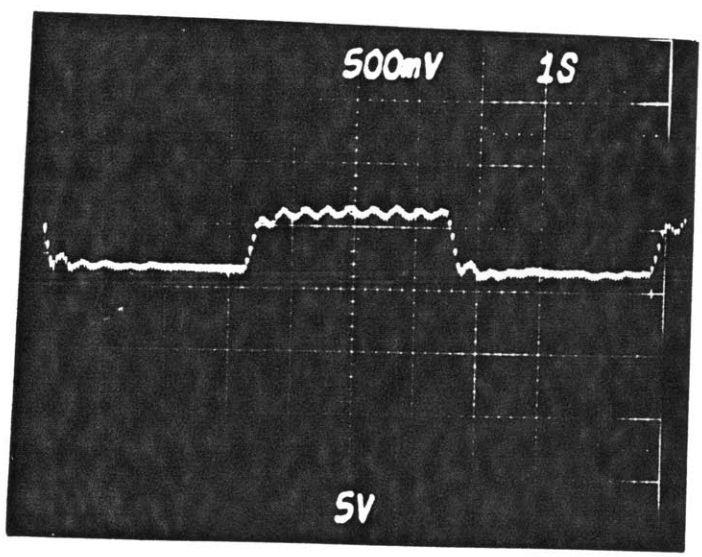
closed-loop poles at: z = 0.2, z = 0.2 $\pm$j 0.2

Fig. 5-11 Closed-loop response of the output current using the generalized controller with a third-order model

InductEV, Inc.
Exhibit 1014
Page 179



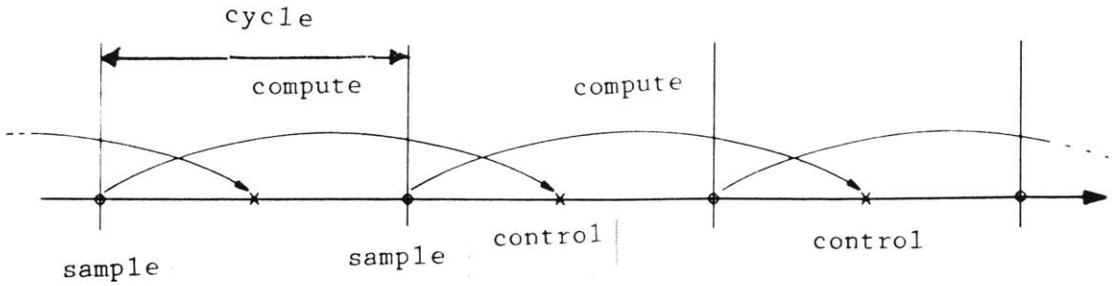
(a) closed-loop poles at: z = 0.2, z = 0.3 $\pm$j 0.3



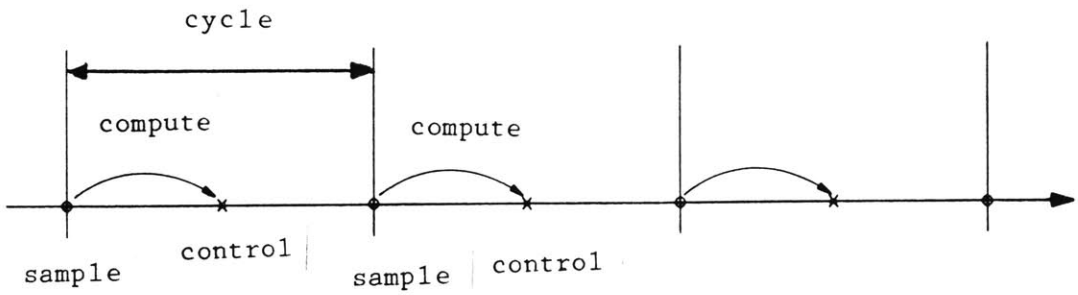
(b) closed-loop poles at: z = 0.1, 0.1, 0.1

Fig. 5-12 Closed-loop response of the output current using the generalized controller with a third order-model

InductEV, Inc.
Exhibit 1014
Page 180

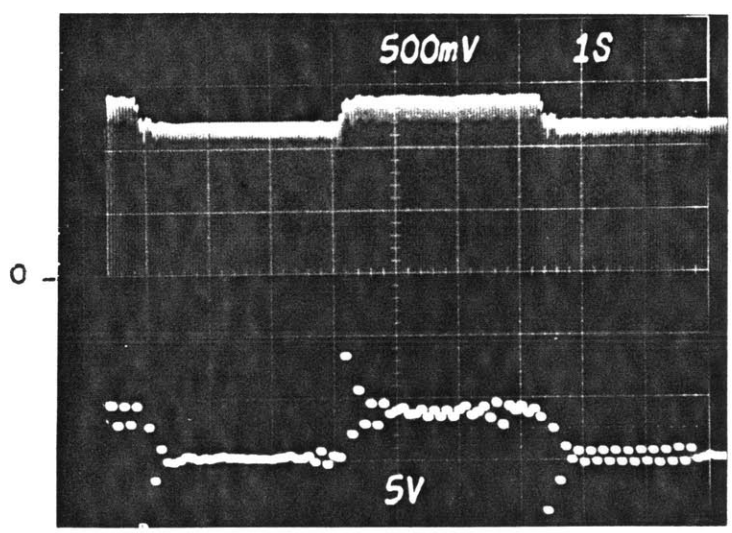


(a) Including the computational delay



(b) Neglecting the computational delay

Fig. 5-13 Sampling and control instants



Upper trace: output current i_o
Lower trace: switching frequency

poles at $z = 0.2 \pm j0.2$

Fig. 5-14 Closed-loop response of the output current using a second-order model without a cycle delay

InductEV, Inc.
Exhibit 1014
Page 181

(ii) Using the Compupro microcomputer

The implementation of the state feedback using the Compupro microcomputer differs from the one using the generalized controller in that the Compupro software is written in the C language, and the generalized controller software is written in assembly language. This makes the calculations faster in the Generalized Controller than in the Compupro microcomputer. Also, the circuit that interfaces the controller with the Simulator is built into the Generalized Controller computer, whereas it is externally built for the Compupro microcomputer. The simulation has therefore been slowed down by a factor of 2 in the case of the Compupro microcomputer. The circuit parameters are changed so that the switching frequency and the resonant frequency of the circuit controlled by the Compupro are half those of the circuit controlled by the Generalized Controller.

Fig. 5-15 shows the open-loop response of the output current to a 5% step change in the switching frequency. In Fig. 5-15a the control signal is taken from the Parity Simulator, while in Fig. 5-15b the control signal is fed from the Compupro computer with the feedback gains being set to zero. The two responses are similar.

Fig. 5-16a shows the closed-loop response with the one-cycle computer delay taken account of. The closed-loop poles are chosen at z = 0.0, 0.1 and 0.5. The response is faster, and with no overshoot, compared to the responses in Fig. 5-15. The response also matches that of Fig. 5-16b, which has been obtained numerical simulation using MATRIX X Also, the kick in the opposite direction to the steady state is present in both responses. This is due to a zero to the right of +1 in the closed-loop transfer function from the switching frequency to the

InductEV, Inc.
Exhibit 1014
Page 182

output current. The zero of that transfer function is in fact found to be at z = 2.3.

(B) Periodic output feedback

Periodic output feedback has been implemented using the third-order model that accounts for the computer delay. The gains are found by substituting the closed-loop poles in (5.11) and matching the coefficients on the two sides of the equation. It turns out that one cannot place the poles arbitrarily inside the unit circle, for a third-order system. Moreover, the gains are very sensitive to small changes in the specified closed loop poles. One might find a set of gains for a certain set of closed-loop poles, but no gains when one of the poles is changed by a small value.

The responses obtained through periodic output feedback are not nearly as good as those obtained using state feedback. The practical problems of implementing the periodic output feedback, and the resulting performance, need further study.

Fig. 5-17 shows the open-loop and closed-loop responses of the system under periodic output feedback using the generalized controller. The closed loop poles are chosen to be at z = 0.0, 0.1 and 0.1. The response of the closed loop is more damped than that of the open loop, but is much slower than the open loop response. The oscillations in the envelope of the closed-loop response are due to problems with the generalized controller, because they are present also in the open-loop response when the control signal is fed from the Generalized Controller.

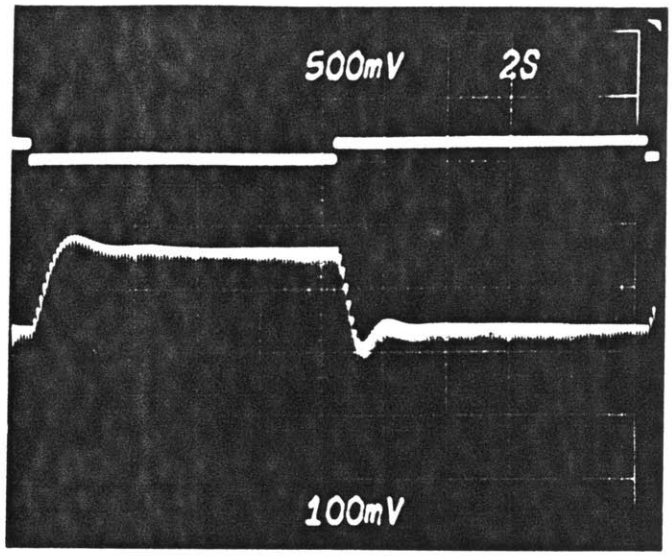
Fig. 5-18 shows the open-loop and the closed loop responses when the periodic output feedback is implemented using the Compupro microcomputer. The gains are calculated for closed loop poles at z = 0,

InductEV, Inc.
Exhibit 1014
Page 183

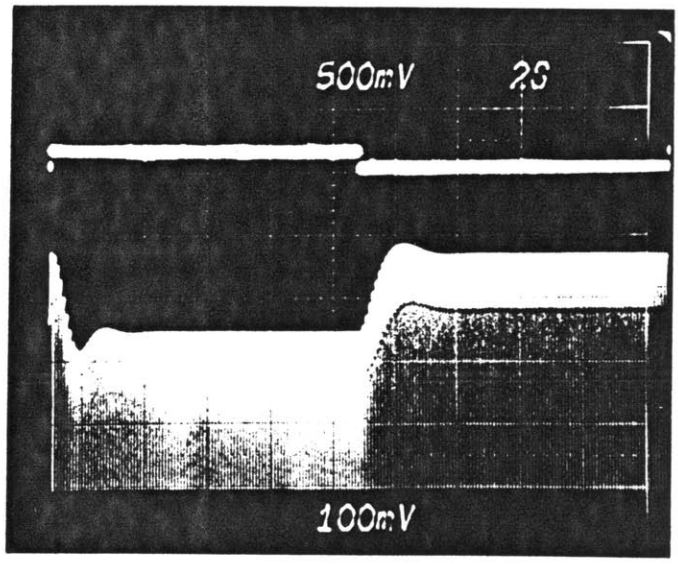
-0.1 and -0.1. In this case, the open-loop response is better than than the closed-loop response. As mentioned earlier, the reason may be the sensitivity of the gains to small changes in the closed loop poles.

To conclude this chapter, note that we have achieved the goals that we set at the beginning. Specifically, we have shown that the dynamic model obtained for the series resonant converter in Chapter IV can be used to design feedback for the converter. Also, we have demonstrated the importance of the computer calculation delay in the dynamics of systems using digital controllers. Moreover, we have pointed out some of the problems associated with the implementation of periodic output feedback, since most of the work done on that area has been theoretical.

InductEV, Inc.
Exhibit 1014
Page 184



(a) Control from the Simulator

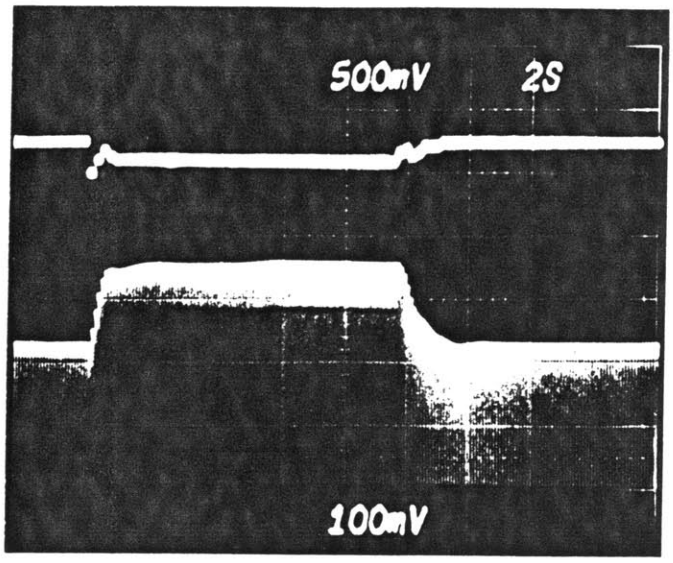


(b) Control from the Compupro computer

For both:
Upper trace: switching frequency
Lower trace: output current

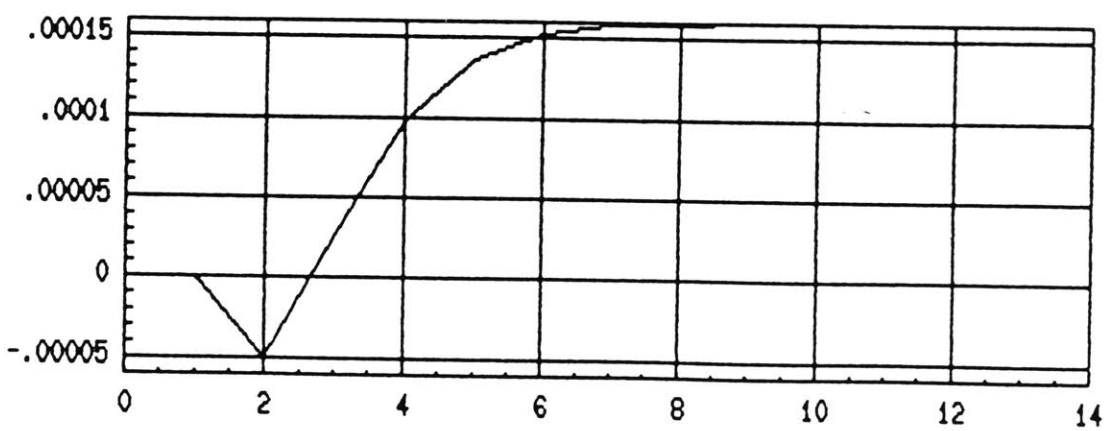
Fig. 5-15 Open-loop response of the output current to a 5% step in the switching frequency

InductEV, Inc.
Exhibit 1014
Page 185



Upper trace: switching frequency
Lower trace: output current

(a) Compupro microcomputer

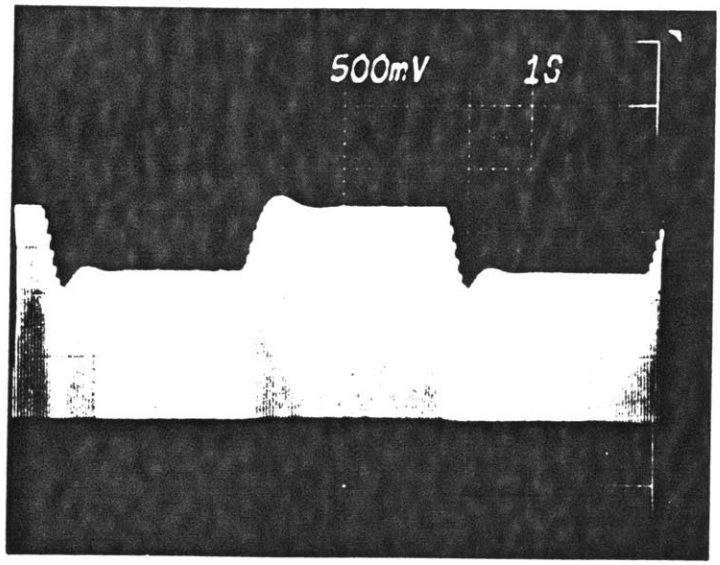


(b) MATRIX X simulations

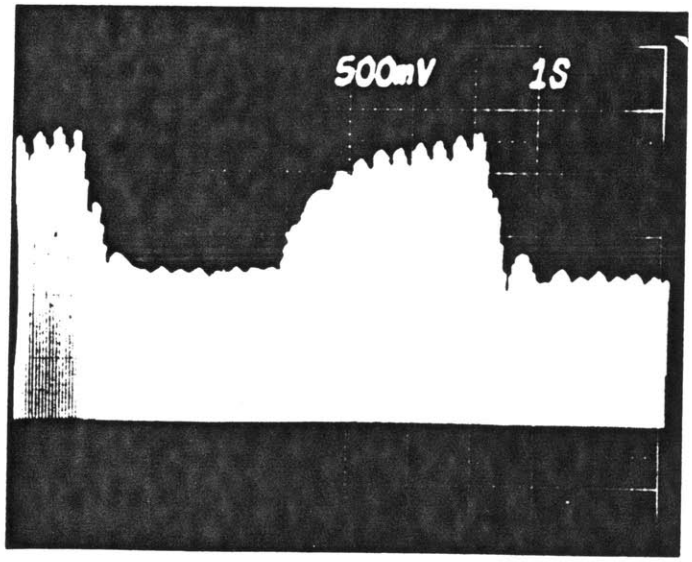
Closed-loop poles at z = 0, 0.1 and 0.5

Fig. 5-16 State feedback response using the Compupro microcomputer

InductEV, Inc.
Exhibit 1014
Page 186



(a) Open-loop response

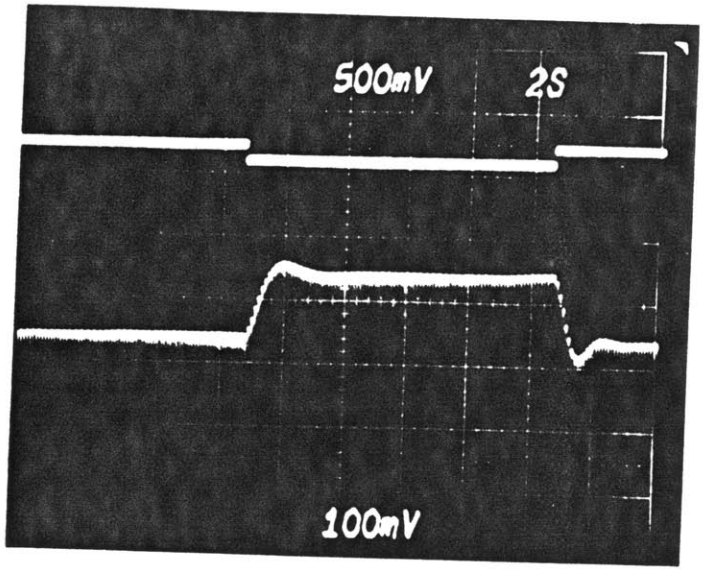


Poles at z = 0, 0.1, 0.1

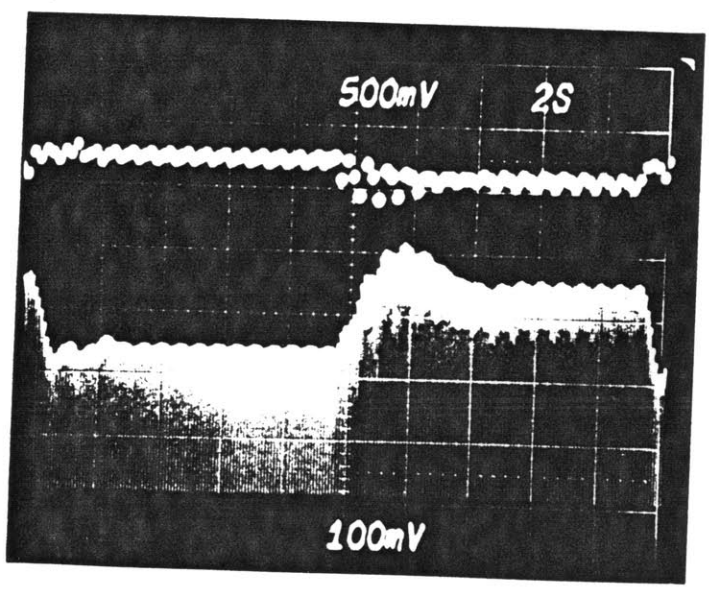
(b) Closed-loop response

Fig. 5-17 Periodic output feedback response of the output current using the generalized controller

InductEV, Inc.
Exhibit 1014
Page 187



(a) Open-loop response



(b) closed loop response with poles at z = 0, -0.1, -0.1

For both:

Upper trace: switching frequency
Lower trace: output current

Fig. 5-18 Periodic output feedback using the Compupro microcomputer

InductEV, Inc.
Exhibit 1014
Page 188

CHAPTER VI

SUMMARY AND DIRECTIONS FOR FURTHER WORK

(1) Summary

The literature review presented in Chapter II summarizes the work done on resonant converters in the following two areas:

(i) Analyzing a specific converter and deriving design nomograms using some normalized parameters such as: the output power range, frequency range, distortion factor on output voltage and current, efficiency, voltage and current ratings of circuit components, and weight and size of the converter [1] - [37].

(ii) Overcoming the limitations of the thyristor turn-off time at high frequency. In this area, thyristor inverter circuits have been modified to perform at frequencies higher than those set by the thyristor turn-off time. Many authors have successfully applied the technique of time-sharing to some conventional thyristor power inverters and developed new time-sharing inverter technology to overcome the operating limitations of the thyristor turn-off time.

The work of this thesis has explored three topics in the area of resonant converters. The first topic is concerned with developing methodologies that systematically categorize the resonant converter topologies. The second topic is the development of dynamic models for resonant converters. The third topic studies the use of these dynamic model to design feedback controls for resonant converters.

In the area of topology, three methods to systematically develop resonant converter topologies have been presented in Chapter III. The first method starts with the fundamental function of a resonant

InductEV, Inc.
Exhibit 1014
Page 189

converter as a dc-ac converter, and the three parts that constitute the converter: source, a switching network and a load. A switching cell that connects the source to the load is suggested, and two basic topologies are then developed. These are the asymmetric and symmetric topologies. In the asymmetric topology the voltage across the load is unidirectional. An asymmetric positive voltage implies that load voltage can be either equal to the dc source or zero, while asymmetric negative voltage implies that the load voltage either equals the negative of the dc source or zero. In the symmetric topology the dc voltage is symmetrically applied to the load. This is can be done in two ways: either by using one voltage source, one switching cell and a load, or by using two voltage sources, two switching cells and one load. The topology that results from the first way is named the full bridge topology, and the topology that results from the second way is named the half bridge topology. For these topologies the types of switch and load are also studied. For a voltage-fed converter, the switch can be either a unidirectional current switch or a bidirectional current switch, and the load can be a series resonant load or a parallel resonant load or their combination.

In the second method the structural symmetry of resonant converters is used to derive other topologies. The topologies are obtained either by splitting the resonant inductor, the resonant capacitor or both of them. When the resonant load inductor is split, the topology is referred to as a divided-inductor topology, and when the resonant load capacitor is split it is referred to as a divided-capacitor topology.

InductEV, Inc.
Exhibit 1014
Page 190

The third method uses duality to explore the relationships among resonant converters. Issues such as the type of switch, the number of components (weight and size), and the modes of operation of dual converters are discussed.

The topologies derived using the above three methods are also derived using linear network theory, as presented in Appendix 3A.

In the area of dynamic modeling of resonant converters, discussed in Chapter IV. Sampled-data models for both large-signal and small perturbations about a cyclic steady state have been developed. Although the procedure is general, it is illustrated using a series resonant converter. Transfer functions to the output of the converter from perturbations in the switching frequency, the input voltage, or load are directly obtained. Results obtained from the model match with simulations done using the MIT's Parity Simulator. Other issues such as sensitivity of the steady state operating point to changes in the circuit parameters, automatability of the converter analysis, and extension of the modeling approach to include other power electronic circuits have been discussed.

In the area of control of resonant converters, two control laws have been implemented, based on the dynamic model obtained in Chapter IV. These are state feedback control and periodic output feedback control. The two control laws are tested on a series resonant converter simulation set up on the Parity Simulator. The laws are implemented using two digital controllers. The first uses the Parity Simulator generalized controller, and the other uses a Compupro microcomputer. Interesting results have been obtained. First, it is demonstrated that one can obtain great improvement in the closed-loop reponse of the

InductEV, Inc.
Exhibit 1014
Page 191

series converter, compared to its open-loop response. Second the effect of the delay caused by the calculations in the computer on the closed-loop dynamics of the converter is investigated. Results have shown that this delay is important and should be modeled in the dynamics.

(2) Suggestions For Future Work

Extensions of the work done in this thesis could be done in the following:

(i) In the area of topologies, a comparative study among resonant converters needs to be done. This would extend the comparisons done in the this thesis, for dual converters.

(ii) A sensitivity study of the dynamic and steady state operation of a converter to changes in the controlling parameters, using the results obtained from the dynamic modeling of Chapter IV, is called for.

(iii) The control results of Chapter V need to be explored further. In particular, the results obtained for the periodic output feedback are not yet satisfactory, though the method holds promise. Also, it is important to apply both state feedback and periodic output feedback to control an actual resonant converter.

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Page 192

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