

THE DESIGN OF CMOS RADIO-FREQUENCY INTEGRATED CIRCUITS

SECOND EDITION

THOMAS H. LEE
Stanford University



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Table 4.4. *Comparison of individual capacitance terms for Case 3*

Method	Capacitance to ground of center wire (fF/ μ m)	Capacitance between center and outer wires (fF/ μ m)	Total capacitance of center wire (fF/ μ m)
Sakurai	0.115	0.039	0.154
2D value	0.056	0.100	0.156

of his two terms that happens to equal the total capacitive load on the center wire; the partitioning of this total into separate ground and mutual capacitances is another thing altogether.

As a specific example, let's consider the same conductor arrangement for which Table 4.3 was generated and compare calculations from Maxwell with those of Sakurai. This is shown in Table 4.4. As you can see, the sum of the Sakurai components equals that given by 2D simulations, but the individual terms don't agree at all.

4.4 INDUCTORS

From the point of view of RF circuits, the lack of a good inductor is by far the most conspicuous shortcoming of standard IC processes. Although active circuits can sometimes synthesize the equivalent of an inductor, they always have higher noise, distortion, and power consumption than "real" inductors made with some number of turns of wire.

4.5.1 SPIRAL INDUCTORS

The most widely used on-chip inductor is the planar spiral, which can assume many shapes; see Figure 4.21. The choice of shape is more often made on the basis of convenience (e.g., whether the layout tool accommodates non-Manhattan geometries) or habit than anything else. Despite stubborn lore to the contrary, the inductance and Q values attainable are very much second-order functions of shape, so engineers should feel free to use their favorite shape with relative impunity. Octagonal or circular spirals are moderately better than squares (typically on the order of 10%) and hence are favored when layout tools permit their use – or when that modest difference represents the margin between success and failure.

The most common realizations use the topmost metal layer for the main part of the inductor (occasionally with two or more levels strapped together to reduce resistance) and provide a connection to the center of the spiral with a crossunder implemented with some lower level of metal. These conventions arise from quite practical considerations: the topmost metal layers in an integrated circuit are usually the thickest and thus generally the lowest in resistance. Furthermore, maximizing the distance to the substrate minimizes the parasitic capacitance between the inductor and the substrate.

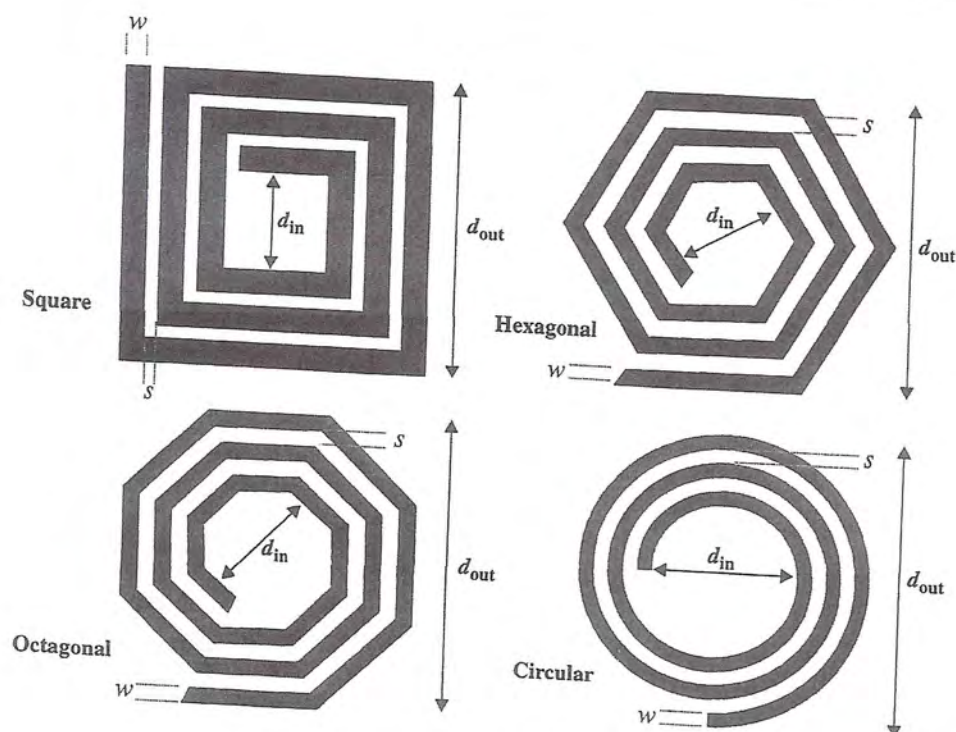


FIGURE 4.21. Planar spiral inductors.

The inductance of an arbitrary spiral is a complicated function of geometry, and accurate computations require the use of field solvers or Greenhouse's method.¹⁴ However, a (very) crude zeroth-order estimate, suitable for quick hand calculations, is

$$L \approx \mu_0 n^2 r = 4\pi \times 10^{-7} n^2 r \approx 1.2 \times 10^{-6} n^2 r, \quad (28)$$

where L is in henries, n is the number of turns, and r is the radius of the spiral in meters. This equation typically yields numbers on the high side, but generally within 30% of the correct value (and often better than that).

For shapes other than square spirals, multiply the value given by the square spiral formula by the square root of the area ratio to obtain a crude estimate of the correct value (see Eqn. 50). Thus, for circular spirals, multiply the square-spiral value by $(\pi/4)^{0.5} \approx 0.89$, and by 0.91 for octagonal spirals.

Perhaps more useful for the approximate *design* of a square spiral inductor is the following equation:

$$n \approx \left[\frac{PL}{\mu_0} \right]^{1/3} \approx \left[\frac{PL}{1.2 \times 10^{-6}} \right]^{1/3}, \quad (29)$$

¹⁴ H. M. Greenhouse, "Design of Planar Rectangular Microelectronic Inductors," *IEEE Trans. Parts, Hybrids, and Packaging*, v. 10, no. 2, June 1974, pp. 101-9. This classic paper describes a readily implemented algorithm for accurately computing the inductance.

CHAPTER NINE

HIGH-FREQUENCY AMPLIFIER DESIGN

9.1 INTRODUCTION

The design of amplifiers at high frequencies involves more detailed considerations than at lower frequencies. One simply has to work harder to obtain the requisite performance when approaching the inherent limitations of the devices themselves. Additionally, the effect of ever-present parasitic capacitances and inductances can impose serious constraints on achievable performance.

At lower frequencies, the method of open-circuit time constants is a powerful intuitive aid in the design of high-bandwidth amplifiers. Unfortunately, by focusing on minimizing various RC products, it leads one to a relatively narrow set of options to improve bandwidth. For example, we may choose to distribute the gain among several stages or alter bias points, all in an effort to reduce effective resistances. These actions usually involve an increase in power or complexity, and at extremes of bandwidth such increases may be costly. In other cases, open-circuit time constants may erroneously predict that the desired goals are simply unattainable.

A hint that other options exist can be found by revisiting the assumptions underlying the method of open-circuit time constants. As we've seen, the method provides a good estimate for bandwidth only if the system is dominated by one pole. In other cases, it yields increasingly pessimistic estimates as the number of poles increases or their damping ratio increases. Additionally, open-circuit time constants can grossly underestimate bandwidth if there are zeros in the passband. These observations suggest that alternative ways to increase bandwidth might involve the deliberate violation of the very conditions on which the method of open-circuit time constants relies.

Following up on this idea leads us to a collection of extremely useful bandwidth extension techniques. We'll consider what happens if we *purposefully* introduce a zero or complex pole pair into a transfer function, for example, or if we deliberately construct a system of high order. We'll also consider the design of *narrowband* amplifiers. As we'll see, it is considerably easier to obtain gain if it is to be provided only over a narrow band centered about some nominal operating frequency.

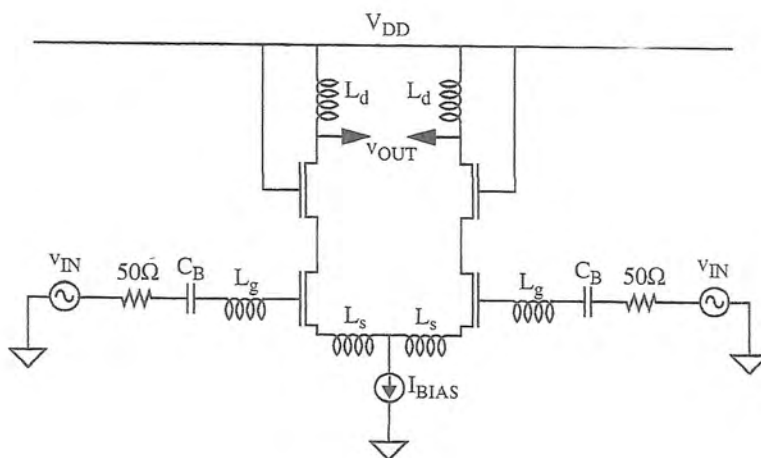


FIGURE 12.10. Differential LNA (simplified).

potential as the bottom of the source degenerating inductor. However, there is inevitably a difference in these potentials because there is always some nonzero impedance between the two points. Since 1.4 nH is not a lot of inductance, small amounts of additional parasitic reactance between the two grounds can have a large effect on amplifier performance. It can even allow signal-dependent currents from subsequent stages to modulate “ground,” forming a parasitic feedback loop that destabilizes the amplifier.

Dedicating additional ground pins or using sophisticated packages can mitigate this problem, but such measures are either of limited effectiveness or somewhat costly. An alternative is to exploit the incremental ground located at the symmetrical point of a differential structure. See Figure 12.10, where the source degenerating inductances return to a virtual ground (for differential signals). Any parasitic reactance in series with the bias current source is largely irrelevant, since a current source in series with an impedance is still a current source. Hence, the real part of the input impedance is controlled only by L_s and is unaffected by parasitics in the current source’s ground return path.

Another important attribute of the differential connection is, of course, its ability to reject common-mode disturbances.²¹ This consideration is particularly important in mixed-signal applications, where both the supply and substrate voltages may be noisy. To maximize common-mode rejection at high frequencies, it is critically important for the layout to be absolutely as symmetrical as possible.

It is important to keep in mind that – for equal total power consumption – the noise figure of this amplifier is higher than its single-ended counterpart. Specifically, the

²¹ To ensure the truth of this statement, the spiral inductors of both half-circuits should be laid out with the same orientation, not mirrored; otherwise, inductively coupled noise will not appear as a common-mode signal.