

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP USA, INC.,
Petitioner,

v.

BELL SEMICONDUCTOR, LLC,
Patent Owner

Case: IPR2024-00142

U.S. Patent No. 7,535,330

**EXPERT DECLARATION OF DR. JOSEPH BERNSTEIN IN SUPPORT
OF PATENT OWNER'S PRELIMINARY RESPONSE**

Mail Stop **PATENT BOARD**
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

TABLE OF CONTENTS

I. INTRODUCTION	1
II. QUALIFICATIONS	1
III. PRIOR TESTIMONY	7
IV. COMPENSATION	7
V. MATERIALS CONSIDERED	8
VI. UNDERSTANDING OF THE LAW	9
A. Legal Standards for Prior Art	11
B. Legal Standards for Anticipation.....	12
C. Legal Standard for Obviousness.....	13
VII. OPINION.....	18
A. The '330 Patent.....	18
B. Marques Does Not Disclose the Features of Claim 1	21
1. Marques Does Not Disclose A Multiple Inductor Array With Three Nodes .	
.....	21
2. Petitioner's "First Node" Does Not Receive a First Current and a Second	
Current.....	26
3. Marques Does Not Disclose a First Inductor Coil Coupled to the First Node	
and a Second Node.....	30
4. Marques Does Not Disclose a Second Inductor Coil Coupled to the First	
Node and a Third Node	31
5. Marques's Inductive Structure Would Not Operate Like the Claimed	
Invention Even If First and Second Currents Are Received at the Fictitious First	
Node	32
C. The Combination of Lee and Marques Does Not Disclose the Features of	
Claim 11	34
1. Lee Teaches Away From The Proposed Combination	34
2. The Combination of Lee and Marques Does Not Disclose the Features of	
Claim 11	35
D. Menegoli Does Not Disclose the Features of Claim 1	37

1. Menegoli Does Not Disclose A Multiple Inductor Array With Three Nodes	38
2. Petitioner’s “First Node” Does Not Receive a First Current and a Second Current.....	41
3. Menegoli Does Not Disclose a First Inductor Coil Coupled to the First Node and a Second Node.....	43
4. Menegoli Does Not Disclose a Second Inductor Coil Coupled to the First Node and a Third Node.....	43
5. Menegoli’s Inductive Structure Would Not Operate Like the Claimed Invention Even If First and Second Currents Are Received at the Fictitious First Node	44

I. INTRODUCTION

1. My name is Dr. Joseph Bernstein and I have been retained as a technical expert by counsel for Patent Owner Bell Semiconductor, LLC (“Bell Semic” or “Patent Owner”) to provide expert opinion testimony in the above captioned matter.

2. I have been asked to render opinions on Petitioner’s unpatentability arguments regarding U.S. Patent No. 7,535,330 (“the ’330 patent”) that have been identified in the Petition. Specifically, I have been asked to consider whether certain references would have disclosed or suggested the features recited in claims 1 and 11 of the ’330 patent to a person of ordinary skill in the art.

3. This report contains statements of my opinions formed to date regarding these references and the ’330 patent and the bases and reasons for those opinions. I may offer additional opinions based on further review of materials in this case, including opinions and/or testimony of other expert witnesses.

II. QUALIFICATIONS

4. This is a summary of my background and qualifications. I set forth my background in more detail in my Curriculum Vitae (“CV”), below.

5. I graduated *Summa Cum Laude* from Union College in Schenectady, NY with a Bachelor of Science degree in Electrical Engineering in 1984.

Subsequently, I attended the Massachusetts Institute of Technology (MIT), where I earned a Master of Science degree in Electrical Engineering and Computer Science in 1986, an Electrical Engineering degree in 1987, and a Doctor of Philosophy in Electrical Engineering and Computer Science in 1990.

6. After earning my Ph.D., I worked at MIT Lincoln Laboratory as a senior research staff member, during which time I taught at Boston University as an Adjunct Professor. My first position at Lincoln Labs was as a senior research staff in the Wafer Scale Integration group. This group was responsible for developing technologies to allow programming and packaging of wafer scale integrated circuits. Technologies we developed included mounting, wiring, routing, programming, packaging, and reliability for very large wafer scale integrated circuits. This is where I developed laser programmable interconnect technology which was my first set of patents and was the basis for my first start-up company, Lightspeed Semiconductor, and my introduction to the field of Microelectronics Reliability. I have a book from that era: Hoang, H.H., Schutz, R., Bernstein, J.B., Vasquez, B., *Multi-level Interconnection: Issues that Impact Competitiveness*, Proceedings of SPIE 2090, 1993.

7. From 1995 to 2007, I was first an Assistant and then Associate Professor of Engineering at the University of Maryland (UMD) while acting as co-

founder and chief scientist of Lightspeed, a Silicon Valley company relating to high performance, metal-configurable gate arrays using laser anti-fuses. Upon arriving at UMD as a professor of Microelectronics Reliability, I was soon invited by the head of the Packaging Reliability Center (CALCE), Professor Michael Pecht, to lead a group of industry packaging experts to investigate the emerging Korean electronics industry. This experience led to my complete immersion and familiarity with the latest packaging techniques in the world, primarily those happening in South Korea. This led to my next book as a co-author: Pecht, M., Bernstein, J.B., Searls, D., and Peckerar, M., *The Korean Electronics Industry*, CRC Press, 1997.

8. Thus, my background started from my collaborations at UMD and my work with the industry. My research programs brought me close with many companies around the world looking into better, cheaper, and more reliable packaging techniques for the latest industrial technologies. I have several journal publications from that era in the field of electronic packaging from my research and student supervision in industry. Some more appropriate publications from the time include the following:

- Gershman and J. B. Bernstein, “*Structural health monitoring of solder joints in QFN package*,” Microelectronics Reliability, Volume 52, Issue 12, Pages 3011–3016 (2012).

- L. Yang and J. Bernstein, “*Reliability Evaluation and Modeling of High Density Electronic Packages*,” Microelectronics International, vol. 29, no. 1, pp. 15-21 (2012).
- Gershman and J. B. Bernstein, “*Solder-Joint Quantitative Crack Analysis—Ohmic Resistance Approach*,” IEEE Transaction on Components, Packaging and Manufacturing Technology, vol. 2, no. 5, pp. 748 - 755 (2012).
- L.-S. Yang and J.B. Bernstein, “*Encapsulation Process Development for Flexible Circuit Based Chip Scale Packages*,” IEEE Trans. Electronics Packaging Manufacturing, vol. 25, no. 4, pp. 344-354 (October 2002).
- L.-S. Yang, J.B. Bernstein and K.C. Leong, “*Effect of the Plasma Cleaning Process on Plastic Ball Grid Array Package Assembly Reliability*,” IEEE Trans. Electronics Packaging Manufacturing, vol. 25, no. 2, pp. 91-99 (April 2002).
- Yang, L., Bernstein, J.B., Chung, K, “*The Impact of Lead-free Soldering on Electronics packages*,” Microelectronics International, vol. 18, no. 3, pp. 20-26 (2001).

9. Many more of my publications and patents (including my work on electronic packaging and testing) are listed in my CV.

10. While at the University of Maryland, I taught in the Reliability program as the specialist in microelectronics device reliability. In the summer of 1998, I joined the Jet Propulsion Laboratories as a NASA Summer Faculty Research Fellow. At UMD, I was promoted from Assistant to Associate Professor with tenure in 2001. From 2003 to 2005, I was a Professor of Engineering at Tel-Aviv University on Sabbatical from the University of Maryland and as a Fulbright Fellow lecturer, and researcher. During my tenure at Maryland, I had many programs also sponsored at the National Institute of Standards and Technology

(NIST), where I worked directly with the semiconductor industry by means of the connection with NIST. This group acted as a government liaison with semiconductor manufacturing companies and often was the center for Joint Electron Device Engineering Council (JEDEC) roundtables and committee groups focused on reliability and standards for the semiconductor industry.

11. I am currently employed at Ariel University of Israel. At Ariel, a large focus of my research is on issues related to chip and packaging reliability, including links between reliability, power, and thermal behavior. My current research focuses on packaged devices at the board level. We look at the functionality and performance of system-level reliability boards and packages, including FPGAs embedded with DRAM and Flash memory. We look at all the failure mechanisms that can affect the reliability of the circuits and systems and model these mechanisms to derive a complete reliability prediction methodology.

12. I also work with several consulting clients in the semiconductor field that apply my methodologies, as well as system level customers and various smaller companies and startups.

13. I have published several books, one new one is completed and expected to be published in 2024. I have published more than 120 refereed journal publications and conference papers, a more complete list of which is included in

my CV. In addition to my publications, I have given numerous tutorials, talks, presentations, and lectures, in both academic and corporate settings, on semiconductor devices and reliability. For at least the past five years, I am the first or second most referenced author in the field of Microelectronics Reliability as listed by Google Scholar.

14. I have been affiliated with the Reliability Program of the Mechanical Engineering Department, the Electrical and Computer Engineering Department, and the Institute for Research in Electronics and Applied Physics at the University of Maryland. I was also affiliated with the Nano-Science and Nano-Technology Center at Tel-Aviv University, which I headed during my Sabbatical there. I also served as the Founder and Faculty advisor for the Israel Electronics Manufacturers Working Group on Reliability (ILTAM), and I lead the Laboratory for Reliable Electronics Systems at Ariel University.

15. I currently supervise two Ph.D. candidates and one post-doc. I have served as the advisor or co-advisor for twenty Ph.D. graduates in electrical and electronic engineering, many of whom graduated in the materials and mechanical engineering departments through the Reliability Program at the University of Maryland and several more in Israel.

16. I teach classes at Ariel University that include undergraduate and

graduate courses in Electrical Engineering. Some courses I have taught include VLSI Design, Reliability Engineering Fundamentals, Microelectronics Device Reliability, Advanced Reliability Engineering, and Quality Engineering Fundamentals. I have also developed coursework and curriculum on Reliability Engineering and Electronic Device Reliability.

17. I am a named inventor on at least eight issued U.S. utility patents in fields including electrical interconnections and repairable systems in microelectronics packaging technology.

III. PRIOR TESTIMONY

18. I have served as a testifying expert in litigation in ten district court cases. I have also served as an expert in several matters at the Patent Trial and Appeal Board, including *inter partes* reviews and patent reexaminations.

19. I have also served as a technical consultant for electronics and computer systems companies on issues including testing and reliability.

20. A list of all such cases in which I have consulted or testified as an expert at trial or by deposition can be found in my CV.

IV. COMPENSATION

21. I am being compensated for my services in this proceeding. My compensation is not contingent upon my performance, the outcome of this case, or

any issues involved in or related to this case. I have no financial interest in this matter.

V. MATERIALS CONSIDERED

22. My opinions are based on my experience in this field, and are necessarily formed by my own experiences, materials I have read over the years, and discussions I have had with colleagues during my career. In addition, I have reviewed and considered the following materials in forming my opinion:

- The '330 patent (Ex. 1001);
- The File History of the '330 patent (Ex. 1004);
- The Marques reference, U.S. Patent No. 7,955,886 (Ex. 1005);
- JR Lucas, "Resonance & Mutual Inductance," University of Maratuwa (Nov. 2001) (Ex. 1006)
- The Menegoli reference, U.S. Patent No. 7,221,251 (Ex. 1007); and
- The disclosed excerpts of the Lee reference, Thomas A. Lee, The Design of CMOS Radio-Frequency Integrated Circuits (2d ed.) (Ex. 1008);
- Ron Schmitt, Electromagnetics Explained (1st ed.) (Ex. 1009); and
- Anant Agarwal, et al., Foundations of Analog and Digital Electronic Circuits (2005) (Ex 1014).

VI. UNDERSTANDING OF THE LAW

23. I am not an attorney. For the purposes of this declaration, Patent Owner's counsel has informed me about certain aspects of the law that are relevant to my opinions. I have applied those legal principles in arriving at my conclusions expressed in this declaration.

24. I understand that the first step in performing a validity analysis of the patent claims is to interpret the meaning and scope of the claims by construing the terms and phrases found in those claims. I understand that a determination of the meaning and scope of the claims is a matter of law. I have been informed that to determine the meaning of the claims, courts consider the intrinsic evidence, which includes the patent's claims, written description, prosecution history, materials incorporated by reference in the patent, and prior art cited in the patent or its prosecution history. Courts give claim terms their ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the content of the entire patent. A patentee may also define his or her own terms or disclaim claim scope. Normally, embodiments and examples appearing in the specification will not generally be read into the claims. However, the intrinsic record may resolve ambiguous claims terms where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to

permit the scope of the claim to be ascertained from the words alone. A term's context in the claims can also be helpful. Differences among the claim terms can also assist in understanding a term's meaning.

25. I have been informed that extrinsic evidence can also be useful in determining the meaning of claims, however, it is less significant than the intrinsic record. Technical dictionaries may be useful to show the way one skilled in the art might use claim terms, but technical dictionaries may provide definitions that are too broad or may not be indicative of how the term is used in the patent.

26. I understand that the claim terms of a patent are to be construed from the point of view of a hypothetical person of skill in the art (POSITA) in the time frame of the patent's priority date. (At times I may refer to a person of skill in the art as simply "a skilled person.") For the purpose of assessing the level of ordinary skill of such an individual, I have considered the types of problems encountered in the art, the prior solutions to those problems found in the literature, the speed with which innovations were made in the time relevant time frame, and the level of education and expertise of active workers in the field.

27. I have been informed that, for the purposes of this declaration only, that a POSITA at the time of the invention of the '330 patent would have had at least the equivalent of a bachelor's degree in electrical engineering and one to two

years of experience in the field of circuit design, particularly the design of circuits operating at high frequencies. Given the above description of a POSITA, and based on my education and advanced experience, I believe that I at least meet or even exceed the necessary qualifications in the timeframe of the invention.

A. Legal Standards for Prior Art

28. I understand that a patent or other publication must first qualify as prior art before it can be used to invalidate a patent claim.

29. I understand that a U.S. or foreign patent qualifies as prior art to an asserted patent if the date of issuance of the patent is prior to the invention of the asserted patent. I further understand that a printed publication, such as an article published in a magazine or trade publication, qualifies as prior art to an asserted patent if the date of publication is prior to the invention of the asserted patent.

30. I understand that a U.S. or foreign patent also qualifies as prior art to an asserted patent if the date of issuance of the patent is more than one year before the filing date of the asserted patent. I further understand that a printed publication, such as an article published in a magazine or trade publication, constitute prior art to an asserted patent if the publication occurs more than one year before the filing date of the asserted patent.

31. I understand that a U.S. patent qualifies as prior art to the asserted

patent if the application for that patent was filed in the United States before the invention of the asserted patent.

B. Legal Standards for Anticipation

32. I have been informed by counsel and understand that to anticipate a patent claim, all of the requirements of that claim must be shown to be present in a single previous device or method that was known of, used, or described in a single previous printed publication or patent. Anticipation should be assessed on a claim-by-claim basis. I also understand that anticipation can occur when an undisclosed limitation is literally missing but is present because the prior art must necessarily function in accordance with, or include, the undisclosed limitation.

33. I have further been informed that only a single reference should be relied upon to anticipate a claim unless any further references are cited solely to:

- a. prove that the primary reference contains an “enabled disclosure;”
- b. explain the meaning of a term used in the primary reference; or
- c. show that a characteristic not disclosed in the reference is inherent.

34. I understand that to anticipate a claim, the prior art does not need to use the same words as the claim, but all the requirements of the claim must have

been disclosed, either stated expressly or implied to a person having ordinary skill in the art in the technology of the invention.

35. I understand that for a reference to anticipate a patent claim, that reference must also enable one of ordinary skill in the art to make and use the full scope of the claimed invention without undue experimentation.

36. I understand that documents and materials that qualify as prior art can be used to invalidate a patent claim via anticipation or obviousness.

37. I understand that, once the claims of a patent have been properly construed, the second step in determining anticipation of a patent claim requires a comparison of the properly construed claim language to the prior art on a limitation-by-limitation basis.

38. I understand that a prior art reference “anticipates” an asserted claim, and thus renders the claim invalid, if all elements of the claim are disclosed in that prior art reference, either explicitly or inherently (i.e., necessarily present).

39. I understand that anticipation in an *inter partes* review must be shown by a preponderance of the evidence, which is a higher standard than the reasonable likelihood required to institute an *inter partes* review.

C. Legal Standard for Obviousness

40. I understand that even if a patent is not anticipated, it is still invalid if

the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole would have been obvious at the time the invention, was made to a person of ordinary skill in the pertinent art.

41. I understand that a person of ordinary skill in the art provides a reference point from which the prior art and claimed invention should be viewed. This reference point prevents one from using his (or her) own insight or hindsight in deciding whether a claim is obvious.

42. I also understand that an obviousness determination includes the consideration of various factors such as:

- a. the scope and content of the prior art,
- b. the differences between the prior art and the asserted claims,
- c. the level of ordinary skill in the pertinent art, and
- d. the existence of secondary considerations such as commercial success, long-felt but unresolved needs, failure of others, etc.

43. I understand that an obviousness evaluation can be based on a combination of multiple prior art references. I understand that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but other times the nexus linking two or more prior art references is just common sense. I further understand that obviousness analysis recognizes that market

demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may be supplied by the direction of the marketplace.

44. I understand that if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

45. I also understand that practical and common-sense considerations should guide a proper obviousness analysis, because familiar items may have obvious uses beyond their primary purposes. I further understand that a person of ordinary skill in the art looking to overcome a problem will often be able to fit together the teachings of multiple publications. I understand that obviousness analysis therefore considers the inferences and creative steps that a person of ordinary skill in the art would employ under the circumstances.

46. I understand that a particular combination may be proven obvious merely by showing that it was obvious to try the combination. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp because the

result is likely the product not of innovation but of ordinary skill and common sense.

47. The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, the patent claim is likely obvious.

48. It is further my understanding that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill in the art, not just the patentee. Accordingly, I understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

49. I understand that a claim can be obvious through consideration of a single reference, without the need to combine references, if the elements of the claim that are not found explicitly or inherently in the reference can be supplied by the common sense of one of skill in the art.

50. I understand that secondary indicia of non-obviousness may include:

- a. a long felt but unmet need in the prior art that was satisfied by

the invention of the patent;

- b. commercial success of processes covered by the patent;
- c. unexpected results achieved by the invention;
- d. praise of the invention by others skilled in the art;
- e. taking of licenses under the patent by others;
- f. deliberate copying of the invention;
- g. failure of others to find a solution to the long-felt need; and
- h. skepticism by experts.

51. I also understand that there must be a relationship between any such secondary considerations and the invention.

52. I further understand that contemporaneous and independent invention by others is a secondary consideration supporting an obviousness determination.

53. In summation, my understanding is that prior art teachings are properly combined where a person of ordinary skill in the art having the understanding and knowledge reflected in the prior art and motivated by the general problem facing the inventor, would have been led to make the combination of elements recited in the claims. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of multiple prior art

references in the claimed manner.

54. I understand that obviousness in an *inter partes* review must be shown by a preponderance of the evidence, which is a higher standard than the reasonable likelihood required to institute an *inter partes* review.

VII. OPINION

A. The '330 Patent

55. The '330 Patent is directed to, among other things, positioning two inductors in a multi-inductor array such that both are coupled to a common node that receives first and second currents and such that the polarities of the magnetic fields produced by each are opposite to each other, causing net reduction in parasitic mutual inductance because the magnetic field produced by each inductor is at least partially canceled out when it interferes with the field produced by the other.

56. The '330 patent was developed to address problems arising from the continual increase of component density within electrical circuits, particularly the effects of electrical cross-coupling, which are a more significant issue in circuits that are operating at high frequencies and negatively impact device timing. ('330 patent at 1:17-19.)

57. An embodiment of the invention, illustrated in Figure 4 of the '330

patent (reproduced below), includes running two currents from a common node through the inductors in opposite directions to generate magnetic fields with opposite polarities, such that the respective magnetic fields interfere with each other and at least partially cancel at a particular point, thereby reducing parasitic mutual inductance. ('330 patent at 2:17-26.)

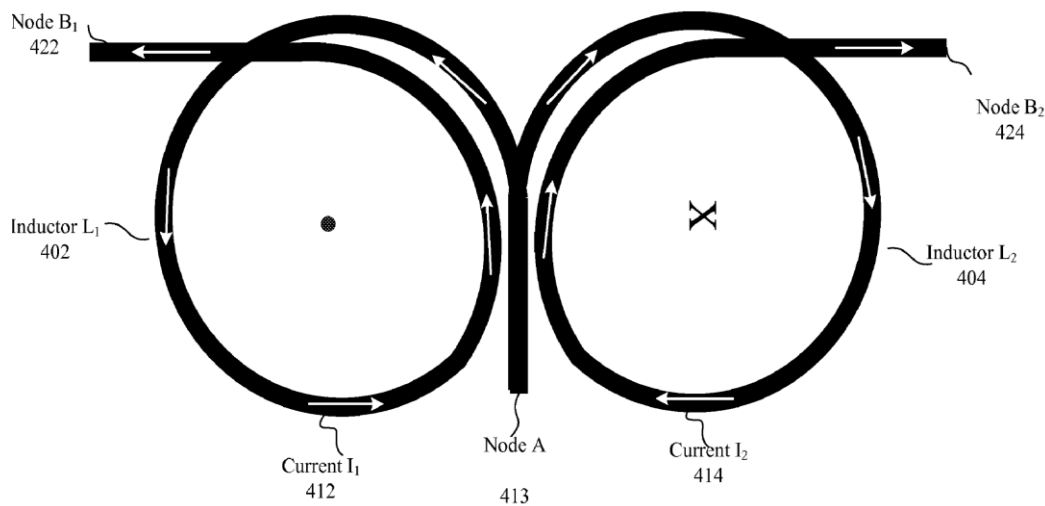


Figure 4

58. The '330 patent contains 3 independent claims and 20 total claims, covering the placement of inductors in electrical circuits. ('330 patent at 5:44-6:65.) Claim 1 of the '330 patent reads:

1. A multiple inductor array comprising:

a first node that receives a first current and a second current;

a first inductor coil, coupled to the first node and to a second node, that communicates the first current in a clockwise direction and generates a first magnetic field;

a second inductor coil, coupled to the first node and to a third node, that communicates the second current in a counter clockwise direction and generates a second magnetic field having an opposing orientation to the first magnetic field; and

wherein the first magnetic field and the second magnetic field at least partially cancel at an interference point.

59. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, including, e.g., meeting electromagnetic compatibility requirements, improving system performance by reducing crosstalk, and improving efficiency and reducing production cost by increasing component density.

60. The development of the innovation described in the '330 patent addressed problems arising from the continual increase of component density within electrical circuits, particularly the effects of electrical cross-coupling, which are a more significant issue in circuits that are operating at high frequencies and negatively impact device timing. ('330 patent at 1:17–19.) Prior to the inventions of the '330 patent, the typical placement of certain electrical components within a circuit (particularly inductors) would produce unwanted cross-coupling. (*Id.* at

1:25–28.) This forced circuit designers to provide a sufficient distance between inductor coils to sufficiently reduce electro-magnetic interference between them, which made it difficult to obtain the frequencies and component densities that current technologies required. (*Id.* at 1:33–37.)

61. The inventors of the '330 Patent developed circuits that could place two inductors more closely than before while minimizing the effects of the cross-coupling, and they ultimately conceived of a method for minimizing mutual inductance between the inductors, at least at particular locations in close proximity to the inductors. (*Id.* at 2:16–17.) One embodiment of the invention includes running current through the inductors in opposite directions to generate magnetic fields with opposite polarities, such that the respective magnetic fields interfere with each other and at least partially cancel at a particular point in proximity to the inductors, thereby reducing parasitic mutual inductance. (*See id.* at 2:17–26.)

B. Marques Does Not Disclose the Features of Claim 1

62. In my opinion, Marques does not disclose all of the features of claim 1.

1. Marques Does Not Disclose A Multiple Inductor Array With Three Nodes

63. In the '330 patent, three nodes are utilized to connect the inductive array to other components in a circuit. (*See, e.g.*, Ex. 1001 at 1:67-2:2, 2:46-48,

5:33-35, and FIG. 2 (showing two inductors L_{s1} and L_{s2} connected by two nodes to a pair of transistors and by a common node to a ground in a DLNA circuit).) (For purposes of this declaration, I have been asked to construe the term “node” to mean “a point of connection or intersection in an electrical circuit.”) Because the claimed inductive array includes three nodes, it is suitable for use in circuits where there may be a transient differential between the first and second currents flowing through the inductors that could result in a change in mutual inductance in one of the inductors. (Ex. 1001 at 4:56-62.) For example, if there is a change of current flowing through the first inductor such that a corresponding first magnetic field produced by the first inductor changes and results in a change in mutual inductance in the second inductor, the claimed invention allows the change in mutual inductance in the second inductor to be addressed by changing the oppositely oriented magnetic field generated by the second inductor to achieve appropriate interference cancellation, e.g., by making a change in the current flowing through the second inductor. (*Id.* at 4:63-5:5.) This interference cancellation results in a reduction of cross talk between the first and second inductors. (*Id.* at 5:5-8.)

64. In my opinion, every inductive structure disclosed in Marques consists of only two nodes—terminals 12 and 14 in FIGS. 2-6 and terminals 20 and 22 in FIGS. 7 and 8—so that each inductive structure may be used in place of a

conventional two-terminal inductor (such as the single loop inductor 10 with two terminals 12 and 14 depicted in FIG. 1 of Marques) in a circuit where an inductance is required. That is, just like a conventional two-terminal inductor, each inductive structure in Marques is designed to be connected in a circuit via two terminals. For example, Marques notes that “[in] some conventional applications, . . . inductor designs use inductors with one loop The present invention utilizes structures with two differential loops, in order to minimize noise and interference with other components in a device.” (Ex. 1005 at 3:35-40.) The conventional inductor is shown and described in Marques as having two terminals, e.g., Ex. 1005 at FIG. 1 labels 12 and 14, as is every disclosed inductor design, *see, e.g.*, Ex. 1005 at FIGS. 2-6 labels 12 and 14 and FIGS. 7-8 labels 20 and 22. There is no disclosure in Marques of there being an additional node that connects the inductive loop structure in a circuit.

65. Because the inductive structures of Marques are two terminal devices, the currents across the inductors are not individually adjustable, so the inductive structures of Marques are not able to address a change in mutual inductance in one inductor caused by a transient change in current in the other inductor. Instead, Marques purports to solve a different problem, namely that “in a circuit where inductors are used, the inductors can interfere with other components in the

circuit.” (*Id.* at 1:14-16). To address this problem, Marques “utilizes structures with two differential loops, in order to reduce or minimize noise and interference with other components in a device.” (*Id.* at 3:38-40.) In other words, Marques proposes replacing conventional inductors with his magnetically differential inductor structures in such cases. (*See, e.g., id.* at 10:62-67, 11:17-20 and 11:25-29.) More specifically, Marques proposes positioning other components of a circuit along an “axis 38” defined where magnetic cancellation between the magnetically differential inductors is optimal. (*See, e.g., id.* at 11:40-53.) Marques explains that magnetic cancellation is optimal “where the two opposite magnetic fields will be equal” (*Id.* at 7:8-12), which is another reason for its two terminal structure in which the same current flows through each inductor.

66. The inductor structure in Figure 5 of Marques is connected in a circuit using terminals 12 and 14. There is no disclosure in Marques of connecting the inductor structure in a circuit using the fictitious extra “node” added to Figure 5 by Petitioner shown in the annotated figure below. For at least these reasons, it is my opinion that FIG. 5 of Marques does not disclose an inductor structure with three nodes as claimed.

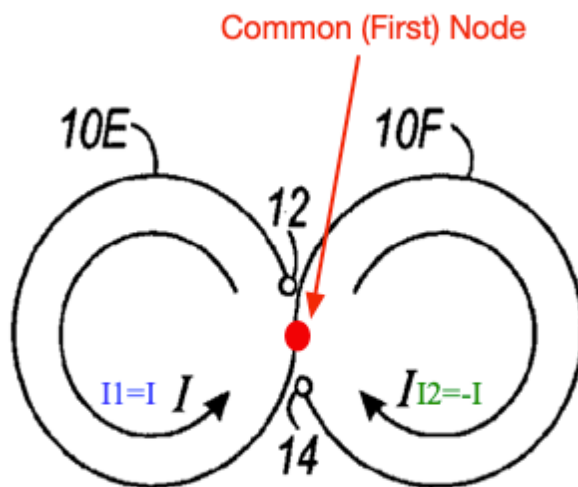


FIG. 5

FIG. 5 of Marques (Ex. 1005) (Annotated by Petitioner)

67. Petitioner also relies on the inductor structure shown in FIGS. 7 and 8 of Marques for disclosure of a first node. (Pet. at 10-11.) More specifically, Petitioner identifies terminal 20 in an annotated version of FIG. 8 of Marques (reproduced below) as a “Common (First) Node.” (Pet. at 10-11.) Notably, Petitioner does not identify either a “second node” or a “third node” in the annotated version of FIG. 8 or in its discussion of the inductor structure shown in FIGS. 7 and 8. (Pet. at 10-17.) In fact, like the inductor structure shown in FIG. 5, the inductor structure in FIGS. 7 and 8 includes only two nodes—terminals 20 and 22. Thus, it is my opinion that FIGS. 7 and 8 of Marques do not disclose an

inductor structure with three nodes as claimed.

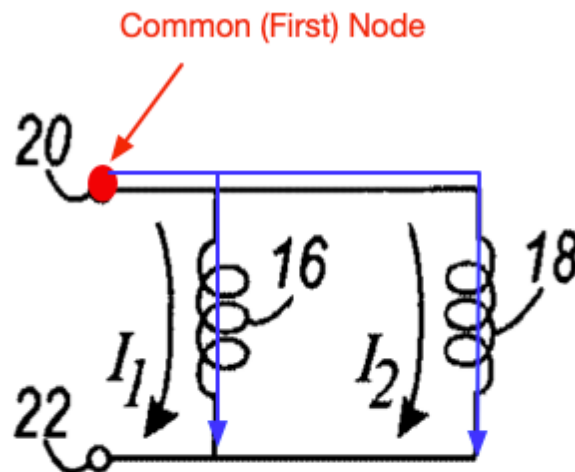


FIG. 8

FIG. 8 of Marques (Ex. 1005) (Annotated by Petitioner)

68. Even assuming Marques discloses a multiple inductor array with three nodes (which it doesn't), Petitioner's three nodes, *i.e.*, Petitioner's fictional "common node" and terminals 12 and 14 (or 20 and 22), do not operate in accordance with the language of claim 1.

2. Petitioner's "First Node" Does Not Receive a First Current and a Second Current

69. Claim 1 calls for a first node that “receives a first current and a second current.” Neither the fictitious “common node” in Petitioner’s annotated FIG. 5 of Marques, which Petitioner identifies as the claimed “first node” (*e.g.*, Pet. at 9-10), nor the terminal 20 in FIG. 8 of Marques, which Petitioner alternatively identifies as the claimed “first node” (*Id.* at 10-11), **receive** a first current **and** a second current, as required by the claim language.

70. The original FIG. 5 of Marques (reproduced below) shows a single current, *I*, flowing from terminal 12 to terminal 14. Inductor coils 10E and 10F are arranged in series between terminals 12 and 14 (Ex. 1005 at 5:12-14) and, therefore, the same current *I* also flows through the two inductor coils of the inductive structure (*Id.* at 5:21-25).

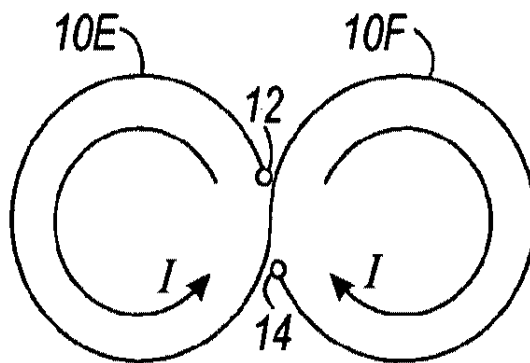


FIG. 5

71. Further, Marques states that “[a]n equivalent circuit diagram of the example shown in FIG. 5 would be similar to the diagram shown in FIG. 3.” (Ex. 1005 at 5:15-17.) Figure 3 of Marques is shown below.



FIG. 3

72. Again, as in FIG. 5, there is only a single current, I , flowing from terminal 12 to terminal 14 in FIG. 3. (See also *Id.* at 3:67-4:2.)

73. In Petitioner’s annotated FIG. 5, the fictitious common node is positioned between the terminals 12 and 14 and will therefore receive only a single current, I . Petitioner asserts that “[t]he common node can . . . be viewed as the intersection of where I_1 and I_2 meet (i.e., the first node receives a first and second current).” (Pet. at 9.) But there is no disclosure in Marques of separate currents, I_1

and I2, in the embodiment of FIG. 5. There is only a single current, I, disclosed. Petitioner re-names the current I as I1 when it travels through the first inductor coil and re-names the same current I as I2 when it travels through the second inductor coil. The separate currents I1 and I2 in Petitioner's annotated version of FIG. 5 are thus fictitious, like its common node. Moreover, even if Marques does disclose separate currents, I1 and I2 (which it does not), an examination of the direction of current flow in annotated FIG. 5 reveals that only I1 would be received at the fictitious common node proposed by the Petitioner, while the fictitious current I2 would flow from the fictitious common node. Thus, it is my opinion that the inductor structure in Petitioner's annotated Figure 5 would not include a first node "that receives a first current and a second current," as required by claim 1.

74. Similarly, there is no disclosure in Marques to support Petitioner's contention that terminal 20 in Petitioner's annotated version FIG. 8 of Marques, which Petitioner identifies as a "Common (First) Node," receives first and second currents I1 and I2. Indeed, an examination of the current flow in FIG. 8 reveals that the first and second currents I1 and I2 flow from the terminal 20 as opposed to being received by the terminal 20. As such, Petitioner's annotated Figure 8 would not include a first node "that receives a first current and a second current," as required by claim 1.

75. For all of the above reasons, it is my opinion that Marques does not disclose a multiple inductor array in which a first of three nodes receives first and second currents.

3. Marques Does Not Disclose a First Inductor Coil Coupled to the First Node and a Second Node

76. Petitioner identifies inductor coil 10F of annotated FIG. 5 of Marques as a first inductor coil coupled to the first node and a second node. (Pet. at 11-13.) However, as noted above, the inductive structure shown in FIG. 5 of Marques lacks a first node that receives a first current and second current. The fictitious first node proposed by Petitioner receives only a single current, I, and therefore cannot be a first node that receives a first current and a second current. Therefore, it is my opinion that Marques does not disclose a first inductor coil coupled to the first node and a second node, wherein the first node receives a first current and a second current.

77. With regard to annotated FIG. 8, as noted previously, Petitioner fails to identify a second node in the figure. Regardless, the terminal 20 identified as the first node by Petitioner has not been shown to “receive a first current and a second current,” as claimed. On the contrary, first and second currents I1 and I2 are shown flowing from the terminal 20. Therefore, it is my opinion that Marques

does not disclose “a first inductor coil, coupled to the first node and to a second node,” wherein the first node “receives a first current and a second current,” as claimed.

78. Accordingly, Petitioner has failed to show a reasonable likelihood that FIG. 5 or FIG. 8 of Marques show this limitation.

4. Marques Does Not Disclose a Second Inductor Coil Coupled to the First Node and a Third Node

79. Petitioner identifies inductor coil 10E of annotated FIG. 5 of Marques as a second inductor coil coupled to the first node and a third node. (Pet. at 11-13.) However, as noted above, the inductive structure shown in FIG. 5 of Marques lacks a first node that receives a first current and second current. The fictitious first node proposed by Petitioner receives only a single current, I , and therefore does not qualify as a first node that receives a first current and a second current. Therefore, it is my opinion that Marques does not disclose a second inductor coil coupled to the first node and a third node, wherein the first node receives a first current and a second current.

80. With respect to annotated FIG. 8 of Marques, as noted previously, Petitioner fails to identify a third node in the figure. Regardless, the terminal 20 identified as the first node by Petitioner has not been shown to receive a first

current and a second current. On the contrary, first and second currents I_1 and I_2 are shown flowing from the terminal 20. Therefore, it is my opinion that Marques does not disclose a second inductor coil coupled to the first node and a third node, wherein the first node receives a first current and a second current.

81. Accordingly, it is my opinion that FIG. 5 or FIG. 8 of Marques do not show this limitation.

5. Marques's Inductive Structure Would Not Operate Like the Claimed Invention Even If First and Second Currents Are Received at the Fictitious First Node

82. I have been asked to assume for the sake of argument that Marques's inductive structure included a first node between the coils that received first and second currents (which there isn't). In such case, it's my opinion that such an inductive structure would not operate as claimed. To demonstrate this point, I prepared an annotated version of Marques's Figure 5 (see below) in which a fictitious common (first) node is positioned between the coils as proposed by Petitioner, and first, second, and third nodes are connected to a circuit so that the fictitious first node receives first and second currents I_1 and I_2 as claimed.

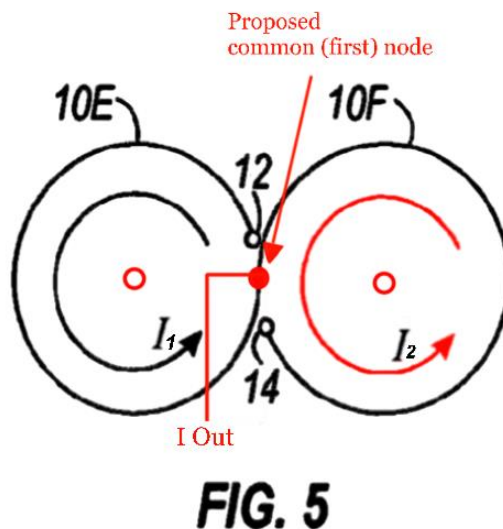


Figure 5 of Marques (Annotated)

83. The first current I_1 flows in a counterclockwise direction from node 12 to the fictitious (first) node, and the second current I_2 flows in a counterclockwise direction from node 14 to the fictitious (first) node. Applying the right-hand rule, both currents generate an electromagnetic field oriented out of the plane (denoted by the small red circles at the centers of the coils), because they are both flowing in a counterclockwise direction. Because the electromagnetic fields generated by the coils have the same orientation, the inductive structure cannot meet the limitations in claim 1 of “a second magnetic field having an opposing orientation to the first magnetic field” and “the first magnetic field and the second magnetic field at least partially cancel at an interference point.” On the contrary, because the

electromagnetic fields generated by Marques's coils would have the same orientation, the first and second magnetic fields would tend to reinforce each other. For this additional reason, it is my opinion that Marques does not anticipate claim 1.

C. The Combination of Lee and Marques Does Not Disclose the Features of Claim 11

84. In my opinion, the combination of Lee and Marques does not disclose all of the features of claim 11.

1. Lee Teaches Away From The Proposed Combination

85. In my opinion, there would have been no motivation to combine the inductor structures of Marques in the differential low noise amplifier of Lee because Lee teaches away from such a combination. That is, Petitioner alleges that the inductor structures of Marques include a first inductor that communicates a first current in a counterclockwise direction and a second inductor that communicate a second current in a clockwise direction (i.e., the first and second inductors are laid out with an "opposite" or "mirrored" orientation) (Pet. at 41-44), whereas Lee teaches "[a]nother important attribute of the differential connection is, of course, its ability to reject common-mode disturbances," and "[t]o ensure the truth of this statement [regarding the circuit's ability to reject common-mode disturbances], the spiral inductors of both half-circuits should be laid out with the

same orientation, not mirrored; otherwise, inductively coupled noise will not appear as a common-mode signal.” (Ex. 1007 at 6 (p. 388, 388 n.21)). Lee goes on further to state “[t]o maximize common-mode rejection at high frequencies, it is critically important for the layout to be absolutely as symmetrical as possible.” (*Id.*) These statements in Lee teaching away from the proposed combination are yet another reason why it is my opinion that claims 11-16 would not have been obvious over Marques and Lee.

2. The Combination of Lee and Marques Does Not Disclose the Features of Claim 11

86. Even if Lee is considered to be prior art, and even if there were motivation to combine the inductor structures of Marques in the differential low noise amplifier of Lee (which there is not), it is my opinion that the resulting combination would not read on claims 11-16. Petitioner states several times that a POSITA would have been motivated “to combine” the inductor structure of Marques in the DLNA of Lee (Pet. at 40, 41, and 43), but fails to explain how they are combined. More specifically, Petitioner notes that Lee discloses, in annotated Figure 12.10 (reproduced below), “a first inductor coil coupled to the voltage source (VDD) and to a first transistor” (Pet. at 41) and “a second inductor coil coupled to the voltage source (VDD), a second transistor, and in parallel with the

first inductor coil” (Pet. at 42).

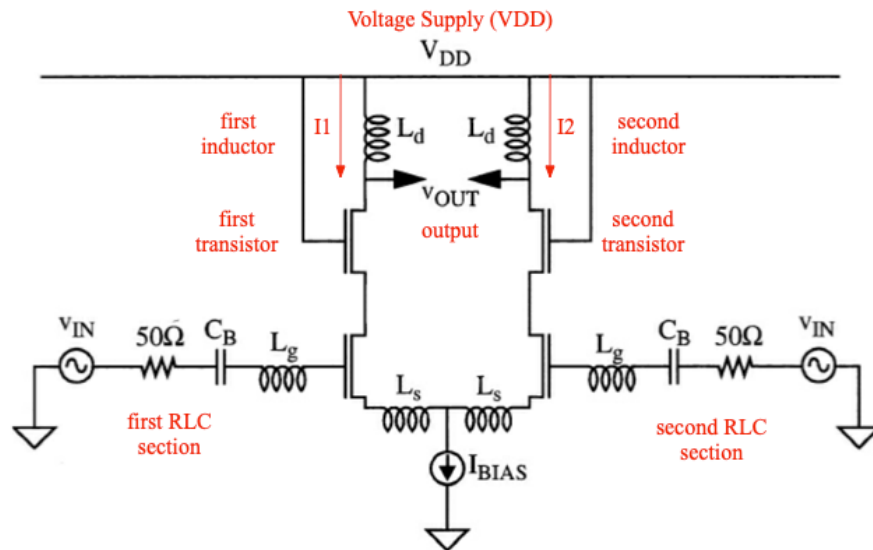


FIGURE 12.10. Differential LNA (simplified).

87. At the same time, Petitioner notes that Marques, in annotated Figure 7 (reproduced below) discloses “a first inductor 16 that communicates a first current I_1 in a first direction (shown here as counterclockwise)” (Pet. at 41), where the first inductor is “in parallel with a second conductor 18 [and] where the second inductor 18 communicates a second current I_2 in a second direction (shown here as clockwise)” (Pet. at 42).

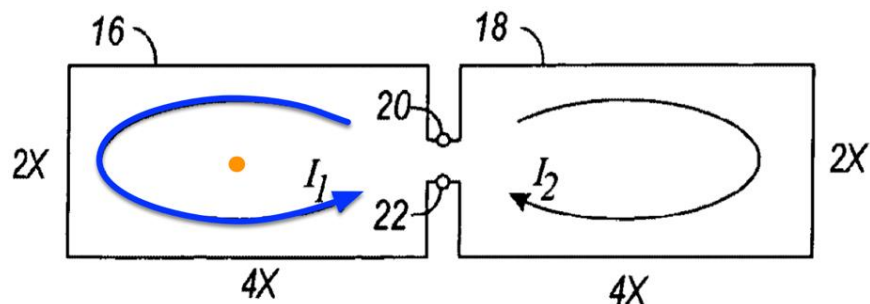


FIG. 7

88. Nowhere in Ground 3 does Petitioner explain how the two terminal (20, 22) inductor structure of Marques shown in annotated FIG. 7 is combined with the DLNA of Lee. For example, Petitioner doesn't explain whether the inductor structure of Marques is substituted for an inductor in the DLNA of Lee, or whether the inductor structure of Marques is split apart into separate inductors that are substituted for inductors in the DLNA, or whether it is combined in some other way. Nor does Petitioner provide any evidence that a POSITA would combine the inductor structure of Marques in the DLNA in any particular way or that there would have been a reasonable expectation of success (which is relevant given Lee's statements teaching away from such a combination).

D. Menegoli Does Not Disclose the Features of Claim 1

89. In my opinion, Menegoli does not disclose all of the features of claim 1.

1. Menegoli Does Not Disclose A Multiple Inductor Array With Three Nodes

90. None of the inductor devices Menegoli discloses include three nodes. To the contrary, every inductor device disclosed in Menegoli consists of only two nodes—i.e., the terminal ends of the inductor devices L2, L3, L4, and L5 shown in the figures—so that each of the inductor devices may be used in place of a conventional two-terminal inductor (such as the two terminal inductor L1 depicted in FIG. 1 of Menegoli) in a circuit where an inductance is required. (*See generally* Ex. 1008.) That is, just like a conventional two-terminal inductor, each inductive device in Menegoli is designed to be connected in a circuit via two terminals. There is no disclosure in Menegoli of there being an extra node to connect the inductor devices in a circuit

91. The inductor devices of Menegoli are two-terminal devices because they are intended to solve a problem with conventional inductors wherein the “[i]nductor creates large undesired magnetic fields” (Ex. 1008 at 2:7-16), and that “[t]he coupling of the magnetic field of a printed wiring inductor to nearby circuitry due to stray magnetic fields can be minimized by the invention” (*Id.* at 3:12-15). By utilizing two terminals, the same current passes through all of the inductors in the inductor device, so that the two generated magnetic fields can be

coupled to each other. (*Id.* at 7:26-29.) Improved coupling of the inductors in the inductor device lowers the radiated magnetic energy that can result in undesirable coupling with nearby circuitry. (*Id.* at 7:34-35; *see also id.* at 3:60-63, 5:23-26, 5:34-42, 5:52-56, 8:29-33, 9:4-9, 9:18-20, and 9:35-39.) Because the inductor devices in Menegoli are two terminal devices, the currents across the inductors are not individually adjustable, so the inductive devices of Menegoli are not able to address a change in mutual inductance in one inductor caused by a transient change in current in the other inductor.

92. The Petition relies on annotated versions of FIG. 2A of Menegoli (reproduced below), in which the Petitioner added an extra “node” to the inductor device L2 between the terminal ends (identified in the Petition as second and third nodes, respectively) to create three nodes where only two exist. (*Compare* Ex. 1008 FIG. 2A with Pet. at 54 and 56.) However, as noted above, the inductor devices in Menegoli (including the inductor device L2 in FIG. 2A) are meant to replace conventional two-terminal inductors to reduce interference with nearby circuitry and are therefore connected in a circuit using the terminal ends of the device (labeled as second and third nodes in Petitioner’s annotated version of FIG. 2A). There is no disclosure in Menegoli of connecting the inductor devices in a circuit using the fictitious extra “node” added to FIG. 2A by Petitioner. For this

reason alone, it is my opinion that Menegoli does not disclose a multiple inductor array with three nodes as claimed.

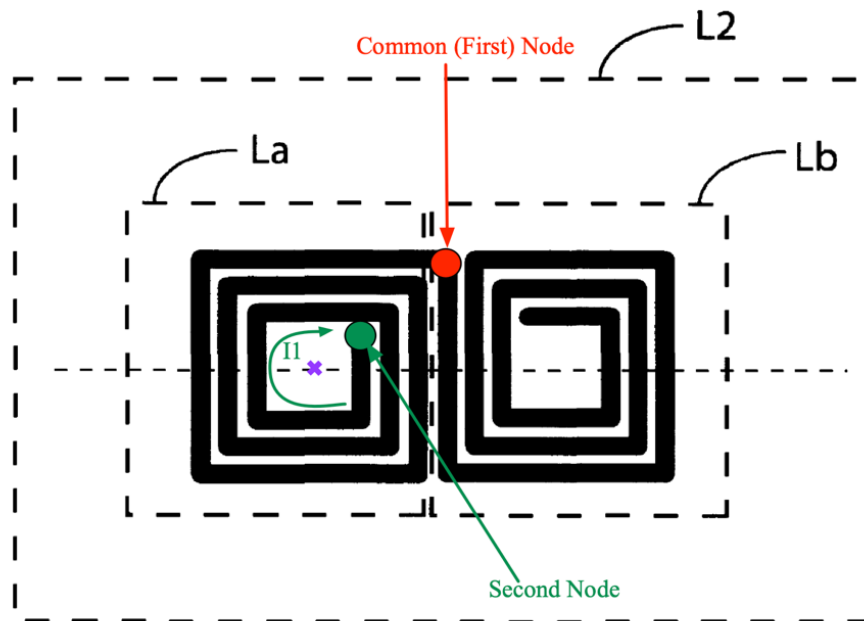


FIG.2A

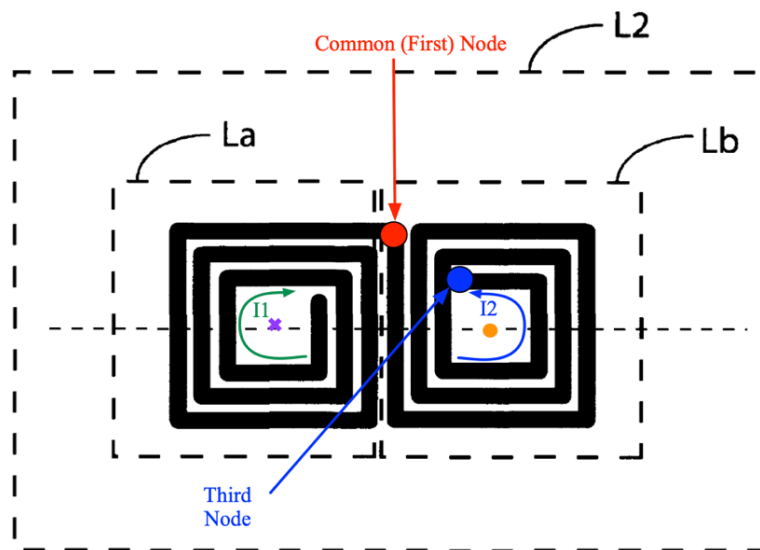


FIG.2A

Annotated Versions of FIG. 2A of Menegoli, Pet. at 54 and 56.

93. Menegoli describes Figure 2A as follows:

The two conductors . . . are electrically connected to each other to form one single inductive element constituted by the series of the two spiral inductors. Namely, the inductor device L2 comprises the paired two spiral formed interconnection structures La and Lb. The current is flowing in the two square spiral conductors in opposite direction. If the current is flowing clockwise in one spiral inductor La then it flows counter-clockwise into the spiral inductor Lb such that the two generated magnetic fields can be coupled to each other.

(Ex. 1008 at 8:13-23.) The fact that the same current is described as flowing through the two spiral conductors confirms that only two terminals are present. So, even assuming Menegoli discloses a multiple inductor array with three nodes (which it doesn't), Petitioner's three nodes, *i.e.*, Petitioner's fictional "common node" and the terminal ends of the inductor device L2, etc., do not operate in accordance with the language of claim 1.

2. Petitioner's "First Node" Does Not Receive a First Current and a Second Current

94. As noted above, claim 1 calls for a first node that "receives a first current and a second current." The made-up "common node" in Petitioner's annotated FIG. 2A of Menegoli, which Petitioner identifies as the claimed "first node" (*e.g.*, Pet. at 52-53), does not receive a first current and a second current, as

required by the claim language.

95. As noted above, the inductive device in FIG. 2A of Menegoli is shown and described as “one single inductive element constituted by the series of the two spiral inductors.” (Ex. 1008 at 8:13-23.) Because the two spiral inductors La and Lb are arranged in series, by definition the same current must flow through the two spiral inductors La and Lb.

96. In Petitioner’s annotated FIG. 2A, the fictitious common node is positioned between terminal ends of the device and will therefore receive only a single current—the same current that flows through the two spiral inductors La and Lb. Nevertheless, Petitioner asserts that “[t]he (common) first node . . . can be viewed as the point where I1 and I2 meet (i.e., the first node receives a first and second current).” (Pet. at 52.) But there is no disclosure in Menegoli of separate currents, I1 and I2, in the embodiment of FIG. 2A. There is only a single current disclosed. Petitioner re-names the single current as I1 when it travels through the first spiral inductor La and re-names the same current as I2 when it travels through the second spiral inductor Lb. (*E.g.*, Pet. at 53). The separate currents I1 and I2 in Petitioner’s annotated version of FIG. 2A are thus fictitious, like its common node. Moreover, even if Menegoli does disclose separate currents, I1 and I2 (which it does not), an examination of the direction of current flow in annotated FIG. 2A

reveals that only I1 would be received at the fictitious common node proposed by the Petitioner, while the fictitious current I2 would flow from the fictitious common node.

97. Thus, it is my opinion that Menegoli does not disclose a multiple inductor array in which a first of three nodes receives first and second currents.

3. Menegoli Does Not Disclose a First Inductor Coil Coupled to the First Node and a Second Node

98. Petitioner identifies spiral inductor La of annotated FIG. 2A of Menegoli as a first inductor coil coupled to the first node and a second node. (Pet. at 53-55.) However, as noted above, the inductive device L2 in FIG. 2A of Menegoli lacks a first node that receives a first current and second current. The fictitious first node proposed by Petitioner receives a single current, and therefore does not qualify as a first node that receives a first current and a second current. Therefore, it is my opinion that Menegoli does not disclose a first inductor coil coupled to the first node and a second node, wherein the first node receives a first current and a second current.

99. Accordingly, it is my opinion that FIG. 2A of Menegoli does not show this limitation.

4. Menegoli Does Not Disclose a Second Inductor Coil Coupled to the First Node and a Third Node

100. Petitioner identifies spiral inductor Lb of annotated FIG. 2A of Menegoli as a second inductor coil coupled to the first node and a third node. (Pet. at 55-57.) However, as noted above, the inductive device L2 shown in FIG. 2A of Menegoli lacks a first node that receives a first current and a second current. The fictitious first node proposed by Petitioner receives a single current, and therefore does not qualify as a first node that receives a first current and a second current. Therefore, it is my opinion that Menegoli does not disclose a second inductor coil coupled to the first node and a third node, wherein the first node receives a first current and a second current.

101. Accordingly, it is my opinion that FIG. 2A of Menegoli does not show this limitation.

5. Menegoli's Inductive Structure Would Not Operate Like the Claimed Invention Even If First and Second Currents Are Received at the Fictitious First Node

102. I have been asked to assume for the sake of argument that Menegoli's inductive structure included a first node between the coils that received first and second currents (even though there isn't). In my opinion, such an inductive structure would not operate as claimed. To demonstrate this point, an annotated version of Menegoli's Figure 2A is provided (see below) in which a fictitious common (first) node is positioned between the coils as proposed by Petitioner, and

first, second, and third nodes are connected to a circuit so that the fictitious first node receives first and second currents I_1 and I_2 as claimed.

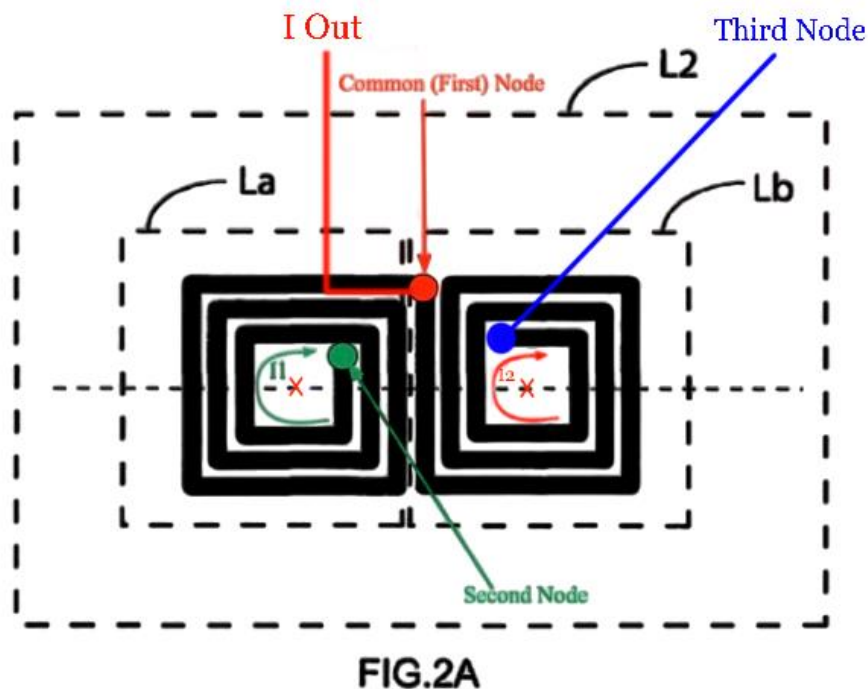


Figure 2A of Menegoli (Ex. 1008) (Re-annotated)

103. The first current I_1 flows in a clockwise direction from the second node to the fictitious (first) node, and the second current I_2 flows in a clockwise direction from the third node to the fictitious (first) node. Applying the right-hand rule, both currents generate an electromagnetic field oriented into the plane (denoted by the small red X's at the centers of the coils), because they are both flowing in a clockwise direction. Because the electromagnetic fields generated by

the coils have the same orientation, the inductive structure cannot meet the limitations in claim 1 of “a second magnetic field having an opposing orientation to the first magnetic field” and “the first magnetic field and the second magnetic field at least partially cancel at an interference point.” On the contrary, because the electromagnetic fields generated by Menegoli’s coils would have the same orientation, the first and second magnetic fields would tend to reinforce each other. For this additional reason, it is my opinion that Menegoli would not have anticipated claim 1.

104. I reserve the right to revise, supplement, and/or amend my opinions in this declaration based on future positions taken by Petitioner and/or their experts, additional documents, testimony, or other information provided by Petitioner or its witnesses, any orders from the Court, or as I may otherwise find necessary and to offer rebuttal analyses and/or opinions to any such positions of the Petitioner.

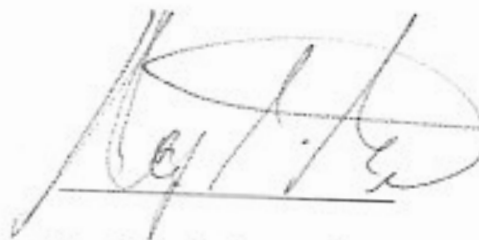
105. I expect to continue to develop my opinions discussed in this report. I also reserve the right to supplement my opinions based on information obtained from additional discovery or from Petitioner’s experts, as indicated above.

106. When called upon to do so, I will offer testimony at trial or otherwise regarding these opinions and will offer rebuttal testimony as appropriate throughout the remainder of this proceeding.

107. I currently hold the opinions expressed in this declaration, but my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

108. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code.

Dated: February 20, 2024

A handwritten signature in black ink, appearing to be 'J. Bernstein', written over a horizontal line.

Dr. Joseph Bernstein

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Professional Summary

Professor Bernstein's expertise lie in several areas of micro-electronic devices, packaging and system reliability, including failure analysis, process variations and reliability prediction. He is a world recognized expert in GaN and SiC power device reliability and on advanced electronic packaging. He has worked directly with companies producing DRAM and SDRAM, SRAM and Flash memory. He has worked also with MEMS and laser programmable metal interconnect. Included in electronic systems are Power Electronic devices, flip-chip devices, packaging and physics of failure research including memory devices, gate oxide integrity and radiation effects. He has licensed his own technology and consulted for RFID, Flash, and other memory related companies including Sandisk, Cypress and Freescale. He directs the Laboratory for Failure Analysis and Reliability of Electronic Systems, teaches VLSI design courses and heads the VLSI program at Ariel University. His Laboratory is a center of research activity dedicated to serving the needs of manufacturers of highly reliable electronic packaging and systems using commercially available off the shelf parts. Research areas include thermal, mechanical, and electrical interactions of failure mechanisms of ultra-thin gate dielectrics, Non-Volatile memory, advanced metallization and power devices. He also works extensively with the semiconductor industry on projects relating to failure analysis, defect avoidance, programmable interconnect used in Field Programmable Gate Arrays and repair in microelectronic circuits and packaging. He has developed an important method for predicting device failure rates based on new JEDEC standards for multiple failure rate-based prediction. Professor Bernstein was a Fulbright Senior Researcher/Lecturer at Tel Aviv University in the Department of Electrical Engineering, Honored lecturer at "Nanorun," and at IEEE Summer-School in Toulouse, France. Professor Bernstein is a senior member of IEEE.

Expertise

- Microelectronics and Electronic Device and System Design and Reliability
- Power Electronics Devices and Architecture
- Advanced Packaging of Electronic Devices
- SiC and GaN Power Device Reliability
- DRAM, SDRAM, SRAM & Flash (NAND and NOR) Memory Cells
- Electronics Lifetime Prediction
- Failure Analysis of Electronic Circuits
- Fuse Processing for Redundancy and Memory Repair
- Gate Oxide Integrity of in Ultra-Thin Gate Dielectrics
- Hot Carrier Degradation of Nanometer Scale Devices
- Processing of Semiconductor Devices and Wafers and Packaging (Ball Grid Array).
- Materials Processing for Advanced Semiconductor Devices
- Materials Processing for MEMS Applications
- Multiple Failure Rate Modeling and Lifetime Prediction
- Programmable Gate array architecture, layout and redundancy
- Semiconductor Device Processing Materials and Technologies
- Thermal Fatigue of Electronic Circuit Boards
- GaN Power Semiconductor Devices

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Education

<u>Year</u>	<u>College or University</u>	<u>Degree</u>
1990	Massachusetts Institute of Technology	Ph.D., Electrical Engineering and Computer Science, GPA: 5.0/5.0
1987	Massachusetts Institute of Technology	E.E., Electrical Engineer, GPA: 5.0/5.0
1986	Massachusetts Institute of Technology	M.S., Electrical Engineering and Computer Science, GPA: 5.0/5.0
1984	Union College, Schenectady, NY	B.S., Electrical Engineering, GPA: 3.9/4.0 Summa Cum Laude

Professional Experience

From:	2012
To:	Present
Organization:	Ariel University, Israel
Title:	Professor, Faculty of Engineering
From:	2009
To:	Present
Organization:	Reliability International Associates LLC, Reliability consulting company
Title:	Founder and Owner
From:	2007
To:	2012
Organization:	Bar Ilan University, Israel
Title:	Professor, Faculty of Engineering
From:	2003
To:	2005
Organization:	Tel-Aviv University, Israel
Summary:	
2003 – 2005	Visiting Associate Professor of Engineering, Faculty of Engineering
2004 – 2005	Fulbright Senior Scholar
From:	1995
To:	2008
Organization:	University of Maryland

Joseph B. Bernstein, Ph.D. Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Summary:

2001 – 2007 Associate Professor, Mechanical Engineering
1995 – 2001 Assistant Professor of Reliability, Materials and Nuclear Engineering Dept.
Summer 1998 NASA/ASEE Summer Faculty Research Fellow, JPL, Pasadena, CA.

From: 2002
To: 2006
Organization: LaserLink Technology, LLC (Maryland based)
Title: Owner

From: 1995
To: 1997
Organization: Lightspeed Semiconductor, Inc.
Title: Founder and Chief Scientist

From: 1991
To: 1993
Organization: Boston University
Title: Adjunct Professor

From: 1990
To: 1995
Organization: MIT Lincoln Library, Lexington, MA
Title: Research Staff

Litigation Support Experience

Expert Engagement:

Type of Matter: Jury Trial for Trade Secret Violation under and NDA
Law Firm: Bejin Bieneman PLC | 2000 Town Center, Suite 800 |
Southfield, MI 48075 313-528-4882 | www.b2iplaw.com
Case Name: **MERSEN USA EP CORP., v. TDK ELECTRONICS INC.**
UNITED STATES DISTRICT COURT
SOUTHERN DISTRICT OF NEW YORK Case No. 21-cv-00763
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and
testimony for the plaintiff, Mersen USA
Disposition: Settled highly favorably for the Plaintiff!
Date: 2023

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Expert Engagement:

Type of Matter: Jury Trial for Reliability fraud
Law Firm: ORRICK HERRINGTON & SUTCLIFFE
405 Howard Street San Francisco, California 94105-2675
Case Name: **Allied Telesis K.K. v. Micron Technology, Inc.**
Santa Clara County, CA Case No. 2015-1-CV-282977
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and testimony for the defendant, Micron Technology, Inc.
Disposition: Settled favorably for the Defendant
Date: 2021-2022

Expert Engagement:

Type of Matter: Due-Diligence Consulting and Patent Analysis
Law Support Firm: Papst Licensing GmbH, Germany and Detroit
Case Name: Trolling software development
Services Provided: Engaged as Expert providing consulting and analysis of a portfolio of IBM patents in order to validate a developing software and provide due-diligence support.
Disposition: Found none of hundreds of patents useful to pursue.
Date: 2021-2022

Expert Engagement:

Type of Matter: Inter-Parte Review defending patent owner.
Law Firm: SKIERMONT DERBY LLP
Case Name: ADVANCED SEMICONDUCTOR ENGINEERING, INC., PETITIONER,
V. BELL SEMICONDUCTOR LLC, PATENT OWNER.
Case No. IPR2021-00180, U.S. Patent No. 6,624,007
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and testimony.
Disposition: Patent was found unpatentable.
Date: 2021-2022

Expert Engagement:

Type of Matter: Inter-Parte Review defending patent owner.
Law Firm: Mishcon De Reya New York, LLP
Case Name: RPX CORPORATION and AMD, INC. vs. IYM Technologies, LLC.
IPR2017-01886 and 88
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and testimony.
Patent was found unpatentable.
2018

Expert Engagement:

Type of Matter: Patent Infringement defending patent owner.
Law Firm: Lowenstein and Weatherwax, LLP
Case Name: KINGSTON Technology v. POLARIS Innovations
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and testimony.

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Disposition: 01623 resolved as NOT un-patentable.
Date: 2017

Expert Engagement:

Type of Matter: Patent Infringement defending patent owner.
Law Firm: TENSEGRITY LAW GROUP, LLP
Case Name: KINGSTON Technology v. POLARIS Innovations
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and testimony.
Disposition: Case was dropped after IPR results
Date: 2017

Expert Engagement:

Type of Matter: Patent Infringement defending patent owner.
Law Firm: DLA Piper
Case Name: MIPOX Corp. v. International Test Solutions, Inc. Inter Partes Reviews of US patents 8,801,869; 7,202,683; and 6,777,966
Services Provided: Engaged as Expert providing expert reports, expert analysis and testimony.
Disposition: Brought to successful settlement and non-institution of necessary claims.
Date: 2017

Expert Engagement:

Type of Matter: Patent Infringement and validity
Law Firm: Dowling Aaron Incorporated
Case Name: *Beco Dairy Automation, Inc. v. Global Tech Systems, Inc.* (Eastern District of California; 1:12-cv-01310-LJO-SMS)
Services Provided: Engaged as Expert providing expert reports, expert circuit analysis and testimony, Claim chart construction and expert testimony covering 8 patents
Disposition: Brought to successful and beneficial settlement
Date: 2016

Expert Engagement:

Type of Matter: Patent Infringement
Law Firm: Nix Patterson, LLP
Case Name: DSS Technology Management, LLC v. Intel Corp., Hynix, Samsung.
Services Provided: Engaged as Expert providing expert reports, expert circuit analysis and testimony.
Disposition: Client pulled out after institution at IPR
Date: 2015

Expert Engagement:

Type of Matter: Patent Infringement
Law Firm: Desmarais, LLP
Case Name: Round Rock Research, LLC v. ACER, INC., and Gateway, Inc.,
Services Provided: Engaged as Expert providing expert reports, expert circuit analysis and testimony, these cases successfully, were settled out of court.
Disposition: Settled
Date: 2014

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Expert Engagement:

Type of Matter: Patent Interference
Law Firm: Oblong, Spivak, McClelland, Maier, & Neustadt, PC, for Defendant
Case Name: Yunlong Sun, Edward J. Swenson and Richard S. Harris v. Donald V. Smart
Services Provided: Engaged as Expert for over 6 years supporting patent interferences cases involving laser processing in semiconductor devices. Numerous expert reports and depositions as well as interviews at the patent office and testimony.
Disposition: Company was purchased by the competition.
Date: 2008-2012

Expert Engagement:

Type of Matter: Patent Re-Examination
Law Firm: Law Office of Andrew D. Fortney
Case Name: MIT/UMD appeal to USPTO
Services Provided: Engaged as Expert writing expert testimony in defense of a patent in the semiconductor field
Disposition: Successful defense of patent
Date: 2012

Expert Engagement:

Type of Matter: Patent Infringement
Law Firm: Townsend Townsend and Crew, LLC
Case Name: Agere v. Samsung
Services Provided: Engaged as Expert providing expert reports and testimony, the case was successfully settled out of court.
Disposition: Settled
Date: 2006

Expert Engagement:

Type of Matter: Patent Infringement
Law Firm: Brown & Bain, PA, for Defendant
Case Name: EMI Group North America, Inc. v. Cypress Semiconductor Corporation
Services Provided: Engaged as Expert over 3 years providing numerous expert reports and trial testimony defending the company's use of technology in alleged violation of a patent, which we proved in court to have been invalid.
Disposition: We defeated the patent at trial and sustained on appeal
Date: 2001, 2003

Expert Engagement:

Type of Matter: Patent Infringement
Law Firm: Choate Hall & Stewart
Case Name: GSI v. A-B Lasers
Services Provided: Engaged as Expert providing hands-on consulting, expert testimony and reports relating to laser processing of silicon wafers for marking technology.
Disposition: Settled
Date: 2001

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Industrial Consultation and Involvement

Consulting Project:

Client: EPC Corporation
Services Provided: GaN Power Circuit Design, Evaluation and Qualification

Consulting Project:

Client: Sandisk
Services Provided: Test and Reliability Consultant.

Consulting Project:

Client: Maradin Corp.
Services Provided: Accelerated Reliability and Qualification Consulting.

Consulting Project:

Client: Camtek Corp.
Services Provided: Reliability Testing and Qualification Consulting.

Consulting Project:

Client: Essence Corp.
Services Provided: Test and Reliability Consultant providing device lifetime characterization.

Consulting Project:

Client: Marvel Corp.
Services Provided: Test and Reliability Consultant providing important device lifetime characterization.

Consulting Project:

Client: Veraz Telecommunication
Services Provided: System Reliability Consultant providing models and accelerated tests

Consulting Project:

Client: Israel Aircraft Industries
Services Provided: Lecturer and Consultant

Consulting Project:

Client: Cypress Semiconductor
Services Provided: Laser processing consultation and trial expert witness

Consulting Project:

Client: Teradyne Corporation
Services Provided: Device and system reliability consultant

Consulting Project:

Client: Freescale Semiconductor
Services Provided: Device qualification and reliability testing and modeling

Consulting Project:

Client: GSI Lumonics
Services Provided: Improving laser cut and link technologies and expert witness

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Professional Affiliations, Achievements & Awards

Laboratory and Programmatic Affiliations

- Laboratory for Reliability of Advanced Microelectronic Systems, Ariel University – current head
- Laboratory for Reliable Electronic Systems at Ariel University, in collaboration with Israeli industry consortium and Bar Ilan University. (2007-2012).
- Founder and Faculty Advisor: Israel Electronics Manufacturers Working Group on Reliability, ILTAM. (2005-present).
- Assoc. Director, University Research Institute for Nanoscience and Nanotechnology at Tel-Aviv University. (2003-2005).

Awards and Honors

- Expert Panelist and Invited Lecturer for GaN and SiC Power MOSFET, ISTFA 2023
- Excellence in Teaching Award, Ariel University 2021
- 32nd MIEL Serbia, Best Paper Award, 2021
- Tech-Connect Innovation Award 2018 (Through Ariel Scientific Innovations)
- Nanorun, distinguished lecturer and contributor, IRT-Saint Exupery, Feb. 2016
- Windows on Science researcher/lecturer, US Air Force, March 2015
- ChipEx 2014, best paper/lecturer award 2014
- Fulbright Senior Researcher. Lecturer, 2004 – 2005
- IEEE Senior Member, 2003

Teaching and Advising

- Courses Taught in the Last 5 Years
 - Reliability Prediction based on Multiple Accelerated Life Tests – Hobbs, IEEE, NASA, STMicro
 - Why Weibull, Why Not! – Hobbs, IEEE Summer School, Toulouse
 - VLSI Design – Ariel University (Advanced Undergraduate)
 - Reliability Engineering Fundamentals - Ariel University
 - Microelectronics Device Reliability – Ariel University
 - VLSI Analog (1 semester) and Digital VLSI (1 semester) Laboratories – Ariel University

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

<u>Project Title</u>	<u>Organization</u>	<u>PI or Co-PI</u>	<u>Funding Amount</u>	<u>Year</u>
Reliability of V-GaN	US ONR	PI	\$400,000	2023-2026
Microwave GaN Rel	MAFAT (Isr.)	PI	\$60,000	2023-2024
Power SOC	Israel Innov.	PI/2	\$400,000	2022-2025
Gate Drive for SiC	US ONR	PI/2	\$450,000	2021-2024
DSM/WBG Reliability	IRT Saint-Exupery	PI	\$200,000	2018-2020
GaN Class-D Amplifier	Kamin Israel	PI/2	\$200,000	2019-2021
GaN Microwave Device	Israel DOD	PI	\$150,000	2018-2022
GaN Device Reliability	ONR	PI	\$500,000	2015-2019
Wide Bandgap Device	AFOSR	PI	\$135,000	2015-2018
FPGA Reliability	USAF	PI	\$150,000	2014-2015
System Reliability	Magnetron Israel	PI	\$100,000	2012-2013
Power Electronic System Reliability	ONR	PI	\$200,000	2010-2011
Systems Reliability in Nanotechnology	ONR	PI	\$200,000	2009-2010
Methods to Account for Early Wear-out	AVSI consortium	PI	\$286,000	2007 - 2010
MIL HDBK 217 Replacement	Wyle Labs	PI	\$86,608	2007
Advanced Gate Dielectric Reliability	NIST	PI	\$69,965 (1st year)	2006-2009
JPL NASA Research Program	JPL	PI	\$65,000	2006-2007
Microelectronic Systems Reliability	AVSI (Aerospace Corporations)	PI	\$180,000 (5th year)	2006
Ultra Thin Dielectric Metrology	NIST	PI	\$56,000	2005
Microelectronic Systems Reliability	AVSI (Aerospace Corporations)	PI	\$210,000 (4th year)	2005
EDCOT Research Consortium	MAGNET (Tel-Aviv Univ.)	Co-PI (50%)	\$100,000	2004-2005
Laser programmable device design	NSA	PI	\$50,000	2004-2005
Microelectronic Systems Reliability	AVSI (Aerospace Corporations)	PI	\$157,000 (3rd year)	2004
Power Device Reliability	ONR	Co-PI (60%)	\$150,000 per year	2004-2008
Microelectronic Systems Reliability	AVSI (Aerospace Corporations)	PI	\$198,000 (2nd year)	2003
Laser programmable device design	NSA	PI	\$50,000	2002-2003
Place and Route for LPAA	Mission Research Corporation	PI	\$198,000	2002-2003
Laser MAKELINK development	MIPS (Matrics Corporation)	PI	\$77,000	2001-2002
Alternate Gate Dielectric Analysis	NIST	PI	\$150,000	2001-2005
Microelectronic Systems Reliability	AVSI (Aerospace Corporations)	PI	\$175,000 (1st year)	2002

Joseph B. Bernstein, Ph.D. Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Design and Layout of LPGA: Phase I.	BAE Systems Co.	PI	\$43,070	2000-2001
Wide band-gap power device reliability	ONR	Co-PI (50%)	\$314,804	2000 - 2003
Laser Process Development	DOD - NSA	PI	\$75,000	2000 - 2001
Thin Dielectric Metrology	NIST	PI	\$234,000	1999 - 2005
Laser Process Development	DOD - NSA	PI	\$146,680	1999 - 2000
Power Semiconductor	NIST	PI	\$42,300	1999 - 2000
Dielectric Metrology	NIST	PI	\$39,231	1999 - 2000
Laser Process Reliability	NASA / JPL	PI	\$54,080	1998
Metrology for Power Device Reliability	COMM - NIST	PI	\$6,000	1998
W Contact evaluation	DOD - NSA	PI	\$5,270	1998
Power Device Reliability	ONR	PI	\$150,000	1997 - 2000
Metal Cut Evaluation	General Scanning	PI	\$25,000	1997
Gate-Oxide Metrology	NIST	PI	\$124,330	1996 - 1999
Laser Restructuring / Evaluation	DOD - NSA	PI	\$200,000	1996 - 1997
Atomic Microscopy and Surface Science	NSA	Co-PI	\$122,810	1994 - 1997

Equipment Donated:

<u>Donated Item</u>	<u>Donating Agency</u>	<u>Value of Donation</u>
Cold/Hot Burn-In Ovens	Anonymous	\$200,000
Laser Timing Probe Microscope	Semicaps	\$3.5 Million
Laser Semiconductor Process Equipment	XRL Corporation	\$300,000
Laser Semiconductor Process Equipment	Electro Scientific Industries	\$700,000
Electromigration Test Equipment	Aetrium Corporation	\$150,000

Patents & Publications

<u>Patent</u>	<u>Date</u>	<u>Description</u>
US17626857	9/15/2022	Power converter suitable for high frequencies
US202063039002P	15/06/2020	Control circuit for ring oscillator-based power controller
US 10,746,781	18/08/2020	Ring oscillator test circuit
PCT/IL2016/050476	05/01/2017	Enhancement mode only ring oscillator test circuit
US2014/0052392	02/20/2014	Solder joint life measurement for prognostics
US2015/0039244	02/15/2015	Failure Rate Estimation from Multiple Mechanisms
6,541,868	04/01/2003	Interconnecting Conductive Links
6,057,221	05/02/2000	Laser-Induced Cutting of Metal Interconnect
5,920,727	07/06/1999	Technique for Producing Interconnecting Conductive Links
5,920,789	07/06/1999	Technique for Producing Interconnecting Conductive Links
5,861,325	01/19/1999	Technique for Producing Interconnecting Conductive Links
5,585,602	12/17/1996	Structure for Providing One or More Conductive Paths

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Publications

Book Authorship and Editorship

1. Joseph B. Bernstein, *Reliability Prediction from Burn-In Data Fit to Reliability Models*, Academic Press, 2014, ISBN: 978-0-12-800747-1
2. Joseph B. Bernstein et.al, *Physics-of-Failure Based Handbook of Microelectronic Systems*, Reliability Information Analysis Center, Utica, NY, 2008, ISBN-10: 1-933904-29-1.
3. Mark White, Joseph B. Bernstein, *Microelectronics Reliability: Physics-of-Failure Based Modeling and Lifetime Evaluation*, NASA JPL Publication, 2008.
4. Mark White, Joseph B. Bernstein, *Microelectronics Reliability Modeling and Lifetime Evaluation Handbook: Derating and Reliability Prediction Guidelines*, NASA JPL Publication, 2007.
5. Pecht, M., Bernstein, J.B., Searls, D., and Peckerar, M., *The Korean Electronics Industry*, CRC Press, 1997 and 2020
6. Hoang, H.H., Schutz, R., Bernstein, J.B., Vasquez, B., *Multi-level Interconnection: Issues that Impact Competitiveness*, Proceedings of SPIE 2090, 1993.

Book Chapters

1. Alain Bensoussan, Joseph B. Bernstein and Alain Bravix, Chapter 1, *Basic Reliability Tools for SHM Protocols*, in "Reliability and Physics-of-Healthy in Mechatronics, Volume 15 - Reliability of Multiphysical Systems Set." ISBN : 978-178-63-0881-8, November 2022.
2. Alain Bensoussan, Joseph B. Bernstein and Alain Bravix, Chapter 2, *Applied Engineering on Physics-of-Healthy and SHM of Microelectronic Equipment for Aeronautic, Space, Automotive and transport operations*, in "Reliability and Physics-of-Healthy in Mechatronics, Volume 15 - Reliability of Multiphysical Systems Set." ISBN : 978-178-63-0881-8, November 2022.
3. Joseph B. Bernstein, *Reliability Prediction Considering Multiple Failure Mechanisms*, Chapter in "System Reliability", INTECH Publication, 2017, ISBN 978-953-51-5532-4.
5. Bernstein, J.B., "Laser Link-Making," in *LIA Handbook of Laser Materials Processing*, Magnolia Publishing, 2001.
6. Stark, B., Bernstein, J.B., "Reliability Overview," *MEMS Reliability Assurance Guidelines for Space Applications*, NASA Publication, 1998.

Articles in Refereed Journals

1. A Chaturvedi, M Sarma, SK Chaturvedi, J Bernstein, "[Performance assessment and RUL prediction of power converters under the multiple components degradation](#)," *Microelectronics Reliability* Vol.144, (2023) pp. 144958
2. E Bender, JB Bernstein, DS Boning, "Mitigation of Thermal Stability Concerns in FinFET Devices," *Electronics* 11 (20), (2022) pp.3305
3. Clay Mayberry, Joseph Bernstein, "[Reliability and Survivability of Advanced Electronics Technologies](#)," AFRL Space Vehicles Directorate, (2022) 3/1

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

4. E Bender, JB Bernstein, "Microchip Health Monitoring System Using the FLL Circuit," Sensors vol.7, (2021) pp.2285
5. E Bender, JB Bernstein, A Bensoussan, "Reliability prediction of FinFET FPGAs by MTOL," Microelectronics Reliability, vol.114, (2020) pp.113809
6. S. Shaheen, G. Golan, M. Azoulay, J. B. Bernstein, "A COMPARATIVE STUDY OF RELIABILITY FOR FINFET," Facta Universitatis, Series: Electronics and Energetics Vol. 31, No 3, September 2018, pp. 343-366
7. G. Golan, M. Azoulay, T. Avraham, I. Kremenetsky, J. B. Bernstein, "An improved reliability model for Si and GaN power FET," Microelectronics Reliability Vol. 81 pp. 77-89 (2018)
8. J. B. Bernstein, A. Bensoussan, E. Bender, "Reliability Prediction with MTOL," Microelectronics Reliability Vol. 68 pp. 91-97 (2017)
9. J. B. Bernstein, M. Gabbay, O. Delly, "Reliability matrix solution to multiple mechanism prediction," Microelectronics Reliability pp. 2951-2955 (2014).
10. Chung, Kuan-Jung, Martin Peckerar, and Joseph B. Bernstein. "Design Optimization of Laser-Induced Microbridges for Low Resistance Interline Connections in ICs." Microelectronic Engineering, Vol. 103, Pages 70-75 (2013).
11. I. Gershman and J. B. Bernstein, "Structural health monitoring of solder joints in QFN package," Microelectronics Reliability, Volume 52, Issue 12, Pages 3011-3016 (2012).
12. L. Yang and J. Bernstein, "Reliability Evaluation and Modeling of High Density Electronic Packages," Microelectronics International, vol. 29, no. 1, pp. 15-21 (2012).
13. I. Gershman and J. B. Bernstein, "Solder-Joint Quantitative Crack Analysis—Ohmic Resistance Approach," IEEE Transaction on Components, Packaging and Manufacturing Technology, vol. 2, no. 5, pp. 748 - 755 (2012).
14. L. Yang, R. Niu, J. Xie, B. Qian, B. Song, Q. Rong, J.B. Bernstein, "Design-for-reliability implementation in microelectronics packaging development," Microelectronics International, vol. 28, no. 1, pp. 29-40 (2011).
15. B. Huang, M. Rodriguez, M. Li, J.B. Bernstein, C.S. Smidts, "Hardware Error Likelihood Induced by the Operation of Software," IEEE Trans. on Reliability, vol. 60, no. 3, pp. 622-639 (2011).
16. Kuan-Jung Chung and J.B. Bernstein, "Experimental investigation of the optimal laser-induced microbridges," Precision Engineering, vol. 34, no. 3, pp. 578-585 (2010).
17. B. Yan, J. Qin, J. Dai, Q. Fan, and J.B. Bernstein, "Reliability Simulation and Circuit-Failure Analysis in Analog and Mixed-Signal Applications," IEEE Trans. on Device and Mat. Rel., vol. 9, no. 3, pp. 339-347 (2009).
18. M. Gurfinkel, P. Livshits, A. Rozen, J.B. Bernstein, "Local Oscillations of On-Die Supply Voltage-A Reliability Issue," IEEE Trans. on Device and Mat. Rel., vol. 9, no. 3, pp. 476-482 (2009).
19. L. Yang, Joseph B. Bernstein, T. Koschmieder, "Assessment of acceleration models used for BGA solder joint reliability studies," Microelectronics Reliability Vol. 49, pp. 1546-1554 (2009).
20. L. Yang, Joseph B. Bernstein, "Failure rate estimation of known failure mechanisms of electronic packages," Microelectronics Reliability Vol. 49, pp. 1563-1572 (2009).
21. X. Li, J. Qin, and J.B. Bernstein, "Compact Modeling of MOSFET Wearout Mechanisms for Circuit-Reliability Simulation," IEEE Trans. on Device and Mat. Rel., vol. 8, no. 1, pp. 98-121 (2008).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

22. M. Gurfinkel, H.D. Xiong, K.P. Cheung, J.S. Suehle, J.B. Bernstein, Y. Shapira, A.J. Lelis, D. Habersat, N. Goldsman, "Characterization of Transient Gate Oxide Trapping in SiC MOSFETs Using Fast I-V Techniques," IEEE Transactions on Electron Devices, vol. 55, no.8, pp. 2004-12 (2008).
23. L. Yang, J.B. Bernstein, "Reliability Study of High-Density EBGA Packages Using the Cu Metalized Silicon," IEEE Transaction on Components and Packaging Technology, vol. 31, no. 3, pp. 702-11 (2008).
24. M. Gurfinkel, J.C. Horst, J.S. Suehle, J.B. Bernstein, Y. Shapira, K.S. Matocha, G. Dunne, R.A. Beaupre, "Time-Dependent Dielectric Breakdown of 4H-SiC/SiO₂ MOS Capacitors," IEEE Trans. on Device and Mat. Rel., vol. 8, no. 4, pp. 635-641 (2008).
25. D. Heh, C.D. Young, G.A. Brown, P.Y. Hung, A. Diebold, E. Vogel, J.B. Bernstein, and G. Bersuker, "Spatial Distributions of Trapping Centers in HfO₂/SiO₂ Gate Stack," IEEE Transactions on Electron Devices, vol. 54, no.6, pp. 1338-45 (2007).
26. Joseph B. Bernstein, Moshe Gurfinkel, Xiaojun Li, Jörg Walters, Yoram Shapira and Michael Talmor, "Electronic circuit reliability modeling," Microelectronics Reliability, vol. 46, pp. 1957-1979 (2006).
27. Heh D, Young CD, Brown GA, Hung PY, Diebold A, Bersuker G, Vogel EM, Bernstein JB, "Spatial distributions of trapping centers in HfO₂/SiO₂ gate stacks," Applied Physics Letters, vol. 88, no.15, pp. 152907 (2006).
28. X. Li, J. Qin, B. Huang, X. Zhang, and J.B. Bernstein, "SRAM Circuit Failure Modeling and Reliability Simulation with SPICE," IEEE Trans. on Device and Mat. Rel., vol. 6, no. 2, pp.235-246 (2006).
29. X. Li, J. Qin, B. Huang, X. Zhang, and J.B. Bernstein, "A New SPICE Reliability Simulation Method for Deep Submicron VLSI Circuits," IEEE Trans. on Device and Mat. Rel., vol. 6, no. 2, pp. 247-257 (2006).
30. J.S. Suehle, B. Zhu, Y. Chen and J.B. Bernstein, "Detailed study and projection of hard breakdown evolution in ultra-thin gate oxides," Microelectronics Reliability, vol. 45, pp. 419-426 (2005).
31. J. Lee, W. Zhang, J.B Bernstein, "Analysis of Energy Process Window of Laser Metal Pad Cut Link Structure," IEEE Transactions on Semiconductor Manufacturing, vol. 16, no. 2, pp. 299-307 (2003).
32. L. Yang, C.K. King, J.B. Bernstein, "Liquid Dispensing Encapsulation in Semiconductor Packaging," Microelectronics International, vol. 20, no. 3, pp. 29-35 (2003).
33. D.W. Heh, E.M. Vogel, J.B. Bernstein, "Impact of Substrate Hot Hole Injection on Ultra-thin Silicon-dioxide Breakdown," Applied Physics Letters, vol. 82, no. 19, pp. 3242-3244 (2003).
34. J.S. Suehle, E.M. Vogel, P. Roitman, J.F. Conley Jr., A.H. Johnston, B. Wang, J.B. Bernstein, and C.E. Weintraub, "Observation of Latent Reliability Degradation in Ultra-Thin Oxides after Heavy-Ion Irradiation," Applied Physics letters, vol. 80, no. 7, pp. 1282-4 (18 Feb 2002).
35. E.M., Vogel, D. Heh, J.B. Bernstein, "Interaction between low-energy electrons and defects created by hot holes in ultrathin Silicon Dioxide," Applied Physics letters, vol. 80, no. 18, pp. 3343-5 (6 May 2002).
36. L.-S. Yang and J.B. Bernstein, "Encapsulation Process Development for Flexible-Circuit Based Chip Scale Packages," IEEE Trans. Electronics Packaging Manufacturing, vol. 25, no. 4, pp. 344-354 (October 2002).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

37. L.-S. Yang, J.B. Bernstein and K.C. Leong, "*Effect of the Plasma Cleaning Process on Plastic Ball Grid Array Package Assembly Reliability*," IEEE Trans. Electronics Packaging Manufacturing, vol. 25, no. 2, pp. 91-99 (April 2002).
38. E.M., Vogel, D. Heh, J.B. Bernstein, J.S. Suehle, "*Impact of the Trapping of Anode Holes in Silicon Dioxide Breakdown*," IEEE Electron Device Letters, vol. 23, no. 11, pp. 667-669 (November 2002).
39. Yang, L., Bernstein, J.B., Chung, K, "*The Impact of Lead-free Soldering on Electronics packages*," Microelectronics International, vol. 18, no. 3, pp. 20-26 (2001).
40. Wang, B., Suehle J.S., Vogel E.M., Bernstein, J.B., "*Time-Dependent Breakdown of Ultra-thin SiO₂ Gate Dielectrics under Pulsed Biased Stress*," IEEE Electron Device Letters, vol. 22, no. 5, pp. 224-226 (2001).
41. Zhang, W., J.-H. Lee, Bernstein, J.B., "*Energy Effect of the Laser Induced Vertical Metallic Link*," IEEE Transactions on Semiconductor Manufacturing, vol. 14, no. 2, pp. 163-169 (2001).
42. J.F. Conley Jr., J.S. Suehle, A.H. Johnston, B.Wang, T. Miyahara, E.M. Vogel, J.B. Bernstein, "*Heavy-Ion Induced soft breakdown of thin gate oxides*," IEEE Transactions on Nuclear Science, vol. 48, no. 6, pp. 1913-16 (Dec. 2001).
43. Shen, C.C., Hefner, A.R., Jr., Berning, D.W., Bernstein, J.B., "*Failure Dynamics of the IGBT During Turn-off For Unclamped Inductive Loading Conditions*," IEEE Transactions on Industry Applications, Vol. 36, no.2, pp.614-24 (2000).
44. Bernstein, J.B., Lee, J., Yang, G., Dahmas, T., "*Analysis of Laser Metal-Cut Energy Process Window*," IEEE Transactions on Semiconductor Manufacturing, vol.13, no. 2, pp. 228-34 (2000).
45. Vogel, E., Suehle, J.S., Edelstein, M.D., Wang, B., Chen, Y., Bernstein, J.B., "*Reliability of Ultra-thin Silicon Dioxide Under Combined Substrate Hot Electron and Constant Voltage Tunneling Stress*," IEEE Transactions on Electron Devices, vol. 47, no.6, pp.1183-91 (2000).
46. Lee, J., Zhang, W., Bernstein, J.B., "*Scalability Study of Laser-induced Vertical Make-link Structure*," IEEE Transactions on Semiconductor Manufacturing, vol. 13, no. 4, pp. 442-447 (2000).
47. Zhang, W., Lee, J.H., Chen, Y., Bernstein, J.B., Suehle, J.S., "*Reliability of laser-induced metallic vertical links*," IEEE Transactions on Advanced Packaging, vol. 22, no.4, pp. 614-19 (1999).
48. Bernstein, J.B., Hua, Y., Zhang, W., "*Laser energy limitation for buried metal cuts*," IEEE Electron Device Letters, vol. 19, no. 1, pp. 4-6 (1998).
49. Bernstein, J.B., Zhang, W., Nicholas, C.H., "*Laser formed metallic connections*," IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, vol. 21, no. 2, pp. 194-8 (1998).
50. Chen, Y., Suehle, J.S., Shen, C.C., Bernstein, J.B., Messick, C., Chaparala, P., "*A new technique for determining long-term TDDB acceleration parameters of thin gate oxides*," IEEE Electron Device Letters, vol. 19, no. 7, pp. 218-21 (1998).
51. Shen, Y-L, Suresh, S., Bernstein, J.B., "*Laser linking of metal interconnect: analysis and design considerations*," IEEE Transactions on Electron Devices, vol. 43, no. 3, pp. 402-10 (1996).
52. Rasera, R.L., Bernstein, J.B., "*Laser linking of metal interconnect: linking dynamics and failure analysis*," IEEE Transactions on Components, Packaging, and Manufacturing Technology, vol. 19, no. 4, pp. 554-61 (1996).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

53. Bernstein, J.B., Ventura, T.M., Radomski, A.T., "*Laser induced microfracture leading to high density metal-to-metal connections*," Proceedings of the SPIE, The International Society for Optical Engineering, vol. 2335, pp. 165-76 (1995).
54. Bernstein, J.B., Colella, B.D., "*Laser-formed metallic connections employing a lateral link structure*," IEEE Transaction on Components, Packaging, and Manufacturing Technology, Part A, vol. 18, no. 3, pp.690-2 (1995).
55. Bernstein, J.B., Ventura, T.M., Radomski, A.T., "*Laser induced microfracture leading to high density metal-to-metal connections*," Proceedings of the SPIE, The International Society for Optical Engineering, vol. 2335, pp. 165-76 (1995).
56. Bernstein, J.B., Colella, B.D., "*Laser-formed metallic connections employing a lateral link structure*," IEEE Transaction on Components, Packaging, and Manufacturing Technology, Part A, vol. 18, no. 3, pp.690-2 (1995).
57. Bernstein, J.B., Ventura, T.M., Radomski, A.I., "*High-density laser linking of metal interconnect*," IEEE Transactions on Components, Packaging and Manufacturing Technology, Part A, vol. 17, no.4, pp. 590-3 (1994).
58. Murguia, J.E., Bernstein, J.B., "*Short-time failure of metal interconnect caused by current pulses*," IEEE Electron Device Letters, vol. 14, no. 10, pp. 481-3 (1993).
59. Bernstein, J.B., "*Improvements to the Electrically Stimulated Acoustic Wave method for analyzing bulk space charge*," IEEE Transactions on Electrical Insulation, vol. 27, no.1, pp. 152-61 (1992).
60. Bernstein, J.B., Cohen, S.S., Wyatt, P.W., "*Metal wire cutting by repeated application of low-power laser pulses*," Review of Scientific Instruments, vol. 63, no. 6, pp. 3516-18 (1992).
61. Cohen, S.S., Bernstein, J.B., Wyatt, P.W., "*The effect of multiple laser pluses on damage to thin metallic films*," Journal of Applied Physics, vol. 71, no. 2, pp. 630-7 (1992).
62. Cohen, S.S., Bernstein, J.B., Wyatt, P.W., "*Laser-induced line melting and cutting*," IEEE Transactions on Electron Devices, vol. 39, no. 11, pp. 2480-5 (1992).
63. Bernstein, J.B., "*Analysis of the electrically stimulated acoustic-wave method for observing space charge in semi-insulating films*," Physical Review B (Condensed Matter), vol.44, no.19, pp. 10804-14 (1991).
64. Bernstein, J.B., Cooke, C.M., "*Bulk space charge behavior in polymethylethacrylate under an imposed virtual cathode condition*," IEEE Transactions on Electrical Insulation, vol. 26, no. 6, pp. 1080-6 (1991).
65. Bernstein, J.B., Cooke, C.M., "*Electric poling behavior of polymethylmethacrylate*," IEEE Transactions on Electrical Insulation, vol. 26, no. 6, pp. 1087-93 (1991).
66. Cohen, S.S., Wyatt, P.W., Bernstein, J.B., "*Laser-induced melting of thin conducting films. II. Heat-dissipating substrates*," IEEE Transactions on Electron Devices, vol.38, no.9 pp. 2051-7 (1991).
67. Cohen, S.S., Wyatt, P.W., Burns, J.A., Bernstein, J.B., "*The mechanism of laser-induced vertical links*," Journal of the Electrochemical Society, vol.138, no.10, pp. 3013-18 (1991).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Refereed Conference Proceedings

1. E Bender, JB Bernstein, DS Boning, "*The Effects of Process Variations and BTI in Packaged FinFET Devices*," IEEE International Reliability Physics Symposium (IRPS), 1-5 Monterey, CA (2023)
2. JB Bernstein, E Bender, A Bensoussan, "*The Correct Hot Carrier Degradation Model*," 2023 IEEE International Reliability Physics Symposium (IRPS), 1-5 Monterey, CA (2023)
3. E. Bender and J. B. Bernstein, "Self-heating Effects Measured in Fully Packaged FinFET Devices," 32ND INTERNATIONAL CONFERENCE ON MICROELECTRONICS, Serbia (2021)
4. I Aharn, Y Shalom, Y Dromi, A Shemaryahu, JB Bernstein, "*GaN based Ring Oscillator PWM Generator*," IEEE 12th Energy Conversion Congress & Exposition-Asia (ECCE-Asia 2021)
5. E Bender, JB Bernstein, A Bensoussan, "*Reliability prediction of FinFET FPGAs by MTOL*," *Microelectronics Reliability, ESREF* (2020)
6. I Aharon, M Sitbon, J Bernstein, "*Design Considerations for GaN Based Converters*," 8th International Conference on Renewable Energy Research and Applications (ICRERA 2019)
7. G Golan, M Azoulay, J Bernstein, "*On the Ballistic Transport in Si Nano-Devices*," *IEEE 31st International Conference on Microelectronics (MIEL)*, 55-58 (Sept. 2019)
8. M Musil, A Bensoussan, J Bernstein, F Coccetti, "Synopsis of Multiphysics Deep Sub-Micron Failure Rate Modeling Technique for CFR and EOL Prediction," 2018 IEEE 13th Nanotechnology Materials and Devices Conference (NMDC) (Nov 2018)
9. G Golan, M Azoulay, S Shaheen, JB Bernstein, "A Novel Reliability Model For GaN Power FET," 2018 IEEE International Conference on the Science of Electrical Engineering {Dec 2018}
10. J.B Bernstein, "Aerospace electronics reliability: Could it be predicted in a cost-effective fashion?," IEEE Aerospace Conference, Colorado (Feb 2015)
11. J.B. Bernstein, O. Delly, M. Gabbay, "Combination of Multiple Mechanism for Post-Silicon Reliability Prediction," ChipEx 2014, Tel Aviv (April 2014)
12. J.B. Bernstein, "Multiple Accelerated Test Matrix for Reliability Prediction," SemIsrael Expo, Airport City, Israel (Nov 2013)
13. J.B. Bernstein and Y. Bot, "Physics Based Reliability Qualification," IEEE-IRIC, (March 2013)
14. J.B. Bernstein, "Physics of Failure Based Reliability Qualification," Proceedings of 19th International Conference of the Israel Society for Quality, pres. 7.1.4 Tel Aviv (October 2012).
15. Hava, F. Barmoav, C. Moulton, B. Kowalski, E. Ribak and J.B. Bernstein, "Prediction of Earpiece field failure rate based on accelerated Life test," 2012 IEEE 27-th Convention, Eilat (2012).
16. J. Qin, M. White, J.B. Bernstein, "A Study of Scaling Effect on DRAM Reliability," Annual Reliability and Maintainability Symposium (RAMS), Final Report, pp. 9C-4 (January 2011).
17. J. Qin, A. Hava, J.B. Bernstein, "FaRBS: a New PoF Based VLSI Reliability Prediction Method," Annual Reliability and Maintainability Symposium (RAMS), pp. 9D-3 (January 2011).
18. M. Gurfinkel, P. Livshits, A. Rozen, Y. Fefer, J.B. Bernstein, Y. Shapira, "Supply signal

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

fluctuations due to chip power grid resonance — a new reliability concern,” Proc. of the IEEE International Reliability Physics Symposium, (April-May 2008).

19. J. Qin, B. Yan, Y. Shoshany, R. Druker, H. Rahamim, H. Marom, J.B. Bernstein, “Study of Transistor and Product NBTI Lifetime Distributions (A),” International Integrated Reliability Workshop (IIRW) Final Report, pp. 1-16 (October 2008).
20. J. Qin, B. Yan, Y. Shoshany, R. Druker, H. Rahamim, H. Marom, J.B. Bernstein, “Study of Transistor and Product NBTI Lifetime Distributions (B),” International Integrated Reliability Workshop (IIRW) Final Report, pp. 64-67 (October 2008).
21. B. Yan, J. Qin, J. Dai, Q. Fan, J.B. Bernstein, “Reliability Simulation and Design Consideration of High Speed ADC Circuits,” International Integrated Reliability Workshop (IIRW) Final Report, pp. 125-128 (October 2008).
22. L. Condra, J. Qin and J.B. Bernstein, “State of the Art Semiconductor Devices in Future Aerospace Systems,” Proceedings of the FAA/NASA/DoD Joint Council on Aging Aircraft Conference, Palm Springs, CA (April 2007).
23. M. Gurfinkel, J. Suehle, J.B. Bernstein, Yoram Shapira, A.J. Lelis, D. Habersat, N. Goldsman, “Ultra-fast Characterization of Transient Gate Oxide Trapping in SiC MOSFETs,” Proc. of the IEEE International Reliability Physics Symposium 2007.
24. J. Qin, X. Li, J.B. Bernstein, “SRAM Stability Analysis Considering Gate Oxide SBD, NBTI and HCI,” 2007 International Integrated Reliability Workshop (IIRW) Final Report, 2.2, (October 2007).
25. M. Gurfinkel, et. al., “Characterization of Interface and Bulk Oxide Traps in SiC MOSFETs with Epitaxially grown and implanted channels,” 2007 International Integrated Reliability Workshop (IIRW) Final Report, 8.3 (October 2007).
26. L. Yang, J.B. Bernstein, D. Gajewski and J. Walls, “Predictive Reliability Assessment and Failure Rate Modeling for Electronic Packages,” IMAPS 40th International Symposium on Microelectronics, Final Report, WA5 (November 2007).
27. M. Gurfinkel, J. Suehle, J.B. Bernstein, Y. Shapira, A.J. Lelis, D. Habersat, N. Goldsman, “Ultra-Fast Measurement of V_{th} Instability in SiC MOSFETs due to Positive and Negative Constant Bias Stress,” 2006 International Integrated Reliability Workshop (IIRW) Final Report, pp. 49-53 (October 2006).
28. M. White, C. Vu, C. Nguyen, R. Ruiz, Y. Chen, J.B. Bernstein, “Product Reliability Trends, Derating Considerations and Failure Mechanisms with Scaled CMOS,” 2006 International Integrated Reliability Workshop (IIRW) Final Report, pp. 156-159 (October 2006).
29. J. Qin, J.B. Bernstein, “Non-Arrhenius Temperature Acceleration and Stress-Dependent Voltage Acceleration for Semiconductor Devices Involving Multiple Failure Mechanisms,” 2006 International Integrated Reliability Workshop (IIRW) Final Report, pp. 93-97 (October 2006).
30. Bernstein, J. B., “Reliability Qualification at the Maryland-Israel Center for Product Realization,” Proceedings of 16th International Conference of the Israel Society for Quality, pp.

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

9.2.01 Tel Aviv (November 2006).

31. M. Gurfinkel, J. Suehle, J.B. Bernstein, Y. Shapira, "Enhanced Gate Induced Leakage Current in HfO₂ MOSFETs due to Remote Interface Trap-Assisted Tunneling," 2006 International Electron Devices Meeting (IEDM) technical digest, pp. 755-758, (Dec 2006).
32. Xiaojun Li; Walter, J.D.; Bernstein, J.B.; "Simulating and Improving Microelectronic Device Reliability by Scaling Voltage and Temperature," Quality of Electronic Design, 2005. ISQED 2005. Sixth International Symposium, pp.496 - 502 (March 2005).
33. Xiaojun Li; Huang, B.; Qin, J.; Zhang, X.; Talmor, M.; Gur, Z.; Bernstein, J.B.; "Deep Submicron CMOS Integrated Circuit Reliability Simulation with SPICE," Quality of Electronic Design, 2005. ISQED 2005. Sixth International Symposium on, pp. 382 - 389 (March 2005).
34. Zhu, B.; Suehle, I.S.; Vogel, E.; Bernstein, J.B.; "The contribution of HFO₂ bulk oxide traps to dynamic NBTI in pMOSFETs," IEEE International Reliability Physics Symposium 2005 Proceedings, pp. 533 – 537 (April 2005).
35. Kuan-Jung Chung; Bernstein, J.B.; Ji Luo; Tuchman, J.A.; Ma, Z.K.; "Experimental Study for Low Resistance Interline Connections Using Pulsed Laser Techniques," Quantum Electronics and Laser Science 2005, Conference Volume 3, pp.1564 - 1566 (May 2005).
36. Bing Huang; Xiaojun Li; Ming Li; Bernstein, J.; Smidts, "Study of the impact of hardware fault on software reliability," Proceedings. 16th IEEE International Symposium on Software Reliability Engineering. Chicago, IL, USA (Nov. 2005).
37. B. Zhu, J.S. Suehle, J.B. Bernstein, "Mechanism for reduced NBTI effect under pulsed bias stress conditions," Proceedings of Integrated Reliability Workshop, Phoenix (Arizona 2004).
38. J.S. Suehle, B. Zhu, Y. Chen, J.B. Bernstein, "Acceleration factors and mechanistic study of progressive breakdown in small area ultra-thin gate oxides," Proceedings of Integrated Reliability Workshop, Phoenix (Arizona 2004).
39. Ji Luo; Bernstein, J.B.; Tuchman, J.A.; Hu Huang; "A high performance radiation-hard field programmable analog array." Proceedings. 5th International Symposium on Quality Electronic Design. p. 522-7. (Los Alamitos, CA, 2004).
40. Hu Huang, Joseph B. Bernstein, Martin Peckerar, Ji Luo; "Combined Channel Segmentation and Buffer Insertion for Routability and Performance Improvement of Field Programmable Analog Arrays," Proceedings of the IEEE International Conference on Computer Design (October 2004).
41. X. Zhang, N. Goldsman, J.B. Bernstein, J.M. McGarrity, "Numerical and Experimental Characterization of 4H-SiC Schottky Diodes," Proceedings of IEEE International Semiconductor Device Research Symposium, p. 120-1 (2003).
42. M. White, M. Cooper, Y. Chen, J. Bernstein, "Impact of Junction Temperature on Microelectronic Device Reliability and Considerations for Space Applications," Proceedings of Integrated Reliability Workshop, p. 133-6 (Nevada 2003).
43. B. Zhu, J.B. Bernstein, J. Suehle, "Negative bias temperature instability of deep sub-micron p-MOSFETs under pulsed bias stress," Proceedings of Integrated Reliability Workshop, pp. 125-9 (Nevada 2003).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

44. Y. Chen, D. Nguyen, S. Guertin, J.B. Bernstein, M. White, R. Menke, S. Kayali, "A Reliability Evaluation Methodology for Memory Chips for Space Applications when Sample Size is Small," Proceedings of Integrated Reliability Workshop, Lake Tahoe (Nevada 2003).
45. Ji Luo, Kuan-Jung Chung, Hu Huang, J.B. Bernstein, "Temperature Dependence of R(on,sp) in Silicon Carbide and GaAs Schottky diodes," Proceedings of IEEE International Reliability Physics Symposium, 40th annual (New Jersey 2002).
46. Zhuo Gao, Ji Luo, Hu Huang, Wei Zhang, J.B. Bernstein, "Reliable laser programmable gate array technology," Proceedings International Symposium on Quality Electronic Design, p. 252-6, Los Alamitos (California 2002).
47. D. Heh, J.B. Bernstein, E.M. Vogel, "Defect generation in ultra-thin oxide over large fluence ranges," Proceedings of Integrated Reliability Workshop, Lake Tahoe (Nevada 2002).
48. Z. Gao, J. Luo, Hu Huang, W. Zhang, J.B. Bernstein, "Reliable laser programmable gate array technology," Proceedings of International Symposium on Quality Electronic Design, pp. 252-256 (California 2002).
49. J.S. Suehle, et.al ... J.B. Bernstein, "Challenges of high-k gate dielectrics for future MOS devices," 6th International Symposium on Plasma and Process Induced Damage, pp. 90-93 (California 2001).
50. B. Wang, J.B. Bernstein, "Latent Reliability Degradation of Ultra-Thin Oxides after Heavy Ion and Gamma Irradiation," Proceedings of Integrated Reliability Workshop (California 2001).
51. Bernstein, J.B. and Lee, J, "A Laser Formed MakeLink for Customization and Repair," Proceedings of IEEE International Symposium on Semiconductor Manufacturing, pp. 347-350 (California 2001).
52. Ji Luo, K. Chung, Hu Huang, J.B. Bernstein, "Comparison of Silicon Carbide Schottky diodes," Proceedings of 2001 GaAs Reliability Workshop (Virginia 2001).
53. Suehle, J.S., Vogel, E., Wang, B., Bernstein, J.B., "Temperature Dependence of Soft Breakdown and Wear-Out in Sub-3 nm SiO₂ Films," International Reliability Physics Symposium - Conference Proceedings, pp. 33-9 (California 2000).
54. E. M. Vogel, M. D. Edelstein, C. A. Richter, N. V. Nguyen, I. Levin, D. L. Kaiser, H. Wu, and J. Bernstein, "Issues in High-κ Gate Dielectrics for Future MOS Devices," Proceedings of IEEE Microelectronics Reliability Qualification Workshop (California 2000).
55. B. Wang, J. Suehle, E.M. Vogel, J.B. Bernstein, "The Effect of Stress Interruption and pulsed bias stress on Ultra-Thin Gate Dielectric Reliability," Proceedings of Integrated Reliability Workshop (California 2000).
56. J. Lee, G. Zhuo and J.B. Bernstein, "Laser Programmable Multichip Module using Vertical Make-link," Proceedings of the IEEE Electronic Components and Technology Conference, pp 932-936 (Nevada 2000).
57. Vogel, E., Suehle, J.S., Edelstein, M.D., Wang, B., Chen, Y., Bernstein, J.B., "Degradation of Ultra-thin SiO₂ Under Combined Substrate Hot Electron and Tunneling Stress," Semiconductor Interface Specialists Conference, (California 2000).
58. Shen, C.C., Kefner, A.R., Jr., Berning, D.W., Bernstein, J.B., "Failure dynamics of the IGBT during turn-off for unclamped inductive loading conditions," Conference Record of 1998 IEEE Industry Applications Conference, p. 3, vol. xxx+2410, 831-9, vol. 2 (New York 1999).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

59. Zhang, W., Bernstein, J.B., "Electromigration simulation under DC/AC stresses considering microstructure," Proceedings of the IEEE 1999 International Interconnect Technology Conference, pp. 295, 41-3 (California 1999).
60. Chen, Y., Suehle, J.S., Shen, C.C., Bernstein, J.B., Messick, C., Chaparala, P., "The correlation of highly accelerated Q_{bd} tests to TDDB life tests for ultra-thin gate oxides," 1998 IEEE International Reliability Physics Symposium Proceedings. 36th Annual, pp. 87-91 (California 1998).
61. Bernstein, J.B., Zhang, W., Nicholas, C.H., "Laser formed connections for programmable wiring," Proceedings of the IEEE 1998 Custom Integrated Circuits Conference, pp. 608, 163-5 (California 1998).
62. Bernstein, J.B., Zhang, W., Nicholas, C.H., "Laser programmable metallic vias," Proceedings of the IEEE 1998 International Interconnect Technology Conference, pp. 304, 205-7 (New York 1998).
63. Chen, Y., Suehle, J.S., Shen, C.C., Bernstein, J.B., Messick, C., Chaparala, P., "The correlation of highly accelerated Q_{bd} tests to TDDB life tests for ultra-thin gate oxides," 1998 IEEE International Reliability Physics Symposium Proceedings. 36th Annual, pp. vii+421, 87-91 (Nevada 1998).
64. Chen, Y., Suehle, J.S., Shen, C.C., Bernstein, J.B., Messick, C., "A New Technique to Extract TDDB Acceleration Parameters from Fast Q_{bd} Tests," Proceedings of International Integrated Reliability Workshop, pp. 67-69, (Nevada 1997).
65. Bernstein, J.B., "Laser Formed Lateral Metallic Connections," Proceedings of the Second International Conference on Beam Processing of Advanced Materials, pp. 101-104 (Ohio 1995).
66. Bernstein, J.B., "Dielectric fracture leading to metallic connections employing a lateral link structure," Thin Films: Stresses and Mechanical Properties V. Symposium, MRS pp. 833-7 (Massachusetts 1994).
67. Bernstein, J.B., Ventura, T.M., Radomski, A.T., "Laser induced microfracture leading to high density metal-to-metal connections," Proceedings of the SPIE, The International Society for Optical Engineering, pp. 165-76 (Texas 1994).
68. Bernstein, J.B., Gleason, E.F., Wetsel, A.E., Liu, E.Z., Wyatt, P.W., "Anomalous Behavior of Semi-insulating Silicon Rich Amorphous Silicon Nitride," Amorphous Insulating Thin Films Symposium, MRS pp. 113-18 (Massachusetts 1993).
69. Bernstein, J.B., Gleason, E.F., Wyatt, P.W., "A thermally stable silicon rich amorphous silicon nitride alloy for electronic device applications," Amorphous Silicon Technology Symposium, MRS pp. 667-72 (California 1992).
70. Bernstein, J.B., Gleason, E.F., Wyatt, P.W., "High density metal cross-point laser linking," International Conference on Wafer Scale Integration Proceedings, pp. 176-81 (California 1992).
71. Bernstein, J.B., Cohen, S.S., Wyatt, P.W., "Fatigue of aluminum films leading to melting by multiple laser pulses," Phase Formation and Modification by Beam-Solid Interactions Symposium, MRS pp. 589-93 (Boston 1991).
72. Cooke, C.M., Wright, K.A., Takasu, N., Bernstein, J.B., Gollin, E., "Calibration of Volume Charge Measurements By Use of Electron Beam Implantation," 1989 Annual Report. Conference on Electrical Insulation and Dielectric Phenomena, pp. 508, 435-41 (Virginia 1989).
73. Bernstein, J.B., Bahl, S., Schlecht, M.F., "A Low Capacitance Power MOSFET with an Integral Gate Driver," Proceeding of the 18th Annual IEEE Power Electronics Specialists Conference, PESC vol. 87, pp. 704, 61-8 (Virginia 1987).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Magazine Articles

1. J.B. Bernstein, "Engineering through Torah," Et Lachshov, Vol. 96, pp. 16-19 (Aug-Sep. 2008).
2. J.B. Bernstein, "The Power of Three" (Hebrew), Et Lachshov, Vol. 89, pp. 32-37 (Jul-Aug 2007).
3. J.B. Bernstein, "Scientific Exploration," Et Lachshov, Vol. 87, pp. 12-15 (May-June 2007).
4. J.B. Bernstein, "Reliable Truth" (In Hebrew), Et Lachshov, Vol. 86, pp. 16-18 (Mar-Apr 2007).
5. J.B. Bernstein, "Good and Bad" (In Hebrew), Et Lachshov, Vol. 82, pp. 16-18 (Dec. 2006).
6. J.B. Bernstein, "Limitations" (In Hebrew), Et Lachshov, Vol. 80, pp. 22-24 (Sep.-Oct. 2006).
7. J.B. Bernstein, "Computers and the Jewish Soul" (In Hebrew), Et Lachshov, Vol. 79, pp. 22-24 (Jul.-Aug. 2006).
8. J.B. Bernstein, "Chess and Free Choice," Et Lachshov, Vol. 76, pp. 14-17 (May 2006).
9. J.B. Bernstein, "Truth through the Scientific Method" (In Hebrew), Et Lachshov, Vol. 74, pp. 25-27 (Feb. 2006).
10. J.B. Bernstein, "Education and Technology," Et Lachshov, Vol. 67, pp. 22-25 (June 2005).
11. J.B. Bernstein, "The Wonders of Silicon," Et Lachshov, Vol. 66, pp. 28-30 (May 2005).
12. J.B. Bernstein, "The Moon" (In Hebrew), Et Lachshov, Vol. 64, pp. 30-32 (March 2005).
13. J.B. Bernstein, "Halacha and Engineering Design" Et Lachshov, Vol. 63, pp. 36-37 (Feb. 2005).
14. J.B. Bernstein, "Statistical Logic" (In Hebrew), Et Lachshov, Vol. 62, pp. 20-22 (Jan. 2005).
15. J.B. Bernstein, "That we should not know from failures..." (In Hebrew), Et Lachshov (time to think), Vol. 61, pp. 32-33 (Oct. – Dec. 2004).
16. J.Lee, J. Ehrmann, D. Smart, J. Griffiths, and J.B. Bernstein, "Analyzing the process window for laser copper-link processing," Solid State Technology, (December 2002).
17. Pecht, M., Bernstein, J.B., Searls, D., Peckerar, M., Karulkar, P., "Korea's Focus on Market Dominance," Semiconductor International, pp. 118-22 (1998).
18. Kump, H.J., Bernstein, J.B., "The Deal fast-surface states are probably deep-level impurities in the semiconductor," IEEE Circuits and Devices Magazine, vol. 1, no. 6, pp. 17-22 (1985).