

A Single-Chip 900 MHz CMOS Receiver Front-End with a High Performance Low-IF Topology

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Abstract—An analog receiver front-end chip realized in a 0.7 μm CMOS technology is presented. It uses a new, high performance, downconverter topology, called double quadrature downconverter, that achieves a phase accuracy of less than 0.3° in a large passband around 900 MHz, without requiring any external component or any tuning or trimming. A high performance low-IF receiver topology is developed with this double quadrature downconverter. The proposed low-IF receiver combines the advantages of both the classical IF receiver and the zero-IF receiver: an excellent performance and a very high degree of integration. In this way, it becomes possible to realize a true fully integrated receiver front-end that does not require a single external component and which is, different from the zero-IF receiver, nonetheless totally insensitive to parasitic baseband signals and self-mixing products.

I. INTRODUCTION

IN THE LAST few years, the world of wireless communications has been changing very rapidly [1]. One aspect of this evolution is the ever increasing level of integration of the transceivers, driven by the need for both a better portability and a lower cost prize. The consequence of this evolution is that the zero-IF downconversion topology is used more and more in receivers for mobile wireless telecommunications applications [2], [3]. The zero-IF receiver can be implemented with a much higher degree of integration than the conventional IF (heterodyne) receiver. This has made the zero-IF downconverter the preferred topology in the research towards the fully integrated single-chip transceiver.

However, the zero-IF topology has two, well known, major drawbacks that makes achieving an acceptable performance with it very hard [4], [5]. Firstly, its baseband configuration makes the zero-IF topology highly sensitive to parasitic baseband signals like dc offset voltages and self-mixing products caused by crosstalk between the RF and the LO signals. The second source of performance reduction is inherent to any analog integrated multipath topology. Excellent matching between the different downconversion paths is required but limited in analog implementations. The effects of mismatch, i.e., phase and amplitude errors, degrade the signal quality because they result in a reduced mirror signal suppression.

The use of multipath topologies is nowadays in analog applications still very limited. In digital and software applications,

matching is always perfect, and multipath topologies are used widely. In these applications, two parallel signals are regarded as one complex signal on which different complex signal processing steps are performed. In this paper, it is shown how the complex signal method can be extended to the world of analog systems with its inherent imperfect matching between parallel processing paths. It is demonstrated in this paper that many more analog multipath signal operations, other than the classical quadrature downconversion and low-pass filtering, are possible. The complex signal method is used to get a clear insight in both the wanted complex signal operation and the unwanted operations caused by mismatch. With these analog complex signal operators and the complex signal analysis method for analog systems, many new receiver topologies can be synthesized. This paper discusses the different possibilities and selects one topology, named the low-IF receiver topology, as the most preferable.

The low-IF receiver is, like the zero-IF receiver, also a multipath topology that can be implemented in a highly integrated way. It uses an IF of a few hundred kHz and is therefore not sensitive to parasitic baseband signals like dc offset voltages and self-mixing products. In this way, the low-IF receiver combines the advantages of both the IF and the zero-IF receiver. It can have a high performance and a high degree of integration at the same time. The main drawback of the low-IF receivers is that they are more sensitive to a good mirror signal suppression, because, in opposition to the zero-IF receiver, here the mirror signal can be larger than the wanted signal. With the complex signal method, it is demonstrated that the phase error of the quadrature downconverter is the main limitation for the mirror signal suppression. A typical quadrature downconverter with a phase error of 3° [6], results in a maximal mirror signal suppression of 26 dB. Therefore, this paper presents a newly developed fully integrated CMOS quadrature downconverter with a phase accuracy of 0.3° , a key building block for high quality low-IF receivers. Its topology is synthesized with the complex signal method and analog complex signal operators, and it is shown how this quadrature downconverter in combination with an LNA and a synthesizer can form the complete and fully integrated analog low-IF receiver front-end.

The quadrature downconverter that is presented here is in many ways different from the conventional realizations [6]. The conventional realizations use an $RC-CR$ network for the quadrature generation of the LO signal and two Gilbert multipliers for the downconversion. The generation of the

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quadrature signal is based on the 90° phase-difference between a pole and zero with the same cutoff frequency. Due to its asymmetric structure is the phase accuracy of an *RC-CR* quadrature generator typically about 3°. Only with tuning and trimming can its phase error be made lower than 1° [7]. Here, sequence asymmetric polyphase filters are used for a high quality broad-band quadrature generation. Both the RF and the LO input signals are put in quadrature and mixed down with four CMOS downconversion multipliers of which the output signals are combined two by two. This new topology is called the double quadrature downconverter. In order to obtain an overall phase error of 0.3°, each quadrature generator of the double quadrature downconverter requires only a phase-error of 4°, resulting in no need for matching, tuning, or trimming.

The presented quadrature downconverter is realized in a 0.7 μm CMOS process, and it does not require any external component. The realization in CMOS has been chosen to prove the abilities of submicron CMOS for the integration of high performance RF circuitry. The trend to a full and low cost integration of the complete wireless system on a single chip, including both the analog and the digital part, will make CMOS a key technology for advanced RF circuitry development.

In the second part of this paper, the complex signal method for the analysis of analog multipath signal processing architectures is introduced. With this technique, the low-IF receiver is synthesized and analyzed, and the qualities of this receiver architecture towards a high degree of integration and a high performance are demonstrated in Section III. Section IV deals with the design and implementation of the double quadrature downconverter. The results of the realized quadrature downconverter are given in Section V. The downconverter has single-ended RF and LO inputs, it delivers fully differential *I*- and *Q*-signals at its output with an amplitude error smaller than 0.5 dB and a phase error smaller than 0.3° in a passband from 500–900 MHz. Its noise figure is 24 dB for a 12 dBm LO signal, and its third-order interception point (IP3) is more than 27 dBm. Its input bandwidth is as high as 900 MHz, and its output bandwidth is 3 MHz.

II. SYNTHESIS OF ANALOG MULTIPATH SYSTEMS

The analysis of multipath systems is greatly simplified when at each point the set of parallel signals is treated as one signal vector. This is perfectly possible for any set of independent signals. By transforming these signal vectors to a new vectorspace, a new set of independent signals can be defined. These new signal sets give, when properly chosen, a clear insight in their frequency information, and special frequency operations can be defined on them.

A two-dimensional signal vector (i.e., a set of two independent signals, e.g., an *I*, *Q*-signal) can be represented as a complex signal

$$\begin{aligned} y(t) &= [i(t) \quad q(t)] = i(t) + jq(t) = y_r(t) + jy_i(t) \\ Y(j\omega) &= [I(j\omega) \quad Q(j\omega)] = I(j\omega) + jQ(j\omega) \\ &= Y_r(j\omega) + jY_i(j\omega). \end{aligned} \quad (1)$$

Any frequency component of a signal can be written as a sum of a positive ($e^{+j\omega}$) and a negative ($e^{-j\omega}$) signal

$$\begin{aligned} A(\omega) \cdot \cos(\omega t + \varphi(\omega)) &= \frac{A(\omega)}{2} \cdot [\cos(\omega t + \varphi(\omega)) + j \cdot \sin(\omega t + \varphi(\omega))] \\ &\quad + \frac{A(\omega)}{2} \cdot [\cos(\omega t + \varphi(\omega)) - j \cdot \sin(\omega t + \varphi(\omega))] \end{aligned} \quad (2)$$

$$\begin{aligned} A(\omega) \cdot [\cos(\omega t + \varphi(\omega)) + j \cdot \sin(\omega t + \varphi(\omega))] &= A(\omega) \cdot e^{j\varphi(\omega)} \cdot e^{j\omega t} \\ A(\omega) \cdot [\cos(\omega t + \varphi(\omega)) - j \cdot \sin(\omega t + \varphi(\omega))] &= A(\omega) \cdot e^{-j\varphi(\omega)} \cdot e^{-j\omega t} \end{aligned} \quad (3)$$

Equations (1) and (3) show that a signal vector can be made that has only a positive or a negative frequency component. In a more general way, it can be said that the positive and negative frequency information content of a complex signal vector can be completely independent. It becomes thus important to always represent a complex signal vector with its positive and negative frequency information.

The possibility of creating a signal, albeit a complex signal pair, which has only a positive frequency content gives many design opportunities because the main problem in receiver design is the fact that the multiplication in a downconverter with a sinus is a multiplication with both a positive and a negative frequency. This is the well known problem of the mirror frequency. This problem is nowadays solved by using either an external high IF and an external high frequency high-*Q* mirror signal suppression filter (IF receiver) or by using no IF (zero-IF receiver). If there would exist a multiplying operation defined on complex signal pairs that would preserve the convolution laws, there would be a third method: a downconversion to an IF frequency by multiplication with only a positive frequency, resulting in no downconversion of the unwanted mirror signal frequency, no need for a high IF, and no need for an external high *Q* HF filter. Such a multiplication for complex signal pairs is given by the complex multiplication

$$\begin{aligned} z(t) &= y(t) \cdot x(t) = (y_r(t) + jy_i(t)) \cdot (x_r(t) + jx_i(t)) \\ &= (y_r(t) \cdot x_r(t) - y_i(t) \cdot x_i(t)) \\ &\quad + j(y_r(t) \cdot x_i(t) + y_i(t) \cdot x_r(t)) \end{aligned} \quad (4)$$

$$\begin{aligned} Z(j\omega) &= Y(j\omega) \otimes X(j\omega) \\ &= (Y_r(j\omega) + jY_i(j\omega)) \otimes (X_r(j\omega) + jX_i(j\omega)) \\ &= (Y_r(j\omega) \otimes X_r(j\omega) - Y_i(j\omega) \otimes X_i(j\omega)) \\ &\quad + j(Y_r(j\omega) \otimes X_i(j\omega) + Y_i(j\omega) \otimes X_r(j\omega)). \end{aligned} \quad (5)$$

Fig. 1 gives the block diagram realization of (4) and (5). It reduces to the classical quadrature multiplier when only a single signal has to be multiplied with a complex signal pair. The problem with an actual analog integrated implementation of this block diagram is that (4) and (5) only hold when the conversion gains of the four mixers are perfectly matched. Perfect matching does not exist in analog circuits, and the higher the operating frequencies, the more difficult the matching becomes. A mismatch between the four conversion gains can be split up as a mismatch between the gains in the different

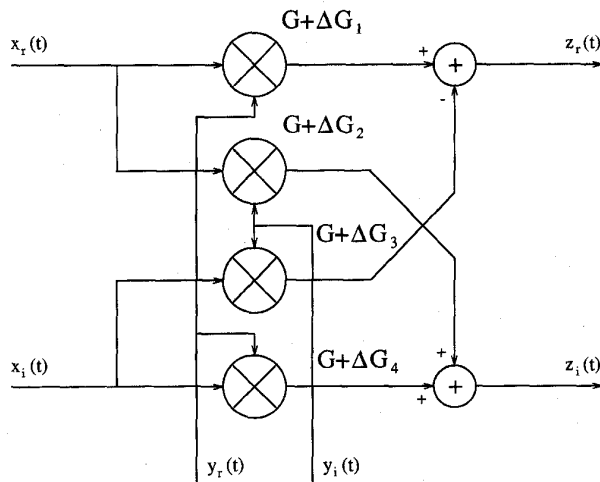


Fig. 1. Mixer topology for the multiplication of two complex signal pairs.

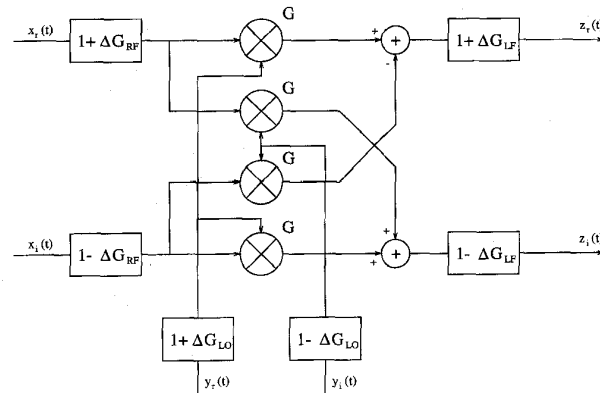


Fig. 2. Conversion gain mismatch in the complex signal multiplier and its equivalent scheme.

signal paths. These mismatches have been added in Fig. 1 as ΔG_i . The equivalent scheme is shown in Fig. 2.

A gain mismatch between two parallel signal paths is equivalent with a crosstalk between positive and negative frequencies. Fig. 3 shows this: the gain mismatch can be rewritten as the sum of two parallel signal operations, the wanted perfectly matched gain operation, and a gain operation as large as the mismatch combined with a frequency mirror operation (positive frequency components become negative frequencies and vice-versa, as proven in (6)). The crosstalk is thus equal to $\Delta A/A$. An amplitude error of 1% gives a -40 dB crosstalk between the positive and negative frequencies. For the complex mixer of Fig. 2, this results in an imperfect mirror signal suppression. The equivalent gain mismatch in the LO signal path makes the multiplication with a pure single positive frequency impossible. There is always also the multiplication with a small negative frequency component. Gain mismatch in the LF path results also in a crosstalk of the unwanted mirror signal, situated at the negative IF, to the wanted signal,

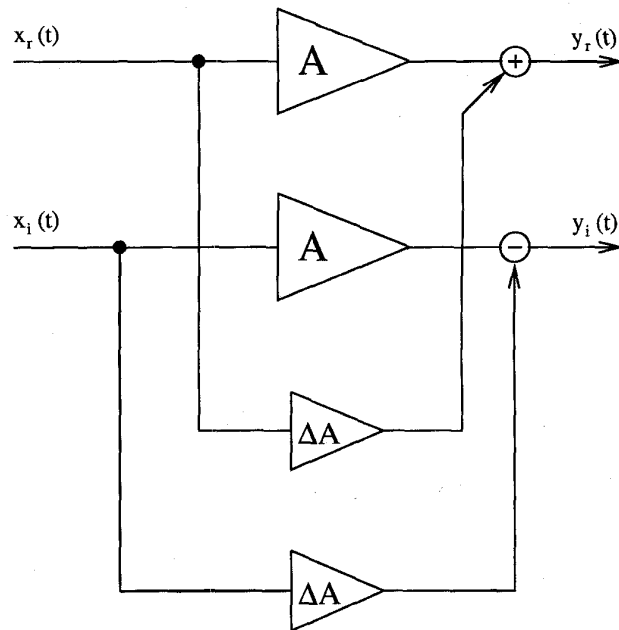


Fig. 3. Equivalent scheme for gain mismatch between two parallel signal processing paths.

situated at the positive IF

$$\begin{aligned} e^{j\omega_c t} &= \cos(\omega_c t) + j \cdot \sin(\omega_c t) \rightarrow \sin(\omega_c t) + j \cdot \cos(\omega_c t) \\ &= j \cdot e^{-j\omega_c t} \\ e^{-j\omega_c t} &= \cos(\omega_c t) - j \cdot \sin(\omega_c t) \rightarrow \sin(\omega_c t) - j \cdot \cos(\omega_c t) \\ &= -j \cdot e^{j\omega_c t}. \end{aligned} \quad (6)$$

The result of a phase error between two parallel signal paths is also an unwanted mirroring of signals to their opposite frequencies. Equation (7) gives the effect of a phase error on a positive frequency component

$$\begin{aligned} e^{j\omega_c t} &= \cos(\omega_c t) + j \cdot \sin(\omega_c t) \rightarrow \cos(\omega_c t + \Delta\varphi) \\ &\quad + j \cdot \sin(\omega_c t - \Delta\varphi) \\ &= \cos(\Delta\varphi) \cdot (e^{j\omega_c t} - j \cdot \tan(\Delta\varphi) \cdot e^{-j\omega_c t}). \end{aligned} \quad (7)$$

Apart from the wanted positive frequency, the total transfer function generates again also a negative and unwanted frequency component. The ratio between the unwanted and the wanted signal is $\tan(\Delta\varphi)$, which can be taken equal to $\Delta\varphi$ for small values of $\Delta\varphi$. This means that a phase error of 1° results in a -35 dB crosstalk between positive and negative frequencies.

Phase errors are not so important as amplitude errors in the complex mixer structure of Fig. 2 as long as its operating frequency is lower than its bandwidth. Phase errors are more dominant in filter operations performed on complex signal pairs. There are basically three different filter operations that can be performed on complex signal pairs. The first one is given in Fig. 4. Putting the same filter in the two parallel paths gives the filter transfer function for both the positive and negative frequencies. Amplitude and phase differences between the two transfer functions will cause frequency crosstalk.

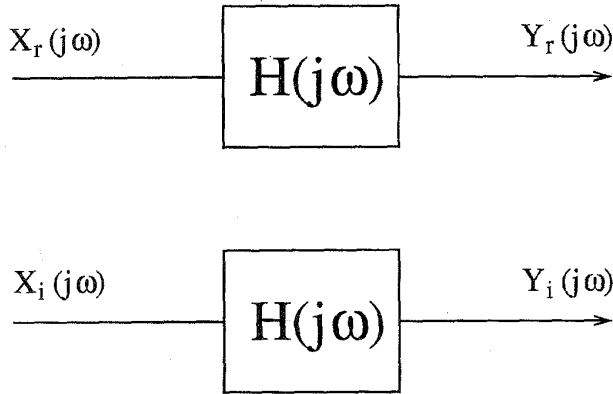


Fig. 4. The classic two-port filtering for complex signals.

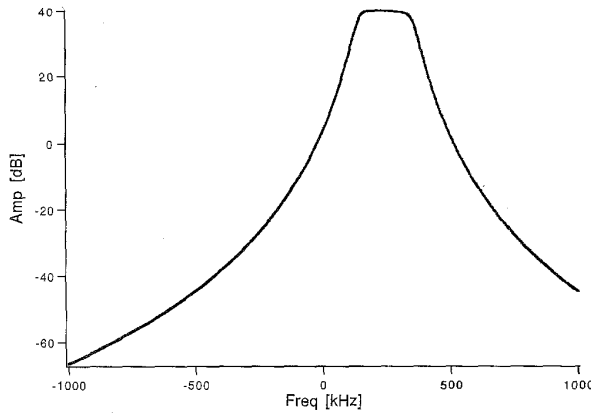


Fig. 5. The transfer function for positive and negative frequencies of an active integrated fifth-order sequence asymmetric polyphase filter.

A second class of filters for complex signal pairs are called active sequence asymmetric polyphase filters [8]. These filters are band-pass filters that have a passband for either only positive or negative frequencies. This makes them suitable for the suppression of the mirror signal after a quadrature downconversion (after quadrature downconversion the mirror signal is situated at frequencies opposite of the wanted signal). The transfer function of an active asymmetric polyphase is a linear frequency translated version of a low-pass filter. For a first-order low-pass filter is this

$$H_{lp}(j\omega) = \frac{1}{1 + j\omega/\omega_o}$$

$$H_{bp}(j\omega) = \frac{1}{1 - j\omega_c/\omega_o + j\omega/\omega_o} = \frac{1}{1 - 2jQ + j\omega/\omega_o} \quad (8)$$

Fig. 5 shows the transfer function of a frequency translated fifth-order low-pass Butterworth filter. The linear transformation $H_{bp}(j\omega) = H_{lp}(j\omega - j\omega_c)$ ensures that there is only a passband for positive frequencies. The aspects of synthesis and implementation of active asymmetric polyphase filters are described in [9].

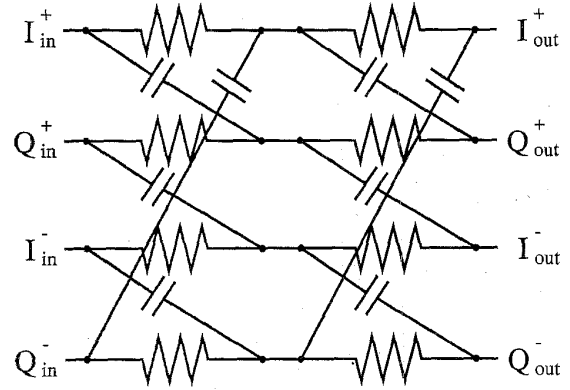


Fig. 6. A passive sequence asymmetric polyphase filter.

The third class of filters for complex signals are the passive sequence asymmetric polyphase filters [10]. Fig. 6 shows one stage of such a filter. It is a symmetric and repetitive version of the classical all-pass RC - CR filter structure that is classically used for the generation of the quadrature LO signals. Where the amplitude and phase errors of classical RC - CR filters are highly sensitive to absolute variations of the R and C values, this is not the case for the symmetric structure. Due to its repetitive four-input four-output structure, it is possible to put several of these filter stages in cascade, allowing the synthesis of more complex and especially more broad-band transfer functions. The latter makes the filter less sensitive to absolute R and C variations.

III. THE LOW-IF RECEIVER

A. The High Frequency Part

The concept of the low-IF receiver starts from the observation that, as illustrated with (4) and (5), a high frequency signal can be downconverted to a lower frequency (IF) without the problem of the mirror signal suppression when the multiplication is done with a single positive frequency (which can only be represented by a signal pair). Fig. 7 is an illustration of these operations in the frequency domain for both the positive and negative frequencies. Fig. 7(a) shows the downconversion by multiplication with a sine (i.e., a positive and a negative frequency). This operation superimposes the wanted and the mirror signal by bringing them down to the same frequencies. Fig. 7(b) and (c) gives the downconversion by multiplication with a single positive frequency for, respectively, the zero-IF and the low-IF receiver. In the low-IF receiver are the mirror and the wanted signal not superimposed but downconverted to opposite IF frequencies.

The downconversion to an IF by multiplication with a single positive frequency has large consequences. They are illustrated with Fig. 8. It is now not necessary anymore to do any mirror signal suppression at high frequencies before the downconversion and the IF may be situated at low frequencies (about one to two times the bandwidth of the wanted signal). Both aspects result in an integrability that is as good as the integrability of the zero-IF receiver. The zero-IF receiver is

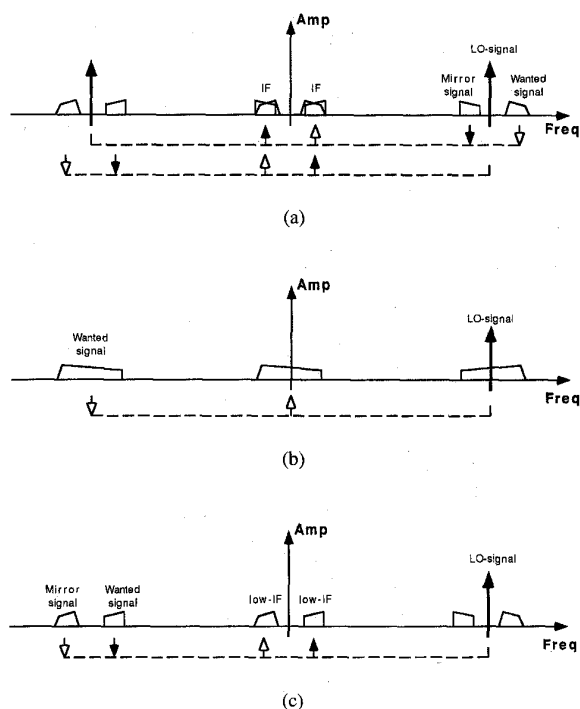


Fig. 7. The downconversion process in (a) an IF receiver. (b) a zero-IF receiver. (c) a low-IF receiver.

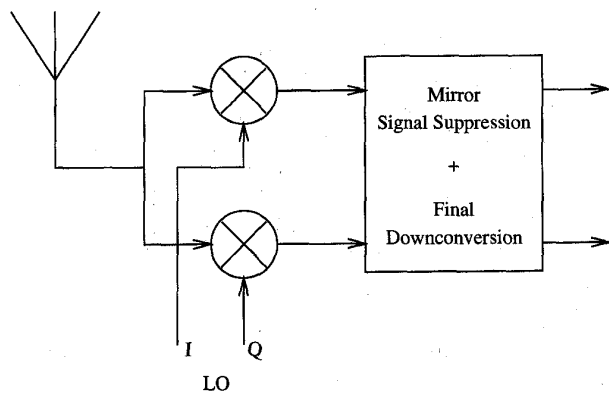


Fig. 8. A downconverter for a low-IF receiver topology.

actually only a special case ($IF = 0$) of a receiver with a downconversion by means of multiplications with a positive frequency. The use of a zero-IF makes the topology however highly sensitive the parasitic baseband signals like dc offset voltages, second-order distortion products and self-mixing products.

The finite matching between the mixers and, more important, the sensitivity of the $RC-CR$ quadrature generator for the LO, make it impossible to generate a perfect single positive frequency. This is not so important for a zero-IF receiver. Here is the mirror signal equal to the wanted signal and a typical 3° phase accuracy (25 dB mirror signal suppression) will suffice for most applications. This is not the case when

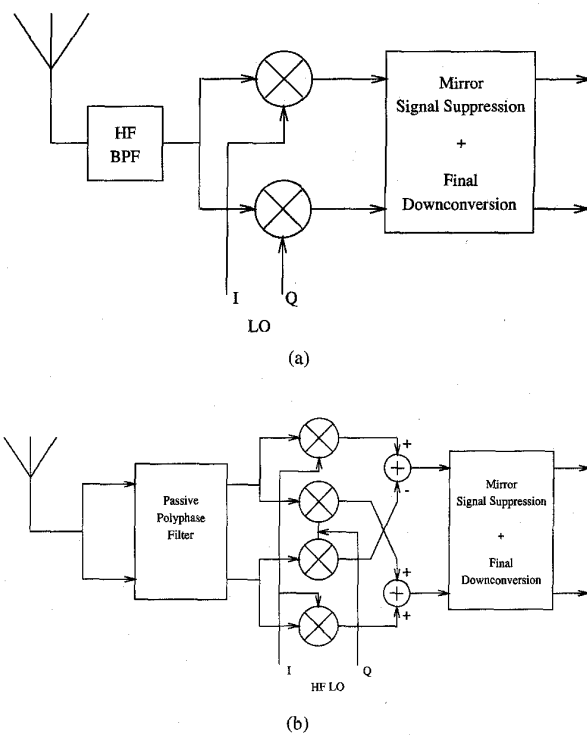


Fig. 9. Low-IF downconversion with (a) an extra external HF filter. (b) a sequence asymmetric polyphase filter.

the downconversion with an imperfect positive frequency is done to an IF frequency. The mirror signal is now completely different from the wanted signal and it can, depending on the application and the exact position of the IF, be up to 20 dB higher than the wanted signal, resulting in a required phase accuracy of 0.3° . This is an accuracy which, with today's typical quadrature downconverters, can only be achieved with the use of extensive tuning and trimming.

It is thus still necessary to do some mirror signal suppression at high frequencies before the downconversion. Fig. 9 gives two possibilities to do this. A quadrature downconverter combined with the classical HF filter, shown in Fig. 9(a), gives only a limited improvement. A HF filter, which can not be integrated, is still necessary, albeit with reduced specifications, and these reduced specifications are only available when still a high IF (between 10 and several hundred MHz) is used. This requires for a further downconversion with a second mixer stage before the wanted signal can be sampled.

A better alternative, which truly combines the advantages of both the IF and the zero-IF receiver, is given in Fig. 9(b). A more close observation of the downconversion process by multiplication with a single frequency component shows that it is only the mirror signal situated at negative frequencies that is superimposed on the wanted signal situated at the IF, while the wanted signal is downconverted from positive frequencies. This means that it is not necessary to suppress the mirror signal at both positive and negative frequencies, as is done with the classical high- Q HF filter. The suppression of only

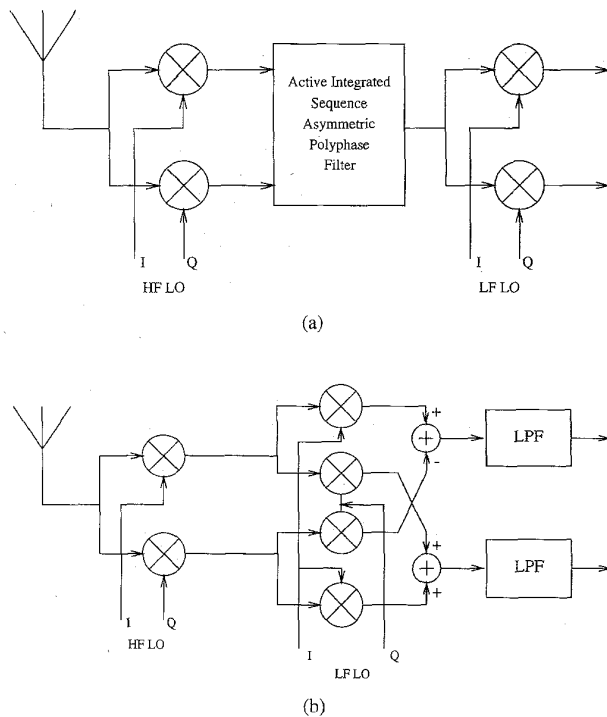


Fig. 10. Further downconversion from IF to baseband with filtering (a) after and (b) before the final downconversion.

the negative frequency components does not require a high Q , even when the wanted and mirror frequency are situated very close to each other (a few hundred kHz). The filtering can be done with a sequence asymmetric polyphase filter. Its output signal will of course be an I, Q -signal pair, requiring for the downconversion mixer the full four-mixer structure of Fig. 1. This new topology is based on the multiplication of two high frequency signals that are both put in quadrature with a quadrature generator. It is therefore called "double quadrature downconverter."

B. The Low Frequency Signal Processing

The structure of Fig. 9(b) allows for the downconversion in quadrature of the wanted signal to a low IF of a few hundred kHz. In this structure is the mirror signal also downconverted to this same low IF. It is the quadrature structure that ensures that both signals can still be separated after downconversion. The wanted signal is situated at the positive frequency components of the quadrature low IF signal, the mirror signal is situated at negative frequencies. In this section is discussed how the mirror signal can be suppressed after the high frequency downconversion and how the wanted signal can be downconverted to the baseband with a final, low frequency, downconversion. In this discussion, it is assumed that the high frequency quadrature downconversion is done with a perfect quadrature downconverter.

There are two ways to separate the wanted signal from the mirror signal at low frequencies: the band-pass filtering of only the positive frequencies with a sequence asymmetric

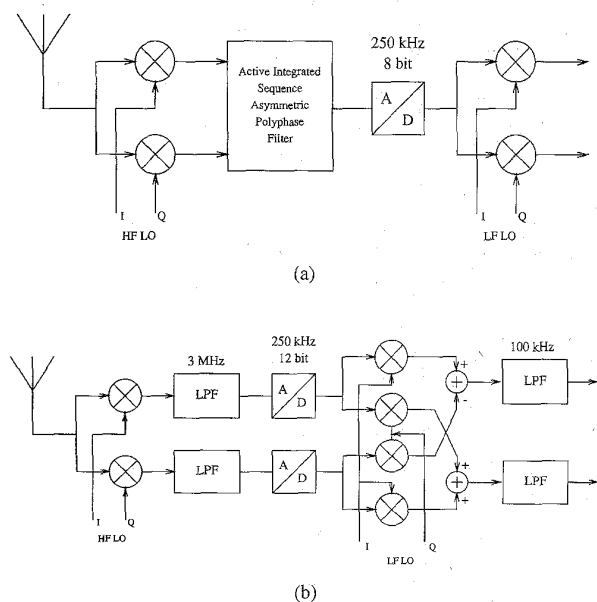


Fig. 11. Direct sampling of the low-IF signal with filtering (a) after and (b) before the A/D-conversion.

polyphase filter followed by a quadrature downconversion, or a further downconversion to baseband by multiplication with a single positive frequency component followed by a low-pass filter operation. Fig. 10 shows both configurations. In both configurations, it is the filter operation that largely reduces the dynamic range of the received signal. A downconversion to baseband can, in the analog domain, only be done with a high accuracy for a low dynamic range signal. High dynamic range signals are too sensitive to parasitic baseband signals. The analog version of Fig. 10(b) is therefore not a good option. The circuit of Fig. 10(a) renders a signal that can be downconverted to baseband without any difficulty. The dynamic range and the center frequencies of the signal after the filter is even so low (e.g., 40 dB and 250 kHz) that it is better sampled at its low IF frequency. This is shown in Fig. 11(a).

The choice between the mirror signal suppression techniques of Fig. 10(a) and (b) is mainly determined on where the conversion from the analog to the digital domain will be performed. Sampling the low frequency signals before the mirror signal has been suppressed, will require an A/D-converter with a larger dynamic range. As the level of integration and the power efficiency of A/D-converters is continuously improving, allowing for ever more digital signal processing and less low frequency analog signal processing, the low frequency mirror signal suppression in the digital domain is becoming ever more feasible. Fig. 11(b) shows a topology in which this is the case. The final downconversion and baseband filtering are now done in the DSP with a high accuracy. The analog front-end implements only a very coarse and broad-band anti-aliasing filtering. The A/D-converters sample a combination of adjacent channels, resulting in a signal with a dynamic range and bandwidth higher than the wanted signal (e.g., 60 dB and 1 MHz). These are specifications that can be achieved at a reasonable area and power cost with today's

embedded A/D-converters. The power cost can even be further reduced by using bandpass $\Sigma\Delta$ -converters that only have to achieve the required dynamic range in the band of the wanted signal [11]. This makes the topology of Fig. 11(b) the preferred topology for the realization of fully integrated high performance receivers. It must of coarse be used in combination with a highly accurate high frequency quadrature downconverter that does not require the use of a high IF. This can be done with the high frequency downconversion topology that has been presented in Fig. 9(b). The properties of this structure, the double quadrature downconverter, are further analyzed in the next section.

IV. THE DOUBLE QUADRATURE DOWNCONVERTER

A. The Double Quadrature Structure

Fig. 12(a) shows the conventional quadrature downconverter. The LO signal is put into quadrature and the downconversion is done twice. Signals situated at a frequency higher than the LO will be downconverted to positive low frequencies. Signals lower than the LO will be downconverted to negative frequencies. With a phase error on the LO signal, signals coming from one side of the LO will also have a signal component coming from the other side of the LO. This is mirror signal crosstalk. This parasitic crosstalk is, according to (7), equal to $\tan(\Delta\varphi)$. For an RC - CR quadrature generator, this phase error is determined by the mismatch between the cutoff frequencies f_c of the pole and the zero of the RC - CR structure. For a certain mismatch, Δf_c is $\tan(\Delta\varphi)$ maximal at f_c and equal to

$$\tan(\Delta\varphi) = \frac{\Delta f_c}{2f_c}. \quad (9)$$

So, a phase error of less than 0.3° requires that the matching between the RC and CR network is better than 1%. This value is then still only achieved in a very small band around f_c . Further away from f_c will the amplitude mismatch of the RC - CR structure dominate, resulting in a very high sensitivity to absolute parameter variations. The limited amplitude matching is often corrected by clipping the quadrature LO signals. A good phase accuracy (better than 1°) can with the RC - CR structure only be achieved by means of extensive tuning and trimming.

Fig. 12(b) shows an alternative for the conventional quadrature downconverter. The RF signal is now put into quadrature and both the HF I - and Q -signals are downconverted with a sine. The effect of a phase error in the quadrature generator are the same: a mirror signal crosstalk equal to $\tan(\Delta\varphi)$. The difference is that this structure can not be used with an RC - CR quadrature generator, as clipping of the RF signal is highly unwanted.

The topology in Fig. 13 is called the double quadrature structure. It is the combination of the structures of Fig. 12: both the RF and the LO signal are put into quadrature. The crosscoupling and combination of the four mixing products makes that the amplitude and phase errors are extra suppressed. The mirror signal crosstalk due to phase and amplitude errors

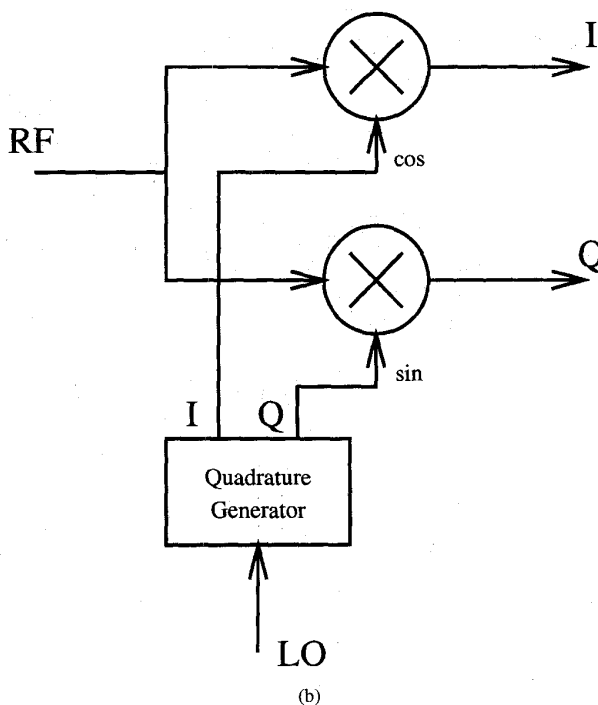
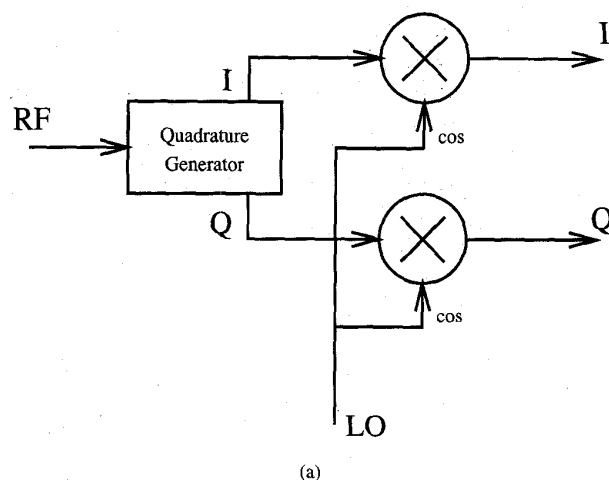


Fig. 12. (a) The conventional quadrature downconverter. (b) an alternative structure.

for this structure is

$$\tan(\Delta\varphi) = \tan(\Delta\varphi_{RF}) \cdot \tan(\Delta\varphi_{LO}) + \frac{\tan(\Delta\varphi_{Mixers})}{2} \quad (10)$$

$$\frac{\Delta A}{A} = \frac{\Delta A_{RF}}{A_{RF}} \cdot \frac{\Delta A_{LO}}{A_{LO}} + \frac{\Delta G}{2G}. \quad (11)$$

Hence, the double quadrature structure is highly insensitive to mismatches in the quadrature generators. Its mirror signal suppression is therefore determined by the matching between the downconversion mixers. The phase mismatch between the downconversion mixers is approximately (f_{BW} is the input

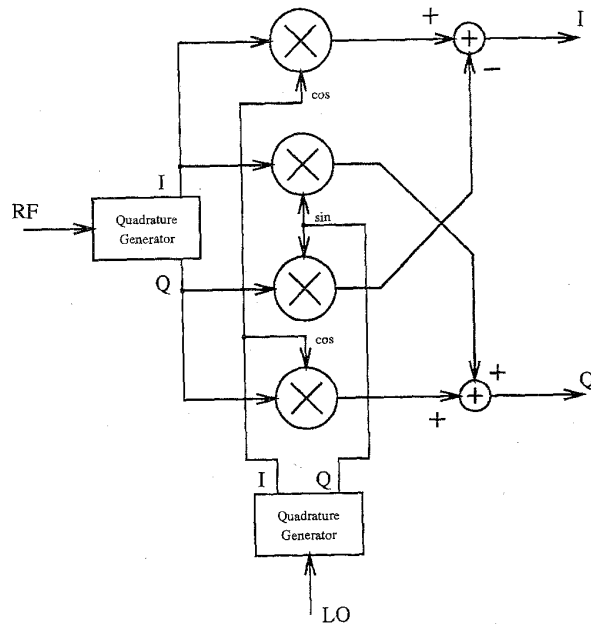


Fig. 13. The double quadrature downconverter topology.

bandwidth of the mixers)

$$\tan(\Delta\varphi) \approx \frac{f_{LO}}{f_{BW}} \cdot \frac{\Delta f_{BW}}{f_{BW}} \quad (12)$$

This means that the phase error can be made low when the mixers have a large input bandwidth. The amplitude error between the mixers is determined by the mismatch in dc conversion gain. It gives a mirror signal crosstalk equal to $\Delta G/2G$, and it is therefore the main remaining source of mirror signal crosstalk. This effect can however easily be eliminated by performing a closely matched digital AGC operation on the sampled low frequency I - and Q -signals in the DSP that does the further processing and demodulation of these signals.

B. The Broad-Band Quadrature Generator

The double quadrature structure requires the use of two quadrature generators that still have a relatively good amplitude and phase matching in a broad passband. Making the quadrature generators broadband eliminates the need for any frequency tuning to compensate for absolute parameter variations.

One stage of a passive sequence asymmetric polyphase filter, as shown in Fig. 6, passes positive sequences and suppresses negative sequences at $1/2\pi RC$. The big advantage of this structure over the classical RC - CR quadrature generator is that several stages can be cascaded. This allows for the synthesis of wideband filters, which largely reduces the sensitivity to absolute parameter variations. Fig. 14 gives the positive and negative frequency response for a two-stage version.

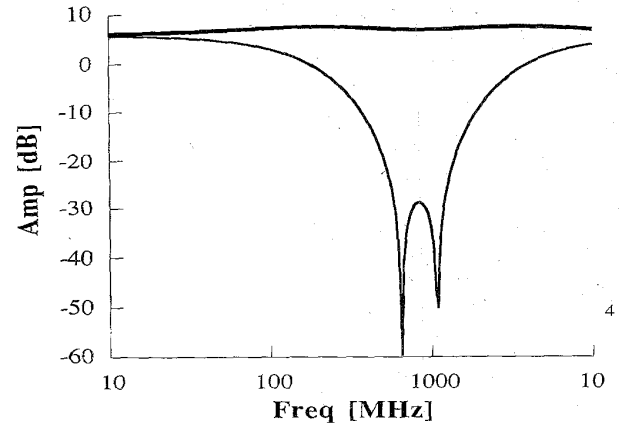


Fig. 14. The transfer function for positive and negative frequencies of a two-stage passive sequence asymmetric polyphase filter.

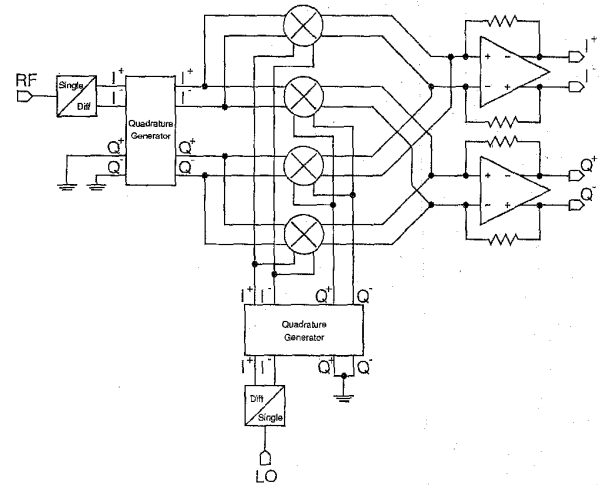


Fig. 15. Block scheme of the realized CMOS receiver front-end chip.

V. FULL CMOS REALIZATION

Fig. 15 shows the block scheme of the realized chip. It has been realized in a standard $0.7 \mu\text{m}$ CMOS technology and does not require any external components, nor does it require any tuning or trimming. First, a single-ended to differential conversion is performed on the RF and LO signal. The circuit schematic of this single ended to differential converter is given Fig. 16. The first stage, with transistor $M1$, performs the conversion. The low-ohmic poly resistors ensure the linearity of the conversion. The dummy transistor $M2$ balances the positive and negative output node. This limits the phase error of the 180° to about 3° at 1 GHz. Transistors $M3p$ and $M3n$ form resistor-loaded amplifiers. They compensate for the 6 dB signal loss of the single ended to differential stage. The resistor loaded single transistor amplifier structure is the only one that can still process 1 GHz signals in $0.7 \mu\text{m}$ CMOS. It does not have a good linearity, but its main distortion components are

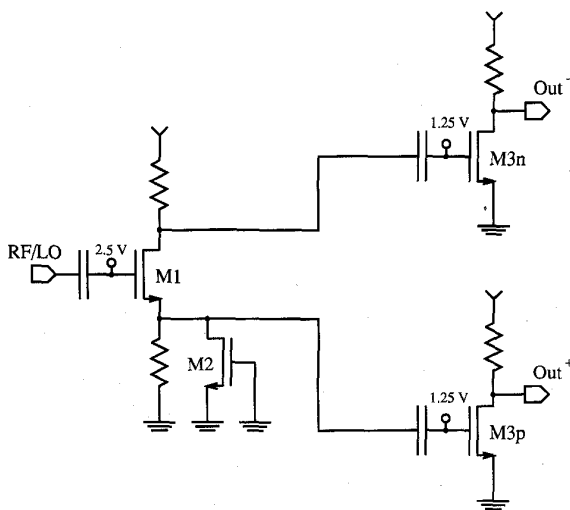


Fig. 16. The single-ended to differential converter.

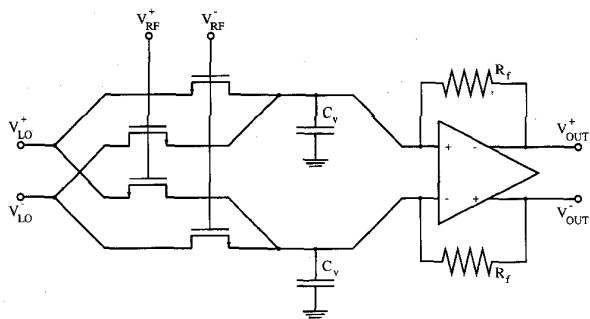


Fig. 17. The highly linear mixer topology.

second order and the second harmonic distortion components are, in this topology, common-mode signals. The common-mode signals pass through the succeeding polyphase filter and are then suppressed at the input of the double-balanced downconversion mixers.

Two two-stage sequence asymmetric polyphase filters are implemented on the chip. Their passband is designed to range from about 600 MHz to 1.2 GHz. The signals at 900 MHz are in this way always set correctly in quadrature, independent of process variations. Amplifier stages are again added after the polyphase filters to compensate for the 6 dB signal loss.

The mixers are realized with a recently developed highly linear CMOS topology for downconverters [12]. This topology is shown in Fig. 17. The mixer is based on crosscoupled nMOS transistors used in the triode area. A high input bandwidth can be achieved with this topology by using small modulating transistors (by applying a large $V_{GS} - V_T$) and large capacitors on the virtual ground nodes. The large capacitors make that the opamp only has to process low frequency signals. This makes it possible to use an opamp with large input transistors, which results in a low noise despite its low power consumption. The four fully balanced downconversion mixers are realized with sixteen HF modulating transistors and two LF opamps.

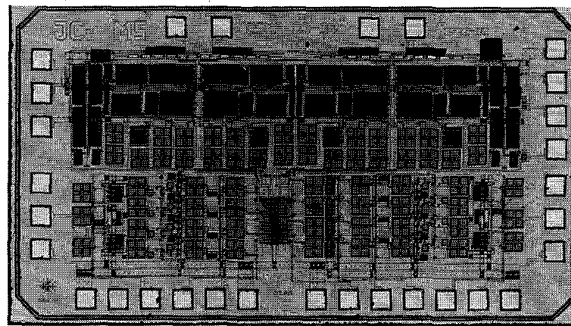


Fig. 18. Microphotograph of the CMOS receiver front-end chip.

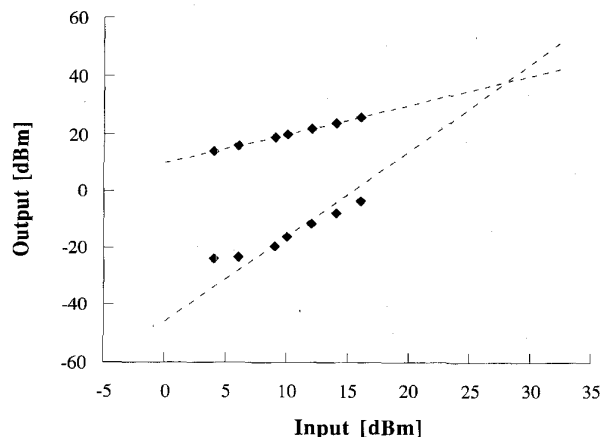


Fig. 19. The third-order interception point measurement (IP3).

VI. MEASUREMENT RESULTS OF THE CMOS FRONT-END CHIP

Fig. 18 shows a microphotograph of the realized chip. It is realized in a standard $0.7\text{ }\mu\text{m}$ CMOS process and measures 6 mm^2 . It operates on a single 5 V power supply voltage and consumes 500 mW , mainly dissipated in the HF resistor loaded amplifiers. The measured conversion gain decays from 16.4 dB at low frequencies to 9.2 dB at 900 MHz . This is equivalent to a 3.1 dB HF signal loss for both the RF and LO signal at 900 MHz . The measured output bandwidth is 3.09 MHz . Fig. 19 shows the third-order interception point (IP3) measurement. The IP3 is 27.9 dBm , the measured noise figure (for a 12 dBm LO signal) is 24.0 dB . The measurements of the phase and amplitude errors in function of frequency are given in Fig. 20. The phase error is less than 0.3° in the $500\text{--}900\text{ MHz}$ band, which is as expected. In this band, the amplitude error is situated at 0.5 dB . These phase and amplitude errors result, after a digital AGC operation, in a mirror signal suppression of 46 dB . Both phase and amplitude errors totally depend on matching. This measurement has therefore been performed on several samples, and all samples show the same or better phase and amplitude errors.

VII. CONCLUSION

A high performance low-IF receiver topology has been presented. This topology combines the advantages of both the IF and the zero-IF receiver: an excellent performance

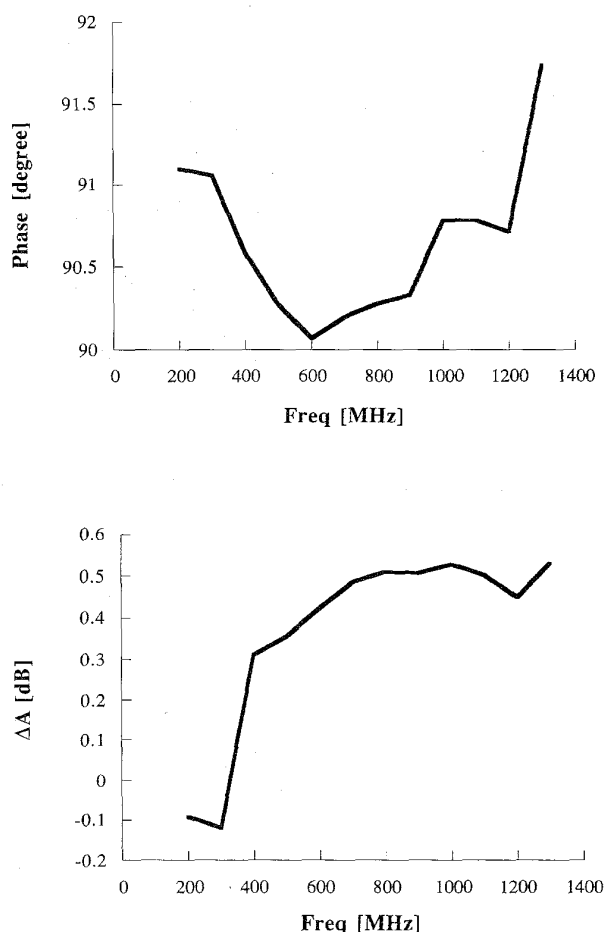


Fig. 20. The measured phase and amplitude errors versus frequency.

and a very high degree of integration. The presented low-IF topology does not require a single external HF or IF filter, and it is at the same time totally insensitive to parasitic baseband signals. A quadrature downconverter with a very high accuracy is a key building block for this low-IF receiver. In this paper, a new quadrature downconverter, called double quadrature downconverter, has been introduced. It achieves a phase accuracy of less than 0.3° in a large passband around 900 MHz without requiring any tuning or trimming. The presented chip is realized in a $0.7\text{ }\mu\text{m}$ CMOS process. It has an IP3 of 27.9 dBm and a noise figure of 24 dB. The chip die area is 6 mm^2 .

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Michel S. J. Steyaert (S'85–A'89–SM'92) for a photograph and biography, see this issue, p. 1482.