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THE CIRCUIT DESIGNER'S COMPANION

Third Edition

Peter Wilson

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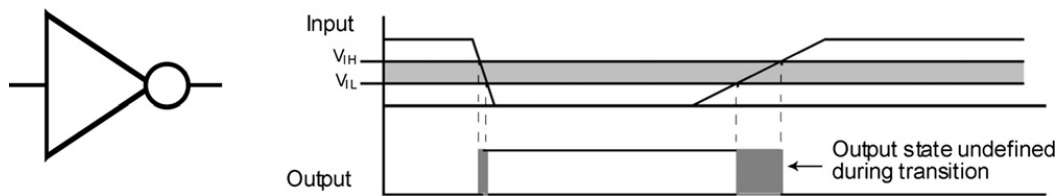


FIGURE 6.1 Transitions through logic thresholds

Each input is designed so that any voltage below one level, conventionally V_{IL} , is regarded as a logic “0” and any voltage above another level, V_{IH} , is regarded as logic “1” (Figure 6.1).

These levels are characterized for each logic or microprocessor family, and worst-case values of V_{IL} and V_{IH} can be found on any data sheet. Note that, as with any hardware-determined parameter, they may vary with temperature and you should ensure that the values you use are guaranteed across the device’s temperature range. They are also a function of supply voltage. If all ICs are fed from the same supply this is not a problem, but it becomes more significant if you are interfacing logic circuits which may be fed from different supply rails.

The significance of the band between V_{IL} and V_{IH} is that the input logic state (and therefore the output state) is undefined while the voltage is in this band. Therefore transitions between logic states must happen as rapidly as possible and no decisions must be taken while the input is in transit, or for a given period (the “settling time”) thereafter. This is why clocked, or synchronous, circuits are normally more reliable than un-clocked or asynchronous ones for complex logic operations: the state of the clock determines when logic decisions are taken, and it is arranged that all data transitions occur when the clock is inactive.

Susceptibility to noise

Provided that all signals to logic inputs, whether from other logic outputs or from interfaces to other circuits, lie outside the V_{IL} – V_{IH} band when they are active, then in theory no misinterpretation of the input should occur. The difference between a “low”-output logic level (V_{OL}) and V_{IL} , or that between a “high”-output level (V_{OH}) and V_{IH} , is the noise immunity (expressed in volts) of the logic interface (Figure 6.2). Notice that noise immunity is not a property of any particular device, but of the interface

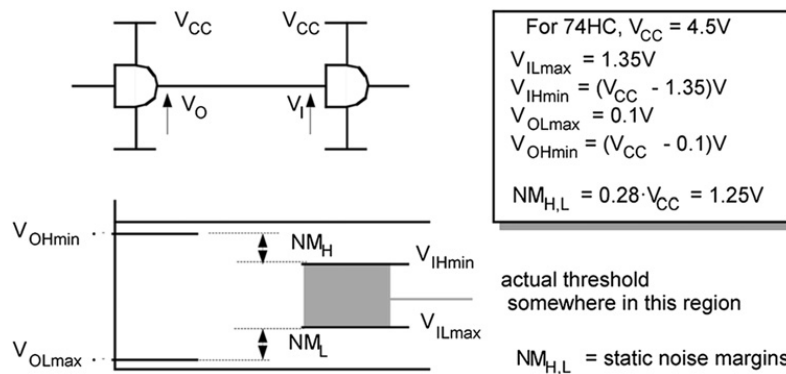


FIGURE 6.2 Noise immunity of a logic interface