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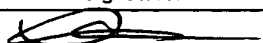
UTILITY PATENT APPLICATION TRANSMITTAL

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Transmitted herewith is a patent application under 37 CFR 1.53(b).

Entitled:	LIGHT EMITTING DIODE LAMP PACKAGE STRUCTURE AND ASSEMBLY THEREOF
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- ☒ 1. Submitted herewith are the following:
- 22 pages of specification, including claims and Abstract.
 - 14 sheet(s) of drawings. (Figs. 1, 2A-2B, 3A-3B, 4A-4B, 5, 6A-6B, 7-16)
 - 24 claim(s).
 - 1 Oath/Declaration signed by each inventor.
 - 1 Application Data Sheet.
 - 1 Assignment of the invention to **SEMISILICON TECHNOLOGY CORP, Taiwan** Cover Sheet, and payment of the \$40 recordal fee.
 - 1 check in the amount of \$ 865.00 including any assignment recordal fee.
- ☒ 2. SMALL ENTITY STATUS IS ASSERTED pursuant to 37 CFR 1.27 for this application.
- ☒ 3. The Commissioner is authorized to credit any overpayment and charge any deficiency in any fees required under 37 CFR 1.16 and/or 1.17, to Deposit Account No. 02-0200.
- ☐ 4. Other: _____

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Light Emitting Diode Lamp Package Structure and Assembly Thereof

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

5 The present invention discloses a light emitting diode (LED) lamp package structure and assembly thereof, more particularly a LED lamp package with light emitting diodes, control integrated circuit (IC) and circuit board encapsulated inside a package body.

DESCRIPTION OF RELATED ART

10 According to the prior art, a light emitting diode (LED) lamp package typically contains a LED chip and two electric conductivity supports. The two electric conductivity supports have a portion each exposed outside the package and are electrically connected to the anode and cathode of the LED chip respectively. This type of LED lamp relies on the two electric conductivity supports for receiving external voltage signal and uses the
15 voltage signal to control its luminosity or flashing pattern.

 In another prior art, the LED package encapsulates simultaneously red, blue and green LED chips and four electric conductivity supports. The four electric conductivity supports have a portion each exposed outside the package. One of the electric conductivity supports serves as a common electrode end for the red, blue and green LED
20 chips, while the other three electric conductivity supports are respectively electrically

chips, while the other three electric conductivity supports are respectively electrically connected to the other electrode of the red, blue and green LED chips inside the package. This type of LED lamp relies on three electric conductivity supports for receiving external voltage signals corresponding to the red, blue and green LED chips and uses those voltage
5 signals to control its luminosity or flashing pattern.

The LED lamp of prior art described above controls its luminosity or flashing through the external voltage signals received by electric conductivity supports, whereas the LED lamp itself does not any autonomous control. In the case of a lamp string comprised of a plurality of interconnected LED lamps, the lamp string controls the
10 luminosity or the flashing pattern of the LED lamps via a controller. As the number of LED lamps in the lamp string increases, the design of such controller becomes more complicated. In addition, LED lamps of prior art do not include a control circuit such that its encapsulated electric conductivity supports lack data input and output pins to exert diverse controls over its luminosity and flashing in a manner similar to data control.

SUMMARY OF THE INVENTION

In view that LED lamps of prior art lack data input and output pins and that the layout and control of the lamp-string circuit are confined by the number of LED lamps in the string, the present invention provides a LED lamp package structure having data input
20 and output pins, and a LED lamp assembly suitable for wiring layout and installation.

An object of the present invention is to provide a LED lamp package having data input and output pins.

Another object of the present invention is to provide a LED lamp assembly that facilitates the mount/dismount of LED lamps and the wiring layout of LED lamp string.

To achieve the aforesaid objects, the LED lamp package of the invention comprises a plurality of light emitting diodes (LEDs), each LED having two electrode ends and one of the electrode ends of each LED being a common electrode end; a control light emitting diode (IC) having a data input electrode and a data output electrode, and electrically connected to the LEDs to control the luminous state of each LED; a circuit board for carrying the LEDs and the control IC; a first electric conductivity support, a second electric conductivity support, a third electric conductivity support and a fourth electric conductivity support, each being electrically connected to the circuit board, the first electric conductivity support being a positive DC voltage pad (Vdd), the second electric conductivity support being connected to the data input electrode, the third electric conductivity support being connected to the data output electrode, the fourth electric conductivity support being a negative DC voltage pad (Vss); and a package body encapsulating the LEDs, the control IC and the circuit board while the first electric conductivity support, the second electric conductivity support, the third electric conductivity support and the fourth electric conductivity support being exposed outside the package body.

The common electrode end is a Vdd pad or a Vss pad.

The LEDs and the control IC are mounted on the same surface of the circuit board or the control IC is mounted on the other surface of the circuit board.

The first electric conductivity support and the fourth electric conductivity support

are connected to two opposing sides or the same side of the package body, and the second electric conductivity support and the third electric conductivity support are connected to two opposing sides of the package body.

The LED lamp package structure further contains a fifth electric conductivity support and a sixth electric conductivity support, the fifth electric conductivity support being a Vdd pad and the sixth electric conductivity support being a Vss pad. The first electric conductivity support and the fifth electric conductivity support are connected to two opposing sides of the package body, the second electric conductivity support and the third electric conductivity support are connected to two opposing sides of the package body, while the fourth electric conductivity support and the sixth electric conductivity support are connected to two opposing sides of the package body.

The two opposing surfaces of the circuit board each carries a red LED, a green LED and a blue LED.

The package body is an injection-molded transparent glue in spherical or semi-spherical shape.

The package body is in rectangular shape having a light emitting window, the LEDs aligning with the light emitting window inside the rectangle.

To achieve the aforesaid objects, the LED lamp assembly provided by the invention comprises a LED lamp having a package body encapsulating a plurality of LEDs and four electric conductivity supports; a lampshade covering the package body of the LED lamp; a socket being a body having a perforation and extended with a plug-in member, the perforation accommodating the LED lamp and enabling the four electric

conductivity supports to expose outside the body; and a mount formed with a socket, the socket having four electrode contacts inside such that when the socket is plugged into the socket, the four electrode contacts are respectively in contact with the four electric conductivity supports.

5 The plurality of LEDs are mounted on a circuit board. The circuit board also carries a control IC. The four electric conductivity supports are respectively a Vdd pad, a data input pad, a data output pad and a Vss pad.

 The four electric conductivity supports have a flat shape and are flexible.

 The upper half of the socket accommodates the body of the socket, and the lower
10 half of the socket is coupled to the plug-in member of the socket.

 The socket forms a through-hole. The four electrode contacts pass through the through-hole to connect to four electrical wires outside respectively.

 To achieve the aforesaid objects, the present invention further provides a LED lamp assembly, comprising a LED lamp consisting of a package body and a circuit board,
15 the package body encapsulating a plurality of LEDs and four electric conductivity supports, the four electric conductivity support being electrically connected to the circuit board, and the circuit board carrying a control IC and forming a positive DC voltage electrode, a data input electrode, a data output electrode and a negative DC voltage electrode; a lampshade covering the package body of the LED lamp; and a mount formed
20 with a socket, the socket having four electrical contacts inside such that when the circuit board of the LED lamp is inserted into the socket, the four electrode contacts are respectively in contact with the positive DC voltage electrode, the data input electrode,

the data output electrode and the negative DC voltage electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is the circuit block diagram of a LED lamp according to the invention.

5 FIG. 2A is a top view of the interior of a LED lamp according to a first embodiment of the invention.

FIG. 2B is a bottom view of the interior of a LED lamp according to a first embodiment of the invention.

10 FIG. 3A and FIG. 3B are side views of the interior of a LED lamp according to a first embodiment of the invention, where the package body is in hemispherical shape and spherical shape respectively.

FIG. 4A and FIG. 4B are structural views of the interior of a LED lamp according to a second embodiment of the invention, wherein the package body has respectively six electrode contacts and four electrode contacts.

15 FIG. 5 is a perspective view of the interior of a LED lamp according to a third embodiment of the invention.

FIG. 6A and FIG. 6B are another perspective views of a LED according to a third embodiment of the invention, wherein the four electric conductivity supports are distributed at four corners.

20 FIG. 7 is yet another perspective view of the interior of a LED lamp according to a third embodiment of the invention, wherein the four electric conductivity supports are linearly arranged.

FIG. 8 is yet another perspective view of the interior of a LED lamp according to a third embodiment of the invention, wherein the LEDs and a part of circuit board encapsulated inside the package body.

FIG. 9 is an exploded view of a LED lamp assembly according to a fourth
5 embodiment of the invention.

FIG. 10 is a perspective view of the mount in the fourth embodiment of the invention.

FIG. 11 is an exploded view of a LED lamp assembly according to a fifth embodiment of the invention.

10 FIG. 12 is an exploded view of a LED lamp assembly according to a sixth embodiment of the invention.

FIG. 13 is a top view of the socket in the sixth embodiment of the invention.

FIG. 14 is a side view of the lampshade, LED lamp and socket in the sixth embodiment of the invention.

15 FIG. 15 is a top view of the mount in the sixth embodiment of the invention.

FIG. 16 is a sectional view of the mount in the sixth embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The technical contents, features and effects of the invention are described in detail
20 below with embodiments in reference to the accompanying drawings.

FIG. 1 shows the circuit block diagram of a LED lamp according to the invention. According to a preferred embodiment of the invention, the LED lamp 10 comprises a red

light emitting diode (R LED) 11, a blue light emitting diode (B LED) 11 and a green light emitting diode (G LED) 11, and a control integrated circuit (IC) 12, the components being mounted on a circuit board 13. The wiring layout of the circuit board 13 enables the control IC 12 to electrically connect the red, blue and green LEDs 11 respectively. The red, blue and green LEDs 11 have a common electrode end, the common electrode end being a Vdd pad. In a different embodiment of the invention, the LED lamp 10 comprises a red light emitting diode (R LED) 11, a blue light emitting diode (B LED) 11, a green light emitting diode (G LED) 11 and a white light emitting diode (W LED) mounted on the same side surface of the circuit board 13; the common electrode end can also be a Vss pad.

The LED lamp 10 has a data input pin Din and a data output pin Dout. The control IC 12 receives external control data via the Din, and controls the luminosity or flashing of LED 11 according to said control data, and outputs the control data via the Dout. In addition, the LED lamp 10 has power supply pins Vdd and Vss to receive a DC voltage.

According to a preferred embodiment of the invention, the LED lamp 10 has a package body 19 to encapsulate the circuit board 13 mounted with a plurality of LEDs 11 and a control IC 12 and four electric conductivity supports, the four electric conductivity supports being respectively a Vdd end, a Din end, a Dout end and a Vss end, a portion of the four electric conductivity supports being exposed outside the package body 19, and the four electric conductivity supports being electrically connected to the circuit board 13 inside the package body 19.

Referring to FIG. 2A and FIG. 2B which are respectively a top view and a bottom view of the interior of the LED lamp according to a first embodiment of the invention, the

first embodiment is a first package structure implemented based on the LED lamp 10 shown in FIG. 1, where one side of the circuit board 13 carries four LEDs 11, which are respectively R LED, B LED, G LED and W LED, while the other side of the circuit board 13 carries a control IC 12. The circuit board 13 is encapsulated in a package body 19 to form a LED lamp 10. The package body 19 is preferably transparent glue having a hemispherical shape as shown in FIG. 3A or a spherical shape as shown in FIG. 3B. The package body 19 can also have a shell body to enclose the circuit board 13 mounted with the plurality of LEDs 11 and the control IC 12. In addition, as in the embodiment shown in FIG. 3B, both sides of the circuit board 13 carry R LED, B LED, G LED and W LED 11 simultaneously such that the entire sphere of the package body 19 illuminates uniformly.

Again referring to FIG. 2A and FIG. 2B, in a first embodiment of the invention, the LED lamp 10 contains six electric conductivity supports exposed outside the package body 19 with three electric conductivity supports each being disposed at two opposing sides of the circuit board 13, wherein the Din electric conductivity support and the Dout electric conductivity support are respectively disposed at two opposing sides of the circuit board 13, while the Vdd ends are two electric conductivity supports disposed at two opposing sides of the circuit board 13. Similarly the Vss ends are two electric conductivity supports disposed at two opposing sides of the circuit board 13. In addition, the six electric conductivity supports can be replaced by a conductive wire to form a lamp string. The conductive wire is soldered to the circuit board 13 and encapsulated inside the package body 19.

According to the first embodiment of the invention, the LED lamps 10 can also be serially connected into a lamp string. Given that the same side of the circuit board 13 has a Vdd electric conductivity support and a Vss electric conductivity support, the Vdd ends and the Vss ends of two adjacent LED lamps 10 can be directly electrically connected. As the Din electric conductivity support and the Dout electric conductivity support are respectively disposed at two opposing sides of the circuit board 13, the Din of a LED lamp 10 can be directly electrically connected to the Dout of the previous-level LED lamp 10, while its Dout can be directly electrically connected to the Din of the next-level LED lamp 10.

According to the first embodiment the LED lamp 10 of the invention, the spherical or hemispherical package structure makes it easier for the lamp string to lay down straight or hang down naturally. The electric conductivity supports at power supply end and the electric conductivity supports at data input and output ends are parallelly arranged such that in serial connection, the LED lamps 10 would not protrude because of the wiring, but are arranged evenly. The illumination of the lamp string can also be single-sided or double-sided as shown in FIG. 3A and FIG. 3B. Such lamp string can be used in ornaments that prefer a flat shape, such as a lamp screen.

Referring to FIG. 4A and FIG. 4 B which are structural views of the interior of a LED lamp 10 according to a second embodiment of the invention, wherein the package body 19 has respectively six electrode contacts and four electrode contacts. The second embodiment is a second package structure implemented based on the LED lamp 10 shown in FIG. 1. In comparison with the first embodiment, the second package body 19 of the

second package structure has a rectangular shape that conforms to 5050 or 3528 package specifications and has a light emitting window 191. The LEDs 11 inside the package body 19 aligns with the light emitting window 191.

5 In the second embodiment, the rectangular package body 19 has six electrodes disposed at two opposing sides or four electrodes disposed at two opposing sides. Inside the package body 19, the circuit board 13 is electrically connected with the electrodes 14, 15, 16, 17 via conductive metal wire 18. As in the package body 19 shown in FIG. 4A, the Din and Dout electrodes 16, 17 are respectively disposed at two opposing sides of the package body 19, while Vdd has two electrodes 14 respectively disposed at two opposing
10 sides of the package body 19. Similarly, Vss also has two electrodes 15 respectively disposed at two opposing sides of the package body 19. As in the package body 19 shown in FIG. 4B, the Din and Dout electrodes 16, 17 are respectively disposed at two opposing sides of the package body 19, while Vdd electrode 14 and Vss electrode 15 are respectively disposed at two opposing sides of the package body 19.

15 According to the LED lamp 10 in the second embodiment, the package body 19 has on right side and left side each three electrode contacts that is suitable for use in printed circuit board (PCB) or light bar that requires SMD solder. The LED lamp 10 in the second embodiment with light dissipating from the top center transparent light emitting window is suitable for light bars surrounding a sign board or a place with limited
20 space that requires decoration. In light that the control IC is encapsulated in the package body 19, the LED lamps 10 can be interconnected in series or in parallel for the lamp string to work.

FIG. 5 is a perspective view of the interior of a LED lamp according to a third embodiment of the invention. The third embodiment is a third package structure implemented based on the LED lamp 10 shown in FIG. 1. In comparison with the first and the second embodiments, the package body 19 of the third package structure has a cylindrical shape with four electric conductivity supports 21, 22, 23, 24 exposed from the bottom of the cylindrical package. Inside the package body 19, the plurality of LEDs 11 are disposed on the top surface of the circuit board 13 to emit light upward, while the control IC 12 is disposed on the other side of the circuit board 13.

The LED lamp 10 in the third embodiment is the most commonly applied style and more readily accepted by the public. It is suitable for applications in electronic screen and TV wall.

FIG. 6A and FIG. 6B are another perspective views of a LED according to a third embodiment of the invention, wherein the four electric conductivity supports are distributed at four corners. In this embodiment, the LED lamp 10 contains a plurality of LEDs 11, a control IC 12 and four electric conductivity supports 21, 22, 23, 24 encapsulated in the package body 19 with the four electric conductivity supports 21, 22, 23, 24 exposed from the bottom of the package body 19, wherein the plurality of LEDs 11 and the control IC 12 are mounted at one end of the electric conductivity supports. FIG. 6B is top view clearly illustrating the interior layout of the package body 19. Electric conductivity support 21 is the common electrode end of the plurality of LEDs 11, i.e. a Vdd electrode. Inside the package body 19, one end of electric conductivity support 21 forms a platform for carrying the plurality of LEDs 11, while one end of electric

conductivity support 22 also forms a platform for carrying the control IC, and conductive metal wires 18 are used to achieve electrical connection between the components without relying on a circuit board 13 to carry the plurality of LEDs 11 and control IC 12.

FIG. 7 is yet another perspective view of the interior of a LED lamp according to a third embodiment of the invention, wherein the four electric conductivity supports are linearly arranged. The embodiments shown in FIG. 7 and FIG. 6A differ only in the layout of electric conductivity supports 21, 22, 23, 24. In FIG. 7, the four electric conductivity supports 21, 22, 23, 24 are linearly arranged.

FIG. 8 is yet another perspective view of the interior of a LED lamp according to a third embodiment of the invention, the figure in this embodiment, the LED lamp encapsulated inside a plurality of the LED 11 and a part of the circuit board 13 being inside said package body. However, a plurality of the LED 11 is mounted a platform of the circuit board 13 being inside said package body, and complete electrical connection from the conductive metal wires 18. Beside, an IC 12 is mounted on a part of the circuit board, and a part of the circuit board 13 being outside said package body formed with a positive DC voltage pad 14, a data input pad 16 (the picture doesn't shown), a data output pad 17 (the picture doesn't shown), and a negative DC voltage pad 15. Said circuit board 13 has wiring to be electrically connected to the control circuit 12, the electrode 14, 15, 16, 17 and the LED. Therefore, the embodiment does not mount a plurality of LED 11 by electric conduction support.

FIG. 9 is an exploded view of a LED lamp assembly according to a fourth embodiment of the invention. The LED lamp assembly in the fourth embodiment

comprises: a LED lamp 10, a lampshade 40 and a mount 60. The LED lamp 10 contains a package body 19 and a circuit board 13. The lampshade 40 covers the package body 19 of LED lamp 10. The package body 19 encapsulates tri-color LED 11 and four electric conductivity supports 21, 22, 23, 24. The four electric conductivity supports 21, 22, 23, 24 are electrically connected to the circuit board 13. The circuit board 13 carries a control IC 12 and forms a positive DC voltage electrode 14, a data input electrode 16, a data output electrode 17 and a negative DC voltage electrode 15.

The mount 60 of the LED lamp assembly forms a socket 61, the socket 61 having four electrode contacts 31, 32, 33, 34 therein. When the circuit board 13 of the LED lamp 10 is inserted into the socket 61, the four electrode contacts 31, 32, 33, 34 are in contact respectively with the Vdd end, Din end, Dout end and Vss end of electric conductivity supports. In addition, to increase the contact area between the four electrode contacts 31, 32, 33, 34 and electrodes 14, 15, 16, 17 of circuit board 13, the contact surface of electrode contacts 31, 32, 33, 34 can have an arc surface as shown in FIG. 10.

According to the LED lamp assembly in the fourth embodiment, a lamp string can form a connection structure with a plurality of mounts 60 where each mount 60 can be easily coupled with the LED lamp 10 and its lampshade 40. If a LED lamp 10 is damaged, the service personnel can replace the LED lamp 10 on the mount 60 without dismantling the connection structure of the lamp string.

FIG. 11 is an exploded view of a LED lamp assembly according to a fifth embodiment of the invention. In the fifth embodiment, a LED lamp assembly is conveniently implemented in a lamp string wherein the LED lamp 10 contains a circuit

board 13. The circuit board 13 has electrodes arranged on two opposing sides, wherein the center electrodes on two sides are respectively Din end and Dout end, while the electrodes on either side of the Din end correspond to the electrodes on either side of the Dout end, which are respectively Vdd end and Vss end. At the center of the circuit board 13, a transparent glue encapsulates a plurality of LEDs and a control IC. The two electrode-mounted sides of the circuit board 13 can be inserted into the socket 61 of mount 60 respectively where the wiring of the mount 60 provides the electrical connection of the lamp string. In addition, there is provided a lampshade 40 between the two mounts 60 to accommodate the LED lamp 10.

FIG. 12 is an exploded view of a LED lamp assembly according to a sixth embodiment of the invention. In the sixth embodiment, a LED lamp assembly comprises: a lampshade 40, a LED lamp 10, a socket 50 and a mount 60. The LED lamp 10, which can be a LED lamp shown in FIG. 5 or a conventional LED lamp without a control IC, has four electric conductivity supports 21, 22, 23, 24. The LED lamp assembly is assembled by covering the package body of LED lamp 10 with the lampshade 40 then the LED lamp is mounted into the socket 50 as shown in FIG.14. A lamp string can be fabricated by having a plurality of mounts 60 form a connection structure where each mount 60 can be easily plugged into the socket 50 as shown in FIG. 14. If a LED lamp 10 is damaged, the service personnel can replace the LED lamp 10 on the mount 60 without dismantling the connection structure of the lamp string.

FIG. 13 is a top view of the socket 50 in the sixth embodiment of the invention. The socket 50 has a body 51 with a perforation 52 and a plug-in member 53 extended

from the bottom of the body 51. The plug-in member 53 has a cross shape to facilitate coupling with the mount 60. The perforation 52 is divided into four small holes by the cross-shaped plug-in member 53. When the body 51 accommodates the LED lamp 10, the four electric conductivity supports 21, 22, 23, 24 align with the four small holes
5 respectively and become exposed outside the body 51. In this embodiment, the four electric conductivity supports 21, 22, 23, 24 are flat shape and flexible. Thus the electric conductivity supports 21, 22, 23, 24 can be folded easily as shown in FIG. 14 illustrating the assembly of a lampshade 40, a LED lamp 10 and a socket 50.

FIG. 15 is a top view of the mount 60 in the sixth embodiment of the invention.
10 The mount 60 is formed with a socket 61, the socket 61 having four electrode contacts 31, 32, 33, 34 inside. When the socket 50 is plugged into the socket 61, the four electrode contacts 31, 32, 33, 34 are respectively in contact with the four electric conductivity supports 21, 22, 23, 24 of the LED lamp 10. In addition, the socket 61 has a cross-shaped slot to be coupled with the cross-shaped plug-in member 53 of the socket 50.

FIG. 16 is a sectional view of the mount along line A as shown in FIG. 15. FIG. 16 clearly shows that the socket 61 forms a through-hole, the upper half of the through-hole accommodating the body 51 of the socket 50, and the lower half of the through-hole forming a cross-shaped slot to couple with the plug-in member 53 of the socket 50, while the four electrode contacts 31, 32, 33, 34 inside the socket 61 are segregated by the cross-shaped slot and extended to the bottom of the mount 60 to connect externally with the wiring of lamp string.

What is claimed is

1. A LED lamp package structure, comprising:

a plurality of light emitting diodes, each light emitting diode having two electrode ends and one of the electrode ends being a common electrode end;

5 a control integrated circuit, having a data input electrode and a data output electrode and electrically connected to the light emitting diodes to control the illumination state of each light emitting diode;

10 a first conductor, a second conductor, a third conductor, and a fourth conductor, the first conductor being a positive DC voltage pad, the second conductor being connected to the data input electrode, the third conductor being connected to the data output electrode, the fourth conductor being a negative DC voltage pad; and

a package body encapsulating the light emitting diodes, the control integrated circuit and the conductors, a portion of the first conductor, the second conductor, the third conductor, and the fourth conductor being exposed outside the package body.

15 2. The light emitting diode lamp package structure according to claim 1, wherein the common electrode end is a positive DC voltage pad or a negative DC voltage pad.

3. The light emitting diode lamp package structure according to claim 1, further comprising a circuit board carrying the light emitting diodes and the control integrated circuit.

20 4. The light emitting diode lamp package structure according to claim 3, wherein the light emitting diodes and the control integrated circuit are mounted on the same surface of the circuit board.

5. The light emitting diode lamp package structure according to claim 3, wherein the light emitting diodes are mounted on one surface of the circuit board and the control integrated circuit is mounted on the other surface of the circuit board.

6. The light emitting diode lamp package structure according to claim 1, wherein the conductors are an electric conductivity support or a conductive wire.
7. The light emitting diode lamp package structure according to claim 1, wherein the first conductor forms a platform inside the package body, said platform carrying the light emitting diodes, and the first conductor being electrically connected to the light emitting diodes.
8. The light emitting diode lamp package structure according to claim 1, wherein the fourth conductor forms a platform inside the package body, the platform carrying the control integrated circuit, and the fourth conductor being electrically connected to the control integrated circuit.
9. The light emitting diode lamp package structure according to claim 1, wherein the first conductor and the fourth conductor are connected to two opposing sides of the package body, and the second conductor and the third conductor are connected to two opposing sides of the package body.
10. The light emitting diode lamp package structure according to claim 1, wherein the first conductor and the fourth conductor are connected to the same side of the package body, while the second conductor and the third conductor are connected to two opposing sides of the package body.
11. The light emitting diode lamp package structure according to claim 1, further comprising a fifth conductor and a sixth conductor, the fifth conductor being a positive DC voltage pad and the sixth conductor being a negative DC voltage pad.
12. The light emitting diode lamp package structure according to claim 11, wherein the first conductor and the fifth conductor are connected to two opposing sides of the package body, the second conductor and the third conductor are connected to two opposing sides of the package body, while the fourth conductor and the sixth conductor are connected to two opposing sides of the package body.
13. The light emitting diode lamp package structure according to claim 3, wherein two

opposing surfaces of the circuit board each carrying a redlight emitting diode, a green light emitting diode, and a bluelight emitting diode.

14. The light emitting diode lamp package structure according to claim 1, wherein the package body is an injection-molded transparent glue in spherical or hemispherical shape.

15. The light emitting diode lamp package structure according to claim 1, wherein the package body is in rectangular shape, said rectangle having a light emitting window, the light emitting diodes aligning with the light emitting window inside the rectangle.

16. A light emitting diode lamp assembly, comprising:

a light emitting diode lamp having a plurality of light emitting diodes and four electric conductivity supports encapsulated in a package body;

a lampshade covering the package body of the light emitting diode lamp;

a socket being a body having a perforation and extended with a plug-in member, the perforation accommodating the light emitting diodes and enabling the four electric conductivity supports to expose outside the body; and

a mount formed with a socket, the socket having four electrode contacts inside such that when the socket is plugged into the socket, the four electrode contacts being in contact with the four electric conductivity supports respectively.

17. The light emitting diode lamp assembly according to claim 16, wherein the plurality of light emitting diodes are mounted on a circuit board, the circuit board carrying a control integrated circuit, the four electric conductivity supports being respectively a positive DC voltage pad, a data input end, a data output end, and a negative DC voltage pad.

18. The light emitting diode lamp assembly according to claim 16, wherein the four electric conductivity supports have a flat shape and are flexible.

19. The light emitting diode lamp assembly according to claim 16, wherein the upper half of the socket accommodates the body, while the lower half of the body is coupled to the plug-in member.

5 20. The light emitting diode lamp assembly according to claim 16, wherein the socket forms a through-hole, the four electrode contacts passing through the through-hole to connect with four external wires respectively.

21. A light emitting diode lamp assembly, comprising:

10 a light emitting diode lamp having a package body and a circuit board, the package body encapsulating a plurality of light emitting diodes and four electric conductivity supports, the four electric conductivity supports being electrically connected to the circuit board, and the circuit board carrying a control integrated circuit and forming a positive DC voltage electrode, a data input electrode, a data output electrode and a negative DC voltage electrode;

a lampshade covering the package body of the light emitting diode lamp; and

15 a mount formed with a socket, the socket having four electrode contacts inside such that when the circuit board of the light emitting diode lamp is plugged into the socket, the four electrode contacts being in contact with the positive DC voltage electrode, the data input electrode, the data output electrode and the negative DC voltage electrode respectively.

20 22. A light emitting diode lamp assembly, comprising:

25 a light emitting diode lamp having a package body and a circuit board, the package body encapsulating a plurality of light emitting diodes and a control integrated circuit disposed on one side of the circuit board, a plurality of electrodes being disposed at two opposing sides of the circuit board, wherein the two opposing sides of the circuit board are respectively disposed with a data input electrode and a data output electrode;

a lampshade covering the periphery of the light emitting diode lamp; and

two mounts, each mount formed with a socket, the socket having electrode contacts inside corresponding to the electrodes of the circuit board, wherein the sockets of the two mounts are respectively coupled to the two opposing sides of the circuit board of light emitting diode lamp, and the lampshade is situated between the two mounts.

23. A package structure of the light emitting diode lamp, comprising:

a plurality of light emitting diodes, each light emitting diode having two electrode ends and one of the electrode ends being a common electrode end;

a circuit board, mounting a plurality of light emitting diodes;

a package body, encapsulating said light emitting diodes and a part of said circuit board; and

a control integrated circuit, having a data input electrode and a data output electrode and electrically connected to said light emitting diodes to control the illumination state of each light emitting diode;

wherein said circuit board being exposed outside the part of the package body carrying said control integrated circuit, and said circuit board having a first conduct electricity, a second conduct electricity, a third conduct electricity, and a fourth conduct electricity being exposed outside the package body;

24. The light emitting diode lamp package structure according to claim 23, wherein said first conduct electricity is the positive DC voltage end, said second conduct electricity connecting said data output electrode, said third conduct electricity connecting said data output electrode, and said fourth conduct electricity is the negative DC voltage end.

Light Emitting Diode Lamp Package Structure and Assembly Thereof

ABSTRACT

The present invention provides a light emitting diode (LED) lamp package structure characterized in which a plurality of light emitting diodes, a control integrated circuit, a circuit board and four electric conductivity supports are encapsulated inside a package body where the electric conductivity supports are respectively a Vdd pad, a data input pad, a data output pad, and a Vss pad. The present invention further provides a LED lamp assembly, comprising a LED lamp, a lampshade, a socket, and a mount formed with a socket. After the LED lamp is mounted on the socket with the four electric conductivity supports exposed and the socket is plugged into the socket of the mount, the electric conductivity supports would contact the four electrode contacts in the socket where the four electrode contacts are respectively a positive DC voltage electrode, a data input electrode, a data output electrode and a negative DC voltage electrode.

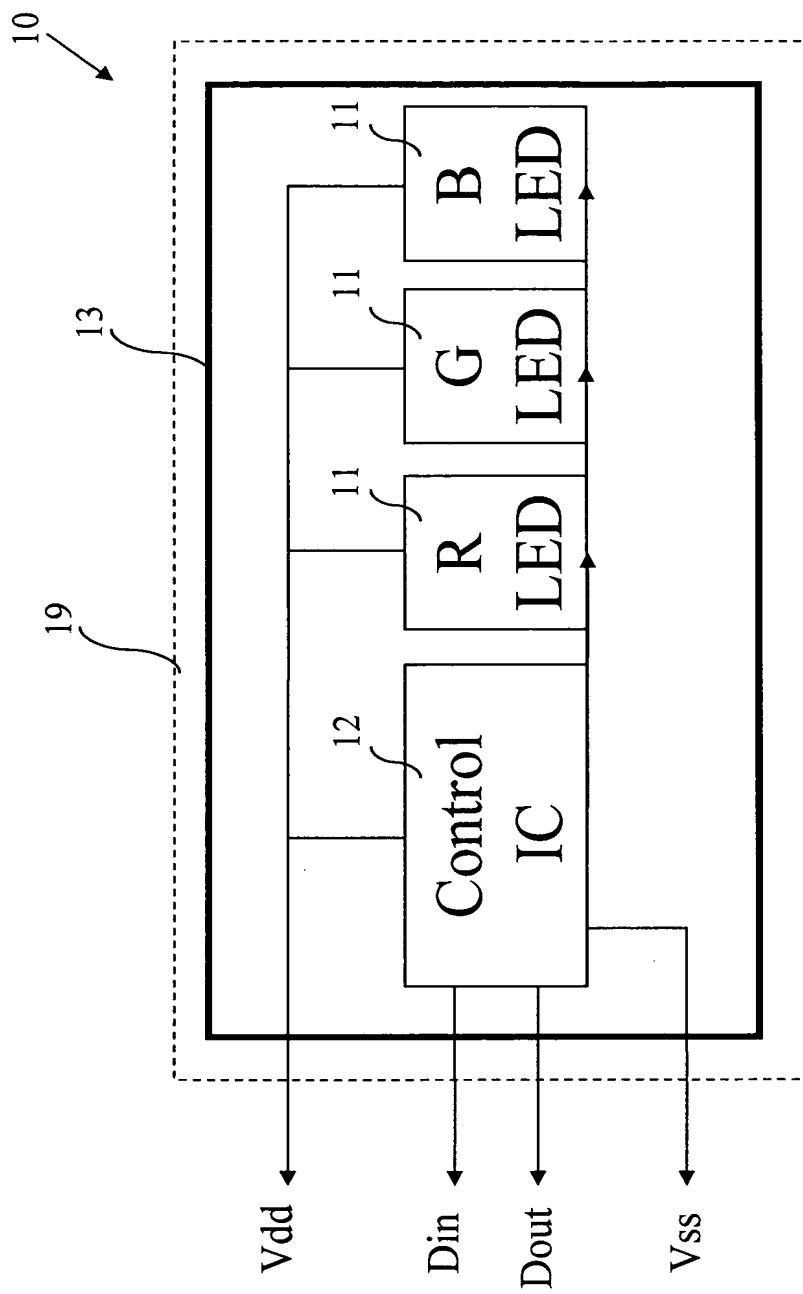


FIG.1

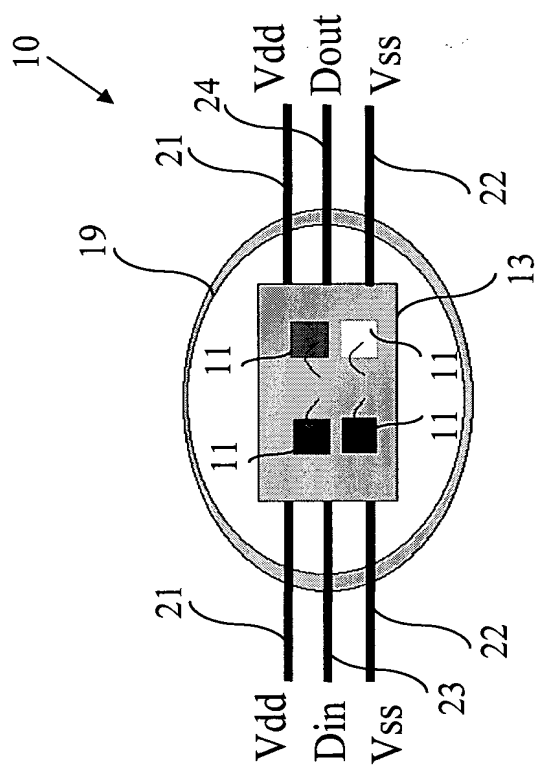


FIG. 2A

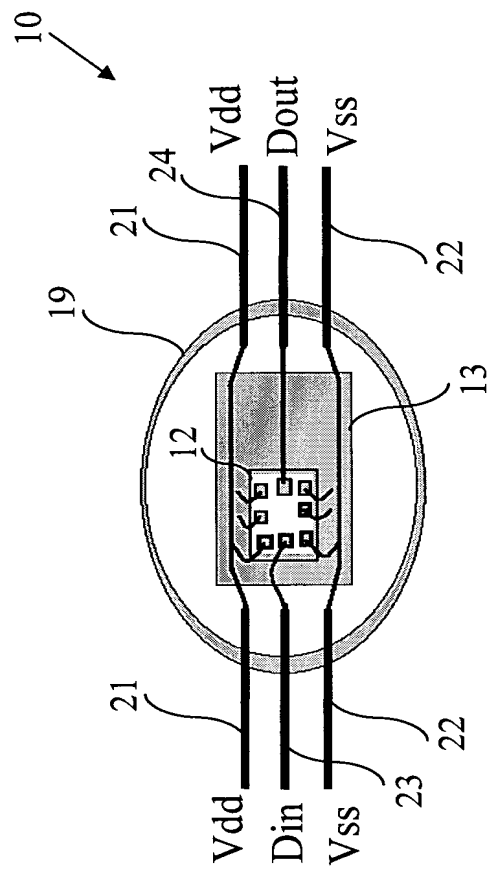


FIG. 2B

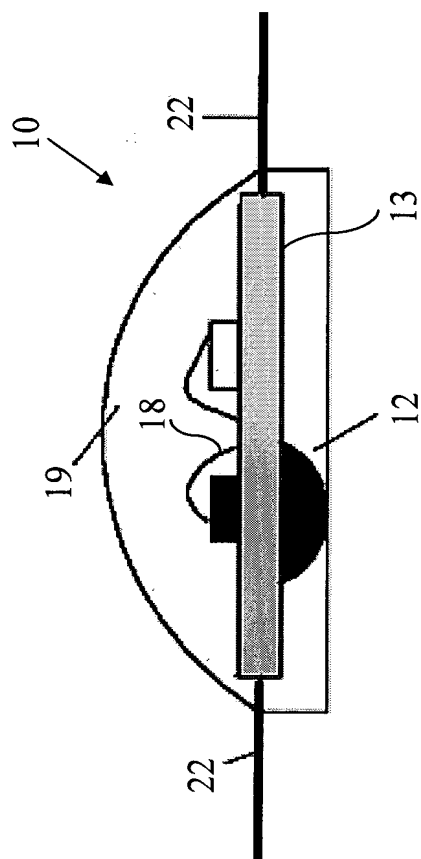


FIG. 3A

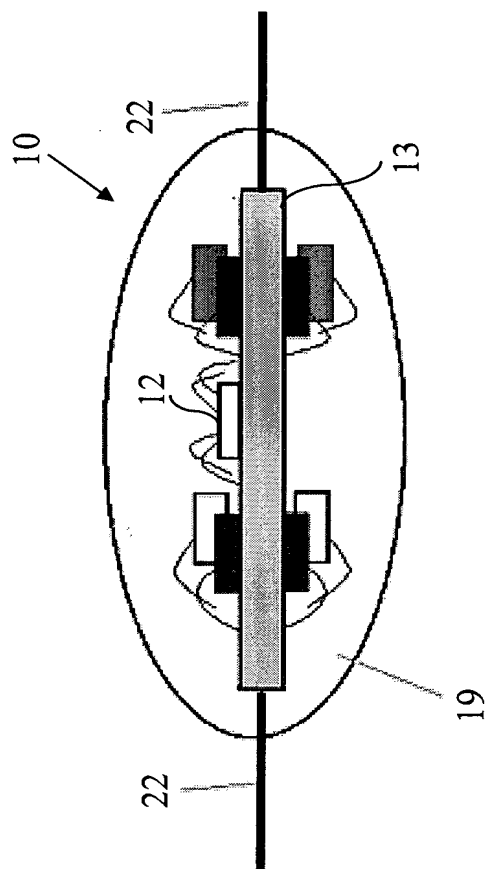


FIG. 3B

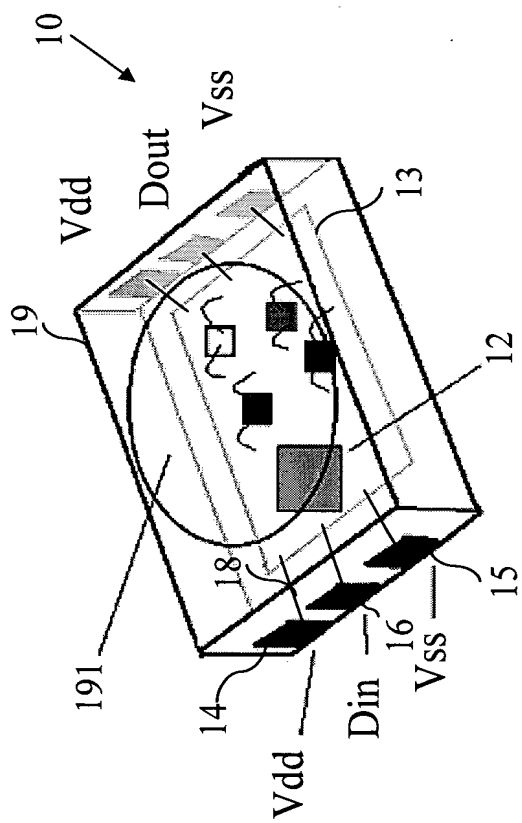


FIG. 4A

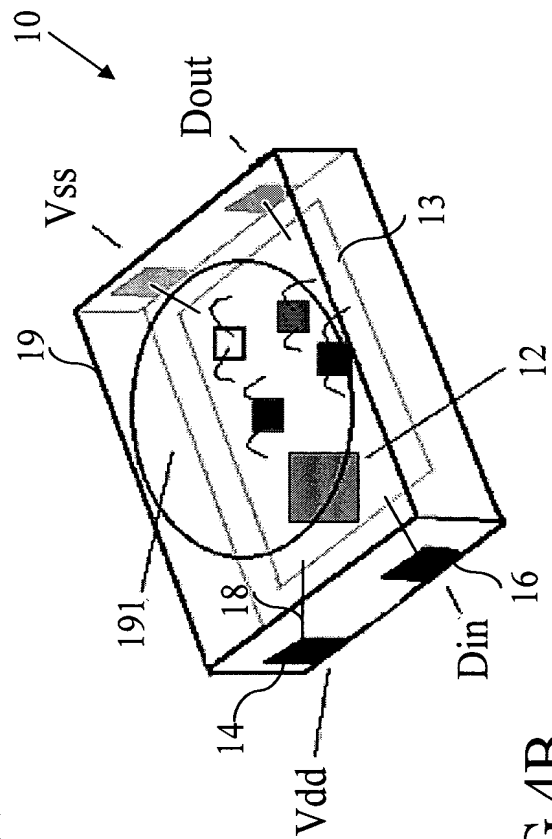


FIG. 4B

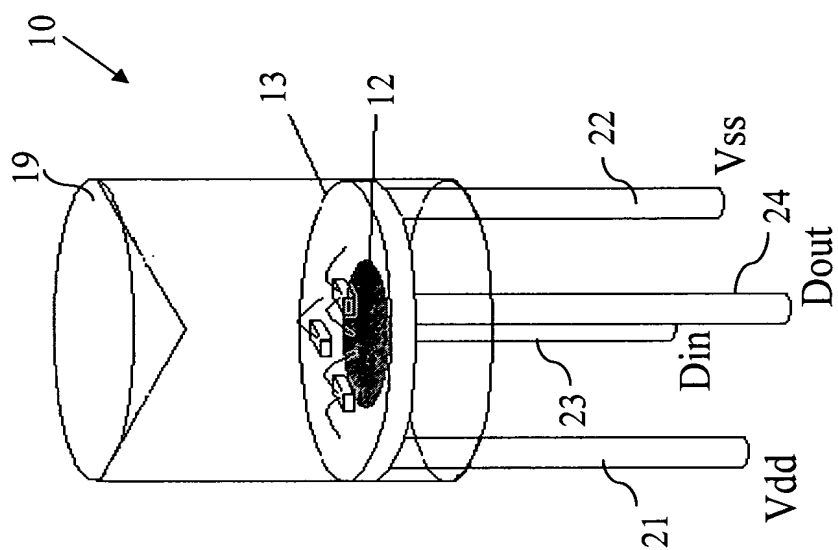


FIG.5

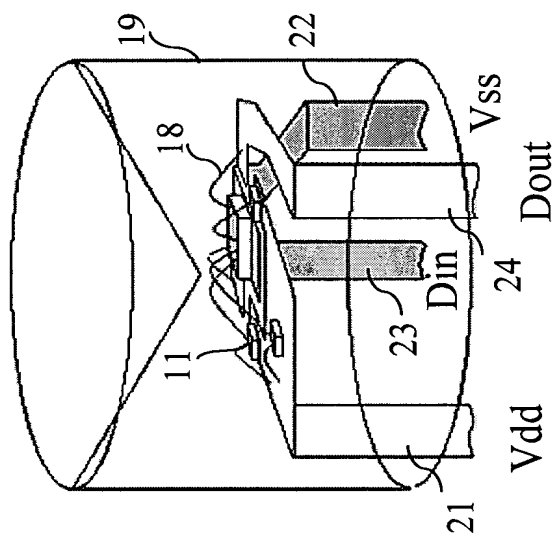


FIG. 6A

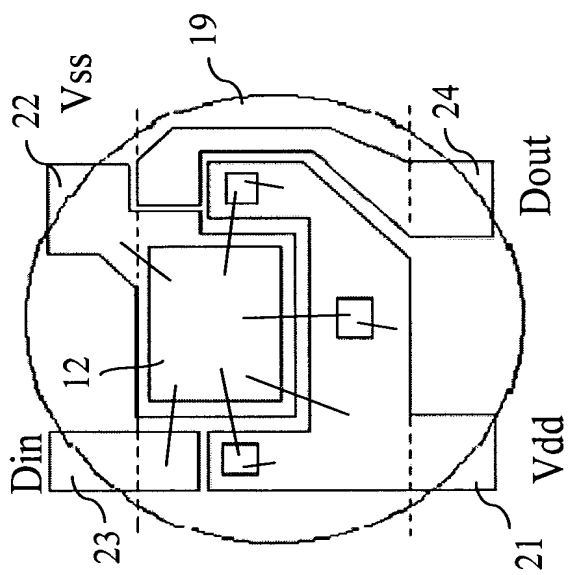


FIG. 6B

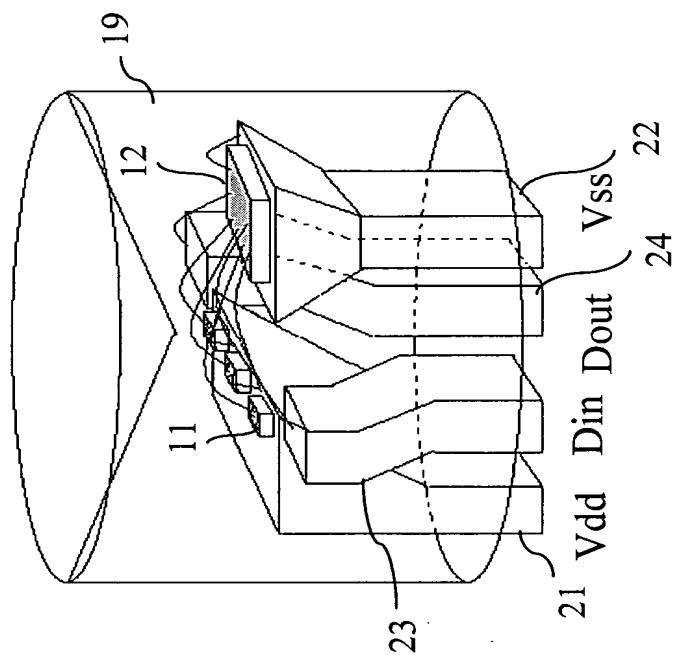


FIG.7

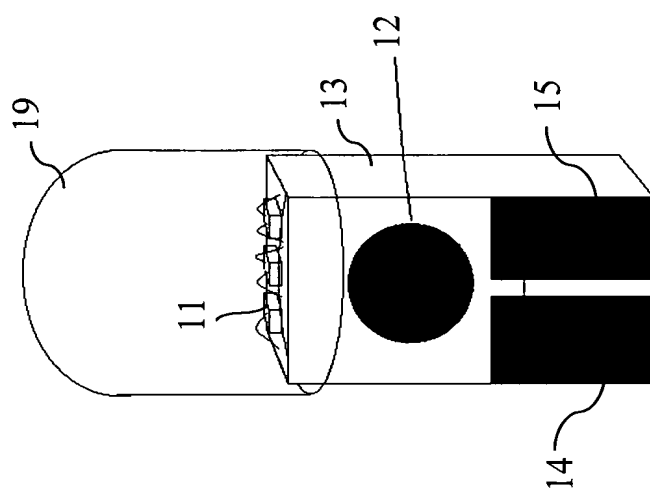


FIG.8

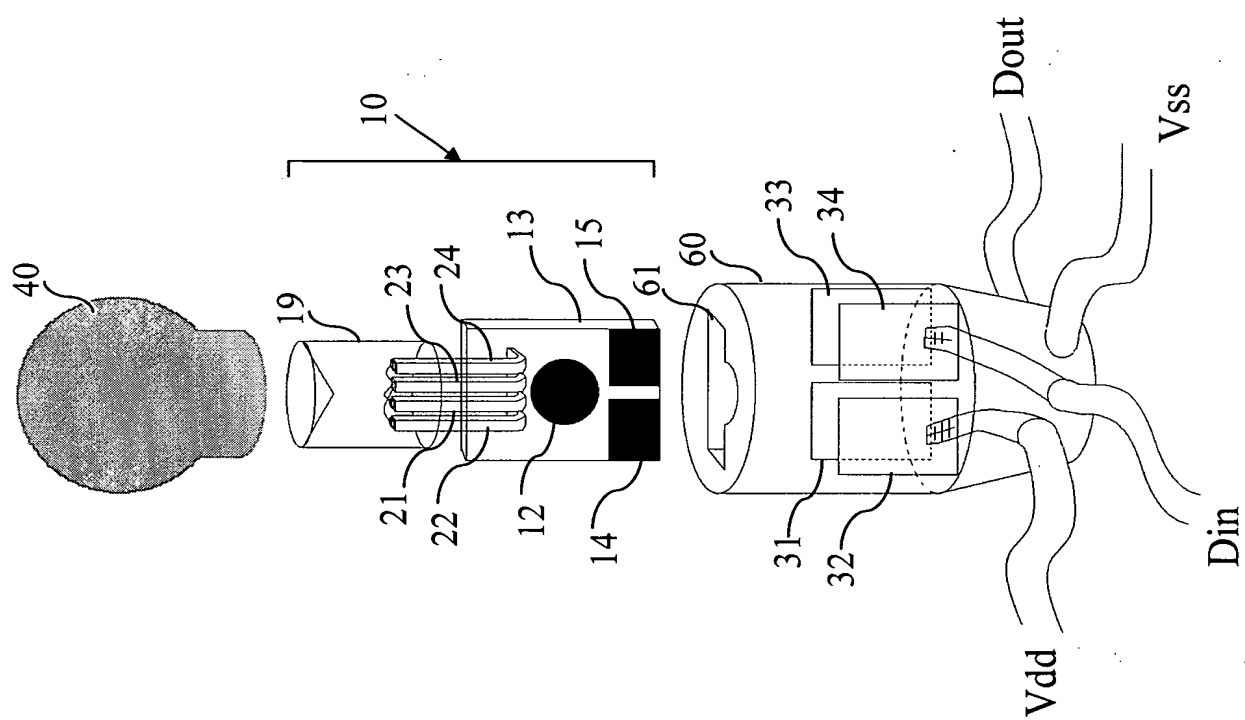


FIG.9

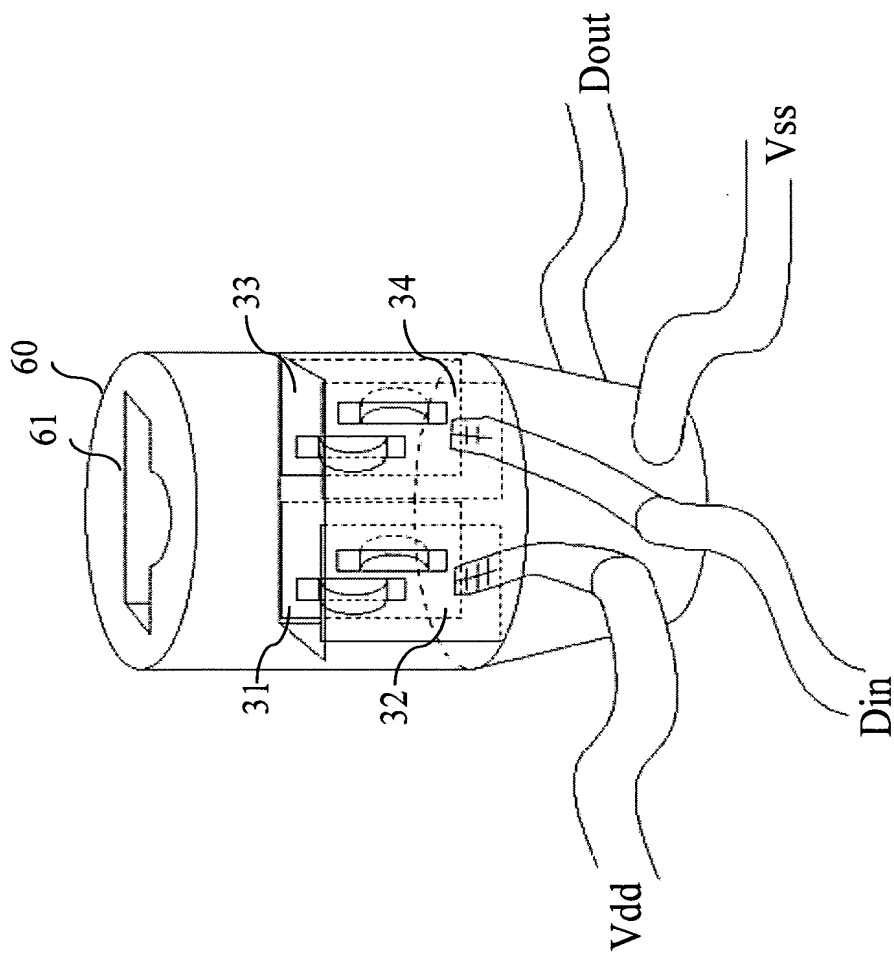


FIG.10

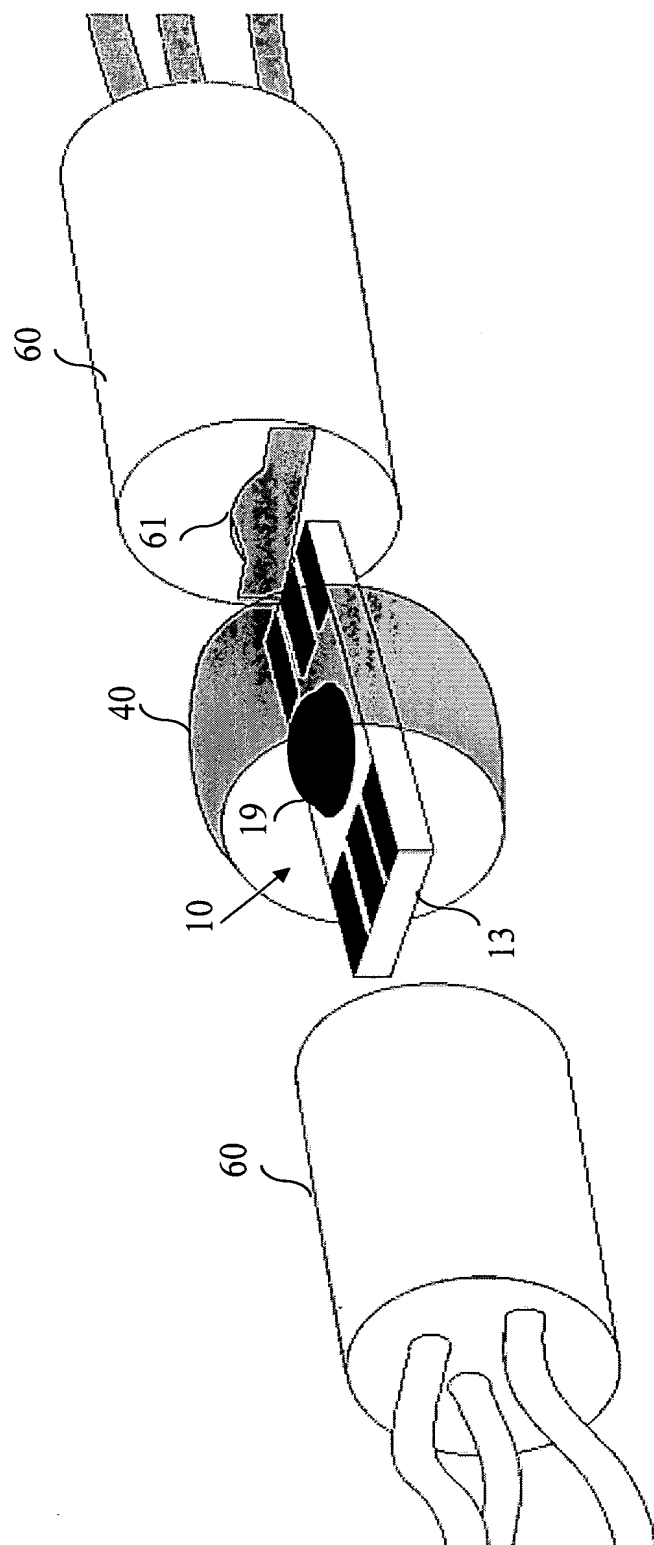


FIG.11

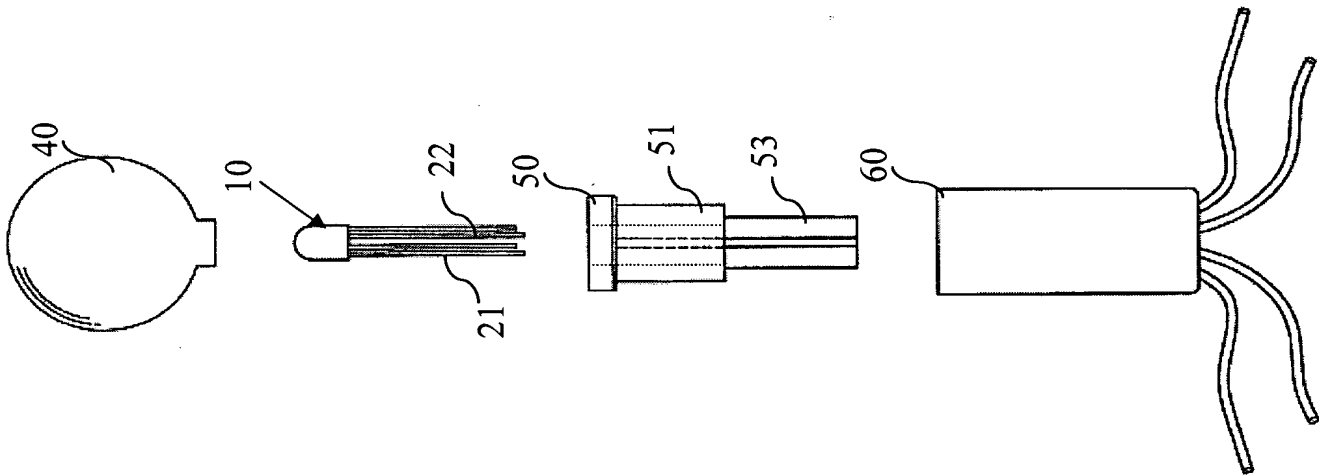


FIG.12

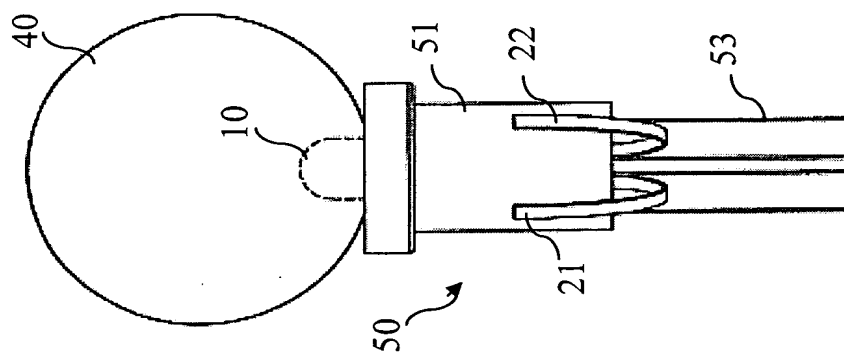


FIG.14

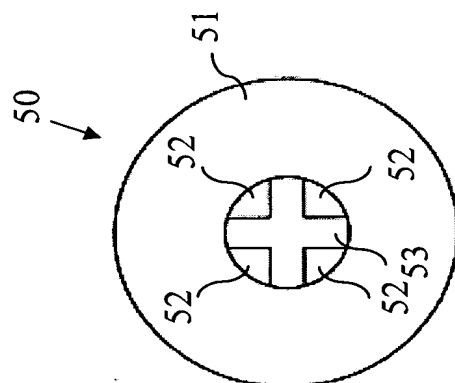


FIG.13

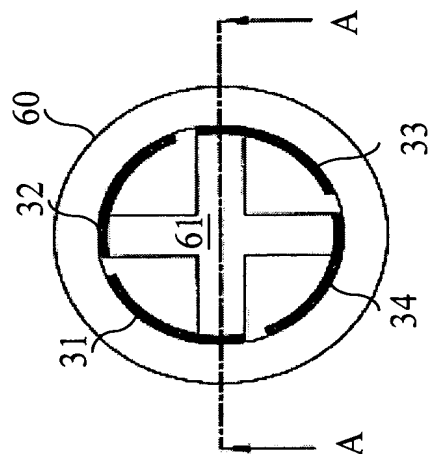


FIG.15

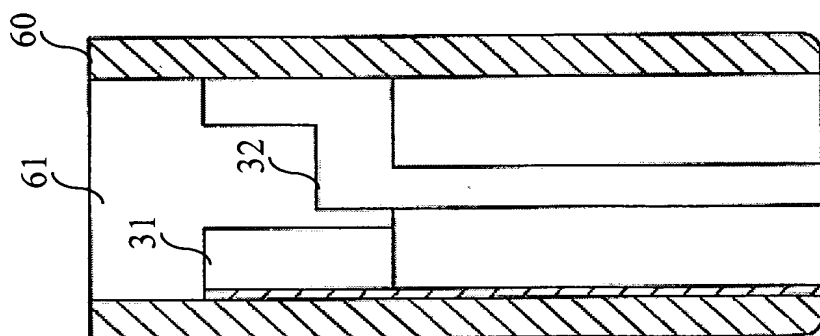


FIG.16

ATTORNEY/DOCKET NO:			
DECLARATION FOR PATENT APPLICATION AND APPOINTMENT OF ATTORNEY			
As a below named inventor, I hereby declare that I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention (Design, if applicable) entitled:			
Title:	Light Emitting Diode Lamp Package Structure and Assembly Thereof		
the specification of which (check at least one of the first three boxes below, as applicable):			
☒	is attached hereto.		
☐	was filed on (day-month-year)		as U.S. Application Number
☐	was filed on (day-month-year)		as PCT Application Number
☐	and (if applicable) was amended on (day-month-year)		
I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56. I hereby claim foreign priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate listed on the Application Data Sheet, and have also identified on the Application Data Sheet any foreign application for patent or inventor's certificate having a filing date before that of each application on which priority is claimed. I hereby claim the benefit under Title 35 U.S. Code §119(e) of any U.S. provisional applications listed on the Application Data Sheet. I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or PCT international application(s) designating The United States of America listed on the Application Data Sheet, and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. POWER OF ATTORNEY: I (We) hereby appoint as my (our) attorneys, with full powers of substitution and revocation, to prosecute this application including the submission and amendment of an application data sheet (37 CFR §1.76), to take instructions from my (our) agent, to receive all communications at the address stated on the Application Data Sheet, and transact all business in the Patent and Trademark Office connected therewith: J. Ernest Kenney, Reg. No. 19,179; Eugene Mar, Reg. No. 25,893; Richard E. Fichter, Reg. No. 26,382; Thomas J. Moore, Reg. No. 28,974; Joseph DeBenedictis, Reg. No. 28,502; and Benjamin E. Urcia, Reg. No. 33,805; each of Bacon & Thomas, PLLC, and			

Full Name of First or Sole Inventor PENG, Jacky	Post Office Address 4F.-9, No.130, Jiankang Rd., Jhonghe City, Taipei County 235, Taiwan (R.O.C.)
Citizenship Taiwan, R.O.C.	Residence (city, and either state or foreign country, MPEP §605.02)
Date <i>May 19 2008</i>	Signature <i>Jacky Peng</i>

☐ See following page(s) for additional joint inventors.

(02Nov2001)

SCORE Placeholder Sheet for IFW Content

Application Number: **12153910**

Document Date: **05/28/2008**

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PATENT APPLICATION SERIAL NO. _____

**U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET**

05/29/2008 MAHMED1 00000013 12153910

01 FC:2011	155.00 OP
02 FC:2111	255.00 OP
03 FC:2311	105.00 OP
04 FC:2201	210.00 OP
05 FC:2202	100.00 OP

PTO-1556
(5/87)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number

12/153,910

APPLICATION AS FILED - PART I

(Column 1)

(Column 2)

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A
TOTAL CLAIMS (37 CFR 1.16(l))	24 minus 20 =	4
INDEPENDENT CLAIMS (37 CFR 1.16(h))	5 minus 3 =	2
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$260 (\$130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))		

RATE (\$)	FEE (\$)
N/A	\$155
N/A	\$255
N/A	\$105
X \$25 =	100
X \$105 =	210
\$130	-
\$185	-
TOTAL	825

RATE (\$)	FEE (\$)
N/A	\$310
N/A	\$510
N/A	\$210
X \$50 =	-
X \$210 =	-
\$260	-
\$370	-
TOTAL	-

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total (37 CFR 1.16(l))	*	Minus	**	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=
	Application Size Fee (37 CFR 1.16(s))				
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					

RATE (\$)	ADDITIONAL FEE (\$)
X \$25 =	-
X \$105 =	-
\$185	-
TOTAL ADD'L FEE	-

RATE (\$)	ADDITIONAL FEE (\$)
X \$50 =	-
X \$210 =	-
\$370	-
TOTAL ADD'L FEE	-

(Column 1)

(Column 2)

(Column 3)

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total (37 CFR 1.16(l))	*	Minus	**	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=
	Application Size Fee (37 CFR 1.16(s))				
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					

RATE (\$)	ADDITIONAL FEE (\$)
X \$25 =	-
X \$105 =	-
\$185	-
TOTAL ADD'L FEE	-

RATE (\$)	ADDITIONAL FEE (\$)
X \$50 =	-
X \$210 =	-
\$370	-
TOTAL ADD'L FEE	-

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/153,910	05/28/2008	2811	825	PENG3033/EM	24	5

CONFIRMATION NO. 1815

23364
BACON & THOMAS, PLLC
625 SLATERS LANE
FOURTH FLOOR
ALEXANDRIA, VA 22314

FILING RECEIPT



OC000000030476651

Date Mailed: 06/16/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Jacky Peng, Taipei County, TAIWAN;

Assignment For Published Patent Application

SEMISILICON TECHNOLOGY CORP., Taipei County, TAIWAN

Power of Attorney:

J Kenney--19179 Benjamin Urcia--33805
Eugene Mar--25893
Richard Fichter--26382
Joseph De Benedictis--28502
Thomas Moore--28974

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 06/13/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/153,910**

Projected Publication Date: 12/03/2009

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

Light emitting diode lamp package structure and assembly thereof

Preliminary Class

257

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/153,910	05/28/2008	Jacky Peng	PENG3033/EM

CONFIRMATION NO. 1815

PUBLICATION NOTICE



OC000000039069045

23364
BACON & THOMAS, PLLC
625 SLATERS LANE
FOURTH FLOOR
ALEXANDRIA, VA 22314-1176

Title:Light emitting diode lamp package structure and assembly thereof

Publication No.US-2009-0294782-A1

Publication Date:12/03/2009

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/153,910

05/28/2008

Jacky Peng

PENG3033/EM

1815

23364 7590 02/03/2010

BACON & THOMAS, PLLC

625 SLATERS LANE

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ALEXANDRIA, VA 22314-1176

EXAMINER

SKYLES, TIFNEY L

ART UNIT

PAPER NUMBER

2814

MAIL DATE

DELIVERY MODE

02/03/2010

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/153,910	Applicant(s) PENG, JACKY	
	Examiner TIFNEY L. SKYLES	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 May 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) _____ is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☒ Claim(s) 1-24 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☐ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

DETAILED ACTION

Election/Restrictions

1. This application contains claims directed to the following patentably distinct species:

- Species I directed to Figure 3A
- Species II directed to Figure 3B
- Species III directed to Figure 4A
- Species IV directed to Figure 4B
- Species V directed to Figure 5
- Species VI directed to Figure 7
- Species VII directed to Figure 8
- Species VIII directed to Figure 9
- Species IX directed to Figure 10
- Species X directed to Figure 11
- Species XI directed to Figures 12-16

2. The species are independent or distinct because claims to the different species recite the mutually exclusive characteristics of such species. In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, there are no generic claims.

There is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics. The species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search queries); and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species**, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election of the species may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are

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added after the election, applicant must indicate which of these claims are readable on the elected species.

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

3. The examiner has required restriction between product and process claims. Where applicant elects claims directed to the product, and the product claims are subsequently found allowable, withdrawn process claims that depend from or otherwise require all the limitations of the allowable product claim will be considered for rejoinder. All claims directed to a nonelected process invention must require all the limitations of an allowable product claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the

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requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product are found allowable, an otherwise proper restriction requirement between product claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product claim will not be rejoined. See MPEP § 821.04(b). Additionally, in order to retain the right to rejoinder in accordance with the above policy, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product claims. **Failure to do so may result in a loss of the right to rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIFNEY L. SKYLES whose telephone number is (571)270-5019. The examiner can normally be reached on Mon-Fri 7:30AM - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2814

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wai-Sing Louie/
Primary Examiner, Art Unit 2814

TLS

<i>Index of Claims</i> 	Application/Control No. 12153910	Applicant(s)/Patent Under Reexamination PENG, JACKY
	Examiner TIFNEY L SKYLES	Art Unit 2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant
 ☐ CPA
 ☐ T.D.
 ☐ R.1.47

CLAIM		DATE									
Final	Original	01/30/2010									
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Application No.:	12/153,910	Examiner:	Skyles, T.
Filing Date:	May 28, 2008	Art Unit:	2814
First Inventor:	Jacky Peng	Customer No.:	23364
Attorney No.:	PENG3033/JJC/KDW	Confirm. No.:	1815

For: **LIGHT EMITTING DIODE LAMP PACKAGE STRUCTURE
AND ASSEMBLY THEREOF**

REPLY TO OFFICE ACTION
OF FEBRUARY 3, 2010

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INTRODUCTORY COMMENTS

This is responsive to the Office action mailed February 3, 2010 in the pending application.

ELECTION

The applicant hereby elects species III, as represented in Fig. 4A, for prosecution on the merits. The claims readable on the species of Fig. 4A are claims 1-4, 6, 9-12 and 15.

The applicant hereby reserves all rights to the non-elected subject matter.

If any issues remain that may be resolved by a telephone or facsimile communication with the applicant's attorney, the examiner is invited to contact the undersigned at the numbers shown below.

BACON & THOMAS, PLLC
625 Slaters Lane, Fourth Floor
Alexandria, Virginia 22314-1176
Phone: (703) 683-0500
Facsimile: (703) 683-1080

Respectfully submitted,

/Kevin D. Williams/

KEVIN D. WILLIAMS
Attorney for Applicant
Registration No. 63,716

Date: March 5, 2010

Electronic Acknowledgement Receipt

EFS ID:	7148353
Application Number:	12153910
International Application Number:	
Confirmation Number:	1815
Title of Invention:	Light emitting diode lamp package structure and assembly thereof
First Named Inventor/Applicant Name:	Jacky Peng
Customer Number:	23364
Filer:	Kevin Denard Williams/Katy Greyson
Filer Authorized By:	Kevin Denard Williams
Attorney Docket Number:	PENG3033/EM
Receipt Date:	05-MAR-2010
Filing Date:	28-MAY-2008
Time Stamp:	13:43:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	PENG3033Election_3510.pdf	189273 5765a576046d4c4d534650b7231f76b411338e0b	no	1

Warnings:

Information:

Xu Peicheng Ex. 1002, p. 58

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/153,910

05/28/2008

Jacky Peng

PENG3033/EM

1815

23364 7590 04/28/2010

BACON & THOMAS, PLLC
625 SLATERS LANE
FOURTH FLOOR
ALEXANDRIA, VA 22314-1176

EXAMINER

SKYLES, TIFNEY L

ART UNIT

PAPER NUMBER

2814

MAIL DATE

DELIVERY MODE

04/28/2010

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/153,910	Applicant(s) PENG, JACKY	
	Examiner TIFNEY L. SKYLES	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 March 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) 5,7,8,13,14 and 16-24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6, 9-12, and 15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) ☐ Notice of Informal Patent Application |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Species III in the reply filed on 03/05/2010 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 6, and 9-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Stoyan (US 2008/0087903).

Regarding Claim 1, Stoyan teaches an LED lamp package structure, comprising: a plurality of light emitting diodes **1000** [Fig. 14A], each light emitting diode **1000** having two electrode ends and one of the electrode ends being a common electrode end; a control integrated circuit **1400B**, having a data input electrode and a data output electrode and electrically connected to the light

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emitting diodes **1000** [see wires connected to control device 1400b] to control the illumination state of each light emitting diode **1000** [Para. 0044]; a first conductor **1130** [Fig. 14B], a second conductor **1120**, a third conductor **1220**, and a fourth conductor **1110 or 1230**, the first conductor being a positive DC voltage pad **1130** [Para. 0066], the second conductor **1120** being connected to the data input electrode, the third conductor **1220** being connected to the data output electrode, the fourth conductor **1110 or 1230** being a negative DC voltage pad [Para. 0066]; and a package body **110** encapsulating the light emitting diodes **1000**, the control integrated circuit **1400B** and the conductors **1110-1130 and 1210-1230**, a portion of the first conductor **1130**, the second conductor **1120**, the third conductor **1220**, and the fourth conductor **1110 or 1230** being exposed outside the package body [see Fig. 5].

Regarding Claim 2, Stoyan teaches the light emitting diode lamp package structure according to claim 1, wherein the common electrode end **1130** is a positive DC voltage pad or a negative DC voltage pad [Para. 0066].

Regarding Claim 3, Stoyan teaches the light emitting diode lamp package structure according to claim 1, further comprising a circuit board **1300** [see Fig. 1A] carrying the light emitting diodes **1000** and the control integrated circuit **1400A**.

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Regarding Claim 4, Stoyan teaches the light emitting diode lamp package structure according to claim 3, wherein the light emitting diodes **1000** and the control integrated circuit **1400A** are mounted on the same surface of the circuit board **1300**.

Regarding Claim 6, Stoyan teaches the light emitting diode lamp package structure according to claim 1, wherein the conductors **1110-1130** and **1210-1230** are an electric conductivity support or a conductive wire [Para. 0066].

Regarding Claim 9, Stoyan teaches the light emitting diode lamp package structure according to claim 1, wherein the first conductor **1130** and the fourth **1230** conductor are connected to two opposing sides of the package body **110**, and the second conductor **1120** and the third conductor **1220** are connected to two opposing sides of the package body **110**.

Regarding Claim 10, Stoyan teaches the light emitting diode lamp package structure according to claim 1, wherein the first conductor **1130** and the fourth conductor **1110** are connected to the same side of the package body **110**, while the second conductor **1120** and the third conductor **1220** are connected to two opposing sides of the package body **110**.

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Regarding Claim 11, Stoyan teaches the light emitting diode lamp package structure according to claim 1, further comprising a fifth conductor **1210** and a sixth conductor **1110**, the fifth conductor **1210** being a positive DC voltage pad and the sixth conductor **1110** being a negative DC voltage pad [Para. 0066].

Regarding Claim 12, Stoyan teaches the light emitting diode lamp package structure according to claim 11, wherein the first conductor **1130** and the fifth conductor **1210** are connected to two opposing sides of the package body **110**, the second conductor **1120** and the third conductor **1220** are connected to two opposing sides of the package body **110**, while the fourth conductor **1230** and the sixth conductor **1110** are connected to two opposing sides of the package body **110**.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stoyan in view of Yan (US 7,473,933).

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Regarding Claim 15, Stoyan teaches the light emitting diode lamp package structure according to claim 1, wherein the package body is in rectangular shape [Para. 0065] but fails to teach said rectangle having a light emitting window wherein the light emitting diodes are aligned with the light emitting window inside the rectangle. However, Yan teaches said rectangle having a light emitting window **690** [Fig. 6B] wherein the light emitting diodes **640** are aligned with the light emitting window **680** inside the rectangle. Therefore, it would have been obvious at the time the invention was made to combine Yan with Stoyan for the purposes of focusing the light emitted from the LED package [Col. 11, Lines 35-40].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIFNEY L. SKYLES whose telephone number is (571)270-5019. The examiner can normally be reached on Mon-Fri 7:30AM - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2814

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Howard Weiss/
Primary Examiner
Art Unit 2814

TLS

Notice of References Cited	Application/Control No. 12/153,910		Applicant(s)/Patent Under Reexamination PENG, JACKY	
	Examiner TIFNEY L. SKYLES		Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2008/0087903	04-2008	Stoyan, Harald	257/088
*	B	US-7,473,933	01-2009	Yan, Xiantao	257/88
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 12153910	Applicant(s)/Patent Under Reexamination PENG, JACKY
	Examiner TIFNEY L SKYLES	Art Unit 2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	01/30/2010	04/24/2010						
	1	÷	✓						
	2	÷	✓						
	3	÷	✓						
	4	÷	✓						
	5	÷	N						
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	22	÷	N						
	23	÷	N						
	24	÷	N						

Search Notes 	Application/Control No. 12153910	Applicant(s)/Patent Under Reexamination PENG, JACKY
	Examiner TIFNEY L SKYLES	Art Unit 2814

SEARCHED			
Class	Subclass	Date	Examiner
257	88, 89	04/24/2010	TLS

SEARCH NOTES		
Search Notes	Date	Examiner
Search history attached	04/24/2010	TLS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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BIB DATA SHEET

CONFIRMATION NO. 1815

SERIAL NUMBER 12/153,910	FILING or 371(c) DATE 05/28/2008 RULE	CLASS 257	GROUP ART UNIT 2814	ATTORNEY DOCKET NO. PENG3033/EM	
APPLICANTS Jacky Peng, Taipei County, TAIWAN; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** ** SMALL ENTITY ** 06/13/2008					
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/TIFNEY L SKYLES/</u> Examiner's Signature	☐ Met after Allowance TLS Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 14	TOTAL CLAIMS 24	INDEPENDENT CLAIMS 5
ADDRESS BACON & THOMAS, PLLC 625 SLATERS LANE FOURTH FLOOR ALEXANDRIA, VA 22314-1176 UNITED STATES					
TITLE Light emitting diode lamp package structure and assembly thereof					
FILING FEE RECEIVED 825	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	816	(257/89).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2010/04/23 17:08
S2	101	S1 and (led or "light emitting diode") and (circuit adj board)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/04/23 17:08
S3	41	S2 and encapsula\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/04/23 17:09
S4	7	S3 and (ic or "integrated circuit")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/04/23 17:09
S5	11	("20030174504" "20040129944" "4900910" "6044548" "6790684" "6793829" "6864627" "6961190" "7064354" "RE35665").PN. OR ("7397068").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/23 17:34
S6	1712	(257/88).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2010/04/23 17:40
S7	1536	S6 and @ad<="20080528"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/04/23 17:41
S8	224	S7 and (led or "light emitting diode") and (circuit adj board)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/04/23 17:41
S9	88	S8 and encapsula\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/04/23 17:41
S10	21	S9 and (ic or "integrated circuit")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/04/23 17:41

EAST Search History (I nterference)

< This search history is empty >

4/ 24/ 2010 1:42:44 PM**C:\ Documents and Settings\ tskyles\ My Documents\ EAST\ Workspaces\ 12153910.wsp**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Application No.:	12/153,910	Confirm. No.:	1815
Filing Date:	May 28, 2008	Examiner:	Skyles, Tifney
First Inventor:	Jacky PENG	Art Unit:	2814
Attorney No.:	PENG3033/JJC/BEL	Customer No.:	23364
For:	LIGHT EMITTING DIODE LAMP PACKAGE ASSEMBLY THEREOF		

REPLY TO OFFICE ACTION
OF APRIL 28, 2010

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INTRODUCTORY COMMENTS

This is responsive to the outstanding Office action dated April 28, 2010 in the above-identified application.

In view of the following amendments and remarks, reconsideration of the application is respectfully requested.

AMENDMENT

In the Claims

The claims are amended as shown on the following pages under the heading AMENDMENT TO THE CLAIMS. The list shows the status of all claims presently in the application and is intended to supersede all prior versions of the claims in the application. Any cancellation of claims is made without prejudice or disclaimer.

AMENDMENT TO THE CLAIMS

1. (Currently Amended) A LED lamp package structure, comprising:
 - a plurality of light emitting diodes, each light emitting diode having two electrode ends and one of the electrode ends being a common electrode end;
 - a control integrated circuit, having a data input electrode and a data output electrode and electrically connected to the light emitting diodes, wherein the control integrated circuit receives external control data via the data input electrode to control the illumination state of each light emitting diode according to the external control data;
 - a first conductor, a second conductor, a third conductor, and a fourth conductor, the ~~first~~ first conductor being a positive DC voltage pad, the second conductor being connected to the data input electrode, the third conductor being connected to the data output electrode, the fourth conductor being a negative DC voltage pad; and
 - a package body encapsulating the light emitting diodes, the control integrated circuit and the conductors, a portion of the first conductor, the second conductor, the third conductor, and the fourth conductor being exposed outside the package body.
2. (Original) The light emitting diode lamp package structure according to claim 1, wherein the common electrode end is a positive DC voltage pad or a negative DC voltage pad.
3. (Currently Amended) The light emitting diode lamp package structure according to claim 1, further comprising a circuit board carrying the light emitting diodes and the control integrated circuit ~~control integrated circuit~~.
4. (Original) The light emitting diode lamp package structure according to claim 3, wherein the light emitting diodes and the control integrated circuit are mounted on the same surface of the circuit board.
5. (Withdrawn) The light emitting diode lamp package structure according to claim 3, wherein the light emitting diodes are mounted on one surface of the circuit board and the control integrated circuit is mounted on the other surface of the circuit board.

6. (Original) The light emitting diode lamp package structure according to claim 1, wherein the conductors are an electric conductivity support or a conductive wire.
7. (Withdrawn) The light emitting diode lamp package structure according to claim 1, wherein the first conductor forms a platform inside the package body, said platform carrying the light emitting diodes, and the first conductor being electrically connected to the light emitting diodes.
8. (Withdrawn) The light emitting diode lamp package structure according to claim 1, wherein the fourth conductor forms a platform inside the package body, the platform carrying the control integrated circuit, and the fourth conductor being electrically connected to the control integrated circuit.
9. (Original) The light emitting diode lamp package structure according to claim 1, wherein the first conductor and the fourth conductor are connected to two opposing sides of the package body, and the second conductor and the third conductor are connected to two opposing sides of the package body.
10. (Original) The light emitting diode lamp package structure according to claim 1, wherein the first conductor and the fourth conductor are connected to the same side of the package body, while the second conductor and the third conductor are connected to two opposing sides of the package body.
11. (Original) The light emitting diode lamp package structure according to claim 1, further comprising a fifth conductor and a sixth conductor, the fifth conductor being a positive DC voltage pad and the sixth conductor being a negative DC voltage pad.
12. (Original) The light emitting diode lamp package structure according to claim 11, wherein the first conductor and the fifth conductor are connected to two opposing sides of the package body, the second conductor and the third conductor are connected to two opposing

sides of the package body, while the fourth conductor and the sixth conductor are connected to two opposing sides of the package body.

13. (Withdrawn) The light emitting diode lamp package structure according to claim 3, wherein two opposing surfaces of the circuit board each carrying a redlight emitting diode, a green light emitting diode, and a bluelight emitting diode.
14. (Withdrawn) The light emitting diode lamp package structure according to claim 1, wherein the package body is an injection-molded transparent glue in spherical or hemispherical shape.
15. (Original) The light emitting diode lamp package structure according to claim 1, wherein the package body is in rectangular shape, said rectangle having a light emitting window, the light emitting diodes aligning with the light emitting window inside the rectangle.
16. (Withdrawn) A light emitting diode lamp assembly, comprising:
 - a light emitting diode lamp having a plurality of light emitting diodes and four electric conductivity supports encapsulated in a package body;
 - a lampshade covering the package body of the light emitting diode lamp;
 - a socket being a body having a perforation and extended with a plug-in member, the perforation accommodating the light emitting diodes and enabling the four electric conductivity supports to expose outside the body; and
 - a mount formed with a socket, the socket having four electrode contacts inside such that when the socket is plugged into the socket, the four electrode contacts being in contact with the four electric conductivity supports respectively.
17. (Withdrawn) The light emitting diode lamp assembly according to claim 16, wherein the plurality of light emitting diodes are mounted on a circuit board, the circuit board carrying a control integrated circuit, the four electric conductivity supports being respectively a positive DC voltage pad, a data input end, a data output end, and a negative DC voltage pad.

18. (Withdrawn) The light emitting diode lamp assembly according to claim 16, wherein the four electric conductivity supports have a flat shape and are flexible.
19. (Withdrawn) The light emitting diode lamp assembly according to claim 16, wherein the upper half of the socket accommodates the body, while the lower half of the body is coupled to the plug-in member.
20. (Withdrawn) The light emitting diode lamp assembly according to claim 16, wherein the socket forms a through-hole, the four electrode contacts passing through the through-hole to connect with four external wires respectively.
21. (Withdrawn) A light emitting diode lamp assembly, comprising:
a light emitting diode lamp having a package body and a circuit board, the package body encapsulating a plurality of light emitting diodes and four electric conductivity supports, the four electric conductivity supports being electrically connected to the circuit board, and the circuit board carrying a control integrated circuit and forming a positive DC voltage electrode, a data input electrode, a data output electrode and a negative DC voltage electrode;
a lampshade covering the package body of the light emitting diode lamp; and
a mount formed with a socket, the socket having four electrode contacts inside such that when the circuit board of the light emitting diode lamp is plugged into the socket, the four electrode contacts being in contact with the positive DC voltage electrode, the data input electrode, the data output electrode and the negative DC voltage electrode respectively.
22. (Withdrawn) A light emitting diode lamp assembly, comprising:
a light emitting diode lamp having a package body and a circuit board, the package body encapsulating a plurality of light emitting diodes and a control integrated circuit disposed on one side of the circuit board, a plurality of electrodes being disposed at two opposing sides of the circuit board, wherein the two opposing sides of the circuit board are respectively disposed with a data input electrode and a data output electrode;
a lampshade covering the periphery of the light emitting diode lamp; and

two mounts, each mount formed with a socket, the socket having electrode contacts inside corresponding to the electrodes of the circuit board, wherein the sockets of the two mounts are respectively coupled to the two opposing sides of the circuit board of light emitting diode lamp, and the lampshade is situated between the two mounts.

23. (Withdrawn) A package structure of the light emitting diode lamp, comprising:

- a plurality of light emitting diodes, each light emitting diode having two electrode ends and one of the electrode ends being a common electrode end;

- a circuit board, mounting a plurality of light emitting diodes;

- a package body, encapsulating said light emitting diodes and a part of said circuit board; and

- a control integrated circuit, having a data input electrode and a data output electrode and electrically connected to said light emitting diodes to control the illumination state of each light emitting diode;

- wherein said circuit board being exposed outside the part of the package body carrying said control integrated circuit, and said circuit board having a first conduct electricity, a second conduct electricity, a third conduct electricity, and a fourth conduct electricity being exposed outside the package body;

24. (Withdrawn) The light emitting diode lamp package structure according to claim 23, wherein said first conduct electricity is the positive DC voltage end, said second conduct electricity connecting said data output electrode, said third conduct electricity connecting said data output electrode, and said fourth conduct electricity is the negative DC voltage end.

REMARKS

Reconsideration of the pending application is respectfully requested in view of the following observations.

1. In the claims

Claims 1 and 3 has been amended. Claims 2-4, 6, 9-12, and 15 are original. Claims 5, 7, 8, 13, 14, and 16-24 have been withdrawn.

Claim 1 has been amended to clarify that the control integrated circuit receives control data via the data input electrode to control the illumination state of each light emitting diode according to the control data and to correct a spelling error by changing “fist” to “first.” Support for this amendment may be found, for example, at least on page 8, lines 10-12 of the specification.

Claim 3 has been amended to correct a typographical error by adding a space between “control” and “integrated.”

The claims are now considered to be placed in condition for allowance.

No new matter is introduced via the amendment to the claims.

Entry of the amendment to the claims is kindly requested.

2. Rejection of claims 1-4, 6, and 9-12 under 35 USC 102(e) as being anticipated by US publication 2008/0087903 (Stoyan)

In view of the amendment to claim 1, it is submitted that the claims are in condition for allowance. Reconsideration of the rejection is respectfully requested in view of the amendment to the claims and the following observations.

Amended claim 1 recites a LED lamp package structure with a plurality of LEDs, a control integrated circuit, four conductors, and a package body. The control integrated circuit (IC) receives external control data via a data input electrode and uses the control data to control the illumination state of each LED. The four conductors are a positive DC voltage pad, a data input electrode, a data output electrode, and a negative voltage pad. The package body encapsulates the LEDs but leaves a portion of the four conductors exposed outside the package body.

Stoyan discloses three types of LED modules (110, 120, 130) that are connected in series (see paragraph [0020]). The control device (1400B) drives the three radiation emitting semiconductor components (1000) on the LED module. The control device is connected to contact strips (1401, 1402) which provide a supply voltage from an external power supply device for the LED module.

It is submitted that *Stoyan* fails to teach a control IC which receives external control data via a data input electrode and uses the external control data to control the illumination state of the LEDs.

Stoyan is silent as to how the control device controls the state of the LEDs. *Stoyan* discloses that the control device is meant to incorporate the functionality of turning on and off the LED but does not disclose how the control device makes the determination of whether to turn the LED on and off. Thus, *Stoyan* does not disclose the control device controlling the illumination of the LED based on the input of an external source.

Moreover, the Office Action (on page 3) cites electrical terminal 1120 as being the data input electrode. *Stoyan*, however, does not disclose electrical terminal 1120 to receive any kind of data. From Fig. 4, electrical terminal (1220) is connected to electrical terminal (1120) of the next LED module via connection carrier (200). *Stoyan* does not disclose that any data is transmitted through this connection. Furthermore, data cannot be transmitted to the control device through electrical terminal (1120). *Stoyan* discloses that the conductor track (1403) is connected to electrical terminal (1220) and is not in electrical contact with the control device (1400) (see paragraph 0069).

As illustrated in Fig. 1 and Fig. 14A, the control device (1400B) is not electrically connected to electrical terminal (1120). The connections to electrical terminal (1120) are with the radiation semiconductor components (1000) in a central module (see Fig. 1B and Fig. 14B). Furthermore, the control device is provided only on the start module and no connections are made to electrical terminal 1120 in the start module (see paragraph [0070]).

Therefore, electrical terminal (1120) cannot function as a data input electrode for the control device since it is not electrically connected to the control device through any of the connections of electrical terminal (1120), and similarly, electrical terminal (1220) cannot function as a data output electrode.

Accordingly, *Stoyan* fails to teach the control integrated circuit and data input electrode as required by amended claim 1.

Moreover, 2-4, 6, and 9-12 depend from claim 1 and are likewise allowable for the reasons above in view of their dependency from claim 1 and their individually recited features.

Therefore, withdrawal of the rejection of the claims in view of the prior art is kindly requested.

3. Rejection of claim 15 under 35 USC 103(a) as being unpatentable over US publication 2008/0087903 (*Stoyan*) in view of US patent 7,473,933 (*Yan*)

Claim 15 depends from claim 1 and is likewise allowable for the reasons above in view of its dependency from claim 1 and its individually recited features. *Yan* does not cure the deficiencies of *Stoyan* as discussed above in claim 1.

Accordingly, claim 15 is patentable at least on the basis of its dependency from claim 1.

Therefore, withdrawal of the rejection of the claims in view of the prior art is kindly requested.

4. Conclusion

As a result of the amendment to the claims, and further in view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is respectfully requested that every pending claim in the present application be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the applicant's attorney, the examiner is invited to contact the undersigned at the numbers shown below.

BACON & THOMAS, PLLC
625 Slaters Lane, Fourth Floor
Alexandria, Virginia 22314-1176
Phone: (703) 683-0500
Facsimile: (703) 683-1080

Date: July 26, 2010

Respectfully submitted,

/Justin J. Cassell/

JUSTIN J. CASSELL
Attorney for Applicant
Registration No. 46,205

JJC/BEL

Electronic Acknowledgement Receipt

EFS ID:	8085185
Application Number:	12153910
International Application Number:	
Confirmation Number:	1815
Title of Invention:	Light emitting diode lamp package structure and assembly thereof
First Named Inventor/Applicant Name:	Jacky Peng
Customer Number:	23364
Filer:	Justin John Cassell/Kim Forsell
Filer Authorized By:	Justin John Cassell
Attorney Docket Number:	PENG3033/JJC/BEL
Receipt Date:	26-JUL-2010
Filing Date:	28-MAY-2008
Time Stamp:	16:05:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		AM_072610.pdf	312451 a0107d11f05bba96b0074e20cb182eec19c29fab	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	9
Warnings:			
Information:			
Total Files Size (in bytes):		312451	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Filing Date
05/28/2008

☐ To be Mailed

OTHER THAN

(Column 2)

SMALL ENTITY ☒

OR

SMALL ENTITY

FOR		NUMBER FILED	NUMBER EXTRA	RATE (\$)		FEE (\$)		OR		RATE (\$)		FEE (\$)	
☐	BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A										
☐	SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A										
☐	EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A										
TOTAL CLAIMS (37 CFR 1.16(j))		minus 20 =	*	X \$	=			X \$	=				
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*	X \$	=			X \$	=				
☐	APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).											
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))													
* If the difference in column 1 is less than zero, enter "0" in column 2.													
				TOTAL						TOTAL			

* If the difference in column 1 is less than zero, enter "0" in column 2.

OTHER THAN

(Column 3)

SMALL ENTITY

OR

SMALL ENTITY

AMENDMENT	07/26/2010	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total (37 CFR 1.16(j))	* 24	Minus	** 24	= 0
	Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0
	☐ Application Size Fee (37 CFR 1.16(s))				
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				
		(Column 1)	(Column 2)	(Column 3)	

RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)
x \$26 =	0	OR	x \$ =	
x \$110 =	0	OR	x \$ =	
		OR		
TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	

(Column 3)

AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		X \$ =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		X \$ =			
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE			

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/THERESA I. OKON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/153,910

05/28/2008

Jacky Peng

PENG3033/JJC/BEL

1815

23364 7590 09/28/2010

BACON & THOMAS, PLLC
625 SLATERS LANE
FOURTH FLOOR
ALEXANDRIA, VA 22314-1176

EXAMINER

SKYLES, TIFNEY L

ART UNIT

PAPER NUMBER

2814

MAIL DATE

DELIVERY MODE

09/28/2010

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/153,910	Applicant(s) PENG, JACKY	
	Examiner TIFNEY L. SKYLES	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 July 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) 5,7,8,13,14 and 16-24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4,6,9-12 and 15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 May 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☐ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) ☐ Notice of Informal Patent Application |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 6, and 9-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Stoyan (US 2008/0087903).

Regarding Claim 1, Stoyan teaches an LED lamp package structure, comprising: a plurality of light emitting diodes **1000** [Fig. 14A], each light emitting diode **1000** having two electrode ends and one of the electrode ends being a common electrode end; a control integrated circuit **1400B**, having a data input electrode (see electrodes in contact with 1400B and facing the upper portion of 110) and a data output electrode (see electrodes in contact with 1400B and facing the lower portion of 110) and electrically connected to the light emitting diodes **1000** (see wires connected to control device 1400b), wherein the control integrated circuit receives external control data via the data input electrode to control the illumination state of each light emitting diode **1000** according to the external control data [Para. 0066-0067]; a first conductor **1401** [Fig. 14A], a

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second conductor **1250** [Fig. 14A], a third conductor **1240**, and a fourth conductor **1402**, the first conductor being a positive DC voltage pad **1401** [Para. 0066], the second conductor **1250** being connected to the data input electrode, the third conductor **1240** being connected to the data output electrode, the fourth conductor **1402** being a negative DC voltage pad [Para. 0066]; and a package body **110** encapsulating the light emitting diodes **1000**, the control integrated circuit **1400B** and the conductors **1240**, **1250**, **1401**, **1402**, a portion of the first conductor **1401**, the second conductor **1250**, the third conductor **1240**, and the fourth conductor **1402** being exposed outside the package body [see Fig. 5].

Regarding Claim 2, Stoyan teaches the light emitting diode lamp package structure according to claim 1, wherein the common electrode end is a positive DC voltage pad **1401** or a negative DC voltage pad **1402** [Para. 0066].

Regarding Claim 3, Stoyan teaches the light emitting diode lamp package structure according to claim 1, further comprising a circuit board **1300** [see Fig. 1A] carrying the light emitting diodes **1000** and the control integrated circuit **1400A**.

Regarding Claim 4, Stoyan teaches the light emitting diode lamp package structure according to claim 3, wherein the light emitting diodes **1000** and the

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control integrated circuit **1400A** are mounted on the same surface of the circuit board **1300**.

Regarding Claim 6, Stoyan teaches the light emitting diode lamp package structure according to claim 1, wherein the conductors **1240**, **1250**, **1401**, and **1402** are an electric conductivity support or a conductive wire [Para. 0066].

Regarding Claim 9, Stoyan teaches the light emitting diode lamp package structure according to claim 1, wherein the first conductor **1401** and the fourth **1402** conductor are connected to two opposing sides of the package body **110**, and the second conductor **1250** and the third conductor **1140** are connected to two opposing sides of the package body **110**.

Regarding Claim 10, Stoyan teaches the light emitting diode lamp package structure according to claim 1, wherein the first conductor **1401** and the fourth conductor **1230** are connected to the same side of the package body **110**, while the second conductor **1250** and the third conductor **1140** are connected to two opposing sides of the package body **110**.

Regarding Claim 11, Stoyan teaches the light emitting diode lamp package structure according to claim 1, further comprising a fifth conductor **1210** and a

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sixth conductor **1230**, the fifth conductor **1210** being a positive DC voltage pad and the sixth conductor **1230** being a negative DC voltage pad [Para. 0066].

Regarding Claim 12, Stoyan teaches the light emitting diode lamp package structure according to claim 11, wherein the first conductor **1401** and the fifth conductor **1210** are connected to two opposing sides of the package body **110**, the second conductor **1250** and the third conductor **1140** are connected to two opposing sides of the package body **110**, while the fourth conductor **1402** and the sixth conductor **1230** are connected to two opposing sides of the package body **110**.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stoyan in view of Yan (US 7,473,933).

Regarding Claim 15, Stoyan teaches the light emitting diode lamp package structure according to claim 1, wherein the package body is in rectangular shape [Para. 0065] but fails to teach said rectangle having a light emitting window

wherein the light emitting diodes are aligned with the light emitting window inside the rectangle. However, Yan teaches said rectangle having a light emitting window **690** [Fig. 6B] wherein the light emitting diodes **640** are aligned with the light emitting window **680** inside the rectangle. Therefore, it would have been obvious at the time the invention was made to combine Yan with Stoyan for the purposes of focusing the light emitted from the LED package [Col. 11, Lines 35-40].

Response to Arguments

5. Applicant's arguments filed 07/26/2010 have been fully considered but they are not persuasive. The Applicant argues that Stoyan fails to teach a control IC which receives external control data via a data input electrode and uses the external control data to control the illumination state of the LEDs. The Applicant further states that Stoyan is silent as to how the control device controls the state of the LEDs. However, the Examiner respectfully disagrees. Referring to paragraphs [0066]-[0067], Stoyan clearly teaches a control device which receives external control data via a data input electrode. The Applicant also argues that data cannot be transmitted to the control device through electrical terminal 1120. However, as shown in Fig. 4 and taught in paragraph [0087], the LED 1000 is connected to the control device via terminal 1120. Therefore, data can very well be transmitted to the control device through the terminal 1120. Thus, the arguments are not persuasive and the rejection stands.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIFNEY L. SKYLES whose telephone number is (571)270-5019. The examiner can normally be reached on Mon-Fri 7:30AM - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2814

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Howard Weiss/
Primary Examiner
Art Unit 2814

TLS

<i>Index of Claims</i> 	Application/Control No. 12153910	Applicant(s)/Patent Under Reexamination PENG, JACKY
	Examiner TIFNEY L SKYLES	Art Unit 2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	01/30/2010	04/24/2010	09/22/2010					
	1	÷	✓	✓					
	2	÷	✓	✓					
	3	÷	✓	✓					
	4	÷	✓	✓					
	5	÷	N	N					
	6	÷	✓	✓					
	7	÷	N	N					
	8	÷	N	N					
	9	÷	✓	✓					
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	22	÷	N	N					
	23	÷	N	N					
	24	÷	N	N					

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S11	2302	257/433	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/22 18:10
S12	2223	S11 and @ad<="20080528"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/22 18:10
S13	240	S12 and (led or "light emitting diode") and (circuit adj board)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/22 18:10
S14	138	S13 and encapsula\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/22 18:11

EAST Search History (I nterference)

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Search Notes 	Application/Control No. 12153910	Applicant(s)/Patent Under Reexamination PENG, JACKY
	Examiner TIFNEY L SKYLES	Art Unit 2814

SEARCHED			
Class	Subclass	Date	Examiner
257	88, 89	04/24/2010	TLS
257	433	09/22/2010	TLS

SEARCH NOTES		
Search Notes	Date	Examiner
Search history attached	04/24/2010	TLS
Search history attached	09/22/2010	TLS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL (Submitted Only via EFS-Web)

Application Number	12153910	Filing Date	2008-05-28	Docket Number (if applicable)	PENG3033/JJC/KDW	Art Unit	2814
First Named Inventor	Jacky Peng			Examiner Name	Skyles, Tifney L.		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☒ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☒ Other
Request for Extension of Time

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to
Deposit Account No 020200

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Signature of Registered U.S. Patent Practitioner			
Signature	/Kevin D. Williams/	Date (YYYY-MM-DD)	2011-01-28
Name	KEVIN D. WILLIAMS	Registration Number	63716

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) FY 2009 <i>(Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)</i>		Docket Number (Optional) PENG3033/JJC/KDW																									
Application Number 12/153,910		Filed May 28, 2008																									
For LIGHT EMITTING DIODE LAMP PACKAGE STRUCTURE AND ASSEMBLY THEREOF																											
Art Unit 2814		Examiner Skyles, Tifney L.																									
This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application. The requested extension and fee are as follows (check time period desired and enter the appropriate fee below): <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 40%;"></th> <th style="width: 15%; text-align: center;"><u>Fee</u></th> <th style="width: 15%; text-align: center;"><u>Small Entity Fee</u></th> <th style="width: 30%;"></th> </tr> </thead> <tbody> <tr> <td>☒ One month (37 CFR 1.17(a)(1))</td> <td style="text-align: center;">\$130</td> <td style="text-align: center;">\$65</td> <td style="text-align: right;">\$ <u>65.00</u></td> </tr> <tr> <td>☐ Two months (37 CFR 1.17(a)(2))</td> <td style="text-align: center;">\$490</td> <td style="text-align: center;">\$245</td> <td style="text-align: right;">\$ _____</td> </tr> <tr> <td>☐ Three months (37 CFR 1.17(a)(3))</td> <td style="text-align: center;">\$1110</td> <td style="text-align: center;">\$555</td> <td style="text-align: right;">\$ _____</td> </tr> <tr> <td>☐ Four months (37 CFR 1.17(a)(4))</td> <td style="text-align: center;">\$1730</td> <td style="text-align: center;">\$865</td> <td style="text-align: right;">\$ _____</td> </tr> <tr> <td>☐ Five months (37 CFR 1.17(a)(5))</td> <td style="text-align: center;">\$2350</td> <td style="text-align: center;">\$1175</td> <td style="text-align: right;">\$ _____</td> </tr> </tbody> </table> ☒ Applicant claims small entity status. See 37 CFR 1.27. ☐ A check in the amount of the fee is enclosed. ☐ Payment by credit card. Form PTO-2038 is attached. ☐ The Director has already been authorized to charge fees in this application to a Deposit Account. ☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number <u>02-0200</u>. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038. I am the ☐ applicant/inventor. ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96). ☐ attorney or agent of record. Registration Number _____ ☒ attorney or agent under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 <u>63,716</u> <u>/Kevin D. Williams/</u> Signature <u>KEVIN D. WILLIAMS</u> Typed or printed name <u>January 28, 2011</u> Date <u>703-683-0500</u> Telephone Number					<u>Fee</u>	<u>Small Entity Fee</u>		☒ One month (37 CFR 1.17(a)(1))	\$130	\$65	\$ <u>65.00</u>	☐ Two months (37 CFR 1.17(a)(2))	\$490	\$245	\$ _____	☐ Three months (37 CFR 1.17(a)(3))	\$1110	\$555	\$ _____	☐ Four months (37 CFR 1.17(a)(4))	\$1730	\$865	\$ _____	☐ Five months (37 CFR 1.17(a)(5))	\$2350	\$1175	\$ _____
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☐ Five months (37 CFR 1.17(a)(5))	\$2350	\$1175	\$ _____																								
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below. ☒ Total of <u>1</u> forms are submitted.																											

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Application No.:	12/153,910	Examiner:	Skyles, Tifney L.
Filing Date:	May 28, 2008	Art Unit:	2814
First Inventor:	Jacky Peng	Customer No.:	23364
Attorney No.:	PENG3033/JJC/KDW	Confirm. No.:	1815
For:	LIGHT EMITTING DIODE LAMP PACKAGE STRUCTURE AND ASSEMBLY THEREOF		

**REPLY TO FINAL OFFICE ACTION
OF SEPTEMBER 28, 2010**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INTRODUCTORY COMMENTS

This is responsive to the Final Office Action mailed September 28, 2010 in the above application. In view of the following amendments and remarks, reconsideration of the application is respectfully requested.

A Request for Continued Examination is filed concurrently herewith.

A petition to extend the period for reply by one month is submitted herewith.

AMENDMENT

Amendments to the Claims

The claims are amended as shown on the following pages under the heading AMENDMENT TO THE CLAIMS. The list shows the status of all claims presently in the application and is intended to supersede all prior versions of the claims in the application. Any cancellation of claims is made without prejudice or disclaimer.

AMENDMENT TO THE CLAIMS

1. (Currently Amended) A LED lamp package structure, comprising:
 - a plurality of light emitting diodes, each light emitting diode having two electrode ends and one of the electrode ends being a common electrode end;
 - a control integrated circuit, having a data input electrode, [[and]] a data output electrode, a positive power-in electrode, and a negative power-in electrode, and electrically connected to the light emitting diodes, wherein the control integrated circuit receives external control data via the data input electrode to control the illumination state of each light emitting diode according to the external control data;
 - a first conductor, a second conductor, a third conductor, and a fourth conductor, the first conductor being a positive DC voltage pad and connected to the common electrode of each light emitting diode and the positive power-in electrode of the control integrated circuit, the second conductor being connected to the data input electrode, the third conductor being connected to the data output electrode, the fourth conductor being a negative DC voltage pad and connected to the negative power-in electrode of the control integrated circuit; and
 - a package body encapsulating the light emitting diodes, the control integrated circuit and the conductors, a portion of the first conductor, the second conductor, the third conductor, and the fourth conductor being exposed outside the package body.
2. (Original) The light emitting diode lamp package structure according to claim 1, wherein the common electrode end is a positive DC voltage pad or a negative DC voltage pad.

3. (Previously Presented) The light emitting diode lamp package structure according to claim 1, further comprising a circuit board carrying the light emitting diodes and the control integrated circuit.
4. (Original) The light emitting diode lamp package structure according to claim 3, wherein the light emitting diodes and the control integrated circuit are mounted on the same surface of the circuit board.
5. (Withdrawn) The light emitting diode lamp package structure according to claim 3, wherein the light emitting diodes are mounted on one surface of the circuit board and the control integrated circuit is mounted on the other surface of the circuit board.
6. (Original) The light emitting diode lamp package structure according to claim 1, wherein the conductors are an electric conductivity support or a conductive wire.
7. (Withdrawn) The light emitting diode lamp package structure according to claim 1, wherein the first conductor forms a platform inside the package body, said platform carrying the light emitting diodes, and the first conductor being electrically connected to the light emitting diodes.
8. (Withdrawn) The light emitting diode lamp package structure according to claim 1, wherein the fourth conductor forms a platform inside the package body, the platform carrying the control integrated circuit, and the fourth conductor being electrically connected to the control integrated circuit.

9. (Original) The light emitting diode lamp package structure according to claim 1, wherein the first conductor and the fourth conductor are connected to two opposing sides of the package body, and the second conductor and the third conductor are connected to two opposing sides of the package body.
10. (Original) The light emitting diode lamp package structure according to claim 1, wherein the first conductor and the fourth conductor are connected to the same side of the package body, while the second conductor and the third conductor are connected to two opposing sides of the package body.
11. (Original) The light emitting diode lamp package structure according to claim 1, further comprising a fifth conductor and a sixth conductor, the fifth conductor being a positive DC voltage pad and the sixth conductor being a negative DC voltage pad.
12. (Original) The light emitting diode lamp package structure according to claim 11, wherein the first conductor and the fifth conductor are connected to two opposing sides of the package body, the second conductor and the third conductor are connected to two opposing sides of the package body, while the fourth conductor and the sixth conductor are connected to two opposing sides of the package body.
13. (Withdrawn) The light emitting diode lamp package structure according to claim 3, wherein two opposing surfaces of the circuit board each carrying a redlight emitting diode, a green light emitting diode, and a bluelight emitting diode.

14. (Withdrawn) The light emitting diode lamp package structure according to claim 1, wherein the package body is an injection-molded transparent glue in spherical or hemispherical shape.
15. (Original) The light emitting diode lamp package structure according to claim 1, wherein the package body is in rectangular shape, said rectangle having a light emitting window, the light emitting diodes aligning with the light emitting window inside the rectangle.
16. (Withdrawn) A light emitting diode lamp assembly, comprising:
- a light emitting diode lamp having a plurality of light emitting diodes and four electric conductivity supports encapsulated in a package body;
 - a lampshade covering the package body of the light emitting diode lamp;
 - a socket being a body having a perforation and extended with a plug-in member, the perforation accommodating the light emitting diodes and enabling the four electric conductivity supports to expose outside the body; and
 - a mount formed with a socket, the socket having four electrode contacts inside such that when the socket is plugged into the socket, the four electrode contacts being in contact with the four electric conductivity supports respectively.
17. (Withdrawn) The light emitting diode lamp assembly according to claim 16, wherein the plurality of light emitting diodes are mounted on a circuit board, the circuit board carrying a control integrated circuit, the four electric conductivity supports being respectively a positive DC voltage pad, a data input end, a data output end, and a negative DC voltage pad.

18. (Withdrawn) The light emitting diode lamp assembly according to claim 16, wherein the four electric conductivity supports have a flat shape and are flexible.
19. (Withdrawn) The light emitting diode lamp assembly according to claim 16, wherein the upper half of the socket accommodates the body, while the lower half of the body is coupled to the plug-in member.
20. (Withdrawn) The light emitting diode lamp assembly according to claim 16, wherein the socket forms a through-hole, the four electrode contacts passing through the through-hole to connect with four external wires respectively.
21. (Withdrawn) A light emitting diode lamp assembly, comprising:
a light emitting diode lamp having a package body and a circuit board, the package body encapsulating a plurality of light emitting diodes and four electric conductivity supports, the four electric conductivity supports being electrically connected to the circuit board, and the circuit board carrying a control integrated circuit and forming a positive DC voltage electrode, a data input electrode, a data output electrode and a negative DC voltage electrode;
a lampshade covering the package body of the light emitting diode lamp; and
a mount formed with a socket, the socket having four electrode contacts inside such that when the circuit board of the light emitting diode lamp is plugged into the socket, the four electrode contacts being in contact with the positive DC voltage electrode, the data input electrode, the data output electrode and the negative DC voltage electrode respectively.

22. (Withdrawn) A light emitting diode lamp assembly, comprising:

a light emitting diode lamp having a package body and a circuit board, the package body encapsulating a plurality of light emitting diodes and a control integrated circuit disposed on one side of the circuit board, a plurality of electrodes being disposed at two opposing sides of the circuit board, wherein the two opposing sides of the circuit board are respectively disposed with a data input electrode and a data output electrode;

a lampshade covering the periphery of the light emitting diode lamp; and

two mounts, each mount formed with a socket, the socket having electrode contacts inside corresponding to the electrodes of the circuit board, wherein the sockets of the two mounts are respectively coupled to the two opposing sides of the circuit board of light emitting diode lamp, and the lampshade is situated between the two mounts.

23. (Withdrawn) A package structure of the light emitting diode lamp, comprising:

a plurality of light emitting diodes, each light emitting diode having two electrode ends and one of the electrode ends being a common electrode end;

a circuit board, mounting a plurality of light emitting diodes;

a package body, encapsulating said light emitting diodes and a part of said circuit board; and

a control integrated circuit, having a data input electrode and a data output electrode and electrically connected to said light emitting diodes to control the illumination state of each light emitting diode;

wherein said circuit board being exposed outside the part of the package body carrying said control integrated circuit, and said circuit board having a first conduct electricity, a second conduct electricity, a third conduct electricity, and a fourth conduct electricity being exposed outside the package body;

24. (Withdrawn) The light emitting diode lamp package structure according to claim 23, wherein said first conduct electricity is the positive DC voltage end, said second conduct electricity connecting said data output electrode, said third conduct electricity connecting said data output electrode, and said fourth conduct electricity is the negative DC voltage end.

REMARKS

The claims were finally rejected in the Office action of September 28, 2010. This response amends the claims as described below. A Request for Continued Examination is concurrently filed herewith to gain entry of the present claims. In view of the following particulars, reconsideration of the pending application is respectfully requested.

1. Interview summary

The applicants thank Examiner Skyles for the opportunity to discuss the pending application on January 6, 2011. During the interview, the subject matter of the pending claims and U.S. patent application publication 2008/0087903 (*Stoyan*) were discussed.

During the interview, the undersigned pointed out that *Stoyan* does not disclose a control integrated circuit that receives external control data via a data input electrode of the control integrated circuit, as required by pending claim 1.

It was further pointed out that the electrode in contact with the control device 1400B and facing the upper portion of the LED module 110 in Fig. 14A is electrically connected to the contact strip 1401, and the electrode in contact with the control device 1400B and facing the lower portion of the LED module 110 is electrically connected to the contact strip 1402. Further, referring to paragraphs [0066] – [0067], the contact strips 1401, 1402 are used to provide a supply voltage only. Thus, it is clear that the electrodes in contact with the control device 1400B and connected to the contact strips 1401, 1402 are not data input electrodes.

The examiner contended that the limitation regarding the data input electrode is a functional limitation and that the electrodes of the control device 1400B are capable of receiving data.

2. In the claims

Claim 1 is amended to recite that the control integrated circuit has a power-in electrode and a negative power-in electrode, and that a positive DC voltage pad is connected to the positive power-in electrode and a negative DC voltage pad is connected to the negative power-in electrode. Support for this amendment is found on page 7, line 21 to page 8, line 20 of the specification, as originally filed.

It is clear that there is support in the specification for the amendatory language; thus, no new matter is added by these amendments.

Entry of the Amendment to the claims is respectfully requested in the next Office action.

3. Rejection of claims 1-4, 6, and 9-12 under 35 USC 102(e) as being anticipated by US publication 2008/0087903 (*Stoyan*)

Reconsideration of this rejection is respectfully requested in view of the amendments to independent claim 1 and the following remarks which demonstrate that *Stoyan* does not teach every feature of the pending claims.

In observing amended claim 1, the claim requires a control integrated circuit having a data input electrode, a data output electrode, power-in electrode and a negative power-in electrode, wherein a positive DC voltage pad is connected to the positive power-in electrode and a negative DC voltage pad is connected to the negative power-in electrode. Further, the control integrated circuit receives external control data via the data input electrode to control the illumination state of each light emitting diode according to the external control data.

It is submitted that *Stoyan* does not disclose a control integrated circuit having a data input electrode, a data output electrode, power-in electrode and a negative power-in electrode, wherein a positive DC voltage pad is connected to the positive power-in electrode, a negative DC voltage pad is connected to the negative power-in electrode, and the control integrated circuit receives external control data via the data

input electrode to control the illumination state of each light emitting diode according to the external control data, as required by amended claim 1.

Stoyan discloses a control device 1400 electrically connected to the contact strips 1401, 1402, and the radiation emitting semiconductor component 100. The contact strips 1401 and 1402 are used to provide a supply voltage and the control device 1400 is provided for supplying that voltage to the radiation emitting semiconductor component 1000.

Similarly, in the embodiment of Fig 14A, the control device 1400B is electrically connected to the contact strips 1401,1402 for providing a supply voltage to the three radiation emitting semiconductor components 1000. The LED modules disclosed in *Stoyan* neither receive nor transmit control data for controlling the illumination state of each LED.

Indeed, as can be seen in Fig. 14A, the electrodes on the top of the control device 1400B are respectively connected to the contact strips 1401,1402, and the electrodes on the bottom of the control device 1400B are respectively connected to the semiconductor components. In other words, the electrodes of the control device 1400B which are input electrodes (the contact strips 1401 and 1402) are used only for providing a supply voltage. That is, the electrodes of the control device 1400B merely correspond to the positive power-in electrode and the negative power-in electrode of the pending claims.

Thus, *Stoyan* does not disclose a control integrated circuit having a data input electrode and a data output electrode, wherein the control integrated circuit receives external control data via the data input electrode to control the illumination state of each light emitting diode according to the external control data.

As such, *Stoyan* does not disclose a control integrated circuit having a data input electrode, a data output electrode, power-in electrode and a negative power-in electrode, wherein a positive DC voltage pad is connected to the positive power-in electrode, a negative DC voltage pad is connected to the negative power-in electrode,

and the control integrated circuit receives external control data via the data input electrode to control the illumination state of each light emitting diode according to the external control data, as recited in amended claim 1.

In addition, the wiring layout of the circuit board 13 of the present invention enables the control IC 12 to electrically connect the red, blue and green LEDs 11 respectively. The red, blue and green LEDs 11 have a common electrode end, the common electrode end being a Vdd pad. Hence, *Stoyan* does not disclose a first conductor being a positive DC voltage pad and connected to a common electrode of each light emitting diode.

Claims 2-4, 6, and 9-12 are also considered to be patentable as containing all of the elements of claim 1, as well as for their respective individually recited features.

In view of these observations, it is respectfully submitted that *Stoyan* fails to anticipate the pending claims of this rejection. Accordingly, withdrawal of this rejection is kindly requested.

4. Rejection of claim 15 under 35 USC 103(a) as being unpatentable over US publication 2008/0087903 (*Stoyan*) in view of US patent 7,473,933 (*Yan*)

Claim 15 depends from claim 1 and is likewise allowable for the reasons above in view of its dependency from claim 1 and its individually recited features. *Yan* does not cure the deficiencies of *Stoyan* as discussed above in claim 1.

Accordingly, claim 15 is patentable at least on the basis of its dependency from claim 1.

Therefore, withdrawal of the rejection of the claims in view of the prior art is kindly requested.

5. Conclusion

As a result of the amendment to the claims, and further in view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is respectfully requested that every pending claim in the present application be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the applicants' attorney, the examiner is invited to contact the undersigned at the numbers shown below.

BACON & THOMAS, PLLC
625 Slaters Lane, Fourth Floor
Alexandria, Virginia 22314-1176
Phone: (703) 683-0500
Facsimile: (703) 683-1080

Date: January 28, 2011

Respectfully submitted,

/Kevin D. Williams/

KEVIN D. WILLIAMS
Attorney for Applicants
Registration No. 63,716

Electronic Patent Application Fee Transmittal

Application Number:	12153910			
Filing Date:	28-May-2008			
Title of Invention:	Light emitting diode lamp package structure and assembly thereof			
First Named Inventor/Applicant Name:	Jacky Peng			
Filer:	Kevin Denard Williams/Katy Ward			
Attorney Docket Number:	PENG3033/JJC/KDW			
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with \$0 paid	2251	Xu Peicheng	EX. 1002, p. 114	

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for continued examination	2801	1	405	405
Total in USD (\$)				470

Electronic Acknowledgement Receipt

EFS ID:	9327598
Application Number:	12153910
International Application Number:	
Confirmation Number:	1815
Title of Invention:	Light emitting diode lamp package structure and assembly thereof
First Named Inventor/Applicant Name:	Jacky Peng
Customer Number:	23364
Filer:	Kevin Denard Williams/Katy Ward
Filer Authorized By:	Kevin Denard Williams
Attorney Docket Number:	PENG3033/JJC/KDW
Receipt Date:	28-JAN-2011
Filing Date:	28-MAY-2008
Time Stamp:	13:18:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$470
RAM confirmation Number	9127
Deposit Account	020200
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and examination processing fees)

Xu Peicheng Ex. 1002, p. 116

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	PENG3033RCE01282011.pdf	698027	no	3
			abd23cb94a4eda0c98bd9eb9cb737410945fe92e		

Warnings:

Information:

2	Extension of Time	PENG3033EOT01282011.pdf	227493	no	1
			bb02271c8e47b7da6fb284e4aeac5b5a79dc9581		

Warnings:

Information:

3		Response_AF_1-28-11.pdf	362886	yes	13
			118897904aee86fc4152761dea87ae62b9925160		

Multipart Description/PDF files in .zip description

	Document Description	Start	End
	Amendment After Final	1	1
	Claims	2	8
	Applicant Arguments/Remarks Made in an Amendment	9	13

Warnings:

Information:

4	Fee Worksheet (PTO-875)	fee-info.pdf	32296	no	2
			ed1746314e05b29069686e3f933d4a14d1093381		

Warnings:

Information:

Total Files Size (in bytes):			1320702
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/153,910		Filing Date 05/28/2008		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☒ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(j))	minus 20 =	*	X \$	=		X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=		X \$	=			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	01/28/2011	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 24	Minus	** 24	= 0	X \$26 =	0		X \$	=
	Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X \$110 =	0		X \$	=
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE	0		TOTAL ADD'L FEE	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=		X \$	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=		X \$	=
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/ZURIASHWORK ZENEBE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/153,910

05/28/2008

Jacky Peng

PENG3033/JJC/KDW

1815

23364 7590 02/16/2011

BACON & THOMAS, PLLC
625 SLATERS LANE
FOURTH FLOOR
ALEXANDRIA, VA 22314-1176

EXAMINER

SKYLES, TIFNEY L

ART UNIT

PAPER NUMBER

2814

MAIL DATE

DELIVERY MODE

02/16/2011

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/153,910	Applicant(s) PENG, JACKY	
	Examiner TIFNEY L. SKYLES	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 January 2011.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) 5,7,8,13,14 and 16-24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4,6,9-12 and 15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 May 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/28/2011 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The amendments to claim 1 state "a positive power-in electrode, and a negative power-in electrode." However, the specification fails to provide support for the newly added limitations.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-4, 6, and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell (US 7,717,596) in view of Stoyan (2008/0087903).

Regarding Claim 1, Bell teaches an LED lamp package structure, comprising: a plurality of light emitting diodes **32** [Fig. 5], each light emitting diode **32** having two electrode ends and one of the electrode ends being a common electrode end (wire that meets and connects with 42); a control integrated circuit **44**, having a data input electrode **18c**, a data output electrode (wire connected to 46), a positive power-in electrode (wire connected to 42), and a negative power-in electrode (wire connected to the wire connected to 18c), and electrically connected to the light emitting diodes **32**, wherein the control integrated circuit **44** receives external control data via the data input electrode **18c** to control the illumination state of each light emitting diode according to the external control data [Col. 5, Lines 13-16]; a first conductor **18a**, a second conductor **18c**, a third conductor **46**, and a fourth conductor **18b**, the first conductor being a positive DC voltage pad **18a** and connected to the common electrode of each light emitting diode **32** and the positive power-in electrode (wire connected to 42) of the control

Art Unit: 2814

integrated circuit **44**, the second conductor being connected to the data input electrode **18c**, the third conductor **46** being connected to the data output electrode, the fourth conductor being a negative DC voltage pad **18b** and connected to the negative power-in electrode (wire connected to the wire connected to 18c) of the control integrated circuit **44**; but fails to teach a package body encapsulating the light emitting diodes, the control integrated circuit and the conductors, a portion of the first conductor, the second conductor, the third conductor, and the fourth conductor being exposed outside the package body. However, Stoyan teaches a package body **110** [Fig. 14a] encapsulating the light emitting diodes **1000**, the control integrated circuit **1400B** and the conductors **1240, 1250, 1401, 1402**, a portion of the first conductor **1401**, the second conductor **1250**, the third conductor **1240**, and the fourth conductor **1402** being exposed outside the package body [see Fig. 5]. Therefore, it would have been obvious to a person having ordinary skill in the art to combine Stoyan with Bell because an individually configurable light emitting diode arrangement will be provided [Para. 0004].

Regarding Claim 2, Bell in view of Stoyan teach the limitations of claim 1 and Bell teaches the light emitting diode lamp package structure according to claim 1, wherein the common electrode end (wire that meets and connects with 42) is a positive DC voltage pad **18a** or a negative DC voltage pad **18b**.

Regarding Claim 3, Bell in view of Stoyan teach the limitations of claim 1 and Bell further teaches the light emitting diode lamp package structure according to claim 1, further comprising a circuit board **84** [Fig. 8] carrying the light emitting diodes **32** and the control integrated circuit **44**.

Regarding Claim 4, Bell in view of Stoyan teach the limitations of claim 3 and Bell further teaches the light emitting diode lamp package structure according to claim 3, wherein the light emitting diodes **32** and the control integrated circuit **44** are mounted on the same surface of the circuit board **84**.

Regarding Claim 6, Bell in view of Stoyan teach the limitations of claim 1 and Bell further teaches the light emitting diode lamp package structure according to claim 1, wherein the conductors are an electric conductivity support or a conductive wire [see Fig. 5].

Regarding Claim 9, Bell in view of Stoyan teach the limitations of claim 1 and Stoyan further teaches the light emitting diode lamp package structure according to claim 1, wherein the first conductor **1401** and the fourth **1402** conductor are connected to two opposing sides of the package body **110**, and the second conductor **1250** and the third conductor **1140** are connected to two opposing sides of the package body **110**.

Regarding Claim 10, Bell in view of Stoyan teach the limitations of claim 1 and Stoyan further teaches the light emitting diode lamp package structure according to claim 1, wherein the first conductor **1401** and the fourth conductor **1230** are connected to the same side of the package body **110**, while the second conductor **1250** and the third conductor **1140** are connected to two opposing sides of the package body **110**.

Regarding Claim 11, Bell in view of Stoyan teach the limitations of claim 1 and Stoyan further teaches the light emitting diode lamp package structure according to claim 1, further comprising a fifth conductor **1210** and a sixth conductor **1230**, the fifth conductor **1210** being a positive DC voltage pad and the sixth conductor **1230** being a negative DC voltage pad [Para. 0066].

Regarding Claim 12, Bell in view of Stoyan teach the limitations of claim 1 and Stoyan further teaches the light emitting diode lamp package structure according to claim 11, wherein the first conductor **1401** and the fifth conductor **1210** are connected to two opposing sides of the package body **110**, the second conductor **1250** and the third conductor **1140** are connected to two opposing sides of the package body **110**, while the fourth conductor **1402** and the sixth conductor **1230** are connected to two opposing sides of the package body **110**.

Art Unit: 2814

1. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bell in view of Stoyan as applied to claims 1-4, 6, and 9-12 above, and further in view of Yan (US 7,473,933).

Regarding Claim 15, Bell in view of Stoyan teach the limitations of claim 1 and Stoyan further teaches the light emitting diode lamp package structure according to claim 1, wherein the package body is in rectangular shape [Para. 0065] but fails to teach said rectangle having a light emitting window wherein the light emitting diodes are aligned with the light emitting window inside the rectangle. However, Yan teaches said rectangle having a light emitting window **690** [Fig. 6B] wherein the light emitting diodes **640** are aligned with the light emitting window **680** inside the rectangle. Therefore, it would have been obvious at the time the invention was made to combine Yan with Bell and Stoyan for the purposes of focusing the light emitted from the LED package [Col. 11, Lines 35-40].

Response to Arguments

2. Applicant's arguments with respect to claims 1-4, 6, 9-12, and 15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIFNEY L. SKYLES whose telephone number is (571)270-5019. The examiner can normally be reached on Mon-Fri 7:30AM - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Howard Weiss/
Primary Examiner
Art Unit 2814

TLS

Notice of References Cited	Application/Control No. 12/153,910	Applicant(s)/Patent Under Reexamination PENG, JACKY	
	Examiner TIFNEY L. SKYLES	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,717,596	05-2010	Bell, Alan	362/494
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 12153910	Applicant(s)/Patent Under Reexamination PENG, JACKY
	Examiner TIFNEY L SKYLES	Art Unit 2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant						☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE									
Final	Original	01/30/2010	04/24/2010	09/22/2010	02/12/2011						
	1	÷	✓	✓	✓						
	2	÷	✓	✓	✓						
	3	÷	✓	✓	✓						
	4	÷	✓	✓	✓						
	5	÷	N	N	N						
	6	÷	✓	✓	✓						
	7	÷	N	N	N						
	8	÷	N	N	N						
	9	÷	✓	✓	✓						
	10	÷	✓	✓	✓						
	11	÷	✓	✓	✓						
	12	÷	✓	✓	✓						
	13	÷	N	N	N						
	14	÷	N	N	N						
	15	÷	✓	✓	✓						
	16	÷	N	N	N						
	17	÷	N	N	N						
	18	÷	N	N	N						
	19	÷	N	N	N						
	20	÷	N	N	N						
	21	÷	N	N	N						
	22	÷	N	N	N						
	23	÷	N	N	N						
	24	÷	N	N	N						

Search Notes 	Application/Control No. 12153910	Applicant(s)/Patent Under Reexamination PENG, JACKY
	Examiner TIFNEY L SKYLES	Art Unit 2814

SEARCHED			
Class	Subclass	Date	Examiner
257	88, 89	04/24/2010	TLS
257	433	09/22/2010	TLS

SEARCH NOTES		
Search Notes	Date	Examiner
Search history attached	04/24/2010	TLS
Search history attached	09/22/2010	TLS
Updated history attached	02/12/2011	TLS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S15	1	"12153910"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/02/12 13:02
S16	2037	(257/88).OCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/02/12 13:18
S17	1657	S16 and @ad<="20080528"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/02/12 13:18
S18	94	S17 and (led or "light emitting diode") and (control adj circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/02/12 13:18
S19	250	S17 and (led or "light emitting diode") and (circuit adj board)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/02/12 15:02
S20	100	S17 and (led or "light emitting diode") and (common adj electrode)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/02/12 15:02
S21	88	S20 not S18	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/02/12 15:02
S22	16	S21 and ((input same output) or "I/O")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/02/12 15:03
S23	2	("20010024368").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/02/12 15:35
S24	47859	(led or "light emitting diode") and ((control adj circuit) and (input same output) or "I/O") and voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/02/12 15:38
S25	758	((led or "light emitting diode") and ((control adj circuit) and (input same output) or "I/O") and voltage).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/02/12 15:38
S26	33692	(led or "light emitting diode") and (control adj circuit) and ((input same output) or "I/O") and voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/02/12 15:39

S27	693	((led or "light emitting diode") and (control adj circuit) and ((input same output) or "I/O") and voltage).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/02/12 15:39
S28	1878	(led or "light emitting diode") same ((control adj circuit) same ((input same output) or "I/O")) same voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/02/12 15:40
S29	347	S28 and packag\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/02/12 15:41
S30	313	S29 and @ad<="20080528"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/02/12 17:05

EAST Search History (I nterference)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Application No.:	12/153,910	Confirm. No.:	1815
Filing Date:	May 28, 2008	Examiner:	Skyles, Tifney L.
First Inventor:	Jacky PENG	Art Unit:	2814
Attorney No.:	PENG3033/JJC/KDW	Customer No.:	23364
For:	LIGHT EMITTING DIODE LAMP PACKAGE STRUCTURE AND ASSEMBLY THEREOF		

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INTRODUCTORY COMMENTS

This pre-appeal brief request for review is filed concurrently with a notice of appeal.

ARGUMENTS

In the outstanding Office Action mailed February 16, 2011, the examiner rejects claims 1-4, 6 and 9-12 as being unpatentable over U.S. patent 7,717,596 (*Bell*) in view of U.S. patent application publication 2008/0087903 (*Stoyan*).

The applicant considers the rejection of at least independent claim 1 to be improper based on clear error in fact and other deficiencies in view of the following observations.

In observing independent claim 1, the claim is directed to an LED lamp package structure, comprising a plurality of light emitting diodes, each light emitting diode having two electrode ends and one of the electrode ends being a common electrode end.

The LED lamp package further includes a control integrated circuit, having a data input electrode, a data output electrode, a positive power-in electrode, and a

negative power-in electrode. The control integrated circuit is electrically connected to the light emitting diodes and receives external control data via the data input electrode to control the illumination state of each light emitting diode according to the external control data.

Further, the package device also includes a first conductor, a second conductor, a third conductor, and a fourth conductor, the first conductor being a positive DC voltage pad and connected to the common electrode of each light emitting diode and the positive power-in electrode of the control integrated circuit, the second conductor being connected to the data input electrode, the third conductor being connected to the data output electrode, the fourth conductor being a negative DC voltage pad and connected to the negative power-in electrode of the control integrated circuit.

1. Rejection of claim 1 under 35 U.S.C. 112 as failing to comply with the written description requirement.

Referring to the Fig. 1 of the present drawing as originally filed, it is clear that the control IC 12 has a positive power-in electrode 14 and a negative power-in electrode 15 connected to the Vdd pad and Vss pad, respectively, to receive a DC voltage (Fig. 4A; col. 11, lines 6-14; col. 3, lines 10-12; col. 8, lines 12-13).

The supply pins Vdd and Vss provide power to the control circuit 12. Thus, it is clear that the electrodes of the control circuit 12 that receive the conductors supply pins Vdd and Vss are positive power-in and negative power-in electrodes. It is submitted that one skilled in the art would understand these features of the control circuit.

Therefore, it is submitted that no new matter has been added to the application.

2. The proposed combination of Bell and Stoyan does not teach or suggest the “each light emitting diode having two electrode ends and one of the electrode ends being a common electrode end,” as required by pending claim 1.

The rejection relies on the LEDs 32 in Bell and the wire extending from the LEDs and connecting to the power supply (Fig. 5; col. 4, lines 51-61) as respective

teachings of the light emitting diodes and the common electrode of the light emitting diodes.

In observing Fig. 5 of Bell, it is clear that the LEDs 32 are connected in series; thus the LEDs do not comprise a common electrode. In contrast to Bell, the light emitting diodes of the pending claims each have two electrodes (Fig. 2B), wherein one of the electrodes of each light emitting diode is commonly connected to the Vdd pad.

As such, the proposed combination of Bell and Stoyan does not teach or suggest the “each light emitting diode having two electrode ends and one of the electrode ends being a common electrode end,” as recited in pending claim 1.

3. The proposed combination of Bell and Stoyan does not teach or suggest “the first conductor being a positive DC voltage pad and connected to the common electrode of each light emitting diode and the positive power-in electrode of the control integrated circuit,” as required by pending claim 1.

The rejection relies on the wire 18a in Bell as a teaching of the positive DC voltage pad, and the “wire connected to power supply 42” as a teaching of the positive power-in electrode of the control integrated circuit of the pending claims.

As explained above, the LEDs do not have a common electrode, since they are connected in series. Further, the wire 18a, itself, is not connected to a positive power in electrode of the control circuit 44.

In contrast to Bell, the first conductor Vdd of the pending claims is connected to the common electrode of each light emitting diode and the positive power-in electrode of the control integrated circuit 12.

As such, the proposed combination of Bell and Stoyan does not teach or suggest “the first conductor being a positive DC voltage pad and connected to the common electrode of each light emitting diode and the positive power-in electrode of the control integrated circuit,” as recited in pending claim 1.

4. The proposed combination of Bell and Stoyan does not teach or suggest a “third conductor being connected to the data output electrode,” as required by claim 1.

The rejection relies on the light intensity control devices 46 as a teaching of the third conductor of the pending claims. The light intensity control devices 46 are resistors used to limit the current to the LEDs 32 (col. 5, lines 32-35). As such, the devices clearly cannot be considered conductors.

In contrast to Bell, the third conductor Dout is provided to transmit electrical signals without diminishing the signals. As such, the proposed combination of Bell and Stoyan does not teach or suggest a “third conductor being connected to the data output electrode” as recited in claim 1.

5. The proposed combination of Bell and Stoyan does not teach or suggest “a data output electrode,” as required by claim 1.

The rejection relies on the wire connecting the control circuit 44 to the light intensity control devices 46 as a teaching of a data output electrode of the pending claims. It is noted that the data output electrode of the pending claims outputs the control data to the data input electrode of the next lamp 10 rather than to the LEDs 11 inside the same lamp.

The wire connected to the LIC device 46 in Bell does not correspond to the data output electrode of the present application.

In view of the foregoing remarks, it is respectfully submitted there is clear error in fact and other deficiencies in the rejection of the claims. As such, withdrawal of the rejection of the claims is kindly requested.

If any issues remain that may be resolved by a telephone or facsimile communication with the applicant’s attorney, the examiner is invited to contact the undersigned at the numbers shown below.

BACON & THOMAS, PLLC
625 Slaters Lane, Fourth Floor
Alexandria, Virginia 22314-1176
Phone: (703) 683-0500
Facsimile: (703) 683-1080

Date: May 16, 2011

Respectfully submitted,

/Kevin D. Williams/

KEVIN D. WILLIAMS
Attorney for Applicant
Registration No. 63,716

Electronic Patent Application Fee Transmittal

Application Number:	12153910			
Filing Date:	28-May-2008			
Title of Invention:	Light emitting diode lamp package structure and assembly thereof			
First Named Inventor/Applicant Name:	Jacky Peng			
Filer:	Kevin Denard Williams			
Attorney Docket Number:	PENG3033/JJC/KDW			
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Notice of appeal	2401	1	270	270
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				270

Electronic Acknowledgement Receipt

EFS ID:	10095325
Application Number:	12153910
International Application Number:	
Confirmation Number:	1815
Title of Invention:	Light emitting diode lamp package structure and assembly thereof
First Named Inventor/Applicant Name:	Jacky Peng
Customer Number:	23364
Filer:	Kevin Denard Williams/Kim Forsell
Filer Authorized By:	Kevin Denard Williams
Attorney Docket Number:	PENG3033/JJC/KDW
Receipt Date:	16-MAY-2011
Filing Date:	28-MAY-2008
Time Stamp:	15:26:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$270
RAM confirmation Number	1797
Deposit Account	020200
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part Pzip	Pages (if appl.)
		Xu Peicheng Ex 1002	1092 p. 140		

1	Notice of Appeal Filed	Appeal_Notice_051611.pdf	39159 b74ef34287b92fe33a7f24081177aa62b0db e174	no	1
Warnings:					
Information:					
2	Transmittal Letter	Pre-Appeal_Xmittal.pdf	242853 01db79b968ed90dc6642d2daf5ea468fec8 2d946	no	1
Warnings:					
Information:					
3	Pre-Brief Conference request	pre-appeal-brief- review_5-16-11.pdf	306733 0f419331c0dafd60ac052ab7a7271f8701eff b7d	no	4
Warnings:					
Information:					
4	Fee Worksheet (PTO-875)	fee-info.pdf	30121 a781af6ab85f0a929d117e999d1f70f2504a59 5341	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			618866		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

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**NOTICE OF APPEAL FROM THE EXAMINER TO
THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Docket Number (Optional)

PENG3033/JJC/KDW

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on _____

Signature _____

Typed or printed
name _____In re Application of
Jacky PENGApplication Number
12/153,910Filed
May 28, 2008

For LIGHT EMITTING DIODE LAMP PACKAGE STRUCTURE AND ASSEMBLY THEREOF

Art Unit
2814Examiner
Skyles, Tifney L.Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the examiner.The fee for this Notice of Appeal is (37 CFR 41.20(b)(1)) \$ 540

☒ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is: \$ 270

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 02-0200.

☐ A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

/Kevin D. Williams/

Signature

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

KEVIN D. WILLIAMS

Typed or printed name

☐ attorney or agent of record.
Registration number _____

703-683-0500

Telephone number

☒ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34. 63,716

May 16, 2011

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 41.31. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) PENG3033/JJC/KDW					
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on _____ Signature _____ Typed or printed name _____	Application Number 12/153,910	Filed May 28, 2008					
	First Named Inventor Jacky PENG						
	Art Unit 2814	Examiner Skyles, Tifney L.					
Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a notice of appeal. The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided. I am the <table style="width: 100%; border: none;"><tr><td style="width: 50%; vertical-align: top; padding-bottom: 10px;">☐ applicant/inventor. ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) ☐ attorney or agent of record. Registration number _____</td><td style="width: 50%; vertical-align: top; padding-bottom: 10px; text-align: right;">/Kevin D. Williams/ _____ Signature KEVIN D. WILLIAMS _____ Typed or printed name 703-683-0500 _____ Telephone number May 16, 2011 _____ Date</td></tr><tr><td style="vertical-align: top;">☒ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 <u>63,716</u></td><td></td></tr></table> NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.				☐ applicant/inventor. ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) ☐ attorney or agent of record. Registration number _____	/Kevin D. Williams/ _____ Signature KEVIN D. WILLIAMS _____ Typed or printed name 703-683-0500 _____ Telephone number May 16, 2011 _____ Date	☒ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 <u>63,716</u>	
☐ applicant/inventor. ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) ☐ attorney or agent of record. Registration number _____	/Kevin D. Williams/ _____ Signature KEVIN D. WILLIAMS _____ Typed or printed name 703-683-0500 _____ Telephone number May 16, 2011 _____ Date						
☒ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 <u>63,716</u>							
☒ *Total of <u>1</u> forms are submitted.							

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/153,910

05/28/2008

Jacky Peng

PENG3033/JJC/KDW

1815

23364 7590 07/19/2011

BACON & THOMAS, PLLC
625 SLATERS LANE
FOURTH FLOOR
ALEXANDRIA, VA 22314-1176

EXAMINER

SKYLES, TIFNEY L

ART UNIT

PAPER NUMBER

2814

MAIL DATE

DELIVERY MODE

07/19/2011

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of Panel Decision from Pre-Appeal Brief Review	Application/Control No.	Applicant(s)/Patent under Reexamination	
	12/153,910	PENG, JACKY	
	TIFNEY SKYLES	Art Unit	
		2814	

This is in response to the Pre-Appeal Brief Request for Review filed 16 May 2011.

1. ☐ **Improper Request** – The Request is improper and a conference will not be held for the following reason(s):

- ☐ The Notice of Appeal has not been filed concurrent with the Pre-Appeal Brief Request.
- ☐ The request does not include reasons why a review is appropriate.
- ☐ A proposed amendment is included with the Pre-Appeal Brief request.
- ☐ Other: .

The time period for filing a response continues to run from the receipt date of the Notice of Appeal or from the mail date of the last Office communication, if no Notice of Appeal has been received.

2. ☒ **Proceed to Board of Patent Appeals and Interferences** – A Pre-Appeal Brief conference has been held. The application remains under appeal because there is at least one actual issue for appeal. Applicant is required to submit an appeal brief in accordance with 37 CFR 41.37. The time period for filing an appeal brief will be reset to be one month from mailing this decision, or the balance of the two-month time period running from the receipt of the notice of appeal, whichever is greater. Further, the time period for filing of the appeal brief is extendible under 37 CFR 1.136 based upon the mail date of this decision or the receipt date of the notice of appeal, as applicable.

☒ The panel has determined the status of the claim(s) is as follows:

Claim(s) allowed: _____.

Claim(s) objected to: _____.

Claim(s) rejected: 1-4, 6, 9-12, and 15.

Claim(s) withdrawn from consideration: 5, 7, 8, 13, 14, and 16-24.

3. ☐ **Allowable application** – A conference has been held. The rejection is withdrawn and a Notice of Allowance will be mailed. Prosecution on the merits remains closed. No further action is required by applicant at this time.

4. ☐ **Reopen Prosecution** – A conference has been held. The rejection is withdrawn and a new Office action will be mailed. No further action is required by applicant at this time.

All participants:

(1) TIFNEY SKYLES.

(3) Wael Fahmy.

(2) Michael Sherry.

(4) _____.

/Tifney L Skyles/
Examiner, Art Unit 2814

/Wael M Fahmy/
Supervisory Patent Examiner, Art
Unit 2814

/Michael J Sherry/
Quality Assurance Specialist

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Application No.:	12/153,910	Confirm. No.:	1815
Filing Date:	May 28, 2008	Examiner:	Skyles, Tifney L
First Inventor:	Jacky Peng	Art Unit:	2814
Attorney No.:	PENG3033/EM/KDW	Customer No.:	23364

For: **LIGHT EMITTING DIODE LAMP PACKAGE STRUCTURE
AND ASSEMBLY THEREOF**

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INTRODUCTORY COMMENTS

This is an appeal brief filed pursuant to the appellant's appeal to the Board of Patent Appeals and Interferences from the rejection of claims 1-4, 6, 9-12 and 15 in the above-identified application.

A petition to extend the period for reply by one month is concurrently filed.

I. REAL PARTY OF INTEREST

The real party of interest is the assignee of record: Semisilicon Technology Corp.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

a. Status of claims in proceeding

Claims 1-24 are currently pending.

Claim 1 is currently rejected under 35 U.S.C. § 112 as failing to comply with the written description requirement.

Claims 1-4, 6 and 9-12 are currently rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent 7,717,596 (*Bell*) in view of U.S. patent application publication 2008/0087903 (*Stoyan*).

Claim 15 are currently rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent 7,717,596 (*Bell*) in view of U.S. patent application publication 2008/0087903 (*Stoyan*), and further in view of U.S. patent 7,473,933 (*Yan*).

Claims 5, 7, 8, 13, 14 and 16-24 are withdrawn from consideration.

b. Identification of claims on appeal

Claims 1-4, 6, 9-12 and 15 are currently appealed herein.

- Claim 1 is an independent claim, and claims 2-4, 6, 9-12 and 15 depend from claim 1.

IV. STATUS OF AMENDMENTS

There are no outstanding amendments to the claims. The most recent amendment was filed on January 28, 2011 and subsequently entered by the examiner.

V. SUMMARY OF CLAIMED SUBJECT MATTER

For the purposes of appeal, the rejections of independent claim 1 are appealed.

The patentability of dependent claims 2-4, 6, 9-12 and 15 will rise or fall based on the determination of the patentability of claim 1.

A. Claim 1

An LED lamp package structure comprises a plurality of light emitting diodes (11). Each light emitting diode has two electrode ends and one of the electrode ends is a common electrode end (col. 3, lines 3-7; Figs. 1 and 4A).

A control integrated circuit (12) has a data input electrode, a data output electrode, a positive power-in electrode, and a negative power-in electrode (Fig. 12). The control integrated circuit is electrically connected to the light emitting diodes, such that the control integrated circuit receives external control data via the data input electrode to control the illumination state of each light emitting diode according to the external control data (col. 8, lines 10-13).

The LED lamp package further comprises a first conductor, a second conductor, a third conductor, and a fourth conductor. The first conductor is a positive DC voltage pad (Vdd) and is connected to the common electrode of each light emitting diode and the positive power-in electrode of the control integrated circuit. The second conductor is connected to the data input electrode. The third conductor is connected to the data output electrode, and the fourth conductor is a negative DC voltage pad (Vss) and is connected to the negative power-in electrode of the control integrated circuit (col. 8, lines 14-20; Fig. 4).

A package body encapsulates the light emitting diodes, the control integrated circuit and the conductors such that a portion of the first conductor, the second conductor, the third conductor, and the fourth conductor is exposed outside the package body (col. 8, lines 14-20).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claim 1 is currently rejected under 35 U.S.C. § 112 as failing to comply with the written description requirement.

Claims 1-4, 6 and 9-12 are currently rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent 7,717,596 (*Bell*) in view of U.S. patent application publication 2008/0087903 (*Stoyan*).

The rejections of independent claim 1 under 35 U.S.C. § 112 and under 35 U.S.C. § 103(a) are currently appealed herein.

VII. ARGUMENT

A. Overview

Claim 1 is currently rejected under 35 U.S.C. § 112 as failing to comply with the written description requirement.

Claims 1-4, 6 and 9-12 are currently rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent 7,717,596 (*Bell*) in view of U.S. patent application publication 2008/0087903 (*Stoyan*).

The rejections of independent claim 1 under 35 U.S.C. § 112 and under 35 U.S.C. § 103(a) are currently appealed herein.

It is submitted that claim 1, as currently written, does indeed comply with the written description requirement.

It is also submitted that the proposed combination of *Bell* and *Stoyan* fails to render the independent claim 1 *prima facie* obvious. Accordingly, reversal of the rejection of claim 1 is requested, as well as the rejection of claims 2-4, 6, 9-12 and 15 which depend from claim 1.

A. Reasons for error in rejection of claim 1 as failing to comply with the written description requirement

1. The skilled artisan would have recognized in the original disclosure a positive power-in electrode and a negative power-in electrode on the control integrated circuit

MPEP 2163(I)(B) states that “while there is no *in haec verba* requirement, newly added claim limitations must be supported in the specification through express, implicit, or inherent disclosure.”

As described on page 8, lines 11-12, the LED lamp (10) has power supply pins Vdd and Vss for receiving a DC voltage. Further, as shown in Fig. 1, the control IC (12) is connected to the power supply pins Vdd and Vss. As such, it would have been clear to the skilled artisan that the control IC has a positive power-in electrode and a negative power-in electrode for receiving the DC voltage from the supply pins Vdd and Vss.

Therefore, it is submitted that no new matter has been added to the application.

B. Pertinent Law on Obviousness

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), viz., (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; and (3) the level of ordinary skill in the art.

The scope and content of the prior art, and the level of ordinary skill in the art may be evidenced by the prior art references. *In re GPAC Inc.*, 57 F.3d 1573, 1579, 35 USPQ2d 1116, 1121 (Fed. Cir. 1995); *see also In re Oelrich*, 579 F.2d 86, 91, 198 USPQ 210, 214 (CCPA 1978).

The examiner bears the initial burden of presenting a prima facie case of obviousness. *In re Oetiker*, 977 F.2d, 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). In order to establish a prima facie case of obviousness, the examiner must show that each and every limitation of the claim is described or suggested by the prior art or would have been obvious based on the knowledge of those of ordinary skill in the art. *See Fine*, 837 F.2d at 1074, 5 USPQ2d at 1598.

Furthermore, “‘there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness’.... [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR Int’l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006)). Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. *See Oetiker*, 977 F.2d at 1445, 24 USPQ2d at 1444; *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984).

C. Reasons for error in rejection of claim 1 as unpatentable over *Bell* in view of *Stoyan*

1. The proposed combination of *Bell* and *Stoyan* does not teach or suggest each light emitting diode having two electrode ends, wherein one of the electrode ends is a common electrode end

It is submitted that the proposed combination of *Bell* and *Stoyan* fails to render obvious independent claim 1, since neither *Bell* nor *Stoyan* teaches or suggests a plurality of light emitting diodes (LED), wherein each LED has a an electrode end that is respectively connected to a Vdd pad.

As described on page 8, lines 3-9 and shown in Fig. 1, the wiring layout of the circuit board (13) enables the control IC (12) to respectively connect to the red, blue and green LEDs.

The rejection relies on the LEDs (32) in *Bell* and the wire extending from the LEDs and connecting to the power supply (Fig. 5; col. 4, lines 51-61) as respective teachings of the light emitting diodes and the common electrode of the light emitting diodes.

In observing Fig. 5 of *Bell*, it is clear that the LEDs (32) are connected in series; thus the LEDs are not respectively connected to the light intensity control devices (46) or the power supply (42). Therefore, the LEDs (32) do not each have an electrode end commonly connected to a power supply or an a control circuit.

In contrast to *Bell*, the light emitting diodes of the pending claims each have two electrodes (Fig. 2B), wherein one of the electrodes of each light emitting diode is commonly connected to the Vdd pad.

It is submitted that there is no teaching, suggestion or other motivation that would have inclined the skilled artisan to modify *Bell* to have the LEDs (32) respectively connected to the light intensity control devices (46) or the power supply (42).

As such, the proposed combination of *Bell* and *Stoyan* does not teach or suggest a plurality of light emitting diodes each having two electrode ends, wherein one of the electrode ends is a common electrode end, as recited in pending claim 1.

2. The proposed combination of *Bell* and *Stoyan* does not teach or suggest a first conductor as a positive DC voltage pad, wherein the first conductor is connected to a common electrode of each

light emitting diode and a positive power-in electrode of a control integrated circuit

As shown in Fig. 1, a positive DC voltage pad (Vdd) is connected to a common electrode of each light emitting diode (11) and a positive power-in electrode of a control integrated circuit (12).

The rejection relies on the wire (18a) in *Bell* as a teaching of the positive DC voltage pad, and the “wire connected to power supply (42)” as a teaching of the positive power-in electrode of the control integrated circuit of the pending claims.

As explained above, the LEDs in *Bell* do not have a common electrode since they are connected in series. Further, the wire (18a), itself, is not connected to a positive power in electrode of the control circuit (44).

In contrast to *Bell*, the first conductor Vdd of the pending claims is connected to the common electrode of each light emitting diode and the positive power-in electrode of the control integrated circuit (12).

As such, the proposed combination of *Bell* and *Stoyan* does not teach or suggest a first conductor as a positive DC voltage pad, where in first conductor is connected to a common electrode of each light emitting diode and a positive power-in electrode of a control integrated circuit, as recited in pending claim 1.

3. The proposed combination of *Bell* and *Stoyan* does not teach or suggest a third conductor connected to a data output electrode

The rejection relies on the light intensity control devices (46) as a teaching of the third conductor of the pending claims. The light intensity control devices (46) are resistors used to limit the current to the LEDs 32 (col. 5, lines 32-35). As such, the devices clearly cannot be considered conductors.

In contrast to *Bell*, the third conductor Dout (Fig. 1) in the instant invention is provided to transmit electrical signals from a data output electrode without diminishing the signals (a resistor would diminish the signals). As such, the proposed combination of *Bell* and *Stoyan* does not teach or suggest a third conductor connected to the data output electrode, as recited in claim 1.

4. The proposed combination of *Bell* and *Stoyan* does not teach or suggest a data output electrode

The rejection relies on the wire connecting the control circuit (44) to the light intensity control devices (46) as a teaching of a data output electrode of the pending claims. It is noted that the data output electrode of the pending claims outputs the control data to the data input electrode of the next lamp (10) rather than to the LEDs (11) inside the same lamp.

The wire connected to the LIC device (46) in Bell does not correspond to the data output electrode of the present application.

5. Closing Remarks

For the reasons described above, the proposed combination of *Bell* and *Stoyan* fails to render obvious independent claim 1. Further, it is submitted that the original disclosure fully supports the current claims.

Reversal of these rejections is kindly requested.

VIII. CONCLUSION

For the reasons set forth above, independent claim 1 of the pending application defines subject matter that is not anticipated or unpatentable within the meaning of 35 U.S.C. § 102(b) and 103(a), respectively. Further, it is submitted that the original disclosure fully supports the current claims, as required in 35 U.S.C. 112.

Reversal of the rejections of claim 1 and allowance of these claims are respectfully requested.

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Date: September 19, 2011

Respectfully submitted,

/Kevin D. Williams/

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IX. CLAIMS APPENDIX

1. (Previously Presented) A LED lamp package structure, comprising:
 - a plurality of light emitting diodes, each light emitting diode having two electrode ends and one of the electrode ends being a common electrode end;
 - a control integrated circuit, having a data input electrode, a data output electrode, a positive power-in electrode, and a negative power-in electrode, and electrically connected to the light emitting diodes, wherein the control integrated circuit receives external control data via the data input electrode to control the illumination state of each light emitting diode according to the external control data;
 - a first conductor, a second conductor, a third conductor, and a fourth conductor, the first conductor being a positive DC voltage pad and connected to the common electrode of each light emitting diode and the positive power-in electrode of the control integrated circuit, the second conductor being connected to the data input electrode, the third conductor being connected to the data output electrode, the fourth conductor being a negative DC voltage pad and connected to the negative power-in electrode of the control integrated circuit; and
 - a package body encapsulating the light emitting diodes, the control integrated circuit and the conductors, a portion of the first conductor, the second conductor, the third conductor, and the fourth conductor being exposed outside the package body.
2. (Original) The light emitting diode lamp package structure according to claim 1, wherein the common electrode end is a positive DC voltage pad or a negative DC voltage pad.
3. (Previously Presented) The light emitting diode lamp package structure according to claim 1, further comprising a circuit board carrying the light emitting diodes and the control integrated circuit.
4. (Original) The light emitting diode lamp package structure according to claim 3, wherein the light emitting diodes and the control integrated circuit are mounted on the same surface of the circuit board.

5. (Withdrawn) The light emitting diode lamp package structure according to claim 3, wherein the light emitting diodes are mounted on one surface of the circuit board and the control integrated circuit is mounted on the other surface of the circuit board.
6. (Original) The light emitting diode lamp package structure according to claim 1, wherein the conductors are an electric conductivity support or a conductive wire.
7. (Withdrawn) The light emitting diode lamp package structure according to claim 1, wherein the first conductor forms a platform inside the package body, said platform carrying the light emitting diodes, and the first conductor being electrically connected to the light emitting diodes.
8. (Withdrawn) The light emitting diode lamp package structure according to claim 1, wherein the fourth conductor forms a platform inside the package body, the platform carrying the control integrated circuit, and the fourth conductor being electrically connected to the control integrated circuit.
9. (Original) The light emitting diode lamp package structure according to claim 1, wherein the first conductor and the fourth conductor are connected to two opposing sides of the package body, and the second conductor and the third conductor are connected to two opposing sides of the package body.
10. (Original) The light emitting diode lamp package structure according to claim 1, wherein the first conductor and the fourth conductor are connected to the same side of the package body, while the second conductor and the third conductor are connected to two opposing sides of the package body.
11. (Original) The light emitting diode lamp package structure according to claim 1, further comprising a fifth conductor and a sixth conductor, the fifth conductor being a positive DC voltage pad and the sixth conductor being a negative DC voltage pad.

12. (Original) The light emitting diode lamp package structure according to claim 11, wherein the first conductor and the fifth conductor are connected to two opposing sides of the package body, the second conductor and the third conductor are connected to two opposing sides of the package body, while the fourth conductor and the sixth conductor are connected to two opposing sides of the package body.
13. (Withdrawn) The light emitting diode lamp package structure according to claim 3, wherein two opposing surfaces of the circuit board each carrying a redlight emitting diode, a green light emitting diode, and a bluelight emitting diode.
14. (Withdrawn) The light emitting diode lamp package structure according to claim 1, wherein the package body is an injection-molded transparent glue in spherical or hemispherical shape.
15. (Original) The light emitting diode lamp package structure according to claim 1, wherein the package body is in rectangular shape, said rectangle having a light emitting window, the light emitting diodes aligning with the light emitting window inside the rectangle.
16. (Withdrawn) A light emitting diode lamp assembly, comprising:
- a light emitting diode lamp having a plurality of light emitting diodes and four electric conductivity supports encapsulated in a package body;
 - a lampshade covering the package body of the light emitting diode lamp;
 - a socket being a body having a perforation and extended with a plug-in member, the perforation accommodating the light emitting diodes and enabling the four electric conductivity supports to expose outside the body; and
 - a mount formed with a socket, the socket having four electrode contacts inside such that when the socket is plugged into the socket, the four electrode contacts being in contact with the four electric conductivity supports respectively.

17. (Withdrawn) The light emitting diode lamp assembly according to claim 16, wherein the plurality of light emitting diodes are mounted on a circuit board, the circuit board carrying a control integrated circuit, the four electric conductivity supports being respectively a positive DC voltage pad, a data input end, a data output end, and a negative DC voltage pad.
18. (Withdrawn) The light emitting diode lamp assembly according to claim 16, wherein the four electric conductivity supports have a flat shape and are flexible.
19. (Withdrawn) The light emitting diode lamp assembly according to claim 16, wherein the upper half of the socket accommodates the body, while the lower half of the body is coupled to the plug-in member.
20. (Withdrawn) The light emitting diode lamp assembly according to claim 16, wherein the socket forms a through-hole, the four electrode contacts passing through the through-hole to connect with four external wires respectively.
21. (Withdrawn) A light emitting diode lamp assembly, comprising:
 - a light emitting diode lamp having a package body and a circuit board, the package body encapsulating a plurality of light emitting diodes and four electric conductivity supports, the four electric conductivity supports being electrically connected to the circuit board, and the circuit board carrying a control integrated circuit and forming a positive DC voltage electrode, a data input electrode, a data output electrode and a negative DC voltage electrode;
 - a lampshade covering the package body of the light emitting diode lamp; and
 - a mount formed with a socket, the socket having four electrode contacts inside such that when the circuit board of the light emitting diode lamp is plugged into the socket, the four electrode contacts being in contact with the positive DC voltage electrode, the data input electrode, the data output electrode and the negative DC voltage electrode respectively.

22. (Withdrawn) A light emitting diode lamp assembly, comprising:

a light emitting diode lamp having a package body and a circuit board, the package body encapsulating a plurality of light emitting diodes and a control integrated circuit disposed on one side of the circuit board, a plurality of electrodes being disposed at two opposing sides of the circuit board, wherein the two opposing sides of the circuit board are respectively disposed with a data input electrode and a data output electrode;

a lampshade covering the periphery of the light emitting diode lamp; and

two mounts, each mount formed with a socket, the socket having electrode contacts inside corresponding to the electrodes of the circuit board, wherein the sockets of the two mounts are respectively coupled to the two opposing sides of the circuit board of light emitting diode lamp, and the lampshade is situated between the two mounts.

23. (Withdrawn) A package structure of the light emitting diode lamp, comprising:

a plurality of light emitting diodes, each light emitting diode having two electrode ends and one of the electrode ends being a common electrode end;

a circuit board, mounting a plurality of light emitting diodes;

a package body, encapsulating said light emitting diodes and a part of said circuit board; and

a control integrated circuit, having a data input electrode and a data output electrode and electrically connected to said light emitting diodes to control the illumination state of each light emitting diode;

wherein said circuit board being exposed outside the part of the package body carrying said control integrated circuit, and said circuit board having a first conduct electricity, a second conduct electricity, a third conduct electricity, and a fourth conduct electricity being exposed outside the package body;

24. (Withdrawn) The light emitting diode lamp package structure according to claim 23, wherein said first conduct electricity is the positive DC voltage end, said second conduct electricity connecting said data output electrode, said third conduct electricity connecting said data output electrode, and said fourth conduct electricity is the negative DC voltage end.

X. EVIDENCE APPENDIX

There are no copies of evidence entered and relied upon in this appeal
of the pending application.

XI. RELATED PROCEEDINGS APPENDIX

There are no related proceedings or decisions rendered by a court or the Board of Appeals in any proceeding identified in the related appeals and interferences section in the pending application.

Under the paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) FY 2009 <i>(Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)</i>		Docket Number (Optional) PENG3033/EM/KDW																									
Application Number 12/153,910		Filed May 28, 2008																									
For LIGHT EMITTING DIODE LAMP PACKAGE STRUCTURE AND ASSEMBLY THEREOF																											
Art Unit 2814		Examiner Skyles, Tifney L.																									
This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application. The requested extension and fee are as follows (check time period desired and enter the appropriate fee below): <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 40%;"></th> <th style="width: 15%; text-align: center;"><u>Fee</u></th> <th style="width: 20%; text-align: center;"><u>Small Entity Fee</u></th> <th style="width: 25%;"></th> </tr> </thead> <tbody> <tr> <td>☒ One month (37 CFR 1.17(a)(1))</td> <td style="text-align: center;">\$130</td> <td style="text-align: center;">\$65</td> <td style="text-align: right;">\$ <u>65</u></td> </tr> <tr> <td>☐ Two months (37 CFR 1.17(a)(2))</td> <td style="text-align: center;">\$490</td> <td style="text-align: center;">\$245</td> <td style="text-align: right;">\$ _____</td> </tr> <tr> <td>☐ Three months (37 CFR 1.17(a)(3))</td> <td style="text-align: center;">\$1110</td> <td style="text-align: center;">\$555</td> <td style="text-align: right;">\$ _____</td> </tr> <tr> <td>☐ Four months (37 CFR 1.17(a)(4))</td> <td style="text-align: center;">\$1730</td> <td style="text-align: center;">\$865</td> <td style="text-align: right;">\$ _____</td> </tr> <tr> <td>☐ Five months (37 CFR 1.17(a)(5))</td> <td style="text-align: center;">\$2350</td> <td style="text-align: center;">\$1175</td> <td style="text-align: right;">\$ _____</td> </tr> </tbody> </table> ☒ Applicant claims small entity status. See 37 CFR 1.27. ☐ A check in the amount of the fee is enclosed. ☐ Payment by credit card. Form PTO-2038 is attached. ☐ The Director has already been authorized to charge fees in this application to a Deposit Account. ☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number <u>02-0200</u>. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038. I am the ☐ applicant/inventor. ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96). ☐ attorney or agent of record. Registration Number _____ ☒ attorney or agent under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 <u>63,716</u> <u>/Kevin D. Williams/</u> Signature <u>KEVIN D. WILLIAMS</u> Typed or printed name <u>September 19, 2011</u> Date <u>703-683-0500</u> Telephone Number					<u>Fee</u>	<u>Small Entity Fee</u>		☒ One month (37 CFR 1.17(a)(1))	\$130	\$65	\$ <u>65</u>	☐ Two months (37 CFR 1.17(a)(2))	\$490	\$245	\$ _____	☐ Three months (37 CFR 1.17(a)(3))	\$1110	\$555	\$ _____	☐ Four months (37 CFR 1.17(a)(4))	\$1730	\$865	\$ _____	☐ Five months (37 CFR 1.17(a)(5))	\$2350	\$1175	\$ _____
	<u>Fee</u>	<u>Small Entity Fee</u>																									
☒ One month (37 CFR 1.17(a)(1))	\$130	\$65	\$ <u>65</u>																								
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☐ Five months (37 CFR 1.17(a)(5))	\$2350	\$1175	\$ _____																								
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below. ☒ Total of <u>1</u> forms are submitted.																											

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	12153910			
Filing Date:	28-May-2008			
Title of Invention:	Light emitting diode lamp package structure and assembly thereof			
First Named Inventor/Applicant Name:	Jacky Peng			
Filer:	Kevin Denard Williams/Laura Khweis			
Attorney Docket Number:	PENG3033/JJC/KDW			
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Notice of appeal	2401	1	270	270
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Xu Peicheng Ex. 1002, p. 168				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension - 1 month with \$0 paid	2251	1	65	65
Miscellaneous:				
Total in USD (\$)				335

Electronic Acknowledgement Receipt

EFS ID:	10976467
Application Number:	12153910
International Application Number:	
Confirmation Number:	1815
Title of Invention:	Light emitting diode lamp package structure and assembly thereof
First Named Inventor/Applicant Name:	Jacky Peng
Customer Number:	23364
Filer:	Kevin Denard Williams/Laura Khweis
Filer Authorized By:	Kevin Denard Williams
Attorney Docket Number:	PENG3033/JJC/KDW
Receipt Date:	19-SEP-2011
Filing Date:	28-MAY-2008
Time Stamp:	13:56:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$335
RAM confirmation Number	216
Deposit Account	020200
Authorized User	WILLIAMS,KEVIN D.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and examination processing fees)

Xu Peicheng Ex. 1002, p. 170

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Appeal Brief Filed	Appeal_brief_9-19-11.pdf	183028	no	21
			f5205537c366063e328109d4e2ffec026792349f		

Warnings:

Information:

2	Extension of Time	EOT_9-19-11.pdf	220061	no	1
			d476cb57c5bf0b02aab22ce31dcdc32d801f578		

Warnings:

Information:

3	Fee Worksheet (SB06)	fee-info.pdf	32032	no	2
			cdacf896e37f93e48df1da01184dad9d38d4b6d8		

Warnings:

Information:

Total Files Size (in bytes):			435121
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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NOTICE OF ALLOWANCE AND FEE(S) DUE

23364 7590 12/23/2011
BACON & THOMAS, PLLC
625 SLATERS LANE
FOURTH FLOOR
ALEXANDRIA, VA 22314-1176

EXAMINER

SKYLES, TIFNEY L

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 12/23/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/153,910

05/28/2008

Jacky Peng

PENG3033/JJC/KDW

1815

TITLE OF INVENTION: LIGHT EMITTING DIODE LAMP PACKAGE STRUCTURE AND ASSEMBLY THEREOF

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$870	\$300	\$0	\$1170	03/23/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

23364 7590 12/23/2011
BACON & THOMAS, PLLC
625 SLATERS LANE
FOURTH FLOOR
ALEXANDRIA, VA 22314-1176

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

12/153,910 05/28/2008 Jacky Peng PENG3033/JJC/KDW 1815

TITLE OF INVENTION: LIGHT EMITTING DIODE LAMP PACKAGE STRUCTURE AND ASSEMBLY THEREOF

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional YES \$870 \$300 \$0 \$1170 03/23/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
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SKYLES, TIFNEY L 2814 257-088000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s); (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Xu Peicheng Ex. 1002, p. 173



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/153,910	05/28/2008	Jacky Peng	PENG3033/JJC/KDW	1815

23364 7590 12/23/2011
BACON & THOMAS, PLLC
625 SLATERS LANE
FOURTH FLOOR
ALEXANDRIA, VA 22314-1176

EXAMINER

SKYLES, TIFNEY L

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 12/23/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 159 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 159 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/153,910	PENG, JACKY	
	Examiner	Art Unit	
	TIFNEY SKYLES	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Appeal Brief filed 09/19/2011.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-24.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| <ol style="list-style-type: none"> 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date ____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | <ol style="list-style-type: none"> 5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date ____. 7. ☐ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other ____. |
|--|--|

DETAILED ACTION

This Office action is in response to the brief filed on 09/19/2011.

Acknowledgment

1. The appeal brief filed on 09/19/2011, responding to the Office action mailed on 02/16/2011, has been entered. The present Office action is made with all the suggested amendments and arguments being fully considered. Accordingly, pending in this Office action are claims 1-24.

Election/Restrictions

2. Claims 1-24 are allowable. Claims 5, 7, 8, 13, 14, and 16-24, previously withdrawn from consideration as a result of a restriction requirement, require all the limitations of an allowable claim. Pursuant to the procedures set forth in MPEP § 821.04(a), **the restriction requirement among inventions I - XI, as set forth in the Office action mailed on 02/03/2010, is hereby withdrawn** and claims 5, 7, 8, 13, 14, and 16-24 are hereby rejoined and fully examined for patentability under 37 CFR 1.104. In view of the withdrawal of the restriction requirement, applicant(s) are advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once the restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Allowable Subject Matter

3. Claims 1-24 are allowed.

4. The following is an examiner's statement of reasons for allowance: the prior art of record fails to teach an LED lamp package structure, comprising: a plurality of light emitting diodes, each light emitting diode having two electrode ends and one of the electrode ends being a common electrode end; a control integrated circuit, having a data input electrode~ [[and]] a data output electrode, a positive power-in electrode, and a negative power-in electrode, and electrically connected to the light emitting diodes, wherein the control integrated circuit receives external control data via the data input electrode to control the illumination state of each light emitting diode according to the external control data; a first conductor, a second conductor, a third conductor, and a fourth conductor, the first conductor being a positive DC voltage pad and connected to the common electrode of each light emitting diode and the positive power-in electrode of the control integrated circuit, the second conductor being connected to the data input electrode, the third conductor being connected to the data output electrode, the fourth conductor being a negative DC voltage pad and connected to the negative power-in electrode of the control integrated circuit; and a package body encapsulating the light emitting diodes, the control integrated circuit and the conductors, a portion of the first conductor, the second conductor, the third conductor, and the fourth conductor being exposed outside the package body.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Stoyan teaches a light emitting diode arrangement comprising a plurality of LED modules.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIFNEY SKYLES whose telephone number is (571)270-5019. The examiner can normally be reached on Mon-Fri 7:30AM - 5:00PM EST.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

Art Unit: 2814

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Marcos D. Pizarro/
Primary Examiner, Art Unit 2814

TLS

EAST Search History

EAST Search History (Prior Art)

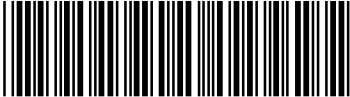
Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L16	2522	(257/88).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/12/16 00:06
L17	1746	L16 and @ad<="20080528"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/12/16 00:06
L18	106	L17 and (led or "light emitting diode") and (common adj electrode)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2011/12/16 00:06

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L27	13	((light adj emitting adj diode) and electrode and common and package).clm.	US-PGPUB	OR	ON	2011/12/16 00:18

12/ 16/ 2011 12:21:28 AM

C:\ Users\ tsyles\ Documents\ EAST\ Workspaces\ 12153910.wsp

Issue Classification 	Application/Control No.		Applicant(s)/Patent under Reexamination	
	12/153,910		PENG, JACKY	
	Examiner		Art Unit	
	TIFNEY SKYLES		2814	

ISSUE CLASSIFICATION												
ORIGINAL					CROSS REFERENCE(S)							
CLASS		SUBCLASS			CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)						
257		88			257	89	433					
INTERNATIONAL CLASSIFICATION												
H	0	1	L	33/48								
				/								
				/								
				/								
				/								
/TIFNEY SKYLES/ (Assistant Examiner) (Date)					/Marcos D. Pizarro/ 12/16/2011 (Primary Examiner) (Date)					Total Claims Allowed: 24		
										O.G. Print Claim(s)	O.G. Print Fig.	
(Legal Instruments Examiner) (Date)										1	4A	

☒ Claims renumbered in the same order as presented by applicant												☐ CPA		☐ T.D.		☐ R.1.47	
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original				
1	1		31		61		91		121		151		181				
2	2		32		62		92		122		152		182				
3	3		33		63		93		123		153		183				
4	4		34		64		94		124		154		184				
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	29		59		89		119		149		179		209				
	30		60		90		120		150		180		210				

<i>Index of Claims</i> 	Application/Control No. 12153910	Applicant(s)/Patent Under Reexamination PENG, JACKY
	Examiner TIFNEY L SKYLES	Art Unit 2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	01/30/2010	04/24/2010	09/22/2010	02/12/2011	12/15/2011				
	1	÷	✓	✓	✓	=				
	2	÷	✓	✓	✓	=				
	3	÷	✓	✓	✓	=				
	4	÷	✓	✓	✓	=				
	5	÷	N	N	N	=				
	6	÷	✓	✓	✓	=				
	7	÷	N	N	N	=				
	8	÷	N	N	N	=				
	9	÷	✓	✓	✓	=				
	10	÷	✓	✓	✓	=				
	11	÷	✓	✓	✓	=				
	12	÷	✓	✓	✓	=				
	13	÷	N	N	N	=				
	14	÷	N	N	N	=				
	15	÷	✓	✓	✓	=				
	16	÷	N	N	N	=				
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	22	÷	N	N	N	=				
	23	÷	N	N	N	=				
	24	÷	N	N	N	=				

Search Notes 	Application/Control No. 12153910	Applicant(s)/Patent Under Reexamination PENG, JACKY
	Examiner TIFNEY L SKYLES	Art Unit 2814

SEARCHED			
Class	Subclass	Date	Examiner
257	88, 89	04/24/2010	TLS
257	433	09/22/2010	TLS

SEARCH NOTES		
Search Notes	Date	Examiner
Search history attached	04/24/2010	TLS
Search history attached	09/22/2010	TLS
Updated history attached	02/12/2011	TLS
Updated search history attached	12/15/2011	TLS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	PGPub Interference search attached	12/15/2011	TLS

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

23364 7590 12/23/2011
BACON & THOMAS, PLLC
625 SLATERS LANE
FOURTH FLOOR
ALEXANDRIA, VA 22314-1176

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/153,910 05/28/2008 Jacky Peng PENG3033/JJC/KDW 1815

TITLE OF INVENTION: LIGHT EMITTING DIODE LAMP PACKAGE STRUCTURE AND ASSEMBLY THEREOF

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$870	\$300	\$0	\$1170	03/23/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
SKYLES, TIFNEY L	2814	257-088000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Bacon & Thomas, PLLC

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

SEMISILICON TECHNOLOGY CORP.

JHONGHE CITY, TAIPEI COUNTY 235, TAIWAN R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

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☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

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- ☐ A check is enclosed.
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5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Eugene Mar/

Date January 17, 2012

Typed or printed name Eugene Mar

Registration No. 25,893

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Xu Peicheng Ex. 1002, p. 185

Electronic Patent Application Fee Transmittal

Application Number:	12153910			
Filing Date:	28-May-2008			
Title of Invention:	LIGHT EMITTING DIODE LAMP PACKAGE STRUCTURE AND ASSEMBLY THEREOF			
First Named Inventor/Applicant Name:	Jacky Peng			
Filer:	Eugene Mar/Laura Khweis			
Attorney Docket Number:	PENG3033/EM			
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	2501	1	870	870
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1170

Electronic Acknowledgement Receipt

EFS ID:	11845466
Application Number:	12153910
International Application Number:	
Confirmation Number:	1815
Title of Invention:	LIGHT EMITTING DIODE LAMP PACKAGE STRUCTURE AND ASSEMBLY THEREOF
First Named Inventor/Applicant Name:	Jacky Peng
Customer Number:	23364
Filer:	Eugene Mar/Laura Khweis
Filer Authorized By:	Eugene Mar
Attorney Docket Number:	PENG3033/EM
Receipt Date:	17-JAN-2012
Filing Date:	28-MAY-2008
Time Stamp:	10:31:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 1170
RAM confirmation Number	13985
Deposit Account	020200
Authorized User	KHWEIS,LAURA

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Xu Peicheng Ex. 1002, p. 188

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	PENG3033_IF.pdf	106456	no	1
			22c25bb8216309c70971f7899e1746c87d7e42a4		

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	32150	no	2
			fd5b24f3599ce4109178d4ea0c9aa2e4cffa1c		

Warnings:

Information:

Total Files Size (in bytes):			138606
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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/153,910	02/28/2012	8124988	PENG3033/EM	1815

23364 7590 02/08/2012
BACON & THOMAS, PLLC
625 SLATERS LANE
FOURTH FLOOR
ALEXANDRIA, VA 22314-1176

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 159 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Jacky Peng, Taipei County, TAIWAN;