

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP USA, INC.

Petitioner

v.

BELL SEMICONDUCTOR, LLC

Patent Owner

Patent No. 7,646,091

**DECLARATION OF R. JACOB BAKER, P.E., PH.D. IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,646,091**

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I, R. Jacob Baker, Ph.D., P.E. declare as follows:

I. INTRODUCTION

1. I have been retained by NXP USA, Inc. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 7,646,091 (“the ’091 Patent”) (Ex. 1001).¹ I have been asked to consider whether certain references disclose or suggest the features recited in claims 1-14 of the ’091 Patent. My opinions are set forth below.

2. I am being compensated at a rate of \$765/hour for my work in this proceeding. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

II. BACKGROUND AND QUALIFICATIONS

3. I am an independent consultant. All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in designing,

¹ Where appropriate, I refer to exhibits that I understand are to be attached to the petition for Inter Partes Review of the ’091 patent.

developing, and fabricating integrated circuit packages, including ground planes and pin spacing of such integrated circuit packaging.

4. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. A copy of my current curriculum vitae, which details my education and professional and academic experience, I'm told will be submitted as Exhibit 1003. The following provides an overview of some of my experience that is relevant to the matters set forth in this declaration.

5. I presently serve as a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). In forming my opinions, I have relied on my knowledge and experience in designing, developing, and researching integrated circuit packaging and my knowledge of electrical circuit design and fabrication and electrical engineering fundamentals. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person having ordinary skill in the art.

6. I have been teaching electrical engineering at UNLV since 2012. Prior to this position, I was a Professor of Electrical and Computer Engineering at Boise State University from 2000. Prior to my position at Boise State University, I was an Associate Professor of Electrical Engineering between 1998 and 2000 and

Assistance Professor of Electrical Engineering between 1993 and 1998 at the University of Idaho. I have been teaching electrical engineering since 1991.

7. I received a Bachelor of Science and Master of Science degrees in Electrical Engineering from UNLV, in 1986 and 1988, respectively. In 1993, I also received a Ph.D. in Electrical Engineering from the University of Nevada, Reno. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada Test Site. During this time, I designed, and oversaw the fabrication and manufacture of over 30 electronic and electronic-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics.

8. From 1997 to 1999, I served as a Consultant for Tower Semiconductor, in the design of CMOS integrated circuit cells for various modem chips, interfaces, and serial buses, including charging circuits based upon power up-down circuits using an MOS or bandgap reference, pre-amplifiers, and comparators. I was also a Senior Designer at Micron Technology from 1994 to 2008, working on the development of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, CMOS Image Sensors (CISs), and power supply design. My

more recent industry experience includes working with Freedom Photonics on the integration, fabrication, and design of optoelectronics with CMOS integrated circuits, including the design of compact optical transceiver for range finding applications, Geiger mode SiGe receiver for long-range communications, and packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies. I have worked as a consultant at other companies designing electronic circuits, including Sun, Oracle, Contour Semiconductor, Lockheed-Martin, and OmniVision.

9. I have taught courses in integrated circuit design (analog, digital, mixed signal, memory circuit design, etc.), linear circuits, microelectronics, communication systems, power electronics, and fiber optics. I have been the main advisor to over 100 Master's and Doctoral students.

10. I am the author of several books covering the area of integrated circuit design including: DRAM Circuit Design: Fundamental and High-Speed Topics (two editions), CMOS Circuit Design, Layout, and Simulation (four editions), and CMOS Mixed-Signal Circuit Design (two editions). I have also authored, or coauthored, more than 100 papers and presentations in the areas of electronic circuit design. I am the named inventor on over 150 granted U.S. patents.

11. I have received numerous awards for my work, including the Frederick Emmons Terman (the "Father of Silicon Valley") Award. The Terman Award is

bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession.

12. I am a Fellow of the IEEE for contributions to memory circuit design. I have also received the IEEE Circuits and Systems Education Award (2011).

13. I have received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001), all from Boise State University.

14. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor award four of the years I have been at UNLV.

15. My curriculum vitae, which includes a more detailed summary of my background, experience, patents, designs, and publications, is Exhibit 1003.

16. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

III. MATERIALS REVIEWED

17. The opinions in this Declaration are based on the documents I reviewed, my knowledge, experience, and professional judgment. In forming my opinions expressed in this Declaration, while drawing on my knowledge and experience in designing, developing, and researching integrated circuit packages, I reviewed the following materials: U.S. Patent No. 7,646,091 (the '091 Patent) (Ex. 1001); the file

history of the '091 Patent (Ex. 1004); U.S. Patent No. 7,515,719 to Okabe et al (“Okabe”) (Ex. 1005); U.S. Patent No. 6,377,464 to Hashemi et al (“Hashemi”) (Ex. 1006); U.S. Patent No. 7,420,286 to Kramer (“Kramer”) (Ex. 1007); U.S. Patent No. 4,933,741 to Schroeder (“Schroeder”) (Ex. 1008); U.S. Patent Publication No. 2006/0001180 to Taggart et al (“Taggart”) (Ex. 1009); Johnson, H. W., & Graham, M. (1993). *High Speed Digital Design: A Handbook of Black Magic*. PTR Prentice Hall., ISBN:0-13-395724-1 (“Digital Design”) (Ex. 1010); Jinwoo Choi, Sung-Hwan Min, Joong-Ho Kim, Madhavan Swaminathan, Wendemagegnehu (Wendem) Beyene, and Xingchao (Chuck) Yuan, *Modeling and Analysis of Power Distribution Networks for Gigabit Applications*, IEEE Transactions on Mobile Computing, Vol. 2, No. 4, October-December 2003, pages 299-313 (“Choi”) (Ex. 1011); U.S. Patent Publication No. 2007/0018292 to Sutardja (“Sutardja”) (Ex. 1012); U.S. Patent No. 7,084,487 to Conn (“Conn”) (Ex. 1013); *High-Speed DSP Systems Design*, Literature Number SPRU889, May 2005, Texas Instruments (“High-Speed DSP”) (Ex. 1014); and Kester, W., & Bryant, J., *Proper Grounding Is Critical For High-Speed Systems*, Wireless Systems Design, May 2000, pages 39-42 (“Kester”) (Ex. 1015); and any other materials I refer to in this declaration in support of my opinions.

18. All of the opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my appreciation of how a person of ordinary skill in the

art would have understood the claims and the specification of the '091 Patent at the time of the alleged invention, which I have been asked to initially consider as the early 2000s (including April 6, 2006, the filing date of the '091 Patent, which I understand is the earliest possible priority date for the '091 Patent). My opinions reflect how one of ordinary skill in the art would have understood the '091 Patent, the prior art to the patent, and the state of the art at the time of the alleged invention.

19. Based on my experience and expertise, it is my opinion that certain prior art references disclose or suggest all the features recited in claims 1-14 of the '091 Patent, as I discuss in detail below.

IV. LEVEL OF ORDINARY SKILL IN THE ART

20. I am familiar with the level of ordinary skill in the art with respect to the alleged inventions of the '091 Patent as of what I understand is the earliest possible priority date of April 6, 2006. Specifically, based on my review of the '091 Patent, the technology, the educational level and experience of active workers in the field, the types of problems faced by workers in the field, the solutions found to those problems, the sophistication of the technology in the field, and drawing on my own experience, I believe a person of ordinary skill in the art would have had a bachelor's degree in a field relating to the semiconductor manufacturing process like materials science, physics, electrical engineering, or other related subjects, and at least two to three years of experience with fabrication and packaging of integrated circuits. More

education can supplement practical experience and vice versa. Depending on the engineering background and level of education of a person, it would have taken a few years for the person to become familiar with the problems encountered in the art and to become familiar with the prior and current solutions to those problems.

21. All of my opinions in this declaration are from the perspective of one of ordinary skill in the art, as I have defined it here, during the relevant timeframe (i.e., prior to April 2006).

V. TECHNICAL BACKGROUND

22. In this section, I discuss the state of the art relevant to the subject matter of the '091 Patent, as would have been known, understood, and appreciated by a person of ordinary skill in the art at the time of the alleged invention of the '091 Patent. In particular, a person of ordinary skill in the art would have been aware of various developments for various types of integrated circuit (IC) packages including various layouts for power and ground thereon, and spacing between traces, as I discuss below.

23. The various types of IC packages include flip-chip, leadframe, leadless leadframe, ball grid array (BGA), etc. The various layouts for the integrated circuits include power and ground planes for distributing power to circuitry within the integrated circuit and spacing out bonding sites, such as bond pads and fingers, to reduce the crosstalk between the bonding connections.

24. Power and ground planes, or islands, within signal routing layers of the integrated circuit as well as multiple dedicated planes for power/ground distributions are commonly used. The use of these planes is to keep the power supply and ground potentials constant, that is, free from variations (noise) which could corrupt or impact the operation of the integrated circuit. One example is the common use of separate grounds for digital and analog circuitry.

25. Similarly, spacing bonding pads/fingers apart results in varying voltage or current signals from one pad/finger having less impact, or influence, on the signals on an adjacent pad/finger. A person of ordinary skill in the art would understand that this spacing between pad/finger connections reduces “crosstalk.” Crosstalk is a term used to describe the interference between two adjacent pad/finger connections. The benefits of utilizing two or more ground planes to reduce noise was well known years prior to the date of the alleged inventions. Further spacing of bond fingers (pads) and their associated traces to minimize crosstalk was also well known years prior to the date of the alleged inventions as further indicated by the prior art references I details below.

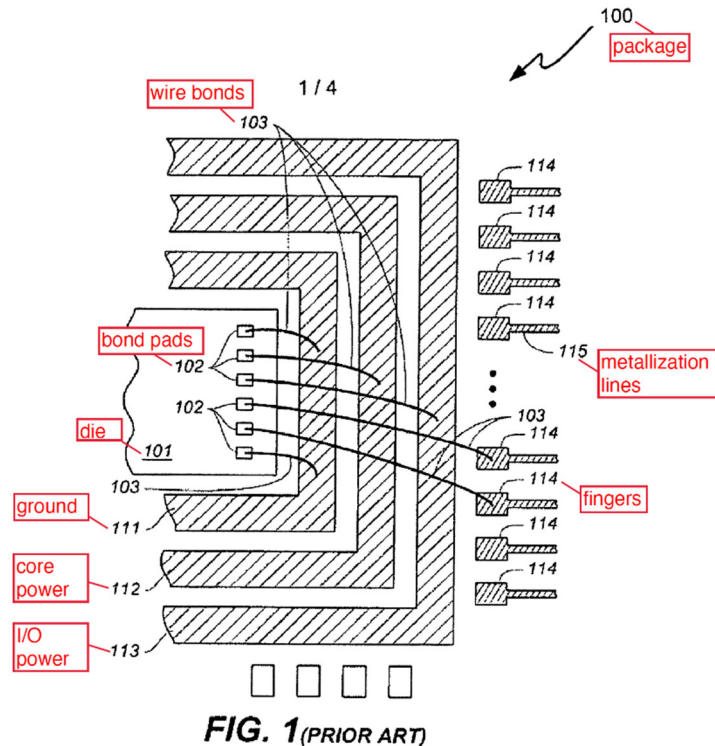
VI. THE '091 PATENT

26. The '091 Patent is entitled “Semiconductor Package and Method using Isolated Vss Plane to Accommodate High Speed Circuitry Ground Isolation” (Ex. 1001, Title) The '091 Patent discloses that it was well known in the semiconductor

industry to make use of packaging substrates to hold and electrically interconnect integrated circuit (IC) die mounted within the packaging substrate, and that implementations of the packaging substrate were configured to enable electrical connections with known external electrical interconnection socket formats. (*Id.*, 1:16-25)

27. As shown in Figure 1 below, the '091 Patent discloses that prior art integrated circuit (IC) packages included a die, a series of metallization structures arranged about the die, and electrical contact “fingers”. (*Id.*, 1:47-58) The series of metallization structures include a ground layer (Vss), a core power layer, and an input output (I/O) layer. (*Id.*, 1:50-56)

28. The '091 Patent further discloses that the prior art taught a series of bond pads of the die that are connected with the fingers, the ground layer, the core power layer, and the I/O power layer. (*Id.*, 1:62-64) The '091 Patent further discloses that the fingers are typically connected to the ground plane and that metallization lines electrically connect the fingers to vias that connect with solder balls on the bottom of the substrate. (*Id.*, 1:58-62)



(*Id.* FIG. 1 (annotated).)

29. The '091 Patent explains that in typical implementations, the IC die is grounded to a single ground plane that is grounded (e.g., by solder attachment) to another system ground (e.g., a mother board ground). (*Id.*, 1:25-29)

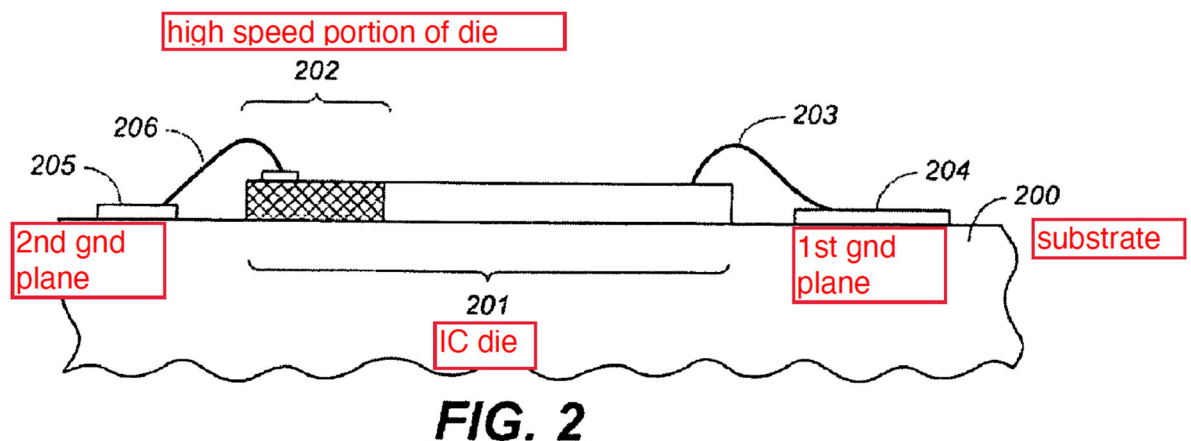
30. The '091 Patent contends that ICs with a single ground plane allows noise from high speed circuitry of the IC to interfere with low speed circuitry of the IC via the shared single ground plane. (*Id.*, 2:10-12) The '091 Patent further discloses that the prior art tried to overcome this issue by using individual pins for grounding each high-speed ground connection, which is undesirable because it uses

up a limited amount of pins of the IC and increases the density of high-speed interconnections, which causes undesirable cross talk between ground and I/O lines.

(*Id.*, 2:24-31)

31. The '091 Patent purports to solve the noise interference resulting from high speed circuitry by separating ground planes in the IC, one ground plane for high speed circuitry and one ground plane for low speed circuitry. (*Id.*, 2:45-48, 5:49-51) Notably, the '091 Patent does not disclose *any* physical or otherwise structural difference (e.g., size, materials, shape, etc.) in a ground plane enabled for use with high speed circuitry as opposed to a ground plane enabled for use with low speed circuitry.

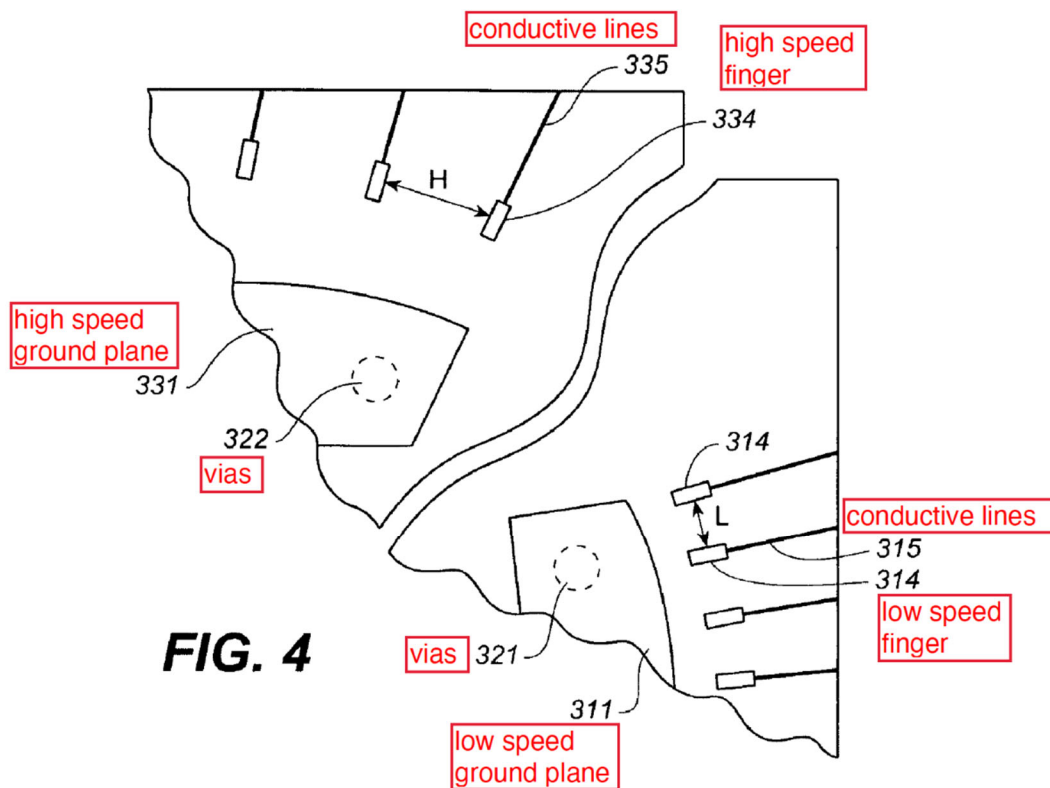
32. The separated ground planes are shown in figure 2 shown below.



(*Id.*, FIG. 2, (annotated).)

33. The '091 Patent further purports to solve the cross-talk issues for the fingers by arranging the I/O bond fingers at “an increased spaced apart distance” to affect a differential impedance sufficient to reduce the cross talk between the high speed bond finger connections and their associated metal interconnect structures. (*Id.*, 3:61 - 4:3)

34. Figure 4 shows the increased spacing for the high speed fingers used in the metal interconnect structures (e.g., conductive lines).



(*Id.*, FIG. 4, (annotated).)

VII. CLAIM CONSTRUCTION

35. I understand that claim terms are typically given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art, at the time of the alleged invention, which I was asked to assume was in April of 2006. In considering the meaning of the claims, however, I understand that one must consider the language of the claims, the specification, the prosecution history of record, and the knowledge of a person of ordinary skill in the art at the relevant time.

VIII. OVERVIEW OF THE PRIOR ART

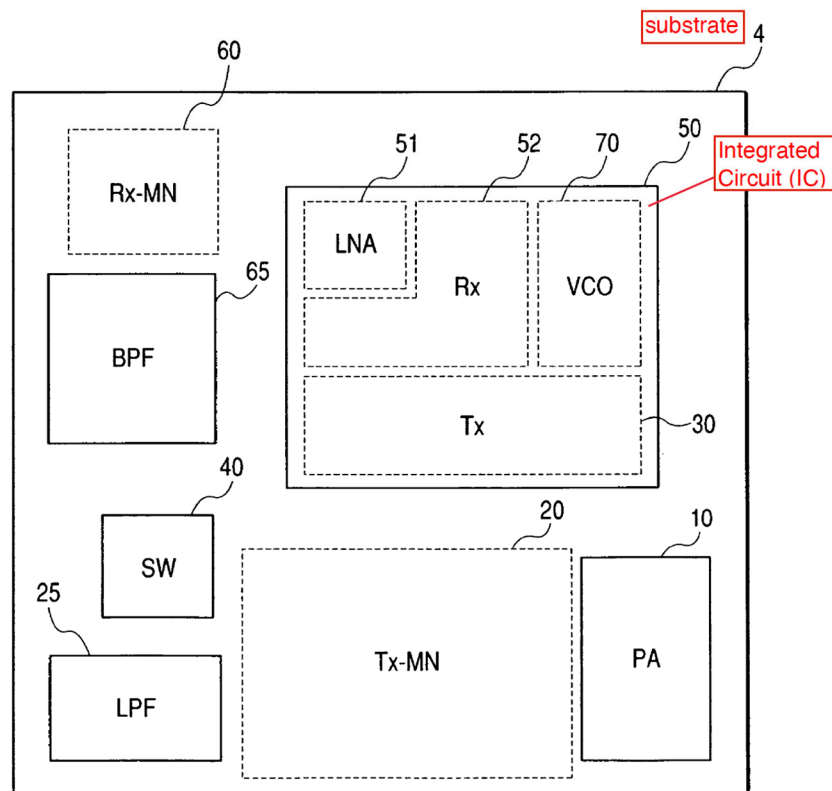
A. Okabe

36. Okabe discloses a radio frequency (RF) module comprising a module substrate that has reduced interference between its electronic circuit blocks, where the electronic circuits operate at different speeds (e.g., frequencies (e.g., 3.8 megahertz (MHz), 1.9 gigahertz (GHz), 2.1 GHz, 200 kilohertz (kHz), etc.)). (Ex. 1005, 2:66 – 3:3; 3:10-18; 7:36-43, 14:5-13) Okabe further discloses the reduced interference results from separate ground planes that are separated and electronically isolated. (*Id.* 5:39-46; Abstract.) Okabe also discloses it was well known in the art to separate ground planes to reduce interference between a first and second active circuit chip on a single interconnect substrate. (*Id.*, 2:24-41)

37. Okabe discloses that the separate ground planes can be extended to individual circuits. (*Id.*, 2:42-49) Okabe also teaches a common ground plane (e.g., a reference plane) to which all separate ground planes are connected, fixes reference potential for the individual circuits for stable performance that is not dependent on the ground land on a motherboard (*Id.*, 11:14-19)

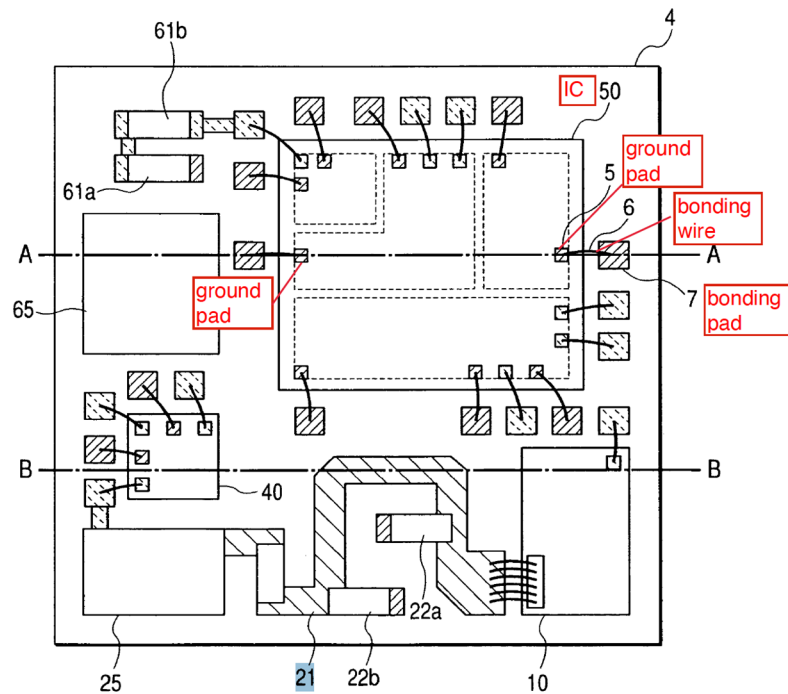
38. As shown below in Figure 3, Okabe discloses an IC 50 on a substrate 4, wherein the IC includes lower speed components and higher speed components.

FIG. 3



(*Id.*, FIG. 3 (annotated).)

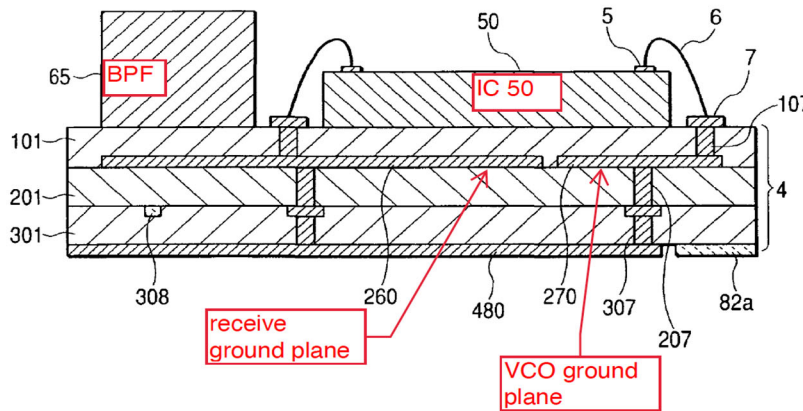
39. For example, IC 50 includes a low noise amplifier (LNA) 51, a receive (Rx) circuit 52, a transmitter (Tx) circuit 30, and a voltage controlled oscillator (VCO) 50. (*Id.*, 9:10-16)



(*Id.*, FIG. 4 (annotated).)

40. Figure 4 of Okabe shows how different components of the same IC are connected to bonding pads of the substrate 4 via bonding wire 6 and ground pad 5. Cross section A of Figure 4 is then shown in Figure 9, shown below, which shows the connection of different components of the same IC 50 to different ground planes of the substrate 4.

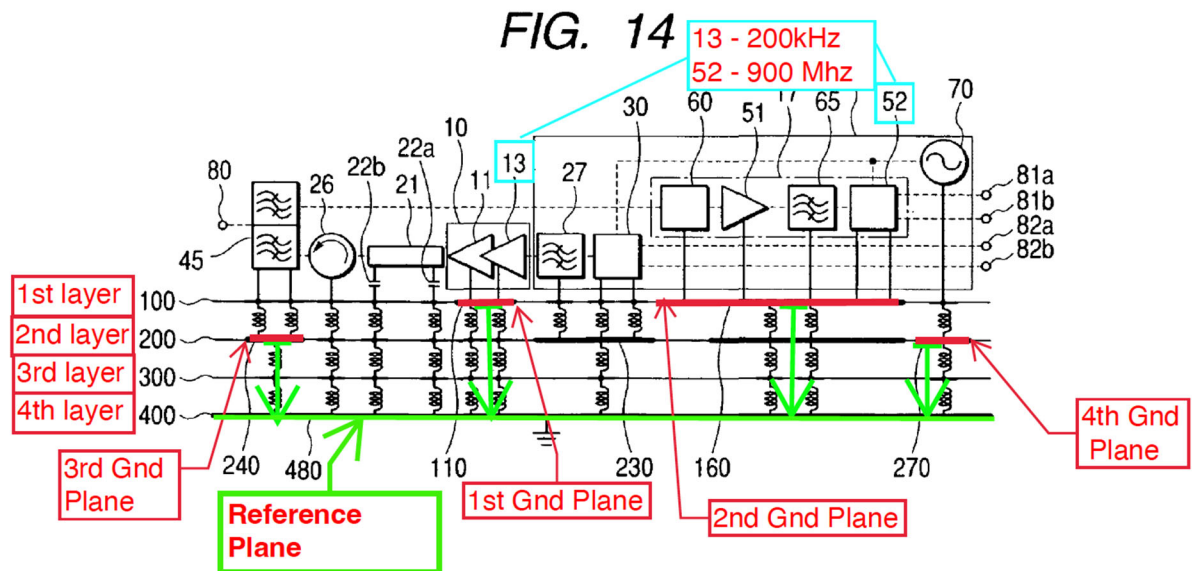
FIG. 9



(*Id.*, FIG. 9 (annotated).)

41. Okabe further discloses in Figure 14, shown below, a substrate that includes four layers 100-400, where layer 100 includes separate ground planes 110 and 160, and layer 200 includes separate ground planes 240, 230, and 270. (*Id.*, 14:26 – 15:3)

42. Okabe provides an example where the frequency of the circuit 13 is operating at 200 kilohertz (kHz), and the circuit 52 is operating at 900 megahertz (MHz). (*Id.*, 7:36-43) Thus, Okabe discloses a first layer 100 includes a first ground plane 110 connected with lower speed circuitry, and a second ground plane 160 connected with higher speed circuitry, where the first and second ground planes are separated and electrically isolated. Okabe further discloses a second layer 200 that includes a third ground plane 240 and a fourth ground plane 270 that are separated and electrically isolated. (*Id.*, 14:13-25)



(*Id.*, FIG. 14 (annotated).)

43. Figure 14 further shows a reference plane (e.g., common ground 480) that is associated with each layer of the substrate (e.g., 100-400) and the ground planes 110, 160, 230, 240, and 270. Reference numbers 81a-82b illustrated electrical contacts configured for connection with electronic circuitry external to the module substrate.

B. Hashemi

44. Hashemi discloses “a multiple chip module (MCM) for use with baseband, RF or IF applications” that includes a number of active circuit chips mounted on a substrate. (Ex. 1006, Abstract) Hashemi teaches the MCM is capable of concurrent operation at different speeds (for example, frequencies for baseband is 45 Megahertz (MHz), RF frequencies is 800 MHz, 900 MHz, 1800 MHz and 2.4

Gigahertz (GHz), and IF frequencies are within the range of approximately 200 MHz to 800 MHz). (*Id.*, 3:5-10, 43-51)

45. Hashemi discloses that the MCM can include split ground planes to achieve electronic isolation between different active circuit chips (e.g., RF and IF) and/or between different functional sections on the same active circuit chip, and vias configured as grounding connections. (*Id.*, C16; Abstract; 7:9-26) The physically separated or split ground planes can reside at different metal layers or at the same metal layer, and in Figure 1, shown below, the first and second ground planes are on the same internal metal layer. (*Id.*, C15; 7:19-21) Hashemi further discloses the substrate can include any number of metal layers with any suitable materials. (*Id.*, 4:21-40)

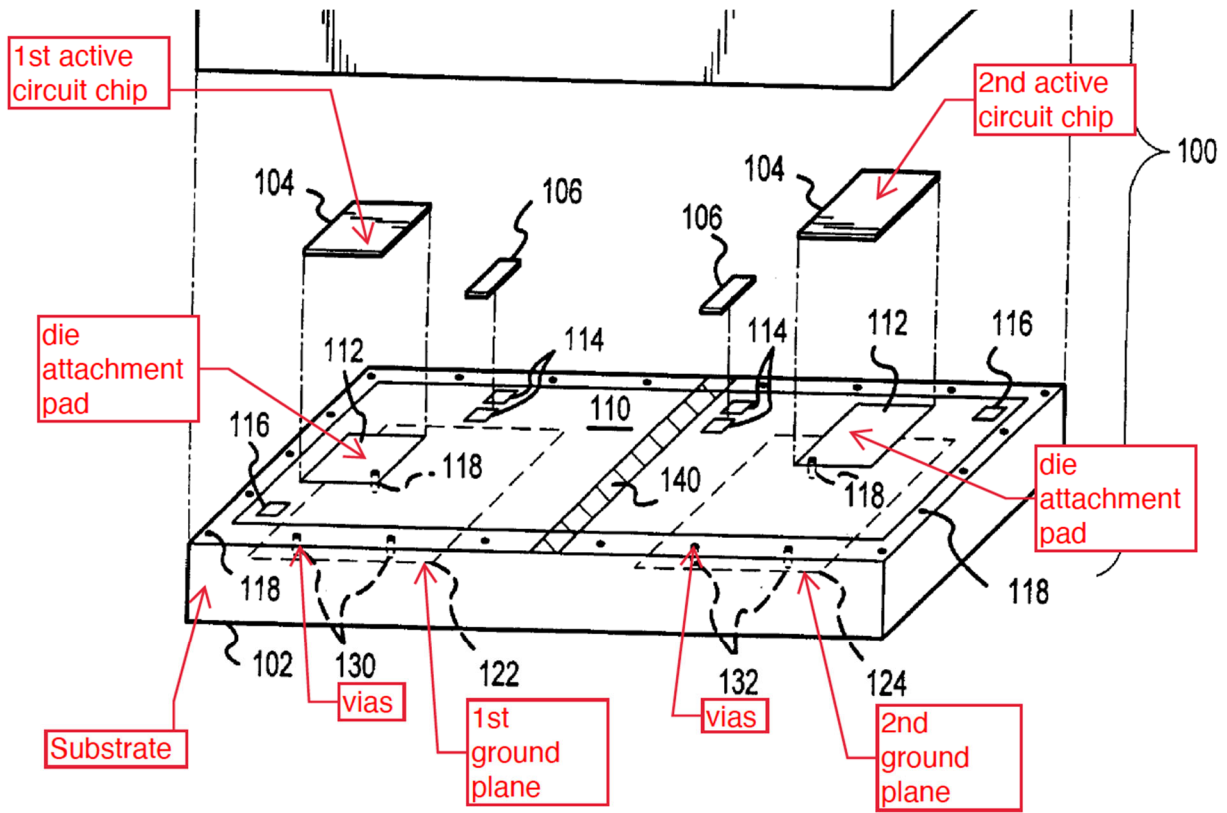


FIG.1

(*Id.*, FIG. 1 (annotated).)

46. Figure 1 of Hashemi, above, shows the split ground planes. A first ground plane 122 is used for a first active chip 104, and a second ground plane 124 is used for a second active chip 104, which reduces unwanted interference (e.g., noise). (*Id.*, 7:16-21) The vias 118 electrically connect any layer of the substrate to other layers of the substrate and electrically connect the first ground plane 122, and the second ground plane 124, to the die attachment pads 112. (*Id.*, 5:40-42; 7:21-24) Hashemi further discloses that solder balls may be used as a termination device (*Id.*,

12:24-25) and that the prior art is “replete with techniques for providing terminal connections between an IC package and a next assembly level, e.g., a mother board.” (*Id.*, 12:9-12).

47. Hashemi in Figure 7, shown below, illustrates split ground planes and although illustrated on different layers, explicitly states in the disclosure that they can be located on the same metal layer (*Id.*, 6:67 – 7:2) Hashemi further shows in Figure 7, shown below, a substrate having an upper surface and a lower surface.

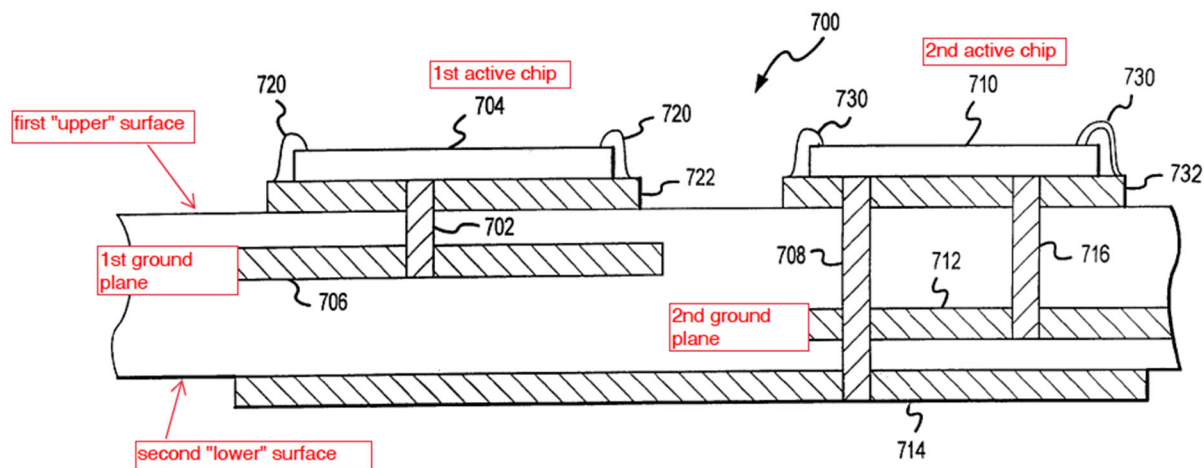


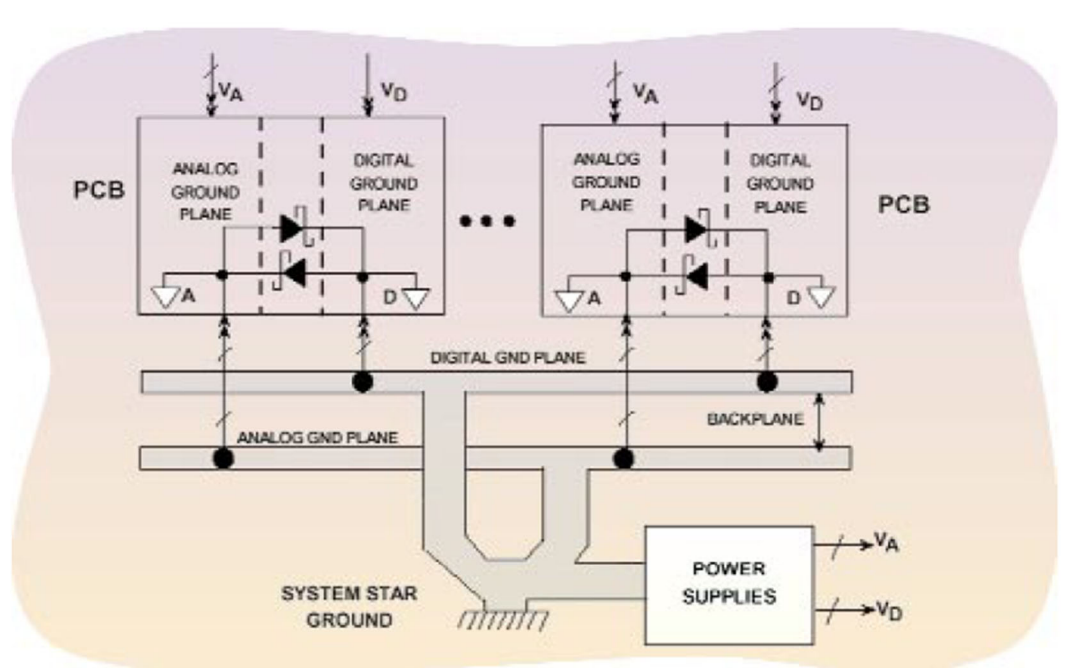
FIG.7

(*Id.*, FIG. 7 (annotated).)

C. Kester

48. Kester is entitled “Proper Grounding is Critical for High-Speed Systems” and was published in Wireless Systems Design in May of 2000. (Ex. 1016, p. 42) Kester discloses that “In other systems, especially high-speed ones with large

amounts of digital circuitry, it is highly desirable to physically separate sensitive analog components from noisy digital components. It is usually desirable to use separate ground planes for the analog and digital circuitry. On PCBs that have analog and digital circuits, there are two separate ground planes.” (*Id.*, p. 40)



1. In order to minimize noise in high-frequency, high-speed circuits, it is essential to separate analog and digital grounds.

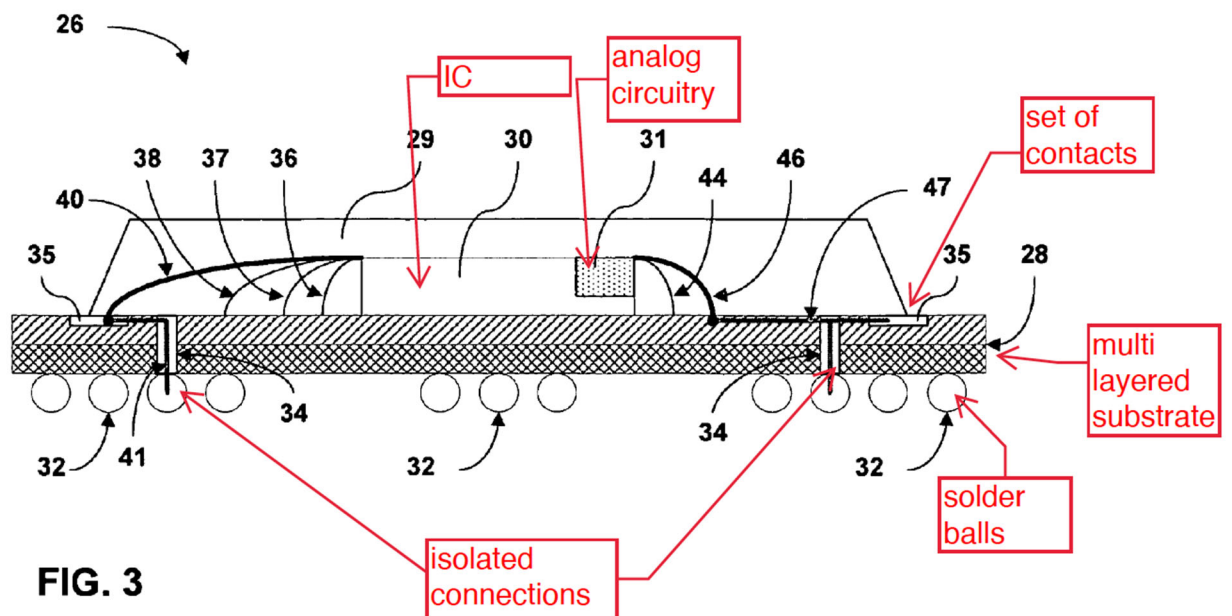
WIRELESS SYSTEMS DESIGN / MAY 2000

(*Id.*, FIG. 1 (emphasis added).)

D. Kramer

49. Kramer is entitled “Reduced Inductance in Ball Grid Array Packages”. (Ex. 1007, Title). Kramer also discloses an example of high-speed signals at speeds of 4.25 Gbit/s [gigabits per second] and above. (*Id.*, 1:35-45) Kramer discloses isolating grounds for separate portions of an integrated circuit. (*Id.*, 5:38-41) As

shown in Figure 3 below, Kramer discloses an integrated circuit 30 attached to BGA package 28. The IC 30 has an analog circuit 31 portion that is connected to a different ground than other portions of the IC 30. Kramer further shows in Figure 3, a first set of electrical connections connect the IC with solder balls on a second surface of the multi-layered substrate and a second set of electrical connections connect the analog circuitry to other solder balls on the second surface. Kramer states that analog circuit 31 “requires isolated power and ground connections to reduce noise on analog circuit 31 from other circuits of IC 30”. (*Id.*)



(*Id.*, FIG. 3, (annotated).)

E. Taggart

50. Taggart is entitled “In-Line Wire Bonding on a Package, and Method of Assembling Same” (Ex. 1009, Title) and discloses aligning bond fingers with die pads in accordance with a particular spacing or pitch. (*Id.*, ¶[0027]) Taggart shows in Figure 9, shown below, a spacing 930 which determines the distance between the bond fingers or pads. The spacing 930 also determines the distance between wire bonds. (*Id.*, ¶¶[0029], [0044], [0048], [0059]) Taggart discloses specific values for the distances ranging from “about 10 um [micrometers] to about 200 um, with specific examples of the pitch being 135 um and 200 um. (*Id.*, ¶[0027])

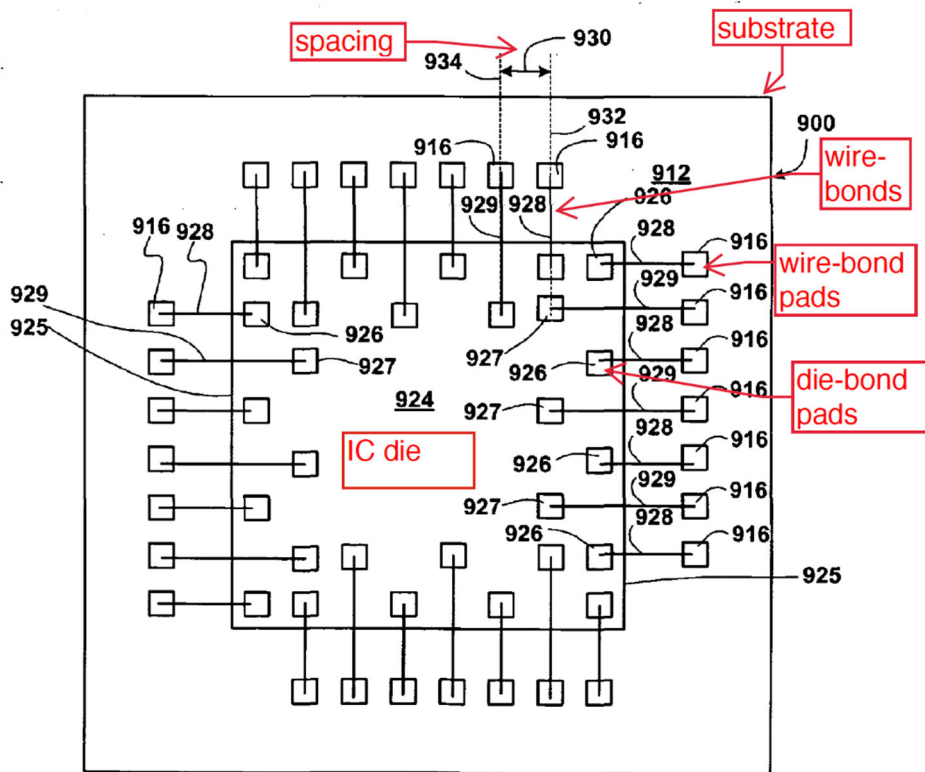
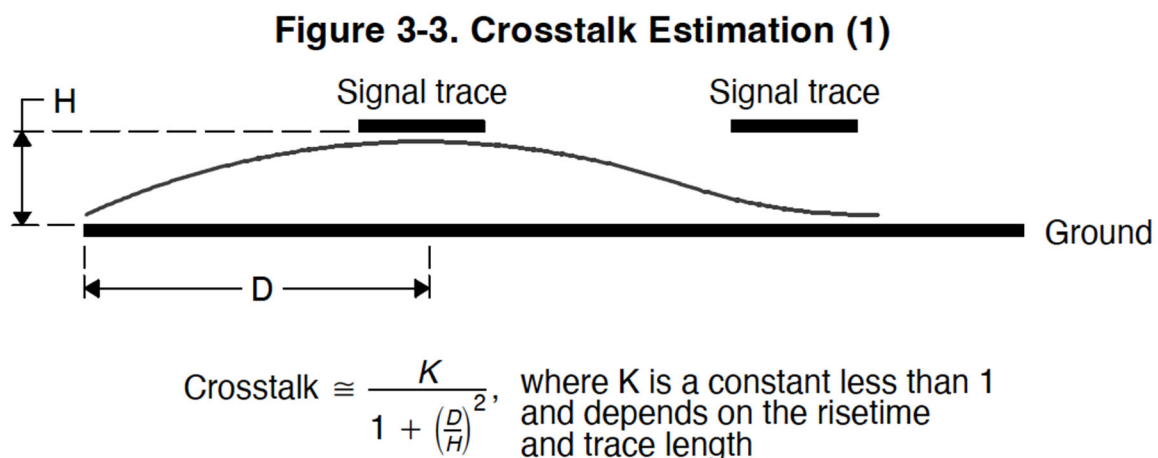


FIG. 9

(*Id.*, FIG. 9, (annotated).)

F. High-Speed DSP Systems Design (hereinafter “High-Speed DSP”)

51. High-Speed DSP discloses “when noise interferes with other circuits it is called crosstalk. Crosstalk can be transmitted through electromagnetic radiation or electrically, such as when unwanted signals propagate on the power and ground planes. In order to minimize crosstalk, designers need to understand two very important concepts, high-speed and low-speed current paths and radiated signal traces.” (Ex. 1014, p. 31) High-Speed DSP discloses in Figure 3-3, shown below, that the spacing or distance, D, between the traces affects the amount of crosstalk. (*Id.*, p. 32)



(*Id.*, FIG. 3-3)

52. Thus, High-Speed DSP discloses that a “higher D yields lower crosstalk.” (*Id.*, p. 35) To further emphasize this point, High-Speed DSP states “Obviously, moving the traces further from each other will reduce the crosstalk.”

(*Id.*, p. 32) High Speed DSP further gives example of high speed at 10 gigahertz (GHz) (*Id.*, p. 60) and low speed below 10 MHz (*Id.*, p. 31).

G. High-Speed Digital Design (hereinafter “Digital Design”)

53. Digital Design discloses design guidelines for various circuits to control crosstalk for high and low speed signals. (Ex. 1010, p. 189). The design guidelines include how far to separate traces to control crosstalk (*Id.*) Digital Design shows in Figure 5.4, shown below, and formula 5.2, that crosstalk for signal traces is based on in part on the distance, D, between signal traces (*Id.*, p. 192). As one example, Digital Design discloses that “more closely spaced traces yield more crosstalk” (*Id.*, p. 215)

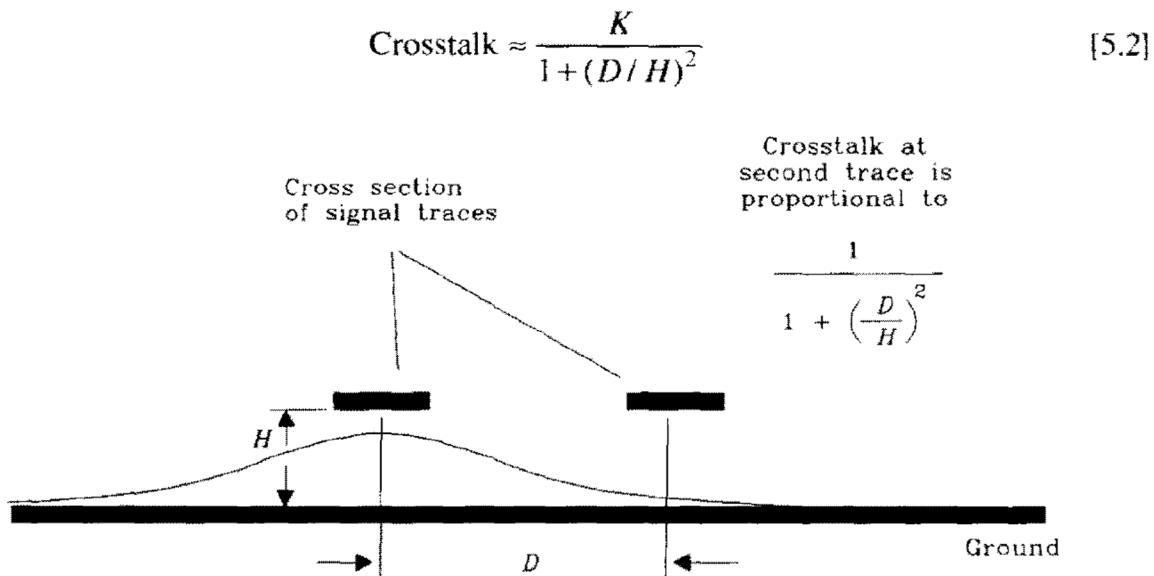


Figure 5.4 Cross section of two traces showing crosstalk.

(*Id.*, Fig. 5.4)

54. Digital Design discloses that typical characteristic impedances include 50 Ohms (*Id.*, p. 202) and 100 Ohms (*Id.*, p. 303). Digital Design shows numerous examples of 50 Ohm impedances for traces. One such example is shown below in Figure 5.24

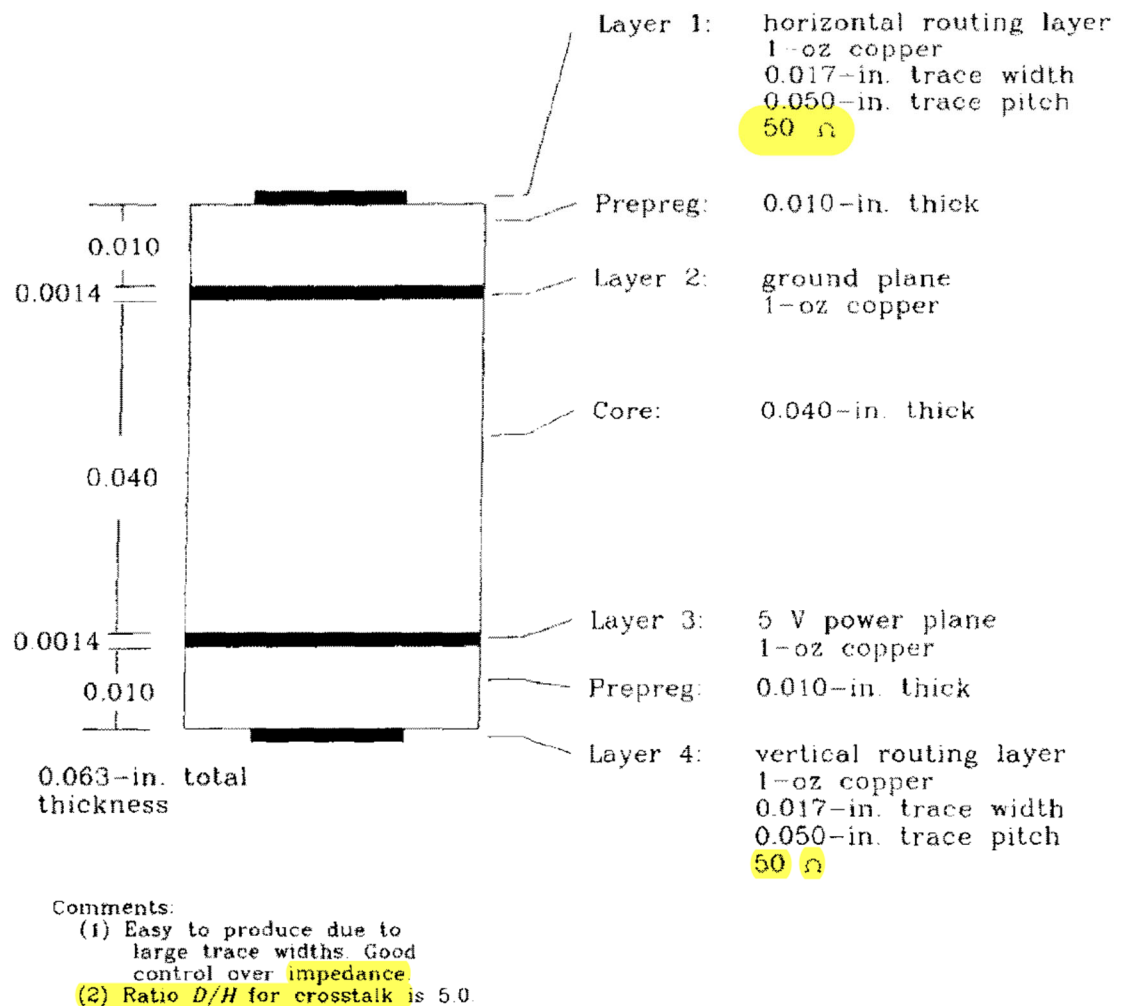


Figure 5.24 Four-layer stack.

(*Id.*, FIG 5.24 [emphasis added])

H. Choi

55. Choi discloses plastic ball grid array (PBGA) packages directly attached to a board using solder balls. (Ex. 1011, p. 304) Choi shows in Figure 6, shown below, a multi-layered PCB that has a low-speed interconnects on layer 1 and high-speed interconnects on layer 6. (*Id.*) Choi discloses that the low-speed signal transmission lines have characteristic impedances designed for 50 Ω (Ohms) and the high-speed signal transmission lines are designed to provide 100 Ohm differential impedance.

Layer 1	0.5 Oz Copper	Top (low-speed transmission lines)
4.5 mils		
Layer 2	1 Oz Copper	Gnd
4.8 mils		
Layer 3	1 Oz Copper	Vdd (5 V and 1.2 V islands)
92.2 mils		
Layer 4	1 Oz Copper	Vdd (3.3 V island and 1.2 V split plane)
4.8 mils		
Layer 5	1 Oz Copper	Gnd
4.5 mils		
Layer 6	0.5 Oz Copper	Bottom (high-speed transmission lines)

Fig. 6. The cross section of the PCB.

(*Id.*, FIG. 6)

56. Choi further gives examples of high speed as 3.2 gigabits per second (Gbps) (*Id.*, p. 310) and simulations from 10 megahertz (MHz) to 6 gigahertz (GHz). (*Id.*, p. 305)

I. Sutardja

57. Sutardja is entitled “Packaging For High Speed Integrated Circuits” (Ex. 1012, Title) and discloses bond wires connected to pads on integrated circuit die and irregularly spaced leads. (*Id.*, ¶[0137]) Sutardja further discloses in Figure 10A, shown below, that spacing between the low speed leads is d1 (annotated in green), and spacing between the pairs of high speed leads is d4 (annotated in yellow), and further that the spacing “may be irregular **to increase or decrease coupling.**” (*Id.*, ¶[0139]) From Figure 10A, it is apparent that Sutardja discloses that a distance between low speed leads is less than a distance between high speed lead pairs.

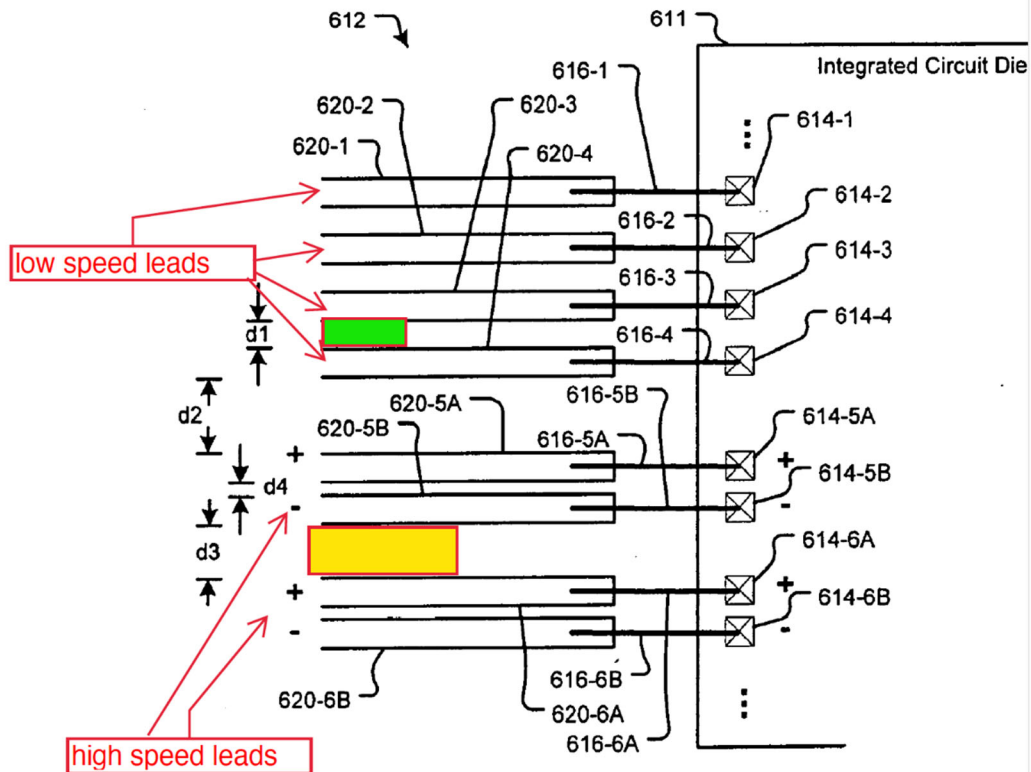


FIG. 10A

(*Id.*, FIG. 10A, (annotated).)

J. Conn

58. Conn is entitled “Shielded Platform for Die-Bonding an Analog Die to an FPGA” (Ex. 1013, Title) and discloses a stacked die arrangement for different IC die. (*Id.*, Abstract) In an example, the FPGA can be operable at frequencies much higher than a die situated above (e.g., audio amp die 44, analog power regulator die 73). (*Id.*, 6:40-50)

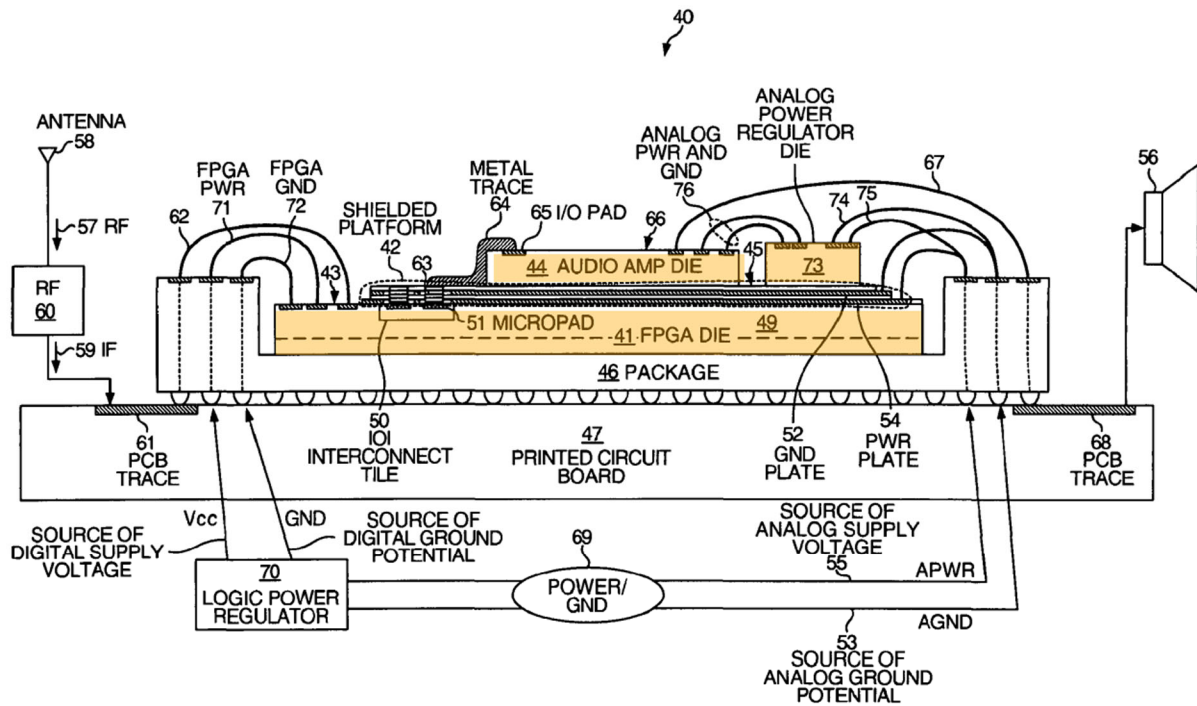


FIG. 2

(*Id.*, Fig. 2 annotated)

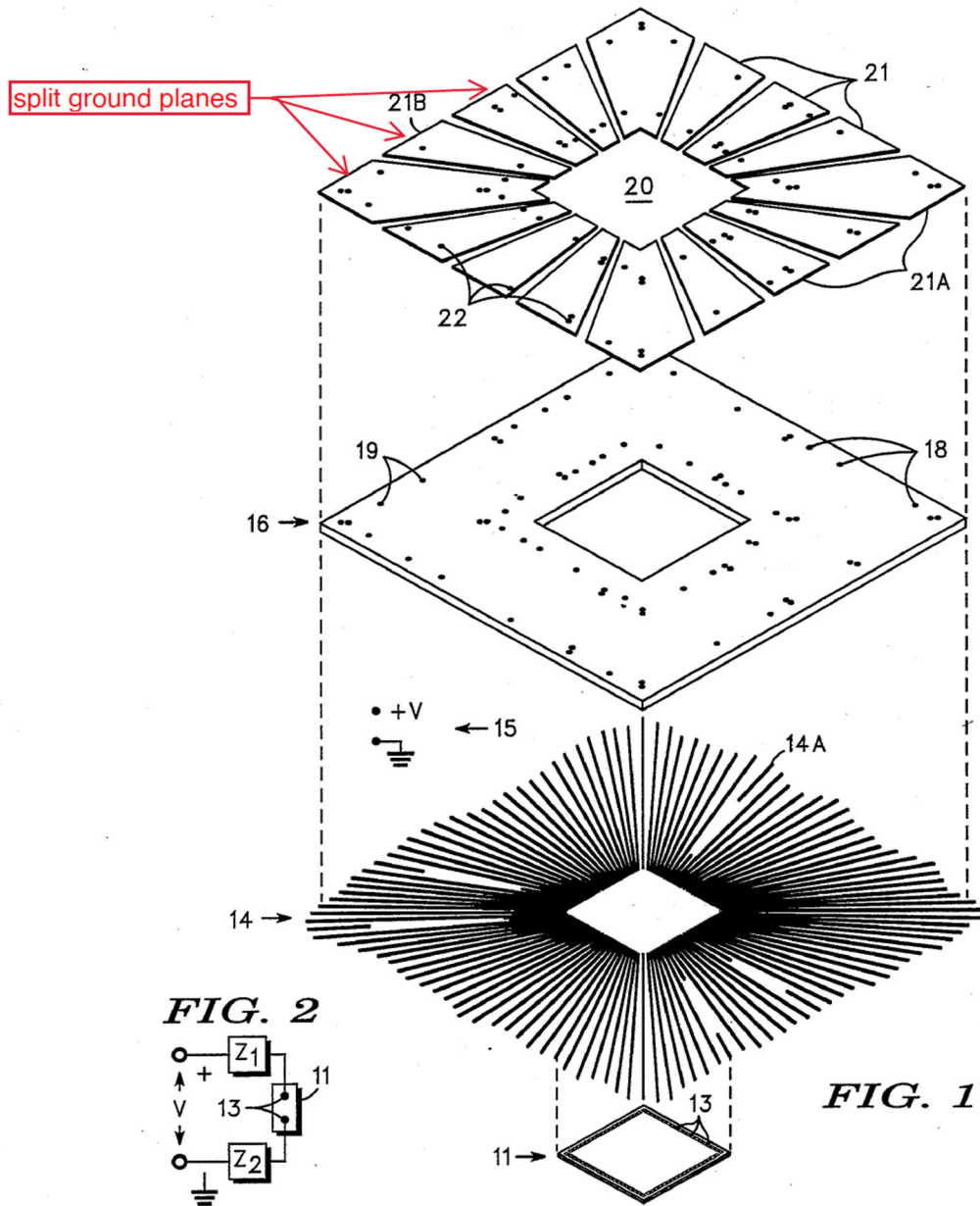
K. Schroeder

59. Schroeder discloses split ground planes to reduce cross talk between conductors of an integrated circuit (Ex. 1008, 4:25-40).

U.S. Patent

Jun. 12, 1990

4,933,741



(*Id.*, FIG. 1 annotated)

IX. EXPLANATION OF MY OPINIONS

60. The following sections provides my opinion that claims 1-14 of the '091 Patent are invalid as discloses and/or rendered obvious by the prior art. Below, I address each claim element on an element-by-element basis for each reference and/or combination of references, as well as the motivation to combine references and reasonable expectation of success in doing so. Given certain similar claim elements and the use of the same references in multiple combinations, many of the explanations herein would apply to multiple claim elements and reasons that a person of ordinary skill in the art would be motivated to combine these references and have a reasonable expectation of success in doing so. As such, my explanation regarding a certain claim element and certain reference or combination may also apply to other claim elements or the use of that same reference in another combination for the same or a similar claim element. This applies even when there is no explicit incorporation by reference. Furthermore, while I have cited portions of each reference to provide my opinions below, I may rely on additional portions of a reference to further support those opinions, or portions of other references, including portions identified above where I discussed the prior art and the technology background.

X. THE PRIOR ART DISCLOSES ALL OF THE FEATURES OF THE CHALLENGED CLAIMS.

A. Okabe discloses all the features of Claim 1.

61. In my opinion, Okabe discloses all of the features of claim 1 of the '091 Patent.

1. Claim 1

a) “A semiconductor integrated circuit (IC) package which comprises:”

62. I understand that “a semiconductor integrated circuit (IC) package which comprises” is the preamble to claim 1 of the '091 Patent.

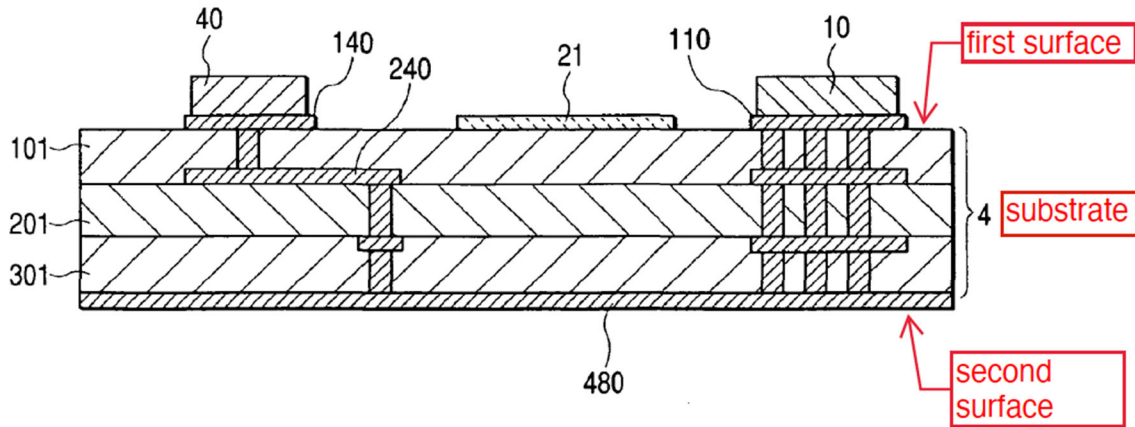
63. I have been asked to assume that the preamble is a claim limitation. Under that assumption, in my opinion, Okabe discloses this claim feature.

64. Okabe discloses various “circuits and chips are mounted onto a substrate of the module 1” (Ex. 1005, 13:66-67) Okabe further discloses prior art multi-chip modules that includes integrated circuit chips bonded to a single interconnect substrate. (*Id.*, 2:24-36) A person of ordinary skill in the art would understand these to be an IC package.

b) “a substrate having a first surface and a second surface wherein;”

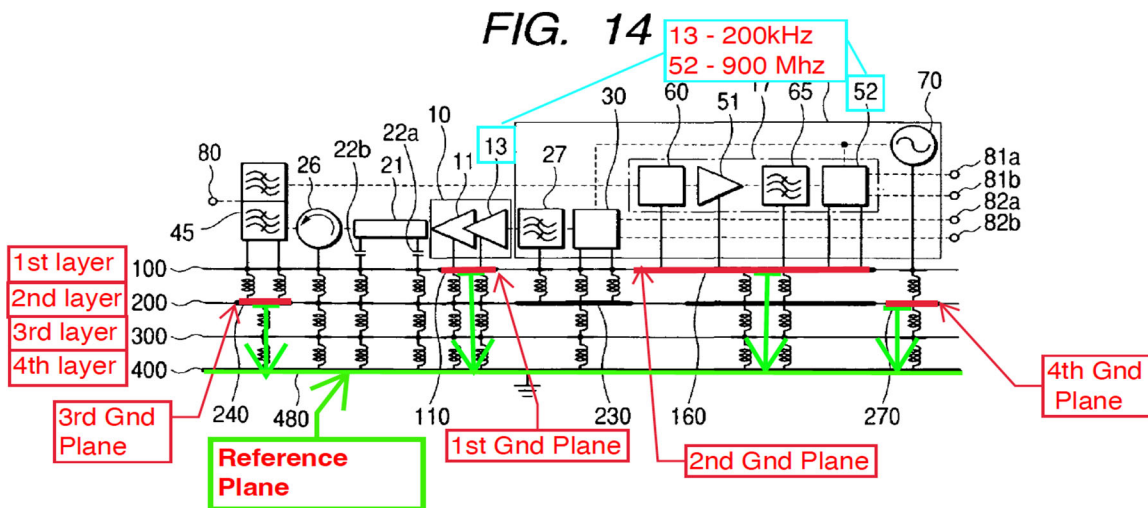
65. In my opinion, *Okabe* discloses this claim feature. As shown in the annotated Figure 10 below, Okabe discloses a substrate 4 having a first surface and a second surface.

FIG. 10



(*Id.*, FIG. 10, (annotated).)

c) “a first layer of the substrate includes,”



(*Id.*, FIG. 14, (annotated).)

66. In my opinion, Okabe discloses this claim feature. *Okabe* discloses in Figure 14, shown above, a first layer 100 of the substrate 4. (*Id.*, 8:18-20, 9:20-22.)

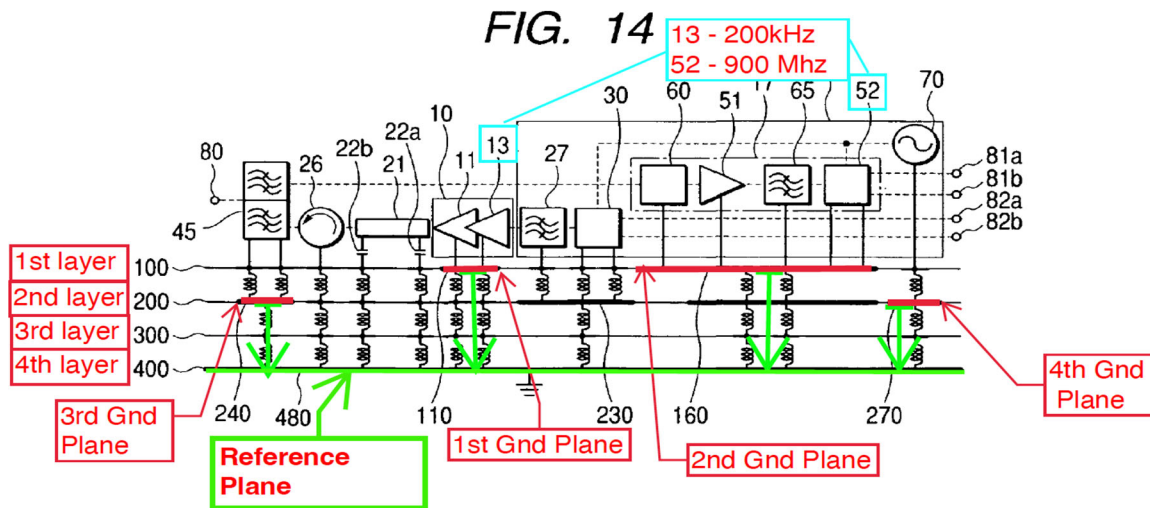
d) “a first ground plane enabling electrical connection with low speed electronic circuitry, and”

67. In my opinion, Okabe discloses this claim feature. As shown in Figure 14 above, Okabe discloses a first ground plane 110 on the first layer 100 of the substrate 4 (*Id.* 8:8-28.) In an example, Okabe teaches that circuit 13 operates in a frequency band of 200 kilohertz (kHz), while circuit 52 operates in a frequency band of 900 megahertz (MHz). (*Id.* 7:36-41). A person of ordinary skill in the art would have understood that 900 MHz is a higher frequency than 200 kHz, and thus circuit 13 would be understood as “low speed electronic circuitry”. Okabe also discloses circuit 13 is a part of power amplifier (PA) circuit 10, and that the PA ground plane 110 (e.g., a first ground plane) is connected to the ground terminals of the PA 10. (*Id.* 7:52-55; 8:25-27). A person of ordinary skill in the art would have understood that connection of the PA circuit 10 to the first ground plane would be an “electrical connection”.

e) “a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection with high speed electronic circuitry;”

68. In my opinion, Okabe discloses this claim feature. As shown in Figure 14, shown below, Okabe discloses a second ground plane 160 on the first layer 100 that is separated from and electrically isolated from the first ground plane 110 on the first layer 100. (*Id.*, 14:13-25; 14:64 – 15:3) Okabe teaches in the example above

that circuit 13 operates in a frequency band of 200 kilohertz (kHz), while circuit 52 operates in a frequency band of 900 megahertz (MHz). (*Id.*, 7:36-41).



(*Id.*, FIG. 14 (annotated).)

69. A person of ordinary skill in the art would have understood that 900 MHz is a higher frequency than 200 kHz, and thus circuit 52 would be understood as “high speed electronic circuitry”. Okabe teaches the “receiver are connected to the receive circuits ground plane 160 by bonding wires or solder bumping”. (*Id.*, 14:65-67). A person of ordinary skill in the art would have understood that bonding wires or solder bumping would be an electrical connection from the second ground plane 160 to the “high speed electronic circuitry” of circuit 52.

f) “a second layer of the substrate includes,”

70. In my opinion, Okabe discloses this claim feature. As shown in Figure 14, shown above, Okabe discloses a second layer 200 of the substrate 4 (*Id.*, 8:18-21, 9:28-31)

g) “a third ground plane configured for electrical connection with low speed electronic circuitry, and”

71. In my opinion, Okabe discloses this claim feature. As shown in Figure 14, shown above, Okabe discloses a third ground plane 240 on the second layer 200 of the substrate 4. (*Id.*, 8:27-35) Ground plane 240 (e.g., a third ground plane as ground plane 110 is a first ground plane and ground plane 160 is a second ground plane) is electrically connected to duplexer 45. (*Id.*, 14:18-19) A person of ordinary skill in the art would understand that duplexer 45 would be capable of operating at a lower frequency than voltage controller oscillator (VCO) 70, thus the third ground plane 240 would be “configured for” electrical connection with “low speed electronic circuitry”.

h) “a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the fourth ground plane configured for electrical connection with high speed electronic circuitry, and”

72. In my opinion, Okabe discloses this claim feature. Okabe shows in Figure 14, shown above, a fourth ground plane 270 separated and electrically

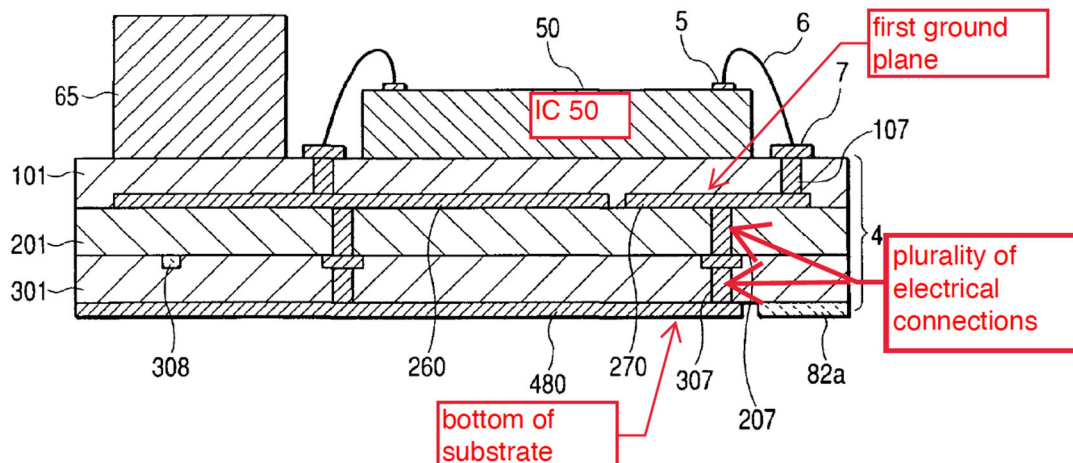
isolated from the third ground plane 240 on the same layer 200 of the substrate 4 (*Id.*, 14:13-33).

73. As discussed above, a person of ordinary skill in the art would understand that voltage controller oscillator (VCO) 70 would be capable of operating at a higher frequency than duplexer 45, thus the fourth ground plane 270 would be “configured for” electrical connection with “high speed electronic circuitry”.

i) **“a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate”**

74. In my opinion, *Okabe* discloses this claim feature. *Okabe* in figure 9, shown below, discloses a first ground plane 270 electrically connected to a bottom of a substrate 4 by way of vias 207 and 307. (*Id.*, 8:38-44)

FIG. 9

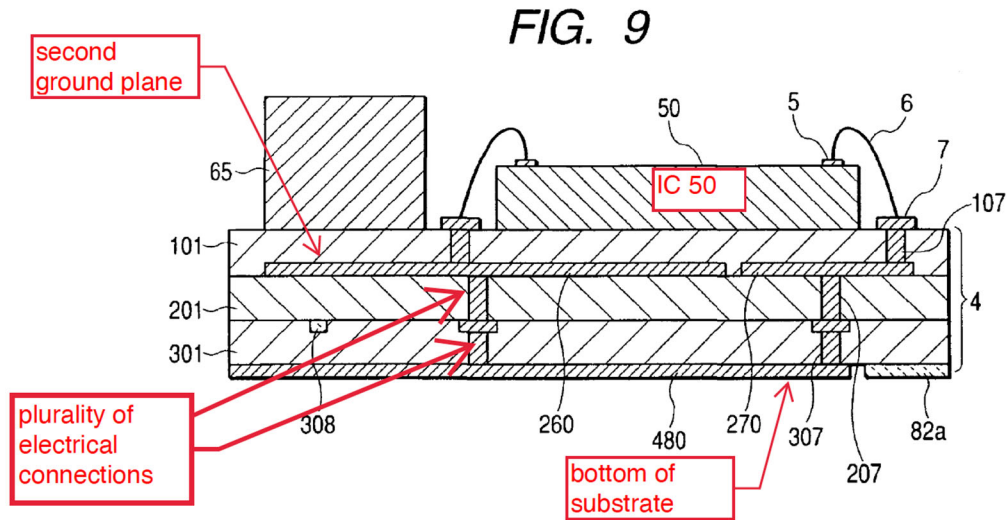


(*Id.*, FIG. 9 (annotated).)

75. *Okabe* also discloses that solder bumping may be used in a flip chip connection process. (*Id.*, 9:32-38) A person of ordinary skill in the art would have understood that “solder bumping” when used in the context of a flip chip connection process is analogous to solder balls, which were known to be placed on the bottom of a substrate in a flip chip process. Thus, a person of ordinary skill in the art would have understood this to mean the solder balls could be electrically connected to ground plane 270 by way of vias 207, and 307 (e.g., a plurality of electrical connections).

j) “a plurality of electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate”

76. In my opinion, *Okabe* discloses this claim feature. As shown below in Figure 9, *Okabe* shows ground plane 260 (e.g., second ground plane) connected to bottom of substrate 4 by way of vias (plurality of additional electrical connections).

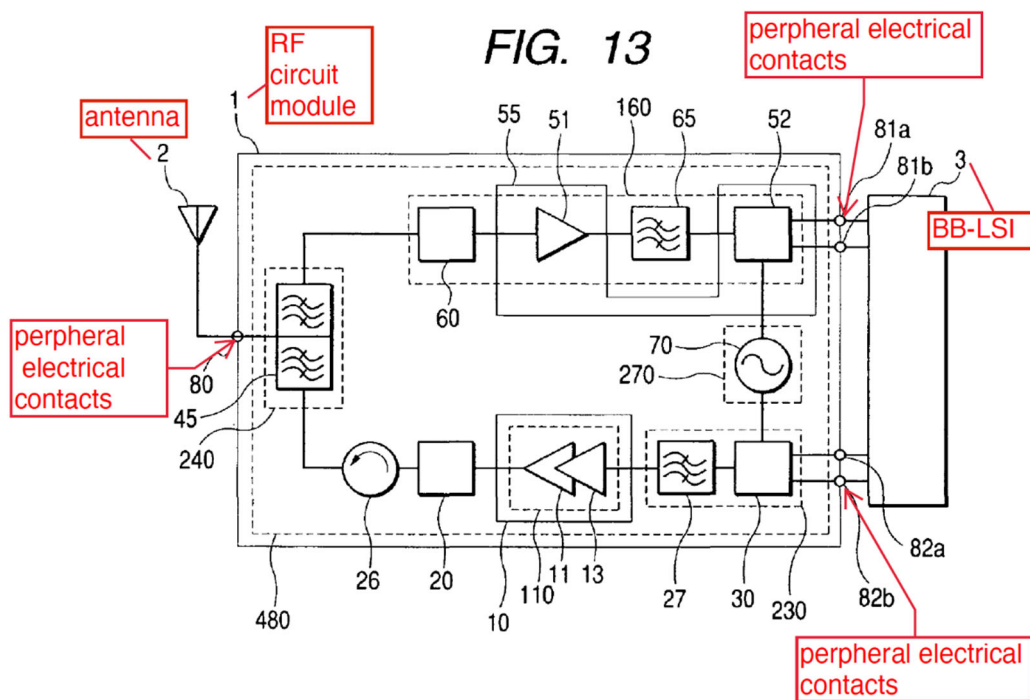


(*Id.*, FIG. 9 (annotated).)

77. As discussed *supra* in Section IX.A.1(i), Okabe discloses solder balls are well known in IC packaging. As such, a person of ordinary skill in the art would have understood the second ground plane could also be electrically connected with the solder balls in a similar fashion to the first ground plane.

k) “peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package; and”

78. In my opinion, Okabe discloses this claim feature. Okabe teaches in Figure 13, shown below, an antenna 2 and an BB-LSI 3 external to RF circuit module 1. A peripheral connection 80 connects switch 40 with the external antenna 2 and peripheral connections 81a-82b connect the RF module 1 with the external BB-LSI 3. (*Id.*, 7:23-35; 13:40-45).



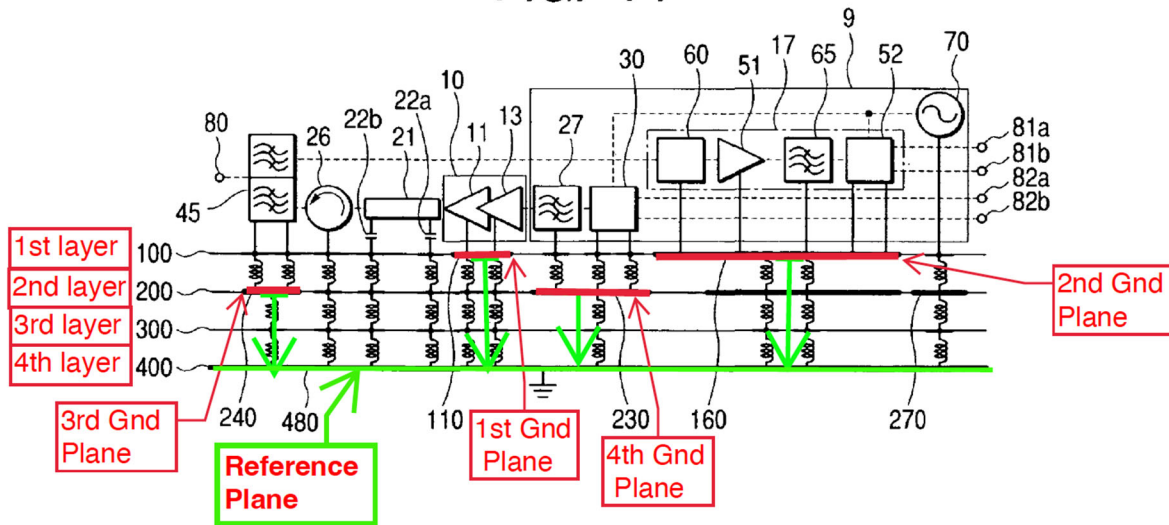
(*Id.*, FIG. 13)

l) “At least one reference plane associated with each layer of the substrate and the ground planes included thereon”

79. In my opinion, Okabe discloses this claim feature. Okabe discloses in Figure 14, shown below, a common ground plane 480 associated with a first layer

100, a second layer 200, a third layer 300, and a fourth layer 400 (e.g., each layer of substrate 4) and each ground plane included on each of the four layers 100-400 (*Id.*, 14:13-25) Okabe further discloses that “by providing the module with the common ground plane 480 to which all ground planes are connected, **reference potential** for all RF circuits can be fixed, not dependent on the ground land on the motherboard.” (*Id.*, 11:14-18 (emphasis added).) As such, a person of ordinary skill in the art would have understood the common ground plane would be “a reference plane”.

FIG. 14



(*Id.*, FIG. 14 (annotated).)

B. Hashemi in view of Okabe discloses all the features of Claim 1.

1. Claim 1

a) “A semiconductor integrated circuit (IC) package which comprises:”

80. I understand that “a semiconductor integrated circuit (IC) package which comprises” is the preamble to claim 1 of the '091 Patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, in my opinion, Hashemi discloses this feature.

81. Hashemi discloses multiple chip modules (MCMs) as integrated circuit packages that may contain a number of bare and/or packaged integrated circuit (IC) chips and a number of discrete components coupled to an interconnecting substrate. (Ex. 1006, 1:14-18; 12:9-12)

b) “a substrate having a first surface and a second surface wherein;”

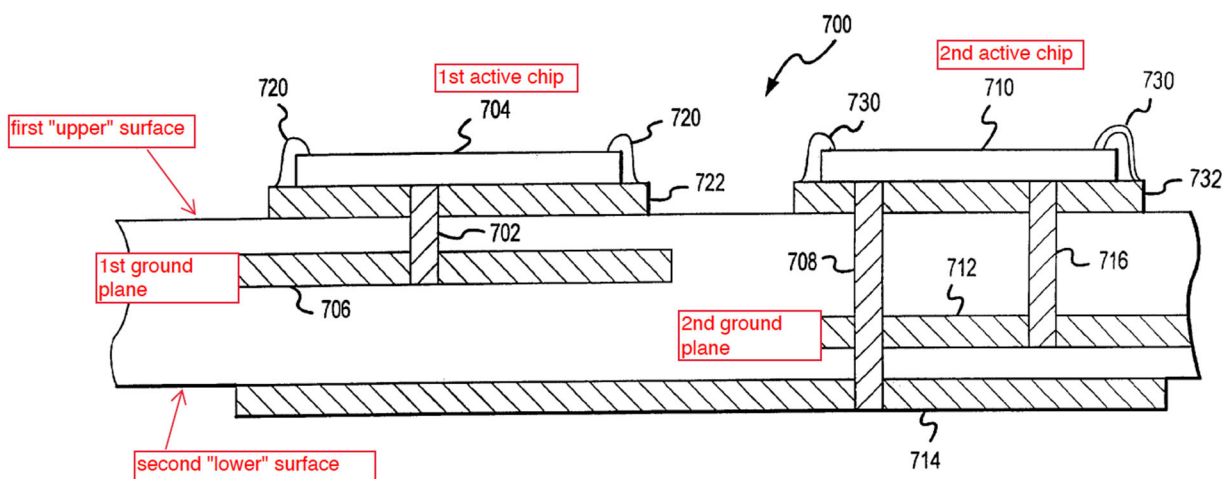


FIG.7

(*Id.*, FIG. 7 (annotated).)

82. In my opinion, Hashemi discloses this claim feature. Hashemi shows in Figure 7, shown above, a substrate with an upper surface and a lower surface. (*Id.*, Claim 35)

c) “a first layer of the substrate includes,”

83. In my opinion, Hashemi discloses this claim feature. Hashemi discloses the substrate may include any number of metal layers with alternating dielectric layers. (*Id.*, 4:21-34)

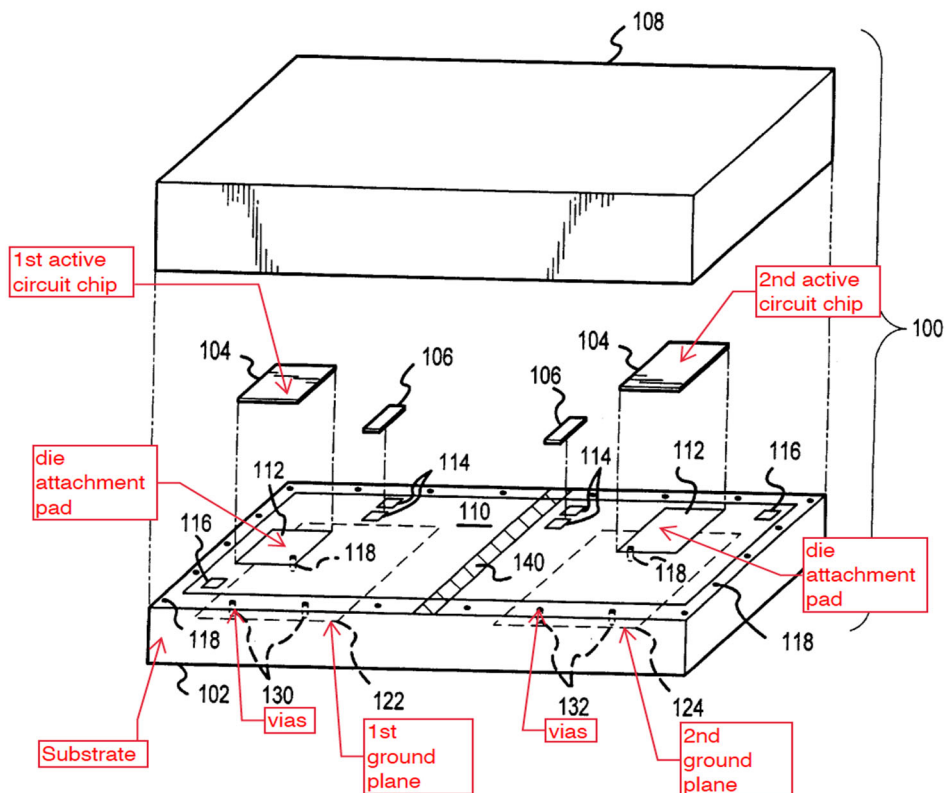


FIG. 1

(*Id.*, FIG. 1 (annotated).)

d) “a first ground plane enabling electrical connection with low speed electronic circuitry, and”

84. In my opinion, Hashemi discloses this claim feature. Hashemi discloses in Figure 1, shown above, a first ground plane 122 connected by way of vias 130 to a first active chip 104. Hashemi further discloses a first active circuit chip 104 operates at different frequencies than a second active circuit chip 104 (*Id.*, Claim 3). As such, a person of ordinary skill in the art would have understood that the first active circuit chip 104 could operate at a lower frequencies than a second active circuit chip 104 and thus could operate as “low speed electronic circuitry”.

e) “a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection with high speed electronic circuitry;”

85. In my opinion, Hashemi discloses this claim feature. As shown above in Figure 1, Hashemi discloses a second ground plane 124 connected with a second active circuit chip 104 by way of vias 132. Hashemi discloses that the second ground plane is physical distinct and electrically isolated from the first ground plane. (*Id.*, 8:4-9; Claims 15-16)

86. Hashemi further discloses a first active circuit chip 104 operates at different frequencies than a second active circuit chip 104 (*Id.*, Claim 3). As such, a person of ordinary skill in the art would have understood that the second active

circuit chip 104 could operate at a higher frequencies than a first active circuit chip 104 and thus could operate as “high speed electronic circuitry”.

f) “a second layer of the substrate includes,”

87. In my opinion, Hashemi discloses this claim feature. Hashemi discloses the substrate includes any number of layers and preferred embodiment includes 2 to four metal layers (*Id.*, 2:21-34)

g) “a third ground plane configured for electrical connection with low speed electronic circuitry, and”

88. In my opinion, Hashemi discloses this claim feature. As discussed above in Section X.B.1(d), Hashemi discloses vias for electrically connecting an active circuit chip 104 with an underlying separate ground plane. Hashemi discloses “the MCM may employ split RF ground planes, located at indeterminate metal **layers** or at the lower exposed metal layer to promote effective RF grounding and isolation between different RF chips”. (*Id.*, 11:11-14) A person of ordinary skill in the art would have understood that the split ground planes were not limited to a single layer, and as such, would include a third and fourth ground plane.

h) “a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the fourth ground plane configured for electrical connection with high speed electronic circuitry, and”

89. In my opinion, Hashemi discloses this claim feature. As discussed above in Section X.B.1(g), Hashemi teaches the split ground planes are not limited

one layer (*Id.*, 11:11-14) Further, as discussed above with reference to Section X.B.1(e), Hashemi teaches the split ground planes are electrically isolated and physically distinct. It would have been very clear to a person of ordinary skill in the art, that split ground planes feature could be implemented at a different layer, and thus would include a third and fourth ground plane on a second layer of a multi-layered substrate. A person of ordinary skill in the art would take note that '091 Patent does not disclose any difference between a third and fourth ground plane on a second layer versus a first and second ground plane on a first layer.

i) “a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate”

90. In my opinion, Hashemi discloses this claim feature. Hashemi discloses that MCMs may employ a ball grid array and that solder balls may be used as a termination device at the bottom of the MCM. (*Id.*, 12:21-25) Hashemi further discloses in the description of Figure 7, shown below, an internal ground plane may be “connected to a suitable ground termination”. (*Id.*, 6:61-63) A person of ordinary skill in the art would have understood that being “connected to” solder balls would include a plurality of electrical connections and that the bottom of the MCM would be the second surface of the substrate.

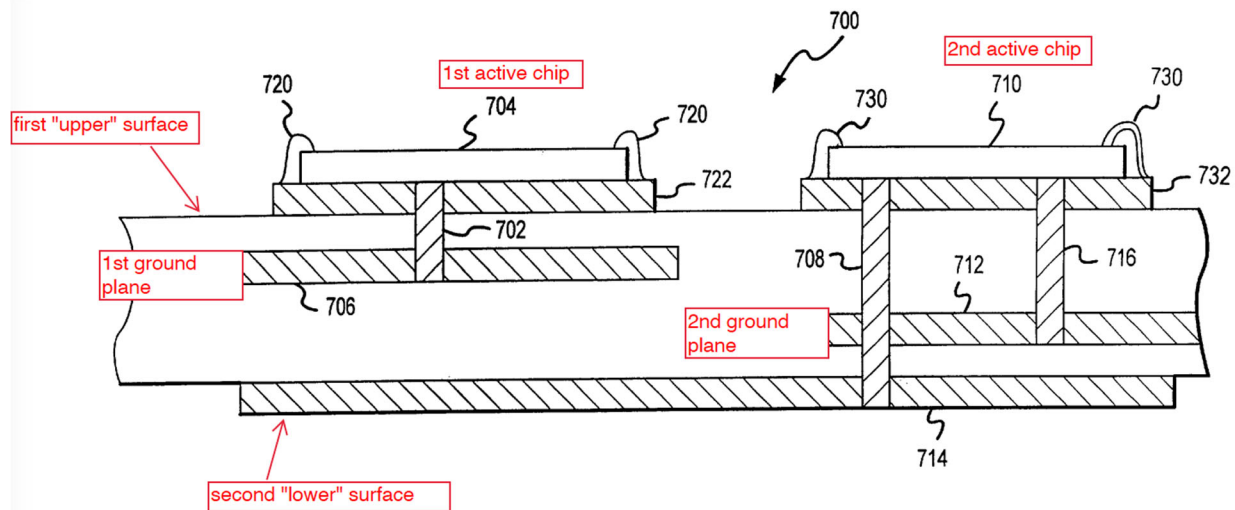


FIG. 7

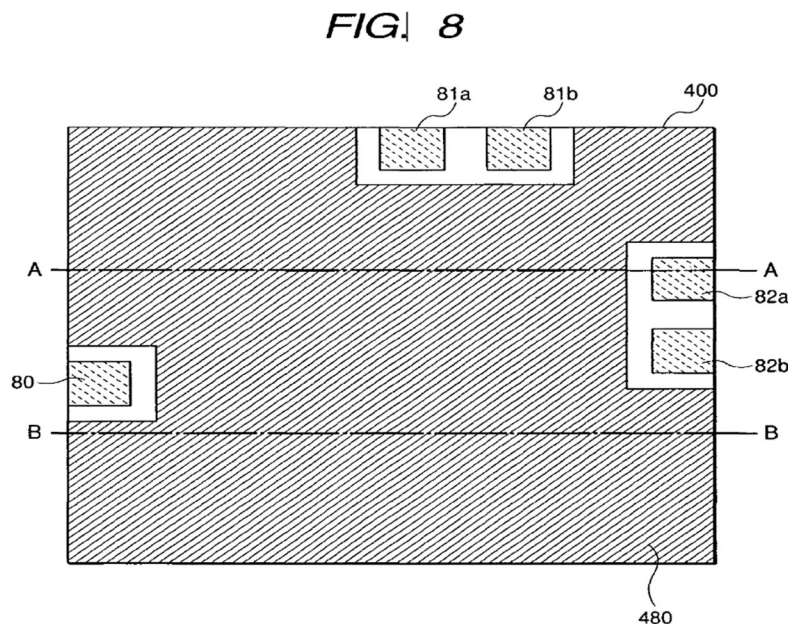
(*Id.*, FIG. 7 (annotated).)

j) “a plurality of electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate”

91. In my opinion, Hashemi discloses this claim feature. Hashemi discloses that MCMs may employ a ball grid array and that solder balls may be used as a termination device at the bottom of the MCM. (*Id.*, 12:21-25) Hashemi further discloses that an internal ground plane may be “connected to a suitable ground termination” (*Id.*, 6:61-63) and that any of the split ground planes may be electrically connected using vias to die attach pads and/or to a ground provided by a motherboard assembly. (*Id.* 7:13-27)

k) “peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package; and”

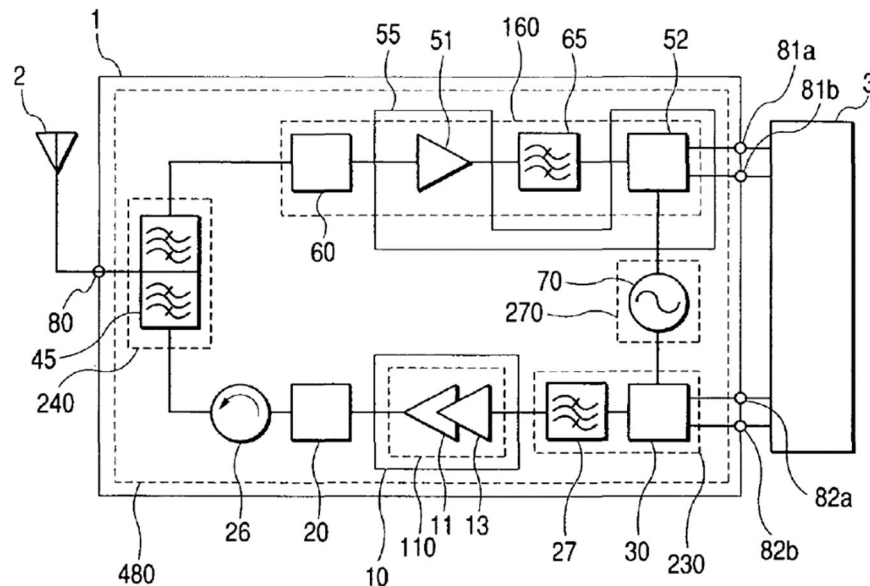
92. In my opinion, Hashemi discloses this claim feature. Hashemi discloses solder balls as a termination device (Ex. 1006, 12:21-25), which a person of ordinary skill in the art would understand as peripheral electrical contacts used to connect with circuitry external to the package. (Ex. 1001, 1:15-29) However, I’ve been asked to assume that Hashemi does not teach “peripheral electrical contacts” for connections with the term “electronic circuitry external to the package”.



(Ex. 1005, FIG. 8)

93. Under this assumption, Okabe discloses peripheral electrical contacts (terminals 80, 81a, 81b, 82a, and 82b) on the peripheral of the substrate for connection with electronic circuitry external to an IC package, shown above in Figure 8. The terminal 80 connects the module to external circuitry (an external antenna) and terminals 81, 81b, 82a and 82b connect the module to an external BB-LSI (base band large scale integrated circuit) as shown in Figure 13 below. (Ex. 1005, 7:4-40)

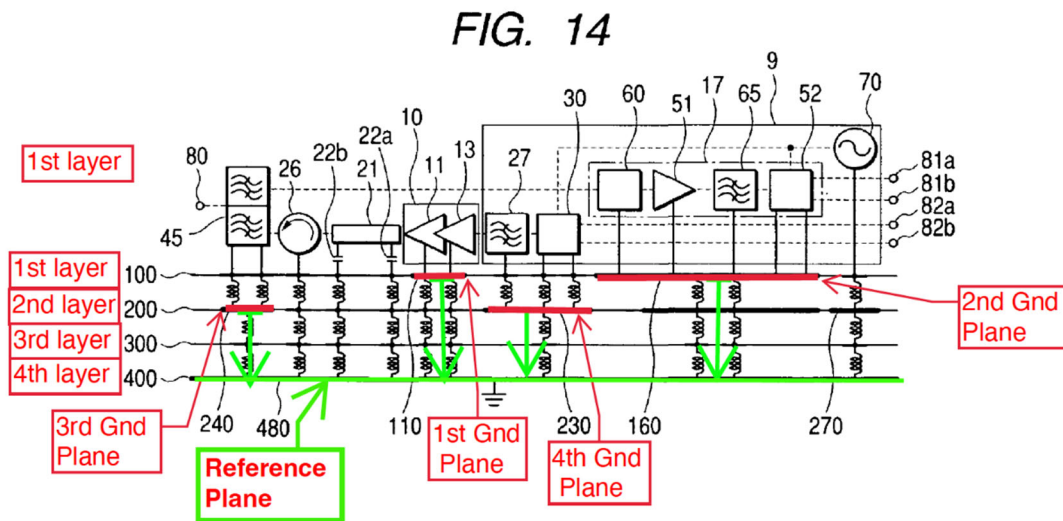
FIG. 13



(*Id.*, FIG. 13)

l) “At least one reference plane associated with each layer of the substrate and the ground planes included thereon”

94. In my opinion, the combination of *Hashemi-Okabe* discloses this claim feature. *Okabe* discloses a common ground plane 480 associated with each layer 100-400 and the ground planes 110, 160, 240, 230, and 270 included thereon.



(*Id.*, FIG. 14 (annotated).)

95. A person of ordinary skill in the art implementing the MCM package of *Hashemi* would have good reason to look to *Okabe* to provide a common reference plane to remove variance of the potential of the separate grounds of *Hashemi*, as they are both in the same field of integrated circuit packages. (Ex. 1005, 2:57-65) Moreover, such a person implementing the IC package of *Hashemi* would be motivated to include the reference plane of *Okabe* to provide stable performance by fixing reference potentials for the integrated circuit which are not dependent on ground lands of a motherboard as disclosed by *Okabe*. (Ex. 1005, 11:14-19)

C. Okabe in combination with Applicant's Admitted Prior Art (AAPA) discloses or suggests all the features of claims 1 and 12.

96. In my opinion, Okabe in combination with AAPA discloses or suggests all of the features of claims 1 and 12 of the '091 Patent.

1. Claim 1

a) "A semiconductor integrated circuit (IC) package which comprises:"

97. I understand that "a semiconductor integrated circuit (IC) package which comprises" is the preamble to claim 1 of the '091 Patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, in my opinion, *Okabe* and the *Applicant's Admitted Prior Art (AAPA)*, both disclose this feature.

98. Okabe discloses various "circuits and chips are mounted onto a substrate of the module 1" (Ex. 1005, 13:66-67.) Okabe further discloses prior art multi-chip modules that include integrated circuit chips bonded to a single interconnect substrate. (*Id.*, 2:24-36)

99. The '091 Patent discloses Element 1a as prior art. (Ex. 1001, 1:15-17 ["The semiconductor industry makes wide use of packaging substrates to hold and electrically interconnect integrated circuit (IC) die mounted within the packaging substrate."])

100. The '091 Patent further discloses in figure 1, shown below, a prior art standard plastic ball grid array (PBGA) package 100 that includes integrated circuit 101. (*Id.*, 1:45-47)

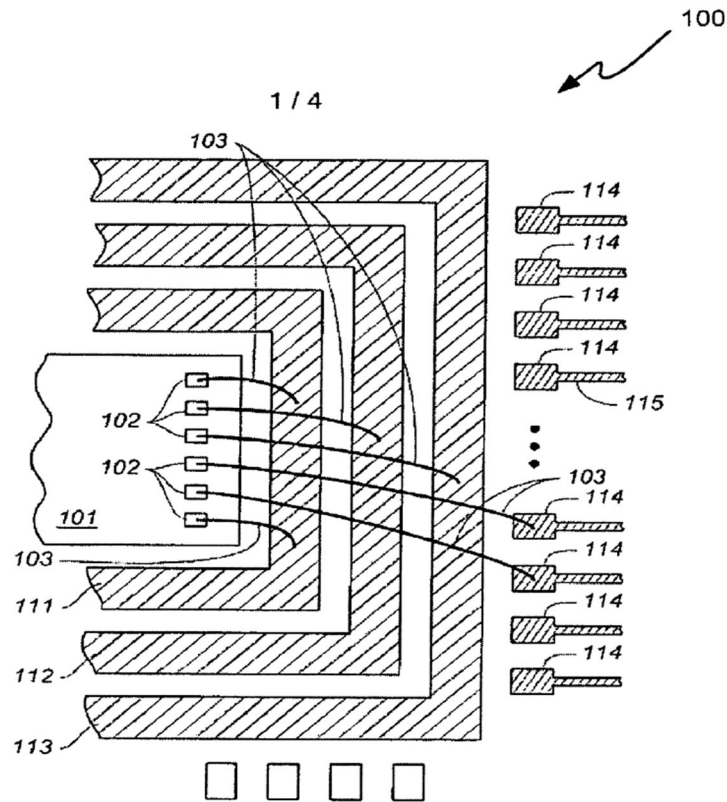


FIG. 1 (PRIOR ART)

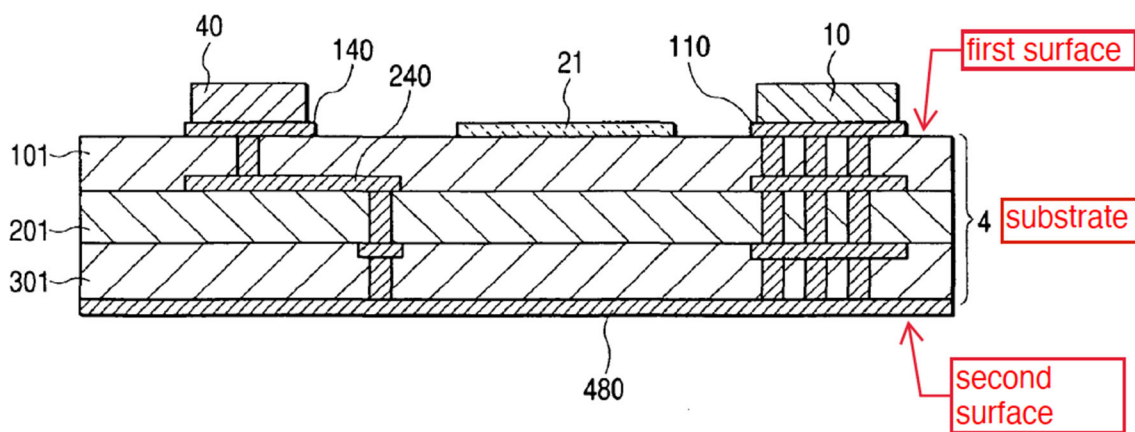
(*Id.*, FIG. 1)

b) “a substrate having a first surface and a second surface wherein;”

101. In my opinion, *Okabe* discloses this claim feature. As shown in the annotated Figure 10 below, *Okabe* discloses a substrate 4 having a first surface and a second surface. Further, *Okabe* discusses a “formation side (top face) of the module substrate”. A person of ordinary skill in the art would understand that a side or a face

of a substrate would be equivalent to a surface, and would also understand that the substrate having a top face or side would indicate the substrate also has a bottom or second side.

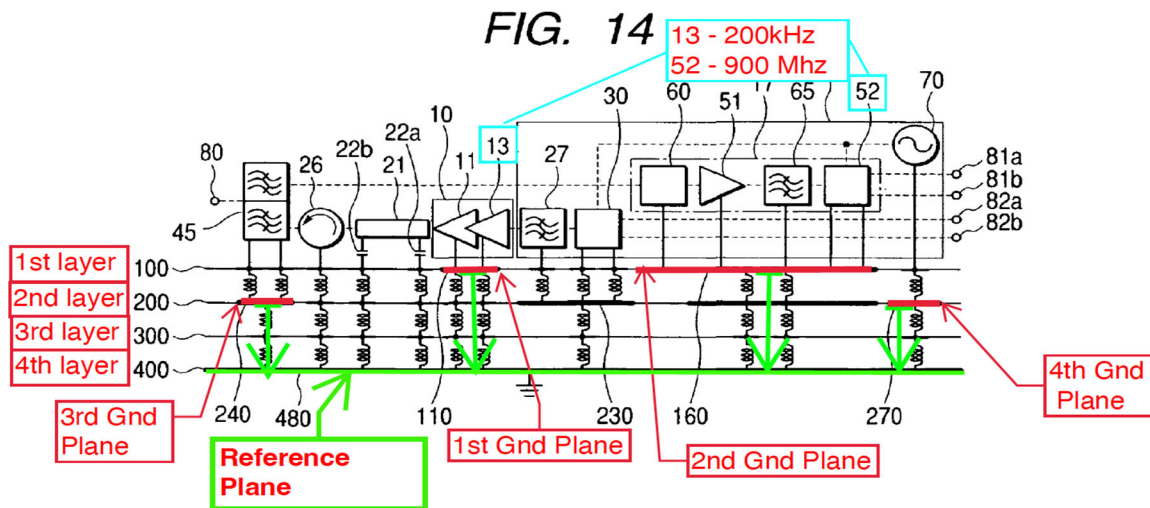
FIG. 10



(*Id.*, FIG. 10, annotated.)

102. The '091 Patent also discloses it was widely known to use packaging substrates. (Ex. 1001, 1:16-20) A person of ordinary skill in the art would understand a substrate would generally include a first and second surface.

c) “a first layer of the substrate includes,”



(*Id.*, FIG. 14, annotated)

103. In my opinion, Okabe and AAPA both disclose this claim feature. *Okabe* discloses in Figure 14, shown above, a first layer 100 of the substrate 4. (*Id.* 8:18-20, 9:20-22.) The '091 Patent discloses as AAPA an IC package includes layers. (Ex. 1004, 1:30-32; 5:1-2.)

d) “a first ground plane enabling electrical connection with low speed electronic circuitry, and”

104. In my opinion, Okabe and AAPA both disclose this claim feature. As shown in Figure 14 above, Okabe discloses a first ground plane 110 on the first layer 100 of the substrate 4 (Ex. 1005, 8:8-28.) In an example, Okabe teaches that circuit 13 operates in a frequency band of 200 kilohertz (kHz), while circuit 52 operates in a frequency band of 900 megahertz (MHz). (*Id.*, 7:36-41).

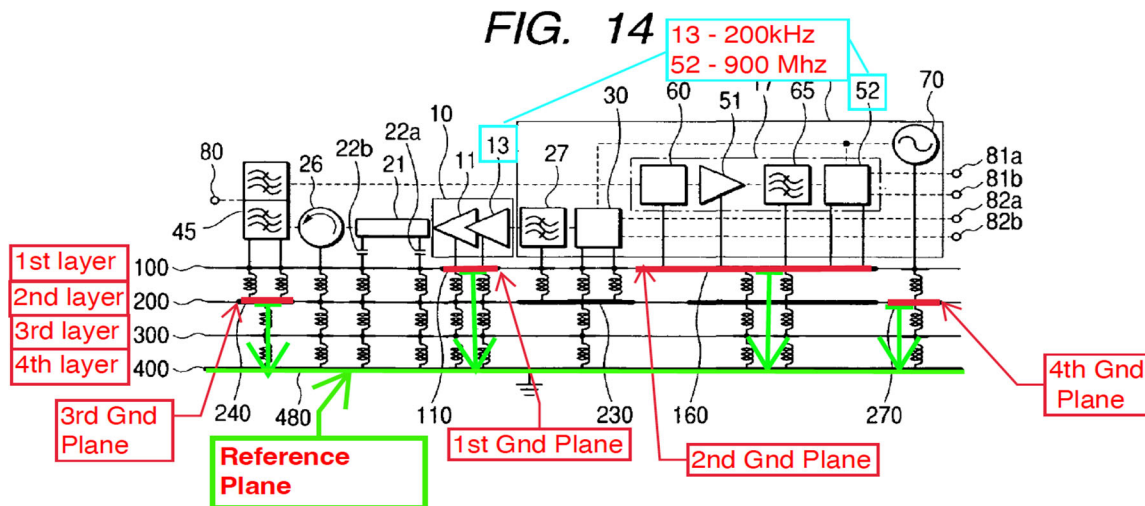
105. A person of ordinary skill in the art would have understood that 900 MHz is a higher frequency than 200 kHz, and thus circuit 13 would be understood as “low speed electronic circuitry”. Okabe also discloses circuit 13 is a part of power amplifier (PA) circuit 10, and that the PA ground plane 110 (e.g., a first ground plane) is connected to the ground terminals of the PA 10. (*Id.*, 7:52-55; 8:25-27). A person of ordinary skill in the art would have understood that connection of the PA circuit 10 to the first ground plane would be an “electrical connection”.

106. Further, the '091 Patent discloses as AAPA that high and low speed circuitry were commonly known in the art and could be electrically connected to a ground plane (Ex. 1001, 1:64-67 [“in the depicted die 101 the **high speed portions** of the die and **low speed portions** of the die are electrically connected to the same ground plane Vss 111.”].)

e) **“a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection with high speed electronic circuitry;”**

107. In my opinion, Okabe discloses this claim feature. As shown in Figure 14, shown below, Okabe discloses a second ground plane 160 on the first layer 100 that is separated from and electrically isolated from the first ground plane 110 on the first layer 100. (Ex. 1005, 14:13-25; 14:64 – 15:3) Okabe teaches in the example

above that circuit 13 operates in a frequency band of 200 kilohertz (kHz), while circuit 52 operates in a frequency band of 900 megahertz (MHz). (*Id.*, 7:36-41).



(*Id.*, FIG. 14 (annotated).)

108. A person of ordinary skill in the art would have understood that 900 MHz is a higher frequency than 200 kHz, and thus circuit 52 would be understood as “high speed electronic circuitry”. Okabe teaches the “receiver are connected to the receive circuits ground plane 160 by bonding wires or solder bumping”. (*Id.*, 14:65-67). A person of ordinary skill in the art would have understood that bonding wires or solder bumping would be an electrical connection from the second ground plane 160 to the “high speed electronic circuitry” of circuit 52.

f) “a second layer of the substrate includes,”

109. In my opinion, Okabe and AAPA both disclose this claim feature. As shown in Figure 14, shown above, Okabe discloses a second layer 200 of the

substrate 4. (*Id.*, 8:18-21, 9:28-31) Further, the '091 Patent discloses as AAPA an IC package includes **layers**. (Ex. 1001, 1:30-32, 5:1-2 (emphasis added).)

g) “a third ground plane configured for electrical connection with low speed electronic circuitry, and”

110. In my opinion, Okabe discloses this claim feature. As shown in Figure 14, shown above, Okabe discloses a third ground plane 240 on the second layer 200 of the substrate 4. (Ex. 1005, 8:27-35) Ground plane 240 (e.g., a third ground plane as ground plane 110 is a first ground plane and ground plane 160 is a second ground plane) is electrically connected to duplexer 45. (*Id.*, 14:18-19) A person of ordinary skill in the art would understand that duplexer 45 would be capable of operating at a lower frequency than voltage controller oscillator (VCO) 70, thus the third ground plane 240 would be “configured for” electrical connection with “low speed electronic circuitry”.

h) “a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the fourth ground plane configured for electrical connection with high speed electronic circuitry, and”

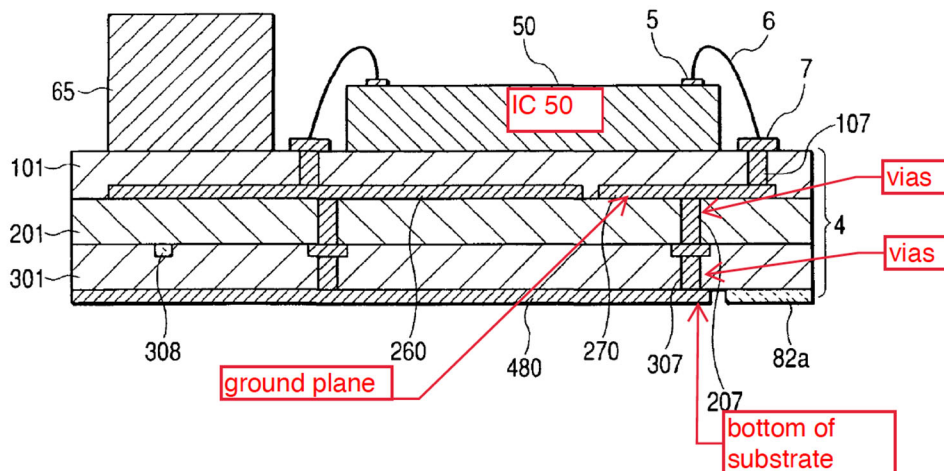
111. In my opinion, Okabe discloses this claim feature. Okabe shows in Figure 14, shown above, a fourth ground plane 270 separated and electrically isolated from the third ground plane 240 on the same layer 200 of the substrate 4. (*Id.* 14:13-33) As discussed above, a person of ordinary skill in the art would understand that voltage controller oscillator (VCO) 70 would be capable of operating

at a higher frequency than duplexer 45, thus the fourth ground plane 270 would be “configured for” electrical connection with “high speed electronic circuitry”.

i) “a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate”

112. In my opinion, Okabe and AAPA disclose this claim feature. Okabe in figure 9, shown below, discloses a first ground plane 270 electrically connected to a bottom of a substrate 4 by way of vias 207 and 307. (*Id.*, 8:38-44) A person of ordinary skill in the art would have understood that “vias” would be a plurality of electrical connections as was well known as discussed below in paragraph 109. Okabe also discloses solder bumping may be used in a flip chip connection process. (*Id.*, 9:32-38)

FIG. 9



(*Id.*, FIG. 9 annotated.)

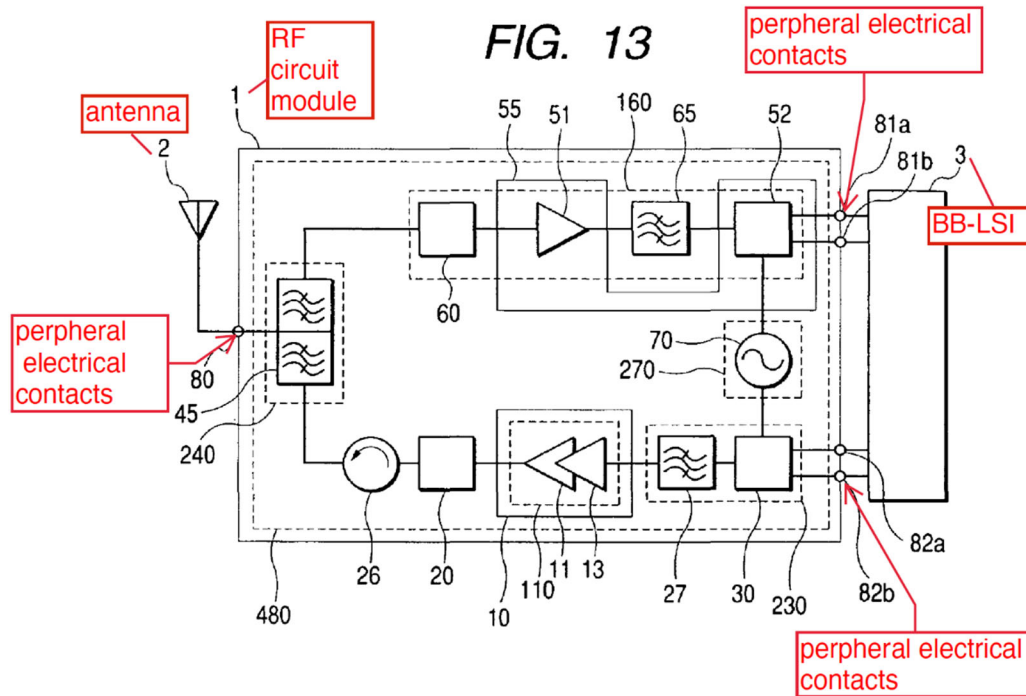
113. I've been asked to assume that Okabe does not teach this limitation. Under this scenario, the '091 Patent also discloses that the prior art teaches solder balls on a bottom of a substrate are electrically connected to a ground layer, either via fingers to vias or directly via interlayer vias. (Ex. 1001, 1:51-67; 4:37-42 [“when the principles of the invention are applied to ball grid array (BGA) type packages, these contacts are typically facilitate[d] by conductive vias that pass through the substrate and are electrically connected to both, a ground plane and an underlying solder pad. Solder balls are then used to make the external ground connections to other grounds”.]) The '091 Patent further discloses as AAPA that the packaging substrate 600 can be “an ordinary multi-layer BGA substrate 600” (*Id.*, 7:34-35)

114. As such, a person of ordinary skill in the art would have understood that a normal (ordinary) BGA substrate would provide a plurality of electrical connections to connect a ground plane with solder balls mounted on a second surface (e.g., bottom) of the BGA substrate. As such, a person of ordinary skill in the art would understand that solder balls could be mounted on the bottom of Okabe's substrate 4 and that Okabe's vias 207 and 307 would be a “plurality of electrical connections” to electrically connect Okabe's ground plane 270 with the solder balls.

j) “a plurality of electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate”

115. In my opinion, both Okabe and AAPA discloses this claim feature. Okabe teaches a second ground plane 260 (e.g., ground plane 260 that is different from ground plane 270) is electrically connected to a second (e.g., bottom) surface of a substrate 4 by way of vias shown in Figure 9, shown below. As discussed in section 1i above, the '091 Patent discloses as AAPA that the prior art taught solder balls mounted on a bottom surface of a BGA package. The '091 Patent further discloses that “typically, metallization lines 115 electrically connects the fingers to vias (not shown) that connect with solder balls on the bottom of the substrate. In some configurations the fingers 114 are typically connected to the ground plane”. (Ex. 1001, 1:50-61) Thus, a person of ordinary skill in the art would have understood the vias would be “a plurality of electrical connections that would electrically connect a second ground plane 260 to commonly used solder balls.

antenna 2 and peripheral connections 81a-82b connect the RF module 1 with the external BB-LSI 3. (*Id.*, 7:23-35; 13:40-45).



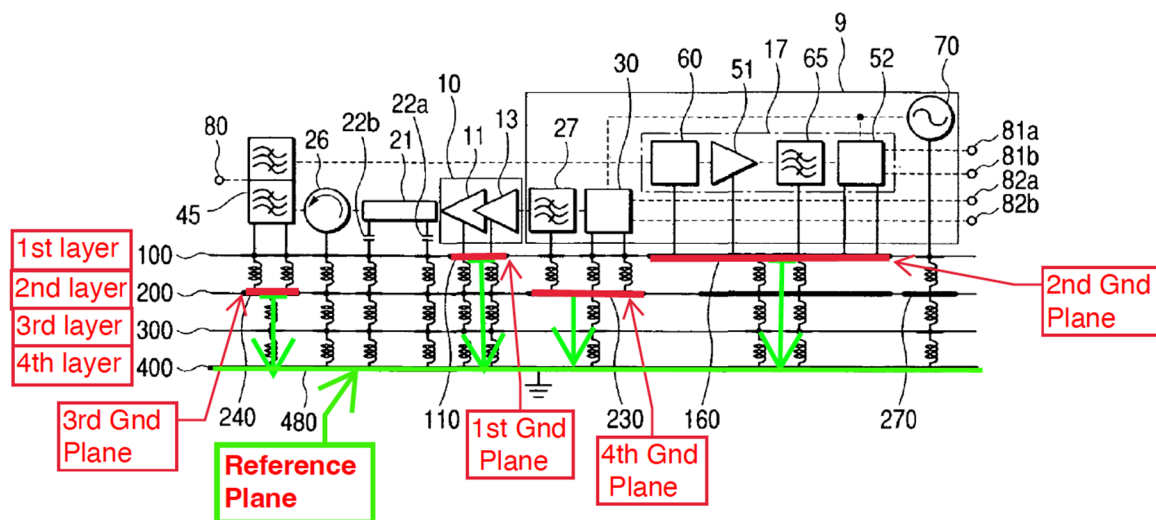
(*Id.*, FIG. 13 (annotated).)

117. The '091 Patent discloses as AAPA that “the semiconductor industry makes wide use of packaging substrates to hold and electrically interconnect integrated circuit (IC) die mounted within the packaging substrate. In some implementations the packaging substrates are configured to protect and secure the delicate IC die while enabling electrical connections with known **external** electrical interconnection socket formats.” (Ex. 1001, 1:16-22.) A person of ordinary skill in the art would have understood that external electrical interconnection socket formats would include “peripheral electrical contacts arranged on the substrate” and that the

external interconnection socket formats would include being configured for connection with circuitry external to an IC package.

I) “At least one reference plane associated with each layer of the substrate and the ground planes included thereon”

118. In my opinion, Okabe discloses this claim feature. Okabe discloses in Figure 14, shown below, a common ground plane 480 associated with a first layer 100, a second layer 200, a third layer 300, and a fourth layer 400 (e.g., each layer of substrate 4) and each ground plane included on each of the four layers 100-400 (Ex. 1005, 14:13-25) Okabe further discloses that “by providing the module with the common ground plane 480 to which all ground planes are connected, **reference potential** for all RF circuits can be fixed, not dependent on the ground land on the motherboard. As such, a person of ordinary skill in the art would have understood the common ground plane would be able to be “a reference plane”.



(*Id.*, FIG. 14 (annotated).)

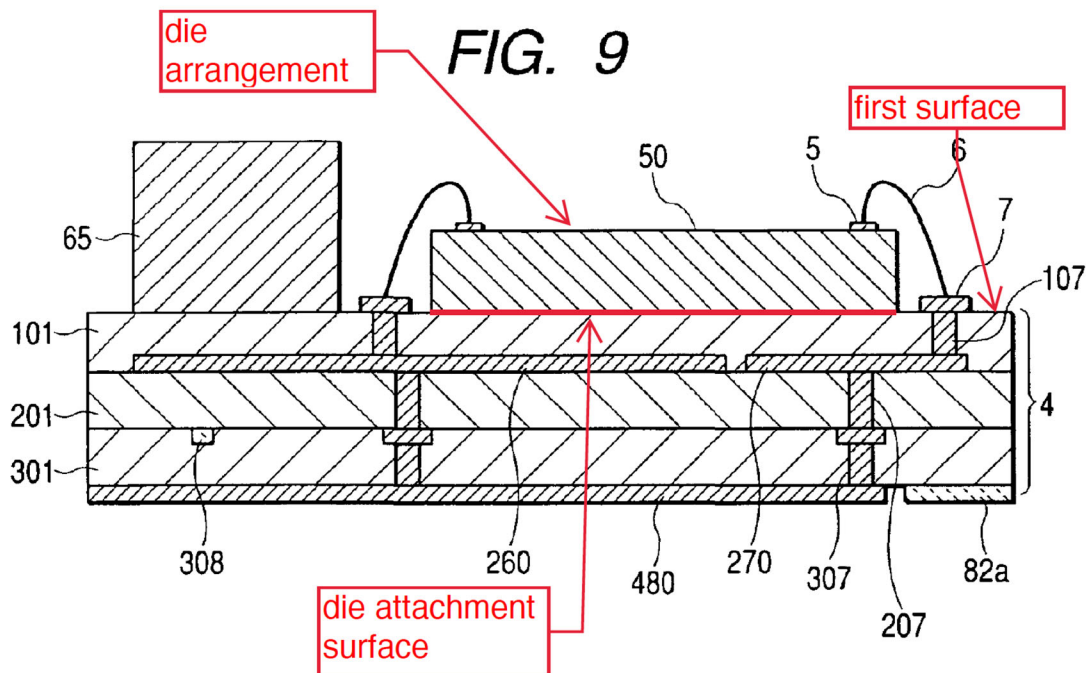
119. This is evidenced further by the background section of the '091 Patent, which discloses as applicant's admitted prior art (AAPA) that "in typical implementations the IC die is grounded to a single ground plane (also referred to herein as a 'Vss plane')" and subsequently refers to a "Vss reference layer", which illustrates that it was well known that a ground layer or plane could serve as a reference layer or plane. (Ex. 1001, 1:25-27; 8:1).

2. Claim 12

120. It is my opinion that Okabe in view of Applicant's Admitted Prior Art discloses or suggests each and every element of dependent claim 12.

a) "An IC package as recited in claim 1, wherein the first surface includes a die attachment surface with a die arrangement attached thereto"

121. In my opinion, the Okabe-AAPA combination discloses or suggests this feature. Okabe discloses in Figure 9, shown below, an IC 50 is mounted (attached) to a first surface (e.g., top) of substrate 4 at a particular area of the substrate (die attachment surface). (Ex. 1005, 9:9-14)



(*Id.*, FIG 9 (annotated).)

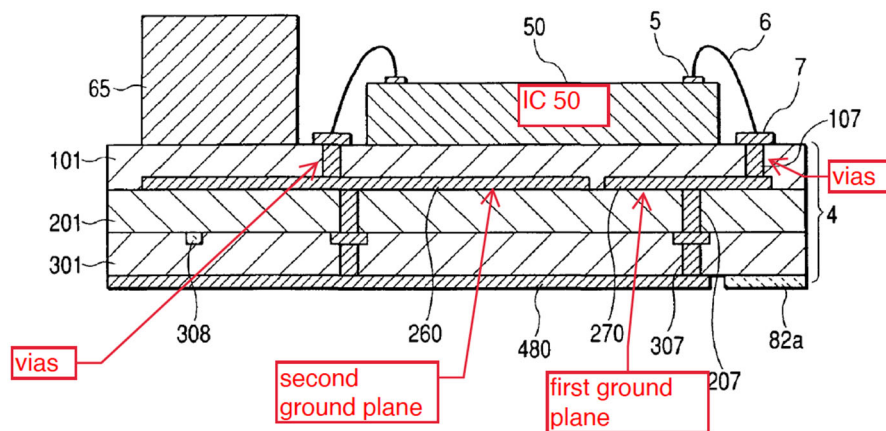
122. Okabe does not explicitly use the term “die attachment surface”. However, the ’091 Patent discloses as AAPA “in one common implementation semiconductor die is attached to the substrate and electrically connected to various electrical connections of the substrate using, for example, wire-bonding techniques. The wire bonds and the die are typically encapsulated with a protective layer of encapsulant. Such packages and the methods of their construction are well known to persons having ordinary skill in the semiconductor packaging arts.” (Ex. 1001, 1:35-42) As such, a person of ordinary skill in the art would have known that the top of

Okabe's substrate where the IC is mounted, would be a "die attachment surface" for mounting an integrated circuit on the first surface of the substrate.

b) "the die arrangement being electrically connected to the first ground plane, the second ground plane, and the peripheral electrical contacts of the substrate"

123. In my opinion, both Okabe alone and the Okabe-AAPA combination disclose or suggest this feature. Okabe discloses an IC being electrically connected to a first ground plane and a second ground plane on a substrate. For example, Figure 9, shown below, shows an integrated circuit 50 connected (e.g., by way of ground pad 5, bond wire 6, bonding pad 7, and via 107) to a first ground plane 270 and a second ground plane 260. (Ex. 1005, 9:24-31)

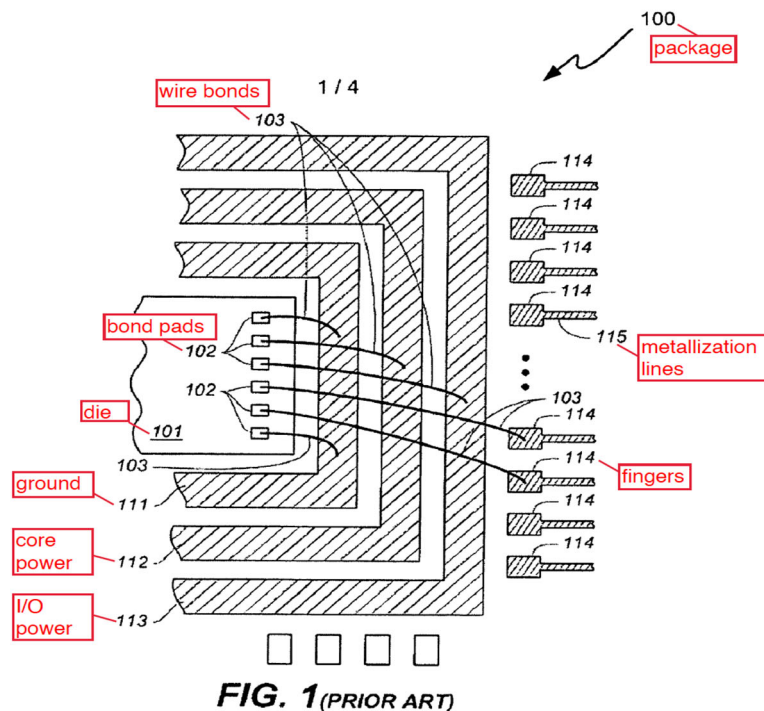
FIG. 9



(*Id.*, FIG. 9 (annotated).)

124. Okabe further discloses the IC being electrically connected to terminals 81a-82b, which are on the peripheral of the substrate module (*Id.*, 7:4-15, 23-35; 8:29-40).

125. The '091 Patent discloses as AAPA that “packaging substrates are configured to protect and secure the delicate IC die while enabling electrical connections with known external electrical interconnection socket formats”. (Ex. 1001, 1:19-22.) The peripheral contacts are clearly shown in the '091 Patents prior art Figure 1, shown below, as fingers 114 and metallization lines 115 that are electrically connected to die 101 via bond pads 102 and wires 103.



(*Id.*, FIG. 1 (annotated).)

126. As such, even in a scenario where Okabe did not disclose a die electrically connected to peripheral contacts, it would have been obvious to a person of ordinary skill in the art to modify Okabe to provide electrical connections from

an IC die arrangement to peripheral contacts in order to route power and signals from the IC to a PCB. The modification of Okabe with the AAPA would have amounted to nothing more than the use of a known technique to improve a similar device, and the results of the modification would have been predictable. This is because at the time of the invention, a person of ordinary skill in the art would have had the requisite skill level to readily modify the device disclosed by Okabe to implement the teachings of electrical connections to peripheral contacts disclosed by the '091 AAPA. Moreover, such modification of Okabe would have been routine for the person of ordinary skill in the art as they would be using well-known elements with no change in their respective functions.

D. Okabe in Combination with AAPA and Sutardja Discloses or Suggests the Features of Claims 2, 5, 6, and 9.

1. Claim 2

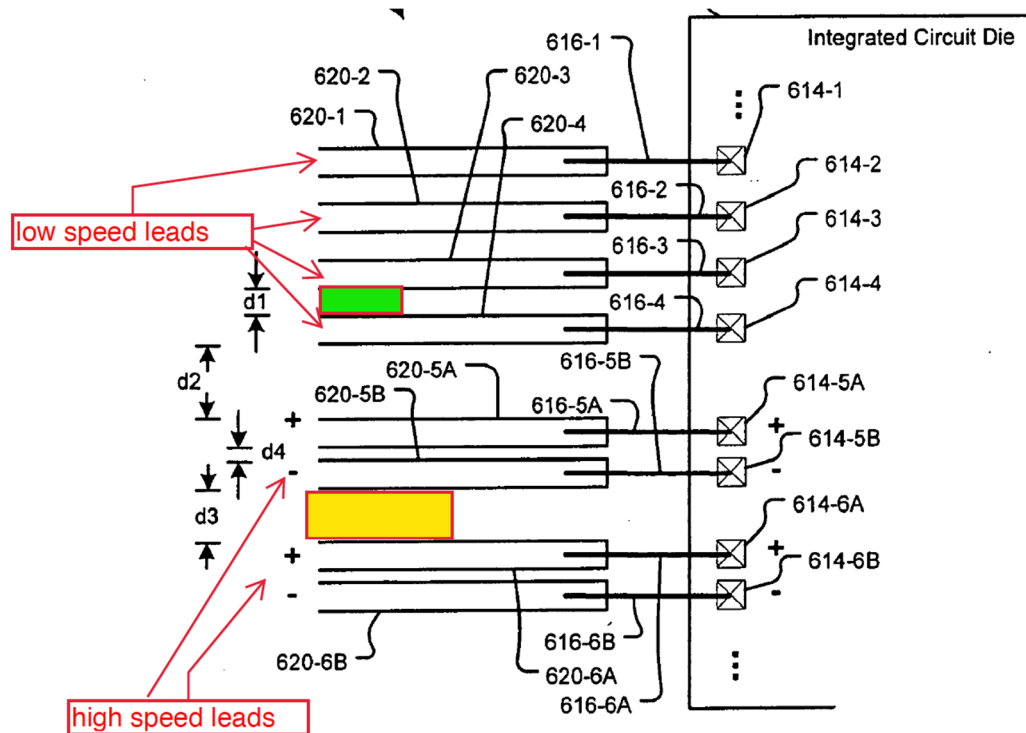
127. It is my opinion that Okabe in view of AAPA and Sutardja discloses or suggests each and every element of dependent claim 2.

a) “An IC package as recited in claim 1, wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with low speed circuitry, and”

b) “a second set of electrical contacts for electrical connection with high speed electronic circuitry; and”

128. In my opinion, the Okabe-AAPA-Sutardja combination discloses these claim features. The *Okabe-AAPA* combination teaches an IC package with peripheral

electrical contacts for electrical connection with low speed and high speed circuitry. (See *supra* Section X.C.1(a-f) regarding claim 1) As shown below in Figure 10A below, *Sutardja* also discloses this claim feature by disclosing an integrated circuit (IC) package that includes an IC die having die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶138) and that the leads 620-1 through 620-4 “operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B”. (*Id.* ¶139)



(*Id.*, FIG. 10A (annotated).)

129. A person of ordinary skill in the art would have understood that the leads operating at a lower speed would be a first set of electrical contacts for

electrical connection with low speed circuitry and the leads operating at a higher speed would be a second set of electrical contacts for electrical connection with high speed circuitry.

c) “wherein the second set of electrical contacts are spaced apart at a distance that is at least twice as far apart as the spacing for the first set of electrical contacts.”

130. Sutardja shows in Figure 10A above, that the second set of leads appear to be twice as far apart as the first set of leads, but does not explicitly state this. However, Sutardja does state that the distances between the high and low speed leads “may be irregular to increase or decrease coupling” (Ex. 1012, ¶0139)

131. It would be obvious to a person of ordinary skill in the art to modify the distances of a first and second set of electrical contacts to “increase or decrease coupling” as disclosed by Sutardja and a spacing for the second set of at least twice as far apart as the first set, as inherently disclosed by Sutardja, would be obvious to try for a person of ordinary skill in the art.

132. A person of ordinary skill in the art would have known that spacing between the leads (electrical contacts) affects the coupling. Thus, such a person would have been motivated to modify the spacing of the leads to minimize cross talk and/or maintain impedance accuracy of such low and high speed leads.

133. A person of ordinary skill in the art implementing an IC package like that of the Okabe-AAPA combination would have had good reason to look to

Sutardja, particularly because all of these references are in the same field of integrated circuit packages. Having looked to Sutardja, such a person of ordinary skill in the art would have been motivated to utilize spacing of the electrical contacts with characteristics suitable for connection with low speed circuitry as disclosed by Sutardja for the peripheral electrical contacts of the IC package of Okabe-AAPA to ensure impedance accuracy and minimize cross-talk (increase or decrease coupling).

134. Moreover, a person of ordinary skill in the art would have found it straightforward to space the high and low speed leads as disclosed by Sutardja. Such an implementation would have simply been the application of a known device (IC with low speed contacts) to a similar device (IC) and would have produce predictable results (increase or decrease coupling). Therefore, in my opinion, the Okabe-AAPA-Sutardja combination discloses or suggests this claim feature.

2. Claim 5

135. It is my opinion that Okabe in view of Applicant's Admitted Prior Art (AAPA) and Sutardja discloses or suggests each and every element of dependent claim 5.

a) “An IC package as recited in claim 1, wherein the low speed electronic circuitry is defined as circuitry having serial transfer rates of less than about 1 Gigabits per second (Gb/s); and”

136. As discussed above in Section X.C.1(d), the *Okabe-AAPA* combination discloses an IC package with low speed electronic circuitry, but does not explicitly state low speed is defined as less than 1 Gb/s. *Sutardja* discloses an integrated circuit die connected to low speed leads and high speed leads. (Ex. 1012, ¶[0139]) *Sutardja* further discloses that the high speed leads are operable to for high speed signals that are “greater than or equal to 1 Gigabit per second”. (*Id.*, ¶[0075]) A person of ordinary skill in the art would have understood that if high speed is greater than or equal to 1 Gb/s, than low speed would be “less than about 1 Gb/s.”

b) “wherein the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 1 Gb/s.”

137. As discussed above, *Sutardja* discloses an integrated circuit die connected to low speed leads and high speed leads. (*Id.*, ¶[0139]) *Sutardja* further discloses that the high speed leads are operable to for high speed signals that are “greater than or equal to 1 Gigabit per second”. (*Id.*, ¶[0075])

138. A person of ordinary skill in the art would take note that the '091 Patent does not provide any specific disclosure regarding any advantages, criticality, or unexpected results related to the specific speed of “greater than about 1 Gb/s

[gigabits per second]” recited in claim 5. As has been shown in numerous contemporaneous references mentioned above, speeds of 1 Gb/s were well known in the art.

3. Claim 6

139. It is my opinion that Okabe in view of Applicant’s Admitted Prior Art, and Sutardja discloses or suggests each and every element of dependent claim 6.

a) “An IC package as recited in claim 1 wherein the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 8.5 Gb/s.”

140. As discussed above in Section X.C.1(e), the Okabe-AAPA combination teaches an IC package with high speed circuitry, but does not explicitly state high speed is defined by 8.5 Gb/s. However, *Sutardja* discloses an integrated circuit die connected to low speed leads and high speed leads. (Ex. 1012, 0139) The high speed leads are operable to for high speed signals that are “greater than or equal to 1 Gigabit per second” (*Id.*, ¶[0075]) A person of ordinary skill in the art would have understood that if high speed is greater than or equal to 1 Gb/s, that would include speeds of 8.5 Gb/s.

141. A person of ordinary skill in the art would take note that the ‘091 Patent does not provide any specific disclosure regarding any advantages, criticality, or unexpected results related to the specific speed of “greater than about 8.5 Gb/s” recited in claim 6. A person of ordinary skill in the art would also take note that the

'091 Patent does not provide any structural difference to the IC package or the high speed electronic circuitry in claims 5 and 6 when differentiating between purported high speed thresholds of 1 Gb/s in claim 5 and 8.5 Gb/s in claim 6. As has been shown in numerous contemporaneous reference mentioned above, speeds of Gb/s and 8.5 Gb/s were well known in the art.

4. Claim 9

142. It is my opinion that Okabe in view of Applicant's Admitted Prior Art (AAPA), and Sutardja discloses or suggests each and every element of dependent claim 9.

a) "An IC package as recited in claim 1 wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with low speed circuitry, and"

b) "a second set of electrical contacts for electrical connection with high speed circuitry; and"

143. As discussed above in Section X.D.1(a-b), Sutardja discloses an integrated circuit (IC) package that includes an IC die having die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B". (*Id.* ¶ [0139])

144. A person of ordinary skill in the art would have understood that “low speed leads” 620-1 through 620-4 would be “a first set of electrical contacts for electrical connection with low speed circuitry” and that “high speed leads” 620-5A through 620-6B would be equivalent to “a second set of electrical contacts for electrical connection with high speed circuitry”.

c) “wherein the electrical contacts are arranged such that, the first spacing between the contacts of the first set of electrical contacts is smaller than a second spacing between the contact of the second set of electrical contacts, thereby enabling greater contact density for the first set of electrical contacts.”

145. Sutardja discloses various spacing between the low speed leads, the high speed leads, and between the low and high speed leads. This spacing “may be irregular to increase or decrease coupling” (*Id.*, ¶[0139]). Sutardja shows in Figure 10A that the spacing (d1) between the first set of electrical contacts is smaller than the spacing (d3) between the second set of electrical contacts. Thus, it would have been obvious to a person of ordinary skill in the art that the smaller spacing of the first set of electrical contacts (low speed leads) would be “enabling greater contact density for the first set of electrical contacts”.

146. A person of ordinary skill in the art implementing an IC package that of Okabe-AAPA would have had good reason to look to Sutardja as these references are in the same field of IC packages. Having looked to Sutardja, such a person of

ordinary skill in the art would have been motivated to use the decreased spacing of Sutardja in order to enable more contacts for the Okabe-AAPA IC package.

147. Moreover, a person of ordinary skill in the art would have found it straightforward to decrease spacing to enable more contact density for the low speed signals where spacing is generally not an issue due to less crosstalk issues with low speed signals.

E. Okabe in Combination with Sutardja and Taggart Discloses or Suggests the Features of Claims 3, 4 and 7.

1. Claim 3

148. It is my opinion that Okabe in view of AAPA, Sutardja, and Taggart discloses or suggests each and every element of dependent claim 3.

a) “An IC package as recited in claim 2, wherein the first set of electrical contacts are spaced apart a distance of at least 70 μm (micrometers)”

149. In my opinion, the Okabe-AAPA-Sutardja-Taggart combination discloses or suggests this limitation. As discussed above in Section X.D.1(a), the Okabe-AAPA-Sutardja combination teaches an IC package with a first set of electrical contacts spaced to minimize cross talk and/or maintain impedance accuracy (increase or decrease coupling), but does not explicitly disclose a spacing of 70 micrometers.

150. However, *Taggart* discloses a distance (pitch) between wire-bond pads, wire-bonds, and die bond pads within a range from about 10 micrometers to about

200 micrometers. (Ex., 1009, ¶[0027]) A person of ordinary skill in the art working with the Okabe-AAPA-Sutardja IC package would look to Taggart as they are all in the integrated circuit packaging field. Moreover, a person of ordinary skill in the art would have understood that any sets of Taggarts' wire-bond pads, wire-bonds, and die bond pads would be "electrical contacts" and the 70 micrometers would be in the range of about 10-200 micrometers. Such a person would have been motivated to space electrical contacts of the IC package of Okabe-AAPA-Sutardja with the ranges of Taggart to increase or decrease coupling which would minimize cross talk and/or maintain impedance accuracy for the electrical contacts as was very well known in the art.

b) "and wherein the second set of electrical contacts are spaced apart a distance of at least 140 um (micrometers)"

151. As discussed above in Section X.D.1(b), the *Okabe-AAPA-Sutardja* combination teaches an IC package with a second set of electrical contacts spaced to increase or decrease coupling, but does not explicitly disclose a spacing of 140 micrometers.

152. However, *Taggart* discloses a distance (pitch) between wire-bond pads, wire-bonds, and die bond pads within a range from about 10 micrometers to about 200 micrometers, (*Id.*, ¶[0027]), with a specific embodiment where the pitch is about 135 micrometers (*Id.*, Claim 13). A person of ordinary skill in the art would have

understood that any other of the sets of wire-bond pads, wire-bonds, and die bond pads would be second “electrical contacts” and the 140 micrometers would be in the range of about 10-200 micrometers and specifically “about 135 micrometers” as disclosed by Taggart.

2. Claim 4

153. It is my opinion that Okabe in view of Applicant’s Admitted Prior Art, Sutardja, and Taggart discloses or suggests each and every element of dependent claim 4.

a) “An IC package as recited in claim 2, wherein the first set of electrical contacts are spaced apart a distance of at least 70 um (micrometers)”

154. In my opinion, the *Okabe-AAPA-Sutardja-Taggart* combination discloses this claim feature. As discussed in Section X.D.1 above, the *Okabe-AAPA-Sutardja* combination discloses this claim feature.

155. The Taggart discloses a distance (pitch) between wire-bond pads, wire-bonds, and die bond pads within a range from about 10 micrometers to about 200 micrometers. (*Id.*, ¶[0027]) A person of ordinary skill in the art would have understood that any sets of wire-bond pads, wire-bonds, and die bond pads would be “electrical contacts” and the 70 micrometers would be in the range of about 10-200 micrometers. Such a person would have been motivated to space electrical

contacts to increase or decrease coupling to minimize cross talk and/or maintain impedance accuracy as was very well known in the art.

b) “and wherein the second set of electrical contacts are spaced apart a distance of at least 200 um (micrometers)”

156. In my opinion, the *Okabe-AAPA-Sutardja-Taggart* combination discloses this claim feature. *Taggart* discloses a distance (pitch) between wire-bond pads, wire-bonds, and die bond pads within a range from about 10 micrometers to about 200 micrometers (um), and gives a specific example of the wire-bond pads, the die bond pads, and the wire-bonds “spaced on 200 um centers”. (*Id.*, 0027).

3. Claim 7

157. It is my opinion that *Okabe* in view of Applicant’s Admitted Prior Art, *Sutardja*, and *Taggart* discloses or suggests each and every element of dependent claim 7.

a) “An IC package as recited in claim 1 wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with low speed circuitry, and”

158. In my opinion, the *Okabe-AAPA-Sutardja-Taggart* combination discloses or suggests this feature. As discussed above in Section X.C.1(a-d), the *Okabe-AAPA* combination teaches an IC package with peripheral electrical contacts for electrical connection with low speed circuitry. As shown below in Figure 10A, *Sutardja* discloses an integrated circuit (IC) package that includes an IC die having

die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 “operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B”. (*Id.* ¶[0139])

159. A person of ordinary skill in the art would have understood that the leads operating at a lower speed would be a first set of electrical contacts for electrical connection with low speed circuitry.

b) “a second set of electrical contacts for electrical connection with high speed circuitry, and”

160. In my opinion, the Okabe-AAPA-Sutardja-Taggart combination discloses or suggests this feature. As shown below in Figure 10A, Sutardja discloses die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 “operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B”. (*Id.* ¶[0139]) A person of ordinary skill in the art would have understood that die pads 614-5A through 614-6B, bondwires 616-5A through 616-6B, and “high speed leads” 620-5A through 620-6B would be equivalent to “a second set of electrical contacts for electrical connection with high speed circuitry”. A person of ordinary skill in the art would have understood that die pads 614-1 through 614-4, bondwires 616-1 through 616-4, and “low speed leads” 620-1

through 620-4 would be equivalent to “a first set of electrical contacts for electrical connection with low speed circuitry”.

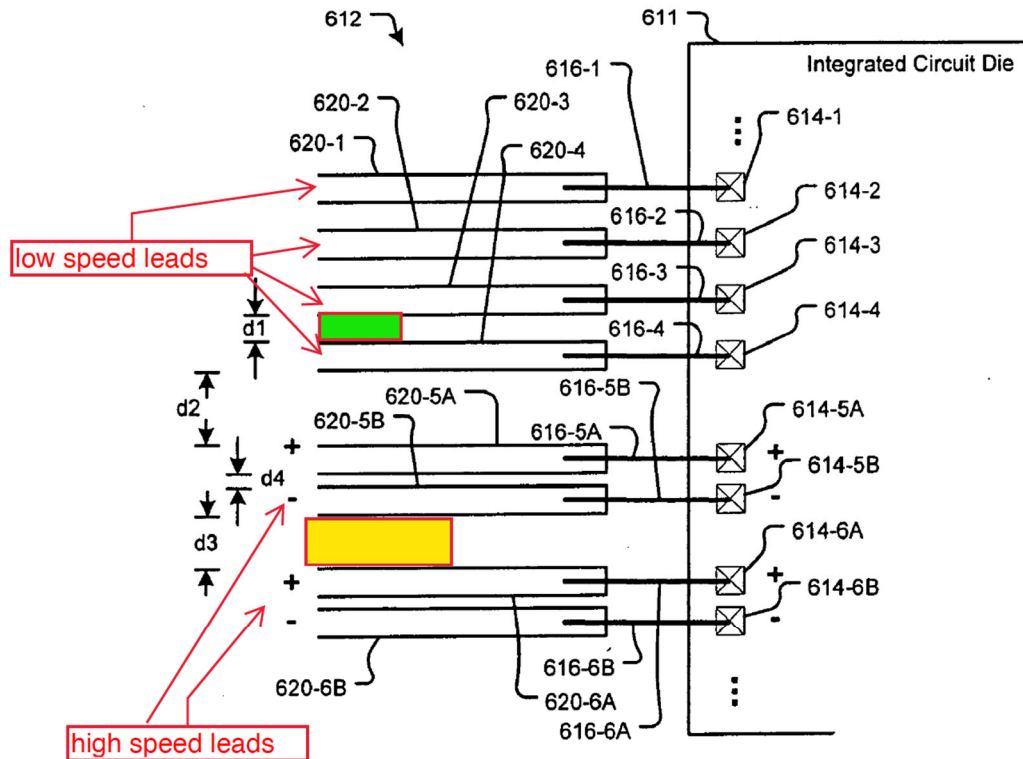


FIG. 10A

(*Id.*, FIG. 10A (annotated).)

c) “wherein the second set of electrical contacts are spaced apart at a distance that is at least three times as far apart as the spacing for the first set of electrical contacts.”

161. In my opinion, the Okabe-AAPA-Sutardja-Taggart combination discloses or suggests this feature. Sutardja discloses various spacing between the low speed leads, the high speed leads, and between the low and high speed leads. Sutardja explicitly states that “this spacing “may be irregular to increase or decrease

coupling” (*Id.*, ¶[0139]). Although Sutardja shows in Figure 10A the spacing (d3) between the second set of electrical contacts is larger than the spacing (d1) between the first set of electrical contacts, Sutardja does not explicitly state the d3 spacing is “at least three times as far apart” as the d1 spacing.

162. Taggart discloses an integrated circuit (IC) package that includes an IC die having die bond pads connected to wire-bond pads via bond wires. Taggart further discloses spacing any of the die bond pads, wire-bond pads, and bond wires in accordance with a pitch that ranges from “about 10 um [micrometers] to 200 um”. A person of ordinary skill in the art would have understood that this range would include many pitch values that would be 3x greater than other pitch values in the ranges. For example, a first pitch value of 10um would leave 30 um – 200 um values that would all be at least three times greater than 10 um.

163. A person of ordinary skill in the art would have good reason to look to Taggart to modify Sutardja to select values within 10 um – 200 um to increase or decrease coupling between the high or low speed leads as needed. Because Taggart and Sutardja both disclose integrated circuit packages very similar to the Okabe-AAPA combination, a person of ordinary skill in the art implementing the IC package of Okabe-AAPA would have good reason to look to Taggart and Sutardja.

164. A person of ordinary skill in the art would have understood that particular spacing between the leads for high speed and low speed would modify the

coupling of signals as disclosed by Sutardja. Such a person would have a reasonable expectation of success in implementing spacing as they were well-known and widely-implemented features of signal traces in integrated circuit packages.

F. Okabe in Combination with Applicant's Admitted Prior Art (AAPA), Sutardja, and Choi Discloses or Suggests the Features of Claims 8 and 11.

1. Claim 8

165. It is my opinion that Okabe in view of Applicant's Admitted Prior Art, Sutardja, and Choi discloses or suggests each and every element of dependent claim 8.

a) "An IC package as recited in claim 1, wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with low speed circuitry, and"

166. As discussed above in Section X.C.1, the Okabe-AAPA combination discloses an IC package with peripheral electrical contacts that can be used with low speed circuitry. I have been asked to assume that the Okabe-AAPA combination does not disclose a first set of electrical contacts.

167. Under this presumption, as discussed above in Section X.G.1(a), Sutardja discloses an integrated circuit (IC) package that includes an IC die having die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-

6A and 620-6B”. (*Id.* ¶ [0139]) A person of ordinary skill in the art would have understood that any of die pads 614-1 through 614-4, bondwires 616-1 through 616-4, and “low speed leads” 620-1 through 620-4 would be “a first set of electrical contacts for electrical connection with low speed circuitry”.

b) “a second set of electrical contacts for electrical connection with high speed circuitry”

168. As discussed above in Section X.G.1(b), Sutardja discloses die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 “operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B”. (*Id.* ¶ [0139]) A person of ordinary skill in the art would have understood that die pads 614-5A through 614-6B, bondwires 616-5A through 616-6B, and “high speed leads” 620-5A through 620-6B would be “a second set of electrical contacts for electrical connection with high speed circuitry”.

c) “wherein the second set of electrical contacts are spaced apart at a distance sufficient to establish a differential impedance of at least 100 ohms between the contacts of the second set of electrical contacts.”

169. Sutardja discloses spacing d_4 between the high speed leads (second set of electrical contacts), and that the spacing can be changed to “increase or decrease coupling”. (*Id.*, ¶ [0139]). However, Sutardja does not explicitly state “a differential impedance of 100 Ohms”.

170. Choi discloses a PBGA package having high speed differential traces designed to provide a 100 ohm differential impedance (Ex. 1011, p. 304). A person of ordinary skill in the art would have been motivated to modify the IC package of Okabe-AAPA with the spacing of Sutardja to achieve the 100 ohm differential impedance as taught by Choi. Such a person implementing the IC package of Okabe-AAPA would have looked to Sutardja and Choi as they are all in the same field of IC packages.

2. Claim 11

171. It is my opinion that Okabe in view of Applicant's Admitted Prior Art, Sutardja, and Choi discloses or suggests each and every element of dependent claim 11.

a) “An IC package as recited in claim 1 wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with low speed circuitry; and”

172. As discussed above in Section X.G.1(a), Sutardja discloses an integrated circuit (IC) package that includes an IC die having die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 “operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B”. (*Id.*, ¶ [0139]) A person of ordinary skill in the art would have understood that die pads

614-1 through 614-4, bondwires 616-1 through 616-4, and “low speed leads” 620-1 through 620-4 would be equivalent to “a first set of electrical contacts for electrical connection with low speed circuitry”.

b) “a second set of electrical contacts for electrical connection with high speed circuitry; and”

173. As discussed above in Section X.G.1(b), Sutardja discloses die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 “operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B”. (*Id.*, ¶ [0139]) A person of ordinary skill in the art would have understood that die pads 614-5A through 614-6B, bondwires 616-5A through 616-6B, and “high speed leads” 620-5A through 620-6B would be equivalent to “a second set of electrical contacts for electrical connection with high speed circuitry”.

c) “wherein the electrical contacts are arranged as part of I/O lines such that,”

174. Sutardja discloses die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 “operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B”. (*Id.*, ¶ [0139]) A person of ordinary skill in the art would have understood that 620-1 through 620-6B would be equivalent to input/output lines.

d) “a first spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance of at least 50Ω between the contacts of the first set of electrical contacts; and”

175. Sutardja discloses spacing d4 between the high speed leads (second set of electrical contacts), and that the spacing can be changed to “increase or decrease coupling” (*Id.*, ¶ [0139]). However, Sutardja does not explicitly state “a differential impedance of 50 Ohms.

176. However, Choi discloses, a multi-layered PCB that has a low-speed interconnects on layer 1 and that the low-speed signal transmission lines have characteristic impedances designed for 50 Ω (Ohms). (Ex. 1011, p. 304) A person of ordinary skill in the art implementing the *Okabe-AAPA-Sutardja* IC package would have had good reason to look to Choi as they are all dealing with multilayered substrates and/or signaling from an integrated circuit. A person of ordinary skill in the art implementing the *Okabe-AAPA-Sutardja* IC package with spacing of a first set of electrical contacts would have good reason to *Choi's* low-speed transmission lines having characteristic impedances of 50 Ohms to avoid impedance mismatch, which was known to cause degradation of a signal.

e) **“a second spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100Ω between the contacts of the second set of electrical contacts”**

177. Sutardja discloses spacing d4 between the high speed leads (second set of electrical contacts), and that the spacing can be changed to “increase or decrease coupling” (*Id.*, ¶ [0139]). However, Sutardja does not explicitly disclose “a differential impedance of at least 100 Ohms between the contacts of the second set of electrical contacts”.

178. However, Choi discloses a multi-layered PCB that has a high-speed interconnects on layer 6 and that the high-speed signal transmission lines have characteristic impedances designed for 100 Ω (Ohms). (Ex. 1011, p. 304)

179. A person of ordinary skill in the art would have good reason to modify the IC package of Okabe-AAPA with the spacing of Sutardja and the characteristic impedance of Choi. Such a person would have been motivated to set the spacing to decrease or increase coupling as needed to maintain a specific impedance.

G. Okabe in Combination with Applicant’s Admitted Prior Art (AAPA), Sutardja, Choi, and Digital Design Discloses or Suggests the Features of Claim 10.

1. Claim 10

180. It is my opinion that Okabe in view of Applicant’s Admitted Prior Art, Sutardja, Choi, and Digital Design discloses or suggests each and every element of dependent claim 10.

a) “An IC package as recited in claim 1 wherein the peripheral electrical contacts include “a first set of electrical contacts for electrical connection with low speed circuitry, and”

181. As discussed above in Section X.D.1(a), Sutardja discloses an integrated circuit (IC) package that includes an IC die having die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 “operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B”. (*Id.* ¶ [0139]) A person of ordinary skill in the art would have understood that die pads 614-1 through 614-4, bondwires 616-1 through 616-4, and “low speed leads” 620-1 through 620-4 would be “a first set of electrical contacts for electrical connection with low speed circuitry”.

b) “a second set of electrical contacts for electrical connection with high speed circuitry, and”

182. As discussed above in Section X.D.1(b), Sutardja discloses die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶ [0138]) and that the leads 620-1 through 620-4 “operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B”. (*Id.* ¶ [0139]) A person of ordinary skill in the art would have understood that die pads 614-5A through 614-6B, bondwires 616-5A through 616-6B, and “high

speed leads” 620-5A through 620-6B would be “a second set of electrical contacts for electrical connection with high speed circuitry”.

c) “wherein the electrical contacts are arranged as part of I/O lines such that,”

183. Sutardja discloses die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B for transmitting and receiving signals. (Ex. 1012, ¶ [0004], [0138])

d) “a first spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance of at least 50Ω between the contacts of the first set of electrical contacts to substantially eliminate cross-talk between I/O lines for the low speed electronic circuitry; and”

184. Sutardja discloses spacing d1 between the low speed leads (first set of electrical contacts), and that the spacing can be changed to “increase or decrease coupling” (*Id.*, ¶ [0139]).

185. Choi discloses, a multi-layered PCB that has a low-speed interconnects on layer 1 and that the low-speed signal transmission lines have characteristic impedances designed for $50\ \Omega$ (Ohms). (Ex. 1011, p. 304)

186. Digital Design discloses in Figure 5.4, shown below, that the spacing of signal traces affects crosstalk. (Ex. 1010, p. 192)

$$\text{Crosstalk} \approx \frac{K}{1 + (D/H)^2} \quad [5.2]$$

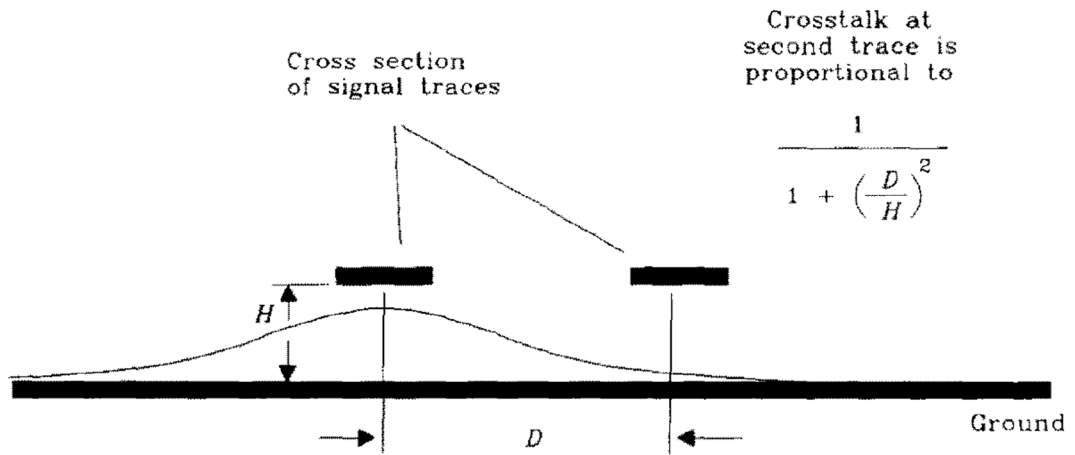


Figure 5.4 Cross section of two traces showing crosstalk.

(*Id.*, FIG. 5.4)

187. Digital Design further shows in Figure 5.20, shown below, measuring cross talk for lines having a 50 Ohm characteristic impedance.

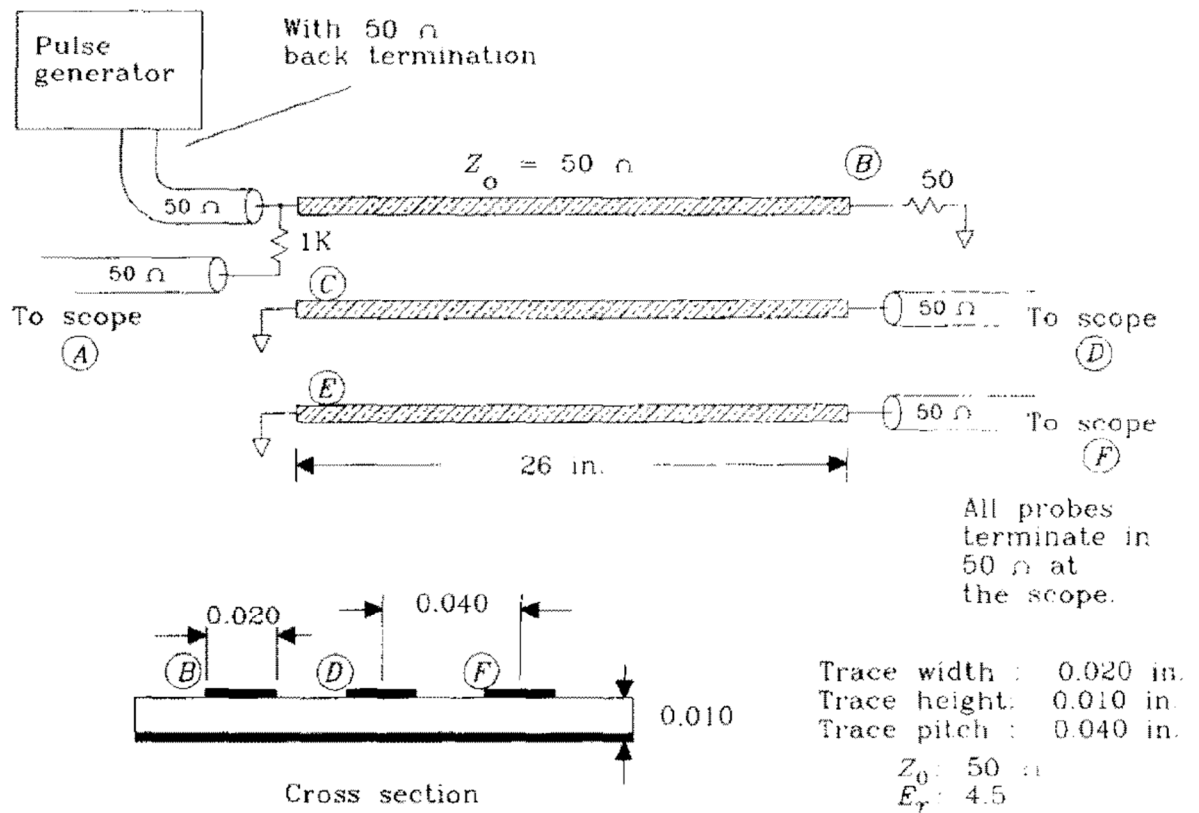


Figure 5.20 Setup for reflected reverse crosstalk measurement.

(*Id.*, FIG. 5.20)

188. A person of ordinary skill in the art implementing the IC package of Okabe-AAPA would have good reason to look at Choi, Digital Design, and Sutardja to modifying the spacing of signal lines of Sutardja to achieve a 50 Ohm impedance as taught by Choi and Digital Design as they are all related to IC packages and/or signal characteristics. Such a person would have been motivated to optimize the spacing as it was widely known in the art that spacing would affect the cross talk as disclosed by Digital Design.

e) **“a second spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100Ω between the contacts of the second set of electrical contacts to substantially eliminate cross-talk between I/O lines for the high speed electronic circuitry.”**

189. Sutardja discloses spacing d4 between the high speed leads (second set of electrical contacts), and that the spacing can be changed to “increase or decrease coupling”. (Ex. 1012, ¶ [0139])

190. Choi discloses, a multi-layered PCB that has a high-speed interconnects on layer 6 and that the high-speed signal transmission lines have characteristic impedances designed for $100\ \Omega$ (Ohms). (Ex. 1011, p. 304)

191. As discussed above with reference to Section X.I.1(d), Digital Design discloses it was well known that spacing of signal traces affects crosstalk (Ex. 1010, p. 192). As such, a person of ordinary skill in the art would have been motivated to implement Choi’s 100 Ohm characteristic impedance for high speed transmission lines, and the spacing of Digital Design and Sutardja to optimize coupling in order to substantially eliminate cross-talk as was widely known in the art. Such a person implementing the IC package of Okabe-AAPA would have good reason to look to Sutardja, Choi, and Digital Design as they all relate to IC packaging and/or signal trace spacing optimization.

H. Okabe in Combination with Applicant's Admitted Prior Art (AAPA), Kramer and Sutardja Disclose or Suggest the Features of Claim 13.

192. It is my opinion that Okabe in view of Applicant's Admitted Prior Art, Kramer, and Sutardja, discloses or suggests each and every element of dependent claim 13.

1. Claim 13

a) "An IC package as recited in claim 12, wherein the die arrangement comprises a die having both high-speed electronic circuitry and low-speed electronic circuitry; and"

193. Kramer shows in Figure 3, below, an integrated circuit 30 having a portion of the IC being analog circuitry 31. (Ex. 1007, 2:47-57). The analog circuitry transmits high-speed differential signals, with speeds over 4.25 Gb/s, via a shortened wire bond 46, while wire bond 40 transmits input/output signals from the other portions of the IC 30. (*Id.*, 11:14-23)

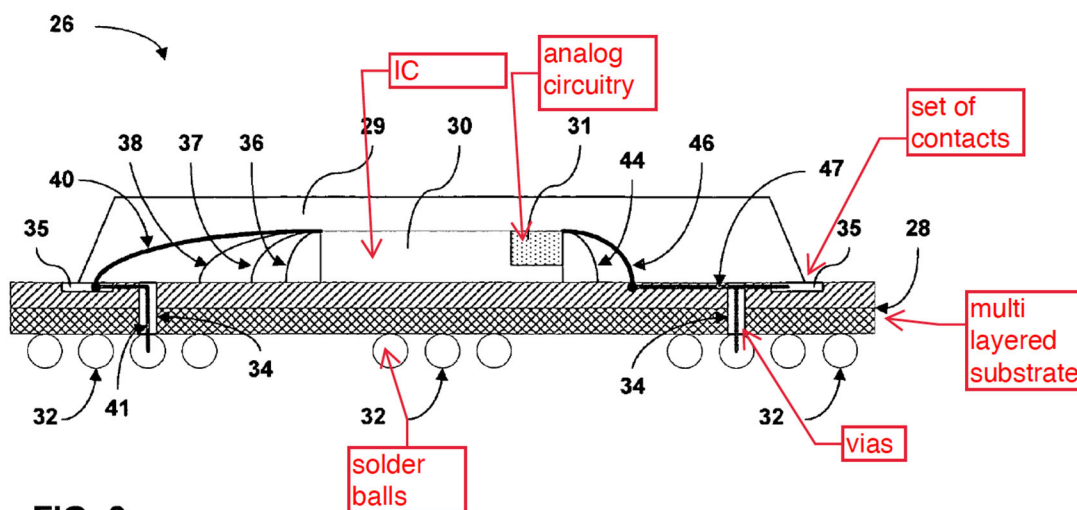


FIG. 3

(*Id.*, FIG. 3 (annotated).)

194. A person of ordinary skill in the art would have understood that analog circuitry operating at speeds of 4.25 Gb/s and above with specific isolated routing of these signals via separate wirebonds, would indicate that the other portions of the IC would not operate at those speeds and thus either the analog or the other portions (whichever has lower speeds), would include “low speed circuitry”.

b) “wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with low speed circuitry; and a second set of electrical contacts for electrical connection with high speed circuitry; and”

195. Sutardja discloses peripheral electrical contacts including high speed leads and low speed leads, shown below, where a first set of electrical contacts (620-1 – 620-4) are utilized for electrical connection with low speed circuitry, and a

second set of electrical contacts (620-5A – 620-6B) are utilized for electrical connection with high speed circuitry. (Ex. 1012, ¶ [0139]).

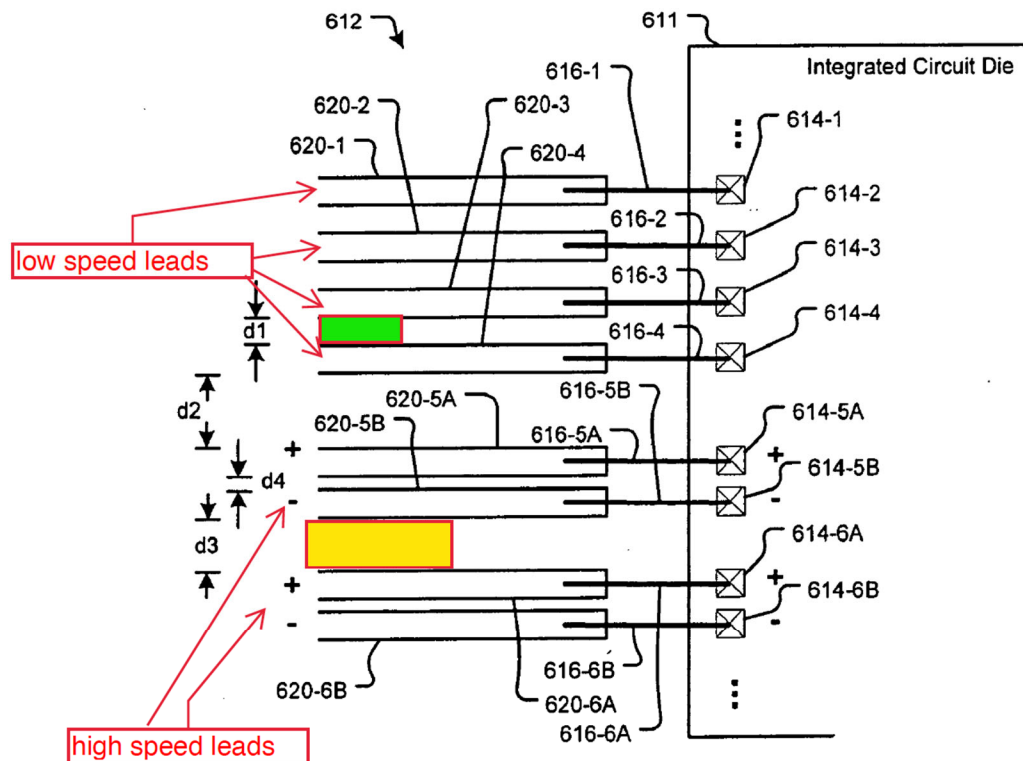


FIG. 10A

(*Id.*, FIG. 10A (annotated).)

c) “wherein the low-speed electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced for connection with the low speed electronic circuitry; and”

196. Kramer discloses in Figure 6, shown below, that an IC circuit 72 includes an analog circuit 73 that is connected with a first portion of ground plane 74 that is separated from the remaining portion of ground plane 74 outside the analog

area. Kramer discloses the analog circuitry operates at higher speeds (e.g., 4.25 Gb/s and above). Kramer also discloses the IC 72 (the non-analog portions) is connected to electrical contacts 77 outside the analog area. “Although not shown in FIG. 6, wire bonds outside of the analog area of the BGA package couple IC 72 to ground ring 74, power stripes 75 and 76, and the set of contacts 77. Analog circuit 73 of IC 72 requires isolated power and ground connections to avoid introducing noise from other circuits on IC 72 into analog circuit 73” (Ex. 1007, 8:60-66)

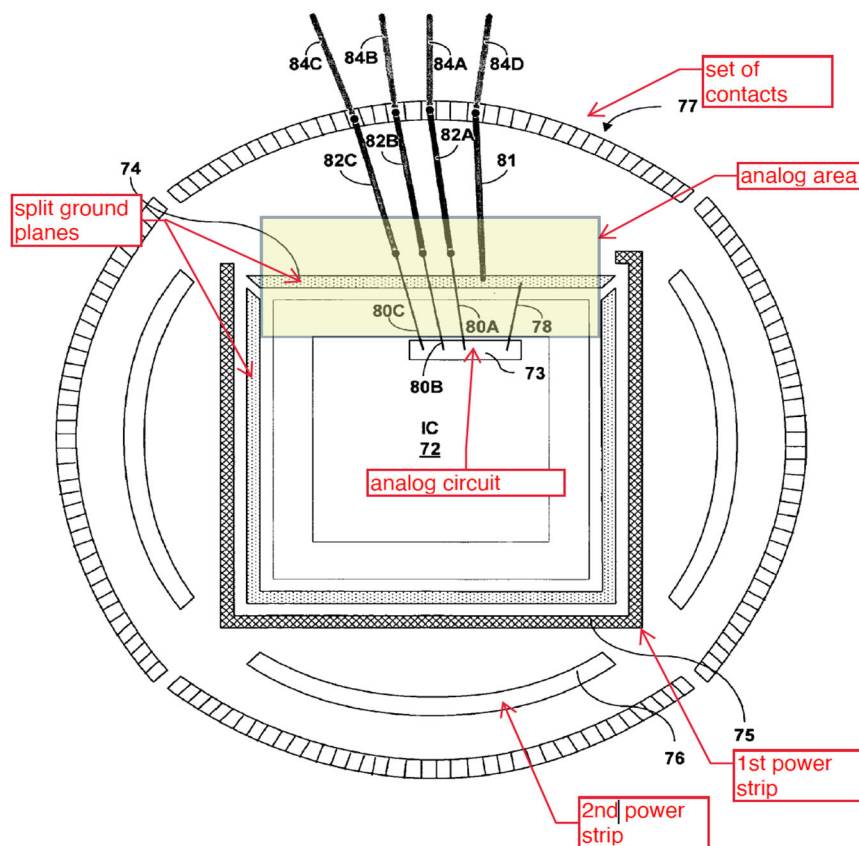


FIG. 6

(Ex. 1007, FIG. 6 (annotated).)

197. A person of ordinary skill in the art would have understood the IC operating at lower speeds than the analog circuit 73 would be low speed circuitry, and that the IC 72 being connected to the portion of the ground plane 74 outside the analog area would be a first ground plane. Kramer does not explicitly disclose the contacts 77 are “spaced for connection with low speed electronic circuitry”.

198. However, Sutardja clearly shows in Figure 10A that low speed leads are spaced closer together than high speed leads. Sutardja further discloses that spacing between the leads may be changed to “increase or decrease coupling. (Ex. 1012, ¶ [0139])

199. As such, a person of ordinary skill in the art would have understood spacing of lines and contacts affects coupling, and would have been motivated to space such low speed leads in order to minimize cross-talk and/or maintain impedance accuracy of the contacts.

d) “wherein the high-speed electronic circuitry is connected with the second ground plane and is electrically connected with the second set of electrical contacts that are spaced for connection with the high speed electronic circuitry.”

200. Kramer discloses in Figure 6, shown above, analog circuitry 73 connected with a first portion of ground plane 74 that is separated from the remaining ground plane 74 outside the analog area. (Ex.1007, FIG. 6) Kramer discloses the analog circuitry 73 operates at higher speeds (e.g., 4.25 Gb/s and above). (*Id.*, 1:35-

42) However, Kramer does not explicitly disclose “the second set of electrical contacts that are spaced for connection with the high speed circuitry”.

201. However, Sutardja shows in Figure 10A, shown above, that the spacing for the high speed leads (second set of electrical contacts) is greater than spacing for low speed leads (first set of electrical contacts). Sutardja further discloses spacing may be irregular to “increase or decrease coupling”. (Ex. 1012, ¶ 0139)

202. As such, a person of ordinary skill in the art implementing the IC package of Okabe-AAPA would have good reason to look to Kramer and Sutardja as they are all in the field of IC packaging. Moreover, a person of ordinary skill in the art would have understood that a particular spacing for Kramer’s high speed contacts would affect a particular impedance and minimize cross talk, and thus it would have been straightforward to modify spacing of the high speed contacts as taught by Sutardja.

I. Okabe in Combination with Applicant’s Admitted Prior Art (AAPA), Conn, Kramer and Sutardja Disclose or Suggest the Features of Claim 14.

203. It is my opinion that Okabe in view of Applicant’s Admitted Prior Art, Conn, Kramer, and Sutardja discloses or suggests each and every element of dependent claim 14.

1. Claim 14

a) “An IC package as recited in claim 12, wherein the die arrangement comprises a stacked die arrangement”

204. As discussed in Section X.C.2(a) above, Okabe-AAPA discloses an IC package with an IC die. However, Okabe-AAPA does not explicitly disclose “a stacked die arrangement”.

205. However, Conn illustrates a stacked die arrangement in Figure 2 shown below. For example, analog power regulator die 73 is stacked on FPGA die 49. (Ex. 1013, 1:35-54)

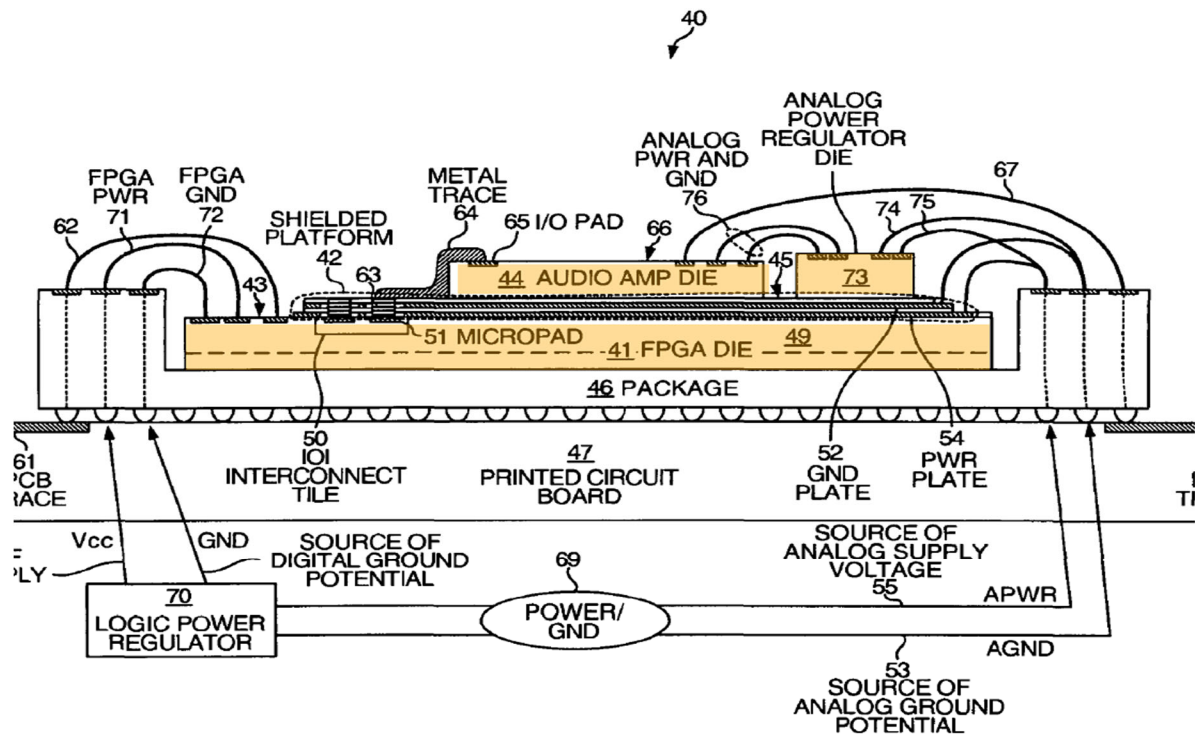


FIG. 2

(*Id.*, FIG. 2 (annotated).)

b) “wherein at least one die has high-speed electronic circuitry and wherein at least one die has low-speed electronic circuitry;”

206. Conn discloses in an example that the analog power regulator die 73 operates at a lower frequency than the underlying FPGA die 49 (*Id.*, 6:30-50) As such, a person of ordinary skill in the art would have understood that a die being capable of operating at a higher frequency than the other would indicate one die having high-speed electronic circuitry and the other die having low speed electronic circuitry.

c) “wherein the low-speed electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced for connection with the low-speed connection with the low speed electronic circuitry; and”

207. Kramer discloses in Figure 6, shown below, an IC 72 is connected with a first portion of ground plane 74 that is separated from the remaining ground plane 74 outside the analog area. Kramer further discloses the analog circuitry operates at higher speeds (e.g., 4.25 Gb/s and above). (Ex. 1007, 1:35-42) Kramer also discloses the IC 72 is connected to electrical contacts 77 outside the analog area.

208. A person of ordinary skill in the art would have understood the IC operating at lower speeds than the analog circuit 73 would be low speed circuitry, and that the IC 72 being connected to the portion of the ground plane 74 outside the

analog area would be a first ground plane. Kramer does not explicitly disclose the contacts 77 are “spaced for connection with low speed electronic circuitry”.

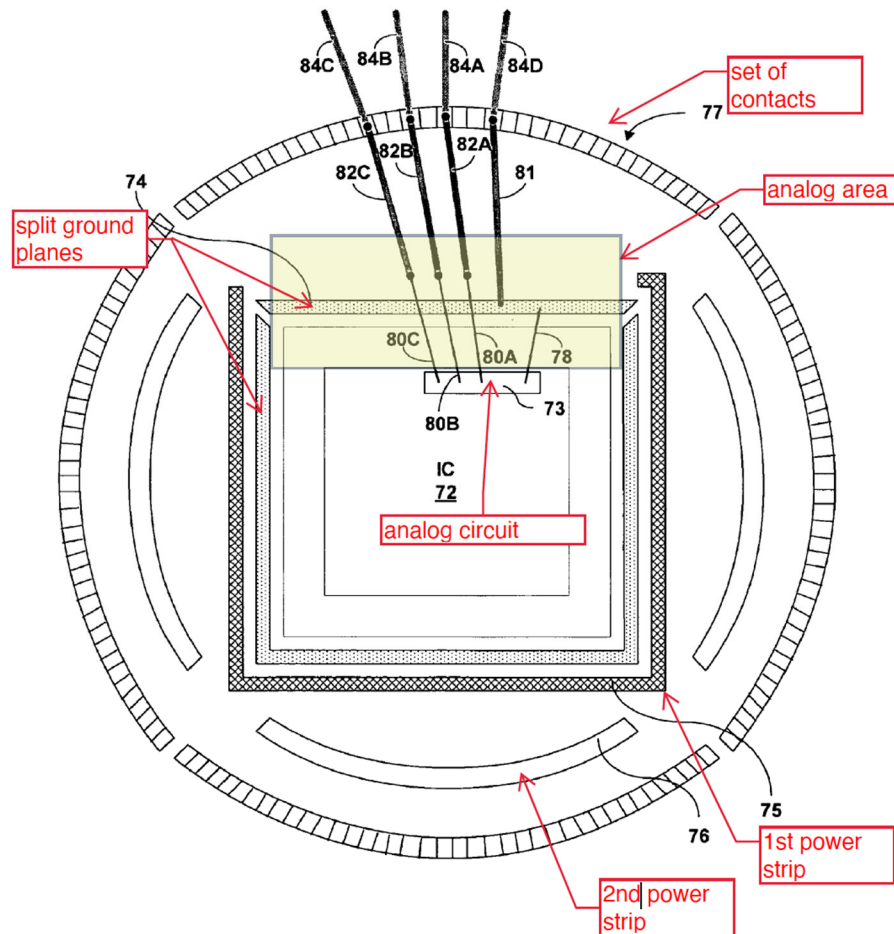


FIG. 6

(*Id.*, FIG. 6 (annotated).)

209. However, Sutardja clearly shows in Figure 10A that low speed leads are spaced closer together than high speed leads. Sutardja further discloses that spacing

between the leads may be changed to “increase or decrease coupling. (Ex. 1012, ¶ [0139])

210. As such, a person of ordinary skill in the art would have understood spacing of lines and contacts affects coupling, and would have been motivated to space such low speed leads in order to minimize cross-talk and/or maintain impedance accuracy of the contacts.

d) “wherein the high-speed electronic circuitry is electronic connected with the second ground plane and is electrically connected with the second set of electrical contacts that are spaced for connection with the high speed electronic circuitry.”

211. Kramer discloses in Figure 6, shown above, analog circuitry 73 connected with a first portion of ground plane 74 that is separated from the remaining ground plane 74 outside the analog area. Kramer discloses the analog circuitry 73 operates at higher speeds (e.g., 4.25 Gb/s and above). However, Kramer does not explicitly disclose “the second set of electrical contacts that are spaced for connection with the high speed circuitry”.

212. However, Sutardja shows in Figure 10A, shown above, that the spacing for the high speed leads (second set of electrical contacts) is greater than spacing for low speed leads (first set of electrical contacts). Sutardja further discloses spacing may be irregular to “increase or decrease coupling”. (Ex. 1012, ¶ [0139])

213. As such, a person of ordinary skill in the art implementing the IC package of Okabe-AAPA would have good reason to look to Conn, Kramer and Sutardja as they are all in the field of IC packaging. Moreover, a person of ordinary skill in the art would have understood that a particular spacing for Kramer's high speed contacts would affect a particular impedance and minimize cross talk, and thus it would have been straightforward to modify spacing of the high speed contacts as taught by Sutardja.

214. A person of ordinary skill in the art implementing the IC package of Okabe-AAPA, would have good reason to look at Conn, Sutardja, and Kramer as they all are in the similar fields of IC packaging, having multi-layered substrates and/or spacing of signal lines.

215. Such an implementation would have simply been the application of a known device (IC package with multiple IC dies) to a similar device (stacked IC dies) and would have produce predictable results. Therefore, in my opinion, the Okabe-AAPA-Conn-Sutardja-Kramer combination discloses or suggests this claim feature.

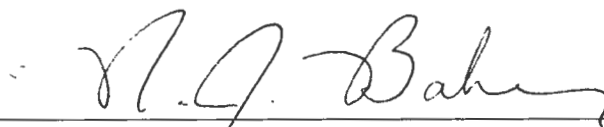
XI. CONCLUSION

216. In summary, it is my opinion that all of the features recited in claims 1-14 of the '091 Patent are disclosed or suggested by the prior art.

Declaration of Dr. R. Jacob Baker
U.S. Patent No. 7,646,091

217. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: November 7, 2023



R. Jacob Baker, Ph.D., P.E.