UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	REQUEST ID
11/399,723	7646091	2826	182980

PAIR Correspondence Address/Fee Address Change

The following fields have been changed to Customer Number 22186 on 01/30/2023 via Private PAIR in view of the certification copied below that authorized the change.

- Maintenance Fee Address

The address for Customer Number 22186 is:
22186
MENDELSOHN DUNLEAVY, P.C.
1500 JOHN F. KENNEDY BLVD., SUITE 910
PHILADELPHIA, PA 19102

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

An attorney or Agent of Record registered to practice before the Patent and Trademark Office who has been given power of attorney in this application

Signature:	/Steve Mendelsohn/
Name:	Steve Mendelsohn
Registration Number:	35951

AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court District of Delaware on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	9/30/2022	District of Delaware

PLAINTIFF	DEFENDANT
BELL SEMICONDUCTOR, LLC	MICRON TECHNOLOGY, INC., et al.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 6,818,953	11/16/2004	BELL SEMICONDUCTOR, LLC
2	US 8,049,340	11/1/2011	BELL SEMICONDUCTOR, LLC
3	US 8,288,269	10/16/2012	BELL SEMICONDUCTOR, LLC
4	US 8,319,343	11/27/2012	BELL SEMICONDUCTOR, LLC
5	US 7,345,245	3/18/2008	BELL SEMICONDUCTOR, LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY			
9/30/2022	☐ Amendment	☐ Answer	☐ Cross Bill	☑ Other Pleading

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 7,646,091	1/12/2010	BELL SEMICONDUCTOR, LLC
2			
3			
4			
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Central District of California on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	8/12/2022	Central District of California

PLAINTIFF	DEFENDANT
BELL SEMICONDUCTOR, LLC	NVIDIA CORPORATION; DELL TECHNOLOGIES INC.; G.B.T. INC.; GIGA-BYTE TECHNOLOGY CO., LTD.; MICRO-STAR INTERNATIONAL CO., LTD.; NINTENDO OF AMERICA INC.; BEST BUY CO. INC.; AND AMAZON.COM, INC.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 8,049,340	11/1/2011	BELL SEMICONDUCTOR, LLC
2	US 8,288,269	10/16/2012	BELL SEMICONDUCTOR, LLC
3	US 7,646,091	1/12/2010	BELL SEMICONDUCTOR, LLC
4	US 7,345,245	3/18/2008	BELL SEMICONDUCTOR, LLC
5	US 7,180,011	2/20/2007	BELL SEMICONDUCTOR, LLC

In the above---entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above---entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1---Upon initiation of action, mail this copy to Director Copy 3---Upon termination of action, mail this copy to Director
Copy 2---Upon filing document adding patent(s), mail this copy to Director Copy 4---Case file copy

AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Central District of California on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	8/12/2022	Central District of California

PLAINTIFF	DEFENDANT
BELL SEMICONDUCTOR, LLC	QUALCOMM INC.; QUALCOMM TECHNOLOGIES, INC.; ARUBA NETWORKS, LLC; COMMSCOPE TECHNOLOGIES LLC; HEWLETT PACKARD ENTERPRISE COMPANY; LINKSYS USA, INC.; NETGEAR, INC.; TP-LINK USA CORPORATION

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 7,646,091	1/12/2010	BELL SEMICONDUCTOR, LLC
2	US 7,345,245	3/18/2008	BELL SEMICONDUCTOR, LLC
3	US 8,288,269	10/16/2012	BELL SEMICONDUCTOR, LLC
4	US 8,049,340	11/1/2011	BELL SEMICONDUCTOR, LLC
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT7282532

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
CORTLAND CAPITAL MARKET SERVICES LLC	04/01/2022

RECEIVING PARTY DATA

Name:	HILCO PATENT ACQUISITION 56, LLC
Street Address:	401 N. MICHIGAN AVE., SUITE 1630
City:	CHICAGO
State/Country:	ILLINOIS
Postal Code:	60611
Name:	BELL SEMICONDUCTOR, LLC
Street Address:	401 N. MICHIGAN AVE., SUITE 1630
City:	CHICAGO
State/Country:	ILLINOIS
Postal Code:	60611
Name:	BELL NORTHERN RESEARCH, LLC
Street Address:	401 N. MICHIGAN AVE., SUITE 1630
City:	CHICAGO
State/Country:	ILLINOIS
Postal Code:	60611

PROPERTY NUMBERS Total: 556

Property Type	Number
Patent Number:	6103615
Patent Number:	6278129
Patent Number:	5776551
Patent Number:	5786073
Patent Number:	5911112
Patent Number:	5793104
Patent Number:	5970321
Patent Number:	5869869
Patent Number:	5955762
Patent Number:	5885855

Property Type	Number
Patent Number:	5952726
Patent Number:	5700723
Patent Number:	5784780
Patent Number:	5637920
Patent Number:	5814536
Patent Number:	5869891
Patent Number:	5827777
Patent Number:	5600182
Patent Number:	5872026
Patent Number:	5739584
Patent Number:	6597189
Patent Number:	RE41516
Patent Number:	6771085
Patent Number:	5537342
Patent Number:	5663872
Patent Number:	8049340
Patent Number:	8288269
Patent Number:	7430700
Patent Number:	7203877
Patent Number:	7960812
Patent Number:	7456716
Patent Number:	7109589
Patent Number:	7465655
Patent Number:	6087732
Patent Number:	6187658
Patent Number:	6818996
Patent Number:	6369448
Patent Number:	6558978
Patent Number:	7224047
Patent Number:	7541669
Patent Number:	6319617
Patent Number:	6306516
Patent Number:	6137168
Patent Number:	5410451
Patent Number:	5898575
Patent Number:	5896651
Patent Number:	5923538
Patent Number:	6008991

Property Type	Number
Patent Number:	7919354
Patent Number:	7405476
Patent Number:	6518193
Patent Number:	6313519
Patent Number:	5744084
Patent Number:	5927505
Patent Number:	6678950
Patent Number:	5990543
Patent Number:	6043100
Patent Number:	6492253
Patent Number:	6054767
Patent Number:	5300815
Patent Number:	5635424
Patent Number:	5399898
Patent Number:	5834799
Patent Number:	5248903
Patent Number:	5284797
Patent Number:	5565385
Patent Number:	5821624
Patent Number:	5744856
Patent Number:	5410805
Patent Number:	5434750
Patent Number:	5744858
Patent Number:	5557150
Patent Number:	5299730
Patent Number:	5168346
Patent Number:	5569963
Patent Number:	5347162
Patent Number:	5594626
Patent Number:	5340772
Patent Number:	5729894
Patent Number:	5329157
Patent Number:	5441917
Patent Number:	5532934
Patent Number:	5111279
Patent Number:	5489804
Patent Number:	5404047
Patent Number:	5262927

Property Type	Number
Patent Number:	5468681
Patent Number:	8507317
Patent Number:	7952206
Patent Number:	5700715
Patent Number:	7053639
Patent Number:	6927079
Patent Number:	7456498
Patent Number:	7550839
Patent Number:	8324019
Patent Number:	8404960
Patent Number:	8653357
Patent Number:	8258016
Patent Number:	7498664
Patent Number:	7646091
Patent Number:	8129759
Patent Number:	8013428
Patent Number:	7352062
Patent Number:	6825556
Patent Number:	8319343
Patent Number:	6991147
Patent Number:	6670214
Patent Number:	6858930
Patent Number:	6680532
Patent Number:	8084857
Patent Number:	7675168
Patent Number:	6972494
Patent Number:	7541674
Patent Number:	8025201
Patent Number:	7074705
Patent Number:	6639321
Patent Number:	6806119
Patent Number:	7582938
Patent Number:	7948036
Patent Number:	8269280
Patent Number:	6979869
Patent Number:	6790757
Patent Number:	5986343
Patent Number:	6207547

Property Type	Number
Patent Number:	7632717
Patent Number:	7423341
Patent Number:	6617181
Patent Number:	6710453
Patent Number:	6118177
Patent Number:	6681482
Patent Number:	6068130
Patent Number:	6554137
Patent Number:	6077725
Patent Number:	5564617
Patent Number:	6409829
Patent Number:	6727567
Patent Number:	6675450
Patent Number:	6465884
Patent Number:	6833286
Patent Number:	6849936
Patent Number:	6781150
Patent Number:	6998638
Patent Number:	6563198
Patent Number:	6281590
Patent Number:	6465336
Patent Number:	7429502
Patent Number:	7327029
Patent Number:	7301231
Patent Number:	7115985
Patent Number:	7443042
Patent Number:	7086148
Patent Number:	7637414
Patent Number:	6342442
Patent Number:	7009299
Patent Number:	6881613
Patent Number:	7224076
Patent Number:	6441473
Patent Number:	7705473
Patent Number:	7056819
Patent Number:	7271485
Patent Number:	7709861
Patent Number:	6136620

Property Type	Number
Patent Number:	5751065
Patent Number:	6335491
Patent Number:	6618938
Patent Number:	5435482
Patent Number:	6088914
Patent Number:	5989937
Patent Number:	8502372
Patent Number:	8101871
Patent Number:	6573113
Patent Number:	6061889
Patent Number:	6266249
Patent Number:	6057594
Patent Number:	6002169
Patent Number:	6143586
Patent Number:	6861748
Patent Number:	6114761
Patent Number:	6445066
Patent Number:	6040632
Patent Number:	6297550
Patent Number:	6083848
Patent Number:	6126063
Patent Number:	5835355
Patent Number:	6081997
Patent Number:	5909056
Patent Number:	5907189
Patent Number:	5992012
Patent Number:	5998242
Patent Number:	6114189
Patent Number:	5834839
Patent Number:	6011304
Patent Number:	6069027
Patent Number:	5972738
Patent Number:	5841191
Patent Number:	5814881
Patent Number:	5977622
Patent Number:	5940271
Patent Number:	5973393
Patent Number:	5899737

Property Type	Number
Patent Number:	5959320
Patent Number:	5723369
Patent Number:	6020221
Patent Number:	5731223
Patent Number:	5801072
Patent Number:	5780924
Patent Number:	5695593
Patent Number:	5719733
Patent Number:	5621616
Patent Number:	8115321
Patent Number:	7479703
Patent Number:	7298036
Patent Number:	7379836
Patent Number:	6777971
Patent Number:	7776648
Patent Number:	7394028
Patent Number:	6960836
Patent Number:	7157361
Patent Number:	6282100
Patent Number:	7148535
Patent Number:	6828682
Patent Number:	7082585
Patent Number:	5898223
Patent Number:	6175158
Patent Number:	6911736
Patent Number:	5918794
Patent Number:	5583285
Patent Number:	5607882
Patent Number:	6768386
Patent Number:	6867480
Patent Number:	7173328
Patent Number:	6654248
Patent Number:	7041516
Patent Number:	6433565
Patent Number:	6861343
Patent Number:	6734697
Patent Number:	6559670
Patent Number:	6431432

Property Type	Number
Patent Number:	6555914
Patent Number:	7566953
Patent Number:	6320127
Patent Number:	6347291
Patent Number:	6133064
Patent Number:	6397944
Patent Number:	6519844
Patent Number:	6411114
Patent Number:	6110815
Patent Number:	5981311
Patent Number:	6828643
Patent Number:	5903050
Patent Number:	6117695
Patent Number:	6459049
Patent Number:	6068727
Patent Number:	6118180
Patent Number:	5949137
Patent Number:	5909057
Patent Number:	6002171
Patent Number:	6111313
Patent Number:	5841198
Patent Number:	6479319
Patent Number:	6531932
Patent Number:	5610442
Patent Number:	5644102
Patent Number:	5686764
Patent Number:	5761048
Patent Number:	5716493
Patent Number:	5786631
Patent Number:	5691568
Patent Number:	5777383
Patent Number:	5465470
Patent Number:	6518161
Patent Number:	5632437
Patent Number:	5598775
Patent Number:	5818102
Patent Number:	6078502
Patent Number:	5767580

Property Type	Number
Patent Number:	7750460
Patent Number:	5831836
Patent Number:	8350375
Patent Number:	6586825
Patent Number:	7737564
Patent Number:	7370257
Patent Number:	6396699
Patent Number:	7557303
Patent Number:	7968999
Patent Number:	6496374
Patent Number:	7804167
Patent Number:	7117467
Patent Number:	7081672
Patent Number:	7235889
Patent Number:	7528616
Patent Number:	7319272
Patent Number:	7354790
Patent Number:	7491579
Patent Number:	7145232
Patent Number:	6847123
Patent Number:	7096748
Patent Number:	7436060
Patent Number:	7328830
Patent Number:	6369596
Patent Number:	7098528
Patent Number:	7368326
Patent Number:	7023087
Patent Number:	7633152
Patent Number:	8183698
Patent Number:	6759860
Patent Number:	7433192
Patent Number:	7030472
Patent Number:	7504728
Patent Number:	6954082
Patent Number:	7777333
Patent Number:	6369444
Patent Number:	6160715
Patent Number:	6933602

Property Type	Number
Patent Number:	7791210
Patent Number:	6371665
Patent Number:	7345245
Patent Number:	6963129
Patent Number:	6178088
Patent Number:	6130141
Patent Number:	6015652
Patent Number:	7221173
Patent Number:	5696405
Patent Number:	6465882
Patent Number:	5608262
Patent Number:	6683384
Patent Number:	6043670
Patent Number:	6480657
Patent Number:	7009282
Patent Number:	6232212
Patent Number:	7132735
Patent Number:	6190940
Patent Number:	5627407
Patent Number:	5741430
Patent Number:	6075427
Patent Number:	6743979
Patent Number:	6372600
Patent Number:	6351033
Patent Number:	5837380
Patent Number:	5667132
Patent Number:	6199464
Patent Number:	6154370
Patent Number:	6232047
Patent Number:	7023225
Patent Number:	5505367
Patent Number:	6798035
Patent Number:	6744130
Patent Number:	6251705
Patent Number:	6509642
Patent Number:	6678167
Patent Number:	6297551
Patent Number:	6790760

Property Type	Number
Patent Number:	6825563
Patent Number:	6342399
Patent Number:	6437990
Patent Number:	6836026
Patent Number:	6591410
Patent Number:	6245993
Patent Number:	6891392
Patent Number:	7190082
Patent Number:	6801437
Patent Number:	6605951
Patent Number:	6781228
Patent Number:	6943446
Patent Number:	6744081
Patent Number:	6798069
Patent Number:	6717423
Patent Number:	6963138
Patent Number:	6648064
Patent Number:	6603201
Patent Number:	6403399
Patent Number:	6951000
Patent Number:	6777314
Patent Number:	6777803
Patent Number:	6815812
Patent Number:	6605954
Patent Number:	6861183
Patent Number:	6700207
Patent Number:	6674176
Patent Number:	6962437
Patent Number:	6769923
Patent Number:	6671865
Patent Number:	6429534
Patent Number:	6573523
Patent Number:	6623992
Patent Number:	6706622
Patent Number:	6590409
Patent Number:	5646828
Patent Number:	5965197
Patent Number:	6074897

Property Type	Number
Patent Number:	7541220
Patent Number:	5834792
Patent Number:	6472304
Patent Number:	6657870
Patent Number:	6475828
Patent Number:	6279889
Patent Number:	6373142
Patent Number:	6441499
Patent Number:	6534968
Patent Number:	6306751
Patent Number:	6425179
Patent Number:	6407462
Patent Number:	6465338
Patent Number:	6115910
Patent Number:	6449748
Patent Number:	6395097
Patent Number:	6603200
Patent Number:	6294840
Patent Number:	6166434
Patent Number:	6617866
Patent Number:	6285077
Patent Number:	6496081
Patent Number:	6225690
Patent Number:	6328347
Patent Number:	6150729
Patent Number:	6127726
Patent Number:	6225695
Patent Number:	6150175
Patent Number:	6242814
Patent Number:	6261870
Patent Number:	6759921
Patent Number:	8350379
Patent Number:	5731635
Patent Number:	7993981
Patent Number:	8384205
Patent Number:	7667321
Patent Number:	6894400
Patent Number:	7745927

Property Type	Number
Patent Number:	7041561
Patent Number:	7075174
Patent Number:	6987052
Patent Number:	6740222
Patent Number:	6313999
Patent Number:	6239382
Patent Number:	6153506
Patent Number:	5936849
Patent Number:	6057700
Patent Number:	5975408
Patent Number:	5975836
Patent Number:	5719449
Patent Number:	5672913
Patent Number:	5501777
Patent Number:	7554133
Patent Number:	8547681
Patent Number:	8134232
Patent Number:	7724023
Patent Number:	8378485
Patent Number:	8580621
Patent Number:	7787252
Patent Number:	8334467
Patent Number:	8869389
Patent Number:	8370777
Patent Number:	8125091
Patent Number:	8653375
Patent Number:	7671450
Patent Number:	7727781
Patent Number:	7724359
Patent Number:	8742535
Patent Number:	9613847
Patent Number:	7671436
Patent Number:	8987137
Patent Number:	7888257
Patent Number:	9054064
Patent Number:	8492911
Patent Number:	7800879
Patent Number:	7973544

Property Type	Number
Patent Number:	7479695
Patent Number:	8664759
Patent Number:	7005880
Patent Number:	7221042
Patent Number:	7956451
Patent Number:	7408246
Patent Number:	8133799
Patent Number:	7598602
Patent Number:	7923347
Patent Number:	7242090
Patent Number:	7235422
Patent Number:	7164200
Patent Number:	7429703
Patent Number:	7367486
Patent Number:	7314781
Patent Number:	7122892
Patent Number:	7009305
Patent Number:	6628001
Patent Number:	6476472
Patent Number:	6358779
Patent Number:	6412680
Patent Number:	6559535
Patent Number:	6417087
Patent Number:	6309097
Patent Number:	6276593
Patent Number:	6043876
Patent Number:	6140710
Patent Number:	6180241
Patent Number:	6145385
Patent Number:	6028772
Patent Number:	6110576
Patent Number:	5955683
Patent Number:	5904859
Patent Number:	6034441
Patent Number:	5897333
Patent Number:	5783465
Patent Number:	5778913
Patent Number:	5747982

Property Type	Number
Patent Number:	6125042
Patent Number:	5735698
Patent Number:	5622305
Patent Number:	5773322
Patent Number:	5646451
Patent Number:	8222745
Patent Number:	5619068
Application Number:	08989098
Application Number:	08653591
Application Number:	07856905
Application Number:	10921497
Application Number:	09618143
Application Number:	08427674
Application Number:	08646014
Application Number:	08427306
Application Number:	10322974
Application Number:	07914621
Application Number:	10694486
Application Number:	08688148
Application Number:	08270123
Application Number:	08015947
Application Number:	07938690
Application Number:	07400572
Application Number:	08105269
Application Number:	07917894
Application Number:	08382147
Application Number:	07993188
Application Number:	07969862
Application Number:	08331263
Application Number:	13934110
Application Number:	08259439
Application Number:	61055505
Application Number:	10951430
Application Number:	13552266
Application Number:	13656092
Application Number:	10939292
Application Number:	10742916
Application Number:	11012838

Property Type	Number
Application Number:	09920144
Application Number:	10755616
Application Number:	08936259
Application Number:	08578049
Application Number:	61377171
Application Number:	13344207
Application Number:	60147106
Application Number:	60095397
Application Number:	60714214
Application Number:	60655816
Application Number:	60535839
Application Number:	60435033
Application Number:	60014182
Application Number:	14678223

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 5749031499
Email: jgammon@hilcoglobal.com
Correspondent Name: JOSHUA GAMMON
Address Line 1: 401 N. MICHIGAN AVE.
Address Line 2: SUITE 1630
Address Line 4: CHICAGO, ILLINOIS 60611

NAME OF SUBMITTER:	JOSHUA GAMMON
SIGNATURE:	//Joshua Gammon//
DATE SIGNED:	04/15/2022
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 215
source=Release of Security Interest - FULLY EXECUTED#page1.tif
source=Release of Security Interest - FULLY EXECUTED#page2.tif
source=Release of Security Interest - FULLY EXECUTED#page3.tif
source=Release of Security Interest - FULLY EXECUTED#page4.tif
source=Release of Security Interest - FULLY EXECUTED#page5.tif
source=Release of Security Interest - FULLY EXECUTED#page6.tif
source=Release of Security Interest - FULLY EXECUTED#page7.tif
source=Release of Security Interest - FULLY EXECUTED#page8.tif
source=Release of Security Interest - FULLY EXECUTED#page9.tif
source=Release of Security Interest - FULLY EXECUTED#page10.tif
source=Release of Security Interest - FULLY EXECUTED#page11.tif

source=Release of Security Interest - FULLY EXECUTED#page12.tif
source=Release of Security Interest - FULLY EXECUTED#page13.tif
source=Release of Security Interest - FULLY EXECUTED#page14.tif
source=Release of Security Interest - FULLY EXECUTED#page15.tif
source=Release of Security Interest - FULLY EXECUTED#page16.tif
source=Release of Security Interest - FULLY EXECUTED#page17.tif
source=Release of Security Interest - FULLY EXECUTED#page18.tif
source=Release of Security Interest - FULLY EXECUTED#page19.tif
source=Release of Security Interest - FULLY EXECUTED#page20.tif
source=Release of Security Interest - FULLY EXECUTED#page21.tif
source=Release of Security Interest - FULLY EXECUTED#page22.tif
source=Release of Security Interest - FULLY EXECUTED#page23.tif
source=Release of Security Interest - FULLY EXECUTED#page24.tif
source=Release of Security Interest - FULLY EXECUTED#page25.tif
source=Release of Security Interest - FULLY EXECUTED#page26.tif
source=Release of Security Interest - FULLY EXECUTED#page27.tif
source=Release of Security Interest - FULLY EXECUTED#page28.tif
source=Release of Security Interest - FULLY EXECUTED#page29.tif
source=Release of Security Interest - FULLY EXECUTED#page30.tif
source=Release of Security Interest - FULLY EXECUTED#page31.tif
source=Release of Security Interest - FULLY EXECUTED#page32.tif
source=Release of Security Interest - FULLY EXECUTED#page33.tif
source=Release of Security Interest - FULLY EXECUTED#page34.tif
source=Release of Security Interest - FULLY EXECUTED#page35.tif
source=Release of Security Interest - FULLY EXECUTED#page36.tif
source=Release of Security Interest - FULLY EXECUTED#page37.tif
source=Release of Security Interest - FULLY EXECUTED#page38.tif
source=Release of Security Interest - FULLY EXECUTED#page39.tif
source=Release of Security Interest - FULLY EXECUTED#page40.tif
source=Release of Security Interest - FULLY EXECUTED#page41.tif
source=Release of Security Interest - FULLY EXECUTED#page42.tif
source=Release of Security Interest - FULLY EXECUTED#page43.tif
source=Release of Security Interest - FULLY EXECUTED#page44.tif
source=Release of Security Interest - FULLY EXECUTED#page45.tif
source=Release of Security Interest - FULLY EXECUTED#page46.tif
source=Release of Security Interest - FULLY EXECUTED#page47.tif
source=Release of Security Interest - FULLY EXECUTED#page48.tif
source=Release of Security Interest - FULLY EXECUTED#page49.tif
source=Release of Security Interest - FULLY EXECUTED#page50.tif
source=Release of Security Interest - FULLY EXECUTED#page51.tif
source=Release of Security Interest - FULLY EXECUTED#page52.tif
source=Release of Security Interest - FULLY EXECUTED#page53.tif
source=Release of Security Interest - FULLY EXECUTED#page54.tif
source=Release of Security Interest - FULLY EXECUTED#page55.tif
source=Release of Security Interest - FULLY EXECUTED#page56.tif
source=Release of Security Interest - FULLY EXECUTED#page57.tif
source=Release of Security Interest - FULLY EXECUTED#page58.tif
source=Release of Security Interest - FULLY EXECUTED#page59.tif

source=Release of Security Interest - FULLY EXECUTED#page60.tif
source=Release of Security Interest - FULLY EXECUTED#page61.tif
source=Release of Security Interest - FULLY EXECUTED#page62.tif
source=Release of Security Interest - FULLY EXECUTED#page63.tif
source=Release of Security Interest - FULLY EXECUTED#page64.tif
source=Release of Security Interest - FULLY EXECUTED#page65.tif
source=Release of Security Interest - FULLY EXECUTED#page66.tif
source=Release of Security Interest - FULLY EXECUTED#page67.tif
source=Release of Security Interest - FULLY EXECUTED#page68.tif
source=Release of Security Interest - FULLY EXECUTED#page69.tif
source=Release of Security Interest - FULLY EXECUTED#page70.tif
source=Release of Security Interest - FULLY EXECUTED#page71.tif
source=Release of Security Interest - FULLY EXECUTED#page72.tif
source=Release of Security Interest - FULLY EXECUTED#page73.tif
source=Release of Security Interest - FULLY EXECUTED#page74.tif
source=Release of Security Interest - FULLY EXECUTED#page75.tif
source=Release of Security Interest - FULLY EXECUTED#page76.tif
source=Release of Security Interest - FULLY EXECUTED#page77.tif
source=Release of Security Interest - FULLY EXECUTED#page78.tif
source=Release of Security Interest - FULLY EXECUTED#page79.tif
source=Release of Security Interest - FULLY EXECUTED#page80.tif
source=Release of Security Interest - FULLY EXECUTED#page81.tif
source=Release of Security Interest - FULLY EXECUTED#page82.tif
source=Release of Security Interest - FULLY EXECUTED#page83.tif
source=Release of Security Interest - FULLY EXECUTED#page84.tif
source=Release of Security Interest - FULLY EXECUTED#page85.tif
source=Release of Security Interest - FULLY EXECUTED#page86.tif
source=Release of Security Interest - FULLY EXECUTED#page87.tif
source=Release of Security Interest - FULLY EXECUTED#page88.tif
source=Release of Security Interest - FULLY EXECUTED#page89.tif
source=Release of Security Interest - FULLY EXECUTED#page90.tif
source=Release of Security Interest - FULLY EXECUTED#page91.tif
source=Release of Security Interest - FULLY EXECUTED#page92.tif
source=Release of Security Interest - FULLY EXECUTED#page93.tif
source=Release of Security Interest - FULLY EXECUTED#page94.tif
source=Release of Security Interest - FULLY EXECUTED#page95.tif
source=Release of Security Interest - FULLY EXECUTED#page96.tif
source=Release of Security Interest - FULLY EXECUTED#page97.tif
source=Release of Security Interest - FULLY EXECUTED#page98.tif
source=Release of Security Interest - FULLY EXECUTED#page99.tif
source=Release of Security Interest - FULLY EXECUTED#page100.tif
source=Release of Security Interest - FULLY EXECUTED#page101.tif
source=Release of Security Interest - FULLY EXECUTED#page102.tif
source=Release of Security Interest - FULLY EXECUTED#page103.tif
source=Release of Security Interest - FULLY EXECUTED#page104.tif
source=Release of Security Interest - FULLY EXECUTED#page105.tif
source=Release of Security Interest - FULLY EXECUTED#page106.tif
source=Release of Security Interest - FULLY EXECUTED#page107.tif

source=Release of Security Interest - FULLY EXECUTED#page108.tif
source=Release of Security Interest - FULLY EXECUTED#page109.tif
source=Release of Security Interest - FULLY EXECUTED#page110.tif
source=Release of Security Interest - FULLY EXECUTED#page111.tif
source=Release of Security Interest - FULLY EXECUTED#page112.tif
source=Release of Security Interest - FULLY EXECUTED#page113.tif
source=Release of Security Interest - FULLY EXECUTED#page114.tif
source=Release of Security Interest - FULLY EXECUTED#page115.tif
source=Release of Security Interest - FULLY EXECUTED#page116.tif
source=Release of Security Interest - FULLY EXECUTED#page117.tif
source=Release of Security Interest - FULLY EXECUTED#page118.tif
source=Release of Security Interest - FULLY EXECUTED#page119.tif
source=Release of Security Interest - FULLY EXECUTED#page120.tif
source=Release of Security Interest - FULLY EXECUTED#page121.tif
source=Release of Security Interest - FULLY EXECUTED#page122.tif
source=Release of Security Interest - FULLY EXECUTED#page123.tif
source=Release of Security Interest - FULLY EXECUTED#page124.tif
source=Release of Security Interest - FULLY EXECUTED#page125.tif
source=Release of Security Interest - FULLY EXECUTED#page126.tif
source=Release of Security Interest - FULLY EXECUTED#page127.tif
source=Release of Security Interest - FULLY EXECUTED#page128.tif
source=Release of Security Interest - FULLY EXECUTED#page129.tif
source=Release of Security Interest - FULLY EXECUTED#page130.tif
source=Release of Security Interest - FULLY EXECUTED#page131.tif
source=Release of Security Interest - FULLY EXECUTED#page132.tif
source=Release of Security Interest - FULLY EXECUTED#page133.tif
source=Release of Security Interest - FULLY EXECUTED#page134.tif
source=Release of Security Interest - FULLY EXECUTED#page135.tif
source=Release of Security Interest - FULLY EXECUTED#page136.tif
source=Release of Security Interest - FULLY EXECUTED#page137.tif
source=Release of Security Interest - FULLY EXECUTED#page138.tif
source=Release of Security Interest - FULLY EXECUTED#page139.tif
source=Release of Security Interest - FULLY EXECUTED#page140.tif
source=Release of Security Interest - FULLY EXECUTED#page141.tif
source=Release of Security Interest - FULLY EXECUTED#page142.tif
source=Release of Security Interest - FULLY EXECUTED#page143.tif
source=Release of Security Interest - FULLY EXECUTED#page144.tif
source=Release of Security Interest - FULLY EXECUTED#page145.tif
source=Release of Security Interest - FULLY EXECUTED#page146.tif
source=Release of Security Interest - FULLY EXECUTED#page147.tif
source=Release of Security Interest - FULLY EXECUTED#page148.tif
source=Release of Security Interest - FULLY EXECUTED#page149.tif
source=Release of Security Interest - FULLY EXECUTED#page150.tif
source=Release of Security Interest - FULLY EXECUTED#page151.tif
source=Release of Security Interest - FULLY EXECUTED#page152.tif
source=Release of Security Interest - FULLY EXECUTED#page153.tif
source=Release of Security Interest - FULLY EXECUTED#page154.tif
source=Release of Security Interest - FULLY EXECUTED#page155.tif

source=Release of Security Interest - FULLY EXECUTED#page156.tif
source=Release of Security Interest - FULLY EXECUTED#page157.tif
source=Release of Security Interest - FULLY EXECUTED#page158.tif
source=Release of Security Interest - FULLY EXECUTED#page159.tif
source=Release of Security Interest - FULLY EXECUTED#page160.tif
source=Release of Security Interest - FULLY EXECUTED#page161.tif
source=Release of Security Interest - FULLY EXECUTED#page162.tif
source=Release of Security Interest - FULLY EXECUTED#page163.tif
source=Release of Security Interest - FULLY EXECUTED#page164.tif
source=Release of Security Interest - FULLY EXECUTED#page165.tif
source=Release of Security Interest - FULLY EXECUTED#page166.tif
source=Release of Security Interest - FULLY EXECUTED#page167.tif
source=Release of Security Interest - FULLY EXECUTED#page168.tif
source=Release of Security Interest - FULLY EXECUTED#page169.tif
source=Release of Security Interest - FULLY EXECUTED#page170.tif
source=Release of Security Interest - FULLY EXECUTED#page171.tif
source=Release of Security Interest - FULLY EXECUTED#page172.tif
source=Release of Security Interest - FULLY EXECUTED#page173.tif
source=Release of Security Interest - FULLY EXECUTED#page174.tif
source=Release of Security Interest - FULLY EXECUTED#page175.tif
source=Release of Security Interest - FULLY EXECUTED#page176.tif
source=Release of Security Interest - FULLY EXECUTED#page177.tif
source=Release of Security Interest - FULLY EXECUTED#page178.tif
source=Release of Security Interest - FULLY EXECUTED#page179.tif
source=Release of Security Interest - FULLY EXECUTED#page180.tif
source=Release of Security Interest - FULLY EXECUTED#page181.tif
source=Release of Security Interest - FULLY EXECUTED#page182.tif
source=Release of Security Interest - FULLY EXECUTED#page183.tif
source=Release of Security Interest - FULLY EXECUTED#page184.tif
source=Release of Security Interest - FULLY EXECUTED#page185.tif
source=Release of Security Interest - FULLY EXECUTED#page186.tif
source=Release of Security Interest - FULLY EXECUTED#page187.tif
source=Release of Security Interest - FULLY EXECUTED#page188.tif
source=Release of Security Interest - FULLY EXECUTED#page189.tif
source=Release of Security Interest - FULLY EXECUTED#page190.tif
source=Release of Security Interest - FULLY EXECUTED#page191.tif
source=Release of Security Interest - FULLY EXECUTED#page192.tif
source=Release of Security Interest - FULLY EXECUTED#page193.tif
source=Release of Security Interest - FULLY EXECUTED#page194.tif
source=Release of Security Interest - FULLY EXECUTED#page195.tif
source=Release of Security Interest - FULLY EXECUTED#page196.tif
source=Release of Security Interest - FULLY EXECUTED#page197.tif
source=Release of Security Interest - FULLY EXECUTED#page198.tif
source=Release of Security Interest - FULLY EXECUTED#page199.tif
source=Release of Security Interest - FULLY EXECUTED#page200.tif
source=Release of Security Interest - FULLY EXECUTED#page201.tif
source=Release of Security Interest - FULLY EXECUTED#page202.tif
source=Release of Security Interest - FULLY EXECUTED#page203.tif

source=Release of Security Interest - FULLY EXECUTED#page204.tif
source=Release of Security Interest - FULLY EXECUTED#page205.tif
source=Release of Security Interest - FULLY EXECUTED#page206.tif
source=Release of Security Interest - FULLY EXECUTED#page207.tif
source=Release of Security Interest - FULLY EXECUTED#page208.tif
source=Release of Security Interest - FULLY EXECUTED#page209.tif
source=Release of Security Interest - FULLY EXECUTED#page210.tif
source=Release of Security Interest - FULLY EXECUTED#page211.tif
source=Release of Security Interest - FULLY EXECUTED#page212.tif
source=Release of Security Interest - FULLY EXECUTED#page213.tif
source=Release of Security Interest - FULLY EXECUTED#page214.tif
source=Release of Security Interest - FULLY EXECUTED#page215.tif

RELEASE OF PATENT SECURITY INTEREST

This RELEASE OF PATENT SECURITY INTEREST ("**Release**") is made and effective as of April 1, 2022 and granted by CORTLAND CAPITAL MARKET SERVICES LLC (the "**Collateral Agent**"), as collateral agent (in such capacity, together with its successors and permitted assigns) for the secured parties under the Loan Agreement referred to below (the "**Secured Parties**"), in favor of HILCO PATENT ACQUISITION 56, LLC, a Delaware limited liability company, BELL SEMICONDUCTOR, LLC, a Delaware limited liability company and BELL NORTHER RESEARCH, LLC, a Delaware limited liability company (each a "**Grantor**" and collectively the "**Grantors**") and their successors, assigns and legal representatives.

Background

Pursuant to the Term Loan Agreement dated as of January 24, 2018 as amended on November 17, 2020 (the "**Loan Agreement**") among Hilco Patent Acquisition 56, LLC, as borrower, Bell Semiconductor, LLC and Bell Northern Research, LLC, as guarantors, the Collateral Agent and the lenders party thereto, the Grantors executed and delivered to the Collateral Agent (i) that certain Security Agreement by and among the Grantors and the Collateral Agent dated as of January 24, 2018 (the "**Master Security Agreement**") and (ii) that certain Patent Security Agreement by and among the Grantors and the Collateral Agent dated as of January 24, 2018 (the "**Patent Security Agreement**" and, together with the Master Security Agreement, the "**Security Agreements**");

Pursuant to the Security Agreements, each Grantor pledged and granted to the Collateral Agent for the ratable benefit of the Secured Parties a security interest in and to all of the right, title and interest of such Grantor in, to and under the Patent Collateral (as defined below);

The Patent Security Agreement was recorded with the United States Patent and Trademark Office at Reel 045216, Frame 0020 on February 1, 2018; and

The Grantors have requested that the Collateral Agent enter into this Release in order to effectuate, evidence and record the release and reassignment to the Grantors of any and all right, title and interest the Collateral Agent and the Secured Parties may have in the Patent Collateral pursuant to the Security Agreements.

Collateral Agent therefore agrees as follows:

1. Release of Security Interest. Collateral Agent, on behalf of itself and the Secured Parties, their successors, legal representatives and assigns, hereby terminates the Patent Security Agreement and terminates, releases and discharges any and all security interests that it has pursuant to the Security Agreements in any and all right, title and interest of the Grantors, and reassigns to the Grantors any and all right, title and interest that it may have, in, to and under the following (collectively, the "**Patent Collateral**"):

(a) any and all patents, patent applications and other patent rights and any other governmental authority-issued indicia of invention ownership, including the patents and patent applications listed in Schedule 1 hereto, and all reissues, divisions, continuations, continuations-in-part, renewals, extensions and reexaminations thereof and amendments thereto (the "**Patents**");

(b) all rights of any kind whatsoever of such Grantor accruing under any of the foregoing provided by applicable law of any jurisdiction, by international treaties and conventions and otherwise throughout the world;

(c) any and all license and other agreements in which such Grantor has granted or is granted a license or other right under any Patent;

(d) any and all royalties, fees, income, payments and other proceeds now or hereafter due or payable with respect to any and all of the foregoing; and

(e) any and all claims and causes of action, with respect to any of the foregoing, whether occurring before, on or after the date hereof, including all rights to and claims for damages, restitution and injunctive and other legal and equitable relief for past, present and future infringement, misappropriation, violation, misuse, breach or default, with the right but no obligation to sue for such legal and equitable relief and to collect, or otherwise recover, any such damages.

2. Further Assurances. Collateral Agent agrees to take all further actions, and provide to the Grantors and their successors, assigns and legal representatives all such cooperation and assistance, including, without limitation, the execution and delivery of any and all further documents or other instruments, as the Grantors and their successors, assigns and legal representatives may reasonably request in order to confirm, effectuate or record this Release.

3. Governing Law. This Release and any claim, controversy, dispute or cause of action (whether in contract or tort or otherwise) based upon, arising out of or relating to this Release and the transactions contemplated hereby shall be governed by, and construed in accordance with, the laws of the United States and the State of New York, without giving effect to any choice or conflict of law provision or rule (whether of the State of New York or any other jurisdiction).

[SIGNATURE PAGE FOLLOWS]

Collateral Agent has caused this Release to be duly executed and delivered by its officer duly authorized as of the date stated in the first paragraph above.

CORTLAND CAPITAL MARKET SERVICES LLC,

as Collateral Agent

By: _____

Name: Emily Ergang Pappas

Title: Head of Legal, North America

ACKNOWLEDGED AND AGREED as of the date stated in the first paragraph above:

HILCO PATENT ACQUISITION 56, LLC, as Grantor

By: _____

Name: Michael Friedman

Title: CEO

BELL SEMICONDUCTOR, LLC, as Grantor

By: _____

Name: John Veschi

Title: CEO

BELL NORTHERN RESEARCH, LLC, as Grantor

By: _____

Name: Afzal Dean

Title: CEO

SCHEDULE 1
TO
RELEASE OF PATENT SECURITY INTEREST
[SEE ATTACHED.]

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08939689	5888120	1997-09-29	1999-03-30	Expired	United States of America	Method and apparatus for chemical mechanical polishing
09216395		1998-12-18		Abandoned	United States of America	Method and Apparatus for Chemical Mechanical Polishing
08700650		1996-08-14		Abandoned	United States of America	Off-Axis Illuminator Lens Mask For Photolithographic Projection System
09105546	5973767	1998-06-26	1999-10-26	Expired	United States of America	Off-axis illuminator lens mask for photolithographic projection system
09089461	6130428	1998-06-02	2000-10-10	Granted	United States of America	Laser fault correction of semiconductor devices
09604865	6407559	2000-06-28	2002-06-18	Granted	United States of America	Laser fault correction of semiconductor devices
08955384	5897381	1997-10-21	1999-04-27	Expired	United States of America	Method of forming a layer and semiconductor substrate
08954791	5893952	1997-10-21	1999-04-13	Expired	United States of America	Apparatus for rapid thermal processing of a wafer
08678718	5756369	1996-07-11	1998-05-26	Expired	United States of America	Rapid thermal processing using a narrowband infrared source and feedback
08924902	5926720	1997-09-08	1999-07-20	Expired	United States of America	Consistent alignment mark profiles on semiconductor wafers using PVD shadowing
09198208	6239499	1998-11-23	2001-05-29	Expired	United States of America	Consistent alignment mark profiles on semiconductor wafers using PVD shadowing
09363084		1999-07-28		Abandoned	United States of America	Nitrogen Implanted Polysilicon Gate For Mosfet Gate Oxide Hardening
08957692	6017808	1997-10-24	2000-01-25	Expired	United States of America	Nitrogen implanted polysilicon gate for MOSFET gate oxide hardening
09022588	6117795	1998-02-12	2000-09-12	Granted	United States of America	Use of corrosion inhibiting compounds in post-etch cleaning processes of an integrated circuit
09583297		2000-05-30		Abandoned	United States of America	Use Of Corrosion Inhibiting Compounds In Post-Etch Cleaning Processes Of An Integrated Circuit
09081403	6239491	1998-05-18	2001-05-29	Granted	United States of America	Integrated circuit structure with thin dielectric between at least local interconnect level and first metal interconnect level, and process for making same
09790821	6486056	2001-02-22	2002-11-26	Granted	United States of America	Process for making integrated circuit structure with thin dielectric between at least local interconnect level and first metal interconnect level
08374193	5646073	1995-01-18	1997-07-08	Expired	United States of America	Process for selective deposition of polysilicon over single crystal silicon substrate and resulting product
08823829	5818100	1997-03-25	1998-10-06	Expired	United States of America	Product resulting from selective deposition of polysilicon over single crystal silicon substrate
08566161		1995-11-30		Abandoned	United States of America	Product Resulting From Selective Deposition Of Polysilicon Over Single Crystal Silicon Substrate
08879100	6121159	1997-06-19	2000-09-19	Expired	United States of America	Polymeric dielectric layers having low dielectric constants and improved adhesion to metal lines

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09618211	6455934	2000-07-10	2002-09-24	Expired	United States of America	Polymeric dielectric layers having low dielectric constants and improved adhesion to metal lines
09362648	6273798	1999-07-27	2001-08-14	Expired	United States of America	Pre-conditioning polishing pads for chemical-mechanical polishing
08841947	5990010	1997-04-08	1999-11-23	Expired	United States of America	Pre-conditioning polishing pads for chemical-mechanical polishing
08791244	6117736	1997-01-30	2000-09-12	Expired	United States of America	Method of fabricating insulated-gate field-effect transistors having different gate capacitances
09594478	6300663	2000-06-15	2001-10-09	Expired	United States of America	Insulated-gate field-effect transistors having different gate capacitances
08701476	5905381	1996-08-22	1999-05-18	Expired	United States of America	Functional OBIC analysis
09244327	6154039	1999-02-03	2000-11-28	Expired	United States of America	Functional OBIC analysis
09109331	6071818	1998-06-30	2000-06-06	Granted	United States of America	Endpoint detection method and apparatus which utilize an endpoint polishing layer of catalyst material
09534652	6258205	2000-03-24	2001-07-10	Granted	United States of America	Endpoint detection method and apparatus which utilize an endpoint polishing layer of catalyst material
08684022	5728612	1996-07-19	1998-03-17	Expired	United States of America	Method for forming minimum area structures for sub-micron CMOS ESD protection in integrated circuit structures without extra implant and mask steps, and articles formed thereby
08748372	5843813	1996-11-13	1998-12-01	Expired	United States of America	I/O driver design for simultaneous switching noise minimization and ESD performance enhancement
08936829	5970321	1997-09-25	1999-10-19	Expired	United States of America	Method of fabricating a microelectronic package having polymer ESD protection
08595021	5869869	1996-01-31	1999-02-09	Expired	United States of America	Microelectronic device with thin film electrostatic discharge protection structure
08723140	5955762	1996-10-01	1999-09-21	Expired	United States of America	Microelectronic package with polymer ESD protection
09188929		1998-11-09		Abandoned	United States of America	Formation Of Gradient Doped Profile Region Between Channel Region And Heavily Doped Source/Drain Contact Region Of MOS Device In Integrated Circuit Structure Using A Re-Entrant Gate Electrode And A Higher Dose Drain Implantation
08690592	5877530	1996-07-31	1999-03-02	Expired	United States of America	Formation of gradient doped profile region between channel region and heavily doped source/drain contact region of MOS device in integrated circuit structure using a re-entrant gate electrode and a higher dose drain implantation
08552461	5670425	1995-11-09	1997-09-23	Expired	United States of America	Process for making integrated circuit structure comprising local area interconnects formed over semiconductor substrate by selective deposition on seed layer in patterned trench
08873809	5895261	1997-06-12	1999-04-20	Expired	United States of America	Process for making integrated circuit structure comprising local area interconnects formed over semiconductor substrate by selective deposition on seed layer in patterned trench

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08718852	5827777	1996-09-24	1998-10-27	Expired	United States of America	Method of making a barrier metal technology for tungsten plug interconnection
08378027	5600182	1995-01-24	1997-02-04	Expired	United States of America	Barrier metal technology for tungsten plug interconnection
08902507		1997-07-29		Abandoned	United States of America	Use Of Reticle Stitching To Provide Design Flexibility
08357728	5652163	1994-12-13	1997-07-29	Expired	United States of America	Use of reticle stitching to provide design flexibility
08233607	5593918	1994-04-22	1997-01-14	Expired	United States of America	Techniques for forming superconductive lines
08454542	5644143	1995-05-30	1997-07-01	Expired	United States of America	Method for protecting a semiconductor device with a superconductive line
11286558	7847285	2005-11-23	2010-12-07	Granted	United States of America	CONFIGURABLE POWER SEGMENTATION USING A NANOTUBE STRUCTURE
12912791	8017512	2010-10-27	2011-09-13	Granted	United States of America	EFFICIENT POWER MANAGEMENT METHOD IN INTEGRATED CIRCUIT THROUGH A NANOTUBE STRUCTURE
10418375	6982229	2003-04-18	2006-01-03	Lapsed	United States of America	Ion recoil implantation and enhanced carrier mobility in CMOS device
11098290	7129516	2005-04-04	2006-10-31	Lapsed	United States of America	Ion recoil implantation and enhanced carrier mobility in CMOS device
11063384	7201633	2005-02-22	2007-04-10	Granted	United States of America	Systems and methods for wafer polishing
11158450		2005-06-21		Abandoned	United States of America	Systems and Methods For Wafer Polishing
11381409		2006-05-03		Abandoned	United States of America	Adjustable Transmission Phase Shift Mask
10972898	7067223	2004-10-25	2006-06-27	Lapsed	United States of America	Adjustable transmission phase shift mask
10039508	6841308	2001-11-09	2005-01-11	Lapsed	United States of America	Adjustable transmission phase shift mask
11016468	6998716	2004-12-16	2006-02-14	Granted	United States of America	Diamond metal-filled patterns achieving low parasitic coupling capacitance
10327283	6867127	2002-12-19	2005-03-15	Granted	United States of America	Diamond metal-filled patterns achieving low parasitic coupling capacitance
60578890		2004-06-10		Abandoned	United States of America	Vortex Phase Shift Mask Applied to Optical Direct Write
13722648	9188848	2012-12-20	2015-11-17	Lapsed	United States of America	Maskless Vortex Phase Shift Optical Direct Write Lithography
13253554	8377633	2011-10-05	2013-02-19	Lapsed	United States of America	Maskless Vortex Phase Shift Optical Direct Write Lithography
11011896	8057963	2004-12-14	2011-11-15	Lapsed	United States of America	Maskless Vortex Phase Shift Optical Direct Write Lithography
11000772	7095483	2004-12-01	2006-08-22	Lapsed	United States of America	Process independent alignment marks
09887131	6856029	2001-06-22	2005-02-15	Granted	United States of America	Process independent alignment marks
10750348	6969683	2003-12-31	2005-11-29	Granted	United States of America	Method of preventing resist poisoning in dual damascene structures
10025304	6713386	2001-12-19	2004-03-30	Granted	United States of America	Method of preventing resist poisoning in dual damascene structures
10195775	6673200	2002-07-12	2004-01-06	Granted	United States of America	Method of reducing process plasma damage using optical spectroscopy
60384499		1900-01-01		Abandoned	United States of America	Impact of F Species on Plasma Charge Damage in a RF Aher

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10680503	6972840	2003-10-06	2005-12-06	Lapsed	United States of America	Method of reducing process plasma damage using optical spectroscopy
10762788	7151059	2004-01-22	2006-12-19	Granted	United States of America	MOS Transistor And Method Of Manufacture
09597012	6740912	2000-06-20	2004-05-25	Granted	United States of America	Semiconductor Device Free Of LDD Regions
10291356		2002-11-08		Abandoned	United States of America	High-K Dielectric Gate Material Uniquely Formed
10643687	6919263	2003-08-19	2005-07-19	Lapsed	United States of America	High-K dielectric gate material uniquely formed
09408299	6323044	1999-09-29	2001-11-27	Granted	United States of America	Integrated Circuit Capacitor And Associated Fabrication Methods
09951178	6525358	2001-09-13	2003-02-25	Granted	United States of America	Capacitor Having The Lower Electrode For Preventing Undesired Defects At The Surface Of The Metal Plug
10459072	6806162	2003-06-11	2004-10-19	Lapsed	United States of America	Method for composing a dielectric layer within an interconnect structure of a multilayer semiconductor device
09164069	6614097	1998-09-30	2003-09-02	Lapsed	United States of America	Method for composing a dielectric layer within an interconnect structure of a multilayer semiconductor device
12256677		2008-10-23		Abandoned	United States of America	Method To Reduce Boron Penetration In SiGe Bipolar Device
11694021	7456061	2007-03-30	2008-11-25	Granted	United States of America	Method To Reduce Boron Penetration In SiGe Bipolar Device
09886780	6649422	2001-06-21	2003-11-18	Granted	United States of America	Integrated Circuit Having A Micromagnetic Device And Method Of Manufacture Therefor
09338143	6255714	1999-06-22	2001-07-03	Granted	United States of America	An Integrated Circuit Having A Micromagnetic Device And Method Of Manufacture Therefor
10234354	7126198	2002-09-03	2006-10-24	Lapsed	United States of America	Protruding Spacers For Self-Aligned Contacts
11542864	7332775	2006-10-04	2008-02-19	Granted	United States of America	Protruding Spacers For Self-Aligned Contacts
09156719	6495407	1998-09-18	2002-12-17	Granted	United States of America	Method Of Making An Article Comprising An Oxide Layer On A GaAs-Based Semiconductor Body
09093557	5962883	1998-06-08	1999-10-05	Expired	United States of America	Article Comprising An Oxide Layer On A GaAs-Based Semiconductor Body, And Method Of Making The Article
11811519	7384801	2007-06-11	2008-06-10	Granted	United States of America	Integrated circuit with inductor having horizontal magnetic flux lines
10614307	7253497	2003-07-02	2007-08-07	Granted	United States of America	Integrated circuit with inductor having horizontal magnetic flux lines
09085913	5949112	1998-05-28	1999-09-07	Granted	United States of America	Integrated Circuits with Tub-Ties
09339306	6054342	1999-06-23	2000-04-25	Granted	United States of America	Method Of Making Integrated Circuits With Tub-Ties
08562235	5773338	1995-11-21	1998-06-30	Expired	United States of America	Bipolar Transistor With MOS-Controlled Protection For Reverse-Biased Emitter-Base Junction
09050711	5949128	1998-03-30	1999-09-07	Expired	United States of America	Bipolar Transistor With MOS\(miControlled Protection For Reverse\(miBiased Emitter\(miBase Junction
08347527	6445043	1994-11-30	2002-09-03	Granted	United States of America	Process for Forming Isolation Regions in An Integrated Circuit and Structure Formed Thereby
08620964	5763314	1996-03-22	1998-06-09	Expired	United States of America	Process For Forming Isolation Regions In An Integrated Circuit

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08777008	5830619	1997-01-07	1998-11-03	Expired	United States of America	Resist Materials
08079310	6159665	1993-06-17	2000-12-12	Granted	United States of America	Processes Using Photosensitive Materials Including A Nitro Benzyl Ester Photoacid Generator
10442533	6864152	2003-05-20	2005-03-08	Granted	United States of America	Fabrication of trenches with multiple depths on the same substrate
10931605	7189628	2004-08-31	2007-03-13	Granted	United States of America	Fabrication of trenches with multiple depths on the same substrate
09943403	6521520	2001-08-30	2003-02-18	Granted	United States of America	Semiconductor wafer arrangement and method of processing a semiconductor wafer
10321250	6707114	2002-12-16	2004-03-16	Granted	United States of America	Semiconductor wafer arrangement of a semiconductor wafer
09162407	6211555	1998-09-29	2001-04-03	Granted	United States of America	Semiconductor device with a pair of transistors having dual work function gate electrodes
09591108	6514824	2000-06-09	2003-02-04	Granted	United States of America	Semiconductor device with a pair of transistors having dual work function gate electrodes
09654689	6613651	2000-09-05	2003-09-02	Lapsed	United States of America	Integrated circuit isolation system
10383031	6831348	2003-03-06	2004-12-14	Lapsed	United States of America	Integrated circuit isolation system
10942444	7381502	2004-09-16	2008-06-03	Lapsed	United States of America	Apparatus and method to improve the resolution of photolithography systems by improving the temperature stability of the reticle
10265856	6866970	2002-10-07	2005-03-15	Lapsed	United States of America	Apparatus and method to improve the resolution of photolithography systems by improving the temperature stability of the reticle
10702165	6830943	2003-11-04	2004-12-14	Lapsed	United States of America	Thin film CMOS calibration standard having protective cover layer
10194578	6674092	2002-07-12	2004-01-06	Lapsed	United States of America	Thin film CMOS calibration standard having protective cover layer
10164909	6555475	2002-06-07	2003-04-29	Granted	United States of America	Arrangement and method for polishing a surface of a semiconductor wafer
09750639	6439981	2000-12-28	2002-08-27	Granted	United States of America	Arrangement and method for polishing a surface of a semiconductor wafer
10607353	6831022	2003-06-26	2004-12-14	Lapsed	United States of America	Method and apparatus for removing water vapor as a byproduct of chemical reaction in a wafer processing chamber
10140536	6630411	2002-05-07	2003-10-07	Granted	United States of America	Method and apparatus for removing water vapor as a byproduct of chemical reaction in a wafer processing chamber
09960765	6504219	2001-09-21	2003-01-07	Granted	United States of America	Indium field implant for punchthrough protection in semiconductor devices
09469579	6342429	1999-12-22	2002-01-29	Granted	United States of America	Method of fabricating an indium field implant for punchthrough protection in semiconductor devices
10819253	7242056	2004-04-05	2007-07-10	Granted	United States of America	Structure And Fabrication Method For Capacitors Integratible With Vertical Replacement Gate Transistors
11809686	7633118	2007-05-31	2009-12-15	Lapsed	United States of America	Structure And Fabrication Method For Capacitors Integratible With Vertical Replacement Gate Transistors

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
12319603	7700432	2009-01-09	2010-04-20	Lapsed	United States of America	Method of Fabricating a Vertical Transistor and Capacitor
11809873	7491610	2007-06-01	2009-02-17	Granted	United States of America	Fabrication Method
09956381		2001-09-18		Abandoned	United States of America	An Integratible Vertical Replacement Gate (VRG)-type Poly-Nitride-Poly (PNP) Or Metal-Nitride-poly (MNP) Capacitor
12610733	7911006	2009-11-02	2011-03-22	Granted	United States of America	Structure And Fabrication Method For Capacitors Integratible With Vertical Replacement Gate Transistors
09723557	6455418	2000-11-28	2002-09-24	Granted	United States of America	Barrier For Copper Metallization
09218649	6288449	1998-12-22	2001-09-11	Granted	United States of America	Barrier For Copper Metallization
09244857	6068130	1999-02-05	2000-05-30	Granted	United States of America	Device And Method For Protecting Electronic Component
09580522	6554137	2000-05-30	2003-04-29	Granted	United States of America	Device And Method For Protecting Electronic Component
10649140	6821851	2003-08-27	2004-11-23	Granted	United States of America	Method Of Making Ultra Thin Body Vertical Replacement Gate Mosfet
10164202	6635924	2002-06-06	2003-10-21	Granted	United States of America	Ultra Thin Body Vertical Replacement Gate Mosfet
10028594	6624498	2001-12-20	2003-09-23	Granted	United States of America	Micromagnetic Device Having Alloy Of Combalt, Phosphorus and Iron
09552627	6495019	2000-04-19	2002-12-17	Granted	United States of America	Device Comprising Micromagnetic Components For Power Applications And Process For Forming Device
09934283	6926841	2001-08-21	2005-08-09	Lapsed	United States of America	Stepped Etalon
09312386	6500521	1999-05-14	2002-12-31	Granted	United States of America	Stepped Etalon
10306565		2002-11-27		Abandoned	United States of America	A Process For Fabricating A Semiconductor Device Having A GATE Dielectric Layer With A High Dielectric Constant
10876183	7223677	2004-06-24	2007-05-29	Granted	United States of America	Process For Fabricating A Semiconductor Device Having An Insulating Layer Formed Over A Semiconductor Substrate
10814682		2004-03-31		Abandoned	United States of America	Semiconductor Device Having A Doped Lattice Matching Layer And A Method Of Manufacture Therefor
10003873	6737339	2001-10-24	2004-05-18	Granted	United States of America	Semiconductor Device Having A Doped Lattice Matching Layer And A Method Of Manufacture Therefor
10814680	6855991	2004-03-31	2005-02-15	Granted	United States of America	Semiconductor Device Having A Doped Lattice Matching Layer And A Method Of Manufacture Therefor
09605931		2000-06-28		Abandoned	United States of America	A Novel Gate Dielectric Structure For Reducing Boron Penetration And Current Leakage
10847789	7081419	2004-05-18	2006-07-25	Lapsed	United States of America	Gate Dielectric Structure For Reducing Boron Penetration And Current Leakage
09146418	6246095	1998-09-03	2001-06-12	Expired	United States of America	System And Method For Forming A Thin Gate Oxide Layer
08814670	5940736	1997-03-11	1999-08-17	Expired	United States of America	Method For Forming A High Quality Ultrathin Gate Oxide Layer
09086252	6060406	1998-05-28	2000-05-09	Granted	United States of America	MOS Transistors With Improved Gate Dielectrics
09519909	6590241	2000-03-07	2003-07-08	Lapsed	United States of America	MOS Transistors With Improved Gate Dielectrics
11821396	7800226	2007-06-22	2010-09-21	Lapsed	United States of America	Integrated Circuit With Metal Silicide Regions

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10245447	7250356	2002-09-17	2007-07-31	Granted	United States of America	Method For Forming Metal Silicide Regions In An Integrated Circuit
11827807	7632690	2007-07-13	2009-12-15	Lapsed	United States of America	Real-Time Gate Etch Critical Dimension Control By Oxygen Monitoring
10675572	7261745	2003-09-30	2007-08-28	Granted	United States of America	Real-Time Gate Etch Critical Dimension Control By Oxygen Monitoring
10978716	7642188	2004-11-01	2010-01-05	Lapsed	United States of America	Mixed Signal Integrated Circuit With Improved Isolation
09911035	6909150	2001-07-23	2005-06-21	Granted	United States of America	Mixed Signal Integrated Circuit With Improved Isolation
08150261	5467883	1993-11-27	1995-11-21	Expired	United States of America	Active Neural Network Control Of Wafer Attributes In A Plasma Etch Process
08468167	5737496	1995-06-06	1998-04-07	Expired	United States of America	Active Neural Network Control Of Wafer Attributes In A Plasma Etch Process
08446122	5653894	1995-05-19	1997-08-05	Expired	United States of America	Active Neural Network Determination Of Endpoint In A Plasma Etch Process
08848141	6054722	1997-04-28	2000-04-25	Expired	United States of America	Current Drive of TFTs in High\(miSpeed SRAMs
08572196	5625200	1995-12-14	1997-04-29	Expired	United States of America	Complementary Devices Using Thin Film Transistors With Improved Current Drive
11385156	7282461	2006-03-21	2007-10-16	Granted	United States of America	Phase-Shifting Mask And Semiconductor Device
10655050	7053405	2003-09-04	2006-05-30	Lapsed	United States of America	Phase-Shifting Mask And Semiconductor Device
09488662	6638663	2000-01-20	2003-10-28	Granted	United States of America	Phase-Shifting Mask And Semiconductor Device
09335707	6197641	1999-06-18	2001-03-06	Granted	United States of America	Process For Fabricating Vertical Transistors
09143274	6027975	1998-08-28	2000-02-22	Granted	United States of America	Process For Fabricating Vertical Transistors
10226930	6869815	2002-08-22	2005-03-22	Granted	United States of America	Electro-Mechanical Device Having A Charge Dissipation Layer And Method Of Manufacture Therefor
10967900	7015056	2004-10-18	2006-03-21	Lapsed	United States of America	Electro-Mechanical Device Having A Charge Dissipation Layer And A Method Of Manufacture Therefor
08753859	5976623	1996-12-03	1999-11-02	Expired	United States of America	Process For Making Composite Films
09197833	6110543	1998-11-23	2000-08-29	Expired	United States of America	Process For Making Compound Films
09568265	6380083	2000-05-10	2002-04-30	Granted	United States of America	Process For Semiconductor Device Fabrication Having Copper Interconnects
09143037	6297154	1998-08-28	2001-10-02	Granted	United States of America	Process For Semiconductor Device Fabrication Having Copper Interconnects
09083168	5998099	1998-05-22	1999-12-07	Expired	United States of America	Energy-Sensitive Resist Material And A Process For Device Fabrication UsingAn Energy-Sensitive Resist Material
08813732	5879857	1997-03-07	1999-03-09	Expired	United States of America	Energy-Sensitive Resist Material And A Process For Device Fabrication Using An Energy-Sensitive Resist Material
08803703	5843624	1997-02-21	1998-12-01	Expired	United States of America	Energy-Sensitive Resist Material And A Process For Device Fabrication Using An Energy-Sensitive Resist Material

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09045062	6103615	1998-03-19	2000-08-15	Granted	United States of America	Corrosion sensitivity structures for vias and contact holes in integrated circuits
09464225	6278129	1999-12-15	2001-08-21	Granted	United States of America	Corrosion sensitivity structures for vias and contact holes in integrated circuits
09370501	6525377	1999-08-09	2003-02-25	Granted	United States of America	Low threshold voltage MOS transistor and method of manufacture
09107767	5985705	1998-06-30	1999-11-16	Granted	United States of America	Low threshold voltage MOS transistor and method of manufacture
09027307	6004880	1998-02-20	1999-12-21	Granted	United States of America	Method of single step damascene process for deposition and global planarization
09365440	6090239	1999-08-02	2000-07-18	Granted	United States of America	Method of single step damascene process for deposition and global planarization
09052851	6057571	1998-03-31	2000-05-02	Granted	United States of America	High aspect ratio, metal-to-metal, linear capacitor for an integrated circuit
09221023	6251740	1998-12-23	2001-06-26	Granted	United States of America	Method of forming and electrically connecting a vertical interdigitated metal-insulator-metal capacitor extending between interconnect layers in an integrated circuit
09219655	6417535	1998-12-23	2002-07-09	Granted	United States of America	Vertical interdigitated metal-insulator-metal capacitor for an integrated circuit
09052793	6358837	1998-03-31	2002-03-19	Granted	United States of America	Method of electrically connecting and isolating components with vertical elements extending between interconnect layers in an integrated circuit
09525489	6441419	2000-03-15	2002-08-27	Granted	United States of America	Encapsulated-metal vertical-interdigitated capacitor and damascene method of manufacturing same
09517150	6479857	2000-03-02	2002-11-12	Lapsed	United States of America	Capacitor having a tantalum lower electrode and method of forming the same
10228859	6861310	2002-08-27	2005-03-01	Lapsed	United States of America	Capacitor having a tantalum lower electrode and method of forming the same
09952343	6620729	2001-09-14	2003-09-16	Lapsed	United States of America	Ion beam dual damascene process
10400281		2003-03-27		Abandoned	United States of America	Ion Beam Double Damascene Process
09211024	6168502	1998-12-14	2001-01-02	Expired	United States of America	Subsonic to supersonic and ultrasonic conditioning of a polishing pad in a chemical mechanical polishing apparatus
08696445	5868608	1996-08-13	1999-02-09	Expired	United States of America	Subsonic to supersonic and ultrasonic conditioning of a polishing pad in a chemical mechanical polishing apparatus
60097750		1998-08-24		Expired	United States of America	Off-Axis Pupil Aperture And Method For Making The Same
09358606	6426131	1999-07-21	2002-07-30	Granted	United States of America	Off-axis pupil aperture and method for making the same
09844531	6596579	2001-04-27	2003-07-22	Granted	United States of America	Method of forming analog capacitor dual damascene process
10959868	7176082	2004-10-06	2007-02-13	Granted	United States of America	Analog capacitor in dual damascene process
10409499	6822282	2003-04-08	2004-11-23	Granted	United States of America	Analog capacitor in dual damascene process
08578741		1995-12-26		Abandoned	United States of America	Integrated Circuit With On-Chip Ground Plane

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08867286	5892272	1997-06-02	1999-04-06	Expired	United States of America	Integrated circuit with on-chip ground base
08277344	5482897	1994-07-19	1996-01-09	Expired	United States of America	Integrated circuit with on-chip ground plane
08943371	5898228	1997-10-03	1999-04-27	Expired	United States of America	On-chip misalignment indication
09150076	6221681	1998-09-09	2001-04-24	Expired	United States of America	On-chip misalignment indication
08811818	5789028	1997-03-04	1998-08-04	Expired	United States of America	Method for eliminating peeling at end of semiconductor substrate in metal organic chemical vapor deposition of titanium nitride
09084027		1998-05-22		Abandoned	United States of America	Method And Apparatus For Eliminating Peeling At End Edge Of Semiconductor Substrate In Metal Organic Chemical Vapor Deposition Of Titanium Nitrite
09158408		1998-09-22		Abandoned	United States of America	Deep Sub-Micron CMOS Device Exhibiting Artificially-Induced Reverse Short-Channel Effects
08761761	5874329	1996-12-05	1999-02-23	Expired	United States of America	Method for artificially-inducing reverse short-channel effects in deep sub-micron CMOS devices
08926220	6030460	1997-09-09	2000-02-29	Expired	United States of America	Method and apparatus for forming dielectric films
08653264	5710079	1996-05-24	1998-01-20	Expired	United States of America	Method and apparatus for forming dielectric films
10944995		2004-09-20		Abandoned	United States of America	Psuedo Low Volume Reticle (PLVR) Design for ASIC Manufacturing
12204290	7763414	2008-09-04	2010-07-27	Lapsed	United States of America	Psuedo Low Volume Reticle (PLVR) Design for ASIC Manufacturing
12191171	7646077	2008-08-13	2010-01-12	Granted	United States of America	Dielectric Barrier Films For Use As Copper Barrier Layers In Semiconductor Trench And Via Structures
10321938	6939800	2002-12-16	2005-09-06	Lapsed	United States of America	Dielectric barrier films for use as copper barrier layers in semiconductor trench and via structures
11131003	7427563	2005-05-16	2008-09-23	Granted	United States of America	Dielectric barrier films for use as copper barrier layers in semiconductor trench and via structures
10991107	7396760	2004-11-17	2008-07-08	Granted	United States of America	Method and system for reducing inter-layer capacitance in integrated circuits
12156281	8015540	2008-05-30	2011-09-06	Granted	United States of America	Method and System for Reducing Inter-Layer Capacitance in Integrated Circuits
10697506	7323228	2003-10-29	2008-01-29	Granted	United States of America	Method of vaporizing and ionizing metals for use in semiconductor processing
11939482	7670645	2007-11-13	2010-03-02	Lapsed	United States of America	Method of Treating Metal and Metal Salts to Enable Thin Layer Deposition in Semiconductor Processing
08502566	5543643	1995-07-13	1996-08-06	Expired	United States of America	Combined JFET and MOS transistor device, circuit
08612337	5631176	1996-03-06	1997-05-20	Expired	United States of America	Method of making combined JFET & MOS transistor device
11286546	7494842	2005-11-23	2009-02-24	Granted	United States of America	PROGRAMMABLE NANOTUBE INTERCONNECT
12354768	8415714	2009-01-15	2013-04-09	Granted	United States of America	PROGRAMMABLE NANOTUBE INTERCONNECT
11389643	7312127	2006-03-23	2007-12-25	Granted	United States of America	Incorporating dopants to enhance the dielectric properties of metal silicates

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10738761	7064062	2003-12-16	2006-06-20	Lapsed	United States of America	Incorporating dopants to enhance the dielectric properties of metal silicates
11768725	7492049	2007-06-26	2009-02-17	Lapsed	United States of America	Multi-layer Registration and Dimensional Test Mark for Scatterometrical Measurement
11046150	7258953	2005-01-28	2007-08-21	Lapsed	United States of America	Multi-layer registration and dimensional test mark for scatterometrical measurement
10035704	6727177	2001-10-18	2004-04-27	Granted	United States of America	Multi-step process for forming a barrier film for use in copper layer formation
11733673	7413984	2007-04-10	2008-08-19	Granted	United States of America	Multi-step process for forming a barrier film for use in copper layer formation
10772133	7229923	2004-02-03	2007-06-12	Granted	United States of America	Multi-step process for forming a barrier film for use in copper layer formation
08604867	5688709	1996-02-14	1997-11-18	Expired	United States of America	Method for forming composite trench-fin capacitors for DRAMS
08879341	6081008	1997-06-20	2000-06-27	Expired	United States of America	Composite trench-fin capacitors for DRAM
08438614		1995-05-10		Abandoned	United States of America	Microelectronic Integrated Circuit Including Triangular Semiconductor "Nand" Gate Device
08561107	5650653	1995-11-21	1997-07-22	Expired	United States of America	Microelectronic integrated circuit including triangular CMOS nand gate device
08704472	5763302	1996-08-20	1998-06-09	Expired	United States of America	Self-aligned twin well process
08768845	5770492	1996-12-18	1998-06-23	Expired	United States of America	Self-aligned twin well process
08488075	5583062	1995-06-07	1996-12-10	Expired	United States of America	Self-aligned twin well process having a SiO2-polysilicon-SiO2 barrier mask
08521795	5585286	1995-08-31	1996-12-17	Expired	United States of America	Implantation of a semiconductor substrate with controlled amount of noble gas ions to reduce channeling and/or diffusion of a boron dopant subsequently implanted into the substrate to form P-LDD region of a PMOS device
08677078	5717238	1996-07-09	1998-02-10	Expired	United States of America	Substrate with controlled amount of noble gas ions to reduce channeling and/or diffusion of a boron dopant forming P-LDD region of a PMOS device
08374195	5598021	1995-01-18	1997-01-28	Expired	United States of America	MOS structure with hot carrier reduction
08695569	5663083	1996-08-12	1997-09-02	Expired	United States of America	Process for making improved MOS structure with hot carrier reduction
08939350	5858864	1997-09-29	1999-01-12	Expired	United States of America	Process for making group IV semiconductor substrate treated with one or more group IV elements to form barrier region capable of inhibiting migration of dopant materials in substrate

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08306179		1994-09-13		Abandoned	United States of America	Group Iv Semiconductor Substrate Treated With One Or More Group Iv Elements To Form Barrier Region Capable Of Inhibiting Migration Of Dopant Materials In Substrate And Process For Making Same
08434673	5654210	1995-05-04	1997-08-05	Expired	United States of America	Process for making group IV semiconductor substrate treated with one or more group IV elements to form one or more barrier regions capable of inhibiting migration of dopant materials in substrate
10791337		2004-03-01		Abandoned	United States of America	Spacer-Less Transistor Integration Scheme For High-K Gate Dielectrics And Small Gate-To-Gate Spaces Applicable To SI, SiGe And Strained Silicon Schemes
11960554	7955919	2007-12-19	2011-06-07	Granted	United States of America	Spacer-Less Transistor Integration Scheme For High-K Gate Dielectrics And Small Gate-To-Gate Spaces Applicable To Si, SiGe And Strained Silicon Schemes
07754201		1991-08-19		Abandoned	United States of America	Bicmos Compacted Logic Array
08410375	6081004	1995-03-27	2000-06-27	Expired	United States of America	BiCMOS compacted logic array
07523445		1990-05-14		Abandoned	United States of America	Bicmos Compacted Logic Array
08014084		1993-02-04		Abandoned	United States of America	Bicmos Compacted Logic Array
12574426	8021955	2009-10-06	2011-09-20	Granted	United States of America	Method Characterizing Materials For A Trench Isolation Structure Having Low Trench Parasitic Capacitance
11262173	7619294	2005-10-28	2009-11-17	Lapsed	United States of America	Shallow Trench Isolation Structure With Low Trench Parasitic Capacitance
09991202	7001823	2001-11-14	2006-02-21	Lapsed	United States of America	Method of manufacturing a shallow trench isolation structure with low trench parasitic capacitance
60314148		1900-01-01		Abandoned	United States of America	Process Enhancement to Prevent LI or Borderless Contact To Well Leakage
10360746	6893937	2003-02-05	2005-05-17	Granted	United States of America	Method for preventing borderless contact to well leakage
11104050	7098515	2005-04-11	2006-08-29	Lapsed	United States of America	Semiconductor chip with borderless contact that avoids well leakage
10006540	6551901	2001-11-30	2003-04-22	Granted	United States of America	Method for preventing borderless contact to well leakage
11090107	7312532	2005-03-24	2007-12-25	Granted	United States of America	Dual damascene interconnect structure with improved electro migration lifetimes
10328333	7033929	2002-12-23	2006-04-25	Lapsed	United States of America	Dual damascene interconnect structure with improved electro migration lifetimes
07982093		1992-11-24		Abandoned	United States of America	Improved Metal Oxide Semiconductors Devices And Method For Making Same
08259575	6432759	1994-06-14	2002-08-13	Granted	United States of America	Method of forming source and drain regions for CMOS devices
11258253	7582938	2005-10-25	2009-09-01	Lapsed	United States of America	I/O and Power ESD Protection Circuits by Enhancing Substrate-Bias In Deep-Submicron CMOS Process

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
12506746	7948036	2009-07-21	2011-05-24	Granted	United States of America	I/O and Power ESD Protection Circuits by Enhancing Substrate-Bias In Deep-Submicron CMOS Process
13110581	8269280	2011-05-18	2012-09-18	Granted	United States of America	I/O and Power ESD Protection Circuits by Enhancing Substrate-Bias In Deep-Submicron CMOS Process
10676602	6979869	2003-10-01	2005-12-27	Granted	United States of America	Substrate-biased I/O and power ESD protection circuits in deep-submicron twin-well process
11838546	8134188	2007-08-14	2012-03-13	Granted	United States of America	Circuits And Methods For Improved FET Matching
13368985	8440512	2012-02-08	2013-05-14	Granted	United States of America	Circuits and Methods for Improved FET Matching
07591646	5123375	1990-10-02	1992-06-23	Expired	United States of America	Structure for filtering CVD chamber process gases
08979733	6113699	1997-11-26	2000-09-05	Expired	United States of America	Purging gas control structure for CVD chamber
08390329	5681613	1995-02-17	1997-10-28	Expired	United States of America	Filtering technique for CVD chamber process gases
07591587		1990-10-02		Abandoned	United States of America	Method For Performing In-Situ Etch Of A Cvd Chamber
07794780	5203956	1991-11-18	1993-04-20	Expired	United States of America	Method for performing in-situ etch of a CVD chamber
07591655		1990-10-02		Abandoned	United States of America	Apparatus For Performing In-Situ Etch Of Of A Cvd Chamber
07809104	5211796	1991-12-12	1993-05-18	Expired	United States of America	Apparatus for performing in-situ etch of CVD chamber
08979734		1997-11-26		Abandoned	United States of America	In-Situ Etch Of Cvd Chamber
07739773	5391394	1991-07-29	1995-02-21	Expired	United States of America	Tungsten deposition process for low contact resistivity to silicon
08851846	5853804	1997-05-06	1998-12-29	Expired	United States of America	Gas control technique for limiting surging of gas into a CVD chamber
07461959		1990-01-08		Abandoned	United States of America	Tungsten Deposition Process For Low Contact Resistivity To Silicon
07592014	5180432	1990-10-02	1993-01-19	Expired	United States of America	Apparatus for conducting a refractory metal deposition process
11937199	7560292	2007-11-08	2009-07-14	Lapsed	United States of America	Voltage Contrast Monitor for Integrated Circuit Defects
10652369	6936920	2003-08-29	2005-08-30	Lapsed	United States of America	Voltage contrast monitor for integrated circuit defects
11131705	7323768	2005-05-18	2008-01-29	Lapsed	United States of America	Voltage contrast monitor for integrated circuit defects
12890336	8527912	2010-09-24	2013-09-03	Lapsed	United States of America	Digitally Obtaining Contours of Fabricated Polygons
11182615	7827509	2005-07-15	2010-11-02	Granted	United States of America	Digitally Obtaining Contours of Fabricated Polygons
12652560	8106480	2010-01-05	2012-01-31	Granted	United States of America	Bipolar Device Having Improved Capacitance
11531477	7666750	2006-09-13	2010-02-23	Lapsed	United States of America	Bipolar Device Having Improved Capacitance
12018849	7582566	2008-01-24	2009-09-01	Lapsed	United States of America	Method and Apparatus For Redirecting Void Diffusion Away From Vias In An Integrated Circuit Design
11323400	7361965	2005-12-29	2008-04-22	Granted	United States of America	Method and apparatus for redirecting void diffusion away from vias in an integrated circuit design
10383149	6872612	2003-03-06	2005-03-29	Lapsed	United States of America	Local interconnect for integrated circuit
11058498	7081379	2005-02-15	2006-07-25	Lapsed	United States of America	Local interconnect for integrated circuit
10801310	7395522	2004-03-16	2008-07-01	Granted	United States of America	Yield profile manipulator
12117379	7930655	2008-05-08	2011-04-19	Granted	United States of America	Yield Profile Manipulator
11414902	7541238	2006-05-01	2009-06-02	Granted	United States of America	Inductor Formed In An Integrated Circuit
10953475	7068139	2004-09-29	2006-06-27	Granted	United States of America	Inductor Formed In An Integrated Circuit

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
12340813	7678639	2008-12-22	2010-03-16	Granted	United States of America	Inductor Formed In An Integrated Circuit
11265062	7635888	2005-11-02	2009-12-22	Granted	United States of America	Interdigitated Capacitors
10886763	7022581	2004-07-08	2006-04-04	Granted	United States of America	Interdigitated Capacitors
12616050	8039923	2009-11-10	2011-10-18	Granted	United States of America	Interdigitated Capacitors
10454027	6880140	2003-06-04	2005-04-12	Lapsed	United States of America	Method to selectively identify reliability risk die based on characteristics of local regions on the wafer
11031564	7390680	2005-01-06	2008-06-24	Granted	United States of America	Method to selectively identify reliability risk die based on characteristics of local regions on the wafer
12728412	8227319	2010-03-22	2012-07-24	Granted	United States of America	A Bipolar Junction Treatment Having A High Germanium Concentration In A Silicon Germanium Layer and a Method for Forming the Bipolar Junction Transistor
10598213	7714361	2006-08-21	2010-05-11	Lapsed	United States of America	A Bipolar Junction Transistor Having A High Germanium Concentration In A Silicon-Germanium Layer And A Method For Forming The Bipolar Junction Transistor
13348415		2012-01-11		Abandoned	United States of America	A Bipolar Junction Transistor Having A High Germanium Concentration In A Silicon-Germanium Layer and a Method for Forming the Bipolar Junction Transistor
10669398	6784044	2003-09-24	2004-08-31	Granted	United States of America	High Dopant Concentration Diffused Resistor And Method Of Manufacture Thereof
10256466	6690082	2002-09-27	2004-02-10	Granted	United States of America	A High Dopant Concentration Diffused Resistor And Method Of Manufacture Thereof
12208929	7776678	2008-09-11	2010-08-17	Lapsed	United States of America	A Thermally Stable BiCMOS Fabrication Method And Bipolar Junction Transistors Formed According To The Method
11361430	7439119	2006-02-24	2008-10-21	Lapsed	United States of America	A Thermally Stable BiCMOS Fabrication Method And Bipolar Junction Transistors Formed According To The Method
12832110	8084313	2010-07-08	2011-12-27	Granted	United States of America	A Thermally Stable BiCMOS Fabrication Method And Bipolar Junction Transistor Formed According To The Method
10828993		2004-04-21		Abandoned	United States of America	Method For Making A Radio Frequency Component And Component Produced Thereby
09715651	6743731	2000-11-17	2004-06-01	Granted	United States of America	Method For Making A Radio Frequency Component And Component Produced Thereby
09528071	6530074	2000-03-17	2003-03-04	Granted	United States of America	Apparatus For Verification Of IC Mask Sets
10317147	7103869	2002-12-11	2006-09-05	Lapsed	United States of America	Method Of Verifying IC Mask Sets
10718536	7456064	2003-11-24	2008-11-25	Lapsed	United States of America	High K Dielectric Material And Method Of Making A High K Dielectric Material
10155173	6680130	2002-05-28	2004-01-20	Lapsed	United States of America	High K Dielectric Material And Method Of Making A High K Dielectric Material

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
12506090	7981305	2009-07-20	2011-07-19	Granted	United States of America	High Density Field Emission Elements And A Method For Forming Said Emission Elements
11057690	7564178	2005-02-14	2009-07-21	Lapsed	United States of America	High Density Field Emission Elements and a Method for Forming Said Emission Elements
09901073		2001-07-09		Abandoned	United States of America	Lateral High-Q Inductor For Semiconductor Devices
09416348	6292086	1999-10-12	2001-09-18	Granted	United States of America	Lateral High-Q Inductor For Semiconductor Devices
09894116	6458016	2001-06-28	2002-10-01	Granted	United States of America	Polishing Fluid, Polishing Method, Semiconductor Device And Semiconductor Device Fabrication Method
09483576	6375541	2000-01-14	2002-04-23	Granted	United States of America	Polishing Fluid, Polishing Method, Semiconductor Device and Semiconductor Device Fabrication Method
10637385	7067048	2003-08-08	2006-06-27	Lapsed	United States of America	Method to improve the control of electro-polishing by use of a plating electrode an electrolyte bath
11409377		2006-04-21		Abandoned	United States of America	Method To Improve The Control Of Electro-Polishing By Use Of A Plating Electrode In An Electrolyte Bath
10152879		2002-05-21		Abandoned	United States of America	Microsrtructure Control Of Copper Interconnects
09419986	6440849	1999-10-18	2002-08-27	Granted	United States of America	Microsrtructure Control Of Copper Interconnects
08814051	5936831	1997-03-06	1999-08-10	Expired	United States of America	Thin Film Tantalum Oxide Capacitors And Resulting Product
08918174	6075691	1997-08-25	2000-06-13	Expired	United States of America	THIN FILM CAPACITORS AND PROCESS FOR MAKING THEM
08678971	5821148	1996-07-12	1998-10-13	Expired	United States of America	Method of Fabricating a Segmented Emitter Low Noise Transistor
08484675	5723897	1995-06-07	1998-03-03	Expired	United States of America	Segmented Emitter Low Noise Transistor
09653616	6690037	2000-08-31	2004-02-10	Granted	United States of America	Field Plated Schottky Diode
10696136	6790753	2003-10-29	2004-09-14	Granted	United States of America	Field Plated Schottky Diode And Method Of Fabrication Thereof
09878657	6482694	2001-06-11	2002-11-19	Granted	United States of America	Semiconductor Device Structure Including A Tantalum Pentoxide Layer Sandwiched Between Silicon Nitride Layers
09259001	6294807	1999-02-26	2001-09-25	Granted	United States of America	Semiconductor Device Structure Including A Tantalum Pentoxide Layer Sandwiched Between Silicon Nitride Layers
11649197	7670203	2007-01-03	2010-03-02	Lapsed	United States of America	Process For Making An On-Chip Vacuum Tube Device
09651696	7259510	2000-08-30	2007-08-21	Granted	United States of America	On-Chip Vacuum Tube Device And Process For Making Device
09643784	6383923	2000-08-22	2002-05-07	Granted	United States of America	Article Comprising Vertically Nano-InterConnected Circuit Devices And Method For Making The Same
09426457	6340822	1999-10-05	2002-01-22	Granted	United States of America	Article Comprising Vertically Nano-InterConnected Circuit Devices And Method For Making The Same
11748569	7407824	2007-05-15	2008-08-05	Granted	United States of America	Guard Ring For Improved Matching
10941665	7253012	2004-09-14	2007-08-07	Granted	United States of America	Guard Ring For Improved Matching
10916322	7405116	2004-08-11	2008-07-29	Granted	United States of America	Application of gate edge liner to maintain gate length CD in a replacement gate transistor flow
12140773	8384165	2008-06-17	2013-02-26	Granted	United States of America	Application of Gate Edge Liner To Maintain Gate Length CD In A Replacement Gate Transistor Flow

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09410686	6410435	1999-10-01	2002-06-25	Granted	United States of America	Process For Fabricating Copper Interconnect For ULSI Integrated Circuits
10120707		2002-04-11		Abandoned	United States of America	Process For Fabricating Copper Interconnect For ULSI Integrated Circuits
12356600	8022481	2009-01-21	2011-09-20	Granted	United States of America	Robust Shallow Trench Isolation Structures And A Method For Forming Shallow Trench Isolation Structures
11321206	7514336	2005-12-29	2009-04-07	Lapsed	United States of America	Robust Shallow Trench Isolation Structures And A Method For Forming Shallow Trench Isolation Structures
09280103	6252245	1999-03-29	2001-06-26	Granted	United States of America	Device Comprising N-Channel Semiconductor Material
09476511	6387727	2000-01-03	2002-05-14	Granted	United States of America	Device Comprising N-Channel Semiconductor Material
11927950	7579245	2007-10-30	2009-08-25	Lapsed	United States of America	Dual-Gate Metal-Oxide Semiconductor Device
10999705	7329922	2004-11-30	2008-02-12	Granted	United States of America	Dual\(miGate Metal\(miOxide Semiconductor Device
09884736	6930056	2001-06-19	2005-08-16	Lapsed	United States of America	Plasma treatment of low dielectric constant dielectric material to form structures useful in formation of metal interconnects and/or filled vias for integrated circuit structure
10422270	6790784	2003-04-24	2004-09-14	Lapsed	United States of America	Plasma treatment of low dielectric constant dielectric material to form structures useful in formation of metal interconnects and/or filled vias for intergrated circuit structure
11530550	7271485	2006-09-11	2007-09-18	Granted	United States of America	Systems And Methods For Distributing I\(slO In A Semiconductor Device
11684674	7709861	2007-03-12	2010-05-04	Granted	United States of America	Systems And Methods For Supporting a Subset of Multiple Interface Types In A Semiconductor Device
09456224	6576529	1999-12-07	2003-06-10	Granted	United States of America	A Method Of Forming An Alignment Feature In Or On A Multi-Layered Semiconductor Structure
10704449	6977128	2003-11-07	2005-12-20	Lapsed	United States of America	Multi-Layered Semiconductor Structure
09867202	6706609	2001-05-29	2004-03-16	Granted	United States of America	Method Of Forming An Alignment Feature In Or On A Multi-Layered Semiconductor Structure
09804783	6586326	2001-03-13	2003-07-01	Lapsed	United States of America	Metal planarization system
10400278	6951808	2003-03-27	2005-10-04	Lapsed	United States of America	Metal planarization system
09617550	6569751	2000-07-17	2003-05-27	Granted	United States of America	Low via resistance system
10400252	6893962	2003-03-27	2005-05-17	Granted	United States of America	Low via resistance system
08718113	5804975	1996-09-18	1998-09-08	Expired	United States of America	Detecting Breakdown In Dielectric Layers
09002497	6043662	1998-01-02	2000-03-28	Expired	United States of America	Detecting Defects In Integrated Circuits
08702073	5969376	1996-08-23	1999-10-19	Expired	United States of America	An Organic Thin Film Transistor Having A Phthalocyanine Semiconductor Layer
09204002	6150191	1998-12-01	2000-11-21	Expired	United States of America	Method of Making an Organic Thin Film Transistor and Article Made by the Method
09135260	6015333	1998-08-17	2000-01-18	Expired	United States of America	Method Of Forming Planarized Layers In An Intergrated Circuit

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08769717	5836805	1996-12-18	1998-11-17	Expired	United States of America	Method of Forming Planarized Layers In An Integrated Circuit
09083072	6024829	1998-05-21	2000-02-15	Granted	United States of America	Method Of Eliminating Agglomerate Particles In A Polishing Slurry
09427306	6355184	1999-10-26	2002-03-12	Granted	United States of America	A Method Of Eliminating Agglomerate Particles In A Polishing Slurry
09992135	6750145	2001-11-14	2004-06-15	Granted	United States of America	A Method Of Eliminating Agglomerate Particles In A Polishing Slurry
08344785	5576763	1994-11-22	1996-11-19	Expired	United States of America	Single-Polysilicon CMOS Active Pixel
08675026	5835141	1996-07-03	1998-11-10	Expired	United States of America	Single-Polysilicon CMOS Active Pixel Image Sensor
08872250	6118351	1997-06-10	2000-09-12	Expired	United States of America	A Micromagnetic Device For Power Processing Applications And Method Of Manufacture Therefor
09292860	6191495	1999-04-16	2001-02-20	Expired	United States of America	Micromagnetic Device Having An Anisotropic Ferromagnetic Core and Method of Manufacture Therefor
09511343	6440750	2000-02-23	2002-08-27	Expired	United States of America	Method Of Making Integrated Circuit Having A Micromagnetic Device
10387846	7021518	2003-03-13	2006-04-04	Lapsed	United States of America	Micromagnetic Device For Power Processing Applications And Method Of Manufacture Therefor
09978871	6696744	2001-10-15	2004-02-24	Expired	United States of America	Integrated Circuit Having A Micromagnetic Device And Method Of Manufacture Therefor
09109963	6163234	1998-07-02	2000-12-19	Expired	United States of America	A Micromagnetic Device For Data Transmission Applications And Method Of Manufacture Therefor
09490655	6160721	2000-01-24	2000-12-12	Expired	United States of America	A Micromagnetic Device For Power Processing Applications And Method Of Manufacture Therefor
10400279	6927494	2003-03-27	2005-08-09	Lapsed	United States of America	Local interconnect
09966464	6576544	2001-09-28	2003-06-10	Granted	United States of America	Local interconnect
08381375	5616368	1995-01-31	1997-04-01	Expired	United States of America	Field Emission Devices Employing Activated Diamond Particle Emitters And Methods For Making Same
08361616	5709577	1994-12-22	1998-01-20	Expired	United States of America	Method Of Making Field Emission Devices Employing Ultra-Fine Diamond Particle Emitters
09006347	5977697	1998-01-13	1999-11-02	Expired	United States of America	Field Emission Devices Employing Diamond Particle Emitters
10368760	6747358	2003-02-18	2004-06-08	Granted	United States of America	Self-aligned alloy capping layers for copper interconnect structures
10004461	6566262	2001-11-01	2003-05-20	Granted	United States of America	Method for creating self-aligned alloy capping layers for copper interconnect structures
09533428	6312565	2000-03-23	2001-11-06	Granted	United States of America	Thin Film Deposition Of Mixed Metal Oxides
09917365	6540974	2001-07-27	2003-04-01	Granted	United States of America	Process For Making Mixed Metal Oxides
10038734	6762459	2001-12-31	2004-07-13	Granted	United States of America	Method For Fabricating MOS Device With Halo Implanted Region
09523782	6362054	2000-03-13	2002-03-26	Granted	United States of America	Method For Fabricating MOS Device With Halo Implanted Region
10368811	6977400	2003-02-18	2005-12-20	Lapsed	United States of America	Silicon germanium CMOS channel
09724444	6544854	2000-11-28	2003-04-08	Granted	United States of America	Silicon germanium CMOS channel

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10641768	6987059	2003-08-14	2006-01-17	Granted	United States of America	Method and structure for creating ultra low resistance damascene copper wiring
11259965	7196420	2005-10-26	2007-03-27	Granted	United States of America	Method and structure for creating ultra low resistance damascene copper wiring
10802522		2004-03-17		Abandoned	United States of America	Interconnect Integration
10448082	6777807	2003-05-29	2004-08-17	Granted	United States of America	Interconnect integration
11314649		2005-12-21		Abandoned	United States of America	Variable Mask Field Exposure
12167381	7638245	2008-07-03	2009-12-29	Lapsed	United States of America	Variable Mask Field Exposure
10429376	7018753	2003-05-05	2006-03-28	Lapsed	United States of America	Variable mask field exposure
10951646		2004-09-28		Abandoned	United States of America	Plasma Removal Of High K Metal Oxide
10413051	7413996	2003-04-14	2008-08-19	Granted	United States of America	High k gate insulator removal
11337460	7220362	2006-01-23	2007-05-22	Granted	United States of America	Planarization with reduced dishing
10421068	7029591	2003-04-23	2006-04-18	Lapsed	United States of America	Planarization with reduced dishing
11695169		2007-04-02		Abandoned	United States of America	Planarization with Reduced Dishing
09894117	6439972	2001-06-28	2002-08-27	Granted	United States of America	Polishing Fluid, Polishing Method, Semiconductor Device And Semiconductor Device Fabrication Method
09483785	6328633	2000-01-14	2001-12-11	Granted	United States of America	Polishing Fluid, Polishing Method, Semiconductor Device And Semiconductor Device Fabrication Method
10964032		2004-10-12		Abandoned	United States of America	Via and Metal Line Interface Capable of Reducing the Incidence of Electro-Migration Induced Voids
10400297	6875693	2003-03-26	2005-04-05	Granted	United States of America	Via and metal line interface capable of reducing the incidence of electro-migration induced voids
11189625		2005-07-25		Abandoned	United States of America	Memory Device Having an Electron Trapping Layer in a High-K Dielectric Gate Stack
10123263	7132336	2002-04-15	2006-11-07	Granted	United States of America	Method and apparatus for forming a memory structure having an electron affinity region
10698169	6989565	2003-10-31	2006-01-24	Lapsed	United States of America	Memory device having an electron trapping layer in a high-K dielectric gate stack
09879642	6495312	2001-06-12	2002-12-17	Granted	United States of America	Method and apparatus for removing photoresist edge beads from thin film substrates
10263593	6614507	2002-10-03	2003-09-02	Granted	United States of America	Apparatus for removing photoresist edge beads from thin film substrates
09775223		2001-02-01		Abandoned	United States of America	Method and Apparatus for Removing Photoresist Edge Beads From Thin Film Substrates
10196787	6787180	2002-07-17	2004-09-07	Granted	United States of America	Exhaust flow control system
09666507	6579371	2000-09-20	2003-06-17	Granted	United States of America	Exhaust flow control system
10328614	6972217	2002-12-23	2005-12-06	Lapsed	United States of America	Low k polymer E-beam printable mechanical support

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11225310	7358594	2005-09-12	2008-04-15	Granted	United States of America	Method of forming a low k polymer E-beam printable mechanical support
10243562	6885436	2002-09-13	2005-04-26	Lapsed	United States of America	Optical error minimization in a semiconductor manufacturing apparatus
11473627	7298458	2006-06-22	2007-11-20	Granted	United States of America	Optical error minimization in a semiconductor manufacturing apparatus
11075195	7098996	2005-03-07	2006-08-29	Lapsed	United States of America	Optical error minimization in a semiconductor manufacturing apparatus
09074837	6090656	1998-05-08	2000-07-18	Granted	United States of America	Linear capacitor and process for making same
09550381	6545305	2000-04-14	2003-04-08	Granted	United States of America	Linear capacitor and process for making same
10623082	7160805	2003-07-17	2007-01-09	Granted	United States of America	Inter-layer interconnection structure for large electrical connections
10272767	6642597	2002-10-16	2003-11-04	Granted	United States of America	Inter-layer interconnection structure for large electrical connections
10197956	6807655	2002-07-16	2004-10-19	Lapsed	United States of America	Adaptive off tester screening method based on intrinsic die parametric measurements
60381746		2002-05-17		Expired	United States of America	Process and Apparatus for Wafer Edge Profile Control Using Gas Flow Control Ring
10821708		2004-04-09		Abandoned	United States of America	Process and Apparatus for Wafer Edge Profile Control Using Gas Flow Control Ring
10200469	6753255	2002-07-18	2004-06-22	Granted	United States of America	Process for wafer edge profile control using gas flow control ring
10160812	6613637	2002-05-31	2003-09-02	Granted	United States of America	Composite spacer scheme with low overlapped parasitic capacitance
10458141	6737342	2003-06-09	2004-05-18	Granted	United States of America	Composite spacer scheme with low overlapped parasitic capacitance
10253158	6713394	2002-09-24	2004-03-30	Granted	United States of America	Process for planarization of integrated circuit structure which inhibits cracking of low dielectric constant dielectric material adjacent underlying raised structures
09661465	6489242	2000-09-13	2002-12-03	Granted	United States of America	Process for planarization of integrated circuit structure which inhibits cracking of low dielectric constant dielectric material adjacent underlying raised structures
10417708	7056392	2003-04-16	2006-06-06	Lapsed	United States of America	Wafer chucking apparatus and method for spin processor
11403137	7201176	2006-04-11	2007-04-10	Granted	United States of America	Wafer chucking apparatus for spin processor
09467622	6375791	1999-12-20	2002-04-23	Granted	United States of America	Method and apparatus for detecting presence of residual polishing slurry subsequent to polishing of a semiconductor wafer
10012847	6716364	2001-12-10	2004-04-06	Granted	United States of America	Method and apparatus for detecting presence of residual polishing slurry subsequent to polishing of a semiconductor wafer
10185537	6699766	2002-07-01	2004-03-02	Granted	United States of America	Method of fabricating an integral capacitor and gate transistor having nitride and oxide polish stop layers using chemical mechanical polishing elimination

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10733034	7148146	2003-12-11	2006-12-12	Granted	United States of America	Method of fabricating an integral capacitor and gate transistor having nitride and oxide polish stop layers using chemical mechanical polishing elimination
10013572	6614093	2001-12-11	2003-09-02	Granted	United States of America	Integrated inductor in semiconductor manufacturing
10463158		2003-06-16		Abandoned	United States of America	Integrated Inductor in Semiconductor Manufacturing
60292832		2001-05-21		Expired	United States of America	Web-Bases Interface With Defect Database To View And Update Failure Events
10128534	6775630	2002-04-23	2004-08-10	Granted	United States of America	Web-based interface with defect database to view and update failure events
10845716		2004-05-14		Abandoned	United States of America	Method And Structure For Forming Dielectric Layers Having Reduced Dielectric Constants
10180661	6774057	2002-06-25	2004-08-10	Granted	United States of America	Method and structure for forming dielectric layers having reduced dielectric constants
09968944	6472314	2001-10-02	2002-10-29	Granted	United States of America	Diamond barrier layer
10238073	6734560	2002-09-09	2004-05-11	Granted	United States of America	Diamond barrier layer
10035501	6743474	2001-10-25	2004-06-01	Granted	United States of America	Method for growing thin films
10804980	7081296	2004-03-16	2006-07-25	Lapsed	United States of America	Method for growing thin films
11906196	8631547	2007-10-01	2014-01-21	Granted	United States of America	Method Of Isolation For Acoustic Resonator Devices
09497993	7296329	2000-02-04	2007-11-20	Granted	United States of America	Method Of Isolation For Acoustic Resonator Devices
12243137	7713811	2008-10-01	2010-05-11	Lapsed	United States of America	Multiple Doping Level Bipolar Junctions Transistors And Method For Forming
12727304	7910425	2010-03-19	2011-03-22	Granted	United States of America	Multiple Doping Level Bipolar Junctions Transistors And Method For Forming
10953894	7095094	2004-09-29	2006-08-22	Lapsed	United States of America	Multiple Doping Level Bipolar Junctions Transistors And Method For Forming
13026528	8143120	2011-02-14	2012-03-27	Granted	United States of America	Multiple Doping Level Bipolar Junctions Transistors And Method For Forming
11458270	7449388	2006-07-18	2008-11-11	Lapsed	United States of America	Method For Forming Multiple Doping Level Bipolar Junctions Transistors
10955238	7345364	2004-09-30	2008-03-18	Granted	United States of America	Structure And Method For Improved Heat Conduction For Semiconductor Devices
11968693	7498204	2008-01-03	2009-03-03	Granted	United States of America	Structure And Method For Improved Heat Conduction For Semiconductor Devices
10773900	7078280	2004-02-06	2006-07-18	Lapsed	United States of America	Vertical Replacement-Gate Silicon-On-Insulator Transistor
11419356	7259048	2006-05-19	2007-08-21	Granted	United States of America	Vertical Replacement-Gate Silicon-On-Insulator Transistor
09968234	6709904	2001-09-28	2004-03-23	Granted	United States of America	Vertical Replacement-Gate (VRG) Silicon-On-Insulator (SOI) CMOS Transistor
09968388		2001-09-28		Abandoned	United States of America	Lithographically Defined CMOS Threshold Voltage

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10619058	7049199	2003-07-14	2006-05-23	Granted	United States of America	Method Of Ion Implantation For Achieving Desired Dopant Concentration
09961477	6686604	2001-09-21	2004-02-03	Granted	United States of America	Multiple Operating Voltage Vertical Replacement-Gate (VRG) Transistor
10684713	7056783	2003-10-14	2006-06-06	Lapsed	United States of America	Multiple Operating Voltage Vertical Replacement-Gate (VRG) Transistor
10409423	6821831	2003-04-08	2004-11-23	Lapsed	United States of America	Electrostatic Discharge Protection In Double Diffused MOS Transistors
09896669	6576506	2001-06-29	2003-06-10	Granted	United States of America	Electrostatic Discharge Protection In Double Diffused MOS Transistors
10777250	6873171	2004-02-12	2005-03-29	Granted	United States of America	Integrated Circuit Early Life Failure Detection By Monitoring Changes In Current Signatures
09558130	6714032	2000-04-25	2004-03-30	Granted	United States of America	Integrated Circuit Early Life Failure Detection By Monitoring Changes In Current Signatures
10147384	6683382	2002-05-16	2004-01-27	Granted	United States of America	Semiconductor Device Having An Interconnect Layer With A Plurality Of Layout Regions Having Substantially Uniform Densities Of Active Interconnects And Dummy Fills
09484310	6436807	2000-01-18	2002-08-20	Granted	United States of America	Method For Making An Interconnect Layer And A Semiconductor Device Including The Same
08820063	5913146	1997-03-18	1999-06-15	Expired	United States of America	Semiconductor Device Having Aluminum Contacts Or Vias And Method Of Manufacture Therefor
09166832	6157082	1998-10-05	2000-12-05	Expired	United States of America	Semiconductor Device Having Aluminum Contacts Or Vias And Method Of Manufacture Therefor
09073556	6028359	1998-05-06	2000-02-22	Expired	United States of America	Integrated Circuit Having Amorphous Silicide Layer In Contacts And Vias And Method Of Manufacture Therefor
08816185	5858873	1997-03-12	1999-01-12	Expired	United States of America	Integrated Circuit Having Amorphous Silicide Layer In Contacts And Vias AndMethod Of Manufacture Therefor
09523210	6139995	2000-03-10	2000-10-31	Granted	United States of America	Method Of Manufacturing Schottky Gate Transistor Utilizing Alignment Techniques With Multiple Photoresist Layers
09111534	6042975	1998-07-08	2000-03-28	Granted	United States of America	Alignment Techniques For Photolithography
09049531	6033202	1998-03-27	2000-03-07	Granted	United States of America	Mold For Non-Photolithographic Fabrication Of Microstructures
09393032	6322736	1999-09-09	2001-11-27	Granted	United States of America	Mold For Non-Photolithographic Fabrication Of Microstructures
11999168	8153484	2007-12-04	2012-04-10	Granted	United States of America	Metal-Oxide-Semiconductor Device Having Trenched Diffusion Region And Method Of Forming Same
13428540	8648445	2012-03-23	2014-02-11	Lapsed	United States of America	Metal-Oxide-Semiconductor Device Having Trenched Diffusion Region And Method Of Forming Same
10953477	7338569	2004-09-29	2008-03-04	Granted	United States of America	Method And System Of Using Offset Gag For CMP Polishing Pad Alignment And Adjustment

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11968930	7527544	2008-01-03	2009-05-05	Lapsed	United States of America	System Of Using Offset Gage For CMP Polishing Pad Alignment And Adjustment
09150529	6215158	1998-09-10	2001-04-10	Granted	United States of America	Device And Method For Forming Semiconductor Interconnections In An Integrated Circuit Substrate
09631546	6503787	2000-08-03	2003-01-07	Granted	United States of America	Device And Method For Forming Semiconductor Interconnections In An Integrated Circuit Substrate
11641507	7537984	2006-12-19	2009-05-26	Lapsed	United States of America	III-V Power Field Effect Transistors
10948897	7180103	2004-09-24	2007-02-20	Granted	United States of America	III/V Power Field Effect Transistors
10926631	7109589	2004-08-26	2006-09-19	Granted	United States of America	Integrated Circuit With Substantially Perpendicular Wire Bonds
11494221	7465655	2006-07-27	2008-12-16	Granted	United States of America	Integrated Circuit With Substantially Perpendicular Wire Bonds
08752235	5811916	1996-11-19	1998-09-22	Expired	United States of America	Field Emission Devices Employing Enhanced Diamond Field Emitters
08752234	5744195	1996-11-19	1998-04-28	Expired	United States of America	Field Emission Devices Employing Enhanced Diamond Field Emitters
08331458	5637950	1994-10-31	1997-06-10	Expired	United States of America	Field Emission Devices Employing Enhanced Diamond Field Emitters
10850812	7235489	2004-05-21	2007-06-26	Granted	United States of America	Device And Method To Eliminate Shorting Induced By Via To Metal Misalignment
11738050	7675179	2007-04-20	2010-03-09	Lapsed	United States of America	Device And Method To Eliminate Shorting Induced By Via To Metal Misalignment
09246402	6214675	1999-02-08	2001-04-10	Granted	United States of America	A Method For Fabricating A Merged Integrated Circuit Device
09789254	6627963	2001-02-20	2003-09-30	Granted	United States of America	Method For Fabricating A Merged Integrated Circuit Device
10300254	6762457	2002-11-20	2004-07-13	Granted	United States of America	LDMOS Device Having A Tapered Oxide
09641086	6506641	2000-08-17	2003-01-14	Granted	United States of America	The Use Of Selective Oxidation To Improve LDMOS Power Transistors
11419252	7381607	2006-05-19	2008-06-03	Granted	United States of America	A Method Of Forming A Spiral Inductor In A Semiconductor Substrate
10646997	7075167	2003-08-22	2006-07-11	Lapsed	United States of America	A Spiral Inductor Formed In A Semiconductor Substrate And A Method For Forming The Inductor
09335646		1999-06-18		Abandoned	United States of America	A CMOS Integrated Circuit Having Vertical Transistors And A Process For Fabricating Same
10211674	6653181	2002-08-02	2003-11-25	Granted	United States of America	A CMOS Integrated Circuit Having Vertical Transistors And A Process For Fabricating Same
10918981	7345354	2004-08-16	2008-03-18	Granted	United States of America	Increased Quality Factor Of A Varactor In An Integrated Circuit Via A High Conductive Region In A Well
10454133	6825089	2003-06-04	2004-11-30	Granted	United States of America	Increased Quality Factor Of A Varactor In An Integrated Circuit Via A High Conductive Region In A Well
09652479	6373087	2000-08-31	2002-04-16	Granted	United States of America	Methods of Fabricating A Metal-Oxide-Metal Capacitor And Associated Apparatus
10080186	6730601	2002-02-21	2004-05-04	Granted	United States of America	Methods of Fabricating A Metal-Oxide-Metal Capacitor

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11116903	7297606	2005-04-28	2007-11-20	Granted	United States of America	Metal\(miOxide\(miSemiconductor Device Including A Buried Lightly\(miDoped Drain Region
10675633	6927453	2003-09-30	2005-08-09	Lapsed	United States of America	Metal-Oxide-Semiconductor Device Including A Buried Lightly-Doped Drain Region
09540473	6373266	2000-03-31	2002-04-16	Granted	United States of America	Apparatus And Method For Determining Process Width Variations In Integrated Circuits
10053097	6728940	2002-01-18	2004-04-27	Granted	United States of America	Apparatus And Method For Determining Process Width Variations In Integrated Circuits
08353015	5576240	1994-12-09	1996-11-19	Expired	United States of America	Method for Making A Metal to metal Capacitor
08644086	5851870	1996-05-09	1998-12-22	Expired	United States of America	Method For Making A Capacitor
08472033	5654581	1995-06-06	1997-08-05	Expired	United States of America	Integrated Circuit Capacitor
08909563	6040616	1997-08-12	2000-03-21	Expired	United States of America	A Device and Method of Forming A Metal To Metal Capacitor Within an Integrated Circuit
08863713	5825073	1997-05-27	1998-10-20	Expired	United States of America	An Electronic Component For An Integrated Circuit
10179057		2002-06-25		Abandoned	United States of America	A Graded Grown Gate Oxide (G3) For A Vertical Replacement Gate (VRG) MOSFET.
10986984	7169714	2004-11-12	2007-01-30	Granted	United States of America	Method And Structure For Graded Gate Oxides On Vertical And Non-Planar Surfaces
09481992	6541394	2000-01-11	2003-04-01	Granted	United States of America	Method Of Making A Graded Grown, High Quality Oxide Layer For A Semiconductor Device
10171701		2002-06-14		Abandoned	United States of America	Coupling Capacitance Reduction
09906331	6432812	2001-07-16	2002-08-13	Granted	United States of America	Method of coupling capacitance reduction
11392375		2006-03-29		Abandoned	United States of America	High\(miDensity Inter\(miDie Interconnect Structure
10638248	7045835	2003-08-08	2006-05-16	Granted	United States of America	High\(miDensity Inter\(miDie Interconnect Structure
11540056	7239160	2006-09-29	2007-07-03	Granted	United States of America	Method Of Electrical Testing Of An Integrated Circuit With An Electrical Probe
11138152	7132840	2005-05-26	2006-11-07	Granted	United States of America	Method Of Electrical Testing
08979297	5849639	1997-11-26	1998-12-15	Granted	United States of America	Method For Removing Etching Residues And Contaminants
09164283	6046115	1998-10-01	2000-04-04	Granted	United States of America	Method for Removing Etching Residues and Contaminants
09434424	6284663	1999-11-04	2001-09-04	Granted	United States of America	Method For Making Field Effect Devices And Capacitors With Thin Film Dielectrics And Resulting Devices
09060420	6001741	1998-04-15	1999-12-14	Granted	United States of America	Method For Making Field Effect Devices And Capacitors With Improved Thin Film Dielectrics And Resulting Devices
09651447	6670242	2000-08-30	2003-12-30	Granted	United States of America	Method For Making An Integrated Circuit Device Including A Graded, Grown, High Quality Gate Oxide Layer And A Nitride Layer
09651593		2000-08-30		Abandoned	United States of America	Method For Making An Integrated Circuit Device Including A Graded, Grown, High Quality Gate Oxide Layer And A Gate Electrode Layer With Improved Dopant Activation

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09651857		2000-08-30		Abandoned	United States of America	Integrated Circuit Device Including a Graded, Grown, High Quality Gate Oxide Layer
09651592		2000-08-30		Abandoned	United States of America	Flash Device w\(slG3 (High Temperature) Oxide Grown In FTP or RTP Furnace
09651458		2000-08-30		Abandoned	United States of America	Integrated Circuit Device Including a Graded, Grown, High Quality Gate Oxide Layer And a Nitride Layer
09651450		2000-08-30		Abandoned	United States of America	Method For Making A High Quality, Graded, Grown Gate Oxide Layer Including Native Oxide Removal
09651451		2000-08-30		Abandoned	United States of America	Method For Making An Integrated Circuit Device Including A Graded, Grown, High Quality Gate Oxide Layer
09015981	6153920	1998-01-30	2000-11-28	Expired	United States of America	A Semiconductor Device Configured to Control Dopant Diffusion In the Semiconductor Device Substrate
08862226	5731626	1997-05-23	1998-03-24	Expired	United States of America	Process For Controlling Dopant Diffusion In A Semiconductor Layer And Semiconductor Layer Formed Thereby
09650164	6635116	2000-08-29	2003-10-21	Granted	United States of America	Residual oxygen reduction system
10640530		2003-08-13		Abandoned	United States of America	Residual Oxygen Reduction System
09006918	6133077	1998-01-13	2000-10-17	Granted	United States of America	Formation of high-voltage and low-voltage devices on a semiconductor substrate
09495512	6194766	2000-02-01	2001-02-27	Granted	United States of America	Integrated circuit having low voltage and high voltage devices on a common semiconductor substrate
09724225	6521549	2000-11-28	2003-02-18	Granted	United States of America	Method of reducing silicon oxynitride gate insulator thickness in some transistors of a hybrid integrated circuit to obtain increased differential in gate insulator thickness with other transistors of the hybrid circuit
10304631	6656805	2002-11-26	2003-12-02	Lapsed	United States of America	Method of reducing silicon oxynitride gate insulator thickness in some transistors of a hybrid integrated circuit to obtain increased differential in gate insulator thickness with other transistors of the hybrid circuit
10260824	7118985	2002-09-27	2006-10-10	Lapsed	United States of America	Method of forming a metal-insulator-metal capacitor in an interconnect cavity
09496971	6504202	2000-02-02	2003-01-07	Granted	United States of America	Interconnect-embedded metal-insulator-metal capacitor
09442078	6179956	1999-11-16	2001-01-30	Granted	United States of America	Method and apparatus for using across wafer back pressure differentials to influence the performance of chemical mechanical polishing
09005364		1998-01-09		Abandoned	United States of America	Method And Apparatus For Using Across Wafer Back Pressure Differentials To Influence The Performance Of Chemical Mechanical Polishing

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09427572	6174798	1999-10-26	2001-01-16	Granted	United States of America	Process for forming metal interconnect stack for integrated circuit structure
09261270	6087726	1999-03-01	2000-07-11	Granted	United States of America	Metal interconnect stack for integrated circuit structure
09454257	6297558	1999-12-02	2001-10-02	Expired	United States of America	Slurry filling a recess formed during semiconductor fabrication
08899111	6069085	1997-07-23	2000-05-30	Expired	United States of America	Slurry filling a recess formed during semiconductor fabrication
10706120	6855586	2003-11-12	2005-02-15	Granted	United States of America	Low voltage breakdown element for ESD trigger device
10055082	6710990	2002-01-22	2004-03-23	Granted	United States of America	Low voltage breakdown element for ESD trigger device
10153011	6794756	2002-05-21	2004-09-21	Granted	United States of America	Integrated circuit structure having low dielectric constant material and having silicon oxynitride caps over closely spaced apart metal lines
09425552	6423628	1999-10-22	2002-07-23	Granted	United States of America	Method of forming integrated circuit structure having low dielectric constant material and having silicon oxynitride caps over closely spaced apart metal lines
09583434	6383332	2000-05-31	2002-05-07	Granted	United States of America	Endpoint detection method and apparatus which utilize a chelating agent to detect a polishing endpoint
09212503	6117779	1998-12-15	2000-09-12	Granted	United States of America	Endpoint detection method and apparatus which utilize a chelating agent to detect a polishing endpoint
08768905	5821572	1996-12-17	1998-10-13	Expired	United States of America	Simple BICMOS process for creation of low trigger voltage SCR and zener diode pad protection
09081475	6130117	1998-05-19	2000-10-10	Expired	United States of America	Simple BICMOS process for creation of low trigger voltage SCR and zener diode pad protection
08469293		1995-06-06		Abandoned	United States of America	Polymorphic Rectilinear Thieving Pad
08781992	5736680	1997-01-06	1998-04-07	Expired	United States of America	Polymorphic rectilinear thieving pad
09395507	6328802	1999-09-14	2001-12-11	Granted	United States of America	Method and apparatus for determining temperature of a semiconductor wafer during fabrication thereof
09952540	6794310	2001-09-14	2004-09-21	Granted	United States of America	Method and apparatus for determining temperature of a semiconductor wafer during fabrication thereof
09070188	5920110	1998-04-30	1999-07-06	Expired	United States of America	Antifuse device for use on a field programmable interconnect chip
08534008	5844297	1995-09-26	1998-12-01	Expired	United States of America	Antifuse device for use on a field programmable interconnect chip
09245193	6063672	1999-02-05	2000-05-16	Granted	United States of America	NMOS electrostatic discharge protection device and method for CMOS integrated circuit
09476295		1999-12-30		Abandoned	United States of America	NMOS Electrostatic Discharge Protection Device and Method for CMOS Integrated Circuit
09072705	6066560	1998-05-05	2000-05-23	Granted	United States of America	Non-linear circuit elements on integrated circuits
09467340	6228767	1999-12-20	2001-05-08	Granted	United States of America	Non-linear circuit elements on integrated circuits
09228906	6261406	1999-01-11	2001-07-17	Lapsed	United States of America	Confinement device for use in dry etching of substrate surface and method of dry etching a wafer surface

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09884805	6852243	2001-06-18	2005-02-08	Lapsed	United States of America	Confinement device for use in dry etching of substrate surface and method of dry etching a wafer surface
10893659	7071094	2004-07-16	2006-07-04	Granted	United States of America	Dual layer barrier film techniques to prevent resist poisoning
11418873	7393780	2006-05-04	2008-07-01	Granted	United States of America	Dual layer barrier film techniques to prevent resist poisoning
09896363	6812134	2001-06-28	2004-11-02	Granted	United States of America	Dual layer barrier film techniques to prevent resist poisoning
12947948	8289051	2010-11-17	2012-10-16	Lapsed	United States of America	Input/Output Core Design and Method of Manufacture Therefor
13443691		2012-04-10		Abandoned	United States of America	Input/Output Core Design and Method of Manufacture Therefor
2008801316818	ZL200880131681.8	2008-09-19	2013-06-19	Lapsed	China	Allotropic Or Morphologic Change In Silicon Induced By Electromagnetic Radiation For Resistance Tuning Of Integrated Circuits
14073526		2013-11-06		Abandoned	United States of America	Allotropic Or Morphologic Change In Silicon Induced By Electromagnetic Radiation For Resistance Tuning Of Integrated Circuits
098130968	I413235	2009-09-14	2013-10-21	Lapsed	Taiwan	Allotropic Or Morphologic Change In Silicon Induced By Electromagnetic Radiation For Resistance Tuning Of Integrated Circuits
13119005	8610215	2011-03-15	2013-12-17	Granted	United States of America	Allotropic Or Morphologic Change In Silicon Induced By Electromagnetic Radiation For Resistance Tuning Of Integrated Circuits
1020117008762	10-1306685	2008-09-19	2013-09-04	Lapsed	Korea, Republic of (KR)	Allotropic Or Morphologic Change In Silicon Induced By Electromagnetic Radiation For Resistance Tuning Of Integrated Circuits
08430084	5891784	1995-04-27	1999-04-06	Expired	United States of America	Transistor Fabrication Method
08587061	6498080	1996-01-16	2002-12-24	Expired	United States of America	Transistor Fabrication Method
12114589		2008-05-02		Abandoned	United States of America	Transistor Fabrication Method
10224220		2002-08-20		Abandoned	United States of America	Transistor Fabrication Method
12689749	8030199	2010-01-19	2011-10-04	Granted	United States of America	Transistor Fabrication Method
08832245	5780329	1997-04-03	1998-07-14	Expired	United States of America	Process for fabricating a moderate-depth diffused emitter bipolar transistor in a BICMOS device without using an additional mask
08823305	6211096	1997-03-21	2001-04-03	Expired	United States of America	Tunable dielectric constant oxide and method of manufacture
2000008156	4777494	2000-01-17	2011-07-08	Granted	Japan	Pyrogenic Devoid Wet Oxidation
09231265	6335295	1999-01-15	2002-01-01	Granted	United States of America	Flame-free wet oxidation
10094520	6654226	2002-03-08	2003-11-25	Lapsed	United States of America	Thermal low k dielectrics
09064802	6418353	1998-04-22	2002-07-09	Granted	United States of America	Automating photolithography in the fabrication of integrated circuits
1998287829	4555410	1998-10-09	2010-07-23	Lapsed	Japan	Apparatus And A Method For Forming An Oxide Film On A Semiconductor

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09474666	6323106	1999-12-29	2001-11-27	Granted	United States of America	Dual nitrogen implantation techniques for oxynitride formation in semiconductor devices
1998096236	4565674	1998-04-08	2010-08-13	Lapsed	Japan	Pre-Conditioning Polishing Pads For Chemical-Mechanical Polishing
87102678	115428	1998-02-25	2000-05-11	Lapsed	Taiwan	Method For Artificially-Inducing Reverse Short-Channel Efforts In Deep Sub-Micron Cmos Devices
09098019	6147409	1998-06-15	2000-11-14	Granted	United States of America	Modified multilayered metal line structure for use with tungsten-filled vias in integrated circuit structures
09920890	6601008	2001-08-02	2003-07-29	Granted	United States of America	Parametric device signature
09098032	6037262	1998-06-15	2000-03-14	Granted	United States of America	Process for forming vias, and trenches for metal lines, in multiple dielectric layers of integrated circuit structure
87103103	135215	1998-03-04	2001-06-07	Lapsed	Taiwan	Insulated-Gate Field-Effect Transistors Having Different Gate Capacitances
09896958	6358806	2001-06-29	2002-03-19	Granted	United States of America	Silicon carbide CMOS channel
10014449	4381491	1998-01-27	2009-10-02	Lapsed	Japan	Insulated-Gate Field-Effect Transistors Having Different Gate Capacitances
1998094757	4996781	1998-04-07	2012-05-18	Lapsed	Japan	Process For Forming Improved Cobalt Silicide Layer On Integrated Circuit Structure Using Two Capping Layers.
1998051650	4881497	1998-03-04	2011-12-09	Lapsed	Japan	Method And Apparatus For Eliminating Peeling At End Edge Of Semiconductor Substrate In Metal Organic Chemical Vapor Deposition Of Titanium Nitrite
09081337	6073361	1998-05-19	2000-06-13	Granted	United States of America	Apparatus for externally monitoring RPM of spin rinse dryer
09069027	6037233	1998-04-27	2000-03-14	Granted	United States of America	Metal-encapsulated polysilicon gate and interconnect
09063801	6061814	1998-04-21	2000-05-09	Granted	United States of America	Test circuitry for determining the defect density of a semiconductor process as a function of individual metal layers
09079413	6166422	1998-05-13	2000-12-26	Granted	United States of America	Inductor with cobalt/nickel core for integrated circuit structure with high inductance and high Q-factor
9762865	0271949	1997-11-25	2000-08-21	Lapsed	Korea, Republic of (KR)	Method For Artificially-Inducing Reverse Short-Channel Effects In Deep Sub-Micron Cmos Devices
09046113	6013952	1998-03-20	2000-01-11	Granted	United States of America	Structure and method for measuring interface resistance in multiple interface contacts and via structures in semiconductor devices
09076399	6331468	1998-05-11	2001-12-18	Granted	United States of America	Formation of integrated circuit structure using one or more silicon layers for implantation and out-diffusion in formation of defect-free source/drain regions and also for subsequent formation of silicon nitride spacers
08979733		1997-11-26		Abandoned	United States of America	Purging Gas Control Structure For Cvd Chamber

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09081403		1998-05-18		Abandoned	United States of America	Integrated Circuit Structure With Thin Dielectric Between At Least Local Interconnect Level And First Metal Interconnect Level, And Process For Making Same
09882124	6503828	2001-06-14	2003-01-07	Granted	United States of America	Process for selective polishing of metal-filled trenches of integrated circuit structures
09076502	6127286	1998-05-11	2000-10-03	Granted	United States of America	Apparatus and process for deposition of thin film on semiconductor substrate while inhibiting particle formation and deposition
09150220	6248180	1998-09-09	2001-06-19	Granted	United States of America	Method for removing particles from a semiconductor wafer
09037588	6087229	1998-03-09	2000-07-11	Granted	United States of America	Composite semiconductor gate dielectrics
09210184	6288773	1998-12-11	2001-09-11	Granted	United States of America	Method and apparatus for removing residual material from an alignment mark of a semiconductor wafer
08990315	6059637	1997-12-15	2000-05-09	Granted	United States of America	Process for abrasive removal of copper from the back surface of a silicon substrate
08915000	5865666	1997-08-20	1999-02-02	Expired	United States of America	Apparatus and method for polish removing a precise amount of material from a wafer
08887910	5902704	1997-07-02	1999-05-11	Expired	United States of America	Process for forming photoresist mask over integrated circuit structures with critical dimension control
08991397	6162714	1997-12-16	2000-12-19	Granted	United States of America	Method of forming thin polygates for sub quarter micron CMOS process
08919394	5851890	1997-08-28	1998-12-22	Expired	United States of America	Process for forming integrated circuit structure with metal silicide contacts using notched sidewall spacer on gate electrode
08914854	5882251	1997-08-19	1999-03-16	Expired	United States of America	Chemical mechanical polishing pad slurry distribution grooves
08879659	5933757	1997-06-23	1999-08-03	Expired	United States of America	Etch process selective to cobalt silicide for formation of integrated circuit structures
08351516	5627099	1994-12-07	1997-05-06	Expired	United States of America	Method of manufacturing semiconductor device
08942991	5944585	1997-10-02	1999-08-31	Expired	United States of America	Use of abrasive tape conveying assemblies for conditioning polishing pads
08918846	5931719	1997-08-25	1999-08-03	Expired	United States of America	Method and apparatus for using pressure differentials through a polishing pad to improve performance in chemical mechanical polishing
08772310	5769692	1996-12-23	1998-06-23	Expired	United States of America	On the use of non-spherical carriers for substrate chemi-mechanical polishing
08760466	5770520	1996-12-05	1998-06-23	Expired	United States of America	Method of making a barrier layer for via or contact opening of integrated circuit structure
08833597	5902129	1997-04-07	1999-05-11	Expired	United States of America	Process for forming improved cobalt silicide layer on integrated circuit structure using two capping layers

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08730809	5717490	1996-10-17	1998-02-10	Expired	United States of America	Method for identifying order skipping in spectroreflective film measurement equipment
08592870	5953631	1996-01-24	1999-09-14	Expired	United States of America	Low stress, highly conformal CVD metal thin film
08586587	6303995	1996-01-11	2001-10-16	Expired	United States of America	Sidewall structure for metal interconnect and method of making same
08475028	5661069	1995-06-06	1997-08-26	Expired	United States of America	Method of forming an MOS-type integrated circuit structure with a diode formed in the substrate under a polysilicon gate electrode to conserve space
2000322452	3527700	2000-10-23	2004-02-27	Lapsed	Japan	Low Dielectric Constant Silicon Oxide-Based Dielectric Layer for Integrated Circuit Structures Having Improved Compatibility with Via Filler Materials, and Method of Making Same
11524107	7408227	2006-09-20	2008-08-05	Granted	United States of America	Apparatus and method of manufacture for integrated circuit and CMOS device including epitaxially grown dielectric on silicon carbide
09777996	6724404	2001-02-06	2004-04-20	Granted	United States of America	Cluster tool reporting system
989197264	69831734.3	1998-04-02	2005-09-28	Granted	Germany (Federal Republic of)	Process for Fabricating a Moderate-Depth Diffused Emitter Bipolar Transistor in a BICMOS Device Without Using an Additional Mask
013033220	60145418.9	2001-04-09	2011-10-05	Lapsed	Germany (Federal Republic of)	Copper ICs Interconnect
2012122801	5744790	2012-05-30	2015-05-15	Granted	Japan	Damascene Capacitors For Integrated Circuits
200864008		2000-05-10		Abandoned	Japan	Damascene Capacitors For Integrated Circuits
09405805	6225215	1999-09-24	2001-05-01	Granted	United States of America	Method for enhancing anti-reflective coatings used in photolithography of electronic devices
10973851	7204920	2004-10-25	2007-04-17	Granted	United States of America	Contact ring design for reducing bubble and electrolyte effects during electrochemical plating in manufacturing
10945777	7300869	2004-09-20	2007-11-27	Granted	United States of America	Integrated barrier and seed layer for copper interconnect technology
10953322	7550236	2004-09-29	2009-06-23	Lapsed	United States of America	MULTI WAVELENGTH MULTI LAYER PRINTING
11012003	7372547	2004-12-14	2008-05-13	Granted	United States of America	Process and apparatus for achieving single exposure pattern transfer using maskless optical direct write lithography
10984286	7148556	2004-11-09	2006-12-12	Granted	United States of America	High performance diode-implanted voltage-controlled poly resistors for mixed-signal and RF applications
09426061	6756674	1999-10-22	2004-06-29	Granted	United States of America	Low dielectric constant silicon oxide-based dielectric layer for integrated circuit structures having improved compatibility with via filler materials, and method of making same
10949760	7315360	2004-09-24	2008-01-01	Granted	United States of America	Surface coordinate system

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10820494	7119432	2004-04-07	2006-10-10	Lapsed	United States of America	Method and apparatus for establishing improved thermal communication between a die and a heatspreader in a semiconductor package
60144277		1999-07-15		Expired	United States of America	Field Emitting Device Comprising Field-Concentrating Nanoconductor Assembly And Method For Making The Same
60141657		1999-06-30		Expired	United States of America	Solvent Absorption By CMP Pads And Its Relationship To Pad Chemistry
60130378		1999-04-21		Expired	United States of America	Dark Spin Rinse/Dry
60115525		1999-01-12		Expired	United States of America	Multi-Layered WSi/WSiN/Poly (Optional) Resistor for Si IC's
60110711		1998-12-03		Expired	United States of America	Semiconductor Device With Increased Gate Insulator Lifetime
60117186		1999-01-26		Expired	United States of America	Planarization Technique For HDPCVD FSG Layer
60168036		1999-11-30		Expired	United States of America	MOS Transistor And Method Of Manufacture
60378476		2002-05-07		Expired	United States of America	A Thin Film Toroidal Inductor
60167132		1999-11-23		Expired	United States of America	Electrically Measured IC Wafer Masks Version Control Indicator
09698375	6306780	2000-10-26	2001-10-23	Granted	United States of America	Method For Making A Photoresist Layer Having Increased Resistance To Blistering, Peeling, Lifting, Or Reticulation
09745236	6606371	2000-12-19	2003-08-12	Granted	United States of America	X-Ray System
10159268	6847433	2002-06-03	2005-01-25	Lapsed	United States of America	Holder, System, And Process For Improving Overlay In Lithography
08558997	5814562	1995-11-16	1998-09-29	Expired	United States of America	Process For Semiconductor Device Fabrication
09469090	6375912	1999-12-21	2002-04-23	Granted	United States of America	Electrochemical Abatement Of Perfluorinated Compounds
09519193	6331484	2000-03-06	2001-12-18	Granted	United States of America	Titanium-Tantalum Barrier Layer Film And Method For Forming The Same
1020047013135	10-979658	2003-02-24	2010-08-27	Lapsed	Korea, Republic of (KR)	Monitoring And Control Of A Fabrication Process
09967074	6727165	2001-09-28	2004-04-27	Granted	United States of America	Fabrication of metal contacts for deep-submicron technologies
10883137	7015096	2004-07-01	2006-03-21	Lapsed	United States of America	Bimetallic oxide compositions for gate dielectrics
09652571	6556409	2000-08-31	2003-04-29	Granted	United States of America	An Integrated Circuit Including ESD Circuits For A Multi-Chip Module And A Method Therefor
09956382	6759730	2001-09-18	2004-07-06	Granted	United States of America	Bipolar Junction Transistor Compatible With Vertical Replacement Gate Transistors
10693110	6927177	2003-10-24	2005-08-09	Lapsed	United States of America	Chemical mechanical electropolishing system
10929706	8685633	2004-08-30	2014-04-01	Lapsed	United States of America	Method for Optimizing Wafer Edge Patterning
10158775	6985229	2002-05-30	2006-01-10	Lapsed	United States of America	Overlay Metrology Using Scatterometry Profiling
10875029	7494888	2004-06-23	2009-02-24	Lapsed	United States of America	Device And Method Using Isotopically Enriched Silicon
10439863	6710416	2003-05-16	2004-03-23	Granted	United States of America	Split-Gate Metal-Oxide-Semiconductor Device
10659134	7138292	2003-09-10	2006-11-21	Granted	United States of America	Apparatus and method of manufacture for integrated circuit and CMOS device including epitaxially grown dielectric on silicon carbide
09310388	6750495	1999-05-12	2004-06-15	Granted	United States of America	Damascene Capacitors For Integrated Circuits

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10700791	7023230	2003-11-03	2006-04-04	Lapsed	United States of America	Method for testing IDD at multiple voltages
09298068	6191017	1999-04-22	2001-02-20	Granted	United States of America	A Method Of Forming A Multi-Layered Dual-Polysilicon Structure
09439048	6459946	1999-11-12	2002-10-01	Granted	United States of America	Method And System For Determining Operating Staffing
09437930	6424160	1999-11-10	2002-07-23	Granted	United States of America	Testing Insulation Between Conductors
09286869	6048256	1999-04-06	2000-04-11	Granted	United States of America	Apparatus And Method For Continuous Delivery And Conditioning Of A Polishing Slurry
09095468	6388290	1998-06-10	2002-05-14	Granted	United States of America	Single Crystal Silicon On Polycrystalline Silicon Integrated Circuits
08907834	6133618	1997-08-14	2000-10-17	Expired	United States of America	A Semiconductor Device Having An Anti\(miReflective Layer And A Method Of Manufacture Thereof
08924730	6074933	1997-09-05	2000-06-13	Expired	United States of America	Integrated Circuit Fabrication
08941556	5972179	1997-09-30	1999-10-26	Expired	United States of America	Silicon IC Contacts Using Composite TiN Barrier Layer
11016014	7075179	2004-12-17	2006-07-11	Granted	United States of America	System for implementing a configurable integrated circuit
10607116	6979251	2003-06-26	2005-12-27	Lapsed	United States of America	Method and apparatus to add slurry to a polishing system
09016475	5994221	1998-01-30	1999-11-30	Granted	United States of America	Device And Method Of Fabricating Vias For ULSI Metallization And Interconnect
09243377	6194750	1999-02-01	2001-02-27	Granted	United States of America	Integrated Circuit Comprising Means For High Frequency Signal Transmission
08853582	5767561	1997-05-09	1998-06-16	Expired	United States of America	Integrated Circuit Devices With Isolated Circuit Elements
10658168	7079966	2003-09-08	2006-07-18	Granted	United States of America	Method of qualifying a process tool with wafer defect maps
08971422	5993947	1997-11-17	1999-11-30	Granted	United States of America	Low Temperature Coefficient Dielectric Material Comprising Binary Calcium Niobate And Calcium Tantalate Oxides
08346806	5549512	1994-11-30	1996-08-27	Expired	United States of America	Mini environment for Hazardous Process Tools
08326444	5510230	1994-10-20	1996-04-23	Expired	United States of America	Device Fabrication Using DUV/EUV Pattern Delineation
08589229	5656399	1996-01-22	1997-08-12	Expired	United States of America	Process for Making An X-Ray Mask
08346810	5441614	1994-11-30	1995-08-15	Expired	United States of America	Method and Apparatus for Planar Magnetron Sputtering
08664227	5670062	1996-06-07	1997-09-23	Expired	United States of America	Method For Producing Tapered Lines
08683291	5656515	1996-07-18	1997-08-12	Expired	United States of America	Method Of Making High-Speed Double-Heterostructure Bipolar Transistor Devices
10452360	7332062	2003-06-02	2008-02-19	Granted	United States of America	Electroplating tool for semiconductor manufacture having electric field control
08413527	5663677	1995-03-30	1997-09-02	Expired	United States of America	Integrated Circuit Multi-Level Interconnection Technique
08439040	5538819	1995-04-10	1996-07-23	Expired	United States of America	Self-Aligned Alignment Marks For Phase-Shifting Masks
08351977	5599730	1994-12-08	1997-02-04	Expired	United States of America	Poly-Buffered LOCOS
08353032	5574291	1994-12-09	1996-11-12	Expired	United States of America	Article Comprising A Thin Film Transistor With Low Conductivity Organic Layer
08918781	5958654	1997-08-25	1999-09-28	Expired	United States of America	Lithographic Process And Energy-Sensitive Material For Use Therein
08324842	6524645	1994-10-18	2003-02-25	Granted	United States of America	A Process For The Electroless Deposition of Metal On A Substrate

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08163967	5959342	1993-12-08	1999-09-28	Expired	United States of America	Semiconductor Device Having A High Voltage Termination Improvement
10410925	6739953	2003-04-09	2004-05-25	Granted	United States of America	Mechanical stress free processing method
07707365	5879997	1991-05-30	1999-03-09	Expired	United States of America	Method For Forming Self Aligned Polysilicon Contact
10423096	6722948	2003-04-25	2004-04-20	Granted	United States of America	Pad conditioning monitor
09547132	6461225	2000-04-11	2002-10-08	Granted	United States of America	Local Area Alloying For Preventing Dishing Of Copper During Chemical Mechannical Polishing (CMP)
10412867	7079963	2003-04-14	2006-07-18	Granted	United States of America	Modified binary search for optimizing efficiency of data collection time
979319175	69709934.2	1997-07-15	2002-01-09	Expired	Germany (Federal Republic of)	Subsonic to Supersonic and Ultrasonic Conditioning of Polishing Pad in a Chemical Mechanical Polishing Apparatus
89123228	NI-165325	2000-11-21	2002-10-21	Lapsed	Taiwan	Method For Making Field Effect Devices And Capacitors With Thin Film Dielectrics And Resulting Devices
91119024	NI-198062	2002-08-22	2004-07-07	Lapsed	Taiwan	Multiple Operating Voltage Vertical Replacement-Gate (VRG) Transistor
90108450	I223427	2001-04-09	2004-11-01	Lapsed	Taiwan	Interconnections To Copper IC's
090113472	NI-157181	2001-06-04	2002-05-11	Lapsed	Taiwan	A Method For Reducing Dishing Related Issues During The Formation Of Shallow Trench Isolation Structures
89104065	NI-144505	2000-03-07	2001-11-11	Granted	Taiwan	Damascene Capacitors For Integrated Circuits
89100158	NI-134826	2000-01-06	2001-10-17	Lapsed	Taiwan	Integrated Circuit Capacitor And Associated Fabrication Methods
87105577	NI-132141	1998-04-13	2001-05-16	Lapsed	Taiwan	Capacitor Comprising Improved Taox-Based Dielectric
90116133	I282168	2001-07-02	2007-06-01	Lapsed	Taiwan	Silicon-On-Insulator (SOI) Semiconductor Structure With Trench Including A Conductive Layer
093110409	I325175	2004-04-14	2010-05-21	Lapsed	Taiwan	Metal-Oxide-Semiconductor Device Including A Buried Lightly-Doped Drain Region
20000064498	675988	2000-11-01	2007-01-23	Lapsed	Korea, Republic of (KR)	Method For Making Field Effect Devices And Capacitors With Thin Film Dielectrics And Resulting Devices
1020010049568	809305	2001-08-17	2008-02-26	Lapsed	Korea, Republic of (KR)	Process For Fabricating A Semiconductor Device Having A Metal Oxide Or A Metal Silicate GateDielectric Layer
1020000001128	699186	2000-01-11	2007-03-19	Lapsed	Korea, Republic of (KR)	Method For Making An Integrated Circuit Including Alignment Marks
1019980018520	505305	1998-05-22	2005-07-25	Lapsed	Korea, Republic of (KR)	Capacitor Comprising Improved Taox-Based Dielectric
1019980050349	495717	1998-11-24	2005-06-08	Lapsed	Korea, Republic of (KR)	Method Of Manufacturing An Integrated Circuit Using Chemical Mechanical Polishing
19990024635	0303937	1999-06-28	2001-07-16	Lapsed	Korea, Republic of (KR)	System And Method Of Manufacturing Semicustom Reticles Using Reticle Primitives
9832710	280565	1998-08-12	2000-11-10	Granted	Korea, Republic of (KR)	A Device and Method of Forming A Metal To Metal Capacitor Within an Integrated Circuit

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
9723238	455640	1997-06-05	2004-10-26	Expired	Korea, Republic of (KR)	Method For Producing Tapered Lines
10335470	7014957	2002-12-31	2006-03-21	Granted	United States of America	Interconnect routing using parallel lines and method of manufacture
1020000016832	367185	2000-03-31	2002-12-23	Lapsed	Korea, Republic of (KR)	Lithographic Process For Device Fabrication Using Dark-Field Illumination
1020000035027	617894	2000-06-24	2006-08-23	Granted	Korea, Republic of (KR)	Semiconductor Device Free Of LDD Regions
1020010019270	707705	2001-04-11	2007-04-09	Lapsed	Korea, Republic of (KR)	Local Area Alloying For Preventing Dishing Of Copper During Chemical Mechannical Polishing (CMP)
1020000074125	753777	2000-12-07	2007-08-24	Lapsed	Korea, Republic of (KR)	Article Comprising A Dielectric Material Of Zr-Ge-Ti-O Or Hf-Ge-Ti-O And Method Of Making The Same
1020060012904	10-1184202	2006-02-10	2012-09-13	Lapsed	Korea, Republic of (KR)	High-Density Field Emission Elements and a Method for Forming Said Emission Elements
1020050085840	10-1215425	2005-09-14	2012-12-18	Granted	Korea, Republic of (KR)	Guard Ring for Improved Matching
1020020056476	10-918779	2002-09-17	2009-09-17	Lapsed	Korea, Republic of (KR)	Bipolar Junction Transistor Compatible With Vertical Replacement Gate Transistors
1020030034713	10-948495	2003-05-30	2010-03-12	Lapsed	Korea, Republic of (KR)	Overlay Metrology Using Scatterometry Profiling
1020020057533	10-908991	2002-09-23	2009-07-16	Lapsed	Korea, Republic of (KR)	Multiple Operating Voltage Vertical Replacement-Gate (VRG) Transistor
2001196104	4931291	2001-06-28	2012-02-24	Lapsed	Japan	Silicon-On-Insulator (SOI) Semiconductor Structure With Trench Including A Conductive Layer
2000135071	3492978	2000-05-08	2003-11-14	Granted	Japan	Improved Wehnelt Gun For Electron Lithography
11015686	3521119	1999-01-25	2004-02-13	Lapsed	Japan	Device And Method Of Fabricating Vias For ULSI Metallization And Interconnect
10227743	3321101	1998-08-12	2002-06-21	Granted	Japan	A Device and Method of Forming A Metal To Metal Capacitor Within an Integrated Circuit
2000233853	3782293	2000-08-02	2006-03-17	Lapsed	Japan	Methods And Apparatus For Testing Integrated Circuits
10313333	6897102	2002-12-06	2005-05-24	Granted	United States of America	Process to minimize polysilicon gate depletion and dopant penetration and to increase conductivity
2003180575	4386680	2003-06-25	2009-10-09	Lapsed	Japan	Capacitor For A Semiconductor Device And Method For Fabrication Therefor
2006035891	5153075	2006-02-14	2012-12-14	Lapsed	Japan	High-Density Field Emission Elements and a Method for Forming Said Emission Elements
2001168642	5239107	2001-06-04	2013-04-12	Lapsed	Japan	A Method For Reducing Dishing Related Issues During The Formation Of Shallow Trench Isolation Structures
2000372277	4358430	2000-12-07	2009-08-14	Lapsed	Japan	A Process for Fabricating Integrated Circuit Devices Having Thin Film Transistors
10245219	6855624	2002-09-17	2005-02-15	Lapsed	United States of America	Low-loss on-chip transmission line for integrated circuit structures and method of manufacture

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09704200	6537923	2000-10-31	2003-03-25	Granted	United States of America	Process for forming integrated circuit structure with low dielectric constant material between closely spaced apart metal lines
983065624	69835260.2	1998-08-18	2006-07-19	Lapsed	Germany (Federal Republic of)	Embedded Thin Film Passive Components
003071784	60000174.1	2000-08-21	2002-05-22	Lapsed	Germany (Federal Republic of)	Semiconductor Device Having Regions Of Insulating Material Formed In A Semiconductor Substrate And Process Of Making The Device
993071026	69902133.2	1999-09-07	2002-07-17	Lapsed	Germany (Federal Republic of)	Method Of Making An Article Comprising An Oxide Layer On A GaAs-Based Semiconductor Body
993064708	69901142.6	1999-08-17	2002-04-03	Granted	Germany (Federal Republic of)	Process For Semiconductor Device Fabrication Having Copper Interconnects
973090285	69724972.7	1997-11-11	2003-09-17	Granted	Germany (Federal Republic of)	Electronic Apparatus
10172849	6917430	2002-06-17	2005-07-12	Lapsed	United States of America	Method to improve the control of source chemicals delivery by a carrier gas
003032737	60032051.0	2000-04-18	2006-11-29	Lapsed	Germany (Federal Republic of)	A Method Of Forming A Multi-Layered Dual-Polysilicon Structure
10078233	6830984	2002-02-15	2004-12-14	Granted	United States of America	Thick traces from multiple damascene layers
10033090	6817941	2001-10-25	2004-11-16	Lapsed	United States of America	Uniform airflow diffuser
10008170	6706583	2001-10-19	2004-03-16	Granted	United States of America	High speed low noise transistor
10053537	6673498	2001-11-02	2004-01-06	Lapsed	United States of America	Method for reticle formation utilizing metal vaporization
09970392	6647348	2001-10-03	2003-11-11	Granted	United States of America	Latent defect classification system
11368780	7476951	2006-03-06	2009-01-13	Granted	United States of America	Selective Isotropic Etch For Titanium Based Materials
08935521	5895960	1997-09-23	1999-04-20	Expired	United States of America	Thin Oxide Mask Level Resistor
09999872	6582568	2001-10-19	2003-06-24	Granted	United States of America	First stage salicidation of cobalt during cobalt deposition or subsequent Ti or Tin cap deposition using energy from a directional plasma
983079187	69832352.1	1998-09-29	2005-11-16	Granted	Germany (Federal Republic of)	Energy-Sensitive Resist Material And A Process For Device Fabrication UsingAn Energy-Sensitive Resist Material
09758603	6741122	2001-01-12	2004-05-25	Granted	United States of America	Routing technique to adjust clock skew using frames and prongs
08924277	6102962	1997-09-05	2000-08-15	Expired	United States of America	Method for estimating quiescent current in integrated circuits
09574771	6506678	2000-05-19	2003-01-14	Granted	United States of America	Integrated circuit structures having low k porous aluminum oxide dielectric material separating aluminum lines, and method of making same
09817642	6476497	2001-03-26	2002-11-05	Granted	United States of America	Concentric metal density power routing
10271860	4094743	1998-09-25	2008-03-14	Lapsed	Japan	A Method and Apparatus for Chemical Mechanical Polishing
09292079	6211051	1999-04-14	2001-04-03	Granted	United States of America	Reduction of plasma damage at contact etch in MOS integrated circuits

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09213847	6177305	1998-12-17	2001-01-23	Granted	United States of America	Fabrication of metal-insulator-metal capacitive structures
87103907	133913	1998-03-17	2001-10-08	Lapsed	Taiwan	Tunable Dielectric Constant Oxide and Method of Manufacture
09112222	6074517	1998-07-08	2000-06-13	Granted	United States of America	Method and apparatus for detecting an endpoint polishing layer by transmitting infrared light signals through a semiconductor wafer
09909175	6970622	2001-07-19	2005-11-29	Lapsed	United States of America	Arrangement and method for controlling the transmission of a light signal based on intensity of a received light signal
08923676	5915414	1997-09-04	1999-06-29	Expired	United States of America	Standardized gas isolation box (GIB) installation
08651018	5966599	1996-05-21	1999-10-12	Expired	United States of America	Method for fabricating a low trigger voltage silicon controlled rectifier and thick field device
08623470	5861652	1996-03-28	1999-01-19	Expired	United States of America	Method and apparatus for protecting functions imbedded within an integrated circuit from reverse engineering
1019980033782	499194	1998-08-20	2005-06-24	Lapsed	Korea, Republic of (KR)	Process For Forming Integrated Circuit Structure With Improved Metal Silicide Contacts Using Notched Sidewall Spacer On Gate Electrode, And Resulting Structure
09703616	6391768	2000-10-30	2002-05-21	Granted	United States of America	Process for CMP removal of excess trench or via filler metal which inhibits formation of concave regions on oxide surface of integrated circuit structure
09948808	6727107	2001-09-07	2004-04-27	Granted	United States of America	Method of testing the processing of a semiconductor wafer on a CMP apparatus
10304974	6867488	2002-11-26	2005-03-15	Lapsed	United States of America	Thick metal top layer
09111271	6114215	1998-07-06	2000-09-05	Granted	United States of America	Generating non-planar topology on the surface of planar and near-planar substrates
09112403	6066266	1998-07-08	2000-05-23	Granted	United States of America	In-situ chemical-mechanical polishing slurry formulation for compensation of polish pad degradation
09928570	6743725	2001-08-13	2004-06-01	Granted	United States of America	High selectivity SiC etch in integrated circuit fabrication
08979734	5914001	1997-11-26	1999-06-22	Expired	United States of America	In-situ etch of CVD chamber
08979733		1997-11-26		Abandoned	United States of America	Gas Control Structure For Cvd Chamber
09072915	5992242	1998-05-04	1999-11-30	Granted	United States of America	Silicon wafer or die strength test fixture using high pressure fluic
09054279	5998226	1998-04-02	1999-12-07	Granted	United States of America	Method and system for alignment of openings in semiconductor fabrication
08995260	6066561	1997-12-19	2000-05-23	Granted	United States of America	Apparatus and method for electrical determination of delamination at one or more interfaces within a semiconductor wafer
08960925	5961375	1997-10-30	1999-10-05	Expired	United States of America	Shimming substrate holder assemblies to produce more uniformly polished substrate surfaces
08984003	5936876	1997-12-03	1999-08-10	Granted	United States of America	Semiconductor integrated circuit core probing for failure analysis
08966637	6028014	1997-11-10	2000-02-22	Granted	United States of America	Plasma-enhanced oxide process optimization and material and apparatus therefor
08895960	6004193	1997-07-17	1999-12-21	Expired	United States of America	Dual purpose retaining ring and polishing pad conditioner

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08926590	6020242	1997-09-04	2000-02-01	Expired	United States of America	Effective silicide blocking
08874055	5985679	1997-06-12	1999-11-16	Expired	United States of America	Automated endpoint detection system during chemical-mechanical polishing
08918483	5893756	1997-08-26	1999-04-13	Expired	United States of America	Use of ethylene glycol as a corrosion inhibitor during cleaning after metal chemical mechanical polishing
08963813	5973398	1997-11-04	1999-10-26	Granted	United States of America	Semiconductor device and fabrication method employing a palladium-plated heat spreader substrate
08786695	5869395	1997-01-22	1999-02-09	Expired	United States of America	Simplified hole interconnect process
08754696	5985746	1996-11-21	1999-11-16	Expired	United States of America	Process for forming self-aligned conductive plugs in multiple insulation levels in integrated circuit structures and resulting product
08596894	5760428	1996-01-25	1998-06-02	Expired	United States of America	Variable width low profile gate array input/output architecture
08520030	5614249	1995-08-28	1997-03-25	Expired	United States of America	Leak detection system for a gas manifold of a chemical vapor deposition apparatus
08486803	5698468	1995-06-07	1997-12-16	Expired	United States of America	Silicidation process with etch stop
08396560	5539246	1995-03-01	1996-07-23	Expired	United States of America	Microelectronic integrated circuit including hexagonal semiconductor gate device
08792479	5773855	1997-01-31	1998-06-30	Expired	United States of America	Microelectronic circuit including silicided field-effect transistor elements that bifunction as interconnects
10015255	6562735	2001-12-11	2003-05-13	Granted	United States of America	Control of reaction rate in formation of low k carbon-containing silicon oxide dielectric material using organosilane, unsubstituted silane, and hydrogen peroxide reactants
09848758	6503840	2001-05-02	2003-01-07	Granted	United States of America	Process for forming metal-filled openings in low dielectric constant dielectric material while inhibiting via poisoning
08627622	5654895	1996-04-04	1997-08-05	Expired	United States of America	Process monitor usig impedance controlled I/O controller
08512678	5663076	1995-08-08	1997-09-02	Expired	United States of America	Automating photolithography in the fabrication of integrated circuits
09808441	6492736	2001-03-14	2002-12-10	Granted	United States of America	Power mesh bridge
2013174500	5710714	2005-03-10	2015-03-13	Lapsed	Japan	A Bipolar Junction Transistor Having A High Germanium Concentration In A Silicon-Germanium Layer And A Method For Forming The Bipolar Junction Transistor
08283296	5474648	1994-07-29	1995-12-12	Expired	United States of America	Uniform and repeatable plasma processing
201184505		2011-04-06		Abandoned	Japan	Method And Structure For DC And RF Shielding Of Integrated Circuits
11534340	7535330	2006-09-22	2009-05-19	Granted	United States of America	LOW MUTUAL INDUCTANCE MATCHED INDUCTORS
2012105770		2012-05-07		Abandoned	Japan	Multiple Operating Voltage Vertical Replacement-Gate (VRG) Transistor

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
1020127015010	10-1216580	2012-06-11	2012-12-21	Granted	Korea, Republic of (KR)	A Bipolar Junction Transistor Having A High Germanium Concentration In A Silicon-Germanium Layer And A Method For Forming The Bipolar Junction Transistor
09730704	6413151	2000-12-06	2002-07-02	Granted	United States of America	CMP slurry recycling apparatus and method for recycling CMP slurry
2012100569		2012-04-26		Abandoned	Japan	An Integrated Circuit Including ESD Circuits For A Multi-Chip Module And A Method Therefor
08475586	5637887	1995-06-07	1997-06-10	Expired	United States of America	Silicon controller rectifier (SCR) with capacitive trigger
08650476	5780347	1996-05-20	1998-07-14	Expired	United States of America	Method of forming polysilicon local interconnects
057254047		2005-03-10		Abandoned	European Patent	A Bipolar Junction Transistor Having A High Germanium Concentration In A Silicon-Germanium Layer And A Method For Forming The Bipolar Junction Transistor
011016839	60133155.9	2001-01-30	2008-03-12	Granted	Germany (Federal Republic of)	Interconnect-Embedded Metal-Insulator-Metal Capacitor and Method of Fabricating Same
08685772	5689134	1996-07-24	1997-11-18	Expired	United States of America	Integrated circuit structure having reduced cross-talk and method of making same
131550428		2005-03-10		Abandoned	European Patent	A Bipolar Junction Transistor Having A High Germanium Concentration In A Silicon-Germanium Layer And A Method For Forming The Bipolar Junction Transistor
2009246032	5404308	2009-10-27	2013-11-08	Granted	Japan	Semiconductor Device Free Of LDD Regions
001226885		2000-10-18		Lapsed	European Patent	Low Dielectric Constant Silicon Oxide-Based Dielectric Layer for Integrated Circuit Structures Having Improved Compatibility with Via Filler Materials, and Method of Making Same
09892250	6559033	2001-06-27	2003-05-06	Granted	United States of America	Processing for forming integrated circuit structure with low dielectric constant material between closely spaced apart metal lines
2009143777	4505036	2009-06-17	2010-04-30	Lapsed	Japan	A Process for Fabricating Integrated Circuit Devices Having Thin Film Transistors
09148028	6340434	1998-09-03	2002-01-22	Granted	United States of America	Method and apparatus for chemical-mechanical polishing
11140142	7106073	2005-05-27	2006-09-12	Lapsed	United States of America	Method and system for area efficient charge-based capacitance measurement
11323405	7429733	2005-12-29	2008-09-30	Granted	United States of America	Method and sample for radiation microscopy including a particle beam channel formed in the sample source
09881151	6914786	2001-06-14	2005-07-05	Lapsed	United States of America	Converter device
10035346	6825546	2001-12-28	2004-11-30	Lapsed	United States of America	CMOS varactor with constant dC/dV characteristic
10966074	7179736	2004-10-14	2007-02-20	Granted	United States of America	Method for fabricating planar semiconductor wafers
11005765	7242074	2004-12-06	2007-07-10	Granted	United States of America	Reduced capacitance resistors
11247517	7284213	2005-10-11	2007-10-16	Granted	United States of America	Defect analysis using a yield vehicle

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11397252	8053824	2006-04-03	2011-11-08	Granted	United States of America	Interdigitated Mesh To Provide Distributed, HIgh Quality Factor Capacitive Coupling
10927802	7137098	2004-08-27	2006-11-14	Granted	United States of America	Pattern component analysis and manipulation
60002275		1995-08-14		Expired	United States of America	A Process For Semiconductor Device Fabrication
60426842		2002-11-15		Expired	United States of America	In-Situ Removal Of Surface Impurities Prior To As Doped Poly Dep
60552308		2004-03-10		Expired	United States of America	Creation of A High Ge Concentration SiGe Layer In BiCMOS Processing Through Thermal Oxidation of the SiGe Base Layer
60541878		2004-02-04		Expired	United States of America	Structure For Improved Heat Conduction For Semiconductor Devices
60115717		1999-01-12		Expired	United States of America	Method Of Making A Graded Grown, High Quality Oxide Layer For A Semiconductor Device
60117242		1999-01-26		Expired	United States of America	Device Comprising Thermally Stable, Low Dielectric Constant Material
10971961	7259083	2004-10-22	2007-08-21	Granted	United States of America	Local interconnect manufacturing process
60115532		1999-01-12		Expired	United States of America	Novel Methods To Fabricate MOM Capacitors
10117487	6878406	2002-04-05	2005-04-12	Lapsed	United States of America	Dynamic use of process temperature
062546304		2006-09-06		Lapsed	European Patent	Robust Shallow Trench Isolation Structures And A Method For Forming Shallow Trench Isolation Structures
60180809		2000-02-07		Expired	United States of America	Improvement Of Thick Photoresist (PR) Integrity For High-Current High-Dose High-Energy Ion Implantation Using A Novel Thermal And UV-Irradiation Treatment
60174566		2000-01-05		Expired	United States of America	An Integrated Circuit And A Method Of Making An Integrated Circuit
10867014	7013192	2004-06-14	2006-03-14	Lapsed	United States of America	Substrate contact analysis
11269275	8076779	2005-11-08	2011-12-13	Granted	United States of America	Reduction of macro level stresses in copper/Low-K wafers
09464297	6759337	1999-12-15	2004-07-06	Granted	United States of America	Process for etching a controllable thickness of oxide on an integrated circuit structure on a semiconductor substrate using nitrogen plasma and plasma and an rf bias applied to the substrate
09972481	6667536	2001-10-05	2003-12-23	Lapsed	United States of America	Thin Film Multi-Layer High Q Transformer Formed In A Semiconductor Substrate
60140666		1999-06-24		Expired	United States of America	Method Of Making A Graded, High Quality Oxide Layer For A Semiconductor Device
60096581		1998-08-14		Expired	United States of America	Process For Fabricating Device Comprising Lead Zirconate Titanate
09271084	6531751	1999-03-17	2003-03-11	Granted	United States of America	Semiconductor Device With Increased Gate Insulator Lifetime
60141656		1999-06-30		Expired	United States of America	Impact Of Post Window Etch Cleans Process On Reliability Of 0.25 (*mm Vintage Windows

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09345039	6368972	1999-06-30	2002-04-09	Granted	United States of America	Method For Making An Integrated Circuit Including Alignment Marks
09376233	6274933	1999-08-17	2001-08-14	Granted	United States of America	An Integrated Circuit Device Having A Planar Interlevel Dielectric Layer
60507335		2003-09-30		Expired	United States of America	A Spiral Inductor Formed In A Semiconductor Substrate
60005141		1995-10-12		Expired	United States of America	A Process For Device Fabrication In Which The Plasma Etch Is Controlled By Monitoring Optical Emission
09345556	6265260	1999-06-30	2001-07-24	Granted	United States of America	Method For Making An Integrated Circuit Capacitor Including Tantalum Pentoxide
09235735	6248394	1999-01-22	2001-06-19	Granted	United States of America	Process For Fabricating Device Comprising Lead Zirconate Titanate
08714909	5835221	1996-09-17	1998-11-10	Expired	United States of America	Process For Fabricating A Device Using Polarized Light To Determine Film Thickness
09113594	6372520	1998-07-10	2002-04-16	Granted	United States of America	Sonic assisted strengthening of gate oxides
60115527		1999-01-12		Expired	United States of America	Technique To Fabricate Gate Mask Photo Alignment Marks For STI
10701328	6939727	2003-11-03	2005-09-06	Lapsed	United States of America	Method for performing statistical post processing in semiconductor manufacturing using ID cells
60326050		2001-09-28		Expired	United States of America	A Resistor Located On A Semiconductor Substrate And A Method of Manufacture Therefor
10928292	7062415	2004-08-27	2006-06-13	Lapsed	United States of America	Parametric outlier detection
10020084	6686272	2001-12-13	2004-02-03	Granted	United States of America	Anti-reflective coatings for use at 248 nm and 193 nm
10799851	7299158	2004-03-12	2007-11-20	Granted	United States of America	Process control data collection
60145127		1999-07-22		Expired	United States of America	Article Comprising Aligned Carbon Nanotubes With Reduced Diameter And Method For Making The Same
2007503058	5393027	2005-03-10	2013-10-25	Granted	Japan	A Bipolar Junction Transistor Having A High Germanium Concentration In A Silicon-Germanium Layer And A Method For Forming The Bipolar Junction Transistor
60149036		1999-08-16		Expired	United States of America	Electrochemical Abatement Of Perfluorinated Compounds
60013093		1996-03-08		Expired	United States of America	An Energy-Sensitive Resist Material And A Process For Device Fabrication Using An Energy-Sensitive Resist Material
09369802	6538367	1999-08-06	2003-03-25	Granted	United States of America	Field Emitting Device Comprising Field-Concentrating Nanoconductor Assembly And Method For Making The Same
60135565		1999-05-24		Expired	United States of America	Use Of Titanium-Tantalum Alloy As A Diffusion Barrier Material For CopperInterconnects
60115881		1999-01-14		Expired	United States of America	A 3-Step Passivation-Depassivation-Passivation D 2 Annealing Process For Hot Carrier Immunity And Transistor Matching
60007002		1995-10-16		Expired	United States of America	A Process For Fabricating A Device Using Polarized Light To Determine Film Thickness
09131860	6136672	1998-08-10	2000-10-24	Granted	United States of America	Process For Device Fabrication Using A High-Energy Boron Implant

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10779966	6971944	2004-02-17	2005-12-06	Lapsed	United States of America	Method and control system for improving CMP process by detecting and reacting to harmonic oscillation
60060869		1997-10-02		Expired	United States of America	An Energy-Sensitive Resist Material And A Process For Device Fabrication Using An Energy-Sensitive Resist Material
10668875	7071811	2003-09-23	2006-07-04	Lapsed	United States of America	High performance voltage control diffusion resistor
09480224	6359339	2000-01-10	2002-03-19	Granted	United States of America	Multi-Layered Metal Silicide Resistor For Si IC's
10505197	7972440	2005-06-10	2011-07-05	Granted	United States of America	Monitoring And Control Of A Fabrication Process
60172654		1999-12-20		Expired	United States of America	X-Ray System
60082076		1998-04-17		Expired	United States of America	Process For Device Fabrication Using A High-Energy Boron Implant
60294566		2001-06-01		Expired	United States of America	Process For Controlling Alignment In A Lithographic Process And Apparatus Therefor
10713951	7166492	2003-11-14	2007-01-23	Granted	United States of America	Integrated circuit carrier apparatus method and system
10513121	7132297	2004-10-27	2006-11-07	Granted	United States of America	Multi-Layer Inductor Formed In A Semiconductor Substrate And Having A Core Of Ferromagnetic Material
1020067018437	10-1173526	2005-03-10	2012-08-07	Granted	Korea, Republic of (KR)	A Bipolar Junction Transistor Having A High Germanium Concentration In A Silicon-Germanium Layer And A Method For Forming The Bipolar Junction Transistor
09594189	6365503	2000-06-14	2002-04-02	Granted	United States of America	A Method Of Inmproving Electromigration In Semiconductor Device Manufacturing Processes
09879783	6765806	2001-06-12	2004-07-20	Granted	United States of America	Composition with EMC shielding characteristics
09296001	6469390	1999-04-21	2002-10-22	Granted	United States of America	Device Comprising Thermally Stable, Low Dielectric Constant Material
10690861	6909591	2003-10-22	2005-06-21	Lapsed	United States of America	Complimentary metal oxide semiconductor capacitor and method for making same
10721971	6998343	2003-11-24	2006-02-14	Lapsed	United States of America	Method for creating barrier layers for copper diffusion
09611844	6503841	2000-07-07	2003-01-07	Granted	United States of America	Oxide Etch
08703756	5877032	1996-08-27	1999-03-02	Expired	United States of America	A Process For Device Fabrication In Which The Plasma Etch Is Controlled By Monitoring Optical Emission
09472332	6290822	1999-12-23	2001-09-18	Granted	United States of America	Sputtering Method For Forming Dielectric Films
09641160	6479404	2000-08-17	2002-11-12	Granted	United States of America	Process For Fabricating A Semiconductor Device Having A Metal Oxide Or A Metal Silicate Gate Dielectric Layer
10156242	6708574	2002-05-24	2004-03-23	Granted	United States of America	Abnormal Photoresist Line\(slSpace Profile Detection Through Signal Processing Of Metrology Waveform
09510015	6361614	2000-02-22	2002-03-26	Granted	United States of America	Method And Apparatus For Dark Spin Rinse/Dry Semiconductor Processing
09514832	6439968	2000-02-28	2002-08-27	Granted	United States of America	A Polishing Pad Having A Water-Repellant Film Thereon And A Method Of Manufacture Therefor
09650604	7439146	2000-08-30	2008-10-21	Granted	United States of America	Field Plated Resistor With Enhanced Routing Area Thereover

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09483297	6465132	2000-01-14	2002-10-15	Granted	United States of America	Article Comprising Small Diameter Nanowires And Method For Making The Same
09378856	6187665	1999-08-23	2001-02-13	Granted	United States of America	A process For Deuterium Passivation And Hot Carrier Immunity
10675575	7556048	2003-09-30	2009-07-07	Lapsed	United States of America	In-Situ Removal Of Surface Impurities Prior TO Arsenic-Doped Polysilicon In The Fabrication Of Heterojuntion Biloplar Transistor
09426453	6297063	1999-10-25	2001-10-02	Granted	United States of America	In-Situ Nano-Interconnected Circuit Devices And Method For Making The Same
09364367	6153901	1999-07-30	2000-11-28	Granted	United States of America	Integrated Circuit Capacitor Including Anchored Plug
09366388	6560735	1999-08-03	2003-05-06	Granted	United States of America	Methods And Apparatus For Testing Integrated Circuits
10650395	7067882	2003-08-28	2006-06-27	Lapsed	United States of America	High quality factor spiral inductor that utilizes active negative capacitance
09521768	6319095	2000-03-09	2001-11-20	Granted	United States of America	Colloidal Suspension Of Abrasive Particles Containing Magnesium As CMP Slurry
09451053	6576980	1999-11-30	2003-06-10	Granted	United States of America	Surface Treatment Anneal Of Hydrogenated Silicon-Oxy-Carbide Dielectric Layer
09334977	6417570	1999-06-17	2002-07-09	Granted	United States of America	Layered Dielectric Film Structure Suitable For Gate Dielectric Application In Sub\(mi0.25 ìm Technologies
09140275	6080625	1998-08-26	2000-06-27	Granted	United States of America	Method For Making Dual-Polysilicon Structures In Integrated Circuits
10723701	7183787	2003-11-26	2007-02-27	Granted	United States of America	Contact resistance device for improved process control
2003572051	4737933	2003-02-24	2011-05-13	Lapsed	Japan	Monitoring And Control Of A Fabrication Process
09653297	6548892	2000-08-31	2003-04-15	Granted	United States of America	Low K Dielectric Insulator and Method of Forming Semiconductor Circuit Structures
10026407	6730588	2001-12-20	2004-05-04	Granted	United States of America	Method of forming SiGe gate electrode
09759120	6509242	2001-01-12	2003-01-21	Granted	United States of America	Heterojunction Bipolar Transistor
10736386	7653523	2003-12-15	2010-01-26	Lapsed	United States of America	Method For Calculating High-Resolution Wafer Parameter Profiles
09121284	6013958	1998-07-23	2000-01-11	Granted	United States of America	Apparatus and Method for Integrated Circuit With Variable Capacitor
10730554	6984869	2003-12-08	2006-01-10	Lapsed	United States of America	High performance diode implanted voltage controlled p-type diffusion resistor
09232418	6111750	1999-01-15	2000-08-29	Granted	United States of America	Electronic Apparatus
09236933	6283812	1999-01-25	2001-09-04	Granted	United States of America	Article Comprising Aligned, Truncated Carbon Nanotubes And Process For Fabricating Article
09277778	6218255	1999-03-29	2001-04-17	Granted	United States of America	Method Of Making A Capacitor
09911364	6844236	2001-07-23	2005-01-18	Granted	United States of America	Method And Structure For DC And RF Shielding Of Integrated Circuits
10644116	7245758	2003-08-20	2007-07-17	Granted	United States of America	Whole-wafer photoemission analysis
09311631	6358865	1999-05-14	2002-03-19	Granted	United States of America	Oxidation Of Silicon Using Fluorine Implant

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09363758	6153268	1999-07-29	2000-11-28	Granted	United States of America	Method For Producing Oriented Piezoelectric Films
09388297	6350659	1999-09-01	2002-02-26	Granted	United States of America	Semiconductor Device Having Regions Of Insulating Material Formed In A Semiconductor Substrate And Process Of Making The Device
09140270	6348393	1998-08-26	2002-02-19	Granted	United States of America	A Capacitor In An Integrated Circuit And A Method Of Manufacturing An Integrated Circuit
09153522	6103607	1998-09-15	2000-08-15	Granted	United States of America	Manufacture Of Mosfet Devices
10261463	6940151	2002-09-30	2005-09-06	Granted	United States of America	Silicon-Rich Low Thermal Budget Silicon Nitride For Integrated Circuits
10260693	6784478	2002-09-30	2004-08-31	Granted	United States of America	Plate Capacitor Structure And Fabrication Method Therefor In A Dual Damascene Process
09236966	6250984	1999-01-25	2001-06-26	Granted	United States of America	Article Comprising Enhanced Nanotube Emitter Structure And Process For Fabricating Article
09108848	6284413	1998-07-01	2001-09-04	Granted	United States of America	System and Method of Manufacturing Semicustom Reticles Using Reticle Primitives
10153231	6686662	2002-05-21	2004-02-03	Granted	United States of America	A Semiconductor Device Barrier Layer
09283528	6379868	1999-04-01	2002-04-30	Granted	United States of America	Lithographic Process For Device Fabrication Using Dark-Field Illumination
10953750	7067890	2004-09-29	2006-06-27	Lapsed	United States of America	Thick Oxide Region In A Semiconductor Device
09082924	6192290	1998-05-21	2001-02-20	Granted	United States of America	System And Method Of Manufacturing Semicustom Integrated Circuits Using Reticle Primitives From A Library And Interconnect Reticles
09456210	6197663	1999-12-07	2001-03-06	Granted	United States of America	A Process For Fabricating Integrated Circuit Devices Having Thin Film Transistors
09226730	6107684	1999-01-07	2000-08-22	Granted	United States of America	Semiconductor Device Having a Signal Pin with Multiple Connections
08847704	6023093	1997-04-28	2000-02-08	Expired	United States of America	Deuterated Dielectric And Polysilicon Film-Based Semiconductor Devices And Method Of Manufacture Thereof
09080430	6002113	1998-05-18	1999-12-14	Granted	United States of America	Apparatus For Processing Silicon Device With Improved Temperature Control
10658017	6865435	2003-09-08	2005-03-08	Lapsed	United States of America	Method of translating a net description of an integrated circuit die
09152189	6101371	1998-09-12	2000-08-08	Granted	United States of America	Article Comprising An Inductor
08568040	5589416	1995-12-06	1996-12-31	Expired	United States of America	Process For Forming Integrated Capacitors
08555594	5648699	1995-11-09	1997-07-15	Expired	United States of America	Field Emission Devices Employing Improved Emitters On Metal Foil And Methods For Making Such Devices
09999848	6734081	2001-10-24	2004-05-11	Granted	United States of America	Shallow trench isolation structure for laser thermal processing
10668021	7081037	2003-09-22	2006-07-25	Lapsed	United States of America	Pad conditioner setup
10719195	6890804	2003-11-21	2005-05-10	Granted	United States of America	Metal-Oxide-Semiconductor Device Formed in Silicon-On-Insulator

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08957122	6556703	1997-10-24	2003-04-29	Expired	United States of America	Scanning Electron Microscope System And Method Of Manufacturing An Integrated Circuit
08538317	5552355	1995-10-03	1996-09-03	Expired	United States of America	Compensation Of The Temperature Coefficient Of The Dielectric Constant Of Barium Strontium Titanate
09280387	6323537	1999-03-29	2001-11-27	Granted	United States of America	A Capacitor For An Integrated Circuit
10675569	7137400	2003-09-30	2006-11-21	Granted	United States of America	Bypass Loop Gas Flow Calibration
10151887	6797525	2002-05-22	2004-09-28	Granted	United States of America	Fabrication Process For A Semiconductor Device Having A Metal Oxide Dielectric Material With A High Dielectric Constant, Annealed With A Buffered Anneal Process
09742855	6625250	2000-12-19	2003-09-23	Granted	United States of America	Optical Structures And Methods For X-Ray Applications
08534356	5642014	1995-09-27	1997-06-24	Expired	United States of America	Self-Powered Devices
09310701	6492647	1999-05-07	2002-12-10	Granted	United States of America	Improved Wehnelt Gun For Electron Lithography
08509930	5739562	1995-08-01	1998-04-14	Expired	United States of America	Combined Photogate And Photodiode Active Pixel Image Sensor
10180910	6847077	2002-06-25	2005-01-25	Granted	United States of America	Capacitor For A Semiconductor Device And Method For Fabrication Therefor
10767205	7037820	2004-01-30	2006-05-02	Granted	United States of America	Cross-Fill Pattern For Metal Fill Levels, Power-Supply Filtering, And Analog Circuit Shielding
09409115	6322934	1999-09-30	2001-11-27	Granted	United States of America	Method For Making Integrated Circuits Including Features With A Relatively Small Critical Dimension
10629496	6818516	2003-07-29	2004-11-16	Lapsed	United States of America	Selective high k dielectrics removal
09364366	6204186	1999-07-30	2001-03-20	Granted	United States of America	Method Of Making Integrated Circuit Capacitor Including Tapered Plug
08380774	5598056	1995-01-31	1997-01-28	Expired	United States of America	Multilayer Pillar Structure For Improved Field Emission Devices
08903974	6566224	1997-07-31	2003-05-20	Expired	United States of America	Process For Device Fabrication
08355787	5670376	1994-12-14	1997-09-23	Expired	United States of America	Methodology For Monitoring Solvent Quality
09178720	6218077	1998-10-26	2001-04-17	Granted	United States of America	Method Of Manufacturing An Integrated Circuit Using A Scanning System And A Scanning System
09209787	6339246	1998-12-11	2002-01-15	Granted	United States of America	Tungsten Silicide Nitride As An Electrode For Tantalum Pentoxide Devices
08431355	5620573	1995-04-28	1997-04-15	Expired	United States of America	Reduced Stress Tungsten Deposition
08581665	5681763	1995-12-29	1997-10-28	Expired	United States of America	Method For Making Bipolar Transistors Having Indium Doped Base
09430147	6294465	1999-10-29	2001-09-25	Granted	United States of America	Method For Making Integrated Circuits Having Features With Reduced Critical Dimensions
08350439	5545916	1994-12-06	1996-08-13	Expired	United States of America	High Q, Integrated Inductors
09388166	6436187	1999-09-01	2002-08-20	Granted	United States of America	Process For Fabricating Article Having Substantial Three-Dimensional Order
08751472	5736749	1996-11-19	1998-04-07	Expired	United States of America	Integrated Circuit Device With Inductor Incorporated Therein
09878820	6875702	2001-06-11	2005-04-05	Lapsed	United States of America	Plasma treatment system

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08948874	5912498	1997-10-10	1999-06-15	Expired	United States of America	Article Comprising An Oxide Layer On GaN
09094920	6200734	1998-06-15	2001-03-13	Granted	United States of America	METHOD FOR FABRICATING SEMICONDUCTOR DEVICES
08344318	5656510	1994-11-22	1997-08-12	Expired	United States of America	Method For Manufacturing Gate Oxide Capacitors Including Wafer Backside Dielectric And Implantation Electron Flood
08775490	6017787	1996-12-31	2000-01-25	Expired	United States of America	Integrated Circuit With Twin Tub
08935121	5981319	1997-09-22	1999-11-09	Expired	United States of America	Method Of Forming A T-Shaped Gate
08393494	5659181	1995-03-02	1997-08-19	Expired	United States of America	Article Comprising alpha-Hexathienyl
09151077	6150271	1998-09-10	2000-11-21	Granted	United States of America	Differential Temperature Control In Chemical Mechanical Polishing Processes
08373732	5631462	1995-01-17	1997-05-20	Expired	United States of America	Laser-Assisted Particle Analysis
09420157	6741019	1999-10-18	2004-05-25	Granted	United States of America	Article Comprising Aligned
08879926	6141050	1997-06-20	2000-10-31	Expired	United States of America	MOS Image Sensor
08366952	5589303	1994-12-30	1996-12-31	Expired	United States of America	Self-Aligned Opaque Regions For Attenuating Phase-Shifting Masks
08366529	5489552	1994-12-30	1996-02-06	Expired	United States of America	Multiple Layer Tungsten Deposition Process
08286606	5472562	1994-08-05	1995-12-05	Expired	United States of America	Method Of Etching Silicon Nitride
08982109	5967885	1997-12-01	1999-10-19	Granted	United States of America	Method Of Manufacturing An Integrated Circuit Using Chemical Mechanical Polishing
08862907	5977582	1997-05-23	1999-11-02	Expired	United States of America	Capacitor Comprising Improved Taox-Based Dielectric
08332179	5623180	1994-10-31	1997-04-22	Expired	United States of America	Electron field emitters comprising particles cooled with low voltage emitting material
10455489	7429749	2003-06-04	2008-09-30	Granted	United States of America	Strained-silicon for CMOS device using amorphous silicon deposition or silicon epitaxial growth
08366515	5532510	1994-12-30	1996-07-02	Expired	United States of America	Reverse Side Etching for Producing Layers with Strain Variation
08570429	5821147	1995-12-11	1998-10-13	Expired	United States of America	Integrated Circuit Fabrication
08587426	5625199	1996-01-16	1997-04-29	Expired	United States of America	Article Comprising Complementary Circuit with Inorganic N-Channel and Organic P-Channel
08749719	6491732	1996-11-15	2002-12-10	Expired	United States of America	Wafer Handling Apparatus and Method
08381262	5561340	1995-01-31	1996-10-01	Expired	United States of America	Field Emission Display Having Corrugated Support Pillars and Method for Manufacturing
08932005	5903493	1997-09-17	1999-05-11	Expired	United States of America	Metal To Metal Capacitor Apparatus And Method For Making
10421421	7442113	2003-04-23	2008-10-28	Lapsed	United States of America	Visual wear confirmation polishing pad
09586384	6500729	2000-06-02	2002-12-31	Granted	United States of America	A Method For Reducing Dishing Related Issues During The Formation Of Shallow Trench Isolation Structures
09611907	6538283	2000-07-07	2003-03-25	Granted	United States of America	Silicon-On-Insulator (SOI) Semiconductor Structure With Trench Including A Conductive Layer
09546037	6620720	2000-04-10	2003-09-16	Granted	United States of America	Interconnections To Copper IC's
09499411	6404027	2000-02-07	2002-06-11	Granted	United States of America	High Dielectric Constant Gate Oxides For Silicon-Based Devices

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10631528	6794304	2003-07-31	2004-09-21	Granted	United States of America	Method and apparatus for reducing microtrenching for borderless vias created in a dual damascene process
09416336	6187647	1999-10-12	2001-02-13	Granted	United States of America	Method Of Manufacturing Lateral High-Q Inductor For Semiconductor Devices
09456807	6437392	1999-12-08	2002-08-20	Granted	United States of America	Article Comprising A Dielectric Material Of Zr-Ge-Ti-O Or Hf-Ge-Ti-O And Method Of Making The Same
09454909	6329281	1999-12-03	2001-12-11	Granted	United States of America	Methods For Fabricating A Multilevel Interconnection For An Integrated Circuit Device Utilizing A Selective Overlayer
10693078	6894524	2003-10-23	2005-05-17	Granted	United States of America	Daisy chain gang testing
89125762	NI-151729	2000-12-04	2002-03-11	Lapsed	Taiwan	A Process For Fabricating Integrated Circuit Devices Having Thin Film Transistors
92114785	I279888	2003-05-30	2007-04-21	Lapsed	Taiwan	Capacitor For A Semiconductor Device And Method For Fabrication Therefor
89108684	NI-159798	2000-07-15	2002-08-01	Lapsed	Taiwan	Improved Wehnelt Gun For Electron Lithography
91118815	NI-190012	2002-08-20	2004-03-04	Granted	Taiwan	A Semiconductor Device Barrier Layer
10698167	6930362	2003-10-30	2005-08-16	Lapsed	United States of America	Calcium doped polysilicon gate electrodes
89112388	NI-204341	2000-06-29	2004-06-21	Granted	Taiwan	Semiconductor Device Free Of LDD Regions
89106001	NI-145942	2000-03-31	2001-12-11	Granted	Taiwan	Apparatus And Method For Continuous Delivery And Conditioning Of A Polishing Slurry
90108664	NI-166224	2001-04-11	2003-03-18	Lapsed	Taiwan	Local Area Alloying For Preventing Dishing Of Copper During Chemical Mechannical Polishing (CMP)
090121356	NI-189135	2001-08-29	2003-11-01	Lapsed	Taiwan	Field Plated Resistor With Enhanced Routing Area Thereover
90121457	NI-180535	2001-08-30	2003-07-01	Lapsed	Taiwan	Low K Dielectric Insulator and Method of Forming Semiconductor Circuit Structures
091100151	NI-193273	2002-01-08	2004-01-01	Granted	Taiwan	Heterojunction Bipolar Transistor
92108572	I300584	2003-04-14	2008-09-01	Lapsed	Taiwan	Overlay Metrology Using Scatterometry Profiling
89100425	NI-138500	2000-02-16	2001-12-05	Lapsed	Taiwan	Method For Making An Integrated Circuit Including Alignment Marks
10368520	6959258	2003-02-18	2005-10-25	Lapsed	United States of America	Methods and structure for IC temperature self-monitoring
093116604	I319598	2004-06-09	2010-01-11	Lapsed	Taiwan	Metal-Oxide-Semiconductor Device Formed in Silicon-On-Insulator
92126350	I315909	2003-09-24	2009-10-11	Granted	Taiwan	Silicon-Rich Low Thermal Budget Silicon Nitride For Integrated Circuits
92125649	I273702	2003-09-17	2007-02-11	Lapsed	Taiwan	Plate Capacitor Structure And Fabrication Method Therefor In A Dual Damascene Process
88104885	NI-138873	1999-03-29	2001-08-21	Granted	Taiwan	Method Of Eliminating Agglomerate Particles In A Polishing Slurry
88105177	NI-122696	1999-04-01	2000-11-01	Lapsed	Taiwan	Apparatus For Processing Silicon Device With Improved Temperature Control
89115497	NI-152144	2000-11-13	2002-03-21	Lapsed	Taiwan	Methods And Apparatus For Testing Integrated Circuits

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
89107369	NI-148715	2000-04-19	2002-01-11	Lapsed	Taiwan	A Method Of Forming A Multi-Layered Dual-Polysilicon Structure
093113007	I325158	2004-05-07	2010-05-21	Lapsed	Taiwan	Split-Gate Metal-Oxide-Semiconductor Device
1020010053350	10-861665	2001-08-31	2008-09-29	Lapsed	Korea, Republic of (KR)	An Integrated Circuit Including ESD Circuits For A Multi-Chip Module And A Method Therefor
1020010052999	10-870256	2001-08-30	2008-11-19	Granted	Korea, Republic of (KR)	Field Plated Resistor With Enhanced Routing Area Thereover
93129464	I362098	2004-09-29	2012-04-11	Lapsed	Taiwan	Inductor Formed In An Integrated Circuit
1020010053414	853360	2001-08-31	2008-08-14	Lapsed	Korea, Republic of (KR)	Low K Dielectric Insulator and Method of Forming Semiconductor Circuit Structures
1020000024335	850034	2000-05-08	2008-07-29	Lapsed	Korea, Republic of (KR)	Improved Wehnelt Gun For Electron Lithography
1019990035378	711526	1999-08-25	2007-04-19	Lapsed	Korea, Republic of (KR)	Process For Semiconductor Device Fabrication Having Copper Interconnects
1020000025275	695028	2000-05-12	2007-03-08	Lapsed	Korea, Republic of (KR)	Damascene Capacitors For Integrated Circuits
19990017990	335703	1999-05-19	2002-04-24	Lapsed	Korea, Republic of (KR)	Method Of Eliminating Agglomerate Particles In A Polishing Slurry
1020000033163	392278	2000-06-16	2003-07-09	Lapsed	Korea, Republic of (KR)	Process For Fabricating Vertical Transistors
1019990003869	0324072	1999-02-05	2002-01-29	Granted	Korea, Republic of (KR)	Electronic Apparatus
9842256	516252	1998-10-09	2005-09-06	Lapsed	Korea, Republic of (KR)	Article Comprising An Oxide Layer On GaN
20000073674	0437743	2000-12-06	2004-06-17	Lapsed	Korea, Republic of (KR)	A Method Of Forming An Alignment Feature In Or On A Multi-Layered Semiconductor Structure
10358968	6986972	2003-02-04	2006-01-17	Lapsed	United States of America	Alternating aperture phase-shift mask fabrication method
20000051024	456705	2000-08-31	2004-11-02	Granted	Korea, Republic of (KR)	Semiconductor Device Having Regions Of Insulating Material Formed In A Semiconductor Substrate And Process Of Making The Device
1019990046565	598471	1999-10-26	2006-07-03	Lapsed	Korea, Republic of (KR)	Method Of Manufacturing An Integrated Circuit Using A Scanning System And A Scanning System
1020000046601	421757	2000-08-11	2004-02-25	Lapsed	Korea, Republic of (KR)	Electrochemical Abatement Of Perfluorinated Compounds
1019990035568	705308	1999-08-26	2007-04-03	Lapsed	Korea, Republic of (KR)	Method For Making Dual-Polysilicon Structures In Integrated Circuits
1019990058177	716436	1999-12-16	2007-05-03	Granted	Korea, Republic of (KR)	Deep Sub-Micron Metal Etch With In-Situ Hard Mask Etch
1019990002654	307421	1999-01-28	2001-08-21	Lapsed	Korea, Republic of (KR)	Device And Method Of Fabricating Vias For ULSI Metallization And Interconnect
9840192	298970	1998-09-28	2001-06-05	Lapsed	Korea, Republic of (KR)	Silicon IC Contacts Using Composite TiN Barrier Layer
9781732	554648	1997-12-31	2006-02-16	Lapsed	Korea, Republic of (KR)	Integrated Circuit With Twin Tub
20000044542	687979	2000-08-01	2007-02-21	Lapsed	Korea, Republic of (KR)	Methods And Apparatus For Testing Integrated Circuits
1020040078024	10-1045195	2004-09-30	2011-06-23	Granted	Korea, Republic of (KR)	Inductor Formed In An Integrated Circuit
20050090978	10-1206628	2005-09-29	2012-11-23	Granted	Korea, Republic of (KR)	Thick Oxide Region In A Semiconductor Device
2001112078	4548759	2001-04-11	2010-07-16	Lapsed	Japan	Local Area Alloying For Preventing Dishing Of Copper During Chemical Mechannical Polishing (CMP)

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
2000373648	5208335	2000-12-08	2013-03-01	Lapsed	Japan	Article Comprising A Dielectric Material Of Zr-Ge-Ti-O Or Hf-Ge-Ti-O And Method Of Making The Same
10392206	6897673	2003-03-19	2005-05-24	Granted	United States of America	Method and integrated circuit for capacitor measurement with digital readout
11353614	4347479	1999-12-13	2009-07-24	Lapsed	Japan	Tungsten Silicide Nitride As An Electrode For Tantalum Pentoxide Devices
1020030033218	10-1003958	2003-05-24	2010-12-20	Granted	Korea, Republic of (KR)	Abnormal Photoresist Line/Space Profile Detection Through Signal Processing of Metrology Waveform
11263647	3725742	1999-09-17	2005-09-30	Lapsed	Japan	Method Of Making An Article Comprising An Oxide Layer On A GaAs-Based Semiconductor Body
2000152242	3445557	2000-05-24	2003-06-27	Granted	Japan	Titanium-Tantalum Barrier Layer Film And Method For Forming The Same
2000003096	3581285	2000-01-12	2004-07-30	Lapsed	Japan	Method For Making An Integrated Circuit Including Alignment Marks
90120871	NI-179943	2001-08-24	2003-06-21	Lapsed	Taiwan	An Integrated Circuit Including ESD Circuits For A Multi-Chip Module And A Method Therefor
89125642	NI-165332	2000-12-01	2002-10-01	Lapsed	Taiwan	A Method Of Forming An Alignment Feature In Or On A Multi-Layered Semiconductor Structure
92108571	I279872	2003-04-14	2007-04-21	Lapsed	Taiwan	Abnormal Photoresist Line/Space Profile Detection Through Signal Processing of Metrology Waveform
89100157	NI-144336	2000-01-06	2002-03-06	Lapsed	Taiwan	Method For Making An Integrated Circuit Capacitor Including Tantalum Pentoxide
10287056	3023090	1998-10-08	2000-01-14	Lapsed	Japan	Article Comprising An Oxide Layer On GaN
11135599	3550315	1999-05-17	2004-04-30	Lapsed	Japan	Apparatus For Processing Silicon Device With Improved Temperature Control
88118471	NI-129146	1999-10-26	2001-04-01	Lapsed	Taiwan	Method Of Manufacturing An Integrated Circuit Using A Scanning System And A Scanning System
88114626	NI-151235	1999-08-26	2002-03-01	Lapsed	Taiwan	Method For Making Dual-Polysilicon Structures In Integrated Circuits
87113667	NI-143565	1998-08-19	2001-10-21	Lapsed	Taiwan	Article Comprising An Oxide Layer On GaN
10303471	3720201	1998-10-26	2005-09-16	Lapsed	Japan	Scanning Electron Microscope System And Method Of Manufacturing An Integrated Circuit
11005911	3062485	1999-01-13	2000-04-28	Lapsed	Japan	Semiconductor Device
09714000	6607967	2000-11-15	2003-08-19	Granted	United States of America	Process for forming planarized isolation trench in integrated circuit structure on semiconductor substrate
10106377	3737277	1998-04-16	2005-11-04	Granted	Japan	Deuterated Dielectric And Polysilicon Film-Based Semiconductor Devices And Method Of Manufacture Thereof

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08262805	3530319	1996-10-03	2004-03-05	Expired	Japan	Compensation Of The Temperature Coefficient Of The Dielectric Constant Of Barium Strontium Titanate
11141016	3550316	1999-05-21	2004-04-30	Lapsed	Japan	Method Of Eliminating Agglomerate Particles In A Polishing Slurry
10171971	3878744	1998-06-19	2006-11-10	Granted	Japan	MOS Image Sensor
11160696	3655497	1999-06-08	2005-03-11	Lapsed	Japan	Single Crystal Silicon On Polycrystalline Silicon Integrated Circuits
11207606	3699301	1999-07-22	2005-07-15	Lapsed	Japan	Apparatus and Method for Integrated Circuit With Variable Capacitor
09283277	3153163	1997-10-16	2001-01-26	Lapsed	Japan	Integrated Circuit Device With Inductor Incorporated Therein
09360176	3253908	1997-12-26	2001-11-22	Granted	Japan	Integrated Circuit With Twin Tub
94128975	I368258	2005-08-24	2012-07-11	Lapsed	Taiwan	Guard Ring for Improved Matching
20030041375	803489	2003-06-25	2008-02-04	Lapsed	Korea, Republic of (KR)	Capacitor For A Semiconductor Device And Method For Fabrication Therefor
1020010018579	857727	2001-04-09	2008-09-03	Lapsed	Korea, Republic of (KR)	Interconnections To Copper IC's
1019990056953	671722	1999-12-11	2007-01-15	Lapsed	Korea, Republic of (KR)	Tungsten Silicide Nitride As An Electrode For Tantalum Pentoxide Devices
19990039502	632613	1999-09-15	2006-09-28	Lapsed	Korea, Republic of (KR)	Manufacture Of Mosfet Devices
1019990017300	304031	1999-05-14	2001-07-18	Lapsed	Korea, Republic of (KR)	Apparatus For Processing Silicon Device With Improved Temperature Control
9834393	373819	1998-08-25	2003-02-13	Lapsed	Korea, Republic of (KR)	THIN FILM CAPACITORS AND PROCESS FOR MAKING THEM
9815164	0307339	1998-04-28	2001-08-20	Lapsed	Korea, Republic of (KR)	Deuterated Dielectric And Polysilicon Film-Based Semiconductor Devices And Method Of Manufacture Thereof
1019970060838	516245	1997-11-18	2005-09-06	Lapsed	Korea, Republic of (KR)	Integrated Circuit Device With Inductor Incorporated Therein
1020000021415	697963	2000-04-22	2007-03-15	Lapsed	Korea, Republic of (KR)	A Method Of Forming A Multi-Layered Dual-Polysilicon Structure
1020010040533	753788	2001-07-06	2007-08-24	Lapsed	Korea, Republic of (KR)	Silicon-On-Insulator (SOI) Semiconductor Structure With Trench Including A Conductive Layer
10676934	6838379	2003-09-30	2005-01-04	Granted	United States of America	Process for reducing impurity levels, stress, and resistivity, and increasing grain size of copper filler in trenches and vias of integrated circuit structures to enhance electrical performance of copper filler
20030031929	10-0977947	2003-05-20	2010-08-18	Granted	Korea, Republic of (KR)	A Semiconductor Device Barrier Layer
1020030067833	10-988446	2003-09-30	2010-10-12	Lapsed	Korea, Republic of (KR)	Plate Capacitor Structure And Fabrication Method Therefor In A Dual Damascene Process
20040076311	10-1099907	2004-09-23	2011-12-21	Lapsed	Korea, Republic of (KR)	Metal-Oxide-Semiconductor Device Including A Buried Lightly-Doped Drain Region
2003334485	5039267	2003-09-26	2012-07-13	Lapsed	Japan	Plate Capacitor Structure And Fabrication Method Therefor In A Dual Damascene Process
09580939	6527867	2000-05-30	2003-03-04	Granted	United States of America	Method for enhancing anti-reflective coatings used in photolithography of electronic devices

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
2000265144	3958506	2000-09-01	2007-05-18	Lapsed	Japan	Semiconductor Device Having Regions Of Insulating Material Formed In A Semiconductor Substrate And Process Of Making The Device
11024534	3084015	1999-02-02	2000-06-30	Lapsed	Japan	Electronic Apparatus
10275117	3386385	1998-09-29	2003-01-10	Lapsed	Japan	Silicon IC Contacts Using Composite TiN Barrier Layer
10140989	3464607	1998-05-22	2003-08-22	Granted	Japan	Capacitor Comprising Improved Taox-Based Dielectric
2000372411	4749537	2000-12-07	2011-05-27	Lapsed	Japan	A Method Of Forming An Alignment Feature In Or On A Multi-Layered Semiconductor Structure
11260600	3774088	1999-09-14	2006-02-24	Lapsed	Japan	Manufacture Of Mosfet Devices
09146787	3550272	1997-06-04	2004-04-30	Lapsed	Japan	Method For Producing Tapered Lines
10453118	6864141	2003-06-03	2005-03-08	Granted	United States of America	Method of incorporating nitrogen into metal silicate based dielectrics by energized nitrogen ion beams
10406847	7005217	2003-04-04	2006-02-28	Lapsed	United States of America	Chromeless phase shift mask
2004283352	4948756	2004-09-29	2012-03-16	Lapsed	Japan	Inductor Formed In An Integrated Circuit
10290437	6837967	2002-11-06	2005-01-04	Granted	United States of America	Method and apparatus for cleaning deposited films from the edge of a wafer
2003145567	4964400	2003-05-23	2012-04-06	Lapsed	Japan	Abnormal Photoresist Line/Space Profile Detection Through Signal Processing of Metrology Waveform
2004144248	4791706	2004-05-14	2011-07-29	Lapsed	Japan	Split-Gate Metal-Oxide-Semiconductor Device
2005277005		2005-09-26		Abandoned	Japan	Thick Oxide Region In A Semiconductor Device
2004333824	5378635	2004-11-18	2013-10-04	Lapsed	Japan	Metal-Oxide-Semiconductor Device Formed in Silicon-On-Insulator
09735084	6586814	2000-12-11	2003-07-01	Lapsed	United States of America	Etch resistant shallow trench isolation in a semiconductor wafer
2000120437	4038530	2000-04-21	2007-11-16	Granted	Japan	A Method Of Forming A Multi-Layered Dual-Polysilicon Structure
2000093711	3387888	2000-03-30	2003-01-10	Lapsed	Japan	Lithographic Process For Device Fabrication Using Dark-Field Illumination
2005266157	4944414	2005-09-14	2012-03-09	Lapsed	Japan	Guard Ring for Improved Matching
2005101096430	ZL200510109643.0	2005-09-14	2012-05-30	Lapsed	China	Guard Ring for Improved Matching
200510078169X	ZL200510078169.X	2005-06-17	2009-09-30	Lapsed	China	Thick Oxide Region In A Semiconductor Device
10153011		2002-05-21		Abandoned	United States of America	Integrated Circuit Structure Having Low Dielectric Constant Material and Having Silicon Oxynitride Caps Over Closely Spaced Apart Metal Lines
09088801	6211517	1998-06-02	2001-04-03	Granted	United States of America	Electron beam fault detection of semiconductor devices
2004278820	5547361	2004-09-27	2014-05-23	Lapsed	Japan	Metal-Oxide-Semiconductor Device Including A Buried Lightly-Doped Drain Region
2001247517	5177924	2001-08-17	2013-01-18	Lapsed	Japan	Process For Fabricating A Semiconductor Device Having A Metal Oxide Or A Metal Silicate GateDielectric Layer
2002274695	5179693	2002-09-20	2013-01-18	Lapsed	Japan	Multiple Operating Voltage Vertical Replacement-Gate (VRG) Transistor

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
2001261004	5176050	2001-08-30	2013-01-18	Lapsed	Japan	Field Plated Resistor With Enhanced Routing Area Thereover
2006345124	5579358	2006-12-22	2014-07-18	Lapsed	Japan	Robust Shallow Trench Isolation Structures And A Method For Forming Shallow Trench Isolation Structures
2002270858	4797185	2002-09-18	2011-08-12	Lapsed	Japan	Bipolar Junction Transistor Compatible With Vertical Replacement Gate Transistors
09108092	6175124	1998-06-30	2001-01-16	Granted	United States of America	Method and apparatus for a wafer level system
10207607	6764749	2002-07-29	2004-07-20	Granted	United States of America	Method to improve the resolution of a photolithography system by use of a coupling layer between the photo resist and the ARC
10251082	7149340	2002-09-20	2006-12-12	Granted	United States of America	Mask defect analysis for both horizontal and vertical processing effects
10267810	6784102	2002-10-09	2004-08-31	Granted	United States of America	Laterally interconnecting structures
09675109	6472715	2000-09-28	2002-10-29	Granted	United States of America	Reduced soft error rate (SER) construction for integrated circuit structures
10216425	6569739	2002-08-08	2003-05-27	Granted	United States of America	Method of reducing the effect of implantation damage to shallow trench isolation regions during the formation of variable thickness gate layers
10288410	6707132	2002-11-05	2004-03-16	Granted	United States of America	High performance Si-Ge device module with CMOS technology
003000536	60023573.4	2000-01-06	2005-11-02	Granted	Germany (Federal Republic of)	Method For Making An Integrated Circuit Capacitor Including Tantalum Pentoxide
973035785	69729913.9	1997-05-27	2004-07-21	Expired	Germany (Federal Republic of)	Method For Producing Tapered Lines
963069646	69607715.9	1996-09-25	2000-04-12	Expired	Germany (Federal Republic of)	Compensation Of The Temperature Coefficient Of The Dielectric Constant Of Barium Strontium Titanate
10135383	7174281	2002-05-01	2007-02-06	Granted	United States of America	Method for analyzing manufacturing data
10106128	6733829	2002-03-19	2004-05-11	Granted	United States of America	Anti-binding deposition ring
983095977	69842401.8	1998-11-24	2011-09-07	Granted	Germany (Federal Republic of)	Method Of Manufacturing An Integrated Circuit Using Chemical Mechanical Polishing
993036359	69944270.2	1999-05-10	2012-06-20	Granted	Germany (Federal Republic of)	Apparatus For Processing Silicon Device With Improved Temperature Control
013070594	60127777.5	2001-08-20	2007-04-11	Lapsed	Germany (Federal Republic of)	Field Plated Resistor With Enhanced Routing Area Thereover
993040732	69942327.9	1999-05-26	2010-05-05	Granted	Germany (Federal Republic of)	Single Crystal Silicon On Polycrystalline Silicon Integrated Circuits
003067238	60006751.3	2000-08-07	2003-11-26	Lapsed	Germany (Federal Republic of)	Electrochemical Abatement Of Perfluorinated Compounds
003095783	60030386.1	2000-10-30	2006-08-30	Lapsed	Germany (Federal Republic of)	Method For Making Field Effect Devices And Capacitors With Thin Film Dielectrics And Resulting Devices

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
003049921	60020011.6	2000-06-13	2005-05-11	Granted	Germany (Federal Republic of)	An Integrated Circuit Having A Micromagnetic Device And Method Of Manufacture Therefor
003047974	60001600.5	2000-06-06	2003-03-12	Granted	Germany (Federal Republic of)	Process For Fabricating Vertical Transistors
993069186	69937217.8	1999-08-31	2007-10-03	Lapsed	Germany (Federal Republic of)	Article Having Passive Self-Assembly Inductor
983002049	69839597.2	1998-01-13	2008-06-11	Granted	Germany (Federal Republic of)	Semiconductor Device
983045238	69804380.4	1998-06-09	2002-03-27	Granted	Germany (Federal Republic of)	MOS Image Sensor
993055078	69900624.4	1999-07-12	2001-12-19	Granted	Germany (Federal Republic of)	Apparatus and Method for Integrated Circuit With Variable Capacitor
983079286	69823450.2	1998-09-29	2004-04-28	Lapsed	Germany (Federal Republic of)	Article Comprising An Oxide Layer On GaN
10242165	6842042	2002-09-11	2005-01-11	Lapsed	United States of America	Global chip interconnect
09792321	6458508	2001-02-23	2002-10-01	Granted	United States of America	Method of protecting acid-catalyzed photoresist from chip-generated basic contaminants
003105228	60039220.1	2000-11-27	2008-06-18	Granted	Germany (Federal Republic of)	Article Comprising A Dielectric Material Of Zr-Ge-Ti-O Or Hf-Ge-Ti-O And Method Of Making The Same
10036621	6935933	2001-12-21	2005-08-30	Lapsed	United States of America	Viscous electropolishing system
003023272	60030024.2	2000-03-22	2006-08-16	Lapsed	Germany (Federal Republic of)	Lithographic Process For Device Fabrication Using Dark-Field Illumination
003037868	60042468.5	2000-05-05	2009-07-01	Granted	Germany (Federal Republic of)	Improved Wehnelt Gun For Electron Lithography
10060002	6710851	2002-01-29	2004-03-23	Granted	United States of America	Multi pattern reticle
10067299	6621134	2002-02-07	2003-09-16	Granted	United States of America	Vacuum sealed RF/microwave microresonator
09213948	6528389	1998-12-17	2003-03-04	Granted	United States of America	Substrate planarization with a chemical mechanical polishing stop layer
09964157	6621146	2001-09-26	2003-09-16	Granted	United States of America	Method and apparatus for the use of embedded resistance to linearize and improve the matching properties of transistors
09209855	6303899	1998-12-11	2001-10-16	Granted	United States of America	Method and apparatus for scribing a code in an inactive outer clear out area of a semiconductor wafer
09974251	6513376	2001-10-10	2003-02-04	Lapsed	United States of America	Liquid level height measurement system
09994083	6549062	2001-11-21	2003-04-15	Granted	United States of America	Method and apparatus for improving the tolerance of integrated resistors
09974008	6658361	2001-10-10	2003-12-02	Lapsed	United States of America	Heaviest only fail potential
10615558	6989331	2003-07-08	2006-01-24	Granted	United States of America	Hard mask removal

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10002981	6613665	2001-10-26	2003-09-02	Granted	United States of America	Process for forming integrated circuit structure comprising layer of low k dielectric material having antireflective properties in an upper surface
10002831	6528423	2001-10-26	2003-03-04	Granted	United States of America	Process for forming composite of barrier layers of dielectric material to inhibit migration of copper from copper metal interconnect of integrated circuit structure into adjacent layer of low k dielectric material
10061519	6752916	2002-02-01	2004-06-22	Granted	United States of America	Electrochemical planarization end point detection
08563688	6043139	1995-11-28	2000-03-28	Expired	United States of America	Process For Controlling Dopant Diffusion in a Semiconductor Layer and Semiconductor Layer
09950008	6664633	2001-09-10	2003-12-16	Lapsed	United States of America	Alkaline copper plating
10603041	7160799	2003-06-24	2007-01-09	Granted	United States of America	Define Via In Dual Damascene Process
2007206087	5121348	2007-08-08	2012-11-02	Granted	Japan	Local Area Alloying For Preventing Dishing Of Copper During Chemical Mechannical Polishing (CMP)
2007034850	5236884	2007-02-15	2013-04-05	Lapsed	Japan	Low K Dielectric Insulator and Method of Forming Semiconductor Circuit Structures
2007060148	4880501	1999-09-09	2011-12-09	Lapsed	Japan	Article Having Passive Self-Assembly Inductor
10435561	6852648	2003-05-09	2005-02-08	Lapsed	United States of America	Semiconductor Device Having A Low Dielectric Constant Dielectric Material And Process For Its Manufacture
09370963	6228748	1999-08-10	2001-05-08	Expired	United States of America	Use Of A Getter Layer To Improve Metal-To-Metal Contact Resistance At Low Radio Frequency Power
09291781	6317948	1999-04-14	2001-11-20	Expired	United States of America	Embedded Thin Film Passive Components
09333626	6264749	1999-06-15	2001-07-24	Expired	United States of America	Process For Making Composite Films
08566445	5688634	1995-12-01	1997-11-18	Expired	United States of America	Energy Sensitive Resist Material And Process For Device Fabrication Using The Resist Material
08716829	5693977	1996-09-05	1997-12-02	Expired	United States of America	N-Channel Field-Efect (sic) Transistor Including A Thin-Film Fullerene
09398977	6143658	1999-09-17	2000-11-07	Granted	United States of America	Multilevel Wiring Structure and Method of Fabricating a Multilevel Wiring Structure
08478133	5710055	1995-06-07	1998-01-20	Expired	United States of America	Method Of Making PMOSFETs Having Indium Or Gallium Doped Buried Channels And N\(plPolysilicon Gates And CMOS Devices Fabricated Therefrom
2001111006	5010782	2000-12-07	2012-06-08	Lapsed	Japan	A Method Of Forming An Alignment Feature In Or On A Multi-Layered Semiconductor Structure
2007108964	5247059	2000-01-12	2013-04-19	Lapsed	Japan	Method For Making An Integrated Circuit Capacitor Including Tantalum Pentoxide
08767153	5923524	1996-12-16	1999-07-13	Expired	United States of America	Dielectric Material Comprising Ta sub 2 O sub 5 Doped With TiO sub 2 And Devices Employing Same

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
200756483		2007-03-07		Abandoned	Japan	An Integrated Circuit Including ESD Circuits For A Multi-Chip Module And A Method Therefor
08746184	5976637	1996-11-06	1999-11-02	Expired	United States of America	Method For Coating Heterogeneous Substrates With Homogeneous Layers
2005060155	4276194	1998-06-19	2009-03-13	Lapsed	Japan	MOS Image Sensor
08931066	5804460	1997-09-15	1998-09-08	Expired	United States of America	Linewidth Metrology Of Integrated Circuit And Structures
08853210	5918116	1997-05-09	1999-06-29	Expired	United States of America	Process For Forming Different Gate Oxides Possessing Different Thicknesses On A Semiconductor Substrate
07866942	5679589	1992-04-03	1997-10-21	Expired	United States of America	FET With Gate Spacer
08156953	5982034	1993-11-19	1999-11-09	Expired	United States of America	Conductive Oxide Films
07719699	5744403	1991-06-25	1998-04-28	Expired	United States of America	Dielectric Film Deposition Method And Apparatus
09404702	6239035	1999-09-23	2001-05-29	Expired	United States of America	Semiconductor Wafer Fabrication
08697402	5728421	1996-08-23	1998-03-17	Expired	United States of America	Article Comprising Spinel-Structure Material On A Substrate, And Method Of Making The Article
08857079	5798300	1997-05-15	1998-08-25	Expired	United States of America	Method For Forming Conductors In Integrated Circuits
08610646	5620907	1996-03-04	1997-04-15	Expired	United States of America	Method For Making A Heterojunction Bipolar Transistor
1019980041563	364338	1998-10-02	2002-11-28	Granted	Korea, Republic of (KR)	Energy-Sensitive Resist Material And A Process For Device Fabrication UsingAn Energy-Sensitive Resist Material
983015629	69800033.1	1998-03-03	1999-10-27	Lapsed	Germany (Federal Republic of)	Energy-Sensitive Resist Material And A Process For Device Fabrication Using An Energy-Sensitive Resist Material
08961383	6106371	1997-10-30	2000-08-22	Expired	United States of America	Effective pad conditioning
08610026	5834800	1996-03-04	1998-11-10	Expired	United States of America	A Heterojunction Bipolar Transistor Having Monocrystalline SiGe Intrinsic Base And Polycrystalline SiGe and Si Extrinsic Base Regions
09543412	6346490	2000-04-05	2002-02-12	Granted	United States of America	Process for treating damaged surfaces of low k carbon doped silicon oxide dielectric material after plasma etching and plasma cleaning steps
09395062	6288453	1999-09-13	2001-09-11	Granted	United States of America	Alignment of openings in semiconductor fabrication
09553140	7751609	2000-04-20	2010-07-06	Lapsed	United States of America	A Method of Performing Oxide End-Point During CMP
1019980007413	588369	1998-03-06	2006-06-02	Lapsed	Korea, Republic of (KR)	Energy-Sensitive Resist Material And A Process For Device Fabrication Using An Energy-Sensitive Resist Material
10280394	3481469	1998-10-02	2003-10-10	Granted	Japan	Energy-Sensitive Resist Material And A Process For Device Fabrication UsingAn Energy-Sensitive Resist Material
09521312	6413881	2000-03-09	2002-07-02	Granted	United States of America	Process for forming thin gate oxide with enhanced reliability by nitridation of upper surface of gate of oxide to form barrier of nitrogen atoms in upper surface region of gate oxide, and resulting product
09706286	6544807	2000-11-03	2003-04-08	Granted	United States of America	Process monitor with statistically selected ring oscillator
10158641	6864563	2002-05-30	2005-03-08	Lapsed	United States of America	Grounding mechanism for semiconductor devices

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09574804	6426286	2000-05-19	2002-07-30	Granted	United States of America	Interconnection system with lateral barrier layer
09639440	6782500	2000-08-15	2004-08-24	Granted	United States of America	Statistical decision system
08770046	6180470	1996-12-19	2001-01-30	Expired	United States of America	FETs having lightly doped drain regions that are shaped with counter and noncounter dorant elements
09438642	6147012	1999-11-12	2000-11-14	Granted	United States of America	Process for forming low k silicon oxide dielectric material while suppressing pressure spiking and inhibiting increase in dielectric constant
08787992	6010952	1997-01-23	2000-01-04	Expired	United States of America	Process for forming metal silicide contacts using amorphization of exposed silicon while minimizing device degradation
09005364	6531397	1998-01-09	2003-03-11	Granted	United States of America	Method and apparatus for using across wafer back pressure differentials to influence the performance of chemical mechanical polishing
09487984	6448084	2000-01-20	2002-09-10	Granted	United States of America	Multiple metal etchant system for integrated circuits
1998542006	4386468	1998-04-02	2009-10-09	Granted	Japan	Process for Fabricating a Moderate-Depth Diffused Emitter Bipolar Transistor in a BICMOS Device Without Using an Additional Mask
09607177	6464566	2000-06-29	2002-10-15	Granted	United States of America	Apparatus and method for linearly planarizing a surface of a semiconductor wafer
10033164	6511925	2001-10-19	2003-01-28	Granted	United States of America	Process for forming high dielectric constant gate dielectric for integrated circuit structure
1999351216	4657412	1999-12-10	2011-01-07	Lapsed	Japan	Slurry Collecting Device for CMP Slurry Circulation
199207577	19920757.7	1999-05-05	2008-05-15	Granted	Germany (Federal Republic of)	Non-Linear Circuit Elements on Integrated Circuits
09347487	6281092	1999-07-02	2001-08-28	Granted	United States of America	Method for manufacturing a metal-to-metal capacitor utilizing only one masking step
87114682	142684	1998-09-04	2002-02-08	Lapsed	Taiwan	Standardized Gas Isolation Box (GIB) Installation
09216394	6235590	1998-12-18	2001-05-22	Granted	United States of America	Fabrication of differential gate oxide thicknesses on a single integrated circuit chip
09211922	6090724	1998-12-15	2000-07-18	Granted	United States of America	Method for composing a thermally conductive thin film having a low dielectric property
87115810	120367	1998-09-23	2001-02-01	Lapsed	Taiwan	A Method and Apparatus for Chemical Mechanical Polishing
09108091	6268224	1998-06-30	2001-07-31	Granted	United States of America	Method and apparatus for detecting an ion-implanted polishing endpoint layer within a semiconductor wafer
86119036	120428	1997-12-17	2001-02-05	Lapsed	Taiwan	Simple BiCMOS Process for Creation of Low Trigger Voltage SCR and Zener Diode Pad Protection
86118838	112608	1997-12-13	2000-07-04	Lapsed	Taiwan	Variable Step Height Control of Lithographic Patterning Through Transmitted Light Intensity Variation
979156007	69706043.8	1997-03-26	2001-08-08	Expired	Germany (Federal Republic of)	Method and Apparatus for Protecting Functions Imbedded Within an Integrated Circuit from Reverse Engineering

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09204767	6174407	1998-12-03	2001-01-16	Granted	United States of America	Apparatus and method for detecting an endpoint of an etching process by transmitting infrared light signals through a semiconductor wafer
09111529	6285035	1998-07-08	2001-09-04	Granted	United States of America	Apparatus for detecting an endpoint polishing layer of a semiconductor wafer having a wafer carrier with independent concentric sub-carriers and associated method
09082810	6206573	1998-05-21	2001-03-27	Granted	United States of America	High reliability bearing structure
86105907	NI-094528	1997-05-03	1998-09-10	Lapsed	Taiwan	Method and Apparatus for Protecting Functions Imbedded Within an Integrated Circuit from Reverse Engineering
87104961	118316	1998-04-02	2000-12-05	Lapsed	Taiwan	Process for Fabricating a Moderate-Depth Diffused Emitter Bipolar Transistor in a BICMOS Device Without Using an Additional Mask
09212931	6277707	1998-12-16	2001-08-21	Granted	United States of America	Method of manufacturing semiconductor device having a recessed gate structure
09942220	6898064	2001-08-29	2005-05-24	Lapsed	United States of America	System and method for optimizing the electrostatic removal of a workpiece from a chuck
09107342	6241847	1998-06-30	2001-06-05	Granted	United States of America	Method and apparatus for detecting a polishing endpoint based upon infrared signals
09131921	6080670	1998-08-10	2000-06-27	Granted	United States of America	Method of detecting a polishing endpoint layer of a semiconductor wafer which includes a non-reactive reporting specie
08580674	5645736	1995-12-29	1997-07-08	Expired	United States of America	Method for polishing a wafer
08767698	5976309	1996-12-17	1999-11-02	Expired	United States of America	Electrode assembly for plasma reactor
09046242	6071817	1998-03-23	2000-06-06	Granted	United States of America	Isolation method utilizing a high pressure oxidation
08763373	5821013	1996-12-13	1998-10-13	Expired	United States of America	Variable step height control of lithographic patterning through transmitted light intensity variation
08773471	5963828	1996-12-23	1999-10-05	Expired	United States of America	Method for tungsten nucleation from WF6 using titanium as a reducing agent
09075029	6093585	1998-05-08	2000-07-25	Granted	United States of America	High voltage tolerant thin film transistor
12344016	7898277	2008-12-24	2011-03-01	Granted	United States of America	Hot-Electron Injection Testing Of Transistors On A Wafer
11469032	7479438	2006-08-31	2009-01-20	Granted	United States of America	Method to Improve Performance Of A Bipolar Device Using An Amorphizing Implant
10953480	7197723	2004-09-29	2007-03-27	Granted	United States of America	Semiconductor Device Manufacturing
10878857	7148540	2004-06-28	2006-12-12	Granted	United States of America	Graded Conductive Structure For Use In A Metal\(miOxide\(miSemiconductor Device
10300365	6825538	2002-11-20	2004-11-30	Granted	United States of America	Semiconductor Device Using An Insulating Layer Having A Seed Layer
10007417	6683465	2001-10-31	2004-01-27	Granted	United States of America	Integrated Circuit Having Stress Migration Test Structure And Method Therefor
10007904	6747445	2001-10-31	2004-06-08	Granted	United States of America	Stress Migration Test Structure And Method Therefor

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09865124	6541819	2001-05-24	2003-04-01	Granted	United States of America	Semiconductor Device Having Non\(miPower Enhanced And Power Enhanced Metal Oxide Semiconductor And Method Of Manufacture Therefor
09935241	6548906	2001-08-22	2003-04-15	Granted	United States of America	Method For Reducing A Metal Seam In An Interconnect Structure And A Device Manufactured Thereby
09964041	6737311	2001-09-26	2004-05-18	Granted	United States of America	Semiconductor Device Having A Buried Layer For Reducing Latchup And A Method Of Manufacture Therefor
09731402	6896583	2001-02-06	2005-05-24	Lapsed	United States of America	Method And Apparatus For Conditioning A Polishing Pad
09653531	6630699	2000-08-31	2003-10-07	Granted	United States of America	Transistor Device Having An Isolation Structure Located Under A Source Region, Drain Region And Channel Region And A Method Of Manufacture Thereof
09653364	6569690	2000-08-31	2003-05-27	Granted	United States of America	Monitoring System For Determining Progress In A Fabrication Activity
09648015	6367329	2000-08-25	2002-04-09	Granted	United States of America	Acoustic Time Of Flight And Acoustic Resonance Methods For Detecting Endpoint In Plasma Processes
09640329	6362094	2000-08-16	2002-03-26	Granted	United States of America	Hydrogenated Silicon Carbide As A Liner For Self-Aligning Contact Vias
09737717	6551410	2000-12-15	2003-04-22	Granted	United States of America	Method Of Cleaning A Semiconductor Wafer With A Cleaning Brush Assembly Having A Contractible An Expandable Arbor
09611581	6435946	2000-07-07	2002-08-20	Granted	United States of America	Technique For Reducing Slivers On Optical Components Resulting From Friction Processes
09397716	6251546	1999-09-16	2001-06-26	Granted	United States of America	An Improved Method Of Fabricating Devices Using An Attenuated Phase-Shifting Mask And An Attenuated Phase-Shifting Mask
09520670	6611729	2000-03-07	2003-08-26	Granted	United States of America	System And Method For Introducing Multiple Component-Type Factors Into An Integrated Circuit Yield Prediction
09603340	6372605	2000-06-26	2002-04-16	Granted	United States of America	Additional Etching To Decrease Polishing Time for Shallow-Trench Isolation In Semiconductor Processing
09459708	6537135	1999-12-13	2003-03-25	Granted	United States of America	Curvilinear Chemical Mechanical Planarization Device And Method
09482390	6401929	2000-01-12	2002-06-11	Granted	United States of America	Insert For Use In Transporting A Wafer Carrier
09430635	6136615	1999-10-29	2000-10-24	Granted	United States of America	Migration From Control Wafer To Product Wafer Particle Checks
09376696	6206770	1999-08-18	2001-03-27	Granted	United States of America	Wafer Carrier Head For Prevention Of Unintentional Semiconductor Wafer Rotation
09399621	6281129	1999-09-20	2001-08-28	Granted	United States of America	Corrosion-Resistant Polishing Pad Conditioner
09338520	6815876	1999-06-23	2004-11-09	Lapsed	United States of America	Cathode With Improved Work Function And Method Of Making Same
10963156	7179148	2004-10-12	2007-02-20	Granted	United States of America	Cathode With Improved Work Function And Method For Making The Same

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
2000188555	3901915	2000-06-23	2007-01-12	Lapsed	Japan	Cathode With Improved Work Function And Method Of Making Same
89111997	NI-141143	2000-06-19	2001-09-11	Lapsed	Taiwan	Cathode With Improved Work Function And Method Of Making Same
003050150	60044167.9	2000-06-13	2010-04-14	Granted	Germany (Federal Republic of)	Cathode With Improved Work Function And Method Of Making Same
20000034530	744896	2000-06-22	2007-07-25	Lapsed	Korea, Republic of (KR)	Cathode With Improved Work Function And Method Of Making Same
003050150	1063669	2000-06-13	2010-04-14	Lapsed	France	Cathode With Improved Work Function And Method Of Making Same
003050150	1063669	2000-06-13	2010-04-14	Lapsed	United Kingdom	Cathode With Improved Work Function And Method Of Making Same
09477310	6559499	2000-01-04	2003-05-06	Granted	United States of America	Process For Fabricating An Integrated Circuit Device Having Capacitors With A Multilevel Metallization
09347313	6258610	1999-07-02	2001-07-10	Granted	United States of America	Method Analyzing A Semiconductor Surface Using Line Width Metrology With Auto-Correlation Operation
09346754		1999-07-02		Abandoned	United States of America	Method For Manufacturing Semiconductor Integrated Circuits With Etch Process Modification
09232120	6162733	1999-01-15	2000-12-19	Granted	United States of America	Method For Removing Contaminants From Integrated Circuits
09222587	6359317	1998-12-28	2002-03-19	Granted	United States of America	Vertical PNP Bipolar Transistor And Its Method Of Fabrication
09024601	6384446	1998-02-17	2002-05-07	Expired	United States of America	Integrated Circuit Fabrication
09090295	6093944	1998-06-04	2000-07-25	Granted	United States of America	Dielectric Materials Of Amorphous Compositions of Ti\(mi 02 Doped With Rare Earth Elements And Devices Employing Same
09058826	6091279	1998-04-13	2000-07-18	Granted	United States of America	Temperature Compensation of LDMOS Devices
09017103	6222863	1998-01-31	2001-04-24	Granted	United States of America	Article Comprising A Stable, Low-Resistance Ohmic Contact
09105712	6075909	1998-06-26	2000-06-13	Granted	United States of America	Optical Monitoring System For III\(miV Wafer Processing
08924728	6013556	1997-09-05	2000-01-11	Expired	United States of America	Method Of Integrated Circuit Fabrication
08727726	5779929	1996-10-07	1998-07-14	Expired	United States of America	Thin Film Metallization For Barium Nanotitanate Substrates
08674956	5683917	1996-07-03	1997-11-04	Expired	United States of America	Method Of Making A Low Noise Semiconductor Device Comprising A Screening Measurement
08572599	5855280	1995-12-14	1999-01-05	Expired	United States of America	Cassette Light
08509678	5620253	1995-07-31	1997-04-15	Expired	United States of America	Method Of Determining The Thermal Conductivity Of Electrically Insulating Crystalline Materials
08561473	5670396	1995-11-21	1997-09-23	Expired	United States of America	Methof Of Forming A DMOS-Controlled Lateral Bipolar Transistor
08412678	5588969	1995-03-29	1996-12-31	Expired	United States of America	Method for Supplying Phosphorous Vapor
08497470	5712176	1995-06-30	1998-01-27	Expired	United States of America	Doping Of Silicon Layers

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08278688	6197375	1994-07-21	2001-03-06	Granted	United States of America	Method Comprising Removal Of Material From A Diamond Film
08774036	5976943	1996-12-27	1999-11-02	Expired	United States of America	Method for Bi-Layer Programmable Resistor
08883403	5854510	1997-06-26	1998-12-29	Expired	United States of America	Low Power Programmable Fuse Structures
09055018	5882998	1998-04-03	1999-03-16	Expired	United States of America	Low power programmable fuse structures and methods for making the same
97342851	3973744	1997-12-12	2007-06-22	Lapsed	Japan	Two-Layer Type Programmable Resistor
099113363	I424152	2010-04-27	2014-01-21	Granted	Taiwan	An Electronic Pressure-Sensing Device
2010109863	5885909	2010-05-12	2016-02-19	Granted	Japan	An Electronic Pressure-Sensing Device
12465309	8037771	2009-05-13	2011-10-18	Granted	United States of America	Electronic Pressure-Sensing Device
1020100042858	101512527	2010-05-07	2015-04-09	Lapsed	Korea, Republic of (KR)	An Electronic Pressure-Sensing Device
101627768		2010-05-13		Application	European Patent	An Electronic Pressure-Sensing Device
2010101787444	ZL201010178744.4	2010-05-12	2014-07-02	Lapsed	China	An Electronic Pressure-Sensing Device
12290054	7972873	2008-10-27	2011-07-05	Granted	United States of America	Material Removing Processes In Device Formation And The Devices Formed Thereby
12112076	7977721	2008-04-30	2011-07-12	Granted	United States of America	High Voltage Tolerant Metal-Oxide-Semiconductor Device
13149122	8105912	2011-05-31	2012-01-31	Granted	United States of America	High Voltage Tolerant Metal-Oxide-Semiconductor Device
09741667	6518619	2000-12-19	2003-02-11	Granted	United States of America	Virtual-Ground, Split Gate Flash Memory Cell Arrangements and Method For Producing Same
11609509	7607112	2006-12-12	2009-10-20	Granted	United States of America	Method And Apparatus For Performing Metalization In An Integrated Circuit Process
100121509	I402965	2011-06-20	2013-07-21	Lapsed	Taiwan	Defectivity-Immune Technique of Implementing MiM-based Decoupling Capacitors
2011101979218	ZL2011101979218	2011-07-15	2015-04-08	Lapsed	China	Defectivity-Immune Technique of Implementing MiM-based Decoupling Capacitors
2011157508	5566346	2011-07-19	2014-06-27	Lapsed	Japan	Defectivity-Immune Technique of Implementing MiM-based Decoupling Capacitors
12839148	8411399	2010-07-19	2013-04-02	Granted	United States of America	Defectivity-Immune Technique of Implementing MiM-based Decoupling Capacitors
1020110069793	10-1395584	2011-07-14	2014-05-09	Lapsed	Korea, Republic of (KR)	Defectivity-Immune Technique of Implementing MiM-based Decoupling Capacitors
111745519		2011-07-19		Abandoned	European Patent	Defectivity-Immune Technique of Implementing MiM-based Decoupling Capacitors
12546855	8318606	2009-08-25	2012-11-27	Lapsed	United States of America	Dielectric Etching
11322103	7712066	2005-12-29	2010-05-04	Lapsed	United States of America	Area-Efficient Power Switching Cell
2006255124	5275558	2006-09-21	2013-05-24	Granted	Japan	Controlling Overspray Coating In Semiconductor Devices
1020060091668	10-1356667	2006-09-21	2014-01-22	Granted	Korea, Republic of (KR)	Controlling Overspray Coating In Semiconductor Devices
11832711	7772085	2007-08-02	2010-08-10	Lapsed	United States of America	Controlling Overspray Coating In Semiconductor Devices
06175889	2431042	2006-09-07	2011-07-27	Lapsed	United Kingdom	Controlling Overspray Coating In Semiconductor Devices

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
095134838	I437785	2006-09-20	2014-05-11	Granted	Taiwan	Controlling Overspray Coating In Semiconductor Devices
11232074	7269197	2005-09-21	2007-09-11	Granted	United States of America	Controlling Overspray Coating In Semiconductor Devices
12680017		2010-03-25	2013-02-05	Abandoned	United States of America	Method to Reduce Trench Capacitor Leakage For Random Access Memory Device
11094975	7329605	2005-03-31	2008-02-12	Granted	United States of America	Semiconductor Structure Formed Using A Sacrificial Structure
11927978	7741702	2007-10-30	2010-06-22	Granted	United States of America	Semiconductor Structure Formed Using A Sacrificial Structure
11068237	7247556	2005-02-28	2007-07-24	Granted	United States of America	Control Of Wafer Warpage During Backend Processing
11124307	7399648	2005-05-06	2008-07-15	Granted	United States of America	Methods And Apparatus For Determining Location-Based On-Chip Variation Factor
11673645	7557010	2007-02-12	2009-07-07	Granted	United States of America	Method To Improve Writer Leakage in a SiGe Bipolar Device
12476994	7898038	2009-06-02	2011-03-01	Granted	United States of America	Method To Improve Writer Leakage in SiGe Bipolar Device
10902332	7111517	2004-07-29	2006-09-26	Lapsed	United States of America	Apparatus And Method For In-Situ Measuring Of Vibrational Energy In A Process Bath Of A Vibrational Cleaning System
10773614	7214568	2004-02-06	2007-05-08	Granted	United States of America	Semiconductor Device Configured For Reducing Post-Fabrication Damage
10778454	7005724	2004-02-13	2006-02-28	Lapsed	United States of America	A Semiconductor Device And A Method Of Manufacture Therefor
11167772	7811944	2005-06-27	2010-10-12	Lapsed	United States of America	A Semiconductor Device And A Method Of Manufacture Therefor
10675581	6906538	2003-09-30	2005-06-14	Granted	United States of America	Alternating Pulse Dual\(miBeam Apparatus, Methods And Systems For Voltage Contrast Behavior Assessment of Microcircuits
10919591	7339274	2004-08-17	2008-03-04	Granted	United States of America	Metallization Performance In Electronic Devices
10695193	6975040	2003-10-28	2005-12-13	Lapsed	United States of America	Fabricating Semiconductor Chips
10999704	7262476	2004-11-30	2007-08-28	Granted	United States of America	Semiconductor Device Having Improved Power Density
10981175	7573097	2004-11-03	2009-08-11	Lapsed	United States of America	Lateral Double Diffused MOS Transistors
10200233	6838213	2002-07-23	2005-01-04	Granted	United States of America	Process For Fabricating A Mask
09882624	6958518	2001-06-15	2005-10-25	Lapsed	United States of America	A Semiconductor Device Having At Least One Source\(slDrain Region Formed On An Isolation Region And A Method Of Manufacture Therefor
09943630	6648734	2001-08-30	2003-11-18	Granted	United States of America	Polishing Head For Pressurized Delivery Of Slurry
10008015	6703712	2001-11-13	2004-03-09	Granted	United States of America	Microelectronic Device Layer Deposited With Multiple Electrolytes
09859316	6433628	2001-05-17	2002-08-13	Granted	United States of America	Wafer Testable Integrated Circuit
09882623	6569744	2001-06-15	2003-05-27	Granted	United States of America	Method Of Converting A Metal Oxide Semiconductor Transistor Into A Bipolar Transistor
09927752	6503793	2001-08-10	2003-01-07	Granted	United States of America	Method For Concurrently Forming An ESD Protection Device And A Shallow Trench Isolation Region
10180221	6825467	2002-06-25	2004-11-30	Granted	United States of America	Apparatus For Scanning A Crystalline Sample And Associated Methods
10274765	6723581	2002-10-21	2004-04-20	Granted	United States of America	Semiconductor Device Having A High-K Gate Dielectric And Method Of Manufacture Thereof

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10120767	6783426	2002-04-10	2004-08-31	Granted	United States of America	Method And Apparatus For Detection Of Chemical Mechanical Planarization Endpoint And Device Planarity
09771621	6440816	2001-01-30	2002-08-27	Granted	United States of America	Alignment Mark Fabrication Process To Limit Accumulation Of Errors In Level To Level Overlay
10140616	6828649	2002-05-07	2004-12-07	Lapsed	United States of America	Semiconductor Device Having An Interconnect That Electrically Connects A Conductive Material And A Doped Layer, And A Method Of Manufacture Therefor
10047516	6576563	2001-10-26	2003-06-10	Granted	United States of America	Method Of Manufacturing A Semiconductor Device Employing A Fluorine-Based Etch Substantially Free Of Hydrogen
09713106	6639285	2000-11-15	2003-10-28	Granted	United States of America	A Semiconductor Device
09606833	6319837	2000-06-29	2001-11-20	Granted	United States of America	Technique For Reducing Dishing In Cu-Based Interconnects
09954341	6659846	2001-09-17	2003-12-09	Granted	United States of America	Pad For Chemical Mechanical Polishing
09882961	6602758	2001-06-15	2003-08-05	Granted	United States of America	Formation Of Silicon On Insulator (SOI) Devices As An Add On Module For System On A Chip (SOC) Processing
02138634	2381378	2002-06-17	2006-01-25	Lapsed	United Kingdom	Formation Of Silicon On Insulator (SOI) Devices As An Add On Module For System On A Chip (SOC) Processing
091113153	NI-183665	2002-06-17	2003-08-11	Lapsed	Taiwan	Formation Of Silicon On Insulator (SOI) Devices As An Add On Module For System On A Chip (SOC) Processing
09632445	6436829	2000-08-04	2002-08-20	Granted	United States of America	Two Phase Chemical\(slMechanical Polishing Process For Tungsten Layers
09692012	6559011	2000-10-19	2003-05-06	Granted	United States of America	Dual Level Gate Process For Hot Carrier Control In Double Diffused MOS Transistors
09792266	6706603	2001-02-23	2004-03-16	Granted	United States of America	Method Of Forming A Semiconductor Device
09559494	6486075	2000-04-27	2002-11-26	Granted	United States of America	Anistropic Wet Etching Method
09966156	6695572	2001-09-28	2004-02-24	Granted	United States of America	Method And Apparatus For Minimizing Semiconductor Wafer Contamination
09706319	6358824	2000-11-03	2002-03-19	Granted	United States of America	Integrated Circuits with Tub-Ties and Shallow Trench Isolation
10122645	6750447	2002-04-12	2004-06-15	Lapsed	United States of America	Calibration Standard For High Resolution Electron Microscopy
09965739	6573183	2001-09-28	2003-06-03	Granted	United States of America	Method And Apparatus For Controlling Contamination During The Electroplating Deposition Of Metals Onto A Semiconductor Wafer Surface
09631862	6525394	2000-08-03	2003-02-25	Granted	United States of America	Improved Substrate Isolation For Analog\(slDigital IC Chips
09542362	6359400	2000-04-04	2002-03-19	Granted	United States of America	Direct Drive Spindle For Use In Chemical Vapor Deposition
09727326	6585830	2000-11-30	2003-07-01	Lapsed	United States of America	Method For Cleaning Tungsten From Deposition Wall Chambers
09713504	6559062	2000-11-15	2003-05-06	Granted	United States of America	Method For Avoiding Notching In A Semiconductor Interconnect During A Metal Etching Step
09651661	6555910	2000-08-29	2003-04-29	Granted	United States of America	Use Of Small Openings In Large Topography Features To Improve Dielectric Thickness Control And A Method Of Manufacture Thereof

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10055583	6800255	2002-01-23	2004-10-05	Lapsed	United States of America	System And Method For The Abatement Of Toxic Constituents Of Effluent Gases
09665279	6558238	2000-09-19	2003-05-06	Granted	United States of America	Apparatus And Method For Reclamation Of Used Polishing Slurry
09532688	6423149	2000-03-22	2002-07-23	Granted	United States of America	Apparatus And Method For Improved Cleaning Of Post-CMP Semiconductor Wafers
09605507	6403397	2000-06-28	2002-06-11	Granted	United States of America	Process For Fabricating Organic Semiconductor Device Involving Selective Patterning
09785756	6544107	2001-02-16	2003-04-08	Granted	United States of America	Composite Polishing Pads For Chemical\(miMechanical Polishing
09490912	6579797	2000-01-25	2003-06-17	Granted	United States of America	Cleaning Brush Conditioning Apparatus
09567373	6519542	2000-05-09	2003-02-11	Granted	United States of America	Method Of Testing An Unknown Sample With An Analytical Tool
09567359	6519543	2000-05-09	2003-02-11	Granted	United States of America	Calibration Method For Quantitative Elemental Analysis
09659668	6495474	2000-09-11	2002-12-17	Granted	United States of America	Method Of Fabricating A Dielectric Layer
09718935	6514123	2000-11-21	2003-02-04	Granted	United States of America	Semiconductor Polishing Pad Alignment Device For A Polishing Apparatus And Method Of Use
09755826	7927939	2001-01-04	2011-04-19	Granted	United States of America	Method of Manufacturing a Laterally Diffused Metal Oxide Semiconductor Device
12555082	7927940	2009-09-08	2011-04-19	Granted	United States of America	Method of Manufacturing a Laterally Diffused Metal Oxide Semiconductor Device
10028614	6815302	2001-12-21	2004-11-09	Granted	United States of America	Method For Making A Bipolar Transistor With An Oxygen Implanted Emitter Window
09727325	6537887	2000-11-30	2003-03-25	Granted	United States of America	Integrated Circuit Fabrication
09821506	6615433	2001-03-29	2003-09-09	Granted	United States of America	Apparatus For Detecting Wetness Of A Semiconductor Wafer Cleaning Brush
09382611	6235072	1999-08-25	2001-05-22	Granted	United States of America	Glove Box Filter System
09809379	6870950	2001-03-15	2005-03-22	Granted	United States of America	Method For Detecting Defects In A Material And A System For Accomplishing The Same
09420234	6511221	1999-10-19	2003-01-28	Granted	United States of America	Apparatus For Measuring Thermomechanical Properties Of Photo\(miSensitive Materials
09442688	6246325	1999-11-18	2001-06-12	Granted	United States of America	A Distributed Communications System For Reducing Equipment Down-Time
09407575	6156675	1999-09-28	2000-12-05	Granted	United States of America	Apparatus And Method For Enhanced Dielectric Film Uniformity
09397459	6406999	1999-09-16	2002-06-18	Granted	United States of America	A Semicondutor Device Having Reduced Line Width Variations Between Tightly Spaced And Isolated Features
09397458	6395639	1999-09-16	2002-05-28	Granted	United States of America	A Process For Improving Line Width Variations Between Tightly Spaced And Isolated Features In Integrated Circuits
09494705	6354910	2000-01-31	2002-03-12	Granted	United States of America	Apparatus And Method For In-Situ Measurement Of Polishing Pad Thickness Loss
09533429	6616965	2000-03-23	2003-09-09	Lapsed	United States of America	Non\(miHydrolytic Sol\(miGel Process For High K Dielectric

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09356396	6259764	1999-07-16	2001-07-10	Granted	United States of America	Zone Plates For X-Rays
09591037	6451660	2000-06-09	2002-09-17	Granted	United States of America	Method Of Forming Bipolar Transistors Comprising A Native Oxide Layer Formed On A Substrate By Rinsing The Substrate In Ozinated Water
09562346	6391668	2000-05-01	2002-05-21	Granted	United States of America	Method Of Determining A Trap Density Of A Semiconductor\(slOxide Interface By A Contactless Charge Technique
09415529	6596639	1999-10-08	2003-07-22	Granted	United States of America	Method For Chemical\(slMechanical Planarization Of A Semiconductor Wafer Having Dissimilar Metal Pattern Densities
09426017	6254454	1999-10-25	2001-07-03	Granted	United States of America	Reference Thickness Endpoint Techniques For Polishing Operations
89112520	NI-139603	2000-06-26	2001-09-01	Granted	Taiwan	Diffusion Preventing Barrier Layer In Integrated Circuit Inter-Metal Layer Dielectrics
1020000048028	757214	2000-08-19	2007-09-04	Granted	Korea, Republic of (KR)	Diffusion Preventing Barrier Layer In Integrated Circuit Inter-Metal Layer Dielectrics
00194837	2359661	2000-08-08	2002-11-20	Lapsed	United Kingdom	Diffusion Preventing Barrier Layer In Integrated Circuit Inter-Metal Layer Dielectrics
09377386	6727588	1999-08-19	2004-04-27	Granted	United States of America	Diffusion Preventing Barrier Layer In Integrated Circuit Inter-Metal Layer Dielectrics
09491836	6368190	2000-01-26	2002-04-09	Granted	United States of America	Electrochemical Mechanical Planarization Apparatus And Method
09575214	6680542	2000-05-18	2004-01-20	Granted	United States of America	Damascene Structure Having A Metal-Oxide-Metal Capacitor Associated Therewith
09354657	6414383	1999-07-16	2002-07-02	Granted	United States of America	Very Low Magnetic Field Integrated Circuit
09388203	6362638	1999-09-01	2002-03-26	Granted	United States of America	Stacked Via Kelvin Resistance Test Structure For Measuring Contact Anomalies In Multi-Level Metal Integrated Circuit Technologies
09444817	6368955	1999-11-22	2002-04-09	Granted	United States of America	Method Of Polishing Semiconductor Structures Using Chemical Mechanical Planarization
09478725	6303426	2000-01-06	2001-10-16	Granted	United States of America	Method Of Forming A Capacitor Having A Tungsten Bottom Electrode In A Semiconductor Wafer
09266912	6048664	1999-03-12	2000-04-11	Granted	United States of America	Energy-Sensitive Resist Material And A Process For Device Fabrication Using An Energy-Sensitive Resist Material
09497982	6306313	2000-02-04	2001-10-23	Granted	United States of America	Selective Etching Of Thin Films
09305722	6736985	1999-05-05	2004-05-18	Granted	United States of America	High-Resolution Method For Patterning A Substrate With Micro-Printing

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09465880	6746577	1999-12-16	2004-06-08	Granted	United States of America	Method And Apparatus For Thickness Control And Reproducibility Of Dielectric Film Deposition
09390181	6387817	1999-09-07	2002-05-14	Granted	United States of America	Plasma Confinement Shield
09273299	6066884	1999-03-19	2000-05-23	Granted	United States of America	Schottky Diode Guard Ring Structures
09363781	6175137	1999-07-29	2001-01-16	Granted	United States of America	Monolithic Resistor Having Dynamically Controllable Impedance And Method Of Manufacturing The Same
09480387	6309900	2000-01-11	2001-10-30	Granted	United States of America	Test Structures For Testing Planarization Systems And Methods For Using Same
1020000046955	718823	2000-08-14	2007-05-10	Granted	Korea, Republic of (KR)	A Silicon-Germanium Transistor And Associated Methods
00194811	2356739	2000-08-08	2002-04-17	Lapsed	United Kingdom	A Silicon-Germanium Transistor And Associated Methods
89116118	NI-151814	2000-08-10	2002-03-11	Lapsed	Taiwan	A Silicon-Germanium Transistor And Associated Methods
09375150	6235560	1999-08-16	2001-05-22	Granted	United States of America	A Silicon-Germanium Transistor And Associated Methods
09370912	6287970	1999-08-06	2001-09-11	Granted	United States of America	Method Of Making A Semiconductor With Copper Passivating Film
09332216	6281128	1999-06-14	2001-08-28	Granted	United States of America	Wafer Carrier Modification For Reduced Extraction Force
09263445	6307252	1999-03-05	2001-10-23	Granted	United States of America	On-Chip Shielding Of Signals
09286430	6217427	1999-04-06	2001-04-17	Granted	United States of America	Mobius Strip Belt For Linear CMP Tools
09441676	6331460	1999-11-17	2001-12-18	Granted	United States of America	A Method Of Fabricating A MOM Capacitor Having A Metal Silicide Barrier
09441561	6335557	1999-11-17	2002-01-01	Granted	United States of America	Metal Silicide As A Barrier For MOM Capacitors In CMOS Technologies
09281642	6317643	1999-03-31	2001-11-13	Granted	United States of America	Manufacturing And Engineering Data Base
09236763	6278105	1999-01-25	2001-08-21	Granted	United States of America	Transistor Utilizing Photonic Band\(miGap Material And Integrated Circuit Devices Comprising Same
09197351	6246060	1998-11-20	2001-06-12	Granted	United States of America	Apparatus For Holding And Aligning A Scanning Electron Microscope Sample
09136095	6080671	1998-08-18	2000-06-27	Granted	United States of America	Process Of Chemical-Mechanical Polishing And Manufacturing An Integrated Circuit
09099715	6121124	1998-06-18	2000-09-19	Granted	United States of America	Process For Fabricating Integrated Circuits With Dual Gate Devices Therein
09113583	6146975	1998-07-10	2000-11-14	Granted	United States of America	Shallow Trench Isolation
08980943	5951382	1997-12-01	1999-09-14	Granted	United States of America	Chemical Mechanical Polishing Carrier Fixture and System
09039213	6043496	1998-03-14	2000-03-28	Granted	United States of America	Method Of Linewidth Monitoring For Nanolithography
09062606	5897362	1998-04-17	1999-04-27	Granted	United States of America	Bonding Silicon Wafers
08878579	6007685	1997-06-19	1999-12-28	Expired	United States of America	Deposition Of Highly Doped Silicon Dioxide Films
09089792	6090534	1998-06-03	2000-07-18	Granted	United States of America	Device And Method Of Decreasing Circular Defects And Charge Buildup In Integrated Circuit Fabrication

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08887587	5811844	1997-07-03	1998-09-22	Expired	United States of America	Low Noise, High Power Pseudomorphic HEMT
08871385	6001701	1997-06-09	1999-12-14	Expired	United States of America	Process For Making Bipolar Having Graded Or Modulated Collector
08988420	6258241	1997-12-10	2001-07-10	Granted	United States of America	Process For Electroplating Metals
08807209	5861651	1997-02-28	1999-01-19	Expired	United States of America	Field Effect Devices And Capacitors With Improved Thin Film Dielectrics And Method For Making Same
08970298	5951372	1997-11-14	1999-09-14	Granted	United States of America	Method Of Roughing A Metallic Surface Of A Semiconductor Deposition Tool
08761052	5894154	1996-12-05	1999-04-13	Expired	United States of America	Improved P\(miChannel MOS Transistor
08834261	5902504	1997-04-15	1999-05-11	Expired	United States of America	Systems And Method For Determining Semiconductor Wafer Temperature And Calibrating A Vapor Deposition Device
08805404	6274198	1997-02-24	2001-08-14	Expired	United States of America	Shadow Mask Deposition
08904527	5930650	1997-08-01	1999-07-27	Expired	United States of America	Method Of Etching Silicon Materials
08767758	5735963	1996-12-17	1998-04-07	Expired	United States of America	Method Of Polishing
08775790	5960302	1996-12-31	1999-09-28	Expired	United States of America	Method Of Making A Dielectric For An Integrated Circuit
08577077	6078035	1995-12-22	2000-06-20	Expired	United States of America	Integrated Circuit Processing Utilizing Microwave Radiation
08705936	5966627	1996-08-30	1999-10-12	Expired	United States of America	In-situ Doped Silicon Layers
08516060	5654540	1995-08-17	1997-08-05	Expired	United States of America	High Resolution Remote Position Detection Using Segmented Gratings
08846769	5942775	1997-04-30	1999-08-24	Expired	United States of America	Photosensing Device With Improved Spectral Response And Low Thermal Leakage
08798580	5768335	1997-02-10	1998-06-16	Expired	United States of America	Apparatus And Method For Measuring The Orientation Of A Single Crystal Surface
08370902	5534465	1995-01-10	1996-07-09	Expired	United States of America	Method For Making Multichip Circuits Using Active Semiconductor Substrates
08362616	5538921	1994-12-22	1996-07-23	Expired	United States of America	Integrated Circuit Fabrication
08573923	5683758	1995-12-18	1997-11-04	Expired	United States of America	Method Of Forming Vias
08316745	5550583	1994-10-03	1996-08-27	Expired	United States of America	Inspection Apparatus And Method
08622797	5705298	1996-03-27	1998-01-06	Expired	United States of America	Holographic Method For Generating Three-Dimensional Conformal Photo-Lithographic Masks
08622795	5764390	1996-03-27	1998-06-09	Expired	United States of America	Holographic Method For Generating Three-Dimensional Conformal Photo-Lithographic Masks
08199910	6211539	1994-02-22	2001-04-03	Granted	United States of America	Semi-Insulated Indium Phosphide Based Compositions

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08943371	5898228	1997-10-03	1999-04-27	Expired	United States of America	On-chip misalignment indication
09150076	6221681	1998-09-09	2001-04-24	Expired	United States of America	On-chip misalignment indication
09943403	6521520	2001-08-30	2003-02-18	Granted	United States of America	Semiconductor wafer arrangement and method of processing a semiconductor wafer
10321250	6707114	2002-12-16	2004-03-16	Granted	United States of America	Semiconductor wafer arrangement of a semiconductor wafer
08796945	5804249	1997-02-07	1998-09-08	Expired	United States of America	Multistep tungsten CVD process with amorphization step
09067545	6016009	1998-04-27	2000-01-18	Expired	United States of America	Integrated circuit with tungsten plug containing amorphization layer
10619978	7071113	2003-07-14	2006-07-04	Granted	United States of America	Process for removal of photoresist mask used for making vias in low K carbon-doped silicon oxide dielectric material, and for removal of etch residues from formation of vias and removal of photoresist mask
09898194	6673721	2001-07-02	2004-01-06	Granted	United States of America	Process for removal of photoresist mask used for making vias in low k carbon-doped silicon oxide dielectric material, and for removal of etch residues from formation of vias and removal of photoresist mask
09946895	6372524	2001-09-05	2002-04-16	Granted	United States of America	Method for CMP endpoint detection
60273959		2001-03-06		Expired	United States of America	Detection of CMP Endpoint With Multiple Wavelength Lasers
08851607	5898478	1997-05-05	1999-04-27	Expired	United States of America	Method of using a test reticle to optimize alignment of integrated circuit process layers
08302598	5627624	1994-10-31	1997-05-06	Expired	United States of America	Integrated circuit test reticle and alignment mark optimization method
09477170	6495408	2000-01-04	2002-12-17	Granted	United States of America	Local interconnection process for preventing dopant cross diffusion in shared gate electrodes
09020029	6034401	1998-02-06	2000-03-07	Granted	United States of America	Local interconnection process for preventing dopant cross diffusion in shared gate electrodes
09076249		1998-05-12		Abandoned	United States of America	Mosfet Device With Improved LDD Region And Method Of Making Same
08791283	5780350	1997-01-30	1998-07-14	Expired	United States of America	MOSFET device with improved LDD region and method of making same
08962420		1997-10-31		Abandoned	United States of America	Hybrid Surface/Buried-Channel MOSFET
08719773	6246093	1996-09-25	2001-06-12	Expired	United States of America	Hybrid surface/buried-channel MOSFET
09300823	6030425	1999-04-27	2000-02-29	Expired	United States of America	Catalytic acceleration and electrical bias control of CMP processing
08652905	5948697	1996-05-23	1999-09-07	Expired	United States of America	Catalytic acceleration and electrical bias control of CMP processing
08788125		1997-01-23		Abandoned	United States of America	Wafer Clamp For Chemical Vapor Deposition
08520058	5635244	1995-08-28	1997-06-03	Expired	United States of America	Method of forming a layer of material on a wafer
08463064	5525837	1995-06-05	1996-06-11	Expired	United States of America	Reliable metallization with barrier for semiconductors

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08378750	5614437	1995-01-26	1997-03-25	Expired	United States of America	Method for fabricating reliable metallization with Ta-Si-N barrier for semiconductors
08942511		1997-10-02		Abandoned	United States of America	Self-Aligned Remote Polysilicon Contacts
08474794	5674774	1995-06-07	1997-10-07	Expired	United States of America	Method of making self-aligned remote polysilicon contacts
09792691	6649219	2001-02-23	2003-11-18	Lapsed	United States of America	Process for forming a low dielectric constant fluorine and carbon-containing silicon oxide dielectric material characterized by improved resistance to oxidation
10652007	7015168	2003-08-29	2006-03-21	Lapsed	United States of America	Low dielectric constant fluorine and carbon-containing silicon oxide dielectric material characterized by improved resistance to oxidation
07954958		1992-09-30		Abandoned	United States of America	Camera
08294076	5432333	1994-08-22	1995-07-11	Expired	United States of America	Image-sensing display panels with LCD display panel and photosensor array
08863372	5977535	1997-05-27	1999-11-02	Expired	United States of America	Light sensing device having an array of photosensitive elements coincident with an array of lens formed on an optically transmissive material
08017202		1993-02-11		Abandoned	United States of America	Camera Based Devices
08287128	5760834	1994-08-08	1998-06-02	Expired	United States of America	Electronic camera with binary lens element array
08287204	5519205	1994-08-08	1996-05-21	Expired	United States of America	Color electronic camera including photosensor array having binary diffractive lens elements
08578746	5648655	1995-12-26	1997-07-15	Expired	United States of America	Sensing device for capturing a light image
08051028	5340978	1993-04-21	1994-08-23	Expired	United States of America	Image-sensing display panels with LCD display panel and photosensitive element array
10942444	7381502	2004-09-16	2008-06-03	Lapsed	United States of America	Apparatus and method to improve the resolution of photolithography systems by improving the temperature stability of the reticle
10265856	6866970	2002-10-07	2005-03-15	Lapsed	United States of America	Apparatus and method to improve the resolution of photolithography systems by improving the temperature stability of the reticle
10838384		2004-05-04		Abandoned	United States of America	Implementation of Si-Ge HBT Module with CMOS Process
10191670	6767842	2002-07-09	2004-07-27	Granted	United States of America	Implementation of Si-Ge HBT with CMOS process
10889901	7365015	2004-07-13	2008-04-29	Granted	United States of America	Damascene replacement metal gate process with controlled gate profile and length using Si1-xGex as sacrificial material
12021728		2008-01-29		Abandoned	United States of America	Damascene replacement metal gate process with controlled gate profile and length using Si1-xGex as sacrificial material
09650038	6500740	2000-08-29	2002-12-31	Expired	United States of America	Process For Fabricating Semiconductor Devices In Which The Distribution Of Dopants Is Controlled
08902044	6406952	1997-07-29	2002-06-18	Expired	United States of America	Process For Device Fabrication

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10272734	6989552	2002-10-17	2006-01-24	Lapsed	United States of America	Method For Making An Integrated Circuit Device With Dielectrically Isolated Tubs And Related Circuit
09728448	6500717	2000-12-01	2002-12-31	Granted	United States of America	Method For Making An Integrated Circuit Device With Dielectrically Isolated Tubs and Related Circuit
10300254	6762457	2002-11-20	2004-07-13	Granted	United States of America	LDMOS Device Having A Tapered Oxide
09641086	6506641	2000-08-17	2003-01-14	Granted	United States of America	The Use Of Selective Oxidation To Improve LDMOS Power Transistors
11390015		2006-03-27		Abandoned	United States of America	A Vertical Replacement-Gate Junction Field-Effect Transistor
09950384	6690040	2001-09-10	2004-02-10	Granted	United States of America	Vertical Replacement-Gate Junction Field-Effect Transistor
10723547	7033877	2003-11-26	2006-04-25	Lapsed	United States of America	A Vertical Replacement-Gate Junction Field-Effect Transistor
09885497	6617251	2001-06-19	2003-09-09	Granted	United States of America	Method of shallow trench isolation formation and planarization
10457942	6949446	2003-06-09	2005-09-27	Lapsed	United States of America	Method of shallow trench isolation formation and planarization
10409423	6821831	2003-04-08	2004-11-23	Lapsed	United States of America	Electrostatic Discharge Protection In Double Diffused MOS Transistors
09896669	6576506	2001-06-29	2003-06-10	Granted	United States of America	Electrostatic Discharge Protection In Double Diffused MOS Transistors
11821396	7800226	2007-06-22	2010-09-21	Lapsed	United States of America	Integrated Circuit With Metal Silicide Regions
10245447	7250356	2002-09-17	2007-07-31	Granted	United States of America	Method For Forming Metal Silicide Regions In An Integrated Circuit
10263638	6770536	2002-10-03	2004-08-03	Granted	United States of America	Process For Semiconductor Device Fabrication In Which A Insulating Layer Is Formed On A Semiconductor Substrate
10870834		2004-06-17		Abandoned	United States of America	Process For Semiconductor Device Fabrication In Which A Insulating Layer Is Formed On A Semiconductor Substrate
08979297	5849639	1997-11-26	1998-12-15	Granted	United States of America	Method For Removing Etching Residues And Contaminants
09164283	6046115	1998-10-01	2000-04-04	Granted	United States of America	Method for Removing Etching Residues and Contaminants
08814051	5936831	1997-03-06	1999-08-10	Expired	United States of America	Thin Film Tantalum Oxide Capacitors And Resulting Product
08918174	6075691	1997-08-25	2000-06-13	Expired	United States of America	THIN FILM CAPACITORS AND PROCESS FOR MAKING THEM
08752235	5811916	1996-11-19	1998-09-22	Expired	United States of America	Field Emission Devices Employing Enhanced Diamond Field Emitters
08752234	5744195	1996-11-19	1998-04-28	Expired	United States of America	Field Emission Devices Employing Enhanced Diamond Field Emitters
08331458	5637950	1994-10-31	1997-06-10	Expired	United States of America	Field Emission Devices Employing Enhanced Diamond Field Emitters
08379052	5561008	1995-01-27	1996-10-01	Expired	United States of America	A Process For Device Fabrication Using Projection Lithography And An Apparatus Therefor
08673705	5701014	1996-06-25	1997-12-23	Expired	United States of America	A Projection Lithography Apparatus
10383149	6872612	2003-03-06	2005-03-29	Lapsed	United States of America	Local interconnect for integrated circuit
11058498	7081379	2005-02-15	2006-07-25	Lapsed	United States of America	Local interconnect for integrated circuit
10028594	6624498	2001-12-20	2003-09-23	Granted	United States of America	Micromagnetic Device Having Alloy Of Combalt, Phosphorus and Iron
09552627	6495019	2000-04-19	2002-12-17	Granted	United States of America	Device Comprising Micromagnetic Components For Power Applications And Process For Forming Device

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09386132	6225182	1999-08-30	2001-05-01	Granted	United States of America	Simplified High Q Inductor Substrate
09800049	6410974	2001-03-05	2002-06-25	Granted	United States of America	Simplified High Q Inductor Substrate
10400279	6927494	2003-03-27	2005-08-09	Lapsed	United States of America	Local interconnect
09966464	6576544	2001-09-28	2003-06-10	Granted	United States of America	Local interconnect
09583434	6383332	2000-05-31	2002-05-07	Granted	United States of America	Endpoint detection method and apparatus which utilize a chelating agent to detect a polishing endpoint
09212503	6117779	1998-12-15	2000-09-12	Granted	United States of America	Endpoint detection method and apparatus which utilize a chelating agent to detect a polishing endpoint
12220644		2008-07-25		Abandoned	United States of America	In-Situ Metrology System and Method for Monitoring Metalization and Other Thin Film Formation
10328066	7414721	2002-12-23	2008-08-19	Granted	United States of America	In-situ metrology system and method for monitoring metalization and other thin film formation
10164909	6555475	2002-06-07	2003-04-29	Granted	United States of America	Arrangement and method for polishing a surface of a semiconductor wafer
09750639	6439981	2000-12-28	2002-08-27	Granted	United States of America	Arrangement and method for polishing a surface of a semiconductor wafer
10099641	6800940	2002-03-15	2004-10-05	Granted	United States of America	Low k dielectric composite layer for integrated circuit structure which provides void-free low k dielectric material between metal lines while mitigating via poisoning
09426056	6391795	1999-10-22	2002-05-21	Granted	United States of America	Low k dielectric composite layer for intergrated circuit structure which provides void-free low k dielectric material between metal lines while mitigating via poisoning
10197956	6807655	2002-07-16	2004-10-19	Lapsed	United States of America	Adaptive off tester screening method based on intrinsic die parametric measurements
60381746		2002-05-17		Expired	United States of America	Process and Apparatus for Wafer Edge Profile Control Using Gas Flow Control Ring
10821708		2004-04-09		Abandoned	United States of America	Process and Apparatus for Wafer Edge Profile Control Using Gas Flow Control Ring
10200469	6753255	2002-07-18	2004-06-22	Granted	United States of America	Process for wafer edge profile control using gas flow control ring
09609527	6455363	2000-07-03	2002-09-24	Granted	United States of America	System to improve SER immunity and punchthrough
10191107		2002-07-09		Abandoned	United States of America	System To Improve SER Immunity And Punchthrough
10602510	6768130	2003-06-24	2004-07-27	Granted	United States of America	Integration of semiconductor on implanted insulator
10060867	6613639	2002-01-30	2003-09-02	Granted	United States of America	Forming a semiconductor on implanted insulator
09690047	6557566	2000-10-16	2003-05-06	Granted	United States of America	Method and apparatus for washing drums
10370812	6672320	2003-02-20	2004-01-06	Lapsed	United States of America	Apparatus for washing drums
10002413	6621404	2001-10-23	2003-09-16	Granted	United States of America	Low temperature coefficient resistor
10615039	6960979	2003-07-08	2005-11-01	Lapsed	United States of America	Low temperature coefficient resistor
09528071	6530074	2000-03-17	2003-03-04	Granted	United States of America	Apparatus For Verification Of IC Mask Sets

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10317147	7103869	2002-12-11	2006-09-05	Lapsed	United States of America	Method Of Verifying IC Mask Sets
08678971	5821148	1996-07-12	1998-10-13	Expired	United States of America	Method of Fabricating a Segmented Emitter Low Noise Transistor
08484675	5723897	1995-06-07	1998-03-03	Expired	United States of America	Segmented Emitter Low Noise Transistor
09643784	6383923	2000-08-22	2002-05-07	Granted	United States of America	Article Comprising Vertically Nano-InterConnected Circuit Devices And Method For Making The Same
09426457	6340822	1999-10-05	2002-01-22	Granted	United States of America	Article Comprising Vertically Nano-InterConnected Circuit Devices And Method For Making The Same
09408299	6323044	1999-09-29	2001-11-27	Granted	United States of America	Integrated Circuit Capacitor And Associated Fabrication Methods
09951178	6525358	2001-09-13	2003-02-25	Granted	United States of America	Capacitor Having The Lower Electrode For Preventing Undesired Defects At The Surface Of The Metal Plug
10776752	6927125	2004-02-11	2005-08-09	Granted	United States of America	Interdigitated Capacitor And Method Of Manufacturing Thereof
09929188	6740922	2001-08-14	2004-05-25	Granted	United States of America	Interdigitated Capacitor And Method Of Manufacturing Thereof
08878242	6090686	1997-06-18	2000-07-18	Expired	United States of America	LOCOS Isolation Process Using Layered PAD Nitride And Dry Field Oxidation Stack And Semiconductor Device Employing The Same
09205413	6380606	1998-12-02	2002-04-30	Expired	United States of America	Locos Isolation Process Using A Layered Pad Nitride And Dry Field Oxidation Stack And Semiconductor Device Employing The Same
08562235	5773338	1995-11-21	1998-06-30	Expired	United States of America	Bipolar Transistor With MOS-Controlled Protection For Reverse-Biased Emitter-Base Junction
09050711	5949128	1998-03-30	1999-09-07	Expired	United States of America	Bipolar Transistor With MOS\(miControlled Protection For Reverse\(miBiased Emitter\(miBase Junction
12253403	7960812	2008-10-17	2011-06-14	Granted	United States of America	Electrical Devices Having Adjustable Capacitance
10746824	7456716	2003-12-24	2008-11-25	Granted	United States of America	Electrical Devices Having Adjustable Electrical Characteristics
08848141	6054722	1997-04-28	2000-04-25	Expired	United States of America	Current Drive of TFTs in High\(miSpeed SRAMs
08572196	5625200	1995-12-14	1997-04-29	Expired	United States of America	Complementary Devices Using Thin Film Transistors With Improved Current Drive
10234354	7126198	2002-09-03	2006-10-24	Lapsed	United States of America	Protruding Spacers For Self-Aligned Contacts
11542864	7332775	2006-10-04	2008-02-19	Granted	United States of America	Protruding Spacers For Self-Aligned Contacts
08381375	5616368	1995-01-31	1997-04-01	Expired	United States of America	Field Emission Devices Employing Activated Diamond Particle Emitters And Methods For Making Same
08361616	5709577	1994-12-22	1998-01-20	Expired	United States of America	Method Of Making Field Emission Devices Employing Ultra-Fine Diamond Particle Emitters
09006347	5977697	1998-01-13	1999-11-02	Expired	United States of America	Field Emission Devices Employing Diamond Particle Emitters
09573137	6566186	2000-05-17	2003-05-20	Granted	United States of America	Capacitor with stoichiometrically adjusted dielectric and method of fabricating same
10382709	6951787	2003-03-06	2005-10-04	Lapsed	United States of America	Capacitor with stoichiometrically adjusted dielectric and method of fabricating same
11122375		2005-05-05		Abandoned	United States of America	Capacitor with Stoichiometrically Adjusted Dielectric and Method of Fabricating Same

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09960765	6504219	2001-09-21	2003-01-07	Granted	United States of America	Indium field implant for punchthrough protection in semiconductor devices
09469579	6342429	1999-12-22	2002-01-29	Granted	United States of America	Method of fabricating an indium field implant for punchthrough protection in semiconductor devices
09211024	6168502	1998-12-14	2001-01-02	Expired	United States of America	Subsonic to supersonic and ultrasonic conditioning of a polishing pad in a chemical mechanical polishing apparatus
08696445	5868608	1996-08-13	1999-02-09	Expired	United States of America	Subsonic to supersonic and ultrasonic conditioning of a polishing pad in a chemical mechanical polishing apparatus
09052851	6057571	1998-03-31	2000-05-02	Granted	United States of America	High aspect ratio, metal-to-metal, linear capacitor for an integrated circuit
09221023	6251740	1998-12-23	2001-06-26	Granted	United States of America	Method of forming and electrically connecting a vertical interdigitated metal-insulator-metal capacitor extending between interconnect layers in an integrated circuit
09219655	6417535	1998-12-23	2002-07-09	Granted	United States of America	Vertical interdigitated metal-insulator-metal capacitor for an integrated circuit
09052793	6358837	1998-03-31	2002-03-19	Granted	United States of America	Method of electrically connecting and isolating components with vertical elements extending between interconnect layers in an integrated circuit
09525489	6441419	2000-03-15	2002-08-27	Granted	United States of America	Encapsulated-metal vertical-interdigitated capacitor and damascene method of manufacturing same
09907424	6489231	2001-07-17	2002-12-03	Granted	United States of America	Method for forming barrier and seed layer
10268735		2002-10-10		Abandoned	United States of America	Barrier and Seed Layer System
09027307	6004880	1998-02-20	1999-12-21	Granted	United States of America	Method of single step damascene process for deposition and global planarization
09365440	6090239	1999-08-02	2000-07-18	Granted	United States of America	Method of single step damascene process for deposition and global planarization
08604867	5688709	1996-02-14	1997-11-18	Expired	United States of America	Method for forming composite trench-fin capacitors for DRAMS
08879341	6081008	1997-06-20	2000-06-27	Expired	United States of America	Composite trench-fin capacitors for DRAM
08552461	5670425	1995-11-09	1997-09-23	Expired	United States of America	Process for making integrated circuit structure comprising local area interconnects formed over semiconductor substrate by selective deposition on seed layer in patterned trench
08873809	5895261	1997-06-12	1999-04-20	Expired	United States of America	Process for making integrated circuit structure comprising local area interconnects formed over semiconductor substrate by selective deposition on seed layer in patterned trench
09454257	6297558	1999-12-02	2001-10-02	Expired	United States of America	Slurry filling a recess formed during semiconductor fabrication
08899111	6069085	1997-07-23	2000-05-30	Expired	United States of America	Slurry filling a recess formed during semiconductor fabrication

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08752334		1996-11-19		Abandoned	United States of America	Structure For Reduction Of Channeling During Implantation Of Source And Drain Regions In Formation Of Mos Integrated Circuit Structures
08546921	5614428	1995-10-23	1997-03-25	Expired	United States of America	Process and structure for reduction of channeling during implantation of source and drain regions in formation of MOS integrated circuit structures
08704472	5763302	1996-08-20	1998-06-09	Expired	United States of America	Self-aligned twin well process
08768845	5770492	1996-12-18	1998-06-23	Expired	United States of America	Self-aligned twin well process
08488075	5583062	1995-06-07	1996-12-10	Expired	United States of America	Self-aligned twin well process having a SiO2-polysilicon-SiO2 barrier mask
08374193	5646073	1995-01-18	1997-07-08	Expired	United States of America	Process for selective deposition of polysilicon over single crystal silicon substrate and resulting product
08823829	5818100	1997-03-25	1998-10-06	Expired	United States of America	Product resulting from selective deposition of polysilicon over single crystal silicon substrate
08566161		1995-11-30		Abandoned	United States of America	Product Resulting From Selective Deposition Of Polysilicon Over Single Crystal Silicon Substrate
08438613		1995-05-10		Abandoned	United States of America	Microelectronic Integrated Circuit Including Triangular Semiconductor And Gate Device
08567952	5631581	1995-12-06	1997-05-20	Expired	United States of America	Microelectronic integrated circuit including triangular semiconductor and gate device
08788403	5739580	1997-01-27	1998-04-14	Expired	United States of America	Oxide formed in semiconductor substrate by implantation of substrate with a noble gas prior to oxidation
08434674	5707888	1995-05-04	1998-01-13	Expired	United States of America	Oxide formed in semiconductor substrate by implantation of substrate with a noble gas prior to oxidation
11383171	7460211	2006-05-12	2008-12-02	Lapsed	United States of America	Apparatus for wafer patterning to reduce edge exclusion zone
10980945	7074710	2004-11-03	2006-07-11	Lapsed	United States of America	Method of wafer patterning for reducing edge exclusion zone
10893659	7071094	2004-07-16	2006-07-04	Granted	United States of America	Dual layer barrier film techniques to prevent resist poisoning
11418873	7393780	2006-05-04	2008-07-01	Granted	United States of America	Dual layer barrier film techniques to prevent resist poisoning
09896363	6812134	2001-06-28	2004-11-02	Granted	United States of America	Dual layer barrier film techniques to prevent resist poisoning
08485517	5696428	1995-06-07	1997-12-09	Expired	United States of America	Apparatus and method using optical energy for specifying and quantitatively controlling chemically-reactive components of semiconductor processing plasma etching gas
08986681		1997-12-08		Abandoned	United States of America	Apparatus For Igniting Low Pressure Inductively Coupled Plasma
11964920	7565592	2007-12-27	2009-07-21	Lapsed	United States of America	Failure Analysis and Testing of Semi-Conductor Devices Using Intelligent Software on Automated Test Equipment (ATE)
11670031	7430700	2007-02-01	2008-09-30	Granted	United States of America	Failure analysis and testing of semi-conductor devices using intelligent software on automated test equipment (ATE)

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11028695	7203877	2005-01-04	2007-04-10	Granted	United States of America	Failure analysis and testing of semi-conductor devices using intelligent software on automated test equipment (ATE)
08955384	5897381	1997-10-21	1999-04-27	Expired	United States of America	Method of forming a layer and semiconductor substrate
08954791	5893952	1997-10-21	1999-04-13	Expired	United States of America	Apparatus for rapid thermal processing of a wafer
08678718	5756369	1996-07-11	1998-05-26	Expired	United States of America	Rapid thermal processing using a narrowband infrared source and feedback
10930590	8404960	2004-08-31	2013-03-26	Granted	United States of America	Method for Heat Dissipation on Semiconductor Device
13775922	8653357	2013-02-25	2014-02-18	Lapsed	United States of America	Method for Heat Dissipation on Semiconductor Device
10921538	7129101	2004-08-18	2006-10-31	Lapsed	United States of America	Failure analysis vehicle for yield enhancement with self test at speed burnin capability for reliability testing
11527108	7420229	2006-09-25	2008-09-02	Granted	United States of America	Failure analysis vehicle for yield enhancement with self test at speed burnin capability for reliability testing
10307018	6781151	2002-11-27	2004-08-24	Granted	United States of America	Failure analysis vehicle
08521795	5585286	1995-08-31	1996-12-17	Expired	United States of America	Implantation of a semiconductor substrate with controlled amount of noble gas ions to reduce channeling and/or diffusion of a boron dopant subsequently implanted into the substrate to form P-LDD region of a PMOS device
08677078	5717238	1996-07-09	1998-02-10	Expired	United States of America	Substrate with controlled amount of noble gas ions to reduce channeling and/or diffusion of a boron dopant forming P-LDD region of a PMOS device
08502566	5543643	1995-07-13	1996-08-06	Expired	United States of America	Combined JFET and MOS transistor device, circuit
08612337	5631176	1996-03-06	1997-05-20	Expired	United States of America	Method of making combined JFET & MOS transistor device
08578743	5686855	1995-12-26	1997-11-11	Expired	United States of America	Process monitor for CMOS integrated circuits
08287653	5486786	1994-08-09	1996-01-23	Expired	United States of America	Process monitor for CMOS integrated circuits
08506821	5631596	1995-07-25	1997-05-20	Expired	United States of America	Process monitor for CMOS integrated circuits
11425295	8089130	2006-06-20	2012-01-03	Granted	United States of America	Semiconductor Device And Process For Reducing Damaging Breakdown In Gate Dielectrics
13311299	8241986	2011-12-05	2012-08-14	Granted	United States of America	Semiconductor Device And Process For Reducing Damaging Breakdown In Gate Dielectrics
09804783	6586326	2001-03-13	2003-07-01	Lapsed	United States of America	Metal planarization system
10400278	6951808	2003-03-27	2005-10-04	Lapsed	United States of America	Metal planarization system
11337460	7220362	2006-01-23	2007-05-22	Granted	United States of America	Planarization with reduced dishing
10421068	7029591	2003-04-23	2006-04-18	Lapsed	United States of America	Planarization with reduced dishing
11695169		2007-04-02		Abandoned	United States of America	Planarization with Reduced Dishing
10801310	7395522	2004-03-16	2008-07-01	Granted	United States of America	Yield profile manipulator
12117379	7930655	2008-05-08	2011-04-19	Granted	United States of America	Yield Profile Manipulator
08473543	5659189	1995-06-07	1997-08-19	Expired	United States of America	Layout configuration for an integrated circuit gate array

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08665016	5650348	1996-06-11	1997-07-22	Expired	United States of America	Method of making an integrated circuit chip having an array of logic gates
08892827	5773854	1997-07-15	1998-06-30	Expired	United States of America	Method of fabricating a linearly continuous integrated circuit gate array
09792683	6572925	2001-02-23	2003-06-03	Granted	United States of America	Process for forming a low dielectric constant fluorine and carbon containing silicon oxide dielectric material
10397993		2003-03-25		Abandoned	United States of America	Low Dielectric Constant Fluorine and Carbon-Containing Silicon Oxide Dielectric Material Characterized by Improved Resistance to Oxidation
10243562	6885436	2002-09-13	2005-04-26	Lapsed	United States of America	Optical error minimization in a semiconductor manufacturing apparatus
11473627	7298458	2006-06-22	2007-11-20	Granted	United States of America	Optical error minimization in a semiconductor manufacturing apparatus
11075195	7098996	2005-03-07	2006-08-29	Lapsed	United States of America	Optical error minimization in a semiconductor manufacturing apparatus
11419548	7259462	2006-05-22	2007-08-21	Granted	United States of America	Interconnect dielectric tuning
10915719	7081406	2004-08-10	2006-07-25	Lapsed	United States of America	Interconnect dielectric tuning
10417708	7056392	2003-04-16	2006-06-06	Lapsed	United States of America	Wafer chucking apparatus and method for spin processor
11403137	7201176	2006-04-11	2007-04-10	Granted	United States of America	Wafer chucking apparatus for spin processor
10153011	6794756	2002-05-21	2004-09-21	Granted	United States of America	Integrated circuit structure having low dielectric constant material and having silicon oxynitride caps over closely spaced apart metal lines
09425552	6423628	1999-10-22	2002-07-23	Granted	United States of America	Method of forming integrated circuit structure having low dielectric constant material and having silicon oxynitride caps over closely spaced apart metal lines
11258253	7582938	2005-10-25	2009-09-01	Lapsed	United States of America	I/O and Power ESD Protection Circuits by Enhancing Substrate-Bias In Deep-Submicron CMOS Process
12506746	7948036	2009-07-21	2011-05-24	Granted	United States of America	I/O and Power ESD Protection Circuits by Enhancing Substrate-Bias In Deep-Submicron CMOS Process
13110581	8269280	2011-05-18	2012-09-18	Granted	United States of America	I/O and Power ESD Protection Circuits by Enhancing Substrate-Bias In Deep-Submicron CMOS Process
10676602	6979869	2003-10-01	2005-12-27	Granted	United States of America	Substrate-biased I/O and power ESD protection circuits in deep-submicron twin-well process
10328614	6972217	2002-12-23	2005-12-06	Lapsed	United States of America	Low k polymer E-beam printable mechanical support
11225310	7358594	2005-09-12	2008-04-15	Granted	United States of America	Method of forming a low k polymer E-beam printable mechanical support
10706120	6855586	2003-11-12	2005-02-15	Granted	United States of America	Low voltage breakdown element for ESD trigger device
10055082	6710990	2002-01-22	2004-03-23	Granted	United States of America	Low voltage breakdown element for ESD trigger device

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11007392	7619272	2004-12-07	2009-11-17	Lapsed	United States of America	Bi-Axial Texturing Of High-K Dielectric Films To Reduce Leakage Currents
12574479	7956401	2009-10-06	2011-06-07	Granted	United States of America	Bi-Axial Texturing Of High-K Dielectric Films To Reduce Leakage Currents
11506659	7456076	2006-08-18	2008-11-25	Granted	United States of America	Techniques for forming passive devices during semiconductor back-end processing
10944373	7122436	2004-09-16	2006-10-17	Lapsed	United States of America	Techniques for forming passive devices during semiconductor back-end processing
11856196	7612427	2007-09-17	2009-11-03	Granted	United States of America	Apparatus For Confining Inductively Coupled Surface Currents
11248509	7397105	2005-10-12	2008-07-08	Granted	United States of America	Apparatus to passivate inductively or capacitively coupled surface currents under capacitor structures
11010970	7285840	2004-12-12	2007-10-23	Granted	United States of America	Apparatus for confining inductively coupled surface currents
60578890		2004-06-10		Abandoned	United States of America	Vortex Phase Shift Mask Applied to Optical Direct Write
13722648	9188848	2012-12-20	2015-11-17	Lapsed	United States of America	Maskless Vortex Phase Shift Optical Direct Write Lithography
13253554	8377633	2011-10-05	2013-02-19	Lapsed	United States of America	Maskless Vortex Phase Shift Optical Direct Write Lithography
11011896	8057963	2004-12-14	2011-11-15	Lapsed	United States of America	Maskless Vortex Phase Shift Optical Direct Write Lithography
11210986		2005-08-24		Abandoned	United States of America	Temperature Control System
09670975	6967177	2000-09-27	2005-11-22	Granted	United States of America	Temperature control system
10035501	6743474	2001-10-25	2004-06-01	Granted	United States of America	Method for growing thin films
10804980	7081296	2004-03-16	2006-07-25	Lapsed	United States of America	Method for growing thin films
11741195	7825522	2007-04-27	2010-11-02	Lapsed	United States of America	Hybrid Bump Capacitor
12885722	8384226	2010-09-20	2013-02-26	Lapsed	United States of America	Hybrid Bump Capacitor
10327283		2002-12-19		Abandoned	United States of America	Diamond Metal-Filled Patterns Achieving Low Parasitic Coupling Capacitance
11016468	6998716	2004-12-16	2006-02-14	Granted	United States of America	Diamond metal-filled patterns achieving low parasitic coupling capacitance
10035704	6727177	2001-10-18	2004-04-27	Granted	United States of America	Multi-step process for forming a barrier film for use in copper layer formation
11733673	7413984	2007-04-10	2008-08-19	Granted	United States of America	Multi-step process for forming a barrier film for use in copper layer formation
10772133	7229923	2004-02-03	2007-06-12	Granted	United States of America	Multi-step process for forming a barrier film for use in copper layer formation
10265867		2002-10-07		Abandoned	United States of America	MOS Transistor Having Aluminum Nitride Gate Structure And Method Of Manufacturing Same
09472331	6495409	1999-12-23	2002-12-17	Granted	United States of America	MOS Transistor Having Aluminum Nitride Gate Structure And Method Of Manufacturing Same

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11106307		2005-04-14		Abandoned	United States of America	Ultra Low Dielectric Constant Thin Film
10691400	6905909	2003-10-22	2005-06-14	Lapsed	United States of America	Ultra low dielectric constant thin film
11540056	7239160	2006-09-29	2007-07-03	Granted	United States of America	Method Of Electrical Testing Of An Integrated Circuit With An Electrical Probe
11138152	7132840	2005-05-26	2006-11-07	Granted	United States of America	Method Of Electrical Testing
10825342	7270942	2004-04-14	2007-09-18	Granted	United States of America	Optimized mirror design for optical direct write
60513780		1900-01-01		Abandoned	United States of America	New Optimized Mirror Design for Optical Direct Write
11769486	7738078	2007-06-27	2010-06-15	Lapsed	United States of America	Optimized Mirror Design For Optical Direct Write
09818799	6400090	2001-03-27	2002-06-04	Granted	United States of America	Electron Emitters For Lithography Tools
09306287	6232040	1999-05-06	2001-05-15	Granted	United States of America	Electron Emitters For Lithography Tools
09332061	6251543	1999-06-14	2001-06-26	Granted	United States of America	Process For Fabricating A Projection Electron Lithography Mask And A Removable, Reuseable Cover For Use Therein
09854753	6372393	2001-05-15	2002-04-16	Granted	United States of America	Process For Fabricating A Projection Electron Lithography Mask And A Removable, Reuseable Cover For Use Therein
08879100	6121159	1997-06-19	2000-09-19	Expired	United States of America	Polymeric dielectric layers having low dielectric constants and improved adhesion to metal lines
09618211	6455934	2000-07-10	2002-09-24	Expired	United States of America	Polymeric dielectric layers having low dielectric constants and improved adhesion to metal lines
10628601	6943055	2003-07-28	2005-09-13	Lapsed	United States of America	Method and apparatus for detecting backside contamination during fabrication of a semiconductor wafer
10138742	6627466	2002-05-03	2003-09-30	Lapsed	United States of America	Method and apparatus for detecting backside contamination during fabrication of a semiconductor wafer
10368811	6977400	2003-02-18	2005-12-20	Lapsed	United States of America	Silicon germanium CMOS channel
09724444	6544854	2000-11-28	2003-04-08	Granted	United States of America	Silicon germanium CMOS channel
10454027	6880140	2003-06-04	2005-04-12	Lapsed	United States of America	Method to selectively identify reliability risk die based on characteristics of local regions on the wafer
11031564	7390680	2005-01-06	2008-06-24	Granted	United States of America	Method to selectively identify reliability risk die based on characteristics of local regions on the wafer
09652479	6373087	2000-08-31	2002-04-16	Granted	United States of America	Methods of Fabricating A Metal-Oxide-Metal Capacitor And Associated Apparatus
10080186	6730601	2002-02-21	2004-05-04	Granted	United States of America	Methods of Fabricating A Metal-Oxide-Metal Capacitor
10020304	6747318	2001-12-13	2004-06-08	Granted	United States of America	Buried channel devices and a process for their fabrication simultaneously with surface channel devices to produce transistors and capacitors with multiple electrical gate oxides
10786481		2004-02-24		Abandoned	United States of America	Buried Channel Devices And A Process For Their Fabrication Simultaneously With Surface Channel Devices To Produce Transistors And Capacitors With Multiple Electrical Gate Oxides
11265062	7635888	2005-11-02	2009-12-22	Granted	United States of America	Interdigitated Capacitors

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10886763	7022581	2004-07-08	2006-04-04	Granted	United States of America	Interdigitated Capacitors
12616050	8039923	2009-11-10	2011-10-18	Granted	United States of America	Interdigitated Capacitors
10649140	6821851	2003-08-27	2004-11-23	Granted	United States of America	Method Of Making Ultra Thin Body Vertical Replacement Gate Mosfet
10164202	6635924	2002-06-06	2003-10-21	Granted	United States of America	Ultra Thin Body Vertical Replacement Gate Mosfet
09335707	6197641	1999-06-18	2001-03-06	Granted	United States of America	Process For Fabricating Vertical Transistors
09143274	6027975	1998-08-28	2000-02-22	Granted	United States of America	Process For Fabricating Vertical Transistors
11641507	7537984	2006-12-19	2009-05-26	Lapsed	United States of America	III-V Power Field Effect Transistors
10948897	7180103	2004-09-24	2007-02-20	Granted	United States of America	III/V Power Field Effect Transistors
10404832	7329926	2003-04-01	2008-02-12	Granted	United States of America	Semiconductor Device With Constricted Current Passage
11872347	7569445	2007-10-15	2009-08-04	Lapsed	United States of America	Semiconductor Device With Constricted Current Passage
09723557	6455418	2000-11-28	2002-09-24	Granted	United States of America	Barrier For Copper Metallization
09218649	6288449	1998-12-22	2001-09-11	Granted	United States of America	Barrier For Copper Metallization
11533785	8049282	2006-09-21	2011-11-01	Lapsed	United States of America	Bipolar Device Having Buried Contacts
13222877	8372723	2011-08-31	2013-02-12	Lapsed	United States of America	Bipolar Device Having Buried Contacts
09602797	6288454	2000-06-23	2001-09-11	Granted	United States of America	Semiconductor wafer having a layer-to-layer alignment mark and method for fabricating the same
09311253	6136662	1999-05-13	2000-10-24	Granted	United States of America	Semiconductor wafer having a layer-to-layer alignment mark and method for fabricating the same
11937199	7560292	2007-11-08	2009-07-14	Lapsed	United States of America	Voltage Contrast Monitor for Integrated Circuit Defects
10652369	6936920	2003-08-29	2005-08-30	Lapsed	United States of America	Voltage contrast monitor for integrated circuit defects
11131705	7323768	2005-05-18	2008-01-29	Lapsed	United States of America	Voltage contrast monitor for integrated circuit defects
09246402	6214675	1999-02-08	2001-04-10	Granted	United States of America	A Method For Fabricating A Merged Integrated Circuit Device
09789254	6627963	2001-02-20	2003-09-30	Granted	United States of America	Method For Fabricating A Merged Integrated Circuit Device
11827807	7632690	2007-07-13	2009-12-15	Lapsed	United States of America	Real-Time Gate Etch Critical Dimension Control By Oxygen Monitoring
10675572	7261745	2003-09-30	2007-08-28	Granted	United States of America	Real-Time Gate Etch Critical Dimension Control By Oxygen Monitoring
10814682		2004-03-31		Abandoned	United States of America	Semiconductor Device Having A Doped Lattice Matching Layer And A Method Of Manufacture Therefor
10003873	6737339	2001-10-24	2004-05-18	Granted	United States of America	Semiconductor Device Having A Doped Lattice Matching Layer And A Method Of Manufacture Therefor
10814680	6855991	2004-03-31	2005-02-15	Granted	United States of America	Semiconductor Device Having A Doped Lattice Matching Layer And A Method Of Manufacture Therefor
10773900	7078280	2004-02-06	2006-07-18	Lapsed	United States of America	Vertical Replacement-Gate Silicon-On-Insulator Transistor
11419356	7259048	2006-05-19	2007-08-21	Granted	United States of America	Vertical Replacement-Gate Silicon-On-Insulator Transistor
09968234	6709904	2001-09-28	2004-03-23	Granted	United States of America	Vertical Replacement-Gate (VRG) Silicon-On-Insulator (SOI) CMOS Transistor

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11419252	7381607	2006-05-19	2008-06-03	Granted	United States of America	A Method Of Forming A Spiral Inductor In A Semiconductor Substrate
10646997	7075167	2003-08-22	2006-07-11	Lapsed	United States of America	A Spiral Inductor Formed In A Semiconductor Substrate And A Method For Forming The Inductor
10918981	7345354	2004-08-16	2008-03-18	Granted	United States of America	Increased Quality Factor Of A Varactor In An Integrated Circuit Via A High Conductive Region In A Well
10454133	6825089	2003-06-04	2004-11-30	Granted	United States of America	Increased Quality Factor Of A Varactor In An Integrated Circuit Via A High Conductive Region In A Well
10648602	6884720	2003-08-25	2005-04-26	Granted	United States of America	Forming copper interconnects with Sn coatings
11074456	7675177	2005-03-07	2010-03-09	Lapsed	United States of America	Forming Copper Interconnects with SN Coatings
09434424	6284663	1999-11-04	2001-09-04	Granted	United States of America	Method For Making Field Effect Devices And Capacitors With Thin Film Dielectrics And Resulting Devices
09060420	6001741	1998-04-15	1999-12-14	Granted	United States of America	Method For Making Field Effect Devices And Capacitors With Improved Thin Film Dielectrics And Resulting Devices
10400310	6753268	2003-03-27	2004-06-22	Granted	United States of America	Reduced particulate etching
09898267	6576981	2001-07-03	2003-06-10	Granted	United States of America	Reduced particulate etching
09071006	5907165	1998-05-01	1999-05-25	Granted	United States of America	InP Heterostructure Devices
09255845	6165859	1999-02-23	2000-12-26	Granted	United States of America	Method Of Making InP Heterostructure Devices
08965706	6107191	1997-11-07	2000-08-22	Granted	United States of America	Method Of Creating An Interconnect In A Substrate And Semiconductor Device Employing The Same
09428073	6222255	1999-10-27	2001-04-24	Granted	United States of America	Method Of Creating an Interconnect In A Substrate And Semiconductor Device Employing The Same
08848109	6025280	1997-04-28	2000-02-15	Expired	United States of America	System And Method For Forming A High Quality Ultrathin Gate Oxide Layer
09338939	6281138	1999-06-24	2001-08-28	Expired	United States of America	System And Method For Forming A High Quality Ultrathin Gate Oxide Layer
09049531	6033202	1998-03-27	2000-03-07	Granted	United States of America	Mold For Non-Photolithographic Fabrication Of Microstructures
09393032	6322736	1999-09-09	2001-11-27	Granted	United States of America	Mold For Non-Photolithographic Fabrication Of Microstructures
08820063	5913146	1997-03-18	1999-06-15	Expired	United States of America	Semiconductor Device Having Aluminum Contacts Or Vias And Method Of Manufacture Therefor
09166832	6157082	1998-10-05	2000-12-05	Expired	United States of America	Semiconductor Device Having Aluminum Contacts Or Vias And Method Of Manufacture Therefor
08346444	5462012	1994-11-29	1995-10-31	Expired	United States of America	Substrates and Methods for Gas Phase Deposition of Semiconductors and Other Materials
08475110	5589693	1995-06-07	1996-12-31	Expired	United States of America	Substrates and methods for gas phase deposition of semiconductors and othermaterials
09073556	6028359	1998-05-06	2000-02-22	Expired	United States of America	Integrated Circuit Having Amorphous Silicide Layer In Contacts And Vias And Method Of Manufacture Therefor

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08816185	5858873	1997-03-12	1999-01-12	Expired	United States of America	Integrated Circuit Having Amorphous Silicide Layer In Contacts And Vias AndMethod Of Manufacture Therefor
09489092	6498364	2000-01-21	2002-12-24	Granted	United States of America	A Capacitor For Integration With Copper Damascene Processes
10195935	7135733	2002-07-16	2006-11-14	Granted	United States of America	Capacitor For Integration With Copper Damascene Processes And A Method Of Manufacture Therefore
09580530	6333508	2000-05-30	2001-12-25	Granted	United States of America	Illumination System For Electron Beam Lithography Tool
09414004	7345290	1999-10-07	2008-03-18	Granted	United States of America	Lens Array For Electron Beam Lithography Tool
09642376	6534851	2000-08-21	2003-03-18	Granted	United States of America	Modular Semiconductor Substrates
10303280	6713409	2002-11-25	2004-03-30	Granted	United States of America	Semiconductor Manufacturing Using Modular Substrates
09557536	6387772	2000-04-25	2002-05-14	Granted	United States of America	Method For Forming Trenches Capacitors In Soi Substrates
10072500	6552381	2002-02-05	2003-04-22	Granted	United States of America	Trench Capacitors In Soi Substrates
09654689	6613651	2000-09-05	2003-09-02	Lapsed	United States of America	Integrated circuit isolation system
10383031	6831348	2003-03-06	2004-12-14	Lapsed	United States of America	Integrated circuit isolation system
09737504	6271911	2000-12-15	2001-08-07	Granted	United States of America	Apparatus for enhancing image contrast using intensity filtration
09557946	6549322	2000-04-24	2003-04-15	Granted	United States of America	Method and apparatus for enhancing image contrast using intensity filtration
10368812	7033710	2003-02-18	2006-04-25	Lapsed	United States of America	Method and apparatus for enhancing image contrast using intensity filtration
09106720		1998-06-29		Abandoned	United States of America	Method and Apparatus for Enhancing Image Contrast Using Intensity Filtration
10418560	6861864	2003-04-16	2005-03-01	Lapsed	United States of America	Self-timed reliability and yield vehicle array
10900642	7308627	2004-07-27	2007-12-11	Granted	United States of America	Self-timed reliability and yield vehicle with gated data and clock
10909821		2004-08-02		Abandoned	United States of America	Semiconductor Wafer Chuck Assembly for a Semiconductor Processing Device
10461255	6805338	2003-06-13	2004-10-19	Granted	United States of America	Semiconductor wafer chuck assembly for a semiconductor processing device
09540473	6373266	2000-03-31	2002-04-16	Granted	United States of America	Apparatus And Method For Determining Process Width Variations In Integrated Circuits
10053097	6728940	2002-01-18	2004-04-27	Granted	United States of America	Apparatus And Method For Determining Process Width Variations In Integrated Circuits
09466715	6458648	1999-12-17	2002-10-01	Granted	United States of America	Method For In-Situ Removal Of Side Walls In MOM Capacitor Formation
10215170	6656850	2002-08-08	2003-12-02	Granted	United States of America	Method For In-Situ Removal Of Side Walls In MOM Capacitor Formation
10147384	6683382	2002-05-16	2004-01-27	Granted	United States of America	Semiconductor Device Having An Interconnect Layer With A Plurality Of Layout Regions Having Substantially Uniform Densities Of Active Interconnects And Dummy Fills

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09484310	6436807	2000-01-18	2002-08-20	Granted	United States of America	Method For Making An Interconnect Layer And A Semiconductor Device Including The Same
10414601	7276441	2003-04-15	2007-10-02	Granted	United States of America	Dielectric barrier layer for increasing electromigration lifetimes in copper interconnect structures
12764004	8043968	2010-04-20	2011-10-25	Granted	United States of America	Dielectric Barrier Layer For Increasing Electromigration Lifetimes In Copper Interconnect Structures
11736402	7728433	2007-04-17	2010-06-01	Lapsed	United States of America	Dielectric Barrier Layer For Increasing Electromigration Lifetimes In Copper Interconnect Structures
09861839	6475931	2001-05-21	2002-11-05	Granted	United States of America	Method For Producing Devices Having Piezoelectric Films
09502868	6329305	2000-02-11	2001-12-11	Granted	United States of America	Method For Producing Devices Having Piezoelectric Films
10418375	6982229	2003-04-18	2006-01-03	Lapsed	United States of America	Ion recoil implantation and enhanced carrier mobility in CMOS device
11098290	7129516	2005-04-04	2006-10-31	Lapsed	United States of America	Ion recoil implantation and enhanced carrier mobility in CMOS device
10360903	6874510	2003-02-07	2005-04-05	Lapsed	United States of America	Method to use a laser to perform the edge clean operation on a semiconductor wafer
11014476		2004-12-16		Abandoned	United States of America	Method to Use a Laser to Perform the Edge Clean Operation on a Semiconductor Wafer
08791244	6117736	1997-01-30	2000-09-12	Expired	United States of America	Method of fabricating insulated-gate field-effect transistors having different gate capacitances
09594478	6300663	2000-06-15	2001-10-09	Expired	United States of America	Insulated-gate field-effect transistors having different gate capacitances
09665988	6553166	2000-09-20	2003-04-22	Lapsed	United States of America	Concentric optical cable with full duplex connectors
09956409		2001-09-19		Abandoned	United States of America	Parallel Active Optical SCSI Cable
10697506	7323228	2003-10-29	2008-01-29	Granted	United States of America	Method of vaporizing and ionizing metals for use in semiconductor processing
11939482	7670645	2007-11-13	2010-03-02	Lapsed	United States of America	Method of Treating Metal and Metal Salts to Enable Thin Layer Deposition in Semiconductor Processing
10253158	6713394	2002-09-24	2004-03-30	Granted	United States of America	Process for planarization of integrated circuit structure which inhibits cracking of low dielectric constant dielectric material adjacent underlying raised structures
09661465	6489242	2000-09-13	2002-12-03	Granted	United States of America	Process for planarization of integrated circuit structure which inhibits cracking of low dielectric constant dielectric material adjacent underlying raised structures
09724225	6521549	2000-11-28	2003-02-18	Granted	United States of America	Method of reducing silicon oxynitride gate insulator thickness in some transistors of a hybrid integrated circuit to obtain increased differential in gate insulator thickness with other transistors of the hybrid circuit

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10304631	6656805	2002-11-26	2003-12-02	Lapsed	United States of America	Method of reducing silicon oxynitride gate insulator thickness in some transistors of a hybrid integrated circuit to obtain increased differential in gate insulator thickness with other transistors of the hybrid circuit
10205229	6566268	2002-07-25	2003-05-20	Granted	United States of America	Method and apparatus for planarizing a wafer surface of a semiconductor wafer having an elevated portion extending therefrom
09364140	6451699	1999-07-30	2002-09-17	Granted	United States of America	Method and apparatus for planarizing a wafer surface of a semiconductor wafer having an elevated portion extending therefrom
09517150	6479857	2000-03-02	2002-11-12	Lapsed	United States of America	Capacitor having a tantalum lower electrode and method of forming the same
10228859	6861310	2002-08-27	2005-03-01	Lapsed	United States of America	Capacitor having a tantalum lower electrode and method of forming the same
12191171	7646077	2008-08-13	2010-01-12	Granted	United States of America	Dielectric Barrier Films For Use As Copper Barrier Layers In Semiconductor Trench And Via Structures
10321938	6939800	2002-12-16	2005-09-06	Lapsed	United States of America	Dielectric barrier films for use as copper barrier layers in semiconductor trench and via structures
11131003	7427563	2005-05-16	2008-09-23	Granted	United States of America	Dielectric barrier films for use as copper barrier layers in semiconductor trench and via structures
09723516	6436845	2000-11-28	2002-08-20	Granted	United States of America	Silicon nitride and silicon dioxide gate insulator transistors and method of forming same in a hybrid integrated circuit
10171700	6562729	2002-06-14	2003-05-13	Granted	United States of America	Silicon nitride and silicon dioxide gate insulator transistors and method of forming same in a hybrid integrated circuit
10195044	6858531	2002-07-12	2005-02-22	Granted	United States of America	Electro chemical mechanical polishing method
11007694	7285145	2004-12-07	2007-10-23	Granted	United States of America	Electro chemical mechanical polishing method and device for planarizing semiconductor surfaces
10131431	6627556	2002-04-24	2003-09-30	Granted	United States of America	Method of chemically altering a silicon surface and associated electrical devices
10600665	6822308	2003-06-20	2004-11-23	Lapsed	United States of America	Method of chemically altering a silicon surface and associated electrical devices
10195775	6673200	2002-07-12	2004-01-06	Granted	United States of America	Method of reducing process plasma damage using optical spectroscopy
60384499		1900-01-01		Abandoned	United States of America	Impact of F Species on Plasma Charge Damage in a RF Aher
10680503	6972840	2003-10-06	2005-12-06	Lapsed	United States of America	Method of reducing process plasma damage using optical spectroscopy
10210365	6641698	2002-08-01	2003-11-04	Granted	United States of America	Integrated circuit fabrication dual plasma process with separate introduction of different gases into gas flow

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09747638	6461972	2000-12-22	2002-10-08	Granted	United States of America	Integrated circuit fabrication dual plasma process with separate introduction of different gases into gas flow
12034750		2008-02-21		Abandoned	United States of America	Laser Marking Hole Shape Of Semiconductor Wafer
10020764	7371659	2001-12-12	2008-05-13	Granted	United States of America	Substrate laser marking
09617550	6569751	2000-07-17	2003-05-27	Granted	United States of America	Low via resistance system
10400252	6893962	2003-03-27	2005-05-17	Granted	United States of America	Low via resistance system
09395507	6328802	1999-09-14	2001-12-11	Granted	United States of America	Method and apparatus for determining temperature of a semiconductor wafer during fabrication thereof
09952540	6794310	2001-09-14	2004-09-21	Granted	United States of America	Method and apparatus for determining temperature of a semiconductor wafer during fabrication thereof
11381409		2006-05-03		Abandoned	United States of America	Adjustable Transmission Phase Shift Mask
10972898	7067223	2004-10-25	2006-06-27	Lapsed	United States of America	Adjustable transmission phase shift mask
10039508	6841308	2001-11-09	2005-01-11	Lapsed	United States of America	Adjustable transmission phase shift mask
09670448	6486064	2000-09-26	2002-11-26	Granted	United States of America	Shallow junction formation
10268736	6605846	2002-10-10	2003-08-12	Granted	United States of America	Shallow junction formation
09212315	6358819	1998-12-15	2002-03-19	Granted	United States of America	Dual gate oxide process for deep submicron ICS
10026282		2001-12-21		Abandoned	United States of America	Dual Gate Oxide Process for Deep Submicron ICS
60314148		1900-01-01		Abandoned	United States of America	Process Enhancement to Prevent LI or Borderless Contact To Well Leakage
10360746	6893937	2003-02-05	2005-05-17	Granted	United States of America	Method for preventing borderless contact to well leakage
11104050	7098515	2005-04-11	2006-08-29	Lapsed	United States of America	Semiconductor chip with borderless contact that avoids well leakage
10006540	6551901	2001-11-30	2003-04-22	Granted	United States of America	Method for preventing borderless contact to well leakage
12574426	8021955	2009-10-06	2011-09-20	Granted	United States of America	Method Characterizing Materials For A Trench Isolation Structure Having Low Trench Parasitic Capacitance
11262173	7619294	2005-10-28	2009-11-17	Lapsed	United States of America	Shallow Trench Isolation Structure With Low Trench Parasitic Capacitance
09991202	7001823	2001-11-14	2006-02-21	Lapsed	United States of America	Method of manufacturing a shallow trench isolation structure with low trench parasitic capacitance
10196787	6787180	2002-07-17	2004-09-07	Granted	United States of America	Exhaust flow control system
09666507	6579371	2000-09-20	2003-06-17	Granted	United States of America	Exhaust flow control system
09952790	6964924	2001-09-11	2005-11-15	Lapsed	United States of America	Integrated circuit process monitoring and metrology system
11072127	7115425	2005-03-04	2006-10-03	Lapsed	United States of America	Integrated circuit process monitoring and metrology system
10044864	7115991	2001-10-22	2006-10-03	Lapsed	United States of America	Method for creating barriers for copper diffusion
11104763	7829455	2005-04-12	2010-11-09	Granted	United States of America	Method For Creating Barriers For Copper Diffusion
09879642	6495312	2001-06-12	2002-12-17	Granted	United States of America	Method and apparatus for removing photoresist edge beads from thin film substrates

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10263593	6614507	2002-10-03	2003-09-02	Granted	United States of America	Apparatus for removing photoresist edge beads from thin film substrates
09775223		2001-02-01		Abandoned	United States of America	Method and Apparatus for Removing Photoresist Edge Beads From Thin Film Substrates
11927950	7579245	2007-10-30	2009-08-25	Lapsed	United States of America	Dual-Gate Metal-Oxide Semiconductor Device
10999705	7329922	2004-11-30	2008-02-12	Granted	United States of America	Dual\(miGate Metal\(miOxide Semiconductor Device
10688231	7005703	2003-10-17	2006-02-28	Lapsed	United States of America	Metal-Oxide Semiconductor Device Having Improved Performance And Reliability.
11348597	7335565	2006-02-07	2008-02-26	Granted	United States of America	Metal\(miOxide Semiconductor Device Having Improved Performance And Reliability.
09083072	6024829	1998-05-21	2000-02-15	Granted	United States of America	Method Of Eliminating Agglomerate Particles In A Polishing Slurry
09427306	6355184	1999-10-26	2002-03-12	Granted	United States of America	A Method Of Eliminating Agglomerate Particles In A Polishing Slurry
09992135	6750145	2001-11-14	2004-06-15	Granted	United States of America	A Method Of Eliminating Agglomerate Particles In A Polishing Slurry
09878657	6482694	2001-06-11	2002-11-19	Granted	United States of America	Semiconductor Device Structure Including A Tantalum Pentoxide Layer Sandwiched Between Silicon Nitride Layers
09259001	6294807	1999-02-26	2001-09-25	Granted	United States of America	Semiconductor Device Structure Including A Tantalum Pentoxide Layer Sandwiched Between Silicon Nitride Layers
09894117	6439972	2001-06-28	2002-08-27	Granted	United States of America	Polishing Fluid, Polishing Method, Semiconductor Device And Semiconductor Device Fabrication Method
09483785	6328633	2000-01-14	2001-12-11	Granted	United States of America	Polishing Fluid, Polishing Method, Semiconductor Device And Semiconductor Device Fabrication Method
09461609	6409829	1999-12-15	2002-06-25	Granted	United States of America	Manufacture Of Dielectrically Isolated Integrated Circuits
10091291	6727567	2002-03-05	2004-04-27	Granted	United States of America	Integrated Circuit Device Substrates With Selective Epitaxial Growth Thickness Compensation
10762962	7276767	2004-01-22	2007-10-02	Granted	United States of America	A Thin Film Resistor Device And A Method Of Manufacture Therefor
09614992	6703666	2000-07-12	2004-03-09	Granted	United States of America	A Thin Film Resistor Device And A Method Of Manufacture Therefor
08347527	6445043	1994-11-30	2002-09-03	Granted	United States of America	Process for Forming Isolation Regions in An Integrated Circuit and Structure Formed Thereby
08620964	5763314	1996-03-22	1998-06-09	Expired	United States of America	Process For Forming Isolation Regions In An Integrated Circuit
08668310	5641994	1996-06-26	1997-06-24	Expired	United States of America	Multilayered Al-alloy Structure For Metal Conductors
08365652	5561083	1994-12-29	1996-10-01	Expired	United States of America	Method of Making Multilayered A1-alloy Structure For Metal Conductors
10750348	6969683	2003-12-31	2005-11-29	Granted	United States of America	Method of preventing resist poisoning in dual damascene structures
10025304	6713386	2001-12-19	2004-03-30	Granted	United States of America	Method of preventing resist poisoning in dual damascene structures
09962641	6495875	2001-09-25	2002-12-17	Granted	United States of America	Method Of Forming Metal Oxide Metal Capacitors Using Multi-Step Rapid Thermal Process And A Device Formed Thereby

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09418106	6323078	1999-10-14	2001-11-27	Granted	United States of America	A Method Of Forming Metal Oxide Metal Capacitors Using Multi-Step Rapid Thermal Process And A Device Formed Thereby
12243137	7713811	2008-10-01	2010-05-11	Lapsed	United States of America	Multiple Doping Level Bipolar Junctions Transistors And Method For Forming
12727304	7910425	2010-03-19	2011-03-22	Granted	United States of America	Multiple Doping Level Bipolar Junctions Transistors And Method For Forming
10953894	7095094	2004-09-29	2006-08-22	Lapsed	United States of America	Multiple Doping Level Bipolar Junctions Transistors And Method For Forming
13026528	8143120	2011-02-14	2012-03-27	Granted	United States of America	Multiple Doping Level Bipolar Junctions Transistors And Method For Forming
11458270	7449388	2006-07-18	2008-11-11	Lapsed	United States of America	Method For Forming Multiple Doping Level Bipolar Junctions Transistors
10953292	7061264	2004-09-29	2006-06-13	Lapsed	United States of America	Test Semiconductor Device And Method For Determining Joule Heating Effects In Such A Device
11403750	7388395	2006-04-13	2008-06-17	Granted	United States of America	Test Semiconductor Device And Method For Determining Joule Heating Effects In Such A Device
09940126	6573149	2001-08-27	2003-06-03	Granted	United States of America	A Semconductor Device Having A Metal Gate With A Work Function Compatible With A Semiconductor Device
10003871	6579775	2001-10-24	2003-06-17	Granted	United States of America	A Semconductor Device Having A Metal Gate With A Work Function Compatible With A Semiconductor Device
09572060	6383879	2000-05-17	2002-05-07	Granted	United States of America	A Semconductor Device Having A Metal Gate With A Work Function Compatible With A Semiconductor Device
09886780	6649422	2001-06-21	2003-11-18	Granted	United States of America	Integrated Circuit Having A Micromagnetic Device And Method Of Manufacture Therefor
09338143	6255714	1999-06-22	2001-07-03	Granted	United States of America	An Integrated Circuit Having A Micromagnetic Device And Method Of Manufacture Therefor
09578082	6465884	2000-05-24	2002-10-15	Granted	United States of America	Semiconductor Device With Variable Pin Locations
10218783	6833286	2002-08-14	2004-12-21	Granted	United States of America	Semiconductor Device With Variable Pin Locations
10038734	6762459	2001-12-31	2004-07-13	Granted	United States of America	Method For Fabricating MOS Device With Halo Implanted Region
09523782	6362054	2000-03-13	2002-03-26	Granted	United States of America	Method For Fabricating MOS Device With Halo Implanted Region
09015981	6153920	1998-01-30	2000-11-28	Expired	United States of America	A Semiconductor Device Configured to Control Dopant Diffusion In the Semiconductor Device Substrate
08862226	5731626	1997-05-23	1998-03-24	Expired	United States of America	Process For Controlling Dopant Diffusion In A Semiconductor Layer And Semiconductor Layer Formed Thereby
08848113	5982020	1997-04-28	1999-11-09	Expired	United States of America	Deuterated Bipolar Transistors And Method Of Manufacture Thereof
09386592	6309938	1999-08-31	2001-10-30	Expired	United States of America	Deuterated Bipolar Transistors And Method Of Manufacture Thereof

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09261346	6153020	1999-03-03	2000-11-28	Granted	United States of America	Process For Fabricating Improved Iron-Cobalt Magnetostrictive Alloy And Article Comprising Alloy
09500855	6299703	2000-02-09	2001-10-09	Granted	United States of America	Process For Fabricating Improved Iron-Cobalt Magnetostrictive Alloy And Article Comprising Alloy
11649197	7670203	2007-01-03	2010-03-02	Lapsed	United States of America	Process For Making An On-Chip Vacuum Tube Device
09651696	7259510	2000-08-30	2007-08-21	Granted	United States of America	On-Chip Vacuum Tube Device And Process For Making Device
08881293	5811796	1997-06-24	1998-09-22	Expired	United States of America	Optical Probe Microscope Having A Fiber Optic Tip That Receives Both A Dither Motion And A Scanning Motion, For Nondestructive Metrology Of Large Sample Surfaces
08657390	5693938	1996-06-03	1997-12-02	Expired	United States of America	Optical Probe Microscope Having A Fiber Optic Tip That Receives Both A Dither Motion And A Scanning Motion, For Nondestructive Metrology Of Large Sample Surfaces
11748569	7407824	2007-05-15	2008-08-05	Granted	United States of America	Guard Ring For Improved Matching
10941665	7253012	2004-09-14	2007-08-07	Granted	United States of America	Guard Ring For Improved Matching
09456224	6576529	1999-12-07	2003-06-10	Granted	United States of America	A Method Of Forming An Alignment Feature In Or On A Multi-Layered Semiconductor Structure
10704449	6977128	2003-11-07	2005-12-20	Lapsed	United States of America	Multi-Layered Semiconductor Structure
09867202	6706609	2001-05-29	2004-03-16	Granted	United States of America	Method Of Forming An Alignment Feature In Or On A Multi-Layered Semiconductor Structure
10360276		2003-02-07		Abandoned	United States of America	Two-Step Oxidation Process For Oxidizing A Silicon Substrate Wherein The First Step Is Carried Out At A Temperature Below The Viscoelastic Temperature Of Silicon Dioxide And The Second Step Is Carried Out At A Temperature Above The Viscoelastic Temperature
09597076	6551946	2000-06-20	2003-04-22	Granted	United States of America	Two-Step Oxidation Process For Oxidizing A Silicon Substrate Wherein The First Step Is Carried Out At A Temperature Below The Viscoelastic Temperature Of Silicon Dioxide And The Second Step Is Carried Out At A Temperature Above The Viscoelastic Temperature
10316386	7148153	2002-12-11	2006-12-12	Granted	United States of America	Process For Oxide Fabrication Using Oxidation Steps Below And Above A Threshold Temperature
11385156	7282461	2006-03-21	2007-10-16	Granted	United States of America	Phase-Shifting Mask And Semiconductor Device
10655050	7053405	2003-09-04	2006-05-30	Lapsed	United States of America	Phase-Shifting Mask And Semiconductor Device
09488662	6638663	2000-01-20	2003-10-28	Granted	United States of America	Phase-Shifting Mask And Semiconductor Device
09533428	6312565	2000-03-23	2001-11-06	Granted	United States of America	Thin Film Deposition Of Mixed Metal Oxides
09917365	6540974	2001-07-27	2003-04-01	Granted	United States of America	Process For Making Mixed Metal Oxides
10819253	7242056	2004-04-05	2007-07-10	Granted	United States of America	Structure And Fabrication Method For Capacitors Integratible With Vertical Replacement Gate Transistors

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11809686	7633118	2007-05-31	2009-12-15	Lapsed	United States of America	Structure And Fabrication Method For Capacitors Integratible With Vertical Replacement Gate Transistors
12319603	7700432	2009-01-09	2010-04-20	Lapsed	United States of America	Method of Fabricating a Vertical Transistor and Capacitor
11809873	7491610	2007-06-01	2009-02-17	Granted	United States of America	Fabrication Method
09956381		2001-09-18		Abandoned	United States of America	An Integratible Vertical Replacement Gate (VRG)-type Poly-Nitride-Poly (PNP) Or Metal-Nitride-poly (MNP) Capacitor
12610733	7911006	2009-11-02	2011-03-22	Granted	United States of America	Structure And Fabrication Method For Capacitors Integratible With Vertical Replacement Gate Transistors
09137920	6215130	1998-08-20	2001-04-10	Granted	United States of America	Thin Film Transistors
09450522	6232157	1999-11-29	2001-05-15	Granted	United States of America	Thin Film Transistors
09280103	6252245	1999-03-29	2001-06-26	Granted	United States of America	Device Comprising N-Channel Semiconductor Material
09476511	6387727	2000-01-03	2002-05-14	Granted	United States of America	Device Comprising N-Channel Semiconductor Material
09276912	6187427	1999-03-27	2001-02-13	Expired	United States of America	Hybrid Inorganic\(miOrganic Composite For Use As An Interlayer Dielectric
08911489	5965202	1997-08-14	1999-10-12	Expired	United States of America	Hybrid Inorganic\(miOrganic Composite For Use As An Interlayer Dielectric
09339895	6320238	1999-06-25	2001-11-20	Granted	United States of America	A Gate Stack Structure For Integrated Circuit Fabrication
08995435	6548854	1997-12-22	2003-04-15	Granted	United States of America	Compound, High-K, Gate And Capacitor Insulator Layer
08872250	6118351	1997-06-10	2000-09-12	Expired	United States of America	A Micromagnetic Device For Power Processing Applications And Method Of Manufacture Therefor
09292860	6191495	1999-04-16	2001-02-20	Expired	United States of America	Micromagnetic Device Having An Anisotropic Ferromagnetic Core and Method of Manufacture Therefor
09511343	6440750	2000-02-23	2002-08-27	Expired	United States of America	Method Of Making Integrated Circuit Having A Micromagnetic Device
10387846	7021518	2003-03-13	2006-04-04	Lapsed	United States of America	Micromagnetic Device For Power Processing Applications And Method Of Manufacture Therefor
09978871	6696744	2001-10-15	2004-02-24	Expired	United States of America	Integrated Circuit Having A Micromagnetic Device And Method Of Manufacture Therefor
09109963	6163234	1998-07-02	2000-12-19	Expired	United States of America	A Micromagnetic Device For Data Transmission Applications And Method Of Manufacture Therefor
09490655	6160721	2000-01-24	2000-12-12	Expired	United States of America	A Micromagnetic Device For Power Processing Applications And Method Of Manufacture Therefor
08718113	5804975	1996-09-18	1998-09-08	Expired	United States of America	Detecting Breakdown In Dielectric Layers
09002497	6043662	1998-01-02	2000-03-28	Expired	United States of America	Detecting Defects In Integrated Circuits
12502057	8097179	2009-07-13	2012-01-17	Granted	United States of America	Arrangement And Method For Abating Effluent From A Process
09942330	7578883	2001-08-29	2009-08-25	Lapsed	United States of America	Arrangement And Method For Abating Effluent From A Process
08353015	5576240	1994-12-09	1996-11-19	Expired	United States of America	Method for Making A Metal to metal Capacitor
08644086	5851870	1996-05-09	1998-12-22	Expired	United States of America	Method For Making A Capacitor

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08472033	5654581	1995-06-06	1997-08-05	Expired	United States of America	Integrated Circuit Capacitor
08909563	6040616	1997-08-12	2000-03-21	Expired	United States of America	A Device and Method of Forming A Metal To Metal Capacitor Within an Integrated Circuit
08863713	5825073	1997-05-27	1998-10-20	Expired	United States of America	An Electronic Component For An Integrated Circuit
09081403	6239491	1998-05-18	2001-05-29	Granted	United States of America	Integrated circuit structure with thin dielectric between at least local interconnect level and first metal interconnect level, and process for making same
09790821	6486056	2001-02-22	2002-11-26	Granted	United States of America	Process for making integrated circuit structure with thin dielectric between at least local interconnect level and first metal interconnect level
09741568	6576404	2000-12-19	2003-06-10	Granted	United States of America	Carbon-doped hard mask and method of passivating structures during semiconductor device fabrication
10405666	6846569	2003-04-02	2005-01-25	Granted	United States of America	Carbon-doped hard mask and method of passivating structures during semiconductor device fabrication
09607169	6541383	2000-06-29	2003-04-01	Granted	United States of America	Apparatus and method for planarizing the surface of a semiconductor wafer
10336444		2003-01-03		Abandoned	United States of America	Apparatus and Method for Planarizing the Surface of a Semiconductor Wafer
09098635	6060370	1998-06-16	2000-05-09	Granted	United States of America	Method for shallow trench isolations with chemical-mechanical polishing
09507042	6424019	2000-02-18	2002-07-23	Granted	United States of America	Shallow trench isolation chemical-mechanical polishing process
09442078	6179956	1999-11-16	2001-01-30	Granted	United States of America	Method and apparatus for using across wafer back pressure differentials to influence the performance of chemical mechanical polishing
09005364	6531397	1998-01-09	2003-03-11	Granted	United States of America	Method and apparatus for using across wafer back pressure differentials to influence the performance of chemical mechanical polishing
08976033	5994211	1997-11-21	1999-11-30	Granted	United States of America	Method and composition for reducing gate oxide damage during RF sputter clean
09251702	6204550	1999-02-17	2001-03-20	Granted	United States of America	Method and composition for reducing gate oxide damage during RF sputter clean
10640778	6943042	2003-08-13	2005-09-13	Lapsed	United States of America	Method of detecting spatially correlated variations in a parameter of an integrated circuit die
10020407	6787379	2001-12-12	2004-09-07	Granted	United States of America	Method of detecting spatially correlated variations in a parameter of an integrated circuit die
08924903	5981352	1997-09-08	1999-11-09	Expired	United States of America	Consistent alignment mark profiles on semiconductor wafers using fine grain tungsten protective layer

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09361684	6060787	1999-07-27	2000-05-09	Expired	United States of America	Consistent alignment mark profiles on semiconductor wafers using fine grain tungsten protective layer
08925200	5966613	1997-09-08	1999-10-12	Expired	United States of America	Consistent alignment mark profiles on semiconductor wafers using metal organic chemical vapor deposition titanium nitride protective
09289828	6157087	1999-04-12	2000-12-05	Expired	United States of America	Consistent alignment mark profiles on semiconductor wafers using metal organic chemical vapor deposition titanium nitride protective layer
10306011	6891219	2002-11-26	2005-05-10	Granted	United States of America	Metal-insulator-metal capacitor formed by damascene processes between metal interconnect layers and method of forming same
09723434	6524926	2000-11-27	2003-02-25	Granted	United States of America	Metal-insulator-metal capacitor formed by damascene processes between metal interconnect layers and method of forming same
08861899		1997-05-22		Abandoned	United States of America	Integrated Circuit With Isolation Of Field Oxidation By Noble Gas Implantation And Method Of Making Such An Integrated Circuit
08479104		1995-06-07		Abandoned	United States of America	Integrated Circuit With Isolation Of Field Oxidation By Nobel Gas Implantation And Method Of Making Such An Integrated Circuit
08641027		1996-04-29		Abandoned	United States of America	Integrated Circuit With Isolation Of Field Oxidation By Noble Gas Implantation And Method Of Making Such An Integrated Circuit.
08918577	6093936	1997-08-19	2000-07-25	Expired	United States of America	Integrated circuit with isolation of field oxidation by noble gas implantation
08701476	5905381	1996-08-22	1999-05-18	Expired	United States of America	Functional OBIC analysis
09244327	6154039	1999-02-03	2000-11-28	Expired	United States of America	Functional OBIC analysis
09526101	6383414	2000-03-15	2002-05-07	Expired	United States of America	Use of corrosion inhibiting compounds to inhibit corrosion of metal plugs in chemical-mechanical polishing
08918360	6068879	1997-08-26	2000-05-30	Expired	United States of America	Use of corrosion inhibiting compounds to inhibit corrosion of metal plugs in chemical-mechanical polishing
08889839	5895267	1997-07-09	1999-04-20	Expired	United States of America	Method to obtain a low resistivity and conformity chemical vapor deposition titanium film
09218780	6297555	1998-12-22	2001-10-02	Expired	United States of America	Method to obtain a low resistivity and conformity chemical vapor deposition titanium film
09388727	6359314	1999-09-02	2002-03-19	Granted	United States of America	Swapped drain structures for electrostatic discharge protection
10026186	6587322	2001-12-20	2003-07-01	Granted	United States of America	Swapped drain structures for electrostatic discharge protection
09177335	6201253	1998-10-22	2001-03-13	Granted	United States of America	Method and apparatus for detecting a planarized outer layer of a semiconductor wafer with a confocal optical system
09754429	6354908	2001-01-04	2002-03-12	Granted	United States of America	Method and apparatus for detecting a planarized outer layer of a semiconductor wafer with a confocal optical system
09863979		2001-05-23		Abandoned	United States of America	Method and Apparatus for Deposition of Porous Silica Dielectrics
09302832	6287987	1999-04-30	2001-09-11	Granted	United States of America	Method and apparatus for deposition of porous silica dielectrics

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10459072	6806162	2003-06-11	2004-10-19	Lapsed	United States of America	Method for composing a dielectric layer within an interconnect structure of a multilayer semiconductor device
09164069	6614097	1998-09-30	2003-09-02	Lapsed	United States of America	Method for composing a dielectric layer within an interconnect structure of a multilayer semiconductor device
09162407	6211555	1998-09-29	2001-04-03	Granted	United States of America	Semiconductor device with a pair of transistors having dual work function gate electrodes
09591108	6514824	2000-06-09	2003-02-04	Granted	United States of America	Semiconductor device with a pair of transistors having dual work function gate electrodes
08954006	6096625	1997-10-20	2000-08-01	Expired	United States of America	Method for improved gate oxide integrity on bulk silicon
08720514		1996-09-30		Abandoned	United States of America	Method for Improved Gate Oxide Integrity on Bulk Silicon
61350494		2010-06-02		Expired	United States of America	CUB eDRAM cell with local Interconnects to reduce stacked contact parasitics Impact
13046973	8283713	2011-03-14	2012-10-09	Granted	United States of America	Logic-Based eDRAM Using Local Interconnects to Reduce Impact of Extension Contact Parasitics
11230188		2005-09-19		Abandoned	United States of America	Shallow Trench Isolation Structures And A Method For Forming Shallow Trench Isolation Structures
11926469	7906407	2007-10-29	2011-03-15	Granted	United States of America	Shallow Trench Isolation Structures And A Method For Forming Shallow Trench Isolation Structures
08430084	5891784	1995-04-27	1999-04-06	Expired	United States of America	Transistor Fabrication Method
08587061	6498080	1996-01-16	2002-12-24	Expired	United States of America	Transistor Fabrication Method
12114589		2008-05-02		Abandoned	United States of America	Transistor Fabrication Method
10224220		2002-08-20		Abandoned	United States of America	Transistor Fabrication Method
12689749	8030199	2010-01-19	2011-10-04	Granted	United States of America	Transistor Fabrication Method
2000079900	3432783	2000-03-22	2003-05-23	Lapsed	Japan	Low Dielectric Constant Multiple Carbon-Containing Silicon Oxide Dielectric Material For Use In Integrated Circuit Structures, And Method Of Making Same
09281602	6204192	1999-03-29	2001-03-20	Granted	United States of America	Plasma cleaning process for openings formed in at least one low dielectric constant insulation layer over copper metallization in integrated circuit structures
2001554123	4831802	2002-07-19	2011-09-30	Lapsed	Japan	Mask Having An Arbitrary Complex Transmission Function
09274457	6303047	1999-03-22	2001-10-16	Granted	United States of America	Low dielectric constant multiple carbon-containing silicon oxide dielectric material for use in integrated circuit structures, and method of making same
09362645	6114259	1999-07-27	2000-09-05	Granted	United States of America	Process for treating exposed surfaces of a low dielectric constant carbon doped silicon oxide dielectric material to protect the material from damage
09233828	6197456	1999-01-19	2001-03-06	Granted	United States of America	Mask having an arbitrary complex transmission function
09207395	6144076	1998-12-08	2000-11-07	Granted	United States of America	Well formation For CMOS devices integrated circuit structures

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
1019980025571	537034	1998-06-30	2005-12-09	Lapsed	Korea, Republic of (KR)	Process For Forming MOS Device In Integrated Circuit Structure Using Cobalt Silicide Contacts As Implantation Media
1998068296	4932980	1998-03-18	2012-02-24	Lapsed	Japan	Semiconductor Die Having On-Die Decoupling Capacitance
09121283	6156620	1998-07-22	2000-12-05	Granted	United States of America	Isolation trench in semiconductor substrate with nitrogen-containing barrier region, and process for forming same
09097081	6185706	1998-06-12	2001-02-06	Granted	United States of America	Performance monitoring circuitry for integrated circuits
09321659	6299723	1999-05-28	2001-10-09	Granted	United States of America	Anti-airlock apparatus for filters
09321658	6276379	1999-05-28	2001-08-21	Granted	United States of America	Anti-microbubble deposition apparatus
09266174	6258514	1999-03-10	2001-07-10	Granted	United States of America	Top surface imaging technique using a topcoat delivery system
09340704	4054424	1997-11-26	2007-12-14	Lapsed	Japan	Method And Apparatus Of Fourier Manipulation In An Optic Lens Or Mirror Train
09045738	6130173	1998-03-19	2000-10-10	Granted	United States of America	Reticle based skew lots
1997355616	4620189	1997-12-24	2010-11-05	Granted	Japan	A Novel Method To Improve Uniformity/Planarity On The Edge Die And Also Remove The Tungsten Stringers From Wafer Chemi-Mechanical Polishing
08978979	6043539	1997-11-26	2000-03-28	Granted	United States of America	Electro-static discharge protection of CMOS integrated circuits
09038684	6033998	1998-03-09	2000-03-07	Granted	United States of America	Method of forming variable thickness gate dielectrics
08995875	6218276	1997-12-22	2001-04-17	Granted	United States of America	Silicide encapsulation of polysilicon gate and interconnect
08947742	5953614	1997-10-09	1999-09-14	Expired	United States of America	Process for forming self-aligned metal silicide contacts for MOS structure using single silicide-forming step
08944247	6054062	1997-10-06	2000-04-25	Expired	United States of America	Method and apparatus for agitating an etchant
08899464	6692338	1997-07-23	2004-02-17	Expired	United States of America	Through-pad drainage of slurry during chemical mechanical polishing
08935584	5888121	1997-09-23	1999-03-30	Expired	United States of America	Controlling groove dimensions for enhanced slurry flow
08912597	6093280	1997-08-18	2000-07-25	Expired	United States of America	Chemical-mechanical polishing pad conditioning systems
08924493	5913715	1997-08-27	1999-06-22	Expired	United States of America	Use of hydrofluoric acid for effective pad conditioning
08942006	6234883	1997-10-01	2001-05-22	Expired	United States of America	Method and apparatus for concurrent pad conditioning and wafer buff in chemical mechanical polishing
08921758	5941761	1997-08-25	1999-08-24	Expired	United States of America	Shaping polishing pad to control material removal rate selectively
08837618	5923047	1997-04-21	1999-07-13	Expired	United States of America	Semiconductor die having sacrificial bond pads for die test
08902343	6064220	1997-07-29	2000-05-16	Expired	United States of America	Semiconductor integrated circuit failure analysis using magnetic imaging
08899629	5990789	1997-07-24	1999-11-23	Expired	United States of America	System and method for preventing smoke and fire damage to people and equipment in a clean room area from a fire
08771472	5960305	1996-12-23	1999-09-28	Expired	United States of America	Method to improve uniformity/planarity on the edge die and also remove the tungsten stringers from wafer chemi-mechanical polishing
08940156	5863825	1997-09-29	1999-01-26	Expired	United States of America	Alignment mark contrast enhancement

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08890222	5874342	1997-07-09	1999-02-23	Expired	United States of America	Process for forming MOS device in integrated circuit structure using cobalt silicide contacts as implantation media
08768428	5963566	1996-12-18	1999-10-05	Expired	United States of America	Application specific integrated circuit chip and method of testing same
08727257	5771267	1996-10-08	1998-06-23	Expired	United States of America	Burn-in activity monitor
08840948	6198153	1997-04-21	2001-03-06	Expired	United States of America	Capacitors with silicized polysilicon shielding in digital CMOS process
08710783	5702957	1996-09-20	1997-12-30	Expired	United States of America	Method of making buried metallization structure
08770109	5963801	1996-12-19	1999-10-05	Expired	United States of America	Method of forming retrograde well structures and punch-through barriers using low energy implants
08652999	5646406	1996-05-24	1997-07-08	Expired	United States of America	Stroboscopic photometer
08932614	5994775	1997-09-17	1999-11-30	Expired	United States of America	Metal-filled via/contact opening with thin barrier layers in integrated circuit structure for fast response, and process for making same
08531727	5759921	1995-09-21	1998-06-02	Expired	United States of America	Integrated circuit device fabrication by plasma etching
09873043	6562700	2001-05-31	2003-05-13	Granted	United States of America	Process for removal of resist mask over low k carbon-doped silicon oxide dielectric material of an integrated circuit structure, and removal of residues from via etch and resist mask removal
08655249	5703376	1996-06-05	1997-12-30	Expired	United States of America	Multi-level resolution lithography
08517479	5834821	1995-08-21	1998-11-10	Expired	United States of America	Triangular semiconductor "AND" gate device
08756662	5959776	1996-11-26	1999-09-28	Expired	United States of America	Method and apparatus of Fourier manipulation in an optic lens or mirror train
08630267	5877045	1996-04-10	1999-03-02	Expired	United States of America	Method of forming a planar surface during multi-layer interconnect formation by a laser-assisted dielectric deposition
08501289	5670393	1995-07-12	1997-09-23	Expired	United States of America	Method of making combined metal oxide semiconductor and junction field effect transistor device
09865900	6506670	2001-05-25	2003-01-14	Granted	United States of America	Self aligned gate
08557721	5744399	1995-11-13	1998-04-28	Expired	United States of America	Process for forming low dielectric constant layers using fullerenes
08192228	5681779	1994-02-04	1997-10-28	Expired	United States of America	Method of doping metal layers for electromigration resistance
2012269037	5650185	1999-03-12	2014-11-21	Granted	Japan	Electronic Components With Doped Metal Oxide Dielectric Materials And A Process For Making Electronic Components With Doped Metal Oxide Dielectric Materials
201398165		2013-05-08		Abandoned	Japan	Method To Improve Metal Defects In Semiconductor Device Fabrication
2000245497		2000-08-14		Abandoned	Japan	A Process For Manufacturing An Integrated Circuit Including A Dual-Damascene Structure And An Integrated Circuit
09792685	6858195	2001-02-23	2005-02-22	Lapsed	United States of America	Process for forming a low dielectric constant fluorine and carbon-containing silicon oxide dielectric material

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09703745	6417093	2000-10-31	2002-07-09	Granted	United States of America	Process for planarization of metal-filled trenches of integrated circuit structures by forming a layer of planarizable material over the metal layer prior to planarizing
11323398	7436040	2005-12-29	2008-10-14	Granted	United States of America	Method and apparatus for diverting void diffusion in integrated circuit conductors
11265040	7571397	2005-11-02	2009-08-04	Lapsed	United States of America	Method of Design Based Process Control Optimization
11078179	7641776	2005-03-10	2010-01-05	Granted	United States of America	System and Method for Increasing Yield from Semiconductor Wafer Electroplating
10327283	6867127	2002-12-19	2005-03-15	Granted	United States of America	Diamond metal-filled patterns achieving low parasitic coupling capacitance
10925497	7312880	2004-08-24	2007-12-25	Granted	United States of America	Wafer edge structure measurement method
10226884	7148131	2002-08-23	2006-12-12	Granted	United States of America	Method for implanting ions in a semiconductor
10879629	7198546	2004-06-29	2007-04-03	Granted	United States of America	Method to monitor pad wear in CMP processing
10867003	7039556	2004-06-14	2006-05-02	Lapsed	United States of America	Substrate profile analysis
60140909		1999-06-24		Expired	United States of America	High Quality Oxide For Use In Integrated Circuits
60115762		1999-01-13		Expired	United States of America	Method Of Making A Capacitor
60115842		1999-01-13		Expired	United States of America	Aluminum Barrier Layer For High-IC Dielectric In Capacitors/Gate Application
60052440		1997-07-14		Expired	United States of America	Process For Device Fabrication
60115520		1999-01-12		Expired	United States of America	Damascene Capacitors For Integrated Circuits
60083547		1998-04-29		Expired	United States of America	Process For Fabricating A Lithographic Mask
60077720		1998-03-12		Expired	United States of America	Article Comprising Fluorinated Diamond-Like Carbon And Method For Fabricating Article
60115604		1999-01-12		Expired	United States of America	Integration Of Low Dielectric Material In Semiconductor Circuit Structures
60163230		1999-11-03		Expired	United States of America	Phase Shift Gate Lithography For High-Speed Low Voltage DSPs
09712732	6588437	2000-11-14	2003-07-08	Lapsed	United States of America	System And Method For Removal Of Material
09597077	6492712	2000-06-20	2002-12-10	Granted	United States of America	High Quality Oxide For Use In Integrated Circuits
09298792	6280644	1999-04-23	2001-08-28	Granted	United States of America	Method Of Planarizing A Surface Of An Integrated Circuit
10930544	7230812	2004-08-30	2007-06-12	Granted	United States of America	Predictive Applications For Devices With Thin Dielectric Regions
10219951	6893806	2002-08-15	2005-05-17	Lapsed	United States of America	Multiple Purpose Reticle Layout For Selectively Printing Of Test Circuits
09364767	6291848	1999-07-30	2001-09-18	Granted	United States of America	Integrated Circuit Capacitor Including Anchored Plugs
09250501	6358790	1999-02-16	2002-03-19	Granted	United States of America	Method Of Making A Capacitor
09464811	6657302	1999-12-17	2003-12-02	Granted	United States of America	Integration Of Low K Dielectric Material In Semiconductor Circuit Structures
09385258	6146913	1999-08-30	2000-11-14	Granted	United States of America	Method For Making Enhanced Performance Field Effect Devices

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09432725	6395611	1999-11-01	2002-05-28	Granted	United States of America	An Inductor Or Low Loss Interconnect And A Method Of Manufacturing An Inductor Or Low Loss Interconnect In An Integrated Circuit
09863979		2001-05-23		Abandoned	United States of America	Method and Apparatus for Deposition of Porous Silica Dielectrics
10680047	6797585	2003-10-07	2004-09-28	Granted	United States of America	Nonintrusive wafer marking
09596382	6762087	2000-06-16	2004-07-13	Granted	United States of America	Process For Manufacturing An Integrated Circuit Including A Dual-Damascene Structure And A Capacitor
09603717	6621280	2000-06-27	2003-09-16	Granted	United States of America	A Method of Testing an Integrated Circuit
09754611	6731386	2001-01-04	2004-05-04	Lapsed	United States of America	Measurement Technique For Ultra-Thin Oxides
09405641	6286226	1999-09-24	2001-09-11	Granted	United States of America	Tactile Sensor Comprising Nanowires And Method For Making The Same
09473876	6287952	1999-12-28	2001-09-11	Granted	United States of America	Method Of Etching Self-Aligned Vias To Metal Using A Silicon Nitride Spacer
09364025	6103586	1999-07-30	2000-08-15	Granted	United States of America	Method For Making Integrated Circuit Capacitor Including Anchored Plugs
09259028	6566181	1999-02-26	2003-05-20	Granted	United States of America	Process For The Fabrication Of Dual Gate Structures For CMOS Devices
10634416	7181353	2003-08-04	2007-02-20	Granted	United States of America	Method and apparatus for integrating Six Sigma methodology into inspection receiving process of outsourced subassemblies, parts, and materials: acceptance, rejection, trending, tracking and closed loop corrective action
09323607	6346222	1999-06-01	2002-02-12	Granted	United States of America	Process For Synthesizing A Palladium Replenisher For Electroplating Baths
09293103	6218057	1999-04-16	2001-04-17	Granted	United States of America	A Lithographic Process Having Sub-Wavelength Resolution
08918394	5846871	1997-08-26	1998-12-08	Expired	United States of America	Integrated Circuit Fabrication
09057420	5985493	1998-04-08	1999-11-16	Granted	United States of America	Membrane Mask For Projection Lithography
08977319	5981403	1997-11-24	1999-11-09	Granted	United States of America	Layered Silicon Nitride Deposition Process
09140276	6365469	1998-08-26	2002-04-02	Granted	United States of America	A Method For Forming Dual-Polysilicon Structures Using A Built-In Stop Layer
09092158	6982226	1998-06-05	2006-01-03	Lapsed	United States of America	Method For The Fabrication Of Contacts In An Integrated Circuit Device
09127373	6087683	1998-07-31	2000-07-11	Granted	United States of America	Silicon Germanium Heterostructure Bipolar Transistor With Indium Doped Base
08770535	6107117	1996-12-20	2000-08-22	Expired	United States of America	Method Of Making An Organic Thin Film Transistor
09023220	6136673	1998-02-12	2000-10-24	Granted	United States of America	A Process For Fabricating A Device With Shallow Junctions
08972904	5969421	1997-11-18	1999-10-19	Granted	United States of America	Integrated Circuit Conductors That Avoid Current Crowding
08554501	5885900	1995-11-07	1999-03-23	Expired	United States of America	Method Of Global Planarization In Fabricating Integrated Circuit Devices

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08280429	5529051	1994-07-26	1996-06-25	Expired	United States of America	Method of Preparing Silicon Wafers
08321362	5500312	1994-10-11	1996-03-19	Expired	United States of America	Masks With Low Stress Multilayer Films And A Process For Controlling The Stress Of Multilayer Films
08546078	5663568	1995-10-20	1997-09-02	Expired	United States of America	Apparatus For Controlling A Charged Particle Beam And A Lithographic Process In Which The Apparatus Is Used
08923316	6110831	1997-09-04	2000-08-29	Expired	United States of America	Method Of Mechanical Polishing
08660632	5736281	1996-06-07	1998-04-07	Expired	United States of America	Dose Modification Proximity Effect Compensation (PEC) Technique For Electron Beam Lithography
08388934	5607800	1995-02-15	1997-03-04	Expired	United States of America	Method and Arrangement for Characterizing Micro-Size Patterns
09491644	6472307	2000-01-27	2002-10-29	Granted	United States of America	Method For Improved Encapsulation Of Thick Metal Features In Integrated Circuit Fabrication
10602357	6954705	2003-06-23	2005-10-11	Lapsed	United States of America	Method of screening defects using low voltage IDDQ measurement
90121234	NI-166024	2001-08-28	2003-03-14	Granted	Taiwan	Methods of Fabricating A Metal-Oxide-Metal Capacitor And Associated Apparatus
90114970	NI-182552	2001-06-20	2003-08-01	Lapsed	Taiwan	A Method of Testing an Integrated Circuit
90106474	NI-161626	2001-03-20	2002-12-11	Lapsed	Taiwan	Vertical Replacement Gate (VRG) MOSFET With A Conductive Layer Adjacent A Source/Drain Region And Method Of Manufacture Therefor
88105178	NI-181704	1999-04-01	2003-07-21	Granted	Taiwan	Device And Method For Polishing A Semiconductor Substrate
89101735	NI-162628	2000-02-01	2002-09-11	Lapsed	Taiwan	A Method For Fabricating A Merged Integrated Circuit Device
86118596	NI-116286	1997-12-10	2000-06-21	Lapsed	Taiwan	Method Of Making An Organic Thin Film Transistor
093110399	I332677	2004-04-14	2010-11-01	Granted	Taiwan	Method And Apparatus For Manufacturing Multiple Circuit Patterns Using A Multiple Project Mask
097118239	I376768	2008-05-16	2012-11-11	Granted	Taiwan	Method For Separating A Semiconductor Wafer Into Individual Semiconductor Dies Using An Implanted Inpurity
093108543	I344685	2004-03-29	2011-07-01	Granted	Taiwan	An integrated circuit device and a process for forming the same
1020000071927	704132	2000-11-30	2007-03-30	Lapsed	Korea, Republic of (KR)	Semiconductor Device Having Self-Aligned Contact And Landing PAD Structure And Method Of Forming Same
1020010042929	829404	2001-07-16	2008-05-07	Lapsed	Korea, Republic of (KR)	Electrostatic Discharge Protection Device With Monolithically Formed Resistor-Capacitor Portion
1020010053297	773256	2001-08-31	2007-10-30	Lapsed	Korea, Republic of (KR)	Stacked Structure For Parallel Capacitors And Method Of Fabrication
1020010006759	859674	2001-02-12	2008-09-17	Lapsed	Korea, Republic of (KR)	Method For Producing Devices Having Piezoelectric Films
20010006412	10-0860182	2001-02-09	2008-09-18	Lapsed	Korea, Republic of (KR)	Method For Producing Piezoelectric Films With Rotating Magnetron Sputtering System
1019990035816	572647	1999-08-27	2006-04-13	Lapsed	Korea, Republic of (KR)	Process For Fabricating Vertical Transistors
20000017524	708585	2000-04-04	2007-04-11	Lapsed	Korea, Republic of (KR)	Method For Processing Silicon Workpieces Using Hybrid Optical Thermometer System

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
1020000050713	614782	2000-08-30	2006-08-16	Lapsed	Korea, Republic of (KR)	A Process For Manufacturing An Integrated Circuit Including A Dual-Damascene Structure And An Integrated Circuit
9847146	320163	1998-11-04	2001-12-26	Lapsed	Korea, Republic of (KR)	Method For Using A Hardmask To Form An Opening In A Semiconductor Substrate
9853846	294359	1998-12-09	2001-04-16	Lapsed	Korea, Republic of (KR)	Lithographic Process For Device Fabrication Using A Multilayer Mask Which Has Been Previously Inspected
1019990020699	373193	1999-06-04	2003-02-10	Lapsed	Korea, Republic of (KR)	Method For The Fabrication Of Contacts In An Integrated Circuit Device
9843136	329139	1998-10-15	2002-03-06	Lapsed	Korea, Republic of (KR)	Thin Film Transistor And Organic Semiconductor Material Therefor
9712486	469221	1997-04-04	2005-01-21	Lapsed	Korea, Republic of (KR)	Process For Device Fabrication In Which A Thin Layer Of Cobalt Silicide Is Formed
1020010043828	803643	2001-07-20	2008-02-05	Lapsed	Korea, Republic of (KR)	A Method Of Manufacturing An Integrated Circuit Package
1020000058829	757215	2000-10-06	2007-09-04	Lapsed	Korea, Republic of (KR)	Lens Array For Electron Beam Lithography Tool
1020020084019	10-905210	2002-12-26	2009-06-23	Lapsed	Korea, Republic of (KR)	CMOS Vertical Replacement Gate (VRG) Transistors
963093182	69624326.1	1996-12-19	2002-10-16	Expired	Germany (Federal Republic of)	Polishing Composition for CMP Operations
1020010036899	10-983457	2001-06-27	2010-09-15	Lapsed	Korea, Republic of (KR)	A Method of Testing an Integrated Circuit
11065740	3328600	1999-03-12	2002-07-12	Lapsed	Japan	Process For Fabricating Bipolar And BICMOS Devices
11065741	3378210	1999-03-12	2002-12-06	Granted	Japan	Article Comprising Fluorinated Diamond-Like Carbon And Method For Fabricating Article
11083888	3538335	1999-03-26	2004-03-26	Lapsed	Japan	Mold For Non-Photolithographic Fabrication Of Microstructures
10043609	3768671	1998-02-25	2006-02-10	Lapsed	Japan	Thin Film Tantalum Oxide Capacitors And Resulting Product
09020253	3677137	1997-02-03	2005-05-13	Expired	Japan	Articles Comprising Magnetically Soft Thin Films And Methods For Making Such Articles
2000056110	3753915	2000-03-01	2005-12-22	Granted	Japan	Fabricating High-Q RF Component
2001262994	5090598	2001-08-31	2012-09-21	Granted	Japan	Methods of Fabricating A Metal-Oxide-Metal Capacitor And Associated Apparatus
2001009397	4718021	2001-01-17	2011-04-08	Lapsed	Japan	Method For Making A Semiconductor Device
10315480	6969621	2002-12-09	2005-11-29	Lapsed	United States of America	Contamination distribution apparatus and method
09577912	6506684	2000-05-24	2003-01-14	Granted	United States of America	Anti-corrosion system
10236226	7016041	2002-09-06	2006-03-21	Lapsed	United States of America	Reticle overlay correction
003055712	60042804.4	2000-07-03	2009-08-26	Granted	Germany (Federal Republic of)	Article Comprising A Variable Inductor
003098035	60043148.7	2000-11-06	2009-10-14	Granted	Germany (Federal Republic of)	Process for Forming Device Comprising Micromagnetic Components for Power Applications
993024413	69944291.5	1999-03-29	2012-07-04	Lapsed	Germany (Federal Republic of)	Membrane Mask for Projection Lithography

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
003103058	60039956.7	2000-11-20	2008-08-20	Granted	Germany (Federal Republic of)	Thin Film Transistors
993064468	69909205.1	1999-08-17	2003-07-02	Lapsed	Germany (Federal Republic of)	Process For Fabricating Vertical Transistors
983011545	69800026.9	1998-02-17	1999-10-13	Lapsed	Germany (Federal Republic of)	GaAs-Based MOSFET, And Method Of Making Same
983018037	69832226.6	1998-03-11	2005-11-09	Lapsed	Germany (Federal Republic of)	Semiconductor Device Having Aluminum Contacts Or Vias And Method Of Manufacture Therefor
983005505	69802659.4	1998-01-27	2001-11-28	Granted	Germany (Federal Republic of)	Electronic Apparatus
09669979	6319836	2000-09-26	2001-11-20	Granted	United States of America	Planarization system
973081268	69734047.3	1997-10-14	2005-08-24	Expired	Germany (Federal Republic of)	Article Comprising A Relatively Temperature-Insensitive Ta-Oxide Based Capacitive Element
013007489	60144587.2	2001-01-29	2011-05-11	Granted	Germany (Federal Republic of)	Method For Producing Piezoelectric Films With Rotating Magnetron Sputtering System
09981154	6586332	2001-10-16	2003-07-01	Lapsed	United States of America	Deep submicron silicide blocking
09966651	6736953	2001-09-28	2004-05-18	Granted	United States of America	High frequency electrochemical deposition
09960441	6770505	2001-09-21	2004-08-03	Granted	United States of America	Arrangement for measuring pressure on a semiconductor wafer and an associated method for fabricating a semiconductor wafer
09997071	6767692	2001-11-28	2004-07-27	Granted	United States of America	Process for inhibiting edge peeling of coating on semiconductor substrate during formation of integrated circuit structure thereon
09953706	6524957	2001-09-17	2003-02-25	Lapsed	United States of America	An In\(miSitu Electroplated Oxide Passivating Film For Corrosion Inhibition
10144511	6930006	2002-05-13	2005-08-16	Lapsed	United States of America	Electronic Circuit Structure With Improved Dielectric Properties
2007237928		2007-09-13		Abandoned	Japan	Method For Making A Semiconductor Device
200810210288X	ZL200810210288.X	2004-08-04	2010-07-21	Lapsed	China	A Spiral Inductor Formed In A Semiconductor Substrate And A Method For Forming The Inductor
08865548	5851922	1997-05-29	1998-12-22	Expired	United States of America	Process For Fabricating A Device Using Nitrogen Implantation Into Silicide Layer
11519614	7547560	2006-09-12	2009-06-16	Lapsed	United States of America	Defect Identification System And Method For Repairing Killer Defects In Semiconductor Devices
11673714	7804291	2007-02-12	2010-09-28	Lapsed	United States of America	Semiconductor Test Device With Heating Circuit
09590310	6365528	2000-06-07	2002-04-02	Granted	United States of America	Low temperature process for forming a low dielectric constant fluorine and carbon-containing silicon oxide dielectric-material characterized by improved resistance to oxidation and good gap-filling capabilities
10005097	6624048	2001-12-05	2003-09-23	Lapsed	United States of America	Die attach back grinding

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08869278	6108093	1997-06-04	2000-08-22	Expired	United States of America	Automated inspection system for residual metal after chemical-mechanical polishing
08918293	6168508	1997-08-25	2001-01-02	Expired	United States of America	Polishing pad surface for improved process control
09580106	6355577	2000-05-30	2002-03-12	Granted	United States of America	System to reduce particulate contamination
09471842	6274395	1999-12-23	2001-08-14	Granted	United States of America	Method and apparatus for maintaining test data during fabrication of a semiconductor wafer
09434340	6090651	1999-11-05	2000-07-18	Granted	United States of America	Depletion free polysilicon gate electrodes
09204815	6115232	1998-12-03	2000-09-05	Granted	United States of America	Method for forming an ion implanted electrostatic chuck
09213803	6316276	1998-12-17	2001-11-13	Granted	United States of America	Apparatus and method of planarizing a semiconductor wafer that includes a first reflective substance and a second reflective substance
87102155	109370	1998-02-17	1999-11-11	Granted	Taiwan	Use of MEV Implantation to Form a Vertically Modulated n+ Buried Layer in an NPN Bipolar Transistor
09163623	6069048	1998-09-30	2000-05-30	Granted	United States of America	Reduction of silicon defect induced failures as a result of implants in CMOS and other integrated circuits
08496861	5654537	1995-06-30	1997-08-05	Expired	United States of America	Image sensor array with picture element sensor testability
09281514	6028015	1999-03-29	2000-02-22	Granted	United States of America	Process for treating damaged surfaces of low dielectric constant organo silicon oxide insulation material to inhibit moisture absorption
09322191	6032529	1999-05-28	2000-03-07	Granted	United States of America	Liquid level sensor for buffered hydrofluoric acid
09013510	6124143	1998-01-26	2000-09-26	Granted	United States of America	Process monitor circuitry for integrated circuits
08986537	6097884	1997-12-08	2000-08-01	Granted	United States of America	Probe points and markers for critical paths and integrated circuits
08972231	5978197	1997-11-18	1999-11-02	Granted	United States of America	Testing ESD protection schemes in semiconductor integrated circuits
08960969	5957757	1997-10-30	1999-09-28	Expired	United States of America	Conditioning CMP polishing pad using a high pressure fluid
08900845	5998853	1997-07-25	1999-12-07	Expired	United States of America	Methods and apparatus for electrical marking of integrated circuits to record manufacturing test results
08895659	5816900	1997-07-17	1998-10-06	Expired	United States of America	Apparatus for polishing a substrate at radially varying polish rates
08961382	6074288	1997-10-30	2000-06-13	Expired	United States of America	Modified carrier films to produce more uniformly polished substrate surfaces
08615437	5660682	1996-03-14	1997-08-26	Expired	United States of America	Plasma clean with hydrogen gas
08659860	5736418	1996-06-07	1998-04-07	Expired	United States of America	Method for fabricating a field effect transistor using microtrenches to control hot electron effects
09186793	4041187	1997-07-11	2007-11-16	Expired	Japan	Rapid Thermal Processing Using A Narrowband Infrared Source And Feedback
08690577	6060375	1996-07-31	2000-05-09	Expired	United States of America	Process for forming re-entrant geometry for gate electrode of integrated circuit structure

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08545880	5670892	1995-10-20	1997-09-23	Expired	United States of America	Apparatus and method for measuring quiescent current utilizing timeset switching
08631360	5904551	1996-04-12	1999-05-18	Expired	United States of America	Process for low energy implantation of semiconductor substrate using channeling to form retrograde wells
08396542	5656850	1995-03-01	1997-08-12	Expired	United States of America	Microelectronic integrated circuit including hexagonal semiconductor "AND" gate
08484003	5682047	1995-06-07	1997-10-28	Expired	United States of America	Input-output (I/O) structure with capacitively triggered thyristor for electrostatic discharge (ESD) protection
09844352	6767832	2001-04-27	2004-07-27	Granted	United States of America	In situ liner barrier
003025905	60012807.5	2000-03-29	2004-08-11	Lapsed	Germany (Federal Republic of)	Plasma Cleaning Process for Openings Formed in One or More Low Dielectric Constant Insulation Layers Over Copper Metallization In Integrated Circuit Structures
08613161	5795682	1996-03-08	1998-08-18	Expired	United States of America	Guard rings to compensate for side lobe ringing in attenuated phase shift reticles
08531659	5662768	1995-09-21	1997-09-02	Expired	United States of America	High surface area trenches for an integrated ciruit device
08481799	5667433	1995-06-07	1997-09-16	Expired	United States of America	Keyed end effector for CMP pad conditioner
09872058	6583026	2001-05-31	2003-06-24	Granted	United States of America	Process for forming a low k carbon-doped silicon oxide dielectric material on an integrated circuit structure
201313971	5580439	2007-05-17	2014-07-18	Lapsed	Japan	Method For Separating A Semiconductor Wafer Into Individual Semiconductor Dies Using An Implanted Inpurity
09870851	6559048	2001-05-30	2003-05-06	Granted	United States of America	Method of making a sloped sidewall via for integrated circuit structure to suppress via poisoning
1020130112914	10-1351293	2013-09-23	2014-01-08	Granted	Korea, Republic of (KR)	Method To Improve Metal Defects In Semiconductor Device Fabrication
08626776	5789783	1996-04-02	1998-08-04	Expired	United States of America	Multilevel metallization structure for integrated circuit I/O lines for increased current capacity and ESD protection
08579383	5956613	1995-12-27	1999-09-21	Expired	United States of America	Method for improvement of TiN CVD film quality
20133034	5579280	2013-01-11	2014-07-18	Lapsed	Japan	CMOS Vertical Replacement Gate (VRG) Transistors
08632550	5890951	1996-04-15	1999-04-06	Expired	United States of America	Utility wafer for chemical-mechanical planarization
09888302	6747464	2001-06-21	2004-06-08	Granted	United States of America	Wafer holder for backside viewing, frontside probing on automated wafer probe stations
08578118	5776831	1995-12-27	1998-07-07	Expired	United States of America	Method of forming a high electromigration resistant metallization system
09605382	6346488	2000-06-27	2002-02-12	Granted	United States of America	Process to provide enhanced resistance to cracking and to further reduce the dielectric constant of a low dielectric constant dielectric film of an integrated circuit structure by implantation with hydrogen ions

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
001226844		2000-10-18		Lapsed	European Patent	Low K Dielectric Composite Layer for Integrated Circuit Structure Which Provides Void-Free Low K Dielectric Material Between Metal Lines While Mitigating Via Poisoning
94124738	I364081	2005-07-21	2012-05-11	Granted	Taiwan	Failure Analysis Vehicle for Yield Enhancement with Self Test at Speed Burnin Capability for Reliability Testing
09725631	6556021	2000-11-29	2003-04-29	Granted	United States of America	Device frequency measurement system
003000437		2000-01-06		Application	European Patent	Damascene Capacitors For Integrated Circuits
09212450	6329720	1998-12-16	2001-12-11	Granted	United States of America	Tungsten local interconnect for silicon integrated circuit structures, and method of making same
2005100882101	ZL200510088210.1	2005-07-25	2010-06-23	Granted	China	Self-Timed Reliability and Yield Vehicle with Gated Data and Clock
094119790	I369504	2005-06-15	2012-08-01	Granted	Taiwan	Self-Timed Reliability and Yield Vehicle with Gated Data and Clock
102102447	I418017	2004-06-29	2013-12-01	Granted	Taiwan	A Spiral Inductor Formed In A Semiconductor Substrate And A Method For Forming The Inductor
11184621	7216279	2005-07-19	2007-05-08	Granted	United States of America	Testing with high speed pulse generator
2000319053	4731670	2000-10-19	2011-04-28	Lapsed	Japan	Low K Dielectric Composite Layer for Integrated Circuit Structure Which Provides Void-Free Low K Dielectric Material Between Metal Lines While Mitigating Via Poisoning
2011236296		2011-10-27		Abandoned	Japan	Aluminum Pad Power Bus And Signal Routing For Integrated Circuit Devices Utilizing Copper Technology Interconnect Structures
11071903	7094687	2005-03-02	2006-08-22	Granted	United States of America	Reduced dry etching lag
11046949	7553772	2005-01-31	2009-06-30	Lapsed	United States of America	Process And Apparatus For Simultaneous Light And Radical Surface Treatment Of Integrated Circuit Structure
10955168	7069178	2004-09-29	2006-06-27	Lapsed	United States of America	Method of predicting quiescent current variation of an integrated circuit die from a process monitor derating factor
11072158	7341978	2005-03-04	2008-03-11	Granted	United States of America	Superconductor wires for back end interconnects
11266133	7327011	2005-11-02	2008-02-05	Granted	United States of America	Multi-surfaced plate-to-plate capacitor and method of forming same
201010115825X	ZL 201010115825.X	2004-08-04	2011-12-28	Lapsed	China	A Spiral Inductor Formed In A Semiconductor Substrate And A Method For Forming The Inductor
09918183	6710616	2001-07-30	2004-03-23	Granted	United States of America	Wafer level dynamic burn-in
60135564		1999-05-24		Expired	United States of America	Low Temperature Tungsten Deposition
60462504		2003-04-10		Expired	United States of America	Aluminum Pad Power Bus In A Copper Technology
60115526		1999-01-12		Expired	United States of America	Stacked High-K Dielectric Capacitor For Dual Damascene Structure
11078830	7482642	2005-03-11	2009-01-27	Lapsed	United States of America	Bipolar Transistors having Controllable Temperature Coefficient of Current Gain
2005100927070	ZL200510092707.0	2005-08-18	2009-10-07	Granted	China	Failure Analysis Vehicle for Yield Enhancement with Self Test at Speed Burning Capability for Reliability Testing
60115781		1999-01-13		Expired	United States of America	Novel Method Of Making EDRAM Capacitor

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
60075293		1998-02-20		Expired	United States of America	A Process For Device Fabrication Using A Variable Transmission Aperture
10927985	7015569	2004-08-26	2006-03-21	Lapsed	United States of America	Method and apparatus for implementing a co-axial wire in a semiconductor chip
10944996	7799166	2004-09-20	2010-09-21	Lapsed	United States of America	Wafer Edge Expose Alignment Method
60165542		1999-11-15		Expired	United States of America	System And Method For Removal Of Material
60168911		1999-12-03		Expired	United States of America	CMOS With Metal Gates By Work Function Engineering
60158268		1999-10-07		Expired	United States of America	Electron Beam Imaging Apparatus
60301295		2001-06-28		Expired	United States of America	Full Via First Integration Method Of Manufacture
10945177	7154734	2004-09-20	2006-12-26	Granted	United States of America	Fully shielded capacitor cell structure
60520265		2003-11-14		Expired	United States of America	Control Of Hot Carrier Degradation In LDMOS Devices By A Dummy Gate Field Plate
60197283		2000-04-14		Expired	United States of America	Novel Method Of Coil Preparation For Ionized Metal Plasma Processes
09560935	6365426	2000-04-30	2002-04-02	Granted	United States of America	Method Of Determining The Impact Of Plasma-Charging Damage On Yield And Reliability In Submicron Integrated Circuits
09972482	6639298	2001-10-05	2003-10-28	Granted	United States of America	A Multi-Layer Inductor Formed In A Semicondutor Substrate
09243047	6259149	1999-02-03	2001-07-10	Granted	United States of America	Fully\(milsolated Thin\(miFilm Trench Capacitor
60141348		1999-06-28		Expired	United States of America	Impact Of Plasma-Charging Damage On Yield And Reliability In Deep Submicron CMOS VLSI Circuits
2009234206	5479839	2009-10-08	2014-02-21	Lapsed	Japan	Architecture for Circuit Connection of a Vertical Transistor
09334491	6309932	1999-06-16	2001-10-30	Granted	United States of America	Process For Forming A Plasma Nitride Film Suitable For Gate Dielectric Application In Sub\(mi0.25 \(*mm Technologies
09121266	6051346	1998-07-23	2000-04-18	Granted	United States of America	Process For Fabricating A Lithographic Mask
1020090066235	10-929335	2009-07-21	2009-11-24	Granted	Korea, Republic of (KR)	Vertical Replacement-Gate Junction Field-Effect Transistor
60115785		1999-01-13		Expired	United States of America	Tapered Plug For EDRAM/Capacitor Application
09190351	6015644	1998-11-12	2000-01-18	Granted	United States of America	Process For Device Fabrication Using A Variable Transmission Aperture
2009038940		2009-02-23		Abandoned	Japan	A Process For Manufacturing An Integrated Circuit Including A Dual-Damascene Structure And An Integrated Circuit
2009032389	5334616	2009-02-16		Granted	Japan	A Process For Manufacturing An Integrated Circuit Including A Dual-Damascene Structure And An Integrated Circuit
11189217	7763908	2005-07-25	2010-07-27	Lapsed	United States of America	Design Of Silicon-Controlled Rectifier By Considering Electrostatic Discharge Robustness In Human-Body Model And Charged-Device Model Devices
60088157		1998-06-05		Expired	United States of America	Method Of Planarizing A Surface Of An Integrated Circuit
60096407		1998-08-13		Expired	United States of America	Yield Improvement Via Automatic Analysis Of Wafer Processing Order

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09365059	6504292	1999-07-30	2003-01-07	Granted	United States of America	Field Emitting Device Comprising Metallized Nanostructures And Method For Making The Same
09943196	7601643	2001-08-30	2009-10-13	Lapsed	United States of America	Use of Non Aqueous Solvents in Low k CMP
60098431		1998-08-31		Expired	United States of America	Method For Making Enhanced Performance Field Effect Devices
60174549		2000-01-05		Expired	United States of America	An Integrated Circuit And A Method Of Making An Integrated Circuit
60524341		2003-11-21		Expired	United States of America	Method Of Determining The Reliability Of Semiconductor Devices Having Thin Gate Oxides
10969745	7171638	2004-10-20	2007-01-30	Granted	United States of America	Methods of screening ASIC defects using independent component analysis of quiescent current measurements
09755828	7638380	2001-01-04	2009-12-29	Lapsed	United States of America	Method for Manufacturing a Laterally Diffused Metal Oxide Semiconductor Device
1020097023840	10-1122521	2007-05-17	2012-02-24	Lapsed	Korea, Republic of (KR)	Method For Separating A Semiconductor Wafer Into Individual Semiconductor Dies Using An Implanted Inpurity
09842214	6969472	2001-04-25	2005-11-29	Lapsed	United States of America	Method of fabricating sub-micron hemispherical and hemicylidrical structures from non-spherically shaped templates
09591626	6420714	2000-06-09	2002-07-16	Granted	United States of America	Electron Beam Imaging Apparatus
2010508351		2007-05-17		Abandoned	Japan	Method For Separating A Semiconductor Wafer Into Individual Semiconductor Dies Using An Implanted Inpurity
10505198	7342225	2005-03-02	2008-03-11	Granted	United States of America	Crystallographic Metrology And Process Control
09364603	6249016	1999-07-30	2001-06-19	Granted	United States of America	Integrated Circuit Capacitor Including Tapered Plug
60128937		1999-04-13		Expired	United States of America	A Method For Matching Thin Film Thickness Measurement Tools
60144547		1999-07-15		Expired	United States of America	Field Emitting Device Comprising Metalized Nanostructures And Method For Making The Same
60143691		1999-07-14		Expired	United States of America	Buried In Glass Silicon Tantalum Integrated Circuit (BIG STIC)
60106945		1998-11-04		Expired	United States of America	An Inductor Or Low Loss Interconnect And A Method Of Manufacturing An Inductor Or Low Loss Interconnect In An Integrated Circuit
60116042		1999-01-14		Expired	United States of America	A Plasma Nitride Process Suitable For Gate Dielectric Application In Sub\(mi0.25 \(*mm Technologies
08943585	5904523	1997-10-03	1999-05-18	Expired	United States of America	Process For Device Fabrication In Which A Layer Of Oxynitride Is Formed At Low Temperatures
60028049		1996-10-03		Expired	United States of America	A Process For Device Fabrication
09205840	6312766	1998-12-04	2001-11-06	Granted	United States of America	Article Comprising Fluorinated Diamond-Like Carbon And Method For Fabricating Article
09211481	6336086	1998-12-14	2002-01-01	Granted	United States of America	Method And System For Analyzing Wafer Processing Order
60116122		1999-01-15		Expired	United States of America	PMOS Device Having A Layered Silicon Gate For Improved Silicide Integrity And Enhanced Boron Penetration Resistance

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
60043235		1997-04-11		Expired	United States of America	A Process For Forming Patterned Dielectric Oxide Films
10696320	7190185	2003-10-29	2007-03-13	Granted	United States of America	Methodology to measure many more transistors on the same test area
09056133	5976625	1998-04-07	1999-11-02	Granted	United States of America	Process For Forming Patterned Dielectric Oxide Films
60033839		1996-12-23		Expired	United States of America	Compound, High K, Gate And Capacitor Insulator Layer
60115718		1999-01-12		Expired	United States of America	Mask And Implant Savings For Dual Voltage CMOS Technologies
60592153		2004-07-29		Expired	United States of America	Method Of Electrical Probing
09481463	6403415	2000-01-11	2002-06-11	Granted	United States of America	A Semiconductor Device Having A Metal Barrier Layer For A Dielectric Material Having A High Dielectric Constant And A Method Of Manufacture Thereof
60756056		2006-01-04		Expired	United States of America	Formation Of An Integrated Circuit Structure With Reduced Dishing In Metallization Levels
09704635	6420277	2000-11-01	2002-07-16	Granted	United States of America	Process for inhibiting crack formation in low dielectric constant dielectric films of integrated circuit structure
60091896		1998-07-07		Expired	United States of America	Fully\(miIsolated Thin\(miFilm Trench Capacitor
60312389		2001-08-15		Expired	United States of America	Multiple Purpose Reticle Layout For Selectively Printing
12618936	8119501	2009-11-16	2012-02-21	Granted	United States of America	Method For Separating A Semiconductor Wafer Into Individual Semiconductor Dies Using An Implanted Inpurity
10610002	7581203	2003-06-30	2009-08-25	Lapsed	United States of America	Method And Apparatus For Manufacturing Multiple Circuit Patterns Using A Multiple Project Mask
09836365	6699372	2001-04-16	2004-03-02	Granted	United States of America	Method Of Coil Preparation For Ionized Metal Plasma Process And Method Of Manufacturing Integrated Circuits
09586586	6720261	2000-06-02	2004-04-13	Granted	United States of America	Method And System For Eliminating Extrusions In Semiconductor Vias
2007800530078		2007-05-17		Abandoned	China	Method For Separating A Semiconductor Wafer Into Individual Semiconductor Dies Using An Implanted Impurity
2015105007177		2007-05-17		Application	China	Method For Separating A Semiconductor Wafer Into Individual Semiconductor Dies Using An Implanted Impurity
09630463	6537867	2000-08-02	2003-03-25	Granted	United States of America	High Speed Low Voltage Semiconductor Devices And Method Of Fabrication
09363769	6207510	1999-07-29	2001-03-27	Granted	United States of America	Method For Making An Integrated Circuit Including High And Low Voltage Transistors
09292422	6271596	1999-04-15	2001-08-07	Granted	United States of America	Damascene Capacitors For Integrated Circuits
10950839	7183181	2004-09-27	2007-02-27	Granted	United States of America	Dynamic edge bead removal
09897517	6680243	2001-06-29	2004-01-20	Granted	United States of America	Shallow junction formation
09967094	7071563	2001-09-28	2006-07-04	Lapsed	United States of America	A Barrier Layer For Interconnect Structures Of A Semiconductor Wafer And Method For Depositing The Barrier Layer
09466285	6303397	1999-12-17	2001-10-16	Granted	United States of America	Method For Benchmarking Thin Film Measurement Tools

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09388682	6320244	1999-09-02	2001-11-20	Granted	United States of America	Integrated Circuit Device Having Dual Damascene Capacitor
09517965	6294468	2000-03-03	2001-09-25	Granted	United States of America	Method Of Chemical Vapor Depositing Tungsten Films
09339894	6303940	1999-06-25	2001-10-16	Granted	United States of America	Charge Injection Transistor Using High-K Dielectrics Barrier Layer
09416491	6313021	1999-10-12	2001-11-06	Granted	United States of America	PMOS Device Having A Layered Silicon Gate For Improved Silicide Integrity And Enhanced Boron Penetration Resistance
09340224	6235594	1999-06-25	2001-05-22	Granted	United States of America	Methods Of Fabricating An Integrated Circuit Device With Composite Oxide Dielectric
09364858	6440852	1999-07-30	2002-08-27	Granted	United States of America	Integrated Circuit Including Passivated Copper Interconnection Lines And Associated Manufacturing Methods
10260727	7005375	2002-09-30	2006-02-28	Granted	United States of America	Method To Avoid Copper Contamination Of A Via Or Dual Damascene Structure
10675258	7566964	2003-09-30	2009-07-28	Granted	United States of America	Aluminum Pad Power Bus And Signal Routing For Integrated Circuit Devices Utilizing Copper Technology Interconnect Structures
10614776	6881664	2003-07-07	2005-04-19	Granted	United States of America	Process for planarizing upper surface of damascene wiring structure for integrated circuit structures
09364208	6169010	1999-07-30	2001-01-02	Granted	United States of America	Method For Making Integrated Circuit Capacitor Including Anchored Plug
10696203	7114143	2003-10-29	2006-09-26	Lapsed	United States of America	Process yield learning
10661013	7013222	2003-09-12	2006-03-14	Lapsed	United States of America	Wafer edge inspection data gathering
09354711	6184755	1999-07-16	2001-02-06	Granted	United States of America	Article Comprising A Variable Inductor
09412089	6430047	1999-10-04	2002-08-06	Granted	United States of America	Standardized Test Board For Testing Custom Chips
09648164	6903411	2000-08-25	2005-06-07	Granted	United States of America	Architecture For Circuit Connection Of A Vertical Transistor
09042388	6121101	1998-03-12	2000-09-19	Granted	United States of America	Process For Fabricating Bipolar And BICMOS Devices
10697507	7084408	2003-10-29	2006-08-01	Lapsed	United States of America	Vaporization and ionization of metals for use in semiconductor processing
08963687	6008123	1997-11-04	1999-12-28	Granted	United States of America	Method For Using A Hardmask To Form An Opening In A Semiconductor Substrate
10036020	6773994	2001-12-26	2004-08-10	Granted	United States of America	CMOS Vertical Replacement Gate (VRG) Transistors
08936132	5912797	1997-09-24	1999-06-15	Expired	United States of America	Dielectric Materials Of Amorphous Compositions And Devices Employing Same
10121370	6899596	2002-04-12	2005-05-31	Lapsed	United States of America	Chemical Mechanical Polishing Of Dual Orientation Polycrystalline Materials
10627289	6958541	2003-07-25	2005-10-25	Lapsed	United States of America	Low gate resistance layout procedure for RF transistor devices
09515730	6599837	2000-02-29	2003-07-29	Granted	United States of America	Chemical Mechanical Polishing Composition And Method Of Polishing Metal Layers Using Same
09384395	6368753	1999-08-27	2002-04-09	Granted	United States of America	Mask Repair
09220417	6110012	1998-12-24	2000-08-29	Granted	United States of America	Chemical-Mechanical Polishing Apparatus And Method

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10920656	7087959	2004-08-18	2006-08-08	Lapsed	United States of America	Metal-Oxide-Semiconductor Device Having An Enhanced Shielding Structure
08804782	5903037	1997-02-24	1999-05-11	Expired	United States of America	GaAs-Based MOSFET, And Method Of Making Same
09386065	6365327	1999-08-30	2002-04-02	Granted	United States of America	A Process For Manufacturing An Integrated Circuit Including A Dual-Damascene Structure And An Integrated Circuit
09384459	6225639	1999-08-27	2001-05-01	Granted	United States of America	Method Of Monitoring A Patterned Transfer Process Using Line Width Metrology
09034079	5955381	1998-03-03	1999-09-21	Granted	United States of America	Integrated Circuit Fabrication
10628614	7968859	2003-07-28	2011-06-28	Granted	United States of America	Wafer edge defect inspection using captured image analysis
09339085	6071808	1999-06-23	2000-06-06	Granted	United States of America	Method Of Passivating Copper Interconnects In A Semiconductor
10953478	7176781	2004-09-29	2007-02-13	Granted	United States of America	Structure And Method For Adjusting Integrated Circuit Resistor Value
10679004	6982206	2003-10-02	2006-01-03	Granted	United States of America	Mechanism for improving the structural integrity of low-k films
09451078	6206054	1999-11-30	2001-03-27	Granted	United States of America	Automatic Compound Shaking Machine
09174503	6363606	1998-10-16	2002-04-02	Granted	United States of America	Process For Forming Integrated Structures Using Three Dimensional Printing Techniques
10628986	6986112	2003-07-28	2006-01-10	Lapsed	United States of America	Method of mapping logic failures in an integrated circuit die
08946413	5989984	1997-10-07	1999-11-23	Expired	United States of America	Method of Using A Getter Layer To Improve Metal To Metal Contact Resistance At Low Radio Frequency Power
09650606	6458669	2000-08-30	2002-10-01	Granted	United States of America	Method of Manufacturing An Integrated Circuit
08346706	5534721	1994-11-30	1996-07-09	Expired	United States of America	Area-Efficient Layout For High Voltage Lateral Devices
08323945	5541402	1994-10-17	1996-07-30	Expired	United States of America	Imaging Active Pixel Device Having A Non-Destructive Read-Out Gate
09653295	6838717	2000-08-31	2005-01-04	Granted	United States of America	Stacked Structure For Parallel Capacitors And Method Of Fabrication
08299470	5504385	1994-08-31	1996-04-02	Expired	United States of America	Spaced-Gate Emission Device And Method For Making Same
08560671	5744840	1995-11-20	1998-04-28	Expired	United States of America	Electrostatic Protection Devices For Protecting Semiconductor Integrated Circuitry
08987491	6042995	1997-12-09	2000-03-28	Granted	United States of America	Lithographic Process For Device Fabrication Using A Multilayer Mask Which Has Been Previously Inspected
08951779	5936259	1997-10-16	1999-08-10	Expired	United States of America	Thin Film Transistor And Organic Semiconductor Material Therefor
09604519	6833557	2000-06-27	2004-12-21	Lapsed	United States of America	Integrated Circuit And A Method Of Manufacturing An Integrated Circuit
08586412	5891605	1996-01-16	1999-04-06	Expired	United States of America	Reduction In Damage To Optical Elements Used In Optical Lithography For Device Fabrication
09617687	6384452	2000-07-17	2002-05-07	Granted	United States of America	Electrostatic Discharge Protection Device With Monolithically Formed Resistor-Capacitor Portion
09250500	6720604	1999-02-16	2004-04-13	Granted	United States of America	Capacitor For An Integrated Circuit

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10675263	7078337	2003-09-30	2006-07-18	Lapsed	United States of America	Selective Isotropic Etch For Titanium Based Materials
08692836	5863843	1996-07-31	1999-01-26	Expired	United States of America	Wafer Holder For Thermal Processing Apparatus
09448349	6245692	1999-11-23	2001-06-12	Granted	United States of America	Method To Selectively Heat Semiconductor Wafers
09337741	6448569	1999-06-22	2002-09-10	Granted	United States of America	Bonded Article Having Improved Crystalline Structure And Work Function Uniformity And Method For Making The Same
08724128	5843827	1996-09-30	1998-12-01	Expired	United States of America	Method Of Reducing Dielectric Damage From Plasma Etch Charging
09009399	6197699	1998-01-20	2001-03-06	Granted	United States of America	Insitu Dry Cleaning Process For Poly Gate Etch
08627560	5728625	1996-04-04	1998-03-17	Expired	United States of America	Process For Device Fabrication In Which A Thin Layer Of Cobalt Silicide Is Formed
09385165	6313025	1999-08-30	2001-11-06	Granted	United States of America	A Process For Manufacturing An Integrated Circuit Including A Dual-Damascene Structure And An Integrated Circuit
09286929	6830942	1999-04-06	2004-12-14	Granted	United States of America	Method For Processing Silicon Workpieces Using Hybrid Optical Thermometer System
09379055	6674151	1999-08-23	2004-01-06	Granted	United States of America	Deuterium Passivated Semiconductor Device Having Enhanced Immunity To Hot Carrier Effects
09413742	6458289	1999-10-06	2002-10-01	Granted	United States of America	CMP Slurry For Polishing Semiconductor Wafers And Related Methods
09430226	6180518	1999-10-29	2001-01-30	Granted	United States of America	Method For Forming Vias in a Low Dielectric Constant Material
09540618	6573818	2000-03-31	2003-06-03	Granted	United States of America	Planar Magnetic Frame Inductors Having Open Cores
09451054	6483144	1999-11-30	2002-11-19	Granted	United States of America	Semiconductor Device Having Self-Aligned Contact And Landing PAD Structure And Method Of Forming Same
08735170	5754392	1996-10-22	1998-05-19	Expired	United States of America	Article Comprising A Relatively Temperature-Insensitive Ta-Oxide Based Capacitive Element
08366192	5559052	1994-12-29	1996-09-24	Expired	United States of America	Integrated Circuit with Interlevel Dielectric
08566766	5620909	1995-12-04	1997-04-15	Expired	United States of America	Method of Depositing Thin Passivating Film on Microminiature Semiconductor Devices
09354928	6322713	1999-07-15	2001-11-27	Granted	United States of America	Nanoscale Conductive Connectors And Method For Making Same
08295303	5461245	1994-08-24	1995-10-24	Expired	United States of America	Article Comprising A Bipolar Transistor With Floating Base
09152185	6242989	1998-09-12	2001-06-05	Granted	United States of America	Article Comprising A Multiport Variable Capacitor
08531115	5711891	1995-09-20	1998-01-27	Expired	United States of America	Wafer Processing Using Thermal Nitride Etch Mask
08176600	5438006	1994-01-03	1995-08-01	Expired	United States of America	Method of Fabricating Gate Stack Having a Reduced Height
07815316	5880022	1991-12-30	1999-03-09	Expired	United States of America	Self-Aligned Contact Window
08977318	6147388	1997-11-24	2000-11-14	Granted	United States of America	Polycide Gate Structure With Intermediate Barrier
08595543	5780175	1996-02-02	1998-07-14	Expired	United States of America	Articles Comprising Magnetically Soft Thin Films And Methods For Making Such Articles
08326449	5521031	1994-10-20	1996-05-28	Expired	United States of America	Pattern Delineating Apparatus For Use In The EUV Spectrum
08856561	6316950	1997-05-15	2001-11-13	Expired	United States of America	Method And Apparatus For Imaging Semiconductor Devices
08299701	5510007	1994-08-31	1996-04-23	Expired	United States of America	Electrochemical Generation Of Silane

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09080992	6051500	1998-05-19	2000-04-18	Granted	United States of America	Device And Method For Polishing A Semiconductor Substrate
08754607	5728607	1996-11-20	1998-03-17	Expired	United States of America	Method Of Making A P-Channel Bipolar Transistor
08565286	5688704	1995-11-30	1997-11-18	Expired	United States of America	Integrated Circuit Fabrication
08538318	5658485	1995-10-03	1997-08-19	Expired	United States of America	Pyrochlore Based Oxides With High Dielectric Constant and Low Temperature Coefficient
08391905	5656182	1995-02-21	1997-08-12	Expired	United States of America	A Process For Fabricating A Device In Which The Process Is Controlled By Near-Field Imaging Latent Features Introduced Into Energy Sensitive Resist Materials
08451283	5948570	1995-05-26	1999-09-07	Expired	United States of America	Process For Dry Lithographic Etching
08505047	5527425	1995-07-21	1996-06-18	Expired	United States of America	Method Of Making In-Containing III/V Semiconductor Devices
08769605	6020256	1996-12-18	2000-02-01	Expired	United States of America	Method of Integrated Circuit Fabrication
08570906	5625140	1995-12-12	1997-04-29	Expired	United States of America	Acoustic Analysis Of Gas Mixtures
08359309	5559360	1994-12-19	1996-09-24	Expired	United States of America	Inductor for High Frequency Circuits
08118109	5838033	1993-09-08	1998-11-17	Expired	United States of America	Integrated Circuit with Gate Conductor Defined Resistor
09503225	6342134	2000-02-11	2002-01-29	Granted	United States of America	Method For Producing Piezoelectric Films With Rotating Magnetron Sputtering System
09450525	6136702	1999-11-29	2000-10-24	Granted	United States of America	Thin Film Transistors
09513390	6406609	2000-02-25	2002-06-18	Granted	United States of America	A Method Of Fabricating An Integrated Circuit
09567675	6603119	2000-05-09	2003-08-05	Granted	United States of America	Calibration Method For Quantitative Elemental Analysis
09551050	6399413	2000-04-18	2002-06-04	Granted	United States of America	Self Alignbed Gated Schottky Diode Guard Ring Structures
09432926	6358359	1999-11-03	2002-03-19	Granted	United States of America	Apparatus for Detecting Plasma Etch Endpoint In Semiconductor Fabrication And Associated Method
09543808	6429040	2000-04-06	2002-08-06	Granted	United States of America	Device Comprising Bipolar Semi-Conducting Film
09484759	6274409	2000-01-18	2001-08-14	Granted	United States of America	Method For Making A Semiconductor Device
09553931	6726537	2000-04-21	2004-04-27	Granted	United States of America	Polishing Carrier Head
09488355	6436608	2000-01-20	2002-08-20	Granted	United States of America	Lithographic Method Utilizing A Phase-Shifting Mask
09996118	6815342	2001-11-27	2004-11-09	Granted	United States of America	Low resistance metal interconnect lines and a process for fabricating them
89112402	NI-198319	2000-09-20	2004-03-21	Lapsed	Taiwan	High Quality Oxide For Use In Integrated Circuits
89108620	NI-203326	2000-07-15	2004-06-11	Lapsed	Taiwan	Electron Emitters for Lithography Tools
91119023	NI-185928	2002-08-22	2004-01-14	Lapsed	Taiwan	CMOS Vertical Replacement Gate (VRG) Transistors
88119230	NI-186701	2000-02-18	2003-09-01	Granted	Taiwan	An Inductor Or Low Loss Interconnect And A Method Of Manufacturing An Inductor Or Low Loss Interconnect In An Integrated Circuit
89109253	NI-172855	2000-05-15	2003-03-01	Lapsed	Taiwan	Charge Injection Transistor Using High-K Dielectrics Barrier Layer
89109252	NI-145230	2000-05-15	2001-12-01	Granted	Taiwan	A Gate Stack Structure For Integrated Circuit Fabrication
89100250	NI-155124	2000-01-10	2002-05-11	Lapsed	Taiwan	Damascene Capacitors For Integrated Circuits
88102935	NI-138362	1999-02-26	2001-08-11	Lapsed	Taiwan	Integrated Circuit Fabrication

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11427494	7982286	2006-06-29	2011-07-19	Granted	United States of America	Method To Improve Metal Defects In Semiconductor Device Fabrication
10691938	6870386	2003-10-23	2005-03-22	Lapsed	United States of America	Method and apparatus for measuring sheet resistance
88119226	NI-132577	1999-11-30	2001-05-28	Granted	Taiwan	Simplified High Q Inductor Substrate
09477833	6517416	2000-01-05	2003-02-11	Granted	United States of America	A Chemical Mechancial Polisher Including A Pad Conditioner And A Method Of Manufacturing An Integrated Circuit Using The Chemical Mechanical Polisher
90121536	I260734	2001-08-29	2006-08-21	Lapsed	Taiwan	Architecture For Circuit Connection Of A Vertical Transistor
91101551	NI-178411	2002-01-30	2003-09-18	Granted	Taiwan	A Barrier Layer For Interconnect Structures Of A Semiconductor Wafer And Method For Depositing The Barrier Layer
89112268	NI-131524	2000-06-22	2001-05-01	Lapsed	Taiwan	Bonded Article Having Improved Crystalline Structure And Work Function Uniformity And Method For Making The Same
90114096	I256683	2001-06-12	2006-06-11	Lapsed	Taiwan	Process For Manufacturing An Integrated Circuit Including A Dual-Damascene Structure And A Capacitor
91121020	NI-189019	2002-09-13	2004-02-16	Lapsed	Taiwan	A Multi-Layer Inductor Formed In A Semicondutor Substrate
89111610	NI-160919	2000-06-14	2002-08-11	Lapsed	Taiwan	A Process For Manufacturing An Integrated Circuit Including A Dual-Damascene Structure And An Integrated Circuit
89111675	NI-162650	2000-06-15	2002-09-11	Lapsed	Taiwan	A Process For Manufacturing An Integrated Circuit Including A Dual-Damascene Structure And An Integrated Circuit
88119654	NI-147721	1999-11-10	2002-01-01	Granted	Taiwan	Chemical-Mechanical Polishing Apparatus And Method
09505762	6383858	2000-02-16	2002-05-07	Granted	United States of America	Interdigitated Capacitor Structure For Use In An Integrated Circuit
093119217	I412119	2004-06-29	2013-10-11	Lapsed	Taiwan	A Spiral Inductor Formed In A Semiconductor Substrate And A Method For Forming The Inductor
87111331	NI-111955	1998-07-13	2000-02-21	Lapsed	Taiwan	Process For Device Fabrication
88110493	NI-124018	1999-06-22	2001-04-20	Granted	Taiwan	Thin Film Transistors
87121335	NI-131816	1998-12-21	2001-09-03	Lapsed	Taiwan	Insitu Dry Cleaning Process For Poly Gate Etch
87114709	NI-118398	1998-09-29	2000-08-01	Lapsed	Taiwan	Method Of Mechanical Polishing
87105344	NI-106777	1998-04-09	1999-09-11	Lapsed	Taiwan	Method And Apparatus For Imaging Semiconductor Devices
09631755	6657281	2000-08-03	2003-12-02	Lapsed	United States of America	Bipolar Tranistor Having A Low K Material In The Emitter Region
86100615	NI-104341	1997-01-21	1999-11-02	Expired	Taiwan	Articles Comprising Magnetically Soft Thin Films And Methods For Making Such Articles
09528753	6518622	2000-03-20	2003-02-11	Granted	United States of America	Vertical Replacement Gate (VRG) MOSFET With A Conductive Layer Adjacent A Source/Drain Region And Method Of Manufacture Therefor
90100857	NI-151372	2001-01-15	2002-06-21	Lapsed	Taiwan	A Capacitor For Integration With Copper Damascene Processes
89103722	NI-146566	2000-05-24	2002-04-08	Granted	Taiwan	Fabricating High-Q RF Component

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09413741	6436830	1999-10-06	2002-08-20	Granted	United States of America	CMP System For Polishing Semiconductor Wafers And Related Method
90118908	NI-169919	2001-08-02	2002-11-21	Granted	Taiwan	Bipolar Tranistor Having A Low K Material In The Emitter Region
09384631	6586310	1999-08-27	2003-07-01	Granted	United States of America	High Resistivity Film For 4T SRAM
1020000035106	734757	2000-06-24	2007-06-27	Granted	Korea, Republic of (KR)	High Quality Oxide For Use In Integrated Circuits
20010002872	676643	2001-01-18	2007-01-25	Lapsed	Korea, Republic of (KR)	Method For Making A Semiconductor Device
1020000019775	614781	2000-04-15	2006-08-16	Granted	Korea, Republic of (KR)	A Lithographic Process Having Sub-Wavelength Resolution
1019990008029	549974	1999-03-11	2006-02-01	Lapsed	Korea, Republic of (KR)	Process For Fabricating Bipolar And BICMOS Devices
1020000063481	756200	2000-10-27	2007-08-31	Lapsed	Korea, Republic of (KR)	Method For Forming Vias in a Low Dielectric Constant Material
1019990034561	667603	1999-08-20	2007-01-05	Lapsed	Korea, Republic of (KR)	Thin Film Transistors
987041	292707	1998-03-04	2001-03-26	Lapsed	Korea, Republic of (KR)	Thin Film Tantalum Oxide Capacitors And Resulting Product
9850861	347648	1998-11-26	2002-07-24	Lapsed	Korea, Republic of (KR)	Method For Removing Etching Residues And Contaminants
9849182	380514	1998-11-17	2003-04-03	Lapsed	Korea, Republic of (KR)	Integrated Circuit Conductors That Avoid Current Crowding
19970024048	279034	1997-06-07	2000-10-26	Expired	Korea, Republic of (KR)	Dose Modification Proximity Effect Compensation (PEC) Technique For Electron Beam Lithography
9817633	271843	1998-05-15	2000-08-21	Lapsed	Korea, Republic of (KR)	Method And Apparatus For Imaging Semiconductor Devices
1019980015165	329580	1998-04-28	2002-03-09	Lapsed	Korea, Republic of (KR)	Deuterated Bipolar Transistors And Method Of Manufacture Thereof
10397451	6746925	2003-03-25	2004-06-08	Granted	United States of America	High-k dielectric bird's beak optimizations using in-situ O2 plasma oxidation
10423184	7262119	2003-04-25	2007-08-28	Granted	United States of America	Method for incorporating germanium into a semiconductor wafer
1020010052995	847233	2001-08-30	2008-07-14	Lapsed	Korea, Republic of (KR)	Method of Manufacturing An Integrated Circuit
1020010025174	445020	2001-05-09	2004-08-10	Lapsed	Korea, Republic of (KR)	Calibration Method For Quantitative Elemental Analysis
1020000001148	695026	2000-01-11	2007-03-08	Lapsed	Korea, Republic of (KR)	Integrated Circuit Device Having Dual Damascene Capacitor
1020000000859	10-0658954	2000-01-10	2006-12-12	Granted	Korea, Republic of (KR)	Damascene Capacitors For Integrated Circuits
1019990031535	570910	1999-07-31	2006-04-07	Lapsed	Korea, Republic of (KR)	Silicon Germanium Heterostructure Bipolar Transistor With Indium Doped Base
19990011551	0313423	1999-04-02	2001-10-19	Lapsed	Korea, Republic of (KR)	Membrane Mask for Projection Lithography
1019990008028	319571	1999-03-11	2001-12-20	Granted	Korea, Republic of (KR)	Electronic Components With Doped Metal Oxide Dielectric Materials And A Process For Making Electronic Components With Doped Metal Oxide Dielectric Materials
1019990001574	371623	1999-01-20	2003-01-27	Granted	Korea, Republic of (KR)	Electronic Apparatus
20010003082	429726	2001-01-19	2004-04-20	Lapsed	Korea, Republic of (KR)	A Capacitor For Integration With Copper Damascene Processes
20000010425	605779	2000-03-02	2006-07-20	Granted	Korea, Republic of (KR)	Fabricating High-Q RF Component
1020000035368	767610	2000-06-26	2007-10-10	Granted	Korea, Republic of (KR)	A Gate Stack Structure For Integrated Circuit Fabrication
1020070065264	10-1359555	2007-06-29	2014-01-29	Lapsed	Korea, Republic of (KR)	Method To Improve Metal Defects In Semiconductor Device Fabrication

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
1020040065903	10-1084959	2004-08-20	2011-11-14	Granted	Korea, Republic of (KR)	A Spiral Inductor Formed In A Semiconductor Substrate And A Method For Forming The Inductor
10435442	7001695	2003-05-09	2006-02-21	Lapsed	United States of America	Multiple alternating phase shift technology for amplifying resolution
2001138037	5544677	2001-05-09	2014-07-09	Granted	Japan	Calibration Method For Quantitative Elemental Analysis
2000135070	3492977	2000-05-08	2003-11-14	Granted	Japan	Electron Emitters for Lithography Tools
2000048754	3524461	2000-02-25	2004-02-20	Lapsed	Japan	Process For The Fabrication Of Dual Gate Structures For CMOS Devices
2000381501	4138232	2000-12-15	2008-06-13	Granted	Japan	Dual Damascene Bond Pad Structure for Lowering Stress and Allowing Circuitry Under Pads
1020040023990	10-1084957	2004-04-08	2011-11-14	Granted	Korea, Republic of (KR)	Aluminum Pad Power Bus And Signal Routing For Integrated Circuit Devices Utilizing Copper Technology Interconnect Structures
10268775	3649917	1998-09-22	2005-02-25	Lapsed	Japan	Dielectric Materials Of Amorphous Compositions And Devices Employing Same
90121470	NI-170349	2001-08-30	2002-12-21	Granted	Taiwan	Stacked Structure For Parallel Capacitors And Method Of Fabrication
91119882	NI-188794	2002-08-30	2004-02-12	Lapsed	Taiwan	Vertical Replacement-Gate Junction Field-Effect Transistor
20040082410	10-1044528	2004-10-15	2011-06-20	Lapsed	Korea, Republic of (KR)	Metal-Oxide Semiconductor Device Having Improved Performance And Reliability.
20050075648	10-1184123	2005-08-18	2012-09-12	Lapsed	Korea, Republic of (KR)	Metal-Oxide-Semiconductor Device Having An Enhanced Shielding Structure
1020020060412	10-939648	2002-10-04	2010-01-25	Lapsed	Korea, Republic of (KR)	A Multi-Layer Inductor Formed In A Semicondutor Substrate
1020040077975	10-1045194	2004-09-30	2011-06-23	Lapsed	Korea, Republic of (KR)	Real-Time Gate Etch Critical Dimension Control By Oxygen Monitoring
10041685	3187764	1998-02-24	2001-05-11	Lapsed	Japan	GaAs-Based MOSFET, And Method Of Making Same
88122552	NI-144804	2000-02-11	2001-11-21	Granted	Taiwan	Barrier For Copper Metallization
89100359	NI-144338	2000-01-11	2002-03-06	Lapsed	Taiwan	Integrated Circuit Device Having Dual Damascene Capacitor
10349957	3242079	1998-12-09	2001-10-19	Lapsed	Japan	Lithographic Process For Device Fabrication Using A Multilayer Mask Which Has Been Previously Inspected
10453821	6911093	2003-06-02	2005-06-28	Lapsed	United States of America	Lid liner for chemical vapor deposition chamber
08314671	3226808	1996-11-26	2001-08-31	Expired	Japan	Method of Depositing Thin Passivating Film on Microminiature Semiconductor Devices
09085442	3600399	1997-04-04	2004-09-24	Expired	Japan	Process For Device Fabrication In Which A Thin Layer Of Cobalt Silicide Is Formed
09256542	3315064	1997-09-22	2002-06-07	Lapsed	Japan	Method Of Reducing Dielectric Damage From Plasma Etch Charging
2001260998	4058710	2001-08-30	2007-12-28	Lapsed	Japan	Method of Manufacturing An Integrated Circuit
2000190017	3737341	2000-06-23	2005-11-04	Granted	Japan	High Quality Oxide For Use In Integrated Circuits
90110939	NI-203745	2001-05-08	2004-06-21	Lapsed	Taiwan	Calibration Method For Quantitative Elemental Analysis

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10295074	3387832	1998-10-16	2003-01-10	Lapsed	Japan	Thin Film Transistor And Organic Semiconductor Material Therefor
10197846	3529634	1998-07-13	2004-03-05	Lapsed	Japan	Process For Device Fabrication
10114190	3405520	1998-04-09	2003-03-07	Lapsed	Japan	Circuit And Method For Providing Interconnections Among Individual Integrated Circuit Chips In A Multi-Chip Module
10306067	6854104	2002-11-27	2005-02-08	Lapsed	United States of America	First approximation for OPC significant speed-up
1020000023964	634727	2000-05-04	2006-10-10	Lapsed	Korea, Republic of (KR)	Electron Emitters for Lithography Tools
1020010034116	727794	2001-06-16	2007-06-07	Lapsed	Korea, Republic of (KR)	Process For Manufacturing An Integrated Circuit Including A Dual-Damascene Structure And A Capacitor
1020010053055	748864	2001-08-25	2007-08-07	Lapsed	Korea, Republic of (KR)	Architecture For Circuit Connection Of A Vertical Transistor
1020010053374	0822331	2001-08-31	2008-04-08	Lapsed	Korea, Republic of (KR)	Methods of Fabricating A Metal-Oxide-Metal Capacitor And Associated Apparatus
20010014032	0437586	2001-03-19	2004-06-16	Lapsed	Korea, Republic of (KR)	Vertical Replacement Gate (VRG) MOSFET With A Conductive Layer Adjacent A Source/Drain Region And Method Of Manufacture Therefor
19990009959	357842	1999-03-24	2002-10-09	Lapsed	Korea, Republic of (KR)	Mold For Non-Photolithographic Fabrication Of Microstructures
08938099	6254456	1997-09-26	2001-07-03	Expired	United States of America	Modifying contact areas of a polishing pad to promote uniform removal rates
1019990008027	333996	1999-03-11	2002-04-11	Lapsed	Korea, Republic of (KR)	Article Comprising Fluorinated Diamond-Like Carbon And Method For Fabricating Article
1020000009286	821494	2000-02-25	2008-04-04	Lapsed	Korea, Republic of (KR)	Process For The Fabrication Of Dual Gate Structures For CMOS Devices
1019990060855	329096	1999-12-23	2002-03-06	Lapsed	Korea, Republic of (KR)	Chemical-Mechanical Polishing Apparatus And Method
1020000035302	684480	2000-06-26	2007-02-13	Lapsed	Korea, Republic of (KR)	Charge Injection Transistor Using High-K Dielectrics Barrier Layer
10403611	7016054	2003-03-31	2006-03-21	Lapsed	United States of America	Lithography line width monitor reflecting chip-wide average feature size
9850222	0296859	1998-11-23	2001-05-15	Lapsed	Korea, Republic of (KR)	Polycide Gate Structure With Intermediate Barrier
10434028	6929532	2003-05-08	2005-08-16	Lapsed	United States of America	Method and apparatus for filtering a chemical polishing slurry of a wafer fabrication process
10409859	6889818	2003-04-09	2005-05-10	Lapsed	United States of America	Wafer blade contact monitor
20000050243	456704	2000-08-29	2004-11-02	Granted	Korea, Republic of (KR)	Simplified High Q Inductor Substrate
20000058700	418231	2000-10-06	2004-01-29	Lapsed	Korea, Republic of (KR)	Electron Beam Imaging Apparatus
1020040078027	10-1214818	2004-09-30	2012-12-17	Granted	Korea, Republic of (KR)	Selective Isotropic Etch For Titanium Based Materials
1020020054579	10-931816	2002-09-10	2009-12-07	Granted	Korea, Republic of (KR)	Vertical Replacement-Gate Junction Field-Effect Transistor
2000328233	4187399	2000-10-27	2008-09-19	Lapsed	Japan	Method For Forming Vias in a Low Dielectric Constant Material
2000104530	3676183	2000-04-06	2005-05-13	Lapsed	Japan	Method For Processing Silicon Workpieces Using Hybrid Optical Thermometer System
2002371914		2002-12-24		Lapsed	Japan	CMOS Vertical Replacement Gate (VRG) Transistors

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
2001217199	4931296	2001-07-17	2012-02-24	Lapsed	Japan	Electrostatic Discharge Protection Device With Monolithically Formed Resistor-Capacitor Portion
2000189020	4108252	2000-06-23	2008-04-11	Lapsed	Japan	Charge Injection Transistor Using High-K Dielectrics Barrier Layer
11240663	3506965	1999-08-27	2003-12-26	Granted	Japan	Process For Fabricating Vertical Transistors
10333150	3306804	1998-11-24	2002-05-17	Lapsed	Japan	Polycide Gate Structure With Intermediate Barrier
11100764	3408990	1999-04-08	2003-03-14	Lapsed	Japan	Membrane Mask for Projection Lithography
2001032114	4917711	2001-02-08	2012-02-03	Lapsed	Japan	Method For Producing Devices Having Piezoelectric Films
2002291750	4903971	2002-10-04	2012-01-13	Granted	Japan	A Multi-Layer Inductor Formed In A Semicondutor Substrate
10132894	3217750	1998-05-15	2001-08-03	Lapsed	Japan	Method And Apparatus For Imaging Semiconductor Devices
10334430	6980917	2002-12-30	2005-12-27	Lapsed	United States of America	Optimization of die yield in a silicon wafer sweet spot
10327452	7171047	2002-12-20	2007-01-30	Granted	United States of America	Adaptive Sem edge recognition algorithm
2004278665	5073159	2004-09-27	2012-08-31	Lapsed	Japan	Real-Time Gate Etch Critical Dimension Control By Oxygen Monitoring
2005237420	5111744	2005-08-18	2012-10-19	Lapsed	Japan	Metal-Oxide-Semiconductor Device Having An Enhanced Shielding Structure
2000309801	3895535	2000-10-10	2006-12-22	Granted	Japan	Lens Array For Electron Beam Lithography Tool
2004114863		2004-04-09		Lapsed	Japan	Aluminum Pad Power Bus And Signal Routing For Integrated Circuit Devices Utilizing Copper Technology Interconnect Structures
2001108267	5036101	2001-04-06	2012-07-13	Lapsed	Japan	Device Comprising Bipolar Semi-Conducting Film
2001218921	4352365	2001-07-19	2009-08-07	Granted	Japan	Integrated Circuit Package Having Partially Exposed Conductive Layer
10251016	6544829	2002-09-20	2003-04-08	Granted	United States of America	Polysilicon gate salicidation
2001119052	5321933	2001-04-18	2013-07-26	Lapsed	Japan	Self Alignbed Gated Schottky Diode Guard Ring Structures
2005100702664	ZL 200510070266.4	2005-05-13	2009-05-06	Lapsed	China	Metal-Oxide-Semiconductor Device Having An Enhanced Shielding Structure
2007101270281	ZL200710127028.1	2007-06-28	2011-06-01	Lapsed	China	Method To Improve Metal Defects In Semiconductor Device Fabrication
2004100558476	ZL200410055847.6	2004-08-04	2010-08-18	Lapsed	China	A Spiral Inductor Formed In A Semiconductor Substrate And A Method For Forming The Inductor
10283630	6849512	2002-10-30	2005-02-01	Lapsed	United States of America	Thin gate dielectric for a CMOS transistor and method of fabrication thereof
09670998	6482075	2000-09-27	2002-11-19	Granted	United States of America	Process for planarizing an isolation structure in a substrate
2004100432567	ZL 200410043256.7	2004-05-14	2009-10-14	Granted	China	Method And Apparatus For Manufacturing Multiple Circuit Patterns Using A Multiple Project Mask
10277025	6869893	2002-10-21	2005-03-22	Granted	United States of America	Laminate low K film
2007171578	5393005	2007-06-29	2013-10-25	Lapsed	Japan	Method To Improve Metal Defects In Semiconductor Device Fabrication
2000189026		2000-06-23		Abandoned	Japan	A Gate Stack Structure For Integrated Circuit Fabrication

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
2004278932	4855665	2004-09-27	2011-11-04	Granted	Japan	Selective Isotropic Etch For Titanium Based Materials
2004300894	5334351	2004-10-15	2013-08-09	Lapsed	Japan	Metal-Oxide Semiconductor Device Having Improved Performance And Reliability.
2000362265	4820978	2000-11-29	2011-09-16	Lapsed	Japan	Semiconductor Device Having Self-Aligned Contact And Landing PAD Structure And Method Of Forming Same
200133034	5093943	2001-02-09	2012-09-28	Lapsed	Japan	Method For Producing Piezoelectric Films With Rotating Magnetron Sputtering System
2001061239	4397537	2001-03-06	2009-10-30	Lapsed	Japan	Vertical Replacement Gate (VRG) MOSFET With A Conductive Layer Adjacent A Source/Drain Region And Method Of Manufacture Therefor
2000362320	5099942	2000-11-29	2012-10-05	Granted	Japan	Thin Film Transistors
10324698	6743701	2002-12-20	2004-06-01	Granted	United States of America	Method for the formation of active area utilizing reverse trench isolation
09274254	6524974	1999-03-22	2003-02-25	Granted	United States of America	FORMATION OF IMPROVED LOW DIELECTRIC CONSTANT CARBON-CONTAINING SILICON OXIDE DIELECTRIC MATERIAL BY REACTION OF CARBON-CONTAINING SILANE WITH OXIDIZING AGENT IN THE PRESENCE OF ONE OR MORE REACTION RETARDANTS
1020050389988	102005038998.8	2005-08-16	2010-02-18	Lapsed	Germany (Federal Republic of)	Metal-Oxide-Semiconductor Device Having An Enhanced Shielding Structure
10328346	6864020	2002-12-24	2005-03-08	Lapsed	United States of America	Chromeless phase shift mask using non-linear optical materials
10293631	6870160	2002-11-13	2005-03-22	Granted	United States of America	Method and apparatus for monitoring the condition of a lubricating medium
10295489	6818365	2002-11-15	2004-11-16	Lapsed	United States of America	Feed forward leveling
10283688	6650958	2002-10-30	2003-11-18	Granted	United States of America	Integrated process tool monitoring system for semiconductor fabrication
09052793		1998-03-31		Abandoned	United States of America	Method of Electrically Connecting and Isolating Components With Vertical Elements Extending Between Interconnect Layers in an Integrated Circuit.
10341082	7023067	2003-01-13	2006-04-04	Lapsed	United States of America	Bond pad design
10201010	6645857	2002-07-22	2003-11-11	Granted	United States of America	Key hole filling
10335177	6812158	2002-12-31	2004-11-02	Granted	United States of America	Modular growth of multiple gate oxides
09695534	6376795	2000-10-24	2002-04-23	Granted	United States of America	Direct current dechucking system
09878741	6498045	2001-06-11	2002-12-24	Granted	United States of America	Optical intensity modifier
10163120	6608365	2002-06-04	2003-08-19	Granted	United States of America	Low leakage PMOS on-chip decoupling capacitor cells compatible with standard CMOS cells
10164227	6743669	2002-06-05	2004-06-01	Granted	United States of America	Method of reducing leakage using Si3N4 or SiON block dielectric films
10254708	6872321	2002-09-25	2005-03-29	Granted	United States of America	Direct positive image photo-resist transfer of substrate design

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10190954	6806038	2002-07-08	2004-10-19	Lapsed	United States of America	Plasma passivation
003025376	60046543.8	2000-03-28	2011-10-12	Lapsed	Germany (Federal Republic of)	Method For Processing Silicon Workpieces Using Hybrid Optical Thermometer System
993015437	69900028.9	1999-03-02	2000-11-15	Lapsed	Germany (Federal Republic of)	Process For Fabricating Bipolar And BICMOS Devices
983072323	69825384.1	1998-09-08	2004-08-04	Lapsed	Germany (Federal Republic of)	Dielectric Materials Of Amorphous Compositions And Devices Employing Same
983035007	69830946.4	1998-05-05	2005-07-27	Granted	Germany (Federal Republic of)	Method And Apparatus For Imaging Semiconductor Devices
10138609	6566244	2002-05-03	2003-05-20	Granted	United States of America	Process for improving mechanical strength of layers of low k dielectric material
003086857	60047649.9	2000-10-03	2012-11-21	Lapsed	Germany (Federal Republic of)	Lens Array For Electron Beam Lithography Tool
013001250	60142863.3	2001-01-08	2010-08-25	Granted	Germany (Federal Republic of)	A Capacitor For Integration With Copper Damascene Processes
003037801	60039551.0	2000-05-05	2008-07-23	Granted	Germany (Federal Republic of)	Electron Emitters for Lithography Tools
993015569	69900076.9	1999-03-02	2001-04-11	Lapsed	Germany (Federal Republic of)	Article Comprising Fluorinated Diamond-Like Carbon And Method For Fabricating Article
013070107	60121685.7	2001-08-17	2006-07-26	Lapsed	Germany (Federal Republic of)	Method of Manufacturing An Integrated Circuit
003090859	60038423.3	2000-10-16	2008-03-26	Lapsed	Germany (Federal Republic of)	Method For Forming Vias in a Low Dielectric Constant Material
993084235	69936175.3	1999-10-25	2007-05-30	Granted	Germany (Federal Republic of)	An Inductor Or Low Loss Interconnect And A Method Of Manufacturing An Inductor Or Low Loss Interconnect In An Integrated Circuit
973020498	69724317.6	1997-03-25	2003-08-27	Expired	Germany (Federal Republic of)	Process For Device Fabrication In Which A Thin Layer Of Cobalt Silicide Is Formed
003000528	60047099.7	2000-01-06	2012-04-18	Granted	Germany (Federal Republic of)	Integrated Circuit Device Having Dual Damascene Capacitor
003015302	60018121.9	2000-02-28	2005-02-16	Lapsed	Germany (Federal Republic of)	Fabricating High-Q RF Component
993087006	69937868.0	1999-11-02	2008-01-02	Granted	Germany (Federal Republic of)	Simplified High Q Inductor Substrate
10077497	6638776	2002-02-15	2003-10-28	Granted	United States of America	Thermal characterization compensation
09596909	6499001	2000-06-20	2002-12-24	Granted	United States of America	Engineering database feedback system
013007406	60143682.2	2001-01-29	2010-12-22	Granted	Germany (Federal Republic of)	Method For Producing Devices Having Piezoelectric Films

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10224025	6764389	2002-08-20	2004-07-20	Granted	United States of America	Conditioning bar assembly having an abrasion member supported on a polycarbonate member
09981200	6750668	2001-10-17	2004-06-15	Granted	United States of America	Vortex unit for providing a desired environment for a semiconductor process
09605380	6492731	2000-06-27	2002-12-10	Granted	United States of America	Composite low dielectric constant film for integrated circuit structure
09639449	6412358	2000-08-15	2002-07-02	Granted	United States of America	Cleanliness verification system
09971329	6472316	2001-10-04	2002-10-29	Granted	United States of America	Photolithography overlay control
09654689		2000-09-05		Abandoned	United States of America	Integrated Circuit Isolation System
09704164	6423630	2000-10-31	2002-07-23	Granted	United States of America	Process for forming low K dielectric material between metal lines
10007405	6537896	2001-12-04	2003-03-25	Granted	United States of America	Process for treating porous low k dielectric material in damascene structure to form a non-porous dielectric diffusion barrier on etched via and trench surfaces in the porous low k dielectric material
09957555	6641635	2001-09-19	2003-11-04	Granted	United States of America	Liquid based air filtration system
11438493	7605064	2006-05-22	2009-10-20	Lapsed	United States of America	Selective Laser Annealing Of Semiconductor Material
10105483	6574525	2002-03-25	2003-06-03	Granted	United States of America	In situ measurement
08277852	5691110	1994-07-20	1997-11-25	Expired	United States of America	Process For Controlled Deprotection Of Polymers And A Process For Fabricating A Device Utilizing Partially Deprotected Resist Polymers
08552998	5656412	1995-11-03	1997-08-12	Expired	United States of America	Energy-Sensitive Resist Material And A Process For Device Fabrication Using An Energy-Sensitive Resist Material
11339540	7342316	2006-01-26	2008-03-11	Granted	United States of America	Cross-Fill Pattern For Metal Fill Levels, Power-Supply Filtering, And Analog Circuit Shielding
2006353600	4797199	2006-12-28	2011-08-12	Lapsed	Japan	Article Comprising A Variable Inductor
2007187885	5676836	2001-08-03	2015-01-09	Granted	Japan	Bipolar Tranistor Having A Low K Material In The Emitter Region
10609889	6869873	2003-06-30	2005-03-22	Granted	United States of America	Copper Silicide Passivation For Improved Reliability
08644596	5596208	1996-05-10	1997-01-21	Expired	United States of America	Article Comprising An Organic Thin Film Transistor
2007063290	5011459	2001-06-27	2012-06-15	Lapsed	Japan	A Method of Testing an Integrated Circuit
2007130041	5392995	2000-06-21	2013-10-25	Lapsed	Japan	Bonded Article Having Improved Crystalline Structure And Work Function Uniformity And Method For Making The Same
2007210590		2004-08-20		Abandoned	Japan	A Spiral Inductor Formed In A Semiconductor Substrate And A Method For Forming The Inductor
20070073750	10-0890080	2001-02-09	2009-03-16	Lapsed	Korea, Republic of (KR)	Method For Producing Piezoelectric Films With Rotating Magnetron Sputtering System
08828155	5956618	1997-03-27	1999-09-21	Expired	United States of America	Process For Producing Multi\(miLevel Metallization In An Integrated Circuit

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08656996	5767557	1996-05-24	1998-06-16	Expired	United States of America	PMOSFETs Having Indium Or Gallium Doped Buried Channels And N\(pl PolysiliconGates And CMOS Devices Fabricated Therefrom
2007104568		2007-04-12		Abandoned	Japan	A Capacitor For Integration With Copper Damascene Processes
10721126	7067419	2003-11-25	2006-06-27	Granted	United States of America	Mask Layer And Dual Damascene Interconnect Structure In A Semiconductor Device
09000930	6228750	1997-12-30	2001-05-08	Expired	United States of America	Method of Doping a Semiconductor Surface
10694611	7301107	2003-10-27	2007-11-27	Granted	United States of America	Semiconductor Device Having Reduced Intra-Level And Inter-Level Capacitance
09391729	6150668	1999-09-08	2000-11-21	Granted	United States of America	Thin-Film Transistor Monolithically Integrated With An Organic Light-Emitting Diode
09241458	6211541	1999-02-02	2001-04-03	Granted	United States of America	An Article For De-Embedding Parasitics In Integrated Circuits
09041434	5923056	1998-03-12	1999-07-13	Expired	United States of America	Electronic Components With Doped Metal Oxide Dielectric Materials And A Process For Making Electronic Components With Doped Metal Oxide Dielectric Materials
08864220	5908312	1997-05-28	1999-06-01	Expired	United States of America	Semiconductor Device Fabrication
08441142	6278127	1995-05-15	2001-08-21	Granted	United States of America	Article Comprising An Organic Thin Film Transistor Adapted For Biasing To Form A N-Type Or A P-Type Transistor
08500729	5633103	1995-07-11	1997-05-27	Expired	United States of America	Self-Aligned Alignment Marks For Phase-Shifting Masks
09607511	6368979	2000-06-28	2002-04-09	Granted	United States of America	Process for forming trenches and vias in layers of low dielectric constant carbon-doped silicon oxide dielectric material of an integrated circuit structure
09574365	6512985	2000-05-19	2003-01-28	Granted	United States of America	Process control system
10012821	7314527	2001-12-10	2008-01-01	Granted	United States of America	Reactor system
09407357	6223770	1999-09-29	2001-05-01	Granted	United States of America	Vacuum valve interface
09932527	6723653	2001-08-17	2004-04-20	Granted	United States of America	Process for reducing defects in copper-filled vias and/or trenches formed in porous low-k dielectric material
09431439	6284586	1999-11-01	2001-09-04	Expired	United States of America	Integrated circuit device and method of making the same using chemical mechanical polishing to remove material in two layers following masking
09641661	6598194	2000-08-18	2003-07-22	Granted	United States of America	Test limits based on position
09428344	6316354	1999-10-26	2001-11-13	Granted	United States of America	Process for removing resist mask of integrated circuit structure which mitigates damage to underlying low dielectric constant silicon oxide dielectric layer
08673655	6115233	1996-06-28	2000-09-05	Expired	United States of America	Integrated circuit device having a capacitor with the dielectric peripheral region being greater than the dielectric central region
09953667	6718524	2001-09-17	2004-04-06	Granted	United States of America	Method and apparatus for estimating state-dependent gate leakage in an integrated circuit

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09607512	6350700	2000-06-28	2002-02-26	Granted	United States of America	Process for forming trenches and vias in layers of low dielectric constant carbon-doped silicon oxide dielectric material of an integrated circuit structure
09587609	6375550	2000-06-05	2002-04-23	Granted	United States of America	Method and apparatus for enhancing uniformity during polishing of a semiconductor wafer
09413667	6355532	1999-10-06	2002-03-12	Granted	United States of America	Subtractive oxidation method of fabricating a short-length and vertically-oriented channel, dual-gate, CMOS FET
09346493	6232658	1999-06-30	2001-05-15	Granted	United States of America	Process to prevent stress cracking of dielectric films on semiconductor wafers
09573123	6341056	2000-05-17	2002-01-22	Granted	United States of America	Capacitor with multiple-component dielectric and method of fabricating same
09946253	6648743	2001-09-05	2003-11-18	Granted	United States of America	Chemical mechanical polishing pad
09272732	6316817	1998-12-14	2001-11-13	Expired	United States of America	MeV implantation to form vertically modulated N+ buried layer in an NPN bipolar transistor
09109335	6077783	1998-06-30	2000-06-20	Granted	United States of America	Method and apparatus for detecting a polishing endpoint based upon heat conducted through a semiconductor wafer
09209704	6121147	1998-12-11	2000-09-19	Granted	United States of America	Apparatus and method of detecting a polishing endpoint layer of a semiconductor wafer which includes a metallic reporting substance
09344056	6348808	1999-06-25	2002-02-19	Granted	United States of America	Mobile ionic contamination detection in manufacture of semiconductor devices
09559934	6342734	2000-04-27	2002-01-29	Granted	United States of America	Interconnect-integrated metal-insulator-metal capacitor and method of fabricating same
10006398	6809824	2001-11-30	2004-10-26	Lapsed	United States of America	Alignment process for integrated circuit structures on semiconductor substrate using scatterometry measurements of latent images in spaced apart test fields on substrate
09302830	6136719	1999-04-30	2000-10-24	Granted	United States of America	Method and arrangement for fabricating a semiconductor device
09052793		1900-01-01		Abandoned	United States of America	Method of Electrically Connecting and Isolating Components with Vertical Elements Extending Between Interconnect Layers in an Integrated Circuit
08822078	5861055	1997-03-20	1999-01-19	Expired	United States of America	Polishing composition for CMP operations
09204813	6120607	1998-12-03	2000-09-19	Granted	United States of America	Apparatus and method for blocking the deposition of oxide on a wafer
08344898	3121274	1996-12-25	2000-10-20	Expired	Japan	Polishing Composition for CMP Operations
09074298	6071562	1998-05-07	2000-06-06	Granted	United States of America	Process for depositing titanium nitride films
08801668	5858828	1997-02-18	1999-01-12	Expired	United States of America	Use of MEV implantation to form vertically modulated N+ buried layer in an NPN bipolar transistor
10044215	6649537	2001-11-19	2003-11-18	Granted	United States of America	Intermittent pulsed oxidation process
08236706	5750312	1994-05-02	1998-05-12	Expired	United States of America	Process for Fabricating a Device

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08479018	5661091	1995-06-06	1997-08-26	Expired	United States of America	Method of manufacturing a semiconductor device having PN junctions separated by depressions
12339407	8423942	2008-12-19	2013-04-16	Granted	United States of America	Fill Patterning For Symmetrical Circuits
11273857	7332924	2005-11-15	2008-02-19	Granted	United States of America	Embedded Test Circuitry And A Method For Testing A Semiconductor Device For Breakdown, Wearout Or Failure
11237410	7291849	2005-09-28	2007-11-06	Granted	United States of America	Calibration Standard For Transmission Electron Microscopy
11853417	7820517	2007-09-11	2010-10-26	Lapsed	United States of America	Control Of Hot Carrier Injection In A Metal-Oxide Semiconductor Device
10977732	7279744	2004-10-29	2007-10-09	Granted	United States of America	Control Of Hot Carrier Injection In A Metal-Oxide Semiconductor Device
10953897	7116174	2004-09-29	2006-10-03	Lapsed	United States of America	Base Current Compensation Circuit For A Bipolar Junction Transistor
10947069	7074628	2004-09-22	2006-07-11	Lapsed	United States of America	Test Structure And Method For Yield Improvement Of Double Poly Bipolar Device
10623983	7138690	2003-07-21	2006-11-21	Granted	United States of America	Shielding Structure For Use In A Metal\(miOxide\(miSemiconductor Device
10643123	6893883	2003-08-18	2005-05-17	Granted	United States of America	Method and Apparatus Using An On-Chip Ring Oscillator For Chip Identification
10929843	7199685	2004-08-30	2007-04-03	Granted	United States of America	Three-Terminal Tuneable Active Inductor
10633334	7033931	2003-08-01	2006-04-25	Granted	United States of America	Temperature Optimization Of A Physical Vapor Deposition Process To Prevent Extrusion Into Openings
10007417	6683465	2001-10-31	2004-01-27	Granted	United States of America	Integrated Circuit Having Stress Migration Test Structure And Method Therefor
10007904	6747445	2001-10-31	2004-06-08	Granted	United States of America	Stress Migration Test Structure And Method Therefor
09993414	6472279	2001-11-05	2002-10-29	Granted	United States of America	Method Of Manufacturing A Channel Stop Implant In A Semiconductor Device
09785636	6462305	2001-02-16	2002-10-08	Granted	United States of America	Method Of Manufacturing A Polishing Pad Using A Beam
09777470		2001-02-06		Abandoned	United States of America	An Alternate Pad Conditioning Method
09778986	6702654	2001-02-07	2004-03-09	Granted	United States of America	Conditioning Wheel For Conditioning A Semiconductor Wafer Polishing Pad And Method Of Manufacture Thereof
09637496	6853048	2000-08-11	2005-02-08	Lapsed	United States of America	Bipolar Transistor Having An Isolation Structure Located Under The Base, Emitter And Collector And A Method Of Manufacture Thereof
09585159	6329226	2000-06-01	2001-12-11	Granted	United States of America	A Method For Fabricating A Thin-Film Transistor
09583936	6445206	2000-05-31	2002-09-03	Granted	United States of America	Method And Apparatus For Determining Yield Impacting Tests At Wafer Level And Package Level For Semiconductor Devices
09742314	6794694	2000-12-21	2004-09-21	Granted	United States of America	Inter-Wiring-Layer Capacitors
09557430	6506690	2000-04-25	2003-01-14	Granted	United States of America	Dielectric Deposition Method and Semiconductor Device

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09496829	6364744	2000-02-02	2002-04-02	Granted	United States of America	CMP System And Slurry For Polishing Semiconductor Wafers And Related Method
09317430	6524872	1999-05-24	2003-02-25	Granted	United States of America	Using Fast Hot-Carrier Aging Method For Measuring Plasma Charging Damage
09472326	6680780	1999-12-23	2004-01-20	Granted	United States of America	Interferometric Probe Stabilization Relative To Subject Movement
09470861	6366803	1999-12-23	2002-04-02	Granted	United States of America	Predictive Probe Stabilization Relative To subject Movement
09231566	6225801	1999-01-14	2001-05-01	Granted	United States of America	Article Comprising Electronic Circuits And Devices With Magnetically Programmable Electrical Resistance
09351971	6294447	1999-07-12	2001-09-25	Granted	United States of America	Method Of Making Devices Having Thin Dielectric Layers
09293510	6121827	1999-04-15	2000-09-19	Granted	United States of America	Digital Noise Reduction In Integrated Circuits And Circuit Assemblies
09223354	6440829	1998-12-30	2002-08-27	Granted	United States of America	N\(miProfile Engineering At The Poly\(slGate Oxide And Gate Oxide\(slSI Interfaces Through ! NH sub 3 !, Annealing Of A Layered Poly\(slá\(miSi Structure
09222110	6093668	1998-12-29	2000-07-25	Granted	United States of America	Low Temperature Coefficient Dielectric Materials And Devices Comprising Same
09162542	6177363	1998-09-29	2001-01-23	Granted	United States of America	A Method for Forming a Nitride Layer Suitable for Use in Advanced Gate Dielectric Materials
09126032	6037621	1998-07-29	2000-03-14	Granted	United States of America	On-Chip Capacitor Structure
09070387	5976331	1998-04-30	1999-11-02	Granted	United States of America	Electrodeposition Apparatus For Coating Wafers
09096998	6323131	1998-06-13	2001-11-27	Granted	United States of America	Passivated Copper Surfaces
09013486	6017805	1998-01-26	2000-01-25	Granted	United States of America	Method Of Reducing Mobile Ion Contaminants In Semiconductor Films
08919192	5894349	1997-08-20	1999-04-13	Expired	United States of America	Manufacturing Method Including Near-Field Optical Microscope Examination OfA Semiconductor Substrate
08756695	5841333	1996-11-26	1998-11-24	Expired	United States of America	Minimal Delay Conductive Lead Lines For Integrated Circuits
08887861	6011404	1997-07-03	2000-01-04	Expired	United States of America	System And Method For Determining Near-Surface Lifetimes And The Tunneling Field Of A Dielectric In A Semiconductor
08695441	5698934	1996-08-12	1997-12-16	Expired	United States of America	Field Emission Device With Randomly Distributed Gate Apertures
08548533	5588894	1995-10-26	1996-12-31	Expired	United States of America	Field Emission Device And Method For Making Same
09026227	6045977	1998-02-19	2000-04-04	Granted	United States of America	Process For Patterning Conductive Polyaniline Films
12953624	8624352	2010-11-24	2014-01-07	Granted	United States of America	Mitigation of Detrimental Breakdown of a High Dielectric Constant Metal-Insulator-Metal Capacitor in a Capacitor Bank
078690823		2007-12-10		Abandoned	European Patent	Chip Identification Using Top Metal Layer
12741839	8242603	2010-07-08	2012-08-14	Granted	United States of America	Chip Identification Using Top Metal Layer
2009549571	5084843	2007-02-14	2012-09-14	Lapsed	Japan	Method To Reduce Collector Resistance Of A Vertical PNP And Integration Into A Standard CMOS Process Flow

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
1020097019023	10-1320913	2007-02-14	2013-10-14	Lapsed	Korea, Republic of (KR)	Method To Reduce Collector Resistance Of A Bipolar Transistor and Integration into a CMOS Flow
12523368	7923340	2009-07-16	2011-04-12	Granted	United States of America	Method To Reduce Collector Resistance Of A Bipolar Transistor And Integration Into A Standard CMOS Flow
11535501	7847666	2006-09-27	2010-12-07	Granted	United States of America	Differential Inductor For Use In Integrated Circuits
11237095	7642617	2005-09-28	2010-01-05	Lapsed	United States of America	Integrated Circuit With Depletion Mode JFET
11383670	7563669	2006-05-16	2009-07-21	Lapsed	United States of America	Integrated Circuit With A Trench Capacitor Structure And Method Of Manufacture
11153893	7141486	2005-06-15	2006-11-28	Granted	United States of America	Shallow Trench Isolation Structures Comprising A Graded Doped Sacrificial Silicon Dioxide Material And A Method For Forming Shallow Trench Isolation Structures
097895247		2009-03-18		Abandoned	European Patent	Integrated Circuit Inductors With Directed Magnetic Flux Lines For Magnetic Coupling Reduction
20107028513	101575387	2009-03-18	2015-12-01	Granted	Korea, Republic of (KR)	Integrated Circuit Inductors With Directed Magnetic Flux Lines For Magnetic Coupling Reduction
098122453	I394180	2009-07-02	2013-04-21	Lapsed	Taiwan	Integrated Circuit Inductors With Directed Magnetic Flux Lines For Magnetic Coupling Reduction
2009801222622	ZL200980122262.2	2009-03-18	2014-03-19	Lapsed	China	Integrated Circuit Inductors With Directed Magnetic Flux Lines For Magnetic Coupling Reduction
2012500769		2010-12-13		Abandoned	Japan	Integrated Circuit Inductors With Directed Magnetic Flux Lines For Magnetic Coupling Reduction
12516301	8143696	2009-05-26	2012-03-27	Granted	United States of America	Integrated Circuit Inductors With Reduced Magnetic Coupling
10953632	7279393	2004-09-29	2007-10-09	Granted	United States of America	A Trench Isolation Structure And Method Of Manufacture Therefor
11649015	7727894	2007-01-03	2010-06-01	Lapsed	United States of America	Formation Of An Integrated Circuit Structure With Reduced Dishing In Metallization Levels
11094975	7329605	2005-03-31	2008-02-12	Granted	United States of America	Semiconductor Structure Formed Using A Sacrificial Structure
11927978	7741702	2007-10-30	2010-06-22	Granted	United States of America	Semiconductor Structure Formed Using A Sacrificial Structure
10903938	7768044	2004-07-30	2010-08-03	Granted	United States of America	Metal Capacitor Stacked With A MOS Capacitor To Provide Increased Capacitance Density
11673645	7557010	2007-02-12	2009-07-07	Granted	United States of America	Method To Improve Writer Leakage in a SiGe Bipolar Device
12476994	7898038	2009-06-02	2011-03-01	Granted	United States of America	Method To Improve Writer Leakage in SiGe Bipolar Device
10842139	7157365	2004-05-10	2007-01-02	Granted	United States of America	A Semiconductor Device Having A Dummy Conductive Via And A Method Of Manufacture Therefor
10778454	7005724	2004-02-13	2006-02-28	Lapsed	United States of America	A Semiconductor Device And A Method Of Manufacture Therefor
11167772	7811944	2005-06-27	2010-10-12	Lapsed	United States of America	A Semiconductor Device And A Method Of Manufacture Therefor
10675259	7087498	2003-09-30	2006-08-08	Lapsed	United States of America	Method for Controlling Trench Depth In Shallow Trench Isolation Features

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10706467	7254002	2003-11-12	2007-08-07	Granted	United States of America	Reverse Conduction Protection Method And Apparatus For A Dual Power Supply Driver
10716299	6910907	2003-11-18	2005-06-28	Lapsed	United States of America	Contact For Use In An Integrated Circuit And A Method Of Manufacture Therefor
10895574	7033257	2004-07-21	2006-04-25	Lapsed	United States of America	Carrier Head For Chemical Mechanical Polishing
11201039	7700491	2005-08-10	2010-04-20	Lapsed	United States of America	Stringer Elimination In A BICMOS Process
11205382	7172496	2005-08-17	2007-02-06	Granted	United States of America	Method And Apparatus For Cleaning Slurry Depositions From A Water Carrier
10382142	6828628	2003-03-05	2004-12-07	Granted	United States of America	Diffused MOS Devices With Strained Silicon Portions And Methods For Forming Same
10435870	6973637	2003-05-12	2005-12-06	Lapsed	United States of America	Process For The Selective Control Of Feature Size In Lithographic Processing
10953585	7084648	2004-09-29	2006-08-01	Lapsed	United States of America	Semiconductor Testing
10260694	6828561	2002-09-30	2004-12-07	Lapsed	United States of America	Apparatus And Method For Detecting Alpha Particles
10262654	6738294	2002-09-30	2004-05-18	Granted	United States of America	Electronic Fingerprinting Of Semiconductor Integrated Circuits
10898792	6963215	2004-07-26	2005-11-08	Lapsed	United States of America	Operation Of Semiconductor Devices Subject To Hot Carrier Injection
10799279	6951510	2004-03-12	2005-10-04	Lapsed	United States of America	Chemical Mechanical Polishing Pad With Grooves Alternating Between A Larger Groove Size And A Smaller Groove Size
10925555	7157375	2004-08-25	2007-01-02	Granted	United States of America	Methods Of Downstream Microwave Photoresist Removal And Via Clean, Particularly Following Stop-On TiN Etching
10768771	7034653	2004-01-30	2006-04-25	Lapsed	United States of America	Semiconductor Resistor
10699021	6919228	2003-10-31	2005-07-19	Lapsed	United States of America	Methods And Apparatus For The Detection Of Damaged Regions On Dielectric Film Or Other Portions Of A Die
09966779	6548422	2001-09-27	2003-04-15	Granted	United States of America	Method And Structure For Oxide/Silicon Nitride Interface Substructure Improvements
02223899	2383686	2002-09-26	2006-03-29	Lapsed	United Kingdom	Method And Structure For Oxide/Silicon Nitride Interface Substructure Improvements
1020020058733	10-0869913	2002-09-27	2008-11-17	Granted	Korea, Republic of (KR)	Method And Structure For Oxide/Silicon Nitride Interface Substructure Improvements
091122325	NI-190044	2002-09-27	2003-11-11	Granted	Taiwan	Method And Structure For Oxide/Silicon Nitride Interface Substructure Improvements
10061475	6767797	2002-02-01	2004-07-27	Granted	United States of America	Method Of Fabricating Complementary Self-Aligned Bipolar Transistors
09964227	6764930	2001-09-26	2004-07-20	Granted	United States of America	Method And Structure For Modular, Highly Linear MOS Capacitors Using Nitrogen Implantation
09689030	6544907	2000-10-12	2003-04-08	Granted	United States of America	A Method Of Forming A High Quality Gate Oxide Layer Having A Uniform Thickness

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09833251	6458696	2001-04-11	2002-10-01	Granted	United States of America	Plated Through Hole Interconnections
09968243	6607927	2001-09-28	2003-08-19	Granted	United States of America	Method And Apparatus For Monitoring In-Line Copper Contamination
10051937	6555852	2002-01-17	2003-04-29	Granted	United States of America	Bipolar Transistor Having An Emitter Comprised Of A Semi-Insulating Material
09727195	6432814	2000-11-30	2002-08-13	Granted	United States of America	Method Of Manufacturing An Interconnect Structure Having A Passivation Layer For Preventing Subsequent Processing Reactions
10038371	6879046	2002-01-02	2005-04-12	Granted	United States of America	Split Barrier Layer Including Nitrogen-Containing Portion And Oxygen-Containing Portion
06003727	2422721	2002-12-03	2006-09-13	Lapsed	United Kingdom	Split Barrier Layer Including Nitrogen-Containing Portion And Oxygen-Containing Portion
06003743	2422722	2002-12-03	2006-09-13	Lapsed	United Kingdom	Split Barrier Layer Including Nitrogen-Containing Portion And Oxygen-Containing Portion
1020030000063	759721	2003-01-02	2007-09-12	Granted	Korea, Republic of (KR)	Split Barrier Layer Including Nitrogen-Containing Portion And Oxygen-Containing Portion
02281962	2387027	2002-12-03	2006-07-12	Lapsed	United Kingdom	Split Barrier Layer Including Nitrogen-Containing Portion And Oxygen-Containing Portion
2002376124	4422403	2002-12-26	2009-12-11	Granted	Japan	Split Barrier Layer Including Nitrogen-Containing Portion And Oxygen-Containing Portion
091135431	I281224	2002-12-06	2007-05-11	Granted	Taiwan	Split Barrier Layer Including Nitrogen-Containing Portion And Oxygen-Containing Portion
09863437	6610464	2001-05-24	2003-08-26	Granted	United States of America	Process For Patterning A Membrane
09853317	6605529	2001-05-11	2003-08-12	Lapsed	United States of America	Method Of Creating Hydrogen Isotope Reservoirs In A Semiconductor Device
09636447	6426263	2000-08-11	2002-07-30	Granted	United States of America	A Method For Making A Merged Contact Window In A Transistor To Electrically Connect The Gate To Either The Source Or The Drain
10259256	6730600	2002-09-27	2004-05-04	Granted	United States of America	Method Of Dry Etching A Semiconductor Device In The Absence Of A Plasma
09767477	6750528	2001-01-23	2004-06-15	Granted	United States of America	Bipolar Device
09887938	6716488	2001-06-22	2004-04-06	Granted	United States of America	Ferrite Film Formation Method And Apparatus
1020020081092	10-927808	2002-12-18	2009-11-13	Granted	Korea, Republic of (KR)	Polysilicon Bounded Snapback Device
021571988	02157198.8	2002-12-19	2007-11-28	Granted	China	Polysilicon Bounded Snapback Device
02294486	2387271	2002-12-18	2005-09-28	Lapsed	United Kingdom	Polysilicon Bounded Snapback Device
2002368138	4477298	2002-12-19	2010-03-19	Lapsed	Japan	Polysilicon Bounded Snapback Device
10024803	6534834	2001-12-19	2003-03-18	Granted	United States of America	Polysilicon Bounded Snapback Device
091136669	I255028	2002-12-19	2006-05-11	Lapsed	Taiwan	Polysilicon Bounded Snapback Device
09878690	6506673	2001-06-11	2003-01-14	Granted	United States of America	Method Of Forming A Reverse Gate Structure With A Spin On Glass Process

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10061542	6730603	2001-10-25	2004-05-04	Granted	United States of America	System And Method Of Determining A Polishing Endpoint By Monitoring Signal Intensity
09631545	6627885	2000-08-03	2003-09-30	Granted	United States of America	A Method Of Focused Ion Beam Pattern Transfer Using A Smart Dynamic Template
09902358	6511872	2001-07-10	2003-01-28	Granted	United States of America	Device Having A High Dielectric Constant Material And A Method Of Manufacture Thereof
09541792	6508363	2000-03-31	2003-01-21	Granted	United States of America	Slurry Container
10259254	6972083	2002-09-27	2005-12-06	Lapsed	United States of America	Electrochemical Method And System For Monitoring Hydrogen Peroxide Concentration In Slurries
09882911	6864547	2001-06-15	2005-03-08	Lapsed	United States of America	Semiconductor Device Having A Ghost Source/Drain Region And A Method Of Manufacture Therefor
09564659	6402599	2000-05-03	2002-06-11	Granted	United States of America	Slurry Recirculation System For Reduced Slurry Drying
09634021	6448581	2000-08-08	2002-09-10	Granted	United States of America	Mitigation Of Deleterious Effects Of Micropipes In Silicon Carbide Devices
09756965	6664800	2001-01-08	2003-12-16	Granted	United States of America	Non-Contact Method For Determining Quality Of Semiconductor Dielectrics
09634401	6475842	2000-08-09	2002-11-05	Granted	United States of America	Novel Process For Gate Oxide Side-Wall Protection From Plasma Damage To Form Highly Reliable Gate Dielectrics
09967435	6641746	2001-09-28	2003-11-04	Granted	United States of America	Control Of Semiconductor Processing
09488899	6471925	2000-01-21	2002-10-29	Granted	United States of America	Method For Treating An Effluent Gas During Semiconductor Processing
09521268	6274490	2000-03-08	2001-08-14	Granted	United States of America	High Pressure Anneal For Semiconductor Devices
09419259	6340327	1999-10-15	2002-01-22	Granted	United States of America	Wafer Polishing Apparatus And Process
09567373	6519542	2000-05-09	2003-02-11	Granted	United States of America	Method Of Testing An Unknown Sample With An Analytical Tool
09567359	6519543	2000-05-09	2003-02-11	Granted	United States of America	Calibration Method For Quantitative Elemental Analysis
09578894	6716657	2000-05-26	2004-04-06	Granted	United States of America	Method For Interconnecting Arrays Of Micromechanical Devices
09419453	6250991	1999-10-15	2001-06-26	Granted	United States of America	Bearing Substitute For Wafer Polishing Arm
09755826	7927939	2001-01-04	2011-04-19	Granted	United States of America	Method of Manufacturing a Laterally Diffused Metal Oxide Semiconductor Device
12555082	7927940	2009-09-08	2011-04-19	Granted	United States of America	Method of Manufacturing a Laterally Diffused Metal Oxide Semiconductor Device
09733570	6576522	2000-12-08	2003-06-10	Granted	United States of America	Methods For Deuterium Sintering
003086840	1091416	2000-10-03	2008-12-31	Lapsed	United Kingdom	GaAs MOSFET Having Low Capacitance and On-Resistance And Method Of Manufacturing The Same
003086840	1091416	2000-10-03	2008-12-31	Lapsed	France	GaAs MOSFET Having Low Capacitance and On-Resistance And Method Of Manufacturing The Same
09927194	6682962	2001-08-10	2004-01-27	Lapsed	United States of America	GaAs MOSFET Having Low Capacitance and On\(miResistance And Method Of Manufacturing The Same

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
003086840	60041233.4	2000-10-03	2008-12-31	Lapsed	Germany (Federal Republic of)	GaAs MOSFET Having Low Capacitance and On-Resistance And Method Of Manufacturing The Same
09412847	6369408	1999-10-06	2002-04-09	Granted	United States of America	GaAs MOSFET Having Low Capacitance and On-Resistance And Method Of Manufacturing The Same
2000307041	4558911	2000-10-06	2010-07-30	Lapsed	Japan	GaAs MOSFET Having Low Capacitance and On-Resistance And Method Of Manufacturing The Same
09397459	6406999	1999-09-16	2002-06-18	Granted	United States of America	A Semicondutor Device Having Reduced Line Width Variations Between Tightly Spaced And Isolated Features
09397458	6395639	1999-09-16	2002-05-28	Granted	United States of America	A Process For Improving Line Width Variations Between Tightly Spaced And Isolated Features In Integrated Circuits
09465633	6524971	1999-12-17	2003-02-25	Granted	United States of America	A Method Of Deposition Of Films
09413149	6324933	1999-10-06	2001-12-04	Granted	United States of America	Planar Movable Stage Mechanism
09667046	6989602	2000-09-21	2006-01-24	Granted	United States of America	Dual Damascene Process With No Passing Metal Features
09430316	6403454	1999-10-29	2002-06-11	Granted	United States of America	Silicon Semiconductor Devices With ä-Doped Layers
09727014	6633032	2000-11-30	2003-10-14	Granted	United States of America	Mass Spectrometer Particle Counter
09589816	6313007	2000-06-07	2001-11-06	Granted	United States of America	Semiconductor Device, Trench Isolation Structure And Methods Of Format Ion
09418078		1999-10-14		Abandoned	United States of America	Method For Chemical Mechanical Polishing Endpoint Detection Using A Hydrogen Sensor
09418087	6293847	1999-10-14	2001-09-25	Granted	United States of America	Apparatus For Chemical Mechanical Polishing Endpoint Detection Using A Hydrogen Sensor
09516836	6368200	2000-03-02	2002-04-09	Granted	United States of America	Polishing Pads From Closed\(miCelled Elastomer Foam
09633241	6410419	2000-08-07	2002-06-25	Granted	United States of America	Silicon Carbide Barrier Layers For Porous Low Dielectric Constant Materials
09553938	6354928	2000-04-21	2002-03-12	Granted	United States of America	Polishing Apparatus With Carrier Ring And Carrier Head Employing Like Polarities
09504306	6358807	2000-02-15	2002-03-19	Granted	United States of America	Bipolar Semiconductor Device And Method Of Forming Same Having Reduced Transient Enhanced Diffusion
09384769	6140170	1999-08-27	2000-10-31	Granted	United States of America	Manufacture Of Complementary MOS And Bipolar Integrated Circuits
09276034	6169036	1999-03-25	2001-01-02	Granted	United States of America	Method For Cleaning Via Openings In Integrated Circuit Manufacturing
09604020	6593151	2000-06-26	2003-07-15	Lapsed	United States of America	Method For Regular Detection Of Phosphorus Striations In A Multi\(miLayered Film Stack

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09431198	6214732	1999-11-01	2001-04-10	Granted	United States of America	Chemical Mechanical Polishing Endpoint Detection By Monitoring Component Activity In Effluent Slurry
09432721	6258231	1999-11-01	2001-07-10	Granted	United States of America	Chemical Mechanical Polishing Endpoint Apparatus Using Component Activity In Effluent Slurry
09366362	6299519	1999-08-03	2001-10-09	Granted	United States of America	Apparatus And Method For Removing A Polishing Pad From A Platen
09338735	6114234	1999-06-23	2000-09-05	Granted	United States of America	Method Of Making A Semiconductor With Copper Passivating Film
09172456	6228277	1998-10-14	2001-05-08	Granted	United States of America	Etch Endpoint Detection
09349538	6444536	1999-07-08	2002-09-03	Granted	United States of America	Method For Fabricating Bipolar Transistors
09337966	6362475	1999-06-22	2002-03-26	Granted	United States of America	Scanning Electron Microscope\(slEnergy Dispersive Spectroscopy Sample Preparation Method And Sample Produced Thereby
09197412	6146909	1998-11-21	2000-11-14	Granted	United States of America	Detecting Trace Levels Of Copper
09353860	6097484	1999-07-15	2000-08-01	Granted	United States of America	Location Of Defects Using Dye Penetration
09426124	6682999	1999-10-22	2004-01-27	Lapsed	United States of America	Semiconductor Device Having Multilevel Interconnections And Method Of Manufacture Thereof
09327793	6124158	1999-06-08	2000-09-26	Granted	United States of America	Method of Reducing Carbon Contamination of a Thin Dielectric Film by Using Gaseous Organic Precursors, Inert Gas, and Ozone to React with Carbon Contaminants
09684015	6251697	2000-10-06	2001-06-26	Granted	United States of America	A Non-Contact Method For Monitoring And Controlling Plasma Charging Damage In A Semiconductor Device
09441676	6331460	1999-11-17	2001-12-18	Granted	United States of America	A Method Of Fabricating A MOM Capacitor Having A Metal Silicide Barrier
09441561	6335557	1999-11-17	2002-01-01	Granted	United States of America	Metal Silicide As A Barrier For MOM Capacitors In CMOS Technologies
09325624		1999-06-03		Abandoned	United States of America	Tungsten Silicide Nitride As A Barrier For High Temperature Anneals To Improve Hot Carrier Reliability
09324946	6365511	1999-06-03	2002-04-02	Granted	United States of America	Tungsten Silicide Nitride As A Barrier For High Temperature Anneals To Improve Hot Carrier Reliability
09088852	6097195	1998-06-02	2000-08-01	Granted	United States of America	Methods And Apparatus For Increasing Metal Density In An Integrated CircuitWhile Also Reducing Parasitic Capacitance
09081406	6056630	1998-05-19	2000-05-02	Granted	United States of America	Polishing Apparatus With Carrier Head Pivoting Device
09082162	6083838	1998-05-20	2000-07-04	Granted	United States of America	Method Of Planarizing A Surface On A Semiconductor Wafer
09205414	6140187	1998-12-02	2000-10-31	Granted	United States of America	Device And In Situ Furnace Gate Stack Process For Metal Oxide Semiconductors

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09099827	6075273	1998-06-18	2000-06-13	Granted	United States of America	Integrated Circuit Device In Which Gate Oxide Thickness Is Selected To Control Plasma Damage During Device Fabrication
09028966	5932379	1998-02-24	1999-08-03	Granted	United States of America	Repairing Fractured Wafers In Semiconductor Manufacturing
09196486	6149778	1998-11-19	2000-11-21	Granted	United States of America	Article Comprising Fluorinated Amorphous Carbon And Process For Fabricating Article
09059359	6156665	1998-04-13	2000-12-05	Granted	United States of America	Trilayer Lift-Off Process For Semiconductor Device Metalization
09053908	6073476	1998-04-02	2000-06-13	Granted	United States of America	Calibration Sample For Particle Analyzers And Method For Making Same
09218574	6410986	1998-12-22	2002-06-25	Granted	United States of America	Multi\(miLayered Titanium Nitride Barrier Structure
09138741	6121624	1998-08-24	2000-09-19	Granted	United States of America	Method for Controlled Implantation Of Elements Into The Surface Or Near Surface Of A Substrate
08922487	6004827	1997-09-03	1999-12-21	Expired	United States of America	Integrated Circuit Processing
09352674	6251486	1999-07-11	2001-06-26	Expired	United States of America	Method For Fabricating An Article Comprising A Ladder Siloxane Polymer AndResultant Article
08868269	5844261	1997-06-03	1998-12-01	Expired	United States of America	InAlGaP Devices
09369105	6153078	1999-08-05	2000-11-28	Granted	United States of America	Process For Forming Device Comprising Metallized Magnetic Substrates
09069215	6303961	1998-04-29	2001-10-16	Granted	United States of America	Improved Complementary Semiconductor Devices
08869944	5856008	1997-06-05	1999-01-05	Expired	United States of America	Article Comprising Magnetoresistive Material
09056555	6576521	1998-04-07	2003-06-10	Granted	United States of America	Method Of Forming Semiconductor Device With LDD Structures
08807310	5756887	1997-02-27	1998-05-26	Expired	United States of America	Mechanism For Changing A Probe Balance Beam In A Scanning Probe Microscope
08871383	5945355	1997-06-09	1999-08-31	Expired	United States of America	Integrated Circuit Fabrication
08760845	5746931	1996-12-05	1998-05-05	Expired	United States of America	Method And Apparatus For Chemical-Mechanical Polishing Of Diamond
08898261	5877407	1997-07-22	1999-03-02	Expired	United States of America	Plasma Etch Endpoint Detection Process
08798327	5939742	1997-02-10	1999-08-17	Expired	United States of America	Field-Effect Photo-Transistor
08657255	5625206	1996-06-03	1997-04-29	Expired	United States of America	High-Speed Double-Heterostructure Bipolar Transistor Devices
08846967	5969337	1997-04-29	1999-10-19	Expired	United States of America	Integrated Photosensing Device For Active Pixel Sensor Imagers
08814817	5793093	1997-03-11	1998-08-11	Expired	United States of America	Substrate Isolation For Analog/Digital IC Chips
08778123	6018272	1997-01-02	2000-01-25	Expired	United States of America	Linearization Of Resistance
08782010	6153452	1997-01-07	2000-11-28	Expired	United States of America	Method Of Manufacturing Semiconductor Devices Having Improved Polycide Integrity Through Introduction Of A Silicon Layer Within The Polycide Structure
08509267	5664884	1995-07-31	1997-09-09	Expired	United States of America	Apparatus For Determining The Thermal Resistivity Of Electrically Insulating Crystalline Materials
08511845	5670391	1995-08-07	1997-09-23	Expired	United States of America	Process For Reducing Transient Diffusion Of Dopant Atoms
08819828	6013934	1997-03-18	2000-01-11	Expired	United States of America	Semiconductor Structure For Thermal Shutdown Protection

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08917955	5930587	1997-08-27	1999-07-27	Expired	United States of America	Stress Migration Evaluation Method
08516368	5596413	1995-08-17	1997-01-21	Expired	United States of America	Sub-Micron Through-the-Lens Positioning utilizing out of phase segmented gratings
08569025	5686359	1995-12-07	1997-11-11	Expired	United States of America	Titanium Silicide Process
08553118	5654903	1995-11-07	1997-08-05	Expired	United States of America	A Method and Apparatus for Real Time Monitoring of Wafer Attributes in a Plasma Etch Process
08789892	5700725	1997-01-29	1997-12-23	Expired	United States of America	Apparatus And Method For Making Integrated Circuits
08550879	5636002	1995-10-31	1997-06-03	Expired	United States of America	Auxiliary Mask Features For Enhancing The Resolution Of Photolithography
08454976	5866436	1995-05-31	1999-02-02	Expired	United States of America	Process Of Manufacturing An Integrated Circuit Having An Interferometrically Profiled Mounting Film
08397346	5721445	1995-03-02	1998-02-24	Expired	United States of America	Semiconductor Device With Increased Parasitic Emitter Resistance And Improved Latch-Up Immunity
08939422	6168904	1997-09-29	2001-01-02	Expired	United States of America	Integrated Circuit Fabrication
08287989	5500391	1994-08-09	1996-03-19	Expired	United States of America	Method For Making A Semiconductor Device Including Diffusion Control
08431341	5607543	1995-04-28	1997-03-04	Expired	United States of America	Integrated Circuit Etching

Schedule B(1)(c) – Semic Packaging

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09045062	6103615	1998-03-19	2000-08-15	Granted	United States of America	Corrosion sensitivity structures for vias and contact holes in integrated circuits
09464225	6278129	1999-12-15	2001-08-21	Granted	United States of America	Corrosion sensitivity structures for vias and contact holes in integrated circuits
08771955	5776551	1996-12-23	1998-07-07	Expired	United States of America	Use of plasma activated NF3 to clean solder bumps on a device
08922141	5786073	1997-08-29	1998-07-28	Expired	United States of America	Integrated circuit comprising solder bumps
08904530	5911112	1997-08-01	1999-06-08	Expired	United States of America	Method for forming electrical connections between a semiconductor die and a semiconductor package
08608679	5793104	1996-02-29	1998-08-11	Expired	United States of America	Apparatus for forming electrical connections between a semiconductor die and a semiconductor package
08936829	5970321	1997-09-25	1999-10-19	Expired	United States of America	Method of fabricating a microelectronic package having polymer ESD protection
08595021	5869869	1996-01-31	1999-02-09	Expired	United States of America	Microelectronic device with thin film electrostatic discharge protection structure
08723140	5955762	1996-10-01	1999-09-21	Expired	United States of America	Microelectronic package with polymer ESD protection
08909312	5885855	1997-08-14	1999-03-23	Expired	United States of America	Method for distributing connection pads on a semiconductor die
08747325	5952726	1996-11-12	1999-09-14	Expired	United States of America	Flip chip bump distribution on die
08989098		1997-12-11		Abandoned	United States of America	Integrated Circuit Package.
08648350	5700723	1996-05-15	1997-12-23	Expired	United States of America	Method of packaging an integrated circuit
08810304		1997-02-28		Abandoned	United States of America	Microelectronioc Integrated Circuit Mounted On Circuit Board With Solder Column Grid Array Interconnection (As Amended)
08595022	5639696	1996-01-31	1997-06-17	Expired	United States of America	Microelectronic integrated circuit mounted on circuit board with solder column grid array interconnection, and method of fabricating the solder column grid array
08778909	5784780	1997-01-03	1998-07-28	Expired	United States of America	Method of mounting a flip-chip
08538631	5637920	1995-10-04	1997-06-10	Expired	United States of America	High contact density ball grid array package for flip-chips
08653591		1996-05-24		Abandoned	United States of America	Powdered Metal Heat Sink With Increased Surface Area

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08578966	5814536	1995-12-27	1998-09-29	Expired	United States of America	Method of manufacturing powdered metal heat sinks having increased surface area
08854780	5869891	1997-05-12	1999-02-09	Expired	United States of America	Powdered Metal Heat Sink With Increased Surface Area
08718852	5827777	1996-09-24	1998-10-27	Expired	United States of America	Method of making a barrier metal technology for tungsten plug interconnection
08378027	5600182	1995-01-24	1997-02-04	Expired	United States of America	Barrier metal technology for tungsten plug interconnection
08916025	5872026	1997-08-21	1999-02-16	Expired	United States of America	Process of Fabricating An Integrated Circuit Die Package Having a Plurality of Pins
08485060	5739584	1995-06-07	1998-04-14	Expired	United States of America	Multiple pin die package
10306064	6597189	2002-11-27	2003-07-22	Granted	United States of America	Socketless/boardless test interposer card
11324119	RE41516	2005-12-30	2010-08-17	Lapsed	United States of America	Socketless/Boardless Test Interposer Card
10428200	6771085	2003-04-30	2004-08-03	Lapsed	United States of America	Socketless/boardless test interposer card
07856905		1992-05-14		Abandoned	United States of America	Encapsulation Of Electronic Components
08331251	5537342	1994-10-28	1996-07-16	Expired	United States of America	Encapsulation of electronic components
08484177	5663872	1995-06-07	1997-09-02	Expired	United States of America	Encapsulation of electronic components
11277188	8049340	2006-03-22	2011-11-01	Granted	United States of America	Device For Avoiding Parasitic Capacitance in an Integrated Circuit Package
13252632	8288269	2011-10-04	2012-10-16	Granted	United States of America	Methods for Avoiding Parasitic Capacitance in an Integrated Circuit Package
14045081		2013-10-03		Abandoned	United States of America	Alternate Pad Structures/Passivation Integration Schemes to Reduce or Eliminate IMC Cracking in Post Wire Bonded Dies During Cu/Low-K BEOL Processing
11283219	8552560	2005-11-18	2013-10-08	Granted	United States of America	Alternate Pad Structures/Passivation Integration Schemes to Reduce or Eliminate IMC Cracking in Post Wire Bonded Dies During Cu/Low-K BEOL Processing
11964920	7565592	2007-12-27	2009-07-21	Lapsed	United States of America	Failure Analysis and Testing of Semi-Conductor Devices Using Intelligent Software on Automated Test Equipment (ATE)

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11670031	7430700	2007-02-01	2008-09-30	Granted	United States of America	Failure analysis and testing of semi-conductor devices using intelligent software on automated test equipment (ATE)
11028695	7203877	2005-01-04	2007-04-10	Granted	United States of America	Failure analysis and testing of semi-conductor devices using intelligent software on automated test equipment (ATE)
12253403	7960812	2008-10-17	2011-06-14	Granted	United States of America	Electrical Devices Having Adjustable Capacitance
10746824	7456716	2003-12-24	2008-11-25	Granted	United States of America	Electrical Devices Having Adjustable Electrical Characteristics
10926631	7109589	2004-08-26	2006-09-19	Granted	United States of America	Integrated Circuit With Substantially Perpendicular Wire Bonds
11494221	7465655	2006-07-27	2008-12-16	Granted	United States of America	Integrated Circuit With Substantially Perpendicular Wire Bonds
09162247	6087732	1998-09-28	2000-07-11	Granted	United States of America	Bond Pad For A Flip Chip Package, And Method Of Forming The Same
09503814	6187658	2000-02-15	2001-02-13	Granted	United States of America	Bond Pad For A Flip Chip Package, And Method Of Forming The Same
10921497		2004-08-18		Abandoned	United States of America	Multi-Level Redistribution Layer Traces for Reducing Current Crowding in FlipChip Solder Bumps
10327333	6818996	2002-12-20	2004-11-16	Granted	United States of America	Multi-level redistribution layer traces for reducing current crowding in flipchip solder bumps
09489302	6369448	2000-01-21	2002-04-09	Granted	United States of America	Vertically integrated flip chip semiconductor package
09993466	6558978	2001-11-05	2003-05-06	Granted	United States of America	Chip-over-chip integrated circuit package
11015534	7224047	2004-12-18	2007-05-29	Granted	United States of America	Semiconductor Device Package With Reduced Leakage
11788346	7541669	2007-04-19	2009-06-02	Granted	United States of America	Semiconductor Device Package With Base Features to Reduce Leakage
09642216	6319617	2000-08-18	2001-11-20	Granted	United States of America	Oxide-Bondable Solder
09466449	6306516	1999-12-17	2001-10-23	Granted	United States of America	Article Comprising Oxide-Bondable Solder
09006356	6064113	1998-01-13	2000-05-16	Granted	United States of America	Semiconductor device package including a substrate having bonding fingers within an electrically conductive ring surrounding a die area and a combined power and ground plane to stabilize signal path impedances
09428164	6137168	1999-10-27	2000-10-24	Granted	United States of America	Semiconductor package with traces routed underneath a die

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09618143		2000-07-17		Abandoned	United States of America	Semiconductor Package With Traces Routed Underneath A Die
08901489	5885848	1997-07-28	1999-03-23	Expired	United States of America	Ball Grid Array Package With Inexpensive Threaded Secure Locking Mechanism To Allow Removal Of A Threaded Heat Sink Therefrom
08724076	5789813	1996-09-30	1998-08-04	Expired	United States of America	Ball grid array package with inexpensive threaded secure locking mechanism to allow removal of a threaded heat sink therefrom
08427674		1995-04-24		Abandoned	United States of America	Electronic System Including Packaged Integrated Circuits With Heat Spreading Stand-Off Support Members
08323817	5673479	1994-10-17	1997-10-07	Expired	United States of America	Method For Mounting A Microelectronic Circuit Peripherally-Leaded Package Including Integral Support Member With Spacer
08646014		1996-05-07		Abandoned	United States of America	Microelectronic Circuit Structure
08427306		1995-04-24		Abandoned	United States of America	Location And Standoff Pins For Chip On Tape
08170102	5410451	1993-12-20	1995-04-25	Expired	United States of America	Location And Standoff Pins For Chip On Tape
08710573	5898575	1996-09-19	1999-04-27	Expired	United States of America	Support Assembly For Mounting An Integrated Circuit Package On A Surface
08713174	5896651	1996-09-12	1999-04-27	Expired	United States of America	Method For Mounting A Microelectronic Circuit Package
08646037	5923538	1996-05-07	1999-07-13	Expired	United States of America	Support member for mounting a microelectronic circuit package
08903241	6008991	1997-07-24	1999-12-28	Expired	United States of America	Electronic system including packaged integrated circuits with heat spreading standoff support members
12139185	7919354	2008-06-13	2011-04-05	Granted	United States of America	Asymmetric Alignment of Substrate Interconnect to Semiconductor Die
11260334	7405476	2005-10-27	2008-07-29	Granted	United States of America	Asymmetric alignment of substrate interconnect to semiconductor die
09802424	6518193	2001-03-09	2003-02-11	Granted	United States of America	Substrate processing system
10322974		2002-12-18		Abandoned	United States of America	Substrate Processing System
08424828	6313519	1995-04-19	2001-11-06	Granted	United States of America	Support for semiconductor bond wires

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
07914621		1992-07-15		Abandoned	United States of America	Support For Semiconductor Bond Wires
08506164	5744084	1995-07-24	1998-04-28	Expired	United States of America	Method of improving molding of an overmolded package body on a substrate
08920430	5927505	1997-08-29	1999-07-27	Expired	United States of America	Overmolded package body on a substrate
10007247	6678950	2001-11-01	2004-01-20	Granted	United States of America	Method for forming a bonding pad on a substrate
10694486		2003-10-27		Abandoned	United States of America	Bonding Pad Design
08908404	5990543	1997-08-07	1999-11-23	Expired	United States of America	Reframed chip-on-tape die
08635288	6043100	1996-04-19	2000-03-28	Expired	United States of America	Chip on tape die reframe process
09477306	6492253	2000-01-04	2002-12-10	Granted	United States of America	Method for programming a substrate for array-type packages
09006584	6054767	1998-01-13	2000-04-25	Granted	United States of America	Programmable substrate for array-type packages
12174479	7829424	2008-07-16	2010-11-09	Lapsed	United States of America	Package Configuration And Manufacturing Method Enabling The Addition Of Decoupling Capacitors To Standard Package Designs
11078052	7508062	2005-03-11	2009-03-24	Lapsed	United States of America	Package Configuration And Manufacturing Method Enabling The Addition Of Decoupling Capacitors To Standard Package Designs
07935449	5300815	1992-08-25	1994-04-05	Expired	United States of America	Technique of increasing bond pad density on a semiconductor die
08430399	5635424	1995-04-28	1997-06-03	Expired	United States of America	High-density bond pad layout arrangements for semiconductor dies, and connecting to the bond pads
08688148		1996-07-29		Abandoned	United States of America	Overmolded Semiconductor Package
07975185	5399898	1992-11-12	1995-03-21	Expired	United States of America	Multi-chip semiconductor arrangements using flip chip dies
08270123		1994-07-01		Abandoned	United States of America	Semiconductor Packaging Technique Yielding Increased Inner Lead Count For A Given Die-Receiving Area
08015947		1993-02-10		Abandoned	United States of America	Floorplanning Techniques Using Multi-Partitioning Based On A Partitions Cost Factor For Non-Square Shaped Partitions
07938690		1992-09-01		Abandoned	United States of America	Ball Bump Array Semiconductor Packages

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
07400572		1989-08-28		Abandoned	United States of America	Method And Apparatus For Isolation Of Flux Materials In Flip-Chip Manufacturing
08105547	5504035	1993-08-12	1996-04-02	Expired	United States of America	Process for solder ball interconnecting a semiconductor device to a substrate using a noble metal foil embedded interposer substrate
08105269		1993-08-12		Abandoned	United States of America	Optically Transmissive Preformed Planar Structures
08679949	5834799	1996-07-15	1998-11-10	Expired	United States of America	Optically transmissive preformed planar structures
07917894		1992-07-21		Abandoned	United States of America	Ball Bump Array Semiconductor Packages
08382147		1995-02-01		Abandoned	United States of America	Ball Bump Array Semiconductor Packages
07947854	5248903	1992-09-18	1993-09-28	Expired	United States of America	Composite bond pads for semiconductor devices
07984206	5284797	1992-11-30	1994-02-08	Expired	United States of America	Semiconductor bond pads
08387154	5565385	1995-02-10	1996-10-15	Expired	United States of America	Semiconductor bond pad structure and increased bond pad count per die
08470945	5821624	1995-06-05	1998-10-13	Expired	United States of America	Semiconductor device assembly techniques using preformed planar structures
07993188		1992-12-18		Abandoned	United States of America	Mounting And Connecting Non-Square Semiconductor Dies
08476431	5744856	1900-01-01	1998-04-28	Expired	United States of America	Non-Square Die For Integrated Circuit And Systems Containing The Same
08194241	5410805	1994-02-10	1995-05-02	Expired	United States of America	Method And Apparatus For Isolation Of Flux Materials In Flip-Chip Manufacturing
08079499	5434750	1993-06-18	1995-07-18	Expired	United States of America	Partially-Molded, Pcb Chip Carrier Package For Certain Non-Square Die Shapes
08720219	5744858	1996-09-26	1998-04-28	Expired	United States of America	Semiconductor packaging technique yielding increased inner lead count for a given die-receiving area
07969862		1992-10-28		Abandoned	United States of America	Overmolded Semiconductor Package
08331263		1994-10-28		Abandoned	United States of America	Overmolded Semiconductor Package
08429605	5557150	1995-04-27	1996-09-17	Expired	United States of America	Overmolded semiconductor package

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
07981096	5299730	1992-11-24	1994-04-05	Expired	United States of America	Method and apparatus for isolation of flux materials in flip-chip manufacturing
07775009	5168346	1991-10-11	1992-12-01	Expired	United States of America	Method and apparatus for isolation of flux materials in flip-chip manufacturing
08428323	5569963	1995-04-25	1996-10-29	Expired	United States of America	Preformed planar structures for semiconductor device assemblies
08105838	5347162	1993-08-12	1994-09-13	Expired	United States of America	Preformed planar structures employing embedded conductors
08432535	5594626	1995-05-02	1997-01-14	Expired	United States of America	Partially-molded, PCB chip carrier package for certain non-square die shapes
07916328	5340772	1992-07-17	1994-08-23	Expired	United States of America	Method of increasing the layout efficiency of dies on a wafer and increasing the ratio of I/O area to active area per die
07978483	5341024	1992-11-18	1994-08-23	Expired	United States of America	Method of increasing the layout efficiency of dies on a wafer, and increasing the ratio of I/O area to active area per die
08664146	5729894	1996-06-14	1998-03-24	Expired	United States of America	Method of assembling ball bump grid array semiconductor packages
07933430	5329157	1992-08-21	1994-07-12	Expired	United States of America	Semiconductor packaging technique yielding increased inner lead count for a given die-receiving area
08251058	5441917	1994-05-31	1995-08-15	Expired	United States of America	Method of laying out bond pads on a semiconductor die
08416457	5532934	1995-04-03	1996-07-02	Expired	United States of America	Floorplanning technique using multi-partitioning based on a partition cost factor for non-square shaped partitions
07576182	5111279	1990-08-30	1992-05-05	Expired	United States of America	Apparatus for isolation of flux materials in flip-chip manufacturing
08106157	5489804	1993-08-12	1996-02-06	Expired	United States of America	Flexible preformed planar structures for interposing between a chip and a substrate
07995644	5404047	1992-12-18	1995-04-04	Expired	United States of America	Semiconductor die having a high density array of composite bond pads
07834182	5262927	1992-02-07	1993-11-16	Expired	United States of America	Partially-molded, PCB chip carrier package
08260078	5468681	1994-06-15	1995-11-21	Expired	United States of America	Process for interconnecting conductive substrates using an interposer having conductive plastic filled vias
13934110		2013-07-02		Abandoned	United States of America	Contact Support Pillar Structure for Flip Chip Semiconductor Devices and Method Of Manufacture Therefore
13093032	8507317	2011-04-25	2013-08-13	Granted	United States of America	Solder Bump Structure For Flip Chip Semiconductor Devices And Method Of Manufacturing Therefore

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11459249	7952206	2006-07-21	2011-05-31	Granted	United States of America	Solder Bump Structure For Flip Chip Semiconductor Devices And Method Of Manufacture Therefore
08259439		1994-06-14		Abandoned	United States of America	Techniques For Isolating Superconducting Substrates From Heat Generated By Semiconductor Devices
08434276	5700715	1995-05-03	1997-12-23	Expired	United States of America	Process for mounting a semiconductor device to a circuit substrate
11131885	7053639	2005-05-18	2006-05-30	Granted	United States of America	Probing fixture for semiconductor wafer
09731596	6927079	2000-12-06	2005-08-09	Granted	United States of America	Method for probing a semiconductor wafer
11506680	7456498	2006-08-18	2008-11-25	Granted	United States of America	Integrated circuit package and system interface
12283820	7550839	2008-09-15	2009-06-23	Granted	United States of America	Integrated Circuit Package and System Interface
61055505		2008-05-23		Expired	United States of America	Solution For Package Cross Talk Minimization
12469985	8324019	2009-05-21	2012-12-04	Granted	United States of America	Solution For Package Cross Talk Minimization
10930590	8404960	2004-08-31	2013-03-26	Granted	United States of America	Method for Heat Dissipation on Semiconductor Device
13775922	8653357	2013-02-25	2014-02-18	Lapsed	United States of America	Method for Heat Dissipation on Semiconductor Device
12337519	8258016	2008-12-17	2012-09-04	Granted	United States of America	Semiconductor Package Having Increased Resistance to Electrostatic Discharge
11304862	7498664	2005-12-14	2009-03-03	Granted	United States of America	Semiconductor Package Having Increased Resistance to Electrostatic Discharge
11399723	7646091	2006-04-06	2010-01-12	Granted	United States of America	Semiconductor Package and Method Using Isolated VSS Plane to Accomodate High Speed Circuitry Ground Isolation
12625457	8129759	2009-11-24	2012-03-06	Granted	United States of America	Semiconductor Package and Method Using Isolated VSS Plane to Accomodate High Speed Circuitry Ground Isolation
10951430		2004-09-28		Abandoned	United States of America	Whisker-Free Lead Frames
12462069	8013428	2009-07-28	2011-09-06	Granted	United States of America	Whisker-Free Lead Frames
10979491	7352062	2004-11-02	2008-04-01	Granted	United States of America	Integrated circuit package design
10271003	6825556	2002-10-15	2004-11-30	Granted	United States of America	Integrated circuit package design with non-orthogonal die cut out

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
12160553	8242378	2008-07-10	2012-08-14	Granted	United States of America	Soldering Method and Related Device for Improved Resistance to Brittle Fracture With An Intermetallic Compound Region Coupling A solder Mass to an NI Layer Which has a low Concentration of P, wherein the amount of P in the underlying NI layer is controlled as a function of the expected volume of the solder mass
13552266		2012-07-18		Abandoned	United States of America	Soldering Method and Related Device for Improved Resistance to Brittle Fracture
11469960	8319343	2006-09-05	2012-11-27	Granted	United States of America	Routing Under Bond Pad For The Replacement Of An Interconnect Layer
13656092		2012-10-19		Abandoned	United States of America	Routing Under Bond Pad For The Replacement Of An Interconnect Layer
10642706	6991147	2003-08-18	2006-01-31	Lapsed	United States of America	Insulated bonding wire tool for microelectronic packaging
09687263	6670214	2000-10-12	2003-12-30	Lapsed	United States of America	Insulated bonding wire for microelectronic packaging
10638772	6858930	2003-08-11	2005-02-22	Granted	United States of America	Multi chip module
10265751	6680532	2002-10-07	2004-01-20	Lapsed	United States of America	Multi chip module
12692209	8084857	2010-01-22	2011-12-27	Granted	United States of America	Method and Article of Manufacture for Wire Bonding with Staggered Differential Wire Bond Pairs
11065838	7675168	2005-02-25	2010-03-09	Granted	United States of America	Integrated Circuit With Staggered Differential Wire Bond Pairs
09639288	6972494	2000-08-15	2005-12-06	Granted	United States of America	Integrated Circuit Die For Wire Bonding And Flip-Chip Mounting
11158435	7541674	2005-06-22	2009-06-02	Granted	United States of America	Integrated Circuit Die For Wire Bonding And Flip-Chip Mounting
11395779	8025201	2006-03-31	2011-09-27	Granted	United States of America	Methods And Apparatus For Integrated Circuit Ball Bonding With Substantially Perpendicular Wire Bond Profiles
10786182	7074705	2004-02-25	2006-07-11	Granted	United States of America	Methods And Apparatus For Integrated Circuit Ball Bonding With Substantially Perpendicular Wire Bond Profiles
09680759	6639321	2000-10-06	2003-10-28	Granted	United States of America	Balanced coefficient of thermal expansion for flip chip ball grid array
10631328	6806119	2003-07-30	2004-10-19	Granted	United States of America	Method of balanced coefficient of thermal expansion for flip chip ball grid array
11258253	7582938	2005-10-25	2009-09-01	Lapsed	United States of America	I/O and Power ESD Protection Circuits by Enhancing Substrate-Bias In Deep-Submicron CMOS Process

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
12506746	7948036	2009-07-21	2011-05-24	Granted	United States of America	I/O and Power ESD Protection Circuits by Enhancing Substrate-Bias In Deep-Submicron CMOS Process
13110581	8269280	2011-05-18	2012-09-18	Granted	United States of America	I/O and Power ESD Protection Circuits by Enhancing Substrate-Bias In Deep-Submicron CMOS Process
10676602	6979869	2003-10-01	2005-12-27	Granted	United States of America	Substrate-biased I/O and power ESD protection circuits in deep-submicron twin-well process
10939292		2004-09-10		Abandoned	United States of America	Wire Bonding Method For Copper Interconnects In Semiconductor Devices
09467253	6790757	1999-12-20	2004-09-14	Granted	United States of America	Wire Bonding Method For Copper Interconnects In Semiconductor Devices
09072369	5986343	1998-05-04	1999-11-16	Granted	United States of America	Bond Pad Design For Integrated Circuits
09305766	6207547	1999-05-05	2001-03-27	Granted	United States of America	Bond Pad Design For Integrated Circuits
12228720	7632717	2008-08-15	2009-12-15	Granted	United States of America	Plastic Overmolded Packages With Mechanically Decoupled Lid Attach Attachment
11505152	7423341	2006-08-16	2008-09-09	Granted	United States of America	Plastic Overmolded Packages With Mechanically Decoupled Lid Attach Attachment
10061518	6617181	2002-02-01	2003-09-09	Granted	United States of America	Flip chip testing
10462524	6710453	2003-06-16	2004-03-23	Granted	United States of America	Integrated circuit containing redundant core and peripheral contacts
09193832	6118177	1998-11-17	2000-09-12	Granted	United States of America	Heatspreader For A Flip Chip Device, And Method For Connecting The Heatspreader
09496989	6681482	2000-02-02	2004-01-27	Granted	United States of America	Heatspreader For A Flip\(miChip Device And Method For Connecting The Heatspreader
09244857	6068130	1999-02-05	2000-05-30	Granted	United States of America	Device And Method For Protecting Electronic Component
09580522	6554137	2000-05-30	2003-04-29	Granted	United States of America	Device And Method For Protecting Electronic Component
07940157	6077725	1992-09-03	2000-06-20	Expired	United States of America	Method and Apparatus for Assembling Multichip Modules
08479587	5564617	1995-06-07	1996-10-15	Expired	United States of America	Method And Apparatus For Assembling Multichip Modules
09461609	6409829	1999-12-15	2002-06-25	Granted	United States of America	Manufacture Of Dielectrically Isolated Integrated Circuits
10091291	6727567	2002-03-05	2004-04-27	Granted	United States of America	Integrated Circuit Device Substrates With Selective Epitaxial Growth Thickness Compensation

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09698175	6675450	2000-10-30	2004-01-13	Granted	United States of America	Method Of Manufacturing And Mounting Electronic Devices To Limit The Effects Of Parasitics
10742916		2003-12-23		Abandoned	United States of America	Method Of Manufacturing And Mounting Electronic Devices To Limit The Effects Of Parasitics
09578082	6465884	2000-05-24	2002-10-15	Granted	United States of America	Semiconductor Device With Variable Pin Locations
10218783	6833286	2002-08-14	2004-12-21	Granted	United States of America	Semiconductor Device With Variable Pin Locations
10254473	6849936	2002-09-25	2005-02-01	Granted	United States of America	System and method for using film deposition techniques to provide an antenna within an integrated circuit package
11012838		2004-12-15		Abandoned	United States of America	System and Method For Using Film Deposition Techniques to Provide an Antenna Within an Integrated Circuit Package
10229601	6781150	2002-08-28	2004-08-24	Granted	United States of America	Test structure for detecting bonding-induced cracks
10856213	6998638	2004-05-28	2006-02-14	Granted	United States of America	Test structure for detecting bonding-induced cracks
09920144		1900-01-01		Abandoned	United States of America	Adhesive Pad Having EMC Shielding Characteristics
09932307	6563198	2001-08-17	2003-05-13	Granted	United States of America	Adhesive pad having EMC shielding characteristics
08838536	6281590	1997-04-09	2001-08-28	Expired	United States of America	Circuit And Method For Providing Interconnections Among Individual Integrated Circuit Chips In A Multi-Chip Module
09873551	6465336	2001-06-04	2002-10-15	Expired	United States of America	Circuit And Method For Providing Interconnections Among Individual Integrated Circuit Chips In A Multi-Chip Module
11868624	7429502	2007-10-08	2008-09-30	Granted	United States of America	Integrated Circuit Device Incorporating Metallurgical Bond To Enhance Thermal Conduction To A Heat Sink
11235920	7327029	2005-09-27	2008-02-05	Granted	United States of America	Integrated Circuit Device Incorporating Metallurgical Bond To Enhance Thermal Conduction To A Heat Sink
11448560	7301231	2006-06-07	2007-11-27	Granted	United States of America	Reinforced Bond Pad For A Semiconductor Device
10955913	7115985	2004-09-30	2006-10-03	Granted	United States of America	Reinforced Bond Pad For A Semiconductor Device
11379256	8601683	2006-04-19	2013-12-10	Granted	United States of America	Method for Electrical Interconnection Between Printed Wiring Board Layers Using Through Holes with Solid Core Conductive Material
10755616		2004-01-12		Abandoned	United States of America	A Printed Wiring Board Including A Solid Core Conductive Material Located Therein

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11385245	7443042	2006-03-21	2008-10-28	Granted	United States of America	Methods And Apparatus For Wire Bonding With Wire Length Adjustment In An Integrated Circuit
10787010	7086148	2004-02-25	2006-08-08	Granted	United States of America	Methods And Apparatus For Wire Bonding With Wire Length Adjustment In An Integrated Circuit
12171903	7637414	2008-07-11	2009-12-29	Granted	United States of America	Methods And Apparatus For Wire Bonding With Wire Length Adjustment In An Integrated Circuit
09197074	6342442	1998-11-20	2002-01-29	Granted	United States of America	Kinetically Controlled Solder Bonding
10021174	7009299	2001-10-29	2006-03-07	Granted	United States of America	Kinetically Controlled Solder Bonding
10266267	6881613	2002-10-08	2005-04-19	Lapsed	United States of America	Electronic Component Package
11080859	7224076	2005-03-15	2007-05-29	Granted	United States of America	Electronic Component Package
10173182	6830999	2002-06-17	2004-12-14	Expired	United States of America	Method Of Fabricating Flip Chip Semiconductor Device Utilizing Polymer Layer For Reducing Thermal Expansion Coefficient Differential
09609582	6441473	2000-06-30	2002-08-27	Expired	United States of America	Flip Chip Semiconductor Device
08938619	5925827	1997-09-25	1999-07-20	Expired	United States of America	System And Method For Empirically Determining Shrinkage Stresses In A Molded Package And Power Module Employing The Same
09127707	5939641	1998-07-31	1999-08-17	Expired	United States of America	System And Method For Empirically Determining Shrinkage Stresses In A Molded Package And Power Module Employing The Same
11385086	7705473	2006-03-21	2010-04-27	Granted	United States of America	Methods And Apparatus For Determining Pad Height For A Wire-Bonding Operation In An Integrated Circuit
10673703	7056819	2003-09-29	2006-06-06	Granted	United States of America	Methods And Apparatus For Determining Pad Height For A Wire\(miBonding Operation In An Integrated Circuit
11530550	7271485	2006-09-11	2007-09-18	Granted	United States of America	Systems And Methods For Distributing I\(slO In A Semiconductor Device
11684674	7709861	2007-03-12	2010-05-04	Granted	United States of America	Systems And Methods For Supporting a Subset of Multiple Interface Types In A Semiconductor Device
09022733	5965903	1998-02-12	1999-10-12	Expired	United States of America	A Device And Method Of Manufacture For An Integrated Circuit Having A BIST Circuit And Bond Pads Incorporated Therein
09288746	6136620	1999-04-08	2000-10-24	Expired	United States of America	A Device And Method Of Manufacture For An Integrated Circuit Having A BIST And Bond Pads Incorporated Therein

Schedule B(1)(c) – Semic Packaging

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08549990	5751065	1995-10-30	1998-05-12	Expired	United States of America	Integrated Circuit With Active Devices Under Bond Pads
09499801	6335491	2000-02-08	2002-01-01	Granted	United States of America	Interposer for semiconductor package assembly
09974157	6618938	2001-10-09	2003-09-16	Granted	United States of America	Interposer for semiconductor package assembly
08506382	5745986	1995-07-24	1998-05-05	Expired	United States of America	Method of planarizing an array of plastically deformable contacts on an integrated circuit package to compensate for surface warpage
08192081	5435482	1994-02-04	1995-07-25	Expired	United States of America	Integrated circuit having a coplanar solder ball contact array
08960831	6088914	1997-10-30	2000-07-18	Expired	United States of America	Method for planarizing an array of solder balls
08918451	5989937	1997-08-26	1999-11-23	Expired	United States of America	Method for compensating for bottom warpage of a BGA integrated circuit
08936259		1997-09-24		Abandoned	United States of America	Integrated Circuit Having A Coplanar Solder Ball Contact Array
08578049		1995-12-26		Abandoned	United States of America	Integrated Circuit Having A Coplanar Solder Ball Contact Array
61377171		2010-08-28		Expired	United States of America	Low Cost 3D-Face to Face Fan Out, F2FFO, Assembly
13217857	8502372	2011-08-25	2013-08-06	Granted	United States of America	Low-Cost 3D Face-to-Face Out Assembly
13344207		2012-01-05		Abandoned	United States of America	Aluminum Bond Pads With Enhanced Wire Bond Stability
12471982	8101871	2009-05-26	2012-01-24	Granted	United States of America	Aluminum Bond Pads With Enhanced Wire Bond Stability
09946033	6573113	2001-09-04	2003-06-03	Granted	United States of America	Integrated circuit having dedicated probe pads for use in testing densely patterned bonding pads
09100665	6061889	1998-06-19	2000-05-16	Granted	United States of America	Device and method for removing heatspreader from an integrated circuit package
09375835	6266249	1999-08-16	2001-07-24	Granted	United States of America	Semiconductor flip chip ball grid array package
08842379	6057594	1997-04-23	2000-05-02	Expired	United States of America	High power dissipating tape ball grid array package
09097883	6002169	1998-06-15	1999-12-14	Granted	United States of America	Thermally enhanced tape ball grid array package

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09097882	6143586	1998-06-15	2000-11-07	Granted	United States of America	Electrostatic protected substrate
10298971	6861748	2002-11-18	2005-03-01	Lapsed	United States of America	Test structure
09122335	6156676	1998-07-24	2000-12-05	Granted	United States of America	Laser marking of semiconductor wafer substrate while inhibiting adherence to substrate surface of particles generated during laser marking
09009580	6114761	1998-01-20	2000-09-05	Granted	United States of America	Thermally-enhanced flip chip IC package with extruded heatspreader
09114345	6130113	1998-07-13	2000-10-10	Granted	United States of America	Enhanced lamination process between heatspreader to pressure sensitive adhesive (PSA) interface as a step in the semiconductor assembly process
09885491	6445066	2001-06-20	2002-09-03	Granted	United States of America	Splitting and assigning power planes
09006784	6040632	1998-01-14	2000-03-21	Granted	United States of America	Multiple sized die
09053357	6297550	1998-04-01	2001-10-02	Granted	United States of America	Bondable anodized aluminum heatspreader for semiconductor packages
09052884	6083848	1998-03-31	2000-07-04	Granted	United States of America	Removing solder from integrated circuits for failure analysis
08975025	6117352	1997-11-20	2000-09-12	Granted	United States of America	Removal of a heat spreader from an integrated circuit package to permit testing of the integrated circuit and other elements of the package
08911515	6126063	1997-08-14	2000-10-03	Expired	United States of America	Integrated circuit packaging apparatus and method
08934529	5835355	1997-09-22	1998-11-10	Expired	United States of America	Tape ball grid array package with perforated metal stiffener
08911418	6081997	1997-08-14	2000-07-04	Expired	United States of America	System and method for packaging an integrated circuit using encapsulant injection
1580331997	4550173	1997-05-30	2010-07-16	Expired	Japan	Wire Bondable Package Design With Maximum Electrical Performance And Minimum Number Of Layers
08868316	5909056	1997-06-03	1999-06-01	Expired	United States of America	High performance heat spreader for flip chip packages
08864994	5907189	1997-05-29	1999-05-25	Expired	United States of America	Conformal diamond coating for thermal improvement of electronic packages
08971769	5992012	1997-11-17	1999-11-30	Granted	United States of America	Method for making electrical interconnections between layers of an IC package

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08958776	5998242	1997-10-27	1999-12-07	Expired	United States of America	Vacuum assisted underfill process and apparatus for semiconductor package fabrication
08927704	6114189	1997-09-10	2000-09-05	Expired	United States of America	Molded array integrated circuit package
08861884	5834839	1997-05-22	1998-11-10	Expired	United States of America	Preserving clearance between encapsulant and PCB for cavity-down single-tier package assembly
08850292	6011304	1997-05-05	2000-01-04	Expired	United States of America	Stiffener ring attachment with holes and removable snap-in heat sink or heat spreader/lid
08859751	6069027	1997-05-21	2000-05-30	Expired	United States of America	Fixture for lid-attachment for encapsulated packages
08852597	5972738	1997-05-07	1999-10-26	Expired	United States of America	PBGA stiffener package
08837530	5841191	1997-04-21	1998-11-24	Expired	United States of America	Ball grid array package employing raised metal contact rings
08770872	5814881	1996-12-20	1998-09-29	Expired	United States of America	Stacked integrated chip package and method of making same
08845696	5977622	1997-04-25	1999-11-02	Expired	United States of America	Stiffener with slots for clip-on heat sink attachment
08850076	5940271	1997-05-02	1999-08-17	Expired	United States of America	Stiffener with integrated heat sink attachment
08771636	5973393	1996-12-20	1999-10-26	Expired	United States of America	Apparatus and method for stackable molded lead frame ball grid array packaging of integrated circuits
08717601	5899737	1996-09-20	1999-05-04	Expired	United States of America	Fluxless solder ball attachment process
08819299	5959320	1997-03-18	1999-09-28	Expired	United States of America	Semiconductor die having on-die de-coupling capacitance
08615865	5723369	1996-03-14	1998-03-03	Expired	United States of America	Method of flip chip assembly
08764039	6020221	1996-12-12	2000-02-01	Expired	United States of America	Process for manufacturing a semiconductor device having a stiffener member
08719266	5731223	1996-09-24	1998-03-24	Expired	United States of America	Array of solder pads on an integrated circuit
08615388	5801072	1996-03-14	1998-09-01	Expired	United States of America	Method of packaging integrated circuits
08644000	5780924	1996-05-07	1998-07-14	Expired	United States of America	Integrated circuit underfill reservoir
08538629	5695593	1995-10-04	1997-12-09	Expired	United States of America	Method of centering a high pressure lid seal

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08556599	5719733	1995-11-13	1998-02-17	Expired	United States of America	ESD protection for deep submicron CMOS devices with minimum tradeoff for latchup behavior
08536002	5621616	1995-09-29	1997-04-15	Expired	United States of America	High density CMOS integrated circuit with heat transfer structure for improved cooling
12432763	8115321	2009-04-30	2012-02-14	Granted	United States of America	Separate Probe And Bond Regions Of An Integrated Circuit
11772267	7479703	2007-07-02	2009-01-20	Granted	United States of America	INTEGRATED CIRCUIT PACKAGE WITH SPUTTERED HEAT SINK FOR IMPROVED THERMAL PERFORMANCE
2013027597	5350550	2013-02-15	2013-08-30	Granted	Japan	Package with Power and Ground Through Silicon Via
068480516		2006-12-21		Application	European Patent	High Thermal Performance PBGA/FSBGA
11283340	7298036	2005-11-18	2007-11-20	Granted	United States of America	Scaling of functional assignments in packages
20117005408	10-1333387	2009-01-07	2013-11-20	Granted	Korea, Republic of (KR)	Package with Power and Ground Through Silicon Via
078524717		2007-09-27		Application	European Patent	Wire Bond Integrated Circuit Package For High Speed I/O
11300789	7379836	2005-12-14	2008-05-27	Lapsed	United States of America	Method of using automated test equipment to screen for leakage inducing defects after calibration to intrinsic leakage
10394445	6777971	2003-03-20	2004-08-17	Granted	United States of America	High speed wafer sort and final test
60147106		1999-08-04		Expired	United States of America	Vacuum-Assisted Integrated Circuit Test Socket
60095397		1998-08-05		Expired	United States of America	An Integrated Circuit Carrier And Method Of Manufacturing And Integrated Circuit
60714214		2005-09-02		Expired	United States of America	Heat Dissipation In Integrated Circuits
12160233	7776648	2008-07-08	2010-08-17	Granted	United States of America	High Thermal Performance Packaging For Circuit Dies
1020107007877	10-1360815	2007-10-31	2014-02-04	Lapsed	Korea, Republic of (KR)	Bond Pad Support Structure For Semiconductor Device
11360200	7394028	2006-02-23	2008-07-01	Granted	United States of America	Flexible Circuit Substrate For Flip-Chip-On-Flex Applications
10675260	6960836	2003-09-30	2005-11-01	Granted	United States of America	Reinforced Bond Pad
10878157	7157361	2004-06-28	2007-01-02	Granted	United States of America	Methods For Processing Integrated Circuit Packages Formed Using Electroplating And Apparatus Made Therefrom
09346100	6282100	1999-07-01	2001-08-28	Granted	United States of America	Low Cost Ball Grid Array Package

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10647863	7148535	2003-08-25	2006-12-12	Granted	United States of America	Zero capacitance bondpad utilizing active negative capacitance
10635276	6828682	2003-08-06	2004-12-07	Granted	United States of America	Substrate voltage connection
10718829	7082585	2003-11-21	2006-07-25	Granted	United States of America	Analysis of integrated circuits for high frequency performance
08946980	5898223	1997-10-08	1999-04-27	Expired	United States of America	Chip-On-Chip IC Packages
09149803	6175158	1998-09-08	2001-01-16	Granted	United States of America	Interposer For Recessed Flip-Chip Package
10456281	6911736	2003-06-06	2005-06-28	Granted	United States of America	Electrostatic discharge protection
08581299	5918794	1995-12-28	1999-07-06	Expired	United States of America	Solder Bonding Of Dense Arrays Of Microminiature Contact Pads
08346454	5583285	1994-11-29	1996-12-10	Expired	United States of America	Method for Detecting A Coating Material on A Substrate
08359973	5607882	1994-12-20	1997-03-04	Expired	United States of America	Multi-Component Electronic Devices and Methods for Making Them
10420219	6768386	2003-04-22	2004-07-27	Granted	United States of America	Dual clock package option
10458130	6867480	2003-06-10	2005-03-15	Granted	United States of America	Electromagnetic interference package protection
10819684	7173328	2004-04-06	2007-02-06	Granted	United States of America	Integrated circuit package and method having wire-bonded intra-die electrical connections
89122966	NI-182345	2000-11-01	2003-08-01	Granted	Taiwan	Testing Integrated Circuits
89100891	NI-138749	2000-04-11	2001-08-21	Granted	Taiwan	Flip Chip Assembly of Semiconductor IC Chips
87115697	NI-124614	1998-09-21	2000-12-11	Lapsed	Taiwan	Chip-On-Chip IC Packages
87103290	NI-125782	1998-03-06	2001-01-11	Lapsed	Taiwan	Circuit And Method For Providing Interconnections Among Individual Integrated Circuit Chips In A Multi-Chip Module
097127688	I452657	2008-07-21	2014-09-11	Granted	Taiwan	Soldering Method and Related Device for Improved Resistance to Brittle Fracture
1019990038064	754752	1999-09-08	2007-08-28	Granted	Korea, Republic of (KR)	Translator For Recessed Flip-chip Package
1019990015968	324832	1999-05-04	2002-02-04	Lapsed	Korea, Republic of (KR)	Bond Pad Design For Integrated Circuits
11289840	3554685	1999-10-12	2004-05-14	Granted	Japan	Flip Chip Metallization
2000012153	3554695	2000-01-20	2004-05-14	Granted	Japan	Flip Chip Assembly of Semiconductor IC Chips
11253017	3803213	1999-09-07	2006-05-12	Granted	Japan	Translator For Recessed Flip-chip Package

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11053116	3503739	1999-03-01	2003-12-19	Granted	Japan	Manufacture Of Flip-Chip Devices
10280566	6654248	2002-10-25	2003-11-25	Granted	United States of America	Top gated heat dissipation
2000284630	3590340	2000-09-20	2004-08-27	Granted	Japan	Integrated Circuit Packages With Improved EMI Characteristics
10268361	7041516	2002-10-10	2006-05-09	Granted	United States of America	Multi chip module assembly
2006261623	5250193	2006-09-27	2013-04-19	Lapsed	Japan	Integrated Circuit Device Incorporating Metallurgical Bond To Enhance Thermal Conduction To A Heat Sink
09846435	6433565	2001-05-01	2002-08-13	Granted	United States of America	Test fixture for flip chip ball grid array circuits
2007101120369	ZL 200710112936.9	2007-06-21	2011-11-16	Granted	China	Plastic Overmolded Packages with Mechanically Decoupled Lid Attach Attachment
10267410	6861343	2002-10-09	2005-03-01	Lapsed	United States of America	Buffer metal layer
10289074	6734697	2002-11-06	2004-05-11	Granted	United States of America	Die location on ungrounded wafer for back-side emission microscopy
993011295	69944012.2	1999-02-16	2012-02-01	Lapsed	Germany (Federal Republic of)	Manufacture Of Flip-Chip Devices
993078310	69918631.5	1999-10-05	2004-07-14	Granted	Germany (Federal Republic of)	Flip Chip Metallization
003011756	60046100.9	2000-02-18	2011-06-22	Lapsed	Germany (Federal Republic of)	Flip Chip Bump Bonding
09441543	6559670	1999-11-16	2003-05-06	Granted	United States of America	Backside liquid crystal analysis technique for flip-chip packages
09596039	6431432	2000-06-15	2002-08-13	Granted	United States of America	Method for attaching solderballs by selectively oxidizing traces
09975871	6555914	2001-10-12	2003-04-29	Granted	United States of America	Integrated circuit package via
12079124	7566953	2008-03-25	2009-07-28	Granted	United States of America	Leadframe Designs For Plastic Overmolded Packages
09465425	6320127	1999-12-20	2001-11-20	Granted	United States of America	Method and structure for reducing the incidence of voiding in an underfill layer of an electronic component package
09478164	6347291	2000-01-05	2002-02-12	Granted	United States of America	Substrate position location system
09322064	6133064	1999-05-27	2000-10-17	Granted	United States of America	Flip chip ball grid array package with laminated substrate

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09494070	6397944	2000-01-28	2002-06-04	Granted	United States of America	Heat dissipating apparatus and method for electronic components
09940130	6519844	2001-08-27	2003-02-18	Granted	United States of America	Overmold integrated circuit package
09884711	6411114	2001-06-18	2002-06-25	Granted	United States of America	Universal test coupon for performing prequalification tests on substrates
09103291	6110815	1998-06-23	2000-08-29	Granted	United States of America	Electroplating fixture for high density substrates
09104838	5981311	1998-06-25	1999-11-09	Granted	United States of America	Process for using a removeable plating bus layer for high density substrates
10287668	6828643	2002-11-04	2004-12-07	Granted	United States of America	Bonding pads over input circuits
1997355620	4709336	1997-12-24	2011-03-25	Granted	Japan	Use Of Plasma Activated Nf3 To Clean Solder Bumps On A Device
09070671	5903050	1998-04-30	1999-05-11	Granted	United States of America	Semiconductor package having capacitive extension spokes and method for making the same
09075300	6117695	1998-05-08	2000-09-12	Granted	United States of America	Apparatus and method for testing a flip chip integrated circuit package adhesive layer
09885299	6459049	2001-06-20	2002-10-01	Granted	United States of America	High density signal routing
09078093	6068727	1998-05-13	2000-05-30	Granted	United States of America	Apparatus and method for separating a stiffener member from a flip chip integrated circuit package substrate
08963553	6118180	1997-11-03	2000-09-12	Granted	United States of America	Semiconductor die metal layout for flip chip packaging
08955929	5973397	1997-10-22	1999-10-26	Expired	United States of America	Semiconductor device and fabrication method which advantageously combine wire bonding and tab techniques to increase integrated circuit I/O pad density
08938100	5949137	1997-09-26	1999-09-07	Expired	United States of America	Stiffener ring and heat spreader for use with flip chip packaging assemblies
08935424	5909057	1997-09-23	1999-06-01	Expired	United States of America	Integrated heat spreader/stiffener with apertures for semiconductor package
08935834	6002171	1997-09-22	1999-12-14	Expired	United States of America	Integrated heat spreader/stiffener assembly and method of assembly for semiconductor package
1580321997	4572011	1997-05-30	2010-08-20	Expired	Japan	Apparatus To Decouple Core Circuits Power Supply From Input-Output Circuits Power Supply In A Semiconductor Device Package
09005491	6111313	1998-01-12	2000-08-29	Granted	United States of America	Integrated circuit package having a stiffener dimensioned to receive heat transferred laterally from the integrated circuit

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08837685	5841198	1997-04-21	1998-11-24	Expired	United States of America	Ball grid array package employing solid core solder balls
09839925	6479319	2001-04-20	2002-11-12	Granted	United States of America	Contact escape pattern
09894210	6531932	2001-06-27	2003-03-11	Granted	United States of America	Microstrip package having optimized signal line impedance control
08412087	5610442	1995-03-27	1997-03-11	Expired	United States of America	Semiconductor device package fabrication method and apparatus
08203919	5644102	1994-03-01	1997-07-01	Expired	United States of America	Integrated circuit packages with distinctive coloration
97143311	I379364	2008-11-10	2012-12-11	Lapsed	Taiwan	Process of grounding heat spreader/stiffener to a flip chip package using solder and film adhesive
09068171	4592122	1997-03-21	2010-09-24	Expired	Japan	Flip Chip Package With Reduced Number Of Package Layers
08619909	5686764	1996-03-20	1997-11-11	Expired	United States of America	Flip chip package with reduced number of package layers
08632952	5761048	1996-04-16	1998-06-02	Expired	United States of America	Conductive polymer ball attachment for grid array semiconductor packages
08538630	5716493	1995-10-04	1998-02-10	Expired	United States of America	High pressure lid seal clip apparatus
08539188	5786631	1995-10-04	1998-07-28	Expired	United States of America	Configurable ball grid array package
08656033	5691568	1996-05-31	1997-11-25	Expired	United States of America	Wire bondable package design with maxium electrical performance and minimum number of layers
08647344	5777383	1996-05-09	1998-07-07	Expired	United States of America	Semiconductor chip package with interconnect layers and routing and testing methods
08299209	5465470	1994-08-31	1995-11-14	Expired	United States of America	Fixture for attaching multiple lids to multi-chip module (MCM) integrated circuit
95108042	I386663	2006-03-10	2013-02-21	Lapsed	Taiwan	Test Vehicle Data Analysis
2006100595493	ZL200610059549.3	2006-03-06	2010-04-14	Lapsed	China	Test Vehicle Data Analysis
09801007	6518161	2001-03-07	2003-02-11	Granted	United States of America	Method for manufacturing a dual chip in package with a flip chip die mounted on a wire bonded die
08538907	5632437	1995-10-04	1997-05-27	Expired	United States of America	Method of centering a lid seal clip
08539189	5598775	1995-10-04	1997-02-04	Expired	United States of America	Centering lid seal clip apparatus
08580800	5818102	1995-12-29	1998-10-06	Expired	United States of America	System having integrated circuit package with lead frame having internal power and ground busses

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08627411	6078502	1996-04-01	2000-06-20	Expired	United States of America	System having heat dissipating leadframes
08573892	5767580	1995-12-18	1998-06-16	Expired	United States of America	Systems having shaped, self-aligning micro-bump structures
08655599	5672911	1996-05-30	1997-09-30	Expired	United States of America	Apparatus to decouple core circuits power supply from input-output circuits power supply in a semiconductor device package
12034745	7750460	2008-02-21	2010-07-06	Granted	United States of America	Ball Grid Array Package Layout Supporting Many Voltage Splits and Flexible Split Locations
07828468	5831836	1992-01-30	1998-11-03	Expired	United States of America	Power plane for semiconductor device
098102349	I453875	2009-01-21	2014-09-21	Granted	Taiwan	Package with Power and Ground Through Via
12121363	8350375	2008-05-15	2013-01-08	Granted	United States of America	Flipchip Bump Patterns for Efficient I-Mesh Power Distribution Schemes
201495711	5922702	2008-08-21	2016-04-22	Granted	Japan	Mitigation of Whiskers in SN-Films
2011197816	5562308	2011-09-12	2014-06-20	Granted	Japan	Reinforced Bond Pad
003086758		2000-10-03		Application	European Patent	Multifunction Lead Frame And Integrated Circuit Package Incorporating The Same
062556691	1827067	2006-11-03	2016-09-21	Completed	European Patent	Flexible Circuit Substrate For Flip-Chip-On-Flex Applications
062556691	60 2006 050 331.8-08	2006-11-03	2016-09-21	Granted	Germany (Federal Republic of)	Flexible Circuit Substrate For Flip-Chip-On-Flex Applications
201489934	5882390	2007-02-23	2016-02-12	Granted	Japan	Flexible Circuit Substrate For Flip-Chip-On-Flex Applications
09843443	6586825	2001-04-26	2003-07-01	Granted	United States of America	Dual chip in package with a wire bonded die mounted to a substrate
2000248741	5069387	2000-08-18	2012-08-24	Granted	Japan	Multiple Layers Tape Ball Grid Array Package
11276938	7180011	2006-03-17	2007-02-20	Granted	United States of America	Device for minimizing differential pair length mismatch and impedance discontinuities in an integrated circuit package design
2009801224755	ZL2009801224755	2009-01-07	2015-04-08	Granted	China	Package with Power and Ground Through Silicon Via
088727722	2248165	2008-11-20	2017-01-18	Granted	Germany (Federal Republic of)	Process of grounding heat spreader stiffener to a FPBGA using solder and film adhesive
088727722	2248165	2008-11-20	2017-01-18	Completed	European Patent	Process of grounding heat spreader stiffener to a FPBGA using solder and film adhesive
11334870	7737564	2006-01-19	2010-06-15	Granted	United States of America	POWER CONFIGURATION METHOD FOR STRUCTURED ASICS
2008801275042	ZL200880127504.2	2008-11-20	2012-07-18	Granted	China	Process of grounding heat spreader stiffener to a FPBGA using solder and film adhesive

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
20107018929	1177039	2008-11-20	2012-08-20	Granted	Korea, Republic of (KR)	Process of grounding heat spreader stiffener to a FPBGA using solder and film adhesive
096144051	I402958	2007-11-21	2013-07-21	Granted	Taiwan	Wire Bond Integrated Circuit Package For High Speed I/O
11102156	7370257	2005-04-08	2008-05-06	Granted	United States of America	Test vehicle data analysis
09766104	6396699	2001-01-19	2002-05-28	Granted	United States of America	Heat sink with chip die EMC ground interconnect
11641989	7557303	2006-12-18	2009-07-07	Granted	United States of America	ELECTRONIC COMPONENT CONNECTION SUPPORT STRUCTURES INCLUDING AIR AS A DIELECTRIC
12038911	7968999	2008-02-28	2011-06-28	Granted	United States of America	Process of grounding heat spreader/stiffener to a flip chip package using solder and film adhesive
09695540	6496374	2000-10-24	2002-12-17	Granted	United States of America	Apparatus suitable for mounting an integrated circuit
11565701	7804167	2006-12-01	2010-09-28	Granted	United States of America	Wire Bond Integrated Circuit Package For High Speed I/O
2011526065	5525530	2009-01-07	2014-04-18	Lapsed	Japan	Package with Power and Ground Through Silicon Via
098133820		2009-01-07		Application	European Patent	Package with Power and Ground Through Silicon Via
10918933	7117467	2004-08-16	2006-10-03	Granted	United States of America	Methods for optimizing package and silicon co-design of integrated circuit
11283044	7205673	2005-11-18	2007-04-17	Granted	United States of America	Reduce or eliminate IMC cracking in post wire bonded dies by doping Aluminum used in bond pads during Cu/low-k BEOL processing
098108322	I336512	2006-09-25	2011-01-21	Granted	Taiwan	Integrated Circuit Device Incorporating Metallurgical Bond To Enhance Thermal Conduction To A Heat Sink
11073802	7081672	2005-03-07	2006-07-25	Granted	United States of America	Substrate via layout to improve bias humidity testing reliability
003002094		2000-01-13		Abandoned	European Patent	Flip Chip Assembly Of Semiconductor IC Chips
60655816		2005-02-24		Expired	United States of America	Structure And Method For Fabricating Flip Chip Devices
60535839		2004-01-12		Expired	United States of America	Post Sn Plate Reflow To Prevent Sn Whisker Formation On Matte Sn\(slNi Plated Cu Lead Frames
10939082	7235889	2004-09-10	2007-06-26	Granted	United States of America	Integrated heatspreader for use in wire bonded ball grid array semiconductor packages
2010548652	5226087	2008-11-20	2013-03-22	Lapsed	Japan	Process of grounding heat spreader stiffener to a FPBGA using solder and film adhesive
11290087	7531442	2005-11-30	2009-05-12	Lapsed	United States of America	Eliminate IMC Cracking in post wirebonded dies: Macro level stress reduction by modifying dielectric/metal film stack in BE layers during Cu/low-k processing

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
2010843	5731121	2010-01-06	2015-04-17	Lapsed	Japan	A Gate Stack Structure For Integrated Circuit Fabrication
11140455	7528616	2005-05-27	2009-05-05	Lapsed	United States of America	Zero ATE Insertion Force Interposer Daughter Card
60435033		2002-12-20		Expired	United States of America	Method Of Bonding TO Copper
11097895	7319272	2005-04-01	2008-01-15	Granted	United States of America	Ball assignment system
11132751	7354790	2005-05-18	2008-04-08	Granted	United States of America	Method and apparatus for avoiding dicing chip-outs in integrated circuit die
60719234		2005-09-21		Expired	United States of America	Aluminum Bond Pad And Interconnect Structure For The Replacing An Upper Level Of Copper Interconnect In An Integrated Circuit Product
11079028	7491579	2005-03-14	2009-02-17	Lapsed	United States of America	Composable System-in-Package Integrated Circuits and Process of Composing the Same
10954940	7145232	2004-09-30	2006-12-05	Granted	United States of America	Construction to improve thermal performance and reduce die backside warpage
10114144	6847123	2002-04-02	2005-01-25	Granted	United States of America	Vertically staggered bondpad array
10900869	7096748	2004-07-28	2006-08-29	Granted	United States of America	Embedded strain gauge in printed circuit boards
10865179	7436060	2004-06-09	2008-10-14	Granted	United States of America	Semiconductor package and process utilizing pre-formed mold cap and heatspreader assembly
10741155	7328830	2003-12-19	2008-02-12	Granted	United States of America	Structure And Method For Bonding To Copper Interconnect Structures
09631150	6369596	2000-08-02	2002-04-09	Granted	United States of America	Vacuum-Assisted Integrated Circuit Test Socket
10744363	7098528	2003-12-22	2006-08-29	Granted	United States of America	Embedded redistribution interposer for footprint compatible chip package conversion
10855148	7368326	2004-05-27	2008-05-06	Granted	United States of America	Methods And Apparatus To Reduce Growth Formations On Plated Conductive Leads
2006800530073	ZL200680053007.3	2006-12-21	2013-07-10	Granted	China	High Thermal Performance Packaging For Circuit Dies
09138146	7023087	1998-08-21	2006-04-04	Granted	United States of America	Integrated Circuit Carrier And Method Of Manufacturing And Integrated Circuit
60014182		2007-12-17		Expired	United States of America	Integrated Circuit Package For High\(miSpeed Signals
11468901	7633152	2006-08-31	2009-12-15	Granted	United States of America	Heat Dissipation In Integrated Circuits

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
12526334	8222719	2009-08-07	2012-07-17	Granted	United States of America	A Quad Flat No Lead (QFN) Integrated Circuit (IC) Package Having a Modified Paddle and Method for Designing the Package
12678405	8183698	2010-03-16	2012-05-22	Granted	United States of America	Bond Pad Support Structure For Semiconductor Device
1020097018981	10-1356591	2007-02-12	2014-01-22	Lapsed	Korea, Republic of (KR)	Enhanced QFN Exposed Pad Geometry To enable PCB Under Package
1020077019305	10-1266335	2006-02-24	2013-05-15	Granted	Korea, Republic of (KR)	Structure And Method For Fabricating Flip Chip Devices
1020087024806	10-1212473	2006-04-14	2012-12-10	Granted	Korea, Republic of (KR)	Method And Apparatus For Improving Thermal Energy Dissipation In A Direct-Chip-Attach Coupling Configuration Of An Integrated Circuit And A Circuit Board
2009542743	5073756	2006-12-21	2012-08-31	Granted	Japan	High Thermal Performance Packaging For Circuit Dies
2006800060148	200680006014.8	2006-02-24	2010-03-03	Lapsed	China	Structure And Method For Fabricating Flip Chip Devices
077504819		2007-02-12		Lapsed	European Patent	Enhanced QFN Exposed Pad Geometry To enable PCB Under Package
09885687	6759860	2001-06-19	2004-07-06	Granted	United States of America	Semiconductor device package substrate probe fixture
11055712	7433192	2005-02-10	2008-10-07	Granted	United States of America	Packaging For Electronic Modules
10816060	7030472	2004-04-01	2006-04-18	Granted	United States of America	Integrated Circuit Device Having Flexible Leadframe
11298030	7504728	2005-12-09	2009-03-17	Lapsed	United States of America	Integrated Circuit Having Bond Pad With Improved Thermal And Mechanical Properties
10727474	6954082	2003-12-04	2005-10-11	Granted	United States of America	Method and apparatus for testing of integrated circuit package
11884328	7777333	2008-05-30	2010-08-17	Granted	United States of America	Structure And Method For Fabricating Flip Chip Devices
09465089	6838769	1999-12-16	2005-01-04	Granted	United States of America	Dual Damascene Bond Pad Structure For Lowering Stress And Allowing Circuitry Under Pads
20097024392	10-1317019	2007-09-21	2013-10-02	Granted	Korea, Republic of (KR)	Soldering Method and Related Device for Improved Resistance to Brittle Fracture
20097012892	10-1323978	2006-12-21	2013-10-24	Granted	Korea, Republic of (KR)	High Thermal Performance Packaging For Circuit Dies
09081448	6369444	1998-05-19	2002-04-09	Expired	United States of America	Packaging Silicon On Silicon Multichip Modules

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09149804	6160715	1998-09-08	2000-12-12	Granted	United States of America	Translator For Recessed Flip-chip Package
2007800522300		2007-02-12		Abandoned	China	Enhanced QFN Exposed Pad Geometry To enable PCB Under Package
2015100536899		2007-02-07		Application	China	A Quad Flat No Lead Integrated Circuit Package and Method
10620074	6933602	2003-07-14	2005-08-23	Granted	United States of America	Semiconductor package having a thermally and electrically connected heatspreader
10702996	7791210	2003-11-05	2010-09-07	Granted	United States of America	Semiconductor Package Having Discrete Non-Active Electrical Components Incorporated Into The Package
09344656	6371665	1999-06-25	2002-04-16	Granted	United States of America	Plastic Packaged Optoelectronic Device
10681554	7345245	2003-10-08	2008-03-18	Granted	United States of America	Robust high density substrate design for thermal cycling reliability
10464178	6963129	2003-06-18	2005-11-08	Granted	United States of America	Multi-chip package having a contiguous heat spreader assembly
09235795	6178088	1999-01-22	2001-01-23	Granted	United States of America	Electronic Apparatus
09172467	6130141	1998-10-14	2000-10-10	Granted	United States of America	Flip Chip Metallization
09032338	6015652	1998-02-27	2000-01-18	Granted	United States of America	Manufacture Of Flip-Chip Devices
10953291	7221173	2004-09-29	2007-05-22	Granted	United States of America	Method And Structures For Testing A Semiconductor Wafer Prior To Performing A Flip Chip Bumping Process
08542995	5696405	1995-10-13	1997-12-09	Expired	United States of America	Microelectronic Package With Device Cooling
09620939	6465882	2000-07-21	2002-10-15	Granted	United States of America	Integrated Circuit Package Having Partially Exposed Conductive Layer
08393628	5608262	1995-02-24	1997-03-04	Expired	United States of America	Packaging Multi-Chip Modules Without Wire-Bond Interconnection
08946693	6683384	1997-10-08	2004-01-27	Expired	United States of America	Air Isolated Crossovers
08991867	6043670	1997-12-16	2000-03-28	Granted	United States of America	Method For Testing Integrated Circuits
09583126	6480657	2000-05-30	2002-11-12	Granted	United States of America	Methods Of Packaging Polarization Maintaining Fibers
10672495	7009282	2003-09-26	2006-03-07	Granted	United States of America	Packaged Integrated Circuit Providing Trace Access To High-Speed Leads

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09256443	6232212	1999-02-23	2001-05-15	Granted	United States of America	Flip Chip Bump Bonding
11074358	7132735	2005-03-07	2006-11-07	Granted	United States of America	Integrated Circuit Package With Lead Fingers Extending Into A Slot Of A Die Paddle
09235011	6190940	1999-01-21	2001-02-20	Granted	United States of America	Flip Chip Assembly Of Semiconductor IC Chips
08430664	5627407	1995-04-28	1997-05-06	Expired	United States of America	Electronic Package With Reduced Bending Stress
08638003	5741430	1996-04-25	1998-04-21	Expired	United States of America	Conductive Adhesive Bonding Means
09012304	6075427	1998-01-23	2000-06-13	Granted	United States of America	MCM With High Q Overlapping Resonator
10652453	6743979	2003-08-29	2004-06-01	Granted	United States of America	Bonding pad isolation
09385735	6372600	1999-08-30	2002-04-16	Granted	United States of America	Etch Stops And Alignment Marks For Bonded Wafers
09413605	6351033	1999-10-06	2002-02-26	Granted	United States of America	Multifunction Lead Frame And Integrated Circuit Package Incorporating The Same
08578816	5837380	1995-12-26	1998-11-17	Expired	United States of America	Multilayer Structures And Process For Fabricating The Same
08633992	5667132	1996-04-19	1997-09-16	Expired	United States of America	Method For Solder-Bonding Contact Pad Arrays
09351546	6199464	1999-07-12	2001-03-13	Granted	United States of America	Method And Apparatus For Cutting A Substrate
09351945	6319450	1999-07-12	2001-11-20	Granted	United States of America	Vented Mold, Method Of Making The Mold, Method Of Encapsulating A Circuit Using The Mold, And Circuit Encapsulated By The Method
09120148	6154370	1998-07-21	2000-11-28	Granted	United States of America	Recessed Flip-Chip Package
09261093	6232047	1999-03-02	2001-05-15	Granted	United States of America	Fabricating High-Q RF Component
10417049	7023225	2003-04-16	2006-04-04	Granted	United States of America	Wafer-mounted micro-probing platform
08333168	5505367	1994-11-02	1996-04-09	Expired	United States of America	Method For Bumping Silicon Devices
10600255	6798035	2003-06-20	2004-09-28	Granted	United States of America	Bonding pad for low k dielectric

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10615063	6744130	2003-07-08	2004-06-01	Granted	United States of America	Isolated stripline structure
09425706	6251705	1999-10-22	2001-06-26	Granted	United States of America	Low Profile Integrated Circuit Packages
09628067	6509642	2000-07-28	2003-01-21	Granted	United States of America	Integrated Circuit Package
09498005	6678167	2000-02-04	2004-01-13	Granted	United States of America	High Performance Multi-Chip IC Package
09401690	6297551	1999-09-22	2001-10-02	Granted	United States of America	Integrated Circuit Packages With Improved EMI Characteristics
09621110	6790760	2000-07-21	2004-09-14	Granted	United States of America	A Method Of Manufacturing An Integrated Circuit Package
10683101	6825563	2003-10-09	2004-11-30	Granted	United States of America	Slotted bonding pad
09435971	6342399	1999-11-08	2002-01-29	Granted	United States of America	Testing Integrated Circuits
09528882	6437990	2000-03-20	2002-08-20	Granted	United States of America	Multi-Chip Ball Grid Array IC Packages
89103182	NI-137162	2000-04-08	2001-11-14	Granted	Taiwan	Flip Chip Bump Bonding
88114052	NI-142196	1999-08-17	2002-02-01	Granted	Taiwan	Flip Chip Metallization
89121960	NI-172446	2000-10-19	2003-02-21	Lapsed	Taiwan	Low Profile Integrated Circuit Packages
90102134	NI-170172	2001-02-02	2003-05-19	Granted	Taiwan	High Performance Multi-Chip IC Package
90117908	NI-160876	2001-07-23	2002-08-11	Granted	Taiwan	Integrated Circuit Package
10614402	6836026	2003-07-03	2004-12-28	Granted	United States of America	Integrated circuit design for both input output limited and core limited integrated circuits
90117328	NI-167645	2001-07-16	2002-12-01	Granted	Taiwan	Integrated Circuit Package Having Partially Exposed Conductive Layer
89124902	NI-147525	2000-11-23	2002-01-01	Granted	Taiwan	Semiconductor Device Having Self-Aligned Contact And Landing PAD Structure And Method Of Forming Same
89126790	NI-147894	2000-12-14	2002-04-24	Granted	Taiwan	Wire Bonding Method For Copper Interconnects In Semiconductor Devices
89126837	NI-150760	2001-01-03	2002-02-21	Lapsed	Taiwan	Dual Damascene Bond Pad Structure for Lowering Stress and Allowing Circuitry Under Pads
89120479	NI-155555	2000-10-02	2002-09-05	Lapsed	Taiwan	Multifunction Lead Frame And Integrated Circuit Package Incorporating The Same
88113740	NI-127340	1999-08-11	2001-02-21	Lapsed	Taiwan	Interposer For Recessed Flip-Chip Package
09752626	6591410	2000-12-28	2003-07-08	Granted	United States of America	Six-to-one signal/power ratio bump and trace pattern for flip chip design

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09416069	6245993	1999-10-12	2001-06-12	Granted	United States of America	Electronic Assembly Having Shielding And Strain-Relief Member
90117314	NI-183318	2001-07-16	2003-08-11	Granted	Taiwan	A Method Of Manufacturing An Integrated Circuit Package
10371386	6891392	2003-02-21	2005-05-10	Granted	United States of America	Substrate impedance measurement
94132327	I364082	2005-09-19	2012-05-11	Granted	Taiwan	Method and Structure for Testing a Semiconductor Wafer Prior to Performing a Flip Chip Bumping Process
095142149	I411052	2006-11-14	2013-10-01	Granted	Taiwan	Flexible Circuit Substrate For Flip-Chip-On-Flex Applications
095135361	I310597	2006-09-25	2009-06-01	Granted	Taiwan	Integrated Circuit Device Incorporating Metallurgical Bond To Enhance Thermal Conduction To A Heat Sink
1020010043826	678878	2001-07-20	2007-01-30	Granted	Korea, Republic of (KR)	Integrated Circuit Package Having Partially Exposed Conductive Layer
20000008193	712772	2000-02-21	2007-04-23	Lapsed	Korea, Republic of (KR)	Flip Chip Bump Bonding
19990028642	0310572	1999-07-15	2001-09-18	Granted	Korea, Republic of (KR)	Recessed Flip-Chip Package
1019990038065	637008	1999-09-08	2006-10-16	Granted	Korea, Republic of (KR)	Interposer For Recessed Flip-Chip Package
20000078613	687994	2000-12-19	2007-02-21	Lapsed	Korea, Republic of (KR)	Wire Bonding Method For Copper Interconnects In Semiconductor Devices
1020000046915	390229	2000-08-14	2003-06-24	Granted	Korea, Republic of (KR)	Integrated Circuit Die For Wire Bonding And Flip-Chip Mounting
1020010043981	675030	2001-07-21	2007-01-22	Granted	Korea, Republic of (KR)	Integrated Circuit Package
20000076794	691051	2000-12-15	2007-02-27	Lapsed	Korea, Republic of (KR)	Dual Damascene Bond Pad Structure for Lowering Stress and Allowing Circuitry Under Pads
1019990049683	662218	1999-11-10	2006-12-21	Granted	Korea, Republic of (KR)	Heatspreader For A Flip Chip Device, And Method For Connecting The Heatspreader
10396955	7190082	2003-03-24	2007-03-13	Granted	United States of America	Low stress flip-chip package for low-K silicon technology
1019990006458	682284	1999-02-26	2007-02-07	Lapsed	Korea, Republic of (KR)	Manufacture Of Flip-Chip Devices
10347759	6801437	2003-01-21	2004-10-05	Lapsed	United States of America	Electronic organic substrate
09735085	6605951	2000-12-11	2003-08-12	Granted	United States of America	Interconnector and method of connecting probes to a die for functional analysis
1020010005358	742107	2001-02-05	2007-07-18	Granted	Korea, Republic of (KR)	High Performance Multi-Chip IC Package

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10339844	6781228	2003-01-10	2004-08-24	Granted	United States of America	Donut power mesh scheme for flip chip package
1020040078075	1150312	2004-09-30	2012-05-21	Granted	Korea, Republic of (KR)	Reinforced Bond Pad
10290953	6943446	2002-11-08	2005-09-13	Granted	United States of America	Via construction for structural support
1020060094257	10-1245114	2006-09-27	2013-03-13	Lapsed	Korea, Republic of (KR)	Integrated Circuit Device Incorporating Metallurgical Bond To Enhance Thermal Conduction To A Heat Sink
10283965	6744081	2002-10-30	2004-06-01	Granted	United States of America	Interleaved termination ring
2000386402	3796116	2000-12-20	2006-04-21	Lapsed	Japan	Wire Bonding Method For Copper Interconnects In Semiconductor Devices
2000306945	4008195	2000-10-06	2007-09-07	Granted	Japan	Multifunction Lead Frame And Integrated Circuit Package Incorporating The Same
90106482	I222205	2001-03-20	2004-10-11	Granted	Taiwan	Multi-Chip Ball Grid Array IC Packages
20070018179	10-1297915	2007-02-23	2013-08-12	Granted	Korea, Republic of (KR)	Flexible Circuit Substrate For Flip-Chip-On-Flex Applications
20050055694	10-1421714	2005-06-27	2014-07-15	Granted	Korea, Republic of (KR)	Methods For Processing Integrated Circuit Packages Formed Using Electroplating And Apparatus Made Therefrom
20050002443	10-1120288	2005-01-11	2012-02-17	Lapsed	Korea, Republic of (KR)	Methods And Apparatus To Reduce Growth Formations On Plated Conductive Leads
11123342	3821984	1999-04-30	2006-06-30	Granted	Japan	Bond Pad Design For Integrated Circuits
88120078	NI-131285	1999-11-26	2001-04-11	Lapsed	Taiwan	Heatspreader For A Flip Chip Device, And Method For Connecting The Heatspreader
88104689	NI-121715	1999-03-25	2000-10-21	Granted	Taiwan	Bond Pad Design For Integrated Circuits
089111993	NI-156707	2000-06-19	2002-06-11	Granted	Taiwan	Integrated Circuit Die For Wire Bonding And Flip-Chip Mounting
11011396	3578931	1999-01-20	2004-07-23	Granted	Japan	MCM With High Q Overlapping Resonator
11205181	3742252	1999-07-19	2005-11-18	Granted	Japan	Recessed Flip-Chip Package
10402054	6798069	2003-03-28	2004-09-28	Granted	United States of America	Integrated circuit having adaptable core and input/output regions with multi-layer pad trace conductors
93127180	I364833	2004-09-08	2012-05-21	Granted	Taiwan	Reinforced Bond Pad
2000189021	3785026	2000-06-23	2006-03-24	Lapsed	Japan	Plastic Packaged Optoelectronic Device
10267814	6717423	2002-10-09	2004-04-06	Granted	United States of America	Substrate impedance measurement
1020000058790	742104	2000-10-06	2007-07-18	Granted	Korea, Republic of (KR)	Multifunction Lead Frame And Integrated Circuit Package Incorporating The Same

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
1019990031985	623895	1999-08-04	2006-09-07	Granted	Korea, Republic of (KR)	Integrated Circuit Carrier And Method Of Manufacturing And Integrated Circuit
1019990002078	617887	1999-01-23	2006-08-23	Granted	Korea, Republic of (KR)	MCM With High Q Overlapping Resonator
9842014	0311356	1998-10-08	2001-09-25	Granted	Korea, Republic of (KR)	Chip-On-Chip IC Packages
10357142	6963138	2003-02-03	2005-11-08	Granted	United States of America	Dielectric stack
20040076318	10-1060430	2004-09-23	2011-08-23	Granted	Korea, Republic of (KR)	Packaged Integrated Circuit Providing Trace Access To High-Speed Leads
1020060021401	10-1184201	2006-03-07	2012-09-13	Granted	Korea, Republic of (KR)	Integrated Circuit Package With Lead Fingers Extending Into A Slot Of A Die Paddle
1020060094340	10-1288790	2006-09-27	2013-07-17	Granted	Korea, Republic of (KR)	Solder Bump Structure For Flip Chip Semiconductor Devices And Method Of Manufacture Therefore
1020070079027	10-1398404	2007-08-07	2014-05-16	Granted	Korea, Republic of (KR)	Plastic Overmolded Packages with Mechanically Decoupled Lid Attach Attachment
2005188120	5676833	2005-06-28	2015-01-09	Granted	Japan	Methods For Processing Integrated Circuit Packages Formed Using Electroplating And Apparatus Made Therefrom
10298338	6648064	2002-11-14	2003-11-18	Granted	United States of America	Active heat sink
2000044330	3588027	2000-02-22	2004-08-20	Granted	Japan	Flip Chip Bump Bonding
11221875	3929651	1999-08-05	2007-03-16	Lapsed	Japan	Integrated Circuit Carrier And Method Of Manufacturing And Integrated Circuit
10354961	3258285	1998-12-14	2001-12-07	Lapsed	Japan	Method For Testing Integrated Circuits
11139175	3476708	1999-05-19	2003-09-26	Granted	Japan	Packaging Silicon On Silicon Multichip Modules
09086440	3168256	1997-04-04	2001-03-09	Expired	Japan	Method For Solder-Bonding Contact Pad Arrays
2007043174	5905181	2007-02-23	2016-03-25	Granted	Japan	Flexible Circuit Substrate For Flip-Chip-On-Flex Applications
2006060406	5550204	2006-03-07	2014-05-30	Granted	Japan	Integrated Circuit Package With Lead Fingers Extending Into A Slot Of A Die Paddle
10278373	6603201	2002-10-23	2003-08-05	Granted	United States of America	Electronic substrate
2001120442	4193019	2001-04-19	2008-10-03	Lapsed	Japan	Micromagnetic Components
2000242828	4130295	2000-08-10	2008-05-30	Granted	Japan	Integrated Circuit Die For Wire Bonding And Flip-Chip Mounting
98106356X	98106356.X	1998-04-08	2004-01-07	Granted	China	Circuit And Method For Providing Interconnections Among Individual Integrated Circuit Chips In A Multi-Chip Module
09636498	6403399	2000-08-11	2002-06-11	Granted	United States of America	Method of rapid wafer bumping

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10349770	6951000	2003-01-22	2005-09-27	Granted	United States of America	Simulated voltage contrasted image generator and comparator
2006101395386	200610139538.6	2006-09-25	2010-05-12	Granted	China	Integrated Circuit Device Incorporating Metallurgical Bond To Enhance Thermal Conduction To A Heat Sink
2006101630672	ZL 200610163067.2	2006-11-30	2009-10-07	Granted	China	Flexible Circuit Substrate For Flip-Chip-On-Flex Applications
2006101519001	ZL 200610151900.1	2006-09-13	2009-07-22	Granted	China	Solder Bump Structure For Flip Chip Semiconductor Devices And Method Of Manufacture Therefore
2004281010	4959929	2004-09-28	2012-03-30	Lapsed	Japan	Reinforced Bond Pad
2007212015	5121353	2007-08-16	2012-11-02	Granted	Japan	Plastic Overmolded Packages with Mechanically Decoupled Lid Attach Attachment
10211914	6777314	2002-08-02	2004-08-17	Granted	United States of America	Method of forming electrolytic contact pads including layers of copper, nickel, and gold
10229659	6777803	2002-08-28	2004-08-17	Granted	United States of America	Solder mask on bonding ring
993003284	69941168.8	1999-01-19	2009-07-29	Granted	Germany (Federal Republic of)	MCM With High Q Overlapping Resonator
003003696	60014461.5	2000-01-19	2004-10-06	Granted	Germany (Federal Republic of)	Article Comprising Aligned, Truncated Carbon Nanotubes And Process For Fabricating Article
983025164	69839861.0	1998-03-31	2008-08-13	Granted	Germany (Federal Republic of)	Circuit And Method For Providing Interconnections Among Individual Integrated Circuit Chips In A Multi-Chip Module
10141252	6815812	2002-05-08	2004-11-09	Granted	United States of America	Direct alignment of contacts
003050135	600 45 904.7	2000-06-13	2011-07-04	Granted	Germany (Federal Republic of)	Plastic Packaged Optoelectronic Device
983079195		1998-09-29		Abandoned	Germany (Federal Republic of)	Chip-On-Chip IC Packages
983079161	69836944.0	1998-09-29	2007-01-24	Granted	Germany (Federal Republic of)	Air Isolated Crossovers
003078318	60037990.6	2000-09-11	2008-02-13	Granted	Germany (Federal Republic of)	Integrated Circuit Packages With Improved EMI Characteristics
10055812	6605954	2002-01-23	2003-08-12	Granted	United States of America	Reducing probe card substrate warpage
10293458	6861183	2002-11-13	2005-03-01	Granted	United States of America	Scatter dots
10212448	6700207	2002-08-05	2004-03-02	Granted	United States of America	Flip-chip ball grid array package for electromigration testing
10082027	6674176	2002-02-20	2004-01-06	Lapsed	United States of America	Wire bond package with core ring formed over I/O cells

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
003050168	60043373.0	2000-06-13	2009-11-25	Lapsed	Germany (Federal Republic of)	Bonded Article Having Improved Crystalline Structure And Work Function Uniformity And Method For Making The Same
09465131	6962437	1999-12-16	2005-11-08	Granted	United States of America	Method and apparatus for thermal profiling of flip-chip packages
10024054	6769923	2001-12-17	2004-08-03	Granted	United States of America	Fluted signal pin, cap, membrane, and stanchion for a ball grid array
09994567	6671865	2001-11-27	2003-12-30	Lapsed	United States of America	High density input output
09478972	6429534	2000-01-06	2002-08-06	Granted	United States of America	Interposer tape for semiconductor package
10021829	6573523	2001-12-12	2003-06-03	Granted	United States of America	Substrate surface scanning
10094549	6623992	2002-03-08	2003-09-23	Granted	United States of America	System and method for determining a subthreshold leakage test limit of an integrated circuit
09949207	6706622	2001-09-07	2004-03-16	Granted	United States of America	Bonding pad interface
10023311	6590409	2001-12-13	2003-07-08	Granted	United States of America	Systems and methods for package defect detection
08697121	5646828	1996-08-20	1997-07-08	Expired	United States of America	Thin Packaging of multi-chip modules with enhanced thermal power management
09187885	5965197	1998-11-06	1999-10-12	Expired	United States of America	Article Comprising Fine-Grained Solder Compositions With Dispersoid Particles
09238706	6074897	1999-01-28	2000-06-13	Expired	United States of America	Integrated Circuit Bonding Method and Apparatus
11302690	7541220	2005-12-14	2009-06-02	Lapsed	United States of America	Integrated Circuit Device Having Flexible Leadframe
2008290462		2008-11-13		Abandoned	Japan	Semiconductor Device Having Self-Aligned Contact And Landing PAD Structure And Method Of Forming Same
2005367979	4279835	2000-12-20	2009-03-19	Granted	Japan	Wire Bonding Method For Copper Interconnects In Semiconductor Devices
2004175054		2004-06-14		Lapsed	Japan	Heatspreader For A Flip Chip Device, And Method For Connecting The Heatspreader
2008045768	5135493	2008-02-27	2012-11-22	Granted	Japan	Integrated Circuit Package Having Partially Exposed Conductive Layer
2007138865	4685834	1998-10-06	2011-02-18	Lapsed	Japan	Air Isolated Crossovers
08111765	5834792	1993-08-25	1998-11-10	Expired	United States of America	Articles Comprising Doped Semiconductor Material

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09864577	6472304	2001-05-24	2002-10-29	Granted	United States of America	Wire Bonding To Copper
11403492	7817434	2006-04-13	2010-10-19	Granted	United States of America	Method And Apparatus For Improving Thermal Energy Dissipation In A Direct-Chip-Attach Coupling Configuration Of An Integrated Circuit And A Circuit Board
09968286	6657870	2001-10-01	2003-12-02	Granted	United States of America	Die power distribution system
09437559	6475828	1999-11-10	2002-11-05	Granted	United States of America	Method of using both a non-filled flux underfill and a filled flux underfill to manufacture a flip-chip
09488438	6279889	2000-01-20	2001-08-28	Granted	United States of America	Loose die fixture
09440492	6373142	1999-11-15	2002-04-16	Granted	United States of America	Method of adding filler into a non-filled underfill system by using a highly filled fillet
09651308	6441499	2000-08-30	2002-08-27	Granted	United States of America	Thin form factor flip chip ball grid array
09928071	6534968	2001-08-10	2003-03-18	Lapsed	United States of America	Integrated circuit test vehicle
09406308	6306751	1999-09-27	2001-10-23	Granted	United States of America	Apparatus and method for improving ball joints in semiconductor packages
09417255	6425179	1999-10-12	2002-07-30	Granted	United States of America	Method for assembling tape ball grid arrays
09753000	6407462	2000-12-30	2002-06-18	Granted	United States of America	Irregular grid bond pad layout arrangement for a flip chip package
09612867	6465338	2000-07-10	2002-10-15	Granted	United States of America	Method of planarizing die solder balls by employing a die's weight
08853154	6115910	1997-05-08	2000-09-12	Expired	United States of America	Misregistration fidutial
09370856	6449748	1999-08-09	2002-09-10	Granted	United States of America	Non-destructive method of detecting die crack problems
09465132	6395097	1999-12-16	2002-05-28	Granted	United States of America	Method and apparatus for cleaning and removing flux from an electronic component package
08928826	6603200	1997-09-12	2003-08-05	Expired	United States of America	Integrated circuit package
09443036	6294840	1999-11-18	2001-09-25	Granted	United States of America	Dual-thickness solder mask in integrated circuit package
08935583	6166434	1997-09-23	2000-12-26	Expired	United States of America	Die clip assembly for semiconductor package

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09921028	6617866	2001-08-02	2003-09-09	Granted	United States of America	Apparatus and method of protecting a probe card during a sort sequence
09377887	6285077	1999-08-19	2001-09-04	Granted	United States of America	Multiple layer tape ball grid array package
09967195	6496081	2001-09-28	2002-12-17	Granted	United States of America	Transmission equalization system and an integrated circuit package employing the same
09467081	6225690	1999-12-10	2001-05-01	Granted	United States of America	Plastic ball grid array package with strip line configuration
09400767	6328347	1999-09-22	2001-12-11	Granted	United States of America	Uniform axial loading ground glass joint clamp
09345432	6150729	1999-07-01	2000-11-21	Granted	United States of America	Routing density enhancement for semiconductor BGA packages and printed wiring boards
09321298	6127726	1999-05-27	2000-10-03	Granted	United States of America	Cavity down plastic ball grid array multi-chip module
08869796	6225695	1997-06-05	2001-05-01	Expired	United States of America	Grooved semiconductor die for flip-chip heat sink attachment
09212366	6150175	1998-12-15	2000-11-21	Granted	United States of America	Copper contamination control of in-line probe instruments
09127486	6242814	1998-07-31	2001-06-05	Granted	United States of America	Universal I/O pad structure for in-line or staggered wire bonding or arrayed flip-chip assembly
09143083	6261870	1998-08-28	2001-07-17	Granted	United States of America	Backside failure analysis capable integrated circuit packaging
09932716	6759921	2001-08-17	2004-07-06	Granted	United States of America	Characteristic impedance equalizer and an integrated circuit package employing the same
09957410	6701270	2001-09-20	2004-03-02	Granted	United States of America	Method for reliability testing leakage characteristics in an electronic circuit and a testing device for accomplishing the source
12206786	8350379	2008-09-09	2013-01-08	Granted	United States of America	Package with Power and Ground Through Via
962020897	59609905.3	1996-07-24	2002-11-27	Expired	Germany (Federal Republic of)	Semiconductor device having a carrier and a multilayer metallization
08692852	5731635	1996-07-24	1998-03-24	Expired	United States of America	Semiconductor device having a carrier and a multilayer metallization
962020897	0756325	1996-07-24	2002-11-27	Expired	European Patent	Semiconductor device having a carrier and a multilayer metallization
962020897	0756325	1996-07-24	2002-11-27	Lapsed	France	Semiconductor device having a carrier and a multilayer metallization

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
962020897	0756325	1996-07-24	2002-11-27	Lapsed	United Kingdom	Semiconductor device having a carrier and a multilayer metallization
962020897	0756325	1996-07-24	2002-11-27	Lapsed	Netherlands	Semiconductor device having a carrier and a multilayer metallization
101657385		2010-06-11		Application	European Patent	Electronic Device Package And Method Of Manufacture
099118956	I413210	2010-06-10	2013-10-21	Lapsed	Taiwan	Electronic Device Package And Method Of Manufacture
12483139	7993981	2009-06-11	2011-08-09	Lapsed	United States of America	Electronic Device Package And Method Of Manufacture
2010102027867	ZL2010102027867	2010-06-10	2016-01-06	Lapsed	China	Electronic Device Package And Method Of Manufacture
2010132552	5784280	2010-06-10	2015-07-31	Lapsed	Japan	Electronic Device Package And Method Of Manufacture
1020100054807		2010-06-10		Abandoned	Korea, Republic of (KR)	Electronic Device Package And Method Of Manufacture
2010040590	167757	2010-06-10	2013-07-31	Lapsed	Singapore	An Electronic Device Package And Method Of Manufacture
13174970	8384205	2011-07-01	2013-02-26	Lapsed	United States of America	An Electronic Device Package and Method of Manufacture
11717227	7667321	2007-03-12	2010-02-23	Granted	United States of America	Wire Bonding Method And Related Device For High-Frequency Applications
10853395	6894400	2004-05-25	2005-05-17	Granted	United States of America	Robust Electronic Device Packages
10879909	7745927	2004-06-29	2010-06-29	Granted	United States of America	Heat Sink Formed Of Multiple Metal Layers On Backside Of Integrated Circuit Die
10814062	7041561	2004-03-31	2006-05-09	Granted	United States of America	Enhanced Substrate Contact For A Semiconductor Device
10788162	7075174	2004-02-26	2006-07-11	Granted	United States of America	Semiconductor Packaging Techniques For Use With Non-Ceramic Packages
10697757	6987052	2003-10-30	2006-01-17	Granted	United States of America	Method For Making Enhanced Substrate Contact For A Semiconductor Device
09876522	6740222	2001-06-07	2004-05-25	Granted	United States of America	Method Of Manufacturing A Printed Wiring Board Having A Discontinuous Plating Layer
09329420	6313999	1999-06-10	2001-11-06	Granted	United States of America	Self-Alignment Device For Ball Grid Array Devices
09388242	6239382	1999-09-01	2001-05-29	Granted	United States of America	Device And Method Of Controlling The Bowing Of A Soldered Or Adhesively Bonded Assembly
09263075	6153506	1999-03-08	2000-11-28	Granted	United States of America	Integrated Circuit Having Reduced Probability Of Wire-Bond Failure
09123370	5936849	1998-07-27	1999-08-10	Granted	United States of America	Test Fixture Retainer For An Integrated Circuit Package

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09073279	6057700	1998-05-06	2000-05-02	Granted	United States of America	Pressure Controlled Alignment Fixture
08956527	5975408	1997-10-23	1999-11-02	Granted	United States of America	Solder Bonding Of Electrical Components
08824574	5975836	1997-03-26	1999-11-02	Expired	United States of America	Apparatus For Visually Reading Semiconductor Wafer Identification Indicia
08724129	5719449	1996-09-30	1998-02-17	Expired	United States of America	Flip-Chip Integrated Circuit With Improved Testability
08663336	5672913	1996-06-13	1997-09-30	Expired	United States of America	Semiconductor Device Having A Layer Of Gallium Amalgam On Bump Leads
08366539	5501777	1994-12-30	1996-03-26	Expired	United States of America	Method For Testing Solder Mask Material
12119575	7554133	2008-05-13	2009-06-30	Granted	United States of America	PAD CURRENT SPLITTING
13032429	8547681	2011-02-22	2013-10-01	Granted	United States of America	Decoupling Capacitor
12061728	8134232	2008-04-03	2012-03-13	Granted	United States of America	HEAT DISSIPATION FOR INTEGRATED CIRCUIT
098124922	I401440	2009-07-23	2013-07-11	Granted	Taiwan	Circuit Apparatus Including Removable Bond Pad Extension
12463718	7724023	2009-05-11	2010-05-25	Granted	United States of America	Circuit Apparatus Including Removable Bond Pad Extension
2009234710	5676868	2009-10-09	2015-01-09	Granted	Japan	Circuit Apparatus Including Removable Bond Pad Extension
2009056979	166712	2009-08-26	2012-07-13	Lapsed	Singapore	Circuit Apparatus Including Removable Bond Pad Extension
101564813	2251703	2010-03-15	2012-01-25	Completed	European Patent	Circuit Apparatus Including Removable Bond Pad Extension
101564813	602010000720.0	2010-03-15	2012-01-25	Lapsed	Germany (Federal Republic of)	Circuit Apparatus Including Removable Bond Pad Extension
1020090085791	10-1420174	2009-09-11	2014-07-10	Granted	Korea, Republic of (KR)	Circuit Apparatus Including Removable Bond Pad Extension
101564813	2251703	2010-03-15	2012-01-25	Lapsed	United Kingdom	Circuit Apparatus Including Removable Bond Pad Extension
12501686	8378485	2009-07-13	2013-02-19	Granted	United States of America	Improvement Of Solder Interconnect By Addition Of Copper
1020100066127	10-1704030	2010-07-09	2017-02-01	Granted	Korea, Republic of (KR)	Improvement Of Solder Interconnect By Addition Of Copper
099122029	I394632	2010-07-05	2013-05-01	Lapsed	Taiwan	Improvement Of Solder Interconnect By Addition Of Copper
101690105		2010-07-09		Abandoned	European Patent	Improvement Of Solder Interconnect By Addition Of Copper
2010158372	5604665	2010-07-13	2014-09-05	Granted	Japan	Improvement Of Solder Interconnect By Addition Of Copper
2010102269692	ZL201010226969.2	2010-07-12	2014-09-03	Granted	China	Improvement Of Solder Interconnect By Addition Of Copper

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
13752524	8580621	2013-01-29	2013-11-12	Granted	United States of America	Solder Interconnect By Addition Of Copper
12327987	7787252	2008-12-04	2010-08-31	Granted	United States of America	Preferentially Cooled Electronic Device
2010102027994	10 1930935	2010-06-10	2014-07-23	Granted	China	Lead Frame Design To Improve Reliability
099118954	I411082	2010-06-10	2013-10-01	Granted	Taiwan	Lead Frame Design To Improve Reliability
12486592	8334467	2009-06-17	2012-12-18	Granted	United States of America	Lead Frame Design To Improve Reliability
101659696		2010-06-15		Application	European Patent	Lead Frame Design To Improve Reliability
1020100055837	10-1676038	2010-06-14	2016-11-08	Granted	Korea, Republic of (KR)	Lead Frame Design To Improve Reliability
13677547	8869389	2012-11-15	2014-10-28	Granted	United States of America	Method of Manufacturing an Electronic Device Package
12485238	8370777	2009-06-16	2013-02-05	Lapsed	United States of America	A Method Of Generating A Leadframe IC Package Model, A Leadframe Modeler And An IC Design System
12331561	8125091	2008-12-10	2012-02-28	Granted	United States of America	Wire bonding over active circuits
200880130797X	ZL200880130797.X	2008-08-21	2014-01-29	Lapsed	China	Mitigation of Whiskers in SN-Films
2011523783		2008-08-21		Abandoned	Japan	Mitigation of Whiskers in SN-Films
088199641		2008-08-21		Abandoned	European Patent	Mitigation of Whiskers in SN-Films
13059502	8653375	2011-02-17	2014-02-18	Granted	United States of America	Mitigation of Whiskers in SN-Films
098127625	I399461	2009-08-17	2013-06-21	Granted	Taiwan	Mitigation of Whiskers in SN-Films
12060387	7671450	2008-04-01	2010-03-02	Granted	United States of America	Integrated Circuit Package For High-Speed Signals
12220182	7727781	2008-07-22	2010-06-01	Granted	United States of America	Manufacture Of Devices Including Solder Bumps
12154794	7724359	2008-05-27	2010-05-25	Granted	United States of America	A Method Of Making Electronic Entities
12969852	8742535	2010-12-16	2014-06-03	Granted	United States of America	Integration of Shallow Trench Isolation and Through-Substrate Vias into Integrated Circuit Designs
2011273948	5670306	2011-12-15	2014-12-26	Granted	Japan	Integration of Shallow Trench Isolation and Through-Substrate Vias into Integrated Circuit Designs
2011104217470	ZL2011104217470	2011-12-16	2015-01-21	Granted	China	Integration of Shallow Trench Isolation and Through-Substrate Vias into Integrated Circuit Designs
111930921		2011-12-12		Application	European Patent	Integration of Shallow Trench Isolation and Through-Substrate Vias into Integrated Circuit Designs

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
1020110134104	10-1475108	2011-12-14	2014-12-15	Granted	Korea, Republic of (KR)	Integration of Shallow Trench Isolation and Through-Substrate Vias into Integrated Circuit Designs
100142971	I463584	2011-11-23	2014-12-01	Granted	Taiwan	Integration of Shallow Trench Isolation and Through-Substrate Vias into Integrated Circuit Designs
14251258	9613847	2014-04-11	2017-04-04	Granted	United States of America	Integration of Shallow Trench Isolation and Through-Substrate Vias into Integrated Circuit Designs
12151108	7671436	2008-05-02	2010-03-02	Granted	United States of America	Electronic Packages
12969836	8987137	2010-12-16	2015-03-24	Granted	United States of America	Method of Fabrication of Through-Substrate Vias
11973859	7888257	2007-10-10	2011-02-15	Granted	United States of America	Integrated Circuit Package Including Wire Bonds
13921707	9054064	2013-06-19	2015-06-09	Granted	United States of America	Stacked Interconnect Heat Sink
111747341		2011-07-20		Application	European Patent	Stacked Interconnect Heat Sink
2011158573	5885952	2011-07-20	2016-02-19	Granted	Japan	Stacked Interconnect Heat Sink
100121685	I413222	2011-06-21	2013-10-21	Granted	Taiwan	Stacked Interconnect Heat Sink
14678223		2015-04-03		Abandoned	United States of America	Stacked Interconnect Heat Sink
12840016	8492911	2010-07-20	2013-07-23	Granted	United States of America	Stacked Interconnect Heat Sink
1020110071262		2011-07-19		Application	Korea, Republic of (KR)	Stacked Interconnect Heat Sink
2011101997470		2011-07-18		Abandoned	China	Stacked Interconnect Heat Sink
11562537	7982307	2006-11-22	2011-07-19	Granted	United States of America	Integrated Circuit Chip Assembly Having Array Of Thermally Conductive Features Arranged In Aperture Of Circuit Substrate
11460459	7800879	2006-07-27	2010-09-21	Granted	United States of America	On-Chip Sensor Array For Temperature Management In Integrated Circuits
12194706	7973544	2008-08-20	2011-07-05	Granted	United States of America	Thermal Monitoring And Management Of Integrated Circuits
11375302	7479695	2006-03-14	2009-01-20	Lapsed	United States of America	Low Thermal Resistance Assembly for Flip Chip Applications
11158370	8664759	2005-06-22	2014-03-04	Granted	United States of America	Integrated Circuit With Heat Conducting Structures For Localized Thermal Control
11097796	7005880	2005-04-02	2006-02-28	Granted	United States of America	Method Of Testing Electronic Wafers Having Lead-Free Solder Contacts

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10997630	7221042	2004-11-24	2007-05-22	Granted	United States of America	Leadframe Designs For Integrated Circuit Plastic Packages
11015535	7956451	2004-12-18	2011-06-07	Granted	United States of America	Packages For Encapsulated Semiconductor Devices And Method Of Making Same
11095929	7408246	2005-03-31	2008-08-05	Granted	United States of America	Controlling Warping In Integrated Circuit Devices
13041674	8133799	2011-03-07	2012-03-13	Granted	United States of America	Controlling Warping In Integrated Circuit Devices
12163453	7598602	2008-06-27	2009-10-06	Granted	United States of America	Controlling Warping In Integrated Circuit Devices
200696225	5657188	2006-03-31	2014-12-05	Granted	Japan	Controlling Warping In Integrated Circuit Devices
12546083	7923347	2009-08-24	2011-04-12	Granted	United States of America	Controlling Warping In Integrated Circuit Devices
11049407	7242090	2005-02-02	2007-07-10	Granted	United States of America	Device Package
11049246	7235422	2005-02-02	2007-06-26	Granted	United States of America	Device Packages
10788678	7164200	2004-02-27	2007-01-16	Granted	United States of America	Techniques For Reducing Bowing In Power Transistor Devices
10722652	7429703	2003-11-26	2008-09-30	Granted	United States of America	Methods And Apparatus For Integrated Circuit Device Power Distribution Via Internal Wire Bonds
10955912	7367486	2004-09-30	2008-05-06	Granted	United States of America	System And Method For Forming Solder Joints
10702875	7314781	2003-11-05	2008-01-01	Granted	United States of America	Device Packages Having Stable Wirebonds
10960680	7122892	2004-10-07	2006-10-17	Granted	United States of America	Multi-Chip Integrated Circuit Module For High-Frequency Operation
10881191	7009305	2004-06-30	2006-03-07	Granted	United States of America	Methods And Apparatus For Integrated Circuit Ball Bonding Using Stacked Ball Bumps
10150790	6628001	2002-05-17	2003-09-30	Granted	United States of America	Integrated Circuit Die Having Alignment Marks In The Bond Pad Region And Method Of Manufacturing Same
09641899	6476472	2000-08-18	2002-11-05	Granted	United States of America	Integrated Circuit Package With Improved ESD Protection For No-Connect Pins
09614854	6358779	2000-07-12	2002-03-19	Granted	United States of America	A Technique For Reducing Dambar Burrs
09669278	6412680	2000-09-26	2002-07-02	Granted	United States of America	Dual In-Line BGA Ball Mounter

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09781423	6559535	2001-02-13	2003-05-06	Granted	United States of America	Lead Structure For Sealing Package
09465075	6417087	1999-12-16	2002-07-09	Granted	United States of America	Process For Forming A Dual Damascene Bond Pad Structure Over Active Circuitry
09492600	6309097	2000-01-27	2001-10-30	Granted	United States of America	Die Coating Material Stirring Machine
09351220	6276593	1999-07-12	2001-08-21	Granted	United States of America	Apparatus And Method For Solder Attachment Of High Powered Transistors To Base Heatsink
09480014	6252289	2000-01-10	2001-06-26	Granted	United States of America	Electrical Contact And Housing For Use As An Interface Between A Texting Fixture And A Device Under Test
09168638	6043876	1998-10-08	2000-03-28	Granted	United States of America	METHOD AND APPARATUS FOR DETECTING A SOLDER BRIDGE IN A BALL GRID ARRAY
09305732	6140710	1999-05-05	2000-10-31	Granted	United States of America	Power And Ground And Signal Layout For Higher Density Integrated Circuit Connections With Flip-Chip Bonding
09135969	6180241	1998-08-18	2001-01-30	Granted	United States of America	Arrangement For Reducing Bending Stress In An Electronics Package
09221726	6145385	1998-12-29	2000-11-14	Granted	United States of America	Measurement Of Mechanical Fastener Clamping Force
09133606	6028772	1998-08-13	2000-02-22	Granted	United States of America	Electronic Assembly Having Improved Resistance to Delamination
09173502	6110576	1998-10-16	2000-08-29	Granted	United States of America	Article Comprising Molded Circuit
09169117	5955683	1998-10-08	1999-09-21	Granted	United States of America	Method and Appartus for Detecting a Solder Bridge in a Ball Grid Array
09072248	6326685	1998-05-04	2001-12-04	Granted	United States of America	Low Thermal Expansion Composite Comprising Bodies Of Negative CTE Material Disposed Within A Positive CTE Matrix
08825923	5904859	1997-04-02	1999-05-18	Expired	United States of America	Flip Chips Metalization
08979063	6034441	1997-11-26	2000-03-07	Granted	United States of America	Overcast Semiconductor Package
08818813	5897333	1997-03-14	1999-04-27	Expired	United States of America	Method For Forming Integrated Composite Semiconductor Devices
08826606	5783465	1997-04-03	1998-07-21	Granted	United States of America	Compliant Bump Technology

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08803474	5778913	1997-02-20	1998-07-14	Expired	United States of America	Cleaning Solder-Bonded Flip-Chip Assemblies
08761047	5747982	1996-12-05	1998-05-05	Expired	United States of America	Multi-Chip Modules With Isolated Coupling Between Modules
09058505	6125042	1998-04-10	2000-09-26	Granted	United States of America	Ball Grid Array Semiconductor Package Having Improved EMI Characteristics
08498738	5735698	1995-07-06	1998-04-07	Expired	United States of America	Connector for Mounting An Electrical Component
08438296	5622305	1995-05-10	1997-04-22	Expired	United States of America	Bonding Scheme Using Group VB Metallic Layer
08884095	5773322	1997-06-27	1998-06-30	Expired	United States of America	Molded Encapsulated Electronic Component
08486844	5646451	1995-06-07	1997-07-08	Expired	United States of America	Multifunctional Chip Wire Bonds
12689806	8222745	2010-01-19	2012-07-17	Granted	United States of America	INTEGRATED HEAT SINK
08430665	5619068	1995-04-28	1997-04-08	Expired	United States of America	Externally Bondable Overmolded Package Arrangements

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09802198	6651202	2001-03-08	2003-11-18	Granted	United States of America	Built-in self repair circuitry utilizing permanent record of defects
09237769		1999-01-26		Abandoned	United States of America	Built-In Self Repair Circuitry Utilizing Permanent Record Of Defects
08735249	5754444	1996-10-29	1998-05-19	Expired	United States of America	Method and system for improving a placement of cells using energetic placement units alternating contraction and expansion operations
08306385	5568636	1994-09-13	1996-10-22	Expired	United States of America	Method and system for improving a placement of cells using energetic placement with alternating contraction and expansion operations
09081387	6088519	1998-05-18	2000-07-11	Expired	United States of America	Method and system for improving a placement of cells using energetic placement with alternating contraction and expansion operations
09265510	6282696	1999-03-09	2001-08-28	Expired	United States of America	Performing optical proximity correction with the aid of design rule checkers
09035110	5972541	1998-03-04	1999-10-26	Expired	United States of America	Reticle and method of design to correct pattern for depth of focus problems
08912887	5900338	1997-08-15	1999-05-04	Expired	United States of America	Performing optical proximity correction with the aid of design rule checkers
08607398	5705301	1996-02-27	1998-01-06	Expired	United States of America	Performing optical proximity correction with the aid of design rule checkers
08229822		1994-04-19		Abandoned	United States of America	Optimization Processing For Integrated Circuit Physical Design Automation System Using Parallel Moving Windows
08987865	5870313	1997-12-09	1999-02-09	Expired	United States of America	Optimization processing for integrated circuit physical design automation system using parallel moving windows
60236902		2000-09-28		Expired	United States of America	Estimation of Clock Buffer Output resistance
60236752		2000-09-28		Expired	United States of America	Wire Delay Distributed Model
09827434	6880141	2001-04-06	2005-04-12	Lapsed	United States of America	Wire delay distributed model
09771272	6543038	2001-01-26	2003-04-01	Granted	United States of America	Elmore model enhancement
08295094	5638288	1994-08-24	1997-06-10	Expired	United States of America	Separable cells having wiring channels for routing signals between surrounding cells
08871212	5905655	1997-06-09	1999-05-18	Expired	United States of America	Separable cells having wiring channels for routing signals between surrounding cells
09299967	6081659	1999-04-26	2000-06-27	Expired	United States of America	Comparing aerial image to actual photoresist pattern for masking process characterization
08853155	6078738	1997-05-08	2000-06-20	Expired	United States of America	Comparing aerial image to SEM of photoresist or substrate pattern for masking process characterization
08672535	5872718	1996-06-28	1999-02-16	Expired	United States of America	Advanced modular cell placement system
08798598	6067409	1997-02-11	2000-05-23	Expired	United States of America	Advanced modular cell placement system
09444975	6292929	1999-11-22	2001-09-18	Expired	United States of America	Advanced modular cell placement system

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08672937	6026223	1996-06-28	2000-02-15	Expired	United States of America	Advanced modular cell placement system with overlap remover with minimal noise
09503691	6223332	2000-02-14	2001-04-24	Expired	United States of America	Advanced modular cell placement system with overlap remover with minimal noise
08229821	5557533	1994-04-19	1996-09-17	Expired	United States of America	Cell placement alteration apparatus for integrated circuit chip physical design automation system
08724025	5793644	1996-09-17	1998-08-11	Expired	United States of America	Cell placement alteration apparatus for integrated circuit chip physical design automation system
08305217		1994-09-13		Abandoned	United States of America	Method And Apparatus For Computing Minimum Wirelength Position (MWP) For Cell In Cell Placement For Integrated Circuit Chip
08690942	5859781	1996-08-01	1999-01-12	Expired	United States of America	Method and apparatus for computing minimum wirelength position (MWP) for cell in cell placement for integrated circuit chip
11092406	7523426	2005-03-29	2009-04-21	Lapsed	United States of America	Intelligent Timing Analysis and Constraint Generation GUI
14010842	8863053	2013-08-27	2014-10-14	Abandoned	United States of America	Intelligent Timing Analysis and Constraint Generation GUI
12388741	8539407	2009-02-19	2013-09-17	Lapsed	United States of America	Intelligent Timing Analysis and Constraint Generation GUI
08294973	5615126	1994-08-24	1997-03-25	Expired	United States of America	High-speed internal interconnection technique for integrated circuits that reduces the number of signal lines through multiplexing
08782585	5898677	1997-01-13	1999-04-27	Expired	United States of America	Integrated circuit device having a switched routing network
10995777	7434180	2004-11-23	2008-10-07	Lapsed	United States of America	Virtual data representation through selective bidirectional translation
12201575	8156454	2008-08-29	2012-04-10	Lapsed	United States of America	Virtual data representation through selective bidirectional translation
08473543	5659189	1995-06-07	1997-08-19	Expired	United States of America	Layout configuration for an integrated circuit gate array
08665016	5650348	1996-06-11	1997-07-22	Expired	United States of America	Method of making an integrated circuit chip having an array of logic gates
08892827	5773854	1997-07-15	1998-06-30	Expired	United States of America	Method of fabricating a linearly continuous integrated circuit gate array
11832516	7480650	2007-08-01	2009-01-20	Lapsed	United States of America	NQL - Netlist Query Language
10956860	7283995	2004-09-30	2007-10-16	Lapsed	United States of America	NQL--netlist query language
11757229	7568175	2007-06-01	2009-07-28	Lapsed	United States of America	Ramptime Propagation on Designs with Cycles
11004309	7246336	2004-12-03	2007-07-17	Granted	United States of America	Ramptime propagation on designs with cycles
11757200	7818703	2007-06-01	2010-10-19	Lapsed	United States of America	Density Driven Layout for RRAM Configuration Module
11007039	7246337	2004-12-08	2007-07-17	Granted	United States of America	Density driven layout for RRAM configuration module
10306064	6597189	2002-11-27	2003-07-22	Granted	United States of America	Socketless/boardless test interposer card
11324119	RE41516	2005-12-30	2010-08-17	Lapsed	United States of America	Socketless/Boardless Test Interposer Card
10428200	6771085	2003-04-30	2004-08-03	Lapsed	United States of America	Socketless/boardless test interposer card

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11706943	7548844	2007-02-13	2009-06-16	Lapsed	United States of America	Sequential Tester for Longest Prefix Search Engines
10387988	7200785	2003-03-13	2007-04-03	Granted	United States of America	Sequential tester for longest prefix search engines
08991785	6269472	1997-12-12	2001-07-31	Expired	United States of America	Optical proximity correction method and apparatus
08607365	5723233	1996-02-27	1998-03-03	Expired	United States of America	Optical proximity correction method and apparatus
10992941	7146591	2004-11-19	2006-12-05	Lapsed	United States of America	Method of selecting cells in logic restructuring
11551573	7496870	2006-10-20	2009-02-24	Lapsed	United States of America	Method of Selecting Cells in Logic Restructuring
11260517	7472358	2005-10-27	2008-12-30	Granted	United States of America	Method and system for outputting a sequence of commands and data described by a flowchart
12315998	8006209	2008-12-09	2011-08-23	Granted	United States of America	Method And System For Outputting A Sequence Of Commands And Data Described By A Flowchart
12015925	7996804	2008-01-17	2011-08-09	Granted	United States of America	A Skew Management Methodology for Highly Skew Sensitive Applications
13544632	8516425	2012-07-09	2013-08-20	Lapsed	United States of America	Method and computer program for generating grounded shielding wires for signal wiring
13173855	8239813	2011-06-30	2012-08-07	Lapsed	United States of America	Method and Apparatus For Balancing Signal Delay Skew
11351091	7689965	2006-02-09	2010-03-30	Lapsed	United States of America	Generation of an Extracted Timing Model File
12695396	8181138	2010-01-28	2012-05-15	Granted	United States of America	Generation of an Extracted Timing Model File
12463509	8161447	2009-05-11	2012-04-17	Lapsed	United States of America	Automation of Tie Cell Insertion, Optimization and Replacement by Scan Flip-Flops to Increase Fault Coverage
11311515	7546568	2005-12-19	2009-06-09	Lapsed	United States of America	Automation of Tie Cell Insertion, Optimization and Replacement by Scan Flip-Flops to Increase Fault Coverage
13442099	8572543	2012-04-09	2013-10-29	Lapsed	United States of America	Automation of Tie Cell Insertion, Optimization and Replacement by Scan Flip-Flops to Increase Fault Coverage
10977386	7302654	2004-10-29	2007-11-27	Granted	United States of America	Method of automating place and route corrections for an integrated circuit design from physical design validation
10975570		2004-10-27		Abandoned	United States of America	Method of Automating Place and Route Corrections for an Integrated Circuit Design from Physical Design Validation
11017015	7398492	2004-12-20	2008-07-08	Lapsed	United States of America	Rules and directives for validating correct data used in the design of semiconductor products
11027266	7290224	2004-12-31	2007-10-30	Lapsed	United States of America	Guided capture, creation, and seamless integration with scalable complexity of a clock specification into a design flow of an integrated circuit
12120965	7945878	2008-05-15	2011-05-17	Granted	United States of America	Rules and directives for validating correct data used in the design of semiconductor products
11017017	7404156	2004-12-20	2008-07-22	Lapsed	United States of America	Language and templates for use in the design of semiconductor products
12122307	8037448	2008-05-16	2011-10-11	Granted	United States of America	Language and templates for use in the design of semiconductor products

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10620057	6946866	2003-07-15	2005-09-20	Lapsed	United States of America	Measurement of package interconnect impedance using tester and supporting tester
10692110		2003-10-23		Abandoned	United States of America	Novel Solution for Low Cost, Speedy Probe Cards
10448987		1900-01-01		Abandoned	United States of America	Measurement Of Package Interconnect Impedance Using Tester And Supporting Tester Hardware
11758975	7822099	2007-06-06	2010-10-26	Lapsed	United States of America	Digital Gaussian Noise Simulator
10429312	7263470	2003-05-05	2007-08-28	Granted	United States of America	Digital gaussian noise simulator
09879380	6615397	2001-06-12	2003-09-02	Granted	United States of America	Optimal clock timing schedule for an integrated circuit
09756561		2001-01-08		Abandoned	United States of America	Optimal Timing Schedule
11107585	7139991	2005-04-14	2006-11-21	Granted	United States of America	Automatic method and system for instantiating built-in-test (BIST) modules in ASIC memory designs
09978141	6931606	2001-10-15	2005-08-16	Lapsed	United States of America	Automatic method and system for instantiating built-in-test (BIST) modules in ASIC memory designs
60236903		2000-09-28		Expired	United States of America	Checking Validity of Memory Addressing in IDDQ Tools
09879506	6694495	2001-06-12	2004-02-17	Lapsed	United States of America	Method of analyzing static current test vectors for semiconductor integrated circuits
08986753	5838585	1997-12-08	1998-11-17	Expired	United States of America	Physical design automation system and method using monotonically improving linear clusterization
08410049		1995-03-24		Abandoned	United States of America	Physical Design Automation System And Method Using Monotonically Improving Linear Clusterization
09089703	6225143	1998-06-03	2001-05-01	Granted	United States of America	Flip-chip integrated circuit routing to I/O devices
09765827	6674166	2001-01-19	2004-01-06	Granted	United States of America	Flip-chip integrated circuit routing to I/O devices
08994430	6134687	1997-12-19	2000-10-17	Granted	United States of America	Peripheral partitioning and tree decomposition for partial scan
09497521	6505316	2000-02-04	2003-01-07	Granted	United States of America	Peripheral partitioning and tree decomposition for partial scan
09568049	6732310	2000-05-10	2004-05-04	Granted	United States of America	Peripheral partitioning and tree decomposition for partial scan
08655438	5867036	1996-05-29	1999-02-02	Expired	United States of America	Domino scan architecture and domino scan flip-flop for the testing of domino and hybrid CMOS circuits
08947271	6108805	1997-10-08	2000-08-22	Expired	United States of America	Domino scan architecture and domino scan flip-flop for the testing of domino and hybrid CMOS circuits
08438605		1995-05-10		Abandoned	United States of America	Microelectronic Integrated Circuit Including Triangular Semiconductor "Or" Gate Circuit
08567894	5654563	1995-12-06	1997-08-05	Expired	United States of America	Microelectronic integrated circuit including triangular semiconductor "OR" gate devices
09875314	6502222	2001-06-04	2002-12-31	Granted	United States of America	Method of clock buffer partitioning to minimize clock skew for an integrated circuit design
60236900		1900-01-01		Abandoned	United States of America	A Top Level Clock Cell Partitioning
11682914	7395478	2007-03-07	2008-07-01	Lapsed	United States of America	Method of generating test patterns to efficiently screen inline resistance delay defects in complex asics

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10900224	7216280	2004-07-27	2007-05-08	Granted	United States of America	Method of generating test patterns to efficiently screen inline resistance delay defects in complex ASICs
07980492	5666289	1992-11-23	1997-09-09	Expired	United States of America	Flexible design system
07957672		1992-10-07		Abandoned	United States of America	Flexible Integrated Circuit Design
08301687	5587923	1994-09-07	1996-12-24	Expired	United States of America	Method for estimating routability and congestion in a cell placement for integrated circuit chip
08774281	5784289	1996-12-20	1998-07-21	Expired	United States of America	Method for estimating routability and congestion in a cell placement fo integrated circuit chip
10844664	7086015	2004-05-12	2006-08-01	Lapsed	United States of America	Method of optimizing RTL code for multiplex structures
11460680	7594201	2006-07-28	2009-09-22	Lapsed	United States of America	Enhanced Method Of Optimizing Multiplex Structures And Multiplex Control Structures In RTL Code
10684119	6842032	2003-10-10	2005-01-11	Lapsed	United States of America	IDDQ test methodology based on the sensitivity of fault current to power supply variations
09862045	6664801	2001-05-21	2003-12-16	Granted	United States of America	IDDQ test methodology based on the sensitivity of fault current to power supply variations
11421722	7539960	2006-06-01	2009-05-26	Lapsed	United States of America	Reducing A Parasitic Graph In Moment Computation Algorithms In VLSI Systems
12340234	8156466	2008-12-19	2012-04-10	Lapsed	United States of America	Moment Computation Algorithms in VLSI System
10301069	7082583	2002-11-20	2006-07-25	Lapsed	United States of America	Method for reducing a parasitic graph in moment computation in VLSI systems
08229826	5495419	1994-04-19	1996-02-27	Expired	United States of America	Integrated circuit physical design automation system utilizing optimization process decomposition and parallel processing
08559206	5636125	1995-11-13	1997-06-03	Expired	United States of America	Computer implemented method for producing optimized cell placement for integrated circiut chip
08862791	5903461	1997-05-23	1999-05-11	Expired	United States of America	Method of cell placement for an integrated circuit chip comprising chaotic placement and moving windows
08604181	5742510	1996-02-21	1998-04-21	Expired	United States of America	Simultaneous placement and routing (SPAR) method for integrated circuit physical design automation system
08558165	5781439	1995-11-13	1998-07-14	Expired	United States of America	Method for producing integrated circuit chip having optimized cell placement
08600588	5745363	1996-02-13	1998-04-28	Expired	United States of America	Optimization processing for integrated circuit physical design automation system using optimally switched cost function computations
08242246	5459085	1994-05-13	1995-10-17	Expired	United States of America	Gate array layout to accommodate multi angle ion implantation
08424905		1995-04-19		Abandoned	United States of America	Gate Array Layout To Accommodate Multi Angles Ion Implantation
08578050		1995-12-26		Abandoned	United States of America	Gate Array Layout To Accommodate Multi Angles Ion Implantation
08839103	5936285	1997-04-23	1999-08-10	Expired	United States of America	Gate array layout to accommodate multi-angle ion implantation
08925360		1997-09-08		Abandoned	United States of America	Gate Array Layout To Accommodate Multi Angles Ion Implantation

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10937049	7376541	2004-09-09	2008-05-20	Lapsed	United States of America	Accurate pin-based memory power model using arc-based characterization
12150846	7640152	2008-05-01	2009-12-29	Lapsed	United States of America	Accurate Pin-Based Memory Power Model Using Arc-Based Characterization
11266687	7467359	2005-11-03	2008-12-16	Lapsed	United States of America	Decoder using a memory for storing state metrics implementing a decoder trellis
10304289	7017126	2002-11-26	2006-03-21	Lapsed	United States of America	Metacores: design and optimization techniques
60383890		1900-01-01		Abandoned	United States of America	Metacors: Design and Optimization Techniques
12336104	7900184	2008-12-16	2011-03-01	Granted	United States of America	Decoder Using a Memory for Storing State Metrics Implementing a Decoder Trellis
09183292	6174742	1998-10-30	2001-01-16	Granted	United States of America	Off-grid metal layer utilization
09693014	6338972	2000-10-20	2002-01-15	Granted	United States of America	Off-grid metal layer utilization
60973550		2007-09-19		Expired	United States of America	Automated Specification Based Functional Test Generation Infrastructure
12212736	8230263	2008-09-18	2012-07-24	Lapsed	United States of America	Automated Specification Based Functional Test Generation Infrastructure
09895668	6611951	2001-06-29	2003-08-26	Granted	United States of America	Method for estimating cell porosity of hardmacs
60250482		2000-11-30		Expired	United States of America	Seglen Method of Estimating Porosity of Tera Gates
07935449	5300815	1992-08-25	1994-04-05	Expired	United States of America	Technique of increasing bond pad density on a semiconductor die
08430399	5635424	1995-04-28	1997-06-03	Expired	United States of America	High-density bond pad layout arrangements for semiconductor dies, and connecting to the bond pads
08688148		1996-07-29		Abandoned	United States of America	Overmolded Semiconductor Package
07975185	5399898	1992-11-12	1995-03-21	Expired	United States of America	Multi-chip semiconductor arrangements using flip chip dies
08270123		1994-07-01		Abandoned	United States of America	Semiconductor Packaging Technique Yielding Increased Inner Lead Count For A Given Die-Receiving Area
08015947		1993-02-10		Abandoned	United States of America	Floorplanning Techniques Using Multi-Partitioning Based On A Partitions Cost Factor For Non-Square Shaped Partitions
07938690		1992-09-01		Abandoned	United States of America	Ball Bump Array Semiconductor Packages
07400572		1989-08-28		Abandoned	United States of America	Method And Apparatus For Isolation Of Flux Materials In Flip-Chip Manufacturing
08105547	5504035	1993-08-12	1996-04-02	Expired	United States of America	Process for solder ball interconnecting a semiconductor device to a substrate using a noble metal foil embedded interposer substrate
08105269		1993-08-12		Abandoned	United States of America	Optically Transmissive Preformed Planar Structures
08679949	5834799	1996-07-15	1998-11-10	Expired	United States of America	Optically transmissive preformed planar structures
07917894		1992-07-21		Abandoned	United States of America	Ball Bump Array Semiconductor Packages
08382147		1995-02-01		Abandoned	United States of America	Ball Bump Array Semiconductor Packages
07947854	5248903	1992-09-18	1993-09-28	Expired	United States of America	Composite bond pads for semiconductor devices
07984206	5284797	1992-11-30	1994-02-08	Expired	United States of America	Semiconductor bond pads

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08387154	5565385	1995-02-10	1996-10-15	Expired	United States of America	Semiconductor bond pad structure and increased bond pad count per die
08470945	5821624	1995-06-05	1998-10-13	Expired	United States of America	Semiconductor device assembly techniques using preformed planar structures
07993188		1992-12-18		Abandoned	United States of America	Mounting And Connecting Non-Square Semiconductor Dies
08476431	5744856	1900-01-01	1998-04-28	Expired	United States of America	Non-Square Die For Integrated Circuit And Systems Containing The Same
08194241	5410805	1994-02-10	1995-05-02	Expired	United States of America	Method And Apparatus For Isolation Of Flux Materials In Flip-Chip Manufacturing
08079499	5434750	1993-06-18	1995-07-18	Expired	United States of America	Partially-Molded, Pcb Chip Carrier Package For Certain Non-Square Die Shapes
08720219	5744858	1996-09-26	1998-04-28	Expired	United States of America	Semiconductor packaging technique yielding increased inner lead count for a given die-receiving area
07969862		1992-10-28		Abandoned	United States of America	Overmolded Semiconductor Package
08331263		1994-10-28		Abandoned	United States of America	Overmolded Semiconductor Package
08429605	5557150	1995-04-27	1996-09-17	Expired	United States of America	Overmolded semiconductor package
07981096	5299730	1992-11-24	1994-04-05	Expired	United States of America	Method and apparatus for isolation of flux materials in flip-chip manufacturing
07775009	5168346	1991-10-11	1992-12-01	Expired	United States of America	Method and apparatus for isolation of flux materials in flip-chip manufacturing
08428323	5569963	1995-04-25	1996-10-29	Expired	United States of America	Preformed planar structures for semiconductor device assemblies
08105838	5347162	1993-08-12	1994-09-13	Expired	United States of America	Preformed planar structures employing embedded conductors
08432535	5594626	1995-05-02	1997-01-14	Expired	United States of America	Partially-molded, PCB chip carrier package for certain non-square die shapes
07916328	5340772	1992-07-17	1994-08-23	Expired	United States of America	Method of increasing the layout efficiency of dies on a wafer and increasing the ratio of I/O area to active area per die
07978483	5341024	1992-11-18	1994-08-23	Expired	United States of America	Method of increasing the layout efficiency of dies on a wafer, and increasing the ratio of I/O area to active area per die
08664146	5729894	1996-06-14	1998-03-24	Expired	United States of America	Method of assembling ball bump grid array semiconductor packages
07933430	5329157	1992-08-21	1994-07-12	Expired	United States of America	Semiconductor packaging technique yielding increased inner lead count for a given die-receiving area
08251058	5441917	1994-05-31	1995-08-15	Expired	United States of America	Method of laying out bond pads on a semiconductor die
08416457	5532934	1995-04-03	1996-07-02	Expired	United States of America	Floorplanning technique using multi-partitioning based on a partition cost factor for non-square shaped partitions
07576182	5111279	1990-08-30	1992-05-05	Expired	United States of America	Apparatus for isolation of flux materials in flip-chip manufacturing
08106157	5489804	1993-08-12	1996-02-06	Expired	United States of America	Flexible preformed planar structures for interposing between a chip and a substrate

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
07995644	5404047	1992-12-18	1995-04-04	Expired	United States of America	Semiconductor die having a high density array of composite bond pads
07834182	5262927	1992-02-07	1993-11-16	Expired	United States of America	Partially-molded, PCB chip carrier package
08260078	5468681	1994-06-15	1995-11-21	Expired	United States of America	Process for interconnecting conductive substrates using an interposer having conductive plastic filled vias
08333367	5578840	1994-11-02	1996-11-26	Expired	United States of America	Microelectronic integrated circuit structure and method using three directional interconnect routing based on hexagonal geometry
08756032		1996-11-26		Abandoned	United States of America	Microeletronic Integrated Circuit Structure And Method Using Three Directional Interconnect Routing Based On Hexagonal Geometry
08517054		1995-08-21		Abandoned	United States of America	Method And Apparatus for Reducing Intermetal Capacitance in a Microelectronic Device
08517266	5801422	1995-08-21	1998-09-01	Expired	United States of America	Hexagonal SRAM architecture
08517892	6097073	1995-08-21	2000-08-01	Expired	United States of America	Triangular semiconductor or gate
08517236	5789770	1995-08-21	1998-08-04	Expired	United States of America	Hexagonal architecture with triangular shaped cells
08685476		1996-07-24		Abandoned	United States of America	Microelectronic Integrated Circuit Structure And Method Using Three Directional Interconnect Routing Based On Hexagonal Geometry
08517142	6407434	1995-08-21	2002-06-18	Expired	United States of America	Hexagonal architecture
08517153	5742086	1995-08-21	1998-04-21	Expired	United States of America	Hexagonal DRAM array
08517406	5973376	1995-08-21	1999-10-26	Expired	United States of America	Architecture having diamond shaped or parallelogram shaped cells
08517171	5822214	1995-08-21	1998-10-13	Expired	United States of America	CAD for hexagonal architecture
08517582		1995-08-21		Abandoned	United States of America	Method For Minimizing Total Wire Length Of Interconnect In A Microelectronic Device
08517339	5889329	1995-08-21	1999-03-30	Expired	United States of America	Tri-directional interconnect architecture for SRAM
08517189	5872380	1995-08-21	1999-02-16	Expired	United States of America	Hexagonal sense cell architecture
08517508	5777360	1995-08-21	1998-07-07	Expired	United States of America	Hexagonal field programmable gate array architecture
08230023		1994-04-19		Abandoned	United States of America	Simultaneous Placement And Routing
08636349	5875117	1996-04-23	1999-02-23	Expired	United States of America	Simultaneous placement and routing (SPAR) method for integrated circuit physical design automation system
08668084		1996-06-19		Abandoned	United States of America	Low Profile Variable Width Input/Output Cells
08307942	5552333	1994-09-16	1996-09-03	Expired	United States of America	Method for designing low profile variable width input/output cells
08837570	5777354	1997-04-21	1998-07-07	Expired	United States of America	Low profile variable width input/output cells
07937643	5629876	1992-08-31	1997-05-13	Expired	United States of America	Method and apparatus for interim in-situ testing of an electronic system with an inchoate ASIC
08335092		1994-11-07		Abandoned	United States of America	Method And Apparatus For Interim, In-Situ Testing Of An Electronic System With An Inchoate Asic

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08696141	5640337	1996-08-13	1997-06-17	Expired	United States of America	Method and apparatus for interim in-situ testing of an electronic system with an inchoate ASIC
08599107		1996-02-09		Abandoned	United States of America	Method And Apparatus For Interim, In-Situ Testing Of An Electronic System With An Inchoate Asic
07911846	5339262	1992-07-10	1994-08-16	Expired	United States of America	Method and apparatus for interim, in-situ testing of an electronic system with an inchoate ASIC
11184401	7401318	2005-07-19	2008-07-15	Lapsed	United States of America	Method and apparatus for optimizing fragmentation of boundaries for optical proximity correction (OPC) purposes
10739460	6988260	2003-12-18	2006-01-17	Lapsed	United States of America	Method and apparatus for optimizing fragmentation of boundaries for optical proximity correction (OPC) purposes
08252231	5493508	1994-06-01	1996-02-20	Expired	United States of America	Specification and design of complex digital systems
08890174	5910897	1997-07-09	1999-06-08	Expired	United States of America	Specification and design of complex digital systems
08603037		1996-02-16		Abandoned	United States of America	Specification And Design Of Complex Digital Systems
12186159	8037432	2008-08-05	2011-10-11	Granted	United States of America	Method And Apparatus For Mapping Design Memories To Integrated Circuit Layout
11280110	7424687	2005-11-16	2008-09-09	Lapsed	United States of America	Method and apparatus for mapping design memories to integrated circuit layout
11349358	7458044	2006-02-07	2008-11-25	Lapsed	United States of America	CDM ESD event simulation and remediation thereof in application circuits
11349356	7493576	2006-02-07	2009-02-17	Lapsed	United States of America	CDM ESD Event Protection in Application Circuits
12791260	8321826	2010-06-01	2012-11-27	Lapsed	United States of America	METHOD AND APPARATUS OF CORE TIMING PREDICTION OF CORE LOGIC IN THE CHIP-LEVEL IMPLEMENTATION PROCESS THROUGH AN OVER-CORE WINDOW ON A CHIP-LEVEL ROUTING LAYER
13657000	8775995	2012-10-22	2014-07-08	Abandoned	United States of America	METHOD AND APPARATUS OF CORE TIMING PREDICTION OF CORE LOGIC IN THE CHIP-LEVEL IMPLEMENTATION PROCESS THROUGH AN OVER-CORE WINDOW ON A CHIP-LEVEL ROUTING LAYER
13547884	8566769	2012-07-12	2013-10-22	Lapsed	United States of America	Method and Apparatus For Generating Memory Models And Timing Database
12508320	8245168	2009-07-23	2012-08-14	Lapsed	United States of America	Method and Apparatus For Generating Memeory Model And Timing Database
11298894	7584442	2005-12-09	2009-09-01	Lapsed	United States of America	Method and Apparatus For Generating Memeory Model And Timing Database
13407830	8499264	2012-02-29	2013-07-30	Lapsed	United States of America	LOW DEPTH CIRCUIT DESIGN
12248187	8166441	2008-10-09	2012-04-24	Lapsed	United States of America	LOW DEPTH CIRCUIT DESIGN
11079017	7376918	2005-03-11	2008-05-20	Lapsed	United States of America	Probabilistic noise analysis
12046169	7661083	2008-03-11	2010-02-09	Lapsed	United States of America	Probabilistic Noise Analysis
10988087		2004-11-12		Abandoned	United States of America	Process And Apparatus For Applying Apodization To Maskless Optical Direct Write Lithography Processes

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
60535586		2004-01-08		Expired	United States of America	Strong Phase Shift for Maskless Lithography
10993603	7189498	2004-11-19	2007-03-13	Granted	United States of America	Process and apparatus for generating a strong phase shift optical pattern for use in an optical direct write lithography process
10305673	6768958	2002-11-26	2004-07-27	Lapsed	United States of America	Automatic calibration of a masking process simulator
10829408	6868355	2004-04-20	2005-03-15	Lapsed	United States of America	Automatic calibration of a masking process simulator
09034550	6174630	1998-03-03	2001-01-16	Granted	United States of America	Method of proximity correction with relative segmentation
09714370	6532585	2000-11-14	2003-03-11	Granted	United States of America	Method and apparatus for application of proximity correction with relative segmentation
12890336	8527912	2010-09-24	2013-09-03	Lapsed	United States of America	Digitally Obtaining Contours of Fabricated Polygons
11182615	7827509	2005-07-15	2010-11-02	Granted	United States of America	Digitally Obtaining Contours of Fabricated Polygons
10382036	6901573	2003-03-05	2005-05-31	Lapsed	United States of America	Method for evaluating logic functions by logic circuits having optimized number of and/or switches
11055752	7328423	2005-02-10	2008-02-05	Lapsed	United States of America	Method for evaluating logic functions by logic circuits having optimized number of and/or switches
11079439	7620924	2005-03-14	2009-11-17	Lapsed	United States of America	BASE PLATFORMS WITH COMBINED ASIC AND FPGA FEATURES AND PROCESS OF USING THE SAME
12576775	8484608	2009-10-09	2013-07-09	Lapsed	United States of America	BASE PLATFORMS WITH COMBINED ASIC AND FPGA FEATURES AND PROCESS OF USING THE SAME
10924531	7107558	2004-08-23	2006-09-12	Lapsed	United States of America	Method of finding critical nets in an integrated circuit design
10458547	7043708	2003-06-09	2006-05-09	Lapsed	United States of America	Intelligent crosstalk delay estimator for integrated circuit design flow
11216918	7325215	2005-08-31	2008-01-29	Lapsed	United States of America	Timing violation debugging inside place and route tool
11946243	7747975	2007-11-28	2010-06-29	Lapsed	United States of America	Timing Violation debugging inside Place and Route Tool
12779312	8584068	2010-05-13	2013-11-12	Lapsed	United States of America	Timing Violation Debugging Inside Place and Route Tool
12229446	8151237	2008-08-22	2012-04-03	Lapsed	United States of America	Disabling unused IO resources in platform-based integrated circuits
10909603	7430730	2004-08-02	2008-09-30	Lapsed	United States of America	Disabling unused IO resources in platform-based integrated circuits
10246286	6894762	2002-09-17	2005-05-17	Lapsed	United States of America	Dual source lithography for direct write application
11075239	7023530	2005-03-07	2006-04-04	Lapsed	United States of America	Dual source lithography for direct write application
12608469	8332801	2009-10-29	2012-12-11	Lapsed	United States of America	Special Engineering Change Order Cells
10897655	7634748	2004-07-22	2009-12-15	Lapsed	United States of America	Special Engineering Change Order Cells
10699276	6900075	2003-10-31	2005-05-31	Lapsed	United States of America	Mixed LVR and HVR reticle set design for the processing of gate arrays, embedded arrays and rapid chip products
11053505	7057261	2005-02-08	2006-06-06	Lapsed	United States of America	Mixed LVR and HVR reticle set design for the processing of gate arrays, embedded arrays and rapid chip products
12432996	8099708	2009-04-30	2012-01-17	Granted	United States of America	I/O planning with lock and insertion features
11115798	7543261	2005-04-27	2009-06-02	Lapsed	United States of America	I/O planning with lock and insertion features
11054879		2005-02-10		Abandoned	United States of America	System and Method for Coevolutionary Circuit Design
10034839	6889366	2001-12-27	2005-05-03	Lapsed	United States of America	System and method for coevolutionary circuit design

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10155620	7035446	2002-05-22	2006-04-25	Lapsed	United States of America	Quality measurement of an aerial image
11011384	7376260	2004-12-14	2008-05-20	Lapsed	United States of America	Method for post-OPC multi layer overlay quality inspection
11724663	7665058	2007-03-15	2010-02-16	Lapsed	United States of America	Customizable Development and Demonstration Platform for Structured ASICs
10725638	7213224	2003-12-02	2007-05-01	Granted	United States of America	Customizable development and demonstration platform for structured ASICs
10135189		1900-01-01		Abandoned	United States of America	Extended Instruction Sets In A Platform Architecture
10809939	7114133	2004-03-25	2006-09-26	Lapsed	United States of America	Broken symmetry for optimization of resource fabric in a sea-of-platform architecture
10626825	7058906	2003-07-23	2006-06-06	Granted	United States of America	Architecture for a sea of platforms
10044781	6640333	2002-01-10	2003-10-28	Granted	United States of America	Architecture for a sea of platforms
10616623	7096442	2003-07-10	2006-08-22	Lapsed	United States of America	Optimizing IC clock structures by minimizing clock uncertainty
11402146	7356785	2006-04-11	2008-04-08	Lapsed	United States of America	Optimizing IC clock structures by minimizing clock uncertainty
09187505	6314545	1998-11-06	2001-11-06	Expired	United States of America	Quadrature Solutions For 3D Capacitance Extraction
09116158	6051027	1998-07-16	2000-04-18	Expired	United States of America	Efficient Three Dimensional Extraction
08904488	6064808	1997-08-01	2000-05-16	Expired	United States of America	Method And Apparatus For Designing Interconnections And Passive Components In Integrated Circuits And Equivalent Structures By Efficient Parameter Extraction
10634634	7051297	2003-08-04	2006-05-23	Lapsed	United States of America	Method and apparatus for mapping platform-based design to multiple foundry processes
10768588		2004-01-29		Abandoned	United States of America	Method and Apparatus for Mapping Platform-based Design to Multiple Foundry Processes
10768558	7076746	2004-01-29	2006-07-11	Lapsed	United States of America	Method and apparatus for mapping platform-based design to multiple foundry processes
08489270	5689685	1995-06-09	1997-11-18	Expired	United States of America	Apparatus And Method For Analyzing Circuits Using Reduced-Order Modeling Of Large Linear Subcircuits
08269230	5537329	1994-06-30	1996-07-16	Expired	United States of America	Apparatus and Method for Analyzing Circuits
10441000	7047470	2003-05-19	2006-05-16	Lapsed	United States of America	Flexible and extensible implementation of sharing test pins in ASIC
10417007	7284211	2003-04-16	2007-10-16	Lapsed	United States of America	Extensible IO testing implementation
10335360	7055113	2002-12-31	2006-05-30	Lapsed	United States of America	Simplified process to design integrated circuits
11156319	7430725	2005-06-18	2008-09-30	Lapsed	United States of America	Suite of tools to design integrated circuits
10232423	6851098	2002-08-28	2005-02-01	Lapsed	United States of America	Static timing analysis and performance diagnostic display tool
11028403	7181713	2005-01-03	2007-02-20	Granted	United States of America	Static timing and risk analysis tool
08401099	5682323	1995-03-06	1997-10-28	Expired	United States of America	System and method for performing optical proximity correction on macrocell libraries
08937296	6425117	1997-09-29	2002-07-23	Expired	United States of America	System and method for performing optical proximity correction on the interface between optical proximity corrected cells

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09964011	6643832	2001-09-26	2003-11-04	Granted	United States of America	Virtual tree-based netlist model and method of delay estimation for an integrated circuit design
60236953		1900-01-01		Abandoned	United States of America	Delay Estimation for Virtual Tree Based Netlist Model
60236589		1900-01-01		Abandoned	United States of America	An Integrated Adaptive Timing Optimization Technique
09964030	7020589	2001-09-26	2006-03-28	Lapsed	United States of America	Method and apparatus for adaptive timing optimization of an integrated circuit design
10769510	7398501	2004-01-30	2008-07-08	Lapsed	United States of America	System and method for optimizing an integrated circuit design
10021696	6751783	2001-10-30	2004-06-15	Granted	United States of America	System and method for optimizing an integrated circuit design
09756568		2001-01-08		Abandoned	United States of America	Process For Fast Cell Placement In Integrated Circuit Design
09879643	6704915	2001-06-12	2004-03-09	Lapsed	United States of America	Process for fast cell placement in integrated circuit design
60227132		2000-08-22		Expired	United States of America	Method for Reducing VCD File Size For IDDQ Testing
09879417	6449751	2001-06-12	2002-09-10	Granted	United States of America	Method of analyzing static current test vectors with reduced file sizes for semiconductor integrated circuits
10974450		2004-10-27		Abandoned	United States of America	Generalized BIST For Multiport Memories
11775956	8201032	2007-07-11	2012-06-12	Granted	United States of America	Generalized BIST For Multiport Memories
12187464	8468478	2008-08-07	2013-06-18	Granted	United States of America	Methods For Measurement And Prediction Of Hold-Time And Exceeding Hold Time Limits Due To Cells With Tied Input Pins
11377778	7424693	2006-03-16	2008-09-09	Lapsed	United States of America	Methods For Measurement And Prediction Of Hold-Time And Exceeding Hold Time Limits Due To Cells With Tied Input Pins
08598155		1996-02-07		Abandoned	United States of America	Method For Repairing An Asic Memory With Redundancy Row And Input/Output Lines
09052043	6065134	1998-03-30	2000-05-16	Expired	United States of America	Method for repairing an ASIC memory with redundancy row and input/output lines
09880607	6453451	2001-06-12	2002-09-17	Granted	United States of America	Generating standard delay format files with conditional path delay for designing integrated circuits
60237737		2000-09-29		Abandoned	United States of America	Conditional Path Delay SDF Generation
09597433	6625770	2000-06-20	2003-09-23	Granted	United States of America	Method of automatically generating schematic and waveform diagrams for relevant logic cells of a circuit using input signal predictors and transition times
09684770	6671846	2000-10-06	2003-12-30	Lapsed	United States of America	Method of automatically generating schematic and waveform diagrams for isolating faults from multiple failing paths in a circuit using input signal predictors and transition times
13599549		2012-08-30		Abandoned	United States of America	A Systematic, Normalized Metric For Analyzing And Comparing Optimization Techniques For Intergrated Circuits Employing Voltage Scaling And Integrated Circuits Designed Thereby
12365010	8281266	2009-02-03	2012-10-02	Abandoned	United States of America	Systematic, Normalized Metric For Analyzing And Comparing Optimization Techniques For Intergrated Circuits Employing Voltage Scaling And Integrated Circuits Designed Thereby

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
13627054	8595668	2012-09-26	2013-11-26	Lapsed	United States of America	Circuit and Methods for Efficient Clock and Data Delay Configuration for Faster Timing Closure
14057441		2013-10-18		Abandoned	United States of America	Circuit and Methods for Efficient Clock and Data Delay Configuration for Faster Timing Closure
14053194		2013-10-14		Abandoned	United States of America	Total Power Optimization for a Logic Integrated Circuit
13103461	8589853	2011-05-09	2013-11-19	Lapsed	United States of America	Total Power Optimization for a Logic Integrated Circuit
14093189		2013-11-29		Abandoned	United States of America	Circuit Timing Analysis Incorporating The Effects Of Temperature Inversion
13453289	8645888	2012-04-23	2014-02-04	Lapsed	United States of America	Circuit Timing Analysis Incorporating The Effects Of Temperature Inversion
12251088	8181144	2008-10-14	2012-05-15	Granted	United States of America	Circuit Timing Analysis Incorporating The Effects Of Temperature Inversion
12117760	7958473	2008-05-09	2011-06-07	Granted	United States of America	Method And Computer Program For Configuring An Integrated Circuit Design For Static Timing Analysis
11364142		2006-02-27		Abandoned	United States of America	DEVICE FOR ANALYZING LOG FILES GENERATED BY PROCESS AUTOMATION TOOLS
11949187	7975248	2007-12-03	2011-07-05	Granted	United States of America	Staged Scenario Generation
13658336		2012-10-23		Abandoned	United States of America	Staged Scenario Generation
13150607	8423933	2011-06-01	2013-04-16	Granted	United States of America	Staged Scenario Generation
08773469	5995740	1996-12-23	1999-11-30	Expired	United States of America	Method for capturing ASIC I/O pin data for tester compatibility analysis
08650248	6539509	1996-05-22	2003-03-25	Expired	United States of America	Clock skew insensitive scan chain reordering
09072566	6083271	1998-05-05	2000-07-04	Granted	United States of America	Method and apparatus for specifying multiple power domains in electronic circuit designs
09968009	6907586	2001-10-02	2005-06-14	Lapsed	United States of America	Integrated design system and method for reducing and avoiding crosstalk
08745526	5983017	1996-11-12	1999-11-09	Expired	United States of America	Virtual monitor debugging method and apparatus
08671659	6085032	1996-06-28	2000-07-04	Expired	United States of America	Advanced modular cell placement system with sinusoidal optimization
09449324	6542834	1999-11-24	2003-04-01	Granted	United States of America	Capacitance estimation
09400686	6417562	1999-09-22	2002-07-09	Granted	United States of America	Silicon verification with embedded testbenches
09934051	6973421	2001-08-21	2005-12-06	Lapsed	United States of America	BZFLASH subcircuit to dynamically supply BZ codes for controlled impedance buffer development, verification and system level simulations
09928471	6701511	2001-08-13	2004-03-02	Lapsed	United States of America	Optical and etch proximity correction
09735255	6634014	2000-12-12	2003-10-14	Granted	United States of America	Delay/load estimation for use in integrated circuit design
08609397	6038385	1996-03-01	2000-03-14	Expired	United States of America	Physical design automation system and process for designing integrated circuit chip using chessboard and jiggle optimization

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09916958	6951017	2001-07-27	2005-09-27	Lapsed	United States of America	Design system upgrade migration
09515376	6820048	2000-02-29	2004-11-16	Lapsed	United States of America	4 point derating scheme for propagation delay and setup/hold time computation
09118661	6182272	1998-07-16	2001-01-30	Granted	United States of America	Metal layer assignment
09847460	6502230	2001-05-02	2002-12-31	Granted	United States of America	Circuit modeling
09866661	6438730	2001-05-30	2002-08-20	Granted	United States of America	RTL code optimization for resource sharing structures
09115464	6240542	1998-07-14	2001-05-29	Granted	United States of America	Poly routing for chip interconnects with minimal impact on chip performance
2001554268	4580134	2000-01-20	2010-09-03	Lapsed	Japan	Geometric Aerial Image Simulator.
09120617	6412102	1998-07-22	2002-06-25	Granted	United States of America	Wire routing optimization
09062254	6057169	1998-04-17	2000-05-02	Granted	United States of America	Method for I/O device layout during integrated circuit design
09233885	6171731	1999-01-20	2001-01-09	Granted	United States of America	Hybrid aerial image simulation
10153504	3001855	1998-04-23	1999-11-12	Granted	Japan	Optical Proximity Correction Method And Apparatus
08991419	6134702	1997-12-16	2000-10-17	Granted	United States of America	Physical design automation system and process for designing integrated circuit chips using multiway partitioning with constraints
09072570	6327696	1998-05-05	2001-12-04	Granted	United States of America	Method and apparatus for zero skew routing from a fixed H trunk
09042230	6243849	1998-03-13	2001-06-05	Granted	United States of America	Method and apparatus for netlist filtering and cell placement
09410405	6385761	1999-10-01	2002-05-07	Granted	United States of America	Flexible width cell layout architecture
09183637	6275973	1998-10-30	2001-08-14	Granted	United States of America	Integrated circuit design with delayed cell selection
09099287	6305001	1998-06-18	2001-10-16	Granted	United States of America	Clock distribution network planning and method therefor
09027512	6263483	1998-02-20	2001-07-17	Granted	United States of America	Method of accessing the generic netlist created by synopsys design compilier
09085143	6687661	1998-05-26	2004-02-03	Lapsed	United States of America	Utilizing a technology-independent system description incorporating a metal layer dependent attribute
09098172	6128757	1998-06-16	2000-10-03	Granted	United States of America	Low voltage screen for improving the fault coverage of integrated circuit production test programs
09026790	6836877	1998-02-20	2004-12-28	Lapsed	United States of America	Automatic synthesis script generation for synopsys design compiler
09027399	6205572	1998-02-20	2001-03-20	Granted	United States of America	Buffering tree analysis in mapped design
09027501	6289491	1998-02-20	2001-09-11	Granted	United States of America	Netlist analysis tool by degree of conformity
09050824	6178541	1998-03-30	2001-01-23	Granted	United States of America	PLD/ASIC hybrid integrated circuit
08961163	6101458	1997-10-30	2000-08-08	Expired	United States of America	Automatic ranging apparatus and method for precise integrated circuit current measurements
09031956	6093214	1998-02-26	2000-07-25	Granted	United States of America	Standard cell integrated circuit layout definition having functionally uncommitted base cells
09027423	6173435	1998-02-20	2001-01-09	Granted	United States of America	Internal clock handling in synthesis script
09027422	6289498	1998-02-20	2001-09-11	Granted	United States of America	VDHL/Verilog expertise and gate synthesis automation system

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09564062	6473891	2000-05-03	2002-10-29	Granted	United States of America	Wire routing to control skew
09007407	6070259	1998-01-15	2000-05-30	Granted	United States of America	Dynamic logic element having non-invasive scan chain insertion
09050823	6334207	1998-03-30	2001-12-25	Granted	United States of America	Method for designing application specific integrated circuits
13163097	4405599	1997-05-07	2009-11-13	Expired	Japan	Method For Creating And Using Design Shells For Integrated Circuit Designs
09010396	6901571	1998-01-21	2005-05-31	Lapsed	United States of America	Timing-driven placement method utilizing novel interconnect delay model
09062217	6175950	1998-04-17	2001-01-16	Granted	United States of America	Method and apparatus for hierarchical global routing descend
09062218	6253363	1998-04-17	2001-06-26	Granted	United States of America	Net routing using basis element decomposition
09062219	6154874	1998-04-17	2000-11-28	Granted	United States of America	Memory-saving method and apparatus for partitioning high fanout nets
09136971	3937032	1997-05-27	2007-04-06	Lapsed	Japan	Domino Scan Architecture And Domino Scan Flip-Flop For The Testing Of Domino And Hybrid Cmos Circuits
09879297	6442738	2001-06-12	2002-08-27	Granted	United States of America	RTL back annotator
08964784	6000038	1997-11-05	1999-12-07	Granted	United States of America	Parallel processing of Integrated circuit pin arrival times
10014746	6675363	2001-10-24	2004-01-06	Lapsed	United States of America	Graphical user interface to integrate third party tools in power integrity analysis
08906946	6075933	1997-08-06	2000-06-13	Expired	United States of America	Method and apparatus for continuous column density optimization
08906950	6070108	1997-08-06	2000-05-30	Expired	United States of America	Method and apparatus for congestion driven placement
09010395	6109201	1998-01-21	2000-08-29	Granted	United States of America	Resynthesis method for significant delay reduction
08956874	6135647	1997-10-23	2000-10-24	Expired	United States of America	System and method for representing a system level RTL design using HDL independent objects and translation to synthesizable RTL code
09363311	6968286	1999-07-28	2005-11-22	Lapsed	United States of America	Functional-pattern management system for device verification
08906949	6123736	1997-08-06	2000-09-26	Expired	United States of America	Method and apparatus for horizontal congestion removal
08798652	5898597	1997-02-11	1999-04-27	Expired	United States of America	Integrated circuit floor plan optimization system
08914493	6083269	1997-08-19	2000-07-04	Expired	United States of America	Digital integrated circuit design system and methodology with hardware
08779628	5886901	1997-01-07	1999-03-23	Expired	United States of America	Flip-flop for scan test chain
08766650	5987239	1996-12-13	1999-11-16	Expired	United States of America	Computer system and method for building a hardware description language representation of control logic for a complex digital system
08818640	5953518	1997-03-14	1999-09-14	Expired	United States of America	Yield improvement techniques through layout optimization
08719508	5886900	1996-09-25	1999-03-23	Expired	United States of America	Protection of proprietary circuit designs during gate level static timing analysis
08958775	5956350	1997-10-27	1999-09-21	Expired	United States of America	Built in self repair for DRAMs using on-chip temperature sensing and heating

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08819856	5831993	1997-03-17	1998-11-03	Expired	United States of America	Method and apparatus for scan chain with reduced delay penalty
09858166	6507939	2001-05-15	2003-01-14	Granted	United States of America	Net delay optimization with ramptime violation removal
08772309	5804340	1996-12-23	1998-09-08	Expired	United States of America	Photomask inspection method and inspection tape therefor
08798653	5875118	1997-02-11	1999-02-23	Expired	United States of America	Integrated circuit cell placement parallelization with minimal number of conflicts
08760641	5980093	1996-12-04	1999-11-09	Expired	United States of America	Integrated circuit layout routing using multiprocessing
09880675	6928598	2001-06-13	2005-08-09	Lapsed	United States of America	Scan method for built-in-self-repair (BISR)
08661889	5768145	1996-06-11	1998-06-16	Expired	United States of America	Parametrized waveform processor for gate-level power analysis tool
08661888	5835380	1996-06-11	1998-11-10	Expired	United States of America	Simulation based extractor of expected waveforms for gate-level power analysis tool
08626773	5822226	1996-04-02	1998-10-13	Expired	United States of America	Hardware system verification environment tool
08674605	5812740	1996-06-28	1998-09-22	Expired	United States of America	Advanced modular cell placement system with neighborhood system driven optimization
08671656	5844811	1996-06-28	1998-12-01	Expired	United States of America	Advanced modular cell placement system with universal affinity driven discrete placement optimization
08671651	6030110	1996-06-28	2000-02-29	Expired	United States of America	Advanced modular cell placement system with median control and increase in resolution
08609359	5796625	1996-03-01	1998-08-18	Expired	United States of America	Physical design automation system and process for designing integrated circuit chip using simulated annealing with chessboard and jiggle optimization
09849919	6487698	2001-05-04	2002-11-26	Granted	United States of America	Process, apparatus and program for transforming program language description of an IC to an RTL description
09879845	6467067	2001-06-12	2002-10-15	Granted	United States of America	epsilon-discrepant self-test technique
09844361	6513148	2001-04-27	2003-01-28	Lapsed	United States of America	Density driven assignment of coordinates
09085717	6397117	1998-05-28	2002-05-28	Granted	United States of America	Distributed computer aided design system and method
08627823	5844818	1996-05-10	1998-12-01	Expired	United States of America	Method for creating and using design shells for integrated circuit designs
08517054		1995-08-21		Abandoned	United States of America	Method And Apparatus For Reducing Intermetal Capacitance In A Microelectronic Device
08536004	5784287	1995-09-29	1998-07-21	Expired	United States of America	Physical design automation system and process for designing integrated circuit chips using generalized assignment
09814417	6845348	2001-03-21	2005-01-18	Lapsed	United States of America	Driver waveform modeling with multiple effective capacitances
08754142	5907494	1996-11-22	1999-05-25	Expired	United States of America	Computer system and method for performing design automation in a distributed computing environment
08318275	5682321	1994-10-05	1997-10-28	Expired	United States of America	Cell placement method for microelectronic integrated circuit combining clustering, cluster placement and de-clustering

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08517441	5808330	1995-08-21	1998-09-15	Expired	United States of America	Polydirectional non-orthoginal three layer interconnect architecture
08409757	5661663	1995-03-24	1997-08-26	Expired	United States of America	Physical design automation system and method using hierarchical clusterization and placement improvement based on complete re-placement of cell clusters
09062418	6269469	1998-04-17	2001-07-31	Granted	United States of America	Method and apparatus for parallel routing locking mechanism
09062309	6324674	1998-04-17	2001-11-27	Granted	United States of America	Method and apparatus for parallel simultaneous global and detail routing
09234422	6263299	1999-01-19	2001-07-17	Granted	United States of America	Geometric aerial image simulation
12193566	8166428	2008-08-18	2012-04-24	Lapsed	United States of America	Multiplexer Implementation
08974846	6212655	1997-11-20	2001-04-03	Granted	United States of America	IDDQ test solution for large asics
09034544	6499003	1998-03-03	2002-12-24	Granted	United States of America	Method and apparatus for application of proximity correction with unitary segmentation
979322997	69737771.7	1997-06-26	2007-05-30	Expired	Germany (Federal Republic	Modular cell placement system with fast procedure for finding a levelizing cut point
11728366	7669155	2007-03-26	2010-02-23	Lapsed	United States of America	Generic Methodology To Support Chip Level Integration Of IP Core Instance Constraints In Integrated Circuits
11724143	7676773	2007-03-14	2010-03-09	Lapsed	United States of America	Trace optimization in flattened netlist by storing and retrieving intermediate results
11538187	7392496	2006-10-03	2008-06-24	Lapsed	United States of America	Device for avoiding timing violations resulting from process defects in a backfilled metal layer of an integrated circuit
09062310	6230306	1998-04-17	2001-05-08	Granted	United States of America	Method and apparatus for minimization of process defects while routing
11509370	7590957	2006-08-24	2009-09-15	Lapsed	United States of America	Method and Apparatus for Fixing Best Case Hold Time Violations in an Integrated Circuit Design
979322989	69739620.7	1997-06-26	2009-10-14	Expired	Germany (Federal Republic	Advanced Modular Cell Placement System With Affinity Driven Discrete Placement Optimization
11280879	7389484	2005-11-16	2008-06-17	Lapsed	United States of America	Method and apparatus for tiling memories in integrated circuit layout
11295351	7406669	2005-12-06	2008-07-29	Lapsed	United States of America	Timing constraints methodology for enabling clock reconvergence pessimism removal in extracted timing models
11256830	7739471	2005-10-24	2010-06-15	Lapsed	United States of America	High Performance Tiling For RRAM Memory
09892241	6588003	2001-06-26	2003-07-01	Granted	United States of America	Method of control cell placement for datapath macros in integrated circuit designs
11323401	7434198	2005-12-29	2008-10-07	Lapsed	United States of America	Method and computer program product for detecting potential failures in an integrated circuit design after optical proximity correction

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11315959	7720556	2005-12-21	2010-05-18	Lapsed	United States of America	Web-Enabled solutions for Memory compilation to support pre-sales estimation of Memory Size, Performance and Power data for memory components
087978847		2008-08-14		Lapsed	European Patent	System and Method for Designing Integrated Circuits that Employ Adaptive Voltage and Scaling Optimization
11324105	7409660	2005-12-29	2008-08-05	Lapsed	United States of America	Method and end cell library for avoiding substrate noise in an integrated circuit
11116616	7240264	2005-04-28	2007-07-03	Granted	United States of America	Scan test expansion module
11136180	7360178	2005-05-24	2008-04-15	Lapsed	United States of America	Mixed-signal functions using R-cells
11125307	7305646	2005-05-09	2007-12-04	Granted	United States of America	Relocatable mixed-signal functions
11192526	7260801	2005-07-29	2007-08-21	Granted	United States of America	Delay computation speed up and incrementality
10990589	7155688	2004-11-17	2006-12-26	Granted	United States of America	Memory generation and placement
11013641	7210083	2004-12-16	2007-04-24	Granted	United States of America	System and method for implementing postponed quasi-masking test output compression in integrated circuit
11131990	7328386	2005-05-18	2008-02-05	Lapsed	United States of America	Methods for using checksums in X-tolerant test response compaction in scan-based testing of integrated circuits
11097936	7206983	2005-03-31	2007-04-17	Granted	United States of America	Segmented addressable scan architecture and method for implementing scan-based testing of integrated circuits
11012741	7197735	2004-12-15	2007-03-27	Granted	United States of America	Floorplan visualization method using gate count and gate density estimations
10894781	7415691	2004-07-20	2008-08-19	Lapsed	United States of America	Method and system for outputting a sequence of commands and data described by a flowchart
11008854	7363608	2004-12-09	2008-04-22	Lapsed	United States of America	Accelerating PCB development and debug in advance of platform ASIC prototype samples
11246880	7467363	2005-10-07	2008-12-16	Lapsed	United States of America	Method for SRAM bitmap verification
10947618	7174524	2004-09-22	2007-02-06	Granted	United States of America	Method of floorplanning and cell placement for integrated circuit chip architecture with internal I/O ring
10830739	7219321	2004-04-23	2007-05-15	Granted	United States of America	Process and apparatus for memory mapping
10830542	7210113	2004-04-23	2007-04-24	Granted	United States of America	Process and apparatus for placing cells in an IC floorplan
10852902	7042242	2004-05-25	2006-05-09	Lapsed	United States of America	Built-in self test technique for programmable impedance drivers for RapidChip and ASIC drivers
10936016	7038257	2004-09-07	2006-05-02	Lapsed	United States of America	System and method for providing scalability in an integrated circuit
11140392	7340700	2005-05-27	2008-03-04	Lapsed	United States of America	Method for abstraction of manufacturing test access and control ports to support automated RTL manufacturing test insertion flow for reusable modules
10956862	7231623	2004-09-30	2007-06-12	Lapsed	United States of America	Netlist database
10794225	6931297	2004-03-05	2005-08-16	Lapsed	United States of America	Feature targeted inspection

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10848994	7117475	2004-05-18	2006-10-03	Lapsed	United States of America	Method and system for utilizing an isofocal contour to perform optical and process corrections
11006349	7373626	2004-12-06	2008-05-13	Lapsed	United States of America	Method and timing harness for system level static timing analysis
10740359	7039896	2003-12-18	2006-05-02	Lapsed	United States of America	Gradient method of mask edge correction
10859857	7065734	2004-06-02	2006-06-20	Lapsed	United States of America	Method of generating multiple hardware description language configurations for a phase locked loop from a single generic model for integrated circuit design
10847691	7360133	2004-05-18	2008-04-15	Lapsed	United States of America	Method for creating a JTAG tap controller in a slice for use during custom instance creation to avoid the need of a boundary scan synthesis tool
10847692	7188330	2004-05-18	2007-03-06	Granted	United States of America	Handling of unused coreware with embedded boundary scan chains to avoid the need of a boundary scan synthesis tool during custom instance creation
10767314	6888367	2004-01-28	2005-05-03	Lapsed	United States of America	Method and apparatus for testing integrated circuit core modules
10740284	7269803	2003-12-18	2007-09-11	Granted	United States of America	System and method for mapping logical components to physical locations in an integrated circuit design environment
10706127	7409602	2003-11-12	2008-08-05	Lapsed	United States of America	Methodology for debugging RTL simulations of processor based system on chip
09994299	6966020	2001-11-26	2005-11-15	Granted	United States of America	Identifying Faulty Programmable Interconnect Resources Of Field Programmable Gate Arrays
08866755	5983007	1997-05-30	1999-11-09	Expired	United States of America	Low Power Circuits Through Hazard Pulse Suppression
08853578	5966516	1997-05-09	1999-10-12	Expired	United States of America	Apparatus For Defining Properties In Finite-State Machines
08832487	5867416	1997-04-02	1999-02-02	Expired	United States of America	Efficient Frequency Domain Analysis Of Large Nonlinear Analog Circuits Using Compressed Matrix Storage
10697357	7107559	2003-10-29	2006-09-12	Lapsed	United States of America	Method of partitioning an integrated circuit design for physical design verification
10693075	7111269	2003-10-23	2006-09-19	Lapsed	United States of America	Comparison of two hierarchical netlist to generate change orders for updating an integrated circuit layout
10683369	7260803	2003-10-10	2007-08-21	Granted	United States of America	Incremental dummy metal insertions
10673721	7024637	2003-09-29	2006-04-04	Lapsed	United States of America	Functionality based package design for integrated circuit blocks
10633856	6988252	2003-08-04	2006-01-17	Lapsed	United States of America	Universal gates for ICs and transformation of netlists for their implementation
10106960	7017096	2002-03-26	2006-03-21	Lapsed	United States of America	Sequential Test Pattern Generation Using Clock-Control Design For Testability Structures
10952194	7231625	2004-09-28	2007-06-12	Granted	United States of America	Method and apparatus for use of hidden decoupling capacitors in an integrated circuit design
10620581	7743391	2003-07-15	2010-06-22	Lapsed	United States of America	Flexible Architecture Component (FAC) for Efficient Data Integration and Information Interchange using Web Services

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10992031	7174532	2004-11-18	2007-02-06	Granted	United States of America	Method Of Making A Semiconductor Device By Balancing Shallow Trench Isolation Stress and Optical Proximity Effects
10624347	7096440	2003-07-22	2006-08-22	Lapsed	United States of America	Methods and systems for automatic verification of specification document to hardware design
09291157	6356861	1999-04-12	2002-03-12	Granted	United States of America	Deriving Statistical Device Models From Worst-Case Files
10704922	7082589	2003-11-10	2006-07-25	Lapsed	United States of America	Method of generating a schematic driven layout for a hierarchical integrated circuit design
11015114	7185298	2004-12-17	2007-02-27	Granted	United States of America	Method of parasitic extraction from a previously calculated capacitance solution
10649215	7076759	2003-08-26	2006-07-11	Lapsed	United States of America	Methodology for generating a modified view of a circuit layout
10453819	6948142	2003-06-02	2005-09-20	Lapsed	United States of America	Intelligent engine for protection against injected crosstalk delay
10757752	7065721	2004-01-14	2006-06-20	Lapsed	United States of America	Optimized bond out method for flip chip wafers
10425155	6728936	2003-04-29	2004-04-27	Granted	United States of America	Datapath bitslice technology
094139974	I372347	2005-11-14	2012-09-11	Lapsed	Taiwan	Method Of Making A Semiconductor Device By Balancing Shallow Trench Isolation Stress and Optical Proximity Effects
10452260	7899659	2003-06-02	2011-03-01	Granted	United States of America	Recording and Displaying Logic Circuit Simulation Waveforms
10810294	7200832	2004-03-26	2007-04-03	Granted	United States of America	Macro cell for integrated circuit physical layer interface
09268902	7016794	1999-03-16	2006-03-21	Lapsed	United States of America	Floor plan development electromigration and voltage drop analysis tool
10339821	6898770	2003-01-09	2005-05-24	Granted	United States of America	Split and merge design flow concept for fast turnaround time of circuit layout design
10254616	6804811	2002-09-25	2004-10-12	Granted	United States of America	Process for layout of memory matrices in integrated circuits
10417706	7127698	2003-04-17	2006-10-24	Lapsed	United States of America	Method for reducing reticle set cost
09808510	6532572	2001-03-14	2003-03-11	Granted	United States of America	Method for estimating porosity of hardmacs
09268867	6675139	1999-03-16	2004-01-06	Granted	United States of America	Floor plan-based power bus analysis and design tool for integrated circuits
10285301	7322021	2002-10-31	2008-01-22	Lapsed	United States of America	Virtual path for interconnect fabric using bandwidth process
09684868	6829751	2000-10-06	2004-12-07	Lapsed	United States of America	Diagnostic architecture using FPGA core in system on a chip design
10318623	7069523	2002-12-13	2006-06-27	Granted	United States of America	Automated selection and placement of memory during design of an integrated circuit
10290019	6961915	2002-11-06	2005-11-01	Granted	United States of America	Design methodology for dummy lines
10210651	6857108	2002-07-31	2005-02-15	Lapsed	United States of America	Interactive representation of structural dependencies in semiconductor design flows
10241317	7043703	2002-09-11	2006-05-09	Lapsed	United States of America	Architecture and/or method for using input/output affinity region for flexible use of hard macro I/O buffers
10330929	7313508	2002-12-27	2007-12-25	Granted	United States of America	Process window compliant corrections of design layout
10166797	6735747	2002-06-10	2004-05-11	Lapsed	United States of America	Pre-silicon verification path coverage
10108286	6842750	2002-03-27	2005-01-11	Lapsed	United States of America	Symbolic simulation driven netlist simplification

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10602570	7020865	2003-06-24	2006-03-28	Lapsed	United States of America	Process for designing comparators and adders of small depth
10194134	6532431	2002-07-12	2003-03-11	Granted	United States of America	Ratio testing
10192989	6810505	2002-07-10	2004-10-26	Lapsed	United States of America	Integrated circuit design flow with capacitive margin
10072008	6701503	2002-02-07	2004-03-02	Lapsed	United States of America	Overlap remover manager
10097419	6813758	2002-03-14	2004-11-02	Lapsed	United States of America	Optical proximity correction driven hierarchy
10163208	6829754	2002-06-04	2004-12-07	Lapsed	United States of America	Method and system for checking for power errors in ASIC designs
10083411	6757877	2002-02-27	2004-06-29	Lapsed	United States of America	System and method for identifying and eliminating bottlenecks in integrated circuit designs
09735233	6341092	2000-12-11	2002-01-22	Granted	United States of America	Designing memory for testability to support scan capability in an asic design
09991574	6550045	2001-11-20	2003-04-15	Granted	United States of America	Changing clock delays in an integrated circuit for skew optimization
10008089	6651239	2001-11-13	2003-11-18	Granted	United States of America	Direct transformation of engineering change orders to synthesized IC chip designs
09800532	6594807	2001-03-06	2003-07-15	Granted	United States of America	Method for minimizing clock skew for an integrated circuit
09106890	6480989	1998-06-29	2002-11-12	Granted	United States of America	Integrated circuit design incorporating a power mesh
09997757	6745358	2001-11-30	2004-06-01	Lapsed	United States of America	Enhanced fault coverage
10021414	6654946	2001-10-30	2003-11-25	Granted	United States of America	Interscalable interconnect
09836129	6598213	2001-04-16	2003-07-22	Granted	United States of America	Static timing analysis validation tool for ASIC cores
09788257	6480994	2001-02-15	2002-11-12	Granted	United States of America	Balanced clock placement for integrated circuits containing megacells
09885596	6507937	2001-06-19	2003-01-14	Granted	United States of America	Method of global placement of control cells and hardmac pins in a datapath macro for an integrated circuit design
09882114	6609238	2001-06-15	2003-08-19	Granted	United States of America	Method of control cell placement to minimize connection length and cell delay
09573806	6470484	2000-05-18	2002-10-22	Granted	United States of America	System and method for efficient layout of functionally extraneous cells
09678481	6532582	2000-10-02	2003-03-11	Granted	United States of America	Method and apparatus for optimal critical netlist area selection
09523224	6546538	2000-03-10	2003-04-08	Granted	United States of America	Integrated circuit having on-chip capacitors for supplying power to portions of the circuit requiring high-transient peak power
09678201	6587990	2000-10-01	2003-07-01	Granted	United States of America	Method and apparatus for formula area and delay minimization
09685990	6519746	2000-10-10	2003-02-11	Granted	United States of America	Method and apparatus for minimization of net delay by optimal buffer insertion
09494605	6425114	2000-01-31	2002-07-23	Granted	United States of America	Systematic skew reduction through buffer resizing
09828553	6766499	2001-04-05	2004-07-20	Lapsed	United States of America	Buffer cell insertion and electronic design automation
09207191	6308292	1998-12-08	2001-10-23	Granted	United States of America	File driven mask insertion for automatic test equipment test pattern generation
09052914	6028995	1998-03-31	2000-02-22	Granted	United States of America	Method of determining delay in logic cell models

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09972100	6792579	2001-10-05	2004-09-14	Lapsed	United States of America	Spice to verilog netlist translator and design methods using spice to verilog and verilog to spice translation
08862233	5995730	1997-05-23	1999-11-30	Expired	United States of America	Method for generating format-independent electronic circuit representations
08940912	5903577	1997-09-30	1999-05-11	Expired	United States of America	Method and apparatus for analyzing digital circuits
08829520	5977574	1997-03-28	1999-11-02	Expired	United States of America	High density gate array cell architecture with sharing of well taps between cells
09515250	6484297	2000-02-29	2002-11-19	Granted	United States of America	4K derating scheme for propagation delay and setup/hold time computation
09045190	6028440	1998-03-20	2000-02-22	Granted	United States of America	Estimation of voltage drop and current densities in ASIC power supply mesh
09017378	6202196	1998-02-03	2001-03-13	Granted	United States of America	Method for optimizing routing mesh segment width
09113995	6714903	1998-07-10	2004-03-30	Granted	United States of America	Placement and routing of circuits using a combined processing/buffer cell
08964997	6292924	1997-11-05	2001-09-18	Granted	United States of America	Modifying timing graph to avoid given set of paths
09007242	6189131	1998-01-14	2001-02-13	Granted	United States of America	Method of selecting and synthesizing metal interconnect wires in integrated circuits
09344169	7596483	1999-06-24	2009-09-29	Lapsed	United States of America	Determining Timing of Integrated Circuits
08613040	5698873	1996-03-08	1997-12-16	Expired	United States of America	High density gate array base cell architecture
08906945	6068662	1997-08-06	2000-05-30	Expired	United States of America	Method and apparatus for congestion removal
08906947	6186676	1997-08-06	2001-02-13	Expired	United States of America	Method and apparatus for determining wire routing
08906948	6058254	1997-08-06	2000-05-02	Expired	United States of America	Method and apparatus for vertical congestion removal
09062432	6247167	1998-04-17	2001-06-12	Granted	United States of America	Method and apparatus for parallel Steiner tree routing
08863798	5822228	1997-05-27	1998-10-13	Expired	United States of America	Method for using built in self test to characterize input-to-output delay time of embedded cores and other integrated circuits
08798880	5930500	1997-02-11	1999-07-27	Expired	United States of America	Parallel processor implementation of net routing
08798648	5859782	1997-02-11	1999-01-12	Expired	United States of America	Efficient multiprocessing for cell placement of integrated circuits
08771004	5898705	1996-12-23	1999-04-27	Expired	United States of America	Method for detecting bus shorts in semiconductor devices
08735450	5880377	1996-10-15	1999-03-09	Expired	United States of America	Method for low velocity measurement of fluid flow
08772400	5974248	1996-12-23	1999-10-26	Expired	United States of America	Intermediate test file conversion and comparison
08641444	5808900	1996-04-30	1998-09-15	Expired	United States of America	Memory having direct strap connection to power supply
08672423	5971588	1996-06-28	1999-10-26	Expired	United States of America	Advanced modular cell placement system with optimization of cell neighborhood system
08672333	5835381	1996-06-28	1998-11-10	Expired	United States of America	Advanced modular cell placement system with minimizing maximal cut driven affinity system
09871129	6463572	2001-05-31	2002-10-08	Granted	United States of America	IC timing analysis with known false paths
09882899	6581194	2001-06-15	2003-06-17	Granted	United States of America	Method for reducing simulation overhead for external models
08434660	5619420	1995-05-04	1997-04-08	Expired	United States of America	Semiconductor cell having a variable transistor width

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08477490	5703788	1995-06-07	1997-12-30	Expired	United States of America	Configuration management and automated test system ASIC design software
08683287	5812416	1996-07-18	1998-09-22	Expired	United States of America	Integrated circuit design decomposition
08396541	6005264	1995-03-01	1999-12-21	Expired	United States of America	Microelectronic integrated circuit including hexagonal CMOS NAND gate device
08377844	5644498	1995-01-25	1997-07-01	Expired	United States of America	Timing shell generation through netlist reduction
08367556	5665989	1995-01-03	1997-09-09	Expired	United States of America	Programmable microsystems in silicon
08580908	5990502	1995-12-29	1999-11-23	Expired	United States of America	High density gate array cell architecture with metallization routing tracks having a variable pitch
08229616	6493658	1994-04-19	2002-12-10	Granted	United States of America	Optimization processing for integrated circuit physical design automation system using optimally switched fitness improvement algorithms
08229949	5682322	1994-04-19	1997-10-28	Expired	United States of America	Optimization processing for integrated circuit physical design automation system using chaotic fitness improvement method
08306189	5638293	1994-09-13	1997-06-10	Expired	United States of America	Optimal pad location method for microelectronic circuit cell placement
08451177	5898595	1995-05-26	1999-04-27	Expired	United States of America	Automated generation of megacells in an integrated circuit design system
09879841	6868535	2001-06-12	2005-03-15	Lapsed	United States of America	Method and apparatus for optimizing the timing of integrated circuits
09842350	6470487	2001-04-25	2002-10-22	Granted	United States of America	Parallelization of resynthesis
09841825	6553551	2001-04-25	2003-04-22	Granted	United States of America	Timing recomputation
09833142	6453453	2001-04-11	2002-09-17	Granted	United States of America	Process for solving assignment problems in integrated circuit designs with unimodal object penalty functions and linearly ordered set of boxes
08229624	5914887	1994-04-19	1999-06-22	Expired	United States of America	Congestion based cost factor computing apparatus for integrated circuit physical design automation system
09804939	6505336	2001-03-13	2003-01-07	Lapsed	United States of America	Channel router with buffer insertion
09849691	7076406	2001-05-04	2006-07-11	Lapsed	United States of America	Minimal bends connection models for wire density calculation
13058176	8539424	2011-02-08	2013-09-17	Lapsed	United States of America	SYSTEM AND METHOD FOR DESIGNING INTERGRATED CIRCUITS THAT EMPLOY ADAPTIVE VOLTAGE SCALING OPTIMIZATION
08672235	5808899	1996-06-28	1998-09-15	Expired	United States of America	Advanced modular cell placement system with cell placement crystallization
08672652	5870312	1996-06-28	1999-02-09	Expired	United States of America	Advanced modular cell placement system with dispersion-driven levelizing system
08672334	5914888	1996-06-28	1999-06-22	Expired	United States of America	Advanced modular cell placement system with coarse overflow remover

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08672936	5963455	1996-06-28	1999-10-05	Expired	United States of America	Advanced modular cell placement system with functional sieve optimization technique
08672725	5831863	1996-06-28	1998-11-03	Expired	United States of America	Advanced modular cell placement system with wire length driven affinity system
08672534	5867398	1996-06-28	1999-02-02	Expired	United States of America	Advanced modular cell placement system with density driven capacity penalty system
08672335	5892688	1996-06-28	1999-04-06	Expired	United States of America	Advanced modular cell placement system with iterative one dimensional preplacement optimization
08608609	5796265	1996-02-29	1998-08-18	Expired	United States of America	Method for metal delay testing in semiconductor devices
09879664	6934410	2001-06-12	2005-08-23	Lapsed	United States of America	Mask correction for photolithographic processes
08586174	5787114	1996-01-17	1998-07-28	Expired	United States of America	Loop-back test system and method
08545879	5668745	1995-10-20	1997-09-16	Expired	United States of America	Method and apparatus for testing of semiconductor devices
09820059	6487697	2001-03-28	2002-11-26	Granted	United States of America	Distribution dependent clustering in buffer insertion of high fanout nets
08560834	5835378	1995-11-20	1998-11-10	Expired	United States of America	Computer implemented method for leveling interconnect wiring density in a cell placement for an integrated circuit chip
08560588	5712793	1995-11-20	1998-01-27	Expired	United States of America	Physical design automation system and process for designing integrated circuit chips using fuzzy cell clusterization
08477827	5663017	1995-06-07	1997-09-02	Expired	United States of America	Optical corrective techniques with reticle formation and reticle stitching to provide design flexibility
08517451	5864165	1995-08-21	1999-01-26	Expired	United States of America	Triangular semiconductor NAND gate
09802043	6545288	2001-03-08	2003-04-08	Granted	United States of America	Gridless router using maze and line probe techniques
08525839	5699265	1995-09-08	1997-12-16	Expired	United States of America	Physical design automation system and process for designing integrated circuit chips using multiway partitioning with constraints
08229954	5815403	1994-04-19	1998-09-29	Expired	United States of America	Fail-safe distributive processing method for producing a highest fitness cell placement for an integrated circuit chip
08306182	5619419	1994-09-13	1997-04-08	Expired	United States of America	Method of cell placement for an itegrated circuit chip comprising integrated placement and cell overlap removal
09837492	6526553	2001-04-18	2003-02-25	Granted	United States of America	Chip core size estimation
08268920	5568395	1994-06-29	1996-10-22	Expired	United States of America	Modeling and estimating crosstalk noise and detecting false logic
11376781	7577928	2006-03-15	2009-08-18	Lapsed	United States of America	Verification of an Extracted Timing Model File
08668064	5867395	1996-06-19	1999-02-02	Expired	United States of America	Gate netlist to register transfer level conversion tool
08616070	5638380	1996-03-14	1997-06-10	Expired	United States of America	Protecting proprietary asic design information using boundary scan on selective inputs and outputs
08611325	5903578	1996-03-08	1999-05-11	Expired	United States of America	Test shells for protecting proprietary information in asic cores
08661186	5691910	1996-06-10	1997-11-25	Expired	United States of America	Generic gate level model for characterization of glitch power in logic cells

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08671699	5870311	1996-06-28	1999-02-09	Expired	United States of America	Advanced modular cell placement system with fast procedure for finding a levelizing cut point
09027520	6292931	1998-02-20	2001-09-18	Granted	United States of America	RTL analysis tool
08560848	5909376	1995-11-20	1999-06-01	Expired	United States of America	Physical design automation system and process for designing integrated circuit chips using highly parallel sieve optimization with multiple jiggles
08491433	5825659	1995-06-16	1998-10-20	Expired	United States of America	Method for local rip-up and reroute of signal paths in an IC design
08683396	5903475	1996-07-18	1999-05-11	Expired	United States of America	System simulation for testing integrated circuit models
08545462	5663967	1995-10-19	1997-09-02	Expired	United States of America	Defect isolation using scan-path testing and electron beam probing in multi-level high density asics
11765691	7849422	2007-06-20	2010-12-07	Granted	United States of America	Efficient Cell Swapping Algorithm for Leakage Power Reduction in A Multi-Threshold Voltage Process
09879846	6611953	2001-06-12	2003-08-26	Granted	United States of America	Mask correction optimization
09062205	6289495	1998-04-17	2001-09-11	Granted	United States of America	Method and apparatus for local optimization of the global routing
11634683	7546560	2006-12-06	2009-06-09	Lapsed	United States of America	Optimization of Flipflop Initialization Structures with Respect to Design Size and Design Closure Effort from RTL to Netlist
2006100841680	ZL 200610084168.0	2006-04-06	2010-05-12	Lapsed	China	Integrated Circuit With Relocatable Processor Hardmac
09841824	6637016	2001-04-25	2003-10-21	Granted	United States of America	Assignment of cell coordinates
09885589	6550044	2001-06-19	2003-04-15	Granted	United States of America	Method in integrating clock tree synthesis and timing optimization for an integrated circuit design
11321260	7480878	2005-12-29	2009-01-20	Lapsed	United States of America	Method and Computer Program Product for Trimming the Analysis of Physical Layout Versus Schematic Design Comparison
11271991	7325216	2005-11-09	2008-01-29	Lapsed	United States of America	Method and computer program for spreading trace segments in an integrated circuit package design
08230383	6155725	1994-04-19	2000-12-05	Granted	United States of America	Cell placement representation and transposition for integrated circuit physical design automation system
11247630	7441210	2005-10-11	2008-10-21	Lapsed	United States of America	On-the-fly RTL instructor for advanced DFT and design closure
08441539	5768130	1995-05-15	1998-06-16	Expired	United States of America	Method of calculating macrocell power and delay values
12072478	8539411	2008-02-26	2013-09-17	Lapsed	United States of America	Multiple Derating Factor Sets for Delay Calculation and Library Generation in Multi-Corner STA Sign-Off Flow
09062246	6260183	1998-04-17	2001-07-10	Granted	United States of America	Method and apparatus for coarse global routing
2011522952		2008-08-14		Abandoned	Japan	System and Method for Designing Integrated Circuits that Employ Adaptive Voltage and Scaling Optimization
11244486	7370309	2005-10-05	2008-05-06	Lapsed	United States of America	Method and computer program for detailed routing of an integrated circuit design with multiple routing rules and net constraints
08907183	6182269	1997-08-06	2001-01-30	Expired	United States of America	Method and device for fast and accurate parasitic extraction

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
030262091	60334275.2	2003-11-14	2010-09-22	Granted	Germany (Federal Republic	Method and System for Classifying an Integrated Circuit for Optical Proximity Correction
09848489	6493851	2001-05-03	2002-12-10	Granted	United States of America	Method and apparatus for indentifying causes of poor silicon-to-simulation correlation
981064298	69830782.8	1998-04-08	2005-07-06	Granted	Germany (Federal Republic	Optical Proximity Correction Method And Apparatus
11204670	7469398	2005-08-16	2008-12-23	Lapsed	United States of America	IP placement validation
11478044	7490307	2006-06-29	2009-02-10	Lapsed	United States of America	Automatic generation of timing constraints for the validation/signoff of test structures
11732092	7496867	2007-04-02	2009-02-24	Lapsed	United States of America	Cell Library Management for Power Optimization
11258738	7401313	2005-10-26	2008-07-15	Lapsed	United States of America	Method and apparatus for controlling congestion during integrated circuit design resynthesis
11257206	7380223	2005-10-24	2008-05-27	Lapsed	United States of America	Method and system for converting netlist of integrated circuit between libraries
09027429	6378123	1998-02-20	2002-04-23	Granted	United States of America	Method of handling macro components in circuit design synthesis
09027283	6295636	1998-02-20	2001-09-25	Granted	United States of America	RTL analysis for improved logic synthesis
098137820	I406147	2009-11-06	2013-08-21	Lapsed	Taiwan	System and Method for Designing Integrated Circuits that Employ Adaptive Voltage and Scaling Optimization
11194299	7464345	2005-08-01	2008-12-09	Lapsed	United States of America	Resource estimation for design planning
09027438	6421818	1998-02-20	2002-07-16	Granted	United States of America	Efficient top-down characterization method
09876736	6442737	2001-06-06	2002-08-27	Granted	United States of America	Method of generating an optimal clock buffer set for minimizing clock skew in balanced clock trees
11465662	7480881	2006-08-18	2009-01-20	Lapsed	United States of America	Method and Computer Program for Static Timing Analysis with Delay De-Rating and Clock Conservatism Reduction
08409191	6345378	1995-03-23	2002-02-05	Granted	United States of America	Synthesis shell generation and use in ASIC design
11099772	7313775	2005-04-06	2007-12-25	Granted	United States of America	Integrated circuit with relocatable processor hardmac
11176514	7451426	2005-07-07	2008-11-11	Lapsed	United States of America	Application specific configurable logic IP
11323468	7458060	2005-12-30	2008-11-25	Lapsed	United States of America	Yield-limiting design-rules-compliant pattern library generation and layout inspection
11074173	7299431	2005-03-07	2007-11-20	Granted	United States of America	Method for tracing paths within a circuit
11133815	7478354	2005-05-20	2009-01-13	Granted	United States of America	Use of configurable mixed-signal building block functions to accomplish custom functions
11205365	7512918	2005-08-17	2009-03-31	Lapsed	United States of America	Multimode Delay Analysis for Simplifying Integrated Circuit Design Timing Models
11000104	7200826	2004-11-30	2007-04-03	Granted	United States of America	RRAM memory timing learning tool
11061292	7202656	2005-02-18	2007-04-10	Granted	United States of America	Methods and structure for improved high-speed TDF testing using on-chip PLL
11036822	7207021	2005-01-14	2007-04-17	Granted	United States of America	Method for estimating a frequency-based ramptime limit

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11244530	7415687	2005-10-05	2008-08-19	Lapsed	United States of America	Method and computer program for incremental placement and routing with nested shells
10936202	7194717	2004-09-08	2007-03-20	Granted	United States of America	Compact custom layout for RRAM column controller
10929218	7191424	2004-08-30	2007-03-13	Granted	United States of America	Special tie-high/low cells for single metal layer route changes
11324084	7617427	2005-12-29	2009-11-10	Lapsed	United States of America	Method and Apparatus for Detecting Defects in Integrated Circuit Die from Simulation of Statistical Outlier Signatures
10914921	7168055	2004-08-10	2007-01-23	Granted	United States of America	Method and apparatus for detecting nets physically changed and electrically affected by design ECO
10186263	7127692	2002-06-27	2006-10-24	Granted	United States of America	Timing abstraction and partitioning strategy
10984115	7380228	2004-11-08	2008-05-27	Lapsed	United States of America	Method of associating timing violations with critical structures in an integrated circuit design
10947498	7149989	2004-09-22	2006-12-12	Granted	United States of America	Method of early physical design validation and identification of texted metal short circuits in an integrated circuit design
11204669	7299446	2005-08-16	2007-11-20	Granted	United States of America	Enabling efficient design reuse in platform ASICs
11243839	7406671	2005-10-05	2008-07-29	Lapsed	United States of America	Method for performing design rule check of integrated circuit
10862049	7223616	2004-06-04	2007-05-29	Granted	United States of America	Test structures in unused areas of semiconductor integrated circuits and methods for designing the same
10975981	7181712	2004-10-27	2007-02-20	Granted	United States of America	Method of optimizing critical path delay in an integrated circuit design
11413236	7739639	2006-04-28	2010-06-15	Lapsed	United States of America	METHOD AND APPARATUS OF CORE TIMING PREDICTION OF CORE LOGIC IN THE CHIP-LEVEL IMPLEMENTATION PROCESS THROUGH AN OVER-CORE WINDOW ON A CHIP-LEVEL ROUTING LAYER
10817419	7620743	2004-04-01	2009-11-17	Lapsed	United States of America	System And Method For Implementing Multiple Instantiated Configurable Peripherals In A Circuit Design
10794683	7264906	2004-03-05	2007-09-04	Granted	United States of America	OPC based illumination optimization with mask error constraints
11165778	7178121	2005-06-24	2007-02-13	Granted	United States of America	Method and computer program for estimating speed-up and slow-down net delays for an integrated circuit design
09885896	6650139	2001-06-20	2003-11-18	Lapsed	United States of America	Modular collection of spare gates for use in hierarchical integrated circuit design process
10819254	7185301	2004-04-06	2007-02-27	Granted	United States of America	Generic method and apparatus for implementing source synchronous interface in platform ASIC
11257289	7404166	2005-10-24	2008-07-22	Lapsed	United States of America	Method and system for mapping netlist of integrated circuit to design
10694208	7036102	2003-10-27	2006-04-25	Lapsed	United States of America	Process and apparatus for placement of cells in an IC during floorplan creation
11257470	7493519	2005-10-24	2009-02-17	Lapsed	United States of America	RRAM Memory Error Emulation
11311388	7415686	2005-12-19	2008-08-19	Lapsed	United States of America	Memory timing model with back-annotating
11239977	7340706	2005-09-30	2008-03-04	Lapsed	United States of America	Method and system for analyzing the quality of an OPC mask

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10732395	7328417	2003-12-09	2008-02-05	Granted	United States of America	Cell-based method for creating slotted metal in semiconductor designs
11054460	7028274	2005-02-09	2006-04-11	Lapsed	United States of America	RRAM backend flow
11113615	7373629	2005-04-25	2008-05-13	Granted	United States of America	
11324082	7334204	2005-12-29	2008-02-19	Lapsed	United States of America	System for avoiding false path pessimism in estimating net delay for an integrated circuit design
11120067	7292063	2005-05-02	2007-11-06	Lapsed	United States of America	Method of interconnect for multi-slot metal-mask programmable relocatable function placed in an I/O region
11041489	7243324	2005-01-24	2007-07-10	Granted	United States of America	Method of buffer insertion to achieve pin specific delays
10990237	7207026	2004-11-16	2007-04-17	Granted	United States of America	Memory tiling architecture
11037306	7299435	2005-01-18	2007-11-20	Granted	United States of America	Frequency dependent timing margin
10999493	7216278	2004-11-30	2007-05-08	Granted	United States of America	Method and BIST architecture for fast memory testing in platform-based integrated circuit
11290186	7496861	2005-11-30	2009-02-24	Lapsed	United States of America	Method for Generalizing Design Attributes in a Design Capture Environment
11005690	7424690	2004-12-07	2008-09-09	Lapsed	United States of America	Interconnect integrity verification
11016192	7290194	2004-12-17	2007-10-30	Lapsed	United States of America	System for performing automatic test pin assignment for a programmable device
11002576	7493577	2004-12-01	2009-02-17	Lapsed	United States of America	Automatic Recognition of Geometric Points in a Target IC Design for OPC Mask Quality Calculation
11071623	7331031	2005-03-03	2008-02-12	Lapsed	United States of America	Method for describing and deploying design platform sets
10976518	7216323	2004-10-29	2007-05-08	Granted	United States of America	Process for designing base platforms for IC design to permit resource recovery and flexible macro placement, base platform for ICs, and process of creating ICs
10988081	7181359	2004-11-12	2007-02-20	Granted	United States of America	Method and system of generic implementation of sharing test pins with I/O cells
10106432	6934597	2002-03-26	2005-08-23	Lapsed	United States of America	Integrated circuit having integrated programmable gate array and method of operating the same
11151043	7380229	2005-06-13	2008-05-27	Lapsed	United States of America	Automatic generation of correct minimal clocking constraints for a semiconductor product
11056838	7494752	2005-02-11	2009-02-24	Lapsed	United States of America	Method and systems for utilizing simplified resist process models to perform optical and process corrections
10875128	7168052	2004-06-23	2007-01-23	Granted	United States of America	Yield driven memory placement system
11010745	7334206	2004-12-13	2008-02-19	Granted	United States of America	Cell builder for different layer stacks
10971911	7979833	2004-10-23	2011-07-12	Granted	United States of America	Debugging Simulation Of A Circuit Core Using Pattern Recorder, Player & Checker
11100986	7398489	2005-04-06	2008-07-08	Lapsed	United States of America	Advanced standard cell power connection

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10902987	7331028	2004-07-30	2008-02-12	Lapsed	United States of America	Engineering change order scenario manager
10952213	7152012	2004-09-28	2006-12-19	Granted	United States of America	Four point measurement technique for programmable impedance drivers RapidChip and ASIC devices
10946274	7272814	2004-09-20	2007-09-18	Granted	United States of America	Reconfiguring a RAM to a ROM using layers of metallization
1020117003375	10-1471237	2008-08-14	2014-12-03	Lapsed	Korea, Republic of (KR)	System and Method for Designing Integrated Circuits that Employ Adaptive Voltage and Scaling Optimization
2008801311778	10 2160054	2008-08-14	2014-05-07	Lapsed	China	System and Method for Designing Integrated Circuits that Employ Adaptive Voltage and Scaling Optimization
11438644	7703059	2006-05-22	2010-04-20	Lapsed	United States of America	METHOD AND APPARATUS FOR AUTOMATIC CREATION AND PLACEMENT OF A FLOOR-PLAN REGION
09022353	6239609	1998-02-11	2001-05-29	Granted	United States of America	Reduced voltage quiescent current test methodology for integrated circuits
10516583	7412343	2005-03-24	2008-08-12	Granted	United States of America	Method For Delay-Fault Testing In Field Programmable Gate Arrays
10879768	7181710	2004-06-28	2007-02-20	Granted	United States of America	Device for estimating cell delay from a table with added voltage swing
10728036	7058909	2003-12-03	2006-06-06	Lapsed	United States of America	Method of generating an efficient stuck-at fault and transition delay fault truncated scan test pattern for an integrated circuit design
10832226	7606692	2004-04-26	2009-10-20	Lapsed	United States of America	Gate-level netlist reduction for simulating target modules of a design
11126880	7272802	2005-05-11	2007-09-18	Granted	United States of America	R-cells containing CDM clamps
11061581	7228516	2005-02-18	2007-06-05	Granted	United States of America	Negative bias temperature instability modeling
11129547	7373622	2005-05-13	2008-05-13	Granted	United States of America	Relocatable built-in self test (BIST) elements for relocatable mixed-signal elements
11305542	7406675	2005-12-16	2008-07-29	Lapsed	United States of America	Method and system for improving aerial image simulation speeds
040213241		2004-09-08		Application	European Patent	Flexible Design of Memory use in Integrated Circuits
11079998	7263678	2005-03-15	2007-08-28	Granted	United States of America	Method of identifying floorplan problems in an integrated circuit layout
10994114	7213223	2004-11-19	2007-05-01	Granted	United States of America	Method of estimating a total path delay in an integrated circuit design with stochastically weighted conservatism
11012618	7260814	2004-12-14	2007-08-21	Granted	United States of America	OPC edge correction based on a smoothed mask design
10928799	7111267	2004-08-27	2006-09-19	Lapsed	United States of America	Process and apparatus to assign coordinates to nodes of logical trees without increase of wire lengths
10992999	7257791	2004-11-19	2007-08-14	Granted	United States of America	Multiple buffer insertion in global routing
11015123	7231626	2004-12-17	2007-06-12	Granted	United States of America	Method of implementing an engineering change order in an integrated circuit design by windows
10903836	7174526	2004-07-30	2007-02-06	Granted	United States of America	Accurate density calculation with density views in layout databases

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10946422	7332917	2004-09-21	2008-02-19	Lapsed	United States of America	Method for calculating frequency-dependent impedance in an integrated circuit
11032720	7234122	2005-01-10	2007-06-19	Granted	United States of America	Three-dimensional interconnect resistance extraction using variational method
10954907	7106074	2004-09-30	2006-09-12	Lapsed	United States of America	Technique for measurement of programmable termination resistor networks on rapidchip and ASIC devices
10859874	7412678	2004-06-02	2008-08-12	Lapsed	United States of America	Method and computer program for management of synchronous and asynchronous clock domain crossing in integrated circuit design
10901841	7062737	2004-07-28	2006-06-13	Lapsed	United States of America	Method of automated repair of crosstalk violations and timing violations in an integrated circuit design
10828408	7219317	2004-04-19	2007-05-15	Granted	United States of America	Method and computer program for verifying an incremental change to an integrated circuit design
10800219	7325222	2004-03-12	2008-01-29	Lapsed	United States of America	Method and apparatus for verifying the post-optical proximity corrected mask wafer image sensitivity to reticle manufacturing errors
10824509	7103858	2004-04-14	2006-09-05	Lapsed	United States of America	Process and apparatus for characterizing intellectual property for integration into an IC platform environment
10803516	7398486	2004-03-17	2008-07-08	Lapsed	United States of America	Method and apparatus for performing logical transformations for global routing
11287927	7254761	2005-11-28	2007-08-07	Granted	United States of America	Platform ASIC reliability
09034658	6175953	1998-03-03	2001-01-16	Granted	United States of America	Method and apparatus for general systematic application of proximity correction
10688460	7111264	2003-10-17	2006-09-19	Lapsed	United States of America	Process and apparatus for fast assignment of objects to a rectangle
10793055	7131103	2004-03-04	2006-10-31	Lapsed	United States of America	Conductor stack shifting
10724851	7584460	2003-12-01	2009-09-01	Lapsed	United States of America	Process and Apparatus for Abstracting IC Design Files
10718291	7003753	2003-11-19	2006-02-21	Lapsed	United States of America	Method of generating a physical netlist for a hierarchical integrated circuit design
10996074	7305634	2004-11-23	2007-12-04	Granted	United States of America	Method to selectively identify at risk die based on location within the reticle
11550448	7610568	2006-10-18	2009-10-27	Lapsed	United States of America	Methods And Apparatus For Making Placement Sensitive Logic Modifications
09659090	6550042	2000-09-11	2003-04-15	Lapsed	United States of America	Hardware/Software Co-Synthesis Of Heterogeneous Low-Power And Fault-Tolerant Systems-On-A-Chip
2003297248	5143994	2003-08-21	2012-11-30	Lapsed	Japan	Automatic Recognition of an Optically Periodic Structure in an Integrated Circuit Design
10228444	6874108	2002-08-27	2005-03-29	Granted	United States of America	Fault Tolerant Operation Of Reconfigurable Devices Utilizing An Adjustable System Clock

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08975250	6182270	1997-11-20	2001-01-30	Granted	United States of America	Low-Displacement Rank Preconditioners For Simplified Non-Linear Analysis Of Circuits And Other Devices
09633795	6640324	2000-08-07	2003-10-28	Lapsed	United States of America	Boundary Scan Chain Routing
10650296	7039891	2003-08-27	2006-05-02	Granted	United States of America	Method of clock driven cell placement and clock tree synthesis for integrated circuit design
10700790	7003421	2003-11-03	2006-02-21	Lapsed	United States of America	VDD over and undervoltage measurement techniques using monitor cells
09138702	6345240	1998-08-24	2002-02-05	Granted	United States of America	Device And Method For Parallel Simulation Task Generation And Distribution
10719787	7003739	2003-11-21	2006-02-21	Lapsed	United States of America	Method and apparatus for finding optimal unification substitution for formulas in technology library
10621737	7082593	2003-07-17	2006-07-25	Lapsed	United States of America	Method and apparatus of IC implementation based on C++ language description
10664636	7703076	2003-09-19	2010-04-20	Lapsed	United States of America	User Interface Software Development Tool and Method for Enhancing the Sequencing of Instructions within a Superscalar Microprocessor Pipeline by Displaying and Manipulating Instructions in the Pipeline
10632622	7007259	2003-07-31	2006-02-28	Granted	United States of America	Method for providing clock-net aware dummy metal using dummy regions
10748068	7055117	2003-12-29	2006-05-30	Lapsed	United States of America	System and Method for Debugging System-On-Chips Using Single Or N-Cycle Stepping
09433702	6493848	1999-11-03	2002-12-10	Granted	United States of America	Rate Equation Method And Apparatus For Simulation Of Current In A MOS Device
09199018	6301688	1998-11-24	2001-10-09	Granted	United States of America	Insertion Of Test Points In RTL Designs
10659138	7028276	2003-09-10	2006-04-11	Lapsed	United States of America	First time silicon and proto test cell notification
10696105	7062739	2003-10-29	2006-06-13	Lapsed	United States of America	Gate reuse methodology for diffused cell-based IP blocks in platform-based silicon products
10641799	6825688	2003-08-15	2004-11-30	Lapsed	United States of America	System for yield enhancement in programmable logic
10887599	7117472	2004-07-09	2006-10-03	Granted	United States of America	Placement of a clock signal supply network during design of integrated circuits
030133243		2003-06-13		Application	European Patent	Automatic Recognition of an Optically Periodic Structure in an Integrated Circuit Design
10719393	7103865	2003-11-21	2006-09-05	Lapsed	United States of America	Process and apparatus for placement of megacells in ICs design
08306088	5566187	1994-09-14	1996-10-15	Expired	United States of America	Method For Identifying Untestable Faults In Logic Circuits
09144799	6687658	1998-09-01	2004-02-03	Lapsed	United States of America	Apparatus And Method For Reduced-Order Modeling Of Time-Varying Systems And Computer Storage Medium Containing The Same
09347628	6591231	1999-07-02	2003-07-08	Granted	United States of America	A Method For Identifying Cyclicity In Circuit Designs

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09128041	6094735	1998-08-03	2000-07-25	Granted	United States of America	Speed-Signaling Testing For Integrated Circuits
10452689	7020859	2003-06-02	2006-03-28	Lapsed	United States of America	Process skew results for integrated circuits
08267109	5623499	1994-06-27	1997-04-22	Expired	United States of America	Method and Apparatus for Generating Conformance Test Data Sequences
09138701	6321181	1998-08-24	2001-11-20	Granted	United States of America	Device And Method For Parallel Simulation
08254218	5513122	1994-06-06	1996-04-30	Expired	United States of America	Method and Apparatus for Determining The Reachable States in A Hybrid Model State Machine
08789353	5995733	1997-01-27	1999-11-30	Expired	United States of America	Method And Apparatus For Efficient Design And Analysis Of Integrated Circuits Using Multiple Time Scales
10914657	7107561	2004-08-09	2006-09-12	Lapsed	United States of America	Method of sizing via arrays and interconnects to reduce routing congestion in flip chip integrated circuits
10724996	7032190	2003-12-01	2006-04-18	Lapsed	United States of America	Integrated circuits, and design and manufacture thereof
10840534	7584437	2004-05-06	2009-09-01	Lapsed	United States of America	Assuring Correct Data Entry To Generate Shells For A Semiconductor Platform
08637026	5625630	1996-04-24	1997-04-29	Expired	United States of America	Increasing Testability By Clock Transformation
10640738	6925626	2003-08-13	2005-08-02	Lapsed	United States of America	Method of routing a redistribution layer trace in an integrated circuit die
10602937	7062736	2003-06-24	2006-06-13	Lapsed	United States of America	Timing constraint generator
08577454	5774477	1995-12-22	1998-06-30	Expired	United States of America	Method And Apparatus For Pseudorandom Boundary-Scan Testing
08378435	5481580	1995-01-26	1996-01-02	Expired	United States of America	Method And Apparatus For Testing Long Counters
10407065	6807656	2003-04-03	2004-10-19	Lapsed	United States of America	Decoupling capacitance estimation and insertion flow for ASIC designs
08327338	5606567	1994-10-21	1997-02-25	Expired	United States of America	Delay Testing of High-Performance Circuits By A Slow-Speed Tester
10603905	7287238	2003-06-25	2007-10-23	Granted	United States of America	Method and apparatus for exposing pre-diffused IP blocks in a semiconductor device for prototyping based on hardware emulation
10439373	7007248	2003-05-15	2006-02-28	Granted	United States of America	Method and apparatus for implementing engineering change orders
10438530	6990651	2003-05-14	2006-01-24	Lapsed	United States of America	Advanced design format library for integrated circuit design synthesis and floorplanning tools
10408205	6922817	2003-04-04	2005-07-26	Lapsed	United States of America	System and method for achieving timing closure in fixed placed designs after implementing logic changes
10369269	6978428	2003-02-14	2005-12-20	Lapsed	United States of America	Mode register in an integrated circuit that stores test scripts and operating parameters
10713492	7257799	2003-11-14	2007-08-14	Granted	United States of America	Flexible design for memory use in integrated circuits
90119140	NI-175325	2001-08-06	2003-04-11	Lapsed	Taiwan	Boundary Scan Chain Routing
09878499	6792578	2001-06-11	2004-09-14	Granted	United States of America	Hard macro having an antenna rule violation free input/output ports

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10453182	7069535	2003-06-03	2006-06-27	Lapsed	United States of America	Optical proximity correction method using weighted priorities
10326717	6948139	2002-12-19	2005-09-20	Lapsed	United States of America	Method for combining states
10426549	7062726	2003-04-30	2006-06-13	Lapsed	United States of America	Method for generating tech-library for logic function
10334731	6848094	2002-12-31	2005-01-25	Lapsed	United States of America	Netlist redundancy detection and global simplification
1020050110790	10-1097710	2005-11-18	2011-12-16	Lapsed	Korea, Republic of (KR)	Method Of Making A Semiconductor Device By Balancing Shallow Trench Isolation Stress and Optical Proximity Effects
10299564	6868536	2002-11-19	2005-03-15	Lapsed	United States of America	Method to find boolean function symmetries
10334743	6907588	2002-12-31	2005-06-14	Lapsed	United States of America	Congestion estimation for register transfer level code
2000335373	4988981	2000-11-02	2012-05-11	Lapsed	Japan	Rate Equation Method And Apparatus For Simulation Of Current In A MOS Device
2001238546	3876380	2001-08-07	2006-11-10	Granted	Japan	Boundary Scan Chain Routing
10459158	6871154	2003-06-11	2005-03-22	Lapsed	United States of America	Method and apparatus for automatically configuring and/or inserting chip resources for manufacturing tests
10349564	6817004	2003-01-22	2004-11-09	Lapsed	United States of America	Net segment analyzer for chip CAD layout
10327314	6898780	2002-12-20	2005-05-24	Lapsed	United States of America	Method and system for constructing a hierarchy-driven chip covering for optical proximity correction
10327451	6911285	2002-12-20	2005-06-28	Lapsed	United States of America	Sidelobe correction for attenuated phase shift masks
10327304	7093228	2002-12-20	2006-08-15	Lapsed	United States of America	Method and system for classifying an integrated circuit for optical proximity correction
10254607	6760896	2002-09-25	2004-07-06	Lapsed	United States of America	Process layout of buffer modules in integrated circuits
10254380	6810515	2002-09-25	2004-10-26	Lapsed	United States of America	Process of restructuring logics in ICs for setup and hold time optimization
10318639	6922823	2002-12-13	2005-07-26	Lapsed	United States of America	Method for creating derivative integrated circuit layouts for related products
10271026	6782523	2002-10-15	2004-08-24	Lapsed	United States of America	Parallel configurable IP design methodology
10291982	7103868	2002-11-12	2006-09-05	Lapsed	United States of America	Optimizing depths of circuits for Boolean functions
10334570	6757885	2002-12-31	2004-06-29	Lapsed	United States of America	Length matrix generator for register transfer level code
10665927	7062731	2003-09-17	2006-06-13	Lapsed	United States of America	Method of noise analysis and correction of noise violations for an integrated circuit design
10301182	7024636	2002-11-20	2006-04-04	Lapsed	United States of America	Chip management system
10014642	3253910	1998-01-27	2001-11-22	Granted	Japan	Method And Apparatus For Efficient Design And Analysis Of Integrated Circuits Using Multiple Time Scales
10465186	6959428	2003-06-19	2005-10-25	Lapsed	United States of America	Designing and testing the interconnection of addressable devices of integrated circuits
10334568	6823502	2002-12-31	2004-11-23	Lapsed	United States of America	Placement of configurable input/output buffer structures during design of integrated circuits
10272182	6880142	2002-10-16	2005-04-12	Lapsed	United States of America	Method of delay calculation for variation in interconnect metal process

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
2005333495	5378636	2005-11-18	2013-10-04	Lapsed	Japan	Method Of Making A Semiconductor Device By Balancing Shallow Trench Isolation Stress and Optical Proximity Effects
10331521	6854103	2002-12-30	2005-02-08	Lapsed	United States of America	Apparatus and method for visualizing and analyzing resistance networks
10316594	6757883	2002-12-11	2004-06-29	Lapsed	United States of America	Estimating free space in IC chips
10253006	6701495	2002-09-23	2004-03-02	Lapsed	United States of America	Model of the contact region of integrated circuit resistors
10341119	6934929	2003-01-13	2005-08-23	Lapsed	United States of America	Method for improving OPC modeling
10435168	7020852	2003-05-08	2006-03-28	Lapsed	United States of America	Automation of the development, testing, and release of a flow framework and methodology to design integrated circuits
10265803	6871333	2002-10-07	2005-03-22	Lapsed	United States of America	Bent gate transistor modeling
10231641	7212961	2002-08-30	2007-05-01	Granted	United States of America	Interface for rapid prototyping system
10231643	7299427	2002-08-30	2007-11-20	Granted	United States of America	Rapid prototyping system
10664137	6910201	2003-09-17	2005-06-21	Lapsed	United States of America	Custom clock interconnects on a standardized silicon platform
10223931	6775818	2002-08-20	2004-08-10	Lapsed	United States of America	Device parameter and gate performance simulation based on wafer image prediction
10236207	6782525	2002-09-05	2004-08-24	Lapsed	United States of America	Wafer process critical dimension, alignment, and registration analysis simulation tool
10185740	6769097	2002-06-27	2004-07-27	Lapsed	United States of America	Scale-invariant topology and traffic allocation in multi-node system-on-chip switching fabrics
10174681	7818157	2002-06-19	2010-10-19	Lapsed	United States of America	Instantaneous Voltage Drop Sensitivity Analysis Tool (IVDSAT)
10231904	6748579	2002-08-30	2004-06-08	Granted	United States of America	Method of using filler metal for implementing changes in an integrated circuit design
10135869	7016748	2002-04-30	2006-03-21	Lapsed	United States of America	Collaborative integration of hybrid electronic and micro and sub-micro level aggregates
10151826	6775811	2002-05-22	2004-08-10	Lapsed	United States of America	Chip design method for designing integrated circuit chips with embedded memories
10224019	6802047	2002-08-19	2004-10-05	Lapsed	United States of America	Calculating resistance of conductor layer for integrated circuit design
10153570	6665850	2002-05-22	2003-12-16	Lapsed	United States of America	Spanning tree method for K-dimensional space
09859149	6587999	2001-05-15	2003-07-01	Granted	United States of America	Modeling delays for small nets in an integrated circuit design
10140967	6683476	2002-05-08	2004-01-27	Lapsed	United States of America	Contact ring architecture
10278150	6795954	2002-10-21	2004-09-21	Lapsed	United States of America	Method of decreasing instantaneous current without affecting timing
10177591	7003510	2002-06-19	2006-02-21	Lapsed	United States of America	Table module compiler equivalent to ROM
10225909	6785871	2002-08-21	2004-08-31	Lapsed	United States of America	Automatic recognition of an optically periodic structure in an integrated circuit design
10092195	6615401	2002-03-06	2003-09-02	Granted	United States of America	Blocked net buffer insertion
10308557	6701499	2002-12-03	2004-03-02	Lapsed	United States of America	Effective approximated calculation of smooth functions

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
10277398	6941533	2002-10-21	2005-09-06	Lapsed	United States of America	Clock tree synthesis with skew for memory devices
10178193	6842883	2002-06-24	2005-01-11	Granted	United States of America	Application of co-verification tools to the testing of IC designs
10027642	6845495	2001-12-20	2005-01-18	Lapsed	United States of America	Multidirectional router
10132360	6948114	2002-04-25	2005-09-20	Granted	United States of America	
10146363	6931612	2002-05-15	2005-08-16	Lapsed	United States of America	Design and optimization methods for integrated circuits
10252488	6747473	2002-09-23	2004-06-08	Lapsed	United States of America	Device under interface card with on-board testing
10059480	6757881	2002-01-29	2004-06-29	Lapsed	United States of America	Power routing with obstacles
10109113	6701493	2002-03-27	2004-03-02	Lapsed	United States of America	Floor plan tester for integrated circuit design
10427609	7082584	2003-04-30	2006-07-25	Lapsed	United States of America	Automated analysis of RTL code containing ASIC vendor rules
10025123	6658628	2001-12-19	2003-12-02	Granted	United States of America	Developement of hardmac technology files (CLF, tech and synlib) for RTL and full gate level netlists
10086232	6662349	2002-02-27	2003-12-09	Granted	United States of America	Method of repeater insertion for hierarchical integrated circuit design
10119821	7024641	2002-04-10	2006-04-04	Lapsed	United States of America	Integrated circuit having a programmable gate array and a field programmable gate array and methods of designing and manufacturing the same using testing IC before configuring FPGA
10105579	6904586	2002-03-25	2005-06-07	Granted	United States of America	Integrated circuit having integrated programmable gate array and field programmable gate array, and method of operating the same
10077066	7043718	2002-02-15	2006-05-09	Lapsed	United States of America	System real-time analysis tool
10005062	6769107	2001-12-03	2004-07-27	Lapsed	United States of America	Method and system for implementing incremental change to circuit design
09735837	6536027	2000-12-13	2003-03-18	Lapsed	United States of America	Cell pin extensions for integrated circuits
10143155	7539680	2002-05-10	2009-05-26	Lapsed	United States of America	Revision Control for Database of Evolved Design
10045473	6647538	2001-11-08	2003-11-11	Lapsed	United States of America	Apparatus and method for signal skew characterization utilizing clock division
10021619	6792584	2001-10-30	2004-09-14	Granted	United States of America	System and method for designing an integrated circuit
09053833	6353906	1998-04-01	2002-03-05	Granted	United States of America	Testing synchronization circuitry using digital simulation
09997888	7006962	2001-11-29	2006-02-28	Lapsed	United States of America	Distributed delay prediction of multi-million gate deep sub-micron ASIC designs
09207878	6370492	1998-12-08	2002-04-09	Granted	United States of America	Modified design representation for fast fault simulation of an integrated circuit
10034535	6691288	2001-12-27	2004-02-10	Lapsed	United States of America	Method to debug IKOS method
10015194	6999910	2001-11-20	2006-02-14	Lapsed	United States of America	Method and apparatus for implementing a metamethodology
09993015	6788091	2001-11-05	2004-09-07	Lapsed	United States of America	Method and apparatus for automatic marking of integrated circuits in wafer scale testing
2006045368	3847774	2006-02-22	2006-09-01	Lapsed	Japan	A Method For Identifying Cyclicity In Circuit Designs
08939498	5828828	1997-09-29	1998-10-27	Expired	United States of America	Method For Inserting Test Points For Full- And Partial-Scan Built-In Self-Testing

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08599289	5559811	1996-02-09	1996-09-24	Expired	United States of America	Method For Identifying Untestable & Redundant Faults In Sequential Logic Circuits
09973153	7051318	2001-10-09	2006-05-23	Lapsed	United States of America	Web based OLA memory generator
09986912	6594805	2001-11-13	2003-07-15	Granted	United States of America	Integrated design system and method for reducing and avoiding crosstalk
10144101	6898767	2002-05-09	2005-05-24	Lapsed	United States of America	Method and apparatus for custom design in a standard cell design environment
10003823	6668359	2001-10-31	2003-12-23	Lapsed	United States of America	Verilog to vital translator
09737239	6557144	2000-12-14	2003-04-29	Lapsed	United States of America	Netlist resynthesis program based on physical delay calculation
09736571	6546539	2000-12-14	2003-04-08	Granted	United States of America	Netlist resynthesis program using structure co-factoring
09883733	7050582	2001-06-18	2006-05-23	Lapsed	United States of America	Pseudo-random one-to-one circuit synthesis
09801392	6532576	2001-03-07	2003-03-11	Granted	United States of America	Cell interconnect delay library for integrated circuit design
09464623	6588006	1999-12-16	2003-07-01	Granted	United States of America	Programmable ASIC
09470362	6625572	1999-12-22	2003-09-23	Granted	United States of America	Cycle modeling in cycle accurate software simulators of hardware modules for software/software cross-simulation and hardware/software co-simulation
09727426	6449760	2000-11-30	2002-09-10	Granted	United States of America	Pin placement method for integrated circuits
09805642	6496967	2001-03-13	2002-12-17	Granted	United States of America	Method of datapath cell placement for an integrated circuit
09808549	6463571	2001-03-14	2002-10-08	Granted	United States of America	Full-chip extraction of interconnect parasitic data
09493467	6446248	2000-01-28	2002-09-03	Granted	United States of America	Spare cells placement methodology
09492881	6457157	2000-01-26	2002-09-24	Granted	United States of America	I/O device layout during integrated circuit design
09789108	6546541	2001-02-20	2003-04-08	Granted	United States of America	Placement-based integrated circuit re-synthesis tool using estimated maximum interconnect capacitances
09677475	6564361	2000-10-02	2003-05-13	Granted	United States of America	Method and apparatus for timing driven resynthesis
09678478	6681373	2000-10-02	2004-01-20	Lapsed	United States of America	Method and apparatus for dynamic buffer and inverter tree optimization
09734539	6725389	2000-12-11	2004-04-20	Granted	United States of America	Method for minimizing clock skew by relocating a clock buffer until clock skew is within a tolerable limit
09823184	6560761	2001-03-29	2003-05-06	Granted	United States of America	Method of datapath cell placement for bitwise and non-bitwise integrated circuit designs
09677940	6637011	2000-10-02	2003-10-21	Granted	United States of America	Method and apparatus for quick search for identities applicable to specified formula
09677276	6530063	2000-10-02	2003-03-04	Granted	United States of America	Method and apparatus for detecting equivalent and anti-equivalent pins
09626037	6536016	2000-07-27	2003-03-18	Lapsed	United States of America	Method and apparatus for locating constants in combinational circuits
09756506	6526540	2001-01-08	2003-02-25	Granted	United States of America	Flip chip trace library generator

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09678479	6543032	2000-10-02	2003-04-01	Granted	United States of America	Method and apparatus for local resynthesis of logic trees with multiple cost functions
08813340	6260175	1997-03-07	2001-07-10	Granted	United States of America	Method for designing an integrated circuit using predefined and preverified core modules having prebalanced clock trees
09715814	6496962	2000-11-17	2002-12-17	Granted	United States of America	Standard library generator for cell timing model
09710359	6658630	2000-11-09	2003-12-02	Granted	United States of America	Method to translate UDPs using gate primitives
09550764	6654919	2000-04-17	2003-11-25	Lapsed	United States of America	Automated system for inserting and reading of probe points in silicon embedded testbenches
09464741	6434735	1999-12-16	2002-08-13	Granted	United States of America	Method for programming an FPGA and implementing an FPGA interconnect
09680893	6442741	2000-10-06	2002-08-27	Granted	United States of America	Method of automatically generating schematic and waveform diagrams for analysis of timing margins and signal skews of relevant logic cells using input signal predictors and transition times
10011796	7065683	2001-12-05	2006-06-20	Lapsed	United States of America	Long path at-speed testing
10125675	7028238	2002-04-18	2006-04-11	Lapsed	United States of America	Input/output characterization chain for an integrated circuit
08630257	6066178	1996-04-10	2000-05-23	Expired	United States of America	Automated design method and system for synthesizing digital multipliers
09592749	6457160	2000-06-13	2002-09-24	Granted	United States of America	Iterative prediction of circuit delays
09151228	6370493	1998-09-10	2002-04-09	Granted	United States of America	Simulation format creation system and method
09894618	6532577	2001-06-27	2003-03-11	Granted	United States of America	Timing driven interconnect analysis
09212769	6216254	1998-12-16	2001-04-10	Granted	United States of America	Integrated circuit design using a frequency synthesizer that automatically ensures testability
09847838	6530073	2001-04-30	2003-03-04	Granted	United States of America	RTL annotation tool for layout induced netlist changes
09955698	6629304	2001-09-19	2003-09-30	Granted	United States of America	Cell placement in integrated circuit chips to remove cell overlap, row overflow and optimal placement of dual height cells
09151900	6272671	1998-09-11	2001-08-07	Granted	United States of America	Extractor and schematic viewer for a design representation, and associated method
09233529	6408265	1999-01-20	2002-06-18	Granted	United States of America	Metastability risk simulation analysis tool and method
08877117	5974241	1997-06-17	1999-10-26	Expired	United States of America	Test bench interface generator for tester compatible simulations
09941359	6587991	2001-08-28	2003-07-01	Granted	United States of America	Optimized metal stack strategy
09047877	6141631	1998-03-25	2000-10-31	Granted	United States of America	Pulse rejection circuit model program and technique in VHDL
09968008	6907590	2001-10-02	2005-06-14	Lapsed	United States of America	Integrated circuit design system and method for reducing and avoiding crosstalk
12190784	7971169	2008-08-13	2011-06-28	Granted	United States of America	System And Method For Reducing The Generation Of Inconsequential Violations Resulting From Timing Analyses
13761828	8667438	2013-02-07	2014-03-04	Lapsed	United States of America	OPTIMIZATION OF LIBRARY SLEW RATIO BASED CIRCUIT
12111836	8418102	2008-04-29	2013-04-09	Granted	United States of America	OPTIMIZATION OF LIBRARY SLEW RATIO BASED CIRCUIT

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
12901588	8484008	2010-10-11	2013-07-09	Lapsed	United States of America	Methods and Systems for Performing Timing Sign-Off of an Integrated Circuit Design
13681283	8694937	2012-11-19	2014-04-08	Lapsed	United States of America	Implementing And Checking Electronic Circuits With Flexible Ramptime Limits and Tools For Performing The Same
12836274	8332792	2010-07-14	2012-12-11	Lapsed	United States of America	Implementing And Checking Electronic Circuits With Flexible Ramptime Limits and Tools For Performing The Same
12423001	8271922	2009-04-14	2012-09-18	Lapsed	United States of America	System and Method for Clock Optimization to Achieve Timing Signoff in an Electronic Circuit and Electronic Design Automation Tool Incorporating the Same
12510082	8122422	2009-07-27	2012-02-21	Granted	United States of America	Establishing Benchmarks For Analyzing Benefits Associated With Voltage Scaling, Analyzing The Benefits And An Apparatus Therefor
12364918	8806408	2009-02-03	2014-08-12	Lapsed	United States of America	
12247992	8499230	2008-10-08	2013-07-30	Lapsed	United States of America	
14305794		2014-06-16		Abandoned	United States of America	
11187455	7444275	2005-07-22	2008-10-28	Lapsed	United States of America	Multi-Variable Polynomial Modeling Techniques For Use In Integrated Circuit Design
10953480	7197723	2004-09-29	2007-03-27	Granted	United States of America	Semiconductor Device Manufacturing
09567606	6539524	2000-05-10	2003-03-25	Granted	United States of America	Method And Apparatus For Matching Capacitance Of Filters Having Different Circuit Topologies
09290321	6560568	1999-04-12	2003-05-06	Granted	United States of America	Deriving Statistical Device Models From Electrical Test Data
09265932	6427216	1999-03-11	2002-07-30	Granted	United States of America	Integrated Circuit Testing Using A High Speed Data Interface Bus
09287862	6456101	1999-04-07	2002-09-24	Granted	United States of America	Chip-On-Chip Testing Using BIST
09168409	6216241	1998-10-08	2001-04-10	Granted	United States of America	METHOD AND SYSTEM FOR TESTING MULTIPORT MEMORIES
09031012	6253355	1998-02-26	2001-06-26	Granted	United States of America	Method For Fast Estimation Of Step Response Found Due To Capacitance Coupling For RC Circuits
09126013	6154716	1998-07-29	2000-11-28	Granted	United States of America	System And Method For Simulating Electronic Circuits
08933733	6072947	1997-09-23	2000-06-06	Expired	United States of America	Method Of Making An Integrated Circuit Including Noise Modelling And Prediction
08720235	6058256	1996-09-26	2000-05-02	Expired	United States of America	Technique For Effectively Routing Conduction Paths In Circuit Layouts
08664020	5784594	1996-06-12	1998-07-21	Expired	United States of America	Generic Interactive Device Model Wrapper
08552421	5677848	1995-11-03	1997-10-14	Expired	United States of America	Method to Derive The Functionality Of A Digital Circuit From Its Mask Layout
13467696	8607180	2012-05-09	2013-12-10	Lapsed	United States of America	Multi-Pass Routing to Reduce Crosstalk
10999468	7315993	2004-11-30	2008-01-01	Lapsed	United States of America	Verification of RRAM Tiling Netlist
13246102	8516424	2011-09-27	2013-08-20	Lapsed	United States of America	Timing Signoff System and Method that Takes Static and Dynamic Voltage Drop into Account

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
12347916	8239801	2008-12-31	2012-08-07	Lapsed	United States of America	Architecturally Independent Noise Sensitivity analysis of Integrated Circuits having a Memory Storage Device and a Noise Sensitivity Analyzer
12336472	8352818	2008-12-16	2013-01-08	Lapsed	United States of America	METHOD FOR GENERATING TEST PATTERNS FOR SMALL DELAY DEFECTS
12211238	8046726	2008-09-16	2011-10-25	Lapsed	United States of America	Waiver Mechanism For Physical Verification of System Designs
12248016	8010935	2008-10-08	2011-08-30	Granted	United States of America	Electronic Design Automation Tool And Method For Optimizing The Placement Of Process Monitors In An Integrated Circuit
12182330	8464198	2008-07-30	2013-06-11	Lapsed	United States of America	Electronic Design Automation Tool And Method For Employing Unsensitized Critical Path Information To Reduce Leakage Power In An Integrated Circuit
12117381	7844929	2008-05-08	2010-11-30	Granted	United States of America	Optimizing Test Code Generation for Verification Environment
13099948	8397196	2011-05-03	2013-03-12	Lapsed	United States of America	Intelligent Dummy Metal Fill Process for Integrated Circuits
12248677	8397184	2008-10-09	2013-03-12	Granted	United States of America	Channel Length Scaling for Footprint Compatible Digital Library Cell Design
12109501	7853901	2008-04-25	2010-12-14	Granted	United States of America	Unified Layer Stack Architecture
12103825	7895550	2008-04-16	2011-02-22	Granted	United States of America	ON CHIP LOCAL MOSFET SIZING
11849391	7895546	2007-09-04	2011-02-22	Granted	United States of America	Statistical Design Closure
13114834	8464202	2011-05-24	2013-06-11	Granted	United States of America	Fully Parameterizable Representation of a Higher Level Design Entity
13367094	8522179	2012-02-06	2013-08-27	Lapsed	United States of America	System and Method for Managing Timing Margin in a Hierarchical Integrated Circuit Design Process
13649909	8543951	2012-10-11	2013-09-24	Lapsed	United States of America	Modeling Approach For Timing Closure In Hierarchical Designs Leveraging The Separation Of Horizontal And Vertical Aspects Of The Design Flow
12905301	8341573	2010-10-15	2012-12-25	Lapsed	United States of America	Novel Modeling Approach For Timing Closure In Hierarchical Designs Leveraging The Separation Of Horizontal And Vertical Aspects Of The Design Flow
12421481	8515695	2009-04-09	2013-08-20	Lapsed	United States of America	Method and Apparatus for Evaluating Small Delay Defect Coverage of a Test Pattern Set on an IC
12510122	8127264	2009-07-27	2012-02-28	Granted	United States of America	Methods for Designing Integrated Circuits Employing Context-Sensitive and Progressive Rules and an Apparatus Employing One of the Methods
13421710	8539419	2012-03-15	2013-09-17	Lapsed	United States of America	Method for Designing Integrated Circuits Employing a Partitioned Hierarchical Design Flow and an Apparatus Employing the Method
12510104	8239805	2009-07-27	2012-08-07	Lapsed	United States of America	A Method for Designing Integrated Circuits Employing A Partitioned Hierarchical Design Flow and an Apparatus Employing the Method

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
13971560	8683407	2013-08-20	2014-03-25	Lapsed	United States of America	Hierarchical Design Flow Generator
12240210	8112734	2008-09-29	2012-02-07	Granted	United States of America	Design Optimization with Adaptive Body Biasing
12251110	8225257	2008-10-14	2012-07-17	Lapsed	United States of America	REDUCING PATH DELAY SENSITIVITY TO TEMPERATURE VARIATION IN TIMING-CRITICAL PATHS
12243768	8001497	2008-10-01	2011-08-16	Granted	United States of America	Control Signal Source Replication
13649996	8539423	2012-10-11	2013-09-17	Lapsed	United States of America	Systematic Benchmarking System And Method For Standardized Data Creation, Analysis And Comparison Of Semiconductor Technology Node Characteristics
13212427	8307324	2011-08-18	2012-11-06	Lapsed	United States of America	Systematic benchmarking system and method for standardized data creation, analysis and comparison of semiconductor technology node characteristics
12365084	8024694	2009-02-03	2011-09-20	Lapsed	United States of America	A Systematic Benchmarking System And Method For Standardized Data Creation, Analysis And Comparison Of Semiconductor Technology Node Characteristics
12206048	7966592	2008-09-08	2011-06-21	Granted	United States of America	Dual Path Static Timing Analysis
12144248	7949986	2008-06-23	2011-05-24	Granted	United States of America	Method for Estimation of Trace Information Bandwidth Requirements
201172482		2011-07-21		Abandoned	Korea, Republic of (KR)	Granular Channel Width for Power Optimization
201110205798X		2011-07-21		Abandoned	China	Granular Channel Width for Power Optimization
100125423		2011-07-19		Abandoned	Taiwan	Granular Channel Width for Power Optimization
12840535	8196086	2010-07-21	2012-06-05	Granted	United States of America	Granular Channel Width for Power Optimization
111747796		2011-07-21		Abandoned	European Patent	Granular Channel Width for Power Optimization
2011158945		2010-07-21	2014-10-03	Lapsed	Japan	Granular Channel Width for Power Optimization
11610825	7617467	2006-12-14	2009-11-10	Lapsed	United States of America	Electrostatic Discharge Device Verification In An Integrated Circuit
12421198	8336012	2009-04-09	2012-12-18	Lapsed	United States of America	Automated Timing Optimization
11567986	7584439	2006-12-07	2009-09-01	Lapsed	United States of America	Cell Modeling For Integrated Circuit Design With Characterization Of Upstream Driver Strength
11749904	7644382	2007-05-17	2010-01-05	Lapsed	United States of America	Command-Language-Based Functional Engineering Change Order (ECO) Implementation
12508898	8219959	2009-07-24	2012-07-10	Lapsed	United States of America	Generating Integrated-Circuit Floorplan Layouts
13549599	8670970	2012-07-16	2014-03-11	Granted	United States of America	Characterizing Performance of an Electronic System
12120894	8255199	2008-05-15	2012-08-28	Lapsed	United States of America	Characterizing Performance Of An Electronic System
11693081	7930674	2007-03-29	2011-04-19	Granted	United States of America	Modifying Integrated Circuit Designs To Achieve Multiple Operating Frequency Targets
11019885	7340697	2004-12-22	2008-03-04	Lapsed	United States of America	Integrated Computer-Aided Circuit Design Kit Facilitating Verification Of Designs Across Different Process Technologies
11469028	8180600	2006-08-31	2012-05-15	Granted	United States of America	Input/Output Buffer Information Specification (IBIS) Model Generation For Multi-Chip Modules (MCM) and Similar Devices

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
11376600	7509609	2006-03-15	2009-03-24	Granted	United States of America	Methods And Apparatus For Reducing Timing Skew
11198930	7480874	2005-08-05	2009-01-20	Lapsed	United States of America	Reliability Analysis Of Integrated Circuits
10880216	7346879	2004-06-29	2008-03-18	Lapsed	United States of America	Symmetric Signal Distribution Through Abutment Connection
10335540	7005873	2002-12-31	2006-02-28	Lapsed	United States of America	Built-In Self-Test Hierarchy For An Integrated Circuit
2003426492	4579531	2003-12-24	2010-09-03	Lapsed	Japan	Built-In Self-Test Hierarchy For An Integrated Circuit
092134419	I303717	2003-12-05	2008-12-01	Lapsed	Taiwan	Built-In Self-Test Hierarchy For An Integrated Circuit
03196847	2394832	2003-08-21	2006-01-25	Lapsed	United Kingdom	SubstrateTopography Comensation at Mask Design: 3D OPC Topography Anchored.
92125773	I-319592	2003-09-18	2010-01-11	Lapsed	Taiwan	Substrate Topography Comensation at Mask Design: 3D OPC Topography Anchored
1020030065848	10-932081	2003-09-23	2009-12-08	Granted	Korea, Republic of (KR)	SubstrateTopography Comensation at Mask Design: 3D OPC Topography Anchored
10254083	6893800	2002-09-24	2005-05-17	Granted	United States of America	SubstrateTopography Comensation at Mask Design: 3D OPC Topography Anchored.
2003328548	4559719	2003-09-19	2010-07-30	Lapsed	Japan	SubstrateTopography Comensation at Mask Design: 3D OPC Topography Anchored.
09866137	6680150	2001-05-25	2004-01-20	Lapsed	United States of America	Proximity Correction Using Shape Engineering
09780861	6728917	2001-02-09	2004-04-27	Lapsed	United States of America	Sequential Test Pattern Generation Using Combinational Techniques
09434961	6578175	1999-11-05	2003-06-10	Granted	United States of America	Method And Apparatus For Evaluating And Correcting Errors In Integrated Circuit Chip Designs
09408371	6463561	1999-09-29	2002-10-08	Granted	United States of America	Almost Full-Scan BIST Method And System Having Higher Fault Coverage And Shorter Test
09427238	6871167	1999-10-26	2005-03-22	Lapsed	United States of America	System And Method For Determining Capacitance For Large-Scale Integrated Circuits
09564438	6732311	2000-05-04	2004-05-04	Lapsed	United States of America	On-Chip Debugger
09283392	6324493	1999-04-01	2001-11-27	Granted	United States of America	Method And Apparatus For Modeling Electromagnetic Interactions In Electrical Circuit Metalizations To Simulate Their Electrical Characteristics
09283393	6289298	1999-04-01	2001-09-11	Granted	United States of America	Method And Apparatus For Quasi Full-Wave Modeling Of Interactions In Circuits
09283394	6397171	1999-04-01	2002-05-28	Granted	United States of America	Method And Apparatus For Modeling Electromagnetic Interactions In Electrical Circuit Metalizations To Simulate Their Electrical Characteristics

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09283395	6367053	1999-04-01	2002-04-02	Granted	United States of America	Method And Apparatus For Modeling Electromagnetic Interactions In Electrical Circuit Metalizations To Simulate Their Electrical Chacteristics
09350645	6545454	1999-07-09	2003-04-08	Granted	United States of America	System And Method For Testing An Integrated Circuit Device Using FFT Analysis Based On A Non\(milterative FFT Coherency Analysis Algorithm
09291448	6363506	1999-04-13	2002-03-26	Granted	United States of America	Method For Self-Testing Integrated Circuits
09197977	6167542	1998-11-23	2000-12-26	Granted	United States of America	An Arrangement For Fault Detection In Circuit Interconnections
09140564	6131174	1998-08-27	2000-10-10	Granted	United States of America	System And Method For Testing Of Embedded Processor
09182543	6370664	1998-10-29	2002-04-09	Granted	United States of America	A Method And Apparatus For Partitioning Long Scan Chains In Scan-Based BISTArchitecture
09240432	6023573	1999-01-29	2000-02-08	Granted	United States of America	Apparatus And Method For Analyzing Circuits Using Reduced-Order Modeling Of Large Linear Subcircuits
09170353	6397349	1998-10-13	2002-05-28	Granted	United States of America	Built-In-Self-Test And Self-Repair Methods And Devices For Computer Memories Comprising A Reconfiguration Memory Device
09170351	6317846	1998-10-13	2001-11-13	Granted	United States of America	System And Method For Detecting Faults In Computer Memories Using A Look Up Table
09338338	6463560	1999-06-23	2002-10-08	Granted	United States of America	A Method For Implementing A BIST Scheme Into Integrated Circuits For Testing RTL Controller-Data Paths In The Integrated Circuits
09058839	6065145	1998-04-13	2000-05-16	Granted	United States of America	Method For Testing Path Delay Faults In Sequential Logic Circuits
09097488	6256759	1998-06-15	2001-07-03	Granted	United States of America	A Hybrid Algorithm For Test Point Selection For Scan-Based BIST
09123380	6170071	1998-07-27	2001-01-02	Granted	United States of America	A Method For Optimizing Test Fixtures To Minimize Vector Load Time For Automated Test Equipment
09120396	6163865	1998-07-22	2000-12-19	Granted	United States of America	Built-In Self-Test Circuit For Read Channel Device
09022759	6148425	1998-02-12	2000-11-14	Granted	United States of America	Built-In Self Test Architecture For Detecting Path-Delay Faults in a Sequential Circuit
08985975	6311146	1997-12-05	2001-10-30	Granted	United States of America	Circuit Simulation With Improved Circuit Partitioning
08867351	6205564	1997-06-02	2001-03-20	Expired	United States of America	Optimized Built-In Self-Test Method And Apparatus For Random Access Memories
08947136	5978935	1997-10-08	1999-11-02	Expired	United States of America	Method For Built-In Self-Testing Of Ring-Address FIFOS Having A Data Input Register With Transparent Latches
08841298	5844821	1997-04-29	1998-12-01	Expired	United States of America	Systems And Methods For Determining Characteristics Of A Singular Circuit
08845963	5930153	1997-04-30	1999-07-27	Expired	United States of America	Systems And Methods For Testing And Manufacturing Large-Scale, Transistor-Based Nonlinear Circuits
08843427	5896401	1997-04-15	1999-04-20	Expired	United States of America	Fault Simulator For Digital Circuitry

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
09036846	6135649	1998-03-09	2000-10-24	Granted	United States of America	Method Of Modeling And Analyzing Electronic Noise Using Pade Approximation-Based Model-Reduction Techniques
08904233	6041170	1997-07-31	2000-03-21	Expired	United States of America	Apparatus And Method For Analyzing Circuits Using Reduced-Order Modeling OfLarge Passive Linear Subcircuits
08905540	6023576	1997-08-04	2000-02-08	Expired	United States of America	Fast Transient Circuit Simulation Of Electronic Circuits Including A Crystal
08962340	6052808	1997-10-31	2000-04-18	Expired	United States of America	Maintenance Registers With Boundary Scan Interface
08902997	5845233	1997-07-30	1998-12-01	Expired	United States of America	Method And Apparatus For Calibrating Timing Analyzer Path Delay Measurements
08901250	6108807	1997-07-28	2000-08-22	Expired	United States of America	Apparatus And Method For Hybrid Pin Control Of Boundary Scan Applications
08866937	6053947	1997-05-31	2000-04-25	Expired	United States of America	Simulation Model Using Object-Oriented Programming
08546055	5680543	1995-10-20	1997-10-21	Expired	United States of America	Method And Apparatus For Built-In Self-Test With Multiple Clock Circuits
08694881	5960009	1996-08-09	1999-09-28	Expired	United States of America	Built In Self Test Method and Apparatus for Booth Multipliers
08365264	5473651	1994-12-28	1995-12-05	Expired	United States of America	Method And Apparatus For Testing Large Embedded Counters
08365394	5513318	1994-12-28	1996-04-30	Expired	United States of America	Method For Built-In Self-Testing Of Ring-Address FIFOs
08233791	5587919	1994-04-22	1996-12-24	Expired	United States of America	Apparatus and Method for Logic Optimization by Redundancy Addition and Removal

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
08909312	5885855	1997-08-14	1999-03-23	Expired	United States of America	Method for distributing connection pads on a semiconductor die
08747325	5952726	1996-11-12	1999-09-14	Expired	United States of America	Flip chip bump distribution on die
2004175054		2004-06-14		Lapsed	Japan	Heatspreader For A Flip Chip Device, And Method For Connecting The Heatspreader
09496989	6681482	2000-02-02	2004-01-27		United States of America	Heatspreader For A Flip\(miChip Device And Method For Connecting The Heatspreader
99056657		1999-11-17		Abandoned	Singapore	Heatspreader For A Flip Chip Device, And Method For Connecting The Heatspreader
11326032		1999-11-16		Application	Japan	Heatspreader For A Flip Chip Device, And Method For Connecting The Heatspreader
1019990049683	662218	1999-11-10	2006-12-21	Granted	Korea, Republic of (KR)	Heatspreader For A Flip Chip Device, And Method For Connecting The Heatspreader
88120078	NI-131285	1999-11-26	2001-04-11	Lapsed	Taiwan	Heatspreader For A Flip Chip Device, And Method For Connecting The Heatspreader
09193832	6118177	1998-11-17	2000-09-12	Granted	United States of America	Heatspreader For A Flip Chip Device, And Method For Connecting The Heatspreader
84102411	NI-078045	1995-03-14	1996-08-29	Expired	Taiwan	Method for Making A Metal to metal Capacitor
953085156		1995-11-28		Abandoned	Spain	Method for Making A Metal to metal Capacitor
953085156		1995-11-28		Abandoned	Netherlands	Method for Making A Metal to metal Capacitor
9547844	273609	1995-12-08	2000-09-04	Lapsed	Korea, Republic of (KR)	Method for Making A Metal to metal Capacitor
7319840	3623569	1995-12-08	2004-12-03	Lapsed	Japan	Method for Making A Metal to metal Capacitor
953085156		1995-11-28		Abandoned	Italy	Method for Making A Metal to metal Capacitor
953085156		1995-11-28		Abandoned	United Kingdom	Method for Making A Metal to metal Capacitor
953085156		1995-11-28		Abandoned	Germany (Federal Republic of)	Method for Making A Metal to metal Capacitor
953085156		1995-11-28		Abandoned	France	Method for Making A Metal to metal Capacitor
951202111		1995-12-04		Abandoned	China	Method for Making A Metal to metal Capacitor
08909563	6040616	1997-08-12	2000-03-21	Expired	United States of America	A Device and Method of Forming A Metal To Metal Capacitor Within an Integrated Circuit
08863713	5825073	1997-05-27	1998-10-20	Expired	United States of America	An Electronic Component For An Integrated Circuit
08472033	5654581	1995-06-06	1997-08-05	Expired	United States of America	Integrated Circuit Capacitor
08644086	5851870	1996-05-09	1998-12-22	Expired	United States of America	Method For Making A Capacitor
10227743	3321101	1998-08-12	2002-06-21	Granted	Japan	A Device and Method of Forming A Metal To Metal Capacitor Within an Integrated Circuit
9832710	280565	1998-08-12	2000-11-10	Granted	Korea, Republic of (KR)	A Device and Method of Forming A Metal To Metal Capacitor Within an Integrated Circuit
08353015	5576240	1994-12-09	1996-11-19	Expired	United States of America	Method for Making A Metal to metal Capacitor

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
60115841		1999-01-13		Expired	United States of America	Use Of Novel Barriers For Ta205 As Gate Capacitor Applications
3001583		2000-01-11		Abandoned	France	Diffusion Barrier For Use With High Dielectric Constant Materials And Electronic Devices Incorporating Same
3001583		2000-01-11		Abandoned	United Kingdom	Diffusion Barrier For Use With High Dielectric Constant Materials And Electronic Devices Incorporating Same
2000004077		2000-01-12		Abandoned	Japan	Diffusion Barrier For Use With High Dielectric Constant Materials And Electronic Devices Incorporating Same
3001583		2000-01-11		Abandoned	Germany (Federal Republic of)	Diffusion Barrier For Use With High Dielectric Constant Materials And Electronic Devices Incorporating Same
20000001552		2000-01-13		Abandoned	Korea, Republic of (KR)	Diffusion Barrier For Use With High Dielectric Constant Materials And Electronic Devices Incorporating Same
89100488		2000-01-13		Abandoned	Taiwan	Diffusion Barrier For Use With High Dielectric Constant Materials And Electronic Devices Incorporating Same
09478647	6340827	2000-01-06	2002-01-22	Granted	United States of America	Diffusion Barrier For Use With High Dielectric Constant Materials And Electronic Devices Incorporating Same
60115783		1999-01-13		Expired	United States of America	Diffusion Barrier For Use With High Dielectric Constant Materials And Electronic Devices Incorporating Same
11356873		1999-12-09		Abandoned	Japan	Deep Sub-Micron Metal Etch With In-Situ Hard Mask Etch
1019990058177	716436	1999-12-16	2007-05-03	Granted	Korea, Republic of (KR)	Deep Sub-Micron Metal Etch With In-Situ Hard Mask Etch
09212228	6194323	1998-12-16	2001-02-27	Granted	United States of America	Deep Sub-Micron Metal Etch With In-Situ Hard Mask Etch
953085370		1995-11-28		Abandoned	France	Method Of Forming Metal Layers Formed As A Composite Of Sub-Layers Using TI Texture Control Layer
953085370		1995-11-28		Abandoned	Germany (Federal Republic of)	Method Of Forming Metal Layers Formed As A Composite Of Sub-Layers Using TI Texture Control Layer
953085370		1995-11-28		Abandoned	United Kingdom	Method Of Forming Metal Layers Formed As A Composite Of Sub-Layers Using TI Texture Control Layer
953085370		1995-11-28		Abandoned	Italy	Method Of Forming Metal Layers Formed As A Composite Of Sub-Layers Using TI Texture Control Layer
7337694	3707627	1995-12-04	2005-08-12	Expired	Japan	Method Of Forming Metal Layers Formed As A Composite Of Sub-Layers Using TI Texture Control Layer
9546636		1995-12-05		Abandoned	Korea, Republic of (KR)	Method Of Forming Metal Layers Formed As A Composite Of Sub-Layers Using TI Texture Control Layer

AppNo	PatentNo	FiledDate	GrantDate	Status	Country	Title
95020178	33616	1995-11-28	1997-12-19	Lapsed	Singapore	Method Of Forming Metal Layers Formed As A Composite Of Sub-Layers Using TI Texture Control Layer
08349649	5523259	1994-12-05	1996-06-04	Expired	United States of America	Method Of Forming Metal Layers Formed As A Composite Of Sub-Layers Using TI Texture Control Layer
3420751995		1995-12-28		Abandoned	Japan	Novel barrier layer treatments for Tungsten plug
9565271		1995-12-29		Abandoned	Korea, Republic of (KR)	Novel barrier layer treatments for Tungsten plug
08366867	5599739	1994-12-30	1997-02-04	Expired	United States of America	Novel barrier layer treatments for Tungsten plug
10600255	6798035	2003-06-20	2004-09-28	Granted	United States of America	Bonding pad for low k dielectric
09752626	6591410	2000-12-28	2003-07-08	Granted	United States of America	Six-to-one signal/power ratio bump and trace pattern for flip chip design
2008124287		2008-05-12		Abandoned	Japan	Tungsten Formation Process
08329806	6323126	1994-10-26	2001-11-27	Granted	United States of America	Tungsten Formation Process
943074658		1994-10-12		Abandoned	France	Tungsten Formation Process
6255908		1994-10-24		Abandoned	Japan	Tungsten Formation Process
943074658		1994-10-12		Abandoned	Germany (Federal Republic of)	Tungsten Formation Process
943074658		1994-10-12		Abandoned	United Kingdom	Tungsten Formation Process
943074658		1994-10-12		Abandoned	Italy	Tungsten Formation Process
8141780		1993-10-22		Abandoned	United States of America	Tungsten Formation Process
9426313		1994-10-14		Abandoned	Korea, Republic of (KR)	Tungsten Formation Process
09864577	6472304	2001-05-24	2002-10-29	Granted	United States of America	Wire Bonding To Copper
3002086	60039800.5	2000-01-13	2008-08-13	Granted	Germany (Federal Republic of)	Wire Bonding To Copper
3002086	1022776	2000-01-13	2008-08-13	Lapsed	United Kingdom	Wire Bonding To Copper
3002086	1022776	2000-01-13	2008-08-13	Lapsed	France	Wire Bonding To Copper
9236406		1999-01-23		Abandoned	United States of America	Wire Bonding To Copper
2000007951	3575676	2000-01-17	2004-07-16	Granted	Japan	Wire Bonding To Copper
2000003060	659801	2000-01-22	2006-12-13	Granted	Korea, Republic of (KR)	Wire Bonding To Copper
88120537	NI-129005	1999-11-24	2001-03-21	Granted	Taiwan	Wire Bonding To Copper
08116309	5643838	1993-09-03	1997-07-01	Expired	United States of America	Low Temperature Deposition of Silicon Oxides for Device Fabrication
08645852	5693561	1996-05-14	1997-12-02	Expired	United States of America	Method Of Integrated Circuit Fabrication Including A Step Of Depositing Tungsten
09370422	6153543	1999-08-09	2000-11-28	Granted	United States of America	High Density Plasma Passivation Layer And Method Of Application

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,646,091 B2
APPLICATION NO. : 11/399723
DATED : January 12, 2010
INVENTOR(S) : Maurice O. Othieno, Chok J. Chia and Amar J. Amin

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification

In Column 1, Line 17, replace "substrates to hold and electrically interconnect integrated" with --substrates to hold and electrically interconnect an integrated--.

In Column 1, Line 18, replace "circuit (IC) die mounted within the packaging substrate. In" with --circuit (IC) die mounted within the packaging substrates. In--.

In Column 1, Line 24, replace "ground planes for grounding the circuitry of integrated circuit" with --ground planes for grounding the circuitry of an integrated circuit--.

In Column 1, Line 35, replace "employed. In one common implementation semiconductor" with --employed. In one common implementation a semiconductor--.

In Column 2, Line 9, replace "much of a problem. However, at highs speeds a number of" with --much of a problem. However, at high speeds a number of--.

In Column 2, Line 15, replace "are configured the I/O and ground contacts spaced more" with --are configured with the I/O and ground contacts spaced more--.

In Column 2, Line 34, replace "the traditional package format is increasingly proving be" with --the traditional package format is increasingly proving to be--.

In Column 2, Line 58, replace "first ground plane. The second ground plane electrically" with --first ground plane. The second ground plane is electrically--.

In Column 2, Line 60, replace "further including peripheral electrical contacts" with --further includes peripheral electrical contacts--.

Signed and Sealed this
Twenty-seventh Day of April, 2021

Drew Hirshfeld
Performing the Functions and Duties of the Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office

In Column 2, Line 66, replace "In another embodiment the invention includes" with --In another embodiment the invention includes a--.

In Column 4, Line 20, replace "circuitry. Also, this particularly the case for high-speed" with --circuitry. Also, this is particularly the case for high-speed--.

In Column 4, Line 23, replace "data rates and frequencies are considered non-high speed" with --data rates and frequencies is considered non-high speed--.

In Column 4, Line 39, replace "facilitates by conductive vias that pass through the" with --facilitated by conductive vias that pass through the--.

In Column 4, Line 40, replace "and are electrically connected to both, a ground plane" with --and are electrically connected to both a ground plane--.

In Column 4, Line 60, replace "invention. The depicted embodiment is view in plan view. The" with --invention. The depicted embodiment is viewed in plan view. The--.

In Column 5, Line 13, replace "metallization structures are arranged about a die attachment" with --metallization structures that are arranged about a die attachment--.

In Column 5, Line 52, replace "ground plane 311 devoted to grounding only the" with --ground plane 331 devoted to grounding only the--.

In Column 6, Line 8, replace "fingers 334, high-speed ground 331, VDD core 312, and" with --fingers 334, high-speed ground plane 331, VDD core 312, and--.

In Column 6, Line 16, replace "ground plane 331 and its associated vias 321. The low speed" with --ground plane 331 and its associated vias 322. The low speed--.

In Column 6, Line 41, replace "H is tripled (to at least 140 μm) relative to the low speed" with --H is tripled (to at least 200 μm) relative to the low speed--.

In Column 7, Line 4, replace "FIG. 5 schematically depicts a portion another" with --FIG. 5 schematically depicts a portion of another--.

In Column 7, Line 6, replace "are assembled into a completed package 500. For sake of" with --are assembled into a completed package. For sake of--.

In Column 7, Line 16, replace "fingers (not shown in this view). Similarly, the speed portions" with --fingers (not shown in this view). Similarly, the high speed portions--.

In Column 7, Line 23, replace "and low speed circuitry of each of the depicted die. As" with --and low speed circuitry of each of the depicted dies. As--.

In Column 7, Line 25, replace "need not be the case. The die 501, 502 and upper metallization" with

--need not be the case. The dies 501, 502 and upper metallization--.

In Column 7, Line 28, replace "package 500. These commonly include, but are not limited to" with --package. These commonly include, but are not limited to--.

In Column 7, Line 33, replace "of the invention. The substrate is 600 is rendered in" with --of the invention. The substrate 600 is rendered in--.

In Column 7, Line 41, replace "material (e.g., ceramic materials and the like)" with --materials (e.g., ceramic materials and the like)--.

In Column 7, Line 51, replace "The depicted substrate 300 further includes a series of" with --The depicted substrate 600 further includes a series of--.

In Column 8, Line 36, replace "As before, the vias 321 electrically connect the high-speed" with --As before, the vias 621 electrically connect the high-speed--.

In the Claims

In Column 9, Line 41, replace "the third ground plane configured for electrical" in Claim 1 with --the fourth ground plane configured for electrical--.

In Column 9, Line 58, replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In Column 9, Line 60, replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In Column 10, Line 3, replace "μm (micrometers) and wherein the second set of electrical are" with -- μm (micrometers) and wherein the second set of electrical contacts are--.

In Column 10, Line 18, replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In Column 10, Line 20, replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In Column 10, Line 27, replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In Column 10, Line 29, replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In Column 10, Line 37, replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In Column 10, Line 39, replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In Column 10, Line 41, replace "the first spacing between the contacts of the first set of" with --a first spacing between the contacts of the first set of--.

In Column 10, Line 49, replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In Column 10, Line 51, replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In Column 11, Line 2, replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In Column 11, Line 4, replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In Column 11, Line 21, replace "arrangement comprises a die having both high-speed" with --arrangement comprises a die having both the high-speed--.

In Column 11, Line 22, replace "circuitry and low-speed electronic circuitry; and" with --circuitry and the low-speed electronic circuitry; and--.

In Column 11, Line 25, replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In Column 12, Line 2, replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In Column 12, Line 12, replace "14. An IC package as recited in claim 13 wherein the die" with --14. An IC package as recited in claim 12 wherein the die--.

In Column 12, Line 14, replace "least one die has high-speed electronic circuitry and wherein" with --least one die has the high-speed electronic circuitry and wherein--.

In Column 12, Line 15, replace "at least one die has low-speed electronic circuitry;" with --at least one die has the low-speed electronic circuitry;--.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/399,723	04/06/2006	Maurice O. Othieno	05-2572/LSI1P272	1398

22186 7590 04/06/2021

MENDELSOHN DUNLEAVY, P.C.
1500 JOHN F. KENNEDY BLVD., SUITE 910
PHILADELPHIA, PA 19102

EXAMINER
CRUZ, LESLIE PILAR

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
04/06/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@mendelip.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Patent No.: 7646091
Issue Date: 01/12/2010
Appl. No.: 11/399,723
Filed: 04/06/2006

PART (A) RESPONSE FOR CERTIFICATES OF CORRECTION

This is a decision on the Certificate of Correction request filed 04 March 2021.

The request for issuance of Certificate of Correction for the above-identified correction(s) under the provisions of 37 CFR 1.322 and/or 1.323 is hereby:

(Check one)
☑ Approved ☐ Approved in Part ☐ Denied

Comments: ____

PART (B) PETITION UNDER 37 CFR 1.324 OR 37 CFR 1.48

☐ This is a decision on the petition filed ____ to correct inventorship under 37 CFR 1.324.

☐ This is a decision on the request under 37 CFR 1.48, petition filed ____. In view of the fact that the patent has already issued, the request under 37 CFR 1.48 has been treated as a petition to correct inventorship under 37 CFR 1.324.

The petition is hereby: ☐ Granted ☐ Dismissed

Comment: ____

The patented filed is being forwarded to Certificate of Corrections Branch for issuance of a certificate naming only the actual inventor or inventors.

/DAVIENNE N MONBLEAU/
Supervisory Patent Examiner, Art Unit 2826
Technology Center 2800
Phone: (571)272-1945

Certificates of Correction Branch email: CustomerServiceCoC@uspto.gov CoC Central Phone Number: (703) 756-1814

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/399,723	04/06/2006	Maurice O. Othieno	05-2572/LSI1P272

CONFIRMATION NO. 1398

POWER OF ATTORNEY NOTICE

24319
Broadcom Limited
4380 Ziegler Road
Fort Collins, CO 80525

OC000000123896941

Date Mailed: 03/10/2021

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/04/2021.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/cnguyen/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/399,723	04/06/2006	Maurice O. Othieno	05-2572/LSI1P272

CONFIRMATION NO. 1398

22186
MENDELSOHN DUNLEAVY, P.C.
1500 JOHN F. KENNEDY BLVD., SUITE 910
PHILADELPHIA, PA 19102

POA ACCEPTANCE LETTER

OC000000123896961

Date Mailed: 03/10/2021

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/04/2021.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/cnguyen/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re: Attorney Docket No. 1385.002A

In re application of: Maurice O. Othieno, Chok J. Chia, and Amar J. Amin

Patent No.: 7,646,091
Issued: 01/12/10

For: Semiconductor Package and Method Using Isolated Vss Plane to Accommodate High Speed Circuitry Ground Isolation

PETITION FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed is a Certificate of Correction listing errors that appear in the above-referenced patent as a result of mistakes of a clerical nature, of a typographical nature, and/or of minor character, the corrections of which neither constitute new matter nor require reexamination. In the following, for ease of identification, the changes corresponding to the corrections are indicated by underlining.

In column 1, line 17, please replace "substrates to hold and electrically interconnect integrated" with --substrates to hold and electrically interconnect an integrated--.

In column 1, line 18, please replace "circuit (IC) die mounted within the packaging substrate. In" with --circuit (IC) die mounted within the packaging substrates. In--.

In column 1, line 24, please replace "ground planes for grounding the circuitry of integrated circuit" with --ground planes for grounding the circuitry of an integrated circuit--.

In column 1, line 35, please replace "employed. In one common implementation semiconductor" with --employed. In one common implementation a semiconductor--.

In column 2, line 9, please replace "much of a problem. However, at highs speeds a number of" with --much of a problem. However, at high speeds a number of--.

In column 2, line 15, please replace "are configured the I/O and ground contacts spaced more" with --are configured with the I/O and ground contacts spaced more--.

In column 2, line 34, please replace "the traditional package format is increasingly proving be" with --the traditional package format is increasingly proving to be--.

In column 2, line 58, please replace "first ground plane. The second ground plane electrically" with --first ground plane. The second ground plane is electrically--.

In column 2, line 60, please replace "further including peripheral electrical contacts" with --further includes peripheral electrical contacts--.

In column 2, line 66, please replace "In another embodiment the invention includes" with --In another embodiment the invention includes a--.

In column 4, line 20, please replace "circuitry. Also, this particularly the case for high-speed" with --circuitry. Also, this is particularly the case for high-speed--.

In column 4, line 23, please replace "data rates and frequencies are considered non-high speed" with --data rates and frequencies is considered non-high speed--.

In column 4, line 39, please replace "facilitates by conductive vias that pass through the" with --facilitated by conductive vias that pass through the--.

In column 4, line 40, please replace "and are electrically connected to both, a ground plane" with --and are electrically connected to both a ground plane--.

In column 4, line 60, please replace "invention. The depicted embodiment is view in plan view. The" with --invention. The depicted embodiment is viewed in plan view. The--.

In column 5, line 13, please replace "metallization structures are arranged about a die attachment" with --metallization structures that are arranged about a die attachment--.

In column 5, line 52, please replace "ground plane **311** devoted to grounding only the" with --ground plane **331** devoted to grounding only the--. Support for this correction is found, for example, in column 5, lines 47-48 ("The high-speed ground plane 331").

In column 6, line 8, please replace "fingers **334**, high-speed ground **331**, $V_{DD\ core}$ **312**, and" with --fingers **334**, high-speed ground plane **331**, $V_{DD\ core}$ **312**, and --. Support for this correction is found, for example, in column 5, lines 47-48 ("The high-speed ground plane 331").

In column 6, line 16, please replace "ground plane **331** and its associated vias **321**. The low speed" with --ground plane **331** and its associated vias **322**. The low speed--. Support for this correction is found, for example, in column 5, lines 58-60 ("The vias **322** electrically connect the high-speed ground plane **331** with underlying solder pads having solder balls formed thereon.") and in element **322** of FIG. **3**.

In column 6, line 41, please replace "H is tripled (to at least 140 μm) relative to the low speed" with --H is tripled (to at least 200 μm) relative to the low speed--. Support for this correction is found, for example, in column 6, lines 21-23 ("In the depicted example, the low speed fingers **314** are spaced apart a distance L of about least 70 μm (micrometers)."); column 6, lines 40-42 ("In another embodiment, the distance H is tripled … relative to the low speed distance L."); and column 10, lines 3-4 ("wherein the second set of electrical [contacts] are spaced apart a distance of at least 200 μm (micrometers)").

In column 7, line 4, please replace "FIG. 5 schematically depicts a portion another" with --FIG. 5 schematically depicts a portion of another--.

In column 7, line 6, please replace "are assembled into a completed package 500. For sake of" with --are assembled into a completed package. For sake of--. Support for this correction is found, for example, in the figures and, in particular, in FIG. 5, which does not have a label "500".

In column 7, line 16, please replace "fingers (not shown in this view). Similarly, the speed portions" with --fingers (not shown in this view). Similarly, the high speed portions--. Support for this correction is found, for example, in column 5, lines 47-48 ("The high-speed ground plane 331").

In column 7, line 23, please replace "and low speed circuitry of each of the depicted die. As" with --and low speed circuitry of each of the depicted dies. As--.

In column 7, line 25, please replace "need not be the case. The die 501, 502 and upper metallization" with --need not be the case. The dies 501, 502 and upper metallization--.

In column 7, line 28, please replace "package 500. These commonly include, but are not limited to" with --package. These commonly include, but are not limited to--. Support for this correction is found, for example, in the figures and, in particular, in FIG. 5, which does not have a label "500".

In column 7, line 33, please replace "of the invention. The substrate is 600 is rendered in" with --of the invention. The substrate 600 is rendered in--.

In column 7, line 41, please replace "material (e.g., ceramic materials and the like)" with --materials (e.g., ceramic materials and the like)--.

In column 7, line 51, please replace "The depicted substrate 300 further includes a series of" with --The depicted substrate 600 further includes a series of--. Support for this correction is found, for example, in column 7, line 42 ("The depicted substrate **600**") and in element 600 of FIG. 6.

In column 8, line 36, please replace "As before, the vias 321 electrically connect the high-speed" with --As before, the vias 621 electrically connect the high-speed--. Support for this correction is found, for example, in element 621 of FIG. 6.

In column 9, line 41, please replace "the third ground plane configured for electrical" in claim 1 with --the fourth ground plane configured for electrical--. Support for this correction is found, for example, in high-speed ground plane 631 of FIG. 6 and in column 8, lines 26-30 and lines 55-58. As taught in column 8, lines 26-30, the high-speed ground plane 631 is (i) dedicated to the grounding of high-speed circuitry and is (ii) electrically and spatially isolated from the low-speed ground plane 611. As taught in column 8, lines 55-58, the principles and methodologies described here can readily be used to construct any multi-layer configuration.

The low-speed ground plane 611 of FIG. 6 is an example of the third ground plane recited in claim 1, and the high-speed ground plane 631 of FIG. 6 is an example of the fourth ground plane recited in claim 1. The third and fourth ground planes are analogous to the first and second ground planes recited in claim 1, where the first ground plane enables "electrical connection with low speed electronic circuitry" and the second ground plane enables "electrical connection with high speed electronic circuitry." See column 9, lines 30-35.

Due to a mistake of a clerical nature, a typographical nature, or of minor character that neither constitutes new matter nor requires reexamination, the third ground plane was incorrectly recited in claim 1 as being both "configured for electrical connection with low speed electronic circuitry" (column 9, lines

37-38) and "configured for electrical connection with high speed electronic circuitry" (column 9, lines 41-42). The proposed correction would result in the third ground plane being "configured for electrical connection with low speed electronic circuitry" and the fourth ground plane being "configured for electrical connection with high speed electronic circuitry," which comports with both the explicit teachings of the specification and the analogous recitations for the first and second ground planes.

In column 9, line 58, please replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In column 9, line 60, please replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In column 10, line 3, please replace "μm (micrometers) and wherein the second set of electrical are" with --μm (micrometers) and wherein the second set of electrical contacts are--.

In column 10, line 18, please replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In column 10, line 20, please replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In column 10, line 27, please replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In column 10, line 29, please replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In column 10, line 37, please replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In column 10, line 39, please replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In column 10, line 41, please replace "the first spacing between the contacts of the first set of" with --a first spacing between the contacts of the first set of--.

In column 10, line 49, please replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In column 10, line 51, please replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In column 11, line 2, please replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In column 11, line 4, please replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In column 11, line 21, please replace "arrangement comprises a die having both high-speed" with --arrangement comprises a die having both the high-speed--.

In column 11, line 22, please replace "circuitry and low-speed electronic circuitry; and" with --circuitry and the low-speed electronic circuitry; and--.

In column 11, line 25, please replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In column 12, line 2, please replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In column 12, line 12, please replace "14. An IC package as recited in claim 13 wherein the die" with --14. An IC package as recited in claim 12 wherein the die--. Support for this correction is found, for example, in FIG. 5, where die 501 has low-speed electronic circuitry and die 502 has high-speed electronic circuitry. See, also, column 7, lines 9-11 ("In the depicted example, one die **501** includes low speed circuitry and another stacked die **502** includes high-speed circuitry.").

In column 12, line 14, please replace "least one die has high-speed electronic circuitry and wherein" with --least one die has the high-speed electronic circuitry and wherein--.

In column 12, line 15, please replace "at least one die has low-speed electronic circuitry;" with --at least one die has the low-speed electronic circuitry;--.

[X] The Commissioner is hereby authorized to charge payment of any fees required under 37 CFR §§ 1.20(a) associated with this communication or credit any overpayment to **Mendelsohn Dunleavy, P.C., Deposit Account No. 50-0782**.

Respectfully submitted,

Date: 03/04/2021
Customer No. 22186
Mendelsohn Dunleavy, P.C.
1500 John F. Kennedy Blvd., Suite 910
Philadelphia, Pennsylvania 19102

/Steve Mendelsohn/
Steve Mendelsohn
Registration No. 35,951
Attorney for Applicant
(215) 557-6657 (phone)
(215) 557-8477 (fax)

PTO/SB/44 (09-07)
Approved for use through 03/31/2023. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,646,091

APPLICATION NO.: 11/399,723

ISSUE DATE : 01/12/2010

INVENTOR(S) : Maurice O. Othieno, Chok J. Chia, and Amar J. Amin

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 1, line 17, replace "substrates to hold and electrically interconnect integrated" with --substrates to hold and electrically interconnect an integrated--.

In column 1, line 18, replace "circuit (IC) die mounted within the packaging substrate. In" with --circuit (IC) die mounted within the packaging substrates. In--.

In column 1, line 24, replace "ground planes for grounding the circuitry of integrated circuit" with --ground planes for grounding the circuitry of an integrated circuit--.

In column 1, line 35, replace "employed. In one common implementation semiconductor" with --employed. In one common implementation a semiconductor--.

In column 2, line 9, replace "much of a problem. However, at highs speeds a number of" with --much of a problem. However, at high speeds a number of--.

In column 2, line 15, replace "are configured the I/O and ground contacts spaced more" with --are configured with the I/O and ground contacts spaced more--.

In column 2, line 34, replace "the traditional package format is increasingly proving be" with --the traditional package format is increasingly proving to be--.

In column 2, line 58, replace "first ground plane. The second ground plane electrically" with --first ground plane. The second ground plane is electrically--.

In column 2, line 60, replace "further including peripheral electrical contacts" with --further includes peripheral electrical contacts--.

In column 2, line 66, replace "In another embodiment the invention includes" with --In another embodiment the invention includes a--.

MAILING ADDRESS OF SENDER (Please do not use Customer Number below):

Steve Mendelsohn
Mendelsohn Dunleavy, P.C.
1500 John F. Kennedy Blvd., Suite 910, Philadelphia, Pennsylvania 19102

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/44 (09-07)
Approved for use through 03/31/2023. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,646,091

APPLICATION NO.: 11/399,723

ISSUE DATE : 01/12/2010

INVENTOR(S) : Maurice O. Othieno, Chok J. Chia, and Amar J. Amin

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 4, line 20, replace "circuitry. Also, this particularly the case for high-speed" with --circuitry. Also, this is particularly the case for high-speed--.

In column 4, line 23, replace "data rates and frequencies are considered non-high speed" with --data rates and frequencies is considered non-high speed--.

In column 4, line 39, replace "facilitates by conductive vias that pass through the" with --facilitated by conductive vias that pass through the--.

In column 4, line 40, replace "and are electrically connected to both, a ground plane" with --and are electrically connected to both a ground plane--.

In column 4, line 60, replace "invention. The depicted embodiment is view in plan view. The" with --invention. The depicted embodiment is viewed in plan view. The--.

In column 5, line 13, replace "metallization structures are arranged about a die attachment" with --metallization structures that are arranged about a die attachment--.

In column 5, line 52, replace "ground plane 311 devoted to grounding only the" with --ground plane 331 devoted to grounding only the--.

In column 6, line 8, replace "fingers 334, high-speed ground 331, VDD core 312, and" with --fingers 334, high-speed ground plane 331, VDD core 312, and --.

In column 6, line 16, replace "ground plane 331 and its associated vias 321. The low speed" with --ground plane 331 and its associated vias 322. The low speed--.

In column 6, line 41, replace "H is tripled (to at least 140 μm) relative to the low speed" with --H is tripled (to at least 200 μm) relative to the low speed--.

MAILING ADDRESS OF SENDER (Please do not use Customer Number below):

Steve Mendelsohn
Mendelsohn Dunleavy, P.C.
1500 John F. Kennedy Blvd., Suite 910, Philadelphia, Pennsylvania 19102

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/44 (09-07)
Approved for use through 03/31/2023. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,646,091

APPLICATION NO.: 11/399,723

ISSUE DATE : 01/12/2010

INVENTOR(S) : Maurice O. Othieno, Chok J. Chia, and Amar J. Amin

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 7, line 4, replace "FIG. 5 schematically depicts a portion another" with --FIG. 5 schematically depicts a portion of another--.

In column 7, line 6, eplace "are assembled into a completed package 500. For sake of" with --are assembled into a completed package. For sake of--.

In column 7, line 16, replace "fingers (not shown in this view). Similarly, the speed portions" with --fingers (not shown in this view). Similarly, the high speed portions--.

In column 7, line 23, replace "and low speed circuitry of each of the depicted die. As" with --and low speed circuitry of each of the depicted dies. As--.

In column 7, line 25, replace "need not be the case. The die 501, 502 and upper metallization" with --need not be the case. The dies 501, 502 and upper metallization--.

In column 7, line 28, replace "package 500. These commonly include, but are not limited to" with --package. These commonly include, but are not limited to--.

In column 7, line 33, replace "of the invention. The substrate is 600 is rendered in" with --of the invention. The substrate 600 is rendered in--.

In column 7, line 41, replace "material (e.g., ceramic materials and the like)" with --materials (e.g., ceramic materials and the like)--.

In column 7, line 51, replace "The depicted substrate 300 further includes a series of" with --The depicted substrate 600 further includes a series of--.

MAILING ADDRESS OF SENDER (Please do not use Customer Number below):

Steve Mendelsohn
Mendelsohn Dunleavy, P.C.
1500 John F. Kennedy Blvd., Suite 910, Philadelphia, Pennsylvania 19102

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/44 (09-07)
Approved for use through 03/31/2023. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,646,091

APPLICATION NO.: 11/399,723

ISSUE DATE : 01/12/2010

INVENTOR(S) : Maurice O. Othieno, Chok J. Chia, and Amar J. Amin

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 8, line 36, replace "As before, the vias 321 electrically connect the high-speed" with --As before, the vias 621 electrically connect the high-speed--.

In column 9, line 41, replace "the third ground plane configured for electrical" in claim 1 with --the fourth ground plane configured for electrical--.

In column 9, line 58, replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In column 9, line 60, replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In column 10, line 3, replace "μm (micrometers) and wherein the second set of electrical are" with --μm (micrometers) and wherein the second set of electrical contacts are--.

In column 10, line 18, replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In column 10, line 20, replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In column 10, line 27, rreplace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In column 10, line 29, replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

MAILING ADDRESS OF SENDER (Please do not use Customer Number below):

Steve Mendelsohn
Mendelsohn Dunleavy, P.C.
1500 John F. Kennedy Blvd., Suite 910, Philadelphia, Pennsylvania 19102

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/44 (09-07)
Approved for use through 03/31/2023. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,646,091

APPLICATION NO.: 11/399,723

ISSUE DATE : 01/12/2010

INVENTOR(S) : Maurice O. Othieno, Chok J. Chia, and Amar J. Amin

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 10, line 37, replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In column 10, line 39, replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In column 10, line 41, replace "the first spacing between the contacts of the first set of" with --a first spacing between the contacts of the first set of--.

In column 10, line 49, replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In column 10, line 51, replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In column 11, line 2, replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

In column 11, line 4, replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In column 11, line 21, replace "arrangement comprises a die having both high-speed" with --arrangement comprises a die having both the high-speed--.

In column 11, line 22, replace "circuitry and low-speed electronic circuitry; and" with --circuitry and the low-speed electronic circuitry; and--.

In column 11, line 25, replace "with low speed electronic circuitry; and" with --with the low speed electronic circuitry; and--.

MAILING ADDRESS OF SENDER (Please do not use Customer Number below):

Steve Mendelsohn
Mendelsohn Dunleavy, P.C.
1500 John F. Kennedy Blvd., Suite 910, Philadelphia, Pennsylvania 19102

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/44 (09-07)
Approved for use through 03/31/2023. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,646,091

APPLICATION NO.: 11/399,723

ISSUE DATE : 01/12/2010

INVENTOR(S) : Maurice O. Othieno, Chok J. Chia, and Amar J. Amin

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 12, line 2, replace "with high speed electronic circuitry; and" with --with the high speed electronic circuitry; and--.

In column 12, line 12, replace "14. An IC package as recited in claim 13 wherein the die" with --14. An IC package as recited in claim 12 wherein the die--.

In column 12, line 14, replace "least one die has high-speed electronic circuitry and wherein" with --least one die has the high-speed electronic circuitry and wherein--.

In column 12, line 15, replace "at least one die has low-speed electronic circuitry;" with --at least one die has the low-speed electronic circuitry;--.

MAILING ADDRESS OF SENDER (Please do not use Customer Number below):

Steve Mendelsohn
Mendelsohn Dunleavy, P.C.
1500 John F. Kennedy Blvd., Suite 910, Philadelphia, Pennsylvania 19102

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	11399723
Filing Date:	06-Apr-2006
Title of Invention:	SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION
First Named Inventor/Applicant Name:	Maurice O. Othieno
Filer:	Steve Mendelsohn/Eri Yoneda
Attorney Docket Number:	05-2572/LSI1P272

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
CERTIFICATE OF CORRECTION	1811	1	160	160

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**160**

Electronic Acknowledgement Receipt

EFS ID:	42094829
Application Number:	11399723
International Application Number:	
Confirmation Number:	1398
Title of Invention:	SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION
First Named Inventor/Applicant Name:	Maurice O. Othieno
Customer Number:	24319
Filer:	Steve Mendelsohn/Eri Yoneda
Filer Authorized By:	Steve Mendelsohn
Attorney Docket Number:	05-2572/LSI1P272
Receipt Date:	04-MAR-2021
Filing Date:	06-APR-2006
Time Stamp:	19:05:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$160
RAM confirmation Number	E202134J07373865
Deposit Account	500782
Authorized User	Eri Yoneda

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	1385-002A_Petition_for_Certificate_of_Correction_7646091_2021-03-04.pdf	318012 a1a2379802ff4304aa96a3ff8cb598c45a2558bb	no	11
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30543 d03d9173501cecc3f924be9a0866cf9d9562d8f2	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	348555		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/81A (12-08)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

Patent Number	7,646,091
Issue Date	01/12/2010
First Named Inventor	Maurice O. Othieno
Title	SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION
Attorney Docket No.	05-2572/LSI1P272

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

22186

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

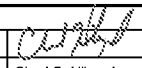
☐ Inventor, having ownership of the patent.

OR

☒ Patent owner.

Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on _____.

SIGNATURE of Inventor or Patent Owner

Signature		Date	February 23, 2021
Name	Chad S. Hilyard	Telephone	
Title and Company	President		

NOTE: Signatures of all the inventors or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.

☒ A total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 15 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/96 (11-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: BELL SEMICONDUCTOR, LLC

Application No./Patent No.: 7,646,091 Filed/Issue Date: 01/12/2010

Titled: SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION

BELL SEMICONDUCTOR, LLC, a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;

2. ☐ an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is _____ %); or

3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel_____, Frame_____, or a copy* is attached.

OR

B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Inventors To: LSI LOGIC COPORATION

The document was recorded in the United States Patent and Trademark Office at Reel 017775, Frame 0366, or a copy* is attached.

2. From: LSI LOGIC CORPORATION To: LSI CORPORATION

The document was recorded in the United States Patent and Trademark Office at Reel 033102, Frame 0270, or a copy* is attached.

3. From: LSI CORPORATION To: AVAGO TECHNOLOGIES GENERAL IP (SINGAPORE) PTE. LTD.

The document was recorded in the United States Patent and Trademark Office at Reel 035390, Frame 0388, or a copy* is attached.

☒ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ *As required by 37 CFR 3.73(b)(1)(i), if a copy/copies is/are attached, the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature — February 23, 2021 Date

Chad S. Hilyard — President

Printed or Typed Name — Title or Registration Number

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

B. A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

4. From: AVAGO TECHNOLOGIES GENERAL IP (SINGAPORE) PTE. LTD To: BELL SEMICONDUCTOR, LLC

The document was recorded in the United States Patent and Trademark Office at Reel 044886, Frame 0766

Electronic Acknowledgement Receipt

EFS ID:	42085136
Application Number:	11399723
International Application Number:	
Confirmation Number:	1398
Title of Invention:	SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION
First Named Inventor/Applicant Name:	Maurice O. Othieno
Customer Number:	24319
Filer:	Steve Mendelsohn/Eri Yoneda
Filer Authorized By:	Steve Mendelsohn
Attorney Docket Number:	05-2572/LSI1P272
Receipt Date:	04-MAR-2021
Filing Date:	06-APR-2006
Time Stamp:	09:37:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	05-2572_LSI1P272_1385-002A_POA81a_Signed.pdf	122189 bc8ddb677e644d1780c420839a206adac860e507	no	1

Warnings:

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	05-2572_LSI1P272_1385-002A_Statement_Under_37_CFR_373b_Signed.pdf	234659 244e2ff747eff94432cc47eb417cc908b2d04542	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	356848		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/399,723	01/12/2010	7646091	05-2572/LSI1P272	1398

24319 7590 12/23/2009

LSI CORPORATION
1621 BARBER LANE
MS: D-105
MILPITAS, CA 95035

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 433 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Maurice O. Othieno, Union City, CA;
Chok J. Chia, Cupertino, CA;
Amar J. Amin, Milpitas, CA;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

24319 7590 09/30/2009

LSI CORPORATION
1621 BARBER LANE
MS: D-105
MILPITAS, CA 95035

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/399,723	04/06/2006	Maurice O. Othieno	05-2572/LSI1P272	1398

TITLE OF INVENTION: SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	12/30/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
CRUZ, LESLIE PILAR	2826	257-691000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Beyer Law Group LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: LSI Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Milpitas, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee

☒ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 504481 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date November 24, 2009

Typed or printed name Francis T. Kalinski II Registration No. 44,177

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	11399723
Filing Date:	06-Apr-2006
Title of Invention:	SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION
First Named Inventor/Applicant Name:	Maurice O. Othieno
Filer:	Francis Theodor Kalinski II/Dawn Wold
Attorney Docket Number:	05-2572/LSI1P272

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1810**

Electronic Acknowledgement Receipt

EFS ID:	6522310
Application Number:	11399723
International Application Number:	
Confirmation Number:	1398
Title of Invention:	SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION
First Named Inventor/Applicant Name:	Maurice O. Othieno
Customer Number:	24319
Filer:	Francis Theodor Kalinski II/Dawn Wold
Filer Authorized By:	Francis Theodor Kalinski II
Attorney Docket Number:	05-2572/LSI1P272
Receipt Date:	24-NOV-2009
Filing Date:	06-APR-2006
Time Stamp:	20:03:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1810
RAM confirmation Number	7144
Deposit Account	504481
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	LSI1P272_Issue_Fee.pdf	123988 3886eca559196585f46c8cf92a8e30a482b4854d	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	32283 cbdf443fac83d278f3ceb748aab2778614a5b009	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	156271		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

24319 7590 09/30/2009

LSI CORPORATION
1621 BARBER LANE
MS: D-105
MILPITAS, CA 95035

EXAMINER	
CRUZ, LESLIE PILAR	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/30/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/399,723	04/06/2006	Maurice O. Othieno	05-2572/LSI1P272	1398

TITLE OF INVENTION: SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	12/30/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

24319 7590 09/30/2009

LSI CORPORATION
1621 BARBER LANE
MS: D-105
MILPITAS, CA 95035

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/399,723	04/06/2006	Maurice O. Othieno	05-2572/LSI1P272	1398

TITLE OF INVENTION: SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	12/30/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
CRUZ, LESLIE PILAR	2826	257-691000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/399,723	04/06/2006	Maurice O. Othieno	05-2572/LSI1P272	1398

24319 7590 09/30/2009

LSI CORPORATION
1621 BARBER LANE
MS: D-105
MILPITAS, CA 95035

EXAMINER	
CRUZ, LESLIE PILAR	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/30/2009

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 433 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 433 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/399,723	OTHIENO ET AL.	
	Examiner	Art Unit	
	Leslie P. Cruz	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Amendment After Final filed on 01 July 2009*.

2. ☒ The allowed claim(s) is/are *3-16*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

The Advisory Action mailed on 23 July 2009 in response to the Amendment After Final filed on 01 July 2009 was sent in error. The Amendment After Final has been entered by the Examiner.

Allowable Subject Matter

Claims 3-16 are allowed over the prior art of record.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record taken either singly or in combination fails to anticipate or fairly suggest the limitations which the Applicant claims in claim 16 in a manner which would warrant a rejection under 35 U.S.C. § 102 or 35 U.S.C. § 103.

There was no prior art found by the examiner that suggested modification or combination with the cited prior art so as to satisfy the combination of the present independent claim 16; especially, the prior art does not provide a semiconductor integrated circuit (IC) which comprises: a fourth ground plane that is spatially separated and electrically isolated from the third ground plane and at least one reference plane associated with each layer of the substrate and the ground planes included thereon in combination with the remaining structure as recited in claim 16.

Telephone/Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leslie P. Cruz whose telephone number is 571-272-8599. The examiner can normally be reached on Monday-Friday 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LPC/
Examiner, Art Unit 2826

/Sue A. Purvis/
Supervisory Patent Examiner, Art Unit 2826

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S106	212	S104 and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/15 16:06
S105	35195	(low near2 speed) and (high near2 speed) and ground	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/15 16:06
S104	16024	(257/203-211,618,684,691,698,700,786, E23.079,E23.153).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/09/15 16:06
S108	36	S107 and S104	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/15 16:10
S107	4738	((low near2 speed) same ground) and ((high near2 speed) same ground)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/15 16:10
S109	33	S108 and (@pd<="20060406" or @ad<="20060406" or @rlad<="20060406")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/15 16:11
S110	33	S109 and (reference)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/15 16:30
S112	9	S109 and (reference near (plane wir$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/15 16:31

S111	30	S109 and (reference).detx.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/15 16:31
S113	7	"793756".ap.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/15 17:16
S114	8	"793576".ap.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/15 17:17
S115	3	S109 not S111	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/15 18:26
S117	163	S116 and (@pd<="20060406" or @ad<="20060406" or @rlad<="20060406")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/15 18:29
S116	179	S106 not S109	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/15 18:29
S118	6	"056535".ap.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 11:24
S126	212	S121 S125	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 12:00
S125	179	S121 not S124	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 12:00
S124	33	S123 and (@pd<="20060406" or @ad<="20060406" or @rlad<="20060406")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 12:00

S123	36	S122 and S119	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 12:00
S122	4738	((low near2 speed) same ground) and ((high near2 speed) same ground)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 12:00
S121	212	S119 and S120	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 12:00
S120	35195	(low near2 speed) and (high near2 speed) and ground	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 12:00
S119	16024	(257/203-211,618,684,691,698,700,786, E23.079,E23.153).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/09/16 12:00
S128	289	S119 and S127 and (@pd<="20060406" or @ad<="20060406" or @rlad<="20060406")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 12:01
S127	49378	(low near2 frequenc$3) and (high near2 frequenc$3) and ground	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 12:01
S129	266	S128 not S126	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 12:02
S130	4	("20040238939" | "20050173807").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 12:23
S131	16	(("6184477") or ("6777802") or ("6518663") or ("6495911") or ("7420286") or ("7279783") or ("20040183171") or ("20040238939")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/09/16 12:35

S135	992	S134 and (reference).detx.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 13:07
S134	1297	S133 and ground	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 13:07
S133	3811	S132 and (@pd<="20060406" or @ad<="20060406" or @rlad<="20060406")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 13:07
S132	4050	(257/698,700).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/09/16 13:07
S137	94	S134 and (low near2 (frequenc$3 speed)) and (high near2 (frequenc$3 speed)) and ground	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 13:08
S136	50614	S134 (low near2 frequenc$3) and (high near2 frequenc$3) and ground	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 13:08
S139	1	S137 not S138	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 13:09
S138	478	S128 S126	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 13:09

9/16/2009 1:27:03 PM
C:\Documents and Settings\lpcruz\My Documents\EAST\Workspaces\11399723.wsp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Othieno et al.	Attorney Docket No.: 05-2572/LSI1P272
Application No.: 11/399,723	Examiner: CRUZ, LESLIE PILAR
Filed: April 6, 2006	Group: 2826
Title: SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION	Confirmation No.: 1398

Okay to enter.
/LPC/
09/16/2009

CERTIFICATE OF EFS-WEB TRANSMISSION
I hereby certify that this correspondence is being transmitted electronically through EFS-WEB to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on July 1, 2009.

Signed: _____/Laura M. Dean/_____
Laura M. Dean

AMENDMENT B

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action dated May 27, 2009, please amend the above-identified patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begin on page 2 of this paper.
Remarks/Arguments begin on page 7 of this paper.

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L12	42	((low near (frequenc $3 speed)) and (high near (frequenc$3 speed)) and ground and (reference) and (semiconductor IC (integrated near circuit$2) chip die)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/16 13:24

9/16/2009 1:27:23 PM
C:\Documents and Settings\lpcruz\My Documents\EAST\Workspaces\11399723.wsp

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1398

SERIAL NUMBER	FILING or 371(c) DATE / RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/399,723	04/06/2006	257	2826	05-2572/LSI1P272

APPLICANTS

Maurice O. Othieno, Union City, CA;
Chok J. Chia, Cupertino, CA;
Amar J. Amin, Milpitas, CA;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
05/16/2006

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	☐ Yes ☐ No	/LESLIE PILAR CRUZ/ Examiner's Signature	☐ Initials	CA	4	25	2

ADDRESS

LSI CORPORATION
1621 BARBER LANE
MS: D-105
MILPITAS, CA 95035
UNITED STATES

TITLE

Semiconductor package and method using isolated Vss plane to accommodate high speed circuitry ground isolation

FILING FEE RECEIVED		
1470	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11399723	OTHIENO ET AL.
	Examiner	**Art Unit**
	Leslie P Cruz	2826

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
257	698	H 0 1 L 23 / 48 (2006.01.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	207	700	E23.079	E23.153	

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1														
	2														
5	3														
6	4														
2	5														
7	6														
8	7														
3	8														
4	9														
9	10														
10	11														
11	12														
12	13														
13	14														
14	15														
1	16														

/Leslie Pilar Cruz/ Examiner.Art Unit 2826 (Assistant Examiner)	09/16/2009 (Date)	**Total Claims Allowed:** 14	
/SUE PURVIS/ Supervisory Patent Examiner.Art Unit 2826 (Primary Examiner)	09/28/2009 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3, 6

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11399723	OTHIENO ET AL.
	Examiner	Art Unit
	Leslie P Cruz	2826

SEARCHED			
Class	Subclass	Date	Examiner
257		09/16/2009	lpc

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (See Search History)	09/16/2009	lpc

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
ALL		09/16/2009	lpc

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Othieno et al.	Attorney Docket No.: 05-2572/LSI1P272
Application No.: 11/399,723	Examiner: CRUZ, LESLIE PILAR
Filed: April 6, 2006	Group: 2826
Title: SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION	Confirmation No.: 1398

CERTIFICATE OF EFS-WEB TRANSMISSION
I hereby certify that this correspondence is being transmitted electronically through EFS-WEB to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on September 15, 2009.

Signed: _____/Laura M. Dean/_____
Laura M. Dean

APPLICANT'S STATEMENT OF SUBSTANCE OF INTERVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Examiner Cruz:

Thank you for your time spent during the brief Examiner Interview of September 15, 2009. During that Interview we discussed the allowance of Claim 16. It was clarified that the only amendment to Claim 16 was the correction of typographical errors. Moreover, the Applicant clarified that the amendments to all other pending claims were in the nature of making such claims dependent on Claim 16. The Examiner responded by indicating that she would do a quick search and then issue a notice of allowance.

As always, the Examiner is cordially invited to telephone the applicants representative to discuss any matters pertaining to this case. Should the Examiner wish to contact the undersigned for any reason, the telephone numbers set out below can be used.

Respectfully submitted,
BEYER LAW GROUP LLP

/Francis T. Kalinski II/
Francis T. Kalinski II
Reg. No. 44,177

P.O. Box 1687
Cupertino, CA 95015-1687
408-255-8001

Electronic Acknowledgement Receipt

EFS ID:	6078461
Application Number:	11399723
International Application Number:	
Confirmation Number:	1398
Title of Invention:	Semiconductor package and method using isolated Vss plane to accommodate high speed circuitry ground isolation
First Named Inventor/Applicant Name:	Maurice O. Othieno
Customer Number:	24319
Filer:	Francis Theodor Kalinski II/Laura Dean
Filer Authorized By:	Francis Theodor Kalinski II
Attorney Docket Number:	05-2572/LSI1P272
Receipt Date:	15-SEP-2009
Filing Date:	06-APR-2006
Time Stamp:	17:49:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant summary of interview with examiner	LSI1P272_Interview_Summ.pdf	21733 292e9d23a0a4ef8d0fa3790fcda7cec398036215	no	1

Warnings:	
Information:	

Total Files Size (in bytes):	21733

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Othieno et al.	Attorney Docket No.: 05-2572/LSI1P272
Application No.: 11/399,723	Examiner: CRUZ, LESLIE PILAR
Filed: April 6, 2006	Group: 2826
Title: SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION	Confirmation No.: 1398

CERTIFICATE OF EFS-WEB TRANSMISSION
I hereby certify that this correspondence is being transmitted electronically through EFS-WEB to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on July 1, 2009.

Signed: _____/Laura M. Dean/_____
Laura M. Dean

AMENDMENT B

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action dated May 27, 2009, please amend the above-identified patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begin on page 2 of this paper.
Remarks/Arguments begin on page 7 of this paper.

Do not enter.
/LPC/
07/20/2009

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/399,723	04/06/2006	Maurice O. Othieno	05-2572/LSI1P272	1398

24319 7590 07/23/2009

LSI CORPORATION
1621 BARBER LANE
MS: D-105
MILPITAS, CA 95035

EXAMINER	
CRUZ, LESLIE PILAR	
ART UNIT	**PAPER NUMBER**
2826	
MAIL DATE	**DELIVERY MODE**
07/23/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 11/399,723	**Applicant(s)** OTHIENO ET AL.	
	Examiner Leslie P. Cruz	**Art Unit** 2826	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 01 July 2009 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *See Continuation Sheet*. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: *16*.
   Claim(s) objected to: _____.
   Claim(s) rejected: *2-15, 26, 27, 29 and 30*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Sue A. Purvis/
Supervisory Patent Examiner, Art Unit 2826

Continuation of 3. NOTE: Applicant deleted the limitations "a plurality of electricaly connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate; a plurality of additional electrical connections that electrically conect the second ground plane with solder balls mounted on the second surface of the substrate; and peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package" from independent claim 16. The amendment broadens the scope of the claim and would require further search and/or consideration.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Othieno et al.	Attorney Docket No.: 05-2572/LSI1P272
Application No.: 11/399,723	Examiner: CRUZ, LESLIE PILAR
Filed: April 6, 2006	Group: 2826
Title: SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION	Confirmation No.: 1398

CERTIFICATE OF EFS-WEB TRANSMISSION
I hereby certify that this correspondence is being transmitted electronically through EFS-WEB to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on July 1, 2009.

Signed: _____/Laura M. Dean/_____
Laura M. Dean

AMENDMENT B

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action dated May 27, 2009, please amend the above-identified patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begin on page 2 of this paper.
Remarks/Arguments begin on page 7 of this paper.

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-2 (Cancelled)

Claim 3: (Currently Amended) An IC package as recited in Claim **16** **[[2]]** wherein the low speed electronic circuitry is defined as circuitry having serial transfer rates of less than about 1 Gigabits per second (Gb/s); and

wherein the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 1 Gb/s.

Claim 4: (Currently Amended) An IC package as recited in Claim **16** **[[2]]** wherein the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 8.5 Gb/s.

Claim 5: (Currently Amended) An IC package as recited in Claim **16** **[[2]]** wherein **the peripheral electrical contacts include,**

a first set of electrical contacts for electrical connection with low speed electronic circuitry; and

a second set of electrical contacts for electrical connection with high speed electronic circuitry; and

wherein the second set of electrical contacts are spaced apart at a distance that is at least twice as far apart as the spacing for the first set of electrical contacts.

Claim 6: (Currently Amended) An IC package as recited in Claim **16** **[[2]]** wherein **the peripheral electrical contacts include,**

a first set of electrical contacts for electrical connection with low speed electronic circuitry; and

a second set of electrical contacts for electrical connection with high speed electronic circuitry; and

wherein the second set of electrical contacts are spaced apart at a distance that is at least three times as far apart as the spacing for the first set of electrical contacts.

Claim 7: **(Currently Amended)** An IC package as recited in Claim **16** **[[2]]** wherein **the peripheral electrical contacts include,**

a first set of electrical contacts for electrical connection with low speed electronic circuitry; and

a second set of electrical contacts for electrical connection with high speed electronic circuitry; and

wherein the second set of electrical contacts are spaced apart at a distance sufficient to establish a differential impedance of at least 100 ohms (Ω) between the contacts of the second set.

Claim 8: (Original) An IC package as recited in Claim 5 wherein the first set of electrical contacts are spaced apart a distance of at least 70 μm (micrometers) and wherein the second set of electrical are spaced apart a distance of at least 140 μm (micrometers).

Claim 9: (Original) An IC package as recited in Claim 5 wherein the first set of electrical contacts are spaced apart a distance of at least 70 μm (micrometers) and wherein the second set of electrical are spaced apart a distance of at least 200 μm (micrometers).

Claim 10: **(Currently Amended)** An IC package as recited in Claim **16** **[[2]]** wherein **the peripheral electrical contacts include,**

a first set of electrical contacts for electrical connection with low speed electronic circuitry; and

a second set of electrical contacts for electrical connection with high speed electronic circuitry; and

wherein the electrical contacts are arranged such that,

the first spacing between the contacts of the first set of electrical contacts is smaller than **a** **[[the]]** second spacing between the contacts of the second set of electrical contacts, thereby enabling greater contact density for the first set of electrical contacts.

Claim 11: **(Currently Amended)** An IC package as recited in Claim **16** **[[2]]** wherein **the peripheral electrical contacts include,**

a first set of electrical contacts for electrical connection with low speed electronic circuitry; and

a second set of electrical contacts for electrical connection with high speed electronic circuitry; and

wherein the electrical contacts are arranged as part of I/O lines such that,

a [[the]] first spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance of at least 50 Ω between the contacts of the first set of electrical contacts to substantially eliminate cross-talk between I/O lines for the low speed electronic circuitry; and

a [[the]] second spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100 Ω between the contacts of the second set of electrical contacts to substantially eliminate cross-talk between I/O lines for the high speed electronic circuitry.

Claim 12: **(Currently Amended)** An IC package as recited in Claim **16 [[2]]** wherein **the peripheral electrical contacts include,**

a first set of electrical contacts for electrical connection with low speed electronic circuitry; and

a second set of electrical contacts for electrical connection with high speed electronic circuitry; and

wherein the electrical contacts are arranged such that,

a [[the]] first spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance of at least 50 Ω between the contacts of the first set of electrical contacts; and

a [[the]] second spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100 Ω between the contacts of the second set of electrical contacts.

Claim 13: **(Currently Amended)** An IC package as recited in Claim **16 [[2]]** wherein the **first surface includes a** die attachment surface **with [[has]]** a die arrangement attached thereto,

the die arrangement being electrically connected to the first ground plane, the second ground plane, and the peripheral electrical contacts of the substrate.

Claim 14: **(Currently Amended)** An IC package as recited in Claim 13 wherein the die arrangement comprises a die having both high-speed electronic circuitry and low-speed electronic circuitry; **and**

wherein the peripheral electrical contacts include,

a first set of electrical contacts for electrical connection with low speed electronic circuitry; and

a second set of electrical contacts for electrical connection with high speed electronic circuitry; and

wherein the low-speed electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced for connection with the low speed electronic circuitry; and

wherein the high-speed electronic circuitry is connected with the second ground plane and is electrically connected with the second set of electrical contacts that are spaced for connection with the high speed electronic circuitry.

Claim 15: **(Previously Presented)** An IC package as recited in Claim 14 wherein the die arrangement comprises a stacked die arrangement wherein at least one die has high-speed electronic circuitry and wherein at least one die has low-speed electronic circuitry;

wherein the low-speed electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced for connection with the low speed electronic circuitry; and

wherein the high-speed electronic circuitry is connected with the second ground plane and is electrically connected with the second set of electrical contacts that are spaced for connection with the high speed electronic circuitry.

Claim 16: **(Currently Amended)** A semiconductor integrated circuit (IC) package which comprises:

a substrate having a first surface and a second surface wherein;

a first layer of the substrate includes,

a first ground plane enabling electrical connection with low speed electronic circuitry, and

a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection with high speed electronic circuitry;

a second layer of the substrate includes,

a third ground plane configured for electrical connection with low speed electronic circuitry, and

a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the third ground plane configured for electrical connection with high speed electronic circuitry;

a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate;

a plurality of additional electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate; and

peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package; and

at least one reference plane associated with each layer of the substrate and the ground planes included thereon.

~~**a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate;**~~

~~**a plurality of additional electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate; and**~~

~~**peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package.**~~

Claims 17-30 (Cancelled).

REMARKS/ARGUMENTS

The applicants thank the Examiner and appreciate the thought and effort put into the Office Action mailed May 27, 2009.

All pending Claims save **Claim 16** are rejected**.**

In this Amendment, **Claim 16 is amended** to remove some redundant and typographical errors. No change in claim scope is engendered by these superficial changes. Additionally, the Applicants specifically point out that no changes are made to Claim 16 in response to the cited art. The Applicants respectfully submit that **Claim 16** is in condition for allowance.

Moreover, **Claims 3-7 and 10-14 have been amended** and are discussed further herein. Also, **Claims 2, 26, 27, 29, and 30 are cancelled**.

Consequently, **Claims 3-16** are now pending in the application. Reconsideration and allowance are hereby requested.

Conclusion:

In view of the foregoing amendments and remarks, it is respectfully submitted that the claimed invention as presently presented is patentable over the art of record and that this case is now in condition for allowance.

Accordingly, the applicants request withdrawal of all pending rejections and request reconsideration of the pending application and prompt passage to issuance. As an aside, the applicants clarify that any lack of response to any of the issues raised by the Examiner is not an admission by the applicant as to the accuracy of the Examiner's assertions with respect to such issues. Accordingly, applicant's specifically reserve the right to respond to such issues at a later time during the prosecution of the present application, should such a need arise.

As always, the Examiner is cordially invited to telephone the applicants representative to discuss any matters pertaining to this case. Should the Examiner wish to contact the undersigned for any reason, the telephone numbers set out below can be used.

Additionally, if any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 12-2252 (Order No. 05-2572).

Respectfully submitted,
BEYER LAW GROUP LLP

/Francis T. Kalinski II/
Francis T. Kalinski II
Reg. No. 44,177

P.O. Box 1687
Cupertino, CA 95015-1687
408-255-8001

Electronic Acknowledgement Receipt

EFS ID:	5628040
Application Number:	11399723
International Application Number:	
Confirmation Number:	1398
Title of Invention:	Semiconductor package and method using isolated Vss plane to accommodate high speed circuitry ground isolation
First Named Inventor/Applicant Name:	Maurice O. Othieno
Customer Number:	24319
Filer:	Francis Theodor Kalinski II/Laura Dean
Filer Authorized By:	Francis Theodor Kalinski II
Attorney Docket Number:	05-2572/LSI1P272
Receipt Date:	01-JUL-2009
Filing Date:	06-APR-2006
Time Stamp:	18:03:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	Amendment_B_Transmittal.pdf	22484 bc7f200bb335005aad53acad7cbd7185a539f320	no	1

Warnings:	
Information:	

2		LSI1P272_Amdt_B.pdf	52416 e7222eadaae8e7c53e2d382c8d4b1d9fcb439ecf	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment After Final	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	8

Warnings:	
Information:	
Total Files Size (in bytes):	74900

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Othieno et al.	Attorney Docket No.: 05-2572/LSI1P272
Application No.: 11/399,723	Examiner: CRUZ, LESLIE PILAR
Filed: April 6, 2006	Group: 2826
Title: SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION	Confirmation No.: 1398

CERTIFICATE OF EFS-WEB TRANSMISSION
I hereby certify that this correspondence is being transmitted electronically through EFS-WEB to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on July 1, 2009.

Signed: _____/Laura M. Dean/_____
Laura M. Dean

AMENDMENT B TRANSMITTAL

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is an Amendment in the above-identified application.

The fee has been calculated as shown below.

	Claims After Amendment		Highest Previously Paid For	Present Extra	Small Entity Rate Fee	Large Entity Rate Fee
Total Claims	14	MINUS	25	0	x 26 = 0	x 52 = 0
Independent Claims	1	MINUS	4	0	x 110 = 0	x 220 = 0
Multiple Dependent Claim Present and Fee Not Previously Paid						
				Total	$0	$0

☒ Applicant(s) believe that no (additional) Extension of Time is required; however, if it is determined that such an extension is required, Applicant(s) hereby petition that such an extension be granted and authorize the Commissioner to charge the required fees for an Extension of Time under 37 CFR 1.136 to Deposit Account No. 12-2252 (Order No. 05 2572).

☒ Please charge the required fees, or any additional fees required to facilitate filing the enclosed response, to Deposit Account No. 12-2252 (Order No. 05 2572).

Respectfully submitted,
BEYER LAW GROUP LLP

/Francis T. Kalinski II/
Francis T. Kalinski II
Reg. No. 44,177

P.O. Box 1687
Cupertino, CA 95015-1687

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/399,723	04/06/2006	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	07/01/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 14	Minus	** 25	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***4	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/VICTORIA BROWN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/399,723	04/06/2006	Maurice O. Othieno	05-2572/LSI1P272	1398

24319 7590 05/27/2009

LSI CORPORATION
1621 BARBER LANE
MS: D-105
MILPITAS, CA 95035

EXAMINER	
CRUZ, LESLIE PILAR	
ART UNIT	**PAPER NUMBER**
2826	
MAIL DATE	**DELIVERY MODE**
05/27/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/399,723	OTHIENO ET AL.	
	Examiner	Art Unit	
	Leslie P. Cruz	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-16 and 26-30* is/are pending in the application.

4a) Of the above claim(s) *28* is/are withdrawn from consideration.

5)☒ Claim(s) *16* is/are allowed.

6)☒ Claim(s) *2-15,26,27,29 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

New claim 28 is withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 08/29/2008.

Drawings

The drawings were received on 02/19/2009. These drawings are acceptable.

Claim Objections

Claim 2 is objected to because of the following informalities: lines 12-13 recite the limitation "a plurality of additional electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate; and". Lines 14-15 repeats the limitation recited in lines 12-13. Appropriate correction is required.

Claim 26 is objected to because of the following informalities: lines 4-5 recite "the first system arranged for connection with a with speed ground plane". Did Applicant mean "the first system arranged for connection with a high speed ground plane"? Appropriate correction is required.

Functional Language (MPEP § 2114)

APPARATUS CLAIMS MUST BE STRUCTUR-ALLY DISTINGUISHABLE FROM THE PRIOR ART

>While features of an apparatus may be recited either structurally or functionally, claims< directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >*In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< *In re Danly,* 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device *is*, not what a device *does*." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).

MANNER OF OPERATING THE DEVICE DOES NOT DIFFERENTIATE APPRATUS CLAIM FROM THE PRIOR ART

A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987) (The preamble of claim 1 recited that the apparatus was "for mixing flowing developer material" and the body of the claim recited "means for mixing ..., said mixing means being stationary and

completely submerged in the developer material". The claim was rejected over a reference which taught all the structural limitations of the claim for the intended use of mixing flowing developer. However, the mixer was only partially submerged in the developer material. The Board held that the amount of submersion is immaterial to the structure of the mixer and thus the claim was properly rejected.).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-14, 26, 27, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (US 2004/0238939 A1).

With respect to claim 2, Wu (Figs. 3, 9a-13) discloses a semiconductor integrated circuit (IC) package which comprises: a substrate [914, 916] having a first surface [928] and a second surface [936]; a die attachment surface [directly below die 10] formed on the first surface; a first ground plane [R21, paragraph 0105] for electrical connection with a first electronic circuitry [paragraph 0095]; a plurality of electrical connections [1014] that electrically connect the first ground plane with solder balls [1020, paragraph 0112] mounted on the second surface of the substrate; a second ground plane [R11, paragraph 0106] that is spatially separated and electrically isolated from the first ground plane, the second ground plane for electrical connection with a second electronic

circuitry [paragraph 0095]; a plurality of additional electrical connections [1206] that electrically connect the second ground plane with solder balls [954, paragraph 0119] mounted on the second surface of the substrate; and peripheral electrical contact [954] arranged on the substrate and configured for connection with electronic circuitry external to the package [paragraph 0117], wherein the peripheral electrical contacts comprise: a first set of electrical contacts [954, paragraph 0112] for electrical connection with the first electronic circuitry and the contacts are arranged at a first spaced apart distance; and a second set of electrical contacts [954, paragraph 0106] for electrical connection with the second electronic circuitry and the contacts are arranged at a second spaced apart distance.

Wu does not specify the first electronic circuitry is low speed electronic circuitry or the second high speed electronic circuitry is high speed electronic circuitry. Wu also does not specify the first set of electrical contacts is for electrical connection with low speed electronic circuitry and configured to pass low bit rate electronic signals wherein the configuration is sufficient to establish a control differential impedance between the contacts effective to substantially eliminate cross-talk between the first set of contacts during cross-talk between the first set of contacts during operation with the low speed electronic circuitry or the second set of electrical contacts for electrical connection with high speed electronic circuitry and configured to pass high bit rate electronic signals wherein the configuration is sufficient to establish a control differential impedance between the contacts effective to substantially eliminate cross-talk between the second set of contacts during operation with the high speed electronic circuitry

However, the claimed apparatus must be distinguished from the prior art in terms of structure rather than function and a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus. Applicant's claim 2 does not distinguish over the Wu reference regardless of the above functional language recited in the claim.

Note Functional Language *(MPEP § 2114)* section above.

With respect to claim 3, Wu discloses an IC package as recited in claim 2. Wu does not specify the first electronic circuitry is defined as circuitry having serial transfer rates of less than about 1 Gigabits per second (Gb/s); and the second electronic circuitry is defined as circuitry having serial transfer rates of greater than about 1 Gb/s.

Note that a recitation of the functional language such as "the low speed electronic circuitry is defined as circuitry having serial transfer rates of less than about 1 Gigabits per second (Gb/s); and wherein the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 1 Gb/s" of the claimed apparatus must be distinguished from the prior art in terms of structure rather than function and a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus. Applicant's claim 3 does not distinguish over the Wu reference regardless of the above functional language recited in the claim.

Note Functional Language *(MPEP § 2114)* section above.

With respect to claim 4, Wu discloses an IC package as recited in claim 2. Wu does not specify the second electronic circuitry is defined as circuitry having serial transfer rates of greater than about 8.5 Gb/s.

Note that a recitation of the functional language use such as "the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 8.5 Gb/s" of the claimed apparatus must be distinguished from the prior art in terms of structure rather than function and a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus. Applicant's claim 4 does not distinguish over the Wu reference regardless of the above functional language recited in the claim.

Note Functional Language *(MPEP § 2114)* section above.

With respect to claims 5-7 and 10, Wu discloses an IC package as recited in claim 2. Wu discloses first set of electrical contacts and second set of electrical contacts may be arranged in order to improve layout flexibility and minimizing package footprint while retaining high levels of system function performance [paragraphs 0032-0044, 0124]. Inner and outer ring segments designated by counting indices (R1j, R2k) of the R1 group and the R2 group are defined by respective annular segment lengths (L1j, L2k) and orthogonal widths (W1j, W2k). The segments (R1j, R2k) are spaced orthogonal from peripheral edges defined by nearest adjacent chip, package or isolated interconnecting routing traces by corresponding proximal (inward directed) and distal (outward directed) spacing distances (Wpj, Wpk, Wdj, Wdk) where (p) indicates a proximal spacing, (d) indicates a distal spacing distance, and (j, k) are the counting

integers designating the jth segment of inner R1 set and the kth segment of the outer R2 set [paragraph 0096]. Wu [paragraph 0097] also discloses the first set of vias [930] provide electrical connection from selected bumps [954] through both layers [914, 916] to selected top layer via pads [960] patterned in the conductive layer [926] at the opposite (top) side [928] of layer [914]. Wu further discloses flexibility is provided for easing the burden of distributing multiple power supply voltages and multiple ground paths for decoupling noise-producing circuits from noise sensitive circuits by the segmented rings of the annular R1 group and the annular R2 group [paragraph [0105]. Therefore, the specific claimed relative spaced apart distance between the second set of electrical contacts and the first set of electrical contacts, absent any criticality, are only considered to be the "optimum" distances that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired adhesive strength, manufacturing costs, etc. (see Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, *i.e.*, results which are different in kind and not in degree from the results of the prior art, will be obtained.

Accordingly, since the applicants have not established the criticality (see next paragraph below) of the stated relative distance, it would have been obvious to one of ordinary skill in the art to use these values in the device of Wu

The specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a

claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to claims 8, 9, Wu discloses an IC package as recited in claim 5. Wu discloses first set of electrical contacts and second set of electrical contacts may be arranged in order to improve layout flexibility and minimizing package footprint while retaining high levels of system function performance [paragraphs 0032-0044, 0124]. The specific claimed relative spaced apart distance between the second set of electrical contacts and the first set of electrical contacts, absent any criticality, are only considered to be the "optimum" distances that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired adhesive strength, manufacturing costs, etc. (see Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, *i.e.*, results which are different in kind and not in degree from the results of the prior art, will be obtained.

Accordingly, since the applicants have not established the criticality (see next paragraph below) of the stated relative distance, it would have been obvious to one of ordinary skill in the art to use these values in the device of Wu

The specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to claims 11 and 12, Wu discloses the IC package as recited in claim 2. Wu discloses the electrical contacts are arranges as part of I/O lines [paragraph 0117]. Wu discloses first set of electrical contacts and second set of electrical contacts may be arranged in order to improve layout flexibility and minimizing package footprint while retaining high levels of system function performance [paragraphs 0032-0044, 0124]. The specific claimed relative spaced apart distance between the second set of electrical contacts and the first set of electrical contacts, absent any criticality, are only considered to be the "optimum" distances that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired adhesive strength, manufacturing costs, etc. (see Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, *i.e.*, results which are different in kind and not in degree from the results of the prior art, will be obtained.

Accordingly, since the applicants have not established the criticality (see next paragraph below) of the stated relative distance, it would have been obvious to one of ordinary skill in the art to use these values in the device of Wu

The specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to claim 13, Wu discloses an IC package as recited in claim 2. Wu (Figs. 3, 9-13) further discloses the die attachment surface has a die [10, paragraph 0094] arrangement attached thereto, the die arrangement being electrically connected to the first ground plane, the second ground plane, and the peripheral electrical contacts of the substrate.

With respect to claim 14, Wu discloses an IC package as recited in claim 13. Wu further discloses the die arrangement comprises a die [paragraph 0094] having both a second electronic circuitry and a first electronic circuitry; wherein a first electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced for connection with the electronic circuitry; and wherein the second electronic circuitry is connected with the second ground plane and is electrically connected with the second set of electrical contacts that are spaced for connection the second speed electronic circuitry. Wu discloses two power ring segments may be used for separate ground return bonding locations for separate ground nets for two separate power nets disposed on a multi-power IC chip mounted in the package [paragraph 0083]. Wu does not specify that first electronic circuitry is a low-speed electronic circuitry; and wherein the second electronic circuitry is high-speed electronic circuitry.

Note that a recitation of the function/intended use such as “high-speed circuitry and low-speed circuitry” of the claimed apparatus must be distinguished from the prior art in terms of structure rather than function and a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the

claimed apparatus from a prior art apparatus. Applicant's claim 14 does not distinguish over the Wu reference regardless of the above functional language recited in the claim.

Note Functional Language *(MPEP § 2114)* section above.

With respect to claim 26, so far as understood, Wu (Figs. 3, 9a-13) discloses a semiconductor operating configuration comprising: a mother board [PC board, paragraph 0094] having two ground systems including a first ground system [paragraph 0112] arranged for connection with a first ground plane [R21, paragraph 0105] of an IC (integrated circuit) package [900] and a second ground system [paragraph 0117] electrically isolated from the first system arranged for connection with a with a second ground plane [R11, paragraph 0106] of the IC chip [10]; an integrated circuit (IC) package mounted on the mother board and configured to comprise both second and first speed electronic circuitry, the IC comprises: a substrate [914, 916]having a first surface [928] and a second surface [936] with an integrated circuit die construction mounted on the substrate, the die construction including both second and first electronic circuitry; a first ground plane [R21, paragraph 0105] electrically connected with the first electronic circuitry of the IC and also electrically connected with first ground system of the motherboard; a plurality of electrical connections [1018] that electrically connect the first ground plane with solder balls [1020] mounted on the second surface of the substrate; a second ground plane [R11, paragraph 0106] that is spatially separated and electrically isolated from the first ground plane, the second ground plane connected with the second electronic circuitry of the IC and also electrically connected with second ground system of the motherboard; a plurality of additional electrical connections [1110,

1116] that electrically connect the second ground plane with solder balls [954] mounted on the second surface of the substrate; and peripheral electrical contacts [926] arranged on the substrate and configured for connection with electronic circuitry of the motherboard. Wu does not specify the first and second electronic circuitry is a low and high speed electronic circuitry, respectively.

However, the claimed apparatus must be distinguished from the prior art in terms of structure rather than function and a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus. Applicant's claim 27 does not distinguish over the Wu reference regardless of the above functional language recited in the claim.

Note Functional Language *(MPEP § 2114)* section above.

With respect to claim 27, Wu (Figs. 3, 9a-13) A semiconductor integrated circuit package, the package comprising: a substrate [914, 916] having a first surface [928] and a second surface [936] with an integrated circuit die [10] construction mounted on the substrate, the die construction including both a first and second electronic circuitry [paragraph 0095]; a first ground plane [R21, paragraph 0105] electrically connected with the first electronic circuitry of the integrated circuit die construction and also arranged for electrical connection with a first ground system external to the package [paragraph 0112]; a first plurality of electrical connections [1012, 1014] that electrically connect the first electronic circuitry of the integrated circuit die construction with the first ground plane; a third plurality of electrical connections [1018] that electrically connect the first ground plane with solder balls [1020] mounted on the second surface of the substrate; a

second ground plane [R11, paragraph 0106] that is spatially separated and electrically isolated from the first ground plane, the second ground plane connected with the second electronic circuitry of the integrated circuit die construction and also arranged for electrical connection with a second ground system external to the package [paragraph 0117] wherein said second ground system is electrically isolated from said first ground system; a second plurality of electrical connections [bonding wire received by R11 from chip bond pads 1202, 1204] that electrically connect the second electronic circuitry of the integrated circuit die construction with the second ground plane; a fourth plurality of electrical connections [1110, 1116] that electrically connect the second ground plane with solder balls [954] mounted on the second surface of the substrate; peripheral electrical contacts [926] arranged on the substrate and configured for connection with the second electronic circuitry and the first electronic circuitry and further configured for electrical connection to circuitry external to the package [paragraph 0094]. Wu does not specify the first and second electronic circuitry is a low and high speed electronic circuitry, respectively.

However, the claimed apparatus must be distinguished from the prior art in terms of structure rather than function and a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus. Applicant's claim 27 does not distinguish over the Wu reference regardless of the above functional language recited in the claim.

Note Functional Language *(MPEP § 2114)* section above.

With respect to claim 29, Wu discloses the semiconductor integrated circuit package as recited in Claim 27. Wu (Figs. 9a-13) discloses the peripheral electrical contacts include a first set of peripheral contacts [926, connected to R21] is in a spaced apart arrangement; and wherein the peripheral electrical contacts further include a second set of peripheral contacts [926, connected to R11] is in a spaced apart arrangement. Wu does not specify such that the spacing between the contacts of the first set of peripheral contacts is sufficient to substantially eliminate cross-talk between the contacts of the first set of contacts when low speed electronic signals are passed through the contacts; and such that the spacing between the contacts of the second set of peripheral contacts is sufficient to substantially eliminate cross-talk between the contacts of the second set of contacts when high speed electronic signals are passed through the contacts

However, the claimed apparatus must be distinguished from the prior art in terms of structure rather than function and a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus. Applicant's claim 29 does not distinguish over the Wu reference regardless of the above functional language recited in the claim.

With respect to claim 30, Wu discloses the semiconductor integrated circuit package as recited in Claim 29. Wu (Figs. 9a-13) further discloses the first set of peripheral contacts is electrically coupled with the first electronic circuitry of the integrated circuit die construction; and wherein the second set of peripheral contacts is

electrically coupled with the second electronic circuitry of the integrated circuit die construction.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu in view of Zhu et al. (US 2005/0173807 A1).

With respect to claim 15, Wu discloses an IC package as recited in claim 14. Wu does not specify the die arrangement comprises a stacked die arrangement wherein at least one die has high-speed electronic circuitry and wherein at least one die has low-speed electronic circuitry.

Zhu et al. (Fig. 4) teaches it is well known in the art for a die arrangement to comprise a stacked die arrangement [401, 403]. Zhu et al. teaches it is beneficial for a die arrangement to comprise a stacked die arrangement in order to increase device density within the footprint of a single die package [paragraph 0012].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the die arrangement of Wu to comprise a stacked die arrangement, such as taught by Zhu et al., in order to increase device density within the footprint of a single die package.

Zhu et al. does not specify at least one die has high-speed electronic circuitry and wherein at least one die has low-speed electronic circuitry.

Note that a recitation of the function/intended use such as “high-speed electronic circuitry and low-speed electronic circuitry” of the claimed apparatus must be distinguished from the prior art in terms of structure rather than function and a recitation with respect to the manner in which a claimed apparatus is intended to be employed

does not differentiate the claimed apparatus from a prior art apparatus. Applicant's claim 15 does not distinguish over the Wu reference regardless of the above functional language recited in the claim.

Note Functional Language *(MPEP § 2114)* section above.

Allowable Subject Matter

Claim 16 is allowed over the prior art of record.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record taken either singly or in combination fails to anticipate or fairly suggest the limitations which the Applicant claims in claim 16 in a manner which would warrant a rejection under 35 U.S.C. § 102 or 35 U.S.C. § 103.

There was no prior art found by the examiner that suggested modification or combination with the cited prior art so as to satisfy the combination of the present independent claim 16; especially, the prior art does not provide a semiconductor integrated circuit (IC) which comprises: a fourth ground plane that is spatially separated and electrically isolated from the third ground plane in combination with at least one reference plane associated with each layer of the substrate and the ground planes included thereon as recited in claim 16.

Response to Arguments

Applicant's arguments filed 02/19/2009 have been fully considered but they are not persuasive.

Applicant argues the invention comprises two ground planes, each dedicated to circuit structures operating at different rates and that the cited art does not teach of suggest these critical limitations. However, Wu discloses in paragraph 0083 that two of the power ring segments may "be used for separate ground return bonding locations for separate ground nets (i.e. non -shared ground, not shown) for two separate power nets disposed on a multi-power IC chip mounted in the package 300". Wu further discloses such separate ground returns "can be useful in applications needing high isolation between noisy digital or RF functions, and highly sensitive analog functions, e.g. low noise, broad-band amplifiers and the like".

Applicant further argues the spacing described (is a structural space relationship) is a spacing that improves cross-talk performance between the contacts and that low speed contacts can be spaced more tightly than is the case for high speed contacts which are generally more affected by high frequency cross talk problems. However, it is well known in the art for variables such as speeds, numbers of signals, the timing of the signals, dielectric constants of dielectric layer isolating contacts, etc., are used to adjust the desired impedances/reduce cross-talk performance between the contacts. Applicant did not show that the particular spacing is critical by showing that the claimed spacing achieves unexpected results relative to the prior art range.

"The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results.

Therefore, claims 2-15, 26, 27, 29 and 30 are not patentably distinguishable over the prior art of record.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Telephone/Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leslie P. Cruz whose telephone number is 571-272-8599. The examiner can normally be reached on Monday-Friday 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LPC/
Examiner, Art Unit 2826

/Sue A. Purvis/
Supervisory Patent Examiner, Art Unit 2826

Notice of References Cited	Application/Control No. 11/399,723	Applicant(s)/Patent Under Reexamination OTHIENO ET AL.	
	Examiner Leslie P. Cruz	Art Unit 2826	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2004/0238939 A1	12-2004	Wu, Ping	257/691
*	B	US-2005/0173807 A1	08-2005	Zhu et al.	257/777
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11399723	OTHIENO ET AL.
	Examiner	Art Unit
	Leslie P Cruz	2826

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/06/2008	12/20/2008	05/22/2009						
	1	÷	✓	-						
	2	÷	✓	✓						
	3	÷	✓	✓						
	4	÷	✓	✓						
	5	÷	✓	✓						
	6	÷	✓	✓						
	7	÷	✓	✓						
	8	÷	✓	✓						
	9	÷	✓	✓						
	10	÷	✓	✓						
	11	÷	✓	✓						
	12	÷	✓	✓						
	13	÷	✓	✓						
	14	÷	✓	✓						
	15	÷	✓	✓						
	16	÷	✓	=						
	17	÷	N	-						
	18	÷	N	-						
	19	÷	N	-						
	20	÷	N	-						
	21	÷	N	-						
	22	÷	N	-						
	23	÷	N	-						
	24	÷	N	-						
	25	÷	N	-						
	26			✓						
	27			✓						
	28			N						
	29			✓						
	30			✓						

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11399723	OTHIENO ET AL.
	Examiner	Art Unit
	Leslie P Cruz	2826

SEARCHED			
Class	Subclass	Date	Examiner
257	618, 684, 698,700	05/11/2009	lpc

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (See Search History)	05/11/2009	lpc

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S71	5489	(257/684,698,700,618).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/05/11 00:57
S72	57	S71 and (high near speed) and (low near speed)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/11 00:58
S74	697	S73 not S72	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/11 01:36
S73	705	S71 and ring	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/11 01:36
S75	5489	(257/684,698,700,618).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/05/11 13:01
S76	205	S75 and power and ground and (EMI crosstalk$3 cross-talk)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/11 13:02
S77	26	S75 and (power with (pitch$2 spac$3)) and (ground with (pitch $2 spac$3))and (EMI crosstalk$3 cross-talk)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/11 13:08
S78	26	S75 and (power with (pitch$2 spac$3)) and (ground with (pitch $2 spac$3)) and (EMI crosstalk$3 cross-talk)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/11 13:09

S79	7	S75 and ((power with (pitch$2 spac$3)) same speed) and ((ground with (pitch$2 spac$3)) same speed)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/11 14:29
S80	2	"20060012054".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/15 11:43
S82	9	("20020050402" | "20030094685" | "20040183171" | "20060012054" | "4016463" | "5095407" | "5834705" | "6348400" | "6459161").PN. OR ("7279798").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/15 11:45
S81	1	("2006/0012054").URPN.	USPAT	OR	ON	2009/05/15 11:45
S83	1	("2004/0183171").URPN.	USPAT	OR	ON	2009/05/15 13:02
S85	18	("5449948" | "5639989" | "5719750" | "5973910" | "5977631" | "6027980" | "6118482" | "6157016" | "6159031" | "6215165" | "6222246" | "6235549" | "6243134" | "6259145" | "6677781" | "6680533").PN. OR ("6806569").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/15 13:03
S84	4	"964811".ap.	USPAT	OR	ON	2009/05/15 13:03
S87	705	257/691.ccls. and (low$3 same high$3)	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/15 15:50
S86	1231	257/691.ccls. and (low high)	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/15 15:50
S88	95	S87 and (ground with isolat$)	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/15 16:08
S89	4	("5714801" | "6184477" | "6586828").PN. OR ("6744130").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/15 16:30
S90	2	("20040207077").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/05/15 17:07

S91	610	S87 not S88	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/15 17:21
S93	18	("5449948" | "5639989" | "5719750" | "5973910" | "5977631" | "6027980" | "6118482" | "6157016" | "6159031" | "6215165" | "6222246" | "6235549" | "6243134" | "6259145" | "6677781" | "6680533").PN. OR ("6806569").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/18 14:01
S92	6	"964811".ap.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/18 14:01
S97	2	S96 and S94	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/18 14:22
S96	5492	(257/684,698,700,618).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/05/18 14:22
S95	0	"L71" and S94	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/18 14:22
S94	191	(motherboard (mother near board)) same (ground with (isolat$3 separat$3))	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/18 14:22
S98	31	S94 and "257"/$.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/18 14:33
L6	1	L3 and ((high with frequenc$3) same (low with frequenc$3) same spac$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/22 14:41
L5	31	L3 and ((high with frequenc$3) same (low with frequenc$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/22 14:41
L4	83	L3 and (high same low)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/22 14:41

L3	120	(US-20070235849-$ or US-20040173822-$ or US-20080075070-$ or US-20060197718-$ or US-20060091507-$ or US-20040201085-$ or US-20070170575-$ or US-20040056344-$ or US-20060237726-$ or US-20040026794-$ or US-20070040284-$ or US-20070241465-$ or US-20040212103-$ or US-20060226447-$ or US-20070170587-$ or US-20080113499-$ or US-20080116988-$ or US-20030025208-$ or US-20060012745-$ or US-20030007442-$ or US-20050281528-$ or US-20030123818-$ or US-20060035510-$ or US-20080088007-$ or US-20060055022-$ or US-20050207131-$).did. or (US-20050051887-$ or US-20040238939-$ or US-20080203562-$ or US-20070090401-$ or US-20050248040-$ or US-20030193078-$ or US-20050127492-$ or US-20040207067-$ or US-20050173807-$ or US-20020003304-$ or US-20030098177-$ or US-20040173880-$ or US-20070102806-$ or US-20080017971-$ or US-20080150123-$ or US-20010004129-$ or US-20060012054-$ or US-20040183171-$ or US-20030052402-$ or US-20040207077-$ or US-20010054760-$).did. or (US-7448132-$ or US-7358555-$ or US-5912809-$ or US-5373187-$ or US-7439449-$ or US-7193311-$ or US-4827327-$ or US-6870273-$ or US-7414322-$ or US-6867668-$ or US-6797891-$ or US-4835120-$ or US-4725878-$ or US-7239527-$ or US-6919226-$ or US-6979897-$ or US-6707164-$ or US-6040524-$ or US-6677831-$ or US-7321166-$ or US-7279783-$ or US-	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2009/05/22 14:41

		7209366-$ or US-7129574-$ or US-7129571-$ or US-7112880-$ or US-6998719-$).did. or (US-6770963-$ or US-6707684-$ or US-6566761-$ or US-6495911-$ or US-7307293-$ or US-7015574-$ or US-6518663-$ or US-6472737-$ or US-6396136-$ or US-5808357-$ or US-5686764-$ or US-7420276-$ or US-7202546-$ or US-6777802-$ or US-6727597-$ or US-7372170-$ or US-7279798-$ or US-7227254-$ or US-6897555-$ or US-7075179-$ or US-7420286-$ or US-6534879-$ or US-6424032-$ or US-6153924-$ or US-4875087-$ or US-4879588-$ or US-6239485-$).did. or (US-6310398-$ or US-5272600-$ or US-5854534-$ or US-6246112-$ or US-6806569-$ or US-6677781-$ or US-6933613-$ or US-7221046-$ or US-6025616-$ or US-6181004-$ or US-6744130-$ or US-6184477-$ or US-6586828-$ or US-7062742-$ or US-6921975-$ or US-6291879-$ or US-6707685-$ or US-6377464-$).did. or (JP-2006303377-$).did. or (US-20040207067-$).did.				
L7	11	L3 and (high same low same spac $3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/22 14:45

5/22/2009 2:58:17 PM
C:\Documents and Settings\lpcruz\My Documents\EAST\Workspaces\11399723.wsp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Othieno et al.	Attorney Docket No.: 05-2572/LSI1P272
Application No.: 11/399,723	Examiner: CRUZ, LESLIE PILAR
Filed: April 6, 2006	Group: 2826
Title: SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION	Confirmation No.: 1398

CERTIFICATE OF EFS-WEB TRANSMISSION
I hereby certify that this correspondence is being transmitted electronically through EFS-WEB to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on February 19, 2009.

Signed: _____/Laura M. Dean/_____
Laura M. Dean

AMENDMENT A

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action dated December 23, 2008, please amend the above-identified patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begin on page 2 of this paper.
Amendments to the Drawings begin on page 8 of this paper and include an attached replacement sheet.
Remarks/Arguments begin on page 9 of this paper.

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1: (**Cancelled**)

Claim 2: (**Currently Amended**) ~~An IC package as recited in Claim 1 wherein the peripheral electrical contacts arranged on the substrate include:~~ **A semiconductor integrated circuit (IC) package which comprises:**

a substrate having a first surface and a second surface;

a die attachment surface formed on the first surface;

a first ground plane for electrical connection with low speed electronic circuitry;

a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate;

a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane for electrical connection with high speed electronic circuitry;

a plurality of additional electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate; and

a plurality of additional electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate; and

peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package, wherein the peripheral electrical contacts comprise:

a first set of electrical contacts ~~**spaced and configured**~~ for electrical connection with low speed electronic circuitry **and configured to pass low bit rate electronic signals wherein said configuration includes arranging the contacts at a first spaced apart distance sufficient to establish a control differential impedance between the contacts effective to substantially eliminate cross-talk between the first set of contacts during operation with the low speed electronic circuitry**; and

a second set of electrical contacts ~~**spaced and configured**~~ for electrical connection with high speed electronic circuitry **and configured to pass high bit rate electronic signals wherein said configuration includes arranging the contacts at a second spaced apart distance sufficient to establish a control differential impedance between the contacts effective to**

substantially eliminate cross-talk between the second set of contacts during operation with the high speed electronic circuitry.

Claim 3: (Original) An IC package as recited in Claim 2 wherein the low speed electronic circuitry is defined as circuitry having serial transfer rates of less than about 1 Gigabits per second (Gb/s); and

wherein the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 1 Gb/s.

Claim 4: (Original) An IC package as recited in Claim 2 wherein the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 8.5 Gb/s.

Claim 5: (Original) An IC package as recited in Claim 2 wherein the second set of electrical contacts are spaced apart at a distance that is at least twice as far apart as the spacing for the first set of electrical contacts.

Claim 6: (Original) An IC package as recited in Claim 2 wherein the second set of electrical contacts are spaced apart at a distance that is at least three times as far apart as the spacing for the first set of electrical contacts.

Claim 7: (Original) An IC package as recited in Claim 2 wherein the second set of electrical contacts are spaced apart at a distance sufficient to establish a differential impedance of at least 100 ohms (Ω) between the contacts of the second set.

Claim 8: (Original) An IC package as recited in Claim 5 wherein the first set of electrical contacts are spaced apart a distance of at least 70 μm (micrometers) and wherein the second set of electrical are spaced apart a distance of at least 140 μm (micrometers).

Claim 9: (Original) An IC package as recited in Claim 5 wherein the first set of electrical contacts are spaced apart a distance of at least 70 μm (micrometers) and wherein the second set of electrical are spaced apart a distance of at least 200 μm (micrometers).

Claim 10: **(Currently Amended)** An IC package as recited in Claim 2 wherein the electrical contacts are arranged such that,

the **first** spacing between the contacts of the first set of electrical contacts is **smaller than the second** ~~sufficient to establish a control differential impedance effective to substantially eliminate cross-talk between I/O lines for the low speed electronic circuitry; and~~

~~the~~ spacing between the contacts of the second set of electrical contacts**, thereby enabling greater contact density for the first set of electrical contacts.** ~~is sufficient to establish a control differential impedance effective to substantially eliminate cross-talk between I/O lines for the high speed electronic circuitry.~~

Claim 11: **(Currently Amended)** An IC package as recited in Claim **2 [[10]]** wherein the electrical contacts are arranged **as part of I/O lines** such that,

the **first** spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance of at least 50 Ω between the contacts of the first set of electrical contacts to substantially eliminate cross-talk between I/O lines for the low speed electronic circuitry; and

the **second** spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100 Ω between the contacts of the second set of electrical contacts to substantially eliminate cross-talk between I/O lines for the high speed electronic circuitry.

Claim 12: **(Currently Amended)** An IC package as recited in Claim **2 [[10]]** wherein the electrical contacts are arranged such that,

the **first** spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance of at least 50 Ω between the contacts of the first set of electrical contacts; and

the **second** spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100 Ω between the contacts of the second set of electrical contacts.

Claim 13: **(Currently Amended)** An IC package as recited in Claim 2 wherein ~~**first surface of the substrate includes a**~~ **the** die attachment surface ~~**having**~~ **has** a die arrangement attached thereto,

the die arrangement being electrically connected to the first ground plane, the second ground plane, and the peripheral electrical contacts of the substrate.

Claim 14: **(Currently Amended)** An IC package as recited in Claim 13 wherein the die arrangement comprises a die having both high-speed electronic circuitry and low-speed electronic circuitry;

wherein the low-speed electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced ~~**and configured**~~ for connection with the low speed electronic circuitry; and

wherein the high-speed electronic circuitry is connected with the second ground plane and is electrically connected with the second set of electrical contacts that are spaced ~~**and configured**~~ for connection with the high speed electronic circuitry.

Claim 15: **(Currently Amended)** An IC package as recited in Claim 14 wherein the die arrangement comprises a stacked die arrangement wherein at least one die has high-speed electronic circuitry and wherein at least one die has low-speed electronic circuitry;

wherein the low-speed electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced ~~**and configured**~~ for connection with the low speed electronic circuitry; and

wherein the high-speed electronic circuitry is connected with the second ground plane and is electrically connected with the second set of electrical contacts that are spaced ~~**and configured**~~ for connection with the high speed electronic circuitry.

Claim 16: **(Currently Amended)** ~~**A semiconductor IC package as recited in Claim 1 wherein the substrate includes a plurality of layers, and wherein;**~~

A semiconductor integrated circuit (IC) package which comprises:

a substrate having a first surface and a second surface wherein;

a first layer of the substrate includes,

[[the]] a first ground plane **enabling electrical connection with low speed electronic circuitry**, and

[[the]] a second ground plane **that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection with high speed electronic circuitry**;

a second layer of the substrate includes,

a third ground plane configured for electrical connection with low speed electronic circuitry, and

a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the third ground plane configured for electrical connection with high speed electronic circuitry;

a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate;

a plurality of additional electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate; and

peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package; and

at least one reference plane associated with each layer of the substrate and the ground planes included thereon.

a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate;

a plurality of additional electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate; and

peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package.

Claims 17-25 (Cancelled).

Claim 26: (New) A semiconductor operating configuration comprising:

a mother board having two ground systems including a first ground system arranged for connection with a low speed ground plane of an IC (integrated circuit) package and a second ground system electrically isolated from the first system arranged for connection with a with speed ground plane of the IC chip;

an integrated circuit (IC) package mounted on the mother board and configured to comprise both high speed and low speed electronic circuitry, the IC comprises:

a substrate having a first surface and a second surface with an integrated circuit die construction mounted on the substrate, the die construction including both high speed and low speed electronic circuitry;

a first ground plane electrically connected with the low speed electronic circuitry of the IC and also electrically connected with first ground system of the motherboard;

a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate;

a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane connected with the high speed electronic circuitry of the IC and also electrically connected with second ground system of the motherboard;

a plurality of additional electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate; and

peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry of the motherboard.

Claim 27: (New) A semiconductor integrated circuit package, the package comprising:

a substrate having a first surface and a second surface with an integrated circuit die construction mounted on the substrate, the die construction including both high speed and low speed electronic circuitry;

a first ground plane electrically connected with the low speed electronic circuitry of the integrated circuit die construction and also arranged for electrical connection with a first ground system external to the package;

a first plurality of electrical connections that electrically connect the low speed electronic circuitry of the integrated circuit die construction with the first ground plane;

a third plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate;

a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane connected with the high speed electronic circuitry of the integrated circuit die construction and also arranged for electrical connection with a second ground system external to the package wherein said second ground system is electrically isolated from said first ground system;

a second plurality of electrical connections that electrically connect the high speed electronic circuitry of the integrated circuit die construction with the second ground plane;

a fourth plurality of electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate;

peripheral electrical contacts arranged on the substrate and configured for connection with the high speed electronic circuitry and the low speed electronic circuitry and further configured for electrical connection to circuitry external to the package.

Claim 28: (New) A semiconductor integrated circuit package as recited in Claim 27 wherein the integrated circuit die construction includes a first die having the low speed electronic circuitry mounted with a second die having the high speed electronic circuitry.

Claim 29: (New) A semiconductor integrated circuit package as recited in Claim 27 wherein the peripheral electrical contacts include a first set of peripheral contacts configured in a spaced apart arrangement such that the spacing between the contacts of the first set of peripheral contacts is sufficient to substantially eliminate cross-talk between the contacts of the first set of contacts when low speed electronic signals are passed through the contacts; and

wherein the peripheral electrical contacts further include a second set of peripheral contacts configured in a spaced apart arrangement such that the spacing between the contacts of the second set of peripheral contacts is sufficient to substantially eliminate cross-talk between the contacts of the second set of contacts when high speed electronic signals are passed through the contacts.

Claim 30: (New) A semiconductor integrated circuit package as recited in Claim 29,

wherein the first set of peripheral contacts is electrically coupled with the low speed electronic circuitry of the integrated circuit die construction;

and

wherein the second set of peripheral contacts is electrically coupled with the high speed electronic circuitry of the integrated circuit die construction.

Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 1. This sheet, which includes Fig. 1 and Fig. 2, replaces the original sheet including Fig. 1 and Fig. 2.

Attachment: Replacement Sheet

REMARKS/ARGUMENTS

The applicants thank the Examiner for the Office Action mailed December 23, 2008.

Claims 1-16 and 17-25 were pending in the application. **Claims 17-25** were subject to restriction and are now cancelled without prejudice.

In this Amendment, **Claim 16 is amended** to independent form as requested by Examiner and is now believed to be in condition for allowance.

Moreover, **Claims 2, 10-12, and 14-16 have been amended** and are discussed further herein. Also, **Claim 1 is cancelled**.

Claims 26-30 are also added. Consequently, **Claims 2-16** and **26-30** are now pending in the application. No new matter has been introduced. Reconsideration and allowance are hereby requested.

Drawing Objections

Fig. 1 is objected to. Accordingly, the number "100" has been added to the drawing.

Rejections Under 35 U.S.C. § 112

Claims 1, 2, 14, and 15 have been rejected under 35 U.S.C. § 112, 2nd paragraph.

The Applicants address the informalities raised above as follows. **Claim 1** is cancelled making further discussion of this claim moot. **Claim 2** has been amended and in the process the previously offending language is removed thereby overcoming this rejection. **Claims 14 and 15** are amended to now recite that the electrical contacts "are spaced ~~and configured~~ for connection with" low or high speed electronic circuitry respectively. This spacing defines a physical relationship between the contacts. The spacing depends on various factors including dielectric materials, physical distance, data rates and frequencies of the signals passed through the contacts and associated lines, and so on. As a general rule, spacing can be much tighter for the contacts dedicated to low speed circuitry due to the lower incidence of cross talk related problems relative to the high speed contacts which typically require greater spacing to eliminate deleterious cross-talk effects. Thus, low speed contacts are generally capable of much tighter density than the associated high speed contacts. Therefore, the two contact patterns are not interchangeable nor

are the relationships strictly functional as the function defines a specific structure (e.g., closeness, dielectric materials, and so on).

Accordingly, for at least these reasons, applicants respectfully request these rejections be withdrawn.

Rejections Under 35 U.S.C. § 102

Claims 1-4 (and although not indicated **Claims 13-14** as well) have been rejected under 35 U.S.C. § 102(b) as being anticipated by US Pat. Pub. 2004/0238939 (hereinafter *"Wu"*).

As to **Claim 1**, the cancellation of this claim alleviates this issue.

Claim 2 has been amended to incorporate by reference the limitations of Claims 1, 2, and 10. This clarifies that a series of variable speed connectors are also used with the variable speed ground planes. Thus, this amendment overcomes the expressed ground of rejection. As these limitations are not set forth in *Wu*, the applicants believe that the amended claims are fundamentally different from the cited art. This point of view is expressly supported in the Action, at page 4, 3rd paragraph, which says that *Wu* does not teach variably configured ground planes. Accordingly, applicants respectfully request this rejection be withdrawn.

As to dependent Claims 3, 4, and 13, these claims are allowable on independent grounds. However, due to the basic sufficiency of the amendment to base claim 2, no further explanation is required at this time to overcome the rejections based on *Wu*.

As to Claim 14 the applicant points out that the Wu references is insufficient for at least the reasons expressed by the Examiner at page 9 of the Action. The Action offers that the limitations of high speed and low speed circuitry do not result in a structural difference and are therefore merely an "intended use". The applicant agrees that this is true, as far as it goes. The problem is that the limitation of, for example, a "first set of electrical contacts that are spaced **...** for connection with the low speed electronic circuitry" is a structural arrangement as specified in the specification and elaborated in some further detail in the dependent claims. The spacing arrangements between the high speed and low speed contacts are different and dependent on the cross talk parameters (e.g., intervening dielectric space material, designed or anticipated bit rate of the data transmitted through the contacts, physical space separation, and so on) and therefore the "function" spells out a structural feature resulting in a cross-talk dependent spacing between the contacts. Thus, the language is structural in nature defining a specified spacing between

contacts.

Accordingly, because the cited art fails to teach all claim elements of the claimed invention, the cited art does not establish a *prima facie* case for anticipation and is therefore insufficient to establish a rejection under 35 U.S.C. § 102. Therefore, the applicants respectfully request that this ground of rejection be withdrawn as to **Claim 2,** and for at least the same reasons, **Claims 3 & 4**).

Rejections Under 35 U.S.C. § 103

Claims 5-12 stand rejected under 35 U. S. C. §§ 103(a) as being unpatentable over *Wu* and **Claim 15** further over the combination of *Wu* and *Zhu et al.* US Pat. Pub. 2005/0173807 (hereinafter *"Zhu"*).

As to **Claims 5-12**, the applicants point out that the changes to base claim 2 are sufficient to overcome the cited art (as explained above).

However, the applicants further discuss the issue of "no disclosure of the critical nature" of the claimed construction. No prior art has been provided in which two separate and electrically isolated ground planes are provided. Nor has any art been provided which teaches two arrays of contacts configured differently wherein each has been spaced or materials used to generate configurations having two different resistances to cross-talk as is the case here.

In reference to the pairs of contact sets, the claimed spaces between the contacts **are critical** because absent such spacing the structures cannot work. The claimed spaces between the contacts **are critical** because they massively increase contact density for low speed contacts. The differences between the claimed spaces between the contacts or the two sets **are critical** because they increase contact density for low speed contacts and enable improved cross-talk performance for the high speed contacts. The cited art simply does not have two sets of dedicated pins arranged with two different differential impedances. This is absent from the cited art. Moreover, nothing in the cited art suggests such a structure or suggests any of the advantages of the present invention. The cited art is expressly admitted as not teaching these limitations, additionally, it provides no teaching, mo suggestion, and no motivation to change and radically redesign the cited art to embody the present invention.

Additionally, the claimed structure is advantageous because it dispenses with the myriad of prior art individualized ground pins used previously to ground each specific high speed circuit, one at a time. This placed burdensome demands on the available pin space which is wiped away at a single stroke in accordance with the teachings of the invention. The claimed

invention comprises two ground planes, each dedicated to circuit structures operating a different data rates. Again, these limitations are missing from the cited art.

As a result, the cited art does not teach or suggest these critical limitations. Therefore, the cited art fails to establish a *prima facie* case of obviousness as to any of the rejected Claims (Claims 2 and **5-12**). Accordingly, applicants respectfully request these rejections be withdrawn.

Additionally, **Claim 15** is rejected over the combination of *Wu* and *Zhu*. As to Claim 15 the applicant points out that the *Wu* and *Zhu* references are insufficient for at least the reasons expressed by the Examiner at page 13 of the Action. The Action offers that the limitations of high speed and low speed circuitry do not result in a structural difference and are therefore merely an "intended use". The applicant offers that such a categorization does not go far enough. The problem is that the limitation of, for example, a "first set of electrical contacts that are spaced **...** for connection with the low speed electronic circuitry" is a structural arrangement as specified in the specification and elaborated in some further detail in the dependent claims. The spacing arrangements between the high speed and low speed contacts are different and dependent on the cross talk parameters (e.g., intervening dielectric space material, designed or anticipated bit rate of the data transmitted through the contacts, physical space separation, and so on) and therefore the "function" spells out the structural features of the invention. Accordingly, the spacing described (is a structural space relationship) is a spacing that improves cross-talk performance between the contacts. Thus, the language is structural in nature defining a specified spacing between contacts. Moreover, the spacing is different between the two groups of contacts. In other words, all other things being equal, low speed contacts can be spaced much more tightly than is the case for high speed contacts which are generally more affected by high frequency cross talk problems.

Therefore, the cited art, either alone or in any reasonable combination, fails to teach all of the recited claim limitations. Accordingly, the cited combination fails to establish a *prima facie* case of obviousness as to Claims 5-12 and 15. Therefore, applicants respectfully request that the withdrawn. pending grounds of rejection be withdrawn.

Allowable Subject Matter.

♦Objectionable Claim 16

Claim 16 has been objected to as being directed to allowable subject matter but being based on rejected base claims. Accordingly, **Claim 16** has been amended to independent form

incorporating the limitations of the base claim. Accordingly, it is submitted that the grounds for objection has been overcome. Therefore, the applicants respectfully submit that Claim 16 is now allowable over the art of record and request that the objection be withdrawn.

Therefore, applicants respectfully submit that all pending grounds of objection have been addressed and that the objection to Claim 16 be withdrawn.

New Claims.

Claims 26-30 have been added to more directly and expressly address aspects of the pending action. The claims have been drafted to more specifically and directly claim structural features of the package.

Conclusion:

In view of the foregoing amendments and remarks, it is respectfully submitted that the claimed invention as presently presented is patentable over the art of record and that this case is now in condition for allowance.

Accordingly, the applicants request withdrawal of all pending rejections and request reconsideration of the pending application and prompt passage to issuance. As an aside, the applicants clarify that any lack of response to any of the issues raised by the Examiner is not an admission by the applicant as to the accuracy of the Examiner's assertions with respect to such issues. Accordingly, applicant's specifically reserve the right to respond to such issues at a later time during the prosecution of the present application, should such a need arise.

As always, the Examiner is cordially invited to telephone the applicants representative to discuss any matters pertaining to this case. Should the Examiner wish to contact the undersigned for any reason, the telephone numbers set out below can be used.

Additionally, if any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 12-2252 (Order No. 05-2572).

Respectfully submitted,
BEYER LAW GROUP LLP

/Francis T. Kalinski II/
Francis T. Kalinski II
Reg. No. 44,177

P.O. Box 1687
Cupertino, CA 95015-1687
408-255-8001

Electronic Patent Application Fee Transmittal

Application Number:	11399723
Filing Date:	06-Apr-2006
Title of Invention:	Semiconductor package and method using isolated Vss plane to accommodate high speed circuitry ground isolation
First Named Inventor/Applicant Name:	Maurice O. Othieno
Filer:	Francis Theodor Kalinski II/Laura Dean
Attorney Docket Number:	05-2572/LSI1P272

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Independent claims in excess of 3	1201	1	220	220
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**220**

Electronic Acknowledgement Receipt

EFS ID:	4825108
Application Number:	11399723
International Application Number:	
Confirmation Number:	1398
Title of Invention:	Semiconductor package and method using isolated Vss plane to accommodate high speed circuitry ground isolation
First Named Inventor/Applicant Name:	Maurice O. Othieno
Customer Number:	24319
Filer:	Francis Theodor Kalinski II/Laura Dean
Filer Authorized By:	Francis Theodor Kalinski II
Attorney Docket Number:	05-2572/LSI1P272
Receipt Date:	19-FEB-2009
Filing Date:	06-APR-2006
Time Stamp:	19:12:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$220
RAM confirmation Number	4009
Deposit Account	504481
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Miscellaneous Incoming Letter	Amendment_A_Transmittal.pdf	22194 801ee7ba0fca3e66c31bc22d3f9a627e9a350e67	no	1
Warnings:					
Information:					
2		LSI1P272_Amendment_A.pdf	82802 e815ed64369d50d862a376c8934f8617e1b45df3	yes	15
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	7	
	Applicant Arguments/Remarks Made in an Amendment		8	15	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	Replacement_Sheet.pdf	361551 4d1dcebb4f3070f1262abc368fecb87efdff43a1	no	1
Warnings:					
Information:					
4	Fee Worksheet (PTO-06)	fee-info.pdf	29857 9c8042cc93d2fc882f8fa72e96770d65769d23ea	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	496404		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Othieno et al.	Attorney Docket No.: 05-2572/LSI1P272
Application No.: 11/399,723	Examiner: CRUZ, LESLIE PILAR
Filed: April 6, 2006	Group: 2826
Title: SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION	Confirmation No.: 1398

CERTIFICATE OF EFS-WEB TRANSMISSION
I hereby certify that this correspondence is being transmitted electronically through EFS-WEB to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on February 19, 2009.

Signed: _____/Laura M. Dean/_____
Laura M. Dean

AMENDMENT A TRANSMITTAL

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is an Amendment in the above-identified application.

The fee has been calculated as shown below.

	Claims After Amendment		Highest Previously Paid For	Present Extra	Small Entity Rate Fee	Large Entity Rate Fee
Total Claims	20	MINUS	20	0	x 26 = 0	x 52 = 0
Independent Claims	4	MINUS	3	1	x 110 = 0	x 220 = 220.00
Multiple Dependent Claim Present and Fee Not Previously Paid						
				Total	$0	$220.00

☒ Applicant(s) believe that no (additional) Extension of Time is required; however, if it is determined that such an extension is required, Applicant(s) hereby petition that such an extension be granted and authorize the Commissioner to charge the required fees for an Extension of Time under 37 CFR 1.136 to 12-2252 (Order No. 05-2572).

☒ Please charge any additional fees required to facilitate filing the enclosed response, to Deposit Account No. 12-2252 (Order No. 05-2572).

Respectfully submitted,
BEYER LAW GROUP LLP

/Francis T. Kalinski II/
Francis T. Kalinski II
Reg. No. 44,177

P.O. Box 1687
Cupertino, CA 95015-1687

DocCode - SCORE

SCORE Placeholder Sheet for IFW Content

Application Number: 11399723 Document Date: 2/19/2009

The presence of this form in the IFW record indicates that the following document type was received in paper and is scanned and stored in the SCORE database.

- Design Drawings

The original paper documents are in the physical artifact folder. The original documents are scanned using a higher quality capture process and stored in SCORE. A copy of these documents are scanned in IFW using the standard quality scanning process. Defects visible in both IFW and SCORE are indicative of defects in the original paper documents.

To access the documents in the SCORE database, refer to instructions developed by SIRA.

At the time of document entry (noted above):

- Examiners may access SCORE content via the eDAN interface.
- Other USPTO employees can bookmark the current SCORE URL (http://es/ScoreAccessWeb/).
- External customers may access SCORE content via the Public and Private PAIR interfaces.

Form Revision Date: October 12, 2006

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/399,723	04/06/2006	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 02/19/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 17	Minus	** 25	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 4	Minus	***3	= 1	X $ =		OR	X $220=	220
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	220

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/LAJUAN HICKSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

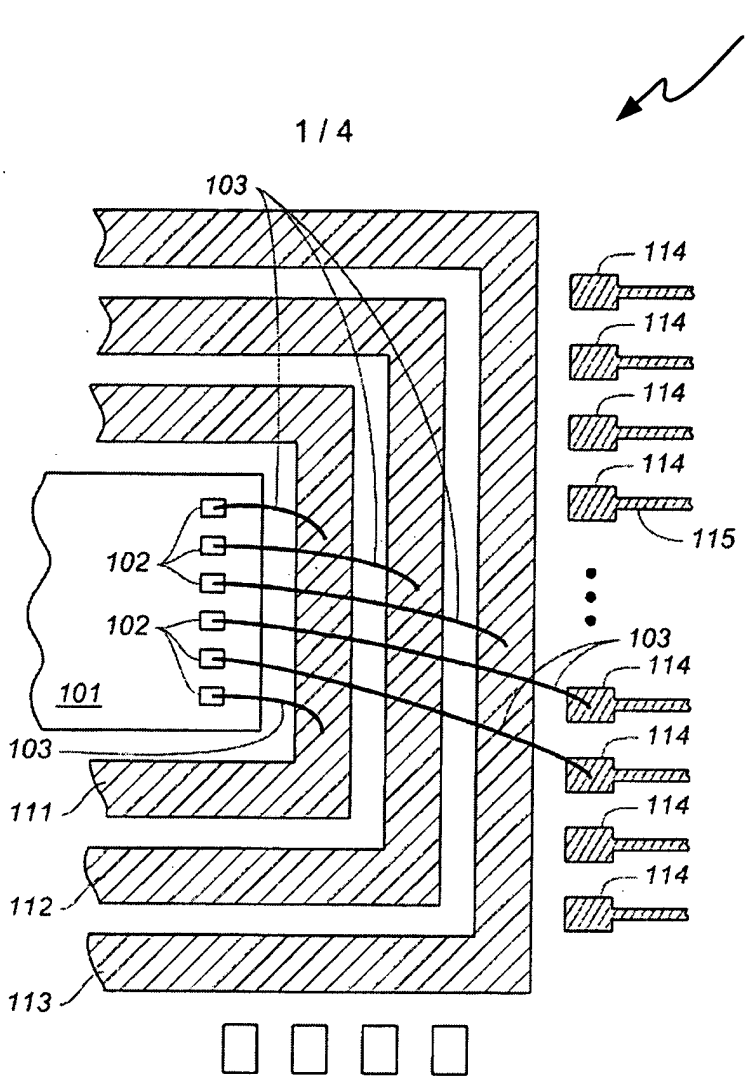


FIG. 1 (PRIOR ART)

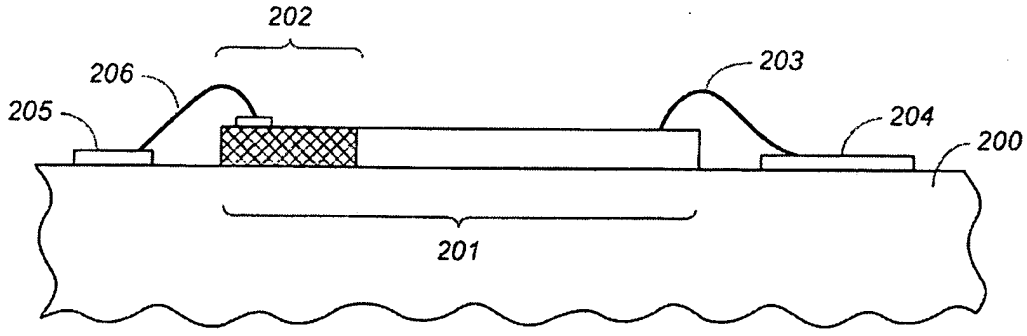


FIG. 2

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/399,723	04/06/2006	Maurice O. Othieno	05-2572/LSI1P272	1398

24319 7590 12/23/2008

LSI CORPORATION
1621 BARBER LANE
MS: D-105
MILPITAS, CA 95035

EXAMINER	
CRUZ, LESLIE PILAR	
ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
12/23/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/399,723	OTHIENO ET AL.	
	Examiner	Art Unit	
	Leslie P. Cruz	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *17-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04/06/2008* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Species I, claims 1-16, in the reply filed on 29 August 2008 is acknowledged.

Oath/Declaration

The oath or declaration filed on 06 April 2006 is acceptable.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 100. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 2, 14 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitations "configured for electrical connection with low speed electronic circuitry" and "configured for electrical connection with high speed".

Claim 2 recites the limitations "configured for electrical connection with low speed electronic circuitry" and "configured for electrical connection with high speed".

Claim 14 recites the limitations "configured for connection with the low speed electronic circuitry" and "configured for connection with the high speed electronic circuitry".

Claim 15 recites the limitations "configured for connection with the low speed electronic circuitry" and "configured for connection with the high speed electronic circuitry".

The words "configured for" in the above recited limitations do not set forth any concrete structural limitations.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu (US 2004/0238939 A1).

With respect to claim 1, Wu (Figs. 3, 9a-13) discloses a semiconductor integrated circuit (IC) package which comprises: a substrate [914, 9116] having a first surface [928] and a second surface [936]; a first ground plane [R21, paragraph 0105]; a plurality of electrical connections [1014] that electrically connect the first ground plane with solder balls [1020, paragraph 0112] mounted on the second surface of the substrate; a second ground plane [R11, paragraph 0106] that is spatially separated and electrically isolated from the first ground plane [paragraph 0091]; a plurality of additional electrical connections [1206] that electrically connect the second ground plane with solder balls [954, paragraph 0119] mounted on the second surface of the substrate; and peripheral electrical contacts [954] arranged on the substrate and configured for connection with electronic circuitry external to the package [paragraph 0117].

Wu et al. discloses two power ring segments may be used for separate ground return bonding locations for separate ground nets for two separate power nets disposed on a multi-power IC chip mounted in the package [paragraph 0083]. Wu et al. does not specify that the first ground plane is configured for electrical connection with low speed electronic circuitry or the second ground plane is configured for electrical connection with high speed electronic circuitry.

Note that a recitation of the function/intended use such as “the first ground plane is configured for electrical connection with low speed electronic circuitry or the second

ground plane is configured for electrical connection with high speed electronic circuitry" of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, and then it meets the claim. >While features of an apparatus may be recited either structurally or functionally, claims< directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >*In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997). See also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< *In re Danly,* 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See MPEP § 2114.

Therefore, claim 1 is not patentably distinguishable over the Wu et al. reference.

With respect to claim 2, Wu et al. discloses an IC package as recited in claim 1. Wu et al. further discloses the peripheral electrical contacts [954] arranged on the substrate include: a first set of electrical contacts [954, paragraph 0112] spaced for electrical connection; and a second set of electrical contacts [954, paragraph 0106] spaced for electrical connection.

Wu et al. does not specify the first set of electrical contacts are configured for electrical connection with low speed electronic circuitry or the second set of electrical contacts are configured for electrical connection with high speed electronic circuitry.

Note that a recitation of the function/intended use such as "the first set of electrical contacts are configured for electrical connection with low speed electronic circuitry or the second set of electrical contacts are configured for electrical connection with high speed electronic circuitry" of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, and then it meets the claim. >While features of an apparatus may be recited either structurally or functionally, claims< directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >*In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997). See also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< *In re Danly,* 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See MPEP § 2114.

Therefore, claim 2 is not patentably distinguishable over the Wu et al. reference.

With respect to claim 3, Wu et al. discloses an IC package as recited in claim 2. Wu et al. does not specify the low speed electronic circuitry is defined as circuitry having serial transfer rates of less than about 1 Gigabits per second (Gb/s); and wherein the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 1 Gb/s.

Note that a recitation of the function/intended use such as "the low speed electronic circuitry is defined as circuitry having serial transfer rates of less than about 1 Gigabits per second (Gb/s); and wherein the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 1 Gb/s" of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, and then it meets the claim. >While features of an apparatus may be recited either structurally or functionally, claims< directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >*In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997). See also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< *In re Danly,* 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See MPEP § 2114.

Therefore, claim 3 is not patentably distinguishable over the Wu et al. reference.

With respect to claim 4, Wu et al. discloses an IC package as recited in claim 2. Wu et al. does not specify the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 8.5 Gb/s.

Note that a recitation of the function/intended use such as "the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 8.5 Gb/s" of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, and then it meets the claim. >While features of an apparatus may be recited either structurally or functionally, claims< directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >*In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997). See also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< *In re Danly,* 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See MPEP § 2114.

Therefore, claim 4 is not patentably distinguishable over the Wu et al. reference.

With respect to claim 13, Wu et al. discloses an IC package as recited in claim 2. Wu et al. (Figs. 3, 9-13) wherein first surface of the substrate includes a die attachment surface having a die [paragraph 0094] arrangement attached thereto, the die arrangement being electrically connected to the first ground plane, the second ground plane, and the peripheral electrical contacts of the substrate.

With respect to claim 14, Wu et al. discloses an IC package as recited in claim 13. Wu et al. further discloses the die arrangement comprises a die [paragraph 0094]; wherein a first electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced for connection with the electronic circuitry; and wherein the second electronic circuitry is connected with the second ground plane and is electrically connected with the second set of electrical contacts that are spaced and configured for connection the second speed electronic circuitry. Wu et al. discloses two power ring segments may be used for separate ground return bonding locations for separate ground nets for two separate power nets disposed on a multi-power IC chip mounted in the package [paragraph 0083]. Wu et al. does not specify that the die has both high-speed electronic circuitry and low-speed electronic circuitry, wherein the first electronic circuitry is a low-speed electronic circuitry; and wherein the second electronic circuitry is high-speed electronic circuitry.

Note that a recitation of the function/intended use such as “high-speed circuitry and low-speed circuitry” of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the

claimed invention from the prior art. If the prior art structure is capable of performing the intended use, and then it meets the claim. >While features of an apparatus may be recited either structurally or functionally, claims< directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >*In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997). See also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< *In re Danly,* 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See MPEP § 2114.

Therefore, claim 14 is not patentably distinguishable over the Wu et al. reference.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al.

With respect to claims 5-7 and 10, Wu et al. discloses an IC package as recited in claim 2. Wu et al. discloses first set of electrical contacts and second set of electrical

contacts may be arranged in order to improve layout flexibility and minimizing package footprint while retaining high levels of system function performance [paragraphs 0032-0044, 0124]. The specific claimed relative spaced apart distance between the second set of electrical contacts and the first set of electrical contacts, absent any criticality, are only considered to be the "optimum" distances that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired adhesive strength, manufacturing costs, etc. (see Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, *i.e.*, results which are different in kind and not in degree from the results of the prior art, will be obtained.

Accordingly, since the applicants have not established the criticality (see next paragraph below) of the stated relative distance, it would have been obvious to one of ordinary skill in the art to use these values in the device of Wu et al.

The specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to claims 8, 9, Wu et al. discloses an IC package as recited in claim 5 and with respect to claims 11 and 12, Wu et al. discloses an IC package as recited in claim 10. Wu et al. discloses first set of electrical contacts and second set of electrical contacts may be arranged in order to improve layout flexibility and minimizing package

footprint while retaining high levels of system function performance [paragraphs 0032-0044, 0124]. The specific claimed relative spaced apart distance between the second set of electrical contacts and the first set of electrical contacts, absent any criticality, are only considered to be the "optimum" distances that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired adhesive strength, manufacturing costs, etc. (see Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, *i.e.*, results which are different in kind and not in degree from the results of the prior art, will be obtained.

Accordingly, since the applicants have not established the criticality (see next paragraph below) of the stated relative distance, it would have been obvious to one of ordinary skill in the art to use these values in the device of Wu et al.

The specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. in view of Zhu et al. (US 2005/0173807 A1).

With respect to claim 15, Wu et al. discloses an IC package as recited in claim 14. Wu et al. does not specify the die arrangement comprises a stacked die

arrangement wherein at least one die has high-speed electronic circuitry and wherein at least one die has low-speed electronic circuitry.

Zhu et al. (Fig. 4) teaches it is well known in the art for a die arrangement to comprise a stacked die arrangement [401, 403]. Zhu et al. teaches it is beneficial for a die arrangement to comprise a stacked die arrangement in order to increase device density within the footprint of a single die package [paragraph 0012].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the die arrangement of Wu et al. to comprise a stacked die arrangement, such as taught by Zhu et al., in order to increase device density within the footprint of a single die package.

Zhu et al. does not specify at least one die has high-speed electronic circuitry and wherein at least one die has low-speed electronic circuitry.

Note that a recitation of the function/intended use such as "high-speed electronic circuitry and low-speed electronic circuitry" of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, and then it meets the claim. >While features of an apparatus may be recited either structurally or functionally, claims< directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >*In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997). See also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< *In re Danly,* 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). A

claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See MPEP § 2114.

Therefore, claim 14 is not patentably distinguishable over the Wu et al. in view of Zhu et al. reference.

Allowable Subject Matter

Claim 16 would be allowable if claim 1 is rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record taken either singly or in combination fails to anticipate or fairly suggest the limitations which the Applicant claims in claim 16 in a manner which would warrant a rejection under 35 U.S.C. § 102 or 35 U.S.C. § 103.

There was no prior art found by the examiner that suggested modification or combination with the cited prior art so as to satisfy the combination of the present dependent claim 16; especially, the prior art does not provide a fourth ground plane that is spatially separated and electrically isolated from the third ground plane in combination with at least one reference plane associated with each layer of the substrate and the ground planes included thereon as recited in claim 16.

Telephone/Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leslie P. Cruz whose telephone number is 571-272-8599. The examiner can normally be reached on Monday-Friday 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leslie Pilar Cruz/
Examiner, Art Unit 2826

/Evan Pert/
Primary Examiner, Art Unit 2826

Notice of References Cited	Application/Control No. 11/399,723	Applicant(s)/Patent Under Reexamination OTHIENO ET AL.	
	Examiner Leslie P. Cruz	Art Unit 2826	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2004/0238939 A1	12-2004	Wu, Ping	257/691
*	B	US-2005/0173807 A1	08-2005	Zhu et al.	257/777
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11399723	OTHIENO ET AL.
	Examiner	Art Unit
	Leslie P Cruz	2826

SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (See Search History)	12/20/2008	lpc

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	"US 20070235849"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2008/12/05 20:19
S2	3407	(257/203,207,208,210,211).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/07 12:59
S3	3160	(high near speed) same (low near speed) same (ground)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 13:01
S4	3	S3 and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 13:08
S7	1022	((high near2 speed) with (ground)) and ((low near2 speed) with ground)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 13:29
S6	0	S5 and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 13:29
S5	767	((high near speed) with (ground)) and ((low near speed) with ground)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 13:29
S8	1	S7 and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 13:30
S9	55	((high near speed) with (ground near (line plane))) and ((low near speed) with (ground near (line plane)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 13:31

S10	41	S9 and (semiconductor ic chip (integrated near circuit$2) die)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 13:32
S11	2	("20020109205" | "6967557").PN. OR ("7358555").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/12/07 13:44
S14	3	S12 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 14:45
S13	0	S12 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 14:45
S12	1651	(257/691).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/07 14:45
S16	285	S5 and (semiconductor ic chip (integrated near circuit$2) die)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 14:51
S15	1298	S3 and (semiconductor ic chip (integrated near circuit$2) die)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 14:51
S18	5465	(257/202-211).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/07 15:13
S17	0	S3 and 257/209.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 15:13
S19	3	S3 and S18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 15:14

S24	1319	S23 same S22	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 15:15
S23	4148	(low near speed) near2 (circuit$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 15:15
S22	37023	(high near speed) near2 (circuit$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 15:15
S21	8851	(low near speed) near2 (device circuit $2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 15:15
S20	76379	(high near speed) near2 (device circuit $2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 15:15
S25	2	S24 and S18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 15:16
S27	0	S24 and S12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 15:18
S26	709	S24 and (semiconductor ic chip (integrated near circuit$2) die)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 15:18
S28	129	S24 same (chip die)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 15:24

S29	11	S24 same (ground near (plane line))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 16:35
S31	19	S24 and S30	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 16:37
S30	19453	(ground near (plane line)) same (substrate carrier interposer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 16:37
S33	81	(serial near transfer near rate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 18:03
S32	1	S30 and (serial near transfer near rate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 18:03
S35	5	(serial near transfer near rate) with (high near speed)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 18:04
S34	7	S33 and (ground near (plane line))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 18:04
S36	20	((MAURICE) near2 (OTHIENO)).INV.	US-PGPUB; USPAT	OR	ON	2008/12/07 18:06
S37	18	("20040097017" | "20070004092" | "20070018291" | "6707164" | "6956286" | "6979897" | "7098528" | "7202559").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 18:10
S38	1052	257/691.ccls. and (ground vss "v.sub. ss" gnd)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 18:13

S39	425	257/691.ccls. and (ground vss "v.sub. ss" gnd) and speed	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 18:14
S40	188	257/691.ccls. and ((ground vss "v.sub. ss" gnd) same speed)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 18:21
S41	89	257/691.ccls. and ((ground vss "v.sub. ss" gnd) with speed)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 18:22
S42	8	("4513266" | "6040524" | "6677831" | "6867668").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 18:24
S43	99	S40 not S41	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 19:15
S47	767	S45 not S46	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 20:56
S46	188	S40 S41	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 20:56
S45	780	257/E23.153.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 20:56
S44	2901	257/E23.079,E23.153.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 20:56

S49	617	S47 and ((ground vss "v.sub.ss" gnd))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 21:57
S48	1052	257/691.ccls. and ((ground vss "v.sub. ss" gnd))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/07 21:57
S51	47	S50 and impedance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/14 14:55
S50	71	(US-20070235849-$ or US-20040173822-$ or US-20080075070-$ or US-20060197718-$ or US-20060091507-$ or US-20040201085-$ or US-20070170575-$ or US-20040056344-$ or US-20060237726-$ or US-20040026794-$ or US-20070040284-$ or US-20070241465-$ or US-20040212103-$ or US-20060226447-$ or US-20070170587-$ or US-20080113499-$ or US-20080116988-$ or US-20030025208-$ or US-20060012745-$ or US-20030007442-$ or US-20050281528-$ or US-20030123818-$ or US-20060035510-$ or US-20080088007-$ or US-20060055022-$ or US-20050207131-$).did. or (US-20050051887-$ or US-20040238939-$ or US-20080203562-$ or US-20070090401-$).did. or (US-7448132-$ or US-7358555-$ or US-5912809-$ or US-5373187-$ or US-7439449-$ or US-7193311-$ or US-4827327-$ or US-6870273-$ or US-7414322-$ or US-6867668-$ or US-6797891-$ or US-4835120-$ or US-4725878-$ or US-7239527-$ or US-6919226-$ or US-6979897-$ or US-6707164-$ or US-6040524-$ or US-6677831-$ or US-7321166-$ or US-7279783-$ or US-7209366-$ or US-7129574-$ or US-7129571-$ or US-7112880-$ or US-6998719-$).did. or (US-6770963-$ or US-6707684-$ or US-6566761-$ or US-6495911-$ or US-7307293-$ or US-7015574-$ or US-6518663-$ or US-6472737-$ or US-6396136-$ or US-5808357-$ or US-5686764-$ or US-7420276-$ or US-7202546-$).did. or (JP-2006303377-$).did. or (US-20040207067-$).did.	US-PGPUB; USPAT; JPO; DERWENT	OR	ON	2008/12/14 14:55

S52	56	S50 and (impedance resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/14 14:56
S56	134	S55 and ((ground vss "v.sub.ss" gnd))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/14 15:12
S55	192	S54 and S53	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/14 15:12
S54	1652	(257/691).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/14 15:12
S53	2417	(257/786).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/14 15:12
S57	44	S55 and (((ground vss "v.sub.ss" gnd)) same (impedance resistance))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/14 15:13
S58	0	("2004/0238939").URPN.	USPAT	OR	ON	2008/12/17 18:10
S59	1	"20040212103".pn.	US-PGPUB; USPAT	OR	ON	2008/12/17 18:31
S60	3	("5274270" | "5801440" | "6445066"). PN.	US-PGPUB; USPAT	OR	ON	2008/12/17 18:37
S61	275	257/691.ccls. and (ground with (wid$3 pitch$3 spac$3))	US-PGPUB; USPAT	OR	ON	2008/12/17 18:43
S62	5	("5530287" | "5801440").PN. OR ("6897555").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/12/17 19:04
S63	13	("20030075812" | "20030089983" | "20040113252" | "5592025" | "5691568" | "5726860" | "6323065" | "6566761" | "6574108" | "6667546" | "6879039" | "6888240" | "6897555"). PN. OR ("7420286").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/12/17 19:07

L5	2	"20040207067".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/20 16:05
L10	18	("20040097017" | "20070004092" | "20070018291" | "6707164" | "6956286" | "6979897" | "7098528" | "7202559").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/20 16:09
L11	8	("20040097017" | "20070004092" | "20070018291" | "6707164" | "6956286" | "6979897" | "7098528" | "7202559").PN.	US-PGPUB; USPAT	OR	ON	2008/12/20 16:10
L13	1	"20040238939".pn. and ("954" same R21)	US-PGPUB; USPAT	OR	ON	2008/12/20 16:44
L12	1	"20040238939".pn. and ("954" and R21)	US-PGPUB; USPAT	OR	ON	2008/12/20 16:44
L17	246	L16 and wire	US-PGPUB; USPAT	OR	ON	2008/12/20 18:08
L16	299	(chip-on-chip) and (speed)	US-PGPUB; USPAT	OR	ON	2008/12/20 18:08

12/ 20/ 2008 6:34:38 PM
C:\ Documents and Settings\ lpcruz\ My Documents\ EAST\ Workspaces\ 11399723.wsp

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11399723	OTHIENO ET AL.
	Examiner	Art Unit
	Leslie P Cruz	2826

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/06/2008	12/20/2008							
	1	÷	✓							
	2	÷	✓							
	3	÷	✓							
	4	÷	✓							
	5	÷	✓							
	6	÷	✓							
	7	÷	✓							
	8	÷	✓							
	9	÷	✓							
	10	÷	✓							
	11	÷	✓							
	12	÷	✓							
	13	÷	✓							
	14	÷	✓							
	15	÷	✓							
	16	÷	✓							
	17	÷	N							
	18	÷	N							
	19	÷	N							
	20	÷	N							
	21	÷	N							
	22	÷	N							
	23	÷	N							
	24	÷	N							
	25	÷	N							

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Othieno et al.	Attorney Docket No.: 05-2572/LSI1P272
Application No.: 11/399,723	Examiner: CRUZ, LESLIE PILAR
Filed: April 6, 2006	Group: 2826
Title: SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED VSS PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION	Confirmation No.: 1398

CERTIFICATE OF EFS-WEB TRANSMISSION
I hereby certify that this correspondence is being transmitted electronically through EFS-WEB to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on August 29, 2008.

Signed: _____/Laura M. Dean/_____
Laura M. Dean

RESPONSE TO RESTRICTION REQUIREMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Restriction Requirement dated August 12, 2008, Applicant hereby elects, **without** traverse, Species I, claims 1-16 to prosecute in the above-identified patent application.

If any fees are due in connection with the filing of this Response to Restriction Requirement, the Commissioner is hereby authorized to charge such fees to Deposit Account 12-2252 (Order No. 05-2572).

Respectfully submitted,
BEYER LAW GROUP LLP

/Francis T. Kalinski II/
Francis T. Kalinski II
Registration No. 44,177

P.O. Box 1687
Cupertino, CA 95015-1687
408-255-8001

Electronic Acknowledgement Receipt

EFS ID:	3868287
Application Number:	11399723
International Application Number:	
Confirmation Number:	1398
Title of Invention:	Semiconductor package and method using isolated Vss plane to accommodate high speed circuitry ground isolation
First Named Inventor/Applicant Name:	Maurice O. Othieno
Customer Number:	24319
Filer:	Francis Theodor Kalinski II/Laura Dean
Filer Authorized By:	Francis Theodor Kalinski II
Attorney Docket Number:	05-2572/LSI1P272
Receipt Date:	29-AUG-2008
Filing Date:	06-APR-2006
Time Stamp:	21:08:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	Response_to_Restriction_Requirement.pdf	21118 00f8c7cea931e006e21f8811f13f2a25cfc21284	no	1

Warnings:	
Information:	

Total Files Size (in bytes):	21118

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/399,723	04/06/2006	Maurice O. Othieno	05-2572/LSI1P272	1398

24319 7590 08/12/2008

LSI CORPORATION
1621 BARBER LANE
MS: D-105
MILPITAS, CA 95035

EXAMINER	
CRUZ, LESLIE PILAR	
ART UNIT	**PAPER NUMBER**
2826	

MAIL DATE	DELIVERY MODE
08/12/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/399,723	OTHIENO ET AL.	
	Examiner	Art Unit	
	Leslie P. Cruz	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-25* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

This application contains claims directed to the following patentably distinct species

Species I. Drawn to Fig. 2;

Species II. Drawn to Fig. 5.

The species are independent or distinct because claims to the different species recite the mutually exclusive characteristics of such species. In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, claim 1 is generic.

There is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics. The species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search queries); and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species**, including any claims subsequently added. An argument that a

claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election of the species may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species.

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim

remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Telephone/Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leslie P. Cruz whose telephone number is 571-272-8599. The examiner can normally be reached on Monday-Friday 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Minh-Loan T. Tran/
Primary Examiner
Art Unit 2826

Leslie Pilar Cruz
Examiner
Art Unit 2826

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11399723	OTHIENO ET AL.
	Examiner	Art Unit
	Leslie P Cruz	2826

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/06/2008								
	1	÷								
	2	÷								
	3	÷								
	4	÷								
	5	÷								
	6	÷								
	7	÷								
	8	÷								
	9	÷								
	10	÷								
	11	÷								
	12	÷								
	13	÷								
	14	÷								
	15	÷								
	16	÷								
	17	÷								
	18	÷								
	19	÷								
	20	÷								
	21	÷								
	22	÷								
	23	÷								
	24	÷								
	25	÷								

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/399,723	04/06/2006	Maurice O. Othieno	05-2572/LSI1P272

CONFIRMATION NO. 1398

24319
LSI CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA95035

Title: Semiconductor package and method using isolated Vss plane to accommodate high speed circuitry ground isolation

Publication No. US-2007-0235849-A1
Publication Date: 10/11/2007

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Pre-Grant Publication Division, 703-605-4283

040606 01576 05-2572 LSI1P272

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF EXPRESS MAILING
I hereby certify that this paper and the documents and/or fees referred to as attached therein are being deposited with the United States Postal Service on April 6, 2006 in an envelope as "Express Mail Post Office to Addressee" service under 37 CFR §1.10, Mailing Label Number **EV622028055US**, addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Laura Dean

Attorney Docket No.: 05-2572/LSI1P272

First Named Inventor: Maurice O. OTHIENO

112950 U.S.PTO 11/399723 040606

UTILITY PATENT APPLICATION TRANSMITTAL (37 CFR. § 1.53(b))

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir: This is a request for filing a patent application under 37 CFR. § 1.53(b) in the name of inventors:
Maurice O. OTHIENO, Chok J. CHIA, and Amar J. AMIN

For: **SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED V_{SS} PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION**

Assigned to: LSI Logic Corporation

Application Elements:

- ☒ **23** Pages of Specification, Claims and Abstract
- ☒ **04** Sheets of Formal Drawings
- ☒ **02** Pages Combined Declaration and Power of Attorney

Accompanying Application Parts:

- ☐ Do not publish this application. Nonpublication Request is attached.
- ☒ Assignment and Assignment Recordation Cover Sheet (recording fee of $40.00 enclosed)
- ☐ 37 CFR 3.73(b) Statement by Assignee
- ☐ Information Disclosure Statement with Form PTO-1449
  - ☐ Copies of IDS Citations
- ☐ Preliminary Amendment
- ☒ Return Receipt Postcard
- ☐ Other:

Claim For Foreign Priority

☐ Priority of Application No. filed on is claimed under 35 U.S.C. § 119.

- ☐ The certified copy is enclosed.
- ☐ The certified copy has been filed in prior application U.S. Application No.
- ☐ The certified copy will follow.

Fee Calculation (37 CFR § 1.16)

☐ Applicant is entitled to Small Entity Status under 37 C.F.R. §1.27.

	(Col. 1) Total Claims		(Col. 2) Claims	(Col. 3) Present Extra	Rate	Additional Fee
TOTAL	25	MINUS	20	= 5	x 50 =	$250
INDEP.	2	MINUS	3	= 0	x 200 =	$-0-
				Utility Search Fee	=	$500
				Utility Examination Fee	=	$200
				Utility Application Size Fee (for each additional 50 sheets that exceeds 100 sheets)	$250	
				[ ] First presentation of multiple dependent claim	$360	
				Basic Filing Fee under 37 C.F.R. §1.16(a)	=	$300
				TOTAL		$1,250
				SMALL ENTITY 50% FILING FEE REDUCTION (if applicable)		

☐ Check No. in the amount of $ is enclosed.

☒ The Commissioner is authorized to charge any fees beyond the amount enclosed which may be required, or to credit any overpayment, to Deposit Account No. 12-2252 (Order No. 05-2572).

General Authorization for Petition for Extension of Time (37 CFR §1.136)

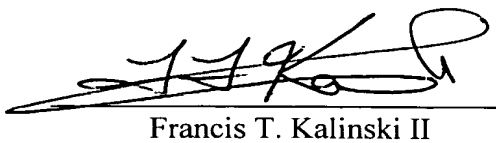
☒ Applicants hereby make and generally authorize any Petitions for Extensions of Time as may be needed for any subsequent filings. The Commissioner is also authorized to charge any extension fees under 37 CFR §1.17 as may be needed to Deposit Account No. 12-2252 (Order No. 05-2572).

☒ Please send correspondence to the following address:

Customer Number 024319

024319

Date: April 6, 2006



Francis T. Kalinski II
Registration No. 44,177

040606 01576 05-2572

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF EXPRESS MAILING
I hereby certify that this paper and the documents and/or fees referred to as attached therein are being deposited with the United States Postal Service on April 6, 2006 in an envelope as "Express Mail Post Office to Addressee" service under 37 CFR §1.10, Mailing Label Number **EV622028055US**, addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Laura Dean

Attorney Docket No.: 05-2572/LSI1P272

First Named Inventor: Maurice O. OTHIENO

112950 U.S.PTO
11/399723
040606

UTILITY PATENT APPLICATION TRANSMITTAL (37 CFR. § 1.53(b))

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir: This is a request for filing a patent application under 37 CFR. § 1.53(b) in the name of inventors:
Maurice O. OTHIENO, Chok J. CHIA, and Amar J. AMIN

For: **SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED V_{SS} PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION**

Assigned to: LSI Logic Corporation

Application Elements:

- ☒ **23** Pages of Specification, Claims and Abstract
- ☒ **04** Sheets of Formal Drawings
- ☒ **02** Pages Combined Declaration and Power of Attorney

Accompanying Application Parts:

- ☐ Do not publish this application. Nonpublication Request is attached.
- ☒ Assignment and Assignment Recordation Cover Sheet (recording fee of $40.00 enclosed)
- ☐ 37 CFR 3.73(b) Statement by Assignee
- ☐ Information Disclosure Statement with Form PTO-1449
  - ☐ Copies of IDS Citations
- ☐ Preliminary Amendment
- ☒ Return Receipt Postcard
- ☐ Other:

Claim For Foreign Priority

☐ Priority of Application No. filed on is claimed under 35 U.S.C. § 119.

- ☐ The certified copy is enclosed.
- ☐ The certified copy has been filed in prior application U.S. Application No.
- ☐ The certified copy will follow.

Fee Calculation (37 CFR § 1.16)

☐ Applicant is entitled to Small Entity Status under 37 C.F.R. §1.27.

	(Col. 1) Total Claims		(Col. 2) Claims	(Col. 3) Present Extra	Rate	Additional Fee
TOTAL	25	MINUS	20	= 5	x 50 =	$250
INDEP.	2	MINUS	3	= 0	x 200 =	$-0-
				Utility Search Fee	=	$500
				Utility Examination Fee	=	$200
				Utility Application Size Fee (for each additional 50 sheets that exceeds 100 sheets)	$250	
				[ ] First presentation of multiple dependent claim	$360	
				Basic Filing Fee under 37 C.F.R. §1.16(a)	=	$300
				TOTAL		$1,250
				SMALL ENTITY 50% FILING FEE REDUCTION (if applicable)		

☐ Check No. in the amount of $ is enclosed.

☒ The Commissioner is authorized to charge any fees beyond the amount enclosed which may be required, or to credit any overpayment, to Deposit Account No. 12-2252 (Order No. 05-2572).

General Authorization for Petition for Extension of Time (37 CFR §1.136)

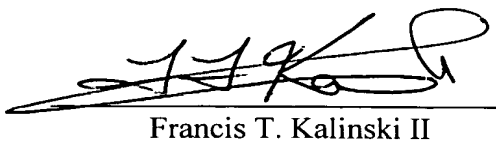
☒ Applicants hereby make and generally authorize any Petitions for Extensions of Time as may be needed for any subsequent filings. The Commissioner is also authorized to charge any extension fees under 37 CFR §1.17 as may be needed to Deposit Account No. 12-2252 (Order No. 05-2572).

☒ Please send correspondence to the following address:

Customer Number 024319

024319

Date: April 6, 2006



Francis T. Kalinski II
Registration No. 44,177

SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED V_{SS} PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION

Inventors:

Maurice O. Othieno
Chok J. Chia
Amar J. Amin

TECHNICAL FIELD

[0001] The invention described herein relates generally to semiconductor device packaging. In particular, the invention relates to a method and apparatus for grounding high speed signals from a semiconductor device using an usolated ground plane.

BACKGROUND

[0002] The semiconductor industry makes wide use of packaging substrates to hold and electrically interconnect integrated circuit (IC) die mounted within the packaging substrate. In some implementations the packaging substrates are configured to protect and secure the delicate IC die while enabling electrical connections with known external electrical interconnection socket formats. When used for low speed integrated circuits, these packaging substrates include standard ground planes for grounding the circuitry of integrated circuit die mounted in semiconductor packages. In typical implementations the IC die is grounded to a single ground plane (also referred to herein as a "V_{ss} plane") which is grounded to another system ground. For example, the package can be grounded by solder attachment to a mother board ground. Typically, a packaging substrate includes a BT (bismaleimide triazine) core having various metallization and solder mask layers to form the substrate. As is known to those having ordinary skill in the art other substrate materials can be used. For example, ceramic and other materials

are also commonly employed. In one common implementation semiconductor die is attached to the substrate and electrically connected to various electrical connections of the substrate using, for example, wire-bonding techniques. The wire bonds and the die are typically encapsulated with a protective layer of encapsulant. Such packages and the methods of their construction are well known to persons having ordinary skill in the semiconductor packaging arts. Typically, the packages are then provided with a stiffener and a heat spreader to complete the packages.

[0003] Fig. 1 is a simplified schematic plan view of a portion of a standard PBGA (plastic ball grid array) package 100 configured in accordance with known prior art technologies. The depicted package 100 includes a circuit die 101 typically arranged on a die attach pad. A series of metallization structures are arranged about the die 101. In the depicted structure, a ground layer (V_{ss}) 111 is arranged about the die 101. A core power layer ($V_{DD\ core}$) 112 forms another metallization layer. $V_{DD\ core}$ 112 is typically connected with metal filled vias to underlying solder balls that are connected to a system power. Another input output (I/O) power layer ($V_{DD\ I/O}$) 113 forms another metallization layer for connection to I/O power. Additionally, the package includes electrical contact "fingers" 114. Typically, metallization lines 115 electrically connect the fingers to vias (not shown) that connect with solder balls on the bottom of the substrate. In some configurations the fingers 114 are typically connected to the ground plane 111. The die 101 includes a series of bond pads 102 that are connected with the fingers 114, V_{ss} 111 (ground), $V_{DD\ core}$ 112, $V_{DD\ I/O}$ 113 with wire bonds 103. In the depicted die 101 the high speed portions of the die and low speed portions of the die are electrically connected to the same ground plane V_{ss} 111.

[0004] However, higher speed circuitry is being employed in the construction of modern IC's. Frequently, these newer IC's include both high speed and lower speed systems. This dichotomy presents a number of problems not solved by existing packaging substrates. As depicted above, existing packages generally include a single ground plane for all IC systems and grounds. When all systems

operated at low frequencies or low serial data transfer rates this situation was not much of a problem. However, at highs speeds a number of problems begin to occur. For one, excessive noise generated by the high-speed circuitry interferes with the operation of the low-speed circuitry sharing the same ground plane. At high data rates this is a serious problem. Additionally, older packaging substrates developed with lower speed circuitry in mind are configured the I/O and ground contacts spaced more closely together for maximum electrical contact density. However, at high frequencies and data rates signal and ground lines that are too closely spaced exhibit large amounts of cross talk. Again with serious consequences. Additionally, at high system performance the problem of ground bounce is magnified. Solutions to these problems have been difficult to solve.

[0005] Combining low speed and high-speed grounds on the same ground plane has generated numerous problems. One approach tried in the prior art required that individual pins be used for separately grounding each high-speed ground connection. This has the undesirable property of using up a limited amount of pins to accommodate ground connections. It also increases the density of high-speed interconnections resulting in undesirable cross talk between all ground and I/O lines. Such commonly constructed packages have until recently provided satisfactory grounding for packaging substrates. Now, with increasing IC speeds and data transfer rates the traditional package format is increasingly proving be unsatisfactory. Accordingly, what is needed is a packaging design and approach that provides superior grounding properties enabling both high speed and low speed circuitry to be used in the same packaging substrate.

SUMMARY OF THE INVENTION

[0006] In accordance with the principles of the present invention, an improved semiconductor package and methods for its fabrication are disclosed.

[0007] In general, the present invention is directed toward methods and packages that provide packages with a dedicated high-speed ground plane that is electrically isolated from the ground plane used to ground the low speed circuitry.

[0008] One embodiment of the invention comprises a semiconductor integrated circuit (IC) package including a substrate with a first ground plane configured for electrical connection with low speed electronic circuitry. This first ground plane has a number of electrical connections electrically connecting the first ground plane with solder balls mounted on the substrate. Additionally the substrate includes a second ground plane that is configured for electrical connection with high speed electronic circuitry and is electrically isolated from the first ground plane. The second ground plane electrically connected with solder balls mounted on the substrate. The substrate further including peripheral electrical contacts arranged on the substrate configured for connection with electronic circuitry external to the package. In another related embodiment, the contacts used for electrical connection with the high speed circuitry have wider spacing that the low speed contacts.

[0009] In another embodiment the invention includes semiconductor integrated circuit (IC) package having a substrate with a die attachment area and having a first ground plane arranged thereon configured for electrical connection with low speed electronic circuitry. The package includes a plurality of electrical connections that electrically connect the first ground plane with electrical contacts that are to be connected with an external ground. The package includes a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane configured for electrical connection with high speed electronic circuitry. The package includes a plurality of additional electrical connections that electrically connect the second ground plane with electrical contacts that are to be connected with an external ground. The package includes electrical I/O contacts configured for connection with the die and enabling electrical connection of the package with external circuitry.

[0010] Other aspects and advantages of the invention will become apparent from the following detailed description and accompanying drawings which illustrate, by way of example, the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The following detailed description will be more readily understood in conjunction with the accompanying drawings, in which:

[0012] Fig. 1 is a simplified plan view of a conventional substrate and package used to package semiconductor IC chips using a common ground plane.

[0013] Fig. 2 is a simplified schematic cross section view of a package embodiment with a dedicated isolated high-speed ground plane constructed in accordance with the principles of the invention.

[0014] Figs. 3 & 4 are simplified plan view depictions of a package embodiment with a dedicated isolated high-speed ground plane constructed in accordance with the principles of the invention.

[0015] Fig. 5 is a simplified schematic cross section view of a package embodiment with a dedicated isolated high-speed ground plane having a stacked die mounted thereon constructed in accordance with the principles of the invention.

[0016] Fig. 6 is a simplified schematic cross section view of a package substrate embodiment configured for use in a multi-layer substrate with a dedicated isolated high-speed ground plane constructed in accordance with the principles of the invention

[0017] It is to be understood that in the drawings like reference numerals designate like structural elements. Also, it is understood that the depictions in the Figures are not necessarily to scale.

DETAILED DESCRIPTION OF THE INVENTION

[0018] The present invention has been particularly shown and described with respect to certain embodiments and specific features thereof. The embodiments set forth hereinbelow are to be taken as illustrative rather than limiting. It should be readily apparent to those of ordinary skill in the art that various changes and modifications in form and detail may be made without departing from the spirit and scope of the invention.

[0019] In general, the present invention encompasses semiconductor package designs and methods that include separate electrically isolated ground planes devoted specifically to the grounding of high-speed circuitry. Additionally, embodiments of the invention include I/O bond fingers arranged at an increased spaced apart distance to establish a differential impedance sufficient to reduce the cross talk between the high speed bond finger connections and their associated metal interconnect structures (i.e., wires, metallization lines, and the like). In particular, the invention addresses package structures enabling a mix of high speed and low speed circuitry with a substantial I/O pin density.

[0020] Fig. 2 presents a simplified schematic depiction of one generalized embodiment illustrating some aspects of the invention. A portion of a packaging substrate 200 is shown. The substrate 200 has a die arrangement mounted thereon. In the depicted embodiment the die arrangement comprises a semiconductor integrated circuit (IC) die 201 mounted with the substrate 200. The depicted die 201 includes a portion 202 of the die having high-speed circuitry. Other portions of the die 201 can include low-speed circuitry.

[0021] As used herein, high-speed circuitry refers to circuitry and electronic systems that operate at higher data rates or higher frequencies than ordinary "low-speed" circuitry. For example, circuitries operating at serial data rates higher than 1 Giga Bits per second (Gb/s) are considered high-speed circuitry. Also, this particularly the case for high-speed circuitry operating at serial data rates higher than 8.5 Gb/s and higher. For purposes of this patent circuitry operating at lower

data rates and frequencies are considered non-high speed circuitry or also low-speed circuitry.

[0022] Returning to a discussion of Fig. 2 separate electrically isolated ground planes are used to isolate high-speed circuitry from low speed circuitry. The low-speed circuitry is electrically connected 203 with a first ground plane 204. A second ground plane 205 is also formed on the substrate 200. The second ground plane 205 is electrically isolated from the first ground plane 204. The high-speed circuitry 202 is electrically connected 206 with the second ground plane 205. Additionally, the first and second ground planes are electrically connected to separate external contacts. These contacts are then grounded to external ground connections (e.g., system grounds of a system upon which the completed package is mounted). When the principles of the invention are applied to ball grid array (BGA) type packages these contacts are typically facilitates by conductive vias that pass through the substrate and are electrically connected to both, a ground plane and an underlying solder pad. Solder balls are then used to make the external ground connections to other grounds. Of course, the inventors specifically contemplate the application of separate isolated ground planes for the high speed systems as applied to many other packaging systems known to those having ordinary skill in the art. Such systems include, but are not limited to, flip chip implementations, leadframe applications, leadless leadframe applications, as well as many other packaging approaches.

[0023] The inventors again point out that Fig. 2 is a very generalized diagram having numerous particular applications that can vary substantially in appearance and implementation while still preserving the principles of the invention.

[0024] Fig. 3 is a plan view of another simplified depiction of a packaging substrate suitable for implementing the principles of the invention. Additionally, Fig. 3 illustrates some other aspects of the invention in greater detail. Fig. 3 depicts an example of an inventive semiconductor packaging substrate 300 constructed in accordance with the principles of the invention. The depicted

embodiment is view in plan view. The packaging substrate 300 in the depicted embodiment can be an ordinary PBGA substrate 300. The substrate can be formed of a number of materials, for example, a BT substrate on the order of 0.60 mm thick can be used (although substrates of any thickness can be employed). Additionally, the substrate 300 can be comprised of any of other common substrate material (e.g., ceramic materials and the like).

[0025] The substrate 300 can be an ordinary two-layer PBGA substrate. Additionally, the substrate can comprise multi-layer substrates (for example, four layer substrates with multiple reference planes and so on). Also, the principles of the invention can be adapted to any BGA (ball grid array) type substrate. Moreover, as briefly touched upon above, the inventors specifically contemplate that the principles of the invention can be applied to flip chip packages, leadframe type packages, leadless lead frame packages, as well as most commonly employed package constructions known to those having ordinary skill in the art.

[0026] The depicted substrate 300 further includes a series of metallization structures are arranged about a die attachment area 302 (onto which a die can be attached). In the depicted structure, the metallization layer includes a core power layer ($V_{DD\ core}$) 312. Typically, underlying the core power layer 312 are conductive metal filled vias (not depicted in this view). The vias electrically connect the power layer 312 with underlying solder pads having solder balls formed thereon. The solder balls are used to electrically connect the core power layer 312 to a system power. Also, the metallization layer includes an I/O power layer ($V_{DD\ I/O}$) 313 for connection of the systems of the die to various I/O power supplies. Additionally, the metallization layer includes a low speed V_{ss} ground (V_{ss}) plane 311. The low speed circuitry of the die is connected to this low speed ground plane 311. Additionally, in the depicted embodiment, underlying the low speed ground plane 311 are conductive metal filled vias 321. The vias 321 electrically connect the low speed ground plane 311 with underlying solder pads

having solder balls formed thereon. The solder balls are used to electrically connect the low speed ground plane 311 to an external ground.

[0027] Additionally, the package includes electrical contact "fingers" 314 for connection to low speed circuitry. These fingers 314 can be connected to I/O signals or ground or to external connections. Metal interconnect lines 315 can be used to electrically connect the fingers 314 to conductive vias (320) that connect with other metallization structures or solder balls on the bottom of the substrate. In some configurations the fingers 314 are connected to the low speed ground plane 311. When a die is attached to the attachment area 302 bond pads of the die can be wire bonded or otherwise connected with the fingers 314, low speed ground 311, $V_{DD\ core}$ 312, and $V_{DD\ I/O}$ 313.

[0028] Additionally, a second ground plane 331 is arranged on the substrate 300. This second ground plane 331 is dedicated to the grounding of high-speed circuitry. The high-speed ground plane 331 is electrically and spatially isolated from the low speed ground plane 311. This prevents much of the noise and cross-talk when the high and low speed systems share the same ground plane. Additionally, by providing an entire dedicated ground plane 311 devoted to grounding only the high-speed circuitry, many bond fingers previously used for grounding high-speed circuitry are no longer needed. This has many advantageous that will be discussed in detail below. Also, in the depicted embodiment, underlying the high-speed ground plane 331 are conductive metal filled vias 322 (identified by the dashed lines). The vias 322 electrically connect the high-speed ground plane 331 with underlying solder pads having solder balls formed thereon. The solder balls are used to electrically connect the high-speed ground plane 331 to an external ground.

[0029] Additionally, the package includes a set of high-speed electrical contact fingers 334 dedicated for connection with high-speed circuitry. These fingers 334 can be connected to high-speed I/O signals or to the high-speed ground 331 or to external connections. Metal interconnect lines 335 can also be

used to electrically connect the fingers 334 to outlying conductive vias 323 that connect with other metallization structures or solder balls on the bottom of the substrate. In some configurations, the high-speed fingers 334 can be connected with the high-speed ground plane 331. When a die is attached to the attachment area 302, high-speed portions of the die can be wire bonded or otherwise connected with the fingers 334, high-speed ground 331, $V_{DD\ core}$ 312, and $V_{DD\ I/O}$ 313 or other portions of the substrate.

[0030] One particular advantage of the configuration illustrated in Fig. 3 will now be discussed with respect to Fig. 4. Fig. 4 schematically illustrates portions of Fig. 3 in an expanded view arranged to more clearly illustrate certain properties of the invention. The low speed ground plane 311 and the associated via 321 are depicted. Also depicted, the high speed ground plane 331 and its associated vias 321. The low speed fingers 314 are depicted, as are the high-speed fingers 334.

[0031] In one example, implementation, the low speed fingers 314 are arranged using a spacing arranged to reduce cross talk and interference between adjacent low speed fingers 314 and their associated lines. In the depicted example, the low speed fingers 314 are spaced apart a distance L of about least 70 μm (micrometers). This results in a control differential impedance of about 50 Ω (ohms). Tighter spacing can be achieved by introducing various dielectric materials between the low speed fingers 314 and their associated conductive lines 315 to maintain the desired level of differential impedance. Due to the increased noise and other frequency dependent effects it is important to increase the spacing between the high-speed fingers 334 and their associated conductive lines 335. In one embodiment, a distance between the high-speed fingers 334 is increased to about double the distance for the low speed circuitry. Accordingly, the high-speed fingers 334 are spaced apart a distance H of about at least 140 μm. This results in a control differential impedance of about 100 Ω (ohms). Tighter spacing can be achieved by introducing various dielectric materials between the high-speed fingers 334 and their associated conductive lines 335 to maintain the desired

level of differential impedance. In another embodiment, the distance H is tripled (to at least 140 μm) relative to the low speed distance L. The general idea of the invention being that for low-speed signals a control differential impedance of about 50 Ω and that for high-speed circuitry a control differential impedance of at least 100 Ω is desired between the high-speed fingers.

[0032] Thus, it should be noted that due to the presence of the high-speed ground plane 331 (and the opportunity for large scale consolidation of high speed ground connections) the need for large numbers of individual high speed ground pins is reduced. Accordingly, the spacing between the contacts of a set of electrical contacts is sufficient to establish a control differential impedance effective to substantially eliminate cross-talk between I/O lines for the high speed electronic circuitry. Additionally, such a configuration allows a narrower spacing between the contacts of a set of low speed electrical contacts that is still sufficient to establish a control differential impedance effective to substantially eliminate cross-talk between I/O lines for the low speed electronic circuitry.

[0033] It should be noted that although the invention is described here with respect to a two-layer BGA package, the principles and methodologies described here can readily be used to construct four and six (or more) layer packages, as well as, EPBGA (enhanced plastic ball grid array) packages, leaded packages (those with leads rather than solder balls), or chip scale packages (those that are 15 x 15 mm^2 or smaller). The support elements can be formed on the front side and/or the backside of the substrate, depending on the amount of stiffening desired.

[0034] Fig. 5 schematically depicts a portion another embodiment of the invention wherein the die and ground structures are assembled into a completed package 500. For sake of simplicity many features are not specifically shown in this view. The package includes a die arrangement that comprises a stacked die structure. In the depicted example, one die 501 includes low speed circuitry and another stacked die 502 includes high-speed circuitry.

[0035] The low speed portions of the die 501 can be wire bonded or otherwise connected with a low speed ground 511, a core power plane 512, and an I/O power plane 513. Also, the low speed portions of the die can be connected to signal I/O fingers (not shown in this view). Similarly, the speed portions of the stacked die 502 can be wire bonded or otherwise connected with a high speed ground 521, the core power plane 512, and the I/O power plane 513. Also, the high-speed portions of the die can be connected to high-speed signal I/O fingers (not shown in this view). It is to be noted that the stacked die arrangement can include any variety of high speed and low speed circuitry of each of the depicted die. As depicted this embodiment uses wire bonds. However, this need not be the case. The die 501, 502 and upper metallization layers 511, 512, 513, and 521 are encased in an encapsulant material 525. Additional accessories can also be added to the package 500. These commonly include, but are not limited to heat spreaders, heat shields, heat sinks, ESD shields, and so on.

[0036] Fig. 6 is a highly simplified depiction of a multi-plane substrate embodiment suitable for implementing the principles of the invention. The substrate is 600 is rendered in simplified schematic cross-section view. The packaging substrate 600 in the depicted embodiment can be an ordinary multi-layer BGA substrate 600. The substrate can be formed of a number of materials, for example, a BT substrate on the order of 0.60 mm thick can be used (although substrates of any thickness can be employed). Additionally, the substrate 600 can be comprised of any of other common substrate material (e.g., ceramic materials and the like).

[0037] The depicted substrate 600 can be an ordinary four-layer BGA substrate. However, the skilled man will be aware that this basic concept can be extended to any type of multi-level BGA-type substrate. Moreover, as briefly touched upon above, the inventors specifically contemplate that the principles of the invention can be applied to flip chip packages, leadframe type packages, leadless lead frame packages, as well as most commonly employed package constructions known to those having ordinary skill in the art.

[0038] The depicted substrate 300 further includes a series of metallization planes arranged in a substrate core 601. These planes are constructed at various levels in the substrate and are connected to accomplish their various functions in a manner known to those having ordinary skill in the art. In the depicted embodiment a top layer is formed on the substrate metallization layer to form a core power layer ($V_{DD\ core}$) 612. Typically, underlying the core power layer 612 are conductive metal filled vias (not depicted in this view). These vias electrically connect the core power layer 612 with underlying solder pads having solder balls formed thereon. The solder balls are used to electrically connect the core power layer 612 to a system power. Also, the metallization layers include an I/O power layer ($V_{DD\ I/O}$) 613 for connection of the systems of the die to various I/O power supplies. The layer 613 can also be connected to solder balls to associated I/O power sources.

[0039] A Vss reference layer 616 is also used in such multi layer configurations. It is to be noted that the top and bottom layers 612, 616 can be exposed at the surfaces or encapsulated by portions of the substrate core. Also, layers of insulating material can be formed over portions of the layers 612, 616. Additionally, the metallization layers include a low speed V_{ss} ground plane 611. The low speed circuitry of the die/substrate are connected to this low speed ground plane 611. Additionally, in the depicted embodiment, underlying the low speed ground plane 611 are conductive metal filled vias 621 that pass through the substrate core 601 and the intervening planes (here 613, 616). The vias 621 electrically connect the low speed ground plane 611 with underlying solder pads 617 having solder balls 618 formed thereon. The solder balls are used to electrically connect the low speed ground plane 611 to an external ground.

[0040] The various planes can be connected to electrical contact "fingers" (not shown). For example, certain fingers can be for connection to low speed circuitry. Also, these fingers can be connected to I/O signals or ground or to external connections. Metal interconnect lines can be used to electrically connect the

fingers to conductive vias that connect with other metallization structures or solder balls on the bottom of the substrate (not shown in this view). In some configurations the fingers can be connected to the low speed ground plane 611.

[0041] Importantly, a second isolated ground plane 631 is formed on the substrate 600. This second ground plane 631 is dedicated to the grounding of high-speed circuitry. As shown here, the high-speed ground plane 631 is electrically and spatially isolated from the low speed ground plane 611. This prevents much of the noise and cross-talk when the high and low speed systems share the same ground plane. Also, in the depicted embodiment, underlying the high-speed ground plane 631 are conductive metal filled vias 621 (that are isolated from the low speed vias connected to the low speed ground plane 611). As before, the vias 321 electrically connect the high-speed ground plane 631 with underlying solder pads 617 having solder balls 618 formed thereon. The solder balls are used to electrically connect the high-speed ground plane 631 to an external ground.

[0042] As before, when a die is attached to an attachment area of the substrate, typically the high-speed portions of the die are electrically connected with the high-speed ground 631, $V_{DD\ core}$ 612, and $V_{DD\ I/O}$ 613 or other portions of the substrate. Such connections can be established using a number of approaches known to those having ordinary skill in the art (e.g., wire bonding).

[0043] The same advantages can be enjoyed by the depicted configuration as with the embodiments previously depicted (e.g., in Fig. 3). For example, the low speed fingers can be arranged in a tight spacing arrangement with the high-speed fingers having a more open and widely spaced arrangement. Similar spacings and control differential impedances can be employed in the multi-layer embodiments.

[0044] Again, it should be noted that although the invention is described here with respect to a four-layer BGA package, the principles and methodologies described here can readily be used to construct any multi-layer configuration, as well as, EPBGA (enhanced plastic ball grid array) packages, leaded packages

(those with leads rather than solder balls), or chip scale packages (those that are 15 x 15 mm^2 or smaller). The support elements can be formed on the front side and/or the backside of the substrate, depending on the amount of stiffening desired.

[0045] The present invention has been particularly shown and described with respect to certain preferred embodiments and specific features thereof. However, it should be noted that the above-described embodiments are intended to describe the principles of the invention, not limit its scope. Therefore, as is readily apparent to those of ordinary skill in the art, various changes and modifications in form and detail may be made without departing from the spirit and scope of the invention as set forth in the appended claims. Other embodiments and variations to the depicted embodiments will be apparent to those skilled in the art and may be made without departing from the spirit and scope of the invention as defined in the following claims. In particular, it is contemplated by the inventors that many different arrangements and configurations can be established for constructing semiconductor packages having isolated high speed grounds. Although only a few configurations are expressly disclosed herein, it should be appreciated by anyone having ordinary skill in the art that, using the teachings disclosed herein, many different package support configurations can be implemented and still fall within the scope of the claims. Further, reference in the claims to an element in the singular is not intended to mean "one and only one" unless explicitly stated, but rather, "one or more". Furthermore, the embodiments illustratively disclosed herein can be practiced without any element which is not specifically disclosed herein.

SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED V_{SS} PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION

5

ABSTRACT OF THE DISCLOSURE

Embodiments of the invention include a semiconductor integrated circuit package that includes a substrate which can have an integrated circuit die attached thereto. The package includes a dedicated high-speed ground plane that is electrically isolated from the ground plane used to ground the low speed circuitry of the package.

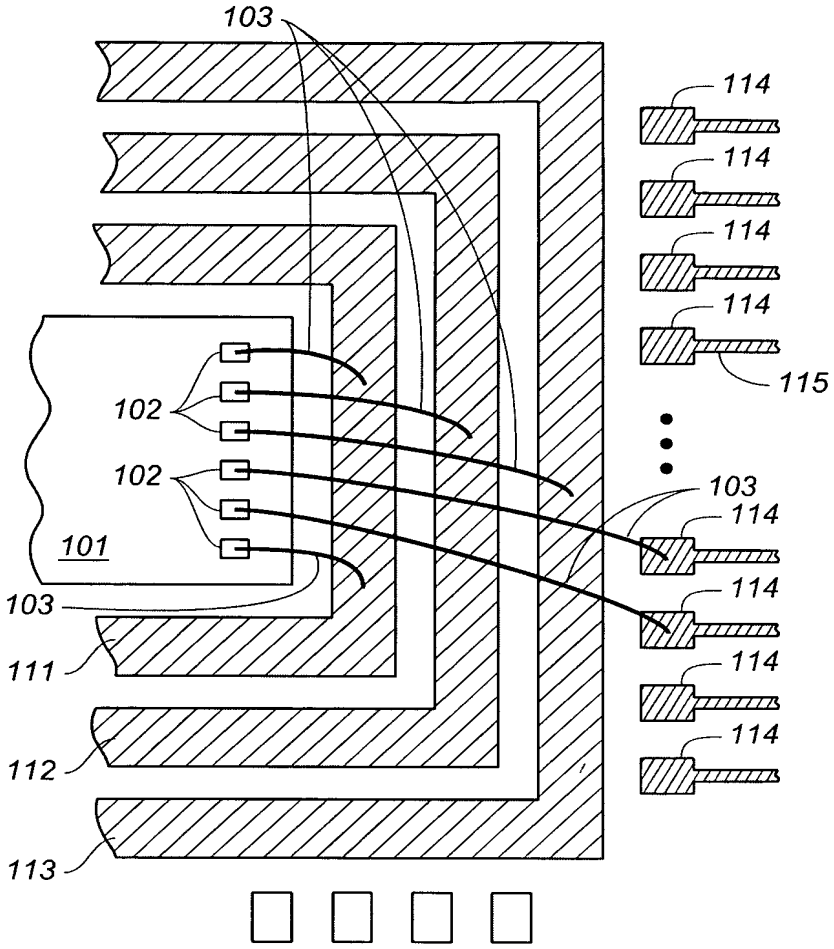


FIG. 1 (PRIOR ART)

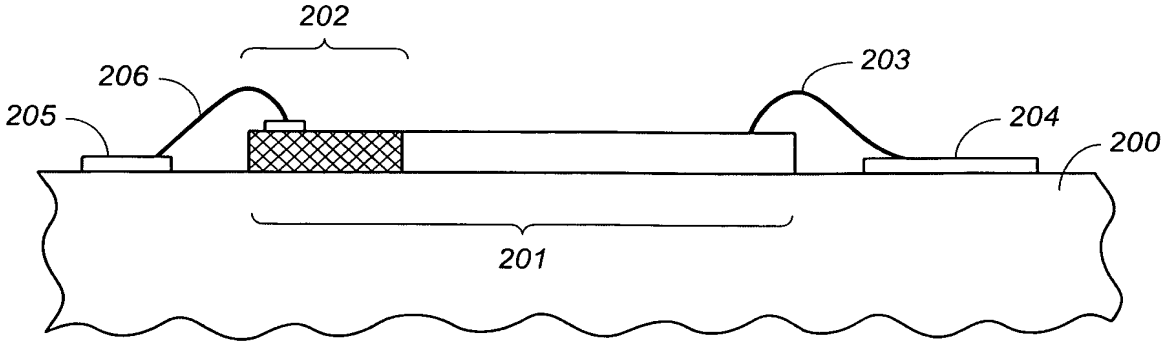


FIG. 2

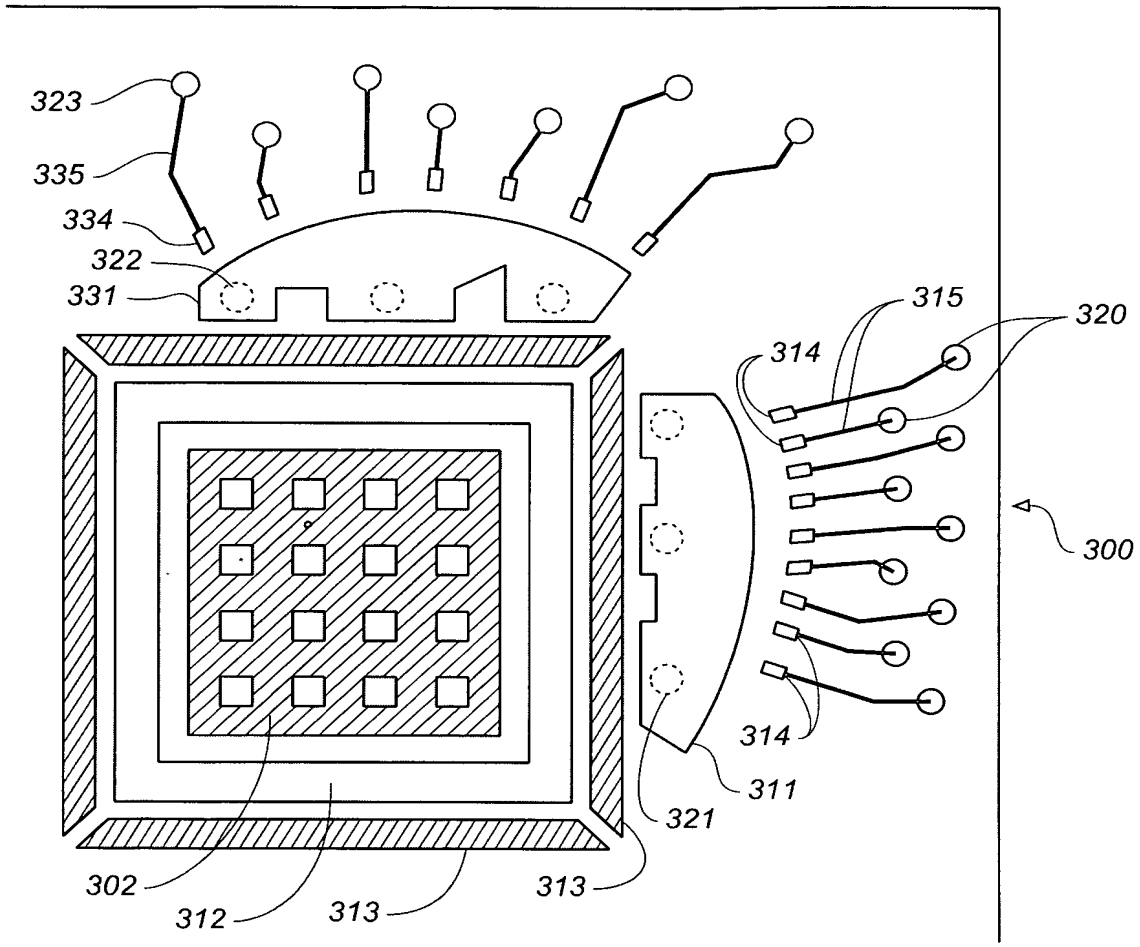


FIG. 3

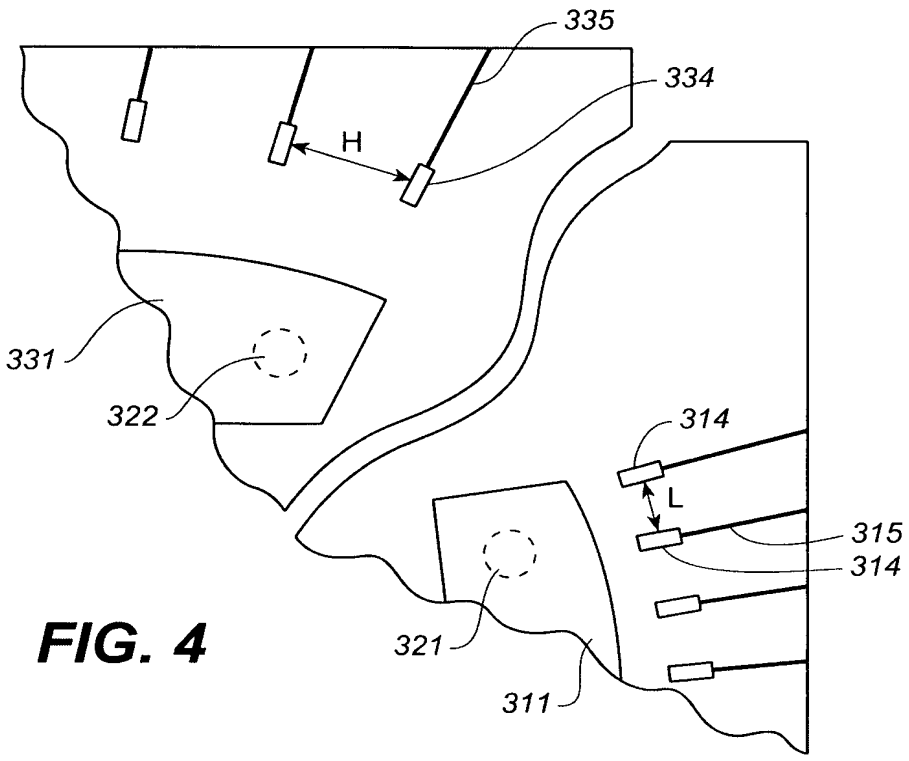

335
334
H
331
322
314
L
315
314
321
311

FIG. 4

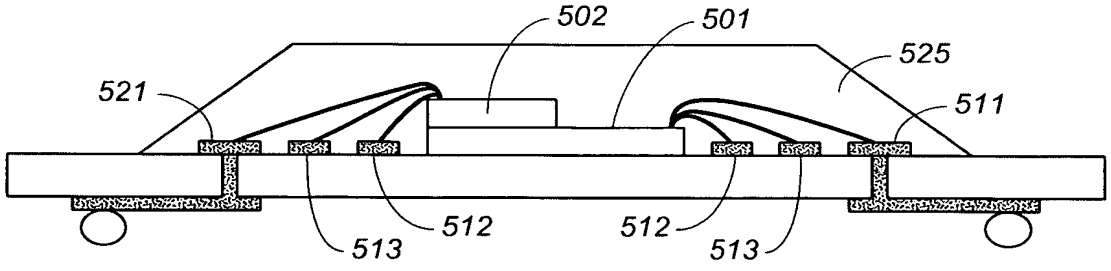

502
501
525
521
511
513
512
512
513

FIG. 5

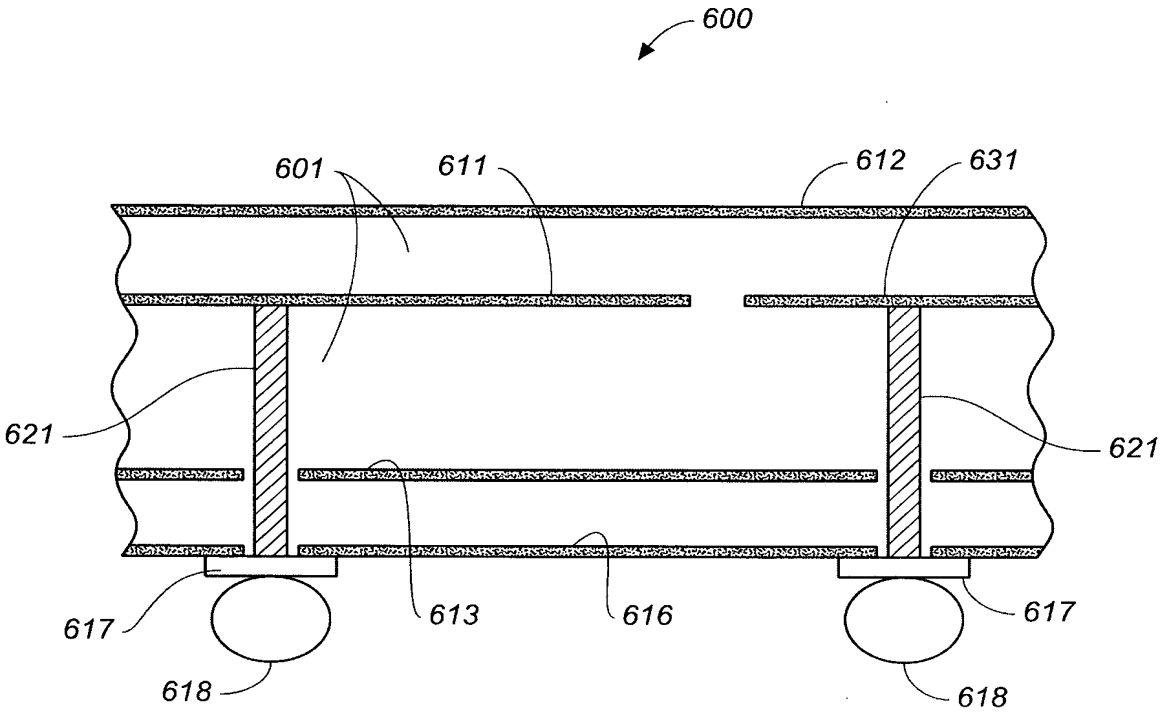


FIG. 6

DECLARATION AND POWER OF ATTORNEY FOR ORIGINAL U.S. PATENT APPLICATION

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: SEMICONDUCTOR PACKAGE AND METHOD USING ISOLATED V_{SS} PLANE TO ACCOMMODATE HIGH SPEED CIRCUITRY GROUND ISOLATION, the specification of which,

(check one)

1. ☒ is attached hereto.

2. ☐ was filed on _____ as
U.S. Application No. _____
and was amended on _____.

3. ☐ was filed on _____ as
PCT International Application No. _____
and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

Prior Foreign Application(s)

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) or (f), or §365(b) of any foreign application for patent or inventor's certificate listed below, or under §365(a) of any PCT international application which designated at least one country other than the United States listed below, and I have identified below, by checking the box, any foreign application for patent or inventor's certificate, or any PCT International application having a filing date before that of the application on which priority is claimed:

			Priority Not Claimed	Cert. Copy Attached
_____ (Application No.)	_____ (Country)	_____ (Filing Date)	☐	☐
_____ (Application No.)	_____ (Country)	_____ (Filing Date)	☐	☐

Power of Attorney

And I hereby appoint all practitioners who are associated with the Customer Number 024319 as my principal attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

BEST AVAILABLE COPY

Direct Correspondence To: **Customer Number 024319**

Direct Telephone Calls To: **Timothy Croll at telephone number (408) 433-8000**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Typewritten Full Name of Sole or First Inventor: MAURICE O. OTHIENO Citizenship: Kenya

Inventor's signature: Maurice Othieno **Date of Signature:** 4/5/2006

Residence: (City) Union City (State/Country) CA/USA

Post Office Address: 2473 Stanford St., Union City, CA 94587

Second Inventor: CHOK J. CHIA Citizenship: USA

Inventor's signature: **Date of Signature:** 4/5/2006

Residence: (City) Cupertino (State/Country) CA/USA

Post Office Address: 10132 Prado Vista Ave., Cupertino, CA 95014

Third Inventor: AMAR J. AMIN Citizenship: USA

Inventor's signature: **Date of Signature:** 4/5/2006

Residence: (City) Milpitas (State/Country) CA/USA

Post Office Address: 1001 S. Main St., Apt. #Q305, Milpitas, CA 94035

BEST AVAILABLE COPY

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875 Effective December 8, 2004

Application or Docket Number: 11-399-723

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	150.00		N/A	300.00
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	$250		N/A	$500
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	$100		N/A	$200
TOTAL CLAIMS (37 CFR 1.16(i))	25 minus 20 =	* 5	X$ 25 =		OR	X$50 =	250
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	* 0	X100 =			X200 =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			+180=			+360=	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1250.

APPLICATION AS AMENDED – PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

04/11/2006 DEMMANU1 00000007 122252 11399723

01 FC:1011	300.00	DA
02 FC:1111	500.00	DA
03 FC:1311	200.00	DA
04 FC:1202	250.00	DA

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-287/69033

CLAIMS

We claim:

Claim 1: A semiconductor integrated circuit (IC) package which comprises:

a substrate having a first surface and a second surface;

a first ground plane configured for electrical connection with low speed electronic circuitry;

a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate;

a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane configured for electrical connection with high speed electronic circuitry;

a plurality of additional electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate; and

peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package.

Claim 2: An IC package as recited in Claim 1 wherein the peripheral electrical contacts arranged on the substrate include:

a first set of electrical contacts spaced and configured for electrical connection with low speed electronic circuitry; and

a second set of electrical contacts spaced and configured for electrical connection with high speed electronic circuitry.

Claim 3: An IC package as recited in Claim 2 wherein the low speed electronic circuitry is defined as circuitry having serial transfer rates of less than about 1 Gigabits per second (Gb/s); and

wherein the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 1 Gb/s.

Claim 4: An IC package as recited in Claim 2 wherein the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 8.5 Gb/s.

Claim 5: An IC package as recited in Claim 2 wherein the second set of electrical contacts are spaced apart at a distance that is at least twice as far apart as the spacing for the first set of electrical contacts.

Claim 6: An IC package as recited in Claim 2 wherein the second set of electrical contacts are spaced apart at a distance that is at least three times as far apart as the spacing for the first set of electrical contacts.

Claim 7: An IC package as recited in Claim 2 wherein the second set of electrical contacts are spaced apart at a distance sufficient to establish a differential impedance of at least 100 ohms (Ω) between the contacts of the second set.

Claim 8: An IC package as recited in Claim 5 wherein the first set of electrical contacts are spaced apart a distance of at least 70 μm (micrometers) and wherein the second set of electrical are spaced apart a distance of at least 140 μm (micrometers).

Claim 9: An IC package as recited in Claim 5 wherein the first set of electrical contacts are spaced apart a distance of at least 70 μm (micrometers) and wherein the second set of electrical are spaced apart a distance of at least 200 μm (micrometers).

Claim 10: An IC package as recited in Claim 2 wherein the electrical contacts are arranged such that,

the spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance effective to substantially eliminate cross-talk between I/O lines for the low speed electronic circuitry; and

the spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance effective to substantially eliminate cross-talk between I/O lines for the high speed electronic circuitry.

Claim 11: An IC package as recited in Claim 10 wherein the electrical contacts are arranged such that,

the spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance of at least 50 Ω between the contacts of the first set of electrical contacts to substantially eliminate cross-talk between I/O lines for the low speed electronic circuitry; and

the spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100 Ω between the contacts of the second set of electrical contacts to substantially eliminate cross-talk between I/O lines for the high speed electronic circuitry.

Claim 12: An IC package as recited in Claim 10 wherein the electrical contacts are arranged such that,

the spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance of at least 50 Ω between the contacts of the first set of electrical contacts; and

the spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100 Ω between the contacts of the second set of electrical contacts.

Claim 13: An IC package as recited in Claim 2 wherein first surface of the substrate includes a die attachment surface having a die arrangement attached thereto,

the die arrangement being electrically connected to the first ground plane, the second ground plane, and the peripheral electrical contacts of the substrate.

Claim 14: An IC package as recited in Claim 13 wherein the die arrangement comprises a die having both high-speed electronic circuitry and low-speed electronic circuitry;

wherein the low-speed electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced and configured for connection with the low speed electronic circuitry; and

wherein the high-speed electronic circuitry is connected with the second ground plane and is electrically connected with the second set of electrical contacts that are spaced and configured for connection with the high speed electronic circuitry.

Claim 15: An IC package as recited in Claim 14 wherein the die arrangement comprises a stacked die arrangement wherein at least one die has high-speed electronic circuitry and wherein at least one die has low-speed electronic circuitry;

wherein the low-speed electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced and configured for connection with the low speed electronic circuitry; and

wherein the high-speed electronic circuitry is connected with the second ground plane and is electrically connected with the second set of electrical contacts that are spaced and configured for connection with the high speed electronic circuitry.

Claim 16: A semiconductor IC package as recited in Claim 1 wherein the substrate includes a plurality of layers, and wherein;

a first layer of the substrate includes,

the first ground plane, and

the second ground plane;

a second layer of the substrate includes,

a third ground plane configured for electrical connection with low speed electronic circuitry, and

a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the third ground plane configured for electrical connection with high speed electronic circuitry; and

at least one reference plane associated with each layer of the substrate and the ground planes included thereon.

Claim 17: A semiconductor integrated circuit (IC) package which comprises:

a substrate having a die attachment area and having a first ground plane arranged thereon configured for electrical connection with low speed electronic circuitry;

a plurality of electrical connections that electrically connect the first ground plane with electrical contacts that are to be connected with an external ground;

a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane configured for electrical connection with high speed electronic circuitry;

a plurality of additional electrical connections that electrically connect the second ground plane with electrical contacts that are to be connected with an external ground; and

electrical I/O contacts configured for connection with the die and enabling electrical connection of the package with external circuitry.

Claim 18: An IC package as recited in Claim 17 wherein the I/O contacts comprise:

a first set of I/O contacts spaced and configured for electrical connection with low speed electronic circuitry; and

a second set of I/O contacts spaced and configured for electrical connection with high speed electronic circuitry.

Claim 19: An IC package as recited in Claim 18 wherein the second set of I/O contacts are spaced apart at a distance sufficient to establish a differential impedance of at least 100 ohms (Ω) between the I/O contacts of the second set.

Claim 20: An IC package as recited in Claim 18 wherein,

the spacing between the contacts of the first set of first set of I/O contacts is arranged to be sufficient to establish a control differential impedance effective to substantially eliminate cross-talk between the first set of I/O contacts for the low speed electronic circuitry; and

the spacing between the contacts of the second set of I/O contacts is sufficient arranged to be sufficient to establish a control differential impedance effective to substantially eliminate cross-talk between I/O contacts for the high speed electronic circuitry.

Claim 21: An IC package as recited in Claim 18 wherein the low speed electronic circuitry is defined as circuitry having serial transfer rates of less than about 1 Gb/s; and

wherein the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 1 Gb/s.

Claim 22: An IC package as recited in Claim 17 wherein the package is configured as a ball grid array package.

Claim 23: An IC package as recited in Claim 17 wherein the package is configured as a flip chip package.

Claim 24: An IC package as recited in Claim 17 wherein the package is configured as a lead frame package.

Claim 25: An IC package as recited in Claim 17 wherein the package is configured as a leadless lead frame package.