

Modeling and Analysis of Power Distribution Networks for Gigabit Applications

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Abstract—As the operating frequency of digital systems increases and voltage swing decreases, it becomes very important to characterize and analyze power distribution networks (PDNs) accurately. This paper presents the modeling, simulation, and characterization of the PDN in a high-speed printed circuit board (PCB) designed for chip-to-chip communication at a data rate of 3.2 Gbps. The test board consists of transmitter and receiver chips wirebonded onto plastic ball grid array (PBGA) packages on a PCB. In this paper, a hybrid method has been applied for analysis which consists of the Transmission Matrix Method (TMM) in the frequency domain and Macromodeling method in the time domain. As an initial step, power/ground planes have been modeled using TMM. Then, the macromodel of the power/ground planes has been generated at the desired ports using macromodeling. Finally, the macromodel of the planes, transmission lines, and nonlinear drivers have been simulated in standard SPICE-based circuit simulators for computing power supply noise. In addition to noise computation, the self and transfer impedances of power/ground planes have been computed and the effect of decoupling capacitors on power supply noise has been analyzed. The methods discussed have been validated using hardware measurements.

Index Terms—Power distribution network, transmission matrix method, macromodeling, decoupling, power bus.

1 INTRODUCTION

OVER the last decade, the scaling of the CMOS transistor has enabled the design of microprocessors operating at multigigahertz frequencies. This trend, based on the International Technology Roadmap on Semiconductors (ITRS), is expected to continue over many years for both desktop and mobile computers. Along with the scaling of the transistor, the number of transistors on a chip is doubling every 18 months, based on Moore's law. In addition, long-haul communication bandwidth is estimated to be doubling every nine months, much faster than Moore's law. This has resulted in the integration of short range, low power communication technologies such as IEEE 802.11, Bluetooth, and Ultra Wide Band into mobile computers. Integration of these technologies has increased the data processing requirements and computing capabilities in mobile devices.

A combination of voltage scaling and Moore's law is causing an alarming increase in the power consumed by microprocessors. Since computers are broadband systems, the current needs to be supplied to the switching circuits over a broad frequency range from DC to at least the second

harmonic of the clock frequency. This trend in microprocessors is causing a major challenge for distributing power in computer systems. With voltage scaling and wireless integration in mobile computers, the tolerance to power supply noise is rapidly decreasing.

A major contribution to power supply noise is from the package and board level interconnections. Due to their distributed electrical characteristics, package and board interconnections can support electromagnetic waves in the power distribution network. These electromagnetic waves cause detrimental effects to the switching circuits such as excessive power supply noise and coupling. To minimize such noise behavior, prelayout analysis and postlayout verification of the power distribution network are necessary.

One of the most important areas in high-speed digital systems is the design and analysis of the power distribution network. The power distribution network supplies power to core logic and I/O circuits in any digital system. As clock speeds increase and signal rise time and supply voltages decrease, the transient currents injected into the power distribution planes can induce voltage fluctuations on the power distribution network [1]. This undesired voltage fluctuation on the power/ground planes is commonly known as switching noise or delta-I noise. Power supply noise leads to unwanted effects on the power distribution network (PDN) such as ground bounce, power supply compression, and electromagnetic interference. It has been shown that power supply noise induced by a large number of simultaneously switching circuits in a printed circuit board (PCB) or multichip module (MCM) can limit the performance of the system [2]. Therefore, the power distribution network should be designed to have a low impedance over the entire bandwidth of the signal so that

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the transient currents do not cause excess voltage noise on the power distribution network [3]. However, the design of the PDN to achieve this goal is difficult since modern CMOS microprocessors or Application Specific Integrated Circuits (ASICs) have thousands of drivers that switch simultaneously within a clock cycle. With the trend toward low voltage and low power signaling in mobile computers, the power supply can be a major bottleneck for the reliable functioning of the system.

For meeting the high bandwidth demands and low power requirements, digital technologies are quickly moving to gigabit data rate and subvoltage range signaling levels. To meet these requirements, Rambus has introduced the Yellowstone signaling technology utilizing a bidirectional 200 mV swing Differential Rambus Signaling Level (DRSL) with a data transfer rate starting at 3.2 Gbps/pair and scalable to 6.4 Gbps/pair [4], [5]. These very high operating frequencies and low voltage swing place increasing demands on the quality of the power distribution network. Therefore, accurate analysis of the PDN has become very critical for optimizing the performance of high-speed systems.

In the past, various numerical methods have been developed for the analysis of power distribution networks. Examples include Speed from Sigrity [6], [7], which is based on a Finite Difference Time Domain (FDTD) method, Transmission Line method [8], [9], which uses a two-dimensional array of transmission lines or distributed RLCG elements in SPICE, the cavity resonator method [10], [11], the Transmission Matrix Method (TMM) [12], [13], [14], and a circuit extraction approach based on the mixed-potential integral equation formulation (CEMPIE) method which is an extension of the partial element equivalent circuit approach [15]. It has been shown in [12] that the Transmission Matrix Method is very efficient for analyzing electrically large power/ground planes of irregular shape. Though TMM computes the frequency response of power/ground planes, the results have to be combined with transmission lines and nonlinear drivers for computing the power supply noise. The frequency to time translation has been demonstrated in [16] using broadband macromodels for multiport networks constructed from rational functions.

In this paper, a hybrid method that combines the Transmission Matrix Method (TMM) and Macromodeling method has been applied to the Rambus board for computing power supply noise. The output of this analysis is a methodology that is very useful for analyzing PDN in digital systems such as mobile computers, which is the primary contribution of this paper. Even though the method presented in this paper has been applied for postlayout verification, the method also lends itself to prelayout analysis. Here, the methods can be used to estimate the layer stack-up, layer assignment, decoupling strategies, power islands, etc. for meeting the power supply noise budget.

This paper is organized as follows: In Section 2, a modeling and simulation methodology for analyzing PDNs is described. This is followed by a description of the Transmission Matrix Method (TMM) in Section 3 and Macromodeling method in Section 4. In Section 5, the Rambus test vehicle is described in detail which includes

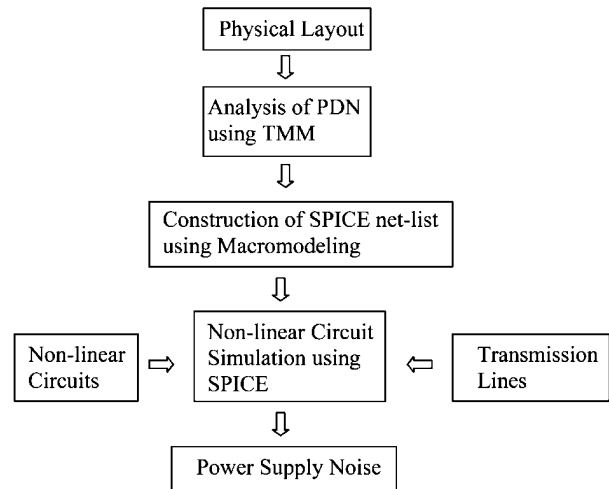


Fig. 1. Modeling and simulation methodology.

the layout and cross section. In Section 6, details on model to hardware correlation are provided on the Rambus board, followed by Section 7 where the modeling methodology is applied to the PDN of the Rambus test vehicle using the Transmission Matrix Method. In Section 8, the frequency response of the PDN is approximated using macromodels and combined with nonlinear drivers and transmission lines for computing power supply noise. Finally, the conclusion is provided in Section 9.

2 MODELING AND SIMULATION METHODOLOGY

Computation of power supply noise requires the simulation of nonlinear drivers in the presence of nonideal supply voltages. The voltages to the nonlinear drivers are supplied through the PDN from the voltage regulator modules on the PCB. The PDN typically contains power/ground planes and decoupling capacitors attached together using numerous vias for high frequency applications. The PDN is best analyzed and designed in the frequency domain [14]. However, the power supply noise is a transient phenomenon that needs to be computed in the time domain. The power supply noise is affected by the nonlinearity of the drivers. Hence, for understanding the impact of power supply noise on system performance, a hybrid method is required whereby nonlinear drivers can be simulated in the time domain with the frequency response of the PDNs.

Recently, a hybrid method for analyzing PDN was proposed in [17]. This methodology preserves the accuracy of field simulators and concurrently improves the computational efficiency for the analysis of the entire system. First, the frequency response, such as impedance, is computed using the Transmission Matrix Method. Then, a black box representation of the PDN is generated at the desired ports using macromodeling. The macromodel can be synthesized into SPICE net-lists and combined with drivers for enabling nonlinear circuit simulation. Finally, the macromodel of the PDN, nonlinear drivers, and transmission lines are simulated in conventional circuit simulators like SPICE. In Fig. 1, this methodology is shown. This paper presents the details of this methodology for analyzing PDNs in complex systems.

The Transmission Matrix Method offers a very efficient technique for analyzing realistic power distribution networks [12], [13], [14]. Using the property that power distribution networks in the package and board can be represented as a cascade of unit cells consisting of distributed and repeated RLCG circuit elements, the multi-input/multi-output Transmission Matrix Method can be used to simulate arbitrarily shaped, electrically large structures efficiently. Since the Transmission Matrix Method is based on a multi-input/multi-output transfer function, the response of the PDN at specific ports can be computed by multiplying the individual square matrices. Once the matrix of the overall network is computed, it can be converted into a scattering matrix (S), an admittance matrix (Y), or an impedance matrix (Z) at specific points on the network. Therefore, while retaining the same size of the matrix for the overall network, the Transmission Matrix Method provides the flexibility for analyzing large networks containing up to 20 power/ground plane pairs with relative ease. The salient features of the method are that it requires small memory and the CPU time scales linearly as the number of power/ground planes are increased. The Transmission Matrix Method has been used in this paper for computing the frequency response of the PDN.

The distributed behavior of interconnects at either the chip or package level can be extracted in the frequency domain from an electromagnetic simulation or measurements. The response of the structure is available as frequency-dependent data that represents the scattering (S), admittance (Y), or impedance (Z) parameters. This information can be represented as a black box, which can be used to capture the behavior of the structure at the input/output ports. This black box representation of passive circuits can be modeled using macromodels based on rational functions. The macromodels can be combined with a larger circuit by synthesizing SPICE net-lists for time domain simulation. In [16], passivity of the macromodels has been satisfied using multiport passivity formulae derived from the pole-residue form of the rational functions. Broadband macromodels having hundreds of poles and residues have been constructed using three methods, namely,

1. the frequency slicing method, which divides the computational domain into subdomains,
2. the frequency sliding method, which enables the movement of the subdomain along the frequency axis, and
3. a drop-pick method, which helps improve the accuracy of the macromodels.

These methods have been applied in this paper for representing the frequency response of PDNs using macromodels.

3 TRANSMISSION MATRIX METHOD (TMM)

Power/ground planes represent large metal layers separated by a small dielectric distance, as shown in Fig. 2. Due to the small dielectric distance, power/ground planes in the package and PCB are capacitive at low frequencies and are therefore ideal for supplying power to the integrated

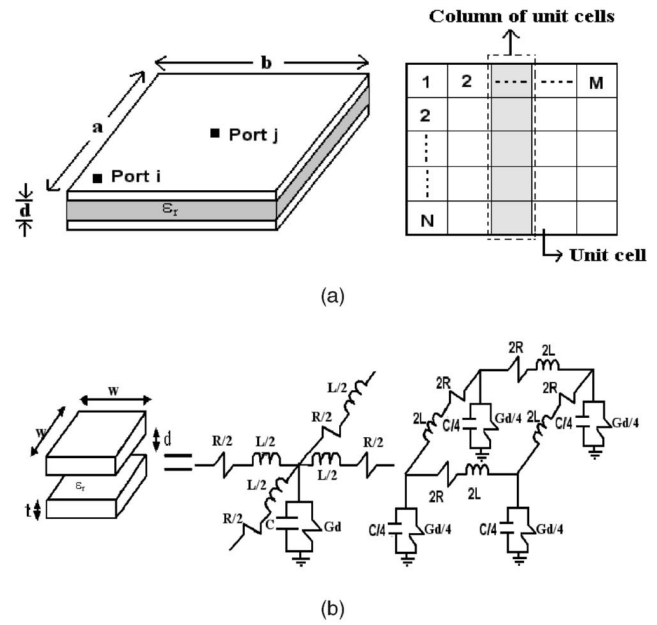


Fig. 2. (a) Plane pair structure. (b) Unit cell and equivalent circuit (T and Π models).

circuits. However, with an increase in frequency, planes become inductive and resonate at discrete frequencies [1]. Integrated circuits that trigger these resonances can result in large voltage variations on the PDNs. Hence, power/ground planes need to be carefully analyzed based on the frequency response. Since power/ground planes are electrically large structures, their analysis is nontrivial.

Power/ground planes can be divided into unit cells, as shown in Fig. 2, and represented using a lumped element model for each cell, as described in [18]. The lumped element model parameters are computed from the physical structure. Each cell consists of an equivalent circuit with R, L, C, and G components, as shown in Fig. 2 for a rectangular structure. Each unit cell can be represented using either a T or Π model [19], [20], as shown in the figure. The primary difference between these two models is an offset of half a unit cell between each other. Both models lead to similar results, as discussed in [12]. The equivalent circuit parameters for a unit cell can be derived from quasi-static models provided the dielectric separation (d) is much less than the metal dimensions (a, b) [21], which is true for power/ground plane pairs. From the lateral dimension of a unit cell (w), separation between planes (d), dielectric constant (ϵ), loss tangent of dielectric ($\tan(\delta)$), metal thickness (t), and metal conductivity (σ_c), the equivalent circuit parameters of a unit cell can be computed as:

$$\begin{aligned}
 C &= \epsilon_o \epsilon_r \frac{w^2}{d} \\
 L &= \mu_o d \\
 R_{dc} &= \frac{2}{\sigma_c t} \\
 R_{ac} &= 2 \sqrt{\frac{\pi f \mu_o}{\sigma_c}} (1 + j) \\
 G_d &= \omega C \tan(\delta).
 \end{aligned} \tag{1}$$

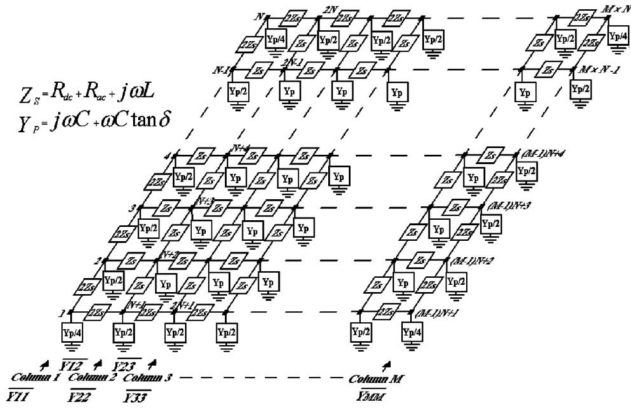


Fig. 3. Equivalent circuit for a pair of power/ground planes.

In the above equation, ϵ_0 is the permittivity of free space, μ_0 is the permeability of free space, and ϵ_r is the relative permittivity of the dielectric. The parameter R_{dc} is the resistance of both the power and ground planes for a steady DC current, where the planes are assumed to be of uniform cross-section. The AC resistance R_{ac} accounts for the skin effect on both conductors. The shunt conductance G_d represents the dielectric loss in the material between the planes.

By approximating the unit cell, a distributed network of RLCG elements can be generated for rectangular planes, as shown in Fig. 2. Using a distributed network of RLCG elements, each rectangular plane pair can be divided into $(M-1) \times (N-1)$ unit cells. The $(M-1) \times (N-1)$ unit cells can be represented as a $2(M \times N) \times 2(M \times N)$ matrix formed by $(M \times N)$ input ports and $(M \times N)$ output ports. This is shown in Fig. 3 for the Π equivalent circuit for the unit cells, which are cascaded to represent a pair of power/ground planes shown in Fig. 2. From Fig. 3, the input ports are indexed as 1 to $(M \times N)$ and the output ports are indexed as $(M \times N) + 1$ to $2(M \times N)$. The transmission matrix for the $2(M \times N)$ port network can be derived in terms of the node voltages and port currents. Using the 2×2 block matrix representation, the transmission matrix can be represented to relate the voltages and currents as:

$$\begin{aligned} \overline{V}_{in} &= [A_p] \overline{V}_{out} + [B_p] \overline{I}_{out} \\ \overline{I}_{in} &= [C_p] \overline{V}_{out} + [D_p] \overline{I}_{out}, \end{aligned} \quad (2)$$

where

$$\begin{aligned} \overline{V}_{in} &= \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_{M \times N} \end{bmatrix} \quad \overline{I}_{in} = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{M \times N} \end{bmatrix} \\ \overline{V}_{out} &= \begin{bmatrix} V_{M \times N + 1} \\ V_{M \times N + 2} \\ \vdots \\ V_{2(M \times N)} \end{bmatrix} \quad \overline{I}_{out} = \begin{bmatrix} I_{M \times N + 1} \\ I_{M \times N + 2} \\ \vdots \\ I_{2(M \times N)} \end{bmatrix}. \end{aligned}$$

The above transmission matrix for a power/ground plane pair can be rewritten in the simpler form:

$$T_p = \begin{bmatrix} A_p & B_p \\ C_p & D_p \end{bmatrix} = \begin{bmatrix} I & 0 \\ C_p & I \end{bmatrix}, \quad (3)$$

where $[I]$ is the identity matrix, $[0]$ is the null matrix, and $[C_p]$ represents $(M \times N) \times (M \times N)$ matrices. In (3), the matrix $[C_p]$ is of the form

$$[C_p] = \begin{bmatrix} \bar{Y}_{11} & -\bar{Y}_{12} & 0 & 0 & \cdots \\ -\bar{Y}_{12} & \bar{Y}_{22} & -\bar{Y}_{23} & 0 & \cdots \\ 0 & -\bar{Y}_{23} & \bar{Y}_{33} & -\bar{Y}_{34} & \cdots \\ \vdots & \vdots & \vdots & \vdots & \cdots \\ 0 & 0 & 0 & 0 & \cdots \bar{Y}_{MM} \end{bmatrix}, \quad (4)$$

where

$$\bar{Y}_{11} = \bar{Y}_{MM} = 0.5\bar{Y}_{22} = 0.5\bar{Y}_{33} = \cdots = 0.5\bar{Y}_{(M-1)(M-1)} =$$

$$\begin{bmatrix} \frac{Y_p}{4} + \frac{1}{Z_s} & -\frac{1}{2Z_s} & 0 & \cdots & 0 & 0 \\ -\frac{1}{2Z_s} & \frac{Y_p}{2} + \frac{2}{Z_s} & -\frac{1}{2Z_s} & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \cdots & \ddots & \frac{Y_p}{2} + \frac{2}{Z_s} & -\frac{1}{2Z_s} \\ 0 & 0 & \cdots & -\frac{1}{2Z_s} & \frac{Y_p}{4} + \frac{1}{Z_s} \end{bmatrix}$$

$$\bar{Y}_{12} = \bar{Y}_{23} = \cdots = \bar{Y}_{(M-1)M} =$$

$$\begin{bmatrix} \frac{1}{2Z_s} & & & & 0 \\ & \frac{1}{Z_s} & & & \\ & & \ddots & & \\ & & & \frac{1}{Z_s} & \\ 0 & & & & \frac{1}{2Z_s} \end{bmatrix}.$$

As can be seen in (4), the transmission matrix for a power/ground pair is tridiagonal and sparse, which enables reduction in memory usage and CPU runtime when this method is applied to realistic structures [14].

The matrix computation in (2), (3), and (4) can be further reduced to compute the frequency response at specific ports in the network [14]. For irregular structures, the structure can be approximated using a rectangular array of unit cells where the nonmetallic areas are padded with zero matrix elements [12].

4 MACROMODELING METHOD

Using rational functions, the frequency response $H(s)$ of any time-invariant linear passive network can be represented as:

$$H(s) = \frac{\sum_{ns=0}^{NS} a_{ns}s^{ns}}{\sum_{ds=0}^{DS} b_{ds}s^{ds}}, \quad (5)$$

where $s = j\omega$, ω is the angular frequency in radians per second, and

$$[a] = [a_0 \quad a_1 \quad \cdots \quad a_{NS}]^T$$

and $[b] = [b_0 \ b_1 \ \dots \ b_{DS}]^T$ are unknown real coefficient vectors. In (5), $H(s)$ can be the scattering, admittance, or impedance parameters generated from an electromagnetic simulation or measurements. The goal of solving (5) is to represent $H(s)$ as a rational function by computing the orders of the numerator and denominator, NS and DS , respectively, and the real coefficient vectors $[a]$ and $[b]$. In (5), $H(s)$ could be the frequency response of the PDN computed using the Transmission Matrix Method. For a linear time invariant system, the transfer function $H(s)$ should be stable and passive [22]. Stability of the macromodel requires that the poles of the transfer function in (5) are on the left half of the s -plane. The passivity of the macromodel implies that $H(s)$ is a positive definite matrix for all frequencies which can be represented as:

$$\text{Re}[H(s = j\omega)] \geq 0 \quad \forall \omega. \quad (6)$$

The stability and passivity conditions are necessary and sufficient conditions for representing Linear Time Invariant (LTI) systems.

The basic idea used in this paper for the construction of passive macromodels for a LTI system is that the sum of passive subnetworks results in a passive system. Equation (5) can be generalized for a distributed multiport network containing common poles in a pole-residue form as [22]:

$$[H(s)] = \sum_{n=1}^{CPN/2} \frac{2[\alpha_n](s - p_{nr}) - 2[\beta_n]p_{ni}}{(s - p_{nr})^2 + p_{ni}^2} + \sum_{m=1}^{RPN} \frac{[\gamma_m]}{s - p_{mr}} + [\delta] + [\eta]s, \quad (7)$$

which can be represented as

$$[\phi_n] = \begin{bmatrix} \phi_n^{11} & \dots & \phi_n^{1P} \\ \vdots & \ddots & \vdots \\ \phi_n^{P1} & \dots & \phi_n^{PP} \end{bmatrix},$$

where $[\phi]$ is a $P \times P$ matrix for a P -port network that represents the residues $[\alpha]$, $[\beta]$, $[\gamma]$, $[\delta]$, and $[\eta]$. The orders CPN and RPN represent the number of complex conjugate poles and real poles, respectively. For satisfying the passivity of a P -port network, the rational function matrix $[H(s)]$ in (7) has to be a positive definite matrix. Using the property for positive definiteness, multiport passivity formulae derived from the pole-residue form can be represented as [16]:

$$\begin{aligned} \text{eigenvalues of } -[\alpha_n]_{P \times P} p_{nr} \pm [\beta_n]_{P \times P} p_{ni} &\geq 0 \\ \text{eigenvalues of } [\gamma_m]_{P \times P} &\geq 0 \\ \text{eigenvalues of } [\delta]_{P \times P} &\geq 0. \end{aligned} \quad (8)$$

In (8), the passivity formulae are only enforced on each subnetwork of $[H(s)]$. The passivity formulae only depend on the poles and residue matrices, which are independent of frequency. Hence, the passivity of the circuit is satisfied over infinite frequency. There are no constraints enforced on the residue matrix $[\eta]$.

Since passivity formulae are only enforced on each subnetwork, there is no relationship for passivity between subnetworks except that they contribute to the overall

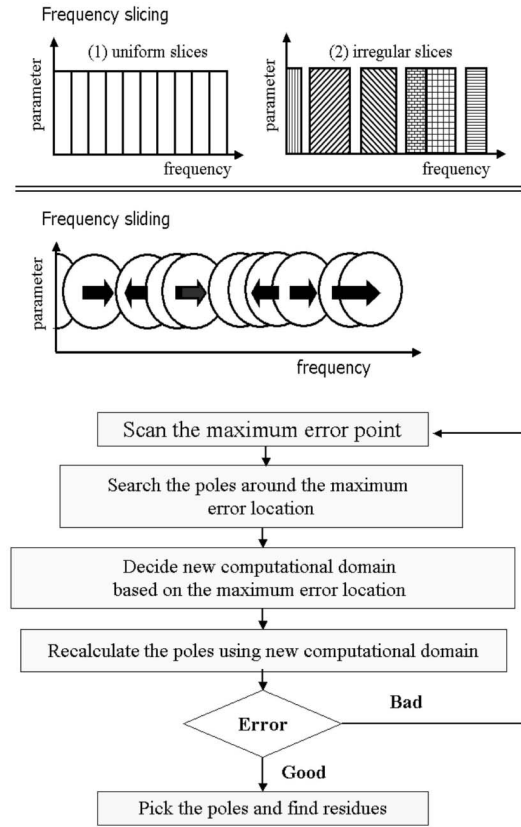


Fig. 4. Frequency slicing, sliding method, and drop-pick method.

response of the macromodels. This enables the entire frequency response to be divided into subbands for the construction of broadband macromodels. The basic idea for the construction of broadband macromodels is that, if complex conjugate poles and real poles can be extracted from a localized region of the frequency response, then the original frequency response can be divided into subcomputational domains (subbands), where local poles can be extracted. A subband is a set of sampled frequency data that can be regularly or irregularly divided over the entire computational domain, as shown in Fig. 4. The size and number of subbands depends on the nature of the frequency response. Though the frequency slicing method divides the computational domain into subbands and enables the efficient extraction of poles within a subband, it may miss the poles at the boundary between the subbands or generate spurious poles within the subband. This paper uses a drop-pick method to improve the accuracy of the constructed macromodels, as shown in Fig. 4, with further details available in [16].

In this paper, broadband macromodels having hundreds of poles and residues have been constructed using three methods, namely,

1. the frequency slicing method, which divides the computational domain into subdomains,
2. the frequency sliding method, which enables the movement of the subdomain along the frequency axis, and

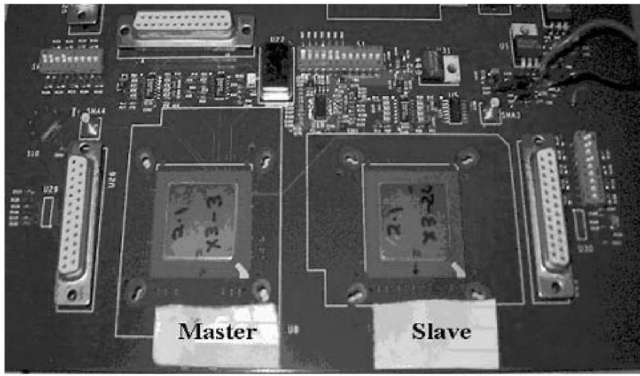


Fig. 5. Yellowstone test vehicle from Rambus.

3. a drop-pick method, which helps improve the accuracy of the macromodels.

The passivity of the macromodels has been satisfied using (8).

5 TEST VEHICLE DESCRIPTION

This section describes the test vehicle used for PDN analysis and for computing power supply noise. The Yellowstone test vehicle from Rambus consists of transmitter and receiver chips wirebonded onto plastic ball grid array (PBGA) packages on a PCB. The PBGA packages are directly attached to the board using solder balls or using sockets. This test vehicle is shown in Fig. 5.

The board is a six layer PCB that is 12.8 inches by 9.5 inches in size and consists of six layers, as shown in Fig. 6. In this figure, the PCB consists of two voltage planes, two ground planes, and two signal layers. Layer 3 is a voltage plane that provides 5 V to the peripherals on the board. It also has two irregularly shaped power islands of 1.2 V, master and slave sections, to supply voltage to the transmitter and receiver chips on the board, respectively, as shown in Fig. 7. Layer 4 is a 1.2 V split plane which serves the master and slave sections and includes a small island at the center with 3.3 V to supply voltage to the clock generation chip, as shown in Fig. 7. The purpose of the split plane is to monitor the power drawn by each subsystem. These two split planes are connected using a jumper. Layers 2 and 5 are continuous ground planes. Layers 1 and 6 are signal layers for low and high-speed

interconnects, respectively, as shown in Fig. 7. The low-speed signal transmission lines are single ended and their characteristic impedances are designed for 50 Ω using trace width of 7 mils and 18 mils spacing. The high-speed signal nets are differential and are designed with 6 mils width and 11.5 mils spacing. The differential traces have been designed to provide a 100 Ω differential impedance. The signal trace thickness on layer 1 and layer 6 is 0.7 mil. There are three ferrite beads on the board. All the ferrite beads are attached on the top surface next to the voltage regulators. One ferrite bead has been used for each supply (i.e., 1.2 V, 3.3 V, and 5 V). The purpose of the ferrite bead is to isolate the power planes from any power supply noise. For example, the ferrite bead is placed on the 1.2 V external supply in layer 1 to ensure that the 1.2 V supply that is being fed to the two islands is clean and free of any power supply noise from other sources. After the ferrite bead, the 1.2 V is split into the master and slave supply in layer 3 through vias [23].

The dielectric material of the PCB is FR4 with a relative permittivity, $\epsilon_r = 4.5$, the conductor is copper with conductivity, $\sigma_c = 5.8 \times 10^7$ S/m, and dielectric loss tangent, $\tan(\delta) = 0.02$ at 1 GHz. The copper thickness for layer 1 and layer 6 is 0.75 mil and copper thickness for other layers is 1.5 mils.

6 MODEL TO HARDWARE CORRELATION

To check the accuracy of the Transmission Matrix Method, the frequency response of the plane pair consisting of layers 4 and 5 were analyzed. The physical layout of layer 4 is shown in Fig. 8, which consists of two planes separated around the midsection. In the test vehicle, layers 4 and 5 contained decoupling capacitors which could either be soldered or removed. Hence, the frequency response of the plane pair could be measured with and without decoupling capacitors. For all cases, the frequency response was measured at locations C238 ($x = 2712.5$ mils, $y = 5687.5$ mils) and C217 ($x = 2712.5$ mils, $y = 687.5$ mils) on the master section, as shown in Fig. 8. These locations represented decoupling capacitor locations where pads were available for probing the power/ground plane.

The Transmission Matrix Method was used to calculate self-impedances at ports C238, C217, and transfer impedance

Layer 1	0.5 Oz Copper	Top (low-speed transmission lines)
4.5 mils		
Layer 2	1 Oz Copper	Gnd
4.8 mils		
Layer 3	1 Oz Copper	Vdd (5 V and 1.2 V islands)
92.2 mils		
Layer 4	1 Oz Copper	Vdd (3.3 V island and 1.2 V split plane)
4.8 mils		
Layer 5	1 Oz Copper	Gnd
4.5 mils		
Layer 6	0.5 Oz Copper	Bottom (high-speed transmission lines)

Fig. 6. The cross section of the PCB.

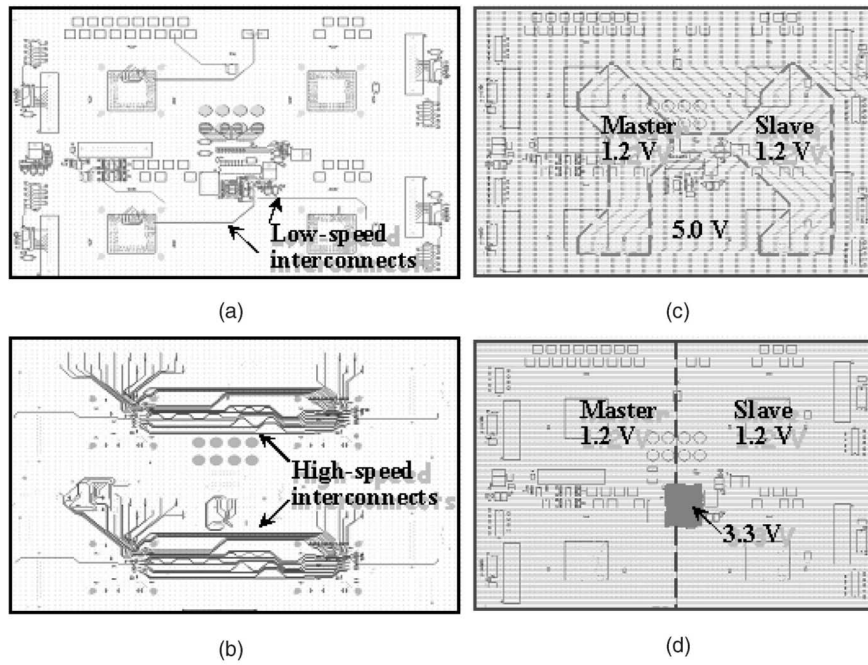


Fig. 7. The power and signal plane layers of the PCB. (a) Layer 1: signal layer for low-speed signal transmission lines. (b) Layer 6: signal layer for high-speed signal transmission lines. (c) Layer 3: power layer (5 V and 1.2 V master and slave islands). (d) Layer 4: power layer (1.2 V split plane and 3.3 V island).

between ports C288 and C217. The planes were approximated as rectangular planes without any loss in accuracy. To verify the accuracy of the Transmission Matrix Method, various measurements using Vector Network Analyzer (VNA) were performed. The model to hardware correlation results for the bare board (no decoupling capacitors) are shown in Fig. 9 from 10 MHz to 6 GHz. From the figure, transfer impedance Z_{12} (dashed line) shows good model to hardware correlation. However, self-impedances Z_{11} (dashed line) and Z_{22} (dashed line) show a large discrepancy between modeling and measurement. This is due to the pad inductance and resistance, which were not included in the initial model.

The importance of the pad inductance and resistance on the frequency response of power/ground planes can be explained using Fig. 10. In this figure, the frequency response of the plane pair is represented as a black box. The resistance and inductance at the input and output ports are due to pads which are added in series to the power/ground planes. Hence, in Fig. 10, the relationship between the measured voltages and currents can be written as:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} + R_1 + j\omega L_1 & Z_{12} \\ Z_{21} & Z_{22} + R_2 + j\omega L_2 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \quad (9)$$

In (9), the pad parasitics only affect the self-impedance, but not the transfer impedance of the power/ground planes.

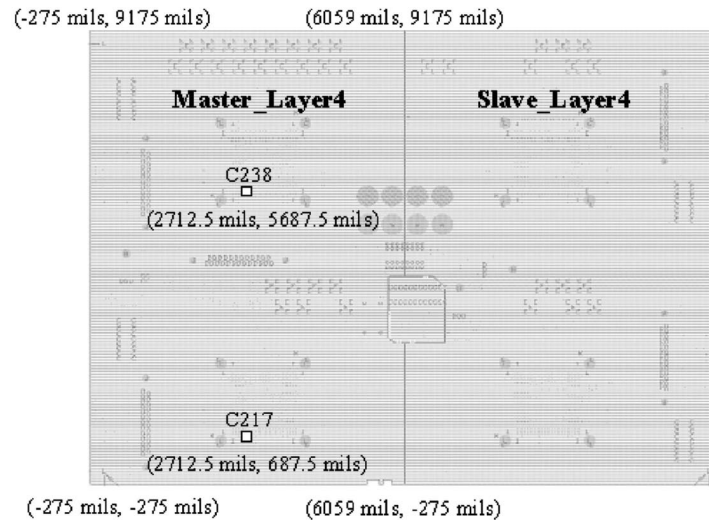


Fig. 8. Locations of C217 and C238 sites on layer 4.

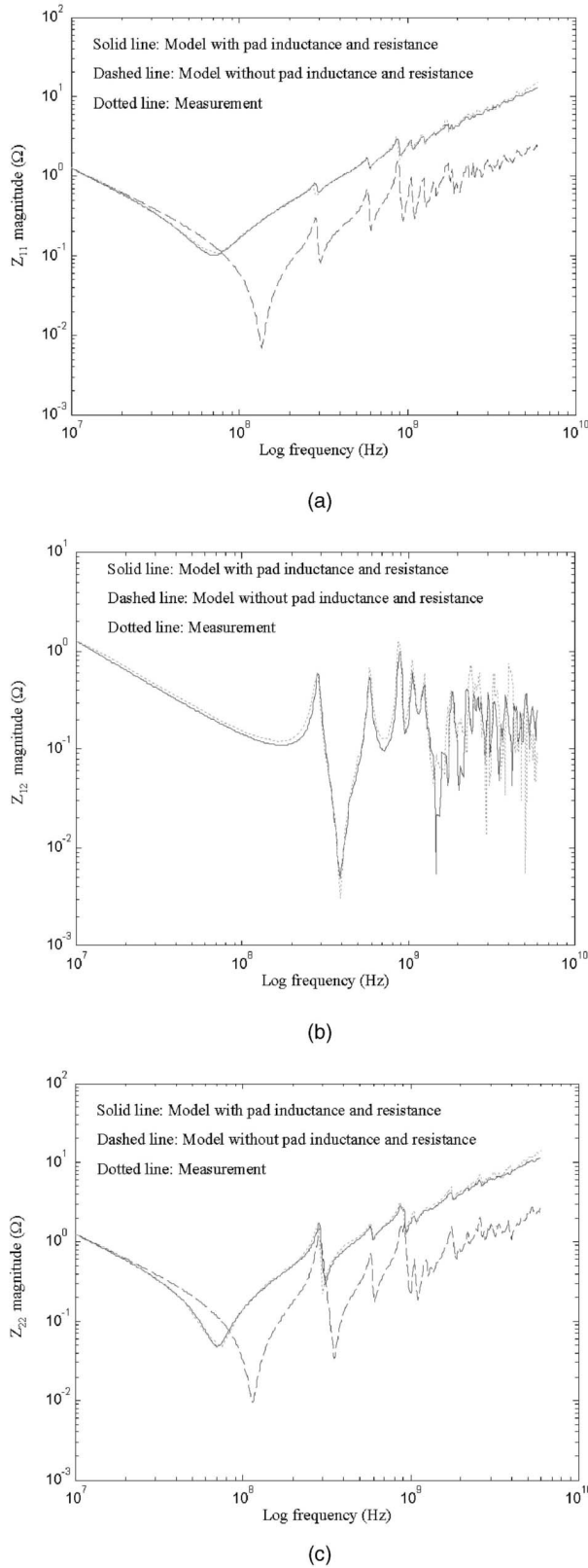


Fig. 9. Model to hardware correlation with and without pad parasitics. (a) Self-impedance at port C238. (b) Transfer impedance between port C238 and port C217. (c) Self-impedance at port C217.

Hence, it is important to note that self-impedances are very sensitive and require accurate calibration and, consequently, transfer impedance measurements are more reliable.

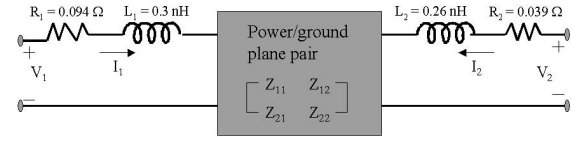


Fig. 10. Modified equivalent network of the power/ground planes.

Since the Transmission Matrix Method is a circuit-based formulation, the pad parasitics can be added to the model, with ease. With the pad parasitics added, the modeling results for self-impedances (Z_{11} and Z_{22} ; solid line) at port C238 and port C217 and transfer impedance (Z_{12} ; solid line) between port C238 and port C217 were compared with measurement results (dotted lines) between 10 MHz and 6 GHz in Fig. 9. These results show very good correlation between modeling and measurement results.

Next, the effects of decoupling capacitors on transfer impedance were investigated. The decoupling capacitors with value of 100 nF were placed at different locations on the board. The equivalent series inductance (ESL) and equivalent series resistance (ESR) of the decoupling capacitors were 0.55 nH and 0.02 Ω , respectively. The model to hardware correlations with decoupling capacitors are shown in Fig. 11. The first null frequency and magnitude of transfer impedances are affected, as can be seen in Fig. 11.

This can be explained using the schematic in Fig. 12, which shows a capacitor represented as a series RLC circuit connected to the power/ground planes. The static capacitance of 12.5 nF between planes is shown in the figure. For a single decoupling capacitor, the self-resonant frequency (SRF) is given as

$$\text{SRF} = \frac{1}{2\pi\sqrt{L_{\text{total}} C_{\text{cap}}}} \cong 16.57 \text{ MHz},$$

where

$$L_{\text{total}} = 0.923 \text{ nH} = L_{\text{cap}}(\text{ESL of decoupling capacitor}) + L_{\text{pad}}(\text{inductance of pad connected to decoupling capacitor})$$

and C_{cap} (capacitance of decoupling capacitor) = 100 nF. The impedance magnitude at the SRF represents the ESR of the decoupling capacitor. If the capacitance between power and ground layers is minimal and $C_{\text{cap}} \gg C_{\text{plane}}$, where C_{plane} (plane capacitance) = 12.5 nF, the parallel resonant frequency (PRF) can be approximated as

$$\text{PRF} = \frac{1}{2\pi\sqrt{L_{\text{total}} C_{\text{plane}}}} \cong 46.86 \text{ MHz}.$$

In Fig. 11a, the addition of a decoupling capacitor results in a first null at 16.57 MHz, while the first peak occurs at 46.86 MHz. Fig. 11b shows the transfer impedance magnitude when two decoupling capacitors are attached. In this case, the first null remains at the same location, while the first peak moves to a higher frequency. This is due to the doubling in the capacitance and reduction in the inductance to half its original value which does not change the SRF but increases the PRF. Both Figs. 11a and 11b show good model to hardware correlation. In Fig. 11c, all the decoupling

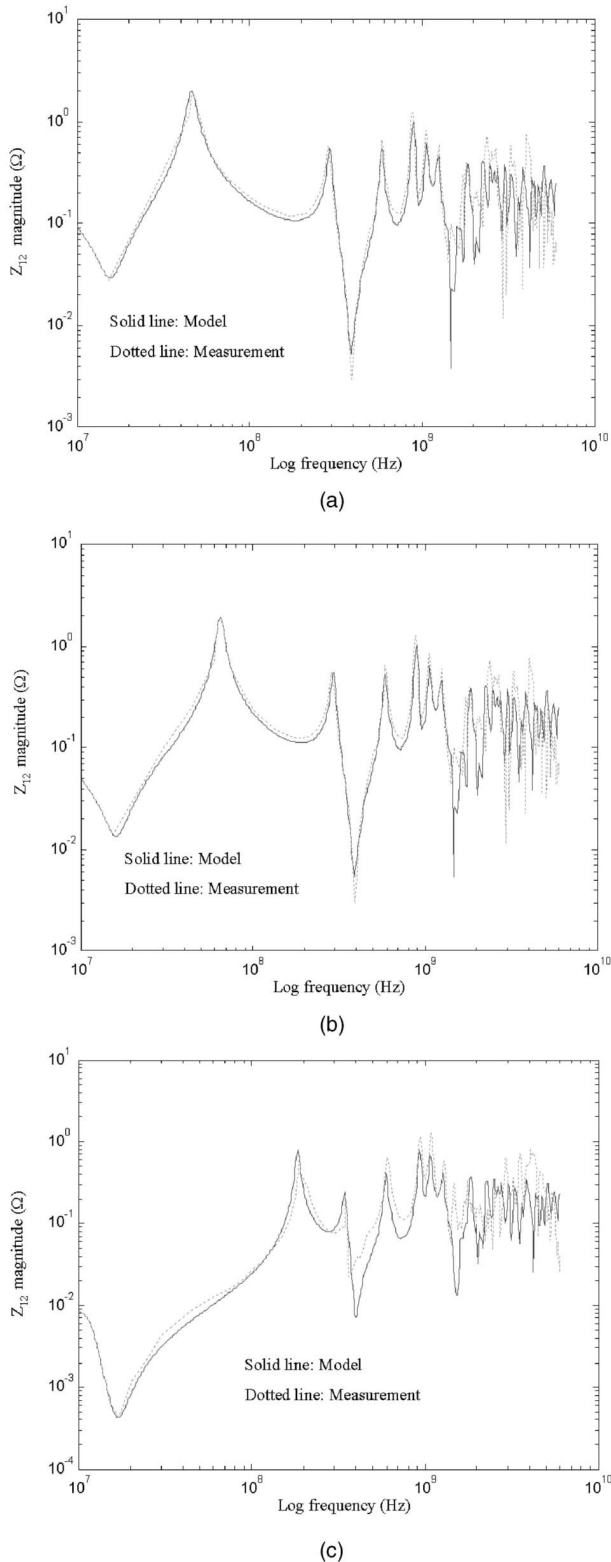


Fig. 11. Model to hardware correlation of transfer impedances between port C238 and port C217 in layer 4 and layer 5 in the PCB. (a) Transfer impedance between port C238 and C217 with a decoupling capacitor. (b) Transfer impedance with two decoupling capacitors. (c) Transfer impedance with 20 decoupling capacitors.

capacitors (20) on the PCB were added and the results still show good model to hardware correlation, validating the accuracy of the Transmission Matrix Method for modeling

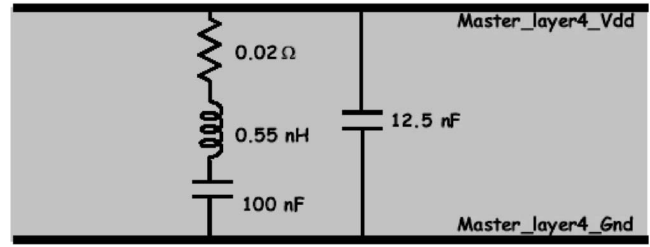


Fig. 12. Model of power/ground plane pair with a decoupling capacitor.

power/ground planes up to high frequencies. From Fig. 11, the addition of 20 decoupling capacitors results in very low impedance up to 100 MHz. In Fig. 11, the peaks in the frequency response are produced by standing wave resonances which are undesirable [10].

It is important to note that the measured results in Fig. 9 and Fig. 11 are for loaded boards containing many nonidealities. Hence, the correlation between modeling and measurements in Fig. 9 and Fig. 11 is considered to be quite good, even though the results do not show exact correlation at higher frequencies.

7 MASTER-SLAVE POWER DISTRIBUTION NETWORK

In the previous section, though layers 4 and 5 were modeled, these represented dummy layers that were used for checking the accuracy of the Transmission Matrix Method. In reality, layers 2 and 3 were used to supply power to the master and slave chips, as shown in Fig. 7. Layer 2 represented a continuous ground plane, while a split plane structure was used in layer 3 for Vdd, as shown in Fig. 13. The two islands on the master and slave sections were connected to a 1.2 V small narrow strip power island and a 1.2 V voltage regulator in layer 1 through 7 vias, as shown in Fig. 13. A ferrite bead of inductance 120 nH was used to filter any power supply noise, as shown in Fig. 13. There were 48 decoupling capacitors on the master and slave power islands in layer 3.

Three ports were defined on the PDN, as shown in Fig. 13, to represent the positions of the voltage regulator (port 1), Master chip (port 2), and Slave chip (port 3). Though additional ports could be used to represent the chip, no major change in the frequency response was observed with additional ports. All the voltages at the ports were defined between the voltage and ground planes, with coordinates as shown in Fig. 13.

The irregular structure shown in Fig. 13 was modeled using the Transmission Matrix Method. A rectangular grid was used, as shown in Fig. 13, with a unit cell size of $0.385 \text{ cm} \times 0.385 \text{ cm}$, which corresponds to an electrical size of $\lambda/13$ at 6 GHz. This resulted in 1,087 unit cells for approximating the structure which included the narrow rectangular strip on layer 1, voltage regulator on layer 1, the continuous ground plane on layer 2, and the split plane in layer 3, as shown in Fig. 13. The seven vias connecting layers 1 and 3 were represented as short circuits and modeled in TMM by enforcing the continuity of the currents and voltages at these sections. TMM was used to

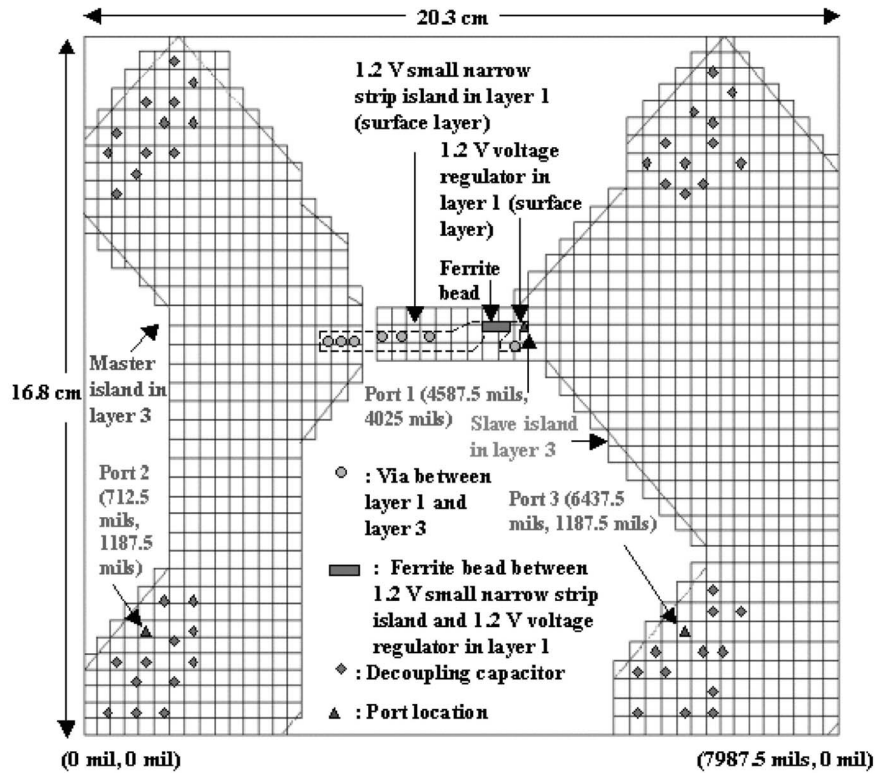


Fig. 13. Modeling of master and slave islands.

compute the 3×3 impedance matrix which provides the self and transfer impedance at the three port locations.

The transfer impedance of the master and slave sections in layer 3 was simulated across the master and slave split sections from 10 MHz to 6 GHz. In addition, the self-impedances of the master and slave sections were computed. The self-impedance within the master and within the slave sections remains almost identical, as shown in Fig. 14a. The self-impedance (Z_{11}) seen from the voltage regulator shows higher impedance than either Z_{22} or Z_{33} . This is because a narrow strip was used to supply the charge to the switching circuits in layer 1. The narrow strip has smaller capacitance, larger inductance, and, therefore, larger impedance. In Fig. 14b, the transfer impedance between the master and slave split sections shows little coupling at low frequencies since separate islands were used to supply power to the master and slave sections. However, substantial coupling between the master and slave sections was observed at high frequencies even though these sections were separated. This is because the narrow strip from the voltage regulator was used to maintain the same potential on the two islands using vias. This induces capacitive coupling between the two islands. When the two islands resonate, they couple energy through the coupling capacitance. This kind of behavior can be explained using a simple equivalent circuit, as shown in Fig. 15. In this figure, 2.5 nH of inductance is the spreading inductance from the decoupling capacitor to the master and slave chips. Each chip has 12 capacitors in parallel and this effect results in a small impedance at low frequencies. The circuit in Fig. 15 generates a null at 21.47 MHz and a peak at

512.15 MHz, similar to the coupling shown in Fig. 14. Hence, isolated islands can couple energy at high frequencies, which is a detrimental effect for low voltage signaling methods.

8 MODELING AND ANALYSIS OF POWER SUPPLY NOISE

Three-port impedance parameters from 10 kHz to 6 GHz, as shown in Fig. 14, were generated using the Transmission Matrix Method. These were converted to admittance parameters which were used as input to the macromodeling program. Using the frequency slicing and sliding method coupled with the drop-pick method described earlier, the frequency response was divided into irregular subbands. This was because the admittance parameters had highly unbalanced amplitude which varied from 7.4498×10^{-9} to 227.6 [mho] from DC to 6 GHz. After applying the macromodeling method, the number of complex conjugate poles and real poles extracted were 150 and 4, respectively. Common poles were used to represent the 3×3 impedance matrix. The comparison between the macromodels and the input Y-parameters is shown in Fig. 16 for Y_{22} and Y_{23} . From this figure, the extrapolation of the macromodel beyond 6 GHz shows smooth behavior, indicating the stability of the macromodel up to infinite frequency. In addition, the results show good agreement between the input data and the macromodel.

The comparison between three eigenvalues from input data and the frequency response of the constructed macromodel over a 6 GHz bandwidth is shown in Fig. 17.

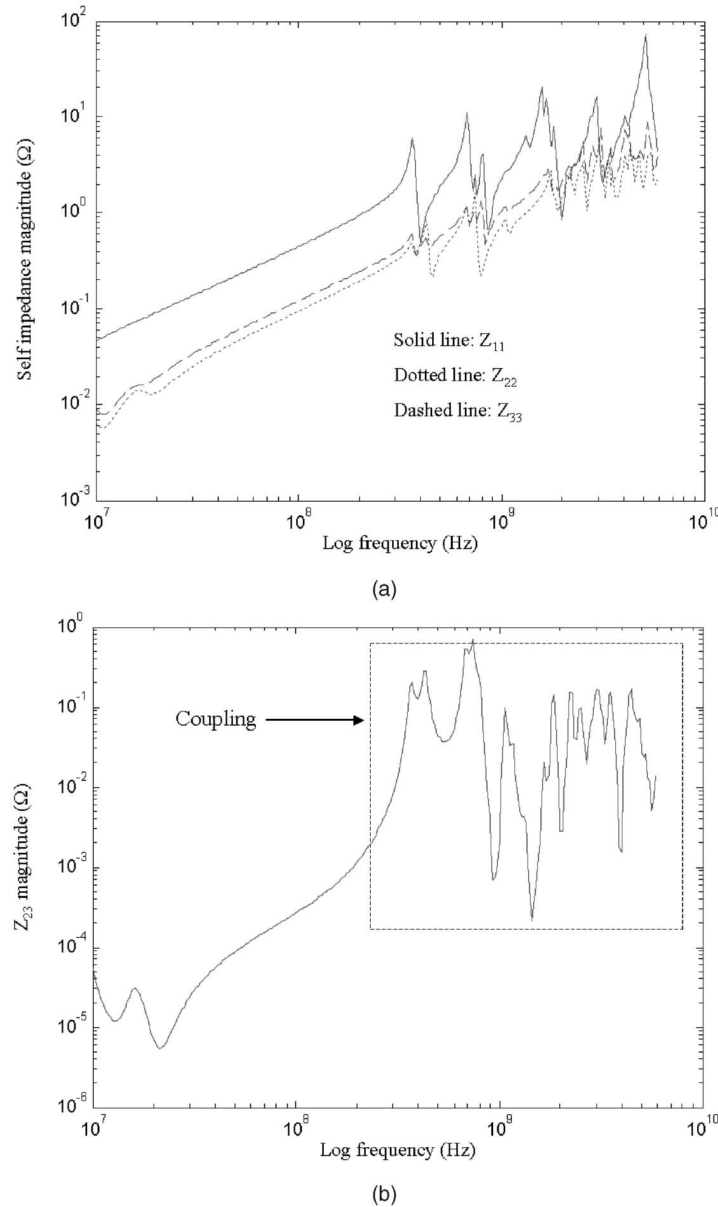


Fig. 14. Impedances of master-slave islands. (a) Self-impedances at ports 1, 2, and 3. (b) Transfer impedance between port 2 in master island and port 3 in slave island.

The eigenvalues are all greater than or equal to zero, demonstrating the passivity and accuracy of macromodel.

The time domain simulation was performed in HSPICE using macromodel of power/ground planes, differential drivers, and transmission lines for computing power supply noise. In Fig. 18, the schematic for simulating power supply noise is shown. The driver model used was a time dependent resistive switch representing four differential drivers. The drivers were connected to four differential transmission lines. The differential drivers with 0.05 ns rise time and 0.05 ns fall time were powered from port 2. The differential transmission lines with 100 Ω characteristic impedance (50 Ω characteristic impedance to ground) and 1 ns delay were connected to the output of the driver. A standard transmission line model available in HSPICE was used to represent the transmission lines. The far end of the transmission lines was terminated in a 50 Ω for matching

and connected to 0.3 V supply voltage. Port 3 representing a 1.2 V power supply for the slave chip was left unterminated. Hence, the differential transmission lines provide the

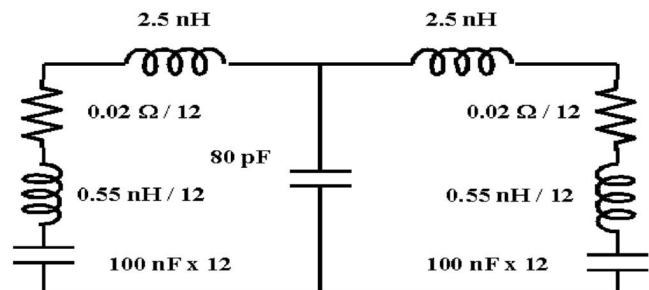


Fig. 15. Equivalent circuit for coupling between master and slave islands.

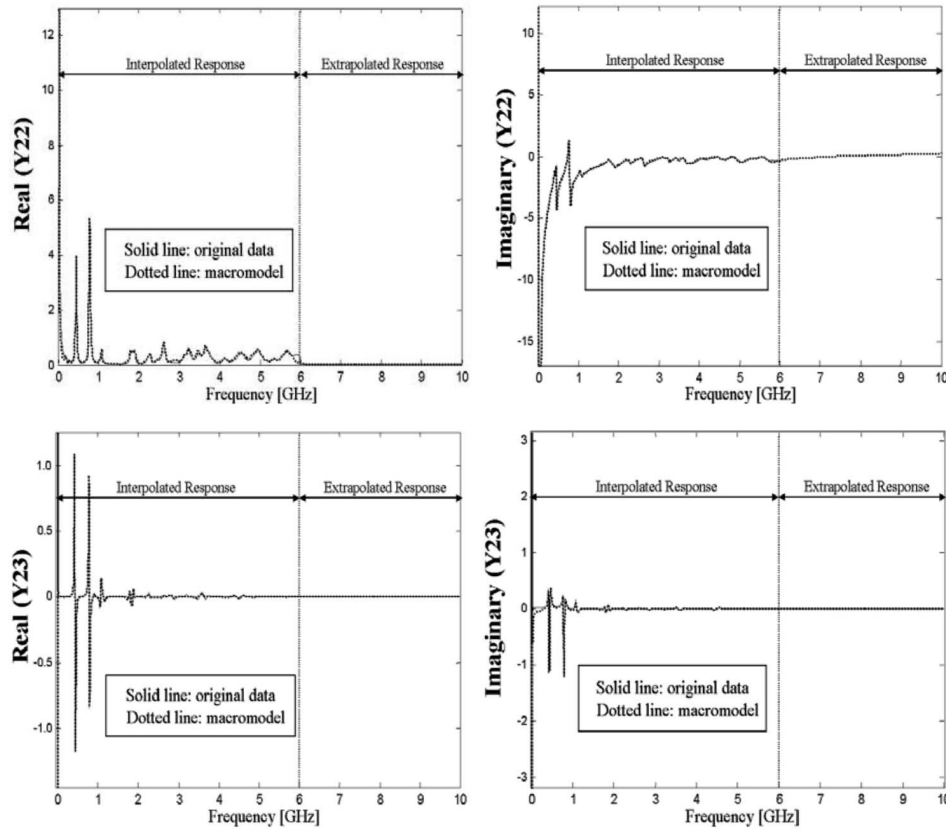


Fig. 16. Comparison between the input Y-parameters and macromodels.

communication path between the master and slave chips. In Fig. 18, the voltage regulator module with 0.6 V supply voltage is connected between port 1 and ground.

In Fig. 6, the two ground planes are connected to each other using numerous vias. Hence, the potential of the two ground planes is maintained constant, at the same potential. In Fig. 18, the differential transmission lines are referenced to the ground plane, which is consistent with the cross section in Fig. 6. When drivers switch from high to low or low to high, they deposit time varying charges on the power/ground planes. These time varying charges result in a current source that excites electromagnetic waves between the power/ground planes, causing them to bounce [24]. The time-varying charges are a direct result of the return current on the planes. Hence, appropriate referencing for the transmission lines in Fig. 18 is important for simulating power supply noise.

The time domain waveform of power supply noise between port 2 and ground is shown in Fig. 19. In Fig. 19, the maximum power supply noise occurs when the driver output changes from low to high or from high to low. This is because the return current from the transmission lines on the power/ground planes excites electromagnetic waves, causing plane bounce. In packages containing planes, the return current is on a reference plane that is in close proximity to the transmission line. This is because, at high speed, the return current follows the path of least inductance, not the path of least resistance. The lowest inductance return path lies directly under a signal conductor, minimizing the total loop area between outgoing and returning current paths [25].

This effect is captured in Fig. 19. In Fig. 19, even though the peak noise occurs during the transition, the power supply continues to bounce, even between transitions. This is due to the Q-factor of the power/ground planes. Perfectly balanced differential drivers cannot generate power supply noise. This is because the current drawn from V_{dd} is perfectly balanced by the current into ground. However, process variations cause an unbalance in the driver output current. This condition has been simulated in this paper by injecting a 10 ps delay between the differential inputs. The bit pattern of the waveform is 0000111100001111..., resulting in a data speed of 3.2 Gbps/pair with a voltage

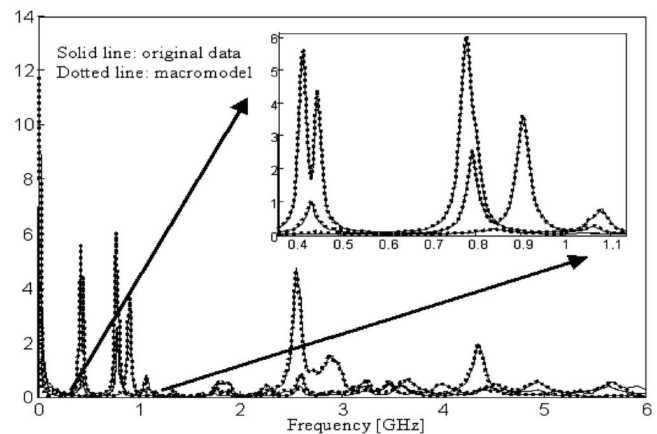


Fig. 17. Comparison of three eigenvalues of original modeling data and the frequency response of constructed macromodel.

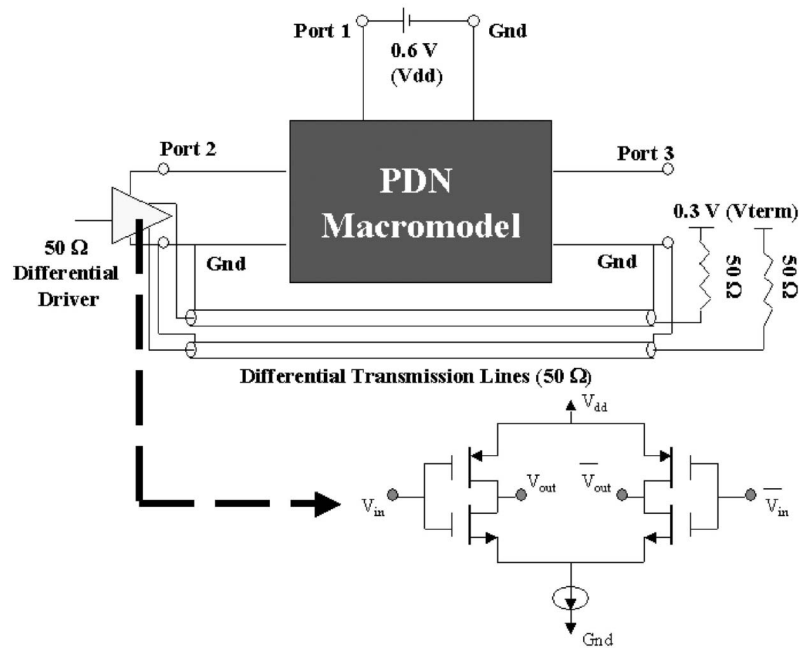


Fig. 18. Modeling of power supply noise with differential drivers, transmission lines, and PDN macromodel.

swing of 271 mV, as shown in Fig. 19. In Fig. 19, switching of four differential transmission lines results in a power supply noise of 40 mV. As can be seen in Fig. 19, the power supply noise is uniform over a time duration of 20 ns, indicating that the macromodel is stable and passive.

To provide a measure of the efficiency of the methodology proposed, the CPU time for computing power supply noise on a Sun workstation was 36.8 secs.

9 CONCLUSION

In this paper, an efficient modeling and analysis methodology for a PDN in a high-speed system has been described. This methodology is based on a hybrid method that combines the TMM in frequency domain and Macromodeling method in time domain. First, TMM was applied to the

PDN in the test vehicle to compute the frequency response. The results were correlated with measurement data using Vector Network Analyzer measurements. Next, the macromodel representation of the plane pairs was generated at the desired ports using macromodeling. Finally, the macromodel of the planes, differential driver model, and transmission lines were cosimulated in HSPICE for computing power supply noise. It was also shown that the time signature of power supply noise was largely dependent on the differential drivers and return currents.

The methodology for modeling and analyzing power distribution networks, as presented in this paper, can be applied to complex systems containing numerous chips on multilayered packages and boards.

ACKNOWLEDGEMENT

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REFERENCES

- [1] R.R. Tummala, E.J. Rymaszewski, and A.G. Klopfenstein, *Microelectronics Packaging Handbook*, pt. I, second ed. New York: Chapman Hall, 1997.
- [2] E.E. Davidson, "Electrical Design of a High Speed Computer Package," *IBM J. Research and Development*, vol. 26, no. 3, pp. 349-361, May 1982.
- [3] B. Young, *Digital Signal Integrity*, chapter 11. Englewood Cliffs, NJ: Prentice Hall, 2001.
- [4] W.T. Beyene, C. Yuan, N. Cheng, and H. Wu, "Interconnect Design and Modeling of 3.2 Gb/s/Pair Bi-Directional Memory System," *Proc. DesignCon 2002: High Performance System Design Conf.*, 2002.

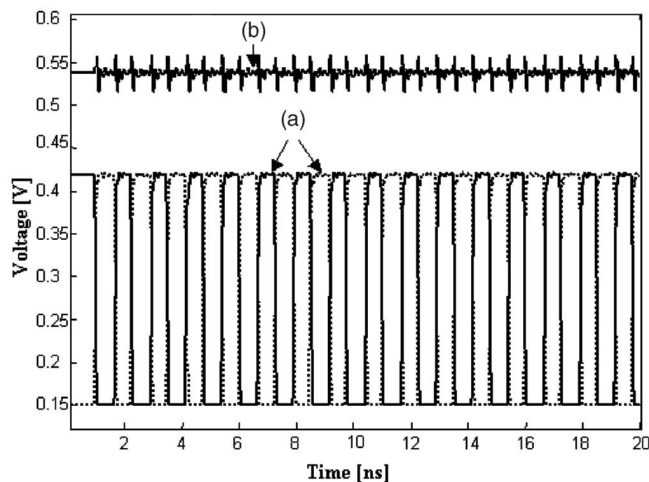


Fig. 19. Power supply noise simulation results. (a) Differential driver output waveform. (b) Power supply noise between port 2 and ground.

- [5] C. Yuan, W. Beyene, N. Cheng, and H. Shi, "Design and Modeling of a 3.2 Gpb/s Memory Channel," *Proc. 11th Topical Meeting Electrical Performance of Electronic Packaging*, pp. 227-230, Oct. 2002.
- [6] Speed 2000 Handout, <http://www.sigrity.com/infos/handout5forweb.htm>, Sigrity Inc., Mar. 2000.
- [7] B. Garben, R. Frech, and J. Supper, "Simulations of Frequency Dependencies of Delta-I Noise," *Proc. 10th Topical Meeting Electrical Performance of Electronic Packaging*, pp. 199-202, Oct. 2001.
- [8] I. Novak, "Lossy Power Distribution Network with Thin Dielectric Layers and/or Thin Conductive Layers," *IEEE Trans. Components, Packaging, and Manufacturing Technology*, vol. 23, no. 3, pp. 353-360, Aug. 2000.
- [9] L. Smith, T. Roy, and R. Anderson, "Power Plane SPICE Models for Frequency and Time Domains," *Proc. Ninth Topical Meeting Electrical Performance of Electronic Packaging*, pp. 51-54, Oct. 2000.
- [10] N. Na, J. Choi, S. Chun, M. Swaminathan, and J. Srinivasan, "Modeling and Transient Simulation of Planes in Electronic Packages," *IEEE Trans. Advanced Packaging*, vol. 23, pp. 340-352, Aug. 2000.
- [11] N. Na, J. Choi, M. Swaminathan, J.P. Libous, and D.P. O' Connor, "Modeling and Simulation of Core Switching Noise for ASICs," *IEEE Trans. Advanced Packaging*, vol. 25, pp. 4-11, Feb. 2002.
- [12] J. Kim and M. Swaminathan, "Modeling of Irregular Shaped Power Distribution Planes Using Transmission Matrix Method," *IEEE Trans. Advanced Packaging*, vol. 24, no. 3, pp. 334-346, Aug. 2001.
- [13] J. Kim, E. Matoglu, J. Choi, and M. Swaminathan, "Modeling of Multi-Layered Power Distribution Planes Including Via Effects Using Transmission Matrix Method," *Proc. Ninth ASP-DAC and 15th Int'l Conf. VLSI Design*, pp. 59-64, Jan. 2002.
- [14] J. Kim and M. Swaminathan, "Modeling of Multi-Layered Power Distribution Planes Using Transmission Matrix Method," *IEEE Trans. Advanced Packaging*, vol. 25, pp. 189-199, May 2002.
- [15] J. Fan, J.L. Drewniak, H. Shi, and J.L. Knighten, "DC Power-Bus Modeling and Design with a Mixed Potential Integral-Equation Formulation and Circuit Extraction," *IEEE Trans. Electromagnetic Compatibility*, vol. 43, no. 4, pp. 426-436, Nov. 2001.
- [16] S.H. Min and M. Swaminathan, "Construction of Broadband Passive Macromodels from Frequency Data for Simulation of Interconnect Networks," *Proc. 15th Int'l Zurich Symp. and Technical Exhibition on Electromagnetic Compatibility*, Feb. 2003.
- [17] J. Kim, J.S. Choi, J. Choi, S. Chun, S. Min, W. Kim, and M. Swaminathan, "Electromagnetic Modeling and Hardware Measurements of Simultaneous Switching Noise in High Speed Systems," *Proc. 2002 IEEE EMC Int'l Symp.*, pp. 748-754, Aug. 2002.
- [18] K. Lee and A. Barber, "Modeling and Analysis of Multichip Module Power Supply Planes," *IEEE Trans. Components, Packaging, and Manufacturing Technology, B*, vol. 18, pp. 628-639, Nov. 1995.
- [19] D.A. Al-Mukhtar and J.E. Sitch, "Transmission-Line Matrix Method with Irregularly Graded Space," *Proc. Elect. Eng. H*, vol. 128, pp. 299-305, Dec. 1981.
- [20] I. Novak, "Reducing Simultaneous Switching Noise and EMI on Ground/Power Planes by Dissipative Edge Termination," *Proc. Seventh Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 181-184, Oct. 1998.
- [21] M. Pozar, *Microwave Engineering*, chapter 2, second ed. New York: Wiley, 1998.
- [22] S. Kami, *Network Theory: Analysis and Synthesis*. pp. 96-98, 118, 393, Allyn and Bacon, 1966.
- [23] W.T. Beyene, C. Yuan, R. Dhat, and D. Secker, "Effects of Plating Stubs on the Electrical Performance of Wirebond PBGA Packages," *Proc. Int'l Conf. Advanced Packaging and Systems (ICAPS)*, pp. 25-30, 2002.
- [24] S. Chun, "Methodologies for Modeling Simultaneous Switching Noise in Multi-Layered Packages and Boards," PhD thesis, School of Electrical and Computer Eng., Georgia Inst. of Technology, Apr. 2002.
- [25] H. Johnson and M. Graham, *High-Speed Digital Design*, pp. 189-191. Englewood Cliffs, N.J.: Prentice Hall, 1993.



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