High-Speed DSP Systems Design

Reference Guide

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Read This First

About this Manual

This document contains the following chapters:

- Chapter 1 provides information about the challenges of high speed DSP, audio, video, and communication systems.
- Chapter 2 provides information about transmission lines in high speed DSP systems.
- Chapter 3 provides information about noise in a DSP system.
- Chapter 4 provides information about power supply design in high-speed DSP.
- Chapter 5 provides information about the development of printed circuit boards.
- Chapter 6 provides information about isolating phase-locked loop from protection of internal and external noises.
- Chapter 7 provides information about electromagnetic interference in a high-speed DSP system.
- Chapter 8 summaries the intricate operations of a high-speed DSP system.

Related Documentation

The following documents describe the reference materials related high speed systems. Some copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

J. Lin, B. Haroun, T. Foo, J. Wang, B. Helmick, S. Randall, T. Mayhugh, C. Barr, and J. Kirkpatrick, "A PVT Tolerant 0.18MHz to 600MHz Self-Calibrated Digital PLL in 90nm CMOS Process," ISSCC, Feb. 2004.

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Texas Instruments Inc, "Multi-Gigabit Board Layout Guidelines with Texas Instruments SERDES," Application note, Feb. 2002.

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Texas Instruments Inc, "OMAP5910 Audio System Design," Application note, SPRA970, Nov. 2003.

Texas Instruments Inc, "OMAP5910 NTSC or VGA Output," Application note, SPRA847, June 2003.

Michael Mardiguian, Controlling Radiated Emissions By Design, Van Nostrand Reinhold publisher, New York, 1992.

Howard Johnson and Martin Graham, High-Speed Signal Propagation, Prentice-Hall, New Jersey, 2003.

Challenges of High-Speed DSP Design

Today's digital signal processors (DSPs) are typically run at a 1GHz internal clock rate while transmit and receive signals to and from external devices operate at rates higher than 200MHz. These fast switching signals generate a considerable amount of noise and radiation, which degrades system performance and creates electromagnetic interference (EMI) problems that make it difficult to pass tests required to obtain certification from the Federal Communication Commission (FCC). Good high-speed system design requires robust power sources with low switching noise under dynamic loading conditions, minimum crosstalk between high-speed signal traces, high- and low-frequency decoupling techniques, and good signal integrity with minimum transmission line effects. This document provides recommendations for meeting the many challenges of high-speed DSP system design.

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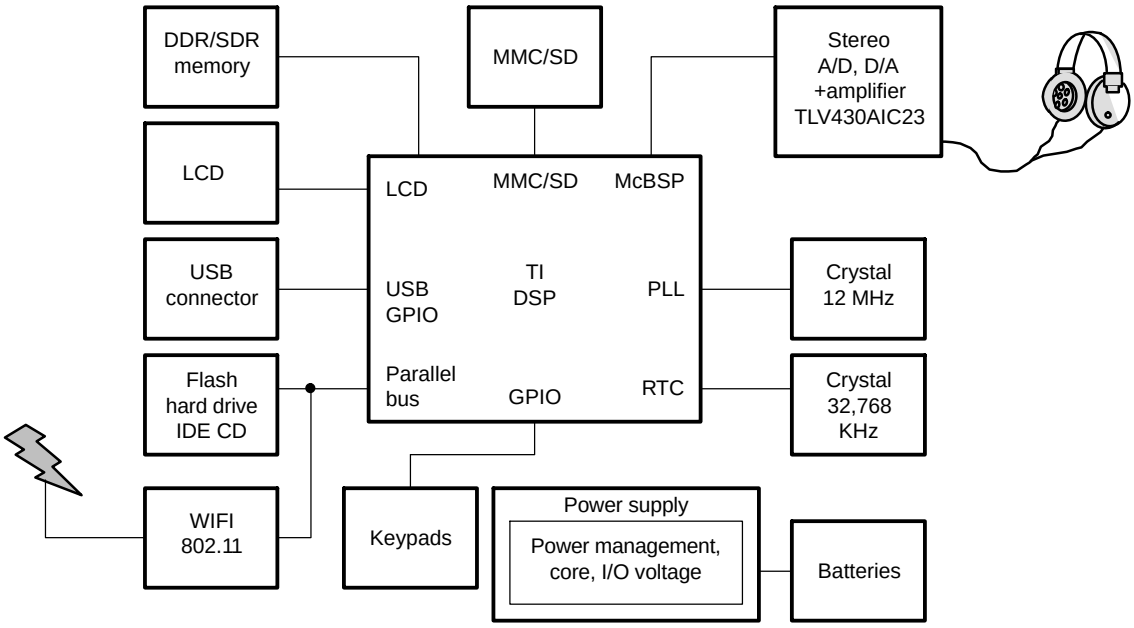
1.1 General Challenges

As DSP performance levels and clock frequencies continue to rise at a rapid rate, managing noise and radiation becomes an increasingly important issue. In the Gigahertz world, lines carrying signals act as transmission lines that can generate signal reflections that cause distortion. Furthermore, since data is packed into smaller and smaller time cycles, the resulting shorter signal pulses are more susceptible to interference. The risk is particularly great in dealing with audio and video systems where noise can cause subtle performance degradation that normally would not have any impact on discrete data.

The rising power and performance of today's DSP systems also creates challenges in achieving electromagnetic compatibility (EMC) compliance. At high frequencies, the traces on a PCB act like mono-pole or loop antennas, generating emissions that can often make it difficult to meet FCC Class A and Class B requirements. Heat sinks and venting that may be required to address the thermal challenges of high performance designs can further exacerbate EMC problems. The trend towards integrating wireless capabilities creates further difficulties as intentional radiators are designed into the system.

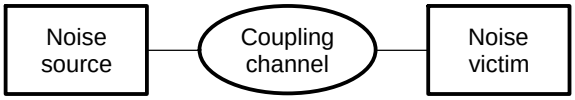
These trends make it necessary to rethink the traditional DSP design process. In the traditional approach, engineers focus on the functional and performance aspects of the design. Noise and radiation are considered only towards the later stages of the design process if and when prototype testing reveals problems. But today, noise problems are becoming increasingly common and more than 70% of new designs fail first-time EMC testing. As a result, it has become essential to begin addressing these issues from the very beginning of the design process. Investing a small amount of time in the use of low-noise and low-radiation design methods from the very beginning of the development cycle will generate a high payoff by minimizing late-stage redesign costs and delays in the product ship date.

Figure 1-1. Typical DSP System



Typical DSP systems such as the one shown in Figure 1-1 consist of many external devices such as audio CODEC, video, LCD display, wireless communication (Bluetooth and IEEE 802.11), Ethernet controller, USB, power supply, oscillators, storage, memory and other supporting circuitries. Each of these components can either be a noise generator or be affected by interferences generated by neighboring components. Therefore, applying good high speed design practices is necessary in order to minimize both component and system related noise and ensure system design success.

Figure 1-2. A Typical Noise Path



The coupling between a noise source and noise victim causes electrical noise. Figure 1-2 shows a typical noise path. The noise source is typically a fast-switching signal and the noise victim is the component carrying the signal whose performance is impacted by the noise. Coupling takes place through the parasitic capacitances and mutual inductances of the adjacent signals and circuits. Electromagnetic coupling occurs when the signal traces become effective antennas, which radiate and generate interferences to the adjacent circuitries.

There are many mechanisms by which noise can be generated in an electronic system. Clock circuits generally have the highest toggle rates and are therefore a primary source of noise. Improperly terminated signal lines may generate reflections and signal distortions. Ground plane resistance caused by the skin effect and proximity effect can result in significant ground noise.

Noise can also be generated within semiconductors themselves:

- **Thermal Noise**: Also known as Johnson noise, thermal noise is present in all resistors and is caused by random thermal motion of electrons. Thermal noise can be addressed in audio and video designs, by keeping resistance as low as possible to improve the signal-to-noise ratio.
- **Shot Noise:** Shot noise is caused by charges moving randomly across the gate in diodes and transistors. This noise is inversely proportional to the DC current flowing through the diode or transistor so higher DC operating current increases the signal-to-noise ratio. Shot noise can become an important factor when the DSP system includes many analog discrete devices on the signal paths, for example discrete video and audio amplifiers.
- **Flicker Noise:** Also known as 1/f noise, flicker noise is present in all active devices. It is caused by traps where charge barriers are captured and released randomly, causing random current fluctuations. Flicker noise is a factor of semiconductor process technologies so DSP system design cannot reduce it at the source but must rather focus on mitigating its effects.
- **Burst Noise and Avalanche Noise:** Burst Noise, also known as popcorn noise, is caused by ion contamination. Avalanche Noise is found in devices such as zener diodes that operate in reverse breakdown mode. Both of these types of noise are again related to the semiconductor process technology rather than system design techniques.

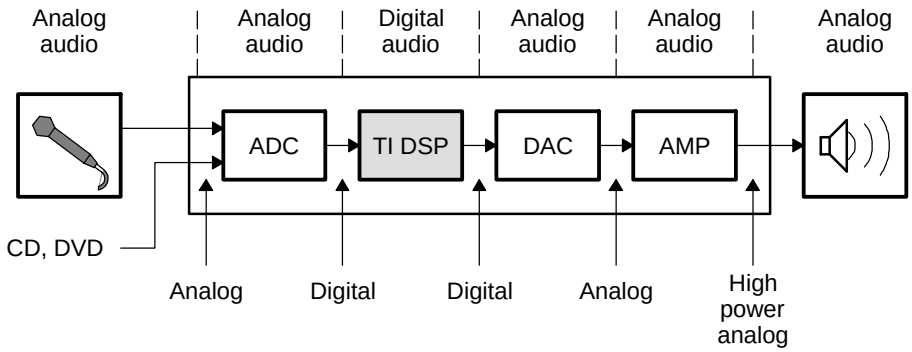
Since governments regulate the amount of electromagnetic energy that can be radiated, DSP systems designers must also be concerned with the potential for radiating noise to the environment. The main sources of radiation are digital signals propagating on traces, current return loop areas, inadequate power supply filtering or decoupling, transmission line effects, and lack of return and ground planes. It is also important to note that at Gigahertz speeds, heat sinks and enclosure resonances can amplify radiation.

Noise in DSP systems cannot be eliminated but it can be minimized to ensure that it is not interfering with other circuits in the system. The three ways to reduce noise are suppressing it at the source, making the adjacent circuits insensitive to the noise, and eliminating the coupling channel. High-speed design practices can be applied to minimize both component and system related noise and improve the probability of system design success. This document will address all three areas by providing guidelines that can be used from the very beginning of the design process through troubleshooting to reduce noise and radiation to acceptable levels. The noise-sensitive interface examples shown in this document are focused on audio, video, and power supply since the performance of these systems is greatly affected by the surrounding DSP circuitries and how these circuits interfaced to the DSP.

1.2 Challenges of DSP Audio Systems

Audio systems represent one of the greatest challenges for high-speed DSP design because relatively small levels of noise often have a noticeable impact on the performance of the finished product. In audio capture and playback, audio performance depends on the quality of the audio CODEC being used, the power supply noise, the audio circuit board layout, and the amount of crosstalk between the neighboring circuitries. Also, the stability of the sampling clock has to be very good to prevent unwanted sounds such pops and clicks during playback and capture. Figure 1-3 shows a typical signal chain of the DSP audio design. Most of Texas Instruments Incorporated™ DSPs include a multi-channel buffered serial port (McBSP) for interfacing with external audio CODECs. Although this is a Texas Instruments Incorporated specific interface, it is configurable to work with the industry standard I2S audio CODECs as shown in Figure 1-4.

Figure 1-3. DSP Audio System

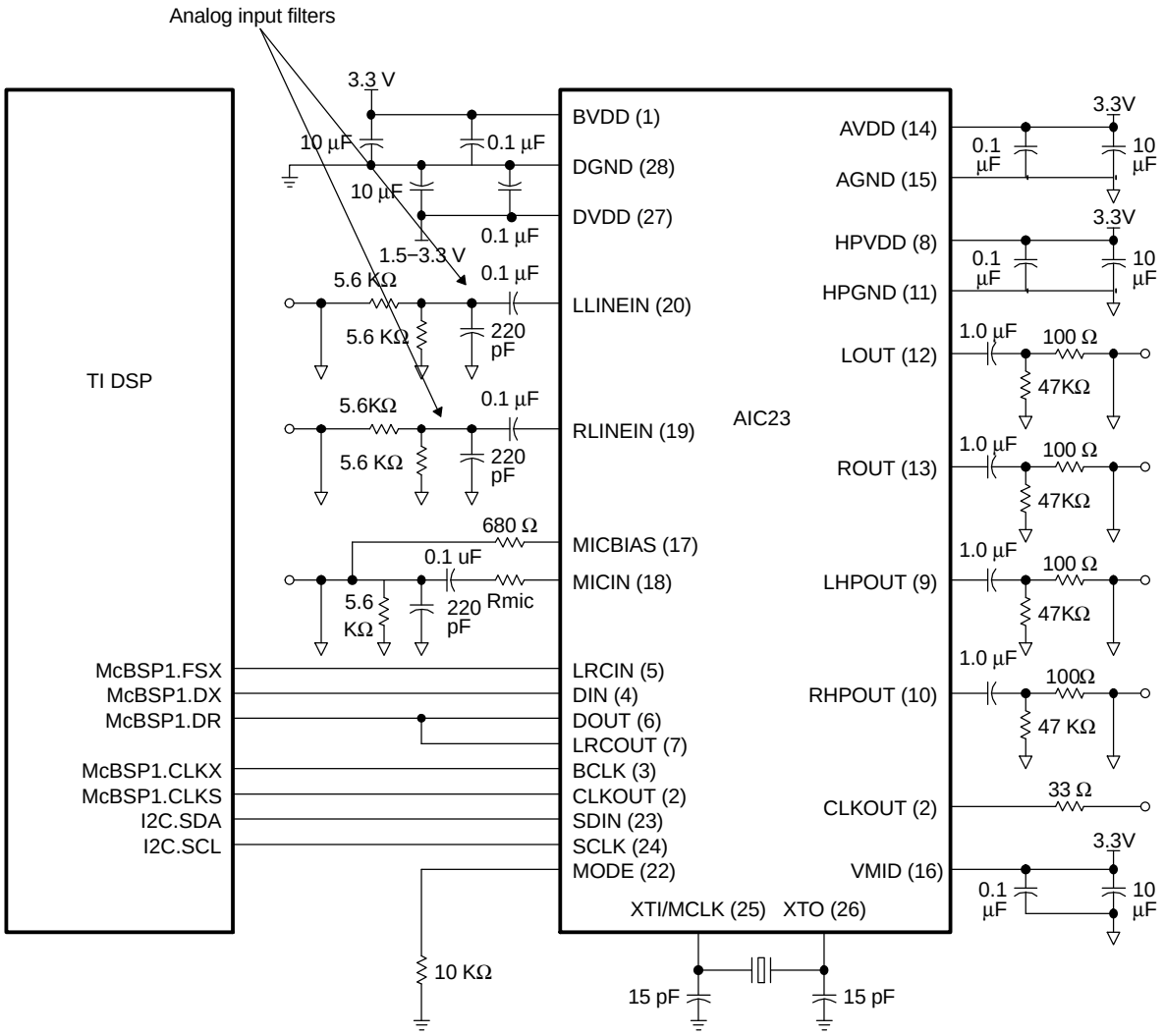


All of the blocks shown in Figure 1-3 from the ADC to the Amp stage are very sensitive to noise so any interference coupled to any of the blocks will propagate and generate unwanted audible sounds. Common audio design problems include:

- Noise coupled to the microphone input
- Not having an anti-aliasing filter at the audio inputs, Line-In and Mic-In
- Excessive distortion due to gain stage and to amplitude mismatch
- Excessive jitter on audio clocks, bit clock and master clock
- Lack of good decoupling and noise isolation techniques
- Not using a linear regulator with high power supply rejection to isolate noise from the audio CODEC
- Not having good decoupling capacitors on the reference voltage used for ADC and DAC converters
- Switching power supply noise coupled to the audio circuits
- High impedance audio traces are adjacent to noisy switching circuits and no shortest current return path is provided in the printed circuit board (PCB) layout to minimize the current return loop between the DSP and the CODEC.

In summary, having good audio performance requires proper design of the input stages of the CODEC, the DSP interface and the output amplifier. The DSP audio architecture example is shown in Figure 1-4 where the I^2S interface is the master driving the bitclock (McBSP1.CLK) and frame sync signals.

Figure 1-4. DSP Audio System Architecture



1.3 Challenges of DSP Video Systems

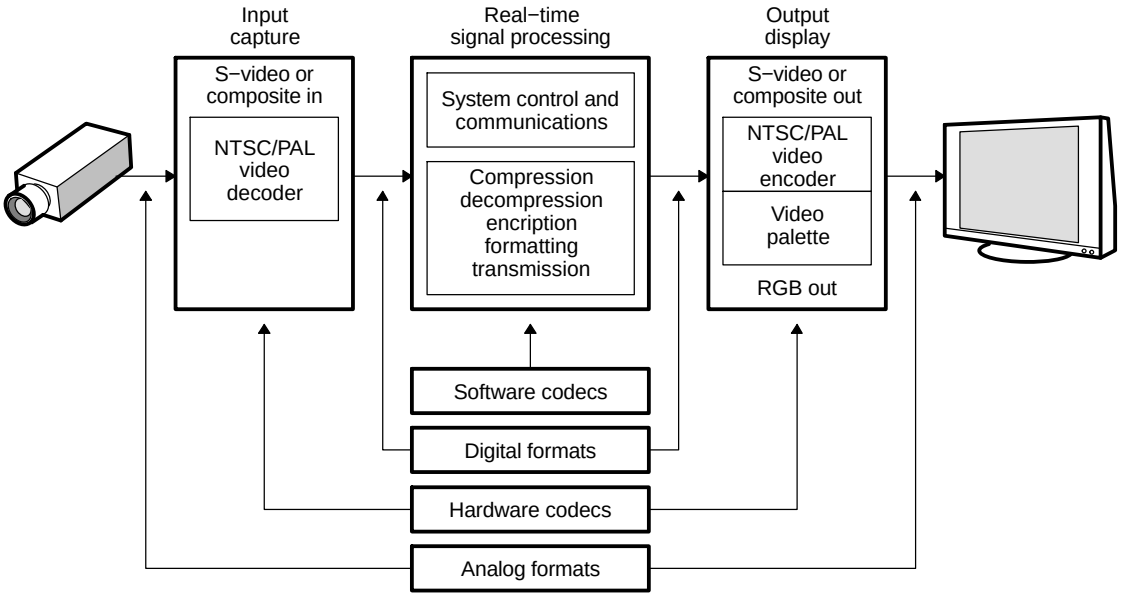
Video processing is another important DSP application that is highly sensitive to noise and radiation. One of the major challenges of video systems design is to how to eliminate video artifacts such as color distortion, 60Hz hum, audio beat, etc. These issues are generally related to improper video board design. For example power supply noise may propagate to the video DAC output, audio playback may cause transients in the power supply, and the audio section may couple to high impedance traces in the video section. Here are some common video noise issues:

- Signal integrity, excessive overshoots and undershoots on the HSYNC, VSYNC, and pixel clocks caused by improper signal terminations.
- Excessive encoder, decoder, and pixel clock jitter causes problems with detecting the color information. For example, the color screen only displays black and white images.
- The lack of video termination resistors causes distortion of the video image. A 75-ohm termination resistor should be used at the input of the video decoder and the output of the video encoder.
- Audio playback may cause a flicker on the video screen. This can be corrected by increasing the isolation of the video and audio circuits. The best method is using high power supply rejection ratio (PSRR) linear regulators to isolate the audio CODEC and the video encoder/decoder supplies. Also, manually route the critical traces away from any of the switching signals to reduce the crosstalk and interferences.

- An isolated analog ground without a high-speed signal return path. It is important to remember that for a low speed signal, below 10 MHz, current returns on the lowest resistance, which is usually the shortest, path. High-speed current, on the other hand, returns on the path with the least inductance, usually underneath the signal.

Figure 1-5 shows a typical DSP video system where the analog video signal is captured, processed and then displayed. The quality of this video signal path determines the video performance of the display, especially at the input video decoder stage and at the output video encoder stage. Since the system design and layout are very critical, it is necessary to apply the high-speed design rules discussed in this document to reduce the negative effects of the switching noise, crosstalk and power supply transients in order to reduce or eliminate video artifacts. As in any electronic systems it is not possible to eliminate the noise totally but applying good design techniques helps reduce the risk of having a negative impact on performance.

Figure 1-5. DSP Video System

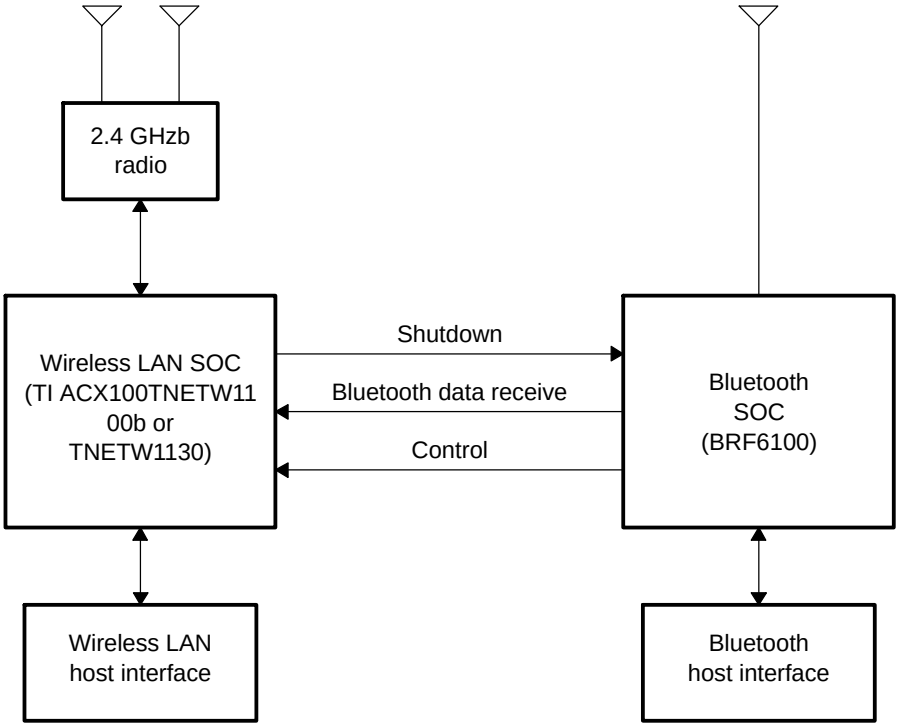


1.4 Challenges of DSP Communication Systems

Like video and audio systems, communication is another important DSP application that is highly sensitive to noise and radiation. One of many challenges here is creating systems with multiple powerful and highly integrated DSPs that deliver high performance but very low bit error rate and interference. In these systems, interference not only generates EMI problems but also jams other communication channels and causes false channel detection. These issues can be minimized by applying proper board design techniques, shielding and RF and mixed analog/digital signals isolation. In some cases, a spread spectrum clock generator may be required to further reduce the interference and to improve the signal-to-noise ratio. Although spread spectrum clock reduces the peak level radiation, the harmonics of this clock are spreading over a wider bandwidth and this can cause inter-channel interference so engineers must be careful when using this type of clock generator circuit.

One example of the communication systems is shown in Figure 1-6 where both Bluetooth and IEEE802.11 are being implemented on the same motherboard and residing on the same 2.4GHz RF spectrum. The most difficult task here is how to prevent the two systems from interfering with each other and this has become one of the hot research topics in the industry. In any case, to improve the probability of design success, applying the rules outlined in this document is a must do.

Figure 1-6. Communication Block Diagram



Transmission Line (TL) Effects

Transmission line (TL) effects are one of the most common causes of noise problems in high-speed DSP systems. When do traces become TLs and how do TLs affect the system performance? A rule-of-thumb is that traces become TLs when the signals on those traces have a risetime (Tr) less than twice the propagation delay (Tp). For example, if a delay from the source to the load is 2nS, then any of the signals with a risetime less than 4nS becomes a TL. In this case, termination is required to guarantee minimum overshoots and undershoots caused by reflections. Excessive TL reflections can cause electromagnetic interference and random logic or DSP false-triggering. As a result of these effects, the design may fail to get the FCC certification or to fully function under all operating conditions such at high temperatures or over-voltage conditions.

There are two types of transmission lines, lossless and lossy. The ideal lossless transmission line has zero resistance while a lossy TL has some small series resistance that distorts and attenuates the propagating signals. In practice, all TLs are lossy. Modeling of lossy TLs is a difficult challenge that is still the subject of ongoing research. Since this document is focused on practical problem-solving methods, it assumes a lossless TL. This is a reasonable assumption because in practice the losses on a printed circuit board trace are negligible compared to losses in the entire system.

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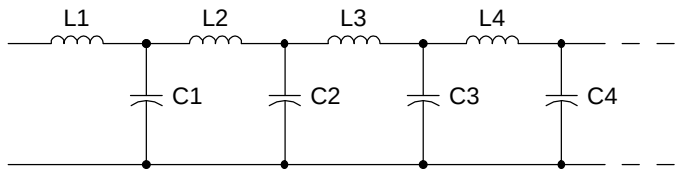
2.1 Transmission Line Theory

A lossless TL is formed by a signal propagating on a trace that consists of series parasitic inductors and parallel capacitors as shown in Figure 2-1.

Figure 2-1. Lossless Transmission Line Model



The speed of the signal, Vp, is dependant on properties such as characteristic impedance, Zo, which is defined as an initial voltage V^+ divided by the initial current I^+ at some instant of time. The equations for Vp and Zo are:

$$V_p = \frac{1}{\sqrt{LC}},$$

$$Z_o = \sqrt{\frac{L}{C}},$$

where L is inductance per unit length and C is capacitance per unit length.

Another important property of the TL is the propagation delay, T_d. The equation for T_d is

$$T_d = \frac{1}{Vp} = \sqrt{LC}.$$

The source and load TL reflections depend on how well the output impedance and the load impedance, respectively, are matched with the characteristic impedance. The load and source reflection coefficients are

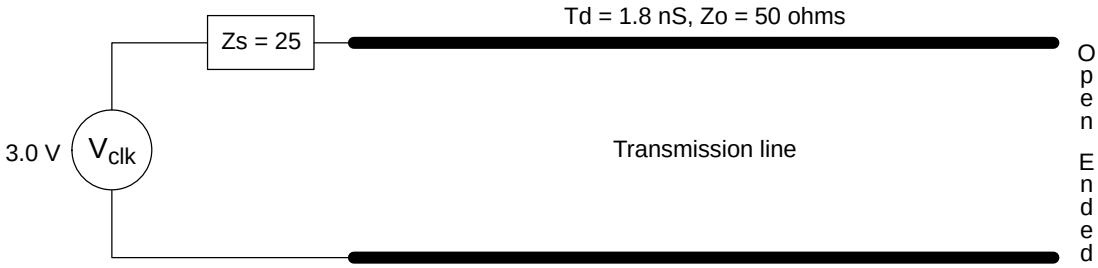
$$\Gamma_s = source_reflections = \frac{Z_s - Z_o}{Z_s + Z_o},$$

$$\Gamma_s = load_reflections = \frac{Z_L - Z_o}{Z_L + Z_o},$$

where Z_S and Z_L are the source impedance and load impedance respectively.

The following example shows the characteristics of a TL with no load and with a 3V signal source driving the line.

Figure 2-2. Example 1



$$V_{initial} = V_{clk}\frac{Zo}{Zs + Zo} = 3\frac{50}{25 + 50} = 2V$$

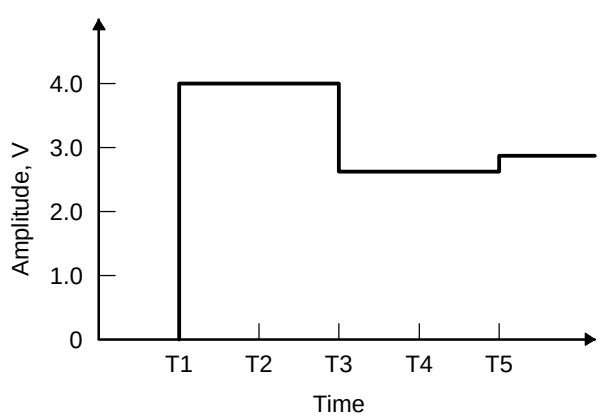
$$\rho_s = \frac{Zs - Zo}{Zs + Zo} = \frac{25 - 50}{25 + 50} = -0.333$$

$$\rho_L = \frac{Z_L - Zo}{Z_L + Zo} = 1$$

In Figure 2-3, the overshoot voltage can be calculated as follows.

At T1 = 1.8nS: $V_L = V_I + \rho_L V_I = 2+2 = 4.0V$
At T2 = 3.6nS: $V_S = 4.0V + \rho_S V_I = 4.0V – 0.67V = 3.33V$
At T3 = 5.4nS: $VL = 3.33V + \rho_L(\rho_S V_I) = 3.33 – 0.67 = 2.66V$
At T4 = 7.2nS: $Vs = 2.66V + \rho_S[\rho_L(\rho_S V_I)] = 2.66 + 0.22 = 2.88V$
At T5 = 9.0nS: $V_L = 2.88 + \rho_L (0.22) = 3.1V$

Figure 2-3. TL Transient Response



As shown in the example, the reflections with a 3V source caused the signal to overshoot as high as 4V at the load as explained below:

- The initial voltage level at the load at time T1 depends on the load impedance, which is infinite for an open load, and the characteristic impedance of the TL.
- The voltage level at time T2, when the reflected signal arrives at the source, depends on the source impedance and the characteristic impedance of the TL.
- The voltage level at time T3, when the reflected signal arrives at the load again, depends on the reflected voltage at T2 plus the reflected voltage at time T3.

- This process continues until steady state is reached. In this example, the steady state occurs at T5, which is 9nS from T1.

Figure 2-4 shows the waveforms at the load for both non-terminated and terminated circuits. As shown in the previous example, the terminated TL has a zero reflection coefficient and therefore no ringing occurs on the waveform as seen on the top graph of Figure 2-4. The problem is that in high-speed digital design, adding a 50-ohm resistor to ground at the load is not practical because this requires the buffer to drive too much current per line. In this case, the current would be 3.3V / 50 = 66mA. A technique known as parallel termination can be used to overcome this problem. It consists of adding a small capacitor in series with the resistor at the load to block DC. The RC combination should be much less than the rise and fall times of the signal propagating on the trace.

Figure 2-4. Waveforms for Terminated and Unterminated Circuits

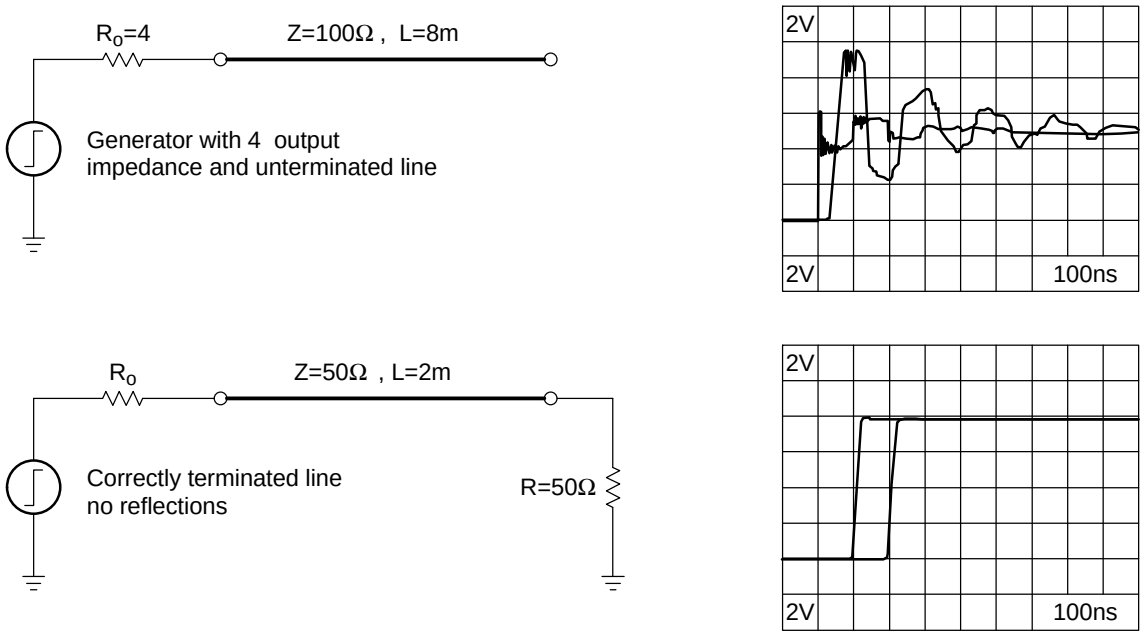


Figure 2-5. Parallel Termination Technique

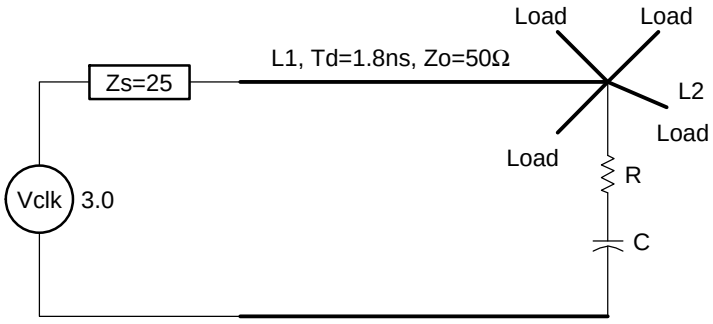


Figure 2-5 shows a parallel termination technique. This method can be used in the application where one output drives multiple loads as long as the traces to the loads called L2 are a lot shorter than the main trace L1.

To use the parallel termination technique, it is necessary to calculate the maximum allowable value for L2 according to the equation below assuming the main trace L1 and the rise time Tr are known.

$$L_2, \max = L_1^{\frac{tr}{10}}$$

2.2 Parallel Termination Simulation

Parallel termination techniques become useful when designers have to use a single clock output to drive multiple loads to minimize the clock skew between the loads. In this case, having a series resistor at the source limits the drive current to the loads and may cause timing violations by increasing risetimes and falltimes. This simulation example includes one 6” trace (L1) and two 2” stubs. The TI OMAP™ processor drives the main L1 trace and one Micron Technology memory device connected to each end of the 2” trace. It is reasonable to neglect the effects of the stubs as long as they are short and meet the criteria shown in Figure 2-6. In this case, only one parallel termination (68 ohms and 10pF) is required at the split of the main trace to the loads. Referring to the simulation result in Figure 2-7, the waveforms at the loads look good and meet all the timing requirements for the memory devices. As expected for the “no series” termination case, the waveform at the source does not look good but this does not affect the system integrity at the load.

Figure 2-6. Parallel Termination Simulation Results

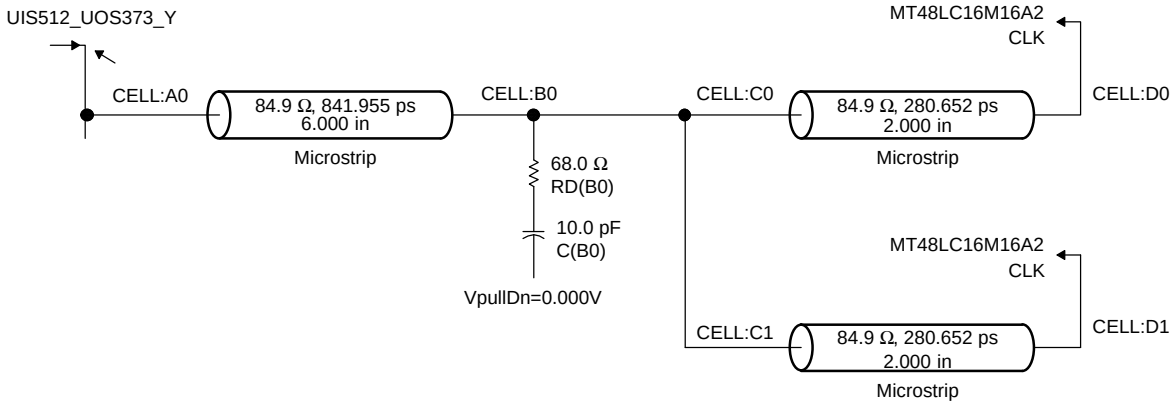
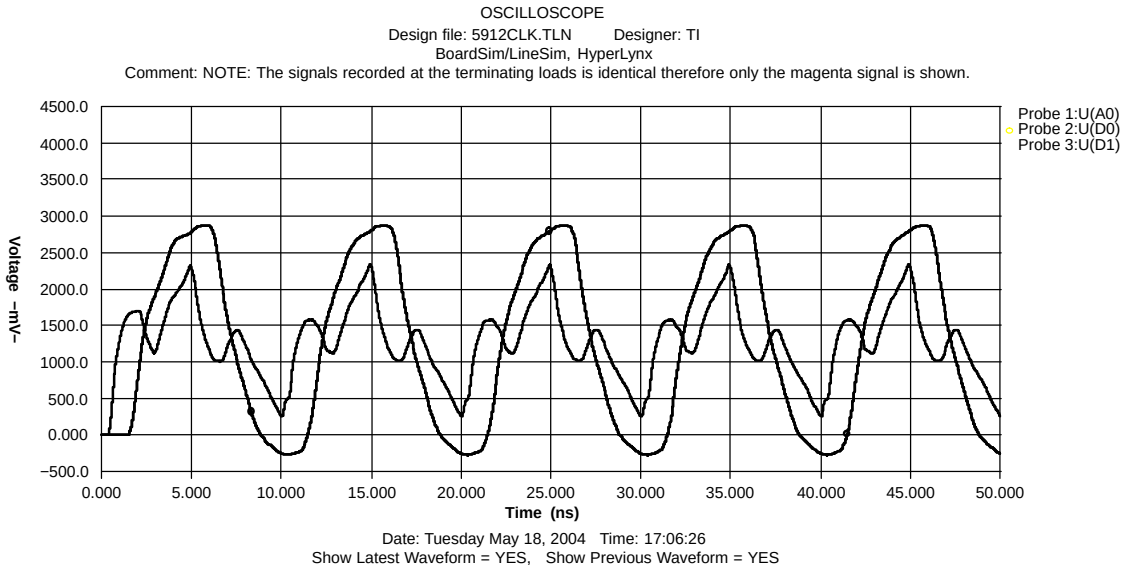


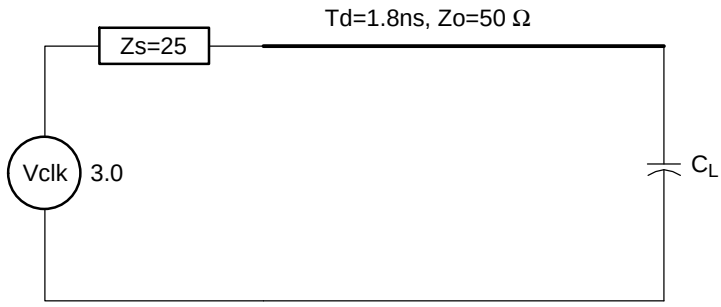
Figure 2-7. Parallel Termination Simulation Results



2.3 Practical Considerations of TL

In general high-speed DSP systems consist of many CMOS devices where the input impedance is very high, typically in Megaohms, and the input capacitance is relatively small, less than 20pF. In this case, with no load termination, the TL looks like a transmission line with a capacitive load, rather than an open circuit. The capacitive load helps reduce the risetime and allows the designers to use only a series termination at the source. This approach is becoming very common in high-speed systems.

Figure 2-8. Practical Model of TL



In Figure 2-8, the voltage at the load is slowly charged up to the maximum amplitude of the clock signal. Initially, the load looks like a short circuit. Once the capacitor is fully charged, the load becomes an open circuit. The source resistor Zs controls the rise and fall times. Higher source resistance yields slower rise time. The load voltage at any instant of time, t, greater than the propagation delay time, can be calculated using the following equation:

$$V_L = V_{clk}\left(1 - e^{-(t-Td)/\tau}\right),$$

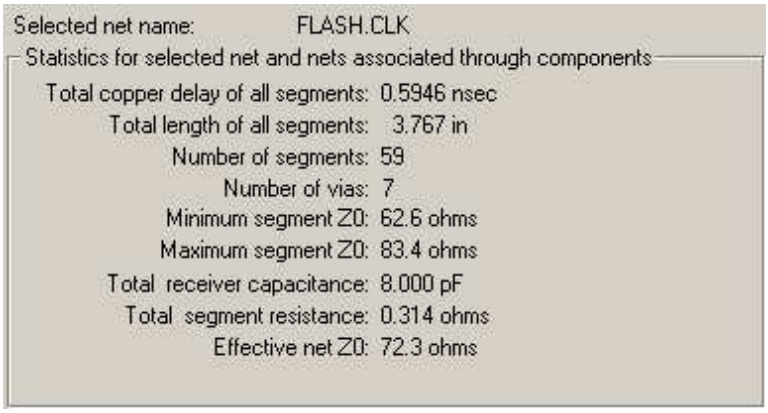
where t is some instant of time greater than the propagation delay and $\tau = C_L Z_o$, where CL and Zo are the load capacitor and characteristic impedance respectively.

2.4 Simulations and Experimental Results of TL

2.4.1 TL Without Load or Source Termination

One of the well-known techniques to analyze the PC board is using Hyperlynx software to simulate the lines. Figure 2-9 shows a setup used for the simulations.

Figure 2-9. Hyperlynx Simulation Setup



The selected signal is FLASH.CLK which is a clock signal generated by a TI DSP. Figure 2-10 shows an actual PC board designed with one of the TI DSPs where the clock is driven by U3 and is measured at U2.

Figure 2-10. PC Board Showing FLASH.CLK Trace

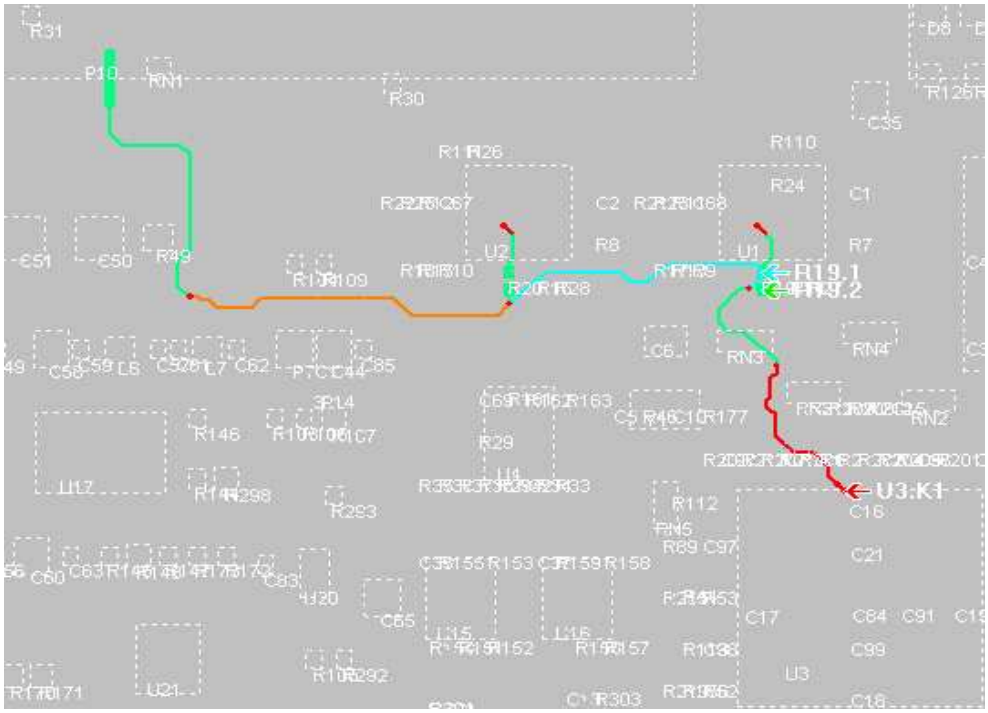


Figure 2-11 shows the simulation result at U2 and Figure 2-12 shows the actual scope measurement in the lab.

Figure 2-11. Hyperlynx Simulation Result of FLASH.CLK

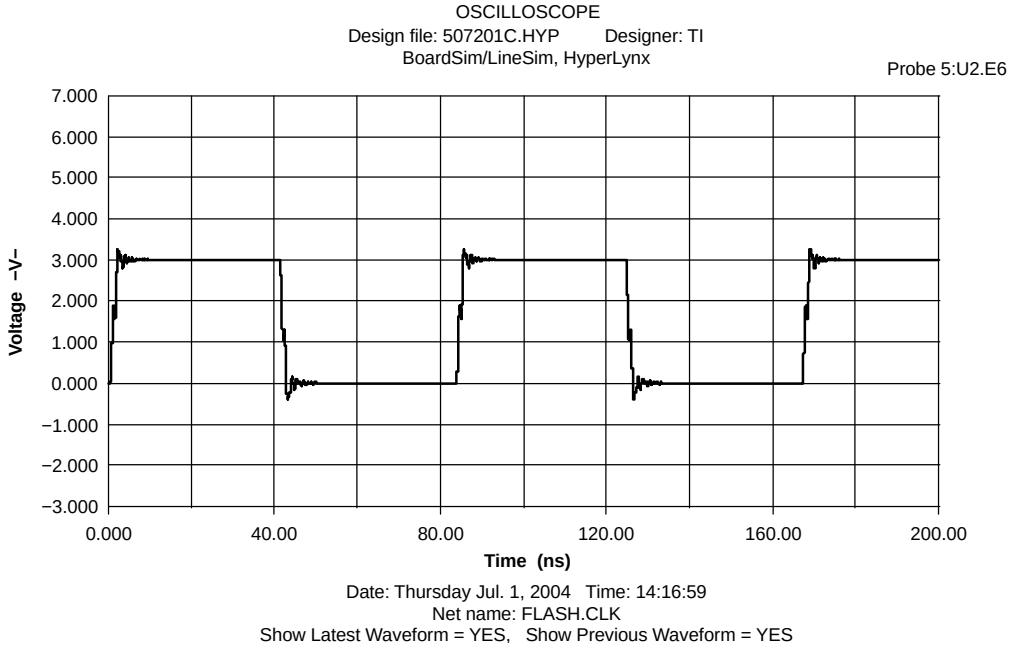
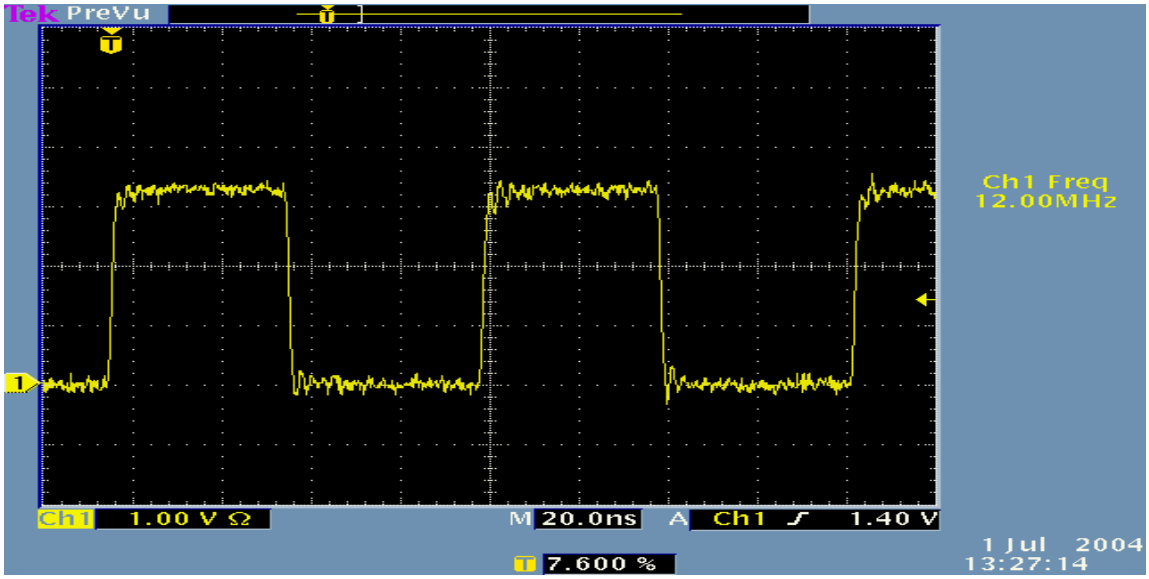


Figure 2-12. Lab Measurement of FLASH.CLK



2.4.2 TL with Series Source Termination

As discussed earlier, most high-speed system designs use this technique since it is possible to optimize the load waveforms simply by adjusting the series termination resistors. This technique also helps reduce the dynamic power dissipation since the initial drive current is limited to the maximum source voltage divided by the characteristic impedance. Figure 2-13 shows the setup used for the Hyperlynx simulation of the audio clock driven by an audio CODEC external to the TI DSP.

Figure 2-13. Series Termination Clock Setup

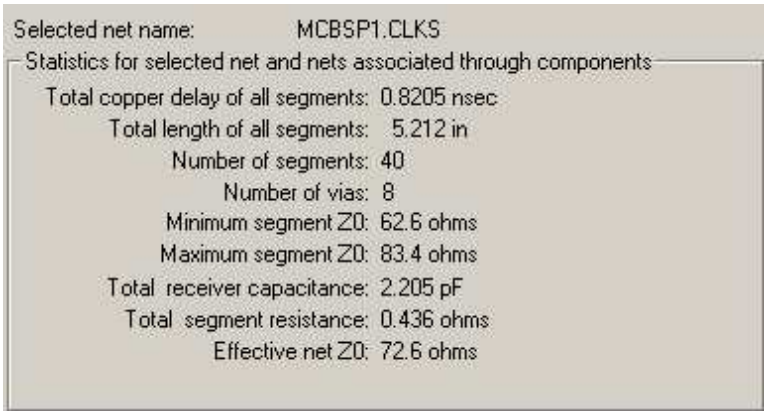
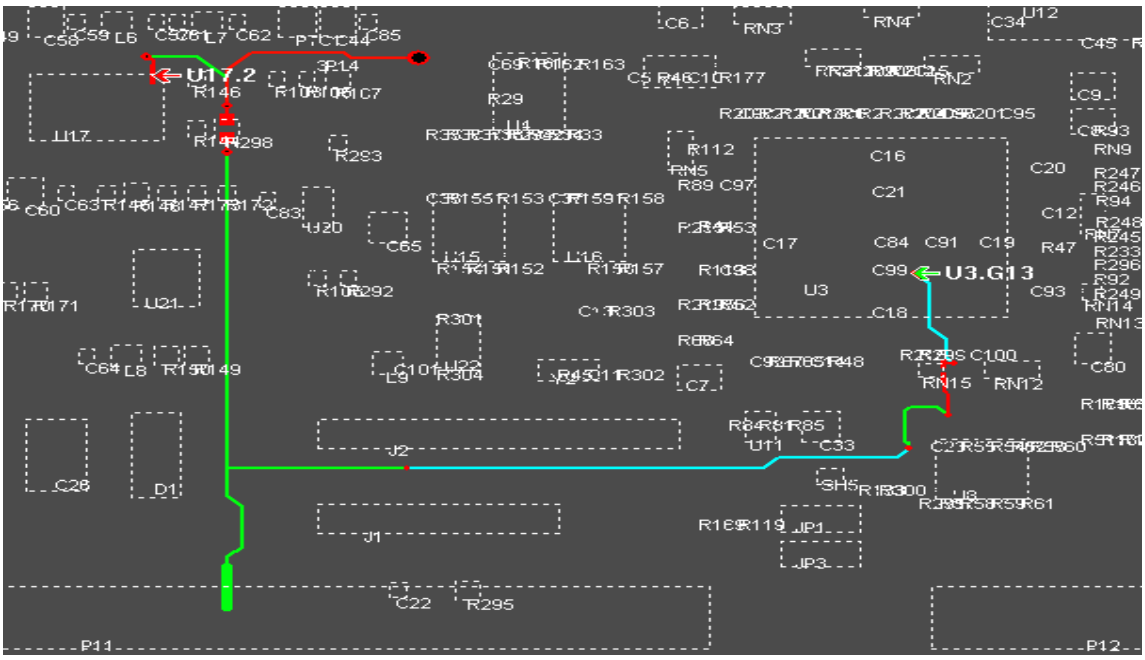


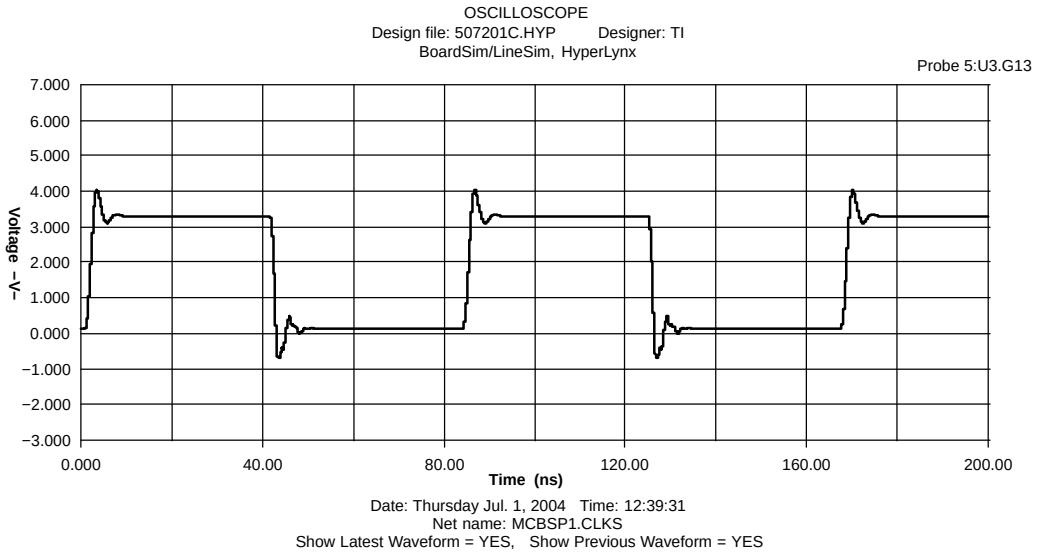
Figure 2-14 shows an audio clock that transmits by U17 and receives by U3. The design has a 20-ohm series termination resistor but no parallel termination at the load. This demonstrates the concept discussed earlier.

Figure 2-14. Audio Clock with Series Termination



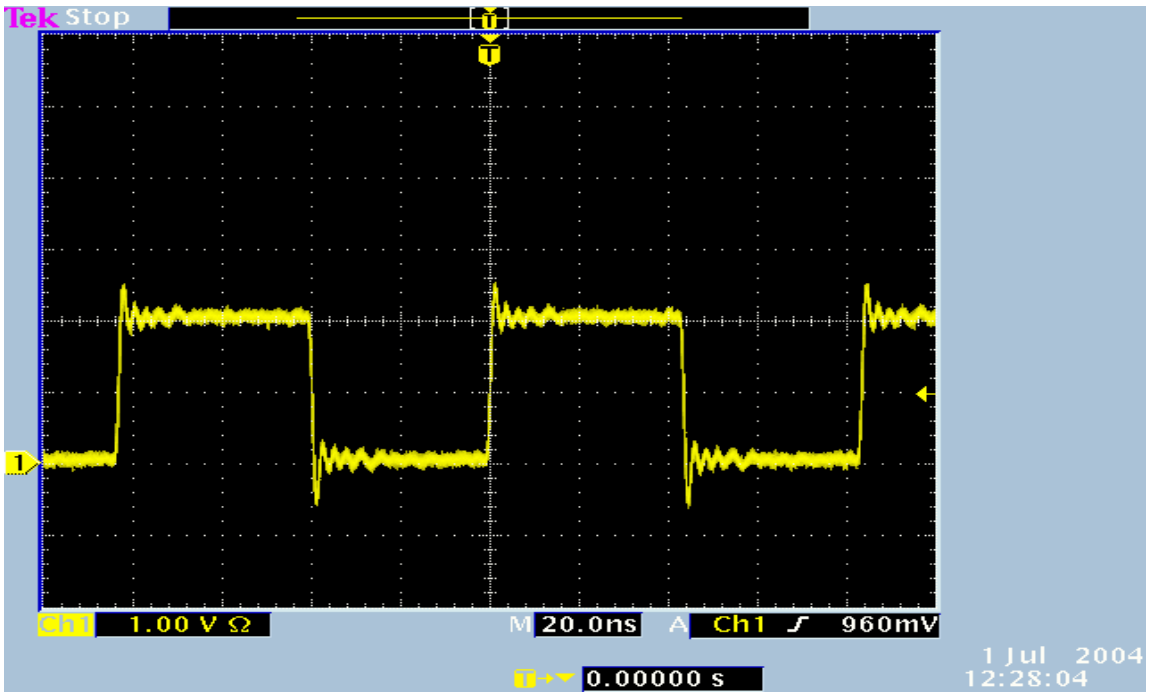
The simulation result is shown in Figure 2-15.

Figure 2-15. Series Termination Simulation Result



The lab measurement shown in Figure 2-16 correlates with the Hyperlynx simulation very well. The 22-ohm series resistor can be modified to lower the overshoots and undershoots. But since the overshoots are less than 0.5V, they are acceptable in this case.

Figure 2-16. Series Termination Lab Measurement



2.5 Ground Grid Effects on TL

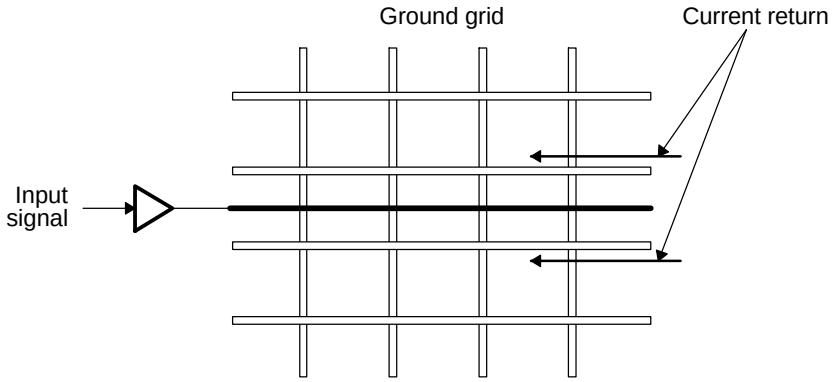
In summary, the simulation results correlate very well with the actual lab measurements. Designers need to understand the TL characteristics and terminate traces to minimize reflections that may cause random circuit failures, excessive noise injected into the power and ground planes and electromagnetic radiation.

One final comment about the TL is that the previous examples were based on a model where a signal trace is on top of a ground plane known as a microstrip model. Other techniques, such as a ground grid, are also commonly used. Example 2 demonstrates the effects of the ground grid. In this configuration, the designers need to understand the current flows and their effect on the characteristic impedance.

Example 2:

Figure 2-17 shows an example of using a ground grid, instead of ground plane for the PC board. As shown in this figure, the current path is not immediately under the signal trace so there is a large current return loop that yields higher inductance and lower capacitance per unit length. In this case, the characteristic impedance is higher than if a continuous ground plane was used.

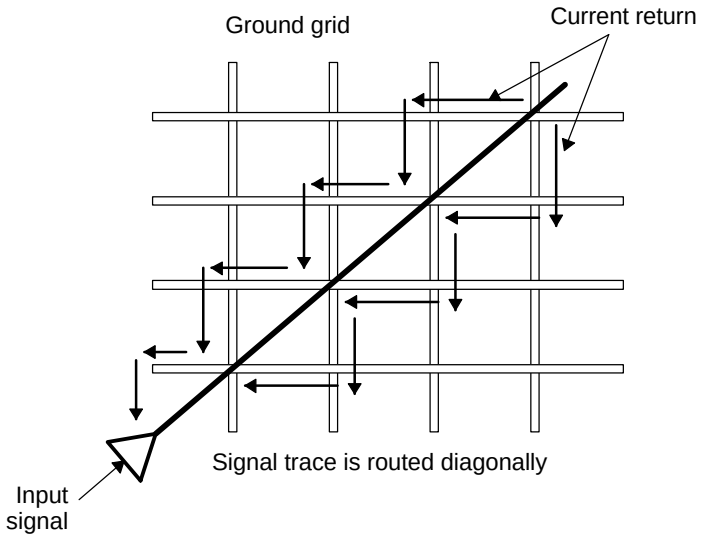
Figure 2-17. Current Return Paths of Ground Grid



Signal trace is routed between the two ground paths of the grid

Figure 2-18 also shows another example of using a ground grid where the signal is being routed diagonally. As shown in this figure, the current return has to travel on a zig zag pattern back to the source and creates a large current return loop that yields higher inductance and lower capacitance per unit length. In this case, the characteristic impedance is higher than using a continuous ground plane and higher than the case where the signal is routed in parallel with the ground grid as shown in Figure 2-17.

Figure 2-18. Current Return Paths for Diagonal Signal Trace



So, if ground grid is a required in a design, the best approach is to route the high speed signals right on top of the grids and parallel to the grid to ensure the smallest current return loops. This lowers the characteristic impedance to the level equivalent to the impedance of the continuous ground plane. This is very difficult to accomplish since complex board has many high speed traces. Therefore, continuous ground plane is still the best method to keep characteristic impedance and EMI low.

Crosstalk

It is not practical nor is it necessary to eliminate all the noise in a DSP system. Noise is not a problem until it interferes with the surrounding circuitry or radiates electromagnetic energy that exceeds FCC limits. When noise interferes with other circuits it is called crosstalk. Crosstalk can be transmitted through electromagnetic radiation or electrically, such as when unwanted signals propagate on the power and ground planes. In order to minimize crosstalk, designers need to understand two very important concepts, high-speed and low-speed current paths and radiated signal traces.

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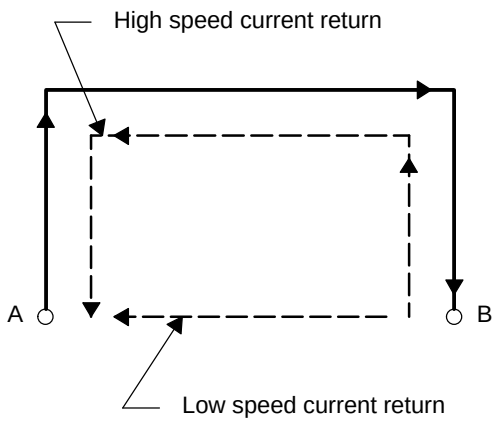
3.1 High-Speed and Low-Speed Current Return Paths **32**
3.1.1 Crosstalk Caused by Radiation **35**

3.1 High-Speed and Low-Speed Current Return Paths

Current returns follow different paths depending on their frequency. Due to skin effect described in Chapter 7 EMI, signals above 10 MHz tend to follow one return path while those below 10 MHz follow another. The low-speed signal current returns on the path of least resistance, normally the shortest route back to the source. The high-speed signal current, on the other hand, returns on the path of least inductance, normally underneath the signal trace. The difference in the behavior of high-speed and low speed signals is shown in Figure 3-1. This concept can be used to optimize the system design to reduce the crosstalk.

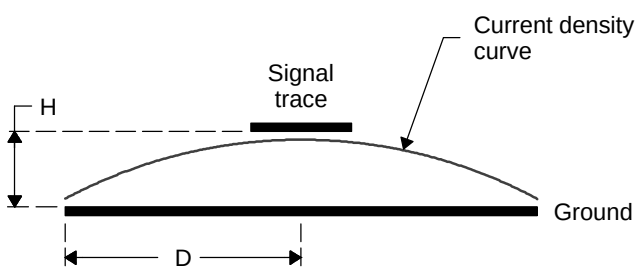
Figure 3-1. Current Return Paths



The current return density and the amount of crosstalk can be estimated as shown in Figure 3-2 and Figure 3-3. Based on the equations shown in the figures, the spacing between the traces and the distance that they run in parallel determines the amount of crosstalk. Obviously, moving the traces further from each other will reduce the crosstalk.

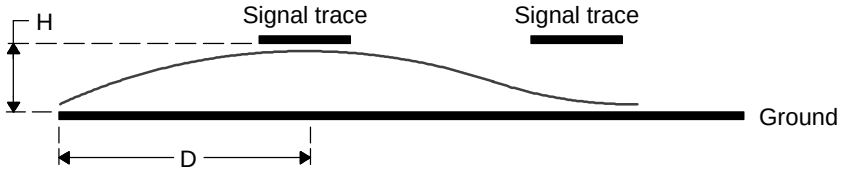
There are two types of crosstalk, forward and backward. Forward crosstalk, also known as capacitive coupled crosstalk, occurs when the current flows in the same direction as the source. With backward crosstalk, which is also called inductive coupled crosstalk, the coupling current flows in the opposite direction of the source, just like in a transformer.

Figure 3-2. Current Return Density (1)



$$\text{Return current density} = I(D) = \frac{Io}{\pi H}\frac{1}{1+\left(\frac{D}{H}\right)^2}$$

Figure 3-3. Crosstalk Estimation (1)



$$\text{Crosstalk} \cong \frac{K}{1 + \left(\frac{D}{H}\right)^2},$$ where K is a constant less than 1 and depends on the risetime and trace length

(1) Source: Howard Johnson's High Speed Digital Design Handbook

The following Hyperlynx simulations demonstrate the concept of forward and backward crosstalk and reducing crosstalk by spacing the aggressor and victim traces. The model simulates two parallel 5 mil wide, 12-inch long traces. The source of the trace is connected to an OMAP processor and the load to DDR memory. As shown in Figure 3-4, D0 line is an aggressor and D1 line is a victim.

Figure 3-4. Crosstalk Simulation Setup

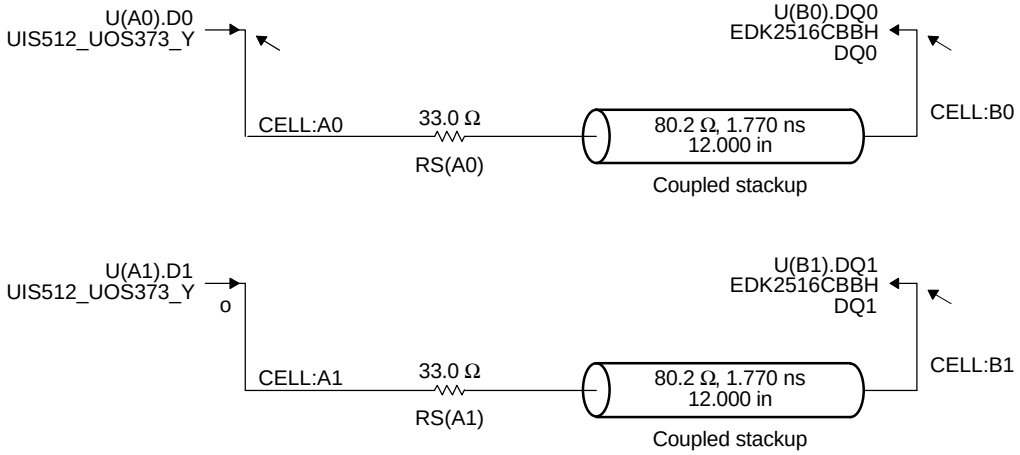


Figure 3-5. Crosstalk Simulation Results for 5 Mil Spacing

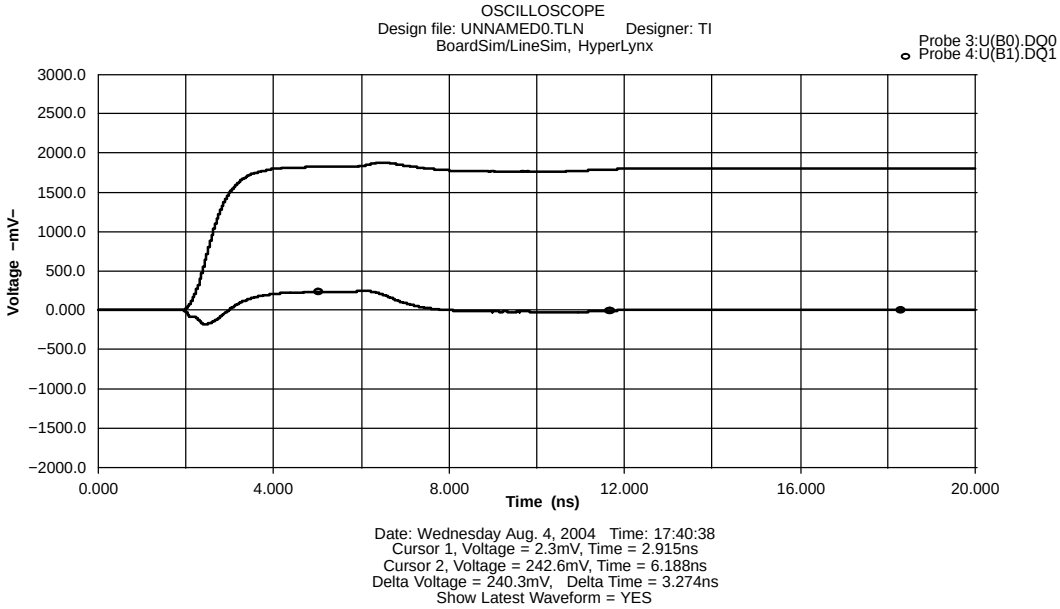


Figure 3-5 shows simulation results. On the victim trace, the first negative-going pulse, which has a –200mV peak, is the forward crosstalk. The positive-going pulse of 240mV is the backward crosstalk. The backward pulse width is about 2 times the coupling region. In this case, the coupling region is 3.54nS and the simulation shows a 4nS backward crosstalk pulse.

The crosstalk can be estimated as

$$\frac{K}{1 + \left[\frac{D}{H}\right]^2},$$

where D is the distance between the traces, H is the height of the signal to the reference plane, and K is the coupling constant less than 1.

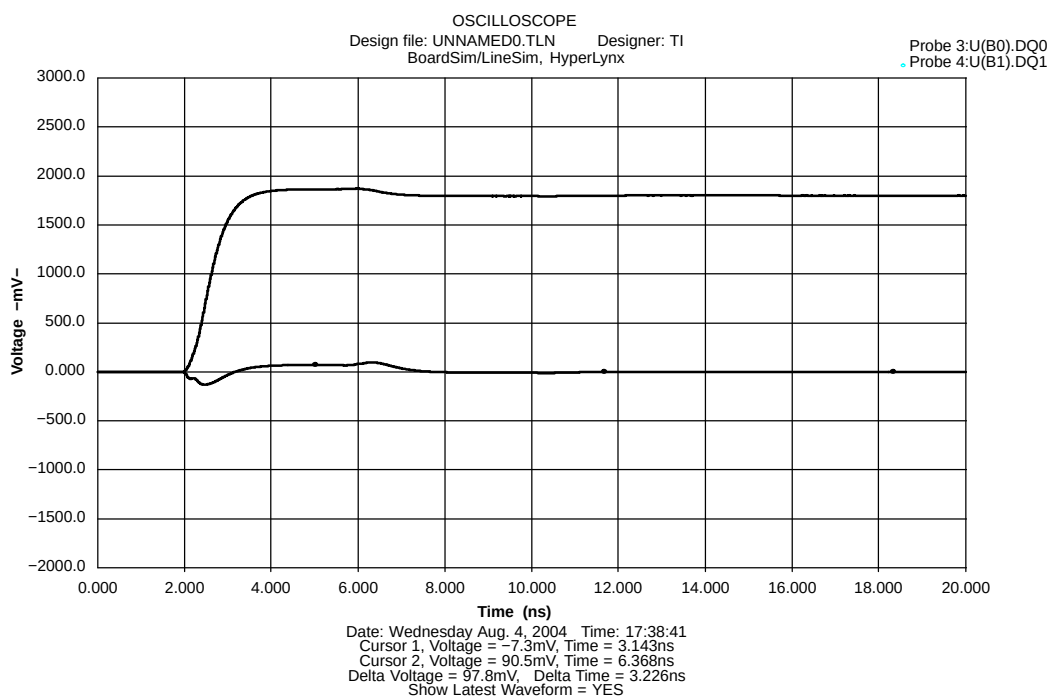
Let us assume that K=1, D=5 mils and H=10 mils as in the Hyperlynx simulation. The maximum crosstalk is then calculated as follows:

$$Max.\ Crosstalk = \frac{K}{1 + \left[\frac{D}{H}\right]^2} = \frac{1}{1 + \left[\frac{5}{10}\right]^2} = 0.8V.$$

As expected, the simulations in Figure 3-5 showed that the peak-to-peak crosstalk is 440mV, which is much less than the maximum crosstalk estimated.

Now, let us test the condition where the two traces are placed further away from each other, by making D=15 mils. The maximum estimated crosstalk is now 0.3V while the simulation in Figure 3-6 shows a forward crosstalk of –100mV and a backward crosstalk of 90mV. The peak-to-peak crosstalk is about 190mV, which is again much less than the calculated maximum of 300mV. This simulation demonstrates how the rule of thumb provided earlier overestimates crosstalk.

Figure 3-6. Crosstalk Simulation for 15 mils Spacing



In summary, accurately calculating and simulating the crosstalk of a system is not possible due to many complex capacitive and inductive coupling paths that are involved. The examples show how difficult it is to estimate and simulate crosstalk and the effects of spacing on the adjacent signal. The following points need to be considered before finalizing the design.

- When the PCB is designed, minimize the height, H, between the high-speed signal routing layer and the ground plane. Lower H yields lower crosstalk.
- Maximize the spacing, D, between the signals. Higher D yields lower crosstalk.
- For board layout, analyze the critical signals and minimize the coupling regions.
- Slow the edge rates if possible because this reduces crosstalk.

3.1.1 Crosstalk Caused by Radiation

Crosstalk can also be caused by high-speed signals that are routed on traces that form effective antennas. The first step in determining whether a trace is acting as an antenna is to calculate the wavelength of the signal using the following equation:

$$\lambda = \frac{C}{f},$$

where C is the speed of light or 3 x 10^8 m/s and f is the frequency in Hertz.

The equation shows that a 100MHz clock signal has a wavelength of 3 meters or 9.84 feet. A good rule for minimizing radiation is making sure that the trace length is not longer than the wavelength divided by 20. So in the case of the 100MHz clock signal, the signal length should be kept below 0.15m or 0.492 feet. Keeping the traces below 0.5 feet is easy but the squarewave clock signal consists of multiple harmonics and each of the harmonics can radiate even when the traces are very short. For example, the fifth harmonic of the 100MHz clock is 500MHz and, at this frequency, a trace of 1.18 inches long can be an affective antenna. The energy of the harmonics depends on the rise and fall times of the signal as shown in Figure 3-7.

Therefore, to minimize the radiating energy, designers need to consider the following.

- Slow down the rise and fall times if possible. Increasing the risetime reduces the power spectral density of the harmonics as shown in Figure 3-7.
- Keep high speed signals as short as possible and make sure that the third and fifth harmonic of the signal is much less than the wavelength divided by 10.
- Shield high-speed signals by adding ground planes between the signal plane.

To demonstrate crosstalk caused by radiation, Figure 3-8 shows a video screen with horizontal lines generated by the third harmonic (55.2MHz) of the 18.4MHz clock radiating to the video circuitry. To eliminate this interference, increase the value of the series termination resistor to slow down the rise and fall times. This reduces the power spectral density of the harmonics, eliminating the interference as shown in Figure 3-9.

Figure 3-7. Radiation Caused by Clock Signal

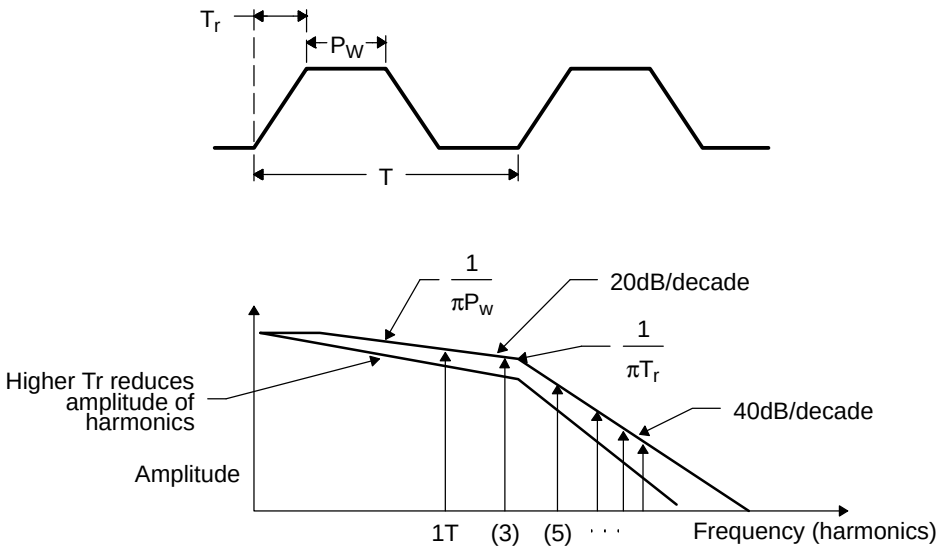


Figure 3-8. Clock Harmonic Interfered with Video

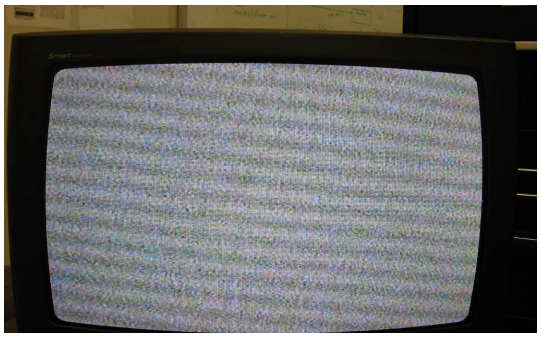
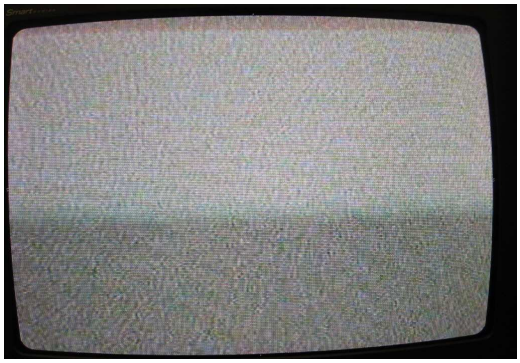


Figure 3-9. Interference Reduction by Increasing the Risetime



DSP Power Supply Design

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4.3 Power Supply Decoupling Techniques 41

4.1 Importance of Power Supply Design

Power supply design is perhaps the most challenging aspect of the entire process of controlling noise and radiation in high-speed DSP design. This is largely because of the complexity of the dynamic load switching conditions. These include the DSP going into or out of low power modes, excessive in-rush current due to bus contention and charging decoupling capacitors, large voltage droop due to inadequate decoupling and layout, and oscillations that overload the linear regulator output. A clean and stable power supply design is required for all DSP systems. Figure 4-1 and Figure 4-2 show two circuits, one of which, Figure 4-2, has a decoupling capacitor close to the DSP. Assuming the same power supply trace inductance, a larger dynamic current return path leads to larger power supply voltage droop and greater electromagnetic radiation. This may cause random system failures that are very difficult to debug.

Figure 4-1. Power Supply Current Return Path Example 1

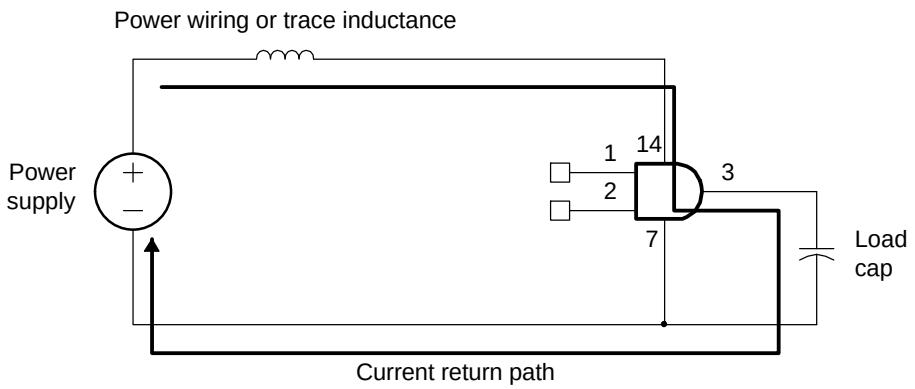
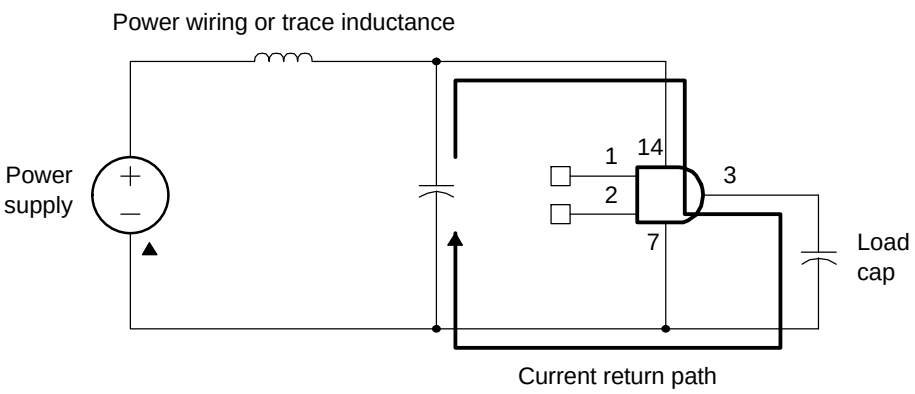


Figure 4-2. Power Supply Current Return Path Example 2



One of the most challenging tasks for system designers is determining an acceptable noise level for a DSP in an particular application. DSP data manuals clearly specify the operating conditions but cannot account for the dynamic nature of high-speed systems. This is because the dynamic switching characteristics very much depend upon on the actual system design and layout. The following are some of the important issues that must be addressed during the power supply design process:

- Power supply transient response, such as load regulation, line regulation, power supple ripple, power supply noise rejection, and power sequencing for multiple rails
- Power supply decoupling to ensure minimum voltage droop at the pins of the DSP
- Linear regulator versus switching regulator
- Power supply planes versus power supply traces
- DSP in-rush currents during power supply ramp and at steady state
- Power cycling: no residual voltage during DSP startup
- Power supply rails sequencing: Core before IO or IO before Core
- Be careful with using a switching regulator to power the PLLs, audio CODECs and video encoders and decoders
- Always asserting reset during power supply ramp to reduce the probability of internal DSP bus contention

4.2 DSP Power Supply Architectural Considerations

Excessive power supply noise can have the following harmful effects:

- Voltage droop, inadequate decoupling capacitors, or current starvation may cause random logic failures. This is very difficult to debug and may even require a re-design of the system to get rid of the noise.
- Inadequate voltage regulation can cause reliability problems or unintentional system shutdown.
- Excessive jitter may appear on clock circuits, especially the PLL.
- Radiation may rise to a level that makes it difficult to pass EMC tests.
- Visible and audible artifacts on video and audio systems.

Designers have three primary methods to overcome these problems: voltage regulator design (linear versus switcher), decoupling techniques, and PCB layout. One of the most important decisions made by designers is whether to use linear regulators or switching regulators. This decision requires a good understanding of the characteristics of the power supply and the impact of the supply on the system noise performance. The design of the power supply itself is beyond the scope of this document. Let us look at the differences between linear and the switch regulators:

Table 4-1. LDO versus Switching Regulators

Linear or Low Drop Out (LDO) Regulators	Switching Regulators
Low noise with high power supply rejection ratio	Switching noise may cause EMI problems or video and audio artifacts
Fast response to load changes, typical 1 µs	Slow response to load changes
Low efficiency, typically 56%, may increase power dissipation, heatsinks may be required	High efficiency, typically 92%, provides low power dissipation
Unstable if the total decoupling capacitance is higher than the maximum limit	Decoupling capacitance has a little or no impact on the supply stability. On the other hand, PCB layout is critical.
Excellent choice for video, audio and PLL circuits.	Excellent choice for the core CPU and the IO power.
Low cost	Higher cost due to need for external filter components such as an LC filter at the output of the switch

Table 4-1 will help determine which power supply solution is a better fit for the application. The next step is to determine the current consumptions and whether or not power sequencing is required. In general TI DSPs have a minimum of two power supply rails, Core and IO. The sequence of ramping the Core and IO voltages can affect the startup current consumption so refer to the device data manuals to help design a robust power supply for a particular DSP. Here are recommended rules for selecting a DSP power supply.

CORE Voltage Regulator Design:

- Refer to the device data manual to get the maximum current consumption for the Core supply. Many of the TI DSPs come with a Power spreadsheet that can be used to estimate the current consumption of a particular CPU operating condition.
- Select a regulator with at least two times the maximum Core current capability. This provides adequate margin to handle the dynamic current condition.
- Be careful with the current starvation condition. During startup, the surge current may exceed the maximum limit of the regulator for a short period of time. The selected regulator should have a soft-start capability to prevent thermal or over-current shutdown conditions from occurring.
- The final design step for the Core voltage regulator is whether or not a heatsink is required.

IO Voltage Regulator Design:

IO voltage regulator design depends on the external loads in the specific application. For fast switching signals, the IO currents are supplied by the decoupling capacitors, not by the regulator itself due the parasitic inductance associated with the power supply trace and plane. The dynamic current calculation will be shown in the decoupling section. The following guidelines provide a conservative method to design an IO voltage regulator for the DSP itself. It should be noted that this method applies to the DSP power alone as opposed to the entire system.

- Count the number of outputs from the DSP. All GPIOs should be considered as outputs.
- Multiply the number of outputs by the source current specified in the data manual.
- Add the total source current using the maximum IO current consumption specified in the data manual.
- Then, multiply the result by 2 to provide a 100% margin.
- Due to transmission line effects, IO current may surge during switching but this condition will be absorbed by the local DSP decoupling capacitors.
- The final step is to determine if heatsink is required or not.

Once designers complete the power supply architecture for a particular DSP, the next step is to determine if the DSP requires sequencing. The supply rails may be sequenced, for example, to ramp up the Core before the IO or vice versa. Proper sequencing is necessary to avoid internal contention.

- Improper reset during power-up. Reset must be asserted longer than the minimum reset pulse specified in the data manual.
- Core and IO not coming up within the specified time limits. Typically, TI DSPs do not require a power sequence but there is a time limit for one supply rail to be on while the other is off.
- Improper reset of the JTAG emulation port. For example, TRST needs to be stable low. Excessive noise coupled to this signal may cause a startup problem or bus contention.
- Boot mode configuration pins not being driven to proper states before releasing reset. Refer to the device data manual to make sure that the configuration pins have proper pull-ups and pull-downs and these pins have reached a stable logic level before releasing reset.

Figure 4-3 and Figure 4-4 show two C67xx DSP power supply architectures. In Figure 4-3, the Core and IO rails are powered up synchronously and in Figure 4-4 the Core supply rail is ramped up before the IO. Refer to the http://www.ti.com web link to obtain reference designs of these architectures.

Figure 4-3. Synchronous Core and IO Supply Rails Example

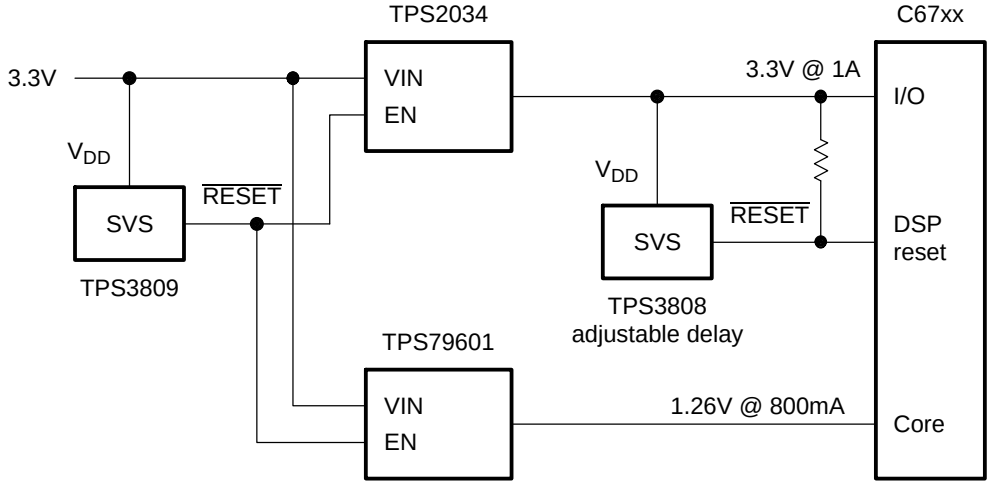
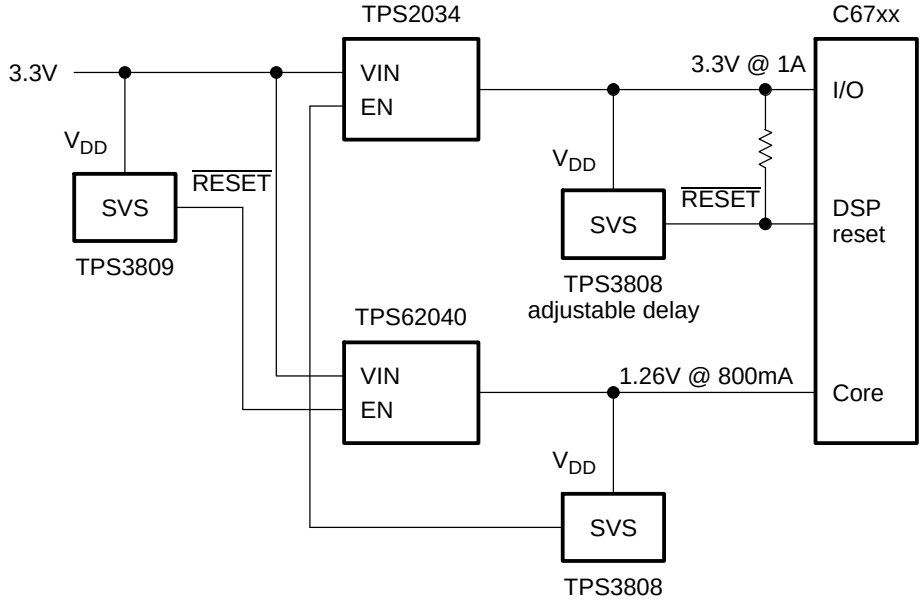


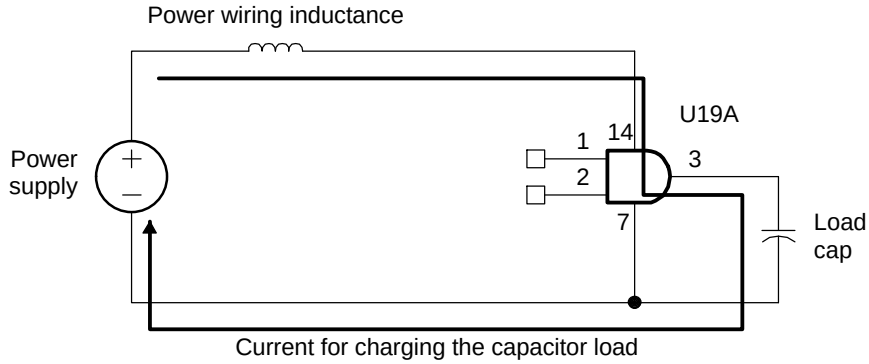
Figure 4-4. Core Before IO Example



4.3 Power Supply Decoupling Techniques

Once designers select a supply architecture for the DSP, the next step is to determine the decoupling capacitors needed to ensure that the power supply droop under all dynamic operating conditions is lower than the specified limits. For example, a 5% tolerance rating on a 3.3V IO supply requires the ripple to be less than 165mV. Let us first consider the situation where no decoupling capacitor is used as shown Figure 4-5.

Figure 4-5. DSP Power w/o Decoupling Capacitor



In Figure 4-5, the DSP labeled U19A is driving a capacitive load and is switching at a fast rate. Now, let us assume that the regulator is placed 5 inches away from the DSP and is routed with a 5 mil trace to the DSP. During fast switching, the power supply trace becomes an open circuit because of the parasitic inductance associated with the trace. This generates a large voltage droop at the pin of the DSP which can be estimated as follows.

$$Droop = L\left(Max\frac{dI}{dt}\right),$$

where L is the parasitic inductance.

$$Max\frac{dI}{dt} = \frac{1.52\Delta V}{(T_r)^2}C,$$

where ΔV is a switching voltage, C is a load capacitor and Tr is a risetime.

For a 5 inch trace, the inductance is estimated by the Hyperlynx simulator to be 600nH/m. The inductance L is

L = 5 in x 2.5 cm/in x 1m/100cm x 600nH/m = 75nH.

Let Tr = 2nS, C=50pF (load capacitance) and delta V = 80% of 3.3V or 2.64V.

The maximum calculated droop is

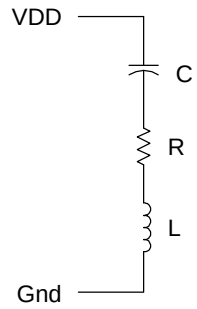
$$Droop = L\left(Max\frac{dI}{dt}\right) = L\left[\frac{1.52\Delta V}{(T_r)}C\right] = 75 \times 10^{-9}\left[\frac{1.52(2.64)}{(2 \times 10^{-9})^2} \times 50 \times 10^{-12}\right] = 3.76V.$$

This example demonstrates that, for a 5 inch trace, 2ns signal, 50pF load and 3.3V IO, the maximum power supply droop is 3.76V. This level of droop is almost certain to cause random system failures. To compensate, decoupling capacitors are placed close to the DSP to provide the required charge during switching. What is the best method to decouple the noise from the DSP system? Noise characteristics differ so much from one system to another that no method guarantees low noise and low radiation for all cases. However, designers can apply best practices outlined here to minimize the noise and to improve the probability of success. This document presents a general rule-of-thumb decoupling method and an analytical decoupling method. Before going into the rules for decoupling, it is important to understand the characteristics of capacitors, inductors and ferrite beads.

4.3.1 Capacitor Characteristics

The key specification of a capacitor used for decoupling is the self-resonant frequency. The capacitor remains capacitive below and starts to appear as an inductor above this frequency. Here is a series equivalent circuit representing the capacitor.

Figure 4-6. Capacitor Equivalent Circuit



The series equivalent circuit for a capacitor has three different components, equivalent series resistance (ESR), equivalent series inductance (ESL) and the capacitance itself. The self-resonant frequency happens at the point where the impedance of the capacitor, C, is equal to the impedance of the inductor, L.

$$Z_c, capacitor = \frac{1}{\omega C},$$

where C is capacitance and ω is 2π times the frequency, f.

$$Z_L, indicator = \omega L,$$

where L is inductance.

At resonance, Z_L is equal to Z_c or

$$\frac{1}{\omega C} = \omega L,$$

$$\omega^2 = \frac{1}{LC},$$

$$\omega = \frac{1}{\sqrt{LC}}, \text{ where } \omega = 2\pi f.$$

Therefore, the self-resonant frequency is

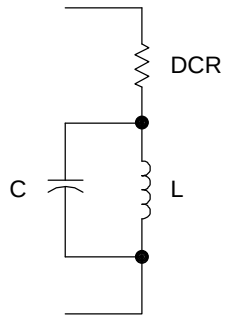
$$f = \frac{1}{2\pi\sqrt{LC}}.$$

As shown in the self-resonance equation, lower capacitance and lower inductance yield a higher resonant frequency. For a given capacitance value, choosing a smaller surface mount component, for example a 0603 part, achieves a higher self-resonant frequency is because a smaller component package typically has lower parasitic and lead inductance. The whole decoupling concept is to provide a low impedance path from the power supply to ground and to shunt the unwanted RF energy. This means that choosing a capacitor with high capacitance but low inductance and impedance is very important.

4.3.2 Inductor Characteristics

The inductor also has a self-resonant frequency. The inductor remains inductive below and starts to appear as a capacitor above this frequency. Here is a series equivalent circuit of the inductor:

Figure 4-7. Inductor Equivalent Circuit



The formula for calculating the resonant frequency of an inductor is the same as for a capacitor:

$$f = \frac{1}{2\pi\sqrt{LC}}.$$

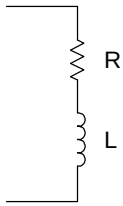
Here are some general rules for using inductors to filter noise in a DSP system.

- Inductors are expensive and are sensitive to noise. Depending on the switching speed of the signals propagating through it, an inductor can also generate noise.
- Inductors are commonly used to filter low frequency noise in high current applications. This practice should be avoided because inductors behave like a short circuit for high frequency noise.

4.3.3 Ferrite Bead Characteristics

Ferrite beads have electrical characteristics that are similar to inductors. The key difference is that the ferrite bead has no or negligible parasitic capacitance. So the ferrite bead behaves like an inductor over a very wide frequency range. As shown in Figure 4-8, ferrite bead has only a series resistance so be careful with the IR drop when using it in a system. The ferrite bead performs very well at frequencies higher than 30MH. So it is commonly used to isolate power supplies and noise sensitive circuits such video and audio CODECs.

Figure 4-8. Ferrite Bead Equivalent Circuit



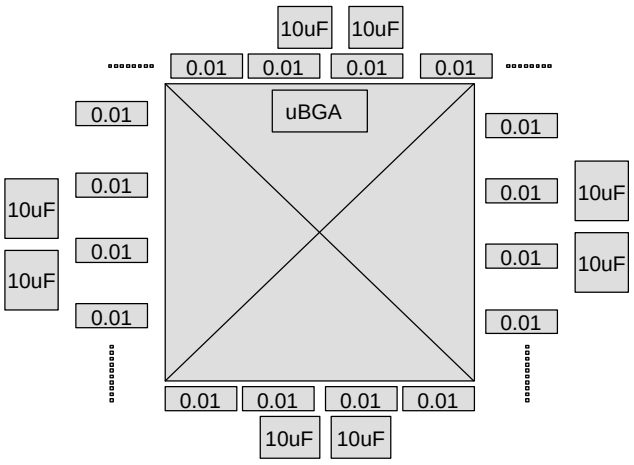
4.3.4 General Rule-Of-Thumb Decoupling Method

In general, the ideal way to decouple the supply noise is having one capacitor between each of the power and ground pins of the DSP. Normally, this is physically impossible because the DSP package area is too small. So, designers have to compromise by reducing the number of decoupling capacitors to fit in the general area underneath the DSP. Refer to the device data manual for a recommended method. But in general, here are the important considerations for decoupling.

- Add as many decoupling capacitors as space allows.
- Add at least 8 bulk capacitors, 4 for Core and 4 for IO supplies. Place each bulk capacitor at each region of the DSP, with region being defined as an edge or a corner of the DSP. Bulk capacitors act as a low frequency noise filter and a charge storage device for the small decoupling capacitors. The use of four smaller bulk capacitors is preferable to one large discrete component because this guarantees a shorter recharge path and a lower parasitic inductance path between the bulk and the decoupling capacitors.
- Keep in mind that all capacitors have equivalent series inductance (ESL) and equivalent series resistance (ESR). ESL and ESR reduce filtering effectiveness. So, select smallest surface mount capacitors that can be used.

Figure 4-9 demonstrates a good scheme for decoupling a particular DSP. Refer to the device data manual to find more details. As shown in this figure, 0.01uF ceramic capacitors are used for the decoupling capacitors and 10uF tantalum capacitors are used as low frequency filtering components. Typically, designers have to go back and change the values to optimize them for their applications. A good approach is changing the capacitor values to achieve less than 50mV power supply ripple for the IO rail and less than 20mV for the Core rail. Another good rule is to use ceramic capacitors for decoupling and tantalum capacitors for low frequency filtering. This is because tantalum capacitors come in higher values than ceramic capacitors. These two types of capacitors provide the low ESR and ESL that is needed for low noise designs operating over a wide range of voltages and temperatures.

Figure 4-9. General Rule for Decoupling



4.3.5 Analytical Method of Decoupling

Another method of decoupling power supply noise from a DSP system is calculating the total capacitance required to keep the power supply ripple under a certain limit. Similar to the general rule of decoupling, this method provides a starting value that must typically be optimized. The large ball grid array (BGA) package typically used for DSPs behaves like a PCB itself with long traces routing from the die out to the balls. These traces can generate interference and are susceptible to crosstalk, power supply droop and other electrical noise. The asymmetry decoupling technique begins with dividing the DSP into 4 regions and then decoupling each region separately. Providing fewer decoupling capacitors in the low speed section leads to a uniform reduction in noise and electromagnetic radiation. The rules for this decoupling technique are:

Core Voltage Decoupling Steps:

1. Divide the DSP package into 4 regions by drawing two diagonal lines across the 4 corners of the DSP as shown in Figure 4-10.
2. Estimate the current consumption of the Core voltage in the region, $\mathbf{I}_{CRegion}$, as shown in the equation below by taking the maximum device current, $\mathbf{I}_{Core}$, divided by the total number of Core voltage pins, **N**, and multiplied by the number of Core voltage pins, **M**, within a region.

$$I_{CRegion} = \frac{I_{Core}}{N} xM$$

3. Calculate the total decoupling capacitance for the region by applying the equation below.

$$I_{CRegion} = C\frac{dV_{Core}}{dt},$$

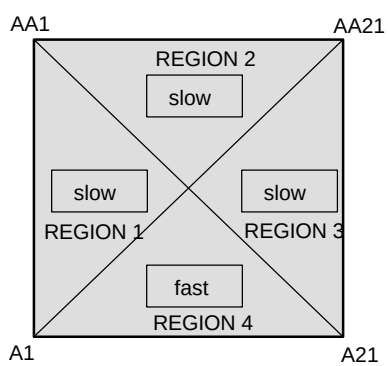
$$C = I_{CRegion} = \frac{dt}{dV_{Core}},$$

where dt is the fastest risetime in the region and dV is the maximum ripple allowed for the Core voltage, assuming 10 mv ripple.

is the maximum ripple allowed for the Core voltage, assuming 10mv ripple.

4. Now, calculate the total bulk capacitance for the region by multiplying the total decoupling capacitance by 40. The rule recommended by Henry Ott for bulk capacitance is at least 10 times the decoupling capacitance. Use one bulk capacitor per region to minimize the parasitic inductance between the bulk and the decoupling capacitors.
5. To figure out the number of decoupling capacitors, review the PCB area to see how many capacitors can be placed within 1.25 cm of the power supply pins. Then, to find the decoupling capacitor value, divide the total capacitance by the number of capacitors allowed for the region. It is good to select a capacitor with the self-resonant frequency equal to the maximum frequency of the particular region. For example, if the SDRAM port runs at 100MHz, then add at least one capacitor with the resonant frequency of 100MHz in this region. The other capacitors within each region should have the highest possible resonant frequency. This helps mitigate EMI over a wide frequency range.

Figure 4-10. Analytical Decoupling Technique



IO Voltage Decoupling Steps:

1. Divide the DSP package into 4 regions by drawing two diagonal lines across the 4 corners of the DSP as shown in Figure 4-10.
2. Count the number of IO voltage, and inputs and outputs of each region.
3. Estimate the IO current consumption of the DSP itself in the region, $\mathbf{I}_{IORegion}$, as shown in the equation below by taking the maximum device current specification, $\mathbf{I}_{IO}$, divided by the total number of IO voltage pins, **K**, and multiplied by the number of IO voltage pins, **J**, within a region.

$$I_{IORegion} = \frac{I_{IO}}{K} xJ$$

4. As designers know, the total IO current is not equal to the IO current consumption of the DSP itself. The majority of the total IO current depends on the external loads, for example resistive, capacitive or transmission line. In this design, let's assume a worse case scenario where all the IOs are outputs and

are loaded with transmission lines. In this case, each output current is equal to the output voltage divided by the characteristic impedance of the transmission line, Z_o.

$$I_{IOTrans} = \frac{V_{IO}}{Z_o}$$

5. The total IO current for the region is

   $$I_{IOTrans} = I_{IORegion} + J \times I_{IOTrans}$$

6. Calculate the total decoupling capacitance for the region by applying the equation below.

   $$I_{IOTotal} = C\frac{dV_{IO}}{dt},$$

   $$C = I_{IOTotal}\frac{dt}{dV_{IO}},$$

   where dt is the fastest risetime in the region and dV is the maximum ripple allowed for the IO voltage, assuming 50 mv ripple.

   where dt is the fastest risetime in the region and dV is the maximum ripple allowed for the IO voltage, assuming 50mv ripple.

7. Now, calculate the total bulk capacitance for the region by multiplying the total decoupling capacitance by 40. The rule recommended by Henry Ott for bulk capacitance is at least 10 times the decoupling capacitance. Use one bulk capacitor per region to minimize the parasitic inductance between the bulk and the decoupling capacitors.
8. To figure out the number of decoupling capacitors, review the PC board area to see how many capacitors can be placed within 1.25 cm of the pins. Then, to find the decoupling capacitor value, take the total capacitance value just calculated and divide it by the number of capacitors allowed for the region. It is good to select a capacitor with the self-resonant frequency equal to the maximum frequency of the particular region. For example, if the SDRAM port runs at 100MHz, then add at least one capacitor with the resonant frequency of 100MHz at this region. For the rest of the capacitors within that region, select a highest possible resonant frequency value.

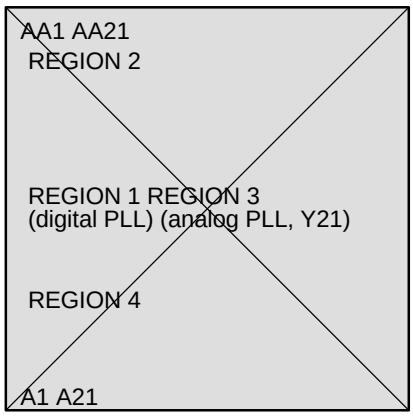
This analytical decoupling method provides designers with a good starting point. As mentioned earlier, designers need to optimize the decoupling capacitors to ensure low noise and EMI during the board characterization process. The following example shows how this process can be applied to a typical design.

Example 3:

Divide the OMAP5910 289-pin GZG package into four regions by drawing two symmetry lines across the part. Then count the number of Core voltage pins, I/O voltage pins and signals, not including the ground pins, in each region. Also, pay special attention to the critical sections such as external memory interface fast (EMIFF), phase-locked loop (PLL) and other high-speed serial/parallel ports. Assume all IOs are outputs driving a 60 ohms transmission line.

Figure 4-11. OMAP GZG Package Diagram

Bottom view of the OMAP5910 package



REGION 1: 3 Core voltage pins, 8 I/O voltage pins, and 54 input/output pins

REGION 2: 3 Core voltage pins, 4 I/O voltage pins, and 59 input/output pins

REGION 3: 3 Core voltage pins, 3 I/O voltage pins, and 59 input/output pins

REGION 4: 4 Core voltage pins, 6 I/O voltage pins, and 55 input/output pins

The next step is to conservatively estimate the switching current requirements for each Region.

Table 4-2 shows the calculations of switching currents for all four Regions. The conservative assumptions used to calculate the capacitors on Table 4-1 are:

- Maximum Core current = Typical Current x 2 plus 100% margin = 170mA x 2 x2 = 680mA.
- Device IO current = Typical IO current x 2 plus 100% margin = 45mA x 2 x 2 = 180mA.
- Assume that half of the inputs and outputs in the Region switching at the same time driving 60-ohm transmission lines. This is a very conservative assumption since many of the signals in the Region are too slow to be considered as transmission lines.

Table 4-2. Switching Current Estimation

Region	Total Peak Core Current	Device IO Current	IO Current for Driving Transmission Lines	Total IO Current
Region 1	$\frac{680mA}{13} x3 = 157mA$	$\frac{180mA}{21} x8 = 69mA$	$\frac{3.3}{60} x27 = 1.5A$	69mA+1.5A=1.57A
Region 2	Same as 1, 157 mA	$\frac{180mA}{21} x4 = 34mA$	$\frac{3.3}{60} x30 = 1.65A$	1.65A + 34mA = 2A
Region 3	Same as 1, 157 mA	Same as 2, 34mA	Same as 2, 1.65A	Same as 2, 2A
Region 4	$\frac{680mA}{13} x4 = 290mA$	$\frac{180mA}{21} x6 = 51mA$	$\frac{3.3}{60} x27 = 1.5A$	1.5A + 51mA = 1.55A

4.3.6 Calculating Decoupling Capacitor Value

Since the Core and I/O voltage operate at different frequencies, they require separate decoupling calculations. The following shows the steps needed to calculate and select the decoupling capacitors for both Core and I/O supplies.

To find the decoupling capacitance, plug the peak current, the risetime and the maximum ripple voltage parameters into the equation below and solve for C. It is acceptable to assume that the maximum ripple voltage is 10mV for Core and 50mV for IO and the typical risetime is 2nS.

$$C = I_{CRegion} \frac{dt}{dV_{Core}}$$

Use the capacitor equation below to calculate the total capacitance for the IO voltage decoupling:

$$C = I_{IOTotal} \frac{dt}{dV_{IO}}$$

Now let us calculate the total capacitance required for each region :

Region 1: Total Core capacitance,

$$C = 157mA \frac{(2nS)}{(10mV)} = 0.03\mu F$$

$$C = 157A \frac{(2nS)}{(50mV)} = 0.06\mu F$$

There are three core voltage pins operating at 150MHz (CPU frequency) and 8 I/O voltage pins operating at 40MHz (EMIFS frequency). It would be desirable to use multiple capacitors for the multiple supply pins but there is a physical limitation due to the limited space available around the device. For the OMAP5910

GZG package, there is enough board space to place about 4 or 5 capacitors per region. In this case, select two capacitors with the total capacitance of around 0.03uF. At least one of the capacitors should have a self-resonant frequency around 150MHz to decouple the Core voltage pins in Region 1. Then, select three capacitors with a total capacitance of around 0.06uF with at least one of the capacitors having the self-resonant frequency around 75MHz to decouple the I/O voltage pins in Region 1.

In summary, for Core voltage in Region 1, use two 0.022uF (0.044uF total) ceramic capacitors and, for the I/O voltage, use three 0.022uF (0.066uF total) ceramic capacitors.

The next step is calculating the bulk capacitors for both Core and IO. Bulk capacitor placement is not as critical as decoupling capacitor placement. But bulk capacitors are needed to filter the low frequency ripple typically generated by switching power supply and to recharge the decoupling capacitors.

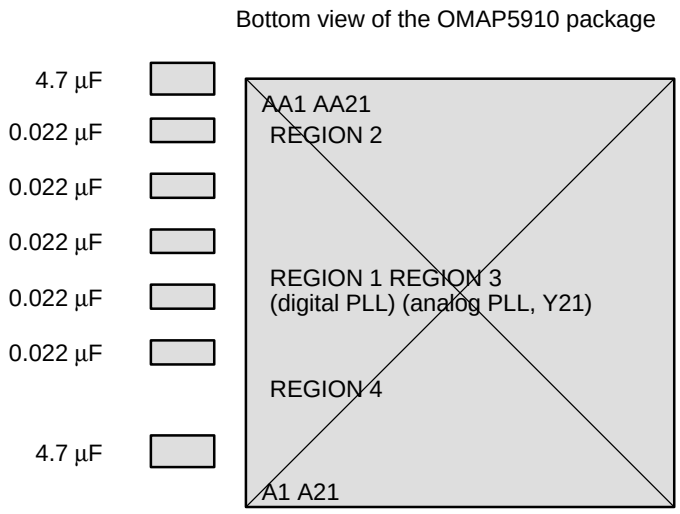
A rule of thumb is to select bulk capacitors with at least ten times the total decoupling capacitance. Let us use 40 times to be conservative. For the Core voltage,

40 x total Core capacitance = 40 x (0.03uF) = 1.2uF for Region 1 of the Core voltage and
40 x total IO capacitance = 40 x 0.066uF = 2.64uF for Region 1 of the IO voltage

As mentioned earlier in this document, the best technique is adding 4 bulk capacitors to 4 regions of the OMAP and the smallest tantalum capacitor available is 4.7uF. In this case, select 4.7uF tantalum bulk capacitors for both IO and Core voltages in Region 1.

In summary, Figure 4-12 shows a complete schematic diagram for decoupling Region 1 of the OMAP5910 DSP. Designers can repeat the calculations for other regions of the DSP if they wish.

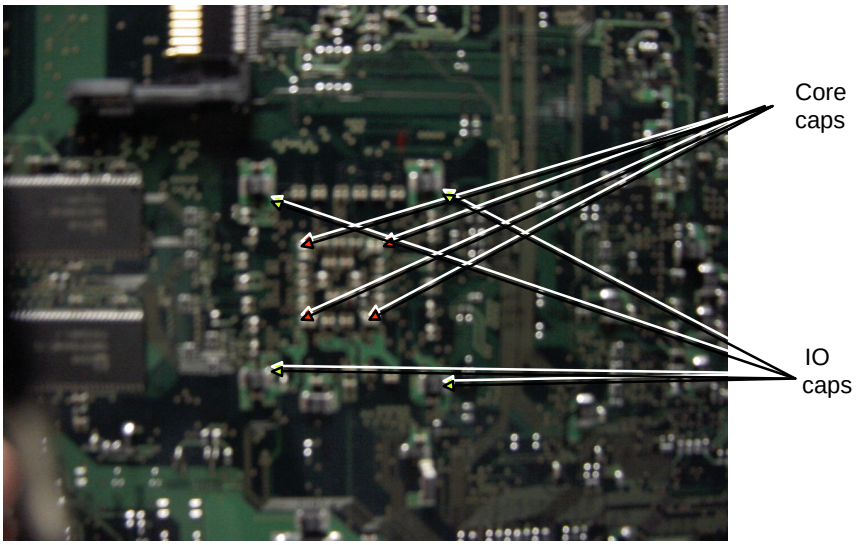
Figure 4-12. Region 1 Decoupling Capacitors Example



4.3.7 Placing Decoupling Capacitors

It is very important to place all the decoupling capacitors as close as possible to the pins, no more than 1.25cm in most cases. The bulk capacitors should be placed as close as possible to the decoupling capacitors. This reduces the trace lengths, reducing the current loops and in turn lowering radiation while minimizing parasitic inductance. The best strategy is placing the decoupling capacitors on the bottom of the PCB and the bulk capacitors on top. In summary, there should be two bulk capacitors per region, one for Core and one for IO, and as many decoupling capacitors as space allows. Figure 4-13 shows a very good example of the capacitors placement on the bottom side of the PCB. The Core decoupling capacitors and four large bulk capacitors are placed on the interior of the BGA package in the open space right under the DSP. The IO decoupling and bulk capacitors are placed on the perimeter of the BGA package.

Figure 4-13. Good Decoupling Capacitors Placement



4.3.8 High Frequency Noise Isolation

The decoupling methods described up to now filter noise locally at the DSP. There are cases where the whole power supply plane for some critical sections needs to be isolated. This may be required to prevent external noise from entering these sections or to prevent noisy circuits such oscillators from radiating onto the power plane. The power supply plane is generally isolated using either Pi or T filters. A Pi filter is constructed with two capacitors and one ferrite bead while a T filter requires one capacitor and two ferrite beads. Each of these filters is commonly used in series with the signals exiting and entering the system or the power supply to reduce the radiated emissions. The passband of the filter has to be calculated precisely to ensure that the bandwidth is wide enough to pass the desired signals without degrading signal quality, especially critical parameters such as rise and fall times and amplitude.

Figure 4-14. Pi Filter Circuit for High Speed Signals

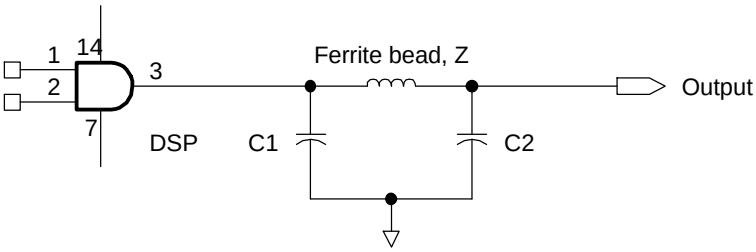


Figure 4-15. T Filter Circuit for High Speed Signals

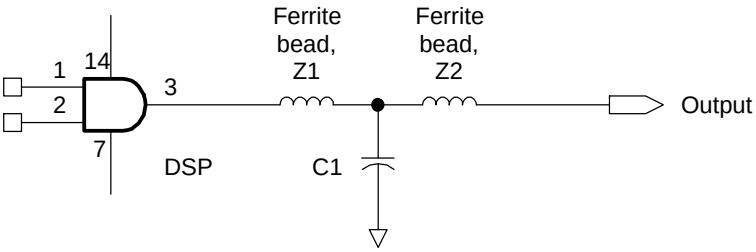
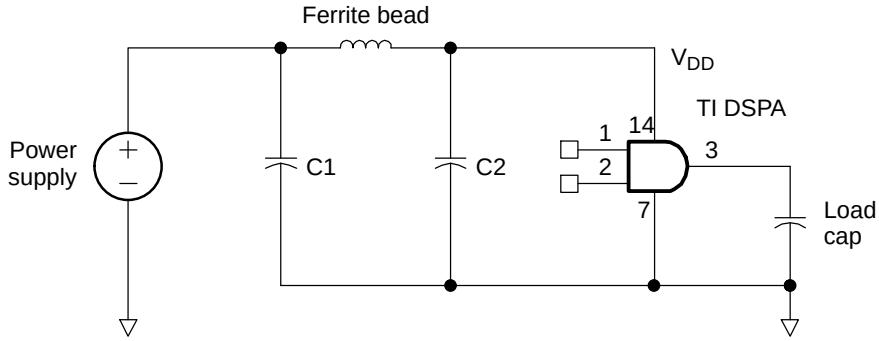


Figure 4-16. Pi Filter Circuit for Power Supply Isolation



The filter bandwidth is calculated as follows:

For Pi filter in Figure 4-14, starting from the DSP output, the first parallel component is C1, second series component is Z and third parallel component is C2. Therefore, the bandwidth of this filter is determined by the two poles formed by the output impedance of the DSP, C1, the ferrite bead, and C2. The first -3dB corner frequency of the filter is

$$f_{-3dB} = \frac{1}{2\pi Z_o C_1},$$

where Z_o is the output impedance of the DSP.

The second -3dB corner frequency of the filter is

$$f_{-3dB} = \frac{1}{2\pi Z C_2},$$

where Z is the impedance of the ferrite bead.

To design the filter, always let C1 equal C2 and only calculate the second -3dB corner frequency. This is because the output impedance of the DSP is very small, which makes the first corner frequency large enough that it has no effect on the signal bandwidth. Why do we need C1 at all? The answer is that C1 becomes an important component when an external source couples back into the DSP. In this case, the first pole composed of C1 and ferrite bead dominates and helps eliminate the RF noise. Another rule of thumb for designing this type of filter is to make the filter's -3dB corner frequency at least 10 times the signal bandwidth.

Pi Filter Design Example:

Let us design a Pi filter for a graphic controller's Red, Green, and Blue (RGB) analog signal output used to drive a monitor. Assuming that RGB signals have 30MHz bandwidth, calculate the filter components as follows.

f-3dB = 10 x 30MHz = 300MHz

Since the filter is dominated by the second pole:

$$f_{-3dB} = \frac{1}{2\pi Z C_2} = 300MHz.$$

Let Z be 100 ohms, a typical ferrite bead value, then C2 is

$$= \frac{1}{2\pi (100) 300 \times 10^6} = 5.3pF.$$

The next capacitor size larger than 5.3pF is 10pF, so select both C1 and C2 capacitors to be 10pF. Place these components as close to the RGB connector as possible. This blocks any RF energy coupled to the signal traces from radiating outward while preventing noise from entering the DSP system.

Looking out from the DSP for the T filter shown in Figure 4-15, the first series component is Z1, the second parallel component is C1, and the third series component is Z2. Just as in the Pi filter, these three components make up a two-pole filter with the first pole consisting of Z1 and C1 and second pole consisting of Z2 and the load capacitor. The first -3dB corner frequency is

$$f_{-3dB} = \frac{1}{2\pi Z_1 C_1}$$

and the second corner frequency is

$$f_{-3dB} = \frac{1}{2\pi Z_2 C_{Load}}.$$

The design rules for the T filter are the same as the rules recommended for the Pi filter. The -3dB corner frequency should be ten times the signal bandwidth and the ferrite beads Z1 and Z2 must have the same impedance characteristics.

T Filter Design Example:

Let us design a T filter for the RGB analog signals output from a graphics controller to drive a display monitor. Assuming that the RGB signals have 30MHz bandwidth, the filter components can be calculated as follows.

f-3dB = 10 x 30MHz = 300MHz

Since the filter is dominated by the first pole, the equation is

$$f_{-3dB} = \frac{1}{2\pi Z_1 C_1} = 300MHz.$$

Let Z1 and Z2 be 100 ohms, typical value of ferrite bead, and C1 is

$$= \frac{1}{2\pi (100)300x10^6} = 5.3pF.$$

The next capacitor size larger than 5.3pF is 10pF so use that value for the C1. Place the filter components as close to the RGB connector as possible. This blocks any RF of the energy coupled to the signal traces from radiating outward while preventing the noise from entering the DSP system.

One note to remember is that the T filter is not as effective as the Pi filter for power supply and RF isolation. This is because, in power supply decoupling, having a capacitor closest to the power supply pin to ground is the most important criteria for low radiation and low noise. The closer the capacitor is to the power pin the smaller the current loop area which lowers the radiation and reduces the power supply droop during fast switching. For RF noise entering and exiting the connectors, Pi filter provides a parallel capacitor right at the point of entry and this helps reduce the RF current loops and radiation.

Table 4-3 below summarizes the advantages and disadvantages of the T and Pi filters.

Table 4-3. Pi and T Filters Comparison

	Pi Filter	T Filter
Components required	Two capacitors and one ferrite	Two ferrites and one capacitor
Cost	Slightly lower because capacitors are less expensive than ferrites	Slightly higher
Effectiveness	Slightly better because having a capacitor to ground next to the RGB connector reduces the RF current loop	Difficult to layout the capacitor close to the connector because of the size of the ferrite bead
Power supply isolation	Recommended for power supply filtering because the capacitor can be placed close to the power supply pin	Not as effective as the Pi filter, the capacitor can not be placed as close to the power supply pin

Printed Circuit Board or PCB Layout

Once all the circuits have been designed, the next step is board layout. This is a very critical step in the development process because the effectiveness of the filtering circuits depends on where the components are placed relative to the DSP pins. Also, the board layout has a big impact on noise, crosstalk and transmission line effects so optimizing the layout can minimize these effects. First, designers need to determine the minimum number of PCB layers and then configure the board stackup. Here are some general guidelines.

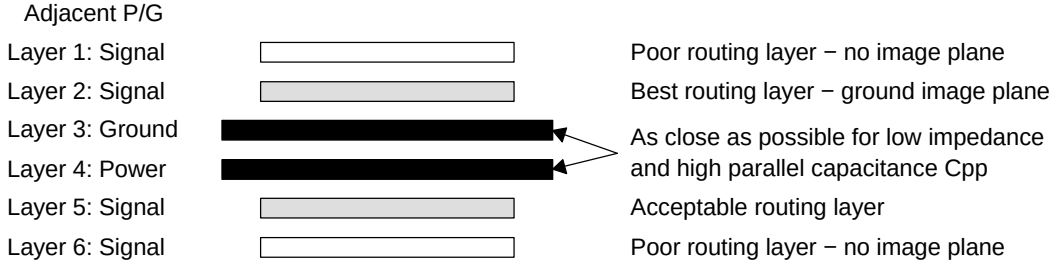
- Perform layout experiments and refer to the DSP reference design package to find the minimum number of layers required to route the signals out from the DSP. If possible, copy the exact layout recommended by TI.
- Consider the need for high-speed signals to be shielded between the ground and power planes.
- Are there buses, such as USB, DDR, Ethernet, and RapidIO, that require a tight differential impedance specification?
- Does the PCB manufacture require a certain trace width and spacing? This determines whether or not a trace can be routed between the balls of a small pitch BGA package. For good signal integrity with minimum skin effect losses, keep the trace width between 4 mils and 12 mils. A common choice is a 5-mil trace and 5-mil spacing.
- Is one power plane and one ground plane sufficient?
- Does the DSP system require a controlled impedance board? This is more expensive but allows the board to be optimized from a signal integrity standpoint.

Two PCB stackup topologies are commonly used, adjacent power and non-adjacent power and ground planes. Figure 5-1 shows what can or cannot be done with each layer when the design is implemented on a 6 layers PCB for the adjacent power and ground topology.

Figure 5-1. Adjacent Power and Ground Board Stackup (1)

$$C_{pp} = k\frac{\epsilon_r A}{d},$$

k = 0.2249 in. or 0.884 cm
ε = dielectric constant = 4.1 to 4.7 for FRA
A = area
d = distance between planes



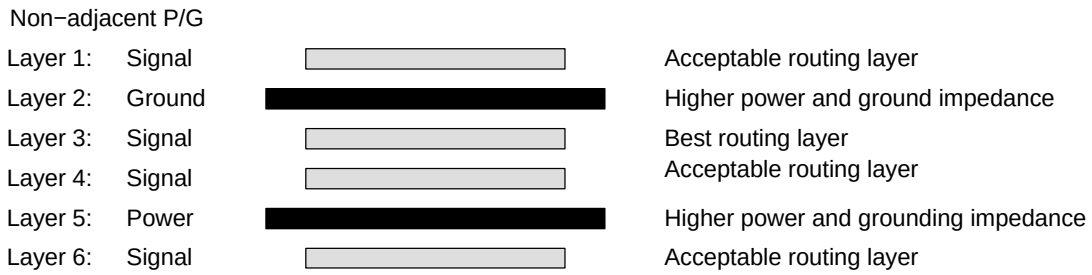
(1) Source: Mark Montrose's Printed Circuit Board Design Techniques book

When using this topology, designers need to consider these points:

- As shown in the equation for Cpp, the distance, d, between the power and ground planes determines the board capacitance. Reducing the distance increases the capacitance and also reduces high frequency impedance. The limiting factor is how closely the layers can be packed together while still maintaining the quality and reliability of the design.
- Route the high-speed signals on the planes next to the power and ground planes.
- The best routing layer is Layer 2 because it is next to the ground plane. This provides optimal current return paths which helps reduce radiation. This is why the adjacent power and ground topology is recommended for DSP systems operating at very high frequency.
- The adjacent power and ground topology is not useable for DSP systems that require many layers to route the signals out from the DSP and interface with other circuits.

Figure 5-2 shows a typical PCB stackup for the non-adjacent power and ground topology. The power and ground planes are placed in Layer 5 and Layer 2 respectively. Layer 3 is best for routing high-speed traces while Layer 1, Layer 4, and Layer 6 are acceptable. As shown in the figure, each of the routing layers is next to either a ground or power plane. Layer 3 is best because it is not only next to a ground plane but is also guarded by a power plane below it. This scheme is best for difficult-to-route DSP systems that do not operate at very high frequencies. One thing to keep in mind is that board capacitance becomes important for systems operating above 300MHz.

Figure 5-2. Non Adjacent Power and Ground Board Stackup (1)



(1) Source: Mark Montrose's Printed Circuit Board Design Techniques book

Here are rules for doing non-adjacent board stackup design.

- For non-adjacent topology, the board capacitance, as shown in capacitance equation Cpp, is low and the board impedance is high between the power and ground planes. This is the opposite of what is needed for systems to have low noise and low EMI.
- This topology requires more high frequency decoupling capacitors to compensate for the board characteristics.

Once board stackup has been decided, next step is to determine the best way to route the signals on the routing layers. Table 5-1 shows the advantages and disadvantages of the two main signal routing technologies, Microstrip shown in Figure 5-3 and Stripeline, shown in Figure 5-4.

Table 5-1. Microstrip and Stripline Comparison

	Microstrip Topology	Stripline Topology
Number of PCB layers	No special requirements	Requires signals to route between the ground planes so it is more expensive
Routability	Easy and can route with minimum number of vias	Difficult to route with limited number of PCB layers. Also, vias are required which can cause signal quality degradation.
Signal Quality	Acceptable	Very Good
EMI	Acceptable but a ground plane is needed just below the routing layer for low EMI.	Very good because high-speed signals are shielded between the planes.

Designers generally make compromises by using both topologies where some of the critical signals are routed between the ground and power planes.

Figure 5-3. Microstrip Topology

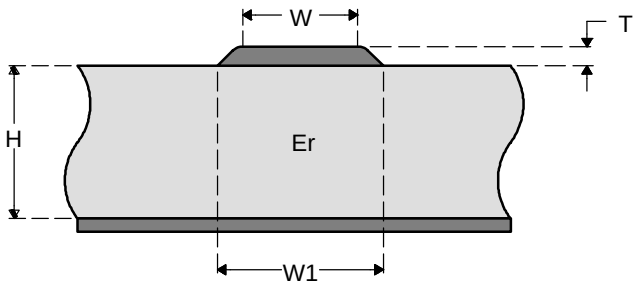
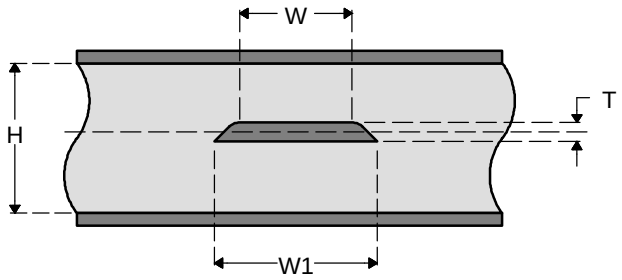


Figure 5-4. Stripline Topology



PCB routing and board stackup are major contributors to EMI so designers need to apply best practices to reduce radiation. An example is the use of an Image Plane, a ground plane located next to the routing layer that provides low inductance current return paths for high-speed signals. An Image plane helps reduce the current loop areas and minimizes the potential differences on the ground plane. Experiments conducted by Clayton compare the EMI for PCBs with and without an image plane. They demonstrate that a PCB with an image plane shows around 15dB reduction in EMI across the frequency spectrum.

Phase-locked Loop (PLL)

System designers need to isolate PLLs to protect them from internal and external noise. The PLL generally functions as a frequency synthesizer, multiplying the input clock by an integer. This integer is a ratio of the feedback counter M divided by the input counter N as shown in Figure 6-1.

Two main PLL architectures are analog PLL (APLL) and digital PLL (DPLL). Understanding the differences helps to make the design tradeoffs often required to minimize noise and jitter caused by external circuitries such as the power supply and other noisy switching devices.

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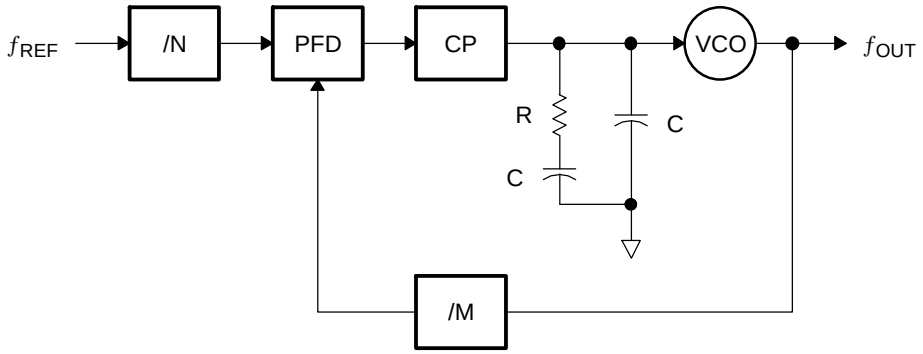
6.1 Analog PLL

Figure 6-1. Analog PLL



The following table provides a brief description of each block shown Figure 6-1 for an APLL.

Table 6-1. APLL Description

Name	Description:	Function
/ N	Divide-by-N	Divide-by-N counter scales down the input frequency
PFD	Phase-Frequency Detector	PFD compares the frequency and the phase of the input and the feedback clock signals and generates an error signal.
CP	Charge Pump	This is typically a constant current source controlled by the error signal output of the PFD block.
VCO	Voltage Controlled Oscillator	This VCO oscillates at a frequency controlled by the DC input voltage derived from the error signal.
/M	Divide-by-M	Divide-by-M counter scales down the output frequency.

The following provides an overview of how the PLL functions as a frequency synthesizer.

1. The reference clock is connected to the PFD input. The Divide-by-N counter reduces the input frequency
2. The PFD compares the output of the Divide-by-M counter with the reference clock and generates an error signal.
3. Based on the error signal, the CP charges or discharges the current store on the loop filter, an RC filter shown in Figure 52. This increases or decreases the VCO control voltage. For some PLL architectures, increasing the VCO control voltage increases the clock frequency and decreasing the voltage lowers the clock output frequency.
4. The phase correction continues until both the feedback signal from the Divide-by-M counter and the reference clock are synchronized. At this point, the error voltage should be zero.
5. The output clock frequency is equal to the ratio of the Divide-by-M counter and the Divide-by-N counter multiplied by the input clock frequency. As a rule of thumb, a higher multiplier ratio yields higher jitter so keep the M and N ratio as low as possible when designing with PLLs. The PLL output frequency, fout, for a given input frequency, f_{in}, is

   $$f_{out} = \frac{M}{N} f_{in},$$

   where M is the PLL feedback counter and N is the input counter.

PLL Jitter

Jitter in PLL design is defined as the signal timing displacement from a reference clock. The three main sources of DSP PLL jitter are jitter generated by the reference clock itself, power supply noise, and noise coupling from external and internal circuitries. The following lists important techniques for designers to minimize the DSP PLL jitter.

- Select a reference clock oscillator with the lowest jitter specification possible.
- Heavily filter the clock circuit to reduce the effect of noise on output jitter. See the following section on PLL isolation.
- Use a series termination resistor at the output of the reference clock to control the edge rate.
- Distribute the clock differentially if possible. Differential signals reject common mode noise and crosstalk.
- Set the multiplier as low as possible to achieve maximum DSP operating frequency. Keep in mind that a higher multiply ratio yields higher output jitter.

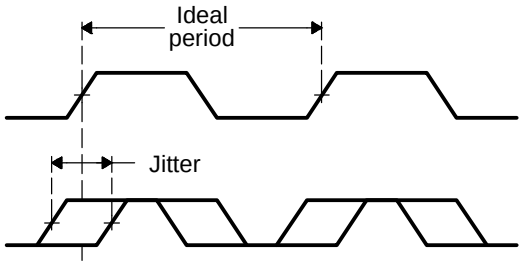
In all cases, jitter can be minimized but cannot be eliminated. The three types of deterministic jitter important for frequency synthesizers and DSP performance are long term jitter, cycle-to-cycle jitter and period jitter.

Long Term Jitter:

See Figure 6-2 where long-term jitter is defined as a time displacement from the ideal reference clock input over a large number of transitions. Long term jitter measures the deviation of a rising edge over a large number of cycles (N) after the first rising edge.

Peak-to-Peak Jitter = Max period (N cycles) – Min period (N cycles)

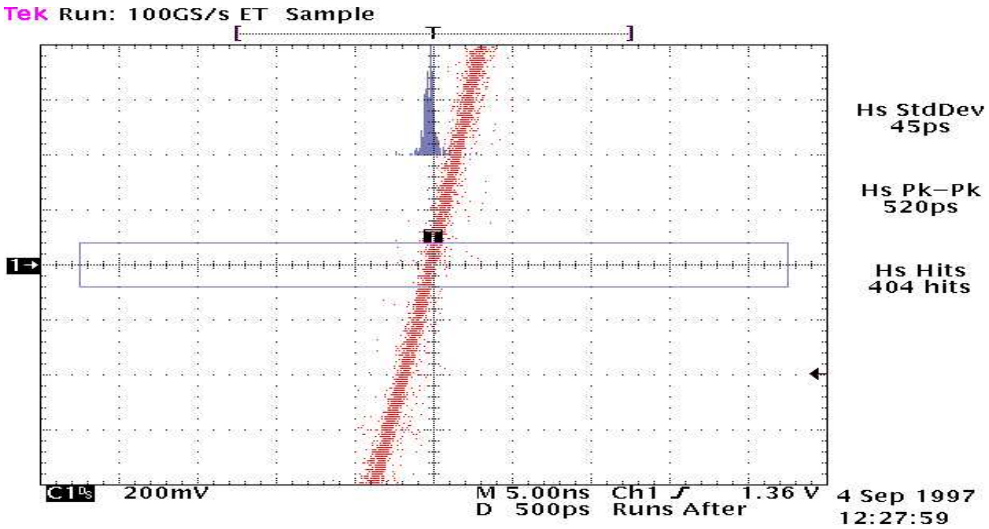
Figure 6-2. Long Term Jitter



Long Term Jitter Measurement:

- Use a high-speed 10GHz sampling oscilloscope, for example an Agilent 54855A.
- Use the input clock to trigger the scope and set the scope in the Infinite Persistence mode.
- The deviation is measured from the first rising edge to the Nth cycle. The “fuzz” shown on the scope in Figure 6-3 is the long term jitter.

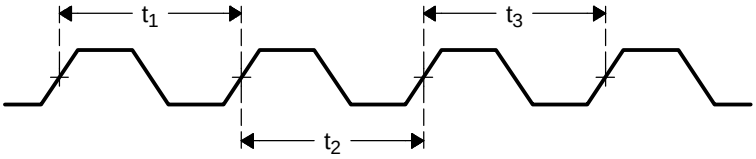
Figure 6-3. Jitter Measured by Digital Scope



Cycle-To-Cycle Jitter:

See Figure 6-4 where cycle-to-cycle is defined as the deviation of the clock period between two consecutive clock cycles.

Figure 6-4. Cycle-To-Cycle Jitter



In Figure 6-4, the cycle-to-cycle is measured by subtracting t2 from t1, t3 from t2, and so on.

Cycle-To-Cycle Jitter Measurement:

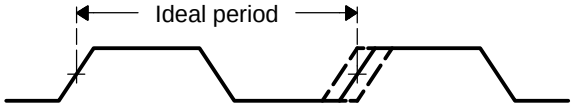
This is a difficult parameter to accurately measure with the high-speed sampling scope. The best way is to use a Timing Interval Analyzer (TIA), which captures one cycle at a time and compares the timing differences between two consecutive cycles. Another method is to use a scope with a cycle-to-cycle jitter measurement option. This method is outlined as follows.

- Use a high-speed 10GHz sampling oscilloscope with cycle-to-cycle jitter option, for example an Agilent 54855A.
- Trigger the PLL output clock and measure the cycle-to-cycle jitter. Use the windowing method to measure the changes from one cycle to another.

Period Jitter:

See Figure 6-5 where period jitter is defined as the maximum deviation in the clock's transition from its ideal position. These periods are non-successive.

Figure 6-5. Period Jitter



Period Jitter Measurement:

- Use a high-speed 10GHz sampling oscilloscope, for example an Agilent 54855A.
- Set the scope in the Infinite Persistence mode and trigger the PLL clock output on the rising edge.
- Measure the “fuzz” shown on the screen at the next rising of the clock.

In summary, the jitter measurements can either be done using a high-speed digital sampling scope, Timing Interval Analyzer (TIA), or Wavecrest jitter measurement system.

6.2 Digital PLL

The main differences between the APLL and DPLL are that the DPLL replaces the analog filter with a digital controller block that filters the phase error in the digital domain and replaces the VCO with a Digital Controller Oscillator (DCO). The advantages of the DPLL are:

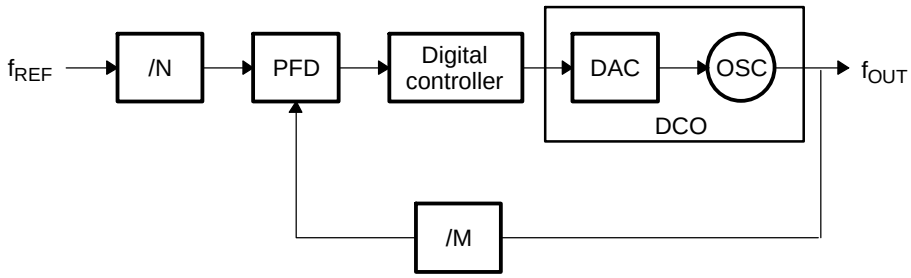
- The DPLL supports a wide range of input frequency, 30KHz to 65MHz.
- The DPLL block requires a smaller silicon area to implement and consumes less power than the APLL.
- The DPLL does not have analog filter components such as capacitors, which can cause leakage current.
- The DPLL block is scalable and portable. The same design can be implemented on different process technology nodes.
- The DPLL design can be optimized for low jitter. But it may not be acceptable for jitter sensitive designs such as USB, audio and video clocks.

The disadvantages of the DPLL are:

- It is very sensitive to external and internal power supply noise. Use of a linear regulator to isolate the power supply from the DPLL is recommended.
- Low power supply rejection ratio.
- In addition to power supply sensitivity, quantization noise and phase detector dead zone are the major sources of output jitter.
- Requiring a DAC block to control the oscillator. This makes the DPLL more sensitive to noise.

Figure 6-6 shows a typical DPLL architecture and Table 6-2 describes the function of each block in the architecture.

Figure 6-6. Digital PLL



$$f_{OUT} = \frac{M}{N} f_{IN}$$

Table 6-2. DPLL Description

Name:	Description:	Function:
/N	Divide-by-N	Divide-by-N counter scales down the input frequency
PFD	Phase-Frequency Detector	PFD compares the frequency and the phase of the input and the feedback clock signals and generates an error signal.
Digital Controller	Digital Controller	This digital filter block detects the phase error information and digitally controls the oscillator.
DCO	Digital controlled oscillator	This DCO converts the control code to analog levels and generates a stable clock output.
/M	Divide-by-M	Divide-by-M counter scales down the output frequency.

APLL and DPLL Jitter Characterization

Table 6-3 shows a jitter comparison between an analog and a digital PLL that shows the effects of process variation where Hot is fast, Cold is slow and Baseline is typical. In this DSP design, the DPLL power supply is isolated by an internal low dropout regulator (LDO) while the APLL is connected directly to the common power supply plane. To test the noise sensitivity, 100mV of noise modulating from 100Hz to 1MHz is injected into the power supply rails. The results showed that the peak-to-peak period jitter is less than 3% for the DPLL and is less than 2% for the APLL. With the LDO, the DPLL jitter is less than 4% up to 50mV of noise on the power supply.

Table 6-3. APLL and DPLL Jitter Comparison

Noise on pwr supply	mW	100		100		100	
	Hz	100		10000		1000000	
	Process	Pk-Pk (ps)	% jitter @ max freq	Pk-Pk (ps)	% jitter @ max freq	Pk-Pk (ps)	% jitter @ max freq
DPLL period jitter CVDD	Cold Baseline Hot	201.21 180.05 156.45	2.90 2.59 2.25	219.12 181.58 149.33	3.16 2.61 2.15	199.38 177.31 160.32	2.87 2.55 2.31
APLL period jitter CVDD	Cold Baseline Hot	195.11 198.30 178.02	1.87 1.90 1.71	192.06 191.38 182.29	1.84 1.84 1.75	195.11 197.96 173.75	1.87 1.90 1.67

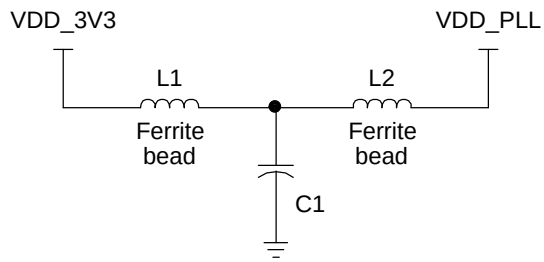
Designers need to be careful when injecting a signal onto the power supply to do jitter measurements. The nature of the signal used for simulating a noisy power supply condition can have a major impact on the PLL jitter. A squarewave signal with a frequency less than the PLL bandwidth characterizes the worst case PLL jitter. As far as the amplitude of the noise, the peak-to-peak voltage has to be within the power supply limits. For example, for a 1.6V +/-3% Core, the maximum acceptable peak-to-peak noise is 96mV (-48mV min and +48mV max).

6.3 PLL Isolation Techniques

As shown in previous sections, both an APLL and a DPLL are sensitive to noise, especially to noise frequency within the PLL bandwidth. PLL isolation is needed in order to prevent the high frequency PLL signal from propagating out of the PLL section and affecting other circuits. PLL isolation can also attenuate the external noise propagating to the PLL circuit which causes excessive jitter. In many cases, external power supply noise causes the PLL to go unstable and the DSP to lock-up randomly.

The two important filter schemes discussed in this document to isolate the PLL are low frequency filtering and high frequency filtering. For high frequency filtering, a Pi or T network filter can be used as shown in Figure 6-7:

Figure 6-7. Pi Filter Circuit



The Pi filter circuit consists of one ferrite bead, L, and two capacitors, C1 and C2. This circuit provides both input and output isolation where noise from the 3.3V supply is attenuated by the ferrite bead and the C2 capacitor and noise generated by the PLL circuit is isolated by the ferrite bead and the C1capacitor. The corner frequency of the lowpass filter formed by the Pi filter is calculated as follows.

$$f_{-3dB}(from_3.3V) = \frac{1}{2\pi ZC_2},$$

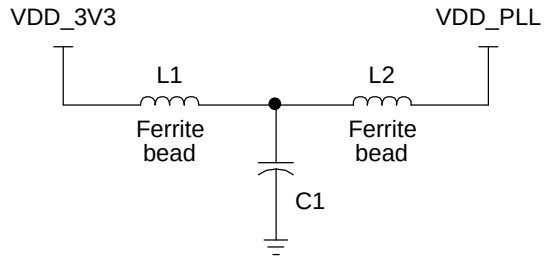
where Z is the resistance of the ferrite bead at the noise frequency.

$$f_{-3dB}(from_PLL) = \frac{1}{2\pi ZC_1},$$

where Z is the resistance of the ferrite bead at the noise frequency.

Select as large as possible capacitor values to filter the low frequency noise and place the Pi filter components as close as possible to the PLL power pin. Also, select a ferrite bead with minimum DC on resistance but large resistance at 30MHz.

Figure 6-8. T Filter Network



A T filter consists of two ferrite beads and one capacitor as shown in Figure 6-8. Just like in a Pi filter, 3.3V supply noise is attenuated by the L1 ferrite bead and the C1 capacitor and PLL noise is isolated by the L2 ferrite bead and C1 capacitor. The equations are as follows.

$$f_{-3dB}(from_PLL) = \frac{1}{2\pi ZC_1},$$

where Z1 is the resistance of the ferrite bead L1.

$$f_{-3dB}(from_PLL) = \frac{1}{2\pi Z_2C_1},$$

where Z2 is the resistance of the ferrite bead L2.

Select as large as possible a capacitor value to filter the low frequency noise and place the Pi filter components as close as possible to the PLL power pin. Also, select ferrite beads with minimum DC on resistance but large resistance at 30MHz.

Both Pi and T circuits are good for filtering high frequency noise. However, the Pi circuit has an advantage because this topology makes it possible to place the capacitor closer to the PLL voltage pin, ensuring low impedance to ground and the smallest current loop area, which reduces EMI.

For low frequency isolation, there are two common techniques, Pi filter with large bulk capacitor and linear voltage regulator.

Figure 6-9. Low Frequency Pi Filter

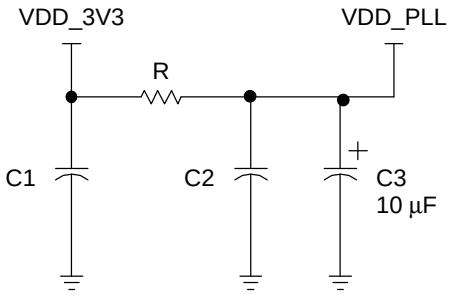
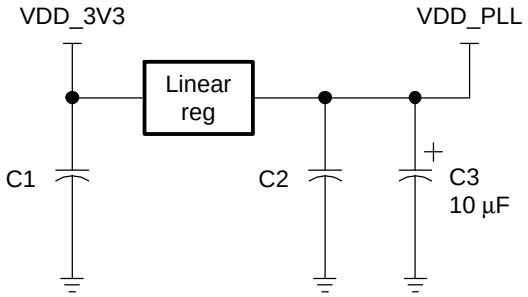


Figure 6-10. Noise Isolation with Voltage Regulator



One method for low frequency filtering is shown in Figure 6-10 where a resistor R replaces the ferrite bead and a bulk capacitor C3 (10uF to 33uF) is added to the circuit. Low frequency noise is attenuated by the resistor R and the bulk capacitor C3. The resistor needs to be selected such that the voltage drop across the resistor is negligible. The PLL supply voltage must be within the specified limits for worst case PLL current consumption.

Another method of low frequency filtering is to use a linear voltage regulator. This method has the least effect on PLL performance. The linear regulator typically has good line regulation and power supply rejection characteristics, preventing low frequency transients and high frequency noise from entering the PLL circuit. The method shown in Figure 6-9 is more expensive to implement than other methods described previously but it is extremely effective in keeping the PLL voltage as clean as possible to guarantee lowest PLL jitter.

Electromagnetic Interference

This chapter discusses the design for high-speed and low-speed electromagnetic interference (EMI).

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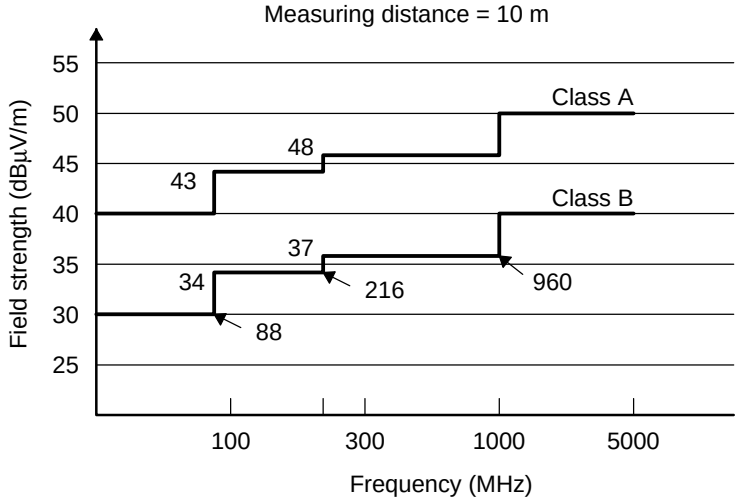
7.1 Introduction

Radiated emissions in high-speed DSP systems are caused by fast-switching currents and voltages propagating through the printed circuit board traces. As DSP speed increases, printed circuit board traces are becoming more effective antennas and these antennas are radiating unwanted energies that interfere with other circuitries and with other systems located nearby. To prevent systems from interfering with each other, the FCC sets maximum limits known as FCC Part 15 A for commercial products and FCC Part 15 B for consumer devices as shown in Figure 7-1.

Figure 7-1. Frequency in MHz (1)



(1) Source: Michael Mardiguian's Controlling Radiated Emissions By Design book

This section outlines different ways to design for low EMI and find the root cause of EMI problems when they occur. It only covers the electrical design aspects of EMI even though shielding, cabling and other mechanical fixes can also be used to help reduce the emissions below the maximum allowable limits. In general, mechanical solutions are very expensive for high volume designs. Even worse, the mechanical solutions may have to be changed when the DSP speed increases. The following lists some of the most common sources of EMI in high speed DSPs.

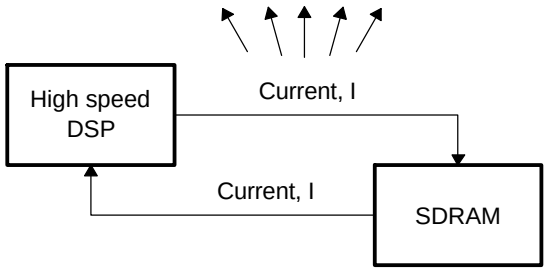
- Fast switching digital signals such as clocks, memory buses, PWM (switching power supplies)
- Large current return loops
- Not having an adequate power supply decoupling scheme around large DSPs
- Transmission lines
- Printed circuit board layout and stackup, lack of power and ground planes
- Unintentional circuit oscillations

7.2 EMI Fundamentals

The five main sources of radiation are digital signals propagating on traces, current return loop areas, inadequate power supply filtering or decoupling, transmission line effects, and lack of power and ground planes.

Radiation is classified in two modes, differential mode radiation and common mode radiation. It is important for engineers to understand the differences between the two modes in order to develop an effective scheme to mitigate the problem. In DSP systems, all electrical currents propagate from the source to the load and return back to the original source. This mechanism generates a current loop which creates differential mode radiation as shown in Figure 7-2.

Figure 7-2. Differential Mode Radiation



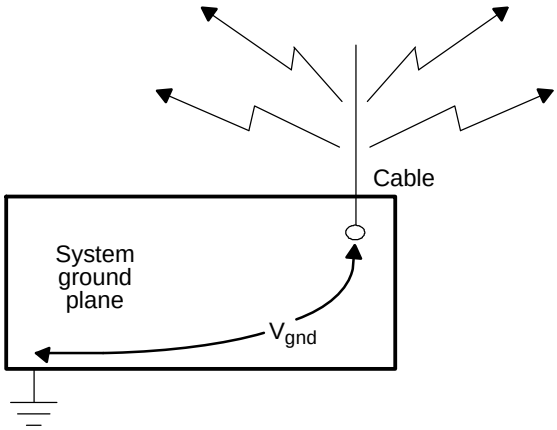
Differential mode radiation is directly related to the length of the signal trace, the driving current and the operating frequency. The electric field caused by differential mode radiation is

$$E = 87.6 \times 10^{-16} [f^2 AI],$$

where f is the operating frequency, A is the current loop area created by the trace length and the board stackup, and I is the driving source current.

Common mode radiation is generated by a differential voltage between two points on a ground plane. It typically radiates from cables connected to the board or chassis. In theory, 100% of the source current returns back to the source but it is not true because a small portion of the current spreads over the entire plane before finding its way back to the source. This current creates an imbalance in the ground potential and causes common mode radiation as shown in Figure 7-3.

Figure 7-3. Common Mode Radiation



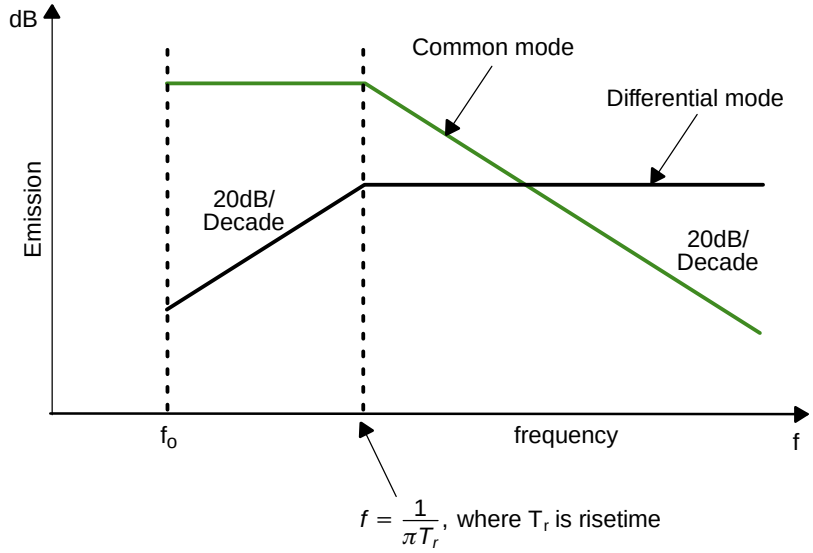
The electric field generated by common radiation is directly related to the frequency propagating on the cable, the length of the cable, and the current driving the cable. Here is an equation to calculate the common mode radiation in an open field.

$$E = 4.2x10^{-7}[fLI]$$

where f is the frequency, L is the length of the cable in meter and I is the source current

The relationship between the common mode and differential mode radiation for a given signal is shown in Figure 7-4. In general, the differential mode dominates at in higher frequency spectrum while the common mode radiates more energy around the operating frequency.

Figure 7-4. Relationship of Common and Differential Mode Radiation (1)

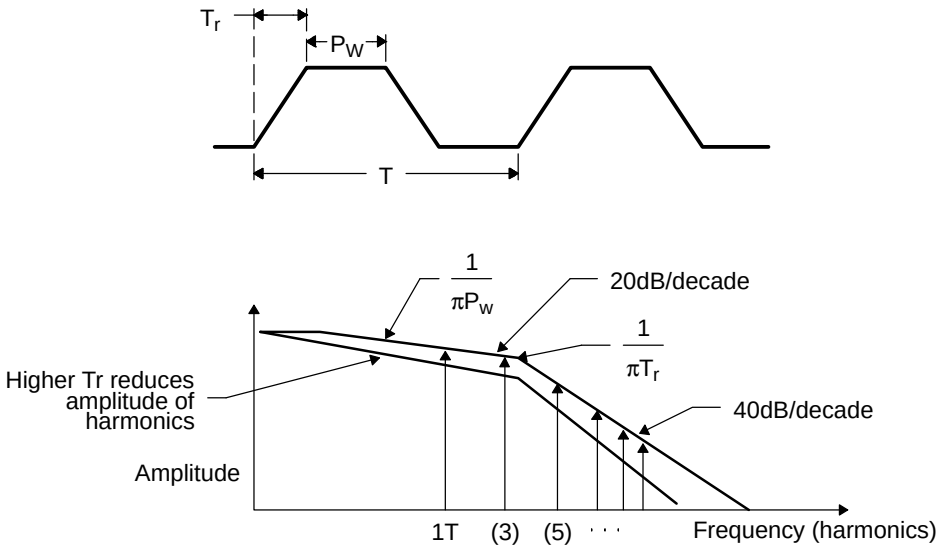


(1) Source: Michael Mardiguian's Controlling Radiated Emissions By Design book

7.3 Digital Signal

A digital or squarewave signal consists of a series of sine and cosine signals superimposed on one another. In the frequency domain, a squarewave consists of many higher frequency harmonics and the harmonic radiated energy is directly depending on the risetime and the pulsewidth of the signal as shown in Figure 7-5.

Figure 7-5. Frequency Spectrum of a Squarewave



In Figure 7-5, assuming a 50% duty cycle signal where only odd harmonics are present, the amplitudes of the harmonics decay slowly as frequency increases. The first pole frequency is at

$$f_{-3dB} = \frac{1}{\pi P_W}$$

and a second pole is at

$$f_{-3dB} = \frac{1}{\pi T_{r,}},$$

where P_W and T_r are the width and the risetime of the signal respectively. Therefore, increasing the risetime increases attenuation of the harmonics which leads to lower radiation. This method is not always practical because the slower risetime reduces the timing margin and may violate electrical requirements such as setup and hold times.

The best technique to minimize EMI generated by digital signals is keeping the high-speed signal traces as short as possible. It is a good practice for engineers to go through the design and analyze the traces to see if they are effective antennas or not. A good rule-of-thumb is keeping the length of the trace less than the wavelength (?) divided by 20. Here is the equation.

$$max_trace_length = \frac{\lambda}{20} = \frac{c}{20f},$$

where C is a speed of light, 3x108 m/s, and f is the frequency.

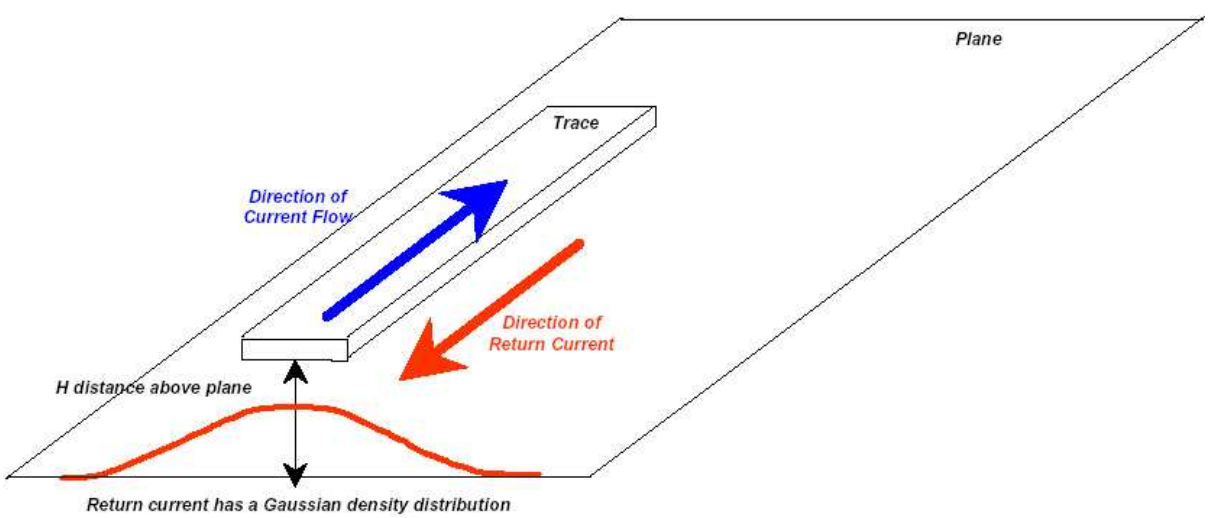
For example, a 1.18 inch trace becomes an effective radiator when it is being driven by a 500MHz signal. The 500MHz signal is a 5th harmonic of 100MHz clock which is a very common frequency in DSP systems today.

7.4 Current Loops

Current loops are the dominant sources of EMI so it is very important for designers to understand high-speed and low-speed current return paths and optimize the design to reduce the loop areas as discussed previously.

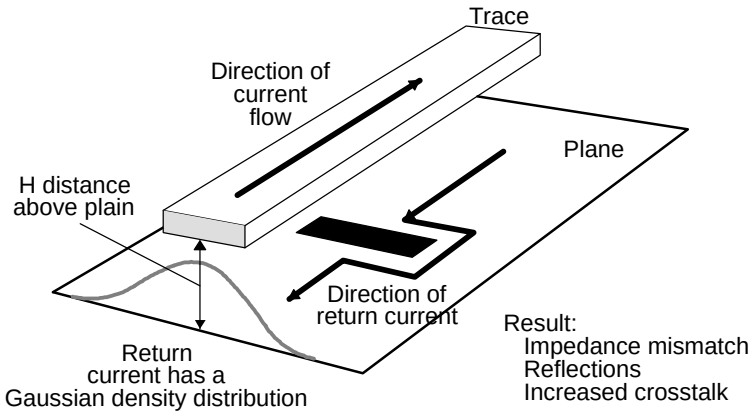
In Section 3.1, current return creates a loop area that is directly related to the radiated electric field, so reducing the loop area lowers radiation. Skin effect modifies the current distribution and changes the resistance within a conductor. Skin effect is negligible at lower frequencies but increases as frequency rises. For a typical conductor used in DSP systems, a 10MHz or higher trace is considered to be a high-speed signal which follows the high speed current return path. Providing a continuous ground plane right underneath a high-speed signal is the most effective way to achieve the lowest current loop area as shown in Figure 7-6.

Figure 7-6. High Speed Current Return on Continuous Ground Plane



If the ground plane is not continuous underneath the high speed signal, all, crosstalk, reflections and EMI, will increase because of the impedance mismatch and larger current loop return area as shown in Figure 7-7.

Figure 7-7. High Speed Current Return on Continuous Ground Plane

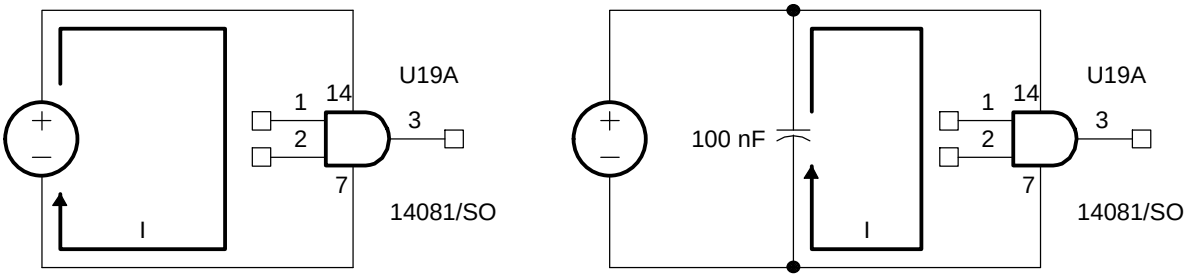


7.5 Power Supply

The power supply is another major source of EMI because:

- The power supply is common to many high-speed sections in a design. RF signals may propagate from one section to another generating excessive EMI.
- A switching power supply generates fast current transients with a large amount of radiated energies. A 1MHz switching power supply can radiate enough energy to fail EMI testing at the 100MHz frequency range.
- Inadequate power supply decoupling may lead to excessive voltage transients on the power supply planes and traces.
- The power supply board layout can be a root cause of oscillations.

Figure 7-8. Power Supply Decoupling Reduces Current Loop Area



As shown in Figure 7-8, decoupling the power supply reduces transients and provides a smaller current loop area. If the power supply trace in Figure 7-8 is long and has no decoupling capacitor, the parasitic inductance is large and requires some time to charge up. This delay is a root cause of the power supply droop problem. Power supply droop occurs when the output buffer switches at a fast rate but is starved for the current needed to drive the load since the parasitic inductance between the power supply and the DSP becomes an open circuit.

Example 1:

- A DSP BGA (ball grid array) package has a trace inductance of 1.44nH.
- This output is driving a 3” trace with 1nS risetime signal.
- This trace is being routed on a typical FR4 printed circuit board. Line characteristic impedance and IO voltage are 68 ohms and 3.3V respectively.

To estimate the power supply droop caused by the parasitic inductance, first let us estimate the as follows. The dynamic IO current is the current transient for transmission line load, not steady state resistive load.

$$I(peak) = \frac{\Delta V}{Zo} = \frac{3.3V}{68} = 48.5mA$$

Since the package inductance is 1.44nH for 1nS risetime signal, the internal voltage droop is

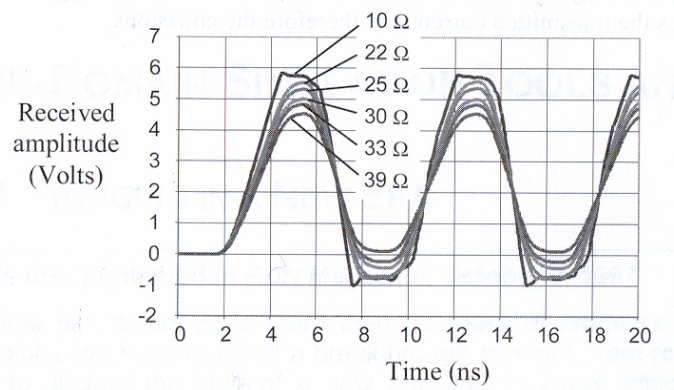
$$V(droop) = L\frac{dI}{dt} = (1.44nH)\ \frac{48.5mA}{1nS} = 70mV$$

Typically, one DSP power supply pin is shared by many output buffers. This creates larger droop and leads to higher radiation. This helps explain why good power supply decoupling is required for low EMI design.

7.6 Transmission Line

To combat TL effects, use simulation tools to fine-tune the series termination resistors to eliminate overshoots and undershoots caused by impedance mismatch explained in the Transmission Line chapter. Improving signal integrity design helps reduce EMI but it is not guaranteed minimum radiation. This is because radiation is depending on the switching current which can be minimized by using large series termination resistors.

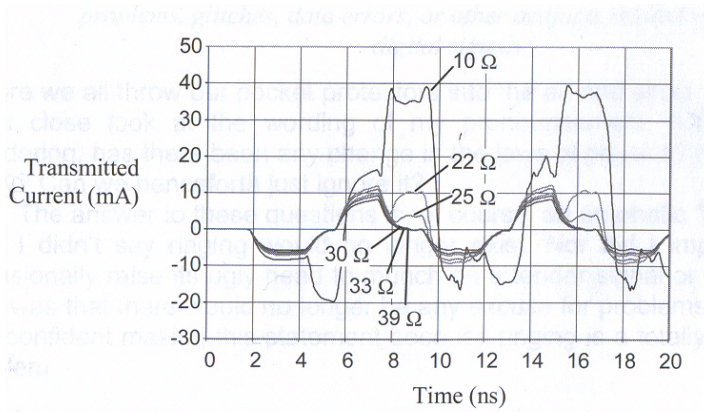
Figure 7-9. Clock Waveforms with Different Series Termination Resistors (1)



(1) Source: Howard Johnson's High-Speed Signal Propagation book

Figure 7-9 shows the waveforms using different values for the series termination resistor. Changing the value from 10 ohms to 39 ohms does not have much effect on the waveform but dramatically reduces the source current as shown in this figure.

Figure 7-10. Source Current Waveforms for Different Series Termination Resistors (1)



(1) Source: Howard Johnson's High-Speed Signal Propagation book

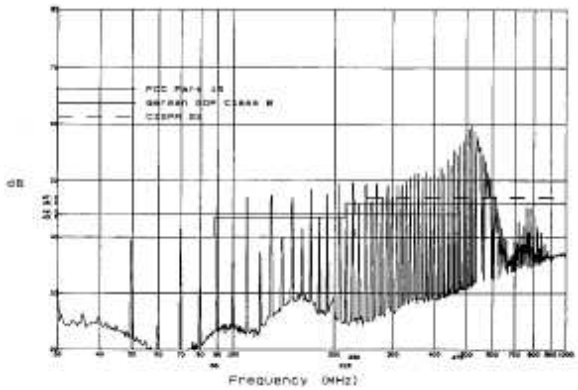
Figure 7-10 shows that using a 39 ohm termination resistor leads to 10dB to 20dB EMI reduction. Therefore, if slower risetime signals are acceptable and do not violate AC timing specifications, designers should use the largest resistor value to terminate high speed signals to optimize the design from an EMI standpoint.

7.7 Power and Ground Planes

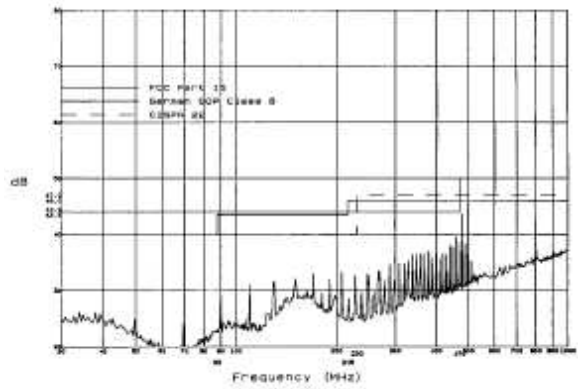
For high-speed DSP systems, it is getting more and more difficult to meet EMI regulations without using multiple layer PCBs and dedicating some of the layers as power and ground planes. Compared to a trace, a power or ground plane has a lower parasitic inductance and provides a shielding effect for high-speed signals. Power and ground planes also provide natural decoupling capacitance. As described in the PCB layout section of this document, natural decoupling capacitance occurs when power and ground planes are spaced very closely, yielding higher capacitance. This effect becomes very important at 300MHz speed or higher. So, adding power and ground planes simplified PCB routing and reduces the number of high-frequency decoupling capacitors required for the DSP.

Another important consideration for the PCB is layer assignment. Refer to the board layout section to determine the best board stackup for your application. Keep in mind that adding a ground plane directly underneath the high-speed signal plane creates an image plane that provides the shortest current return paths. Studies by Mark Montrose show that image planes great reduce radiated emissions. See Figure 7-11.

Figure 7-11. Radiated Emissions Comparison (1)



Radiated Emissions from PCB



Radiated Emissions from PCB With Image Plane

(1) Source: Mark Montrose's Analysis on the Effectiveness of Image Planes technical paper

7.8 EMI Reduction Guidelines

In summary, here are the guidelines for low EMI system design.

- Add image planes wherever possible.
- Create ground planes if there are spaces available on the routing layers. Connect these ground areas to the ground plane with vias. Creating a quarter-inch via grid is ideal.
- Add guard traces to high-speed signals if possible.
- Reduce the risetime of the signal if timing is not critical. This can be accomplished by including series termination resistors on high-speed buses and fine-tuning the resistors for optimal signal integrity and EMI. Series termination resistors lower the source current, increase the signal risetime and reduce transmission effects. Substantial benefits can be achieved with this approach at a low cost.
- Keep the current loops as small as possible. Add as many decoupling capacitors as possible. Always apply current return rules to reduce loop areas.
- Keep high-speed signals away from other signals and especially away from input and output ports or connectors.
- Avoid isolating the ground plane. If this is required for performance reasons, such as high performance audio CODECs, apply current return rules to connect the grounds together.
- Avoid connecting the ground splits with a ferrite bead. At high frequencies, a ferrite bead has high impedance and creates a large ground potential difference between the planes.
- Use multiple decoupling capacitors with different values. Every capacitor has a self-resonant frequency so be careful. Refer to the Power Supply Decoupling Techniques section for more information.
- For PC board stackup, add as many power and ground planes as possible. Keep the power and ground planes next to each other to ensure low impedance stackup or large natural capacitance stackup.
- Add an EMI pi filter on all the signals exiting the box or entering the box.
- If the system fails EMI tests, find the source by tracing the failed frequencies to their source. For example, assume the design fails at 300MHz but there is nothing on the board running at that frequency. The source is likely be a 3rd harmonic of a 100HMz signal.
- Determine if the failed frequencies are common mode or differential mode. Remove all the cables connected to the box. If the radiation changes, it is common mode, if not, then it is differential mode. Then, go to the source and use termination or decoupling techniques to reduce the radiation. If it is common mode, add pi filters to the inputs and outputs. Adding a common choke onto the cable is an effective solution but expensive method for EMI reduction.

Conclusions

As operating frequencies rise, high-speed DSP system design is becoming difficult and complex. This document is designed to aid designers by highlighting the pitfalls of high-speed systems design and providing solutions that improve the probability of success. Use of the following methodology will help prevent noise and radiation problems:

- Printed circuit board floor planning: Place high-speed circuits far away from noise sensitive video, audio and communication circuits. Place these circuits in the middle of the PC board if possible to help reduce EMI.
- Power supply distribution: Design the power supply plane to have a minimum number of power splits. If possible, create one continuous 3.3V power plane and one multi-voltage plane, which includes all other voltages, such as 2.5V for memory, 1.2V for core, and 1.8V for memory. Use linear regulators to isolate analog circuits such as DAC, ADC, video encoder, and decoder.
- Ground distribution: Do not isolate high-speed circuit grounds. Understand current return paths and design signal routings to minimize crosstalk as described in this guide. There must be at least one continuous ground plane. The empty space on the top and bottom layers should be filled with grounds and place ground vias around the perimeter with about quarter of an inch spacing.
- Decoupling techniques: Apply the decoupling techniques described in this document or follow the recommendations of the device manufacturer.
- Clock distribution: Put the clock generator/buffer circuit in the middle of the PC board and route the signals evenly to all the loads. Review the clock termination techniques outlined in this document. Avoid having more than two loads on each output buffer.
- PLL: Review the PLL isolation techniques described in this guide. For noisy systems, use a high power supply rejection regulator to create a clean supply for the PLL circuit.
- Power sequencing: Review the design to make sure that all the voltages ramp up continuously to avoid latch-up and bus contention possibilities. Be sure to have RESET asserted during power-up and to follow a device specific power sequencing requirement.
- External pull-ups and downs: Review all the critical signal pins, such as configuration pins, TRST, NMI, etc., and make sure that they have external pull-ups and pull-downs if they are routed out to external circuits. If they are not routed out, use the internal pull-ups and pull-downs to force the signals to the valid states. Do not rely on the internal pull-ups and pull-downs to drive external circuits.
- High speed buses (DDR, RapidIO, EMIF): Follow the recommended layout. Add resistor terminations as suggested in the device specific reference design.
- Board stackup: Make sure to have one continuous ground plane and one continuous power plane. The ground and power planes should be placed next each other to increase the natural board capacitance and this helps filtering high frequency noise (above 300MHz). Place the critical signal routing plane next to the ground plane.

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