BELL SEMICONDUCTOR LLC'S ANALYSIS OF INFRINGEMENT

NXP

U.S. Patent No. 7,646,091

Bell Semiconductor, LLC ("Bell Semic") provides evidence of infringement of claims 1, 5, 6, 8, 10, 11, 12, and 13 of U.S. Patent No. 7,646,091 ("the '091 patent") by NXP USA, Inc. ("NXP"). In support thereof, Bell Semic provides the following claim charts.

"Accused Products" as used herein refers to the Layerscape products listed by part number in the table below. These Accused Products include at least devices produced or sold by NXP that are or include semiconductor packaged devices having isolated V_{ss} plane to accommodate high speed circuitry ground isolation, with the understanding that infringement has also taken place through the manufacture, importation, offer for sale, and/or sale of products including such Accused Products. These Accused Products include the representative LX2160XN72029B Processor, along with any devices or other products comprising the LX2160XN72029B Processor or another one of the Accused Products. The LX2160XN72029B Processor is representative of the other Layerscape products below, for example, because they share the same or similar Data Sheets, and on information and belief, therefore share the same high-performance processor features shown below. These claim charts demonstrate infringement by comparing each element of the asserted claims to corresponding components, aspects, and/or features of the Accused Products. These claim charts are not intended to constitute an expert report on infringement. These claim charts include information provided by way of example, and not by way of limitation.

The analysis set forth below is based only upon information from available resources regarding the Accused Products, as NXP has not yet provided any non-public information. An analysis of NXP's (or other third parties') technical documentation may assist in fully identifying all infringing features and functionality. Accordingly, Bell Semic reserves the right to supplement this infringement analysis once such information is made available to Bell Semic. Furthermore, Bell Semic reserves the right to revise this infringement analysis, as appropriate, upon issuance of a court order construing any terms recited in the asserted claims.

Unless otherwise noted, Bell Semic contends that NXP and customers of NXP directly infringe under 35 U.S.C. § 271(a) the '091 patent by selling, offering to sell, making, using, and/or importing semiconductor products designed and/or produced at least in part by the Accused Products. Unless otherwise noted, Bell Semic further contends that the evidence below supports a finding of indirect infringement under 35 U.S.C. § 271(b) since January 30, 2022, the time when NXP had actual notice of NXP's infringement of the '091 patent.

NXP and/or its customers make, use, sell, import, or offer for sale in the United States, or have done the same in the past, without authority, and/or induce or have induced others to make, use, sell, import, or offer for sale in the United States, without authority, products, equipment, or services that infringe claims 1, 5, 6, 8, 10, 11, 12, and 13 of the '091 patent, including without limitation the Accused Products or semiconductor products designed and/or produced at least in part using the Accused Products.

Unless otherwise noted, Bell Semic believes and contends that each element of each claim asserted herein is literally met through NXP's provision of the Accused Products. However, to the extent that NXP attempts to allege that any asserted claim element is not literally met, Bell Semic believes and contends that such elements are met under the doctrine of equivalents. More specifically, in its investigation and analysis of the Accused Products, Bell Semic did not identify any substantial differences between the elements of the patent claims and

the corresponding features of the Accused Products, as set forth herein. In each instance, the identified feature of the Accused Products performs at least substantially the same function in substantially the same way to achieve substantially the same result as the corresponding claim element.

To the extent the chart of an asserted claim relies on evidence about certain specifically-identified Accused Products, Bell Semic asserts that, on information and belief, any similarly-functioning instrumentalities also infringes the charted claim. Bell Semic reserves the right to amend this infringement analysis based on other products made, used, sold, imported, or offered for sale by NXP. Bell Semic also reserves the right to amend this infringement analysis by citing other claims of the '091 patent, not listed in the claim chart, that are infringed by the Accused Products. Bell Semic further reserves the right to amend this infringement analysis by adding, subtracting, or otherwise modifying content in the "Accused Products" column of each chart.

Part Number	**Data Sheet**
LX2160XN72029B	https://www.mouser.com/datasheet/2/302/phgl_s_a0010925048_1-2279606.pdf
LX2080CA72232B	https://www.mouser.com/datasheet/2/302/phgl_s_a0010925048_1-2279606.pdf
LX2080CA72232B	https://www.mouser.com/datasheet/2/302/phgl_s_a0010925048_1-2279606.pdf
LX2080CC72232B	https://www.mouser.com/datasheet/2/302/phgl_s_a0010925048_1-2279606.pdf
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LX2082RC82029B	https://www.mouser.com/datasheet/2/302/LX2162AFS-2089757.pdf
LX2082RC82029B	https://www.mouser.com/datasheet/2/302/LX2162AFS-2089757.pdf
LX2082RE82029B	https://www.mouser.com/datasheet/2/302/LX2162AFS-2089757.pdf
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LX2120XN72232B	https://www.mouser.com/datasheet/2/302/phgl_s_a0010925048_1-2279606.pdf
LX2122RC82029B	https://www.mouser.com/datasheet/2/302/LX2162AFS-2089757.pdf
LX2122RC82029B	https://www.mouser.com/datasheet/2/302/LX2162AFS-2089757.pdf
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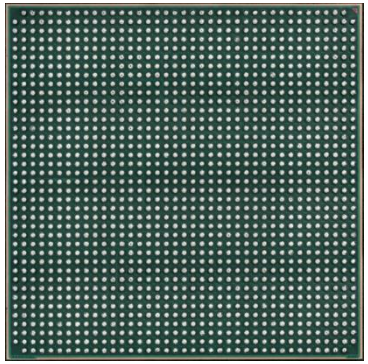
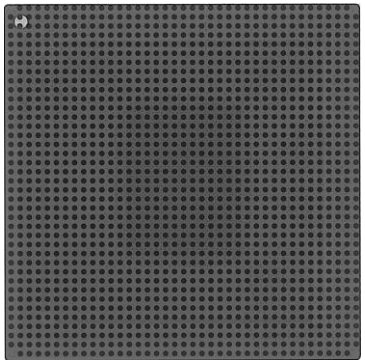
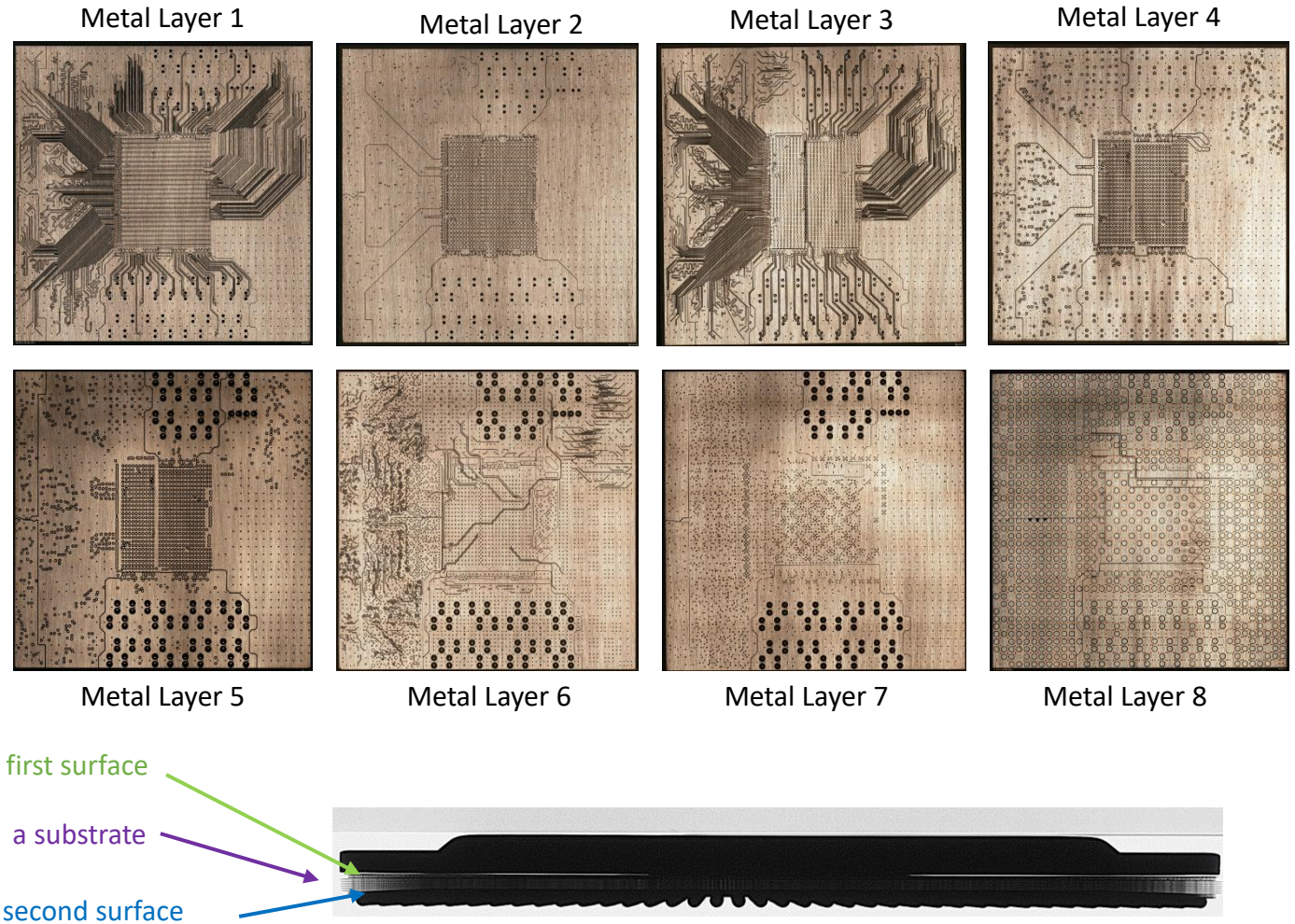
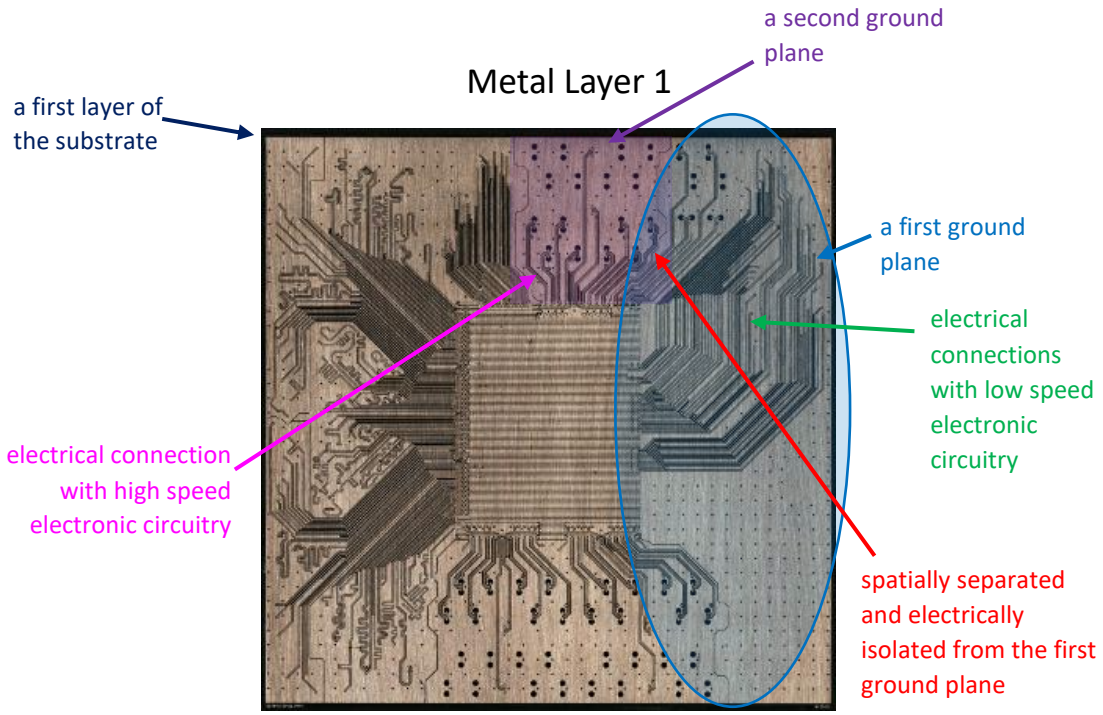
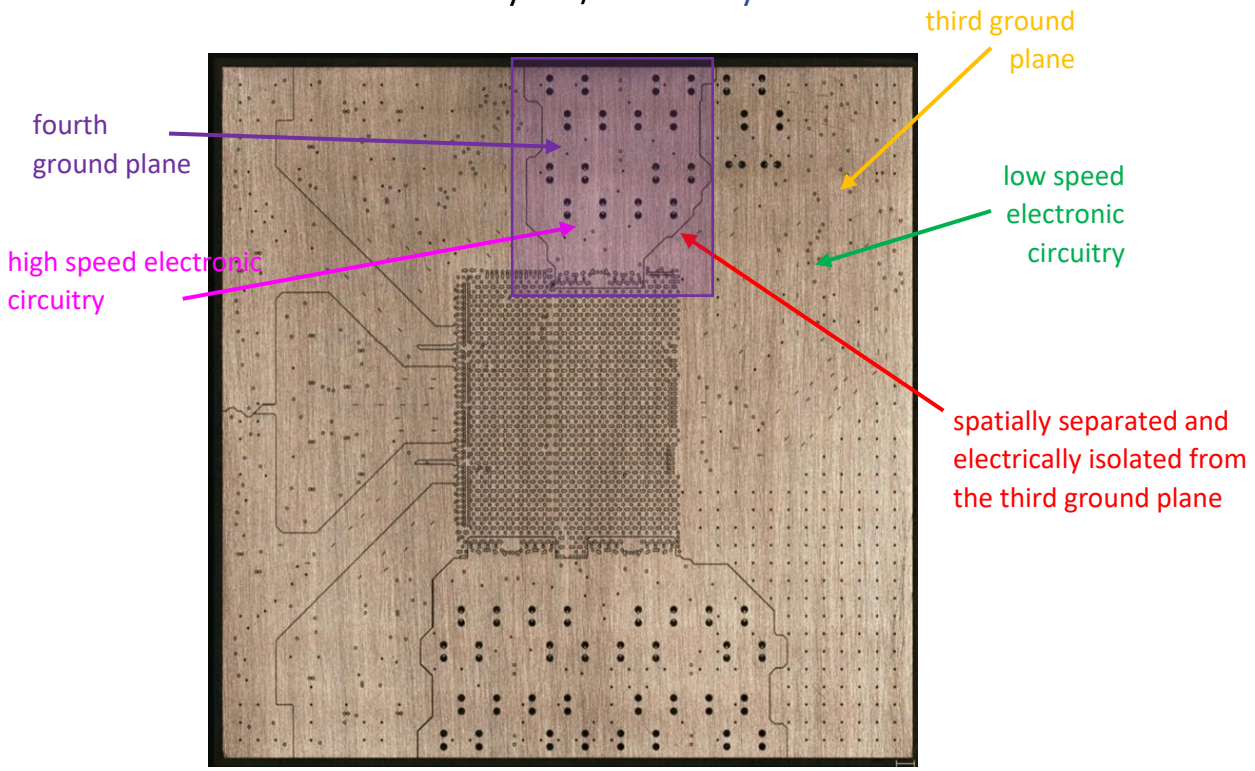
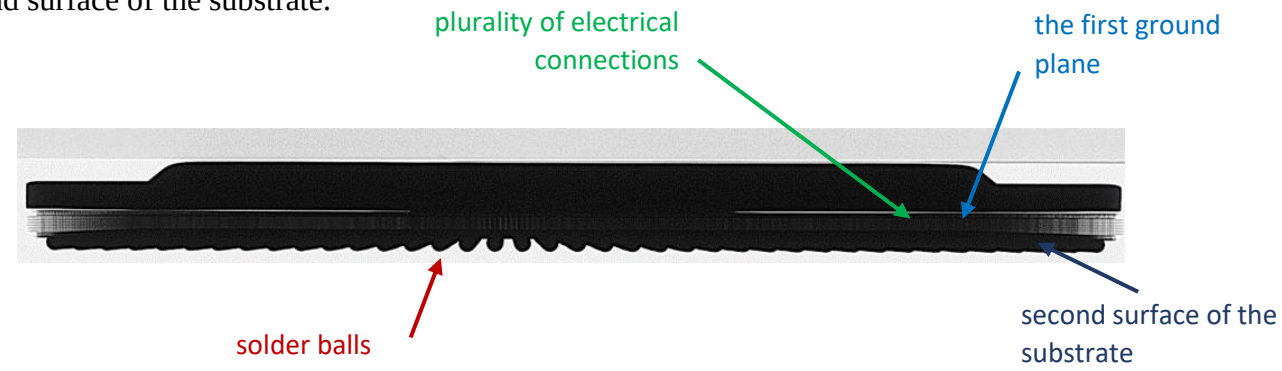
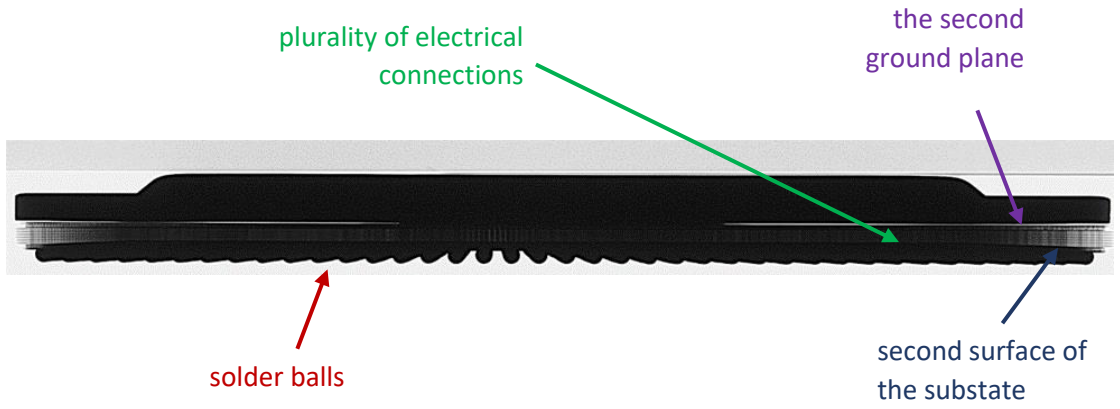
LX2162RE82029B	https://www.mouser.com/datasheet/2/302/LX2162AFS-2089757.pdf
LX2162RN82029B	https://www.mouser.com/datasheet/2/302/LX2162AFS-2089757.pdf

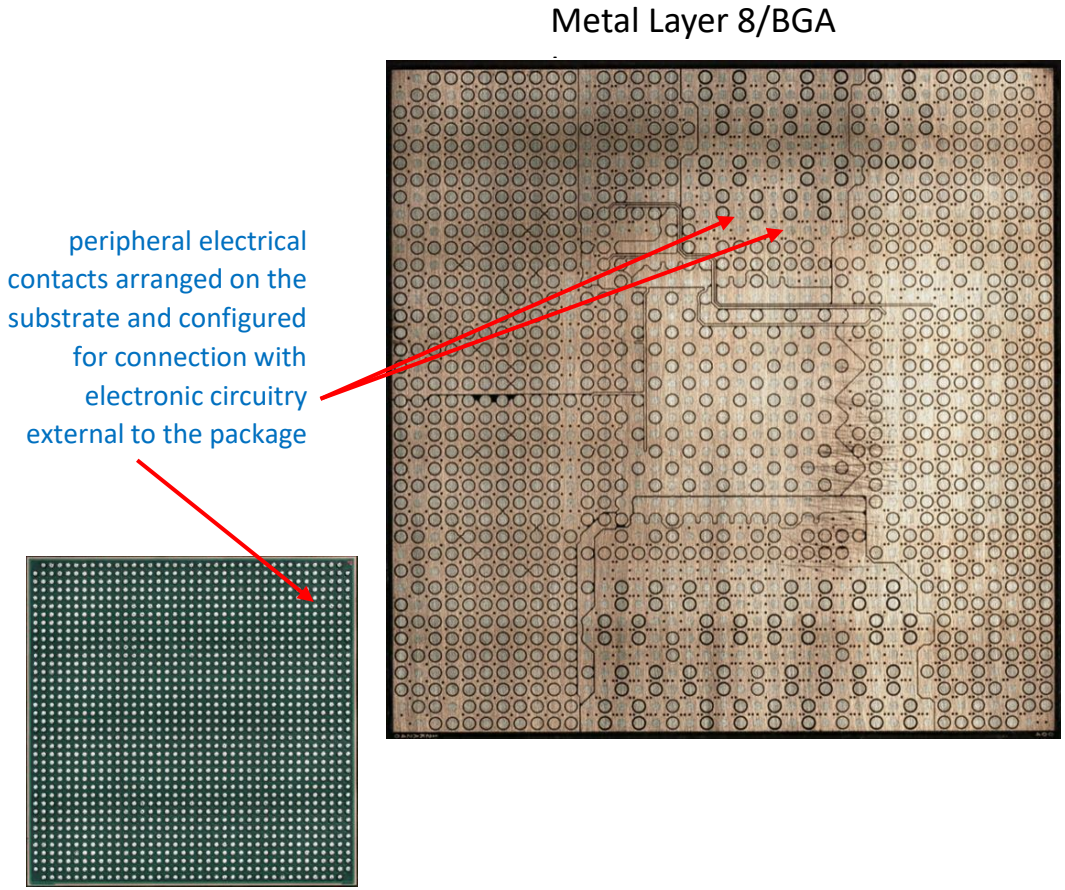
Claim 1	Accused Products
1. A semiconductor integrated circuit (IC) package which comprises:	To the extent the preamble is limiting, the NXP LX2160XN72029B Processor is a semiconductor integrated circuit (IC) package with a semiconductor integrated circuit therein. Component – Top View Component – Bottom View (BGA Layer)   X-ray – Top View X-ray – Side

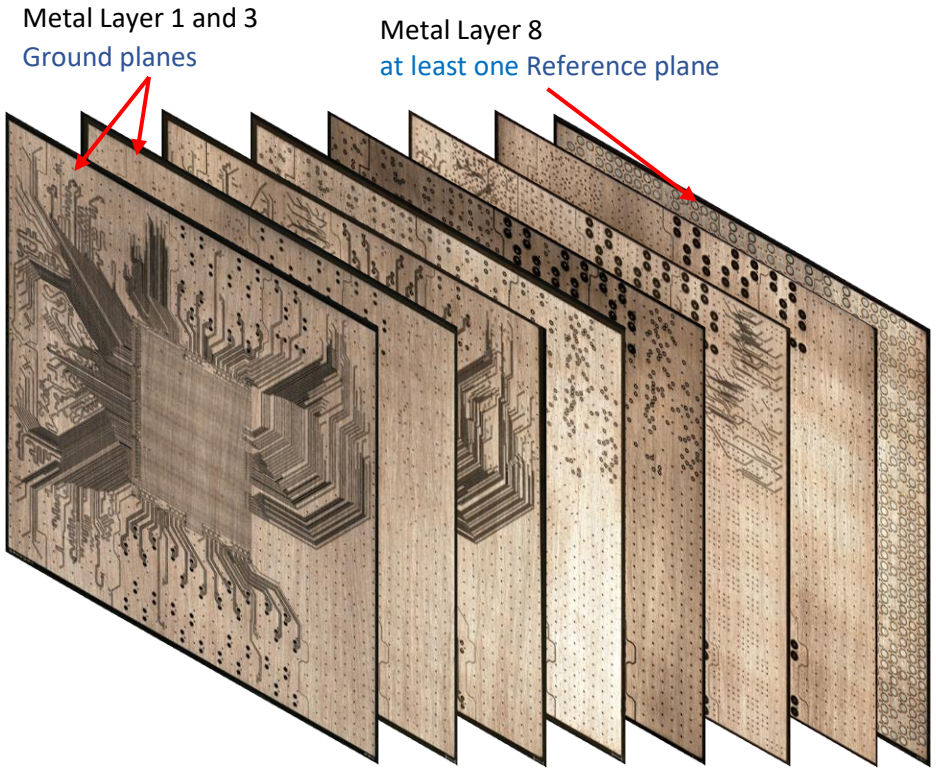
a substrate having a first surface and a second surface	The integrated circuit package of the NXP LX2160XN72029B Processor is manufactured to have 8 metal layers, thus the substrate of the NXP LX2160XN72029B Processor includes the 8 metal layers. The substrate has an upper surface (first surface) and a lower surface (second surface). 

wherein; a first layer of the substrate includes, a first ground plane enabling electrical connection with low speed electronic circuitry, and a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection with high speed electronic circuitry;	Metal Layer 1 (the first layer) of the NXP LX2160XN72029B Processor includes a first ground plane (blue) which enables electrical connection to low speed electronic circuitry on the die (green). The first ground plane is spatially seperated from and electrically isolated from a second ground plane (purple). The second ground plane enables electrical connection to high speed electronic circuitry on the die (e.g. electrical connection to high speed PCIe circuitry on the die) (pink). 

a second layer of the substrate includes, a third ground plane configured for electrical connection with low speed electronic circuitry, and a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the fourth ground plane configured for electrical connection with high speed electronic circuitry;	Metal Layer 2 (the second layer) of the NXP LX2160XN72029B Processor includes a third ground plane (yellow) which is configured for electrical connection to low speed electronic circuitry on the die (green). The third ground plane is spatially seperated from and electrically isolated from a fourth ground plane (purple). The fourth ground plane enables electrical connection to high speed electronic circuitry on the die (e.g. electrical connection to high speed PCIe circuitry on the die) (pink). Metal Layer 2/Second layer 

a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate;	The NXP LX2160XN72029B Processor includes a plurality of electrical connections through the package substrate that electrically connect the first ground plane of Metal Layer 1 with solder balls mounted on the second surface of the substrate. 
a plurality of additional electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate; and	The NXP LX2160XN72029B Processor includes a further plurality of electrical connections through the package substrate that electrically connect the second ground plane of Metal Layer 1 with solder balls mounted on the second surface of the substrate. 

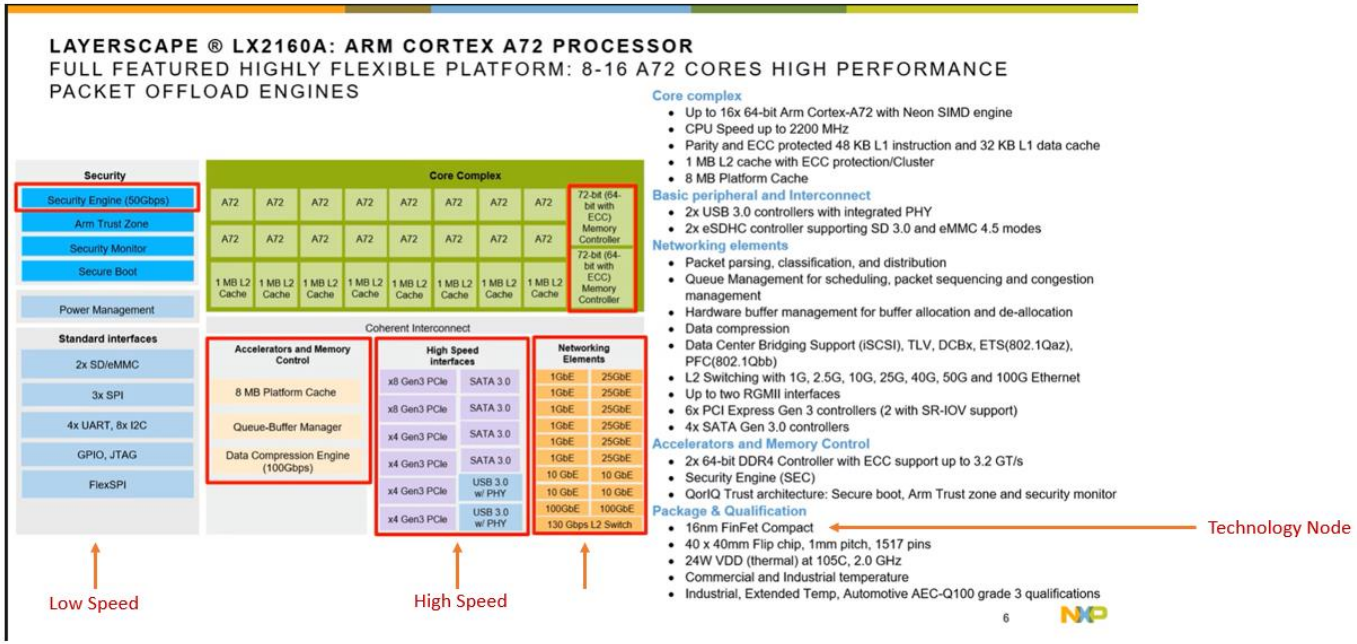
peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package; and	The NXP LX2160XN72029B Processor includes peripheral electrical contacts arranged on Metal Layer 8of the package substrate, which are configured for connection with external electronic circuitry through solder balls mounted on the second surface of the substrate. 

at least one reference plane associated with each layer of the substrate and the ground planes included thereon.	The NXP LX2160XN72029B Processor includes at least one reference plane (*e.g.*, one or more of the ground plane(s) of Metal Layer 8) associated with each layer of the substrate, and which serves as a reference plane relative to each of the ground planes included on each layer of the package substrate. 

Claim 5	Accused Products
5. An IC package as recited in claim 1 wherein the low speed electronic circuitry is defined as circuitry having serial transfer rates of less than about 1 Gigabits per second (Gb/s); and wherein the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 1 Gb/s.	The Accused Products contain an IC package as recited in claim 1, wherein low speed electronic circuitry that is defined as circuitry having serial transfer rates of less than about 1 Gigabits per second (Gb/s); and wherein the high speed electronic circuity is defined as circuitry having serial transfer rates of greater than about 1 Gb/s. *See* claim 1.

- Arm Cortex®-A72 cores:
  - Up to 2.2 GHz
  - Single-threaded cores with 48KB L1 instruction cache and 32KB L1 data cache
  - LX2160A has 16 cores, 8 MB L2 cache; LX2120A has 12 cores, 6 MB L2 cache; LX2080A has 8 cores, 8 MB L2 cache
- Cache Coherent Interconnect Fabric
  - Up to 1500 MHz
  - 8 MB Level 3 cache with ECC and On-Chip Memory (OCM) mode
- Two 72-bit (64-bit + ECC) 3.2 GT/s DDR4 SDRAM memory controllers with ECC
- Datapath acceleration architecture 2.0 (DPAA2)
  - Packet parsing, classification, and distribution (WRIOP)
  - Queue and Hardware buffer management
  - Cryptography acceleration (SEC) at up to 50 Gbps
  - Decompression/compression acceleration (DCE) at up to 100 Gbps
  - Queue Direct Memory Access (QDMA) engine
  - Management Complex (MC)
  - 2 MB Packet Express Buffer
  - L2 Switching (114 Gbps)
- 24 SerDes lanes at up to 25 Gbps
- High-speed peripheral interfaces
  - Two PCIe Gen 3.0 8-lane controllers supporting SR-IOV
  - Four PCIe Gen 3.0 4-lane controllers
  - Four serial ATA (SATA 3.0) controllers
- Ethernet interfaces supporting IEEE 1588
  - Up to 18 Ethernet MACs
  - Support for 10G-SXGMII (USXGMII)
  - Support for SGMII (and 1000Base-KX)
  - Support for XFI, SFI, and 10GBase-KR
  - Support for CAUI4 (100G), CAUI2 (50G), 25G-AUI (25G)
  - Support for XLAUI4 (and 40GBase-KR4) for 40G
  - Support for two RGMII parallel interfaces
  - Energy-efficient support (802.3az)
- Additional peripheral interfaces
  - Two USB 3.0 controllers with integrated PHY
  - Two enhanced secure digital host controllers
  - Two Controller Area Network (CAN) modules, optionally supporting Flexible Datarate
  - Flexible Serial Peripheral Interface (FlexSPI) and three Serial Peripheral Interface (SPI) controllers
  - Eight I2C controllers
  - Four UARTs
  - General Purpose IO (GPIO)
- Support for hardware virtualization and partitioning enforcement (ARM MMU-500)
- Global interrupt controller (ARM GIC-500)
- QorIQ platform trust architecture 3.0 with 256 KB on-chip RAM for trusted accesses
- Two Flextimers, one secure watchdog timer and one non-secure watchdog timer
- Debug supporting run control, data acquisition, high-speed trace, and performance/event monitoring
- Support for Voltage ID (VID) for yield improvement

Source: https://www.mouser.com/datasheet/2/302/phgl_s_a0010925048_1-2279606.pdf



Source: https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/layerscape-processors/layerscape-lx2160a-lx2120a-lx2080a-processors:LX2160A

Claim 6	Accused Products
6. An IC package as recited in claim 1 wherein the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 8.5 Gb/s.	The Accused Products include an IC package as recited in claim 1 wherein the high speed electronic circuitry is defined as circuitry having serial transfer rates of greater than about 8.5 Gb/s. *See* claims 1 and 5.

Claim 8	Accused Products
8. An IC package as recited in claim 1 wherein the peripheral electrical contacts include: a first set of electrical contacts for electrical connection with low speed electronic circuitry; and a second set of electrical contacts for electrical connection with high speed electronic circuitry; and wherein the second set of electrical contacts are spaced	The Accused Products include an IC package as recited in claim 1, wherein the peripheral electrical contacts include: a first set of electrical contacts for electrical connection with low speed electronic circuitry; and a second set of electrical contacts for electrical connection with high speed electronic circuitry; and wherein the second set of electrical contacts are spaced apart at a distance sufficient to establish a differential impedance of at least 100 ohms (Ω) between the contacts of the second set. *See* claims 1 and 5.

apart at a distance sufficient to establish a differential impedance of at least 100 ohms (Ω) between the contacts of the second set.	

Claim 10	Accused Products
10. An IC package as recited in claim 1 wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with low speed electronic circuitry; and a second set of electrical contacts for electrical connection with high speed electronic circuitry; and wherein the electrical contacts are arranged as part of I/O lines such that, a first spacing between the contacts of the first set of electrical contacts is sufficient to establish a	The Accused Products include an IC package as recited in claim 1, wherein the peripheral electrical contacts include: a first set of electrical contacts for electrical connection with low speed electronic circuitry; and a second set of electrical contacts for electrical connection with high speed electronic circuitry; and wherein the electrical contacts are arranged as part of I/O lines such that, a first spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance of at least 50Ω between the contacts of the first set of electrical contacts to substantially eliminate cross-talk between I/O lines for the low speed electronic circuitry; and a second spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100Ω between the contacts of the second set of electrical contracts to substantially eliminate cross-talk between I/O lines for the high speed electronic circuitry. *See* claims 1 and 5.

control differential impedance of at least 50Ω between the contacts of the first set of electrical contacts to substantially eliminate cross-talk between I/O lines for the low speed electronic circuitry; and a second spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100Ω between the contacts of the second set of electrical contracts to substantially eliminate cross-talk between I/O lines for the high speed electronic circuitry.	

Claim 11	Accused Products
11. An IC package as recited in claim 1 wherein the peripheral electrical contacts include, a first set of	The Accused Products include an IC package as recited in claim 1, wherein the peripheral electrical contacts include: a first set of electrical contacts for electrical connection with low speed electronic circuitry; and a second set of electrical contacts for electrical connection with high speed electronic circuitry; and wherein the electrical contacts are arranged such that, a first spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance of at least 50Ω

electrical contacts for electrical connection with low speed electronic circuitry; and a second set of electrical contacts for electrical connection with high speed electronic circuitry; and wherein the electrical contacts are arranged such that, a first spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance of at least 50Ω between the contacts of the first set of electrical contacts; and a second spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100Ω between the contacts of the second	between the contacts of the first set of electrical contacts; and a second spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100Ω between the contacts of the second set of electrical contacts. *See* claims 1 and 5.

set of electrical contacts.	

Claim 12	Accused Products
12. An IC package as recited in claim 1 wherein the first surface includes a die attachment surface with a die arrangement attached thereto, the die arrangement being electrically connected to the first ground plane, the second ground plane, and the peripheral electrical contacts of the substrate.	The Accused Products include an IC package as recited in claim 1, wherein the first surface includes a die attachment surface with a die arrangement attached thereto, the die arrangement being electrically connected to the first ground plane, the second ground plane, and the peripheral electrical contacts of the substrate. *See* claims 1 and 5.

Claim 13	Accused Products
13. An IC package as recited in claim 12 wherein the die arrangement comprises a die having both high-speed electronic	The Accused Products include an IC package as recited in Claim 1 wherein the die arrangement comprises a die having both high-speed electronic circuitry and low-speed electronic circuitry; and wherein the peripheral electrical contacts include: a first set of electrical contacts for electrical connection with low speed electronic circuitry; and a second set of electrical contacts for electrical connection with high speed electronic circuitry; and wherein the low-speed electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced for connection with the

circuitry and low-speed electronic circuitry; and wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with low speed electronic circuitry; and a second set of electrical contacts for electrical connection with high speed electronic circuitry; and wherein the low-speed electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced for connection with the low speed electronic circuitry; and wherein the high-speed electronic circuitry is connected with the second ground plan and is electrically	low speed electronic circuitry; and wherein the high-speed electronic circuitry is connected with the second ground plan and is electrically connected with the second set of electrical contacts that are spaced for connection with the high speed electronic circuitry. *See* claims 1, 12, and 5.

connected with the second set of electrical contacts that are spaced for connection with the high speed electronic circuitry.	

Caveat: The notes and/or cited excerpts utilized herein are set forth for illustrative purposes only and are not meant to be limiting in any manner. For example, the notes and/or cited excerpts, may or may not be supplemented or substituted with different excerpt(s) of the relevant reference(s), as appropriate. Further, to the extent any error(s) and/or omission(s) exist herein, all rights are reserved to correct the same.