

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP USA, INC.,

Petitioner,

v.

BELL SEMICONDUCTOR, LLC,

Patent Owner

Case: IPR2024-00167

U.S. Patent No. 7,646,091

PATENT OWNER'S PRELIMINARY RESPONSE

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TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	BACKGROUND	2
A.	The '091 Patent	2
B.	The Cited References	6
III.	LEVEL OF ORDINARY SKILL IN THE ART	7
IV.	CLAIM CONSTRUCTION	7
V.	ARGUMENT	8
A.	PETITIONER FAILS TO ESTABLISH A REASONABLE LIKELIHOOD THAT ANY OF THE CHALLENGED CLAIMS ARE UNPATENTABLE	8
1.	Ground 1: Anticipation of Claim 1 by Okabe.....	8
a.	Distinctions Between Claim 1 and Okabe.....	9
2.	Ground 2: Obviousness of Claim 1 Over Hashemi in View of Okabe	21
a.	Distinctions Between Claim 1 and the Proposed Combination of Hashemi and Okabe	21
B.	Ground 3: Obviousness of Claims 1 and 12 Over Okabe in View of Supposed Applicant's Admitted Prior Art ("AAPA").....	25
1.	Claim 1	26
2.	Claim 12	26
C.	Ground 4: Obviousness of Claims 2, 5, 6, and 9 Over Okabe in View of Supposed AAPA and Sutardja.....	27
D.	Ground 5: Obviousness of Claims 3, 4, and 7 Over Okabe in View of Supposed AAPA, Sutardja, and Taggart.....	27
E.	Ground 6: Obviousness of Claims 8 and 11 Over Okabe in View of Supposed AAPA, Sutardja, and Choi	28
F.	Ground 7: Obviousness of Claim 10 Over Okabe in View of Supposed AAPA, Sutardja, Choi, and Digital Design.....	29
G.	Ground 8: Obviousness of Claim 13 Over Okabe in View of Supposed AAPA, Kramer, and Sutardja.....	29

Case IPR2024-00167
Patent No. 7,646,091
Patent Owner Preliminary Response

H.	Ground 9: Obviousness of Claim 14 Over Okabe in View of Supposed AAPA, Conn, Kramer, and Sutardja	30
VI.	CONCLUSION.....	31

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>Guangdong Alison Hi-Tech Co. v. Int'l Trade Comm'n</i> , 936 F.3d 1353 (Fed. Cir. 2019)	8
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005)	7
Statutes	
35 U.S.C. § 314	8
Regulations	
37 C.F.R. § 42.100	7
37 C.F.R. § 42.107	1

Case IPR2024-00167
Patent No. 7,646,091
Patent Owner Preliminary Response

TABLE OF EXHIBITS

Exhibit	Description
2001	Expert Declaration of Dr. Joseph Bernstein in Support of Patent Owner's Preliminary Response

Through the undersigned Counsel, Patent Owner Bell Semiconductor, LLC (“PO” or “Bell Semic”) submits the following Patent Owner Preliminary Response pursuant to 37 C.F.R. § 42.107(a).

I. INTRODUCTION

The *Inter Partes* Review Petition (the “Petition”) filed by NXP USA, INC. (“NXP”) against U.S. Patent No. 7,646,091 (“’091 Patent”) should be denied because it fails to establish a reasonable likelihood that any of the challenged claims are unpatentable.

Claims 1-14 of the ’091 Patent (the “Challenged Claims”) recite a semiconductor integrated circuit package that includes a dedicated high-speed ground plane that is electrically isolated from the ground plane used to ground the low speed circuitry of the package. Petitioner fails to show a reasonable likelihood that these claims are anticipated or obvious over the cited references at least because the first primary reference fails to disclose any electrically isolated ground planes, much less a dedicated high-speed ground plane that is electrically isolated from a low-speed ground plane on the same layer; and the second primary reference suffers from similar deficiencies. The cited references also lack a reference plane as set forth in the claims. Thus, no *inter partes* review of claims 1-14 should be instituted.

II. BACKGROUND

A. The '091 Patent

The '091 patent (Ex. 1001), entitled “Semiconductor package and method using isolated Vss plane to accommodate high speed circuitry ground isolation,” is entitled to a priority date of April 6, 2006. The '091 Patent is directed to, among other things, reducing noise in a semiconductor integrated circuit (“IC”) package. (Ex. 2001 at ¶ 55.)

Many modern integrated circuits require both low-speed and high-speed circuitry. (Ex. 2001 at ¶ 56.) Excessive noise generated by the high-speed circuitry interferes with the operation of the low-speed circuitry sharing the same ground plane. (Ex. 2001 at ¶ 56.) At high data rates this is a serious problem. (Ex. 2001 at ¶ 56.) Another problem is ground bounce, which can adversely affect performance. (Ex. 2001 at ¶ 56.)

In order to eliminate such problems, the '091 patent teaches a semiconductor integrated circuit package that includes a dedicated high-speed ground plane that is electrically isolated from the ground plane used to ground the low-speed circuitry. (Ex. 2001 at ¶ 57.)

The '091 patent contains 1 independent claim and 14 total claims, covering a semiconductor integrated circuit package. (Ex. 1001 at 9:25-12:24.) Claim 1 of the '091 patent reads:

1. A semiconductor integrated circuit (IC) package which comprises:

a substrate having a first surface and a second surface wherein;

a first layer of the substrate includes,

a first ground plane enabling electrical connection with low speed electronic circuitry, and

a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection with high speed electronic circuitry;

a second layer of the substrate includes,

a third ground plane configured for electrical connection with low speed electronic circuitry, and

a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the fourth¹ ground plane configured for electrical connection with high speed electronic circuitry;

a plurality of electrical connections that electrically

¹ A Certificate of Correction was issued by the Patent Office on April 27, 2021 changing, at Col. 9, line 41, “the third ground plane configured for electrical” to “the fourth ground plane configured for electrical.” (Ex. 1004 at 243.)

connect the first ground plane with solder balls mounted on the second surface of the substrate;

- a plurality of additional electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate; and

peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package; and

at least one reference plane associated with each layer of the substrate and the ground planes included thereon.

(Ex. 1001 at 9:25-54.) This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, e.g., improving system performance by reducing cross-talk and ground-bounce. (Ex. 2001 at ¶ 59.)

Prior to the '091 patent, the traditional approach for designing a semiconductor integrated circuit package was to include a single ground plane for all IC systems and grounds. (Ex. 1001 at 1:23–28; Ex. 2001 at ¶ 60.) This arrangement did not present problems when all systems in the package operated at low frequencies or low serial data transfer rates. (Ex. 2001 at ¶ 60.) However, at high speeds a number of problems begin to occur. (Ex. 2001 at ¶ 60.) For one, excessive noise generated by the high-speed circuitry interferes with the operation of the low-speed circuitry sharing the same ground plane, presenting a serious problem at high data rates. (Ex. 1001 at 2:10–12; Ex. 2001 at ¶ 60.) Furthermore,

older packaging substrates developed with lower speed circuitry in mind were configured with the I/O and ground contacts spaced more closely together for maximum electrical contact density. (Ex. 2001 at ¶ 60.) However, at high frequencies and data rates, signal and ground lines that are too closely spaced exhibit large amounts of cross-talk, harming signal integrity and device performance. (Ex. 1001 at 2:13–19; Ex. 2001 at ¶ 60.) These issues were difficult to overcome. (Ex. 2001 at ¶ 60.) For example, one prior art approach required that individual pins be used for separately grounding each high-speed ground connection, which used up a large number of the limited number of pins available in the package. (Ex. 1001 at 2:24-27; Ex. 2001 at ¶ 60.) This also increased the density of high-speed interconnections, producing additional undesirable cross-talk between all ground and I/O lines. (Ex. 1001 at 2:27–31; Ex. 2001 at ¶ 60.) Such packages had provided satisfactory grounding for packaging substrates, but with the increasing IC speeds and data transfer rates, it became clear to the inventors, Maurice O. Othieno, Chok J. Chia, and Amar J. Amin (“the ’091 Inventors”), that this traditional package format needed improvement. (Ex. 2001 at ¶ 60.)

The ’091 Inventors understood the limitations of the prior technologies and set out to develop a package design that provided superior grounding properties enabling both high speed and low speed circuitry to be used in the same packaging

substrate. (Ex. 1001 at 2:35–38; Ex. 2001 at ¶ 61.) The '091 Inventors ultimately devised a package with a dedicated high-speed ground plane that is electrically isolated from the ground plane used to ground the low-speed circuitry. (Ex. 1001 at 2:45–48; Ex. 2001 at ¶ 61.)

B. The Cited References

The Petition cites the following references:

- U.S. Patent No. 7,515,879 to Okabe et al. (“Okabe”) (Ex. 1005), issued on April 7, 2009, based on an application filed December 17, 2004;
- U.S. Patent No. 6,377,464 to Hashemi et al. (“Hashemi”) (Ex. 1006), issued April 23, 2002, based on an application filed January 29, 1999;
- U.S. Patent No. 7,420,286 to Kramer (“Kramer”) (Ex. 1007), issued September 2, 2008, based on an application filed July 22, 2005;
- U.S. Patent Pub. No. 2006/0001180 to Taggart et al. (“Taggart”) (Ex. 1009), published January 5, 2006;
- Johnson, H. W., & Graham, M. (1993). *High Speed Digital Design: A Handbook of Black Magic*. PTR Prentice Hall., ISBN:0-13-395724-1 (“Digital Design”) (Ex. 1010);
- Jinwoo Choi, Sung-Hwan Min, Joong-Ho Kim, Madhavan Swaminathan, Wendemagegnehu (Wendem) Beyene, and Xingchao (Chuck) Yuan, *Modeling and Analysis of Power Distribution Networks for Gigabit Applications*, IEEE Transactions on Mobile Computing, Vol. 2, No. 4, October-December 2003, pages 299-313 (“Choi”) (Ex. 1011);
- U.S. Patent Pub. No. 2007/0018292 to Sutardja (“Sutardja”) (Ex. 1012), published January 25, 2007; and

- U.S. Patent No. 7,084,487 to Conn (“Conn”) (Ex. 1013), issued August 1, 2006, based on an application filed December 9, 2003.

III. LEVEL OF ORDINARY SKILL IN THE ART

Petitioner and its expert Dr. Baker allege a definition of a person of ordinary skill in the art (“POSITA”). (Pet. at 4; Ex. 1002 at ¶ 20.) Neither explain why a POSITA would require such qualifications. For purposes of this Preliminary Response only, PO’s analysis of the Challenged Claims and the cited art adopts Petitioner’s alleged definition. Should *inter partes* review be instituted, PO reserves the right to present an alternative definition for a person of ordinary skill in the art, along with any appropriate additional evidence.

IV. CLAIM CONSTRUCTION

Claims in an *inter partes* review are construed using the same claim construction standard as in a civil action. 37 C.F.R. § 42.100(b). Under this standard, claims are construed in accordance with their ordinary and customary meaning as understood by a person of ordinary skill in the art (“POSITA” or “skilled artisan”). *Id.* The person of ordinary skill in the art is deemed to read the claim term in the context of the entire patent, including the specification and prosecution history. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313-1316 (Fed. Cir. 2005) (en banc). Indeed, claims must be construed so as to be consistent with the specification. *Id.*

The Petition alleges that no express constructions of the claims are necessary to assess whether the cited art reads on the challenged claims. (Pet. at 8.) For purposes of this Preliminary Response only, Patent Owner presents no express constructions of the claims. Patent Owner reserves the right to propose constructions of the claims should *inter partes* review be instituted.

V. ARGUMENT

A. PETITIONER FAILS TO ESTABLISH A REASONABLE LIKELIHOOD THAT ANY OF THE CHALLENGED CLAIMS ARE UNPATENTABLE

The petitioner in an *inter partes* review bears the burden of proving that there is a reasonable likelihood that it will prevail with respect to at least one of the challenged claims. 35 U.S.C. § 314(a). Petitioner has failed to meet this burden. Specifically, Petitioner has failed to show that it is more likely than not that the cited art anticipates or renders obvious the claimed invention.

1. Ground 1: Anticipation of Claim 1 by Okabe

Petitioner has failed to show a reasonable likelihood that Okabe anticipates claim 1 by expressly or inherently disclosing each and every element of the claim. *Guangdong Alison Hi-Tech Co. v. Int'l Trade Comm'n*, 936 F.3d 1353, 1363 (Fed. Cir. 2019) (“A patent claim is invalid as anticipated only if each and every element of the claim is expressly or inherently disclosed in a single prior art reference.”).

a. Distinctions Between Claim 1 and Okabe

(1) Okabe Does Not Disclose Electrically Isolated Ground Planes

Claim 1 recites a semiconductor integrated circuit (IC) package which comprises, *inter alia*, the following limitations:

a first layer of the substrate includes,

a first ground plane enabling electrical connection with low speed electronic circuitry, and

a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection with high speed electronic circuitry;

a second layer of the substrate includes,

a third ground plane configured for electrical connection with low speed electronic circuitry, and

a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the fourth ground plane configured for electrical connection with high speed electronic circuitry.

(Ex. 1001 at 9:25-54) (emphasis added).

Okabe does not disclose the claimed “a second ground plane that is spatially separated and ***electrically isolated*** from the first ground plane” or “a fourth ground plane that is spatially separated and ***electrically isolated*** from the third ground plane.” (Ex. 2001 at ¶ 64.) Though Petitioner asserts that such ground planes are disclosed (e.g., Pet. at 11, 24-27), one need only read the Abstract of Okabe to see

that its ground planes are not “electrically isolated,” but rather share a “common ground plane,” through which they are electrically connected. (Ex. 1005 at Abstract; Ex. 2001 at ¶ 64.) Petitioner admits as much: “Okabe also teaches a common ground plane . . . to which all separate ground planes are connected[.]” (Pet. at 8; Ex. 2001 at ¶ 64.)

Petitioner relies on an annotated version of Figure 14 of Okabe (reproduced below) for alleged disclosure of the “first ground plane,” “second ground plane,” “third ground plane,” and “fourth ground plane” features of claim 1. (Pet. at 23-25.) According to Okabe, Figure 14 “depicts the ground connections” of the invention. (Ex. 1005 at 14:26; Ex. 2001 at ¶ 65.) Petitioner identifies “PA ground plane 110” as the claimed “first ground plane” (Pet. at 24), and Okabe’s specification states, “The PA ground plane 110 is connected to the common ground plane 480,” which Petitioner identifies as a “Reference Plane” in its annotated FIG. 14, below. (Ex. 1005 at 14:35-36; Ex. 2001 at ¶ 65.)

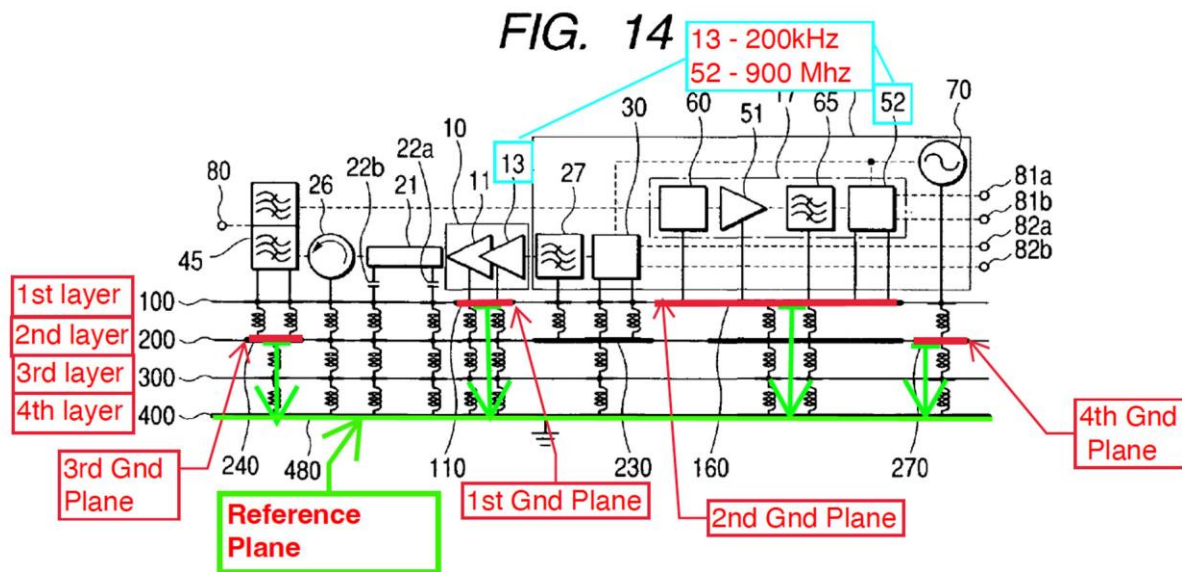


FIG. 14 of Okabe (Ex. 1005) (Annotated by Petitioner), Pet. at 24

Petitioner next identifies the “receive circuits ground plane 160” as the claimed “second ground plane.” (Pet. at 25.) But “the receive circuits ground plane 160 is connected to the common ground plane 480” too. (Ex. 1005 at 14:67-15:1; Ex. 2001 at ¶ 66.) So, Petitioner’s alleged “first ground plane” and “second ground plane” of Okabe are, at minimum, connected to each other via their respective connections to the “common ground plane” and therefore cannot be “electrically isolated” from each other as required by claim 1. (Ex. 2001 at ¶ 66.)

With respect to the claimed “third ground plane” and “fourth ground plane,” Petitioner falls into the same trap, equating these ground planes with ground planes 240 and 270 of Okabe, respectively, both of which also connect to the “common

ground plane 480.” (Pet. at 26-27; Ex. 1005 at 14:48-63, FIG. 14; Ex. 2001 at ¶ 67.)

The alleged third and fourth ground planes in Okabe are therefore electrically connected, as opposed to being “electrically isolated” as required by claim 1. (Pet. at 26-27; Ex. 1005 at 14:48-63; Ex. 2001 at ¶ 67.)

For these reasons alone, it is clear that Figure 14 of Okabe does not establish a reasonable likelihood of anticipation of claim 1. (Ex. 2001 at ¶ 68.)

(2) Okabe Does Not Disclose Electrically Isolated Low Speed and High Speed Ground Planes on a First Layer

Claim 1 recites, *inter alia*, the following limitations:

. . . a first layer of the substrate includes,

a first ground plane enabling ***electrical connection with low speed electronic circuitry***, and

a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling ***electrical connection with high speed electronic circuitry*** . . .

(Ex. 1001 at 9:29-35) (emphasis added).

Okabe does not disclose the claimed “a first ground plane enabling ***electrical connection with low speed electronic circuitry***,” and “a second ground plane . . . enabling ***electrical connection with high speed electronic circuitry***” on a first layer. (Ex. 2001 at ¶ 70.) Though Petitioner asserts that ground planes meeting these limitations are disclosed by Okabe (e.g., Pet. at 11, 24-25), Petitioner overlooks a

typo—in a portion of Okabe upon which Petitioner relies—conflating the “BB-LSI 3” with the “first-stage amplifier 13.” (Ex. 2001 at ¶ 70.) That is, Okabe mistakenly refers to BB-LSI 3 as “BB-LSI 13” in the paragraph beginning at Col. 7, line 36, and Petitioner relies on this typo to “prove” that the first-stage amplifier 13 is a low speed circuit (*e.g.*, Pet. at 24). (Ex. 2001 at ¶ 70.)

This is a critical error on Petitioner’s part because, under Petitioner’s criteria for “low speed” versus “high speed,” BB-LSI 3 is a low speed electronic circuit, whereas the first-stage amplifier 13 is actually a high speed electronic circuit. (Ex. 2001 at ¶ 71.) As a result, the components in Okabe identified by Petitioner as the first and second ground planes do not meet the “low speed” and “high speed” limitations of claim 1. (Ex. 2001 at ¶ 71.) More specifically, the ground plane 110 identified by the Petitioner as the “first ground plane” does not enable connection with low speed electronic circuitry as required by claim 1. (Ex. 2001 at ¶ 71.) Rather, the ground plane 110 enables connection with high speed circuitry (*i.e.*, the first-stage amplifier 13). (Ex. 2001 at ¶ 71.)

When read in the context of the entire Okabe disclosure, it is clear that the language at issue is a typographical error. (Ex. 2001 at ¶ 72.) According to Okabe, the BB-LSI 3 is a base band large scale integrated circuit that encodes a voice input from a microphone, which is then modulated into a transmit signal and converted

into a transmitting frequency by the transmitter in the radio frequency integrated circuit (“RF-IC”). (Ex. 1005 at 2:3-7; Ex. 2001 at ¶ 72.) Under Petitioner’s criteria for low speed versus high speed in the context of Okabe (i.e., 200 kHz vs. 900 MHz) (Pet. at 24), a POSITA would understand the BB-LSI 3 to be low speed circuitry (operating up to around 200 kHz) and the RF-IC to be high speed circuitry (operating at 900 MHz). (Ex. 2001 at ¶ 72.) Okabe further explains how the low speed transmit signal from the BB-LSI 3 is converted to a high speed RF transmit signal by the RF-IC. (Ex. 1005 at 2:3-7; Ex. 2001 at ¶ 72.) Later, Okabe explains how the first-stage amplifier 13 is part of the power amp (PA 10) that amplifies the RF transmit signal from the RF-IC. (Ex. 1005 at 7:52-55; Ex. 2001 at ¶ 72.) As such, the first-stage amplifier must be able to operate at the same RF frequency as the RF signal from the RF-IC and would therefore also be considered by a POSITA to be high speed circuitry. (Ex. 2001 at ¶ 72.)

The order of appearance of the terms in Okabe also confirms that Petitioner relied on a typographical error for its argument. (Ex. 2001 at ¶ 73.) As noted above, Okabe first mentions the BB-LSI in the Summary of the Invention. (Ex. 1005 at 2:3-7 (“a voice input from a microphone is encoded by a base band large scale integrated circuit (hereinafter referred to as ‘BB-LSI’)”); Ex. 2001 at ¶ 73.) The BB-LSI is mentioned again in a paragraph (“first paragraph”) of the Detailed Description

immediately preceding the paragraph in which the typographical error appears. (Ex. 1005 at 7:4-15 (“transmitter 30 . . . converts the frequency of the transmit signal . . . which is output from ***an external*** BB-LSI 3 . . . into a transmitting frequency. . .”) (emphasis added); Ex. 2001 at ¶ 73.) The following paragraph (“second paragraph”) then refers to “the transmit signal which is output from ***the*** BB-LSI **13**” and “the receive signal which is input to ***the*** BB-LSI **13**,” which “are in a frequency band of about 200 kHz[.]” (Ex. 1005 at 7:36-38 (emphasis added); Ex. 2001 at ¶ 73.) And, “the RF transmit signal which is output from the transmitter 30 and the RF receive signal which is input to the receiver 52 are in a frequency band of 900 MHz.” (Ex. 1005 at 7:38-41; Ex. 2001 at ¶ 73). It is not until the next paragraph (“third paragraph”) that “***a*** . . . first-stage amplifier 13” is introduced as a component of power amplifier “PA 10.” (Ex. 1005 at 7:52-55 (emphasis added); Ex. 2001 at ¶ 73.) The reference to “***the*** BB-LSI” in the second paragraph, after discussion of “***an external*** BB-LSI 3” in the first paragraph and before “***a*** . . . first-stage amplifier 13” is introduced in the third paragraph, confirms that the reference to “BB-LSI 13” in the second paragraph is a typographical error and that Okabe meant to say “BB-LSI 3.” (Ex. 2001 at ¶ 73.)

For the convenience of the Board, components BB-LSI 3 and first-stage amplifier 13 are both highlighted in yellow in annotated versions of FIGS. 1-2 below

to show that they represent separate components. (Ex. 2001 at ¶ 74.)

FIG. 1

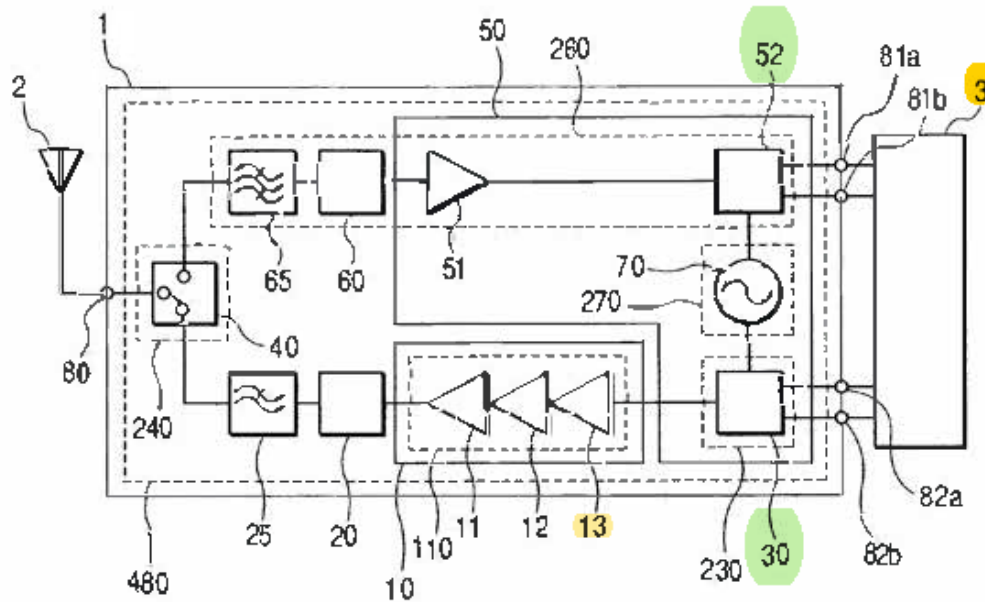
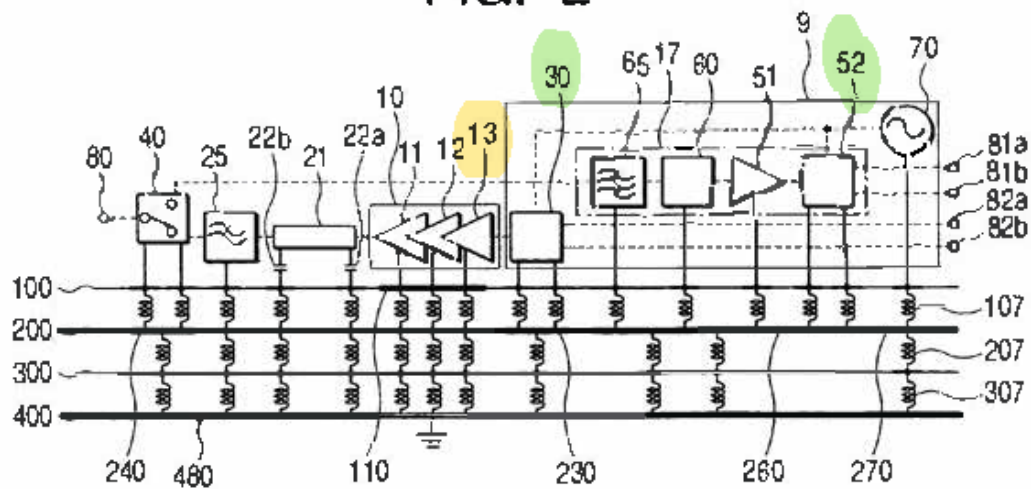


FIG. 2



FIGS. 1-2 of Okabe (Ex. 1005) (Annotated by PO)

As noted above, Petitioner relies on the typo for its argument that “circuit 13

operates in a frequency band of 200 kilohertz (kHz), while circuit 52 operates in a frequency band of 900 megahertz (MHz),” citing only the second paragraph at 7:36-41. (Pet. at 24; Ex. 2001 at ¶ 75.) It should be noted that Okabe makes clear in that paragraph that “the RF transmit signal which is output from the transmitter 30 and the RF receive signal which is input to the receiver 52 are in a frequency band of 900 MHz.” (Ex. 1005 at 7:38-41; Ex. 2001 at ¶ 75; *see also* green highlights in annotated FIGs. 1-2 above). Further, “the PA 10 . . . amplifies the power level of an RF transmit signal . . . output from the transmitter 30.” (Ex. 1005 at 7:10-12; Ex. 2001 at ¶ 75.) So, the “PA 10” component receives the “output from the transmitter 30,” which is an “RF transmit signal . . . in a frequency band of 900 MHz,” and the “receiver 52” receives an “RF receive signal,” which is also “in a frequency band of 900 MHz.” (Ex. 2001 at ¶ 75.) The “first-stage amplifier 13” is a component of “PA 10” and therefore receives an RF signal in a frequency band of 900 MHz, which is the same frequency band that component 52 receives. (Ex. 2001 at ¶ 75.) Thus, components 13 and 52 operate in the same frequency band, and one cannot be said to be “high-speed” while the other is “low-speed.” (Ex. 2001 at ¶ 75.)

The same typo is present with respect to FIGs. 13-14, with the difference being that components 13 and 52 operate at approximately 2.0GHz instead of 900MHz. (Ex. 1005 at 14:5-11; Ex. 2001 at ¶ 76.) FIG. 13 and Petitioner’s

annotated FIG. 14 are shown below, confirming that component first-stage amplifier 13 is again different from component BB-LSI 3. (Ex. 2001 at ¶ 76.)

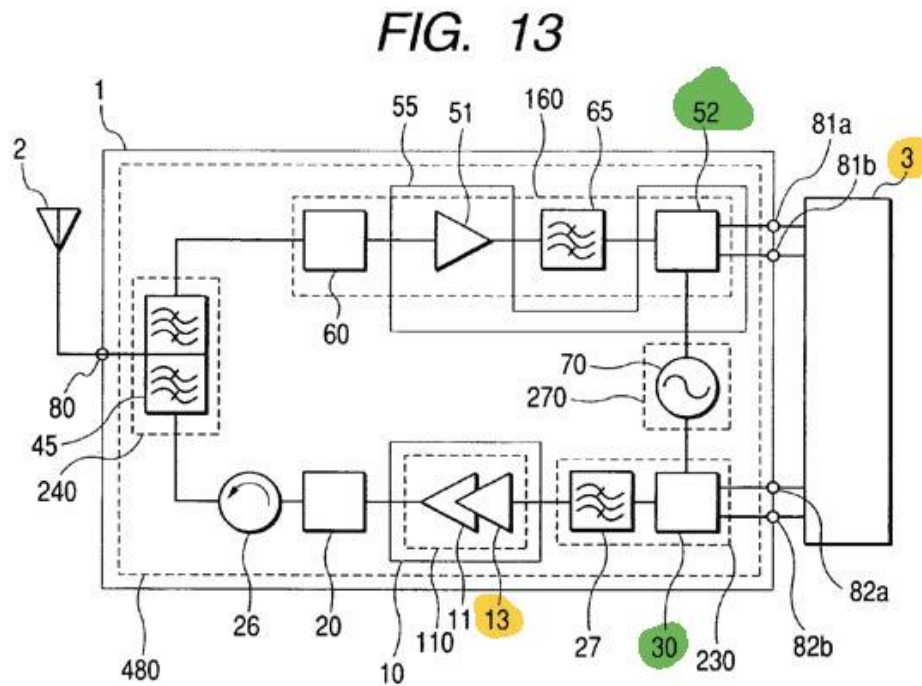


FIG. 13 of Okabe (Ex. 1005) (Annotated by PO)

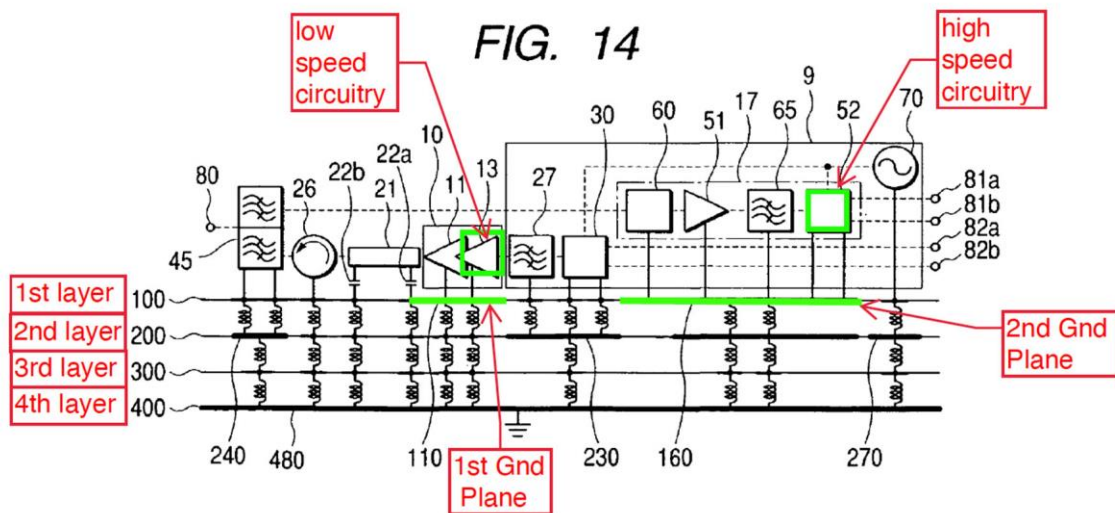


FIG. 14 of Okabe (Ex. 1005) (Annotated by Petitioner), Pet. at 25

For at least all of the above reasons, Petitioner's argument that Okabe teaches the first layer "high speed" and "low speed" ground plane limitations of claim 1 is simply wrong. (Ex. 2001 at ¶ 77.)

(3) Okabe Does Not Disclose Electrically Isolated Low Speed and High Speed Ground Planes on a Second Layer

Claim 1 recites, *inter alia*, the following limitations:

. . . a second layer of the substrate includes,
a third ground plane configured for ***electrical connection with low speed electronic circuitry***, and
a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the fourth ground plane configured for electrical connection ***with high speed electronic circuitry*** . . .

(Ex. 1001 at 9:36-42) (emphasis added).

Okabe does not disclose the claimed "a third ground plane configured for ***electrical connection with low speed electronic circuitry***," and "a fourth ground plane . . . configured for electrical connection ***with high speed electronic circuitry***" on a second layer. (Ex. 2001 at ¶ 79.) Petitioner asserts that the third ground plane limitation is met by ground plane 240 in Figure 14 of Okabe because it connects to duplexer 45, and that the fourth ground plane limitation is met by ground plane 270 that is located on the same substrate layer as ground plane 240 and connected to

voltage control oscillator (“VCO”) 70 in the RF-IC, because VCO 70 allegedly operates at a higher speed than duplexer 45. (Pet. at 26-27.) However, Petitioner does not specify the respective speeds at which the duplexer 45 and VCO 70 operate or provide any criteria for classifying circuitry as high speed or low speed. (*Compare* with Ex. 1001 at 4:15-24; Ex. 2001 at ¶ 79.) Petitioner fails to provide any evidence at all to corroborate its conclusory statement that the duplexer meets the “low speed circuitry” limitation and the VCO meets the “high speed circuitry” limitation. (Ex. 2001 at ¶ 79.) In fact, Okabe provides evidence to the contrary. (Ex. 2001 at ¶ 79.)

For example, according to Okabe, “an RF signal received by the antenna goes through the antenna duplex circuit” and “a local oscillation signal with a specific frequency, generated by the VCO in the RF-IC, is used for the frequency conversion by the transmitter and the receiver.” (Ex. 1005 at 2:13-23; Ex. 2001 at ¶ 80.) Petitioner contends that the VCO 70, which provides a radio frequency (“RF”) modulating signal for frequency conversion in such circuits (Ex. 2001 at ¶ 80), meets the “high speed circuitry” limitation. (Pet. at 26-27.) To be consistent, it follows that the duplexer 45, which transfers RF signals, must also be considered “high speed circuitry.” (Ex. 2001 at ¶ 80.) Accordingly, both VCO 70 and duplexer 45 would be “high speed circuitry,” and Petitioner has not shown a reasonable likelihood that

Okabe discloses electrically isolated low speed and high speed ground planes on a second layer. (Ex. 2001 at ¶ 80.)

(4) Okabe Does Not Teach the Claimed Reference Plane

Petitioner argues that Okabe’s common ground plane 480 teaches the claimed “reference plane” because Okabe states, “By providing the module with the common ground plane 480 to which all ground planes are connected, **reference potential** for all RF circuits can be fixed, not dependent on the ground land on the motherboard.” (Pet. at 30, citing Ex. 1005 at 11:14-18) (original emphasis). But this statement contradicts the claim language. (Ex. 2001 at ¶ 81.) Claim 1 requires that the ground planes be “electrically isolated,” and Okabe’s common ground plane “to which ***all ground planes are connected***” creates a situation in which all ground planes are electrically connected instead of isolated. (Ex. 2001 at ¶ 81.) Therefore, Okabe’s “common ground plane” cannot be the claimed “reference plane,” and Petitioner’s argument fails. (Ex. 2001 at ¶ 81.)

2. Ground 2: Obviousness of Claim 1 Over Hashemi in View of Okabe

a. Distinctions Between Claim 1 and the Proposed Combination of Hashemi and Okabe

(1) Petitioner Has Not Shown That The Proposed Combination Includes, on a First Layer, First and Second Electrically Isolated Ground Planes Connected to Respective Low Speed and High

Speed Circuitry

Claim 1 recites, *inter alia*, the following limitations:

. . . a first layer of the substrate includes,
a first ground plane enabling ***electrical connection with low speed electronic circuitry***, and
a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection ***with high speed electronic circuitry*** . . .

(Ex. 1001 at 9:29-35) (emphasis added).

Petitioner has not shown a reasonable likelihood that the proposed combination of Hashemi and Okabe discloses the claimed “first ground plane enabling ***electrical connection with low speed electronic circuitry***,” and “second ground plane . . . enabling electrical connection ***with high speed electronic circuitry***” on a first layer. (Ex. 2001 at ¶ 84.) Petitioner argues that Hashemi teaches these limitations because it discloses a first ground plane 122 that connects to a first circuit chip 104 that operates “at different frequencies” than a second circuit chip 104 connected to a second ground plane 124. (Pet. at 32-33.) However, Petitioner completely fails to address the claim requirement that the first and second ground planes be on a first layer of the substrate. (Ex. 2001 at ¶ 84.) And, apart from noting that the first and second circuit chips 104 may operate at different frequencies, Petitioner fails to provide any criteria for classifying circuitry as low speed or high

speed and fails to provide any evidence to corroborate its conclusory statement that the first circuit chip 104 meets the “low speed circuitry” limitation and that the second circuit chip 104 meets the “high speed circuitry” limitation. (Ex. 2001 at ¶ 84.) In fact, Hashemi provides evidence to the contrary. (Ex. 2001 at ¶ 84.)

For example, Hashemi states that its “split ground plane techniques” may be utilized to achieve “the use of active circuit chips having multiple and isolated RF functions on a single dielectric substrate” (Ex. 1006 at 8:4-9), and that “the MCM may employ split RF ground planes . . . to promote effective RF grounding and isolation between different RF chips or different sections within a single RF chip” (Ex. 1006 at 11:10-15). (Ex. 2001 at ¶ 85.) In RF systems, baseband components may be thought of by the POSITA as low speed circuitry, and RF/IF components may be thought of as high speed circuitry. (Ex. 2001 at ¶ 85.) These statements and others in Hashemi are evidence that the split ground planes in Hashemi are in fact each connected to a chip that can be considered high speed circuitry (e.g., RF/IF chips and components)—while Petitioner has failed to provide anything other than conclusory statements that Hashemi teaches use of split ground planes to isolate low speed circuitry from high speed circuitry. (Ex. 2001 at ¶ 85.)

(2) Petitioner Has Not Shown That The Proposed Combination Includes, on a Second Layer, Third and Fourth Electrically Isolated Ground Planes Connected to Respective Low Speed and High

Speed Circuitry

Claim 1 recites, *inter alia*, the following limitations:

. . . a second layer of the substrate includes,
a third ground plane configured for ***electrical connection with low speed electronic circuitry***, and
a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the fourth ground plane configured for electrical connection ***with high speed electronic circuitry*** . . .

(Ex. 1001 at 9:36-42) (emphasis added).

Petitioner has not shown a reasonable likelihood that the proposed combination of Hashemi and Okabe discloses the claimed “a third ground plane configured for ***electrical connection with low speed electronic circuitry***,” and “a fourth ground plane . . . configured for electrical connection ***with high speed electronic circuitry***” on a second layer. (Ex. 2001 at ¶ 87.) Petitioner argues that Hashemi teaches these limitations because it discloses “the MCM may employ split RF ground planes, located at indeterminate metal layers or at the lower exposed metal layer,” and that a POSITA would understand that the split ground planes were not limited to a single layer, but would include a third and fourth ground plane on another layer. (Pet. at 33-35.) However, Petitioner overlooks Hashemi’s characterization of the split ground planes as split “***RF***” ground planes, suggesting that the split ground planes are both high speed ground planes—not one low speed

and the other high speed. (Ex. 2001 at ¶ 87.)

Petitioner also refers to Okabe as backup support if it is found that Hashemi does not disclose these claim features. (Pet. at 33-35.) However, as noted above in Sections A.1.a.(1) and A.1.a.(3), Okabe also fails to disclose these features. Accordingly, Petitioner has not shown a reasonable likelihood that the proposed combination of Hashemi and Okabe would read on these claim features.

(3) Petitioner Has Not Shown That The Proposed Combination Includes the Claimed “Reference Plane”

Petitioner relies on Okabe to teach the “reference plane” limitation in claim 1. (Pet. at 37.) However, as discussed above in Section A.1.a.(4), Okabe does not teach the claimed reference plane because Okabe’s alleged “reference plane” electrically connects all ground planes, rendering the ground planes electrically **connected** as opposed to electrically **isolated**, as required by the claim language. (Ex. 2001 at ¶ 88.) Therefore, because Okabe does not teach the claimed “reference plane,” and Petitioners rely exclusively on Okabe to teach this claim term, the combination of Hashemi and Okabe does not teach or suggest the claimed “reference plane.” For at least this reason, Petitioner’s proposed combination does not establish a reasonable likelihood that claim 1 would have been obvious. (Ex. 2001 at ¶ 88.)

B. Ground 3: Obviousness of Claims 1 and 12 Over Okabe in View of Supposed Applicant’s Admitted Prior Art (“AAPA”)

1. Claim 1

In the proposed combination of references, Petitioner relies only on Okabe for the “second ground plane,” the “third ground plane,” and the “fourth ground plane” limitations in claim 1. (Pet. at 39-40.) As discussed above in Section A.1, Okabe does not teach these limitations. Therefore, Petitioner’s combination of Okabe and supposed AAPA does not establish a reasonable likelihood that claim 1 is obvious.

PO reserves the right to present additional arguments for patentability of claim 1 over Okabe in view of supposed AAPA should *inter partes* review be instituted.

2. Claim 12

Claim 12 depends from claim 1. A dependent claim contains all of the limitations of the claim or claims from which it depends. Therefore, claim 12 distinguishes over Okabe for at least all of the reasons discussed above with regard to claim 1 in Section A.1.

Ground 3 does not rely on the supposed AAPA to overcome the deficiencies of Okabe with respect to claim 1, from which claim 12 depends. (See Pet. at 38-46.) Therefore, Petitioner fails to establish a reasonable likelihood that claim 12 is obvious over Okabe in view of Supposed AAPA.

PO reserves the right to present additional arguments for patentability of claim 12 should *inter partes* review be instituted.

C. Ground 4: Obviousness of Claims 2, 5, 6, and 9 Over Okabe in View of Supposed AAPA and Sutardja

Claims 2, 5, 6, and 9 depend from claim 1. A dependent claim contains all of the limitations of the claim or claims from which it depends. Therefore, claims 2, 5, 6 and 9 distinguish over Okabe for at least all of the reasons discussed above with regard to claim 1 in Section A.1.

Ground 4 does not rely on the supposed AAPA or Sutardja to overcome the deficiencies of Okabe with respect to claim 1, from which claims 2, 5, 6, and 9 depend. (See Pet. at 47-53.) Therefore, Petitioner fails to establish a reasonable likelihood that claims 2, 5, 6, and 9 are obvious over Okabe in view of Supposed AAPA and Sutardja.

PO reserves the right to present additional arguments for patentability of claims 2, 5, 6, and 9 over Okabe in view of supposed AAPA and Sutardja should *inter partes* review be instituted.

D. Ground 5: Obviousness of Claims 3, 4, and 7 Over Okabe in View of Supposed AAPA, Sutardja, and Taggart

Claims 3, 4, and 7 depend from claim 1. A dependent claim contains all of the limitations of the claim or claims from which it depends. Therefore, claims 3, 4, and 7 distinguish over Okabe for at least all of the reasons discussed above with regard to claim 1 in Section A.1.

Ground 5 does not rely on the supposed AAPA or Sutardja or Taggart to overcome the deficiencies of Okabe with respect to claim 1, from which claims 3, 4, and 7 depend. (See Pet. at 54-60.) Therefore, Petitioner fails to establish a reasonable likelihood that claims 3, 4, and 7 are obvious over Okabe in view of Supposed AAPA and Sutardja.

PO reserves the right to present additional arguments for patentability of claims 3, 4, and 7 over Okabe in view of supposed AAPA and Sutardja and Taggart should *inter partes* review be instituted.

E. Ground 6: Obviousness of Claims 8 and 11 Over Okabe in View of Supposed AAPA, Sutardja, and Choi

Claims 8 and 11 depend from claim 1. A dependent claim contains all of the limitations of the claim or claims from which it depends. Therefore, claims 8 and 11 distinguish over Okabe for at least all of the reasons discussed above with regard to claim 1 in Section A.1.

Ground 6 does not rely on the supposed AAPA or Sutardja or Choi to overcome the deficiencies of Okabe with respect to claim 1, from which claims 8 and 11 depend. (See Pet. at 60-63.) Therefore, Petitioner fails to establish a reasonable likelihood that claims 8 and 11 are obvious over Okabe in view of Supposed AAPA and Sutardja and Choi.

PO reserves the right to present additional arguments for patentability of

claims 8 and 11 over Okabe in view of supposed AAPA and Sutardja and Choi should *inter partes* review be instituted.

F. Ground 7: Obviousness of Claim 10 Over Okabe in View of Supposed AAPA, Sutardja, Choi, and Digital Design

Claim 10 depends from claim 1. A dependent claim contains all of the limitations of the claim or claims from which it depends. Therefore, claim 10 distinguishes over Okabe for at least all of the reasons discussed above with regard to claim 1 in Section A.1.

Ground 7 does not rely on the supposed AAPA, Sutardja, Choi, or Digital Design to overcome the deficiencies of Okabe with respect to claim 1, from which claim 10 depends. (*See* Pet. at 64-67.) Therefore, Petitioner fails to establish a reasonable likelihood that claim 10 is obvious over Okabe in view of Supposed AAPA.

PO reserves the right to present additional arguments for patentability of claim 10 should *inter partes* review be instituted.

G. Ground 8: Obviousness of Claim 13 Over Okabe in View of Supposed AAPA, Kramer, and Sutardja

Claim 13 depends from claim 1. A dependent claim contains all of the limitations of the claim or claims from which it depends. Therefore, claim 13 distinguishes over Okabe for at least all of the reasons discussed above with regard to claim 1 in Section A.1.

Ground 8 does not rely on the supposed AAPA, Kramer, or Sutardja to overcome the deficiencies of Okabe with respect to claim 1, from which claim 13 depends. (See Pet. at 68-73.) Therefore, Petitioner fails to establish a reasonable likelihood that claim 13 is obvious over Okabe in view of Supposed AAPA.

PO reserves the right to present additional arguments for patentability of claim 13 should *inter partes* review be instituted.

H. Ground 9: Obviousness of Claim 14 Over Okabe in View of Supposed AAPA, Conn, Kramer, and Sutardja

Claim 14 depends from claim 1. A dependent claim contains all of the limitations of the claim or claims from which it depends. Therefore, claim 14 distinguishes over Okabe for at least all of the reasons discussed above with regard to claim 1 in Section A.1.

Ground 9 does not rely on the supposed AAPA, Conn, Kramer, or Sutardja to overcome the deficiencies of Okabe with respect to claim 1, from which claim 14 depends. (See Pet. at 74-79.) Therefore, Petitioner fails to establish a reasonable likelihood that claim 14 is obvious over Okabe in view of Supposed AAPA.

PO reserves the right to present additional arguments for patentability of claim 14 should *inter partes* review be instituted.

VI. CONCLUSION

For at least the foregoing reasons, Petitioner has failed to meet its burden to show that it has a reasonable likelihood of success with respect to at least one claim. The Petition should be denied.

Dated: February 20, 2024

Respectfully submitted,

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Case IPR2024-00167
Patent No. 7,646,091
Patent Owner Preliminary Response

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITS

This Patent Owner Preliminary Response consists of 6,399 words, excluding cover page, table of contents, table of authorities, certificate of service, this certificate, or table of exhibits. The POPR complies with the type-volume limitation of 14,000 words as mandated in 37 C.F.R. §42.24. In preparing this certificate, counsel has relied on the word count of the word-processing system used to prepare the paper (Microsoft Word).

Dated: February 20, 2024

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on this 20th day of February, 2024, the foregoing document was served by electronic mail to the following attorneys of record:

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