

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP USA, INC.,
Petitioner,

v.

BELL SEMICONDUCTOR, LLC,
Patent Owner.

IPR2024-00167
Patent 7,646,091 B2

Before JEFFREY W. ABRAHAM, JOHN D. HAMANN, and
BRIAN D. RANGE, *Administrative Patent Judges*.

ABRAHAM, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

NXP USA, Inc. (“Petitioner”) filed a Petition for an *inter partes* review (Paper 1 (“Pet.”)) challenging claims 1–14 of U.S. Patent No. 7,646,091 B2 (Ex. 1001 (“the ’091 Patent”)). Bell Semiconductor, LLC (“Patent Owner”) filed a Preliminary Response. Paper 9 (“Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a). For the reasons set forth below, we do not institute an *inter partes* review of the challenged claims.

B. *Real Parties-in-Interest*

Petitioner identifies itself, NXP Semiconductors N.V., NXP B.V., and Freescale Semiconductor Holdings V, Inc. as real parties-in-interest. Pet. 1. Patent Owner identifies itself as the real party-in-interest in this proceeding, and indicates that Patent Owner is a wholly owned subsidiary of Hilco Patent Acquisition 56, LLC, which is owned by Hilco IP Merchant Capital, LLC, Hilco, Inc., Vulcan Ventures Inc., CDPQ Investments (U.S.) Inc., and KLIM AIV, LP. Paper 6, 1.

C. *Related Matters*

The parties identify the following proceeding involving the ’091 patent: *Bell Semiconductor, LLC v. NXP USA, Inc.*, No. 8:22-cv-02133-HDV-ADS (C.D. Cal. Nov. 23, 2022). Pet. 1; Paper 6, 1.

D. *The ’091 Patent (Ex. 1001)*

The ’091 patent is directed to semiconductor device packaging, and particularly “a method and apparatus for grounding high speed signals from a semiconductor device using an isolated ground plane.” Ex. 1001, 1:8–12. The ’091 patent explains that newer integrated circuits include both high

speed and lower speed systems, which can present a number of problems when both systems are connected to the same ground plane. Ex. 1001, 2:1–10. These problems may include excessive noise generated by the high speed circuitry that interferes with the operation of the low speed circuitry sharing the same ground plane, cross talk between signal and ground lines that are too closely spaced, and magnified “ground bounce.” Ex. 1001, 2:10–22.

To overcome the problems and insufficient solutions in the prior art, the ’091 patent discloses an integrated circuit package that includes a substrate with a first ground plane configured for electrical connection with low speed electronic circuitry, and a second ground plane configured for electrical connection with high speed electronic circuitry, in which the second ground plane is electrically isolated from the first ground plane. Ex. 1001, 2:49–58.

The ’091 patent states:

As used herein, high-speed circuitry refers to circuitry and electronic systems that operate at higher data rates or higher frequencies than ordinary “low-speed” circuitry. For example, circuitries operating at serial data rates higher than 1 Giga Bits per second (Gb/s) are considered high-speed circuitry. Also, this particularly the case for high-speed circuitry operating at serial data rates higher than 8.5 Gb/s and higher. For purposes of this patent circuitry operating at lower data rates and frequencies are considered non-high speed circuitry or also low-speed circuitry.

Ex. 1001, 4:15–24.

E. Illustrative Claim

Claim 1, the only independent claim challenged, is illustrative of the subject matter of the challenged claims and is reproduced below:

1. A semiconductor integrated circuit (IC) package which comprises:

a substrate having a first surface and a second surface wherein;

a first layer of the substrate includes,

a first ground plane enabling electrical connection with low speed electronic circuitry, and

a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection with high speed electronic circuitry;

a second layer of the substrate includes,

a third ground plane configured for electrical connection with low speed electronic circuitry, and

a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the fourth ground plane configured for electrical connection with high speed electronic circuitry;

a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate;

a plurality of additional electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate; and

peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package; and

at least one reference plane associated with each layer of the substrate and the ground planes included thereon.

Ex. 1001, 9:25–54; Ex. 1004, 243 (certificate of correction issued April 27, 2021, changing “the third ground plane configured for electrical” to “the fourth ground plane configured for electrical,” at column 9, line 41).

F. Asserted Unpatentability Challenges

Petitioner asserts that claims 1–14 are unpatentable based on the following challenges:

Claim(s) Challenged	35 U.S.C. §¹	Reference(s)
1	102	Okabe ²
1	103	Hashemi, ³ Okabe
1, 12	103	Okabe, Applicant’s Admitted Prior Art (AAPA)
2, 5, 6, 9	103	Okabe, AAPA, Sutardja ⁴
3, 4, 7	103	Okabe, AAPA, Sutardja, Taggart ⁵
8, 11	103	Okabe, AAPA, Sutardja, Choi ⁶
10	103	Okabe, AAPA, Sutardja, Choi, Digital Design ⁷
13	103	Okabe, AAPA, Sutardja, Kramer ⁸
14	103	Okabe, AAPA, Sutardja, Kramer, Conn ⁹

Petitioner relies on the declaration testimony of R. Jacob Baker, P.E., Ph.D. (Ex. 1002). Patent Owner relies on the declaration testimony of Joseph Bernstein, Ph.D. (Ex. 2001).

¹ The relevant sections of the Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, took effect on March 16, 2013. Because the ’091 patent has an effective filing date prior to the effective date of the applicable AIA amendments, the pre-AIA versions of §§ 102 and 103 apply. *See* Pet. 2–3.

² US 7,515,879 B2, issued Apr. 7, 2009 (Ex. 1005).

³ US 6,337,464 B1, issued Apr. 23, 2002 (Ex. 1006).

⁴ US 2007/0018292 A1, published Jan. 25, 2007 (Ex. 1012).

⁵ US 2006/0001180 A1, published Jan. 5, 2006 (Ex. 1009).

⁶ Choi et al., *Modeling an Analysis of Power Distribution Networks for Gigabit Applications*, IEEE TRANSACTIONS ON MOBILE COMPUTING, Vol. 2, No. 4, 299–313 (2003) (Ex. 1011).

II. ANALYSIS

A. Legal Standards

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016). The burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros. Inc., v. Union Oil Co.*, 814 F.2d 628, 631 (Fed. Cir. 1987); *see also Finisar Corp. v. DirecTV Grp., Inc.*, 523 F.3d 1323, 1334 (Fed. Cir. 2008) (to anticipate a patent claim under 35 U.S.C. § 102, “a single prior art reference must expressly or inherently disclose each claim limitation”). Moreover, “[b]ecause the hallmark of anticipation is prior invention, the prior art reference—in order to anticipate under 35 U.S.C. § 102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements ‘arranged as in the claim.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)).

Whether a reference anticipates is assessed from the perspective of one of ordinary skill in the art. *See Dayco Prods., Inc. v. Total Containment*,

⁷ Howard Johnson and Martin Graham, HIGH-SPEED DIGITAL DESIGN, A HANDBOOK OF BLACK MAGIC (1993) (Ex. 1010).

⁸ US 7,420,286 B2, issued Sept. 2, 2008 (Ex. 1007).

⁹ US 7,084,487 B1, issued Aug. 1, 2006 (Ex. 1013).

Inc., 329 F.3d 1358, 1368 (Fed. Cir. 2003) (“[T]he dispositive question regarding anticipation [i]s whether one skilled in the art would reasonably understand or infer from the [prior art reference’s] teaching’ that every claim element was disclosed in that single reference.” (alterations in original) (quoting *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991))). Additionally, “[u]nder the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claimed limitations, it anticipates.” *MEHL/Biophile Int’l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999) (citation omitted); *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349–50 (Fed. Cir. 2002).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and “the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art would have had a “bachelor’s degree in a field relating to the integrated circuit package manufacturing process like materials science, physics, electrical engineering, or other related subjects, and at least two to three years of experience with fabrication and packaging of integrated circuits.” Pet. 4 (citing Ex. 1002

¶ 20). Patent Owner adopts Petitioner’s definition only for purposes of the Preliminary Response. Prelim. Resp. 7.

In light of the record before us, and for purposes of this Decision, we adopt Petitioner’s proposal regarding the level of ordinary skill in the art.

C. Claim Construction

In an *inter partes* review, we construe claim terms according to the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–17 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b). Under *Phillips*, claim terms are afforded “their ordinary and customary meaning.” *Phillips*, 415 F.3d at 1312. “[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Id.* at 1313. “Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.” *Id.*

Petitioner contends that we do not need to expressly construe any claim terms for purposes of this Decision. Pet. 22. Patent Owner likewise presents no express construction of any claim term. Prelim. Resp. 8.

After considering the arguments and information presented in the Petition, we determine that it is not necessary to construe any terms for purposes of this Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”)).

D. Grounds based on Okabe

Petitioner contends that Okabe anticipates claim 1, and that claims 1–14 are unpatentable under 35 U.S.C. § 103 as obvious over Okabe in view of one or more of AAPA, Sutardja, Taggart, Choi, Digital Design, Kramer, and Conn. Pet. 22–30, 38–79. Patent Owner disputes Petitioner’s arguments and evidence. Prelim. Resp. 8–21, 25–30.

1. Okabe (Ex. 1005)

Okabe is a U.S. Patent titled “Radio Frequency Circuit Module.” Ex. 1005, code (54). Okabe relates to a radio frequency (RF) circuit module that is employed in wireless equipment, particularly “[a]n RF circuit module, in which a power amplifier and a transceiver are united, with reduced interference between its electronic circuit blocks, downsized and still having high performance.” Ex. 1005, 1:12–16, code (57). Okabe depicts one embodiment of its RF module in Figure 2, reproduced below.

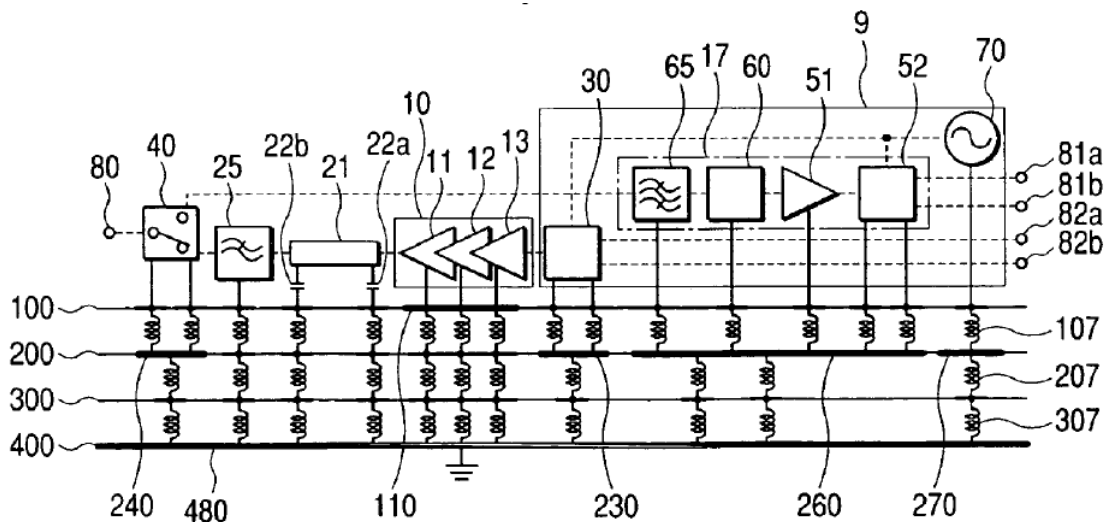


Figure 2 shows the circuit arrangement of RF module 1, including transceiver 9, comprised of transmitter 30 and receive circuit 17, and power amplifier 10. Ex. 1005, 6:43–49, 6:57–60. Receive circuit 17 comprises receiving band pass filter (“BPF”) 65, receiving matching network 60, low noise amplifier (“LNA”) 51, and receiver 52. Ex. 1005, 1:61–65, 6:53–57. Power amplifier 10 is a three-stage power amplifier consisting of last-stage amplifier 11, middle-stage amplifier 12, and first-stage amplifier 13. Ex. 1005, 7:52–55. Figure 2 also shows transmission line 21 and capacitors 22a and 22b, which comprise output matching network 20 (not labeled in Figure 2). Ex. 1005, 8:62–63. Okabe’s RF Module 1 also includes switch circuit 40, low pass filter (“LPF”) 25, and voltage control oscillator (“VCO”) 70. Ex. 1005, 1:56–63, 6:61–67. Additionally, Figure 2 depicts first conductor layer 100 containing ground plane 110, second conductor layer 200 containing ground planes 230, 240, 260, and 270, third conductor layer 300, and fourth conductor layer 400 containing common ground plane 480, as well as via-holes 107, 207, and 307. Ex. 1005, 8:18–44. Okabe explains that the circuits are grounded to separate ground planes, and eventually connected to a common ground plane. Ex. 1005, 7:61–63.

According to Okabe, by isolating the various ground planes, the embodiment depicted in Figure 2 is able to (1) prevent the feedback of a current flowing across the common ground plane 480, (2) effectively prevent a decrease in the receiving sensitivity and malfunction of LNA 51, (3) maintain a higher performance of receive circuit 17 by isolation between the antenna duplex circuit ground plane 240 and the receive circuit ground plane 260, (4) prevent a feedback current flowing into the receive circuit ground plane 260 as the result of heat and output current from the transmitter 30, thus maintaining a higher performance of the receive circuit 17,

(5) prevent the feedback of a current flowing across ground plane 110 and common ground plane 480, (6) prevent oscillation of power amplifier 10 and a decrease in the quality of local oscillation signals that VCO 70 outputs, (7) prevent the deterioration of receiving sensitivity of a desired receive signal, and (8) minimize transmission loss due to conductor loss. Ex. 1005, 10:20–11:6.

Figure 1 of Okabe, reproduced below, shows a different perspective of RF module 1 and includes additional components.

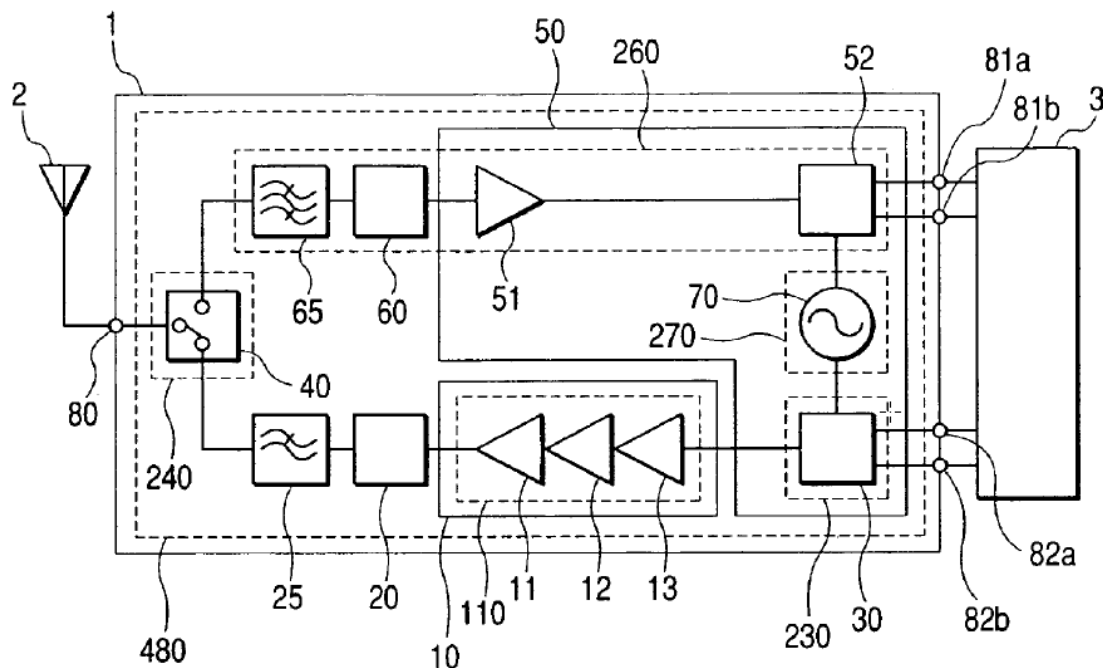


Figure 1 shows RF module 1 (including the components having the same reference numbers used in Figure 2) connected to base band large scale integrated circuit (“BB-LSI”) 3 and external antenna 2. Ex. 1005, 2:3–5, 7:4–17. Okabe explains that BB-LSI 3 outputs a transmit signal, which is received by transmitter 30 through input terminals 82a and 82b. Ex. 1005, 6:4–8. Transmitter 30 converts the frequency of the transmit signal and

outputs the converted signal to power amplifier 10, which amplifies the power level of the RF transmit signal. Ex. 1005, 7:4–13. An RF receive signal may be transmitted from antenna 2, via antenna terminal 80, to the reception chain comprised of BPF 65, which removes unwanted interference noise, LNA 51, which amplifies the power level of the receive signal, and receiver 52, which converts the frequency of the RF receive signal and supplies the receive signal to BB-LSI 3 through output terminals 81a and 81b. Ex. 1005, 7:15–35.

Okabe further explains that in the embodiment shown in Figures 1 and 2, the transmit signal output from the BB-LSI and the receive signal input to the BB-LSI are in a frequency band of about 200 kHz, and the RF transmit signal output from transmitter 30 and RF receive signal input to receiver 52 are in a frequency band of 900 MHz. Ex. 1005, 7:36–41.

2. Analysis

a. Independent claim 1

Petitioner contends that Okabe anticipates claim 1, and that claim 1 is unpatentable under 35 U.S.C. § 103 as obvious over Okabe in combination with Applicant's Admitted Prior Art. Pet. 22–30, 38–43.

Independent claim 1 recites a semiconductor integrated circuit package with a first layer that includes “a first ground plane enabling electrical connection with low speed electronic circuitry” and a “second ground plane enabling electrical connection with high speed electronic circuitry.” Ex. 1001, 9:25–36. Petitioner provides an annotated version of Figure 14, reproduced below, to identify the components of Okabe that purportedly satisfy these claim limitations. Pet. 25.

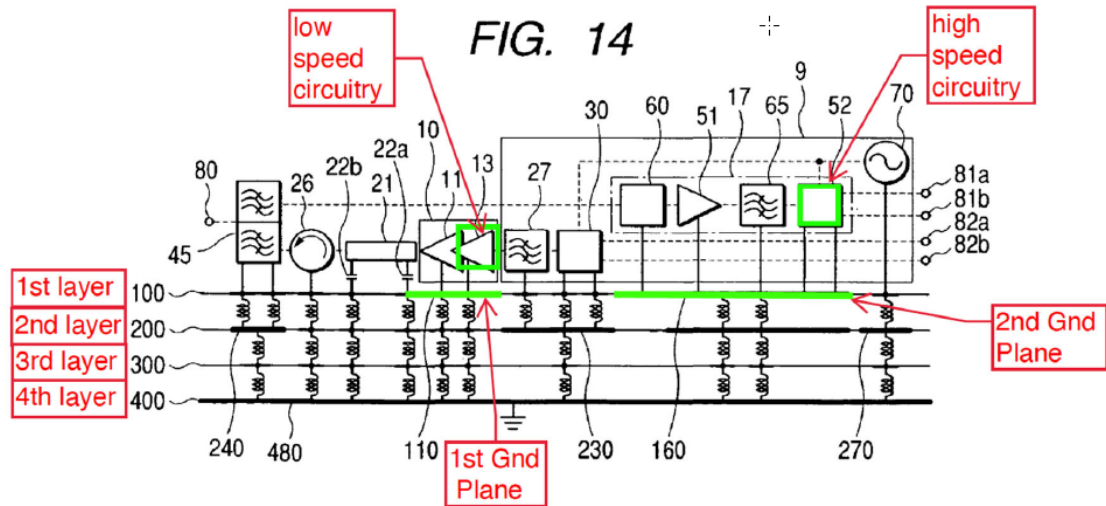


Figure 14, similar to Figure 2 of Okabe shown above, shows the circuit arrangement of one embodiment of an RF module, including transceiver 9, comprised of transmitter 30 and receive circuit 17, and power amplifier 10. Petitioner has highlighted in green the component corresponding to reference number 13 (Petitioner’s “circuit 13”), and identifies it with the label “low speed circuitry.” Pet. 25. Petitioner has also highlighted the component corresponding to reference number 52 in green (Petitioner’s “circuit 52”), and added a corresponding label of “high speed circuitry.” Pet. 25.

Petitioner asserts that Okabe teaches “circuit 13 operates in a frequency band of 200 kilohertz (kHz), while circuit 52 operates in a frequency band of 900 megahertz (MHz).” Pet. 24 (citing Ex. 1005, 7:36–41); *see also* Pet. 24 (providing another annotated version of Figure 14 that identifies the component corresponding to reference number 13 as operating at 200 kHz and the component corresponding to reference number 52 as operating at 900 MHz). Petitioner contends that based on these frequencies, a person of ordinary skill in the art would have understood circuit 13

constitutes low speed electronic circuitry and circuit 52 constitutes high speed electronic circuitry, as recited in claim 1. Pet. 24–25.

Patent Owner contends that Petitioner’s arguments are based on a typographical error in Okabe that undermines Petitioner’s argument that Okabe discloses the “low speed” and “high speed” circuitry limitations. Prelim. Resp. 12–13. Specifically, Patent Owner asserts that what Petitioner identifies as “circuit 13” in Figure 14 is first-stage amplifier 13, not “the BB-LSI 13” discussed in column 7, lines 36–41, which Petitioner relies upon to satisfy the “low speed electronic circuitry” limitation in claim 1. Prelim. Resp. 13. Patent Owner further contends that first-stage amplifier 13 is a high speed electronic circuit under Petitioner’s criteria, and, therefore, the components Petitioner identifies in Okabe do not meet the “low speed” and “high speed” circuitry limitations in claim 1. Prelim. Resp. 13 (citing Ex. 2001 ¶ 71).

We agree with Patent Owner that what Petitioner identifies as “circuit 13” in Figure 14 is first-stage amplifier 13, and not a BB-LSI. It is clear from Figure 14 itself that the component Petitioner identifies as “circuit 13” is part of power amplifier 10. Ex. 1005, Fig. 14; *see also* Ex. 1005, Fig. 13 (showing first-stage amplifier 13 as part of power amplifier 10); Prelim. Resp. 16–18 (providing annotated versions of Okabe Figures 1, 2, 13, and 14 showing first-stage amplifier 13 as part of power amplifier 10, and separate from BB-LSI 3). Consistent with this depiction in the figures, Okabe describes “first-stage amplifier 13” as part of power amplifier 10 in the specification. Ex. 1005, 7:53–55, 13:58–61. We do not discern, nor does Petitioner direct us to, any disclosure in Okabe that power amplifier 10 includes a BB-LSI.

Furthermore, Okabe states that power amplifier 10 “amplifies the power level of an RF transmit signal . . . output from the transmitter 30” and that the RF transmit signal output from the transmitter 30 is “in a frequency band of 900 MHz.” Ex. 1005, 7:10–12, 7:38–41. Thus, Petitioner’s “circuit 13,” i.e., first-stage amplifier 13, which is part of power amplifier 10, operates in a frequency band of 900 MHz, not 200 kHz, as Petitioner asserts.

Okabe also states that the RF receive signal input to receiver 52 is “in a frequency band of 900 MHz.” Ex. 1005, 7:38–41. Therefore, according to Okabe, the two components Petitioner identifies in annotated Figure 14, circuit 13 and receiver 52, operate in the same frequency band. As a result, one cannot be “high speed” circuitry while the other is “low speed” circuitry. Ex. 1005, 7:10–12, 7:38–41; Prelim. Resp. 17; Ex. 2001 ¶ 75.

We recognize that Okabe states “the transmit signal which is output from the BB-LSI 13 and the receive signal which is input to the BB-LSI 13 are in a frequency band of about 200 kHz.” Ex. 1005, 7:36–38. This language, however, does not demonstrate that the component Petitioner identifies as “circuit 13” in Figure 14 operates at this frequency. Moreover, Patent Owner offers evidence suggesting “BB-LSI 13” is a typographical error in Okabe. For example, Patent Owner and Dr. Bernstein direct us to the previous paragraph of Okabe’s specification, where Okabe refers to BB-LSI 3, and describes how BB-LSI 3 outputs an RF transmit signal to transmitter 30 and receives an RF receive signal from receiver 52. Ex. 1005, 7:4–35; Prelim. Resp. 12–15; Ex. 2001 ¶¶ 71–73. This is consistent with Okabe’s description of the input and output of “BB-LSI 13” at column 7, lines 36–38, which refers to “the transmit signal which is output from the BB-LSI” and “the receive signal which is input to the BB-LSI.” Thus, it

appears that Okabe mistakenly refers to BB-LSI 13 instead of BB-LSI 3 in lines 36–38 of column 7.

But even if Okabe’s reference to BB-LSI 13 is not a typographical error, the evidence of record suggests a person of ordinary skill in the art would not have considered what Petitioner identifies as “circuit 13” in annotated Figure 14 to be the BB-LSI 13 described in the specification because the “receive signal” is not “input” into the component corresponding to reference number 13 in Figure 14. Instead, the component corresponding to reference number 13 only receives and amplifies the transmit signal that is output from transmitter 30. Ex. 1005, 7:10–12, Figs. 13, 14. Therefore, what Petitioner identifies as “circuit 13” in Okabe Figure 14 does not match the description of “the BB-LSI 13” in the specification, and would not operate in a frequency band of 200 kHz.

For all of the foregoing reasons, Petitioner has failed to demonstrate sufficiently that Okabe discloses a semiconductor integrated circuit package with a first layer that includes “a first ground plane enabling electrical connection with low speed electronic circuitry” and a “second ground plane enabling electrical connection with high speed electronic circuitry.” Ex. 1001, 9:25–36.

Claim 1 also requires a second layer that includes a “third ground plane configured for electrical connection with low speed electronic circuitry” and a “fourth ground plane configured for electrical connection with high speed electronic circuitry.” Ex. 1001, 9:37–43. For these limitations, Petitioner directs us to duplexer 45, connected to third ground plane 240, and VCO 70, connected to fourth ground plane 270, both in second layer 200. Pet. 26–27 (citing Ex. 1005, 8:27–35, 14:13–33; Ex. 1002 ¶¶ 71–73). Petitioner argues that a person of ordinary skill in the art “would

understand that duplexer 45 could operate at a lower speed than VCO 70” and that “VCO 70 would be capable of operating at a higher frequency than duplexer 45.” Pet. 26–27. Based on this, Petitioner contends that duplexer 45 constitutes “low speed electronic circuitry” and VCO 70 constitutes “high speed electronic circuitry” as required in claim 1. Pet. 26–27.

Petitioner’s arguments are not persuasive. As Patent Owner and Dr. Bernstein point out, Petitioner does not specify the frequencies at which duplexer 45 and VCO 70 operate in Okabe. Prelim. Resp. 20; Ex. 2001 ¶ 79. Nor does Petitioner direct us to any criteria for classifying circuitry as “high speed” or “low speed.” Prelim. Resp. 20; Ex. 2001 ¶ 79. As a result, we are left with only the assertion of what a person of ordinary skill in the art would have understood about duplexer 45 and VCO 70. To support this assertion, Petitioner directs us to statements in Dr. Baker’s declaration that mirror the Petition. Pet. 26–27 (citing Ex. 1002 ¶¶ 71–73). Dr. Baker, however, does not cite to any supporting evidence or provide any technical reasoning to support his statements. Ex. 1002 ¶¶ 71–73. “Thus, the cited declaration testimony is conclusory and unsupported, adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight.” *Xerox Corp. v. Bytemark Inc.*, IPR2022-00624, Paper 9 at 15 (August 24, 2022) (precedential); *see also* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”). Accordingly, Petitioner has failed to demonstrate sufficiently that Okabe discloses a second layer that includes a “third ground plane configured for electrical connection with low speed electronic circuitry” and a “fourth ground plane configured for electrical connection with high speed electronic circuitry.” Ex. 1001, 9:37–43.

For all of these reasons, we determine that Petitioner has failed to demonstrate sufficiently that Okabe discloses all of the limitations of claim 1. As a result, Petitioner has failed to establish a reasonable likelihood that it would prevail in showing that Okabe anticipates claim 1.

For Petitioner's challenge that claim 1 is unpatentable as obvious over Okabe in combination with Applicant's Admitted Prior Art (AAPA), Petitioner relies solely on Okabe as teaching a first layer that includes a "second ground plane enabling electrical connection with high speed electronic circuitry," and a second layer that includes a "third ground plane configured for electrical connection with low speed electronic circuitry" and a "fourth ground plane configured for electrical connection with high speed electronic circuitry." Pet. 39; Ex. 1001, 9:25–43. Nothing in Petitioner's analysis of AAPA cures the deficiencies discussed above regarding Okabe.

Therefore, for the same reasons discussed above, Petitioner has failed to demonstrate that the combination of Okabe and AAPA discloses or suggests all of the limitations in claim 1. Accordingly, Petitioner has failed to establish a reasonable likelihood that it would prevail in showing that claim 1 would have been unpatentable as obvious in view of Okabe and AAPA.

b. Dependent claims 2–14

Claims 2–14 depend, directly or indirectly, from claim 1. Ex. 1001, 9:55–12:24. For its challenges of these claims, Petitioner relies on the arguments regarding Okabe and AAPA presented for independent claim 1. *See, e.g.*, Pet. 47 (stating, "[t]he Okabe-AAPA combination teaches an IC package with peripheral electrical contacts for electrical connection with low speed and high speed circuitry. (*See supra* Section IX.C.1(a-f) regarding claim 1)"). Nothing in Petitioner's analysis of the additional references

relied upon for its challenges of the dependent claims cures the deficiencies discussed above regarding the Okabe-AAPA combination. Therefore, for the same reasons discussed above for independent claim 1, we determine Petitioner has failed to establish a reasonable likelihood of prevailing on its challenges that claims 2–14 are unpatentable as obvious in view of Okabe in combination with one or more of AAPA, Sutardja, Taggart, Choi, Digital Design, Kramer and Conn.

3. Summary

Having reviewed the record, we determine that Petitioner has failed to establish a reasonable likelihood of prevailing on its challenges that Okabe anticipates claim 1 or that claims 1–14 are unpatentable as obvious in view of Okabe in combination with one or more of AAPA, Sutardja, Taggart, Choi, Digital Design, Kramer and Conn.

E. Grounds based on Hashemi

Petitioner contends claim 1 is unpatentable as obvious in view of Hashemi and Okabe. Pet. 31–37. Patent Owner disputes Petitioner’s arguments and evidence. Prelim. Resp. 21–25.

1. Hashemi (Ex. 1006)

Hashemi is a U.S. Patent titled “Multiple Chip Module with Integrated RF Capabilities.” Ex. 1006, code (54). Hashemi is directed to “[a] multiple chip module (MCM) for use with baseband, RF, or IF applications [that] includes a number of active circuit chips having a plurality of different functions.” Ex. 1006, code (57). Hashemi teaches that the MCM “may incorporate split ground planes to achieve electronic shielding and isolation.” Ex. 1006, code (57).

2. Analysis

As discussed above, independent claim 1 recites a semiconductor integrated circuit package with a first layer that includes “a first ground plane enabling electrical connection with low speed electronic circuitry” and a “second ground plane enabling electrical connection with high speed electronic circuitry.” Ex. 1001, 9:25–36. For these limitations, Petitioner argues that Hashemi discloses first active chip 104 connected to ground plane 122, and second active chip 104 connected to second ground plane 124. Pet. 32–33. According to Petitioner, Hashemi discloses that “the first circuit chip 104 operates at different frequencies than a second circuit chip 104. Pet 32 (citing Ex. 1006, claim 3; Ex. 1002 ¶ 84). Petitioner asserts that a person of ordinary skill in the art “would have understood the first circuit chip 104 operating at lower frequencies would be ‘low speed electronic circuitry’.” Pet. 33 (citing Ex. 1002 ¶ 84). Petitioner relies on similar reasoning in asserting the second active chip would be “high speed electronic circuitry.” Pet. 33 (citing Ex. 1002 ¶ 86).

Patent Owner argues that “apart from noting that the first and second circuit chips 104 may operate at different frequencies, Petitioner fails to provide any criteria for classifying circuitry as low speed or high speed,” and that Petitioner fails to provide any evidence to support its conclusory statement that the first circuit chip 104 meets the “low speed circuitry” limitation and that the second circuit chip 104 meets the “high speed circuitry” limitation. Prelim. Resp. 22–23 (citing Ex. 2001 ¶ 84).

We agree with Patent Owner, and are not persuaded by Petitioner’s arguments. Petitioner directs us to claim 3 of Hashemi, which states that its “first and second RF/IF active circuit chips are configured to operate at different RF/IF frequencies.” Ex. 1006, 14:6–8 (claim 3). Petitioner,

however, does not direct us to any evidence demonstrating the frequencies at which these chips operate, or provide any indication of what constitutes “low speed” and “high speed” circuitry. *See* Pet. 32–33. The fact that two chips may operate at different speeds, without more, is insufficient to establish that one chip constitutes “low speed electronic circuitry” and the other constitutes “high speed electronic circuitry” in the context of claim 1. Furthermore, Dr. Baker’s declaration testimony that Petitioner cites is conclusory and unsupported, and is entitled to little or no weight. *See Xerox*, IPR2022-00624, Paper 9 at 15; 37 C.F.R. § 42.65(a).

Accordingly, Petitioner has failed to demonstrate sufficiently on this record that Hashemi discloses or suggests a semiconductor integrated circuit package with a first layer that includes “a first ground plane enabling electrical connection with low speed electronic circuitry” and a “second ground plane enabling electrical connection with high speed electronic circuitry.” Ex. 1001, 9:25–36. Petitioner’s assertion that Hashemi discloses a semiconductor integrated circuit package with a second layer that includes a “third ground plane configured for electrical connection with low speed electronic circuitry” and a “fourth ground plane configured for electrical connection with high speed electronic circuitry” suffers from the same deficiencies. Pet. 33–35; Ex. 1001, 9:37–43.

4. Summary

Having reviewed the record, we determine that Petitioner has failed to establish a reasonable likelihood of prevailing on its challenge that claim 1 is unpatentable as obvious in view of Hashemi in combination with Okabe.

III. CONCLUSION

Upon consideration of the Petition, the Preliminary Response, and the evidence presented, we determine that Petitioner has not demonstrated a reasonable likelihood that it will prevail in showing that at least one of the challenged claims is unpatentable. Accordingly, we do not institute an *inter partes* review of any challenged claim based on any ground asserted in the Petition.

IV. ORDER

For the reasons given, it is:

ORDERED that, pursuant to 35 U.S.C. § 314, the Petition is denied, and no *inter partes* review is instituted.

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Patent 7,646,091 B2

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