

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP USA, INC.

Petitioner

v.

BELL SEMICONDUCTOR, LLC

Patent Owner

Patent No. 7,345,245

**DECLARATION OF R. JACOB BAKER, P.E., PH.D. IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,345,245**

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I, R. Jacob Baker, Ph.D., P.E. declare as follows:

I. INTRODUCTION

1. I have been retained by NXP USA, Inc. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 7,345,245 (“the ’245 patent”) (Ex. 1001).¹ I have been asked to consider whether certain references discloses or suggests the features recited in claims 1-12 of the ’245 patent. My opinions are set forth below.

2. I am being compensated at a rate of \$765/hour for my work in this proceeding. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

II. BACKGROUND AND QUALIFICATIONS

3. I am an independent consultant and all of my opinions stated in this declaration are based on my own personal knowledge and my own professional judgment. In forming these opinions, I have relied on my knowledge and experience

¹ Where appropriate, I refer to exhibits that I understand are to be attached to the petition for Inter Partes Review of the ’245 patent.

in designing, developing, and fabricating integrated circuit packages, including multilayer substrates and signal routing within integrated circuit packaging.

4. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. I'm told a copy of my current curriculum vitae, which details my education and professional and academic experience, will be submitted as an Exhibit. However, the following provides an overview of some of my experience that is relevant to the matters set forth in this declaration.

5. I presently serve as a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). In forming my opinions, I have relied on my knowledge and experience in designing, developing, and researching integrated circuit packaging and my knowledge of electrical circuit design and fabrication and electrical engineering fundamentals. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person having ordinary skill in the art.

6. I have been teaching electrical engineering at UNLV since 2012. Prior to this position, I was a Professor of Electrical and Computer Engineering at Boise State University from 2000. Prior to my position at Boise State University, I was an Associate Professor of Electrical Engineering between 1998 and 2000 and

Assistance Professor of Electrical Engineering between 1993 and 1998 at the University of Idaho. I have been teaching electrical engineering since 1991.

7. I received a Bachelor of Science and Master of Science degrees in Electrical Engineering from UNLV, in 1986 and 1988, respectively. In 1993, I also received a Ph.D. in Electrical Engineering from the University of Nevada, Reno. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada Test Site. During this time, I designed, and oversaw the fabrication and manufacture of over 30 electronic and electronic-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics.

8. From 1997 to 1999, I served as a Consultant for Tower Semiconductor, in the design of CMOS integrated circuit cells for various modem chips, interfaces, and serial buses, including charging circuits based upon power up-down circuits using an MOS or bandgap reference, pre-amplifiers, and comparators. I was also a Senior Designer at Micron Technology from 1994 to 2008, working on the development of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, CMOS Image Sensors (CISs), and power supply design. My

more recent industry experience includes working with Freedom Photonics on the integration, fabrication, and design of optoelectronics with CMOS integrated circuits, including the design of compact optical transceiver for range finding applications, Geiger mode SiGe receiver for long-range communications, and packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies. I have worked as a consultant at other companies designing electronic circuits, including Sun, Oracle, Contour Semiconductor, Lockheed-Martin, and OmniVision.

9. I have taught courses in integrated circuit design (analog, digital, mixed signal, memory circuit design, etc.), linear circuits, microelectronics, communication systems, power electronics, and fiber optics. I have been the main advisor to over 100 Master's and Doctoral students.

10. I am the author of several books covering the area of integrated circuit design including: DRAM Circuit Design: Fundamental and High-Speed Topics (two editions), CMOS Circuit Design, Layout, and Simulation (four editions), and CMOS Mixed-Signal Circuit Design (two editions). I have also authored, or coauthored, more than 100 papers and presentations in the areas of electronic circuit design. I am the named inventor on over 150 granted U.S. patents.

11. I have received numerous awards for my work, including the Frederick Emmons Terman (the "Father of Silicon Valley") Award. The Terman Award is

bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession.

12. I am a Fellow of the IEEE for contributions to memory circuit design. I have also received the IEEE Circuits and Systems Education Award (2011).

13. I have received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001), all from Boise State University.

14. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor award four of the years I have been at UNLV.

15. My curriculum vitae, which includes a more detailed summary of my background, experience, patents, designs, and publications, is Exhibit 1003.

16. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

III. MATERIALS REVIEWED

17. The opinions in this Declaration are based on the documents I reviewed, my knowledge, experience, and professional judgment. In forming my opinions expressed in this Declaration, while drawing on my knowledge and experience in designing, developing, and researching integrated circuit packages, I reviewed the following materials: U.S. Patent No. 7,345,245 (the '245 patent) (Ex. 1001); the file

history of the '245 patent (Ex. 1004); U.S. Patent Pub. No. 2003/0183919 to Devnani et al ("Devnani") (Ex. 1005); U.S. Patent Pub. No. 2003/0003705 to Chung et al ("Chung") (Ex. 1006); U.S. Patent No. 6,680,530 to Pillai et al ("Pillai") (Ex. 1007); Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages Datasheet (April 2003) ("Celeron") (Ex. 1008); U.S. Patent No. 6,172,305 to Tanahashi ("Tanahashi") (Ex. 1009); Thomas D. Moore and John L. Jarvis, The effects of in-plane orthotropic properties in a multi-chip ball grid array assembly, Microelectronics Reliability, Volume 42, Issue 6, June 2002, pages 943-949 ("Moore & Jarvis") (Ex. 1010); D.J. Xie and Z.P. Wang, Process capability study and thermal fatigue life prediction of ceramic BGA solder joints, Finite Elements in Analysis and Design, Volume 30, Issues 1-2, July 15, 1998, pages 31-45 ("Xie and Wang") (Ex. 1011); Critical Review and Technology Assessments '91-'92, Reliability Analysis Center, AD-A278 419; April 21, 1994, 452 pages ("CRTA") (Ex. 1016); 2000 Packaging Handbook, Chapter 4: Performance Characteristics of IC Packages; pages 1-66, 2000 ("PCIP") (Ex. 1017); A Review of Ball Grid Arrays For Electronic Assembly, S B Dunkerton and J M Goward, Presented at ICAWT '98, The 1998 International Conference on Advances in Welding Technology - 'Joining applications in electronics and medical devices', Columbus, Ohio, USA, 30 September - 2 October 1998 ("Review of BGAs") (Ex. 1018), and any other materials I refer to in this declaration in support of my opinions.

18. All of the opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my appreciation of how a person of ordinary skill in the art would have understood the claims and the specification of the '245 patent at the time of the alleged invention, which I have been asked to initially consider as the early 2000s (including October 8, 2003, the filing date of the '245 patent, which I understand is the earliest possible priority date for the '245 patent). My opinions reflect how one of ordinary skill in the art would have understood the '245 patent, the prior art to the patent, and the state of the art at the time of the alleged invention.

19. Based on my experience and expertise, it is my opinion that certain prior art references disclose or suggest all the features recited in claims 1-12 of the '245 patent, as I discuss in detail below.

IV. LEVEL OF ORDINARY SKILL IN THE ART

20. I am familiar with the level of ordinary skill in the art with respect to the alleged inventions of the '245 patent as of what I understand is the earliest possible priority date of October 8, 2003. Specifically, based on my review of the '245 patent, the technology, the educational level and experience of active workers in the field, the types of problems faced by workers in the field, the solutions found to those problems, the sophistication of the technology in the field, and drawing on my own experience, I believe a person of ordinary skill in the art would have had a

bachelor's degree in a field relating to the semiconductor manufacturing process like materials science, physics, electrical engineering, or other related subjects, and at least two to three years of experience with fabrication and packaging of integrated circuits. More education can supplement practical experience and vice versa. Depending on the engineering background and level of education of a person, it would have taken a few years for the person to become familiar with the problems encountered in the art and to become familiar with the prior and current solutions to those problems.

21. All of my opinions in this declaration are from the perspective of one of ordinary skill in the art, as I have defined it here, during the relevant timeframe (i.e., prior to October 2003).

V. TECHNICAL BACKGROUND

22. In this section, I discuss the state of the art relevant to the subject matter of the '245 patent, as would have been known, understood, and appreciated by a person of ordinary skill in the art (POSITA) at the time of the alleged invention of the '245 patent. In particular, a person of ordinary skill in the art would have been aware of various developments for various types of integrated circuit (IC) packages including layers of a substrate, traces on one of the layers for routing the signals thereon, and placement of the traces away from high stress areas, as I discuss below.

23. The various types of IC packages include flip-chip, leadframe, leadless leadframe, ball grid array (BGA), etc. IC packages typically include multiple layers having conductors separated by insulating layers. The conductor layers include power layer(s), ground layer(s), and signal routing layers. Conductive vias intercouple the power layer(s), ground layer(s), and signal routing layers. These multiple layers and vias of the IC package intercouple an IC die with a PCB. With a BGA package, a top layer has solder pads that intercouple the IC package to the IC die via first solder balls and a bottom layer that has solder pads that intercouple the IC package to the PCB via second solder balls.

24. Generally, IC packages are comprised of various materials attached together in a variety of ways. The coefficient of thermal expansion (CTE) for each of the materials is generally different, and this mismatch leads to various stress in the IC package. Thus, an IC package designer would have known that various sizes, orientations, layouts, etc. of the components of the IC package must be considered with respect to each CTE of the materials such that the stresses will not degrade or destroy the functionality of the IC package.

25. A person of ordinary skill in the art would have understood that stress from CTE would be greatest near the corner of an IC die, and thus would take this into account when designing the IC package. This was well known years prior to

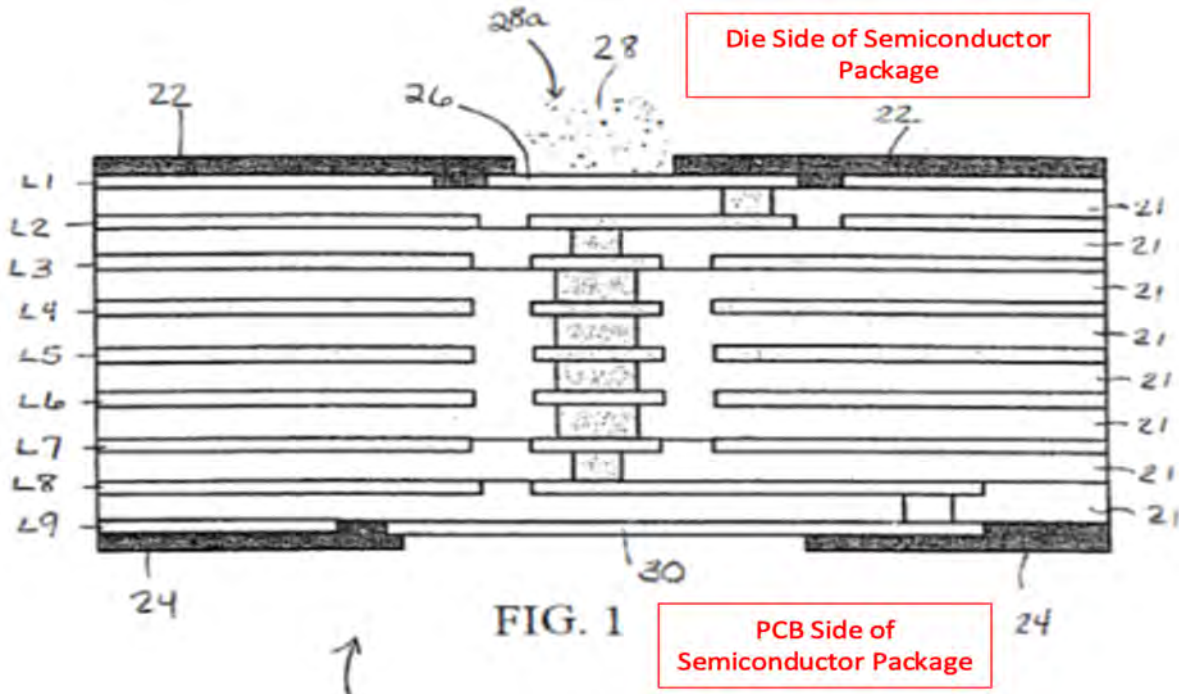
the date of the alleged inventions as further indicated by the prior art references I details below.

VI. THE '245 PATENT

26. The '245 patent is entitled “Robust High Density Substrate Design For Thermal Cycling Reliability.” (Ex. 1001, Title.) The '245 patent discloses a semiconductor package upon which an IC die (die) mounts and which may be mounted upon a Printed Circuit Board (PCB). The semiconductor package purports to provide improved thermal cycling reliability by routing signal traces away from high stress areas defined by corners of an attached die. (*Id.*, Abstract) More specifically, “Signal traces are routed away from the high stress area and in particular signal traces are routed away from the ball pads associated with the high stress to eliminate the cracks in the routed traces.” (*Id.*, Abstract).

27. The '245 patent includes substantial discussion of prior art to which features of the '245 patent are directed (Applicant's admitted prior art (“AAPA”)). For example, AAPA of the '245 patent includes Figures 1, 2 and 3 and the detailed description from column 1, line 7 to column 2, line 22. (Ex. 1001, 1:7 – 2:22) The '245 patent's detailed description for the purported invention includes Figures 4 and 5 and the detailed description from column 3, line 6 to column 4, line 3. (Ex. 1001, 3:6 – 4:3) Note that I have annotated each of the Figures 1-5 of the '245 patent to assist in understanding the disclosed features. Further note that none of annotations

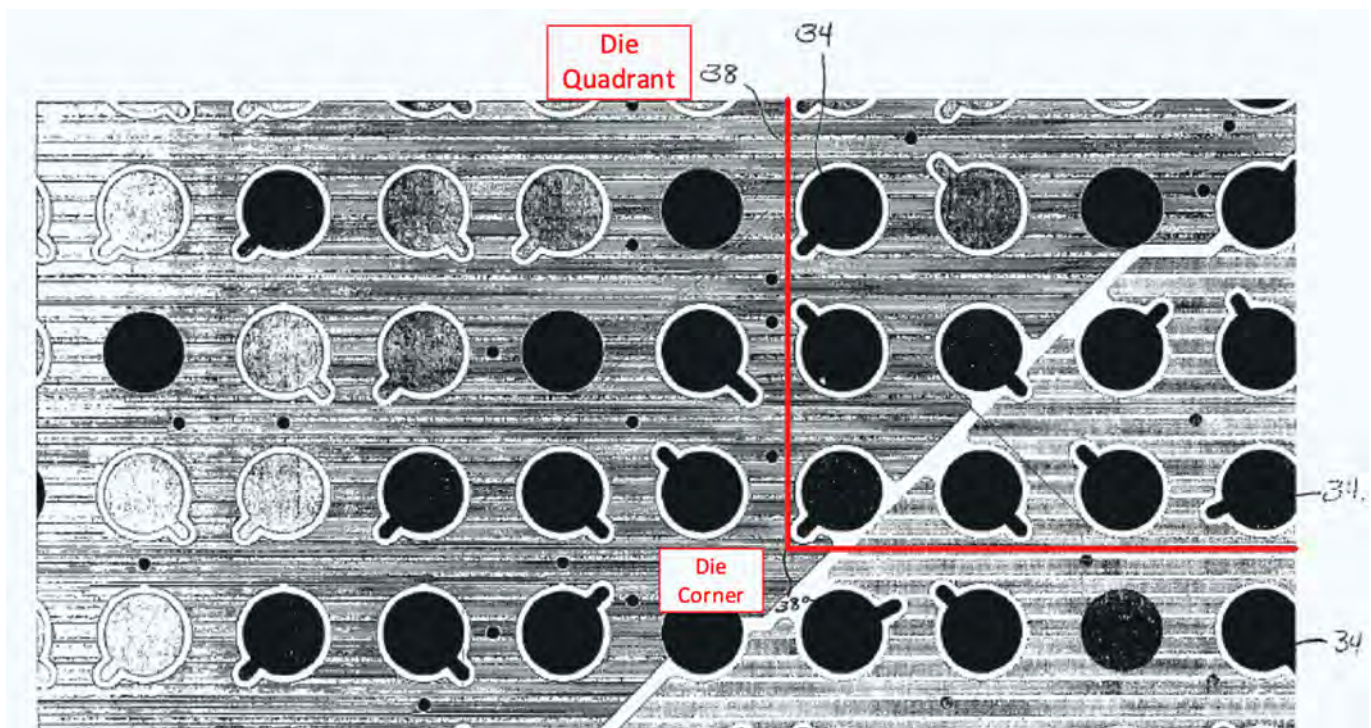
of Figures 1-5 are drawn to scale and that any annotations made thereto are based upon '245 patent related description.



(Ex. 1001, Fig. 1001 annotated)

28. As shown above, Figure 1 of the '245 patent illustrates (a portion of) a prior art (AAPA) semiconductor package with 9-layer stackup. (*Id.*, 50-51) “As an example, FIG. 1 shows a typical multi-layer organic BGA flip chip substrate that uses a 9-layer stackup 20 with a thin core. The 9-layer stackup 20 includes a layer L1, a layer L2, a layer L3, a layer L4, a layer L5, a layer L6, a layer L7, a layer L8, and a layer L9. Each of the layers is formed of a conductive material such as copper. Insulative material 21 is provided between each of the conductive layers” (*Id.* 1:26-35)

29. The '245 patent further discloses as AAPA that "Layer L1 provides a plurality of bump pads 26 (one of which is shown) on which a plurality of solder masses 28 (one of which is shown) are provided. The upper surfaces 28a of the solder masses 28 provide a die site on which the die (not shown) will be placed. A plurality of ball pads 30 (one of which is shown) are provided on Layer L9." (*Id.*, Fig. 1; 1:36-41). A person of ordinary skill in the art would understand that the plurality of ball pads 30 on Layer L9 would provide interconnection between the 9-layer stackup and a printed circuit board (PCB) via solder balls.

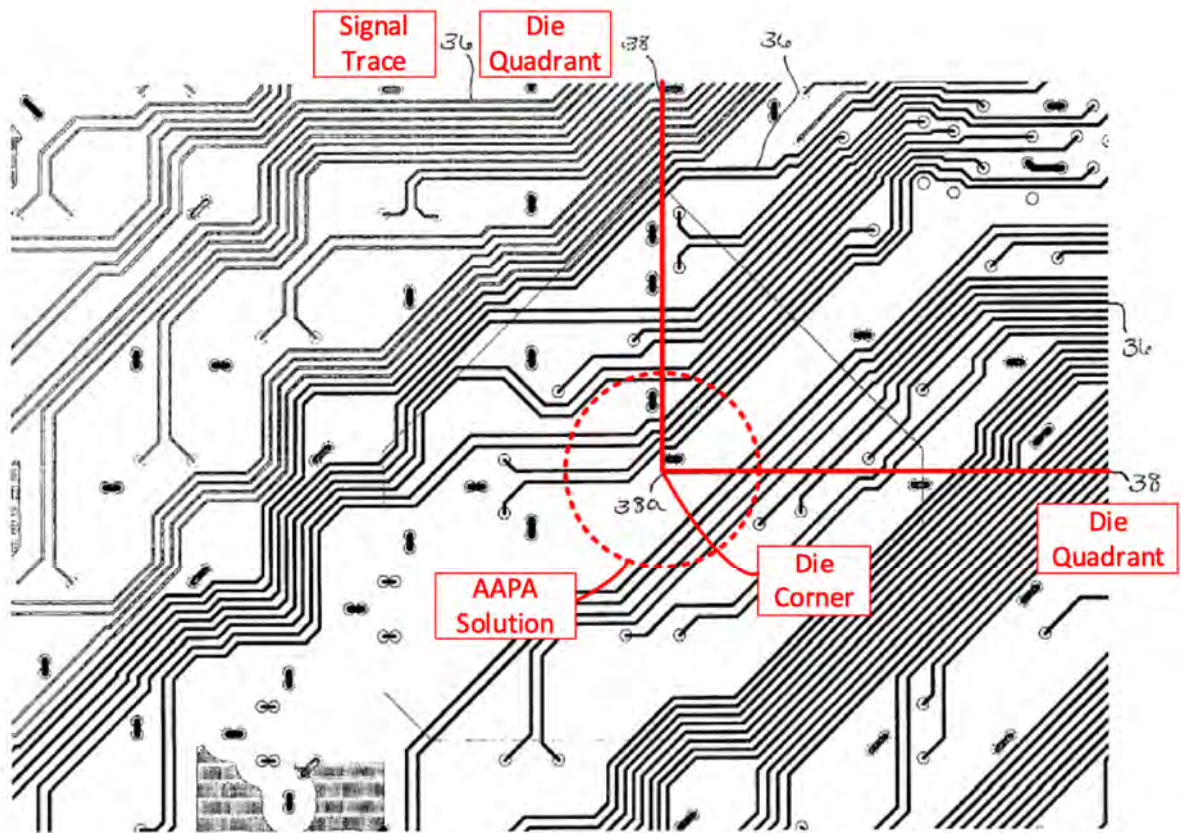


(*Id.*, Fig. 2 annotated)

30. As shown above in Figure 2, the '245 patent further discloses as AAPA a diagram representing Layer L9 (ball pad layer) of the 9-layer stackup of Figure 1

(Ex. 1001, 2:42-44). “A portion of Layer L9 of the 9-layer stackup 20 is shown in FIG. 2. Circularly shaped ball pads 34 of layer L9 are dispersed throughout layer L9. The ball pads 34 (*referred to as ball pads 30 in Figure 1 of the '245 patent*) may be dispersed in a partial or full-array format. Placement of a quadrant of the die over the solder masses 28 is represented by line 38, which is annotated in Figure 2. Placement of one of the corners of the die is represented by the point 38a.” (*Id.*, 1:43-49 annotated)

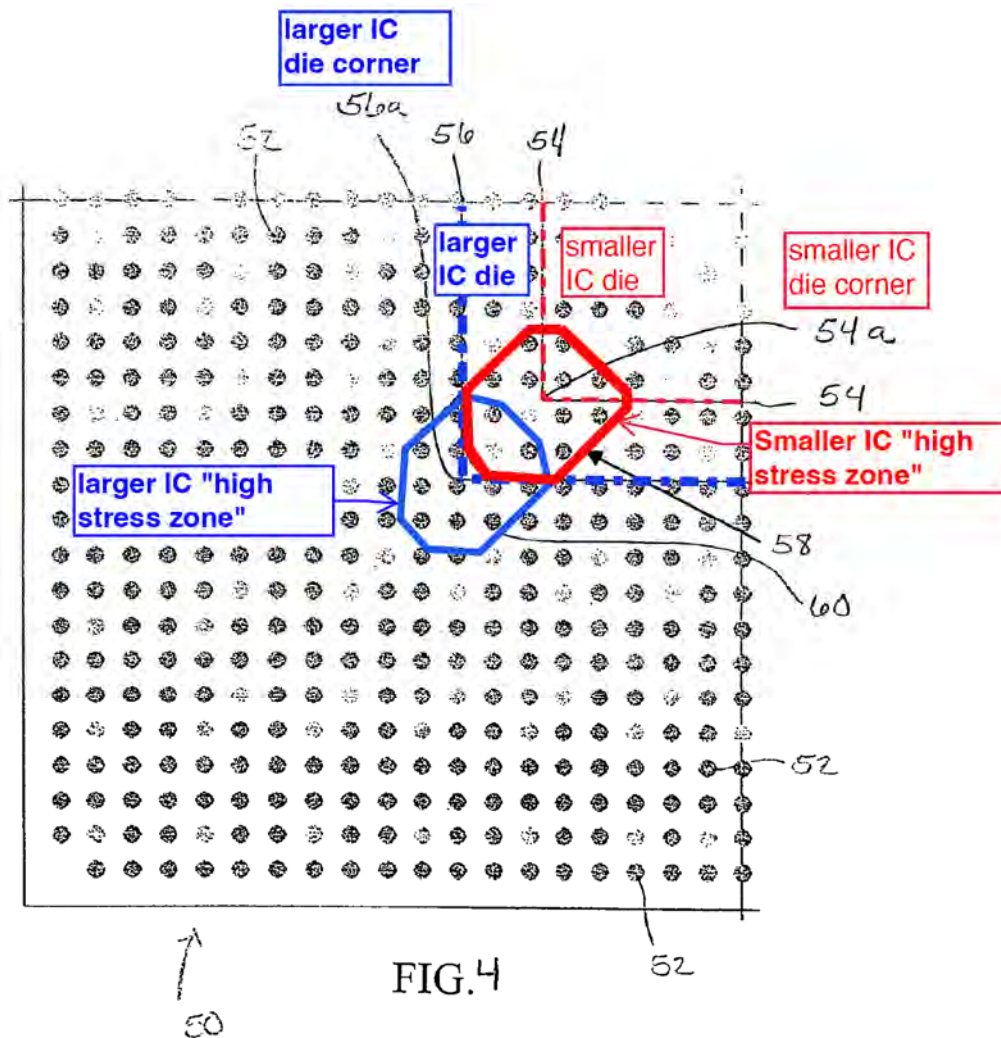
31. The '245 patent in Figure 3, shown below, discloses further prior art (AAPA) of a portion of layer L8 (bottom routing layer) of the 9-layer stackup of AAPA Figure 1 of the '245 patent. The '245 patent states that “the signal traces 36 of layer L8 are routed over the ball pads 34 of layer L9. Areas of high stress are associated with the die corner 38a and in particular the ball pads which are positioned under the area surrounding the die corner 38a. The edges of the ball pads 34, which are associated with the die corner 38a act as stress concentration points and under thermal cycling conditions, cracks are initiated from the edges of the ball pads 34 and extend into the dielectric layer above layer L9. If traces 36 are routed or other metal structures are provided on layer L8 over the ball pads 34 associated with the die corner 38a, the cracks can extend through the traces 36 and cause failures due to trace cracks under cycled stress conditions.” (*Id.*, 1:51-2:2)



(*Id.*, Fig. 3 annotated)

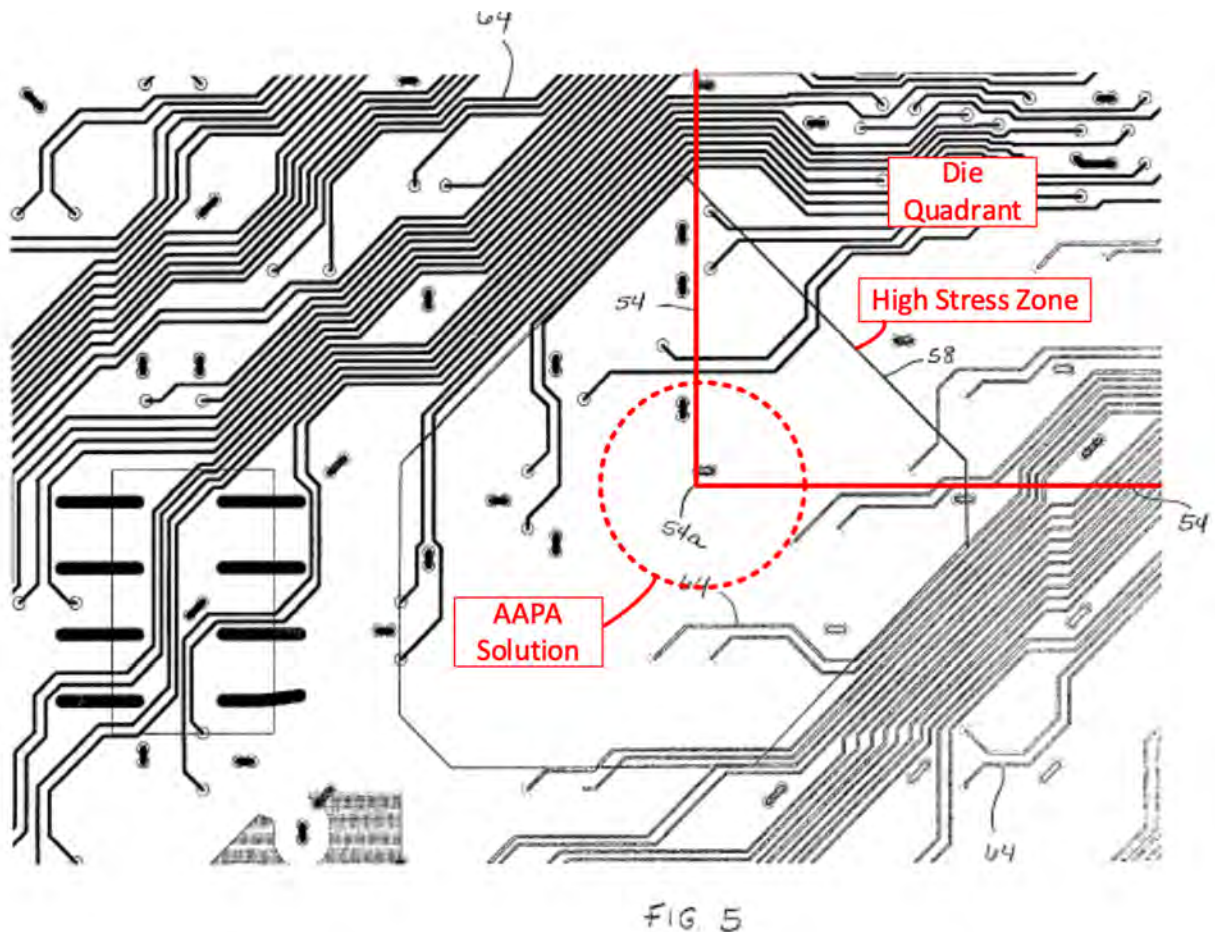
32. The '245 patent describes prior solutions to this problem. In particular, the '245 patent states, "Another existing solution to overcoming this problem is to define a circular shaped area with a one (1) millimeter radius using placement of the die corner 38a as the center of the circle." (*Id.*, 2:6-9) I've annotated Figure 3 with this admitted prior art solution labeled as "AAPA Solution." With the AAPA Solution, L8 signal traces 36 are "not routed within the circular region." (*Id.*, 2:10-11)

33. But, according to the specification of the '245 patent, the 1 mm radius circle (AAPA Solution) used to define the area of stress is not large enough. "A disadvantage of having a one (1) millimeter radius region under the die corner 38a is that it is not sufficient to avoid trace cracks in the layer L8 under thermal cycling conditions" for all packaging technologies. (Ex. 1001, 2:11-15)



(Id., Fig. 4 annotated)

34. The '245 patent purports a solution to overcome the problem of thermal cycling causing trace cracks of a routing layer, described herein with reference to Figures 4 and 5 of the '245 patent and related text. Figure 4 of the '245 patent, shown above and which I've annotated in red and blue, illustrates a quadrant of a semi-conductor package, showing L9 layer 50 (ball pad layer) having ball pads 52 dispersed thereon. (*Id.*, 2:56-58) Figure 5 is a diagram representing layer L8 of a 9-layer stackup of a substrate package. (*Id.*, 2:59-60) Line 54 represents placement of a die on an opposite surface of the semi-conductor package.



(*Id.*, Fig. 5 annotated)

35. A first stated improvement to the AAPA 1 mm radius is to provide “a substrate package in which signal traces are routed away from the high stress area associated with the ball pads and the corner of the die.” (*Id.*, 3:6-9). More specifically, rather than defining the area of stress as the circular area having a 1 mm radius (of the AAPA Solution), the '245 patent defines the area of stress as a high stress zone 58 that is associated with the die corner 54a that “extends approximately two ball pitches away from the die corner 54a in each direction.” (*Id.*, 3:20-26) Notably, this “two ball pad pitch” distance is the same for each high stress zone 58, 60 shown above in Figure 4 and “each high stress zone 58, 60 is similarly shaped.” (*Id.*, 3:22-23)

36. “Signal traces 64 and other metal structures are provided throughout layer L8, however, within the high stress area 58, the signal traces 64 and other metal structures, for example, voltage bus bars, are routed away from the die corner 54a. Thus, the high stress area 58 on layer L8 includes a very small number of signal traces 64 and other metal structures. Preferably, all of the signal traces 64 are routed outside the high stress area 58. If, however, the traces 64 cannot be moved outside the high stress Zone 58, the traces 64 are routed so as to avoid routing the traces 64 over the ball pads 52 of layer L9 within the high stress area 58. Traces on L8 may be routed over sections of continuous solid plane on L9 within the high stress region.” (*Id.*, 3:39-54)

37. A person of ordinary skill in the art would take note that the '245 patent does not disclose any specific reason, advantage, or unexpected result for a distance of “two ball pad pitches” or for the size or shape of the “high stress area” around the corner of a die.

38. As explained below (*infra* Section X), the above purported inventive features were either all known in the prior art or are obvious variants thereof.

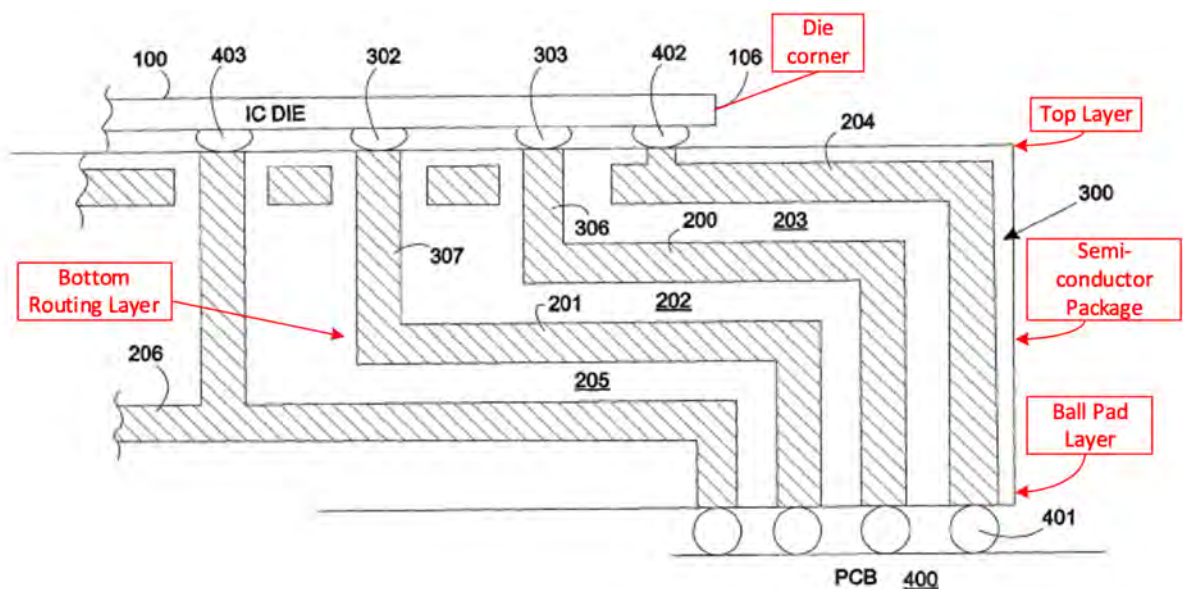
VII. CLAIM CONSTRUCTION

39. I understand that claim terms are typically given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art, at the time of the alleged invention, which I was asked to assume was in April of 2006. In considering the meaning of the claims, however, I understand that one must consider the language of the claims, the specification, the prosecution history of record, and the knowledge of a person of ordinary skill in the art at the relevant time.

VIII. OVERVIEW OF THE PRIOR ART

A. Devnani

40. Devnani discloses a packaged integrated circuit (IC) that includes an IC die that has an IC die edge. (Ex. 1005, ¶0020) The IC package has a top layer, a bottom routing layer, and a ball pad layer for solder balls 401 as shown below in Figure 4.



(*Id.*, Fig. 4 annotated)

41. In Figure 3 below, Devnani further discloses an absence of signal traces of the IC package near the corner of the IC die.

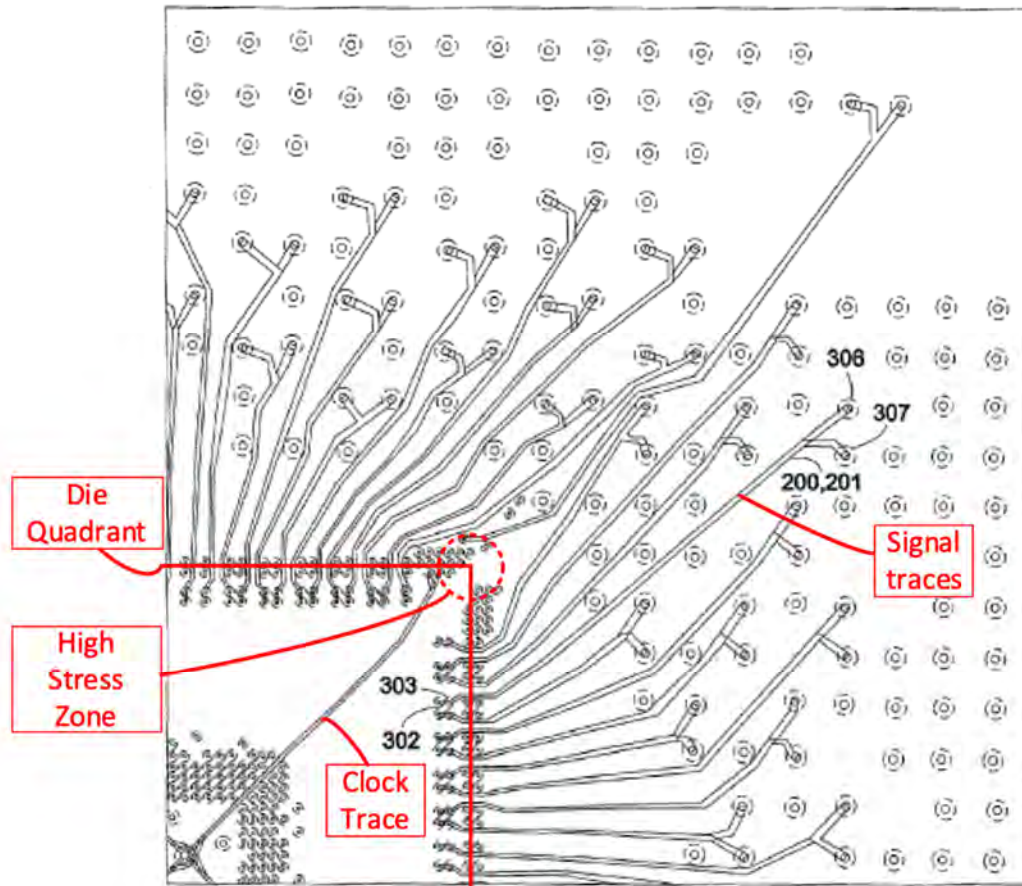


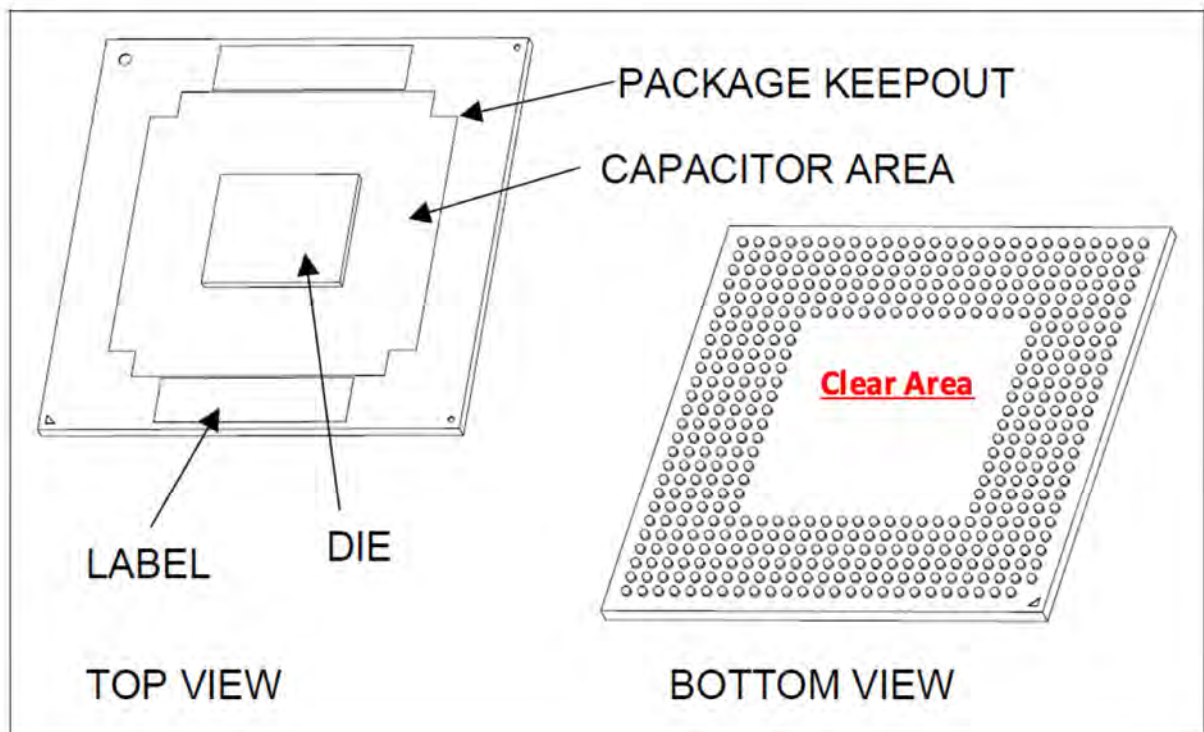
FIG. 3

(*Id.*, Fig. 3 annotated)

42. As evidenced above by Applicant's Admitted Prior Art, and numerous contemporaneous references (below), it was well known that a corner of a die and associated solder pads are stress concentration points. (Ex. 1001, 2:57-65)

B. Celeron

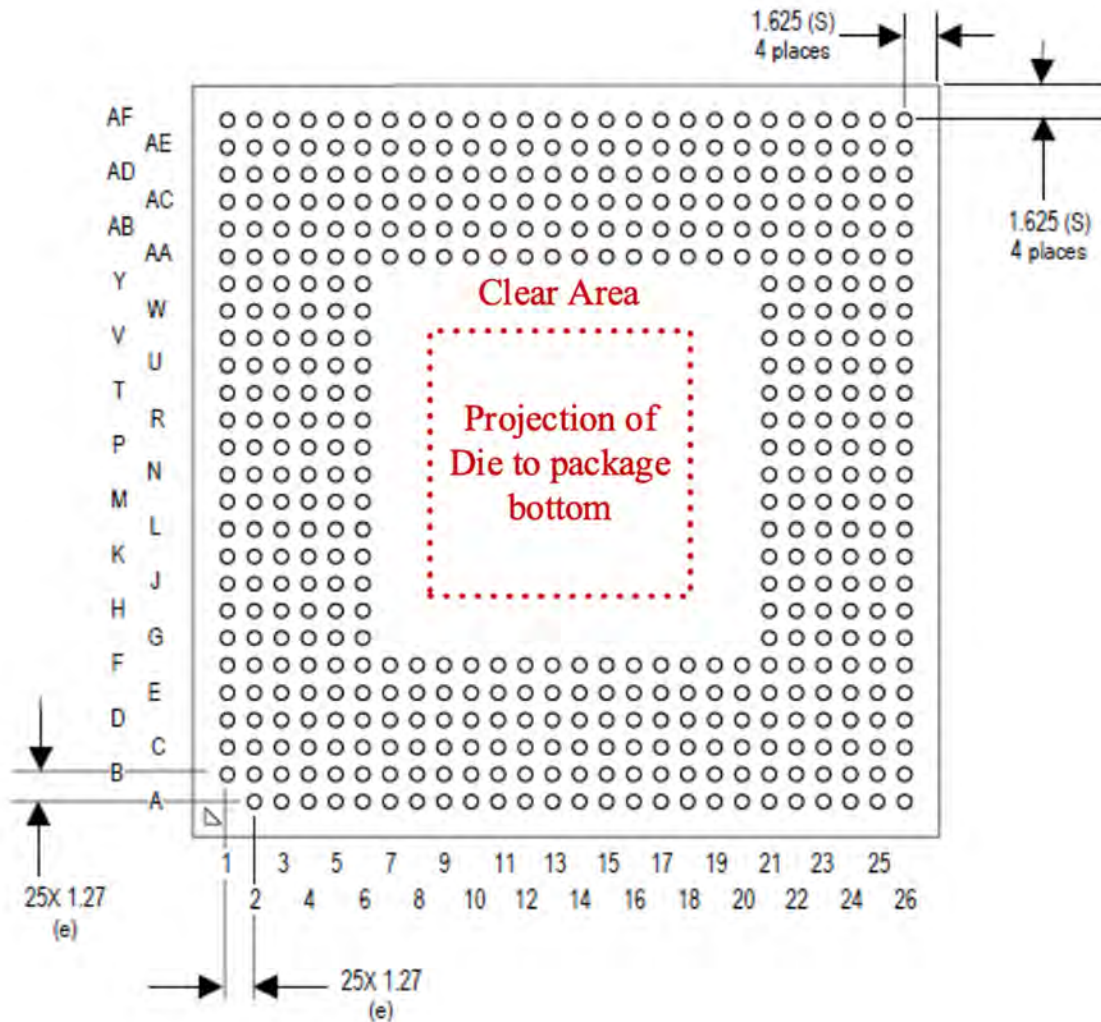
43. Celeron discloses a Micro-FCPGA IC package that includes an IC die. (Ex. 1008, p. 70) As shown below in Figure 28, the IC package includes a clear area where the bottom of the package is free of solder balls.



(*Id.*, Fig. 28 annotated)

44. Celeron further discloses in Table 44, the distances from the edge of the package to the first solder ball, the pitch of the solder balls, the size of the IC die, and the size of the IC package. (*Id.*, Table 44).

45. Figure 30 of Celeron is annotated below to show where the die is in relation to the clear area. As shown, there are no solder balls near the edges and corners of the die.



(Id., Fig. 30 annotated)

C. Moore

46. Moore discloses warpage and thermomechanical stress damage within an IC package, including to copper traces (Ex. 1010, Abstract). Moore shows in

Figure 3, an example of an IC package substrate that includes 4 layers, an attachment area for an IC die, and that sits on solder balls. (*Id.*, Section 4)

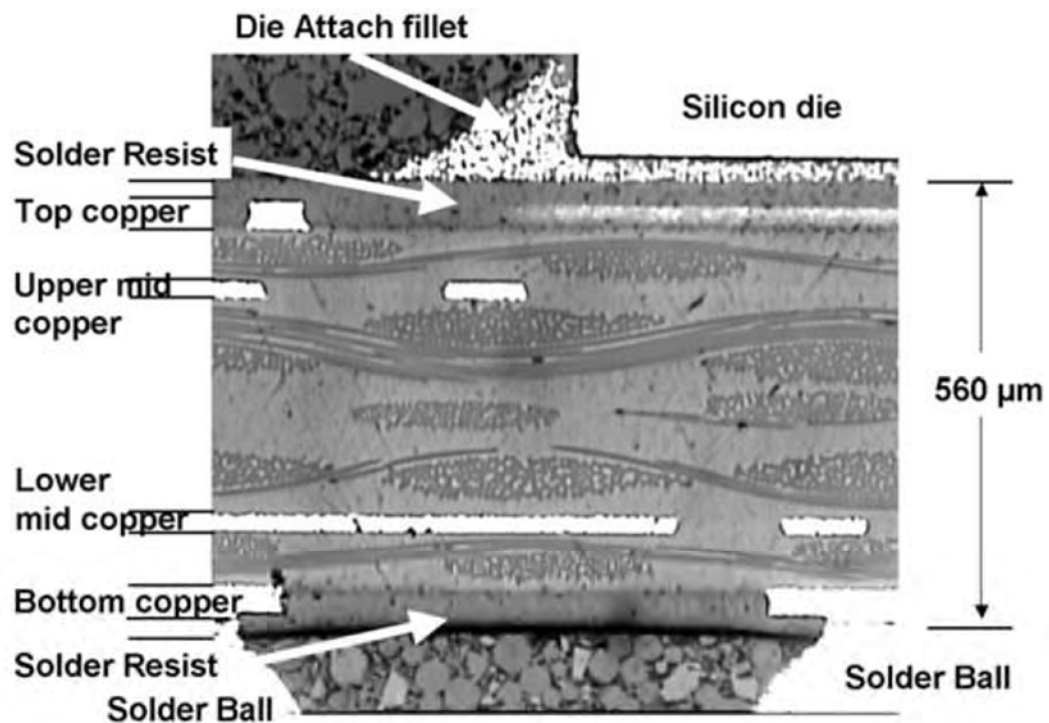


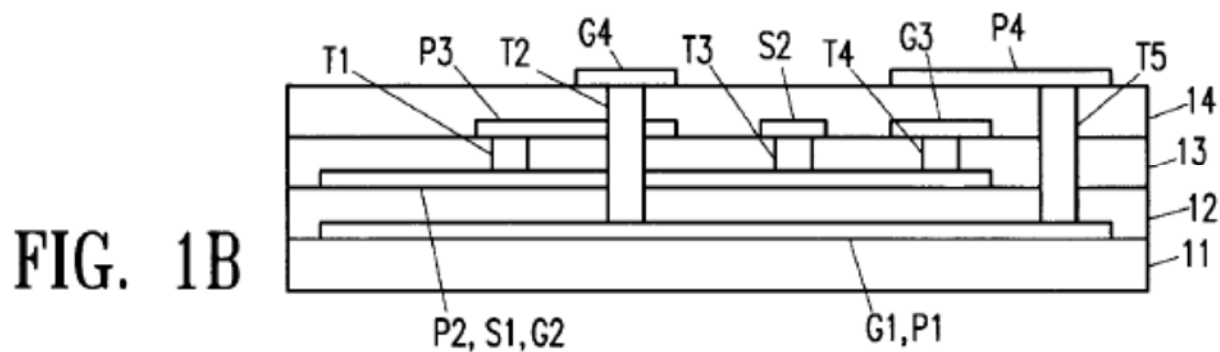
Fig. 3. Cross-section of 4-layer BGA substrate.

(*Id.*, Fig. 3)

47. Moore discloses that IC packages are composed of a variety of materials, which are assembled at elevated temperatures. Each of the materials has a different coefficient of thermal expansion, which during these elevated temperatures and subsequent cooling gives rise to thermomechanical stress that can damage the IC assembly. (*Id.*, Section 2)

D. Tanahashi

48. Tanahashi discloses signal trace S1 and a voltage bar P2 on a same internal layer of an IC package. As shown in Figure 1B, Tanahashi shows the trace and voltage bar routed on the layer immediately above a layer having ground and power (lowest layer). (Ex. 1009, 9:10-28)

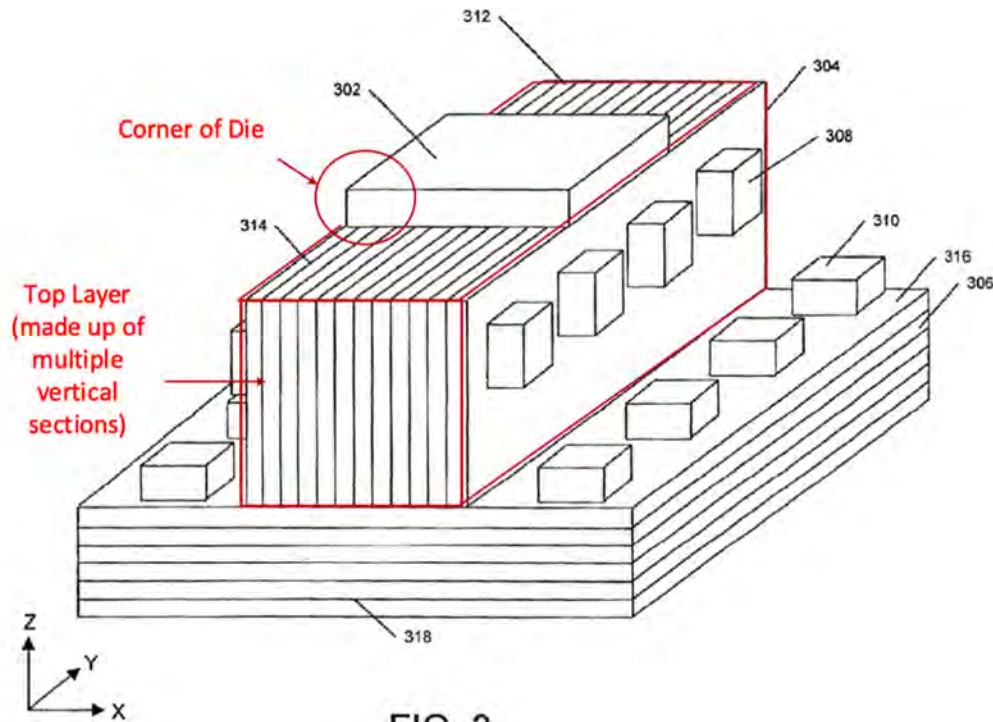


(*Id.*, Fig. 1B)

E. Chung

49. Chung discloses an integrated circuit (IC) package that has a plurality of layers and also includes an IC die 302 that has a die corner, as shown below in

Figure 3. The package includes a vertical section 304 and a horizontal section 306.
(Ex. 1006, ¶0036) As shown in Figure 3, the die 302 is mounted to the top layer 304.



(*Id.*, Fig. 3 annotated)

50. Chung further discloses the layers include a ball pad layer and a bottom routing layer. (*Id.*, ¶0047)

F. Pillai

51. Pillai discloses in Figure 1 (below), an integrated circuit package for high speed applications that includes routing signals thru a layers of the package that is connected to a substrate 10 via bold pads 24 and solder balls 22. (Ex. 1007, 2:1-

20) As shown in Figure 1 below, the layers of package 100 include a bottom routing layer 104-1 and a ball pad layer 102-1.

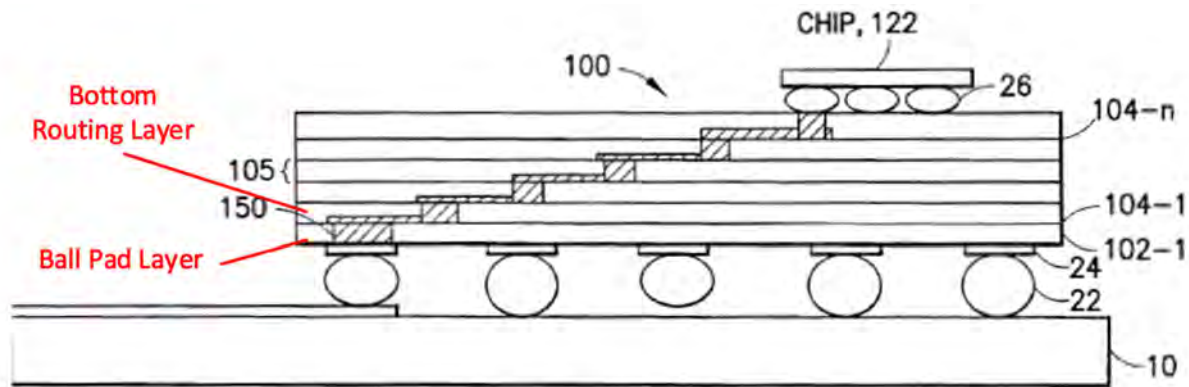
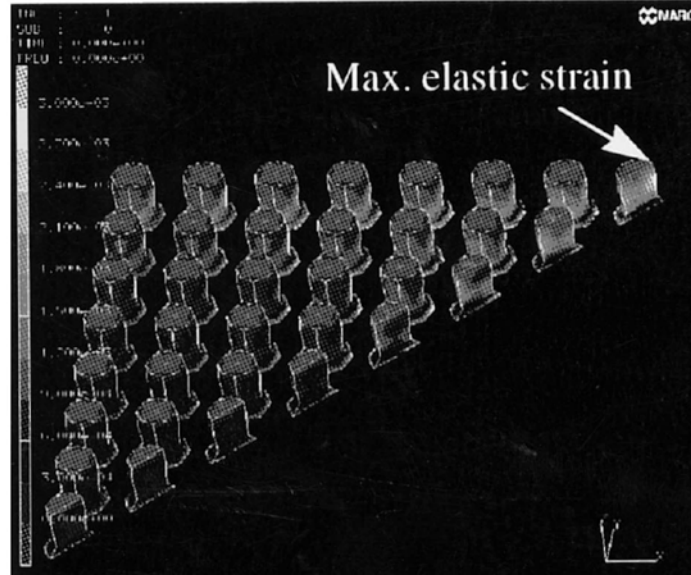


FIG. 1

(*Id.*, Fig. 5 annotated)

G. Xie

52. Xie discloses thermal fatigue life prediction for ball grid array (BGA) solder joints (Ex. 1011, Title) Xie discloses that a “**maximum strain** is located in the **corner joint**” as shown in Figure 1B (below). (*Id.*, p.33 [emphasis added])



(*Id.*, Fig. 1B)

53. Xie further discloses that this strain concentration indicate that “**cracks would initiate and propagate from that location**” due to temperature cycling. (*Id.* p. 44 [emphasis added])

H. CRTA (Critical Review and Technology Assessments '91-'92)

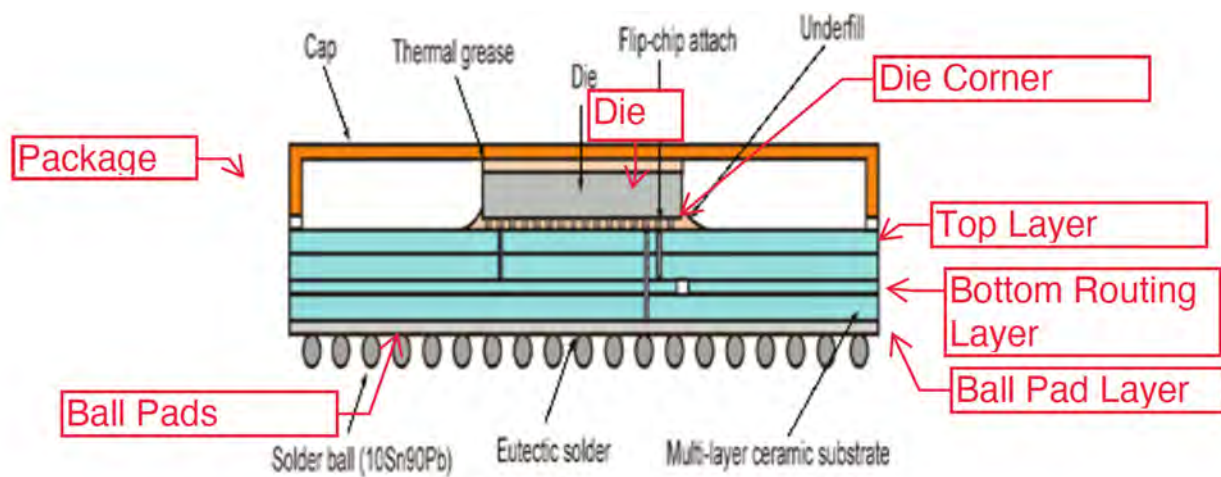
54. CRTA discloses that thermal coefficient of Expansion (TCE) mismatch have be identified by major manufacturers that cause cracking during temperature cycling (Ex. 1016, p. 32) The damage from these cracks include cracks in the package (*Id.*, p. 33) CRTA further discloses that the “cracking generally occurs **near the corners of the chip**”. (*Id.*, [emphasis added]) Further, CRTA states that “package stress increases exponentially from the package center along a radius line to the die corner.” (*Id.*, p. 34)

I. Performance Characteristics of IC Packages (PCIP)

55. PCIP discloses “A typical electronic package assembly consists of different materials which are attached together in a variety of ways. The coefficient of thermal expansion mismatch between these different materials induces stresses in the attached components during manufacture and in operation. Flexing of a card, or other types of mechanical loads on the card with surface mounted components attached to it **causes stresses to be induced in the surface mounted joints.** Irrespective of the origin of the stress, when these stresses exceed the strength of the material, **a crack initiates at the weakest point.** After initiation, **the crack propagates until complete failure occurs.** Depending on the material and the location at which failure initiates, loss of functionality of the component (**electrical** or mechanical) can take different periods of time. The manufacturing process typically introduces many small flaws at different regions of the component. **Crack initiation usually occurs at these pre-existing flaws at high stress locations in the component.**” (Ex. 1017, p. 18 [emphasis added]) PCIP further discloses that thermal mismatches introduce stresses in an IC package and that “high stresses occur locally at the die edges”. (*Id.*, p. 19)

J. Review of Ball Grid Arrays for Electronic Assembly (“Review of BGAs”)

56. Review of BGAs discloses various ball grid array packages, and in Figure 3 below, shows a package with a die mounted on a top layer, a plurality of layers under the package, a ball pad layer under a bottom routing layer. (Ex. 1017, p. 6)



(*Id.*, Fig. 3 annotated)

57. Review of BGAs states “a solder resist mask can induce a point of high stress in the ball, resulting in a cracked joint. The worst case scenario would be that the crack propagates 360° around the ball causing electrical failure.” (*Id.*, p. 14) Review of BGAs also discloses ways to increase I/O counts that in multilayer packages, would still allow vias “to be placed away from the solder joint” (*Id.*) Review of BGAs states “Cracking of the solder joint, induced by thermal fatigue,

has been identified as a major failure mode in electronics packages”. (*Id.*, p. 17))

Review of BGAs also discloses that “in the case of BGAs constructed from thin laminates with the die bonded directly to the laminate, the greatest strains are found beneath the edges of the silicon die. In this case, fatigue life may be extended by depopulating the area immediately beneath the silicon die; i.e. **by having solder balls around the perimeter of the package and at the centre only**. (*Id.* [emphasis added])

IX. EXPLANATION OF MY OPINIONS

58. The following sections provides my opinion that claims 1-12 of the '245 patent are invalid as discloses and/or rendered obvious by the prior art. Below, I address each claim element on an element-by-element basis for each reference and/or combination of references, as well as the motivation to combine references and reasonable expectation of success in doing so. Given certain similar claim elements and the use of the same references in multiple combinations, many of the explanations herein would apply to multiple claim elements and reasons that a person of ordinary skill in the art (POSITA) would be motivated to combine these references and have a reasonable expectation of success in doing so. As such, my explanation regarding a certain claim element and certain reference or combination may also apply to other claim elements or the use of that same reference in another combination for the same or a similar claim element. This applies even when there

is no explicit incorporation by reference. Furthermore, while I have cited portions of each reference to provide my opinions below, I may rely on additional portions of a reference to further support those opinions, or portions of other references, including portions identified above where I discussed the prior art and the technology background.

X. THE PRIOR ART DISCLOSES ALL OF THE FEATURES OF THE CHALLENGED CLAIMS.

A. Ground 1 – Claims 7, 8 and 10-11 are obvious by Devnani in view of Applicant’s Admitted Prior Art (AAPA)

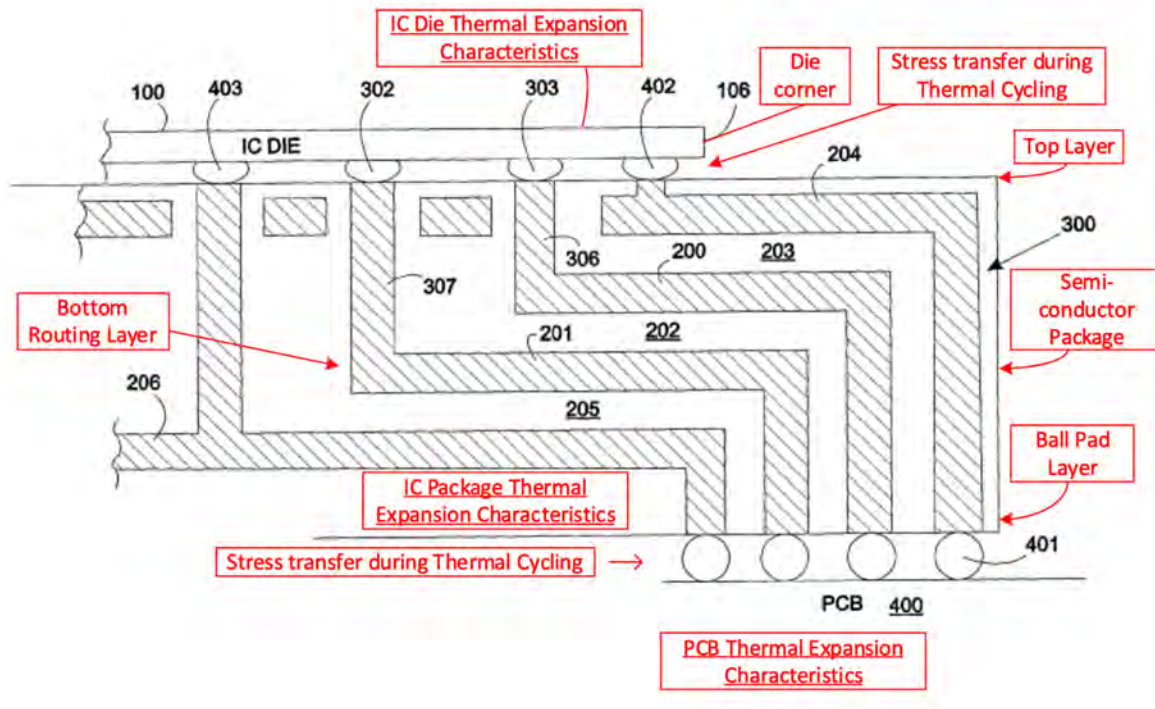
59. As shown in detail below, Devnani in combination with AAPA discloses or suggest all features recited in claims 7, 8 and 10-11.

1. Claim 7

a) “A semi-conductor package comprising:”

60. I understand that “a semi-conductor package comprising” is the preamble to claim 1 of the ’245 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, in my opinion, Devnani and AAPA both disclose this claim feature.

61. Figure 4 of Devnani, as shown and annotated below, discloses a semi-conductor package 300. (Ex. 1005, ¶0023)



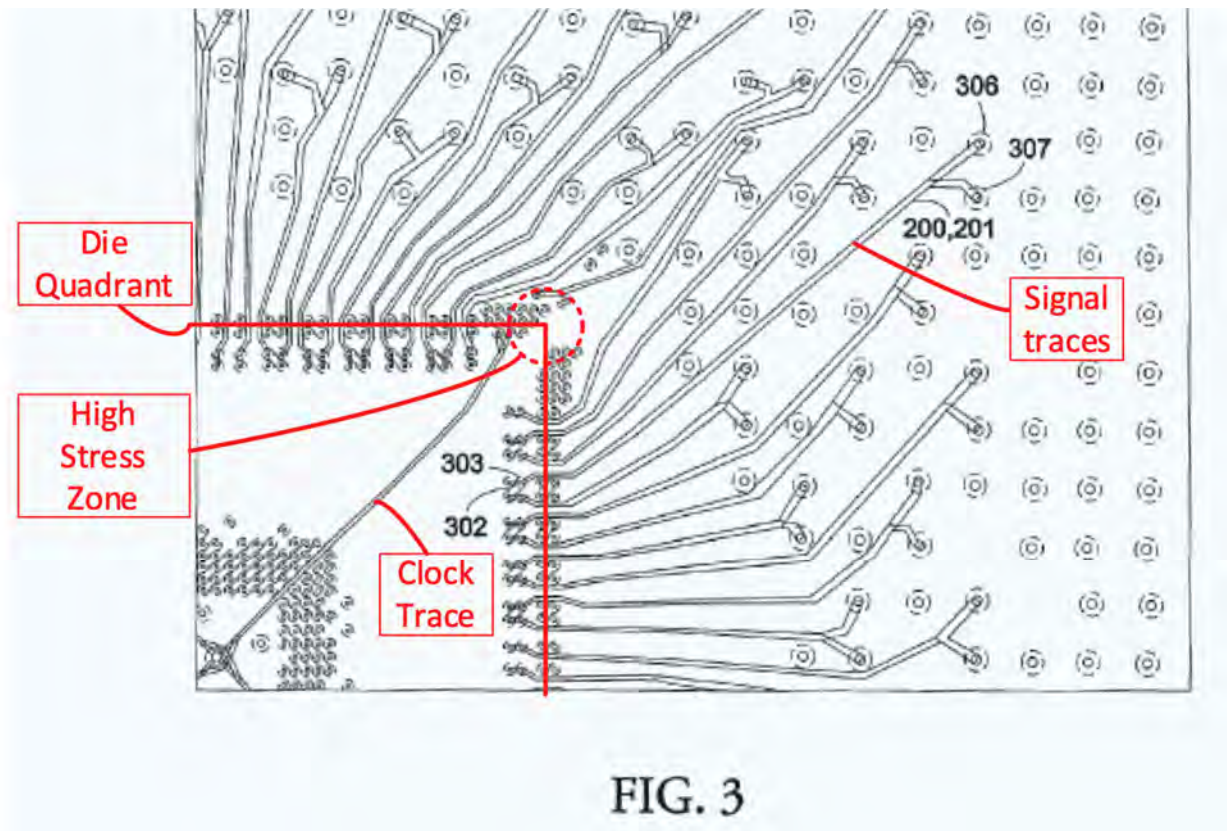
(*Id.*, Fig. 4 annotated)

62. AAPA also discloses a semi-conductor package. (Ex. 1001, 1:7-12)

b) “a top layer having a die mounted thereon, said die having a corner defining a surrounding area of increased stress; and”

63. In my opinion, Devnani in combination with AAPA discloses this claim feature. Devnani shows in Figure 4 above, a die 100 mounted upon a top layer of the semi-conductor package 300, where die 100 has a die edge 106, which a person of ordinary skill in the art would understand to include a die corner (Ex. 1005, ¶0022) Figure 4 has also been annotated to show stresses from thermal cycling based on

differing thermal expansion characteristics for the various materials of the IC die, the semiconductor package, and the printed circuit board (PCB) as was well known in the art as admitted by AAPA. Figure 3, shown below, has been annotated to show the area of increased stress (“high stress zone”) near the die corner and how Devnani implicitly discloses routing signal traces away from such stress. However, Devnani does not explicitly state that the “corner defines a surrounding area of increased stress”.



(*Id.*, Fig. 3 annotated)

64. Nonetheless, AAPA discloses that “areas of high stress are associated the die corner 38a”. Further as discussed above in Section VIII, this die corner

associated stress was well known in the art before the date of invention of the '245 patent. (*Id.*, 1:58-60)

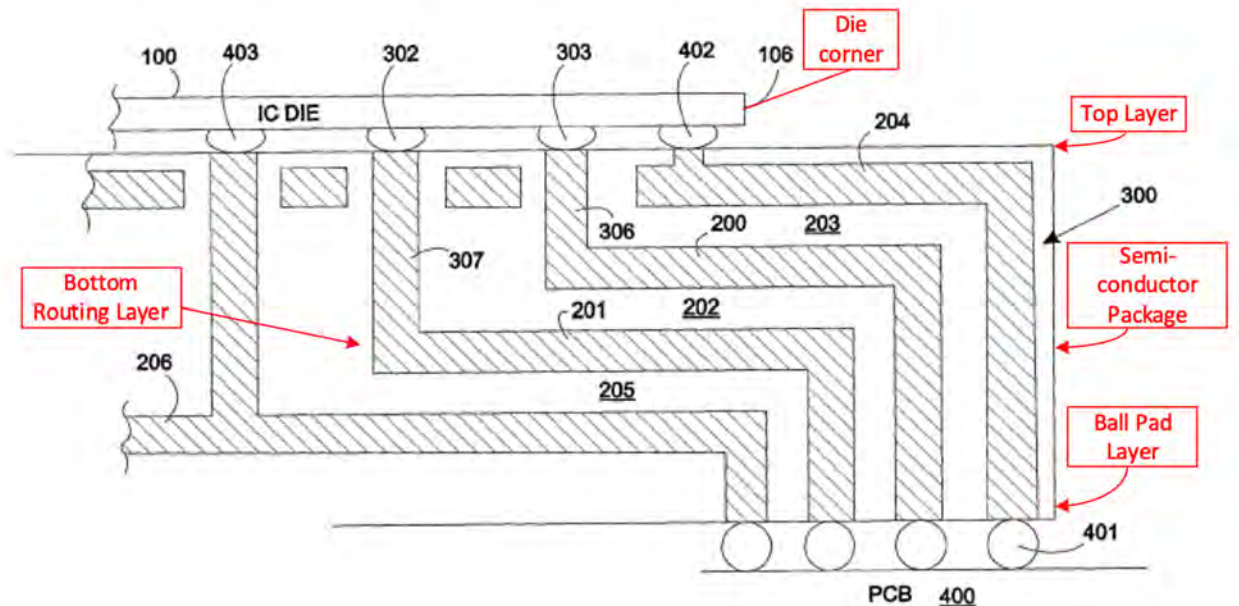
c) “a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces thereon,”

65. In my opinion, Devnani and AAPA discloses this claim feature. Figure 4 of Devnani discloses “a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces 201 thereon”. (Ex. 1005, ¶0023) Devnani discloses layers in an IC package (*Id.*, ¶0005) and also shows in Figure 4 a layer for routing signals (e.g., signal 201) that is lower than other layers of the IC package. (*Id.*, ¶0005; 0025; Claim 1) A person of ordinary skill in the art would understand that a “bottom routing layer” would be a routing layer beneath another layer of the IC package.

66. I’ve been asked to assume that Devnani does not disclose this feature. Under this assumption, AAPA discloses “signals are typically routed directly over the ball pads under the die corner on **the bottom routing layer**” (Ex. 1001, 1:24-26) and further discloses “a typical multi-layer organic BGA flip chip substrate that uses a 9-layer stackup”. (*Id.*, 1:27-29). As such, AAPA discloses a plurality of layers under a top layer (e.g., layers 2-9 of the 9-layers) and that signal traces are on a bottom routing layer. Thus, in my opinion, both Devnani and AAPA discloses this claim feature.

d) “and a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads dispersed thereon,”

67. In my opinion, Devnani and AAPA discloses this claim feature. Figure 4 of Devnani below, and related text discloses a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads 401 dispersed thereon. (Ex. 1005, ¶0023)



(Id., Fig. 4 annotated)

68. I’ve been asked to assume that Devnani does not disclose this feature. The AAPA discloses “The 9-layer stackup 20 includes a layer L1, a layer L2, a layer L3, a layer L4, a layer L5, a layer L6, a layer L7, a layer L8, and a layer L9....An upper protective mask 22 is provided proximate layer L1 and a lower protective layer 24 is provided proximate layer L9.” (Ex. 1001, 1:28-35) AAPA further discloses that

“A plurality of ball pads 30 (one of which is shown) are provided on Layer L9.”

AAPA further discloses that “signal traces 36 of layer L8”. (*Id.*, 1:57)

69. As such, the AAPA is disclosing a ball pad layer (L9) is under the bottom routing layer (L8) and that a plurality of ball pads (ball pads 34) are dispersed thereon.

e) “wherein none of the signal traces of the bottom routing layer are located within the area of increased stress defined by the corner of the die.”

70. In my opinion, Devnani and AAPA discloses this claim feature. Figure 3 (below) of Devnani is annotated to show where a die quadrant resides when the IC die is mounted upon the package 300 and to identify the high stress zone associated with the corner of the die as disclosed by AAPA.

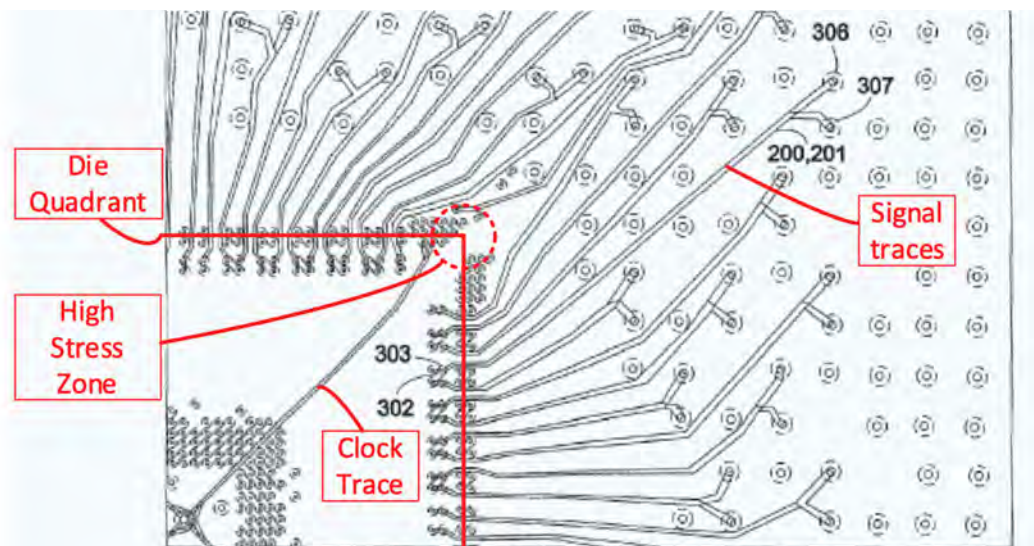
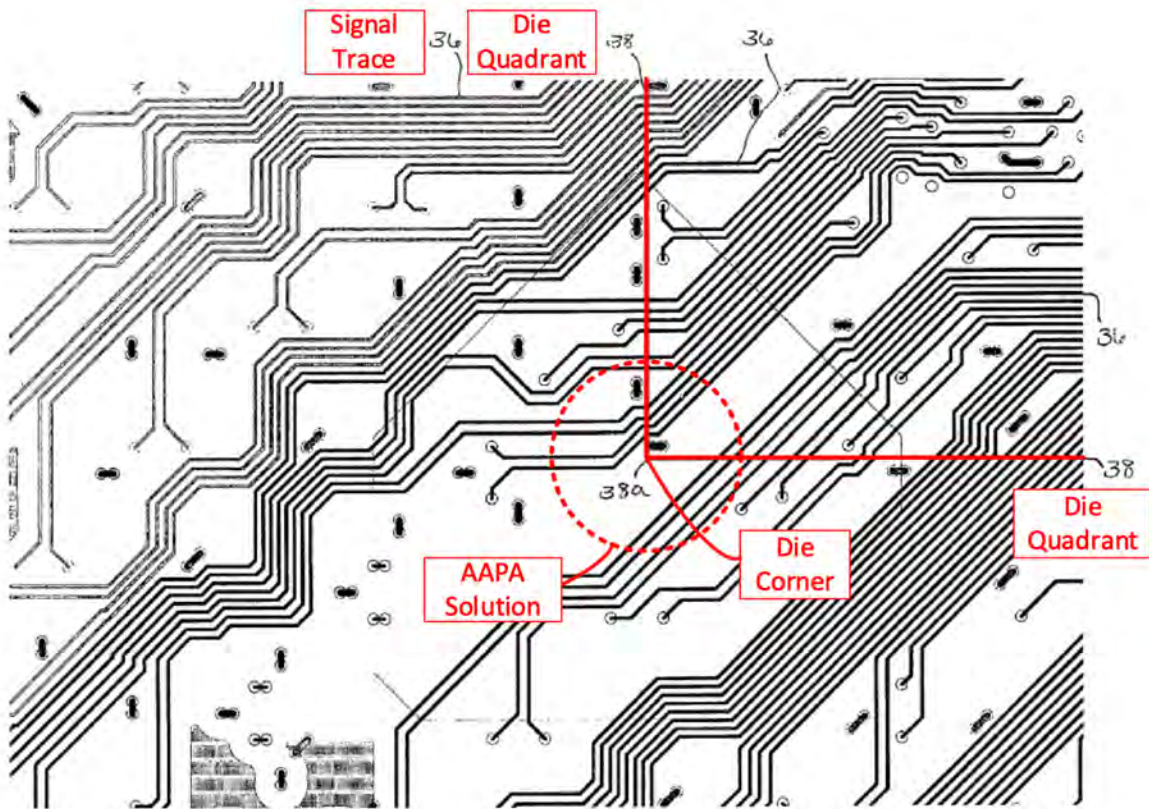


FIG. 3

(Ex. 1005, Fig. 3 annotated)

71. As is shown in Figure 3 of Devnani, all of the signal traces are routed from edges of the die and outside of an area near the die corner. Thus, in my opinion, this inherent feature of Devnani discloses signal traces being routed away from the high stress zone. I've been asked to assume a scenario where Devnani does not disclose the claim feature. Under this assumption, AAPA also discloses this claim feature.

72. AAPA discloses in Figure 3 (shown below) of the '245 patent and its accompanying description, an existing, *i.e.*, prior art, solution (AAPA Solution) used to prevent stress cracks in traces is by routing the traces on the bottom routing layer outside a high stress zone associated with the corner of the die. (Ex. 1005, 1:56 – 2:2) The AAPA Solution defines the high stress zone as being a circular area having a radius of 1 mm around the corner of the die. In particular, AAPA states that “Another existing solution to overcoming this problem is to define a circular shaped area with a one (1) millimeter radius using placement of the die corner 38a as the center of the circle. **When routing traces on layer L8, traces are not routed within this circular region.**”) (*Id.*, 2:6-11, emphasis added) Note that Figure 3 does show some traces routed near the die corner.



(*Id.*, Fig. 3 annotated)

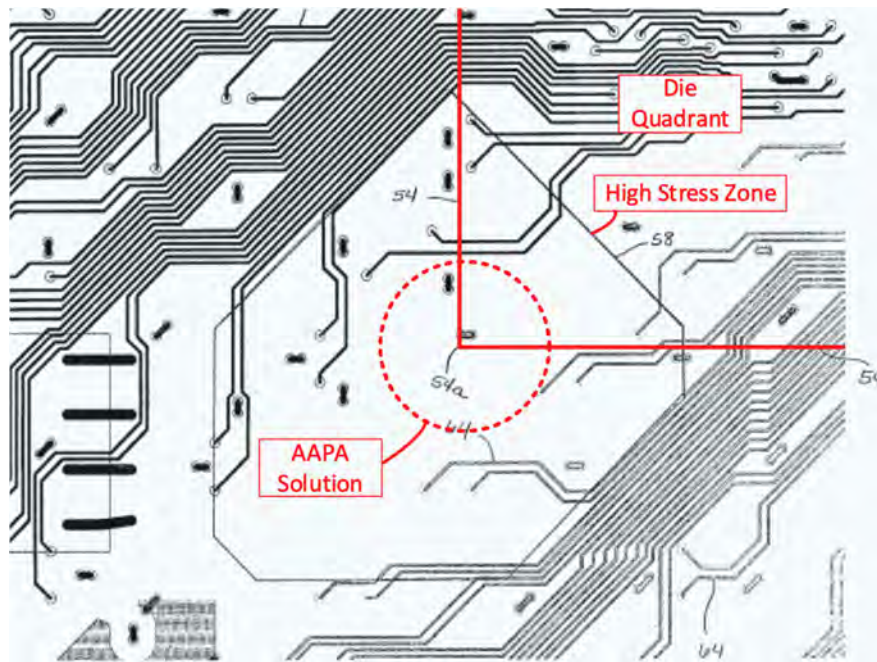
73. Further, a person of ordinary skill in the art implementing the semiconductor package of Devnani would have good reason to look to AAPA to route signal traces away from a high stress area associated with the corner of a die as they both are in the same field of semiconductor packages. As was well known years prior to the date of the '245 patent, the corner of the die and the ball pads near the corner of the die experience the most stress during thermal cycling (see generally Section VIII above). Thus, a person of ordinary skill in the art would have been

motivated to implement AAPA to move traces away from high stress areas to prevent trace cracking with the IC package of Devnani.

74. Further, the modification of Devnani with the AAPA would have amounted to nothing more than the use of a known technique to improve a similar device, and the results of the modification would have been predictable. This is because at the time of the invention, a person of ordinary skill in the art would have had the requisite skill level to readily modify the IC package disclosed by Devnani to implement the teachings of routing traces away from an area of high stress as disclosed by AAPA of the '245 patent. Moreover, such modification of Devnani would have been routine for the person of ordinary skill in the art as they would be using well-known elements with no change in their respective functions.

75. Notably, the only difference between the AAPA solution and the purported invention of the '245 patent is the increased area of the high stress zone as shown below in Fig. 5 of the '245 patent and which is annotated with a rough estimate of the high stress area of the AAPA solution. The AAPA Solution defines the area of increased stress as a circle centered on the corner of the die.

76. The AAPA Solution, as shown in Figure 5 of the '245 patent, discloses that “none of the signal traces of the bottom routing layer are located within the area of increased stress defined by the corner of the die the circle centered at the corner of the die” as required by the last element of claim 7 of the '245 patent.



(*Id.*, Fig. 5 annotated)

77. A person of ordinary skill in the art would have been motivated to combine the teachings of Devnani with the AAPA Solution to select a high stress zone that is larger than the AAPA Solution to reduce potential damage to signal traces of a package during thermal cycling. A person of ordinary skill in the art would have been motivated to select dimensions of such a high stress zone based upon an analysis of thermal expansion characteristics of die 100, the package 300, and a PCB

upon which the package mounts as these characteristics were all well known as evidenced by the AAPA the numerous contemporaneous references discussed above.

As such, in my opinion, claim 7 is obvious over Devnani in view of the AAPA.

2. Claim 8

a) **“A package as recited in claim 7, wherein none of the signal traces of the bottom routing layer are located within two ball pad pitches of the corner of the die.”**

78. In my opinion, Devnani in combination with AAPA discloses this claim feature. Devnani in combination with AAPA discloses a package with signal traces on a bottom routing layer and discloses a corner of a die as discussed above in Section X.A.1 regarding claim 7. Devnani does not explicitly state the signal traces that are not near the corner of the die are farther than “two ball pad pitches”. However, this distance would be obvious for a person of ordinary skill in the art implementing the IC package of Devnani-AAPA.

79. The '245 patent discloses as AAPA that an existing solution to overcoming the problem of trace cracks near a die corner “is to define a circular shaped area with a one (1) millimeter radius using placement of the die corner 38a as the center of the circle. **When routing traces on layer L8, traces are not routed within this circular region.**” (Ex. 1001, 2:7-11, emphasis added). The '245 patent states, “[a] disadvantage of having a one (1) millimeter radius region under the die

corner 38a is that it is not sufficient to avoid trace cracks in the layer L8 under thermal cycling conditions for all packaging technologies [sic].” (*Id.*, 2:11-15)

80. Thus, a person of ordinary skill in the art would have been motivated to use a larger area than the AAPA solution--e.g., an area with a diameter 2 ball pad pitches from the corner of the die, rather than a smaller circle with a 1 mm radius, to decrease the risk of cracks in signal traces during thermal cycling of the semiconductor package. Simply using a larger area (high stress zone) within which to exclude signal traces uses an admittedly known technique to achieve an admittedly known result, namely a reduction in failures due to trace cracks under thermal cycling.

81. A person of ordinary skill in the art would take note that in the '245 patent, there is no specific disclosure regarding any advantages, criticality, or unexpected results related to the specific selection of a high stress zone defined by 2 ball pad pitches from the corner of the die. A person of ordinary skill in the art would have anticipated success in reducing the number of stress cracks in signal traces by routing those signal traces outside of an area larger than 1 mm from the corner of the die, which would include an area defined by 2 ball pad pitches from the corner of the die.

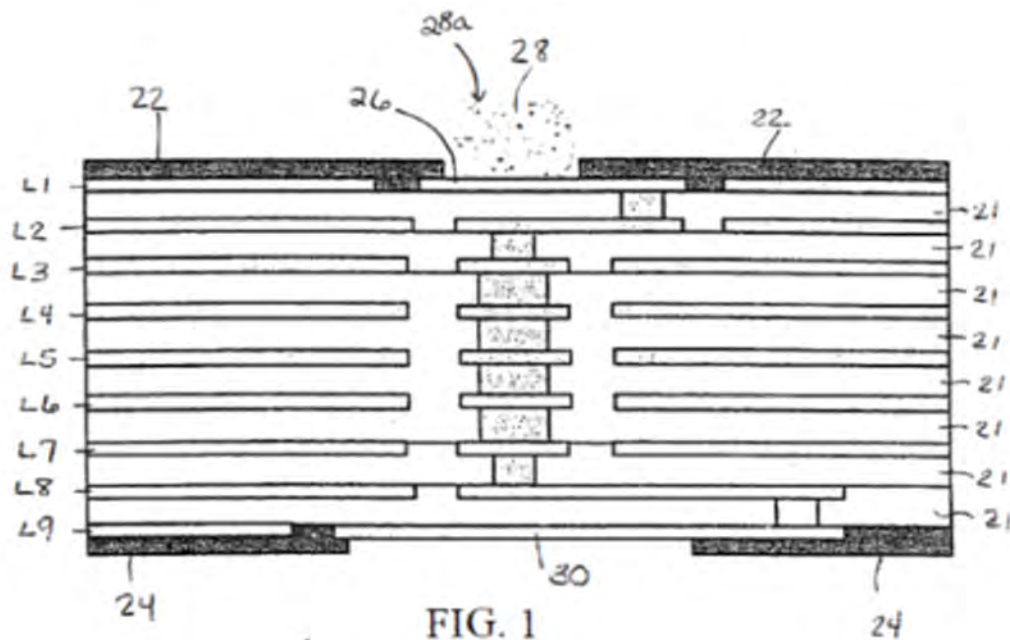
82. This is further evidence by the AAPA, which states that “under cycled thermal excursions, cracks can initiate from the ball pad edges and spread into the

layers above the ball pad layer” (Ex. 1001, 1:19-21) and “areas of high stress are associated with the die corner 38a and in particular the ball pads which are positioned under the area surrounding the die corner” (*Id.*, 1:58-60). Thus, a person of ordinary skill in the art would have good reason to include these areas of high stress under the ball pads near the corner of the die when determining the size of the high stress area. Thus, in my opinion, claim 8 would be obvious over Devnani in view of AAPA.

3. Claim 10

a) “A package as recited in claim 7, wherein the package comprises nine layers with the routing layer being the eighth layer, and the ball pad layer being the ninth layer, on a bottom of the package.”

83. In my opinion, Devnani in combination with AAPA discloses this claim feature. Devnani in combination with AAPA discloses a package with nine layers with a routing layer on layer 8 and a ball pad layer on layer 9 as discussed above in Section X.A.1(d) regarding claim 7.



(Ex. 1001, Fig. 1)

84. This is further evidenced by Figure 1 of the '245 patent, which shows a prior art IC package with 9 layers, with a bottom routing layer on layer 8 and a ball pad layer on layer 9. A person of ordinary skill in the art would have been motivated to combine the AAPA 9-layer stackup with a ball pad layer and routing layer with the IC package of Devnani to route signals, power, and ground between a die and a PCB as was widely known in the art.

4. Claim 11

a) “A package as recited in claim 7, wherein the die is mounted to the top layer in an arrangement other than a pin connection.”

85. In my opinion, Devnani and AAPA discloses this claim feature. Devnani discloses the additional element of claim 11, “wherein the die is mounted to the top layer in an arrangement other than a pin connection.”

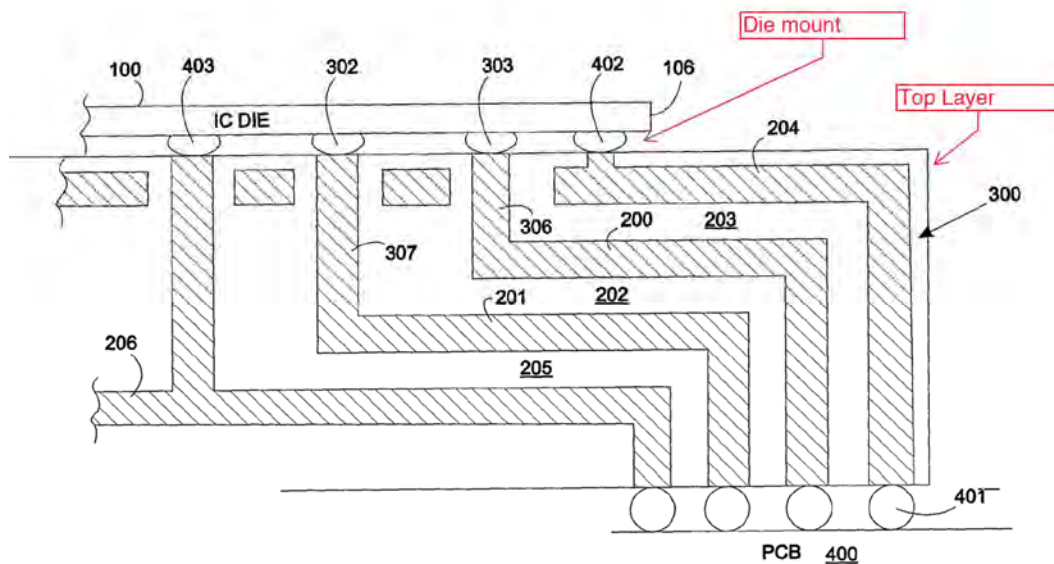
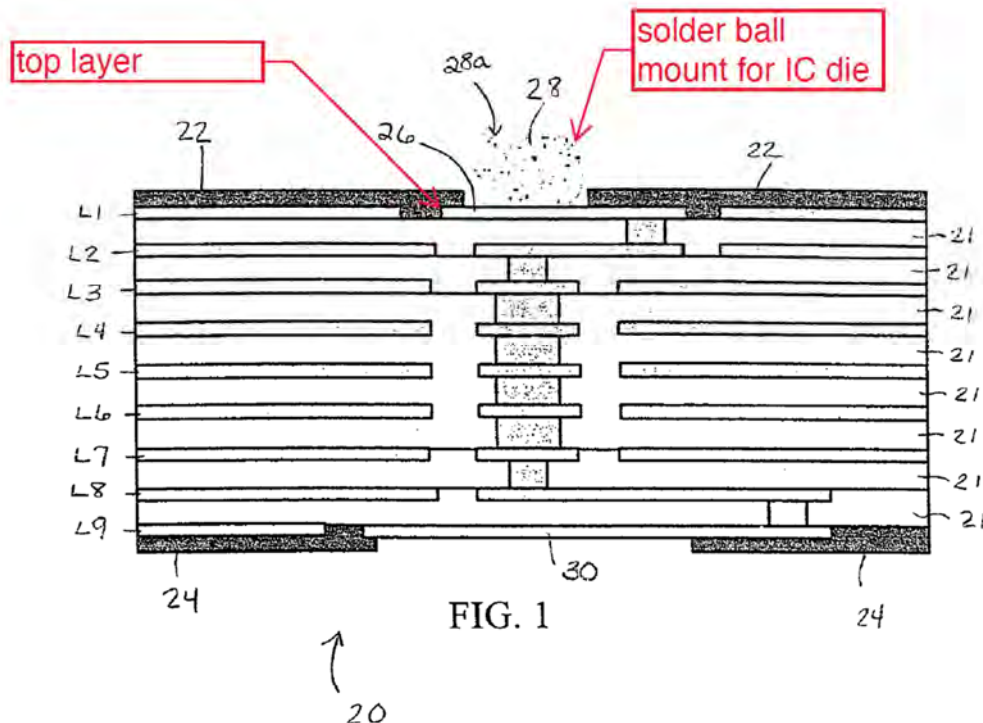


FIG. 4

(Ex. 1005, Fig. 4 annotated)

86. Referring to Figure 4 of Devnani (above) and related text, Devnani discloses a die 100 mounted upon a top layer of the semi-conductor package 300 via balls 302, 303, 402 and 403. (Ex. 1005, ¶0023) Devnani further discloses that balls may be “balls of a conventional ball grid array package”. (*Id.*, ¶0027)

87. I've been asked to assume Devnani does not disclose this claim feature. However, the AAPA does disclose this claim feature. "As an example, FIG. 1 (below) of the '245 patent discloses as prior art a typical multi-layer organic BGA flip chip substrate that uses a 9-layer stackup 20 with a thin core." (Ex. 1001., Fig. 1, 1:26-28) A person of ordinary skill in the art would understand that in BGA packages, the die is mounted to a top layer of the package using solder balls.



(Ex. 1001, Fig. 1 annotated)

B. Ground 2 – Claim 9 is obvious by Devnani in view of AAPA, and further in view of Pillai

88. In my opinion, the combination of Devnani, AAPA and Pillai discloses or suggests each and every element of dependent claim 9.

1. Claim 9

a) “A package as recited in claim 7, wherein said ball pad layer has a plurality of ball pads dispersed thereon and no metal traces on the ball pad layer which are connected to the ball pads.”

89. In my opinion, the Devnani-AAPA-Pillai combination discloses this claim feature. As discussed above in Section X.A.1(d) regarding claim 7, Devnani-AAPA discloses a package with a ball pad layer that has a plurality of ball pads dispersed thereon. Pillai discloses that the ball pad layer does not include metal traces connected to the ball pads as shown in a zoomed in portion of Figure 1 of Pillai below.

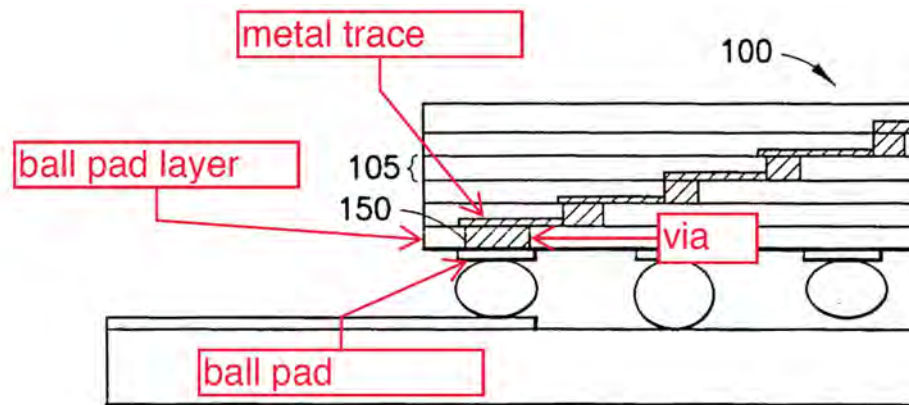


FIG.1

(Ex. 1007, Fig. 1 annotated)

90. A person of ordinary skill in the art implementing the semiconductor package of Devnani-AAPA would have had good reason to look to Pillai as they are all in the same field of IC packages. Moreover, a person of ordinary skill in the art

would have been motivated to combine the teachings of Pillai with the combination of Devnani and AAPA to use vias to connect the balls of the ball pad layer to metal traces of routing layers and NOT have metal traces on the ball pad layer. The use of vias was in widespread use at the time of the '245 patent, and a person of ordinary skill in the art would have been motivated to combine Pillai vias to connect traces with ball pads with Devnani-AAPA semiconductor package as this would reduce potential damage to metal traces of the package during thermal cycling.

C. Ground 3 – Claim 12 is obvious by Devnani in view of AAPA, and further in view of Tanahashi

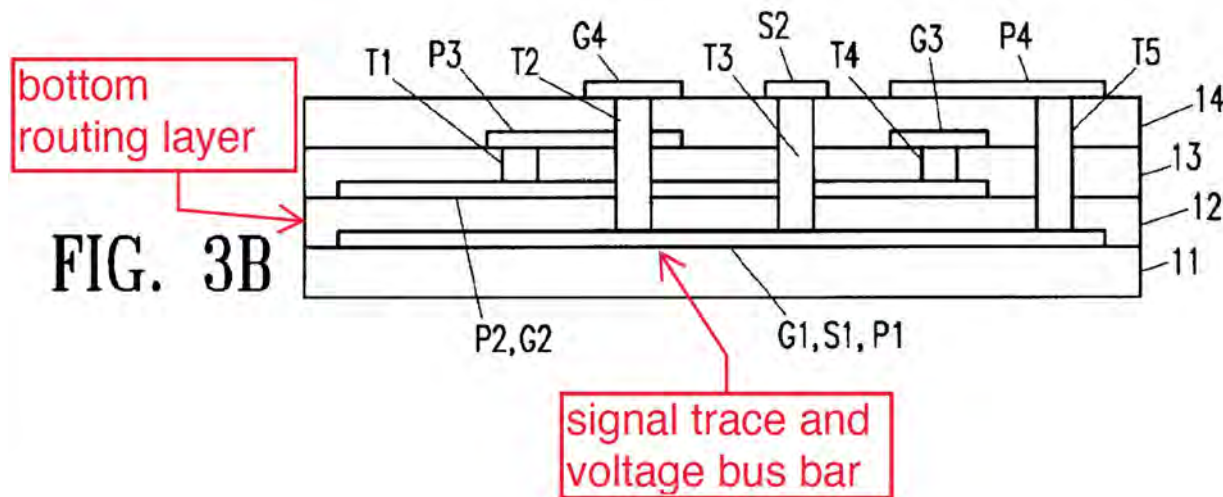
91. In my opinion, the combination of Devnani, AAPA and Tanahashi discloses or suggests each and every element of dependent claim 12.

1. Claim 12

a) “A package as recited in claim 7 wherein the signal traces on the bottom routing layer comprise at least one voltage bus bar.”

92. In my opinion, the combination of Devnani, AAPA and Tanahashi disclose or suggest all features recited in claim 12. The Devnani-AAPA combination discloses a package wherein the signal traces are on a bottom routing layer as discussed above in Sections X.A.1(a)-(c) regarding claim 7.

93. Tanahashi discloses a routing layer including both a signal trace (signal wiring conductor S1) and a voltage bus bar (power wiring conductor P1) on the same layer. (Ex. 1009, 13:28-33)



(*Id.*, Fig. 3B annotated)

94. Tanahashi does not explicitly state that the routing layer, which includes the signal trace and the voltage bus bar, is the “bottom routing layer.” However, as is shown in Figure 3B of Tanahashi, signal trace S1 and a voltage bar P1 are routed on the layer immediately above layer 11 (lowest layer). A person of ordinary skill in the art would understand that the lower layer that included signal traces would be the “bottom routing layer.”

95. A person of ordinary skill in the art implementing the semiconductor package of Devnani-AAPA would have had good reason to look to Tanahashi as they are all directed to multilayer structures on which semiconductor devices are

mounted. A person of ordinary skill in the art would have been motivated to combine Tanahashi's teaching of combining voltage conductors and signal conductors on a single layer with the Devnani-AAPA semiconductor package to provide additional routing flexibility and/or to decrease the number of layers of a semiconductor package.

D. Ground 4 – Claims 1-2 and 4-5 are obvious by Devnani in view of AAPA

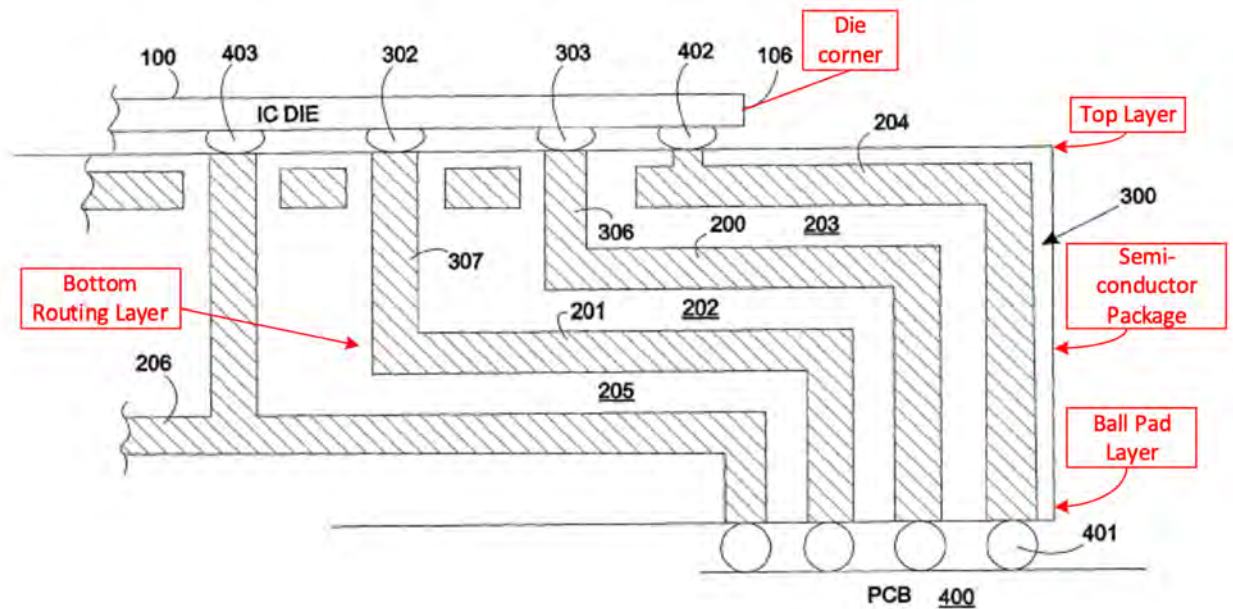
96. In my opinion, Devnani and AAPA disclose or suggest all features recited in claims 1-2 and 4-5. Independent claim 1 is very similar to independent claim 7 and similar arguments are made herein for Ground 4 as were made regarding Ground 1 as discussed in Section X.A.1 through Section X.A.4 above.

1. Claim 1

a) “A semi-conductor package comprising: a top layer having a die mounted thereon, said die having a corner;”

97. I understand that “a semi-conductor package comprising” is the preamble to claim 1 of the '245 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, in my opinion, Devnani discloses this claim feature.

98. Figure 4 of Devnani (below) discloses a semi-conductor package 300. (Ex. 1005, ¶0023) Devnani further discloses an IC die 100 mounted upon a top layer of the semi-conductor package 300 and the die 100 has a die edge 106 (*Id.*, ¶¶0022;-0023) A person of ordinary skill in the art would understand the die edge would include a corner.



(*Id.*, Fig. 4 annotated)

b) “a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces thereon,”

99. In my opinion, Devnani and AAPA discloses this claim feature. Figure 4 of Devnani, shown below, discloses “a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces thereon”. (Ex. 1005, ¶0023) As shown in Figure 4 of Devnani below, Devnani discloses a plurality of layers in an IC package (*Id.*, ¶0005) and also shows a layer for routing

signals (e.g., signal 201) that is lower than other layers of the IC package. (*Id.*, ¶0005; 0025; Claim 1)

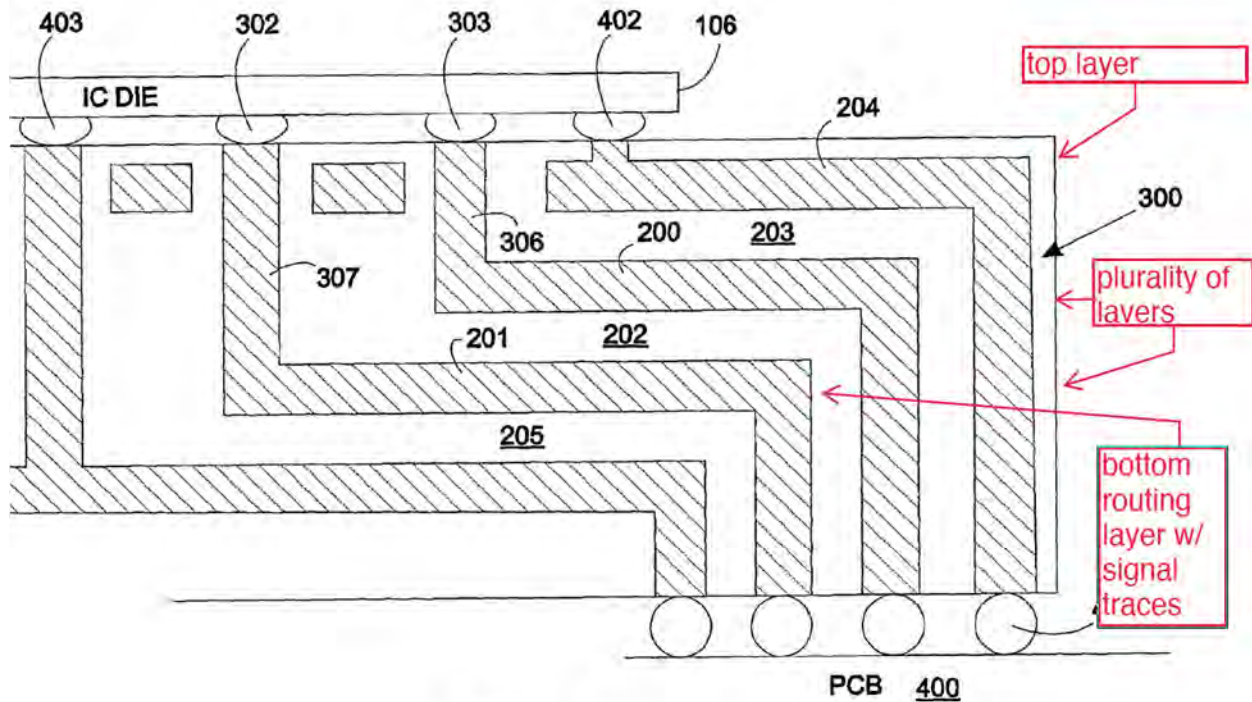


FIG. 4

(*Id.*, Fig. 4 annotated)

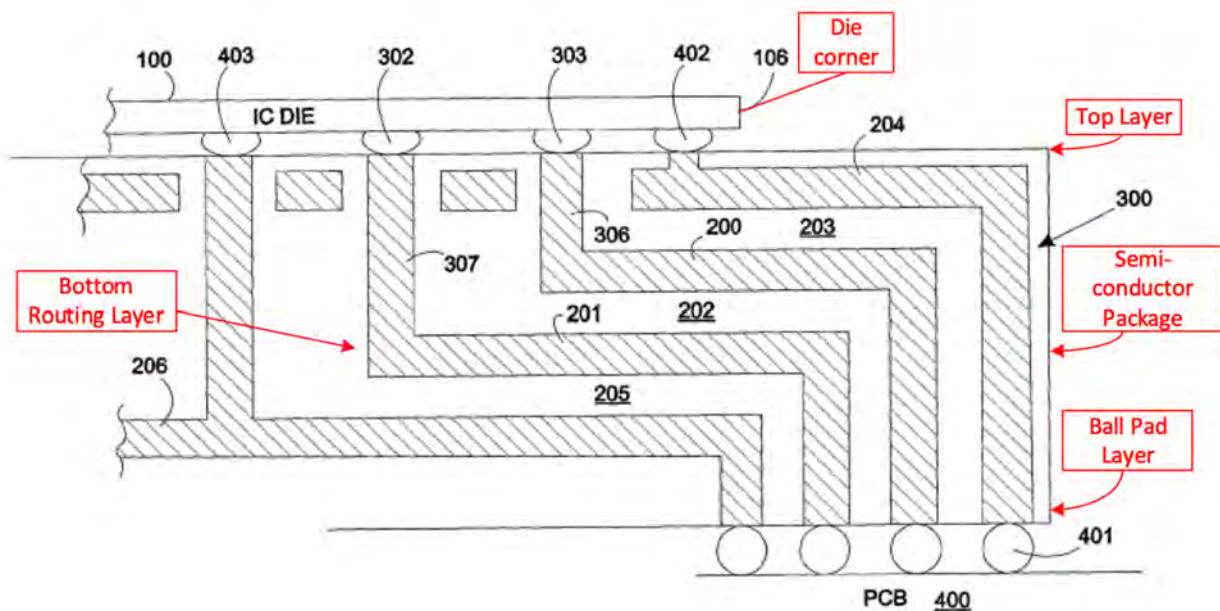
100. A person of ordinary skill in the art would understand that a “bottom routing layer” would be a routing layer beneath another layer of the IC package.

101. I’ve been asked to assume scenario where Devnani does not disclose this feature. In this scenario, AAPA discloses “signals are typically routed directly over the ball pads under the die corner on **the bottom routing layer**” (Ex. 1001, 1:24-26) and further discloses “a typical multi-layer organic BGA flip chip substrate

that uses a 9-layer stackup”. (*Id.*, 1:27-29). As such, AAPA discloses a plurality of layers under a top layer (e.g., layers 2-9 of the 9-layers) and that signal traces are on a bottom routing layer. Thus, in my opinion, both Devnani and AAPA discloses this claim feature.

c) “and a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads,”

102. In my opinion, Devnani and AAPA discloses this claim feature. Figure 4 of Devnani, shown below, and related text discloses a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads 401 dispersed thereon. (Ex. 1005, ¶0023)



(*Id.*, Fig. 4 annotated)

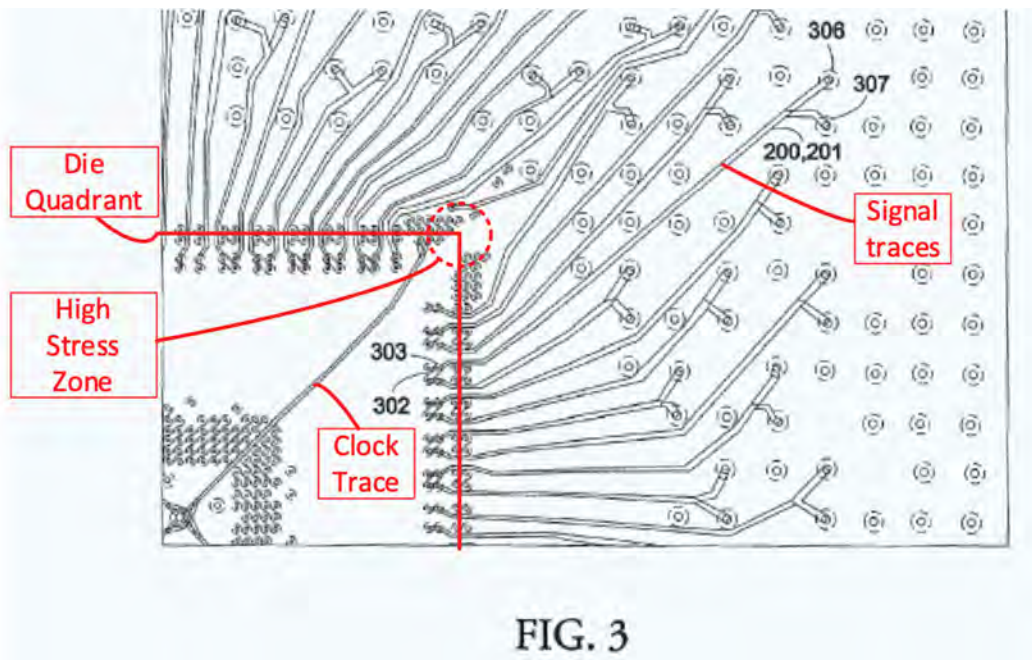
103. I’ve been asked to assume that Devnani does not disclose this feature. In this scenario, AAPA discloses “The 9-layer stackup 20 includes a layer L1, a layer

L2, a layer L3, a layer L4, a layer L5, a layer L6, a layer L7, a layer L8, and a layer L9....An upper protective mask 22 is provided proximate layer L1 and a lower protective layer 24 is provided proximate layer L9.” (Ex. 1001, 1:28-35) AAPA further discloses that “A plurality of ball pads 30 (one of which is shown) are provided on Layer L9.” AAPA further discloses that “the signal traces 36 of layer L8 are routed over the ball pads 34 of layer L9”. (*Id.*, 1:57-58)

As such, AAPA is disclosing a ball pad layer (L9) is under the bottom routing layer (L8) and that a plurality of ball pads (ball pads 34) are dispersed thereon.

d) “wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die.”

104. In my opinion, the combination of Devnani-AAPA disclose this claim feature. Figure 3 of Devnani (shown below) is annotated to illustrate where a die quadrant resides when the IC die is mounted upon the package 300 and to identify the high stress zone associated with the corner of the die. As is shown in Figure 3 of Devnani, signal traces 200 of the bottom routing layer are routed from edges of the die and around the high stress zone associated with the die corner.



(Ex. 1005, Fig. 3 annotated)

105. This feature of Devnani shows all signal traces 200 of the bottom routing layer being routed away from the high stress zone. With all signal traces of Devnani routed away from the high stress zone, “none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer” within the high stress area near the corner of the die. However, Devnani does not explicitly disclose that high stress area is defined by “two ball pad pitches of the corner of the die.” However, AAPA renders this claim feature obvious.

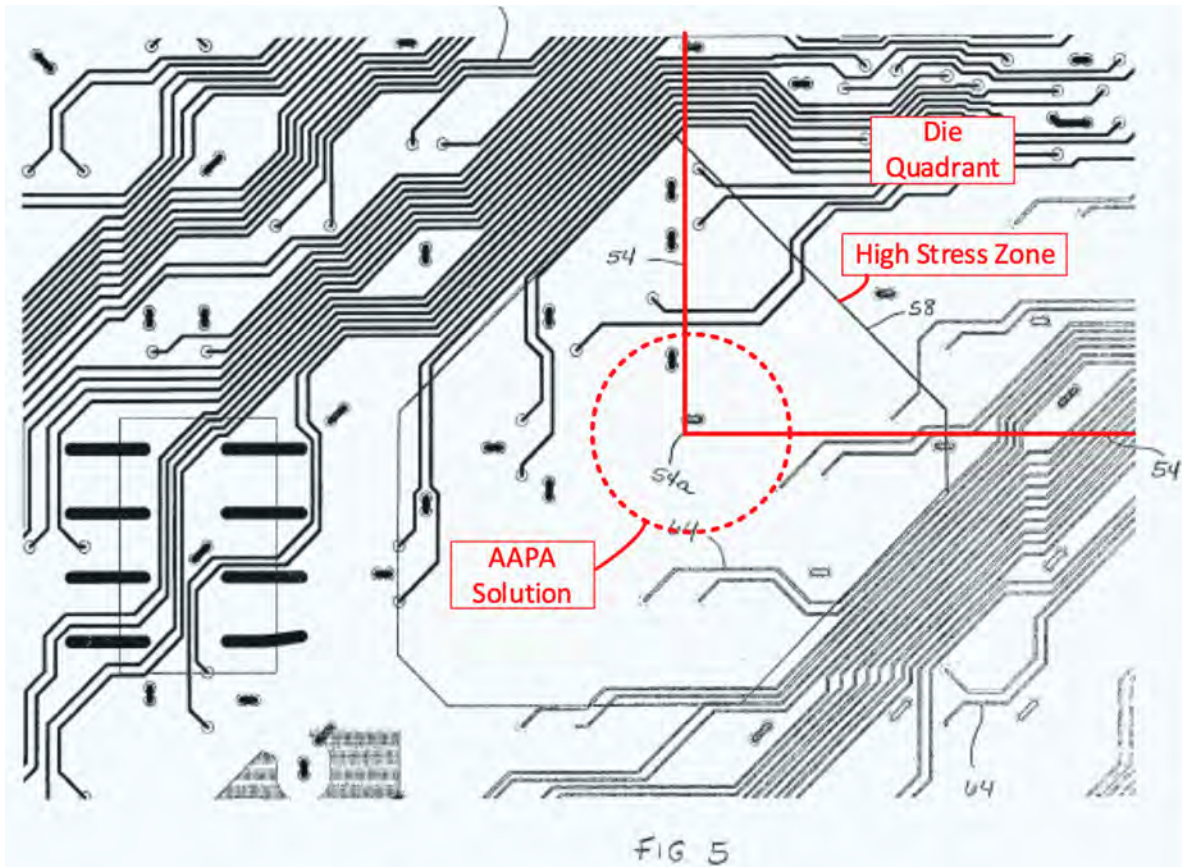
106. AAPA Figure 3 of the ‘245 patent and its accompanying description discloses an existing, *i.e.*, prior art, solution (AAPA Solution) used to **prevent stress cracks in traces** is by routing the traces on the bottom routing layer outside a high stress zone associated with the corner of the die. Thus, the AAPA Solution is one

existing solution of defining the high stress zone as being a circular area having a radius of 1 mm around the corner of the die.

107. In particular, AAPA states that “Another existing solution to overcoming this problem is to define a circular shaped area with a one (1) millimeter radius using placement of the die corner 38a as the center of the circle. **When routing traces on layer L8, traces are not routed within this circular region.**”) (*Id.*, 2:6-11, emphasis added)

108. Figure 5 of the '245 patent (AAPA annotated), presented below, includes the AAPA Solution overlaid on the high stress zone solution purported by the '245 patent. The AAPA Solution defines the area of increased stress as a circle centered on the corner of the die. The only differences in the areas between the AAPA Solution and the high stress zone solution of the '245 patent illustrated in Figure 5 of the '245 patent are differing respective sizes and shapes--the shape and size of the circle of the AAPA Solution as compared to the shape and size of the die high stress zone 58. However, a POSITA would have known that the die corner and the underlying solder balls near the die corner would be high stress points as shown by numerous references. (See Section VIII above regarding the prior art) Thus, a POSITA would have been motivated to define an area sufficient in size such that traces would not crack due to thermal cycling and would have been motivated to

move traces from under ball pads (great stress areas) for the same reason the AAPA moved traces from a 1mm circular from the corner of the die (great stress area).



(*Id.*, Fig. 5 annotated)

109. This POSITA solution is partly illustrated in Figure 5 (below) of the '245 patent, a POSITA solution overlays the solution of the '245 patent (routing signal traces outside of the die high stress zone). The only difference between the AAPA Solution and the POSITA Solution is the size of the circle, both of which are centered on the die corner 54a, and routing traces from high stress points (corner of

die and underlying solder balls). This POSITA Solution is nearly identical to the high stress zone solution of Figure 5. The shape of the area of increased stress presented in Figure 5 of '245 patent differs from the circular POSITA Solution only in its shape.

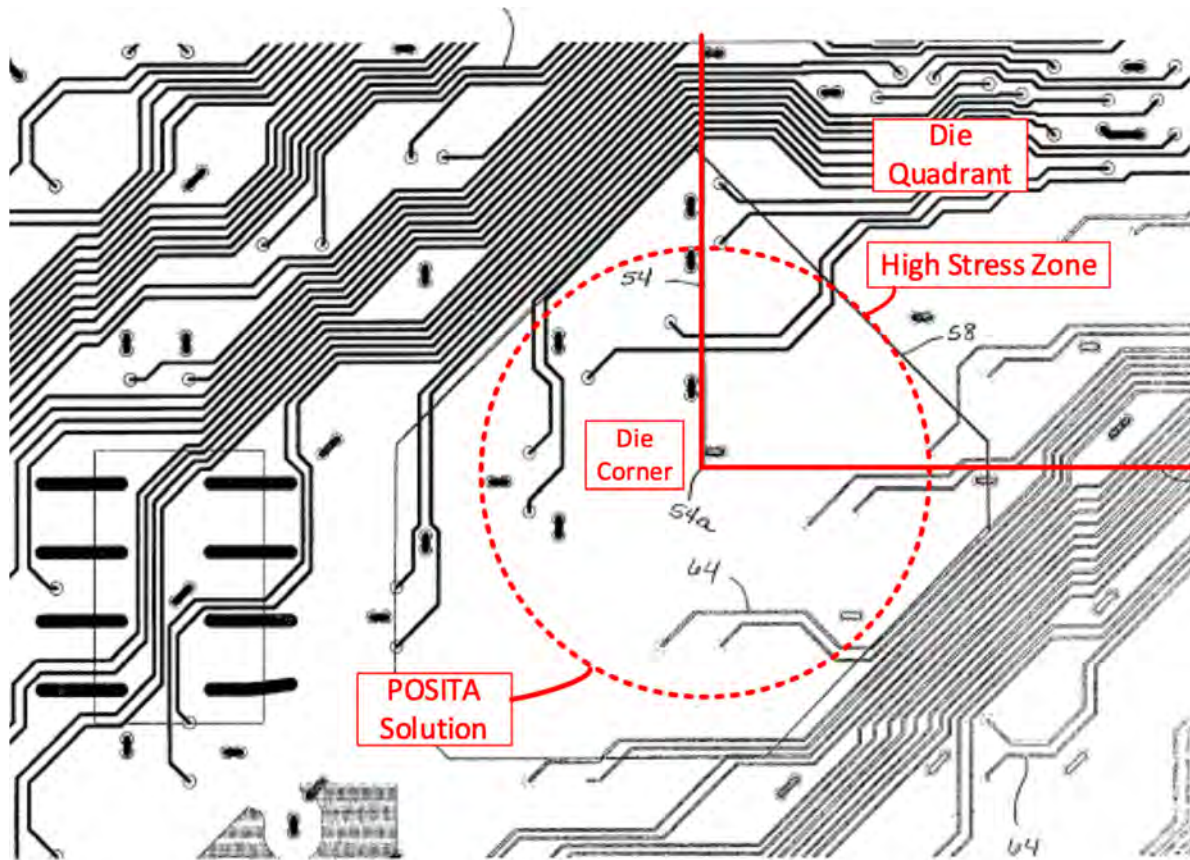


FIG 5

(Id., Fig. 5 annotated)

110. Claim 1 does not require a particular shape of a high stress zone, only that “none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die.” (Ex. 1001, Claim 1)

111. A person of ordinary skill in the art would have been motivated to use a larger area--e.g., an area with **a diameter 2 ball pad pitches from the corner of the die**, rather than a smaller circle with a 1 mm radius, to decrease risk of cracks in signal traces during thermal cycling of the semiconductor package and further would have been motivated to move traces from under ball pads near corner of die (high stress points) for the same reason the AAPA solution moved traces from the corner of a die (high stress area). Simply using a larger area (high stress zone) within which to exclude signal traces uses an admittedly known technique to achieve an admittedly known result, namely a reduction in failures due to trace cracks under thermal cycling.

112. A person of ordinary skill in the art would take note that there is no specific disclosure in the '245 patent regarding any advantages, criticality, or unexpected results related to the specific selection of the shape or size of the high stress zone. Thus, a person of ordinary skill in the art would naturally select any size or shaped area that the designer believed would result in reducing failures due to trace cracks. As such, a person of ordinary skill in the art would have anticipated success in reducing the number of stress cracks in signal traces by routing signal traces around a larger area than 1 mm from the corner of the die, such area defined by 2 ball pad pitches from the corner of the die, and around other stress points such as ball pads near the die corner.

2. Claim 2

a) “A package as recited in claim 1, wherein none of the signal traces of the bottom routing layer are located within two ball pad pitches of the corner of the die.”

113. In my opinion, the combination of Devnani-AAPA discloses this claim feature as discussed above in Section X.D.1(d) regarding claim 1. As discussed above, Devnani-AAPA would lead a person of ordinary skill in the art to route traces of a bottom routing layer away from a high stress area (e.g., corner of a die).

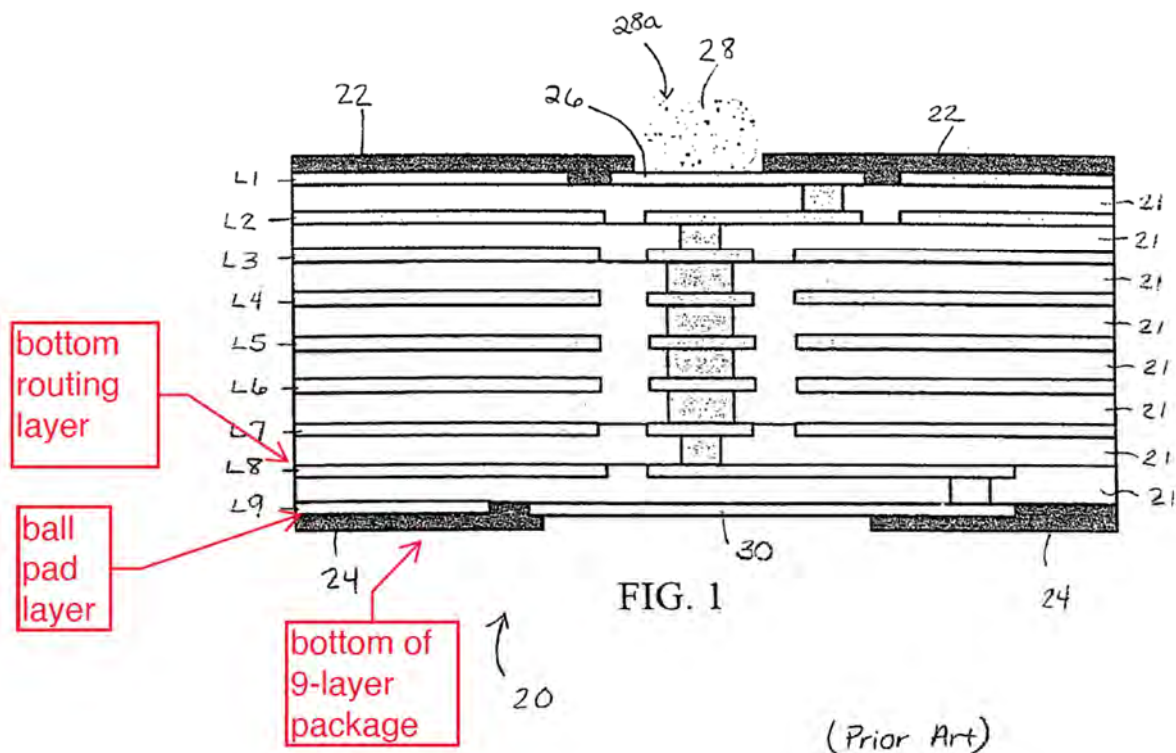
114. As discussed above, numerous references disclose that stress from the corner of the die and ball pad area could cause cracking. (see generally Ex. 1010, Ex. 1011, Ex. 1016; Ex. 1017; AAPA) As such, a person of ordinary skill in the art would be motivated to define the contours of the AAPA's high stress area to route Devnani's traces away from this area to reduce track cracking and this area would include a distance of two ball pad pitches.

3. Claim 4

a) “A package as recited in claim 1, wherein the package comprises nine layers with the routing layer being the eighth layer and the ball pad layer being the ninth layer, on a bottom of the package.”

115. In my opinion, the combination of Devnani-AAPA discloses this claim feature. See Section X.A.3(a) above regarding claim 10.

116. Figure 1 of the '245 patent (below) shows a prior art IC package with 9 layers, with a bottom routing layer on layer 8 and a ball pad layer on layer 9. A person of ordinary skill in the art would have been motivated to combine the AAPA 9-layer stackup 20 with the package 30 of Devnani to route signals, power, and ground between a die and a PCB as was widely known in the art.



(Ex. 1001, Fig. 1)

4. Claim 5

a) “A package as recited in claim 1, wherein the die is mounted to the top layer in an arrangement other than a pin connection.”

117. In my opinion, Devnani and AAPA discloses this claim feature. See Section X.A.4(a) above regarding claim 11.

118. Devnani discloses the additional element of claim 11, “wherein the die is mounted to the top layer in an arrangement other than a pin connection.”

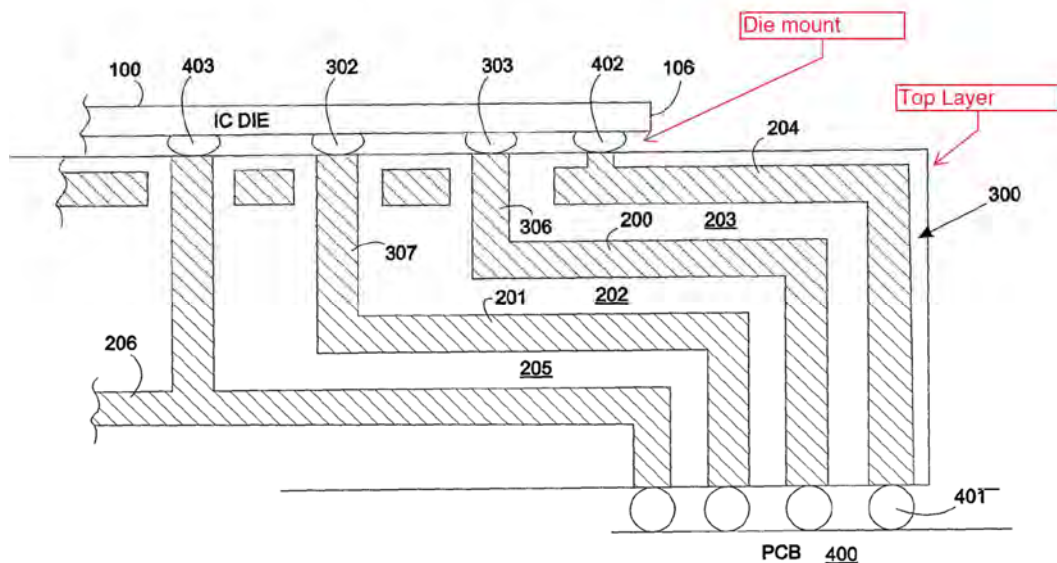
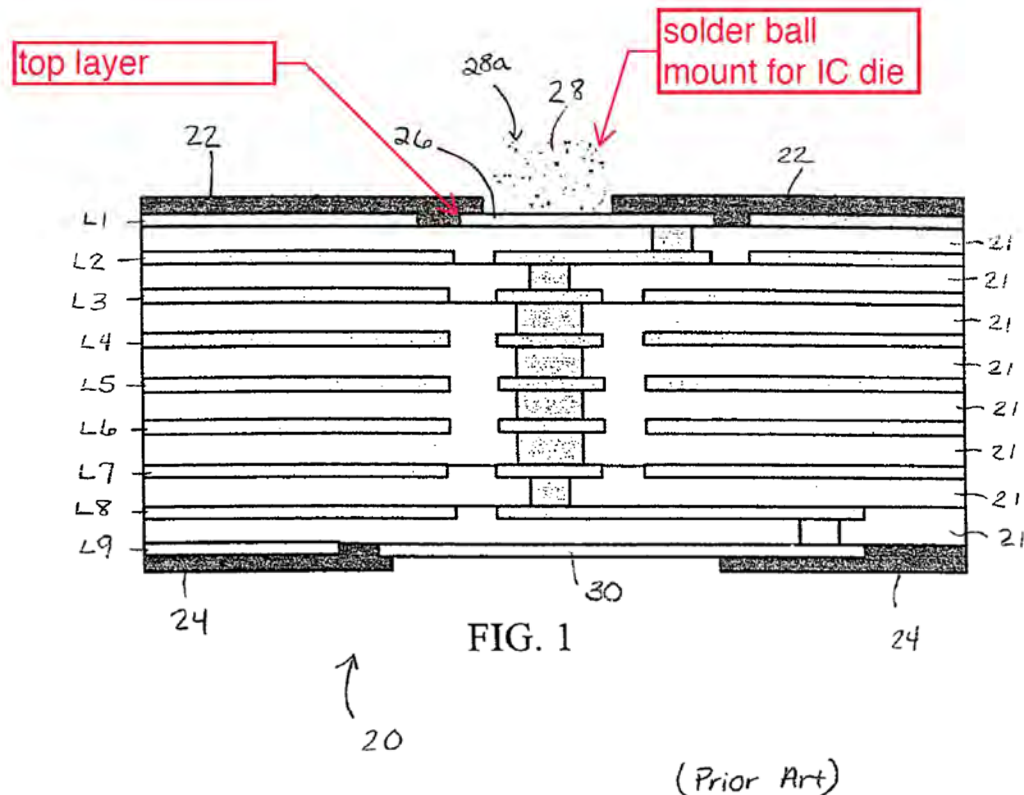


FIG. 4

(Ex. 1005, Fig. 4 annotated)

119. Referring to Figure 4 of Devnani (above) and related text, Devnani discloses a die 100 mounted upon a top layer of the semi-conductor package 300 via balls 302, 303, 402 and 403. (Ex. 1005, ¶0023) Devnani further discloses that balls may be “balls of a conventional ball grid array package”. (*Id.*, ¶0027) A person of ordinary skill in the art would understand that a ball grid array package uses solder balls to mount a die to a top layer of a package substrate.

120. AAPA also discloses this claim feature. “As an example, FIG. 1 (below) of the '245 patent discloses as prior art a typical multi-layer organic BGA flip chip substrate that uses a 9-layer stackup 20 with a thin core.” (Ex. 1001., 1:26-28)



(Ex. 1001, Fig. 1 annotated)

E. Ground 5 – Claim 3 is obvious by Devnani in view of AAPA, and further in view of Pillai

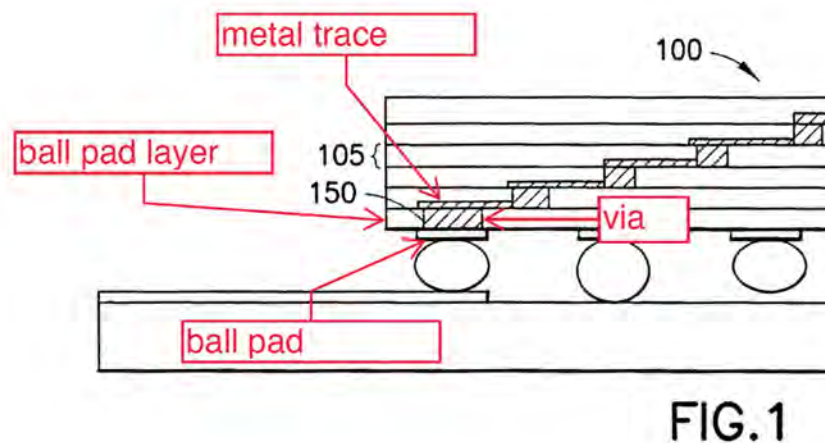
121. In my opinion, the Devnani-AAPA-Pillai combination discloses or suggests each and every element of dependent claim 3. See Section X.B.1(a) above.

1. Claim 3

a) “A package as recited in claim 1, wherein said ball pad layer has a plurality of ball pads dispersed thereon and no

metal traces on the ball pad layer which are connected to the ball pads.”

122. In my opinion, the Devnani-AAPA-Pillai combination discloses this claim feature. As discussed above in Section X.B.1 regarding claim 9, Devnani-AAPA discloses a package with a ball pad layer that has a plurality of ball pads dispersed thereon. Pillai discloses that the ball pad layer does not include metal traces connected to the ball pads as shown in a zoomed in portion of Figure 1 of Pillai below.



(Ex. 1007, Fig. 1 annotated)

123. A person of ordinary skill in the art implementing the semiconductor package of Devnani-AAPA would have had good reason to look to Pillai as they are all in the same field of IC packages. Moreover, a person of ordinary skill in the art would have been motivated to combine the teachings of Pillai with the combination of Devnani and AAPA to use vias to connect the balls of the ball pad layer to metal traces of routing layers and NOT have metal traces on the ball pad layer. The use of

vias was in widespread use at the time of the '245 patent, and a person of ordinary skill in the art would have been motivated to combine Pillai vias to connect traces with ball pads with Devnani-AAPA semiconductor package as this would reduce potential damage to metal traces of the package during thermal cycling.

F. Ground 6 – Claim 6 is obvious by Devnani in view of AAPA, and further in view of Tanahashi

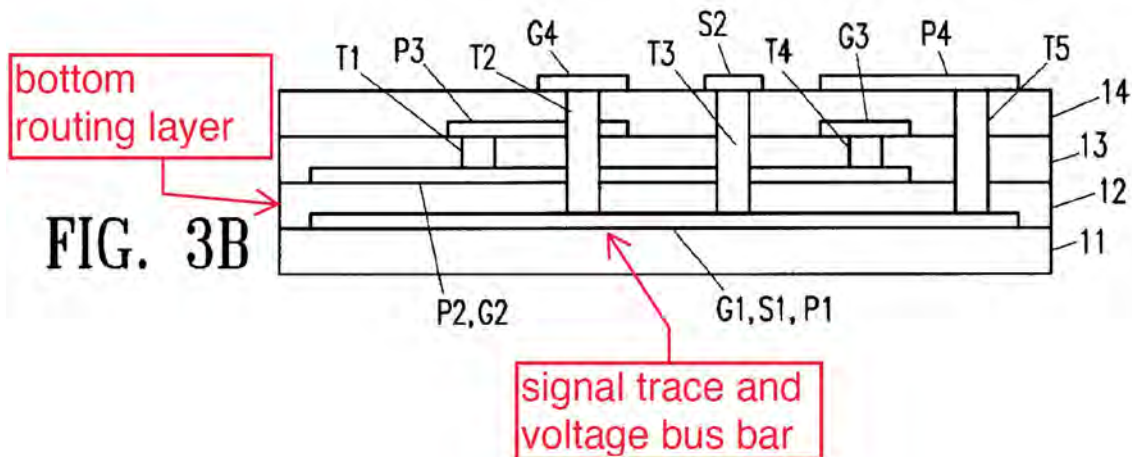
124. In my opinion, the combination of Devnani, AAPA and Tanahashi discloses or suggests each and every element of dependent claim 6.

1. Claim 6

a) “A package as recited in claim 1, wherein the signal traces on the bottom routing layer comprise at least one voltage bus bar.”

125. The Devnani-AAPA combination discloses a package wherein the signal traces are on a bottom routing layer as discussed above in Sections X.A.1(a)-(c) regarding claim 7.

126. Tanahashi discloses, in Figure 3B below, a routing layer including both a signal trace (signal wiring conductor S1) and a voltage bus bar (power wiring conductor P1) on the same layer. (Ex. 1009, 13:28-33)



(*Id.*, Fig. 3B annotated)

127. Tanahashi does not explicitly state that the routing layer, which includes the signal trace and the voltage bus bar, is the “bottom routing layer.” However, as is shown in Figure 3B of Tanahashi, signal trace S1 and a voltage bar P1 are routed on the layer immediately above layer 11 (lowest layer). A person of ordinary skill in the art would understand that the lower layer that included signal traces would be the “bottom routing layer.”

128. A person of ordinary skill in the art implementing the semiconductor package of Devnani-AAPA would have had good reason to look to Tanahashi as they are all directed to multilayer structures on which semiconductor devices are mounted. A person of ordinary skill in the art would have been motivated to combine Tanahashi’s teaching of combining voltage conductors and signal conductors on a single layer with the Devnani-AAPA semiconductor package to provide additional

routing flexibility and/or to decrease the number of layers of a semiconductor package.

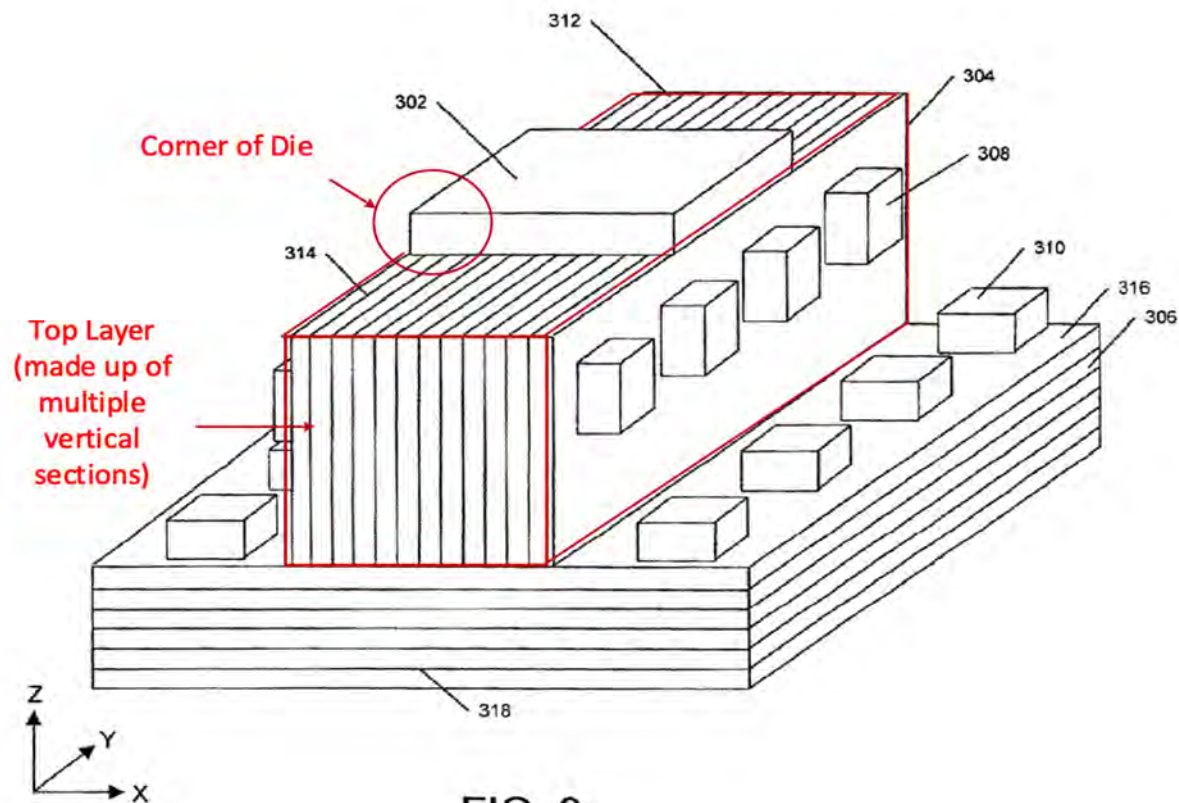
G. Ground 7 – Claims 1, 2 and 5 are obvious by Chung in view of Celeron

129. In my opinion, the combination of Chung and Celeron discloses or suggests each and every element of dependent claims 1, 2 and 5.

1. Claim 1

a) “A semi-conductor package comprising a top layer having a die mounted thereon, said die having a corner;”

130. Chung discloses a semi-conductor package having a top layer having a die mounted thereon, where the die has a corner as shown below in Figure 3. Figure 3 also shows vertical package section 304, which is made up of multiple vertically arranged portions, that corresponds to the claimed top layer of the semiconductor package. “FIG. 3 illustrates a three-dimensional view of an electrical assembly in accordance with one embodiment of the present invention. The electrical assembly includes an integrated circuit 302 (IC) and an IC package consisting of a vertical package section 304 and a horizontal package section 306.” (Ex. 1006, ¶0027)



(*Id.*, Fig. 3 annotated)

b) “a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces thereon”

131. Chung in Figure 3 (above) illustrates a plurality of layers under the top layer. “Horizontal section 306 includes multiple layers of conductive materials separated by multiple layers of dielectric materials.” (*Id.*, ¶0037)

132. Figure 5 of Chung, reproduced below in an annotated form, illustrates that the plurality of layers includes a bottom routing layer, which can include traces used to route signals, power, and ground. “Each of these conductive layers 540, 542,

544 could include planar conductive areas and/or traces.” (*Id.*, ¶0050 [emphasis added]) “The function of the horizontal section 306 is to carry I/O signals, power, and ground between the next level of interconnect and vertical section 304.” (*Id.*, ¶0038)

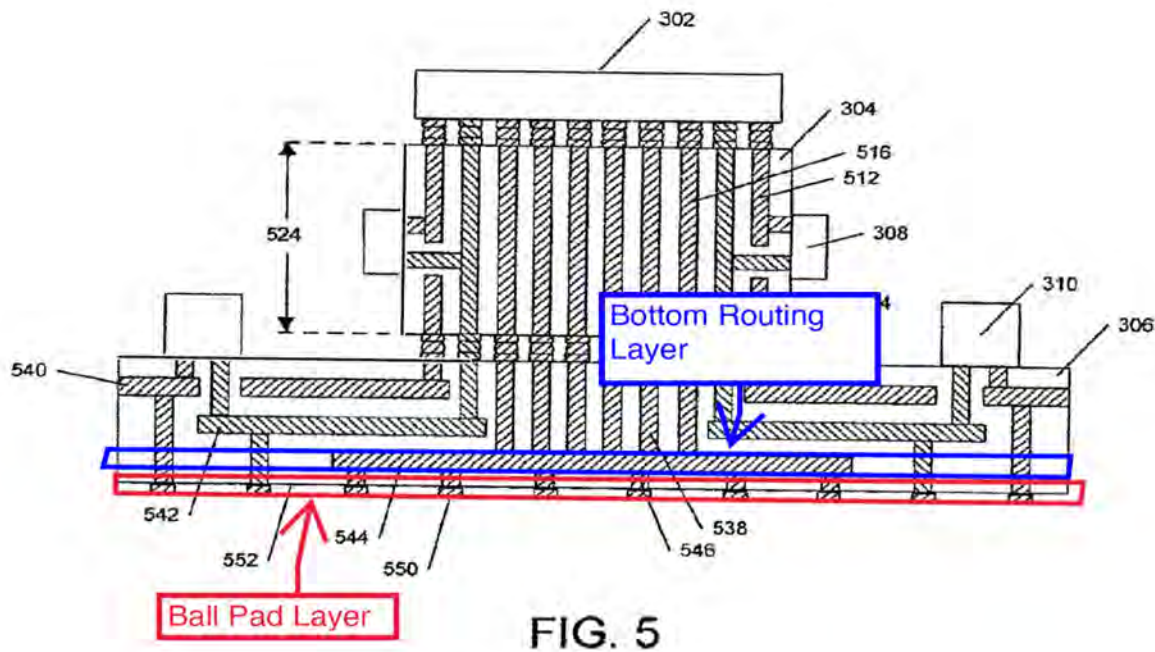


FIG. 5

(*Id.*, Fig. 5 annotated)

c) “a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads”

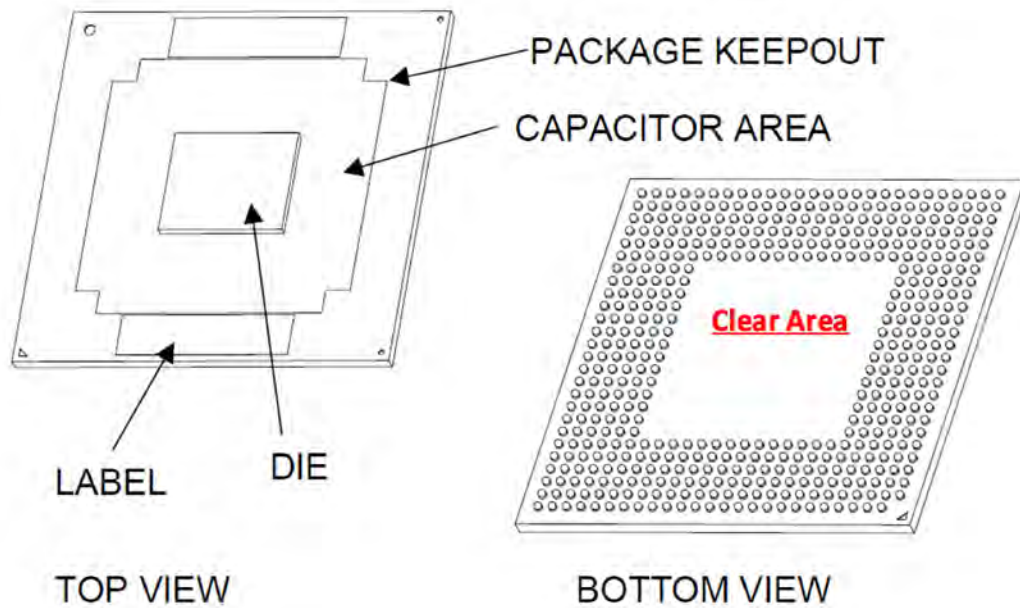
133. Chung includes a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads as shown by bond pads 550 in Figure 5 above being on the ball pad layer. Chung further discloses that “Along with vias 538, 546, conductive layers 540, 542, 544 electrically connect the set of top surface bond pads with a set of connectors (e.g., bond pads 550 or pins) on the bottom surface 552

of horizontal section 306.”. (Ex. 1006, ¶0050) As such, a person of ordinary skill in the art would have understood Chung’s bond pads on the bottom surface of the horizontal section correspond to the ball pad layer of claim 1.

d) “wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die.”

134. Chung does not explicitly show that “none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die” required by the last element of claim 1.

135. However, Celeron, in the same field of endeavor, discloses a clear area (shown in Figure 28 below) on the bottom of a BGA package where there are no solder balls (Ex. 1008, p. 69-72)



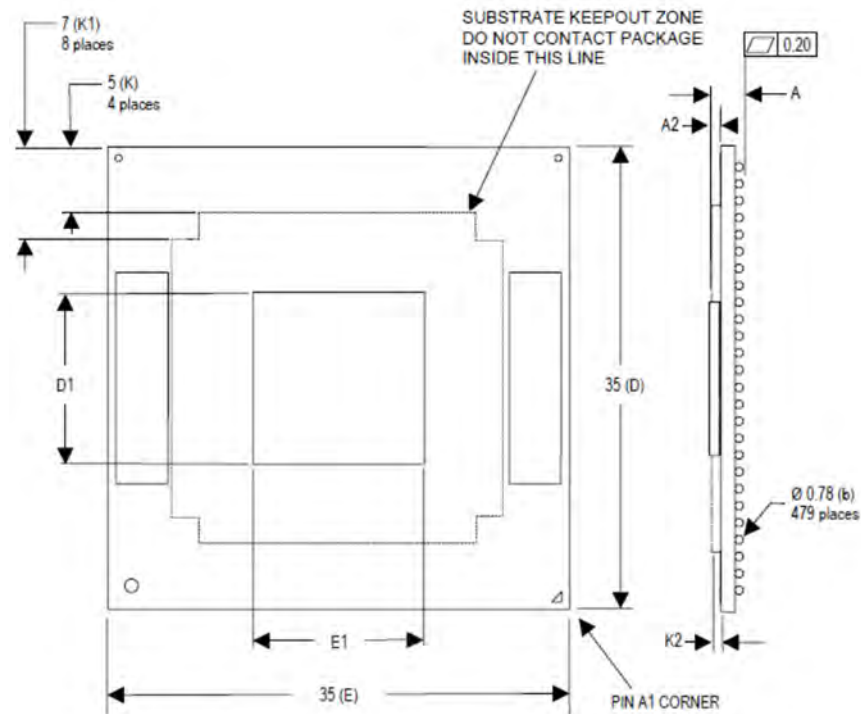
(*Id.*, Fig. 28 annotated)

136. Celeron further discloses dimensions for the ball pad pitch, die size, package size, and other elements along with specific values given in Table 44 that can be mapped to Figures 29 and 30, below. (Ex. 1008, p. 69)

Table 44. Micro-FCBGA Package Mechanical Specifications

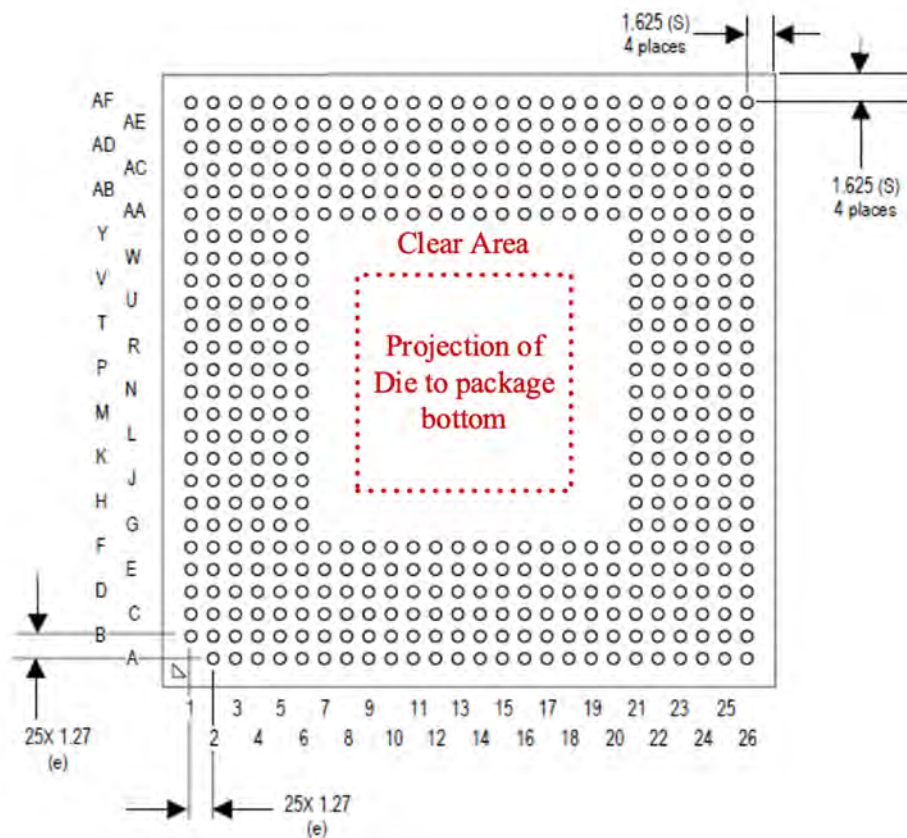
Symbol	Parameter	Min	Max	Unit
A	Overall height, as delivered (1)	2.27	2.77	mm
A2	Die height	0.854		mm
b	Ball diameter	0.78		mm
D	Package substrate length	34.9	35.1	mm
E	Package substrate width	34.9	35.1	mm
D1	Die length	11.18 ³ 10.82 ⁴		mm
E1	Die width	7.20 ³ 6.85 ⁴		mm
e	Ball pitch	1.27		mm
N	Ball count	479		each
K	Keep-out outline from edge of package	5		mm
K1	Keep-out outline at corner of package	7		mm
K2	Capacitor keep-out height	-	0.7	mm
S	Package edge to first ball center	1.625		mm
--	Solder ball coplanarity	0.2		mm
Pdie	Allowable pressure on the die for thermal solution	-	689	kPa
W	Package weight	4.5		g

(Id., Table 44)



(Id., Fig. 29)

137. As illustrated by Celeron in Figure 30 below, the ball pad pitch is approximately 1.27 mm. (Ex. 1008, Fig. 30 (dimension e), Table 44 (dimension e)). Celeron discloses that the largest edge of the largest die is 11.18 mm long and the die is centered in the semiconductor package, which has a minimum length of 34.9 mm. (Ex. 1008, Table 44 (dimensions D, E, D1, E1)). The closest that any of the four corners of the die is located in relation to the edge of the clear zone, which is clear of ball pads, is 3.10 mm, which is greater than two ball pad pitches.



(Id., Fig. 30 annotated)

138. The edge of the clear zone (the area devoid of ball pads) is 8.76 mm from each package edge. (*Id.*, Fig. 30 (dimensions S, e, and b), Table 44 (dimensions S, e, and b) (dimensions $S (1.625) + 5 \times e (1.27) + b (.78)$) Celeron discloses that the largest die is 11.18 mm long. (Ex. 1008., Fig. 29 (dimension D1), Table 44 (dimension D1)). *Celeron* further discloses that the die is centered on top of the semiconductor package. (Ex. 1008, Figs. 28, 29) The nominal distance from the center of the minimum length package to its edge is 17.45 mm. (*Id.*, (dimension D/2)).

139. Celeron also discloses that the distance from the center of the package to the edge of the largest die positioned at the center of the package is 5.59 mm. (*Id.*, (dimension D1/2)). Thus, the distance from the edge of the package to the edge of the largest die is 11.86 mm. (*Id.*, (D/2 – D1/2)). The edge of the clear zone is 8.78 mm, making the distance from the edge of the die going to the edge of the clear zone being 3.10 mm, which is greater than 2.54 mm (two ball pad pitches).

140. Thus, *Celeron*, discloses that there are no ball pads on the ball pad layer “disposed in an area within two ball pad pitches of the corner of the die.” Because there are no ball pads “disposed in an area within two ball pad pitches of the corner of the die, there can be no “signal traces of the bottom routing layer [that] are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die,” as recited by claim 1.

141. A person of ordinary skill in the art implementing the IC package of Chung would have had good reasons to look to Celeron as they both are in the same field of IC packages. Moreover, it would be straightforward for such a person to implement the clear area of Celeron in Chung's IC package as Celeron's clear area would not change function when implemented in Chung's package. A person of ordinary skill in the art would have been motivated to combine the multiple routing layers of Chung with the clear area of Celeron to prevent damage to signal traces of the bottom routing layer during thermal cycling.

2. Claim 2

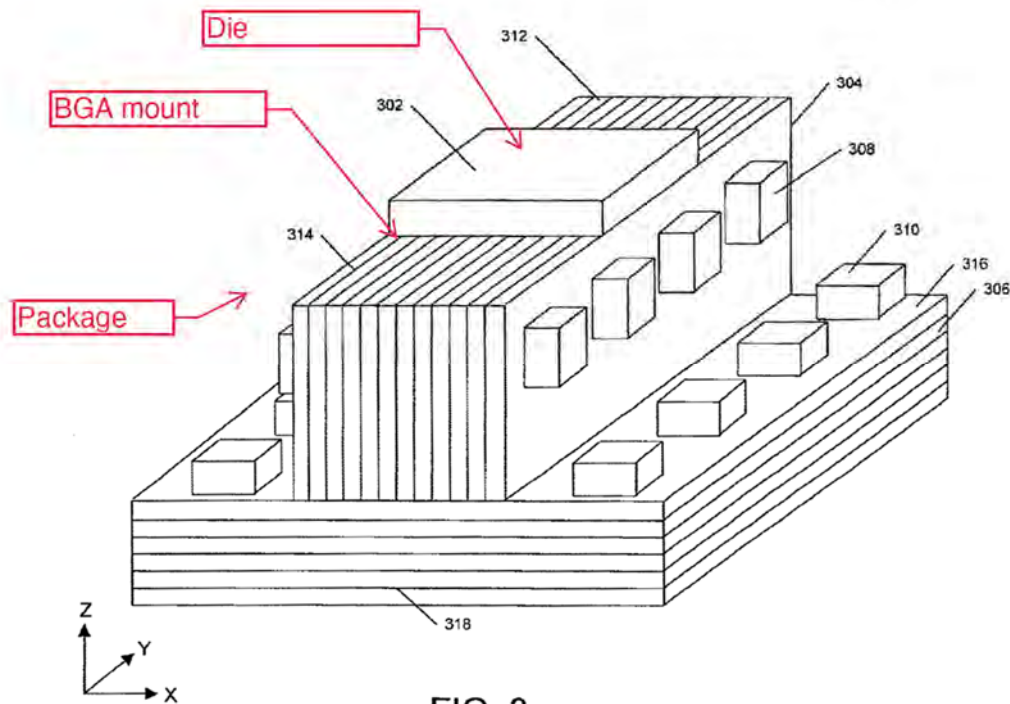
a) "A package as recited in claim 1, wherein none of the signal traces of the bottom routing layer are located within two ball pad pitches of the corner of the die."

142. The Celeron-Chung combination discloses a semiconductor package with a bottom routing layer and no ball pads within two ball pad pitches of the corner of the die as discussed above in Section X.G.1 regarding claim 1. The additional negative element of removing ball pads within the area two ball pad pitches from the corner of the die is disclosed as discussed above because the Chung-Celeron combination discloses no solder balls within two ball pad pitches from the corner of the die.

3. Claim 5

a) A package as recited in claim 1, wherein the die is mounted to the top layer in an arrangement other than a pin connection.

143. Chung in Figure 3 shows an integrated circuit 302 (IC) and an IC package consisting of a vertical package section 304 and a horizontal package section 306.” (Ex. 1006, ¶0027)



(*Id.*, Fig. 3 annotated)

144. Chung discloses, “a die mounted to the top layer of a semiconductor package in an arrangement other than a pin connection.” “[T]he chip is flipped over and attached, via solder bumps or balls to matching pads on the top surface 312 of the vertical section 304.” (*Id.*, ¶0028) Solder bumps or balls are used with ball grid

array (BGA) packages, which were in widespread use prior to the invention of the '245 patent as shown in number references outlined in Section VIII above.

H. Ground 8 – Claim 3 is obvious by Chung in view of Celeron, and further in view of Pillai

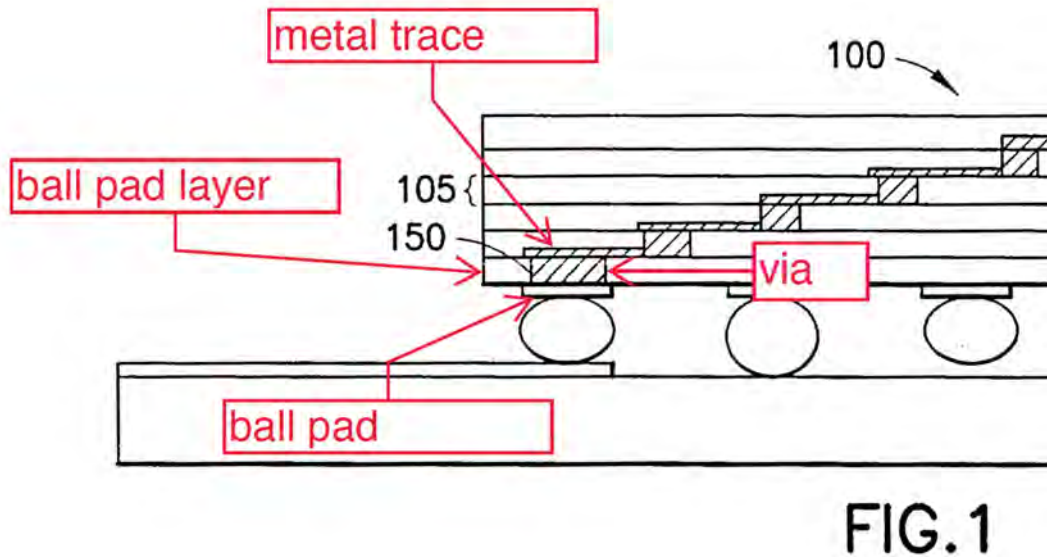
145. In my opinion, the combination of Chung, Celeron and Pillai discloses or suggests each and every element of dependent claim 3.

1. Claim 3

a) “A package as recited in claim 1, wherein said ball pad layer has a plurality of ball pads dispersed thereon and no metal traces on the ball pad layer which are connected to the ball pads.”

146. The Chung-Celeron combination discloses an IC package with a ball pad layer having a plurality of ball pads as discussed above in Section X.G.1 regarding claim 7. Pillai discloses no metal traces being on the ball pad layer as discussed above in Section X.B.1 regarding claim 9.

147. For convenience, Figure 1 of Pillai is reproduced below and illustrates that the ball pad layer does not include metal traces connected to the ball pads.



(*Id.*, Fig. 1 annotated)

148. A person of ordinary skill in the art implementing the IC package of Chung-Celeron would have had good reason to look to Pillai as they are all in the same field of IC packaging. A person of ordinary skill in the art would have been motivated to combine the teachings of Pillai with the combination of Chung and Celeron to use vias to connect the balls of the ball pad layer to metal traces of routing layers and NOT have metal traces on the ball pad layer. The motivation to combine would be due to reduced potential damage to metal traces of the package during thermal cycling.

I. Ground 9 – Claim 4 is obvious by Chung in view of Celeron, and further in view of AAPA

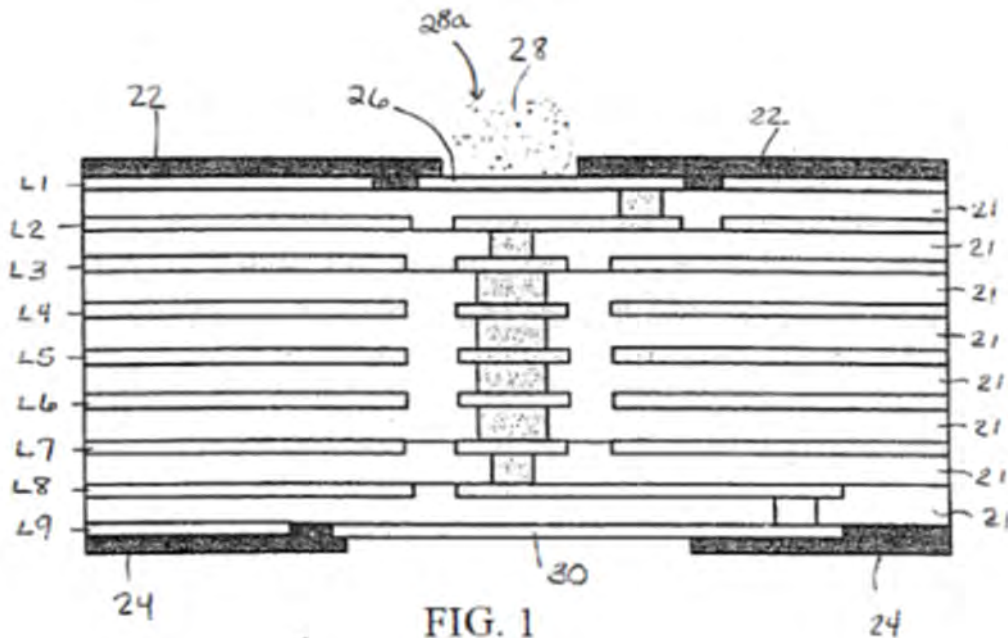
149. In my opinion, the combination of Chung, Celeron and AAPA discloses or suggests each and every element of dependent claim 4.

a) “A package as recited in claim 1, wherein the package comprises nine layers with the routing layer being the eighth layer and the ball pad layer being the ninth layer, on a bottom of the package.”

150. The Chung-Celeron combination discloses a multiple layered IC package as discussed above in Section X.G.1 regarding claim 7. AAPA discloses the additional claim feature as discussed above in Section X.A.3 regarding claim 10.

151. AAPA discloses in Fig. 1, shown below that “As an example, FIG. 1 shows a typical multi-layer organic BGA flip chip substrate that uses a 9-layer stackup 20 with a thin core. The 9-layer stackup 20 includes a layer L1, a layer L2, a layer L3, a layer L4, a layer L5, a layer L6, a layer L7, a layer L8 , and a layer L9...The upper surfaces 28a of the solder masses 28 provide a die site on which the die (not shown) will be placed. A plurality of ball pads 30 (one of which is shown) are provided on Layer L9.” (*Id.*, Fig. 3, 1:27-53 [emphasis added])

152. “Layer L8 provides the bottom routing layer. Placement of a quadrant of the die over the solder masses 28 is represented by line 38. Signal traces 36 are dispersed throughout layer L8.” (*Id.*, 1:51-54)



(*Id.*, Fig. 1 annotated)

153. A person of ordinary skill in the art implementing the packages of Chung and Celeron would have been motivated to look to the AAPA 9-layer stackup 20 to route signals, power, and ground between a die and a PCB. Such a person would have had good reason to look to AAPA as Chung, Celeron and AAPA are all in the same field of IC packaging.

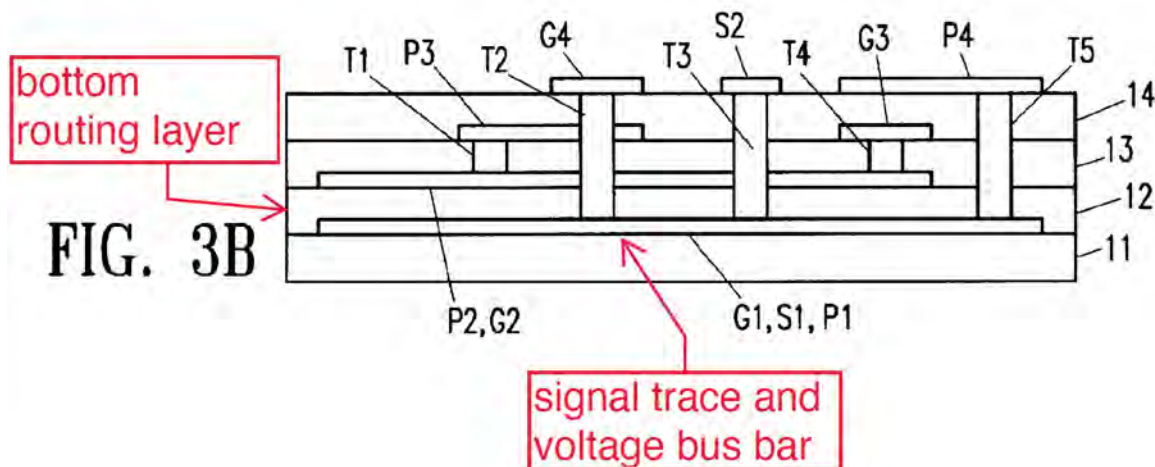
J. Ground 10 – Claim 6 is obvious by Chung in view of Celeron, and further in view of Tanahashi

154. In my opinion, the combination of Chung, Celeron, and Tanahashi discloses or suggests each and every element of dependent claim 6.

1. Claim 6

a) “A package as recited in claim 1 wherein the signal traces on the bottom routing layer comprise at least one voltage bus bar.”

155. The Chung-Celeron combination discloses an IC package with signal traces on a bottom routing layer as discussed above in Section X.G.1 regarding claim 7. Tanahashi discloses in Figure 3B (below) that signal traces and a voltage bus bar can be on the same layer as discussed above in Section X.F.1 regarding claim 6.



(Ex. 1009, Fig. 3B annotated)

156. Tanahashi does not explicitly state that the routing layer, which includes the signal trace and the voltage bus bar, is the “bottom routing layer.” However, as is shown in Figure 3B (above) of Tanahashi, signal trace S1 and a voltage bar P1 are routed on the layer immediately above layer 11 (lowest layer). A person of ordinary skill in the art would understand that the lower layer that included signal traces would be on the “bottom routing layer.”

157. A person of ordinary skill in the art implementing the IC package of Chung-Celeron would have had good reason to look to Tanahashi as they are all directed to multilayer structures on which semiconductor devices are mounted. A

person of ordinary skill in the art would have been motivated to combine Tanahashi's teaching of combining voltage conductors and signal conductors on a single layer with the Chung-Celeron semiconductor package to provide additional routing flexibility and/or to decrease the number of layers of a semiconductor package.

K. Ground 11 – Claims 1 and 5 are obvious by Devnani in view of Celeron

158. In my opinion, the combination of Devnani and Celeron disclose or suggest all features of claims 1 and 5.

1. Claim 1

a) “A semi-conductor package comprising: a top layer having a die mounted thereon, said die having a corner;”

159. Devnani discloses this limitation as discussed above in Section X.D.1(a).

b) “a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces thereon,”

160. Devnani discloses this limitation as discussed above in Section X.D.1(b).

c) “and a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads,”

161. Devnani discloses this limitation as discussed above in Section X.D.1(c).

d) “wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die.”

162. Celeron discloses this limitation as discussed above in Section X.G.1(e). A person of ordinary skill in the art implementing the IC package of Devnani would have had good reason to look to Celeron as they are both in the same field of IC packaging. A person of ordinary skill in the art would have been motivated to combine the routing layer of Devnani that routed traces away from high stress areas with the clear area of Celeron to prevent damage to signal traces of the bottom routing layer during thermal cycling.

2. Claim 5

a) “A package as recited in claim 1, wherein the die is mounted to the top layer in an arrangement other than a pin connection.”

163. Celeron discloses this limitation as discussed above in Section X.G.3(a). Further, Devnani discloses that a conventional ball grid array (BGA) package could be used. (Ex. 1005, ¶0027) As stated by Devnani and numerous contemporaneous references, BGA packages were in widespread use prior to the invention of the '245 patent. A person of ordinary skill in the art would have been motivated to use the BGA package of Devnani to mount a die upon a semiconductor package of Celeron, which “is an arrangement other than a pin connection.”

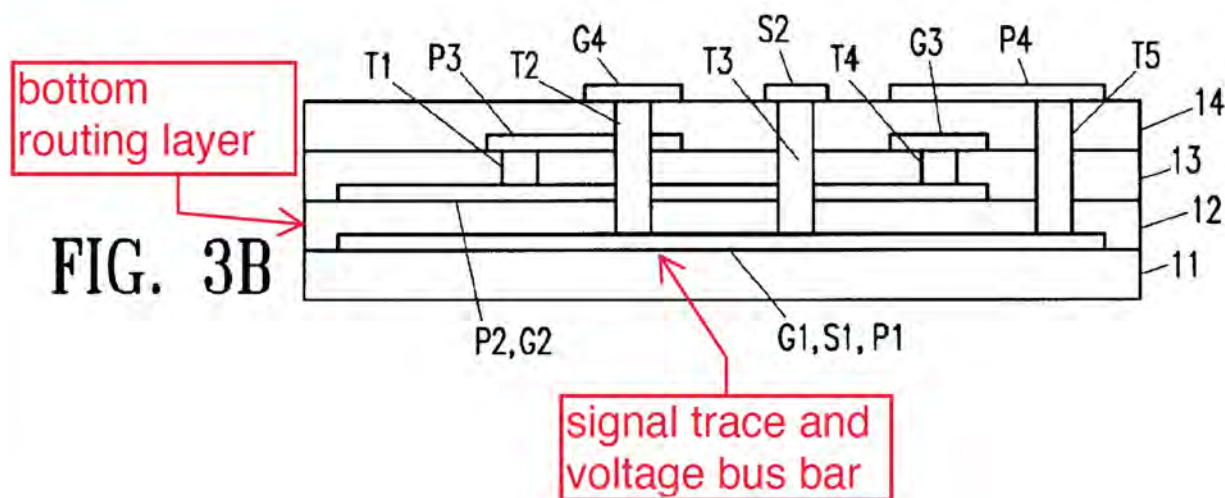
L. Ground 12 – Claim 6 is obvious by Devnani in view of Celeron, and further in view of Tanahashi

164. In my opinion, the combination of Devnani, Celeron and Tanahashi disclose or suggest all features of claim 6.

1. Claim 6

a) “A package as recited in claim 1, wherein the signal traces on the bottom routing layer comprise at least one voltage bus bar.”

The Devnani-Celeron combination discloses an IC package with as discussed above in Section X.K.1 regarding claim 1. Tanahashi discloses in Figure 3B (below) that signal traces and a voltage bus bar can be on the same layer.



(Ex. 1009, Fig. 3B annotated)

165. Tanahashi does not explicitly state that the routing layer, which includes the signal trace and the voltage bus bar, is the “bottom routing layer.” However, as is shown in Figure 3B (above) of Tanahashi, signal trace S1 and a voltage bar P1 are

routed on the layer immediately above layer 11 (lowest layer). A person of ordinary skill in the art would understand that the lower layer that included signal traces would be the “bottom routing layer.”

166. A person of ordinary skill in the art implementing the IC package of Devnani-Celeron would have had good reason to look to Tanahashi as they are all directed to multilayer structures on which semiconductor devices are mounted. A person of ordinary skill in the art would have been motivated to combine Tanahashi’s teaching of combining voltage conductors and signal conductors on a single layer with the Devnani-Celeron semiconductor package to provide additional routing flexibility and/or to decrease the number of layers of a semiconductor package.

M. Ground 13 – Claim 7 is obvious by Review of BGAs, in view of Devnani and CRTA.

1. Claim 7

a) “A semi-conductor package comprising:”

167. I understand that “a semi-conductor package comprising” is the preamble to claim 1 of the ’245 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, in my opinion, the combination of Review of BGAs, Devnani and CRTA discloses this claim feature. Figure 3 of

Review of BGAs, as shown and annotated below, discloses a semi-conductor package. (Ex. 1018, p. 6)

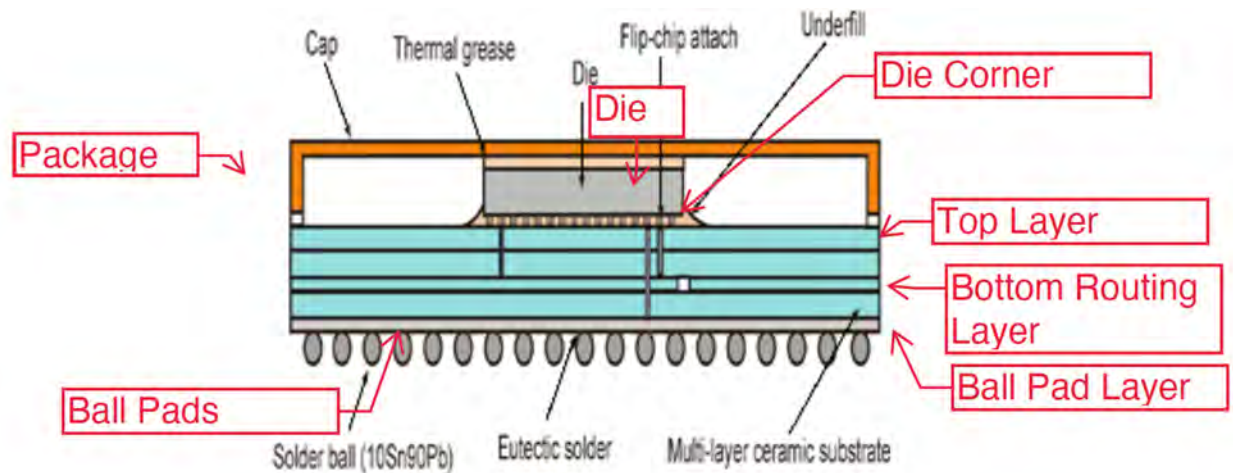


Fig. 3. Ceramic ball grid array (CBGA) [3]

(*Id.*, Fig. 3 annotated)

b) “a top layer having a die mounted thereon, said die having a corner defining a surrounding area of increased stress; and”

168. In my opinion, the combination of Review of BGAs, Devnani and CRTA discloses this claim feature. Review of BGAs shows in Figure 3 above, a die mounted upon a top layer of the semi-conductor package, where the die has a die corner. Review of BGAs further discloses “the greatest strains are found beneath the edges of the silicon die” (*Id.*, p. 17) Review of BGAs does not explicitly use the term “corner”. However, CRTA discloses “that thermal coefficient of expansion (TCE) mismatch have been identified by major manufacturers that cause cracking during temperature cycling”. (Ex. 1016, p. 32) CRTA further discloses that the “cracking

generally occurs near the corners of the chip”. (*Id.* [emphasis added]) Further, CRTA states that “package stress increases exponentially from the package center along a radius line to the die corner.” (*Id.*, p. 34 [emphasis added])

169. A person of ordinary skill in the art implementing the IC package of Review of BGAs would have had good reason to look to CRTA as they both are in the same field of IC packages and deal with thermal cycling stresses. Further, such a person would have been motivated to include the high stress of a die corner of CRTA in implementing a change to the BGA package of Review of BGAs to reduce package failure. Such a modification would have been straightforward for such a person as it would be a simple substitution of including the high stress of at a die corner with Review of BGAs stress along a die edge in a package design.

c) “a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces thereon,”

d) “and a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads dispersed thereon,”

170. In my opinion, the combination of Review of BGAs, Devnani and CRTA discloses these claim features.

171. Review of BGAs shows in Figure 3, below, the package has a plurality of layers, that include a top layer, a bottom routing layer, and a ball pad layer under the bottom routing layer having a plurality of ball pads.

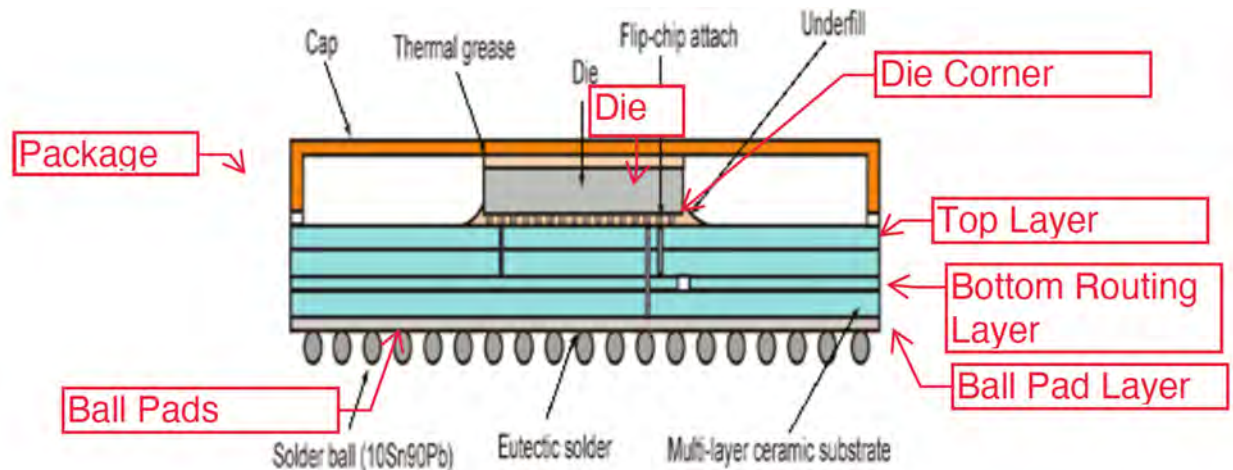
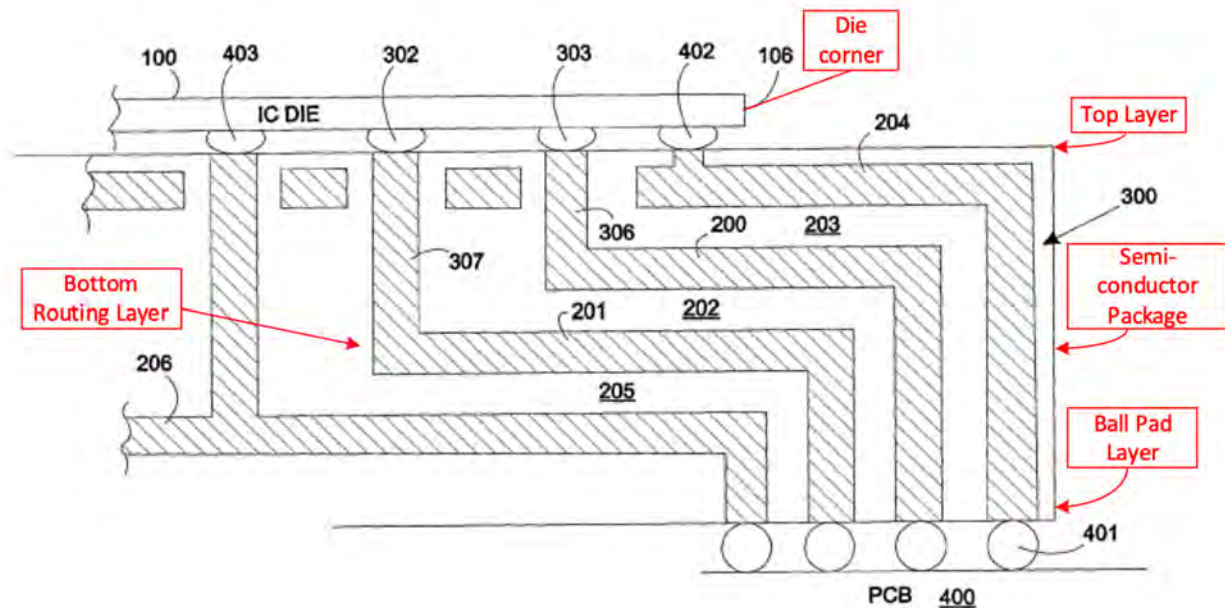


Fig. 3. Ceramic ball grid array (CBGA) [3]

(*Id.*, Fig. 3 annotated)

172. I've been asked to assume that Review of BGAs does not disclose this limitation. However, Devnani also discloses this limitation.

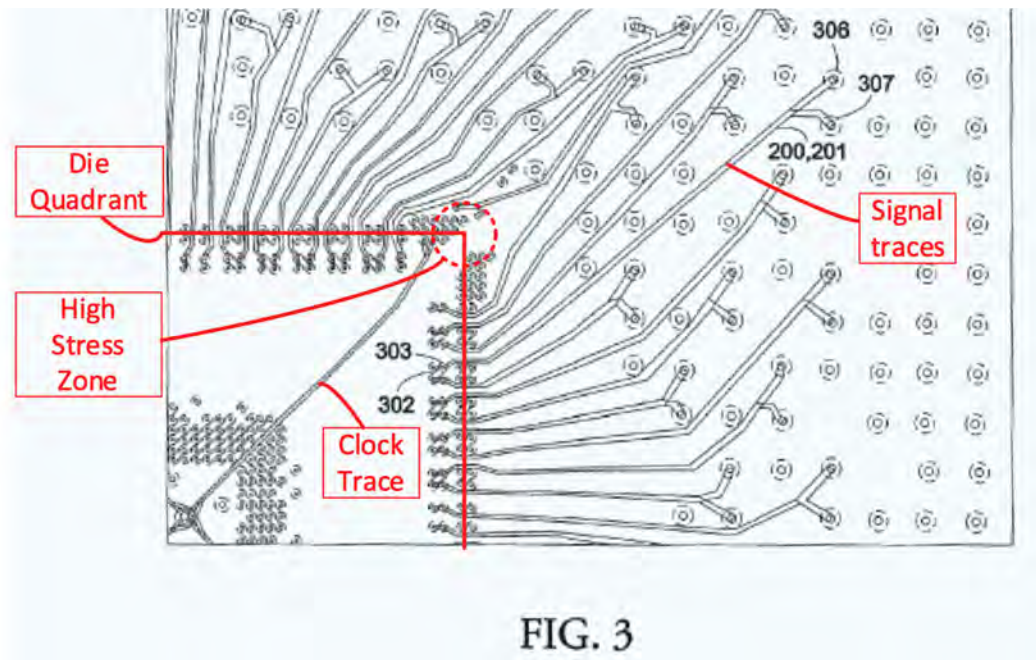
173. Devnani discloses layers in an IC package (Ex. 1005, ¶10005) and also shows in Figure 4, below, a layer for routing signals (e.g., signal 201) that is lower than other layers of the IC package. (*Id.*, ¶¶10005; 0025; Claim 1) A person of ordinary skill in the art would understand that a "bottom routing layer" would be a routing layer beneath another layer of the IC package.



(Id., Fig. 4 annotated)

e) “wherein none of the signal traces of the bottom routing layer are located within the area of increased stress defined by the corner of the die.”

174. In my opinion, the combination of Review of BGAs, Devnani and CRTA discloses this claim feature. Figure 3 (below) of Devnani is annotated to show where a die quadrant resides when the IC die is mounted upon the package 300 and to identify the high stress zone of CRTA associated with the corner of the die. Devnani implicitly shows routing traces 201 away from the edges of the die and NOT routing any traces directly under the corner of the die.



(Ex. 1005, Fig. 3 annotated)

175. Thus, in my opinion, this inherent feature of Devnani discloses signal traces being routed away from the high stress areas and NOT routing any traces within the highest stress area near the die corner.

176. A person of ordinary skill in the art implementing the semiconductor package of Review of BGAs and Devnani would have good reason to look to CRTA to NOT route any signal traces inside the highest stress area associated with the corner of a die as they both are in the same field of semiconductor packages. Such a person of ordinary skill in the art would have been motivated to implement CRTA's highest stress die corner to move Devnani's traces away from such high stress areas to prevent trace cracking with the IC package of Review of BGAs-Devnani.

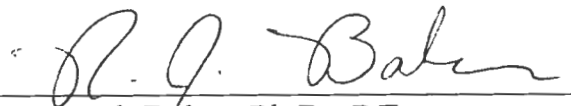
177. Further, the modification of Review of BGAs-Devnani with CRTA would have amounted to nothing more than the use of a known technique to improve a similar device, and the results of the modification would have been predictable. This is because at the time of the invention, a person of ordinary skill in the art would have had the requisite skill level to readily modify the IC package disclosed by Review of BGAs-Devnani to route traces on a bottom layer based on CRTA teaching a highest stress being in a die corner. Moreover, such modification of Devnani would have been routine for the person of ordinary skill in the art as they would be using well-known elements with no change in their respective functions.

XI. CONCLUSION

178. In summary, it is my opinion that all of the features recited in claims 1-12 of the '245 patent are disclosed or suggested by the prior art.

179. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: November 7, 2023



R. Jacob Baker, Ph.D., P.E.