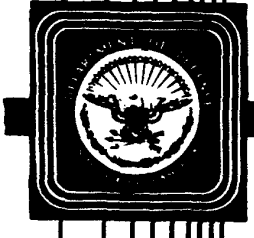
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The increased complexity and speed requirements of computers, communications, military and aerospace systems has increased the need for devices with performance levels that cannot be attained or are difficult to achieve with silicon designs. This has caused component vendors to seek other materials such as Gallium Arsenide (GaAs) for device construction. GaAs is a compound semiconductor material which exhibits superior carrier mobility, radiation hardness and power efficiency in high frequency applications up to 100 GHz. The Department of Defense (DoD) has provided research funds toward the development of GaAs technology since the benefits of faster components and the inherent radiation hardness of GaAs is appealing to military applications.

This technology review covers design and application issues for GaAs devices including Monolithic Microwave Integrated Circuits (MMICs), field effect transistors, millimeter wave diodes, and photonic components. Highlighted is a review of models which have been proposed to predict the reliability of gallium arsenide components.

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PREFACE

The increased complexity and speed requirements of computers, communications, military and aerospace systems has increased the need for devices which can not effectively be manufactured using current silicon technology. This has caused component vendors to seek other materials such as gallium arsenide (GaAs) for device construction. The Department of Defense (DoD) has provided research funds toward the development of GaAs technology because the benefits of faster components and gallium arsenide's inherent radiation hardness is appealing to military applications. This publication provides an overview of the reliability of GaAs devices and the current status of GaAs technology.

I would like to acknowledge Daniel Fayette of Rome Laboratory and Bill Denson, Jack Farrell and George Ebel of IIT Research Institute for their support and contributions to this publication.

1.0 INTRODUCTION

Once considered the material of the future, gallium arsenide (GaAs) has finally come of age as a production technology and is being inserted into military and commercial systems. These systems require devices manufactured from gallium arsenide since the performance advantages it can offer can improve their operational capability. It has qualities which tend to make it more suitable for high speed integrated circuits than silicon. GaAs is a semi-insulating material, not semiconducting like silicon. This greatly reduces the parasitic capacitance that forces silicon manufacturers to junction or oxide isolate their transistors to avoid a loss of speed. This along with increased carrier mobility allows the fabrication of devices that can operate at frequencies which outperform their silicon counterparts. Additionally, GaAs offers inherent radiation hardness and improved power efficiency for high frequency digital and analog circuitry.

Monolithic Microwave Integrated Circuits (MMIC) are conceptually a hybrid microwave device whose substrate is GaAs. Previous to the development of GaAs MMIC technology, discrete packaged devices and multifunction assemblies were commonly utilized in microwave applications. MMIC technology however offers several advantages which include weight/size reduction, process tolerances and uniform performance with a reduced need of tuning circuits. These advantages combined with GaAs's inherent performance advantages, have led to a significant interest in the technology. Many military contractors have invested in the technology to varying degrees. The Department of Defense (DoD) has invested heavily in the technology, most notably through the Microwave and Millimeter Wave Integrated Circuit (MIMIC) and DARPA Digital Insertion programs. In the last few years several large system houses have begun to manufacture GaAs monolithic integrated circuits. Additionally many independent companies were formed that manufacture discrete GaAs devices. Recently, original equipment manufacturers, vendors and independent foundries have begun to form alliances to manufacture GaAs devices. The cost continues to drop as the manufacturing ability matures. Projections of growth in the GaAs market are excellent, as shown in Figure 1.

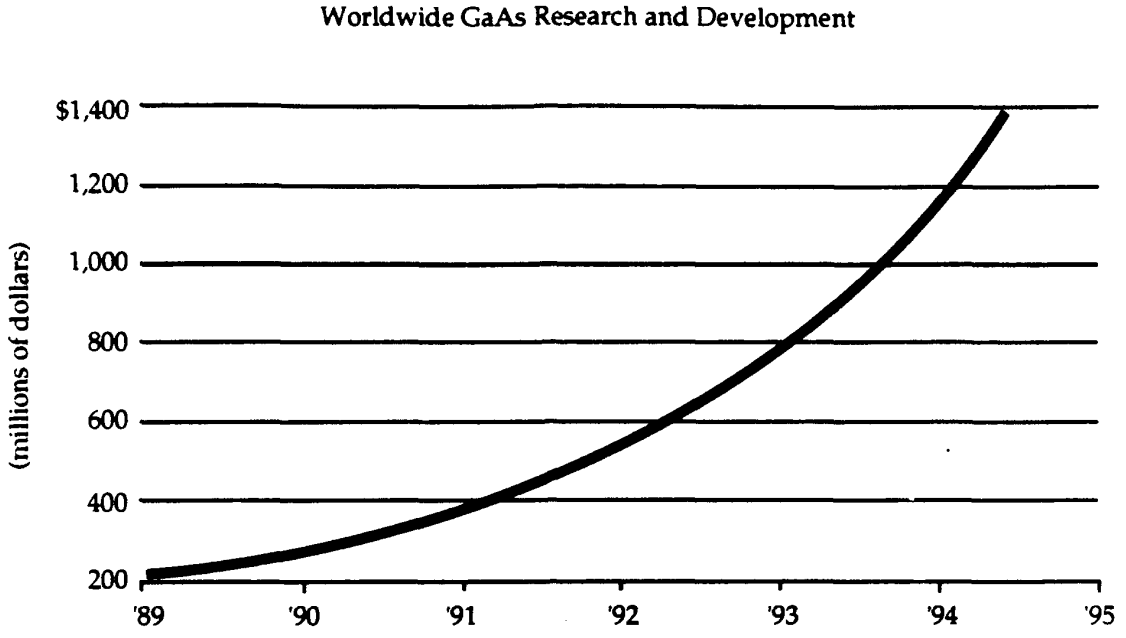


Figure 1: GaAs Forecast

Only limited information concerning the reliability of GaAs and MMIC components has been published to date. This document presents an overview of this topic while providing a description of the types of devices that are currently manufactured using the technology. Additionally, a review of the MIMIC program, reliability prediction techniques and a comprehensive list of acronyms have been presented.

2.0 WHY GaAs?

Silicon technology is a mature technology, based on an inexpensive, elemental and abundant material whose oxide is one of the best and easily grown. Silicon has been used extensively towards the development of integrated circuits and other semiconductor components. Silicon however has performance limitations which have component vendors seeking alternative materials such as gallium arsenide (GaAs) for device construction.

Gallium arsenide is a III-V compound semiconductor which offers reduced inherent (or parasitic) capacitance and increased carrier mobility. These properties have allowed the development of Monolithic Microwave Integrated Circuits (MMIC) which can run at frequencies up to 100 Gigahertz (GHz) while silicon parts of similar complexity approach speed limitations in the 1-5 GHz range. Studies have shown that GaAs digital circuits either have lower power dissipation or run at least two to five times faster than similar silicon circuits. Current analog GaAs Field Effect Transistors (FETs) operate into the 20 GHz range while laboratory devices have been shown to operate at speeds in excess of 60 GHz. Most current silicon transistors can not operate at 1 GHz. Since GaAs has a higher electron velocity, the higher speed of a GaAs device does not necessarily result in proportionally higher power consumption. As seen in Figure 2, enhancement/depletion mode GaAs integrated circuits offer the best speed-power product advantage over silicon.

The energy gap for GaAs is larger than silicon allowing GaAs components to have good performance, even at higher temperatures. This energy gap is direct, allowing the development of optically active elements which can be incorporated on the same substrate of a GaAs integrated circuit. The wider gap and shorter carrier life also provide greater radiation resistance. The material allows for the development of high resistive substrates which can be used as dielectrics that simplify the insulation of active areas in digital circuits. Table 1 offers a comparison of the basic material properties of silicon and GaAs.

Table 1: Comparison of GaAs and Silicon Properties

Property	GaAs	Silicon	Importance
Energy Gap (eV)	1.424 (Direct)	1.100 (Indirect)	Optical Properties Radiation Tolerance
Intrinsic Carrier Concentration (cm^{-1})	$2x10^6$	$1x10^{10}$	Semi-insulating
Intrinsic Resistivity (ohm-cm)	$4x10^8$	$4x10^6$	High Isolation
Electron Mobility ($cm^2/V-s$) ($N=10^{17}cm^{-3}$)	6000	1000	High Speed
Thermal Conductivity (W/cm-deg. C)	0.5	1.4	Circuit Density
Linear Coefficient of Thermal Expansion (deg C^{-1})	$6.86x10^{-6}$	$2.6x10^{-6}$	Thermal mismatches between materials for GaAs is a concern

The aforementioned features and advantages of GaAs have led to significant interest in the technology. Millimeter wave diodes and photonic devices have been widely used since the 1970's, however GaAs integrated circuits are in relatively early stages of development and production. The advantages that GaAs integrated circuits can offer over their silicon counterparts have been mentioned, however the GaAs semiconductor industry is still perceived by many as being immature. DoD funded programs such as the MIMIC program are striving to change this through GaAs semiconductor development and testing. Early indications are optimistic that these programs are achieving this goal and that within a few years GaAs semiconductor technology will be a widely used and mature technology.

3.0 REVIEW OF CURRENT TECHNOLOGY

Gallium arsenide with intrinsic high electron mobility and semi-insulating properties has long been envisioned as the basis for high speed electronic technology. It was first synthesized by V.M. Goldschmidt in 1929 and its semiconducting properties were studied by H. Welker in 1952. In 1963 J.B. Gunn announced the discovery of the negative resistance property of GaAs and within a short time GaAs FETs, the building blocks of GaAs ICs were developed. In the early 1970s, GaAs FETs were developed for microwave applications while prototype development of gallium arsenide ICs did not begin until the mid 1970's. The first digital GaAs IC exhibiting a single FET logic gate was built in 1974, roughly 20 years after silicon development. Six years prior, Professor Mead of Cal Tech introduced the first GaAs field effect transistor (FET) using a Schottky gate. Sales of commercial market GaAs ICs however, did not really begin until 1984.

Since the release of the first GaAs integrated circuit the technology has experienced rapid growth. This is indicative of how much has been borrowed from silicon fabrication technology. Some drawbacks to this rapid development however exist. Generally , there has been a lack of available circuits for testing. The GaAs integrated circuit industry has not had the benefit of standard or widely used technologies, like silicon IC manufacturers did with TTL type devices, to learn from. Efforts through programs like the DoD MIMIC program are currently being pursued to change this. Figures 3, 4, and 5 indicate that the military is the driving force behind the early stages of GaAs production and development, however by 1995 it is predicted that the commercial market will be the major user.

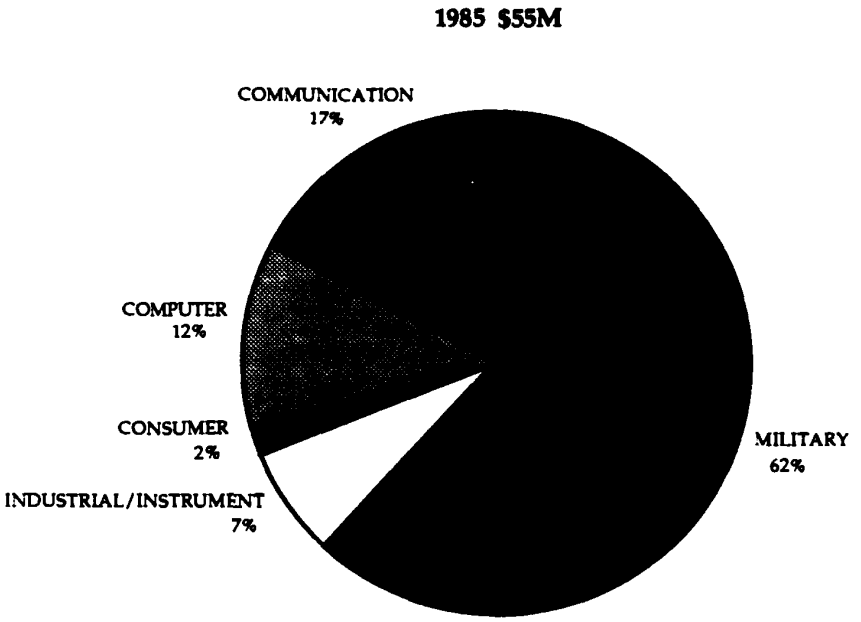


Figure 3: 1985 GaAs Integrated Circuit Market

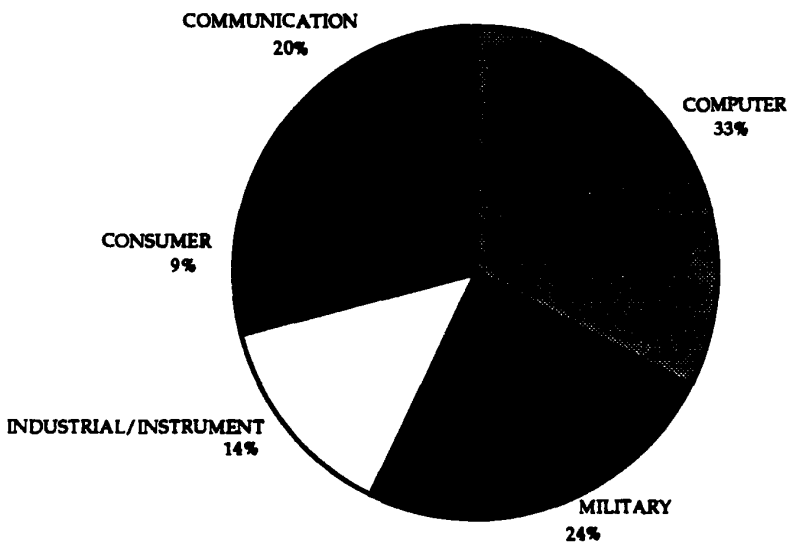


Figure 4: 1990 GaAs Integrated Circuit Market

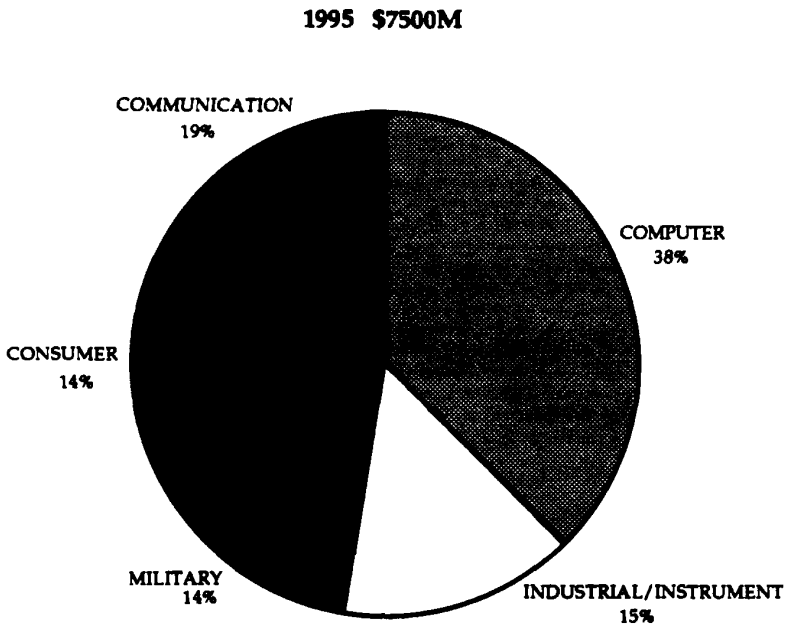


Figure 5: Estimated 1995 GaAs Integrated Circuit Market

Different classes of devices including GaAs MMIC and digital integrated circuits are currently being manufactured or developed using GaAs technology. A brief description and the principles of operation of components manufactured using current GaAs technology are presented in the following sections with emphasis placed on mature device types. Other new or unique component styles exist which have not been covered in this treatise and may be addressed in future publications.

3.1 GaAs MMIC and Digital Integrated Circuits

Gallium arsenide technology allows the development of optically active devices on the same substrate as GaAs integrated circuits. When fully realized, photonic interfaces and the development of optoelectronic integrated circuits will revolutionize the semiconductor industry. Currently GaAs technology has been used successfully towards the development of digital and analog MMIC microwave circuits. Digital GaAs integrated circuits resemble digital silicon circuits while GaAs MMICs are similar to hybrid microstrip circuits. GaAs MMICs are structurally more complex than silicon circuits. They are essentially three dimensional, utilizing both the front and back sides of the chip. They additionally contain novel structures such as air bridges, a thinned substrate and via hole grounding. A cross-section of a MMIC device portraying these structures is given by Figure 6.

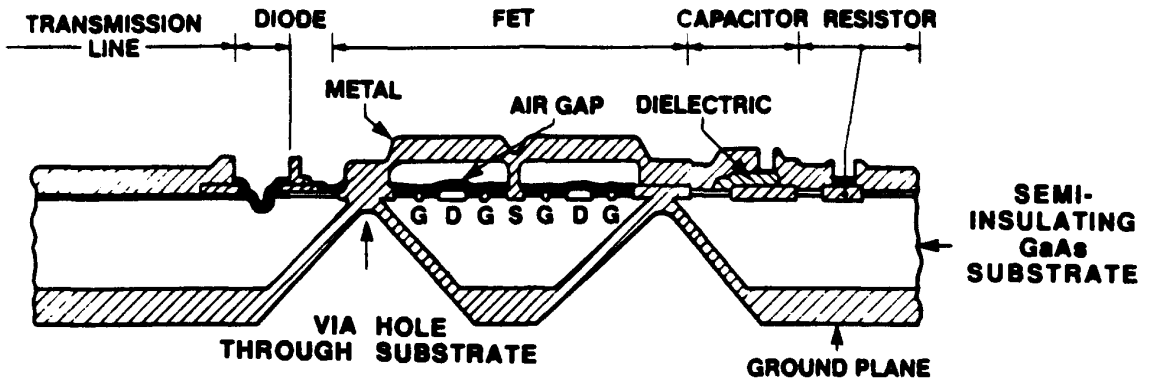


Figure 6: Cross-Section of a GaAs MMIC[1]

MMICs use the GaAs wafer for microstrip transmission lines. The electric field propogates through the bulk of the GaAs die, not just on the surface. Air bridges provide low capacitance RF crossovers and a thinned wafer permits formation of via holes that connect the metallized back of the wafer to circuit elements on the front side as well as provide a reduced thermal path for power devices. Digital GaAs integrated circuits incorporate small devices and have a high packing density while GaAs MMIC circuit elements are much larger. In general, the elements of GaAs digital circuits are up to five times smaller in area while microwave circuit elements can be up to twenty times larger in area than their silicon counterparts. Table 2 outlines MMIC structures and their typical dimensions.

Air bridges are widely used in GaAs circuits to connect passive and active components. They are required for GaAs MMICs operating at gigahertz frequencies, since the capacitance of crossovers using a dielectric layer would be too high. They may be used to interconnect sources of FETs, to cross over a lower level of metallization, or to connect a Metal-Insulator-Metal (MIM) capacitor to adjacent metallization. In many cases there is no material other than air between the bridge and the wafer beneath it, giving it its name. Air bridges have been found to be resistant to shock and vibration but can be damaged during handling since it typically rises above other features on the GaAs circuit chip. The maximum width of an airbridge is typically 3 μm. For mechanical integrity it has been reported that the span to width ratio of an airbridge can be as high as 25:1.

1 MFAT-II, GaAs Characterization and Failure Analysis Techniques - A Procedural Guide.

Table 2: Typical Dimensions of MMIC Structures

MMIC Structure	Function	Typical Size	μm
MMIC	Microwave IC	length	3000
Physical Structures			
1. Air Bridge	RF Crossover	height	3
2. Thinned GaAs	Microstrip substrate thermal conductance via hole formation	thickness	100
3. Via Hole	low inductance ground	diameter	100
Active Elements			
4. GaAs FET	power gain	gate length	1
5. HEMT	low-noise gain	gate length	0.25
6. Diode	switch	contact width	2
Passive Elements			
7. Microstrip	distributed element	width	75
8. Spiral Inductor	lumped element	diameter	300
9. MIM Capacitor	lumped element	square	100
10. Resistor	lumped element	length	100

The semi-insulating properties of GaAs are ideal when electrically isolating circuit elements. A dielectric constant of 12.9 and the ability to thin the GaAs substrate allows for the development of compact microstrip transmission line structures. Additionally, thinning of the GaAs wafer allows for the fabrication of via holes. A via hole has two definitions depending on how it is used. In digital applications a via can be an opening in the front side dielectric coating that permits connection between the first and second level metallization. A via through a GaAs MMIC substrate provides connection from the front side metallization to the backside ground plane. Vias can only be incorporated in thinned GaAs since etching through a thick substrate to form a via would cause the back side of a via to be too large. Thinning additionally provides good thermal conductance for cooling large power FETs. Additionally, via holes in GaAs substrates can act as low inductance grounding for FETs and transmission line stubs. They are bowl shaped and typically measure 100 μm on the front side and approximately three times as large on the back side of a GaAs substrate.

3.2 Millimeter Wave Diodes

Several types of millimeter wave diodes are currently manufactured using GaAs technology. This section will address the principles of operation for Gunn diodes and Impact Ionization Avalanche Transit Time (IMPATT) devices.

3.2.1 Gunn Diodes

Gunn diodes or Transferred Electron Devices (TED) are used to generate power at microwave and mm-wave frequencies. The operation of a Gunn diode relies on the unusual band structure of GaAs, see Figure 7. The lowest energy conduction band of GaAs has a high electron mobility, a low effective mass and a low density of states. The next higher conduction band provides lower mobility, higher effective mass, and the density of states is higher than in the lower conduction band. As an electric field is applied to the GaAs, electrons gain enough energy to transfer themselves from the lower conduction band (the central energy valley) to the higher (satellite energy valley). At the higher band, the lower electron mobility and higher mass result in a decrease of the mean velocity of the electrons. The electrons in the higher band act as if their mass is approximately 20 times greater and a velocity field curve as seen in Figure 8 results. This effect is generally known as the Gunn Effect.

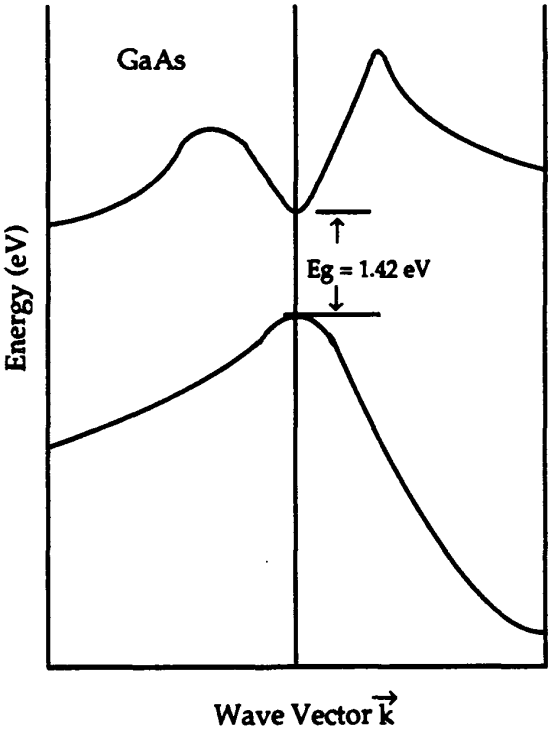


Figure 7: Band Structure of GaAs

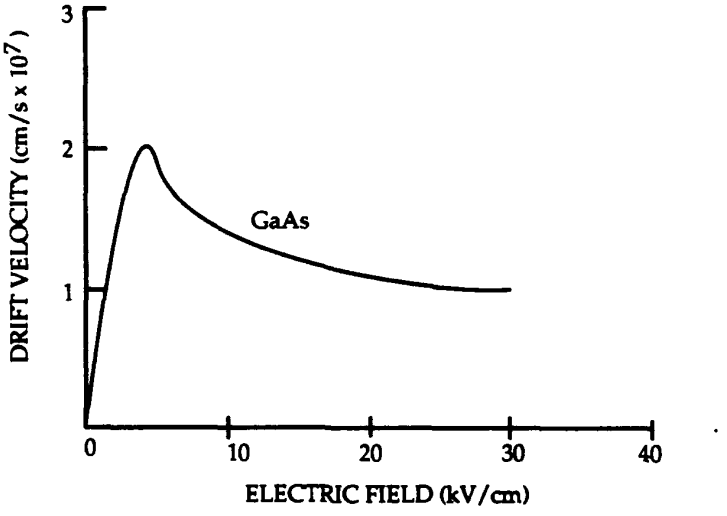


Figure 8: Velocity Field of GaAs

3.2.2 Impact Ionization Avalanche Transit Time (IMPATT) Diodes

Impact Ionization Avalanche Transit Time (IMPATT) diodes use a p-n junction operated in the avalanche mode. Various types of IMPATT diodes exist. Figure 9, illustrates a Read IMPATT diode, which was so named after its inventor. Operation of this diode occurs when the p-n junction of the diode is reverse biased into avalanche causing depletion of the intrinsic region of the diode. Electrons are generated at the p-n junction, by impact ionization or avalanche drift across this intrinsic region at saturated drift velocity, and are collected at the anode. Depending on the RF voltage, more or less avalanche current is generated, see Figure 10. IMPATT diodes are constructed in such a way that avalanche and drift time delays result in the RF current of the device being a half cycle out of phase with its RF voltage. Additionally the diode supplies energy to an outside resonant circuit instead of absorbing it.

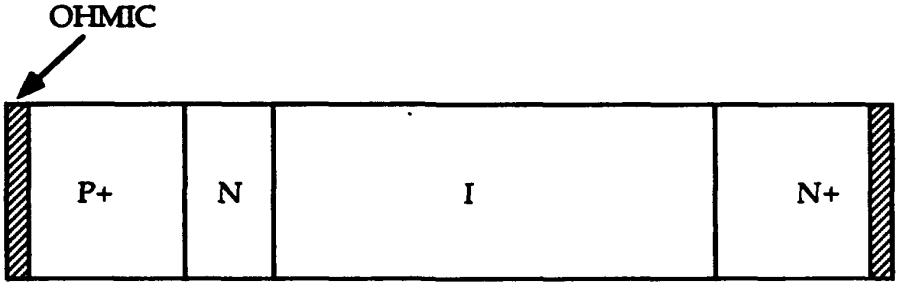


Figure 9: Basic Structure of the Read (IMPATT) Diode

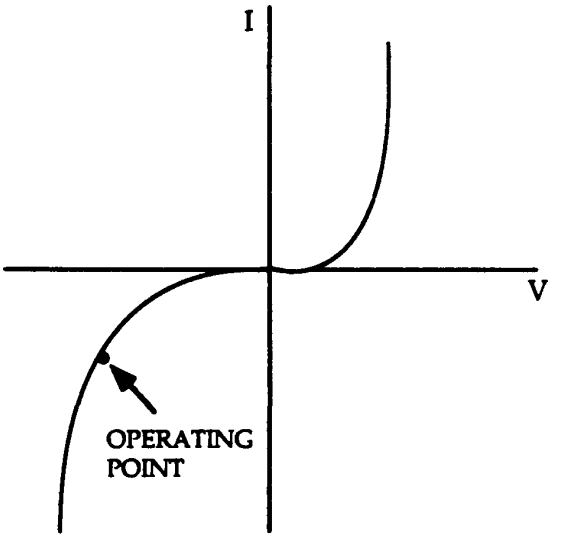


Figure 10: Current Voltage Characteristics of a Read Diode, Shown with its Operating Point

3.3 Transistors

Transistors are the building blocks of GaAs integrated circuits and as a result have received much attention by the GaAs semiconductor industry. Many types of transistors are currently manufactured using GaAs technology and even more are in development. The principles of operation for Metal Semiconductor FETs (MESFET), Junction FETs, Heterojunction Bipolar Transistors (HBT), Heterostructure Field Effect Transistors (HFET), and High Electron Mobility Transistors (HEMT) are addressed in the following sections.

3.3.1 Metal Semiconductor FETs (MESFETs)

Metal Semiconductor Field Effect Transistor (MESFET) technology currently dominates the GaAs FET industry. They were first developed and prototyped in the mid-1960's. Two types of MESFETs currently exist, depletion mode and enhancement mode devices. A cross section of a MESFET is shown in Figure 11.

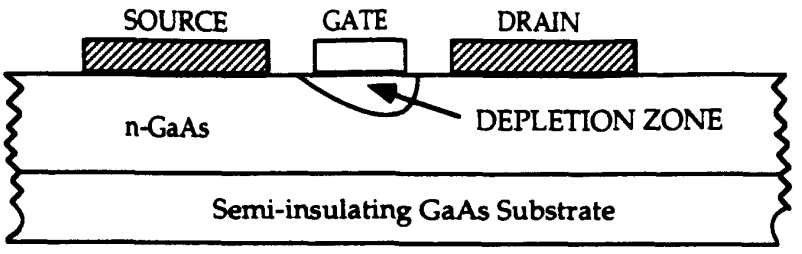


Figure 11: Cross Section of a Metal-Semiconductor FET (MESFET)

MESFETs contain two ohmic contacts, a source and drain which permit current to flow into or out of the GaAs. The surface layer of the GaAs is conductive while the underlying material is insulating. Through etching or ion implantation, the FET is isolated so that a direct current path exists between the source and drain. In depletion mode FETs, source-drain current flows at zero gate bias. An applied negative gate bias expands the depletion region and reduces the current to zero. Depletion mode FETs are often used as analog FET amplifiers and oscillators. At zero gate bias an enhancement mode FET does not exhibit current flow. In order to allow current flow a positive gate bias is required. Enhancement mode FETs have high transconductance, draw little power, and are normally off, making them widely used in digital circuits.

3.3.2 Junction FETs (JFETs)

Junction field erfect transistors (JFET) are fabricated using a double implantation of a n-type channel and a p-type gate structure with an ohmic gate contact. The JFET differs from a MESFET in that the gate of the JFET is not a Schottky barrier at the surface, but is formed internal to the bulk material as a p-n junction. Figure 12 provides a cross sectional diagram of a typical JFET.

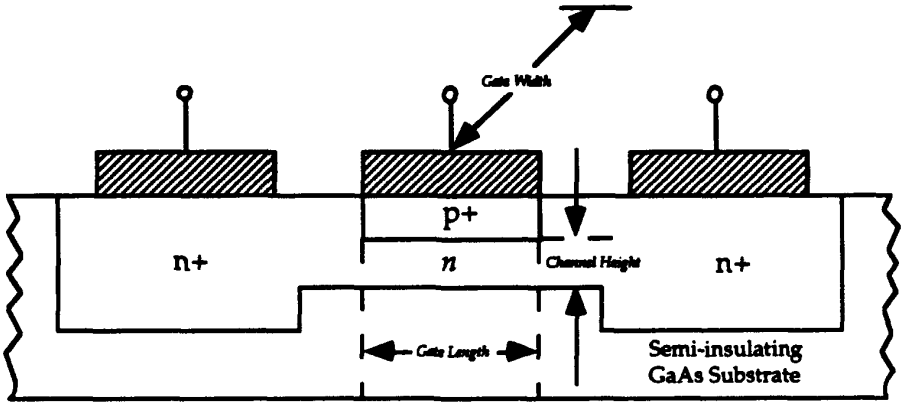


Figure 12: Cross Section of an Ion-Implanted Enhancement Mode JFET

JFETs were first developed in 1952 and the first prototype was manufactured in 1953. JFET devices offer a higher noise margin than MESFETs and it is possible to fabricate true complementary circuits with JFETs that offer decreased power consumption and increased radiation resistance.

3.3.3 Heterostructure FETs (HFET)

A Heterostructure Field Effect Transistor (HFET) is a transistor that includes a junction between materials of different compositions such as GaAs and AlGaAs. Varying types of HFETs exist, the High Electron Mobility Transistor (HEMT), being the most popular. HEMT devices were the first HFET device developed. HEMTs however have not been able to meet the needs of all applications. This has created a need for and the development of other types of HFETs. Table 3 categorizes the various types of Heterostructure FETs and their methods of construction.

Table 3: HFET Device Types

Donor layer	Selectively doped	Bulk doped donor layer (MODFET, TEGFET, HEMT, etc.) δ-doped donor layer Superlattice donor layer
	Insulated gate	MISFET, HIGFET SISFET
Channel confinement	Quantum well channel Inverted structure (I-HEMT, I^2-HEMT, etc.)	
Channel doping	Undoped Doped (DMT, etc.)	

Characteristics of the Schottky gate used by the HFET and backgating limit its capabilities for digital applications. A description of the HEMT, currently the most widely used HFET device, follows.

3.3.3.1 High Electron Mobility Transistor (HEMT)

The high electron mobility transistor (HEMT) is a heterostructural device used for high frequency operation. It is also referred to as a modulation doped FET (MODFET), a two dimensional electron gas FET (TEGFET), a hetero-interface FET (HIFET), a selectively doped heterostructure transistor (SDHT), or the multi-

acronym device (MAD), for obvious reasons. The HEMT, similar to other FETs, incorporates two ohmic contacts and a Schottky barrier gate that regulates the flow of current between the two contacts. The HEMT offers improved performance, when compared to other FETs, which results from the semiconductor materials used in its construction. As shown in Figure 13, the HEMT incorporates a doped AlGaAs layer and an undoped GaAs layer separated by a very thin layer of undoped AlGaAs (approx. 70 Angstrom).

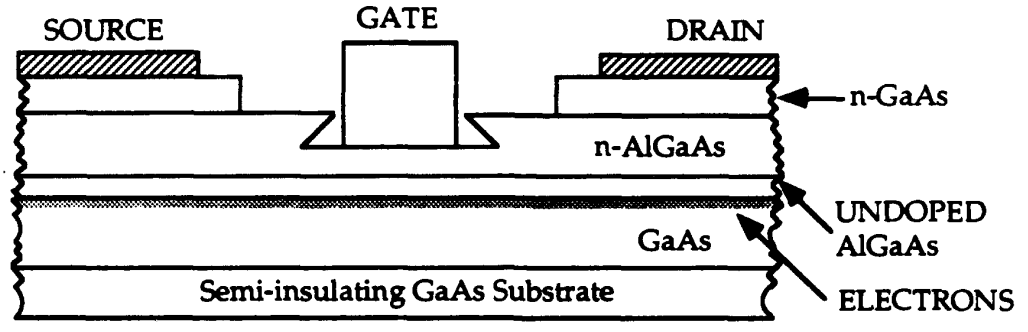


Figure 13: High Electron Mobility Transistor (HEMT)

Electrons are supplied from the doped AlGaAs layer, but electron flow occurs in the undoped adjacent GaAs layer. A conduction band discontinuity between the high bandgap AlGaAs and the undoped GaAs which localizes electrons in a thin two dimensional gas (2-DEG) layer on the GaAs side of the AlGaAs/GaAs interface exists. The electrons in the 2-DEG layer exhibit high mobility and velocity which result in a device with a much higher channel mobility than a comparably doped GaAs FET. Additionally, HEMTs have advantages over GaAs MESFETs of high power gain and high efficiency in power applications.

3.3.4 Heterojunction Bipolar Transistors (HBTs)

Heterojunction Bipolar Transistors contain one or more heterojunctions or junctions between distinct semiconductors, such as GaAs and AlGaAs. A cross-sectional diagram of a heterojunction bipolar transistor is shown in Figure 14.

These transistors exhibit electron flow vertically through a thin base region instead of under a metal gate which tend to make them operate faster. Development of HBTs has been slow due to the complex materials processing sequence that is involved in their manufacture.

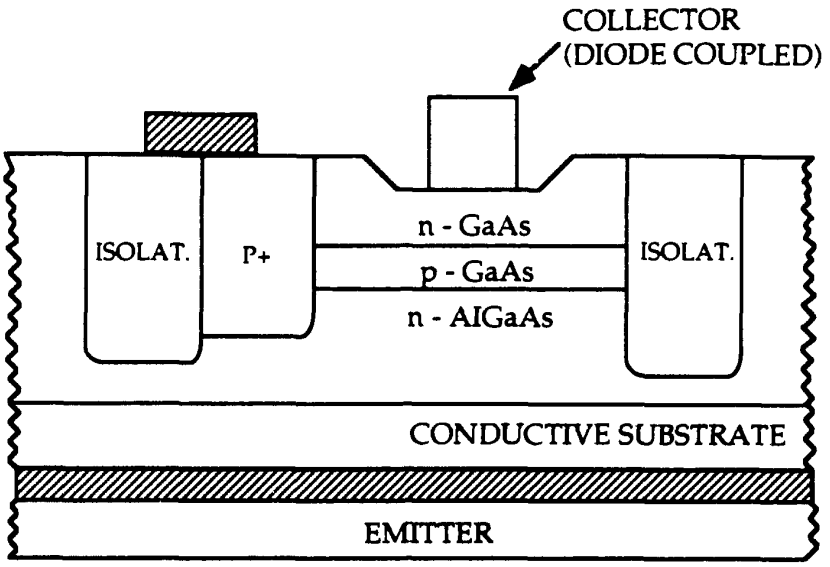


Figure 14: Heterojunction Bipolar Transistor (HBT)

3.4 Photonic and Optoelectronic GaAs Components

GaAs has been used towards the development of optoelectronic integrated circuits and photonic devices. Photonics is a relatively new but growing field and in the near future it is expected that GaAs optoelectronic integrated circuits will be readily available and used extensively. GaAs photonic components such as transmitters, receivers and repeaters are already available or in production and have actually been used in various military and commercial applications. The development of photonic devices began in the 1970's using primarily GaAs and AlGaAs materials. Recently, advances into InP and InGaAsP materials have been made in the development of photonic emitters and detectors which have led to improved performance. Device yields have steadily improved due to increased research being performed in GaAs technology and the photonic area.

3.4.1 Emitters

Gallium arsenide is commonly used as a construction material for emitters. Light emitting diodes (LEDs), some of the earliest emitters, have available optical power on the order of hundreds of microwatts. Within the past two decades, advances have led to the development of coherent emission lasers with powers into the tens of milliwatts. Coherent emission lasers provide improved performance to optical fiber transmissions, especially for long distance transmissions. Emitters translate an electrical signal to an optical one. This is accomplished by an electron transition from one energy level to another with the energy involved being released as a photon. The energy release for GaAs devices is considered direct gap and is only

associated with photon emissions. Materials such as silicon experience both photon and phonon emissions and are considered indirect gap. Only direct gap materials are used in the fabrication of emitters. Figures 15 and 16 illustrate the physical structures of GaAs LEDs and AlGaAs/GaAs lasers. Emitters developed using current technology have not fully met expectations and the optimization of their performance is being pursued.

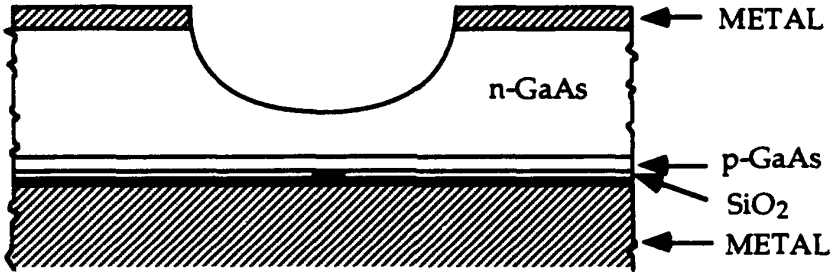


Figure 15: Cross Section of a GaAs LED

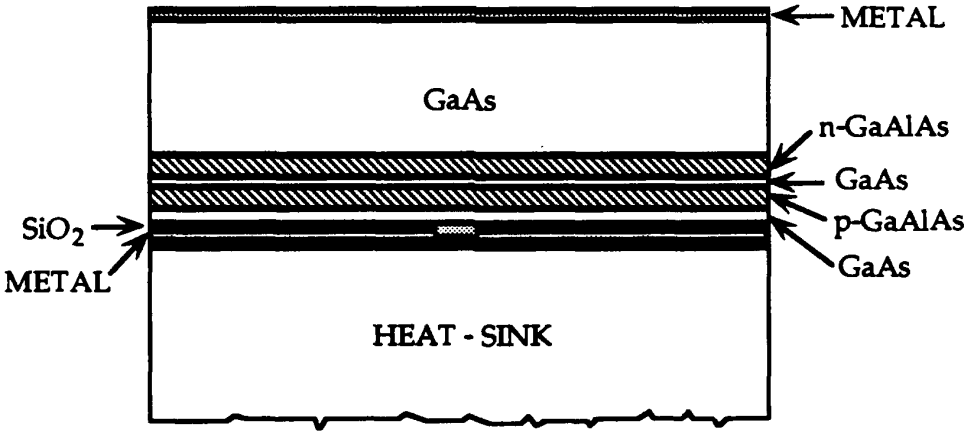


Figure 16: Cross Section of an AlGaAs/GaAs Laser

3.4.2 Detectors

A detector is a device which translates an optical signal into an electrical signal. Since the initial stages of photodetector development, silicon has been material of choice for detector construction. Silicon detector technology is therefore well established. Compared to current GaAs detectors, silicon devices offer greater noise and sensitivity characteristics. Devices manufactured from silicon are however limited by their speed and eventually applications requiring faster speed or a higher data rate will increase the need for gallium arsenide devices. Currently detectors constructed of InGaAs have been developed and used. Two types of detectors exist, photodiodes (Schottky and PIN structures) and avalanche photodiodes. Figures 17 and 18 illustrate planar and mesa cross section structures of PIN photodetectors respectively while Figure 19 illustrates an avalanche photodiode cross section.

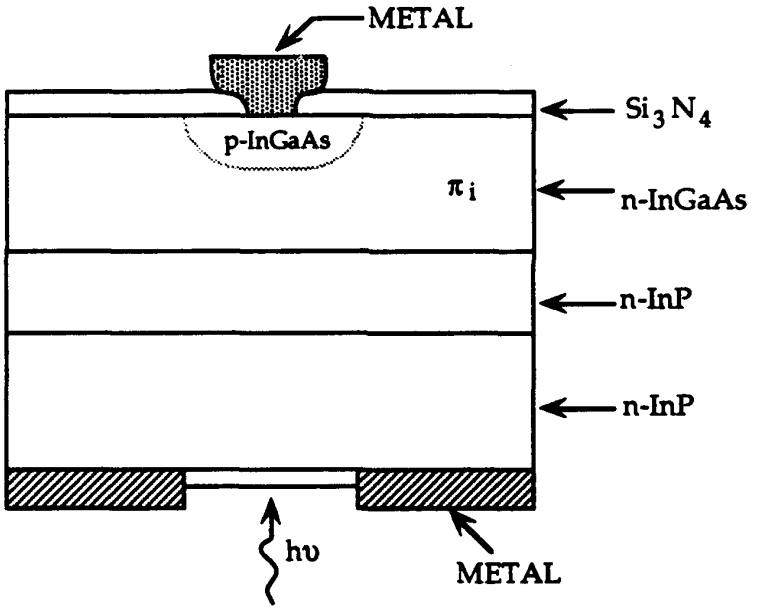


Figure 17: Cross Section of an InGaAs PIN with a Planar Structure

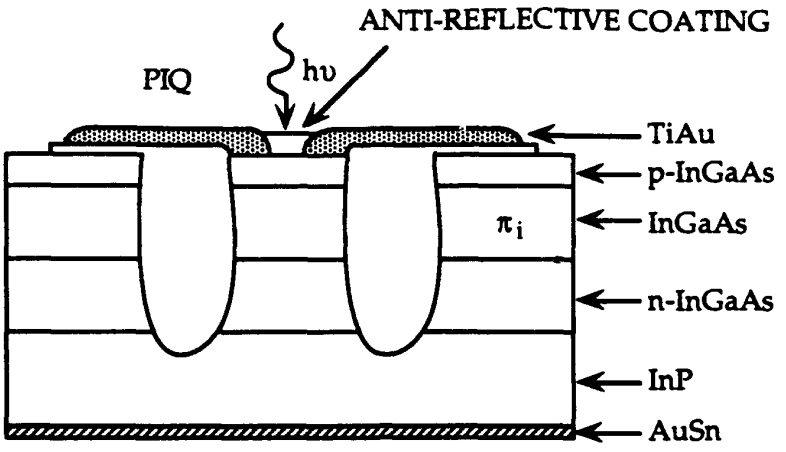


Figure 18: Cross Section of an InGaAs PIN with a Mesa Structure

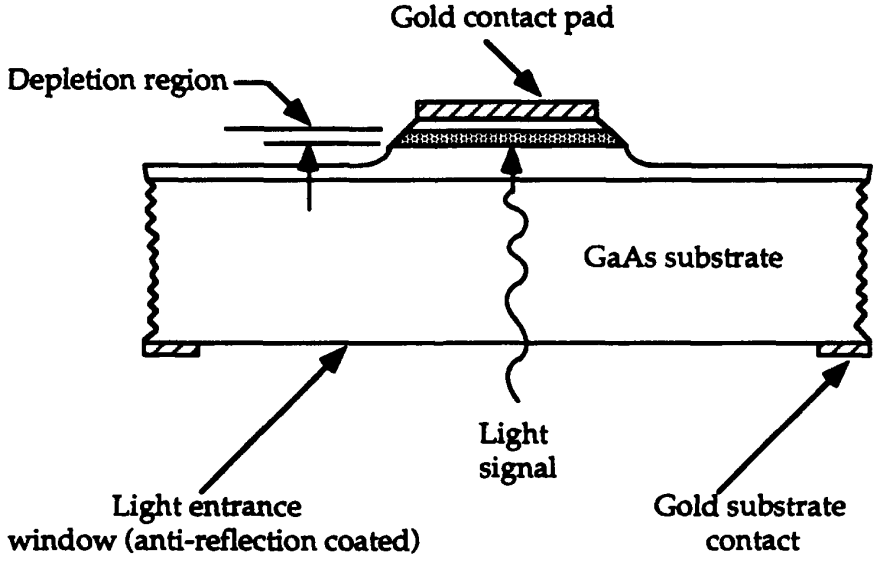


Figure 19: Schematic Diagram of an Inverted Heterojunction Mesa APD

4.0 GaAs DEVICE RELIABILITY

GaAs technology has experienced rapid growth in the past five years. The reliability improvements of GaAs microcircuit devices appear to be occurring much faster than they did originally for silicon microcircuits. It has been reported that the reliability of GaAs microcircuits in their short history has improved at rates that exceed an order of magnitude per year. (Ref. 92)

This high rate of improvement may be attributed to several factors. Techniques developed to assess and monitor the reliability and yields of silicon devices are applicable to GaAs or require limited modification. Additionally, inherent characteristics of GaAs, such as a lower electric field at peak electron velocity (7 KV/cm compared to 30 KV/cm for silicon) permits the development of GaAs devices that have lower power dissipation than silicon devices of the same function. Therefore, thermally activated failures and electromigration effects, and failures due to high electric fields may be reduced by GaAs technology.

4.1 GaAs Component Failure Mechanisms

The reliability of a device can not be measured without understanding the physics of failure for that device. Each device failure mechanisms occur at a rate which is dependent on temperature and has a unique activation energy (Ea) associated with it. This activation energy is based on the Arrhenius model. Failure mechanisms with low activation energies have low temperature dependence while those with higher activation energies have greater dependence. This chapter investigates the reliability of selected GaAs devices which include GaAs MMIC and digital integrated circuits, GaAs Field Effect Transistors, millimeter wave diodes, and photonic devices. Failure mechanisms, accelerating factors, published activation energies, and known methods to reduce or alleviate potential failure mechanisms are presented.

4.1.1 GaAs MMIC and Digital Integrated Circuits

Material and structural differences between silicon and GaAs circuits exist which can affect the reliability of GaAs ICs. The gate length of an active GaAs MMIC device may be as small as 0.25 μm. The GaAs substrate thinned to 100 μm is brittle and difficult to handle. Thermal considerations are also of importance. The thermal conductivity of GaAs is approximately one third to one fifth that of silicon. Additionally, in an elemental semiconductor technology such as silicon, device quality is a function of material purity. In a compound semiconductor such as GaAs, the material composition is of importance. For example, defects that could degrade GaAs device performance may be caused by a deficiency of arsenic atoms.

There is a need in the field of GaAs to have a better understanding of device failure modes and mechanisms. Field Effect Transistors have been found to be a major cause of GaAs IC failures. Gate sinking (the interdiffusion of the gate metal

and the GaAs) is generally considered to be a major reliability problem. Gate sinking involves the slow degradation in the contact and Schottky gate regions of GaAs MESFET components. The channel regions of the MESFET are reduced and hot spots can develop. An increase in ohmic contact resistance in the drain and source contacts of the MESFET as well as in other contacts within the IC will occur. Parametric changes in the device will be initially seen however catastrophic failures will eventually precipitate. Effects due to electromigration should also be closely monitored especially in the design of digital GaAs integrated circuits and high power GaAs MMICs where high current densities (required for shorter propogation delays) are incorporated.

Failure mechanisms have a time and temperature relationship which can be reflected by the activation energy of the Arrhenius model. Those mechanisms exhibiting lower activation energies are manifested as device failures earlier and can thus limit a device's useful life. The literature contains contradictory information on activation energies for various mechanisms. For instance the activation energy for gate sinking has been reported to be from 1.0 to 1.6 eV. It is expected that differences in reported activation energies exist since manufacturing processes, especially between HEMTs, MESFETs, microwave digital and linear devices are significantly different..

GaAs and silicon integrated circuits in general experience the same classes of failure mechanisms. They can be differentiated into three basic areas: metallization, dielectric and semiconductor. Failure mechanisms of GaAs FETs and ICs are related to interactions of gate and contact metals with the GaAs substrate at elevated temperature. The results of accelerated life test studies and corresponding device activation energies for GaAs MMIC and Digital microcircuits are outlined in Tables 4 and 5.

It is apparent from these activation energies that the failure mechanisms currently identified by industry for GaAs MMIC and digital integrated circuits are accelerated by temperature. Therefore accelerated life testing will be very successful at identifying mechanisms with high activation energies but other failure mechanisms with smaller activation energies may be masked by this testing. If other mechanisms with lower activation energies do exist, they may not be discovered until significant cumulative hours under normal operating conditions are logged. This could have an impact on reliability as the technology matures. The majority of failures associated with GaAs MMIC and digital integrated circuits result from the FETs which they are comprised of. Prior to a description of FET failure mechanisms, a description of failure mechanisms associated with other component types are presented in the following sections. Failure mechanisms associated with FETs are addressed in Section 4.1.2.

Table 4: GaAs MMIC Data Summary

Reference	Sample Size	Test Temp (°C)	Failure Rate Reference to 150°C	Activation Energy (eV)
91, 92	131	225	0.43×10^{-6}	1.60
48, 92	31	200	0.44×10^{-6}	1.60
35	17	200	1.29×10^{-6}	1.50
33	20	250	0.21×10^{-6}	1.35
34	30	220	0.78×10^{-6}	1.17

Table 5: GaAs Digital Data Summary

Reference	Sample Size	Test Temp (°C)	Failure Rate Reference to 150°C	Activation Energy (eV)
92	130	225	0.35×10^{-6}	1.60
113	658	150	4.58×10^{-6}	1.40
107	30	220	0.03×10^{-6}	1.40

4.1.1.1 Passive Component Failures

GaAs integrated circuits contain resistors, capacitors, and inductors which are subject to failure. They do not appear to be a major contributor in GaAs device failures as long as they are properly designed into the circuit. However, these components can still exhibit drift or catastrophic failure with time. Nichrome resistor life testing performed by Triquint, projected that more than 10 million hours at 100°C is needed to produce 1.5% resistance drift. Testing of capacitors resulted in no degradation. Triquint also determined that passive components exhibit a median life which is almost twice that of FETs. Results of resistor life testing are illustrated in Table 6.

Table 6: Resistor Life Test Results

Integrated Circuit Element	Sample Size	Test Temp (°C)	Failure Rate Reference to 150°C	Activation Energy (eV)
Implanted Resistors/ Ohmic Contacts	~ 90	203	0.16×10^{-6}	-----
Thin Film Resistors	70	125 150 175 200	0.31×10^{-6}	1.0

4.1.1.2 Airbridge Failures

Airbridges are subject to failure due to electromigration if the current density of a GaAs microcircuit is too high or to mechanical collapse if they are not designed properly. Airbridges are cooled primarily through the ends of the bridge and run hotter than the same metallization deposited on the chip surface. To minimize airbridge problems, the length of the bridge and the current density through it should be minimized. Triquint reported an activation energy of 0.43 eV and mechanical stability has been demonstrated by several device manufacturers. Other studies have detected particles trapped under airbridges. These trapped particles must be detected during device processing if the airbridge is to function properly. Table 7 portrays the results of airbridge life testing.

Table 7: Airbridge Life Test Results

Integrated Circuit Element	Sample Size	Test Temp (°C)	Failure Rate Reference to 150°C	Activation Energy (eV)
Air Bridge Metallization	~ 70	170	0.07×10^{-6}	0.43

4.1.1.3 Backgating-Isolation Effects

Backgating-isolation effects are the result of interactions between components on a GaAs integrated circuit. When a potential is applied to one component on a chip it can affect the operation of another device on the same chip due to a phenomena known as backgating. Backgating occurs when a depletion layer at the interface

between the channel and the semi-insulating substrate exists. Conduction through the substrate causes this depletion layer to be modulated resulting in the modulation of the channel resistance and current. Its magnitude is a function of density of deep levels or traps in the substrate.

As GaAs digital technology moves to higher package densities and larger scales of integration, backgating will play an important role in the performance of GaAs integrated circuits. It has been demonstrated that the insertion of a superlattice buffer in an HFET structure between the 2DEG and the substrate can reduce backgating. A study of backgating threshold voltage for HFET structures found a low threshold voltage for backgating implying excessive buffer layer leakage current. Yokoyama (Ref. 123) determined that independent of the substrate source that the use of molecular beam epitaxy (MBE) resulted in large backgating on both HFETs and MESFETs. Devices not using MBE growth or those incorporating a thermal etch prior to MBE growth were found to have reduced backgating. This study concluded that a conducting layer at the substrate-epitaxial layer interface was a large backgating contributor but that it could be removed by thermal etching of the wafer prior to growth.

4.1.1.4 Chip Fracture

Chip fracture can be a problem particularly for microwave power ICs that have large area thin chips. Frequently microwave power ICs have metal vias connecting the top and bottom of the chip and are eutecticly bonded to the package or substrate. This mechanism is the result of the die bonding process. When a eutectic solder fills a via, a thermal mismatch is introduced between the solder in the via and the GaAs. Fracture can result from the initial cooling or from repeated thermal cycling causing undue stress from the mismatch. Additionally, chip fracture may result if the die attach is not uniform. GaAs chips with epoxy die attach, that did not extend to the edge of the die, have been found to fracture during wirebonding.

4.1.2 GaAs Field Effect Transistors

GaAs integrated circuits have several failure mechanisms but predominant failures are associated with the FET and can be broadly grouped into "soft" and "catastrophic" categories. Soft failures are those which produce changes in DC and/or RF performance parameters. Most manufacturers have, in the absence of an industry standard, established values which indicate soft failures. Catastrophic failures are those which result in cessation of transistor action and generally are characterized by shorter terminals within the FET. A listing and brief description of soft and catastrophic failure mechanisms are found in Table 8. A comprehensive listing of activation energies for failure mechanisms identified in this section is detailed in Appendix A.

Table 8: GaAs FET Failure Mechanisms

Mechanisms	Description	Solution	Type
Gate Metal Sinking	Gate metal reacts with GaAs moving interface into channel	Non-reactive metal, control of thickness	Soft
Electromigration	Self-diffusion of drain or gate metal at high current density and temperature	Gold gate metal, control current density, coat with nitride	Catastrophic
Surface Degradation	Oxidation of GaAs releases free arsenic; Reaction with silicon dioxide causes erosion; Mobile ions in passivation	PECVD nitride passivation	Both
Ohmic Contact Degradation	Out diffusion of gallium. In diffusion of gold.	Barrier layer between contact and to gold.	Both
Instantaneous Burnout	Breakdown and melting at drain contact	n^+ ledge at drain contact	Catastrophic
Long Term Burnout	Reaction of GaAs with surface oxide release free arsenic	PECVD nitride passivation	Catastrophic
Channel Degradation	Diffusion of dopant from channel; diffusion of defects or traps into channel	No known solution	Soft
Intermetallic Phase Formation	Kirkendahl voiding due to Au-Al interdiffusion, aided by electromigration	Use of all Au system; separate Au and Al.	Soft

4.1.2.1 Gate Metal Sinking

GaAs FETs have been reported having drain current reduction with time and temperature. This mechanism has been identified as "Gate Sinking" and has an activation energy of 1.6 eV. It involves the interdiffusion of gate metal into the GaAs or the "sinking" of the gate metal causing a decrease in FET channel depth. The effect appears to be negligible for aluminum gate FET devices due to the stability of the Al-GaAs interface. It does however appear to be prominent for FETs with TiWAu, TiPdAu, and TiAu gates. The effect was first mentioned in 1982 (Ref. 15) as a potential failure mechanism, but was not reported until some time later. Rate of diffusion is a function of the gate metal system used since diffusion rate varies for different metals. Gold is a fast diffuser into GaAs and for this reason barrier metals such as TiPt, TiPd, or TiW have been typically used to retard diffusion. The mechanism causes a reduction in Idss, gm, and pinch-off voltage. Defects in barrier layer metallization can cause localized gate metal sinking. It has been found at gate edges where shadowing has occurred during deposition resulting in a thin barrier metal deposition. A reduction of 20% in drain current or up to a 500 mV threshold voltage increase is typical with this mechanism. At 300°C this degradation can occur within 20 to 40 hours.

4.1.2.2 Electromigration

Electromigration is the movement of atoms within a conductor carrying a high current caused by the momentum exchange between moving electrons and atoms. This mechanism can cause voids in the conductor causing a loss of continuity or the accumulation of metal atoms which, if become large enough, can cause shorting to other conductors. Lighter metals such as aluminum are more susceptible to this mechanism. Electromigration in aluminum can be retarded by doping with a few percent of copper. The activation energy for this mechanism has been reported between 0.5 and 1.0 eV. The mechanism has been observed in GaAs FETs with both aluminum and barrier metal gold gates. It becomes a concern for RF power FETs which simultaneously have high current densities and operate at high temperatures. Covering the metal with SiO_2 or Si_3N_4 or limiting current density will retard this failure mechanism.

4.1.2.3 Surface Degradation

Several types of surface degradation can affect the performance of GaAs field effect transistors. Unpassivated devices are susceptible to oxidation. This oxidation can result in a reduction of breakdown voltage and an increase in low voltage gate current. The reduction in breakdown voltage will cause the power output of power devices to decrease and eventually result in catastrophic failure. Devices passivated with SiO_2 can experience GaAs surface erosion due to an interaction of the SiO_2 with the GaAs. This interaction results in a narrowing of the channel and an increase in the drain and source resistance. Mobile ion contamination of the oxide

or nitride passivation can also result in FET instability. This instability is the result of the accumulation of mobile charges near the dielectric-GaAs interface. It has been found that a plasma enhanced chemical vapor deposited (PECVD) nitride layer can reduce failures resulting from surface instabilities.

4.1.2.4 Ohmic Contact Degradation

Ohmic contacts are typically formed to n-type GaAs by alloying Au/Ge or Au/Ge/Ni with the substrate at temperatures typically in excess of 360°C. For bondability and conductivity a thicker gold layer is deposited on top of the alloyed contact. The contacts are not thermally stable and with time and temperature the structure degrades due to outdiffusion of gallium into the top gold layer and the indiffusion of gold to form high resistive alloys that increase contact resistance. There is a question as to whether the contacts of current devices are still not thermally stable or whether this was just true in past devices. Metal or dielectric barrier layers such as silver, TiPt, or TiW between the AuGeNi and the top gold layer tend to retard this process.

4.1.2.5 Burn-out

It has been published that this mechanism can account for 30 to 50% of the observed failures for GaAs FETs. Burnout exists in two forms, instantaneous and long term.

4.1.2.5.1 Instantaneous Burnout

Instantaneous burnout occurs when the source to drain voltage exceeds the breakdown voltage of the device. The mechanism that causes this catastrophic failure is not clear. It has been shown that the breakdown voltage can be increased by extending the n+ layer under the contact towards the gate. The FET is then observed to have a much higher breakdown voltage (40-50 V). The breakdown, when it occurs, is associated with the substrate buffer layer. When the power dissipation of the device causes the buffer temperature to rise to 500-550°C it becomes an intrinsic conductor and thermal runaway results.

4.1.2.5.2 Long Term Burnout

Long term burnout is a result of the gradual decrease in the gate drain breakdown of the FET which occurs during dc aging. Also, surface degradation of the GaAs at the vicinity of the drain contact has been associated with this mechanism. PECVD silicon nitride passivation has been found to suppress this mechanism.

4.1.2.6 Channel Degradation

Degradation of the properties of GaAs in FET channels have been found to cause GaAs FET wearout. The mechanism, channel degradation, is accelerated by temperature. It has an activation energy of 1.5 eV and in several tests has been observed at 250°C within a few hundred hours. Several speculations to the cause of this mechanism have been proposed. Irvin has speculated that the mechanism is due to deep levels which are created in the GaAs or migrate to the channel region from the substrate due to electric fields and carrier recombination existing in the channel. Omori and Wholey have speculated that the degradation is due to either the diffusion of dopants out of the channel or the diffusion of impurities/defects from the substrate to the channel. In either case, the mechanism is not expected to be a major problem for devices operated at normal temperatures, but could limit the maximum power output that power FET devices can be reliably operated.

4.1.2.7 Intermetallic Phase Formation

This mechanism is only predominant for GaAs FETs that have aluminum gate metallization. Gold metallization has been used for wire bonding pads since it is compatible with the ohmic contact materials (AuGeNi) and the gold wires used to package the devices. Therefore an aluminum gate device requires a transition from the aluminum gate to the gold bonding pad. If this transition is not carefully designed, Al-Au intermetallics will form when the devices are stressed at higher temperatures. Aluminum metallization more recently has been utilized for wire bonding pads. In one study (Ref. 126) gold wires were ball bonded to Al/Si/Cu bonding pads. Devices were found to exhibit extensive intermetallic formation after burn-in and high temperature testing. To reduce this intermetallic problem components were assembled with aluminum wire and ultrasonically wedge bonded. Though the study did not uncover intermetallic problems between the aluminum wire and the gold plated package land bonds, there is the potential for its existance. Barrier layers such as chromium and TiPt have been found to retard intermetallic formation. It has been documented that some failures attributed to this mechanism have resulted from a misalignment in the metallization. Since the occurrence of the mechanism is a result of process design and fabrication, a screen could eliminate wafers that would be susceptible to the mechanism.

4.1.3 Millimeter Wave Diodes

GaAs impact ionization avalanche transit time (IMPATT) and gunn diodes are typically used to generate or amplify microwave signals and can produce higher power and operate at higher frequencies than FETs. Although gunn diodes produce relatively low noise, millimeter wave diodes are generally noisier than FETs. In addition there is little isolation between the input and output of these devices and impedance matching is crucial. This chapter reviews the reliability of IMPATT and gunn diodes.

4.1.3.1 Impact Ionization Avalanche Transit Time (IMPATT)

Junction temperature is a major influence on the reliability of IMPATT diodes. These diodes can experience contact metal diffusion into the semiconductor material which causes the device to short. The failure mode is influenced by device construction materials and junction temperature.

Schottky Read IMPATT diodes have been found to experience long term degradation mechanisms. The cause of this degradation relates to the migration of the platinum barrier metallization into the active area of the device. If this platinum layer is less than 200 Angstroms the reaction will cease due to the depletion of platinum and the effect on diode performance will be limited. Additionally, the penetration of gold from the final metallization layer of the diode through either diffusion or migration leading to acceptor formation and net donor density reduction can occur. Metallization systems have been developed which reduce this mechanism. Published activation energies for failure mechanisms of GaAs IMPATT diodes are presented in Table 9.

Table 9: GaAs IMPATT Diode Activation Energies

Reference	Test Temp. (°C)	Activation Energy (eV)
6	<300 (J)	0.20 -0 .40
6	<300 (J)	1.60
107	350 - 400 (J)	1.80
45	180 - 260 (J)	1.36

(J) - Junction Temperature

4.1.3.2 Gunn

Gunn Devices operate at high current and high power densities and typically require heat sinks. High power gunn devices incorporate a gold plated heat sink on the metallized contact layer of the device. Temperature is an accelerating factor in the failure modes of this device and an activation energy of 2.3 eV has been reported (Ref. 89). Many of the failure modes associated with this device occur in its early life. These failure modes include:

- Hot spot formations which are a result of mesa cracking that allows flexing of the gold plated heat sink
- Micro cracks caused during the application of lead wires to the chip
- Metallization shorts that result from excessive bonding pressure

Long term failure mechanisms for gunn devices result from interactions between materials used in the metallization and contacts of the device and from the cooling efficiency of the anode heat sink. The effect of these failure mechanisms will usually result in device shorts.

4.1.4 Photonic Devices

Gallium arsenide has been used extensively in the development of emitters that operate in the infrared region and in the design and development of photodetectors that offer increased speed and data rates over silicon counterparts. This chapter investigates the current reliability of GaAs emitters and detectors.

4.1.4.1 Emitters

The main cause to emitter failure and device parameter drift are defects that exist in the active area of the emitter. These defects may either be present in the substrate of the device or form during epitaxial growth or the manufacturing process. A description of failure mechanisms for GaAs light emitting diodes and laser diodes are presented.

4.1.4.1.1 GaAs LEDs

GaAs light emitting diodes experience degradation in their optical power which is usually the result of dark spots in the active emitting area. The presence of gold contact material in the vicinity of the active area of the device is a major influence on this mechanism. Gold acts as a non-radiative recombination center and decreases the efficiency of the device. Devices with alloyed (AuZn) top p-electrode contacts have been shown to exhibit rapid degradation at high temperature and current after about 2000 hrs. However, those utilizing Schottky barrier contacts (Ti/Pt/Au) are much more stable since the platinum acts as a barrier preventing gold migration. Though it has been shown that reliable devices can be manufactured using Schottky barrier contacts it has been found that the series resistance of these devices can increase with time. This increase is the result of the material inter-diffusion. Published activation energies for GaAs LEDs are presented in Table 10.

Table 10: GaAs LED Activation Energies

Reference	Test Temp. (°C)	Activation Energy (eV)
125	65-185 (J)	0.65-0.75
84	88-167 (J)	0.30
120	N/R	0.80

(J) - Junction temperature N/R - Not Reported

4.1.4.1.2 Laser Diodes Failure Mechanisms

Laser diode failure mechanisms can be characterized as being either catastrophic, gradual degradation, or functional degradation. Catastrophic failures are caused by optical flux density, metallization, and bonding anomolies. Gradual degradation is related to the electron hole recombination process and is dependent on the laser technology and operating conditions. Functional degradation failures are related to the ability of the laser to function in specific design applications. Published activation energies for GaAs lasers are presented in Table 11. A description of the catastrophic, gradual, and functional degradation failure mechanisms are presented in the following sections.

Table 11: GaAs Laser Diode Activation Energies

Reference	Test Temp. (°C)	Activation Energy (eV)
111	25-90 (A)	0.80
120	N/R	0.75
60	50-70 (A)	0.62
44	70(A)	0.70
59	60-100 (A)	0.90-1.30
7	40-70 (C)	0.34

(C) - Case temperature (A) - Ambient Temperature N/R- Not Reported

4.1.4.1.2.1 Catastrophic

Catastrophic degradation mechanisms fall into two categories - P-side metallization breakdown and catastrophic facet damage. P-side metallization breakdown is attributed to metal penetration into the semiconductor material. Since it is a metal diffusion process, temperature is most likely the major activating influence. Catastrophic facet damage occurs at optical power densities greater than several milliwatts per micrometer of emitting facet width after short operating times. The physical process leading to this failure mechanism is a function of the optical power density and pulse length.

4.1.4.1.2.2 Gradual Degradation

The gradual degradation of semiconductor laser diodes have been attributed to the following failure mechanisms:

- Dark line defects
- Dark spot defects
- Thermal resistance degradation
- Homogeneous degradation

- Non-catastrophic facet degradation

The nature of these mechanisms and their effect on reliability will be discussed in the following paragraphs.

Both dark line defects (DLDs) and dark spot defects (DSDs) propogate during operation. They are both regions of high non-radiative recombination so that the carriers injected into that region do not contribute to the luminescent output. Additionally, light travelling in the junction plane can be absorbed in these regions since they are regions of loss which result in a further reduction of output. It has been suggested that DSDs can develop into DLDs. Both DLDs and DSDs initiate at native defects in the semiconductor material. Sources of DLDs that have been identified include crystal edges, stacking faults, DSDs and various kinds of surface damages induced by scratches, indentations, and non-uniform bonding. Sources of DSDs are substrate dislocation, segregated impurities and macroscopic foreign particles such as carbon powder. Both DLDs and DSDs are activated by the presence of strain or temperature gradients and result in the rapid degradation of the laser. One study (Ref. 89) reported a thermal activation energy of 1.0 eV for this mechanism. These degradation mechanisms were most prevalent in earlier versions of semiconductor lasers. The newer lasers and more sophisticated manufacturing and quality assurance techniques have reduced the impact of this degradation mechanism on the life of the laser.

Thermal resistance degradation can result from contact deterioration. In Au-In metallization systems this deterioration results in an increase in thermal resistance which is due to intermetallic and void formation in the indium used to solder the Au-evaporated chip to the gold plated header. Intermetallic growth is a function of temperature, length of time exposed at the given temperature and the ratio of gold to indium.

Homogeneous degradation is a gradual degradation that occurs in lasers. This degradation process is both current density (J) and temperature dependant and reported to be caused by defects formed by small radiative centers. The number of non-radiative centers increase in proportion to the number of radiative centers resulting in reduced laser output power.

Non-catastrophic facet deterioration (erosion) is a gradual degradation of the laser facets which is caused by some photochemical reaction at the facet. The deterioration is enhanced by the ambient conditions and optical flux densities. The gradual oxidation introduces extra non-radiative recombination centers near the facet causing the

threshold to rise and introducing losses resulting in a decrease in external quantum efficiency. The presence of oxygen or moisture in the ambient gases having contact with the facet additionally accelerate facet erosion. This erosion decreases mirror reflectivity and increases the non-radiative recombination rate at the facets. Facet erosion can be prevented by coating the facet with an Al_2O_3 half wave length thick film. A half wave film is used to leave the facet reflective and threshold current unchanged. The application of a quarter wavelength thick film would decrease the reflectivity and increase the threshold current accelerating other failure mechanisms. The coating is additionally believed to provide a moisture barrier.

4.1.4.1.2.3 Functional Degradation

Functional degradation failure mechanisms fall into three categories:

- Intensity pulsations
- Optical frequency shifts
- Emission symmetry changes

The following paragraphs provide a brief description of these mechanisms and their effect on device reliability.

Intensity pulsations are self-sustained oscillations (SSOs) that have been reported to occur at frequencies between 200 MHz and 3 GHz and at a modulation depth approaching 100%. The onset of SSOs could be detrimental if the laser were utilized in a digital application. The failure mechanisms that cause SSOs have yet to be confirmed but it has been suggested that either second order mode locking or switching between two lateral filaments, effects associated with electron-photon interactions in the prescience of non-uniform gain or loss or the effect of saturable absorbers in the active region are the cause. The absorber may result from a localized region of lower population inversion caused by a region of non-radiative recombination, surface recombination at the facets or unpumped regions at the edges of the stripe. The absorption in these areas will decrease when pumping is increased, giving rise to a Q-switching effect. It has been reported that SSOs were present in new devices and that the SSOs become enhanced by forward biased operation and/or elevated temperature.

Optical frequency shifts are basically small alterations in beam direction and mode shape. It has been reported that these changes result from minor internal degradation which perturbs the cavity parameters in the junction plane without significantly changing the efficiency.

Emission symmetry changes are light intensity differences at the two ends of the laser. The light intensity at one end is not the same as the other and the difference varies with aging and drive current. One study (Ref. 113) reported that after accelerated testing that 49% of the samples tested exhibited an emission symmetry change in the light polarized perpendicular to the junction plane (TM). Emission symmetry changes in the light polarized parallel to the junction plane (TE) were also reported.

4.1.4.2 Detectors

Dark current has been reported as being the sole critical parameter to detector malfunctioning. Failure mechanisms of planar and mesa avalanche and PIN photodiodes are outlined in Table 12.

Table 12: Planar and Mesa Avalanche and PIN Photodiode Failure Mechanisms

Structure	Current Component	Failure Mechanism
Planar diffused APD/PIN	Bulk	Junction degradation Localized breakdown
Mesa	Surface	Oxide contamination

Both recoverable and non-recoverable dark current degradations in PIN detectors have been observed. The recovery rate for PIN detectors whose dark current recovers has been found to be voltage dependent with dark current at higher voltages requiring longer recovery times. Surface problems such as mobile ion contamination are the most likely culprit for this failure mechanism. Non-recoverable dark current degradation has been reported to result from localized degradation/damage to device passivation at the junction perimeter.

4.2 MMIC Packaging

The packaging of MMICs require special consideration and therefore are addressed in this section. The characteristic impedance of MMIC packages usually need to be matched to a specific value since after it is packaged the tuning of a MMIC circuit is not desirable or in many cases possible. Additionally, packaging is a major influence in device reliability. Manufacturing techniques used in MMIC packaging include:

- glass sealed ceramic enclosures with thin film metallization
- ceramic enclosures with thick film metallization
- metal enclosures with ceramic feedthroughs
- metal enclosures with glass feedthroughs

Packaging for GaAs MMICs must be able to provide support to the die while offering protection from environmental stresses such as vibration, acceleration, thermal shock and temperature and still allow the MMIC to have good performance at high frequencies. When using GaAs, especially for MMICs and digital ICs, package design is crucial to device performance. Noise and cross-talk caused by very fast rise and fall times must be minimized. The loading of transmission lines must be kept low to minimize ringing and voltage standing wave ratio. Generally, a MMIC package capable of providing good performance should provide:

- low insertion loss and VSWR per lead feed-through
- good isolation between leads
- microstrip compatibility
- thermal management
- protection from the environment
- low cost in reasonable volume

Until recently microcircuit package design primarily considered application defined issues such as cost, configuration, reliability, and weight. However, MMIC devices with their extremely high clock rates and fast rise times require special attention to electrical characteristics. A MMIC package must be able to effectively transfer the electrical performance of a device to the system level. Propogation delays caused by the device package or interconnection system can limit the speed of a MMIC device. Propogation delay is a major consideration in MMIC package design and is represented by Voltage Square Wave Ratio (VSWR). Signal quality and performance can be affected by the characteristic impedance device transmission lines. Transmission line impedance must match specific device input values which are usually 50 or 75 ohms. The transmission lines must terminate with a resistance value that matches the line impedance since unterminated lines could result in propogation delays, signal degradation, ringing , or reflections. Cross talk or mutual coupling can occur if the isolation between ports and high density wiring layouts is not effective. To optimize device performance a MMIC package must be designed to minimize insertion loss. Package leads, pins, and their attachment method must be designed in such a way that load fluctuations are prevented while maintaining characteristic impedance uniformity. Additionally inefficient interconnection coupling can cause return loss (VSWR) and result in performance degradation. Power supply disturbances can raise havoc with high speed MMIC devices. In order to reduce signal delays and false switching decoupling capacitors can be utilized at or near power junctions.

Though MMIC packages have special considerations regarding electrical characteristics, the requirements of MIL-STD-883 must be considered when implementing or designing a MMIC package. Packaging must withstand shock and vibration, be hermetic, chemically inert, and be thermally conductive and insulating over a device's intended temperature range. Environment can play an important role in the failure mechanisms of GaAs MMIC devices and can not be forgotten.

4.3 Electrostatic Discharge (ESD) Sensitivity

Electrostatic Discharge (ESD) is the transfer of electrostatic charge between bodies at different electrostatic potentials caused by direct contact or induced by an electrostatic field. These charges can be great enough to cause damage to either GaAs or silicon electronic devices. ESD testing performed on depletion mode MESFET based GaAs integrated circuits and circuit elements have indicated that the majority of GaAs devices are sensitive to pulses under 2000 Volts. Table 13 provides a comparison of the ESD sensitivity of GaAs and silicon devices.

Table 13: ESD Sensitivity of GaAs and Silicon Devices

Technology	ESD Sensitive Voltage Range
Bipolar Transistors	380 - 7000 V
CMOS	250 - 3000 V
ECL	500 - 3000 V
GaAs FET	100 - 300 V
JFET	140 - 7000 V
MOSFET	100 - 200 V
Schottky TTL	1000 - 2500 V

Three ESD sensitivity classifications are defined by DOD-STD-1686 and DOD-HDBK-263. These classifications are defined as:

Class 1: Items which can be damaged by 0 to 1000 volts
Class 2: Items which can be damaged by 1000 to 4000 volts
Class 3: Items which can be damaged by 4000 to 15000 volts

From these classifications and the data presented it is clear that devices manufactured using both silicon and GaAs are susceptible to ESD damage. Therefore static control methods must be routinely used in manufacturing, assembly and test areas for microwave products employing these devices. Some manufacturers have incorporated device protection into their designs. Rugged shunt diodes are typically connected between the input traces and to sensitive input gates of the FET and ground. Similarly they have been installed on local oscillator input gates. These diodes are able to absorb ESD transient pulses with no damage to the diodes or gates that they are intended to protect.

4.4 Radiation Resistance

It is of importance that electronic devices used in space, military, and in nuclear applications be able to withstand exposure to radiation environments. Semiconductor devices are susceptible to radiation that may come from various

sources including alpha particles emitted from packaging materials. One of the primary advantages of GaAs devices and ICs over their silicon counterparts is their high tolerance to radiation exposure. GaAs ICs are inherently one to two orders of magnitude more resistant to radiation than the most radiation resistant silicon devices. This radiation resistance is a result of a semi-insulating substrate which eliminates the need to junction isolate between devices and the lack of a gate oxide which has a tendency to charge when exposed to radiation.

The term radiation accounts for both high energy photons (x-ray and gamma rays) and high energy particles (electrons, protons, neutrons, etc.). Atomic collisions and electronic ionization are responsible for the radiation effects of semiconductor devices. Atomic collisions displace atoms from their normal position in the crystal lattice creating a vacancy and an interstitial atom. Traps in the energy band gap are generated which results in a decrease in carrier concentration and bandgap. Ionization is the removal of electrons from the semiconductor atoms producing ions and free electrons. Radiation tolerance levels of GaAs devices can differ due to component manufacturing and design differences. GaAs devices have been shown to operate under continuous radiation of 10^6 rads. The effects of transient radiation however, have not been determined and are currently being investigated. Figure 20 compares the radiation hardness of GaAs to silicon devices.

GaAs devices are able to withstand a higher tolerance of radiation exposure than silicon manufactured devices. The MIMIC program requires that MMIC devices be able to withstand doses of transient radiation of at least 10^8 rads per second and goals of 10^9 rads per second (at a 100 nanosecond pulse) have been established. Additionally they must be able to withstand a radiation pulse of 10^7 rads per second (100 nanosecond pulse) without transient upset and while in operation function after a neutron dose of at least 10^1 neutrons/cm^2.

GaAs semiconductors are susceptible to both temporary and permanent damage from radiation. Temporary damage usually is a result of ionization radiation creating electron hole pairs that result in device voltage and current disturbances. Permanent damage results from atomic collisions or from charge transfer. Charge transfer is the transfer of charge from radiation to an insulating portion of the device. Charge transfer has little effect on GaAs, however it can affect coatings (i.e., nitrides) used in device manufacture causing changes in device performance.

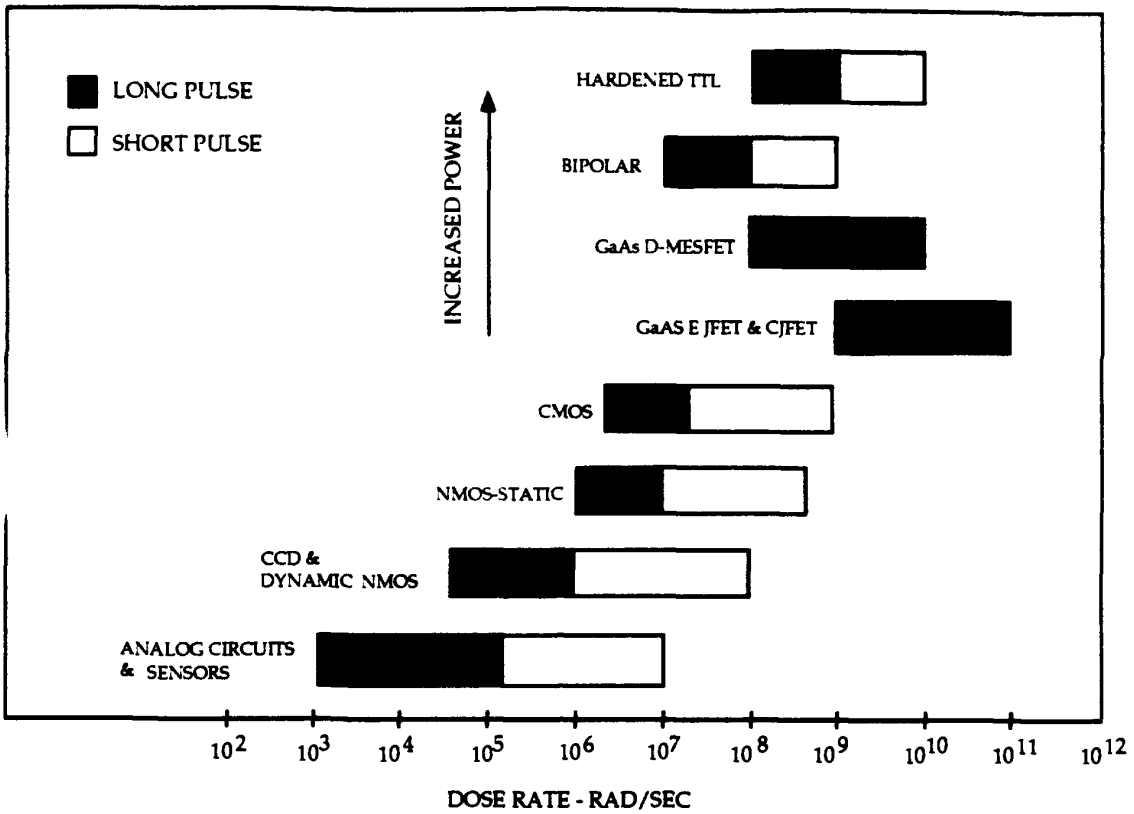


Figure 20: Radiation Hardness of GaAs and Silicon Devices

5.0 GaAs PRODUCT EVALUATION AND RELIABILITY ASSURANCE

GaAs, once thought of as a technology of the future, is rapidly becoming utilized in both military and commercial systems. Its performance advantages, which are detailed throughout this report, have started this trend. To assure insertion of the GaAs technology into all environments, device reliability test and analysis efforts and device cost reduction (especially for GaAs integrated circuits) must continue. The various DoD reliability efforts in place to further these goals are described in section 6.0.

Additionally, several critical issues which must be considered are outlined below:

- All possible failure mechanisms of GaAs devices must be identified (see Section 4.1). Additionally, the following characteristics must be fully understood: temperature dependence, time to failure characteristics, probability of occurrence relative to other mechanisms whether defect related or common cause, process variations, the underlying physics and their affect on different active and passive structures.

- Potential screening techniques must be identified for each mechanism. The level at which these techiques are performed (wafer, package, assembly), their cost effectiveness and screening effectiveness (probability of identifying a weak part with the screen) must also be considered.

- Data analysis must be effectively performed with a full understanding of the statistical significance of results and whether the results agree with physics of failure principles.

- The QML concept must be fully understood so that the accurate and timely identification and elimination of failure mechanisms, through the use of reliability physics and knowledge based, well designed Process Monitors (PMs), Technology Characterization Vehicles (TCVs) and Standard Evaluation Circuits (SECs) at various test conditions will be most effective.

The GaAs community is gaining a better understanding of the failure modes, mechanisms and analyses but some contradictory information on activation energies for various mechanisms exists in the literature. For instance, the activation energy for gate sinking (the interdiffusion of gate metal and the GaAs) has been reported to be from 1.0 to 1.6 eV. The MESFET gate sinking problem is generally conceded to be one of the predominant reliability problem for a mature line. For this mechanism, temperature is the major accelerating stress and RF operation is not required for reliability assessment. The high activation energy for

this mechanism results in two problems. The first is the need for accurate temperature measurements and hot spots locations. The second problem is that so much emphasis has been placed on the high activation energy problems that can be accelerated significantly by temperature, that low activation energy and RF induced failure modes have not received proper attention. Recently NRL (Naval Research Laboratory) ran a test on 14 MMIC devices using both RF and temperature for stress testing. The failures were about equally distributed between burnout and loss of over 20% in power output. Electromigration of AuGe ohmic contact metallization was the suspected mechanism. The activation energy was measured to be only 0.5 eV. A review of other testing shows that in general, RF testing produces more burnout failures while DC testing generally results in slow degradation failures. These types of problems require further investigation

The major reason for analyzing failures is to determine the physical mechanisms that caused the failure to facilitate future corrective actions. Therefore a failure, if well understood, can be duplicated at will. When proper corrective action is taken, parts that will pass or fail a specific test should be predicted with a high level of confidence prior to the test. Using this failure analysis technique, first pass success at every step of the process can be achieved. Also, any test methods and procedures developed are based on documented data with well defined boundary conditions. If these boundary conditions change in the future, the methods and procedures can be efficiently altered based on historically documented data.

In performing detailed failure analyses to support the technique described above, there are three major considerations that distinguish GaAs from silicon devices. The most obvious is the need for special fixturing and test set-ups for accurate RF measurements. The second is the brittle nature of GaAs which makes cross-sectioning of the devices and wafer difficult. Thirdly, the special elements used in GaAs technology such as airbridges, substrate vias, inductors, and to a lesser extent, resistors and capacitors, present unique failure analysis challenges.

While DoD programs are addressing GaAs IC reliability and yield, the development of QML procedures (discussed later in this section) for GaAs IC devices is critical to assuring reliability. These procedures will provide the means for the DoD to procure from manufacturers who demonstrate the ability to consistently produce reliable products.

5.1 Product Evaluation

When the need for a product type has been determined, vendor selection begins. The procurement of any device, either packaged or in chip form, requires a disciplined program for supplier selection, evaluation and certification. Due to the relative infancy of GaAs technology and its vendors, it is recommended that a diligent approach be taken to assure trouble free, timely and cost effective receipt of product. There are many references on this subject and most agree on five necessary criteria:

- Quality
- Delivery
- Technical Support
- Management Attitude
- Cost

It is recommended that the QML concept defined in MIL-I-38535 be used as a model to certify suppliers. The procedure detailed below can be modified to buy material, third party services (i.e., design, foundry, packaging and assembly), unpackaged die and hermetically sealed components.

5.2 Reliability Assurance

The system usage of GaAs devices is occurring in two forms; unpackaged die for inclusion in hybrid microcircuits (i.e., T/R modules) and discrete hermetic packaged devices. For both cases, the Qualified Manufacturers List (QML) program will be tailored to assure the quality and reliability of GaAs devices.

A recent DoD technology assessment report identified six key elements to excellence in manufacturing. They are:

- Recognition of manufacturing as a strategic factor
- Concurrent design of product and life cycle processes
- Emphasis on quality
- Continuous improvement
- Workforce and their education
- Vendor and user working relationships

The QML approach emphasizes these elements in assuring microcircuit quality, reliability, and rapid insertion into electronic systems.

The DoD has recently implemented the QML system for the procurement of microcircuits to complement the existing Qualified Products List (QPL) system. Specifications used are MIL-H-38534, General Specification for Hybrid Microcircuits, and MIL-I-38535, General Specification for Integrated Circuits Manufacturing, which utilizes "generic qualification."

Device qualification is burdensome when the process is applied to complex microcircuits such as Application Specific Integrated Circuits (ASICs) where quick turn around and low volumes are involved. These problems have been addressed through the development of a process oriented system known as generic qualification. The process defined in MIL-I-38535, certifies and qualifies the design, fabrication, assembly, and test for a given technology, not individual devices. Manufacturers who successfully complete the requirements of MIL-I-38535 will be

listed on a Qualified Manufacturers List (QML) and all products built and tested on the QML flow will be qualified for use in military systems.

The main goal of any qualification system is to stress quality and reliability throughout all phases of the product development and build. The implementation of a TQM Program, an initiative for continuously improving performance at every level, has been embraced by Generic Qualification as the cornerstone for quality and reliability improvement and assurance. Every manufacturer who applies for QML status must demonstrate implementation of the TQM principles outlined in Table 14. The manufacturers approach is then assessed during certification and qualification.

Table 14: TQM Principles (from DoD TQM Pamphlet 1988)

TQM PRINCIPLES	
Continuous Process Improvement	Constancy of Purpose
Process Knowledge	Total Involvement
User Focus	Teamwork
Commitment	Investment in People
Top-Down Implementation	

To assure that all aspects of the device fabrication are involved, the manufacturer must establish a Technology Review Board (TRB) which is chaired by management and consists of key individuals from necessary disciplines such as design, fabrication, mask making, assembly, package and test. The TRB is responsible for the implementation of a TQM program throughout the entire manufacturing operation and for the establishment of well controlled, understood and stable processes which are the key foundations of a quality product.

The approval of process control involves review of a manufacturer's TQM implementation documentation including: Quality Improvement Plan, Statistical Process Control (SPC) program, Field Failure Return Program, Corrective Action Plans, Change Control and Product Recall Program. These procedures typically exist in every manufacturing facility, but are seldom brought within the cognizance of a controlling umbrella. Effective utilization of TQM assures their control by the TRB who is solely responsible for the development and implementation of these plans and processes. This responsibility may be delegated, but the TRB must monitor to guarantee their implementation and accomplishment.

5.2.1 QML Requirements

MIL-I-38535 is divided into five areas of requirements as shown in Table 15. The first area involves the establishment of a TRB and a TQM program which was outlined earlier.

Table 15: QML Requirements

Phase 1	TQM Program Technology Review Board - TQM Implementation - Controlled, Stable Process
Phase 2	Certification - Document Process Control - Demonstrate Process Capability - Validation Review
Phase 3	Qualification - Complex Product Built/Tested
Phase 4	Product Procurement Specification - Customer Interface - Critical Parameters
Phase 5	Product Tests - Screening - Electrical/Mechanical - Sample Testing

The certification and qualification requirements assess whether the TRB has accomplished their tasks and validates the technology flow. Certification, a three step process involves: documentation of process control, demonstration of process capability, and validation review by qualifying activity. This phase is the key step in assuring the building blocks for a technology flow are verified for completeness by the manufacturer and validated by the Qualifying Activity.

The demonstration of process capability is the most involved portion of the certification phase where each of the key disciplines, model verification, chip performance, layout verification, and testability/fault coverage verification are tested to assess their capabilities. Under model verification, for example, the manufacturer must demonstrate how fabrication process models, are developed, verified and controlled. Some key indicators are whether the manufacturer continuously strives to improve these models and sets sigma limits on the output of the tools.

The chip performance requirement assesses how well the manufacturer's post-layout simulation predicts the measured results over temperature and voltage. The layout verification refers to the rules used to check a design. These include: design, electrical and reliability rules. Table 16 defines, in more detail, what these rules entail. For digital circuits, the manufacturer must demonstrate a capability to design utilizing testability. A fault coverage measurement capability, (fault simulation, test algorithm analysis, etc.) in accordance with procedures defined in MIL-STD-883, test method 5012 must also be demonstrated. For non-digital circuits this requirement is

not applicable but may be included as measures of analog fault coverage become better defined. The fault coverage measurements requirement however fully applies to the digital portion of microcircuits which contain analog and digital portions. The results of all these requirements' assessments are deliverable to the Qualifying Activity before the Validation Review is scheduled.

Table 16: Layout Verification

DESIGN RULES	ELECTRICAL RULES	RELIABILITY RULES
Geometric Physical	Connectivity Opens/Shorts	Single Event Upset (SEU) IR Drop ESD Hot Electron Latchup Electromigration

To assess the capability of the fabrication process, the manufacturer must build and test a group of test structures. These include the Technology Characterization Vehicle (TCV), Process Monitor (PM), and Standard Evaluation Circuit (SEC). The roles that each of these play in establishing and controlling the stability, quality and reliability of the fabrication process are described in Table 17.

Table 17: Fabrication Test Vehicles

Test Vehicles	Role
Technology Control Vehicle	Assess Intrinsic Reliability Failure Mechanisms
Process Monitors	Assess Electrical Characteristics of Wafer After or During Processing
Standard Evaluation Circuit	Assess Process Reliability

The assembly, package and test areas also require a process capability including modeling of package electrical and mechanical characteristics, control of assembly materials, assessment of moisture control in packages and evaluation of final tests. Once all the processes have been assessed, the manufacturer demonstrates and evaluates the interfaces between the building blocks for completeness.

MIL-H-38534 and MIL-I-38535 tailored for GaAs will include requirements from the GaAs boule to final module or device testing.

5.2.2 MIL-I-38534 Device Criteria

Developing the GaAs criteria for MIL-I-38535 is an on-going project including representatives from both government and industry. During the evaluation of MIL-I-38535 for inclusion of GaAs requirements, it became apparent that only minor changes would be required to the main body of the document. However, major changes are required in sections needing criteria specific for GaAs technology devices such as process monitors (PM), technology characterization vehicles (TCV) and the definition of a standard evaluation circuit (SEC) for baselining the manufacturer's process. Table 18 and the following paragraphs highlight the proposed changes to MIL-I-38535 for GaAs RF/Microwave devices.

The MIL-I-38535 section which discusses the implementation of TQM/QML philosophy and establishment of the TRB requires very few changes. The major change proposed will allow shipment of compliant QML unpackaged chips and wafers to users for final assembly into modules, the predominant end use for analog microwave devices. Note, that this criterion is not GaAs specific but is required to meet the manufacturer and users needs for shipping and receiving compliant QML chips for end use.

Significant changes are required in the process capability demonstration portion of the specification. The main concern was that the GaAs device models being developed by industry are not as accurate as the device models which currently exist in other technologies. Another area of concern are the testability requirements. The following short term solution has been proposed. For non-digital microcircuits, testability is not applicable, but will be supplemented as measures of analog fault coverage are defined. For microcircuits with both analog and digital functions, testability requirements apply only to the digital portions of the microcircuit. Therefore, only the digital portions of a microcircuit design will be required to demonstrate 99% or greater fault coverage. (Ref. 69).

Table 18: MIL-I-38535 Potential Changes

PARA NO.	POTENTIAL CHANGE
1.1	Include unpackaged devices
3.4.2.2	Add, GaAs specifics
3.4.3.1	Add, unpackaged device criteria
3.4.4.1a	Change to design library
3.4.4.2k	Add, glassivation
3.4.4.2	Add, following processes • Gate Formation • Ohmic Contact Formation • Backside • Starting Materials Qualification
3.4.4.3b	Add, ribbon interconnect
3.5.1.2	Add, fabrication to and from materials
3.5.1.3.1a	Add, transistor modeling
3.5.1.3.1b	Add, backgating to reliability rules
3.5.1.3.1d	Identify analog fault coverage applicability
3.5.1.3.2a4	Add, or concentration after diffusion
3.5.1.3.2a7	Replace etch with resultant
3.5.1.3.2a9	Add, and/or implant anneal after diffusion
3.5.1.3.2a19	Add, and Via hole process
3.5.1.3.2a	Add, following new process • *gate formation* • *air bridge*
3.5.1.3.2b	Add, gate sinking, ohmic contact degradation and backgating after (TDDB)
3.5.1.3.2c	Allow glassivation, if required for the device and technology being characterized. Also allow use of suitable TCV packaging. Add sinking gate, ohmic contact degradation and backgating test stucture requirements to TCV
3.5.1.3.2d	Identify when a SEC is required, SEC packaging and SEC complexity requirements
3.5.1.3.2e	Add, RHA test structure requirements, GaAs PM parameters and fast test structures, i.e., contact resistance, gate diffusion
3.5.1.3.3	Include TM 5013 for use
3.5.1.3.5	Add, ribbon bond
3.5.1.4.3	Add, wafer boule evaluation, ribbon bonding
3.5.2.1	Clarify microcircuit design qualification
3.5.2.1.2	Allow usage of suitable packaging
3.7	Add, unpackaged die marking requirements
3.7.8	Add, unpackaged die container marking requirements
4.2.2	Require traceability to wafer level
4.2.6.2	Add, passivation
4.3.4	Identify alternate visual does not apply
Table VIII	Clarify unpackaged device testing
Table IX	Clarify unpackaged device testing

Three new test structures have been identified for inclusion in a Technology Characterization Vehicle (TCV) to account for unique GaAs failure mechanisms. These are gate sinking, ohmic contact degradation and backgating test structures. For "chip" QML packaging evaluation the following has been added: TCV test structures shall be packaged, if possible, using the same packaging materials and assembly procedures used for standard circuits in the technology. Additionally, TCVs may be packaged in a suitable package that does not compromise testing (Ref. 69) to qualify the chip technology.

A standard evaluation circuit definition for analog microcircuits has been proposed. The digital device definition states that for digital microcircuits, the complexity of the SEC microcircuit shall contain, as a minimum, one half the number of transistors expected to be used in the largest microcircuit to be built on the QML line. (Ref. 69) It was decided that the analog SEC definition would stress functions and not complexity even though complexity is still a concern. For analog microcircuits, the SEC shall exercise the functionality of the process technology flow, be of representative complexity and comprised of major circuit element types. (Ref. 69) Provisions for housing the SEC are similar to those specified for the TCV.

A new paragraph will be added to the process monitor (PM) section for GaAs specific parameters (i.e., sheet resistance, MIM Capacitor, Fat FET, isolation, ohmic contacts and GaAs parameters (Idss, gm, pinch-off, etc.)

Only editorial changes are necessary in the assembly and packaging requirements of the specification because the extensive packaging tests presently required are not technology specific.

Extensive changes are contemplated in the screening/technology conformance inspection requirements. First, wafer acceptance would be accomplished per the new MIL-STD-883, TM 5013. Burn-in conditions and criteria are not resolved but are being discussed by the government and industry through the JEDEC JC13.6 committee, responsible for RF/Microwave technology devices. In addition, lot acceptance of all GaAs chip/wafers submitted for final assembly in a hybrid or module is required. The lot acceptance is based on a reduced sample size (proposed 10(0)) and will consist of wafer acceptance, burn-in, bond strength, die shear, and visual examination. QML requirements were included to address both packaged and chip requirements. Package level screens such as temperature cycle, constant acceleration, seal and external visual were effectively eliminated. Also wafer traceability will be required for GaAs devices only until the technology matures.

The criteria presented are proposals and could be revised based on beta-site implementation of criteria for GaAs technology devices.

5.2.3 MIL-H-38534 Module Criteria

The module criteria for MIL-H-38534 is being developed by government and industry representatives. It has been determined that an additional appendix would be the best way to incorporate the new requirements. Major changes are the inclusion of a TRB, a statistical process control (SPC) program and alternative methods to achieve quality and reliability requirements. The following paragraph highlights the proposed changes to MIL-H-38534 and related issues.

The appendix provides requirements taken from MIL-I-38535, for the structure, duties, and responsibilities of the TRB. The TRB may modify the requirements of MIL-H-38534 provided that the TRB has the reliability data supporting the change and the modification will not adversely affect the quality and reliability of the product. The TRB must keep the qualifying activity updated on the reliability status of the QML technology and notify the qualifying activity when making a change in the manufacturers baseline. GaAs issues, similar to those outlined in MIL-I-38535, currently being addressed are: die shear and burn-in requirements, element evaluation and visual inspection. For example, if GaAs chips are bought from a qualified QML supplier, element evaluation can be waived. The TRB will also perform analysis of the current hybrid requirements and based on the data collected recommend modification of the specification requirements.

Implementation of the QML concept through MIL-H-38534 and MIL-I-38535 and its utilization by both users and OEM's will result in reliable, cost effective and timely insertion of GaAs devices into high technology systems.

6.0 SUMMARY OF THE MIMIC PROGRAM

The Defense Advanced Research Project Agency (DARPA) and other DoD agencies have provided support to the GaAs industry to establish pilot production lines for digital and analog GaAs integrated circuits. This support has been provided through several different programs such as include the DARPA Digital Insertion Program, US Air Force MANTECH program and the Microwave/Millimeter Wave Monolithic IC (MIMIC) Program. The MIMIC program is one of the largest of the DoD sponsored programs and will be addressed by this section.

The overall objective of the 7 year, 3 phase, $577 million MIMIC program is twofold. It will allow the development of high performance, low cost microwave and millimeter wave circuits and subsystems that meet DoD requirements. Also, since the design and manufacturing capabilities developed will be made available to all US contractors developing hardware for the DoD, the overall US industrial market base for the production of GaAs integrated circuits will be strengthened. During the performance of the MIMIC program the following tasks will be accomplished:

- Controllable and robust processing capabilities will be developed. MMIC chips with high yields will be produced.
- On-wafer testing of MMIC devices will be developed. This testing will determine if chips and wafers are within specifications early in the fabrication process and ensure that additional processing steps are not performed on devices that do not meet specifications. Contactless wafer probing techniques will be investigated.
- A standardized computer aided design (CAD) system that allows a wide variety of software tools from different organizations to function on it will be developed.
- Modern production disciplines such as QML will be used during the design, fabrication, and testing to ensure low cost reliable devices.

The program began in the fall of 1985 when the Office of the Undersecretary of Defense for Research and Advanced Technology initiated the Microwave/Millimeter-wave Monolithic Integrated Circuit (MIMIC) program. A one year study to define the development program of state of the art GaAs analog integrated circuits, devices, materials, packaging and testing was performed. Twelve primary and four secondary teams participated in the developmental phase.

On May 20, 1988 the DoD announced the awards of phase 1 MIMIC teams. Four contractor teams which consisted of 26 individual companies were awarded contracts totalling $225 million. Phase 1 is the first of two 3 year hardware development phases under the MIMIC program. Prime contractors for this phase

include ITT/Martin Marietta, Hughes/GE, Raytheon/Texas Instruments, and TRW. Companies that comprise each MIMIC team are:

ITT (microwave applications)/ Martin Marietta (mm-wave)
- Alpha Industries
- Pacific Monolithics (modeling)
- Watkins Johnson (packaging)
- Harris Government Systems
- TriQuint (foundry)

Hughes (airborne radar)/GE (ground-based radar)
- E-Systems (GPS)
- AT&T (foundry)
- Harris-Microwave (foundry and development work)
- Cascade Microtech (DC and RF probing & noise measuring techniques)
- Hercules (systems associate)
- EEsof

Raytheon/Texas Instruments
- General Dynamics
- Norden systems (radar applications)
- Teledyne Microelectronics (EW applications)
- Compact Software
- Consillium Inc., (CAD/CAM)
- Litton Airtron (GaAs materials)
- Aerojet (smart munitions)
- Magnavox (communications)

TRW
- Honeywell (smart munitions)
- General Dynamics/Pomona
- Hittite (MOFA-HDL)

Each MIMIC phase 1 team has the expertise required to accomplish one or more of the technical portions of the program. These areas include gallium arsenide material growth, wafer development, device and circuit modeling, computer aided manufacturing, packaging, automated test equipment, and microwave system development. The MIMIC program is additionally comprised of two further phases. Phase 2 is a second three year hardware development program that will build on the achievements of phase 1. Phase 3 runs in parallel with phases 1 and 2 and includes specialized technological efforts that assist in meeting the overall objective of the MIMIC program.

MIMIC components and the manufacturing capability required to produce them will be developed during phases 1 and 2 of the MIMIC program. MIMIC components produced during phase 1 will be inserted in several military equipments to demonstrate the overall benefits of this technology. Proposed phase 1 system insertions are outlined for each phase 1 team in Figures 21 through 24.

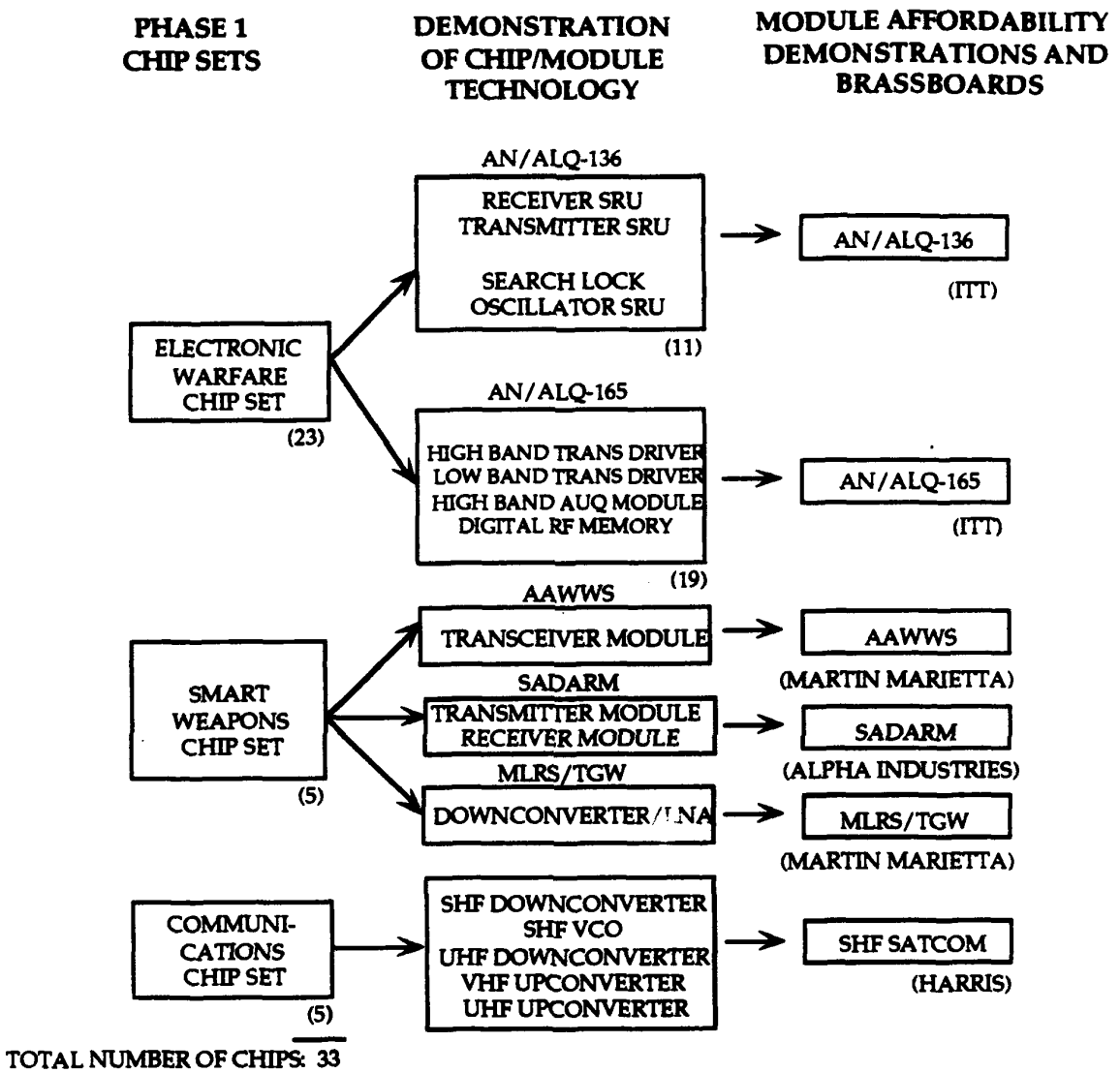


Figure 21: ITT/Martin Marietta Team Hardware Demonstrations are Focused on Electronic Warfare, Smart Weapons and Communications

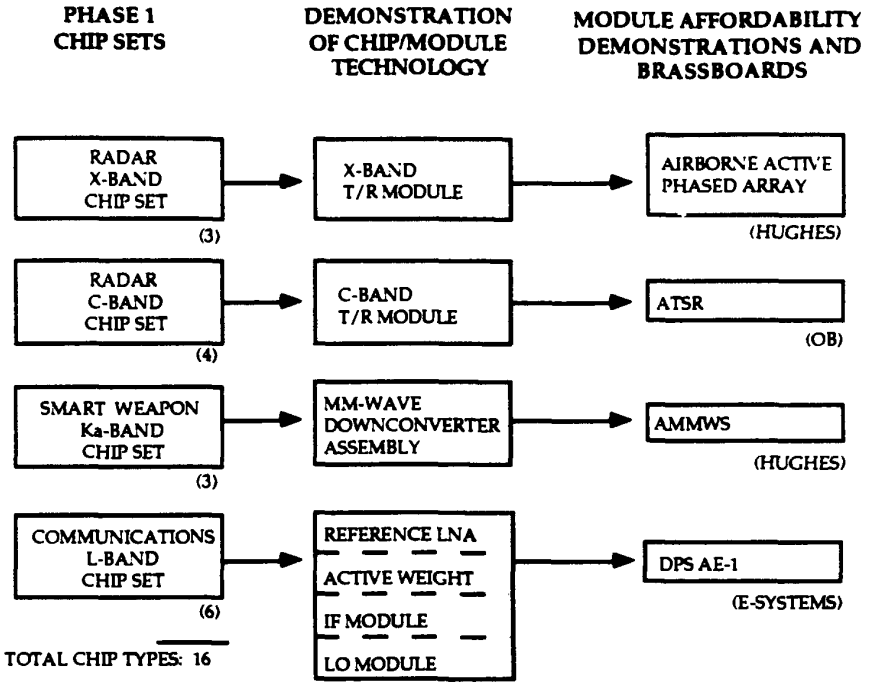


Figure 22: Hughes/GE Team Hardware Demonstrations are Focused on Radar, Smart Weapons and Communications

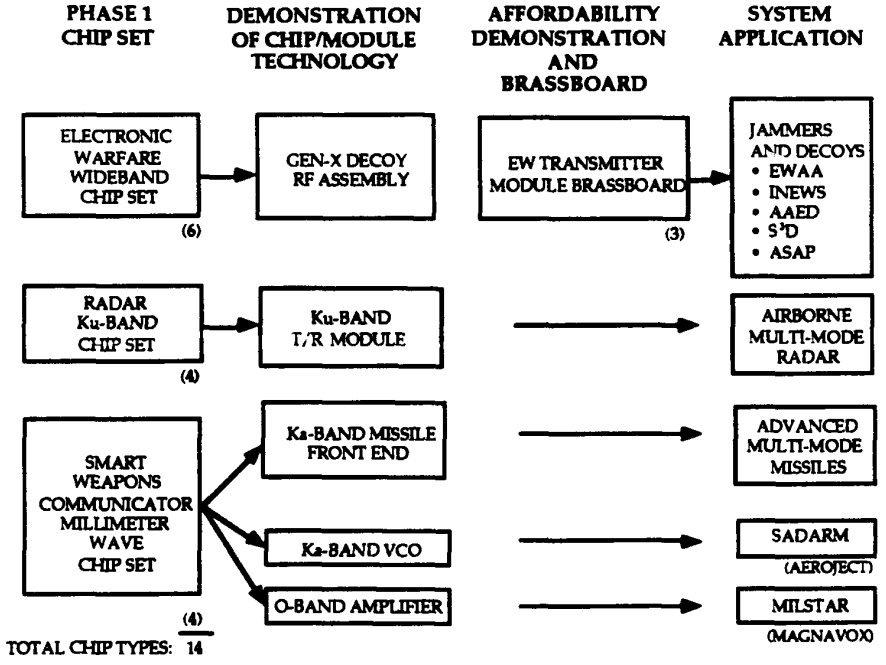


Figure 23: Raytheon/TI MMIC Team is Developing Wideband Chip Sets for EW and Millimeter-wave ICs for Smart Weapons and Communications

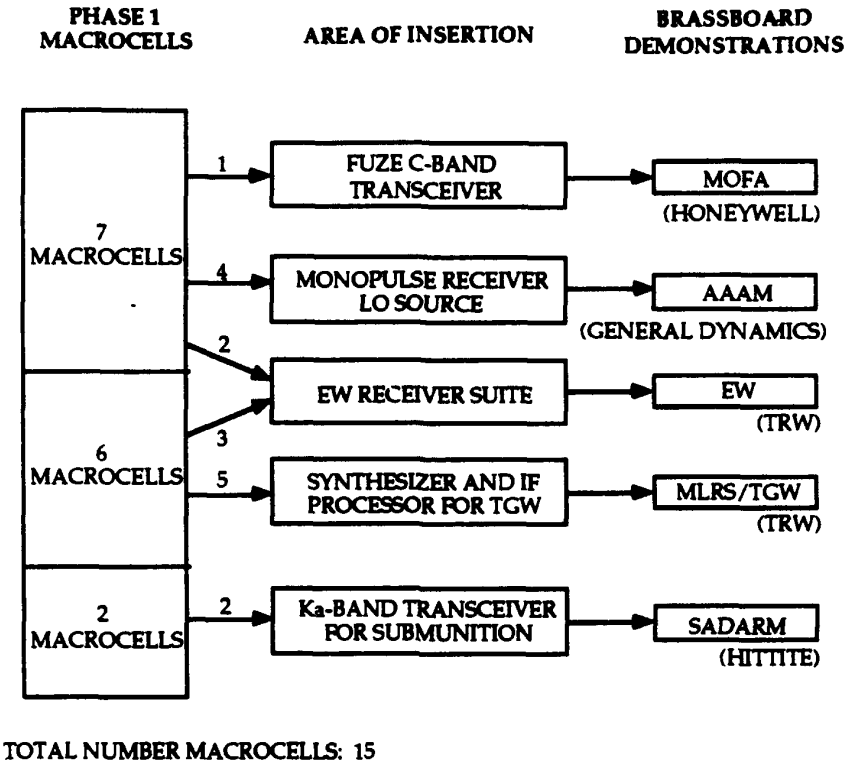


Figure 24: TRW is Building Macrocells for use in Fuzing, Electronic Warfare and Submunitions

At the conclusion of phase 1, the second phase of MIMIC hardware development will commence. A number of phase 3 efforts which run in parallel with phase 1 and 2 have been awarded. These projects are primarily in the areas of computer aided design (CAD), automated test equipment (ATE), and improved material growth techniques. Phase 3 offers the opportunity for universities and smaller companies to become involved. Phase 3 efforts include awards to the following organizations:

CAD Support
- Gateway Modelling Inc.
- North Carolina State University
- University of Colorado

Material Support
- Spire Corporation
- Varian Associates Molecular Beam
- Epitaxy Operation

Automated Testing
- AT&T Bell Labs
- Ball Communications Systems Division
- Comsat Laboratories Microelectronics Division
- M/A-COM Advanced Semiconductor Division
- Varian Associates Research Center

Process/Device Construction Support
- ITT Avionics
- TRW
- Avantek Inc.
- Triquint Semiconductor Inc.

The Microwave and Millimeter Wave Monolithic Integrated Circuit Program provides the required resources and structure to transition years of research and development in GaAs technology into a production process. The MIMIC program will provide a 10 to 100:1 reduction in the size and weight over presently used circuits, a 100:1 improvement in reliability, a 30:1 reduction in device part count, and a 10 to 20:1 reduction in life cycle cost. Through combined and cooperative industry support and the assurance that the design and manufacturing capabilities developed will be available to all US contractors developing electronic hardware and systems for the DoD, the MIMIC program will provide the framework for reliable and low cost GaAs MMIC devices.

7.0 GaAs RELIABILITY PREDICTION METHODOLOGIES

Reliability prediction models as found in MIL-HDBK-217E (Ref. 68) are used to determine trade-offs between various system designs, to provide a baseline measurement of system reliability, and to assist in producing an optimally reliable design. It is imperative that major reliability risks in system designs be accurately identified and eliminated prior to manufacture without unnecessary reliability design complications. Reliability prediction models must be capable of estimating the reliability of each component comprising a system. There currently does not exist a GaAs integrated circuit reliability prediction model in MIL-HDBK-217E, although there does exist a GaAs discrete FET model. Several models have been developed which address GaAs reliability predictions for both monolithic IC's and discrete FET's. These models are presented in this section.

There are several uses for reliability prediction models. First, they are often contractually required by the government, to be used by systems development engineers in the reliability assessment of proposed designs. A second use for reliability models are for device manufacturers to model failure mechanisms to insure that manufacturing processes are under control and producing high quality products. Models for these two uses have inherently different goals and are based on different types of data.

Typically, a requirement for models used by systems engineers is that they be relatively simple and based on easily accessible information that is available to engineers in the design phases. This information usually includes application specific information such as temperature and operating environment, and also includes device variables that are available in the device specification or data sheet. Examples of such models are those contained in MIL-HDBK-217.

The second type of model used by manufacturers typically rely on very specific manufacturing data that is usually available to the device manufacturer. The detailed form of the "VHSIC/VHSIC Like Reliability Model" (Ref. 13) (of which some aspects are to be presented later in this section) is an example of this type of model. This model includes factors such as chip area an defect density, which are typically available only to the manufacturer of the device. Table 19 summarizes the pros and cons of each of these model types.

Table 19: Pros/Cons of Each Model Type

MODEL TYPE	PROS	CONS
Models used by systems engineers (Generic models)	• Easy to use • Based on readily accessible data • Provide an industry average failure rate	• Cannot be based on fundamental parameters that affect reliability • Limited accuracy • Relies on field data and thus requires long lead times for development
Manufacturers model	• More accurate than generic models • Based on fundamental reliability parameters • Since they are based on fabrication data, short development times are possible	• Can only be used by manufacturers or those with access to detailed fabrication data • Relatively complex and difficult to use

Failure mechanisms or causes can generally be grouped into two categories; common cause and special cause. These two types of mechanisms have very different failure characteristics and must be treated separately in a reliability model.

Common cause failures are due to inherent failure mechanisms that have the potential of affecting the entire population of parts. An example of these mechanisms is electromigration. This is a mechanism which can be controlled through design and fabrication to insure the device is robust enough to operate reliably for a given period of time under a given set of conditions. For these mechanisms, physics based reliability models are appropriate since the mechanisms are typically well understood.

Special cause failure mechanisms are those resulting from defects or from events. Examples of these are metallization failures resulting from voids or thinning metal and electrical overstress. Since these mechanisms are defect or event related, they tend to occur in a random manner and thus typically exhibit decreasing or constant failure rates. For these mechanisms, purely physics based models are not appropriate due to the random nature of their occurrence. For this reason, models based on the statistical analysis of empirical data are usually the appropriate modeling alternative.

The intent of this report section is to present several reliability models for GaAs devices, analyze their strengths and weaknesses, and present a model form which may be used in the future at a time when more laboratory and field data are available.

7.1 TI's Model

Ruff (Ref. 94) has proposed a methodology to derive a GaAs failure rate from the median life times obtained from life data in conjunction with existing MIL-HDBK-217 GaAs model. This methodology basically converts an observed median life to an average worst case failure rate and uses this for a new base failure rate in the GaAs FET model of MIL-HDBK-217. It also uses test results at various temperatures in conjunction with the Arrhenius relationship to derive an activation energy and hence a temperature dependent failure rate. All other MIL-HDBK-217 model factors are left intact.

The model then extrapolates the failure rate of individual GaAs FET's to MMIC's (with n transistors) with;

$$\lambda_{MMIC} = \sum_{i=1}^{n} \lambda_{FET}$$

The model also proposes a correction factor similar to that contained in MIL-HDBK-217 to account for the fact that the failure rate does not increase linearly with the number of transistors (n). This proposed correction factor is;

$$\pi_C = \frac{1}{\sqrt{n}}$$

Ruff also notes that if additional failure mechanisms or modes are present, they should be accounted for by deriving a failure rate in a manner similar to that which has been done for FET's. He also points out, however, that the preliminary test results of MMIC's indicate that the FET is the primary cause of failure. This observation is corroborated by others as evidenced by discussions elsewhere in this publication.

The advantages and disadvantages for the approach proposed by Ruff are summarized in Table 20.

Table 20: Advantages and Disadvantages of Ruff's Approach

ADVANTAGES	DISADVANTAGES
• Temperature of individual FET's can be accounted for	• Assumes only FET failures
• Uses empirical data	• Assumes MIL-HDBK-217 GaAs FET model form is valid for MMIC devices

7.2 Westinghouse Model

In May 1990 a report (RADC-TR-90-72) (Ref. 35) containing a reliability prediction model for GaAs integrated circuits was published. The GaAs model was developed from information obtained through industry contacts, surveys and from published sources. The model developed dealt primarily with GaAs MMICs and GaAs digital circuits. Separate models for MMIC and digital GaAs IC's were developed due to the significant processing differences that existed between the two circuit types. The differences as outlined by Westinghouse include the following:

- GaAs MMICs typically use depletion mode MESFETs with fewer transistors dissipating more power than digital circuits which tend to use more smaller size depletion or enhancement mode MESFETs that dissipate less power.

- MMICs use many capacitors, inductors, resistors, and gold based air bridge interconnects. Digital GaAs circuits do not incorporate air bridge interconnects.

- Higher frequency MMICs require additional controls over interconnect and substrate dimensions to ensure good quality transmission line interconnects.

- MMIC devices use more extensive backside processing steps because of the low inductance ground connections that are required. This can increase the thermal conductivity through the MMIC substrate. This does not pertain to digital GaAs circuits.

In light of these differences two independent GaAs MMIC and GaAs digital IC reliability prediction models were developed. These models are summarized on the following pages.

DESCRIPTION
Gallium Arsenide Microwave Monolithic Integrated Circuit (GaAs MMIC) and GaAs Digital Integrated Circuits using MESFET Transistors and Gold Based Metallization

$$\lambda_p = [(C_{1A} \pi_{TA} + C_{1P} \pi_{TP}) \pi_A + C_2 \pi_E] \pi_L \pi_Q \text{ Failures/}10^6 \text{ Hours}$$

MMIC: Die Complexity Failure Rates - C_{1A} and C_{1P}

Complexity (No. of Elements)	C_{1A}	C_{1P}
1 to 10	4.5	2.3
11 to 100	7.2	2.9

1. C_{1A} accounts for the following active elements: transistors, diodes.
2. C_{1P} accounts for the following passive elements: resistors, capacitors, inductors.

Digital: Die Complexity Failure Rates - C_{1A} and C_{1P}

Complexity (No. of Elements)	C_{1A}	C_{1P}
1 to 1000	25	.69
1,001 to 10,000	51	.69

1. C_{1A} accounts for the following active elements: transistors, diodes.
2. C_{1P} accounts for the following passive elements: resistors, capacitors, inductors.

Device Application Factor - π_A

Application	π_A
MMIC Devices	
Low Noise & Low Power (≤ 100 mW)	1.0
Driver & High Power (>100 mW)	3.0
Unknown	3.0
Digital Devices	
All Digital Applications	1.0

Package Failure Rate for all Microcircuits - C_2

Package Type					
Number of Functional Pins, N_p	DIPs w/Solder or Weld Seal, Pin Grid Array (PGA), Plastic DIPs[1]	DIPs with Glass Seal[2]	Flatpacks with Axial Leads on 50 Mil Centers[3]	Cans[4]	SMT (Leaded and Nonleaded)[5]
3	.00092	.00047	.00022	.00027	.00061
4	.0013	.00073	.00037	.00049	.0010
6	.0019	.0013	.00078	.0011	.0022
8	.0026	.0021	.0013	.0020	.0036
10	.0034	.0029	.0020	.0031	.0055
12	.0041	.0038	.0028	.0044	.0076
14	.0048	.0048	.0037	.0060	.010
16	.0056	.0059	.0047	.0079	.013
18	.0064	.0071	.0058		.016
22	.0079	.0096	.0083		.023
24	.0087	.011	.0098		.027
28	.010	.014			.036
36	.013	.020			.056
40	.015	.024			.068
64	.025	.048			.16
80	.032				.24
128	.053				.57
180	.076				1.1
224	.097				1.6

1. $C_2 = 2.8 \times 10^{-4} (N_p)^{1.08}$
2. $C_2 = 9.0 \times 10^{-5} (N_p)^{1.51}$
3. $C_2 = 3.0 \times 10^{-5} (N_p)^{1.82}$
4. $C_2 = 3.0 \times 10^{-5} (N_p)^{2.01}$
5. $C_2 = 8.28 \times 10^{-5} (N_p)^{1.82}$

NOTE: If DIP Seal type is unknown, assume glass.

Temperature Factor For All Microcircuits - π_T

	GaAs MMIC Active Devices, π_{TA}	GaAs Digital Active Devices, π_{TA}	GaAs Passive Devices (MMIC & Digital), π_{TP}
Ea(eV) → T_J (°C)	1.5	1.4	.43
25	3.3e-09	1.0e-08	7.1e-04
30	8.6e-09	2.5e-08	9.4e-04
35	2.2e-08	6.0e-08	1.2e-03
40	5.4e-08	1.4e-07	1.6e-03
45	1.3e-07	3.2e-07	2.0e-03
50	3.0e-07	7.0e-07	2.6e-03
55	6.8e-07	1.5e-06	3.3e-03
60	1.5e-06	3.2e-06	4.1e-03
65	3.3e-06	6.5e-06	5.2e-03
70	6.9e-06	1.3e-05	6.4e-03
75	1.4e-05	2.6e-05	7.9e-03
80	2.9e-05	5.0e-05	9.7e-03
85	5.8e-05	9.5e-05	1.2e-02
90	1.1e-04	1.8e-04	1.4e-02
95	2.2e-04	3.2e-04	1.7e-02
100	4.1e-04	5.9e-04	2.1e-02
105	7.5e-04	1.0e-03	2.5e-02
110	1.4e-03	1.8e-03	2.9e-02
115	2.5e-03	3.1e-03	3.5e-02
120	4.3e-03	5.4e-03	4.1e-02
125	7.6e-03	9.0e-03	4.8e-02
130	1.3e-02	1.5e-02	5.6e-02
135	2.2e-02	2.4e-02	6.5e-02
140	3.7e-02	4.0e-02	7.5e-02
145	6.1e-02	6.3e-02	8.7e-02
150	1.0e-01	1.0e-01	1.0e-01
155	1.6e-01	1.6e-01	1.1e-01
160	2.6e-01	2.4e-01	1.3e-01
165	4.1e-01	3.7e-01	1.5e-01
170	6.4e-01	5.6e-01	1.7e-01
175	9.9e-01	8.5e-01	1.9e-01

$$\pi_T = .1 \exp\left(\frac{-Ea}{8.63 \times 10^{-5}}\left(\frac{1}{T_J + 273} - \frac{1}{298}\right)\right)$$ Silicon Devices

$$\pi_T = .1 \exp\left(\frac{-Ea}{8.63 \times 10^{-5}}\left(\frac{1}{T_J + 273} - \frac{1}{423}\right)\right)$$ GaAs Devices

E_a = Effective Activation Energy (eV) (Shown Above)

T_J = Worst Case Junction Temperature (Silicon Devices) or Average Active Device Channel Temperature (GaAs Devices). See Section 5.11 (or Section 5.12 for Hybrids) for T_J Determination.

NOTE: $T_J = T_C + P\theta_{JC}$

T_C = Case Temperature (°C)

P = Device Power Dissipation (W)

θ_{JC} = Junction to Case Thermal Resistance (°C/W)

θ_{JC} should be obtained from the device manufacturer or from the default values shown in Section 5.11 for the closest equivalent device.

Environment Factor - π_E

Environment	π_E
G_B	.5
G_F	2.0
G_M	4.0
N_S	4.0
N_U	6.0
A_{IC}	4.0
A_{IF}	5.0
A_{UC}	5.0
A_{UF}	8.0
A_{RW}	8.0
S_F	.50
M_F	5.0
M_L	12
C_L	220

Learning Factor - π_L

Years in Production, Y	π_L
≤ .1	2.0
.5	1.8
1.0	1.5
1.5	1.2
≥ 2.0	1.0

$\pi_L = .01 \exp(5.35 - .35Y)$

Common Quality Factors

Description	π_Q
Procured in full accordance with MIL-M-38510, Class S requirements. Screens 1-12 shown below (8S).	0.7
Procured in full accordance with MIL-M-38510, Class B requirements. Screens 3, 4, 5, 6, 8B, 9, 10, 12 shown below.	1.0
Parts with normal reliability screening and manufacturer's quality assurance practices. Burn-in per MIL-STD-883, Method 1015 (Series), Class B, and final electrical testing at component rated temperature extremes. Screens 8B and 9 shown below.	3.3
Commerical (or non-MIL standard) parts with no screening other than final electrical test at component rated temperature extremes. Screen 9 shown below.	6.5
Parts screened to quality levels other than those shown above.	See note for custom screening program

NOTE: This table is derived from the table shown below and is provided for easy reference. For custom and intermediate screening programs π_Q is determined by dividing 71.3 by the sum of the point valuations, as determined below. Nonhermetic parts should be used only in controlled environments.

Quality Factor Calculation - π_Q

No.	MIL-STD-883 Method	Screen	Point Valuation
1	5007	Wafer Lot Acceptance Testing	0.5
2	2023	Non-destructive Bond Pull	0.2
3	2010/17	Internal Visual Examination	6.0
4	1008	Stabilization Bake, Condition B Minimum	4.5
5	1010	Temperature Cycling, Condition B Minimum	11.6
6	2001	Constant Acceleration, Condition B Minimum	12.8*
7	2020	PIND (Particle Impact Noise Detection)	11.3*
8 (S/B)	1015	Burn-in (S-Level/B-Level)	16.3/10.9
9	5005	Final Electrical Testing at Temperature Extremes	10.9
10	1014	Seal Test (Test Conditions A, B or C)	7.3*
11	2012	Radiography	11.3
12	2009	External Visual Inspection	7.3

* Not Meaningful for Plastic Parts. Point Valuation = 0 for Plastics.

$$\pi_Q = \frac{71.3}{\Sigma \text{ Point Valuations}}$$

Commercial Part with No Screening or unknown Screening Level	$\pi_Q = 10$

7.3 Model Extrapolation Examples

This section of the report presents an example of a model which is not based on test data or field data, but rather is based on an extrapolation from MIL-HDBK-217E models. Although not actually a model, it is being presented to illustrate techniques that are being used in the absence of accepted failure rate models. This particular example being presented uses the ratio of MIL-HDBK-217E failure rates of discrete GaAs FET and Si FET transistors to extrapolate the MIL-HDBK-217E Si monolithic failure to GaAs MMIC's. This premise is illustrated as follows;

$$\frac{\lambda_{GD}}{\lambda_{SD}} = \frac{\lambda_{GM}}{\lambda_{SM}}$$

λ_{GD} = GaAs FET Discrete Failure Rate

λ_{GM} = GaAs MMIC Failure Rate

λ_{SD} = Si FET Discrete Failure Rate

λ_{SM} = Si Monolithic Failure Rate

These values were calculated under a specific set of conditions (temperature, environment, quality, complexity, etc.)

Such approaches may seem attractive in the absence of accepted failure rate models, especially considering the pressure that equipment contractors are under to perform a reliability prediction on all constituent parts of a design. However, there are several problems with such an approach;

- It assumes that similar failure mechanisms are present in discrete and monolithic devices (both GaAs and Si), where in fact very different mechanisms occur.
- It assumes the process maturity ratio for Si/GaAs discrete is the same as that for monolithics
- It assumes some degree of commonality between GaAs and silicon monolithics when in fact they are entirely different technologies.

7.4 MIL-HDBK-217E GaAs FET Model

The current version of MIL-HDBK-217 contains a model for high and low power discrete GaAs FET transistors. This model is summarized as follows;

GaAs Power FET

Part operating failure rate model (λ_p) for GaAs power FETs (output power ≥ 100 mW):

$$\lambda_p = \lambda_b \pi_A \pi_m \pi_Q \pi_T \pi_E \quad \text{Failures}/10^6 \text{ operating hours}$$

where:

λ_b = base failure rate, Table 21

π_A = application factor
- = 1.0, pulsed applications
- = 5.0, CW applications

π_m = matching network factor
- = 1.0, input and output internal matching
- = 2.0, input internal matching
- = 4.0, no internal matching

π_Q = quality factor, Table 22

π_T = temperature factor, Table 23

π_E = environmental factor, Table 24

Table 21: GaAs Power FET Base Failure Rates (λ_b)

Operating Frequency (GHz)	Average Output Power (Watts)					
	.1	.5	1	2	4	6
4	.054	.066	.084	.14	.36	.96
5	.083	.10	.13	.21	.56	1.5
6	.13	.16	.20	.32	.85	2.3
7	.20	.24	.30	.50	1.3	3.5
8	.30	.37	.47	.76	2.0	
9	.46	.56	.72	1.2		
10	.71	.87	1.1	1.8		

$$\lambda_b = .0093 \exp(.429(f) + .486(P))$$

where:

f = Frequency (GHz)
P = Average Output Power (Watts)

GaAs FET

Part operating failure rate model (λ_p) for GaAs FETs (output power < 100 mW):

$$\lambda_p = \lambda_b \pi_A \pi_Q \pi_T \pi_E \quad \text{Failures}/10^{6} \text{ operating hours}$$

where:

λ_b = base failure rate
= .052

π_A = application factor
= 1.0, low noise
= 7.1, driver

π_Q = quality factor, Table 22

π_T = temperature factor, Table 23

π_E = environmental factor, Table 24

Table 22: Quality Factors (π_Q)

Quality Class	RF Transistors (1) (Group VI, VII)
JANTXV	0.5
JANTX	1.0
JAN	2.0
Lower	5.0
Plastic	-

(1) For RF Power Transistors (≥ 200 MHz and avg. power ≥ watt), JANTXV quality class must include IR scan for die attach and screen barrier layer pinholes on gold metallized devices.

Table 23: Temperature Factor for Transistors (π_T)

Junction/Channel Temp. (°C)	GaAs FETs
25	1.0
35	1.6
45	2.6
55	4.0
65	5.9
75	8.7
85	12
95	18
105	24
115	33
125	44
135	58
145	75
155	97
165	123
175	154

$$\pi_T = \exp\left(-4485\left(\frac{1}{T_j + 273} - \frac{1}{298}\right)\right)$$

where:

T_j = junction/channel temperature (°C)

Table 24: Environmental Factors for Discrete Semiconductor Devices (π_E)

Environment	High Frequency Diodes and Transistors (Groups II, VI, VII)
G_B	1.0
G_{MS}	1.1
G_F	2.0
G_M	4.9
M_P	4.9
N_{SB}	3.6
N_S	4.7
N_U	11
N_{UU}	11
N_H	11
A_{IC}	3.7
A_{IT}	3.7
A_{IB}	3.7
A_{IA}	4.6
A_{IF}	4.6
A_{UC}	7.0
A_{UT}	7.0
A_{UB}	7.0
A_{UA}	12
A_{UF}	12
A_{RW}	16
U_{SL}	22
S_F	1.0
M_{FF}	7.5
M_{FA}	11
M_L	55
C_L	250

The primary data set used to derive this model is given in Table 25, which has been extracted from RAC publication DSR-4. (Ref. 87).

An interesting analysis in the study developing these models centered around the exponential probability density function of discrete semiconductors. Since the analysis used a relatively large data set of GaAs devices, it will be further discussed in the following paragraphs.

The primary purpose of failure rate prediction models for electronic components such as those in MIL-HDBK-217E is to estimate the reliability of electronic equipment and systems. Such failure rate prediction models are based upon the assumption of an exponential time-to-failure distribution, which assumes a constant failure rate over time.

However, most failure mechanisms of discrete semiconductor devices investigated in the literature reportedly follow a log-normal failure distribution. An investigation of such data was conducted to determine the validity of an exponential approximation in this light. The analysis presented in this section was performed by IIT Research Institute under contract to Rome Laboratory (formerly Rome Air Development Center) (contract number F30602-85-C-0131).

There are many practical reasons why the assumption of a constant failure rate is preferred to a time-dependent failure rate for MIL-HDBK-217E type failure rate prediction models.

- **Simplicity** - The mean time between failures (MTBF) of a system whose component parts exhibit constant failure rates is not time dependent. Alternatively, for a system made up of components having nonconstant failure rates, the system MTBF will be time-dependent and is therefore undefined unless a particular mission time is specified. The assumption of exponentiality allows for failure rates to be summed in a series reliability network.

- **Precedent** - The exponential assumption is currently used for the electronic components in accepted models such as those in MIL-HDBK-217E.

- **Data Availability** - If any distribution other than exponential is assumed, the parameters of the distribution must be determined by analysis of cumulative time-to-failure data. This detailed information is seldom available for field data sources. The exponential distribution allows population parameter estimates to be made based upon total part operating hours and total number of failures.

Table 25: Test Data

Test Type: TEST
Device: TRANSISTOR, MICROWAVE/RF, FIELD EFFECT

Part Number	Slash Number	Equipment Reference	Package Type	Semi. Material	Quality Level	App Env.	Temp °C	Rated Power (W)	Voltage Stress	Current Stress	Freq. Band	Duty Cyc.	Parts Tested	Number Failed	Part Hours (E06)	Failure Rate (F/10^6 Hrs.)
--	--	N/A	--	GaAs	--	---	175J	5.20000	--	--	C	--	139	1	1.059500	0.94384
--	--	N/A	--	GaAs	--	---	210J	5.20000	--	--	C	--	36	0	0.015320	--
--	--	N/A	--	GaAs	--	---	228J	0.25000	--	--	X	--	7	4	0.014387	278.02878
--	--	N/A	--	GaAs	--	---	200J	5.20000	--	--	C	--	6	0	0.134100	--
--	--	N/A	--	GaAs	--	---	210J	5.20000	--	--	C	--	24	0	0.147800	--
--	--	N/A	--	GaAs	--	---	210J	5.20000	--	--	C	--	14	0	0.028100	--
--	--	N/A	--	GaAs	--	---	250J	5.20000	--	--	C	--	16	0	0.063500	--
--	--	N/A	--	GaAs	--	---	250J	5.20000	--	--	C	--	16	0	0.097800	--
--	--	N/A	--	GaAs	--	---	275J	--	--	--	C	--	--	1	0.000109	9174.31193
--	--	N/A	--	GaAs	--	---	228J	0.11000	--	--	X	--	--	4	0.008400	476.19048
--	--	N/A	--	GaAs	--	---	218J	0.19000	--	--	X	--	--	0	0.00260	--
--	--	N/A	--	GaAs	--	---	220J	<0.10000	--	--	C	--	--	30	0.021160	1417.76938
--	--	N/A	--	GaAs	--	---	274J	--	--	--	X	--	--	3	0.000825	3636.36364
--	--	N/A	--	GaAs	--	---	218J	--	--	--	X	--	--	1	0.001800	555.55556
--	--	N/A	--	GaAs	--	---	275J	1.00000	--	--	C	--	--	13	0.008500	1529.41176
--	--	N/A	--	GaAs	--	---	225J	1.00000	--	--	C	--	--	4	0.077100	51.88067
--	--	N/A	--	GaAs	--	---	208J	2.50000	--	--	C	--	--	8	0.033000	242.42424
--	--	N/A	--	GaAs	--	---	240J	<0.110000	--	--	C	--	--	24	0.022960	1045.29617
--	--	N/A	--	GaAs	--	---	150J	2.00000	--	--	C	--	--	8	0.014000	571.42857
--	--	N/A	--	GaAs	--	---	190J	2.00000	--	--	C	--	--	11	0.004200	2619.04762
--	--	N/A	--	GaAs	--	---	225J	2.00000	--	--	C	--	--	6	0.001040	5769.23077
--	--	N/A	--	GaAs	--	---	180J	6.00000	--	--	C	--	--	8	0.068960	116.00928
--	--	N/A	--	GaAs	--	---	240J	6.00000	--	--	C	--	--	8	0.027300	293.04029
--	--	N/A	--	GaAs	--	---	270J	6.00000	--	--	C	--	--	8	0.006560	1219.51220
--	--	N/A	--	GaAs	--	---	240J	<0.10000	--	--	C	--	--	5	0.004765	1049.31794
--	--	N/A	--	GaAs	--	---	280J	--	--	--	X	--	--	7	0.000840	8333.33333
--	--	N/A	--	GaAs	--	---	260J	<0.10000	--	--	C	--	--	22	0.012600	1746.03175
--	--	N/A	--	GaAs	--	---	200J	<0.10000	--	--	C	--	--	6	0.010000	600.00000
--	--	N/A	--	GaAs	--	---	265J	2.50000	--	--	C	--	--	66	0.088000	750.00000
--	--	N/A	--	GaAs	--	---	220J	<0.10000	--	--	C	--	--	10	0.007800	1282.05128
--	--	N/A	--	GaAs	--	---	160J	2.50000	--	--	C	--	--	4	0.146000	27.39726
--	--	N/A	--	GaAs	--	---	230J	--	--	--	C	--	--	1	0.001645	607.90274
--	--	N/A	--	GaAs	--	---	250J	1.00000	--	--	C	--	--	10	0.105000	95.23810
--	--	N/A	--	GaAs	--	---	260J	<0.10000	--	--	C	--	--	11	0.003300	3333.33333
--	--	N/A	--	GaAs	--	---	200J	--	--	--	X	--	--	1	0.002200	454.54545
--	--	N/A	--	GaAs	--	---	249J	--	--	--	X	--	--	1	0.000620	1612.90323
--	--	N/A	--	GaAs	--	---	255J	--	--	--	C	--	--	1	0.000254	3937.00787
--	--	N/A	--	GaAs	--	---	200J	<0.10000	--	--	C	--	--	21	0.026539	791.28829
RLK 9027	--	N/A	--	GaAs	--	---	280J	0.50000	--	--	X	--	7	7	0.000900	7777.77778

- **Accuracy** - When developing models such as those employed in MIL-HDBK-217E, any improvement in model accuracy resulting from the use of a more complex distribution (than exponential) may be insignificant when compared to the inherent variability associated with reliability prediction and the "statistical noise" in the data.

An analysis of constant versus time-dependent failure rate distributions was undertaken using observed time-to-failure data collected for this databook. However, due to the above-mentioned advantages, it was predetermined that if discrete semiconductor failure rate prediction models could be established as accurately with an exponential time-to-failure distribution as by a log-normal or other time dependent failure distribution, the former is preferable.

The following paragraphs describe the analysis procedure followed.

All time-to-failure data for discrete semiconductor components were extracted from the available literature. This data consisted of life test results at high temperature. Ideally, it would have been preferable to analyze time-to-failure field data since such data would more closely approximate the actual usage environments. However, such data is not available. High temperature life time-to-failure data was available for the following device types:

Low Noise GaAs FETs
High power GaAs FETs
General Purpose Transistors (NPN & PNP)
GaAs Laser Diodes
IMPATT Diodes
Schottky Diodes

Weibull analysis was then applied. The Weibull distribution is particularly useful in analyzing life data since (1) it has repeatedly been observed to provide a good fit to the data, and (2) it is a flexible distribution which can approximate many other statistical distributions, depending upon the value of β, the shape parameter. Table 26 gives some shapes of the Weibull distribution which approximate other common distributions. The form of the Weibull distribution varies between texts, but a common one is given by the probability density function:

$$f(t) = \frac{\beta}{\alpha}\left(\frac{t}{\alpha}\right)^{\beta-1} \exp\left(-\left(\frac{t}{\alpha}\right)^{\beta}\right)$$

where:

$f(t)$ = Weibull probability density function
β = shape parameter
α = scale parameter (characteristic life)
t = time

Table 26: Weibull Shape Parameters

SHAPE PARAMETER, β	DISTRIBUTION TYPE
β < 1	Gamma (k < 1)
β = 1	Exponential
β = 2	Rayleigh
β = 3.44	Normal (approx.)

Twenty-one individual data sets were plotted on the Weibull probability paper, and the value of β was determined. The results of this step of the analysis were encouraging since, as can be seen from the plots, the values of β seemed to center around 1.0. Table 27 presents a summary of the best fit Weibull parameters.

Table 27: Observed Weibull Parameters

TEMPERATURE (°C)(1)	β	α
200(Tc)	1.15	600
70 (Tc)	.69	4,400
55 (Tc)	1.25	8,000
70 (Tc)	.82	5,200
70 (Tc)	.95	230
70 (Tc)	.57	10,000
245 (Tc)	1.10	950
231 (Ta)	1.60	580
90 (Tc) 220 (T_j)	1.15	1,300
90 (Tc) 220 (T_j)	.75	2,000
70 (Ta)	.87	8,000
20 (Tc)	1.05	6,000
300 (T_j)	1.60	4,000
228 (T_j)	1.00	2,700
200 (Ta)	1.20	1,600
200 (Ta)	.73	1,500
220 (Ta)	1.00	500
220 (Ta)	1.32	700
85 (Ta)	.85	3,100
120 (Ta)	1.00	2,100
240 (Ta)	1.46	1,200

NOTES: (1) Tc = case temperature
Ta = ambient temperature
T_j = junction temperature

The next step of the analysis was to force the best line with $\beta = 1.0$ through the observed data points. The Kolmogorov-Smirnov (K-S) goodness-of-fit test was then applied to the forced line. The intent of this step was to determine the degree of error resulting from the exponential assumption. To apply the test, the value of the D statistics, the largest deviation of the observed from expected or theoretical value is compared to the standard tables of critical values at some predetermined level of significance (in this case 0.2). If D exceeds the critical value, it can be concluded that the observations do not fit the theoretical distribution.

Otherwise, it can be assumed that the observed distribution is not significantly different from the exponential model. None of the data sets was significantly different from the exponential model at 20% significance. This implies that the available data does not indicate deficiencies with the exponential assumption. The results of the Kolmogorov-Smirnov test (KS) are presented in Table 28.

Table 28: D Statistics Test Results

# of Failures	Maximum Deviation	D Statistic (0.2 Significance Level)	Conclusion
4	0.22	.494	Fits $\beta = 1.0$
5	.078	.446	Fits $\beta = 1.0$
5	.054	.446	Fits $\beta = 1.0$
6	.200	.410	Fits $\beta = 1.0$
7	.083	.381	Fits $\beta = 1.0$
4	.116	.494	Fits $\beta = 1.0$
9	.090	.339	Fits $\beta = 1.0$
7	.227	.381	Fits $\beta = 1.0$
11	.055	.323	Fits $\beta = 1.0$
15	.231	.276	Fits $\beta = 1.0$
74	.118	.124	Fits $\beta = 1.0$
7	.140	.381	Fits $\beta = 1.0$
13	.025	.297	Fits $\beta = 1.0$
4	.080	.494	Fits $\beta = 1.0$
11	.250	.323	Fits $\beta = 1.0$
13	.040	.297	Fits $\beta = 1.0$
15	.090	.276	Fits $\beta = 1.0$
14	.060	.274	Fits $\beta = 1.0$
11	.090	.323	Fits $\beta = 1.0$
16	.190	.258	Fits $\beta = 1.0$
10	.250	.322	Fits $\beta = 1.0$

Based on the results of the K-S test, it was assumed that the failure distributions of the semiconductor devices analyzed could be described by a Weibull distribution with a slope of 1.0. Assuming anything other than a constant failure rate would introduce unnecessary complexity into the prediction models. The observed time-to-failure distributions were accurately represented by an exponential distribution over the range of variables in the data. Additionally, as many different time-dependent failure mechanisms distributions are summed (since a device can be susceptible to several failure mechanisms at one time) an exponential distribution often results.

7.5 Proposed GaAs Model Form

All models summarized thus far have been MIL-HDBK-217 type models that, as discussed earlier, are used primarily by systems engineers and thus need to be based on readily accessible data. The intent of this section is to structure a model form for a model that can be used by device manufacturers or by those having access to detailed device fabrication data. The basis for this model form is a recent study performed for Rome Laboratory (formerly Rome Air Development Center) which developed a model for VHSIC/VHSIC-Like CMOS devices (Ref. 13). That effort was an attempt to develop a model consistent with the objectives of the QML program. The foundation for that model, and the model being proposed herein, is the relationship reliability has to device area, defect density, and yield. Due to the importance of these relationships, they will be discussed further later in this section.

The model to be presented, in its present form, cannot be used to predict a failure rate. It is presented to allow those with access to detailed fabrication and reliability data for a specific process line to structure a customized reliability model. Time to failure data for specific failure mechanisms is required along with process specific information such as yield and defect density. As more reliability data becomes available from a wider variety of device types and manufacturers, RAC will collect and analyze this combined dataset to quantify factors in this model so that the model can be used to predict failure rates by those who do not have access to detailed fabrication data. Such a model will be generic and will yield predicted failure rates that are industry averages.

The model form being proposed is based on three separate classes of failure mechanisms, each of which can have contributing failure rates from any number of specific failure mechanisms. Each failure mechanism is modeled with an exponentially decreasing early life failure rate term (for early/mid life), a wearout failure rate based on the lognormal (wearout), a constant failure rate term (for event related mechanism) or a combination thereof. In the context of this model, event related mechanisms are those occurring as the result of externally applied overstress conditions, such as electrostatic discharge. The occurrence of such events are typically random and not related to the inherent reliability of the device. Figure 25 illustrates these three terms.

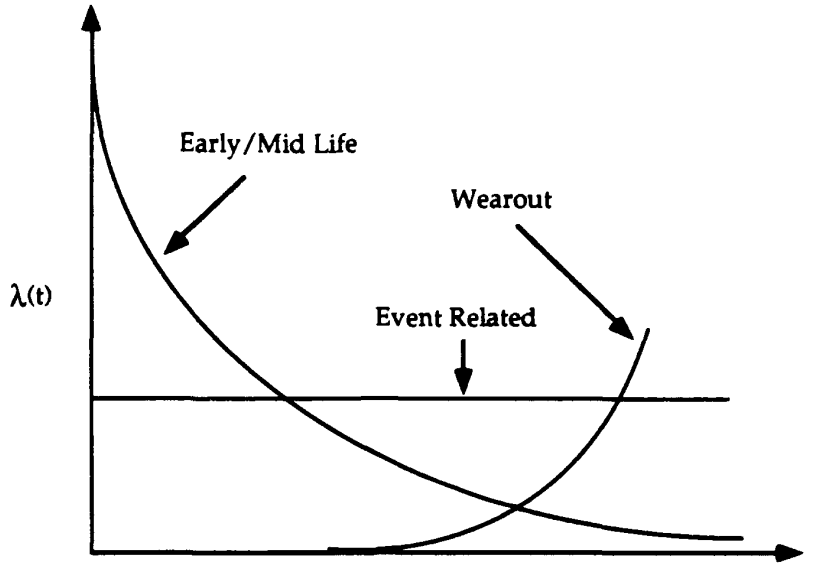


Figure 25: Illustration of Three Types of Model Terms

Each potential failure mechanism must be analyzed to determine which failure rate term or combination of terms adequately model the particular failure mechanism. In an analog of the Si VHSIC/VHSIC-Like CMOS model of Ref. 13, oxide and metallization both can exhibit early life and wearout failures. Hot Carrier effects however, are only wearout related.

7.5.1 Early Life Failures

Most of the failure mechanisms discussed previously in this report are common cause, wearout type mechanisms. Modeling these alone with statistical wearout models such as the lognormal or Weibull distributions (with $\beta > 1$) would result in very low early life failure rates. This clearly is inadequate since empirical evidence has shown that there are early life special cause type failure that occur. It may be possible that wearout mechanisms can also manifest themselves as early life failures as a result of defects. Therefore, the best manner to model early life failure mechanisms is from empirical life data. The following exponentially decreasing failure rate model was chosen to empirically model each failure mechanism;

$$\lambda(t) = \lambda_b e^{-\tau t}$$

where:

λ_b is the failure rate (constant), τ is the time constant of the exponential and t is time.

Time to failure data can then be used and a regression performed to derive λ_b and τ for each mechanism. All data should be normalized to a 25°C temperature by multiplying the actual time by the acceleration (based on the Arrhenius model) due to temperature (between the actual temperature and 25°C). The activation energies for these acceleration factors can be those summarized in Appendix A.

The above relationship can be expanded to include the effects of temperature, duty cycle, and screening (or burn-in). This expanded relationship is as follows:

$$\lambda(t) = \lambda_b e^{\tau t_0} A_T (DC) e^{-\tau(DC) A_T t}$$

where:

t_0 = equivalent screening time (actual time x A_T)
A_T = temperature acceleration based on the Arrhenius relationship
DC = duty cycle (percent operating time)

It should be noted that the Arrhenius model, although originally intended to model chemical reaction rates, is the most widely accepted empirical model for estimating temperature acceleration rates for most die related failure mechanisms.

7.5.2 Wearout Failure Mechanisms

Most wearout failure mechanisms follow the lognormal time to failure distribution. To model the wearout mechanisms of interest, the t_{50} (50% cumulative failure time) and sigma can be derived as a function of the applicable stress and fabrication variables, and can be based on life data or test structure data.

Since the prediction model is in the form of a hazard (h(t)) or failure rate, the hazard rate of the lognormal must be used. This is given by:

$$\lambda(t) = h(t) = \frac{f(t)}{R(t)}$$

Since R(t), the reliability function, involves an integral and becomes complex for the lognormal distribution, the hazard rate cannot be obtained in closed form over all times. If however, the reliability is relatively high the probability density function itself represents a good approximation to the hazard rate. For example, if the reliability is greater than .8, there is no more than 20% error in approximating the hazard rate h(t) with the probability density function f(t) although this value of .8 was chosen somewhat arbitrarily, it represents a reasonable time before which this approximation is valid and after which it is not. Therefore, the point at which the reliability is .8 for any given mechanism signals that the device population is reaching end of life, and the hazard rate will be dramatically increasing. By defining

the model to be valid only for those times in which the reliability is greater than .8, the closed form probability density function can be used to approximate the hazard rate. Beyond this time, the model is not valid. Since there are several variables affecting the failure rate of the wearout mechanisms, the end of life time can be defined to be that in which the time is equal to half of the t_{50} time (.5 t_{50}) or when the failure rate for a single mechanism has reached .1 failures per million hours ($F/10^6$), whichever time is less. Although these values of .5 t_{50} and .1 $F/10^6$ were also chosen somewhat arbitarily, they also typically represent a time beyond which the failure rate will dramatically increase, signalling the end of life is immenant. The failure rate predictions are therefore invalid beyond these times.

One area of concern in the use of the lognormal distribution is its high sensitivity to variations in sigma. In all distributions defined thus far, a sigma of 1.0 is typical. Although it is evident that this value is fairly well accepted, slight deviations from it can significantly affect the model, especially in the tail of the distribution. While a sigma in the range of 1.0 is reasonable and consistent with theory, the range of sigma reported in published data vary widely. An ideal model would derive the t_{50} and sigma for a specific process by measuring how aggressive a manufacturer's design rules and process controls were. For example, if every metal strip carried the maximum current density and the process was marginal or had wide variations (i.e., step coverage varied from 10% to 60% with design rules specifying 30%), then there would be a considerable electromigration risk. Another design may have just a few stripes where the current density is maximum and never experience electromigration.

Since derivation of the t_{50} expressions required the use of extremely large acceleration factors (due to test data being taken at highly accelerated conditions), there is some concern over the accuracy of the derived value. However, this is not a significant effect in this model since the failure rate contribution of the lognormal distribution only becomes significant when the device is approaching its wearout period, and thus the wearout terms do not significantly contribute to the failure rate prior to its wearout period. Therefore, the wearout relationship will only provide an estimate for the end of life and very little information about the failure rate during the useful life of the device. The wearout relationship should however provide an estimate, under a specific set of stresses, of the time at which wearout occurs.

7.5.3 Event Related Mechanism

The two failure mechanisms that are considered event related are package related and electrical overstress. The assumption is that the stress causing failure is an event, such as an electrostatic discharge. Since they are not inherent reliability failure mechanisms, they are modeled with a constant failure rate. This failure rate

is dependent on the probability of an event, the stress magnitude, and the susceptibility of the device to damage from that event.

Derivation of failure rates for event related mechanisms require a knowledge of event statistics (i.e., failure analysis of field failures). These are generally not available, but the models could be improved in this area if large amounts of event data become available.

7.5.4 Area/Defect Density

A key feature of the Ref. 13 model is the use of area and defect density as measures of complexity. Die area, feature size, defect density and yield are all interrelated and heavily influence reliability. Although yield is highly correlated to reliability, many yield inhibitors do not influence reliability.

In silicon CMOS technologies, defect density is undoubtedly a prime indicator of reliability and its value typically available from text structures. Defect densities of GaAs devices however may be more difficult to obtain due to the fact that their is not large oxide areas available for analysis. An alternative to defect density in the proposed model is therefore some function of yield. Although not as intimately related to reliability as defect density, it is usually much more readily accessible data.

Reference 13 has derived a linear relationship between failure rate and the area-defect density product. This can be used as a baseline for this factor to be used in this model. This methodology is consistent with Reference 91 which concludes that reliability is not necessarily correlated to complexity as measured by the number of elements. That study had demonstrated that a large digital ASIC with over 1000 MESFETs had a median life nearly equal to a microwave amplifier containing only four MESFETs. This conclusion is consistent with recent trends in the silicion semiconductor industry. Remaining to be accomplished however is the relationship between area-defect density and yield. Unfortunately, there is no concensus among industry experts regarding this relationship. The relationships in Reference 13 were based on a model developed by Price (Ref. 85) using Bose-Einstein statistics. A more general defect model was derived by Stapper (Ref. 108). In this model the probability defect density function is related to the gamma distribution. For this model the yield is given by:

$$Y = 1/(1 + AD_0/S)^S$$

where Y is the yield percentage, A is the chip area, D_0 the average defect density, and S a shape parameter. This model assumes that the defects have a given distribution pattern across the wafer. In the limiting case where S approaches 0, the distribution is a delta function, meaning the defect density is constant and all defects are randomly distributed and independent. This condition leads to the Poisson yield estimate

$$Y = e^{-D_0A}$$

Also it can be seen that when the S of the Stapper model is 1, the yield model reduces to

$$Y = 1/(1 + AD_0)$$

which was described previously as the Price model, but actually used earlier by Seeds (Ref. 99). In this case the defect density distribution is exponential. A comparison of these and two other yield models is shown in Figure 26. The Poisson model is the most pessimistic and the Seeds model is the most optimistic. The Stapper model can be adjusted by the shape parameter to cover the area in between.

Due to its simplicity and the fact that it is between the most pessimistic and optimistic relationships, the Stapper model with S = 1 is proposed for use in the model.

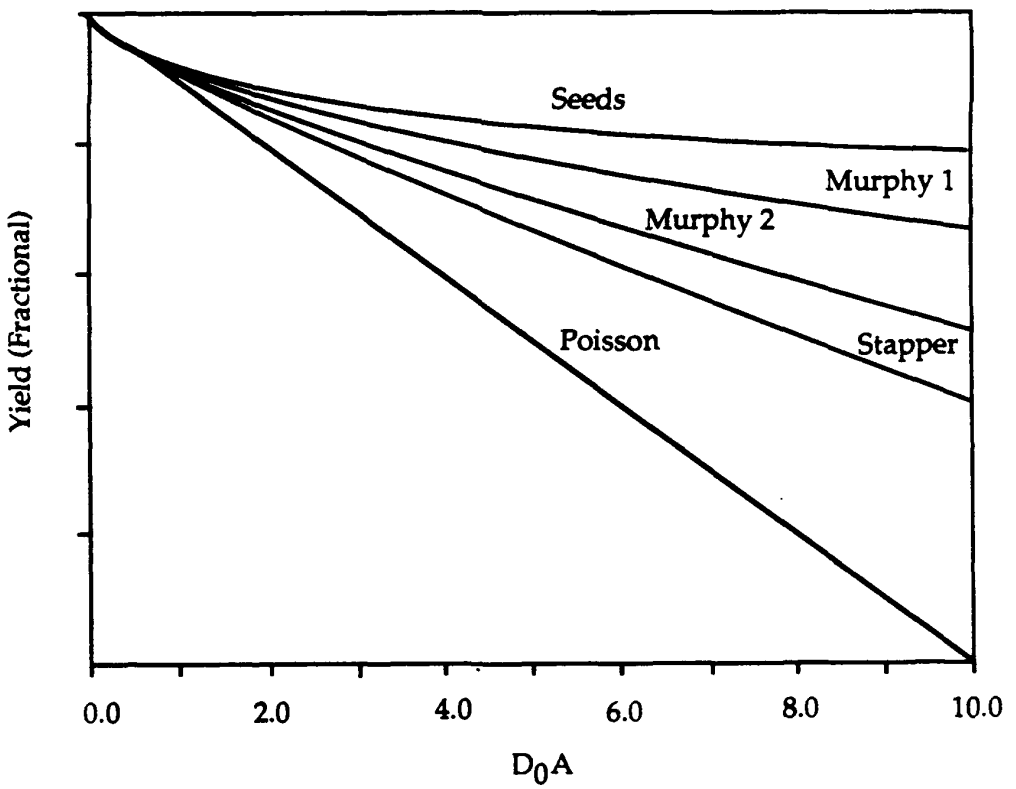


Figure 26: Yield as a Function of Defects and Area for Different Models

This relationship is;

$$Y = \frac{1}{1 + AD_0} \qquad \text{or} \qquad AD = \frac{1}{Y} - 1$$

To compensate for the percentage of yield inhibitors which affect reliability, constants B and C are added to the relationship. B is the percentage of total failure rate which is due to failure mechanisms that are also yield inhibitors. To derive this factor, life data from a production run of known yield is needed. Therefore, using this relationship in conjunction with the fact that failure rate is directly proportional to AD_0 yields;

$$\lambda_p \ \alpha \ B\left(\frac{1}{Y} - 1\right) + C$$

One possible model form for GaAs MMICs is therefore;

$$\lambda_p = \left(B\left(\frac{1}{Y} - 1\right) + C\right)\left(\sum_{i=1}^{n} \lambda_{iE}\right) + \sum_{i=1}^{m} \lambda_{iW} + \sum_{i=1}^{l} \lambda_{ER}$$

where:

C,B = constants to compensate for the percentage of yield inhibitors which affect reliability. B is the percentage of total failure rate which is due to failure mechanisms that are also yield inhibitors.

Y = Fabrication Yield, % of total die that are acceptable.

$\sum_{i=1}^{n} \lambda_{iE}$ = The sum of early life failure rates for the n most predominant failure mechanisms. Each a function of their individual A_T, λ_b and τ. Also a function of screen time, duty cycle.

$\sum_{i=1}^{m} \lambda_{iW}$ = Sum of the wearout failure rates for the m most predominant wearout mechanisms. Each is a function of its appropriate design and application variables. These are all based on the lognormal distribution for which a t_{50} and α must be derived.

$\sum_{i=1}^{l} \lambda_{ER}$ = Sum of the event related failure rates for the l most predominant failure mechanisms.

If more detailed information is available so that yield can be determined for specific failure mechanisms, a more accurate model can be derived by adding a yield factor for each failure mechanism term. The form for this model would be:

$$\lambda_p = \sum_{i=1}^{n} \lambda_{iE} \left(\frac{1}{Y_i} - 1 \right) + \sum_{i=1}^{m} \lambda_{iw} + \sum_{i=1}^{l} \lambda_{ER}$$

where:

Y_i = yield for a specific failure mechanism or structure

All other terms are as defined above.

In either of these two model forms presented, the base failure rates will need to be adjusted to insure that the predicted failure rate for each failure mechanism correlates to observed values after accounting for yield.

8.0 SUMMARY

The Department of Defense through programs such as MIMIC has sparked increased interest in the field of GaAs technology. The resources and structure needed to transition the results of years of research in gallium arsenide technology into a developed production process is being provided. The current reliability of GaAs components is considered by many to lag that of silicon. However, the influx of research being spawned by the MIMIC program and other large DoD funded programs is changing this.

Until recently GaAs IC manufacturers have mainly limited their production to DoD funded development efforts while others performed research and evaluated developments in the technology and in the market. Projections of the markets growth and the need for faster GaAs analog microwave and digital circuits in computer, communications and consumer applications have begun to expand the GaAs commercial market. Alliances have been formed between several GaAs manufacturers. Vitesse Semiconductor has teamed with Fujitsu Ltd. and Thomson-CSF S.A. Additionally, Anadigics is teaming with Thomson and TriQuint Semiconductor has recently teamed with Rockwell International Corp. There is also a strong commitment to GaAs IC development by almost all Japanese Semiconductor manufacturers. A current listing of manufacturers of GaAs MMIC and digital integrated circuits comprising both the military and industrial markets are found in Table 29 and 30.

Table 29: Builds MMIC GaAs

Harris Microwave Semiconductor	G.E.
TriQuint Semiconductor	Avantek
Watkins Johnson Co.	Sanders Microelectronic Center
Anadigics	NEC Corp.
M/A-COM AAD	Raytheon Special Microwave Devices Operation
Alpha	Eaton-AIL-Division
Texas Instruments	

Table 30: Builds Digital GaAs

Harris Microwave Semiconductor	Anadigics
TriQuint Semiconductor	Alpha
Vitesse Semiconductor	NEC Corp.
M/A-COM AAD	

Data published to date, concerning GaAs device reliability indicates that devices with respectable failure rates can be produced. Data concerning activation energy values for known failure mechanisms do not all agree, however most agree that the activation energies associated with these known mechanisms are high. A high activation energy, which is easily accelerated by temperature, may mask other currently unknown failure mechanisms. In addition, RF induced failure modes may not be receiving proper attention. The evaluation of GaAs device failure mechanisms needs to continue to verify that other failure mechanisms due not exist.

Military standards are currently being updated and written to incorporate GaAs devices. Test methods within MIL-STD-883 are being modified to incorporate GaAs devices while MIL-I-38535 and MIL-H-38534 are being written to define a QML program for GaAs technology that will provide required procedures that assure high quality and reliable microcircuits. Prediction methods currently exist in MIL-HDBK-217 that address millimeter wave diodes and photonic devices. Models which address GaAs MMIC and digital integrated circuits, described by this text, have been written and will be incorporated into the next update of this document.

Packaging is a major influence in device reliability. The package must be able to provide support to the die while offering protection from environmental stresses such as vibration, acceleration, thermal shock, and temperature. When using GaAs, for MMICs and digital ICs, the package design is crucial to the devices performance. Noise and cross-talk caused by very fast rise and fall times must be minimized. The loading of transmission lines must be kept to a minimum to reduce ringing and voltage standing wave ratio.

Gallium arsenide has long been known to offer performance advantages over silicon based technologies. These performance advantages have led to the development of devices, such as MMICs, which can operate at frequencies up to 100 GHz. Silicon parts begin to approach speed limitations in the 1 to 5 GHz range. These speed advantages combined with the inherent radiation hardness of GaAs will provide and increasing need for GaAs devices within military and commercial markets.

APPENDIX A:

TRANSISTOR RELIABILITY STUDIES

Table A-1: GaAs Transistor Reliability Studies

Device	Temperature	Failure Mechanisms	E_a	Ref.
Digital IC FET (Ti/Pd/Au gate)	T_j = 245, 260, 275, 290 310°C	sinking gate	1.6 eV	78
FET (Al Gate)	----	Au-Al phase formation. Al electromigration	0.8 eV	52
HEMT (0.3 μm gate)	T_c = 220, 225, 250°C	stress induced traps or sinking gate	1.0 eV	42
HEMT (0.3 μm gate)	T_c = 150, 175, 200°C	stress induced traps or sinking gate	1.1 eV	42
HEMT (0.3 μm gate)	T_c = 175, 200, 255°C	stress induced traps or sinking gate	1.0 eV	42
HEMT (0.7 μm gate)	T_c = 200, 225°C	stress induced traps or sinking gate	1.5 eV	42
low-noise	100-275°C		no-bias/bias	10
		Au-Cr interdiffusion	0.64 eV 0.10 eV	
		Ga and As outdiffusion	0.92 eV 0.32 eV	
		Ni diffusion	0.76 eV 0.60 eV	
		Ge diffusion	0.50 eV 1.96 eV	
low-noise	230-270°C	increase of ohmic contact resistance	1.5 eV	64
low-noise	88-275°C	RF parameter degradation	0.8 eV	52
		Au-Al	0.5 eV	
low-noise	175-275°C	interdiffusion at ohmic contacts	1.0 eV	74
low-noise	230-300°C	contact stability	1.05 eV	79
low-noise	200-260°C	Au-Al	1.5 1.9 eV	9
low-noise	170-220°C	electromigration	0.8 eV	14
low-noise	225-275°C	electromigration	1.3 eV	118
low-noise	100-200°C	ohmic contact degradation	0.7 eV	72
low-noise and power	170-250°C	Schottky-metal	Al: 0.93 eV	8
		interaction with substrate	Au: 1.53 eV 1.74 eV	
low-noise and power	180-337°C	Au-Al	1.1 eV	73
		ohmic contact degradation	1.5 eV	
low-noise and power	200-300°C	ohmic contact degradation	1.8 eV	28
		Au-Al with barrier	1.2 eV	
		surface oxidation	0.7 eV	

Table A-1: GaAs Transistor Reliability Studies (cont'd)

Device	Temperature	Failure Mechanisms	E_a	Ref.
power (Ti/Al/Ti gate)	T_j = 240, 270, 300°C	30% degradation in BV_{op} and Burnout Ti, AlGaAs interaction	1.0 eV	57
power (Al gate)	T_j = 240, 270, 300°C	Al gate open and burnout	1.0 eV	57
power	T_j - 210, 250°C	mobility and saturated velocity decrease	1.2 eV	32
power	T_j = 150, 190, 225°C	Die attach, gate voiding, burnout	1.5 eV	95
power	T_j = 210, 230, 250°C	Al gate diffusion into GaAs leading to burnout	1.2 eV	54
power	T_j = 210, 230, 250°C	Al gate diffusion into GaAs leading to burnout	1.2 eV	54
power	120-220°C	Au-Al	2.0 eV	116
power	140-200°C	gate pad interdiffusion drain electromigration	1.0 eV 1.85 eV	26
power	175-250°C	gradual degradation channel compensation	1.2-1.8 eV 1.5 eV	31
power	180-200°C	ohmic contacts electromigration Ti oxidation and As outdiffusion	1.1 eV 1.8 eV	18
power	137-197°C	high gate resistance surface contamination	0.9 eV 2.3 eV	22
power	190-215°C	Al electromigration	0.61 eV	105
power	240-337°C	Al voids ohmic contact degradation	1.0 eV 1.8 eV	55
power	150-225°C	gate voids	1.5 eV	95
power	210-250°C	Al-GaAs interdiffusion	1.15 eV	54
power (Ti/Al)	T_j = 240, 270, 300°C	burnout	1.0 eV	57
small signal	200°C	metal migration at ohmic contacts	1.0 eV	2
small signal	150 - 295°C	increase of ohmic contact resistance	1.8 eV	50

APPENDIX B:

ACRONYMS

Acronym	Description
2-DEG	Two-Dimensional Electron Gas
ALS	Advanced Low Power Schottky
APD	Avalanche Photo Diode
ASIC	Application Specific Integrated Circuit
ATE	Automated Test Equipment
BFL	Buffered Field Effect Transistor Logic
CAD	Computer Aided Design
CBE	Chemical Beam Epitaxy
CDFL	Capacitor-Diode Field Effect Transistor Logic
CML	Current Mode Logic
CMOS	Complimentary Metal Oxide Semiconductor
CRTA	Critical Review and Technology Assessment
D-FET	Depletion Mode Field Effect Transistor
D-HFET	Depletion Mode Heterostrucure Field Effect Transistor
D-MESFET	Depletion Mode Metal Semiconductor Field Effect Transistor
DARPA	Defense Advanced Research Project Agencfy
DBQW	Double-Barrier Quantum Well
DC	Direct Current
DCFL	Direct-Coupled Field Effect Transistor Logic
DH-FET	Double Heterostructure Field Effect Transistor
DLD	Dark Line Defect
DLTS	Deep Level Transient Spectroscopy
DMT	Doped-channel, Metal Insulated Semiconductor-like Field Effect Transistor
DSD	Dark Spot Defect
E-FET	Enhancement-Mode Field Effect Transistor
E-HFET	Enhancement Mode Heterostrucure Field Effect Transistor
E-JFET	Enhancement-Mode Junction Field Effect Transistor
E-MESFET	Enhancement-Mode Metal Semiconductor Field Effect Transistor
E/D	Enhancement/Depletion Mode
EBIC	Electron Beam Induced Current
ECL	Emitter Coupled Logic
ESD	Electrostatic Discharge
FET	Field Effect Transistor
GHz	Gigahertz
HBT	Heterojunction Bipolar Transistor
HC	Hot Carrier
HEMT	High Electron Mobility Transistor
HFET	Heterostructure Field Effect Transistor
HIFET	Hetero-interface FET
HIGFET	Heterostructure Insulated Gate Field Effect Transistor
HMESFET	Heterostructure Metal Semiconductor Field Effect Transistor
I^2L	Integrated Injection Logic
IC	Integrated Circuit

IGFET	Insulated Gate Field Effect Transistor
IHEMT	Inverted Structure High Electron Mobility Transistor
IITRI	Illinois Institute of Technology Research Institute
IMPATT	Impact Ionization Avalanche Transit Time
JFET	Junction Field Effect Transistor
LEC	Liquid Encapsulated Czochralsky
LED	Light Emitting Diode
LPE	Liquid Phase Epitaxy
LSI	Large Scale Integration
MAD	Multi-acronym device
MANTECH	Manufacturing Technology
MBE	Molecular Beam Epitaxy
MESFET	Metal Semiconductor Field Effect Transistor
MHz	Megahertz
MIM	Metal Insulator Metal
MIMIC	Microwave and Millimeter Wave Integrated Circuit
MISFET	Metal Insulated Semiconductor Field Effect Transistor
MMIC	Monolithic Microwave Integrated Circuit
MOCVD	Metal Organic Chemical Vapor Deposition
MODFET	Modulation Doped Field Effect Transistor
MOMBE	Metal Organic Molecular Beam Epitaxy
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MQW	Multiple Quantum Well
MSI	Medium Scale Integration
NMOS	N-Channel Metal Oxide Semiconductor
NRL	Naval Research Laboratory
OEIC	Optic-Electronic Integrated Circuits
OEM	Original Equipmetn Manufacturer
OMVPE	Organo-Metallic Vapor Phase Epitaxy
OPFET	Optical Field Effect Transistor
PBT	Permeable Base Transistor
PCM	Process Control Monitor
PECVD	Plasma Enhanced Chemical Vapor Deposited
PIN	P-I-N Structure
PM	Process Monitor
QML	Qualified Manufacturers List
QPL	Qualified Products List
QW	Quantum Well
RAC	Reliability Analysis Center
RADC	Rome Air Development Center
RAM	Random Access Memory
RF	Radio Frequency
RHET	Resonant Tunneling Hot Electron Transistor
RL	Rome Laboratory
RT-FET	Resonant Tunneling Field Effect Transistor

RTBT	Resonant Tunneling Bipolar Transistor
SAGFET	Self Aligned Gate Field Effect Transistor
SDFL	Schottky Diode Field Effect Transistor Logic
SDHT	Selectively Doped Heterojunction Transistor
SE-LED	Surface Emitting Light Emitting Diode
SEC	Standard Evaluation Circuit
SEED	Self-Electro-Optic-Effect Device
SEU	Single Event Upset
SISFET	Semiconductor-Insulator-Semiconductor Field Effect Transistor
SPC	Statistical Process Control
SQW	Single Quantum Well
SRAM	Static Random Access Memory
SSI	Small Scale Integration
SSO	Self-sustained oscillation
SWAT	Sidewall Assisted Transistor
TCV	Technology Characterization Vehicle
TED	Transferred Electron Device
TEGFET	Two-Dimensional Electron Gas Field Effect Transistor
TM	Test Method
TQM	Total Quality Management
TRB	Technology Review Board
TTL	Transistor Transistor Logic
VLSI	Very Large Scale Integration
VPE	Vapor Phase Epitaxy
VSWR	Voltage Square Wave Ratio

APPENDIX C:

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APPENDIX D:

RAC PRODUCTS

RAC Product Order Form

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MFAT-2	GaAs Characterization and Failure Analysis Techniques - A Procedural Guide	100.00	130.00		
*MFAT 1&2	Combined set of MFAT-1 and MFAT-2	200.00	300.00		
FTA	Fault Tree Analysis Application Guide	80.00	90.00		
NPS-1	Analysis Techniques for Mechanical Reliability	60.00	70.00		
PRIM-91	A Primer for DoD Reliability, Maintainability and Safety Standards	120.00	140.00		
RELIABILITY DATA					
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NPRD-91P	Nonelectronic Parts Reliability Data - 1991 (IBM PC database)	400.00	440.00		
DSR-4	Discrete Semiconductor Device Reliability - 1988	100.00	120.00		
FMD-91	Failure Mode Distribution Critical Technology Review Assessment	100.00	120.00		
NONOP-1	Nonoperating Reliability Data - 1987	150.00	160.00		
MDR-22	Microcircuit Screening Analysis - 1987	125.00	135.00		
VZAP-90	Electrostatic Discharge Susceptibility Data	150.00	160.00		
VZAP-90P	VZAP-90 Data on diskette (IBM PC database)	350.00	380.00		
VZAP-90C	Complete VZAP package including VZAP-90 publication and VZAP-90P	450.00	480.00		
MDR-21	Trend Analysis Databook - 1985	100.00	110.00		
STATE-OF-THE-ART REPORTS AND SOFTWARE					
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SOAR-3	IC Quality Grades: Impact on System Reliability and Life Cycle Cost	50.00	60.00		
SOAR-4	Confidence Bounds for System Reliability	50.00	60.00		
SOAR-5	Surface Mount Technology: A Reliability Review	60.00	70.00		
SOAR-6	ESD Control in the Manufacturing Environment	60.00	70.00		
SOAR-7	A Guide for Implementing Total Quality Management	75.00	85.00		
CRTA-PEM	Plastic Microcircuit Packages: A Technology Review	50.00	60.00		
CRTA-QML	Qualified Manufacturer's List: New Device Mfg. and Procurement Technique	50.00	60.00		
CRTA-GaAs	Assessment of GaAs Device Quality and Reliability	50.00	60.00		
VPRED	VHSIC Reliability Prediction Software	150.00	160.00		
RAC-NRPS	Nonoperating Reliability Prediction Software (Includes NONOP-1)	1400.00	1450.00		
RELIABILITY INDICES AND PROCEEDINGSs					
TRS-2	Search and Retrieval Index to IRPS Proceedings - 1968 to 1978	24.00	34.00		
TRS-2A	Search and Retrieval Index to IRPS Proceedings - 1979 to 1984	24.00	34.00		
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TRS-4	Search and Retrieval Index to EOS/ESD Proceedings - 1979 to 1984	36.00	46.00		
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MIL-HDBK-338	MIL-HDBK-338: Subject Index	25.00	35.00		
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QUALIFIED MANUFACTURER'S LIST: NEW DEVICE MANUFACTURING AND PROCUREMENT TECHNIQUE

1991

Prepared by:

Reliability Analysis Center
201 Mill St.
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Under contract to:

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13. ABSTRACT (Maximum 200 words)

The DoD has recently implemented a Qualified Manufacturers List (QML) system for the procurement of microcircuits to complement the existing Qualified Products List (QPL) system. Specifications used are -- MIL-H-38534, "General Specifications for Hybrid Microcircuits," and MIL-I-38535, "General Specification for Integrated Circuit Manufacturing," which utilizes "generic qualification." Ongoing and future changes to these documents, appropriate modifications to MIL-STD-883, "Test Methods and Procedures for Microelectronics, and responsible organizations are provided. This document will concentrate on MIL-I-38535 which incorporates the final QML procedure to describe the process. Details on certification and qualification of a technology flow including device design, fabrication, packaging and assembly and the use of surrogate devices, wafer process monitors and a technology control vehicle (TCV) to baseline and control a process and provide ongoing reliability testing will be discussed. This document provides a past, present and future perspective of efforts to develop the new QML concept which is in place today. A companion document to the QML, the "Microcircuit Application Guidebook" will be introduced. Appropriate comments on the qualification procedure for both QML's is included.

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PREFACE

On February 22, 1989 the following news release No. 80-89 from the Office of Assistant Secretary of Defense (Public Affairs) announced a new microcircuit manufacturing and procurement technique.

The Department of Defense (DoD) and the Semiconductor Industry Association (SIA) have announced a new strategy for military microcircuit manufacturing and procurement that is expected to save DoD more than $800 million annually while accelerating introduction of new technology into defense systems.

The strategy, the result of more than two years of industry and government negotiations, encourages manufacturers to become globally competitive by increasing efficiency at onshore facilities. Under the program, called Generic Qualification for Microcircuits, as the manufacturers' production processes are certified and qualified, they will be listed on the Qualified Manufacturers List (QML). All products of those technology methods will be generically qualified products.

By streamlining the certification and qualification process at the manufacturer level, industry will be able to bring new technologies to market faster, improve quality and reliability, reduce costs, and extend U.S. leadership in application of state-of-the-art microelectronics in defense systems.

The key features of the QML program includes the following:

- Manufacturing decisions, such as major and minor process changes, rest solely with the Technology Review Board (TRB), which resides within the manufacturer.
- Government determines by a management audit whether the company has a stable controlled process including integration of design, fabrication, and assembly of microcircuits.
- A certified line may produce a variety of qualified integrated circuits with only one audit. Systems manufacturers will not be required to re-audit a QML facility as long as the method remains under control.
- The manufacturer will have flexibility to become more globally competitive through a program of continuing improvement in his own process.
- The market will be concentrated among the high quality manufacturers thereby increasing their loading of qualified lines and further improving quality and reliability while lowering cost.

- The program is being institutionalized in the semiconductor industry. First sites nearing completion are at General Electric and AT&T. The second part of the program, which now includes Intel, Harris, GE Solid State, Texas Instruments, National, VLSI Technology, and IBM, was started in October 1988 and will be completed by 1990. Several QML lines are expected to be producing QML parts by mid-1989.

- A plan is being developed for manufacturers to transition Qualified Parts List (QPL) products to the QML program.

- The program will serve as a model for non-military customers who want the highest quality at the lowest price. It will facilitate future transition to a national standard for manufacturing of integrated circuits.

Ultimately, the use of generic qualification and QML listings are expected to be employed in other product areas based on the model developed for microcircuits."

This document provides a past, present and future perspective to explain efforts leading up to and after the news release including rationale for the development of the new concept defined by the hybrid and monolithic QML's which are in place today. Current QML listings for both MIL-H-38534, "General Specification for Hybrid Microcircuits" and MIL-I-38535, "General Specification for Integrated Circuits (Microcircuits) Manufacturing," on going and future changes to these documents, appropriate modifications to MIL-STD-883, "Test Methods and Procedures for Microelectronics" and responsible organizations are provided. A companion document to the QML, the "Microcircuit Application Guidebook" will be introduced. Finally, appropriate comments on the qualification procedure for both QML's is included.

The following QML definition is recommended for use:

> QML - The Qualified Manufacturers List approach defines a procedure that certifies and qualifies the manufacturing processes and materials of potential vendors as opposed to the individual qualification of devices. Hence, all devices produced and tested using the QML certified/qualified technology flow are qualified products.

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1.0 BACKGROUND

Establishing certified and qualified vendors to provide Department of Defense (DoD) contractors with quality components is paramount to the manufacture of highly reliable and supportable equipment. However, the existing part-by-part qualification system, documented by a Qualified Product List (QPL) developed to support low cost, high volume devices was not keeping pace with new technology. Before a device is listed on the QPL, it is put through a rigid series of tests designed to assess the reliability and quality of the individual device. The procedure a vendor must follow in order to have a device on the QPL are outlined here:

- Industry Specification DoD Usage Data
  - Characterization
    - Physical
    - Electrical
    - Reliability
  - Detail Specification ("Slash Sheet")
  - Facility Certification (MIL-STD-976)
  - Screening (MIL-STD-883 Test Method 5004)
  - Qualification Conforming Inspection/Qualification (MIL-STD-883 Test Method 5005)
  - General Requirements (MIL-M-38510)
  - Qualification Report
  - QPL

It is important to note that each device listed on the QPL must go through this sequence. Outside of the facility certification step, which needs to be performed only once for a given technology flow, there is limited generic data from a device which can be utilized for other devices of a technology family. Also, requalification of a device is required periodically when a major change to the device is made or a reliability/quality problem occurs. Consequently, the product qualification concept can be time consuming, even when utilizing the technology family qualification option of paragraph 4.4.2.6 in MIL-M-38510, "General Specification for Microcircuits."

Another problem associated with product qualification is the number of actual devices required for qualification testing. Since many of the required tests are destructive, these devices are lost. For the high volume ("jelly bean") devices, the cost for the number of devices used for qualification testing is insignificant. However, for the higher integration, low volume devices produced today, the number of end-of-line actual devices needed for qualification testing takes on a new meaning-much higher cost.

The combination of these product qualification concept problems has resulted in practically no hybrid microcircuit QPL listings and fewer new monolithic microcircuits being submitted for QPL status. This statement is reflected in Figure 1

which was used to illustrate the slow response of the QPL system to include new technology and complex devices. QPL data from the early eighties was used to prepare this graphic showing the Integrated Circuit (IC) product life cycle and military use pattern. It is evident that the QPL system did not adequately address the insertion of new technology and standardization aspects. Additionally, once a product is defined by a source control drawing and approved for use in a particular system, it most likely will never be replaced by a QPL device. What was needed was to create more interest by microcircuit vendors in the qualification of high cost and low volume devices. The DoD solution was to develop and implement a Qualified Manufactuers List (QML) system for the procurement of microcircuits to complement the existing QPL system and include all devices into the standardization program early in their life cycle.

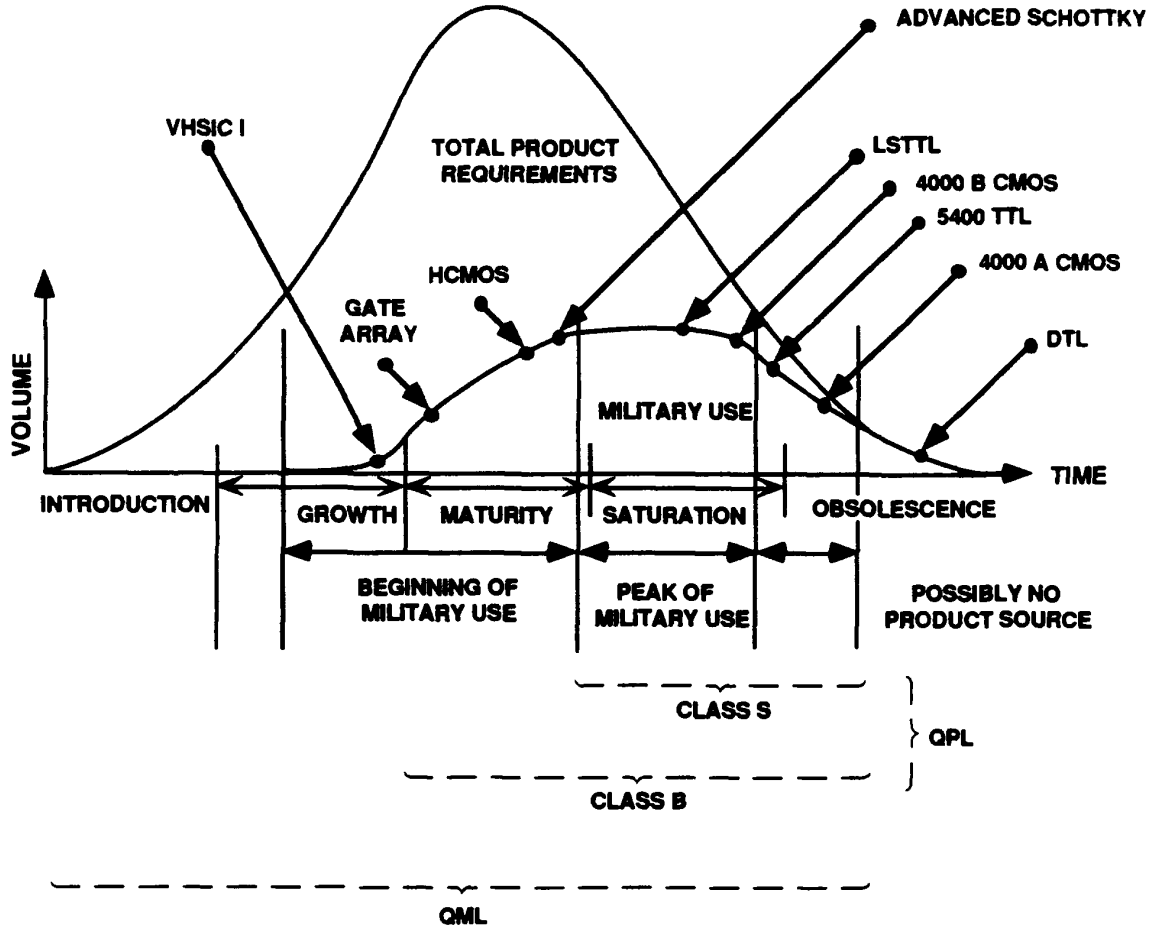


Figure 1: IC Product Life Cycle & Military Use Pattern

The goals of the QML system are presented in Figure 2. The following sections provide a summary of the hybrid QML, which was issued first and the integrated circuit QML which followed. This report will use MIL-I-38535 which incorporates the final QML procedure to describe the enhanced process. However, lessons learned from the hybrid QML program strengthened the monolithic QML in an evolutionary way. Hybrid QML updates are discussed later.

A recent DoD technology assessment report identified six elements as keys to excellence in manufacturing. These elements are also the goals of the QML system. They are:

- Recognition of manufacturing as a strategic factor
- Concurrent design of product and life cycle processes
- Emphasis on quality
- Continuous improvement
- Workforce and its education
- Vendor and user working relationships

Figure 2: Goals of QML System

1.1 Responsible Organizations

Who develops, monitors, maintains the standardization of items, materials and engineering practices within the DoD and what procedure is used to coordinate/issue new/revised documents? The Defense Standardization and Specification Program Policies, Procedures and Instruction Manual, DoD 4120.3-M defines the standardization of products/areas covered by the Federal Stock Code (FSC) system. Each FSC product/area has a military Preparing Activity (PA) responsible for preparation and maintenance of standardization documents and the conduct of study projects. Additionally, each PA can have an agent activity which acts for, and by authority of, the PA in the preparation of standardization documents, performance of study projects and administration of QPL's and QML's. The PA, however, retains responsibility and approval authority for the work accomplished. Figure 3 is an example of the system in place for microcircuits where Rome Laboratory (RL) is the preparing activity and Defense Electronic Supply Center (DESC) is their agent. Figure 4 identifies the various microcircuit vendors and user groups involved in the document coordination process. In addition, these are military review activities that have an essential technical interest in the standardization document, thus requiring a review of all proposed actions affecting it. A custodian is the activity responsible for coordination of standardization projects within its own Department/Agency. Figure 5 lists the military activities that participate in the coordination of microcircuit documentation.

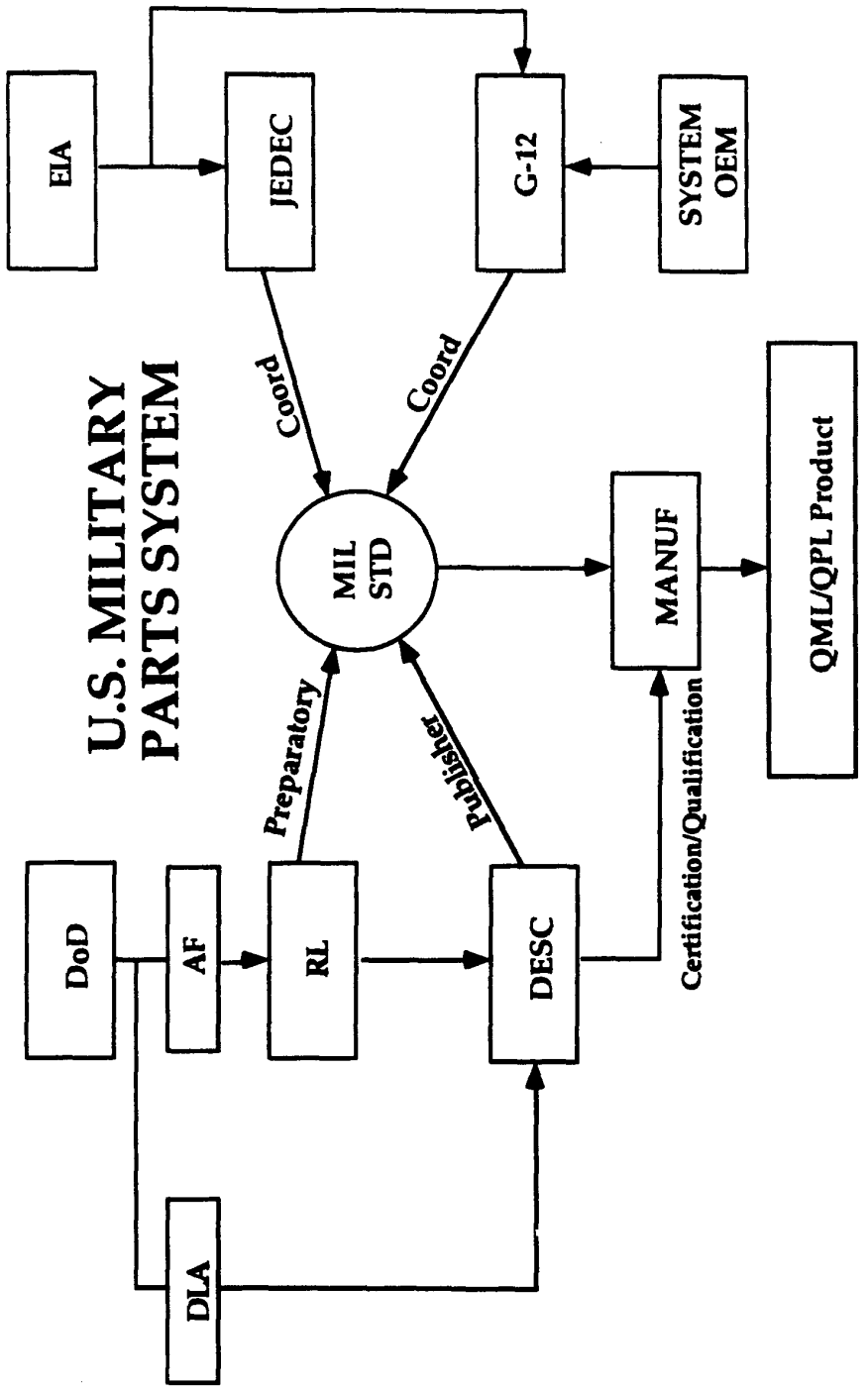


Figure 3: Microcircuit Activity Example

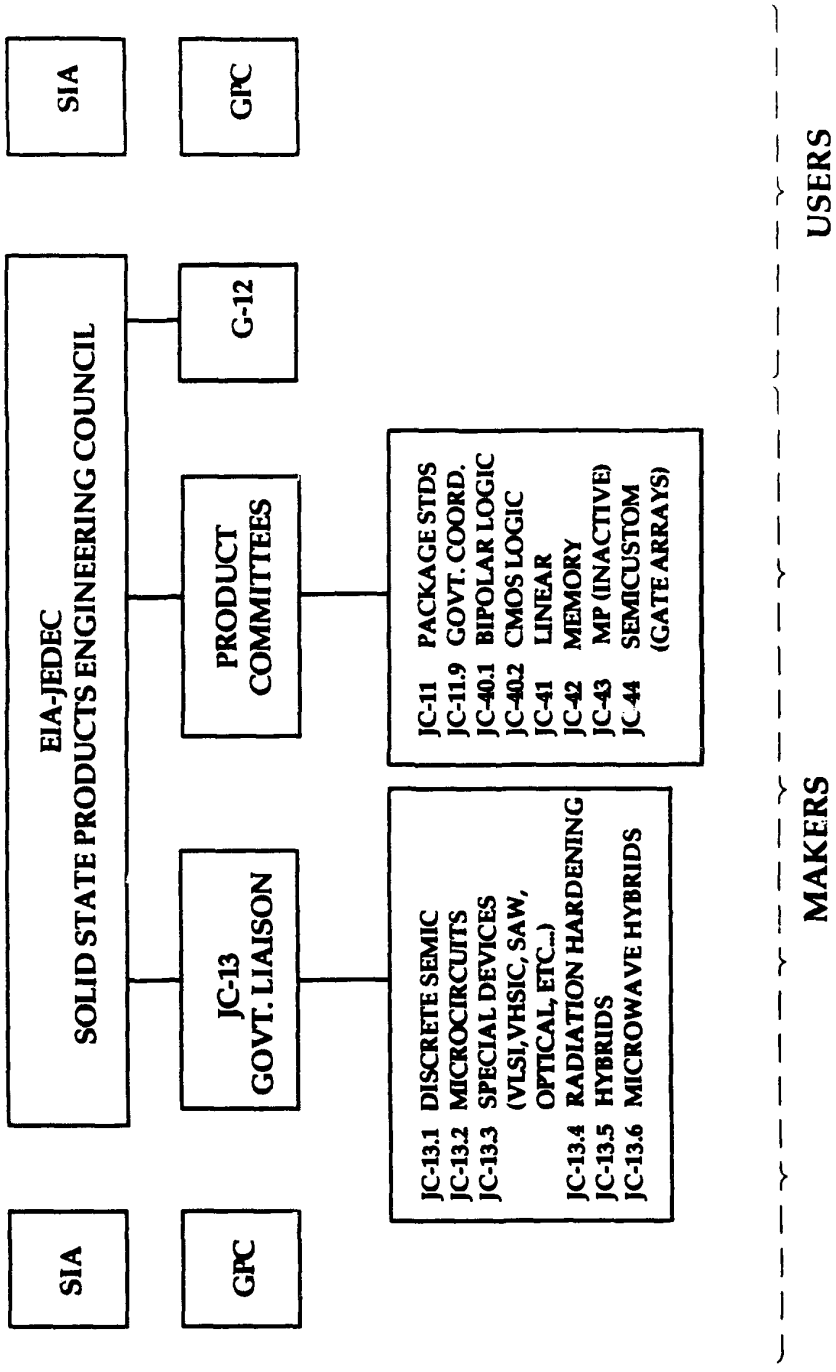


Figure 4: Industry Groups Involved

Preparing Activity	Air Force - 17	Rome Laboratory
Agent	DLA-ES	DESC
Custodians	Air Force - 17	Rome Laboratory
	- 19	Space Division
	Army - ER	Fort Monmouth
	- MI	Redstone Arsenal
	Navy - 003-114	Space & Naval Warefare Systems Command
	DLA - ES	DESC
User Activities	Army - AR	Picatinny Arsenal
	Navy - MC	Marine Corp. Research Development and Acquisition Command

Figure 5: Military Coordination Activities

Each documentation action is defined in an approval standardization project plan on behalf of all users, and coordinated with designated custodian and review activities. Comments are designated as either essential or suggested. An essential comment supported with justification must be resolved. Comments from industry and industry associations are given full consideration and the associations are notified of actions taken and rationale. The documents are then issued as coordinated and are implemented where applicable by DoD activities. Revisions are treated the same as new documents except for determination of review and user activities which may be different.

2.0 HYBRID MICROCIRCUIT QML

A DoD Tri-service/NASA working group was tasked with the responsibility of assuring the quality and availability of hybrid microcircuits for military systems. Initial efforts confirmed that complex devices such as hybrids did not fit the existing part-by-part qualification procedure already in place. Therefore, it was decided to take a building block approach requiring certification and qualification of packages, attached components, materials, and processes. This approach would not only eliminate the costly qualification of each hybrid microcircuit but would enhance device yield and quality, resulting in a more cost effective procedure. In addition, acceptance of this procedure would eliminate the costly and time consuming practice of each original equipment manufacturer (OEM) auditing his hybrid vendors.

The result of a research and development effort by the Rome Air Development Center (RADC)[1], now Rome Laboratory (RL), provided the strawman procedures which led to the QML procedure for hybrid microcircuits. Extensive new developments were proposed for Test Method 5008 of MIL-STD-883, and Appendix G to MIL-M-38510. In addition, MIL-STD-1772 "Certification Requirements for Hybrid Microcircuit Facilities" was prepared, coordinated and issued on May 15, 1984, establishing the minimum requirements governing the approval of fabrication processes and lines for hybrid microcircuits. The criteria specified requires a hybrid manufacturer to demonstrate his capability to continuously produce quality products. This is accomplished by evaluating a manufacturer's capability to control critical processes within established limits at specified points and then continuously maintain this control during subsequent production runs. The original format contained a section for audit and certification and a section for qualification.

2.1 Certification/Qualification Procedure

The QML concept established by MIL-STD-1772 requires the certification of all materials, processes and testing. A representative product is then fabricated, using the certified hybrid baseline capabilities and qualified. Section A of MIL-STD-1772 established the audit plan for facilities and line certification. The audit plan provides a systematic method for determining a manufacturer's conformance to the specified product assurance requirements of MIL-M-38510 and MIL-STD-883.

Compliance to these requirements serve as the basis for initial and continued certification of hybrid microcircuit manufacturers.

Section B of MIL-STD-1772 defines requirements for the qualification of fabrication processes such as thick and thin film substrate manufacture, element and substrate

[1] RADC-TR-83-74 , "Application Guidelines for Quality Assurance Procedures for Hybrid Microcircuits"

ttachment, wire bonding, sealing, delidding, and resealing. In addition, it provides a method to establish a manufacturer's baseline and, subsequently, is used to evaluate proposed changes to any process, material, or design. Limits must be based on process capability rather than field requirements. This assures that accepted changes will maintain or enhance the quality and reliability of the hybrid microcircuit fabricated. The qualification test limits are, in some cases, specified over and above that found in normal screening or quality conformance inspection, to demonstrate a degree of process margin. The manufacturer is required to perform all necessary testing and corrective actions, and submit the results to the certifying activity for review and approval.

Implementation of the original MIL-STD-1772 procedure identified areas where improvements could be made without reducing the standard's effectiveness in certifying and qualifying hybrid microcircuits and vendors. Those areas included testing which were found to be excessive and redundant in many cases. Also, allowing the start of qualification testing, prior to line certification resulted in various interpretations of MIL-STD-883 test methods, and in some cases, poor manufacturing discipline. This resulted in processing inconsistencies. Accordingly, a two phase system consisting of line certification and process qualification was considered and subsequently implemented in Revision A to MIL-STD-1772, dated, May 15, 1987. The two phased program requires that the manufacturer achieve Section A line certification before performance of qualification testing to Section B. Using this approach, the certifying activity can evaluate a manufacturer's facility and processes and provide feedback identifying any deficiencies before implementation of Section B testing, thus eliminating any problem areas. In an effort to expedite QML listings the proposed Revision B to MIL-H-38534 will once again permit qualification testing prior to certification. Manufacturers that take advantage of this option should be confident of their ability to pass the Section A audit as the acceptance of the qualification data will be contingent upon its result. This approach reduced and streamlined the number of tests and added a new Qualification Option, Section B-5, to allow actual functioning hybrids or test vehicles to be used for qualification testing. In addition, the preconditioning of test samples was changed from the worst case combination of process steps to being fully screened to Test Method 5008 of MIL-STD-883.

Upon successful completion of Section B qualification testing, the manufacturer and approved materials and processes are listed on the QML. Included are such categories as: substrate fabrication, substrate attachment, die and element attachment, internal wire bonding and sealing, delidding, and resealing. Figure 6 shows the user that companies are actually utilizing the QML system. Compliant Standard Military Drawings (SMDs) are listed along with the number of other compliant products built.

Manufacturer	Cage Code	Symbol Code
Analog Devices Incorporated Micro Electronics Division 829 Woburn Street Wilmington, MA 01887	51640	CEUJ

PRODUCT ELIGIBILITY: The manufacturer, IC Analog Devices Inc., has certified that the following listing of hybrid microcircuits are built, tested, and shipped using the above certified FLOW/QUALIFIED MATERIALS and MANUFACTURING TECHNIQUES and are in FULL COMPLIANCE with MIL-H-38534 and MIL-STD-1772 requirements. The listing does not in anyway represent or imply interchangeability, equivalency.

SPECIFIC PRODUCT TYPES				
Standardized Military Drawing (SMD)	ESDS Class	Manufacturer Similar Part Number 4/	Product Type/Description	Shipped
8300201JX	1	DAC87	D/A Conv., 12-bit, programmable	Yes
8503001XX 5/	1	2700SD	Reference, Precision Voltage, +10V	Yes
8503002XX 5/	1	2700UD	Reference, Precision Voltage, +10V	Yes
8503003XX 5/	1	2701SD	Reference, Precision Voltage, -10V	Yes
8503004XX 5/	1	2702SD	Reference, Precision Voltage, +/-10V	Yes
8503005XX	1	2702UD	Reference, Precision Voltage, +/-10V	Yes
8503006XX	1	2701UD	Reference, Precision Voltage, -10V	Yes
5962-8850901XX	1	AD390S	D/A conv, 12-bit, bipolar, linear, quad	Yes
5962-8850902XX	1	AD390T	D/A conv, 12-bit, bipolar, linear, quad	Yes
5962-8851001XX	1	AD394S	D/A conv, 12-bit, bipolar	Yes
5962-8851002XX	1	AD394T	D/A conv, 12-bit, quad, bipolar	Yes
5962-8851003XX	1	AD395S	D/A conv, 12-bit, quad, unipolar	Yes
5962-8851004XX	1	AD395T	D/A conv, 12-bit, quad, unipolar	Yes
5962-8865801XX	1	AD578X	A/D conv, 12-bit, high speed	Yes
5962-8865802XX	1	AD578T	A/D conv, 12-bit, high speed	Yes
5962-8865803XX	1	AD578ZSD	A/D conv, 12-bit, high speed	NO
5962-8865804XX	1	AD578ZTD	A/D conv, 12-bit, high speed	NO

Figure 6: Hybrid Microcircuit QML-38534-10 Example

Using the new procedure and judiciously selecting a set of test samples, a manufacturer can qualify all processes and materials included on his unique test sample. For example, a vendor could conceivably cover all manufacturing processes and materials through the use of a very complex hybrid as a test vehicle. On the other hand, by using simple devices which have limited coverage, a multiple set of test samples would be required to cover all processes. It is left up to the manufacturer to determine which method best suits his needs. As the government

and industry gained experience with the implementation of MIL-STD-1772, modifications have been made to reduce the cost of qualification without compromising the continuous production of quality, highly reliable product.

2.2 Hybrid Microcircuit QML Program Activity

Interest in being certified and qualified to MIL-STD-1772 and listed on the hybrid microcircuit QML exceeded all government expectations. More than 150 companies requested the DESC information packet, which provided information on the program. As a result of this strong manufacturer interest and the newness of the system, it became difficult to audit all potential companies on a timely basis. To assure that companies ready for evaluation would be audited in a timely manner, the government revised the certification and qualification procedure. A streamlined program was established and based on a vendor self audit to standard procedures, prior to the performance of an audit by DESC. This minimized the extensive evaluation of the manufacturer's facility that was needed in previous versions of MIL-STD-1772 and required more manufacturer responsibility and greater emphasis on self-audits and controls.

In summary, major changes made to the original Hybrid Microcircuit QML procedure are:

1. The two step line certification and process qualification procedure was introduced requiring MIL-STD-1772 Section A line certification prior to the performance of qualification testing to Section B

2. The addition of a new qualification procedure (option B-5) that simplifies the complex test flows while still maintaining the original tests and conditions that show a degree of margin above and beyond normal screening and (QCI) requirements

3. Established new audit procedure.

4. Increased certification period from one to two years and incorporated MIL-H-38534 (MIL-STD-1772B dated 22 August 1990)

The DESC, RL's agent, is responsible for the certification and qualification of vendors and product and maintaining the QML.

2.3 Hybrid Microcircuit General Specification

The successful implementation of the hybrid microcircuit QML resulted in the issuance of MIL-H-38534 on 31 March 1989 which replaced MIL-M-38510 and Appendix G as the controlling document for hybrid microcircuits.

MIL-H-38534 establishes the general requirements for hybrid microcircuits and specifies the quality and reliability assurance requirements which must be met in the procurement of "fully compliant" military hybrid microcircuits. Individual characteristics of a given hybrid microcircuit type are defined by the procurement documentation which includes the purchase order, detail drawings and specifications. It is important to note that a hybrid device must meet without exception all of the applicable requirements of MIL-H-38534 to be deemed a "MIL-H-38534 compliant hybrid microcircuit" and to be marked with the compliant identifier, "QML" (Qualified Manufacturers List). Only manufacturers who have been certified and whose processes/devices have been qualified are listed in the QML by DESC.

The types of devices covered by MIL-H-38534 include but are not limited to traditional custom and standard product hybrid microcircuits and Radio Frequency (RF)/Microwave hybrid/integrated microcircuits. Three (3) quality assurance requirement options are currently provided which are directed at but not limited to the following:

a. Low volume custom devices (Option 1)

b. Medium volume custom and catalog standard devices (Option 2)

c. High volume catalog standard devices (Option 3)

Today, most hybrid QML vendors are baselined to Option 2 and are now moving toward Option 1.

A manufacturer is required to elect any one of the options for a hybrid microcircuit type prior to starting to build. Normally, this would be done at the time the contract for the device is negotiated or, in the case of standard devices, when the device is released to manufacturing. Quality Assurance (QA) requirements for each option are summarized in Table 1.

Table 1: MIL-H-38534: Quality Assurance Requirements

Requirement	Reference Paragraph	Option 1	Option 2	Option 3
Certification General MIL-STD-1772	3.4.1 3.4.1.1	Required Section A	Required Section A	Required Section A
Qualification Product, MIL-STD-883	3.4.1	Not Required	Not Required	Method 5005, test conditions A, B, C, D
Process, MIL-STD-1772		Section B	Section B	Not Required
Configuration Control	3.4.1.3 and 3.4.7	Required	Required	Required
Traceability	3.4.6	Required	Required	Required
Element Evaluation	3.2.4 and 4.4	Required	Required	Not Required
Process Control	3.4.3	Required	Required	Required
Serialization	3.6.6	Class K	Class K	Class K
Screening	3.4.4 and 4.5	Method 5008	Method 5008	Method 5004 except preseal Method 2017
Quality Conformance Inspection Group A Group B Group C Group D	3.4.5 and 4.6	In-Line 4.6.2.1.1 4.6.2.1.2 4.6.2.1.3 4.6.2.1.4	Method 5008 4.6.2.2.1 4.6.2.2.2 4.6.2.2.3 4.6.2.2.4	Method 5005 4.6.2.3 4.6.2.3 4.6.2.3 4.6.2.3

Option 2 requirements are similar to the requirements that existed in MIL-M-38510G and MIL-STD-883C, Test Method 5008. For this option a manufacturer must be certified and qualified in accordance with MIL-STD-1772, Section A and B and Quality Conformance Inspection (QCI) is performed as an end-of-line function.

For Option 2 QCI, Group A and B are performed on each inspection lot; Group C is performed on the first inspection lot and for changes; and Group D is performed on the first inspection lot and then on a periodic basis thereafter.

Option 1 requirements are the same as Option 2 except in-line Group B and D testing, instead of end-of-line QCI is required. In-line Group B testing, highlighted later in this report, is essentially a series of process control oriented inspections assuring conformance of products built with controlled processes and eliminating the need for end-of-life product testing.

Option 3 requires MIL-STD-1772, Section A certification; however, qualification is to be performed on a product-by-product basis in accordance with MIL-STD-883, Method 5005 rather than process qualification as required by MIL-STD-1772, Section B. QCI for this option is performed periodically in accordance with MIL-M-38510, Paragraph 4.5 and Groups A, B, C and D of MIL-STD-883, Method 5005. Also,

element evaluation is not required for this option and screening is performed in accordance with MIL-STD-883, Method 5004, except preseal visual is in accordance with Method 2017.

Revision A to MIL-H-38534 included the addition of "The One Part-One Part Number-One Drawing Standardization System"[2] and the Standard Military Drawing (SMD) requirements as the format to be used in preparing detail specifications.

The development and implementation of the first QML system was both successful and rewarding. The statement made in Figure 7, was true in 1513 and was found to still apply in establishing the QML which now contains thirty-five qualified and 52 certified vendors.

> *'It must be Remembered that there is nothing more Difficult to Plan, More Doubtful of Success, Nor More Dangerous to Manage, Than the Creation of a New System. For the Initiator has the Enmity of all Who Would Profit by the Preservation of the Old Institutions and Merely Lukewarm Defenders in Those Who Would Gain by the New Ones.'*
>
> *Niccolo Machiavelli, 'The Prince,' (1513)*

Figure 7: A Thought-Provoking Quote

3.0 MONOLITHIC QML

In addition to the QPL difficulties described in Section 1.0, during the early eighties other major changes were noticed in the types of microcircuits available for use in military systems. Application Specific Integrated Circuits (ASICs) (i.e., gate array, standard cell (i.e., semi-custom, full custom)) OEM designs, foundry fabricated and assembly house packaged devices, started to appear. Device characterization/ specification resulting in JAN QPL MIL-M-38510 slash sheets was decreasing. Figure 8 graphically shows the decrease of available microcircuit JAN specification/slash sheets and the increase of Specification Control Drawing (SCD) and Standard Military Drawings (SMDs) to procure microcircuits for military systems. Due to the success of the hybrid microcircuit QML and the need for quality and reliability improvement concepts the decision was made to evaluate the extension of the QML system for monolithic microcircuits. RL efforts[3,4] in this time frame outlined the

2 RAC Quarterly, Volume 1, Issue 1
3 RADC-TR-82-43, "Quality Assurance Procedure for LSI"

start of the monolithic QML procedure. Test Method 5010 "Test Procedures for Complex Monolithic Microcircuits" of MIL-STD-883 was developed for use in defining and testing complex microcircuits which included OEM design, fabrication at a foundry and packaged at another location. Generic qualification, the standard evaluation circuit (SEC), wafer acceptance, computer-aided-design (CAD) and the cell library approval procedures were conceived and developed. Gate array specifications, MIL-M-38510/605 for Complementary Metal Oxide Semiconductor (CMOS) Technology and /600 for bipolar technology were developed. These specifications are not typical because they do not contain performance parameters but instead include generic qualification, screening, and certification requirements. Gate arrays, the simplest form of an ASIC, were chosen to demonstrate the new concept. Basically all wafers are processed the same with the personalization of final metal layers used to functionalize devices. This approach allowed early evaluation of the generic qualification concept. The advent of the VHSIC program and the work of the Very High Speed Integrated Circuit (VHSIC) Qualification Committee further emphasized the need for generic qualification and the Monolithic QML.

3.1 Generic Qualification

The foundation of Generic Qualification is the implementation of Total Quality Management (TQM) within the manufacturing environment and requires that all levels of management and nonmanagement be actively involved in the commitment to quality. A Technology Review Board (TRB) that represents the company must be established to control, stabilize, monitor and improve the qualified technology. The Boards first duty is to develop a Quality Management Plan that outlines how the manufacturing operation for a given technology is controlled, monitored and improved throughout its entire "Life Cycle." Key aspects of this plan are the establishment of Statistical Process Control (SPC), Field Failure Return Programs (FFRP), Corrective Action Procedures, Quality Improvement and

[4] RADC-TR-85-219, "Quality Procedures for VLSI/VHSIC Type Devices"

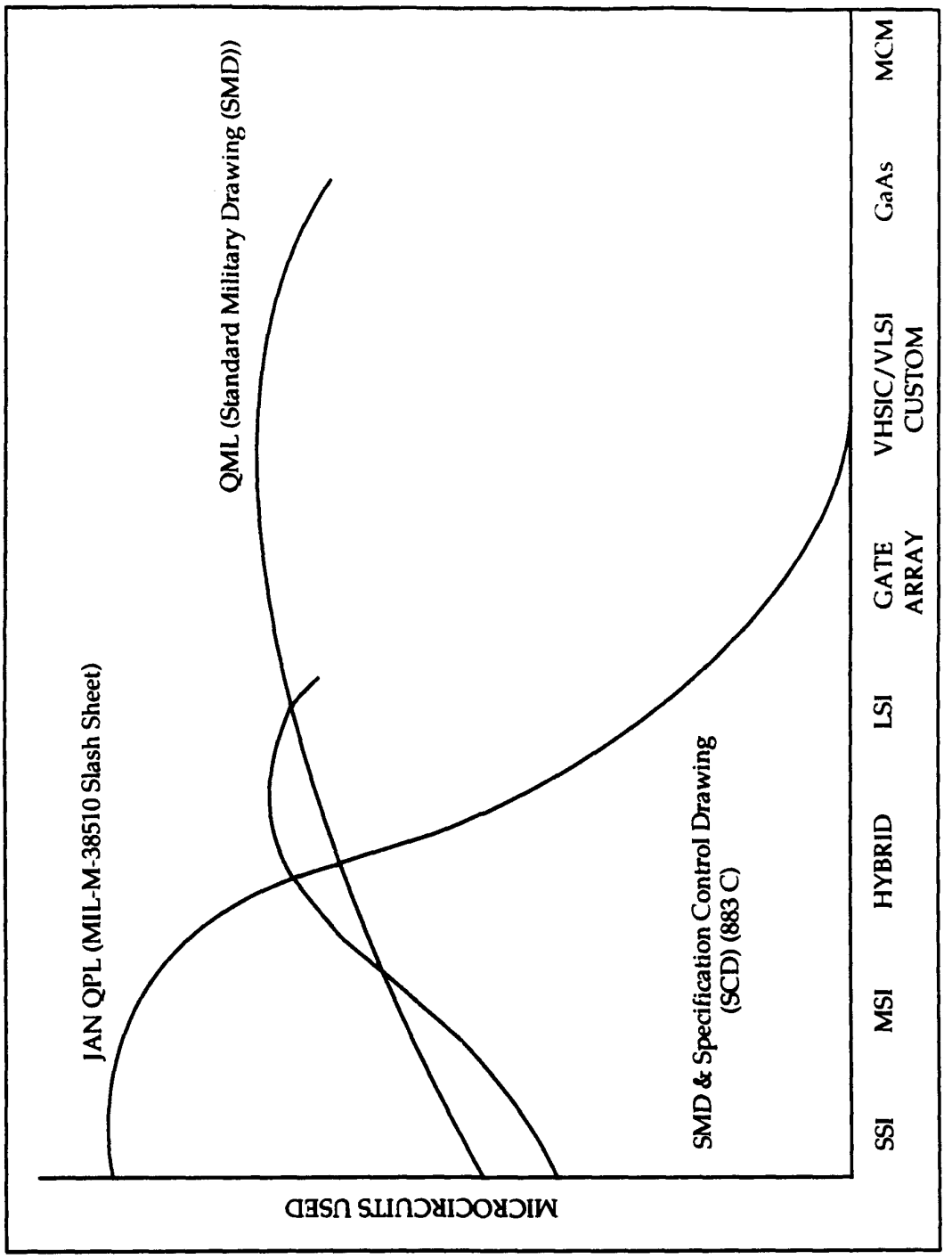


Figure 8: Device vs. Specification Profile

any other approaches required to control and improve product quality and reliability. These requirements are detailed in MIL-I-38535.

Further, MIL-I-38535 describes procedures and requirements for listing manufacturers on the QML for ICs. Manufacturers listed on the QML are able to produce microcircuits without the need for extensive end-of-manufacturing qualification testing and quality conformance inspections on each device design. Any reduction of end-of-manufacturing testing will be replaced with in-line monitoring and testing and SPC. Also, surrogate devices, such as the SEC are used to assess the technology's reliability. Introduction of this methodology shifts the emphasis from the need of individual microcircuit qualification to process (technology) certification and qualification thereby accelerating the insertion of high quality and reliable microcircuits.

The generic qualification philosophy, leading to QML, is a process by which a manufacturer acquires a manufacturing line or technology flow certification and qualification. Ongoing monitoring techniques are used to maintain QML status. The manufacturing line consists of facilities and procedures appropriate to accomplish the design, mask making, wafer fabrication, assembly, package and testing of microcircuits (see Figure 9). Figure 10 illustrates six possible combinations of a manufacturing line utilizing three design centers, two mask fabrication facilities, three wafer fabrication facilities, two package/assembly sites and two test facilities.



Figure 9: Manufacturing Line

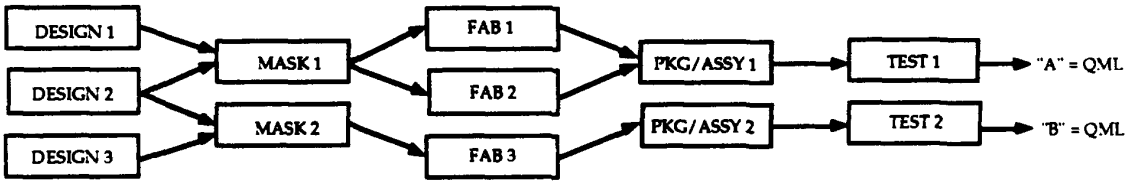


Figure 10: Manufacturing Line Combinations

The procedure of generic qualification is accomplished in two stages: certification and qualification. The process of certification is the recognition of evidence by the Qualifying Activity that the manufacturing line is capable of producing microcircuits of high quality and compliant with the requirements. Qualification is the actual demonstration of the certified manufacturing line capabilities by

producing compliant "first pass" microcircuits. In Figure 10, each block can be individually reviewed, but must be certified as a flow. The only process flow which would be qualified (QML listed) would be the group of blocks which are linked together and tested during qualification. The letters "A" and "B" in Figure 10 indicate a QML flow where qualification testing has qualified a complete path. The other paths are not listed until certification and qualification testing of the processes is done. The complete generic flow process is illustrated in Figure 11.

TQM does not stop with a manufacturer being listed on the QML. MIL-I-38535 identifies the necessary screens which still must be done on each device built. However, these screens can be reduced or changed by the manufacturers TRB when reliability data gathered on the technology indicates that such changes are appropriate.

The philosophy of generic qualification incorporates the idea that high quality and reliable microcircuits can be obtained without excessive testing if the processes are properly monitored and controlled at each step of the manufacturing line. The following paragraphs describe the monitors and controls which may be used.

1. The design procedure and tools are controlled in such a manner that the ensuing microcircuit design performs only within limits that have been shown to be reliable for the technology being used, within the constraints of established design rules (electrical, geometric and reliability)

2. The mask fabrication facility is controlled such that an error free mask is produced from the microcircuit design database. Monitoring, controlling and reducing defect density is helpful in obtaining error free masks.

3. The wafer fabrication process is controlled with the following:

   - use of in-line statistical control
   - use of a Parametric Monitor (PM) structure for measuring electrical parameters
   - use of a Technology Characterization Vehicle (TCV) structure to study intrinsic reliability mechanisms
   - use of a Standard Evaluation Circuit (SEC) to monitor the fabrication process and to serve as a surrogate microcircuit for reliability testing

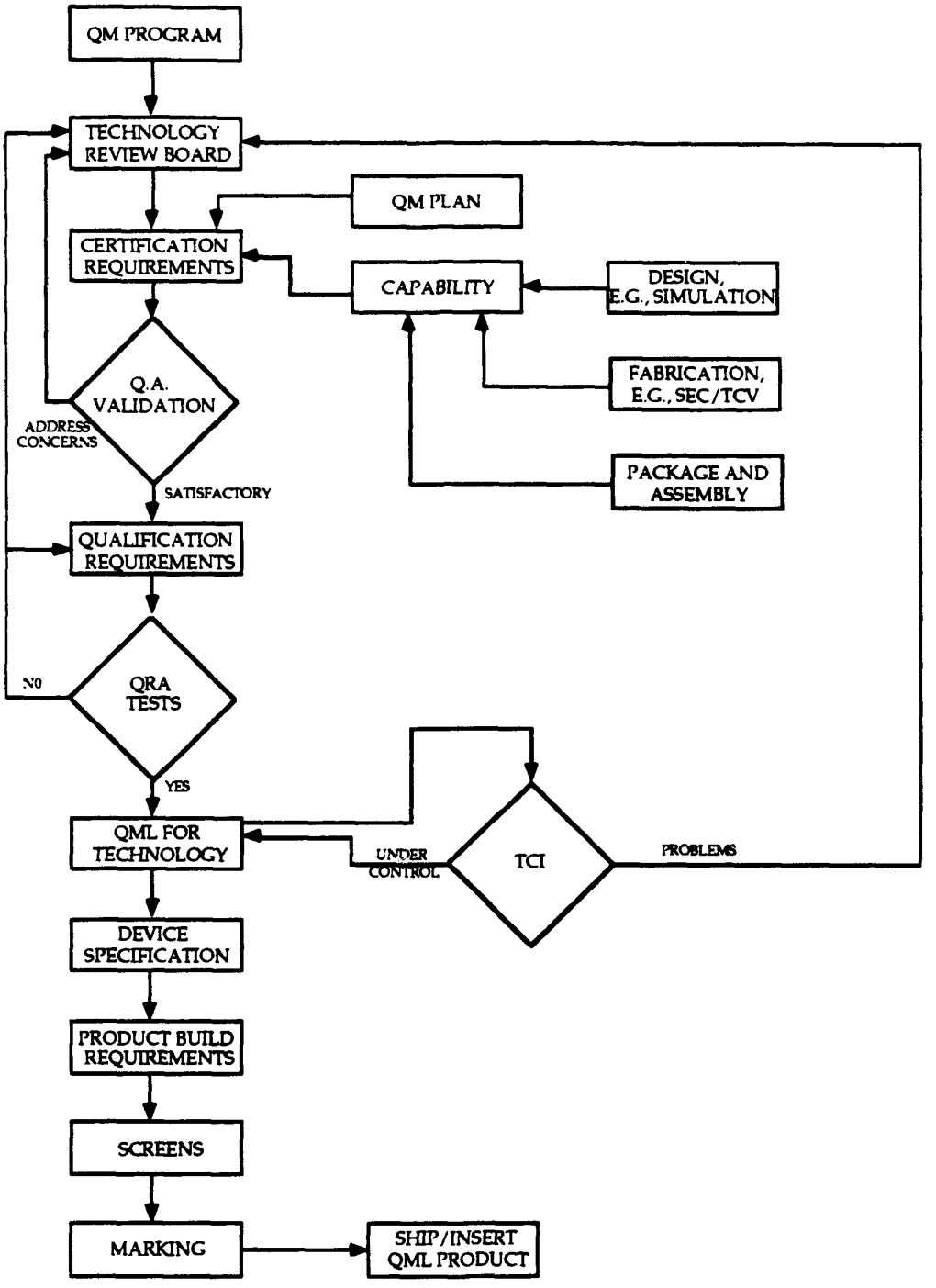


Figure 11: Generic Qualification Flow Diagram

4. The package/assembly facility is controlled with emphasis on in-line statistical process control of all assembly steps and package certification prior to microcircuit assembly.

5. The test area controls ensure test equipment accuracy and calibration as well as a controlled interface to the microcircuit design center.

6. The overall control of the processes are under the auspices of a Technology Review Board (TRB) which is established by the manufacturer. The TRB is solely responsible for the QML flow that has been certified and qualified.

7. For Radiation Hardness Assurance (RHA), procedures and requirements are used for establishing and demonstrating a Radiation Hardened Assurance Capability Level (RHACL) for the technology. Many device oriented tests can be reduced or eliminated when correlation data for models and test structures have been established by the TRB. The main concern in the RHA community is whether the device specification accurately describes the device performance in the radiation environment specified. Until such models and test structures are developed, some actual device radiation testing will be required.

8. An appendix to MIL-I-38535 defines an implementation approach which may be used for space or other critical environment applications.

3.2 General Specification for Silicon Monolithic Microcircuits

In 1986 RL awarded a DoD VHSIC Program funded contract to General Electric, Utica, NY; AT&T Bell Labs, Whippany NJ; and Honeywell, Plymouth MN, to establish the guidelines and requirements for a QML system for complex monolithic microcircuits such as ASICs.[5] To broaden the base for key technical inputs, an Industry Coordinating Working Group (ICWG) consisting of over 90 colleagues from the DoD, vendor and OEM communities was established. The ICWG was divided into five distinct technical areas and developed the technical tools necessary to implement a quality and process oriented system. The output was integrated into a complete procedural guide and requirements document entitled "QML - Implementation Requirements for Microcircuits," dated April 1988 which was the predecessor to MIL-I-38535, dated 18 December 1989. The format of MIL-I-38535 makes it a "living document" and sets the standards for a TQM system for monolithic silicon microcircuits.

[5] RADC-TR-90-405, "Qualification Procedures for VHSIC/VLSI"

This RL effort solidified the approach to develop a QML concept which qualifies the manufacturing building blocks or processes used to manufacture complex silicon devices. Therefore, through qualification of the processes and building the device correctly at all stages of the manufacture, quality is no longer tested in, but rather quality is designed and built in.

3.2.1 Total Quality Management

The main goal of any qualification system is to stress quality and reliability throughout all phases of the product development and build. The implementation of a TQM program, a DoD initiative for continuously improving quality at every level, has been embraced by Generic Qualification as the cornerstone for quality and reliability improvement and assurance. Every manufacturer who applies for QML status must demonstrate implementation of the principles of TQM (Table 2) and the Qualifying Activity will assess the manufacturer's approach to TQM during certification and qualification.

Table 2: TQM Principles[6]

TQM PRINCIPLES	
Continuous Process Improvement	Constancy of Purpose
Process Knowledge	Total Involvement
User Focus	Teamwork
Commitment	Investment in People
Top-Down Implementation	

To assure that all aspects of device fabrication are involved, the manufacturer must establish a TRB consisting of key individuals from necessary disciplines, (i.e., design, fabrication, mask making, assembly, package and test). The TRB is responsible for the implementation of a TQM program throughout the entire manufacturing operation and for the establishment of well controlled, understood and stable processes which are the key foundations of a quality product. Work is ongoing to include the TRB concept in the hybrid QML.

3.2.2 Silicon QML Requirements

MIL-I-38535 is divided into five areas of requirements as shown in Table 3. The first area involves the establishment of a TRB and a TQM program which were outlined earlier. The certification and qualification requirements assess whether the TRB has

6 DoD TQM Pamphlet, 1988

accomplished its tasks and validates the technology flow. Certification, a three step process involves: documentation of process control, demonstration of process capability, and validation review by the qualifying activity. This phase is the key step in assuring that the building blocks for a technology flow are complete and capable.

Table 3: QML Requirements

Phase 1 TQM Program Technology Review Board - TQM Implementation - Controlled, Stable Process	Phase 4 Product Procurement Specification - Customer Interface - Critical Parameters
Phase 2 Certification - Document Process Control - Demonstrate Process Capability - Validation Review	Phase 5 Product Tests - Screening - Electrical/Mechanical - Sample Testing
Phase 3 Qualification - Complex Product Built/Tested	

The documentation of process control involves a review of a manufacturer's critical documents for TQM implementation including quality improvement plan, SPC program, field failure return program, corrective action plans, change control and product recall program. These plans typically exist in every manufacturer, but are seldom brought under one controlling umbrella. Under TQM these are brought under the auspices of the TRB who is solely responsible for the development and implementation of the programs/plans. This responsibility may be delegated to others, but the TRB must monitor to see that things are being accomplished.

The demonstration of process capability is the most involved portion of the certification phase where each of the key disciplines is assessed to determine successful implementation of a QML program. In the design area, model verification, chip performance, layout verification, and testability/fault coverage verification are tested to assess their capabilities. Under Model Verification, the manufacturer must demonstrate how the models, for example, fabrication process models, are developed, verified and controlled. Some key indicators are whether the manufacturer continuously strives to improve his models and sets sigma limits on the output of the tools.

The chip performance requirement assesses how well the manufacturer's post-layout simulation predicts the measured results from actual silicon over ranges of temperature and voltage. The layout verification refers to the rules used to check a

design. These include design, electrical and reliability rules. Table 4 defines, in more detail what these rules entail. Finally, for testability which is a major concern, the manufacturer must demonstrate a capability to design utilizing testability features along with the fault coverage analysis capability. The results of all these requirements' assessments are deliverable to the Qualifying Activity before the Validation Review is scheduled.

Table 4: Layout Verification

Design Rules	Electrical Rules	Reliability Rules
Geometric Physical	Connectivity Opens/Shorts	Single Event Upset (SEU) IR Drop ESD Hot Electron Latchup Electromigration Time Dependent Dielectric Breakdown (TDDB)

To assess the capability of the fabrication process, the manufacturer must build and test a group of test structures. These include the Technology Characterization Vehicle (TCV), Parametric Monitor (PM), and Standard Evaluation Circuit (SEC). The roles that each of these play in establishing and controlling the stability, quality and reliability of the fabrication process are described in Table 5.

Table 5: Fabrication Test Vehicles

Test Vehicles	Role
Technology Characterization Vehicle	Assess Intrinsic Reliability Failure Mechanisms
Parametric Monitors	Assess Electrical Characteristics of Wafer after or during Processing
Standard Evaluation Circuit	Assess Process Reliability

The assembly, package and test areas also require a process capability demonstration including modeling of package electrical and mechanical characteristics, control of assembly materials, assessment of moisture control in packages and evaluation of final tests. Once all the processes have been assessed, the manufacturer demonstrates and evaluates the interfaces between the building blocks for completeness.

This total review differs from today's QPL audits and has been renamed a validation review. The change is from a "how to" approach to one that evaluates that the procedures are correctly derived from premises supported by sound experiments designed to validate an approach. It concentrates on management issues and attempts to minimize the number of actual spot checks. Crucial is the determination of whether the TRB is in control of the complete technology flow and whether the various disciplines are working together. Other key areas assessed will be the manufacturer's capability to convert the customer's requirements to a workable specification, software "configuration" control and documentation of design for future replacement.

The last step in achieving QML status is the Qualification Phase. Here the manufacturer builds complex products utilizing the certified processes and tests the product to a series of qualification tests. Upon successful completion of the tests, the manufacturer will be listed on the QML for the approved technology flow.

3.2.3 QML Monitoring

For a vendor who is listed on the QML all products produced and tested on the approved QML flow are considered qualified. After qualification has been granted, Generic Qualification takes the approach that the TRB is the controlling authority (i.e., determining whether a product has a reliability or quality flaw which requires a recall) to assure that the proper quality and reliability tests are performed to confirm the quality level of a technology flow. With this degree of freedom, how does the Qualifying Activity assure that the process is operating correctly? This is done by monitoring and reviewing the Status Reports of the TRB which summarize the activities which are ongoing within the QML technology flow. Proposed changes to the process are discussed along with the action items of the TRB within the Status Reports. The intent of the TRB is to allow the manufacturer to set his own quality goals and strive to achieve them without interruption from the Qualifying Activity or other customers. However, if product reliability or quality degrade or TRB reports indicate other potential problems, the right to investigate and question the TRB documentation supporting any changes to their originally certified procedures can be exercised and QML status can be changed.

3.2.4 Device Procurement Specification

Appendix A of MIL-I-38535 contains a Device Procurement Specification section which outlines the critical parameters which must be identified as part of any device manufacture. The parameters listed are technology oriented and need to be expanded to cover other technologies such as linear, bipolar and GaAs. In general, this section is intended to be a checklist for the customer and vendor to use as a guideline in defining the requirements of the ASIC. This specification becomes the criteria to assess whether "first pass success" was achieved by the designer. In other words, does the first silicon of the design meet the negotiated specification?

3.2.5 Product Tests

TQM does not stop when a manufacturer is listed on the QML. Every time a device is manufactured it must go through the certified/qualified processes and must be screened to the requirements of MIL-I-38535. For each design, physical, electrical, and reliability rule checks, along with device simulation and testability (fault coverage) evaluation, must be done before it is released to fabrication. In the fabrication arena, evaluation of test structures must be accomplished to assess whether the proper steps were performed on the wafers. After assembly of the devices, the QML certified screens must be done (i.e, burn-in, thermal cycling and leak testing). The Technology Conformance Inspection (TCI) tests, which replace Quality Conformance Inspection (QCI) tests, no longer apply to each individual product, but do apply to the processes and are accomplished through testing on the SEC per the certified TCI schedules. However, Group A electrical tests on the product are still required.

Another key aspect of Generic Qualification is the flexibility in TCI and screening allowed. If the TRB has sufficient data to substantiate a reduction or change to a given test, it can be done. This allows the manufacturer to introduce innovative tests and new process flows as a natural progression of the technology maturity.

3.2.6 Concept Demonstration

In order to demonstrate the applicability of the MIL-I-38535 requirements to establish a quality process oriented system, two Alpha sites and eight Beta sites were chosen. Table 6 lists these participants. The Alpha sites were part of the original RL 1986 contract while the Beta sites were all voluntary participants with high level management commitment. The Alpha and Beta site companies hosted meetings with members of various DoD organizations to discuss the QML concept, requirements and procedures detailed in MIL-I-38535 resulting in changes to the original requirements.

After the start of the actual QML certification/qualification process additional companies were added to the potential list of QML participants/candidates. Section 4.0 gives the QML status as it exists today.

Presentation and discussion of the QML program and criteria occurred at the annual VHSIC Qualification Workshop (circa 1985) and is now called the Advanced Microelectronic Technology, Qualification, Reliability and Logistics Workshop which will be held 13-15 August 1991 in Seattle Washington and the QML program will again be an integral topic of discussion. Also RAC in conjunction with NECQ and EIA sponsored a QML Workshop on 6-7 June 1990 in Dayton Ohio where QML activity/status from DoD, OEM and vendor perspectives were openly discussed.

Table 6: Alpha/Beta Demonstration Participants

Alpha Sites	Beta Sites
General Electric - Design (Utica, NY) - Manufacturing (Research Triangle Park, NC) AT&T (Allentown, PA)	Harris (Findlay, OH) (formerly RCA) LSI Logic (Milipitas, CA) Harris Semiconductor (Melbourne, FL) Intel (Chandler, AZ) IBM (Manassas, VA) Texas Instruments (Dallas, TX) National Semiconductor (Santa Clara, CA) VLSI Technology (Tempe, AZ)

3.2.7 Field Failure Return Program

A key aspect of the QML process is the establishment of a field failure return program. The field failure program is a cradle to grave concept including QML vendor identified problems, OEM incoming inspection, manufacturing and qualification/acceptance testing fallout and failures during deployment. The government, OEMs, and component vendors have long recognized the need to capture field experience and use it to improve system reliability. This need is the driving force behind establishment of a DoD Field Failure Return Program. Its mission is to improve the reliability and cost-effectiveness of equipment by channeling component manufacturing, quality and field failure experience data to designers, manufacturers, and maintainers. In pursuit of this objective, the program:

- Compiles vendor outgoing inspection and field failure data with attention to manufacture data code, source equipment and failure mode information

- Identifies "high burners," using collected data, external databases, and information from contacts, and focuses data collection and lab testing to pinpoint the root cause of failure

- Recommends corrective actions to minimize the cost and risk of similar failures, such as replacement, redesign, and/or part requalification.

- Makes manufacturing quality and field failure data available to designers and OEMs to allow intelligent part selection.

- Prioritizes R&D efforts on basic reliability physics problems such as electromigration, package integrity, outgassing of polymeric materials and electrostatic discharge.

3.2.8 Radiation Hardness

In the QML procedure radiation hardness of the device is considered a unique technology which must undergo certification where the process is baselined and controled and parameters for a radiation hardness assured capability level (RHACL) is demonstrated. The philosophy is that each QML vendors RHACL must be demonstrated to show that he can meet the radiation hardness requirements and specifications of his selected market. Typical QML qualification will demonstrate that his technology operates and performs in conformance with the RHACL. The key phase of the QML implementation on radiation hardened technology conformance verfies that the radiation hardness (i.e., the RHACL) of individual wafer lots conforms to the capability of the process. The manufacturer can perform either (1) standard technology conformance inspections, (e.g., Group E testing of IC's for total-dose radiation hardness), or (2) in-line control testing at the wafer level on parameters and structures relevant to the radiation response. Even though a manufacturer's technology flow is listed on the QML, sample testing of each new design must be performed to determine its actual radiation tolerance. This requirement can be waived if simulation models are verified and demonstrated to adequately address the critical issue of design validation.

There are meetings underway to redefine the radiation environments which will result in new RHA category levels. Until this occurs all parts will be marked with the M, D, R and H categories.

3.2.9 Space QML Application

Appendix B defines the requirements to supplement MIL-I-38535 for space system microcircuits and is intended to be a transitional document. The document includes NASA and Air Force Space Division representatives on the validation team, adds value added screening tests and modifies technology conformance inspection.

4.0 MICROCIRCUIT VENDOR CERTIFICATION/QUALIFICATION STATUS

How do OEM's/users know when device vendors complete the rigorous QML certification/qualification procedure? The government has chosen to use QML-38534-X (x is the issue number) for hybrid microcircuits and QML-38535-x for advanced microcircuits each with its own format. The information contained in the hybrid microcircuits QML reflects the material and construction techniques of the particular vendors test sample(s). Supplemental application and testing of additional material and construction techniques can be accomplished by application to and approval by DESC-EQ. Table 7 lists the manufacturers who are pursuing certification/qualification to MIL-H-38534. A sample hybrid microcircuit vendor, listing is included in Table 8. The information contained in the advanced devices QML reflects the actual operational flows that were certified by testing of the particular test samples. Again supplemental application and testing of additional material and construction techniques can be accomplished by application and approval by DESC-EQ. For descriptive purposes the following tables detail certification and qualification status by company for both hybrid and silicon. Table 9 lists the manufacturers who are actively pursuing certification/qualification to MIL-I-38535. Table 10 lists the technologies which have been certified to date for the monolithic QML. A sample microcircuit vendor listing is included in Table 11.

Table 7: Hybrid Manufacturers Pursuing Certification/ Qualification to MIL-H-38534

* Advanced Analog 2270 Martin Avenue Santa Clara, CA 95050-2781	* Aeroflex Laboratories Incorporated 35 South Service Road Planview, NY 11803-000
* Analog Devices Computer Labs Division 7910 Triad Center Drive Greensboro, NC 27409-9605	* Analog Devices Incorporated Microelectronics Division 831 Woburn Street Wilmington, MA 01887-000
* Apex Microtechnology Corporation 5980 North Shannon Road Tucson, AZ 85741-000	* Beckman Industrial Corporation Electronic Technologies Division 4141 Palm Street Fullerton, CA 92635-000
* Boeing Electronics Company Seattle, WA 98124-2499	Canadian Marconi Company 2442 Trenton Avenue Montreal, Quebec H3P 1Y9 Canada
* CTS Corporation Microelectronics Division 1201 Cumberland Avenue West Lafayette, IN 47906-000	Datel Incorporated 11 Cabot Boulevard Mansfield, MA 02048-1191
* Comlinear Corporation 4800 Wheaton Drive Fort Collins, CO 80525-000	* Film Microelectronics Incorporated 10B Centennial Drive Peabody, MA 01960-000
* Elantec Incorporated 1996 Tarob Court Milpitas, CA 95035-000	* General Microcircuits Corporation 780 Boston Road, Suite 1 Billerica, MA 61821-000
Hewlett-Packard Company Optical Communication Division 350 West Trimble Road San Jose, CA 95131-000	* Honeywell Incorporated Military Avionics Division 13350 U.S. Highway 19 South Clearwater, FL 33546-7290
* Honeywell Incorporated Sperry Commercial Flight Systems Group Phoenix, AZ 85036-111	Hughes Aircraft Company Ground Systems Group Fullerton, CA 92634-000
* Hughes Aircraft Company Microelectronics Circuits Division 500 Superior Avenue Newport Beach, CA 92658-8903	Hytek Military Microsystems Incorporated 400 Hot Springs Road Carson City, NV 89706-000
* Hycomp Incorporated 165 Cedar Hill Street Marlboro, MA 01752-000	* ITT Defense Avionics Division 100 Kingsland Road Clifton, NJ 07014-000

*Denotes companies that have passed Section B testing and are listed on the QML. All others are certified and in various phases of Section B testing.

Table 7: Hybrid Manufacturers Pursuing Certification/ Qualification to MIL-H-38534 (cont'd)

* ILC Data Device Corporation
105 Wilbur Place
Bohemia, NY 11716-000

* Interpoint Corporation
10301 Willows Road
Redmond, WA 98073-9705

* Martin Marietta Electronic Systems
Orlando, FL 32862-8007

* Micro Systems Engineering Inc.
6024 Southwest Jean Road
Lake Oswego, OR 97034-000

* Micropac Industries Incorporated
725 East Walnut Street
Garland, TX 75040-000

* National Hybrid Incorporated
2200 Smithtown Avenue
Ronkonkoma, NY 11779-000

Omnirel Corporation
205 Crawford Street
Leominster, MA 01453-000

* Raytheon Company
Microwave and Power Tube Division
465 Centre Street
Quincy, MA 02169-000

* Sipex Corporation
Hybrid Systems Division
22 Linnell Circle
Billerica, MA 01821-000

TRW Incorporated
Manufacturing Division
One Space Park
Redondo Beach, CA 92078-1001

* Teledyne Microelectronics
12964 Panama Street
Los Angeles, CA 90066-000

* Vitarel Microelectronics Inc.
6828 Nancy Ridge Drive
San Diego, CA 92121-2232

* Lockheed Sanders Incorporated
Daniel Webster Highway
Nashua, NH 03061-2041

Medtronic Incorporated
Micro-Rel Division
2343 West Tenth Place
Tempe, AZ 85281-5164

* Micronetworks Corporation
324 Clark Street
Worcester, MA 01606-000

* Natel Engineering Corporation
4550 Runway Street
Simi Valley, CA 93063-000

National Semiconductor Corp.
5901 South Calle Santa Cruz
Tucson, AZ 85746-3949

* Phillips Circuit Assemblies
Slatersville Division
100 Providence Pike
Slatersville, RI 02876-0278

STC Components Limited
South Denes
Norfolk NR30 EPX England

Solitron Devices Incorporated
Semi-Conductor Group
1177 Blue Heron Boulevard
Riviera Beach, FL 33404-000

* Teledyne Components
40 Allied Drive, Route 128
Dedham, MA 02026-000

Texas Instruments Incorporated
Microelectronics Packaging Systems
13532 North Central Expressway
Dallas, TX 75265-000

* Westinghouse Electric Corporation
Baltimore, MD 21203-000

*Denotes companies that have passed Section B testing and are listed on the QML. All others are certified and in various phases of Section B testing.

Table 8: Sample Hybrid Microcircuit Vendor Listing

MANUFACTURER	CAGE CODE	SYMBOL CODE
Analog Devices Incorporated Micro Electronics Division 829 Woburn Street Wilmington, MA 01887	51640	CEUJ

QUALIFICATION LETTER(S)	PRODUCT CLASS DESIGNATOR	RADIATION HARDNESS LEVEL	TECHNOLOGY TYPES
EQ(EQM-87-2531)	Class B	N/A	AD/DA Converters Voltage Reference
EQ(EQC-89-253)			Signal Processor

SUBSTRATE FABRICATION OPERATION (S) 1/

LOCATION: Wilmington, MA	LOCATION: N/A
FLOW: EE-QA-8419	FLOW: N/A
CAPABILITY: Thick film on alumina, 2 conductor levels, resistors	CAPABILITY: N/A

ASSEMBLY OPERATION(S) 1/

LOCATION: Wilmington, MA	LOCATION: N/A
FLOW: EE-QA-8122	FLOW: N/A
CAPABILITY: polymer conductive/non-conductive epoxy, gold & aluminum wire bonding	CAPABILITY: N/A

ADD-ON ELEMENTS: unpackaged die, chip capacitors, chip resistor
SUBSTRATE ATTACH: polymer nonconductive epoxy

PACKAGE INFORMATION: 1/2/3

PACKAGE TYPE:	Ceramic dual in-line
SEAL METHOD:	Seam Seal
LEAD COUNT:	32
SEAL PERIMETER:	4.35
LEAD FINISH:	Gold

Table 9: Microcircuit Vendors Pursuing Certification/Qualification to MIL-I-38535

Company	QM Plan	Cert. Date	Qual. Date	Level	Notes
AT&T	10/09/89	12/19/89	03/30/90	Q	
Gould/AMI	01/23/91				3
Honeywell	06/05/90	11/05/90	est. 3 Qtr. 91	Q, V, RHA	1
IBM	05/16/90	11/21/90	est. 3 Qtr. 91	Q, V, RHA	1
Intel	06/07/89	03/23/90	11/16/90	Q	
Texas Inst.	12/27/90				2

NOTES:
1. Third Party Design Pending
2. Validation Review 15 April 1991
3. Anticipated Validation Review 3 Qtr. 91
4. LSI Logic Motorola, National Semiconductor and VLSI Technology may request certification in 1991

Table 10: Certified QML Technologies

Company	Source Technology	Product
Intel	1.0 micron single, poly/double level metal	CMOS Standard Product (Microprocessor, Peripherals) processes and materials - 80386 80387
AT&T	1.25 micron, CMOS, Single and Double Level Metal	Full custom and standard cell processors and materials
IBM	1 micron, CMOS radiation hardened, flip chip, custom, semi-custom, gate array logic and memory processes and materials	
Honeywell	1.25 micron, CMOS, radiation hardened, single/double level metal custom, semi-custom logic and memory processes and materials	

Table 11: QML-38535-1

MANUFACTURER	CAGE CODE	SYMBOL CODE
AT&T Microelectronics 555 Union Blvd., Allentown, PA 18103	98379	CERU

TEST REPORT	PRODUCT CLASS DESIGNATOR	RADIATION HARDNESS LEVEL	TECHNOLOGY	DESIGN CENTER	MASK DEVELOPMENT
QML001 1289	Q	Non-Radhard	ASICS Full Custom/Standard Cell	LOCATION: Allentown, PA LINE: LAB 5227/5223 FLOW: A89AL1528	LOCATION: Allentown, PA LINE: MOS V FLOW: SIF-MK29-MFG. METH

WAFER FABRICATION OPERATIONS(S)

LOCATION: Allentown, PA LINE: MOS V FLOW: PFC-074-LOG84 & PEC-074-LOG185	LOCATION: LINE: FLOW:	LOCATION: LINE: FLOW:

ASSEMBLY OPERATIONS(S) 1/ TEST OPERATIONS(S)

LOCATION: Allentown, PA LINE: JIT MOS Ceramic Assy FLOW: SIF-QMP3-FLOW	LOCATION: LINE: FLOW:	ELECTRICAL LOCATION: Allentown, PA LINE: JIT MOS Ceramic Flow FLOW: SIF-QMP3-FLOW	ENVIRONMENTAL LOCATION: Allentown, PA LINE: Reliability Lab FLOW: QMP3-BIC/SIF-IL5349FLOW2

PACKAGE INFORMATION 2/

TYPE:	PIN GRID ARRAY	DUAL-IN-LINE	CHIP CARRIER	FLAT PACKS	MISC PACKAGES	MISCELLANEOUS DATA
CASE OUTLINE:	P-AE	D-10				
LEAD COUNT:	133	28				
MATRIX SIZE:	13 X 13	--				
LEAD FINISH:	Gold	Gold				

SPECIFIC PRODUCT TYPES 3/

STANDARDIZED MILITARY DRAWING (SMD)	ESDS CLASS	MANUFACTURER SIMILAR PART NUMBER 4/	PRODUCT TYPE/DESCRIPTION	SHIPPED
6962-9070401QXX	1(1.4)	WE-DSP-16	Digital Signal Processor, 16 BIT	No

4.1 Additional Generic Qualification Activity

Gate Array qualification is ongoing with various degrees of success. The MIL-M-38510 QPL is used to indicate vendor status. Table 12 summarizes current status of vendor qualification to the MIL-M-38510 Gate Array specifications:

Table 12: Gate Array Vendors Pursuing Certification/Qualification to MIL-M-38510

Vendor	Status
UTMC per/605	3μ CMOS - Part I Qualified 1.2μ CMOS - Awaiting changes to address Class S and Rad Hard issues
ATMEL per/605	.8μ CMOS - Considering QPL Activity
Raytheon per/706	Bipolar Technology - Part II Qualified

Activity has begun in the linear gate array area also. The bipolar technology is covered by MIL-M-38510/706 and Raytheon is Part II qualified. A specification to cover Bi-FET technology is being prepared and will be covered by MIL-M-38510/708.

The response to the RL gate array specification effort was less than expected. The format/procedure was the same as used for PROMS, without the generic certification requirements, which had reasonable success. Both specifications cover a nonfunctionalized device, unprogrammed for a PROM or prior to last metal for a gate array and uses an altered item drawing to define function/parametrics. One reason for the minimal response may be the emergence of the QML system.

5.0 QML CERTIFICATION/QUALIFICATION

The QML concept which changed from the QPL part by part qualification to a vendor/technology qualification where potentially every product is qualified generically also changed the certification philosophy. This is especially true for the monolithic QML where the audit has been changed to a validation. The previous emphasis on "how to" is now placed on evaluating premises and resultant conclusions allowing different approaches to various aspects of certification being acceptable.

In order to provide the most information to future applicants to the QML and to users/OEM's selecting a vendor, a lessons learned approach will be used for hybrid

microcircuits while a guidelines/typical question scenario will be provided for silicon microcircuits.

5.1 Hybrid Microcircuit Certification

Since the inception of the hybrid QML program, DESC has performed over 50 audits of hybrid vendors with varying procedures in place. Additionally many different reasons and motives were found to be factors for requesting a MIL-STD-1772 audit. Table 13 provides guidance in deciding whether or when you are ready to be assessed for inclusion on the hybrid microcircuit QML. A systematic and practical review or self audit of an existing system can be enhanced by using the tips provided in Table 14.

Table 13: Considerations Recommended for Resolution Prior To Requesting a MIL-H-38534 Audit

- Is the task of meeting MIL-H-38534 a sideline to meet certain customer driven requirements, or is the company/management committed to its use as a basis for doing business?
- Are the right people working the MIL-H-38534 requirements issue?
- Is hybrid fabrication and test in a production mode or strictly on a development or prototype basis? If the latter is the case, does the MIL-H-38534 QML make sense, can it work in our system?
- Are we required or will we be required to meet MIL-STD-883, MIL-H-38534, MIL-M-38510, or MIL-STD-1772? If not, do these specifications provide a baseline for doing business? Does our business plan include seeking orders for hybrids built to these requirements? Are processes, materials and procedures capable of meeting both certification and qualification requirements?
- Are processes and procedures well documented and do they thoroughly cover the operation? Does the company and do employees understand the importance of following procedures and maintaining a consistent operation?
- Does our company view military specifications as minimum requirements or as the maximum that we are required to do? Are they ever used to justify the existence or continuation of a bad process or practice even though common sense and good engineering judgement indicate otherwise?
- Do we promote an atmosphere of continual improvement? Are lines of communication open between the different company organizations? Is there a recognition of what continual improvement means throughout the company from management on down?
- Is our initial response to problems "get a waiver" or "it's not really a problem because we haven't had any customer returns"? Or is the policy to look at the reliability impact, fix the root cause of the problem and notify the customer if necessary?
- Do we have a customer return policy to adequately address and correct problems?
- Is first pass success stressed or is rework considered a fix-all?
- What kind of track record can we present - are we proud of it?

Table 14: Audit Preparation Tips

- Have one procedure for each operation. There should not be any difference in a competent operation whether it be for military or commercial use.
- Read and understand the specifications and standards. Ask questions up front. Do not assume a procedure is OK because that's the way it has always been done.
- Invite feedback and criticism from the people that actually perform the work.
- Implement all necessary procedures prior to performing a self audit.
- Take responsibility for running the program. Don't wait for the customer auditor to catch your problems. You may fail the audit as a result.
- Direct audit questions to the people that actually perform the work as opposed to the supervisors or managers. Observe the operation prior to asking questions. Verify that procedures are adequate, followed and that the applicable requirements are met.
- When reviewing logs and other records look for patterns (i.e., different operators over different times) and consistency of follow-on results. Records that look good may not be.
- Do not get audit "tunnel vision" but keep in mind how one operation may effect another.
- Relate process times, temperatures and other conditions to what the actual device will be exposed to during testing and the manufacturing process. Keep process repeatability in mind.
- Re-examine product workmanship practices.
- Perform an internal pre-qualification and analysis on your companies ability to pass the QML qualification tests.

5.1.1 Hybrid Audit Findings

The following analysis of audit findings highlights some of the most common problems detected during DESC audits of hybrid microcircuit manufacturing facilities. These findings are not intended to give details or provide a technical course of action for problems but rather contain a broad categorization of the problems. This information should assist manufacturers self-audit teams and user/OEM audit teams.

FINDING #1: Many of the screening and sample tests are not being performed correctly or to the requirements specified in the applicable military Test Method. The following lists the most frequent problems:

a. Internal Visual: Exceptions taken to wirebond, die attach, foreign material and element defect criteria.

b. Temperature Cycling: Performed to improper temperature conditions or in equipment not capable of meeting the required temperature recovery time. Instances of devices being tested prior to package seal.

c. Fine and Gross Leak: Pressure bomb not performed or performed improperly. Wrong leak rates used.

d. Constant Acceleration: Improper radius used to compute the required r.p.m. Dwell time started prior to the required acceleration level being reached.

e. Burn In: Incorrect temperature tolerance and times, load resistors used on more than one device; no revision control on burn-in boards; required socket and board checks not performed, cool down performed improperly; 96 hours electrical test window missed; and percent defects allowed (PDA) not computed or computed improperly.

FINDING #2: Lack of procedures and controls for incoming inspections, especially for integrated circuits (chips) and packages, as required by MIL-STD-883, Test Method 5008, Section 3.2.

a. Microcircuits not being test at 25°C, at maximum and minimum rated operating temperature.

b. Microcircuits wafer lot traceability requirements not being met.

c. Package evaluation (Table V of Test Method 5008) not performed.

d. Elements (e.g., failed element evaluation lots are being accepted for use in hybrids without even being reviewed by the manufacturer's internal material review board).

FINDING #3: Lack of environmental and contamination procedures and control as required preventive measures.

a. Many manufacturers have not addressed human contamination prevention.

b. Finger cots and gloves not used after devices are cleaned.

c. Smocks worn or carried into uncontrolled areas (e.g., cafeterias, machine shops, outside, etc.)

d. No gowning.

e. No spittle control (masks/shields).

f. A reliance by the manufacturer on internal package preseal cleaning to remove any human contamination, without realizing that it is largely ineffective in removing process trapped contamination (spittle under a wire bond, for example).

g. Devices are not maintained in a Class 1000 controlled environment after precap.

FINDING #4: Lack of rework controls and traceability which results in rework limitations being routinely exceeded.

a. Manufacturers had exceeded the rework and repair limitations specified in MIL-H-38534.

b. Deliddings performed in excess of allowance.

c. Epoxy cure temperature not localized to the defective elements.

d. Multiple rebond attempts made on die pads (only one permitted).

e. Die and element replacement limitations have been exceeded.

f. Hybrid microcircuits not being fully rescreened after rework.

g. Manufacturer not tracking all rework and repair performed on hybrids as required in MIL-H-38534.

FINDING #5: Lack of procedures and control in thick film fabrication areas.

a. Manufacturers have not documented all of the processes for thick film (e.g., printing, drying, resistor blending, firing).

b. Manufacturers continue to process product through drying and firing furnaces which are outside the specified profile.

FINDING #6: Quality conformance inspection (QCI) evaluation testing omitted or not performed properly.

a. Group B samples that are required for each inspection lot are being pulled from a previously passed Group B inspection lot to cover products from an entirely different inspection lot.

b. Groups A, B, C, D tests not performed in their entirety.

c. Inspection lots not formed, even though this is the basis for all acceptance testing.

d. No internal system to verify QCI coverage exists prior to shipment of product.

FINDING #7: Manufacturers (especially first time manufacturers to the program) consistently use DESC resources to determine compliance to the requirements and identify problems for corrective actions.

a. Self audits not effective in preventing return audits as part of the corrective action cycle.

b. Military Specifications requirement not thoroughly reviewed or understood.

FINDING #8: Failure of some manufacturers to properly apply Conversion of Customer Requirements to all military product. This is necessary because the customer's contractual requirements may require compliance, and at the same time require exceptions or noncompliance conditions, creating confusing and contradictory requirements.

CAUTION: The SCD/Contract must specify all exceptions or a written waiver must be obtained from the applicable military acquiring activity and must be available for review. When an order requires a complaint product or implies a product is compliant by referencing the applicable MIL-STD-883 screening/QCI tables, as a minimum the product shall meet all the requirements of MIL-H-38534 or MIL-M-38510. This includes being produced in a facility certified to MIL-STD-1772. The customer conversion procedure is intended to identify areas of noncompliance which requires action. This is for the protection of the contractor as well as the government.

a. There is a misconception by some manufacturers that additional product requirements are reason enough to process the product as noncompliant (example: a requirement to pass Internal Water Vapor testing on every inspection lot does not negate the basic compliance requirements).

b. A problem also exists that a manufacturer or customer believes that "close to compliance" is enough to claim compliance. A compliant part must meet all requirements of the applicable military specification.

FINDING #9: Electrical test accuracy requirements and temperature testing not in compliance with MIL-STD-883 requirements.

a. Difficulty in interpreting and meeting static parameters tolerances for certain precision devices.

b. Difficulty in controlling device test temperature during required electrical testing over the military temperature range.

5.2 Monolithic Microcircuit Certification

Certification of silicon microcircuit vendors has started and is summarized in Section 4.0. Experience data similar to that presented for hybrid microcircuit certification is limited at this time. As a result this section will discuss preaudit data and documentation submission requirements which must be reviewed by RL and DESC prior to scheduling a validation review. Appendix A outlines a typical validation review scenario that will allow the potential QML vendor to convince

the government validators that he has a quality organization and a stable baseline and with controlled technology for manufacture of reliable microcircuits.

5.2.1 Prevalidation Requirement Elements

The procedure begins with a manufacturer requesting the scheduling of a validation review of his facility, organization and technology flow. At this time he must establish that a QML program is in place and that he has implemented a self-audit program. This will assure that all critical processes/operations are identified and documented with valid supporting data leading to a successful audit. Additionally, this can allow for auditing a sample of the self assessed system resulting in approval of the implemented system. The next step is to submit a Quality Management (QM) plan per the DESC letter for "Scheduling of Validation Review, MIL-I-38535, FSC 5962." The following outlines the QM Plan.

QM Plan

The QM plan documents the major elements of the manufacturer's QML process, defines what the manufacturer is certified/qualified for and baselines his system from the time of certification.

(1) Index of certified baseline documents

A list of the specification titles, document numbers, and revisions which make up your QML program. This serves as the baseline that the manufacturer will be certified to at the validation review.

(2) Conversion of customer requirements

A system for converting the customer's requirements into in-house requirements and determining if certification and QML coverage exists for the customer's product. Items 3-14 listed below are used as the basis for the conversion of customer requirements systems for QML product.

(3) Device specification requirements (SMD)

(4) Controlled design procedures and tools (established geometric, reliability and electrical design rules and performance parameters)

(5) Mask generation procedure within the controlled design procedures of (4)

(6) Wafer fabrication and assembly capabilities baselined

(7) Product build per approved design/mask/fab/assembly/test generic flows

(8) QML listing coverage

(9) SEC/TCV/PM program and procedures

This section should include, as a minimum, description of what makes up the SEC/TCV/PM, what tests are performed, how often, and what roles do these elements play

(10) Incoming inspection/vendor procurement document covering design/mask/fab/assembly

(11) Screening and traveler format and content

(12) Technology Conformance Inspection (TCI) procedures (formerly Quality Conformance Inspection (QCI))

(13) Marking

(14) Rework

(15) Organizational chart (TRB, QA, Production)

(16) Change control program

A system which describes how changes to the QML program will be addressed, qualified and documented. Documentation should address, as a minimum, the following items:

- Major change
- Required testing
- TRB responsibility
- TRB MIL-I-38535 program interface for government

(17) Field failure return and analysis program

(18) Self-audit program and audit results from last audit

A system through which the QML Program is verified as working and acts as a provision for quality enhancement.

(19) TRB reporting (to DESC) checklist/procedure

(20) Quality and Yield improvement program

(21) SPC program

Define manufacturer's goals and plans to impose a SPC program within the manufacturing process to the requirements of JEDEC Publication 19. Include in-line process monitors along with the location within the flow where in-line monitors and SPC measurements are in place.

(22) Test method(s) suitability/outside laboratory

A list of test methods for which the manufacturer is certified.

(23) Major test methods submitted

Specific documents to submit will be decided on a case by base basis. Shown below are examples of documents which may be required. This item need not be part of the QM Plan.

- Burn-in
- Temperature cycle
- Fine/gross leak
- PIND

(24) Calibration

(25) Retention of Qualification

(26) Training

(27) Cleanliness and atmospheric controls

(28) ESD program

(29) Line certification test plan

(30) Line qualification test plan

Define the two qualification devices and tests to be performed

5.2.2 Data Submissions

Summary of the test results that determine the capability of the vendors manufacturing processes in the following areas shall be provided.

Demonstration of:

(1) Design/process capability for modeling, layout, performance and fault coverage verification.

(2) Technology susceptibility to intrinsic reliability failure mechanisms (TCV characterization)

(3) Demonstration of technology fabrication process reliability (SEC testing).

(4) Assembly/Packaging characterization data

5.2.3 Present Status and Plans for the Future (Milestones)

The manufacturer is required to submit information, present status and future plans concerning products to be offered as QML, status of SPC in terms of C_P and C_{PK}, yield/quality of outgoing product, and differences between commercial and military processing and how they are being brought together as one system.

This will give the validation team confidence that the manufacturer has established goals, is committed to the program, and has plans for reducing cost and increasing availability of QML product.

5.2.4 Manufacturer has a Self Audited System that is in Place and Functioning (implemented)

Implementation is accomplished by running test structures, test vehicles and production product through the QML system. By meeting these requirements the manufacturer will know the capability of his program, which can be verified by the existing data on the production floor (e.g., PM, SPC, Test, and SEC data). The manufacturer will also have determined through his self audit system that his QML program meets the requirements of the QM Plan as well as MIL-I-38535.

Through the audit requirements and the manufacturer having an implemented, self audited system, the validation team can then perform a confident sampling of the manufacturer's QML program during a validation review.

5.3 Validation Review

Upon successful completion of the preaudit requirements a five day (usually Monday to Friday) validation review schedule is developed. Coordination of this schedule to ensure availability of proper personnel and necessary area access is accomplished prior to the validation review. The first day is dedicated to vendor presentations in-depth review of the vendors quality program, SPC program and technology baseline. The validation team spends the next three days performing in-

depth reviews of specific manufacturing operations. Typically this consists of four individual teams. Late Friday afternoon an exit critique is presented by the validation team, including all Deficiency Area Reports (DAR). The manufacturer is required to respond to the government with a complete corrective action package. Typical validation review questions are included in Appendix A.

6.0 CHANGES TO MIL-STD-883

Revision or addition of test methods and procedures to MIL-STD-883 is a continuing task that assures adequate testing/control of the evolving microcircuit technology. Those changes or additions that will assist the expansion of the QML are indicated in the following subparagraphs.

6.1 Internal Visual (Monolithic) Test Method 2010.10

The usage of GaAs chip devices in hybrid microcircuits, i.e., T/R modules and discretely packaged GaAs devices required the addition of visual reject criteria to Test Method 2010. These criteria are interspersed throughout and limited to GaAs device inspections. Additionally, selection of the applicable high power magnification for individual features of GaAs devices is in accordance with Table 15.

Table 15: GaAs Device High Magnification Requirements

Feature Dimensions	Magnification Range
>5 microns	75 - 150X
1-5 microns	150 - 400 X
<1 micron	400 - 1000X

Depth of field problems at the higher level magnifications that would occur due to chip packaging are minimized by performance of visual inspection at the die level.

6.2 Fault Coverage Measurement for Digital Microcircuits

The requirement to perform fault coverage measurement analysis in MIL-I-38535, Requirement 64 of MIL-STD-454 and the bipolar and CMOS gate array slash sheets, (i.e., MIL-M-38510 600 series), necessitated the preparation of Test Method 5012. This method which assists in the measurement and reporting of fault coverage for digital microcircuits is needed because of the large discrepancies that arise from different fault simulators and logic modeling styles. The test procedure specifies the methods by which fault coverage is reported for a test program applied to a microcircuit under test and describes the following requirements governing the development of the device logic model:

- Assumed fault model
- Fault universe
- Fault classing
- Fault simulation
- Fault coverage reporting

The use of this procedure will provide a consistent means of reporting fault coverage regardless of the specific logic and fault simulator used.[7]

6.3 Wafer Acceptance

Wafer Acceptance Wafer Fabrication Control and Wafer Acceptance Procedures for Front-Side Processed GaAs Wafers, Test Method 5013 was generated to assist in assuring the quality and reliability of GaAs devices through wafer control procedures. It is especially useful in the procurement of GaAs chip devices for hybrid microcircuits tested to Test Method 5008.

Wafer fabrication line requires a characterized and baselined process, statistical process control, incoming material evaluation and an electrostatic discharge sensitivity control program. Wafer lot acceptance is based on wafer visual inspection and electrical testing of process monitors (PM's). A suggested list of test structures, their locations and evaluation procedure are included in the test methods.

7.0 MICROCIRCUIT APPLICATION GUIDEBOOK

The Defense Science Board (DSB) 1986 Summer Study Group "Use of Commercial Components in Military Equipment" reports dated January 87 and June 89 recommended the generation of a selection guidebook. The Army Laboratory Command was tasked to lead the effort and prepare the document. The guidebook is to be used in conjunction with the QML and QPL for the selection of devices for military systems, based on cost-effective performance and reliability in a given application.

A major purpose of the guidebook is to marry component selection with applications requirements to allow tailoring of microcircuit selection requirements to achieve performance and life cycle cost benefits. Its use is recommended for System Program Offices (SPO), equipment manufacturers and microelectronic device vendors. The proposed outline for the document includes:

1 - Introduction
2 - Quality Systems
3 - DoD Procurement Procedures

[7] Winter '91, RAC Quarterly, Volume 1, Issue 1

4 - Technology Information
5 - Selection Guidance
6 - Communication Procedures
7 - System Guidance

Chapters Two and Three contain background information for all military departments and contractors involved in device selection. Knowledge of how to use this information is essential for establishing an effective communication process and to insure proper device selection. Chapter Two discusses the various quality systems under which military microcircuits are purchased. It also describes the various attributes of each system and their selection criteria. Chapter Three describes DoD procurement practices and the basic traditional flow down of selection requirements.

Chapter Four is intended to raise an awareness, on the part of the system integrators and device manufacturers, concerning potential problems associated with device "handling" and "process abuses." This chapter should be used as the basis for a two way communication process, to be focused on preventing the misapplication of military integrated circuits.

The shifting of emphasis, from a selection process based on uniform generic requirements to an application specific requirement system, necessitates accurate identification and communication of all device level requirements. A selection matrix and criteria are provided in Chapter Five for the Program Manager/SPO, system integrator and components manufacturer. The matrix identifies several quality system candidates, according to the end-use environments for which devices may be intended. The selection criteria is used to determine the device level requirements of the application as related to the system design, assembly method(s), end use and maintenance requirements. The matrix is intended only for use in conjunction with the selection criteria and the various application requirements employed in determining acceptable candidate systems.

System integrators should use chapter five as a guide for determining device level requirements. Component manufacturers should make available device capability/limitation data for each selection criteria. The SPO/PM should consider the cost, performance, and reliability tradeoffs associated with using devices from the different systems.

Chapter Six outlines the various requirements useful in achieving effective communication within and among the program office, the system integrator and the device fabricators.

Chapter Seven provides a general listing and brief explanation of some potential reliability problems that should be addressed early in the development of all electronic hardware. The SPO/PM and system integrator should discuss these issues to insure they are adequately addressed in the initial system design and device

selection stage. This information should serve as a valuable reference tool for the system integrator.

A draft of this document has just entered the review/coordination cycle, with release expected in summer of 91.

8.0 QML ADDITIONS/EXTENSIONS

The QML document, MIL-I-38535, is responding to both industry and government needs as additional areas are identified. The following paragraphs summarize ongoing changes while pointing out additional technologies that should be covered by the QML umbrella.

8.1 Third Party Certification

The building block approach detailed in MIL-I-38535 corresponds to how OEM's acquire ASIC's. Three distinct, well defined areas of ASIC procurement philosophy are design, fabrication and packaging/assembly which can occur at different locations/companies. The 10 January 91 draft of MIL-I-38535 has included criteria for third party design. Basically, this requires a QML vendor to certify a design house to the applicable criteria and verify their capability. The government would perform spot checks to assure integrity of the system. Upon completion of this activity the design house capability would become part of the approved QML technology flow. The certification requirements for assembly houses using the third party philosophy will probably take place in the fall of 1991.

8.2 GaAs

GaAs requirements which were developed through the MIMIC program and JEDEC JC 13.6 committee activity have been included in the 10 January 1991 draft of MIL-I-38535. Primarily additions are necessary to add GaAs QML requirement as well as chip requirements for their use in modules. Unique GaAs criteria which are being defined include the standard evaluation circuit, die requirements, parametric test structures for process monitors and visual inspection and wafer acceptance procedures. Die requirements will include sample testing of each chip lot, suitable packaging for qualification and TRB focus. RF/DC wafer probe will be added to SEC testing. Typical parametric monitor measurements are sheet resistance, MIM capacitor, Fat FET, isolation, ohmic contacts and GaAs FET parameters. Structures for ohmic contact degradation, backgating/sidegating and sinking gate will be added to the TCV. Further definition of GaAs QML requirements for testability, limitation to only digital portion at present time, traceability to the wafer level and chip QML features such as die carrier marking, die manufacturer part number and final product tracking are being worked on. The proposed changes are summarized in Table 16 GaAs potential changes. The GaAs QML schedule is shown in Figure 12. GaAs QML beta site participants are listed in Figure 13.

Table 16: GaAs Potential Changes to MIL-I-38535

PARA NO.	POTENTIAL CHANGE
1.1	Include unpackaged devices
3.4.2.2	Add, GaAs specifics
3.4.3.1	Add, unpackaged device criteria
3.4.4.1a	Change to design library
3.4.4.2k	Add, glassivation
3.4.4.2	Add, following processes • Gate Formation • Ohmic Contact Formation • Backside • Starting Materials Qualification
3.4.4.3b	Add, ribbon interconnect
3.5.1.2	Add, fabrication to and from materials
3.5.1.3.1a	Add, transistor modeling
3.5.1.3.1b	Add, backgating/sidegating to reliability rules
3.5.1.3.1d	Identify analog fault coverage applicability
3.5.1.3.2a4	Add, or concentration after diffusion
3.5.1.3.2a7	Replace etch with resultant
3.5.1.3.2a9	Add, and/or implant anneal after diffusion
3.5.1.3.2a19	Add, and VIA hole process
3.5.1.3.2a	Add, following new process • gate formation • air bridge
3.5.1.3.2b	Add, gate sinking, ohmic contact degradation and backgating after (TDDB)
3.5.1.3.2c	Allow glassivation, if required for the device and technology being characterized. Also allow use of suitable TCV packaging. Add sinking gate, ohmic contact degradation and backgating test structure requirements to TCV
3.5.1.3.2d	Identify when a SEC is required, SEC packaging and SEC complexity requirements
3.5.1.3.2e	Add, RHA test structure requirements, GaAs PM parameters and fast test structures, i.e., contact resistance, gate diffusion
3.5.1.3.3	Include TM 5013 for use
3.5.1.3.5	Add, ribbon bond
3.5.1.4.3	Add, wafer boule evaluation, ribbon bonding
3.5.2.1	Clarify microcircuit design qualification
3.5.2.1.2	Allow usage of suitable packaging
3.7	Add, unpackaged die marking requirements
3.7.8	Add, unpackaged die container marking requirements
4.2.2	Require traceability to wafer level
4.2.6.2	Add, passivation
4.3.4	Identify alternate visual does not apply
Table VIII	Clarify unpackaged device testing
Table IX	Clarify unpackaged device testing

MIMIC QML Program Schedule

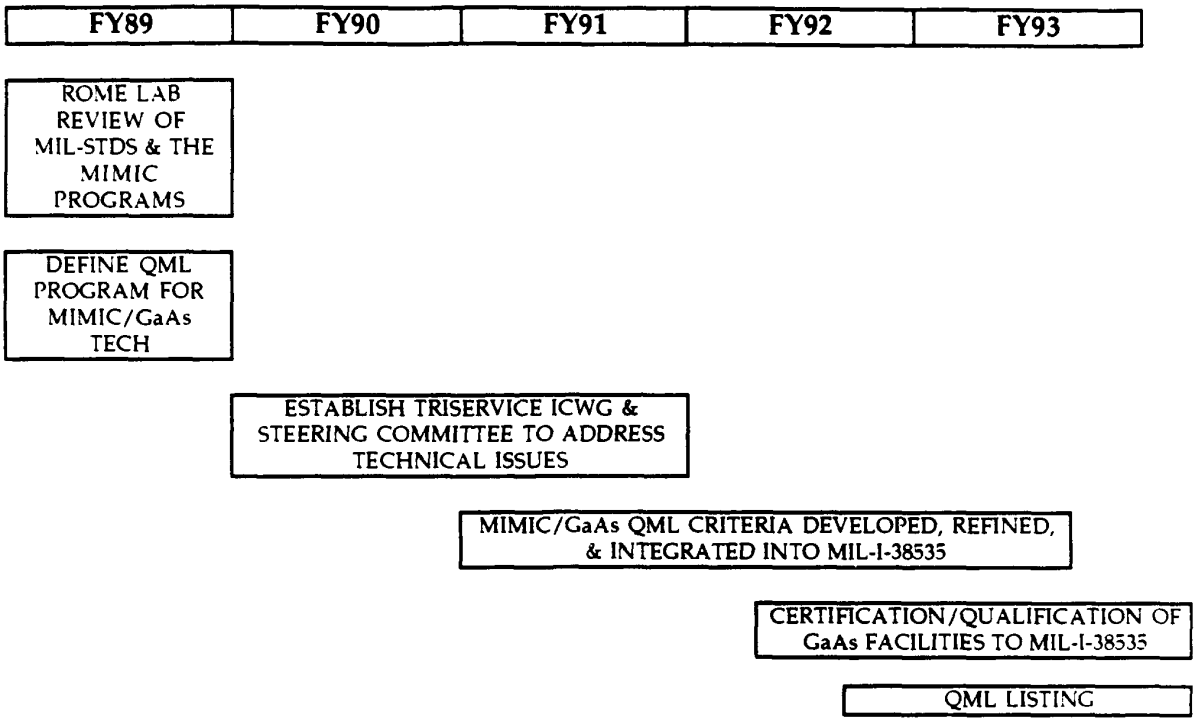


Figure 12: MIMIC QML Program Schedule

Company	Location	Technology
Alpha Industries, Inc.	Woburn, MA	0.25 Micron MESFET/MODFET Epitaxial (MBE)
AT&T	Reading, PA	0.5 Micron MESFET Epitaxial (MBE)/Ion-Implant
Comsat Laboratories	Clarksburg, PA	0.5 Micron MESFET Epitaxial (MBE or VPE)
Hughes Aircraft Company Microwave Products Div.	Torrance, CA	0.5 Micron MESFET Ion-Implant
ITT Gallium Arsenide Technology Center	Roanoke, VA	0.5 Micron MSAG Ion-Implant
Lockheed Sanders, Inc.	Nashua, NH	0.5 Micron MESFET Ion-Implant
Texas Instruments	Dallas, TX	0.5 Micron MESFET Ion-Implant
TriQuint Semiconductor	Beaverton, OR	0.5 Micron MESFET Ion-Implant
TRW	Redondo Beach, CA	HBT, HEMT Epitaxial (MBE)

Figure 13: GaAs QML Beta Site Participants

8.3 Hybrid Microcircuit QML Update

The government and the hybrid industry are working on updating MIL-H-38534 through the JEDEC JC13.5 and 13.6 committees to integrate innovations from the monolithic QML program. Additions include the incorporation of Test Method 5008 and MIL-STD-1772 Qualification requirements. Additionally MIL-STD-1772 process qualification will be combined with QCI testing. Option 4 will be added as an appendix to MIL-H-38534 to include the need for a TRB, endorsement of a SPC program, establishment of QML validation requirements (i.e., Design → Final Product), and modification of element evaluation to include GaAs QML chips. The Hybrid/Module QML program schedule is described in Figure 14.

Hybrid/Module QML Program Schedule

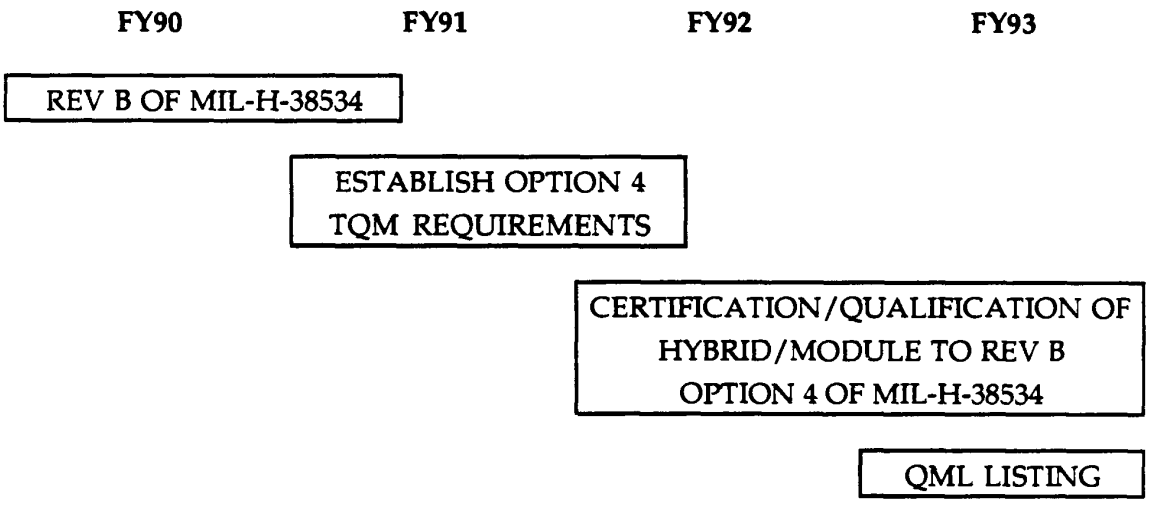


Figure 14: Hybrid/Module QML Program Schedule

8.4 Plastic Encapsulated Microcircuits

Plastic device criteria is another feature of the 10 January 1991 draft of MIL-I-38535. It must be pointed out that this inclusion doesn't change military usage requirements for plastic devices but identifies the necessary criteria to allow a plastic device vendor to be included in the QML. MIL-STD-454, Requirement 64, Microelectronic Devices limits the use of plastic devices to use in ground fixed (GF) or ground benign (GB) environments when approved by the procuring activity. However, this proposed change, the Wright Laboratory "Reliability Without Hermeticity

(RWOH)," program and the improving plastic device data base indicates a relook at the usage of plastic devices. A new RAC publication[8] available later this summer will discuss the past, the current status and future trends for packaging.

8.5 On Shore vs. Off Shore Manufacturing

Under existing QML policy all procedures and operations must be located in the United States. The Defense Microcircuit Planning Group which determines DoD policy for microcircuits is presently evaluating this policy. This group is made up of representatives from:

- Rome Laboratory
- Navy
- Army
- Space Division (AF)
- NASA
- NSA

A possible change to the policy would allow packaging/assembly and maybe design to be performed offshore while wafer fabrication would remain onshore.

8.6 Multichip Modules (MCM's)

The next logical technology area of extension for the QML are MCM's. The two existing QML documents complement one another when applied to the MCM technology area. In order to achieve manufacturable, cost effective MCM's maximized chip yield is necessary with emphasis on wafer level testing. The procedures of MIL-I-38535 can be tailored to obtain the highest quality and most reliable chip device utilizing the unpackaged chip qualification procedure being developed for GaAs (See Section 8.2).

A necessary addition would be requirements for establishing and certifying the interconnect design and fabrication process. The design section of MIL-I-38535 could be used as a strawman to assure integrity of the interconnect (i.e., design rules, simulation, performance, testability). The assembly/packaging requirements of both QML documents can be tailored to assess MCM fabrication including special test methods and conditions as required for MCM's depending on packaging (i.e., plastic, hermetic), technology (i.e., TAB, EP TAB, flip chip, HDI (High Density Interconnect)). Various DoD funded programs are investigating MCM's as a technology for reliable use in DoD/commercial systems. Rome Laboratory, the logical candidate to assure MCM quality and reliability is presently assessing the extension of the QML process for MCM's.

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8 Plastic and Hermetic Packaging a Critical Review of the State of the Art

8.7 Printed Wiring Assemblies (PWA)

Component quality and reliability and their attachment processes have been individually assessed and evaluated in great detail. Microcircuits, which have had the greatest scrutiny, have a multitude of specifications and standards requiring certification and qualification. Much work has gone on in evaluating attachment processes and printed wiring boards (PWBs). In fact, a new proposed High Reliability, General Specification for Printed Wiring/Printed Circuit Board, MIL-P-RRRR is being prepared by DESC. However, their is no process in place to assure manufacturability of the marriage of components at the next level of interconnect. The systems in place today to assure integrity of discrete components (i.e., active, passive, PWB) could easily complement a procedure to verify manufacturability of Printed Wiring Assemblies (PWA's). Printed wiring boards have traditionally used test coupons to evaluate PWB processing. Expanded coupon testing/evaluation could establish QML type confidence in OEM design/fabrication processes that could be verified by surrogate devices. Areas of concern would be board/interconnect design (i.e., design rules, materials compatibility, performance, electrical, mechanical and thermal simulation and process control). Verification of technology could be achieved by populating a PWB with appropriate components and attachment procedures thereby developing a representative surrogate device for test. Finally development of a philosophy for printed wiring assembly electrical testing and associated conditions is needed. Any additional QML extension to other technologies should:

- Utilize Malcolm Baldrige Criteria (See Appendix B)
- Use Microcircuit QML as a Guideline
- Instill Corporate Discipline and Commitment

RAC is very interested in pursuing this objective and would welcome any comments/discussion.

9.0 NATIONAL QML SPECIFICATION

Work has started to prepare a QML specification that will be acceptable for both military and commercial microcircuit applications. The JEDEC JC-14.5 committee on National Electronic Quality Process Standard (NEQPS) is preparing the draft document.

This committee's activities include the development and maintenance of a Total Quality Manufacturing Oriented NEQPS for the certification and qualification of solid state products. The committee will use relevant information and expertise from available government and industry sources and maintain a direct liaison with the NECQ to promote standards commonality across all electronic components.

This committee will rely heavily on standards and procedures developed by other JEDEC committees and international committees whose tasks are related to the NEQPS. The committee is made up of both manufacturers and users.

The JC 14.5 objective is to develop a document for process qualification for use by U.S. Industry that the NECQ could implement and use as a national standard. The starting point for NEQPS is MIL-I-38535 and the CECC/WG9 # 105 document developed by France. The following additional documents were reviewed:

- NECQ Certification Standard by QRE
- PAQ 92 Quality Management according to TQM Principles and Qualification Procedures
- TIEGEC/WG2 Capability Approval of ASICS
- ISO 900 Series (ASQC 90 series)
- ISO 8402 (R&QA Terms for relating to ISO 9000)
- Partnering for Quality (SEMATECH)

9.1 Status

A new document, rather than a change to existing documentation such as MIL-I-38535, general enough for use in acquisition of other components will be prepared. Drafts of four major sections, quality management, design, manufacturing and technology assurance have been drafted and reviewed. A JC 14.5 letter ballot has been prepared and sent out for comment. The following basic principles were used in preparing the draft NEQPS letter ballot:

1. The document must provide a methodology for certifying and qualifying a complete manufacturing flow, Conception to Field Use.

2. It must not be time or technology dependent (i.e., can't update as technology advances).

3. It will avoid telling the manufacturer how to do his job.

4. It will specifically state the areas of evaluation, ask how the requirements were set by the manufacturer, and validate the methodology used to meet those requirements.

5. It will be a short document (20 pages) that consolidates the outline into short definitive paragraphs? (Details can be put into Validation Check Lists, which can be easily changed).

6. The document's basic principles are:
   - Controlled Process
   - Quality Management Approach
   - Continuous Improvement
   - Self Audit Program with Quality Enhancement

- Technical Management Structure (previously called Technical Review Board)
- Verified Reliability

7. It will eliminate duplication of areas

8. It will develop requirements from a validation approach to determine the viability of the process after certification and qualification (i.e., a complete functional self audit program).

9. It will propose a method for maintaining technical and management contact to strengthen the partnership after certification and qualification.

10. It will encourage the use of commonly accepted test standards where applicable.

11. It will develop a document that is compatible with International Standards Organizations (i.e., ISO 9000 & ASQC 90).

Figure 15 illustrates the time frame of the national QML development starting with MIL-I-38535. Note that the Europeans are also actively involved in preparing their QML standard. The goal is to have an international electronic component standard. Table 17 identifies the documents the Europeans are preparing.

Table 17: European QML Status

Documents/Draft for New Qualification Cor

CECC 00107111 & 90000 Issue 4	Annex Capability Approval (Procedure)
CECC/WG9	Specifications for Generic Qualification for ASIC's & IC's Part I TQM Principals Part II EQML for IC's and ASIC's
PAQ 92	Quality Management According to TQM Principles and Qualification Procedures
TIEGEC/WG2	Capability Approval of ASIC's

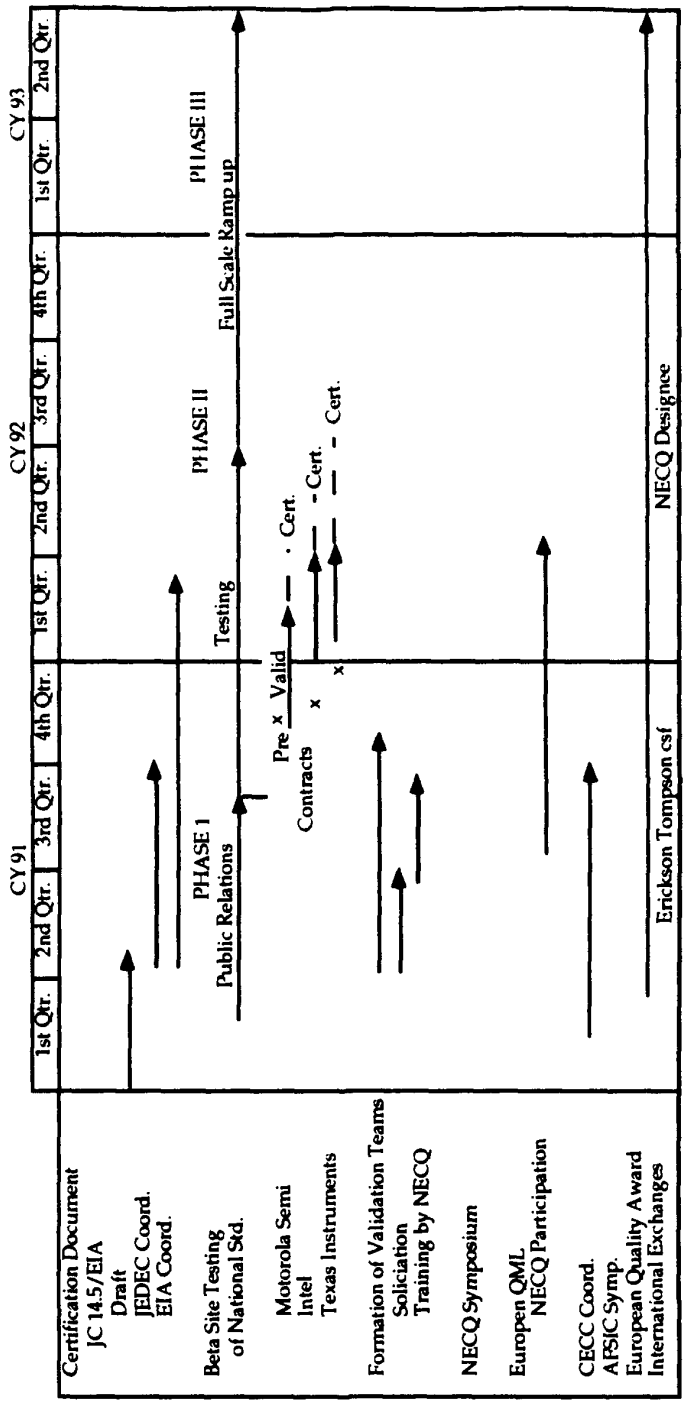


Figure 15: National QML Implementation Road Map

10.0 SUMMARY

This document has presented the latest QML approach by the DoD, to assure highest quality and most reliable microcircuits for electronic systems. However, the philosophy is not new or radical.

In conclusion, let us cite from a keynote address at the DoD symposium on Guided Missile Reliability in November 1955: "The desired reliability cannot be attained solely by specification . . . The process of selecting the best components from a rather heterogeneous population is wasteful . . . We still need better components, and we must learn how to make them with greater uniformity. We must know more of the characteristics and the variability of these components. We must know the environments in which they must live. Tests to failure must be conducted to determine modes of failure. Designs must be based on adequate safety factors, a specified number of standard deviations between average strength and maximum stress. Reliability must be designed in."

These words, haven't lost any of their meaning. In fact it seems that they are more timely than ever, particularly in the field of microcircuits. The new approaches described herein are leading the culture change to improve microelectronic device quality and reliability. In addition, the combination of the manufacture of commercial and military products in the same facility, and on the same line are encouraged resulting in globally competitive products.

APPENDIX A:

TYPICAL VALIDATION REVIEW QUESTIONS

TRB/Management/Business

1. Quality Program

   - Malcolm Baldrige Award questions
   - How do you respond to customer requests and problems?
   - How do you report and what are your quality levels?
   - Do you have a Field Failure Report Program?
     - How does it work?
     - Do you routinely analyze failures or defects found during processing? Explain.

2. Self-Audit

   - Briefly explain who did them, the criteria and the results.
   - Demonstrate that the QML system is in place and working.

3. Marketing

   - How do you intend to market/advertise/promote QML product?
   - What devices will be QML'd?
   - When will Device Procurement Specifications be available for DESC?
   - Discuss pricing?

4. Business

   - Future QML product technologies
   - Future plans for fabrication and design
   - Plans/problems with merging commercial and military

5. SPC program - overall corporate

6. Conversion of customer requirements

   - Specification
   - How do you guarantee that a QML product will see all the certified processes, tests, screens, etc.? This will be validated indepth by the validation team
   - Training
     - SPC
     - Operators

7. Product/Technology

- ESD programs
  - Goals
  - Where are you?
- Reliability
  - Discuss program
  - Examples
- Electromigration - What are current densities?
- Failure Mechanisms
  - How are they monitored?
  - Controlled?
- Failure Analysis Program
- Corrective Action Program

8. Change Control

- Explain your system.
- How are the DoD's concerns addressed?
- How are customers notified of changes? DESC?
- Would you be opposed to a requirement to notify prior to implementation changes to screens or TCI tests? Explain.
- Are all areas of change listed in MIL-I-38535 addressed?

9. QML Qualification

- Detail plans including schedule
- Discuss report

Design Discussion Topics

1. Design Management

- TQM - How does this fit into design?

  First pass success:

  - Explain what this means to the company.
  - What is your success rate? Your design complexity?
- What improvements are on the horizon for design?
- What will happen when a new process is available from the fabrication?

2. Design methodology

- Outline the process of designing a device.

Design reviews:

- What happens?
- Who attends?
- What tradeoffs are made?
- Who controls the meeting?
- What is documented?

3. Customer Interface

- Who are your customers?
- How are their requirements addressed?
- Specification

4. Modeling

- Verification
  - Process variation, temperature, radiation
- Who controls and updates?
- What are the goals?
- Product vs. simulation

5. Design Procedure

- Are any or all of the following levels of design performed, and if so, who does and who approves them?
- Requirements definition?
- Detailed function definition?
- Detailed design (e.g., gate level design)?
- Layout and mask generation?
- What automatic aids are used for refinement from each design level to the next?
- What automatic aids are used for verifying the refinement at each level (e.g., automatic checking of layout vs. schematic)?

6. Design Capture

- Behavioral
- Schematic capture
- Boolean

7. Simulation

- Process variation, temperature, radiation
- Back annotation
- Logic
- Circuit
- Timing
- Critical path
- Fault simulation

8. Physical Layout

- Place and route
- Extraction
  - Net list
  - Parasitics

9. Design Verification

- Geometric rules - General and Verification "Designer Notes"
- Electrical rules - Generation and Verification
- Reliability rules - Generation and Verification i.e., electromigration, IR drop, Hot electron, TDDB, ESD, SEU
- Layout vs. schematic

10. Testing

- What are the differences between testing done for "functionality" and for fault coverage?
- How is fault coverage determined?
- What guidelines govern development of models for fault simulation and use of fault simulators?
- Test vector generation.

11. Training and Instructions

- What training is provided to personnel performing design, specification generation, test generation, testing, etc.?
- Are there written Operating Instructions to provide guidelines?
- How do personnel communicate problems, solutions, procedures, etc.?
- How are tradeoffs (e.g., speed vs. testability features) handled consistently between individuals or departments?
- Are there written plans for improvements?

12. Software Control

- What commercial software tools are used?
- Are modifications to commercial tools permitted?
- Who develops internal software tools?
- How is software controlled, verified and certified for use?
  - Frequency of major/minor revisions?
  - Trouble reports?
  - Regression testing with benchmarks?
  - How are benchmarks updated?
- Are results from software tools periodically checked against actual data or other tools?
- How are tools "integrated", i.e., how do multiple tools access the same data, and are the output data from one tool in the correct format for input to the next tool without manual translation?
- What simulators are used for:
  - Process simulation?
  - Circuit simulation?
  - Gate level simulation?
  - Switch level simulation?
  - Behavioral/functional simulation?
  - Dynamic timing analysis (to include actual delays due to placement and routing)?
- What tools are used for:
  - Automatic test vector generation?
  - Fault simulation?
  - Insertion of Design-For-Testability/Built-In-Test features?
- Who is responsible for:
  - Design?
  - Test vector generation?
  - Test program generation?
- Discuss involvement with JTAG.

13. Interfaces

- How is interfacing done with foundries and/or customer?
  - Data formats?
  - Media (e.g., magtapes, modems, networking)?
- Discuss relationships with fab, assembly and packaging

14. IC Testing

- Who tests the integrated circuits?
  - At wafer level?
  - After packaging?
  - Burn-in?

- Life testing?
- What types of Automatic Test Equipment are used?

15. Design Documentation

- Discuss your involvement with VHDL, TISSS

FAB - Discussion Topics

1. Baseline Flows - Capability

- Design Rules - Describe

2. SPC Policy

- Goals - Cp, Cpk
- Examples of charts
- DOE, etc.

3. SEC, TCV, PM

- Describe them
- How are they utilized? Examples
- PM - Are all parameters listed in MIL-I-38535 addressed?
  - Discuss PM program

4. Wafer Acceptance

- TM2018
- Lot formation
  - Monitoring program
  - Accept/reject criteria
- Metallization coverage

5. Traceability

6. Failure Analysis/Corrective Action

7. Change Control

- Describe policy and procedures
- Are all concerns outlined in MIL-I-38535 addressed? Discuss
- What type changes require requalification?

- What tests are done to verify change?
- Are all customers notified?
- Give examples

8. Mask

   - Inspection routine

9. Inspection

   - Process Controls
   - Visual

Assembly - Discussion Topics

1. Baseline Flow

2. Process Control

   - SPC program
     - How was it established?
     - How does it work?
     - Goals - Cp, Cpk - Where are you?
     - What is your approach? DOE?
     - What is covered? Examples of charts
     - Who does what to what? Operator, Engineering?

   - Other Controls
     - Die attach material - if epoxy use Test Method 5011 of MIL-STD-883
     - Material control

3. Traceability

   - Explain your approach
   - Examples of it working
   - To what level of risk - lot size, time, etc.

4. General

   - Is the SEC used to baseline or quality assembly processes?
   - Are all changes listed in MIL-I-38535, addressed?
   - Are all tests in MIL-I-38535, addressed?
   - Yield Improvement

Package - Discussion Topics

1. Package Qualification Program

   - Are requirements of MIL-I-38535, addressed and completed?
   - Are all packages qualified and characterized?
   - Is electrical characterization data made available to designers?
   - Is a thermal characterization done?
   - Who does these tests - you or package vendor?
   - How are packages procured?
   - Is there an incoming inspection?
   - Do you have a modeling program?

2. Product

   - What tests are done on packages with actual product in?
   - What package styles do you presently support?
     - Future plans

3. Package Characterization

   - Does the proposed testing for qualification of a group of packages within a style encompass variations in design (e.g., I/O count, lead spacing, lead-to-lid seal surface distance, die cavity size, etc.), and materials (e.g., Kovar or Alloy 52 leads, copper or Kovar case, gold or nickel plating, etc.) within a package style?
   - Does this testing incorporate worst-case design and/or material conditions?

4. Incoming Inspection

   - Do the package quality control procedures and incoming package acceptance procedures contain methods or tests to insure that packages accepted at incoming will: (a) not leak, (b) be solderable, (c) not outgas excessive harmful contaminants, and (d) survive corrosive environments after being fully assembled and tested?
   - Do the package quality control procedures and incoming package acceptance procedures account for lot-to-lot hermeticity and corrosion resistance variations due to vendor glass sealing and plating process variations?
   - What procedures are proposed to insure that the die attach materials accepted at incoming will: (a) bond properly, (b) not cause excessive outgassing of harmful contaminants during assembly, testing or field use,

and (c) be compatible with component and substrate design during anticipated assembly and field use?

Test - Discussion Topics

1. Equipment

   - Briefly describe capability
   - Do you go outside for some tests?
     - Which ones?
     - How are results reported?
     - DESC certified?

2. Policy

   - Describe which tests are done and to what degree?
     - Electrical
     - Screens
     - TCI
   - Describe Burn-in program
     - Examples/results
   - Traceability
     - Lot identification
   - Future plans
     - Are any tests under consideration for change? Discuss

3. Electrical Test

   - Discuss fault coverage, testability, self-test
   - Vector generation
     - Describe procedure
   - Specification

4. ESD - How is it verified?

5. General

   - How do internal screens on product relate to Table VIII of MIL-I-38535 screens?
   - Discuss with examples

Capability Demonstrations

1. Design

   - Model Verification
   - Layout Verification
   - Performance Verification
   - Testability/Fault Verification

2. Wafer Fabrication

   - TCV Program
   - SEC Program
   - Parametric Monitor
   - Wafer Acceptance Program

3. Assembly/Packaging

4. Screens

   - Burn-in
   - Temperature Cycle
   - Fine/Gross Leak
   - PIND

5. TCI Plans

APPENDIX B:

MALCOLM BALDRIGE CRITERIA

1991 EXAMINATION CATEGORIES AND ITEMS

Malcolm Baldrige National Quality Award



1991 Examination Categories/Items		Maximum Points
1.0	**Leadership**	**100**
1.1	Senior Executive Leadership	40
1.2	Quality Values	15
1.3	Management for Quality	25
1.4	Public Responsibility	20
2.0	**Information and Analysis**	**70**
2.1	Scope and Management of Quality Data and Information	20
2.2	Competitive Comparisons and Benchmarks	30
2.3	Analysis of Quality Data and Information	20
3.0	**Strategic Quality Planning**	**60**
3.1	Strategic Quality Planning Process	35
3.2	Quality Goals and Plans	25
4.0	**Human Resource Utilization**	**150**
4.1	Human Resource Management	20
4.2	Employee Involvement	40
4.3	Quality Education and Training	40
4.4	Employee Recognition and Performance Measurement	25
4.5	Employee Well-Being and Morale	25
5.0	**Quality Assurance of Products and Services**	**140**
5.1	Design and Introduction of Quality Products and Services	35
5.2	Process Quality Control	20
5.3	Continuous Improvement of Processes	20
5.4	Quality Assessment	15
5.5	Documentation	10
5.6	Business Process and Support Service Quality	20
5.7	Supplier Quality	20
6.0	**Quality Results**	**180**
6.1	Product and Service Quality Results	90
6.2	Business Process, Operational, and Support Service Quality Results	50
6.3	Supplier Quality Results	40
7.0	**Customer Satisfaction**	**300**
7.1	Determining Customer Requirements and Expectations	30
7.2	Customer Relationship Management	50
7.3	Customer Service Standards	20
7.4	Commitment to Customers	15
7.5	Complaint Resolution for Quality Improvement	25
7.6	Determining Customer Satisfaction	20
7.7	Customer Satisfaction Results	70
7.8	Customer Satisfaction Comparison	70
	TOTAL POINTS	**1000**

1.0 LEADERSHIP (100 POINTS)

The *Leadership* category examines how senior executives create and sustain clear and visible quality values along with a management system to guide all activities of the company toward quality excellence. Also examined are the senior executives' and the company's quality leadership in the external community and how the company integrates its public responsibilities with its quality values and practices.

1.1 Senior Executive Leadership *(40 pts.)*
Describe the senior executives' leadership, personal involvement, and visibility in developing and maintaining an environment for quality excellence.

AREAS TO ADDRESS

a. senior executives' leadership, personal involvement, and visibility in quality-related activities of the company: (1) goal setting; (2) planning; (3) reviewing company quality performance; (4) communicating with employees; and (5) recognizing employee contributions. Other activities may include participating in teams, learning about the quality of domestic and international competitors, and meeting with customers and suppliers.
b. senior executives' approach to building quality values into the leadership process of the company.
c. senior executives' leadership and communication of quality excellence to groups outside the company. Groups may include national, state, community, trade, business, professional, education, health care, standards, and government organizations.

Notes:
(1) The term "senior executives" refers to the highest-ranking official of the organization applying for the Award and those reporting directly to that official.
(2) The type and extent of the activities of senior executives within and outside the company could depend upon company size, resources, and other business factors.

1.2 Quality Values *(15 pts.)*
Describe the company's quality values, how they are projected in a consistent manner, and how adoption of the values throughout the company is determined and reinforced.

AREAS TO ADDRESS

a. brief summary of the content of policy, mission, or guidelines that demonstrate the company's quality values.
b. company's communications activities to project the quality values throughout the company. Briefly describe what is communicated and the means and frequency of communications.
c. how the company determines and evaluates how well the quality values have been adopted throughout the company, such as through surveys, interviews, or other means, and how employee adoption is reinforced.

1.3 Management for Quality *(25 pts.)*
Describe how the quality values are integrated into day-to-day leadership, management, and supervision of all company units.

AREAS TO ADDRESS

a. key approaches for involving and encouraging leadership in, all levels of management and supervision in quality; principal roles and responsibilities at each level.
b. key approaches for promoting cooperation among managers and supervisors across different levels and different functions of the company.
c. types, frequency and content of reviews of company and of unit quality performance; types of actions taken to assist units not performing according to plans or goals.
d. key indicators the company uses to evaluate the effectiveness of its approaches to integrating quality values into day-to-day management and how the evaluation is used to improve its approaches.

Note: *Key indicators refer to principal measures of some characteristics of quality or effectiveness.*

1.4 Public Responsibility *(20 pts.)*
Describe how the company extends its quality leadership to the external community and includes its responsibilities to the public for health, safety, environmental protection and ethical business practice in its quality policies and improvement activities.

AREAS TO ADDRESS

a. how the company promotes quality awareness and sharing with external groups. Groups may include national, state, community, trade, business, professional, education, health care, standards and government organizations.
b. how the company encourages employee leadership and involvement in quality activities of organizations mentioned above.
c. how the company includes its public responsibilities such as business ethics, public health and safety, environmental protection and waste management into its quality policies and practices. For each area relevant and important to the company's business, briefly summarize: (1) principal quality improvement goals and how they are set; (2) principal improvement methods; (3) principal indicator used to monitor quality; and (4) how and how often progress is reviewed.

Note:
(1) Health and safety of employees are not covered in this item. These are addressed in Item 4.5.

2.0 INFORMATION AND ANALYSIS (70 pts.)

The ***Information and Analysis*** category examines the scope, validity, use, and management of data and information that underlie the company's overall quality management system. Also examined is the adequacy of the data, information and analysis to support a responsive, prevention-based approach to quality and customer satisfaction built upon "management by fact."

2.1 Scope and Management of Quality Data and Information *(20 pts.)* Describe the company's base of data and information used for planning, day-to-day management, and evaluation of quality, and how data and information reliability, timeliness, and access are assured.

AREAS TO ADDRESS

a. (1) criteria for selecting data to be included in the quality-related data and information base; and (2) scope and types of data; customer-related; internal operations are processes; employee-related; safety, health, and regulatory; quality performance; supplier quality; and other.
b. processes and techniques the company uses to ensure reliability, consistency, standardization, review, timely update, and rapid access throughout the company. If applicable, describe approach to ensuring software quality.
c. how the company evaluates and improves the scope and quality of its data and information and how it shortens the cycle from data gathering to access.

Note:
(1) The purpose of this item is to permit the applicant to demonstrate the breadth and depth of the data assembled as part of its total quality management system. Applicants should give brief descriptions of the types of data under major headings such as "employees" and subheadings such as "education and training," "teams," and "recognition." Under each subheading, give a brief description of the data and information. Actual data should not be reported in this item. Such data are requested in other Examination Items.
(2) Information on the scope and management of competitive and benchmark data is requested in Item 2.2.

2.2 Competitive Comparisons and Benchmarks *(30 pts)*
Describe the company's approach to selecting quality-related competitive comparisons and world-class benchmarks to support quality planning, evaluation, and improvement.

AREAS TO ADDRESS

a. criteria and rationale the company uses for seeking competitive comparisons and benchmarks: (1) relationship to company goals and priorities for improvement of product and service quality and/or company operations; (2) with whom to compare - within and outside the company's industry.
b. current scope of competitive and benchmark data: (1) product and service quality; (2) customer satisfaction and other customer data; (3) supplier performance; (4) employee data; (5) internal operations, business processes, and support services; and (6) other. For each type: (a) list sources of comparisons and benchmarks, including company and independent testing or evaluation; and (b) how each type of data is used.
c. how the company evaluates and improves the scope, sources, and uses of competitive and benchmark data.

2.3 Analysis of Quality Data and Information *(20 pts.)*
Describe how data and information are analyzed to support the company's overall quality objectives

AREAS OF ADDRESS

a. how data described in 2.1 and 2.2, separately and in combination, are analyzed to support: (1) company planning and priorities; (2) company-level review of quality performance; (3) improvement of internal operations, business processes, and support services; (4) determination of product and service features and levels of quality performance that best predict improvement in customer satisfaction; and (5) quality improvement projections based upon potential use of alternative strategies or technologies.
b. how the company evaluates and improves its analytical capabilities and shortens the cycle of analysis and access to analytical results.

Note: *This item focuses primarily on analysis for company-level evaluation and decision making. Some other items request information based on analysis of specific sets of data for special purposes such as human resource practices and complaint management.*

3.0 STRATEGIC QUALITY PLANNING (60 pts.)

The *Strategic Quality Planning* category examines the company's planning process for achieving or retaining quality leadership and how the company integrates quality improvement planning into overall business planning. Also examined are the company's short-term and longer-term plans to achieve and/or sustain a quality leadership position.

3.1 Strategic Quality Planning Process *(35 pts.)*
Describe the company's strategic quality planning process for short-term (1-2 years) and longer-term (3 years or more) quality leadership and customer satisfaction

AREAS TO ADDRESS

a. how goals for quality leadership are set using: (1) current and future quality requirements for leadership in the company's target markets; and (2) company's current quality levels and trends versus competitors' in these markets.
b. principal types of data, information, and analysis used in developing plans and evaluating feasibility based upon goals: (1) customer requirements; (2) process capabilities; (3) competitive and benchmark data; and (4) supplier capabilities: outline how these data are used in developing plans.
c. how strategic plans and goals are implemented and reviewed: (1) how specific plans, goals and performance indicators are deployed to all work units and suppliers; and (2) how resources are committed for key requirements such as capital expenditures and training; and (3) how performance relative to plans and goals is reviewed and acted upon.
d. how the goal-setting and strategic planning processes are evaluated and improved.

Notes:
(1) *Strategic quality plans address in detail how the company will pursue market leadership through providing superior quality products and services and through improving the effectiveness of all operations of the company.*
(2) *Item 3.1 focuses on the processes of goal setting and strategic planning. Item 3.2 focuses on actual goals and plans.*

3.2 Quality Goals and Plans *(25 pts.)*
Summarize the company's goals and strategies. Outline principal quality plans for the short term (1-2 years) and longer term (3 years or more).

AREAS TO ADDRESS

a. major quality goals and principal strategies for achieving these goals
b. principal short-term plans: (1) summary of key requirements and performance indicators deployed to work units and suppliers; and (2) resources committed to accomplish the key requirements.
c. principal longer-term plans: brief summary of major requirements, and how they will be met.
d. two-to five-year projection of significant changes in the company's most important quality levels. Describe how these levels may be expected to compare with those of key competitors over this time period.

Note: *The company's most important quality levels are those for the key product and service quality features. Projections are estimates of future quality levels based upon implementation of the plans described in Item 3.2.*

4.0 HUMAN RESOURCE UTILIZATION (150 pts.)

The ***Human Resource Utilization*** category examines the effectiveness of the company's efforts to develop and realize the full potential of the work force, including management, and to maintain an environment conductive to full participation, quality leadership, and personal and organization growth.

4.1 Human Resource Management
(20 pts.)
Describe how the company's overall human resource management effort supports its quality objectives

AREAS TO ADDRESS

a. how human resource plans are derived from the quality goals, strategies, and plans outlined in 3.2: (1) short term (1-2 years); and (2) longer term (3 years or more). Address major specific requirements such as training, development, hiring, involvement, empowerment, and recognition.
b. key quality goals and improvement methods for human resource management practices such as hiring and career development
c. how the company analyzes and uses its overall employee-related data to evaluate and improve the effectiveness of all categories and all types of employees

Notes:

(1) *Human resource plans and improvement activities might include one or more of the following: mechanisms for promoting cooperation such as internal customer/supplier techniques or other internal partnerships; initiatives to promote labor-management cooperation such as partnerships with unions; creation or modifications in recognition systems; mechanisms for increasing or broadening employee responsibilities; and education and training initiatives. They might also include developing partnerships with educational institutions to develop employees and to help ensure the future supply of well-prepared employees.*

(2) *"Types of employees" takes into account factors such as employment status, bargaining unit membership, and demographic makeup.*

4.2 Employee Involvement
(40 pts.)
Describe the means available for all employees to contribute effectively to meeting the company's quality objectives; summarize trends and current levels of involvement.

AREAS TO ADDRESS

a. management practices and specific mechanisms, such as teams or suggestion systems, the company uses to promote employee contributions to quality objectives, individually and in groups. Summarize how and when the company gives feedback.
b. company actions to increase employee authority to act (empowerment), responsibility, and innovation. Summarize principal goals for all categories of employee.
c. key indicators the company uses to evaluate the extent and effectiveness of involvement by all categories and types of employees and how the indicators are used to improve employee involvement.
d. trends and current levels of involvement by all categories of employees. Use the most important indicator(s) of effective employee involvement for each category of employee.

Note: *Different involvement goals and indicators may be set for different categories of employees, depending upon company needs and upon the types of responsibilities of each employee category.*

4.3 Quality Education and Training
(40 pts.)
Describe how the company decides what quality education and training is needed by employees and how it utilizes the knowledge and skills acquired; summarize the types of quality education and training received by employees in all employee categories

AREAS TO ADDRESS

a. (1) how the company assesses the needs for the types and amounts of quality education and training received by all categories of employees (Describe how the needs assessment addresses work unit requirements to include or have access to skills in problem analysis and problem solving to meet their quality objectives); (2) methods for the delivery of quality education and training; and (3) how the company ensures on-the-job reinforcement of knowledge and skills
b. summary and trends in quality education and training received by employees. The summary and trends should address: (1) quality orientation of new employees; (2) percent of employees receiving quality education and training in each employee category annually; (3) average hours of quality education and training annually per employee; (4) percent of employees who have received quality education and training; and (5) percent of employees who have received education and training in statistical and other quantitative problem-solving methods.
c. key methods and indicators the company uses to evaluate and improve the effectiveness of its quality education and training. Describe how the indicators are used to improve the quality education and training of all categories and types of employees.

Note: *Quality education and training addresses the knowledge and skills employees need to meet the quality objectives associated with their responsibilities. This may include basic quality awareness, problem solving, meeting customer requirements, and other quality-related aspects of skills.*

4.0 HUMAN RESOURCE UTILIZATION (150 pts.)

The ***Human Resource Utilization*** category examines the effectiveness of the company's efforts to develop and realize the full potential of the work force, including management, and to maintain an environment conductive to full participation, quality leadership, and personal and organization growth.

4.1 Human Resource Management
(20 pts.)
Describe how the company's overall human resource management effort supports its quality objectives

AREAS TO ADDRESS

a. how human resource plans are derived from the quality goals, strategies, and plans outlined in 3.2: (1) short term (1-2 years); and (2) longer term (3 years or more). Address major specific requirements such as training, development, hiring, involvement, empowerment, and recognition.
b. key quality goals and improvement methods for human resource management practices such as hiring and career development
c. how the company analyzes and uses its overall employee-related data to evaluate and improve the effectiveness of all categories and all types of employees

Notes:

(1) *Human resource plans and improvement activities might include one or more of the following: mechanisms for promoting cooperation such as internal customer/supplier techniques or other internal partnerships; initiatives to promote labor-management cooperation such as partnerships with unions; creation or modifications in recognition systems; mechanisms for increasing or broadening employee responsibilities; and education and training initiatives. They might also include developing partnerships with educational institutions to develop employees and to help ensure the future supply of well-prepared employees.*

(2) *"Types of employees" takes into account factors such as employment status, bargaining unit membership, and demographic makeup.*

4.4 Employee Recognition and Performance Measurement (25 pts.) Describe how the company's recognition and performance measurement processes support quality objectives; summarize trends in recognition.

AREAS TO ADDRESS

a. how recognition, reward and performance measurement for individuals and groups, including managers, supports the company's quality objectives; (1) how quality relative to other business considerations such as schedules and financial results is reinforced; and (2) how employees are involved in the development and improvement of performance measurements
b. trends in recognition and reward of individuals and groups, by employee category, for contributions to quality
c. key indicators the company uses to evaluate and improve its recognition, reward and performance measurement processes.

4.5 Employee Well-Being and Morale (25 pts.) Describe how the company maintains a work environment conductive to the well-being and growth of all employees; summarize trends and levels in key indicators of well-being and morale.

AREAS TO ADDRESS

a. how well-being and morale factors such as health, safety, satisfaction and ergonomics are included in quality improvement activities. Summarize principal improvement goals and methods for each factor relevant and important to the company's work environment. For accidents and work-related health problems, describe how underlying causes are determined and how adverse conditions are prevented.
b. mobility, flexibility and retraining in job assignments to support employee development and/or accommodate changes in technology, improved productivity, or changes in work processes
c. special services, facilities and opportunities the company makes available to employees. These might include one or more of the following: counseling, assistance, recreational or cultural, and non-work-related education.
d. how employee satisfaction is determined and interpreted for use in quality improvement.
e. trends and levels in key indicators of well-being morale such as safety, absenteeism, turnover, attrition rate for customer-contact personnel, satisfaction, grievances, strikes, and worker compensation. Explain important adverse results, if any, and how problems were resolved or current status. Compare the current levels of the most significant indicators with those industry averages and industry leaders.

5.0 QUALITY ASSURANCE OF PRODUCTS AND SERVICES (140 pts.)

The ***Quality Assurance of Products and Services*** category examines the systematic approaches used by the company for assuring quality of goods and services based primarily upon process design and control, including control of procured materials, parts and services. Also examined is the integration of process control with continuous quality improvement.

5.1 Design and Introduction of Quality Products and Services *(35 pts.)*
Describe how new and/or improved products and services are designed and introduced and how processes are designed to meet key product and service quality requirements.

AREAS TO ADDRESS

a. how designs of products, services and processes are developed so that: (1) customer requirements are translated into design requirements; (2) all quality requirements are addressed early in the overall design process by all appropriate company units; (3) designs are coordinated and integrated to include all phases of product and delivery; and (4) a process control plan is developed that involves selecting and setting key process characteristics for production and delivery of products and services and how these characteristics are to be measured and controlled.
b. how designs are reviewed and validated taking into account key factors: (1) product and service performance; (2) process capability and future requirements; and (3) supplier capability and future requirements
c. how the company evaluates and improves the effectiveness of its designs and design processes and how it shortens the design-to-introduction cycle

Notes:

(1) *Design and introduction may include modification and variants of existing products and services and/or new products and services emerging from research and development.*
(2) *Service and manufacturing businesses should interpret product and service requirements to include all product- and service-related requirements at all stages of production, delivery, and use. See also Item 7.1 Note (3).*
(3) *Depending on their type of business, applicants need to consider many factors in product and service design such as health, safety, long-term performance, measurement capability, process capability, maintainability and supplier capability. Applicant responses should reflect the key requirements of the products and services they delivery.*

5.2 Process Quality Control *(20 pts.)*
Describe how the processes used to product the company's products and services are controlled.

AREAS TO ADDRESS

a. how the company assures that processes are controlled within limits set in process design. Include information on: (1) types and frequencies of measurements; and (2) what is measured, such as process, product, and service characteristics.
b. for out-of-control occurrences, describe: (1) how root causes are determined: (2) how corrections are made so that future occurrences are prevented; and (3) how corrections are verified.
c. how the company evaluates the quality of the measurements used in process quality control and assures measurement quality control.

Note:

(1) For manufacturing and service companies with measurement requirements, it is necessary to demonstrate that measurement accuracy and precision meet process, service and product requirements (measurement quality assurance). For physical, chemical and engineering measurements, indicate approaches for ensuring that measurements are traceable to national standards through calibrations, reference materials or other means.

(2) Verification of corrections and verification of improvements in 5.2b, 5.3c, and 5.4b should include comparison with expected or predicted results.

5.3 Continuous Improvement of Processes *(20 pts.)* Describe how processes used to produce products and services are continuously improved.

AREAS TO ADDRESS

a. principal types of data and information the company uses to determine needs and opportunities for improvement in processes: (1) data from day-to-day process control; (2) field data such as customer data, data on product and service performance, and data on competitors' performance; (3) evaluation of all process steps; (4) process benchmark data, and (5) data of other types such as from process research and development and evaluation of new technology or alternative processes.

b. how the company evaluates potential changes in processes to select from among alternatives.

c. how the company integrates process improvement with day-to-day process quality control: (1) resetting process characteristics; (2) verification of improvements; and (3) ensuring effective use by all appropriate company units.

Note: *The focus of this item is on <u>improvement</u> of the primary processes used to produce the company's products and services, not on maintaining them or on correcting out-of-control occurrences, which is the focus of Item 5.2.*

5.4 Quality Assessment *(15 pts.)*
Describe how the company assesses the quality of its systems, processes, practices, products, and services.

AREAS TO ADDRESS

a. approaches the company uses to assess the quality of its systems, processes, practices, products and services such as process reviews or audits. Include the types and frequencies of assessments, what is assessed, who conducts the assessments, and how the validity of assessment tools is assured.
b. how assessment findings are used to improve systems, processes, practices, training, or supplier requirements. Include how the company verifies that improvements are effective.

5.5 Documentation *(10 pts.)*
Describe documentation and other modes of knowledge preservation and knowledge transfer to support quality assurance, quality assessment and quality improvement.

AREAS TO ADDRESS

a. (1) principal quality-related purposes of documents such as for recording procedures and practices and for retaining key records; and (2) uses of documents such as in standardization, orientation of new employees, training, maintaining records for legal purposes, or for quality-related tracking of products, processes, and services.
b. how the company improves its documentation system: (1) to simplify and harmonize documents; (2) to keep pace with changes in practice, technology, and systems; (3) to ensure rapid access wherever needed; and (4) to dispose of obsolete documents.

Note: *Documents may be written or computerized.*

5.6 Business Process and Support Service Quality *(20 pts.)*
Summarize process quality, quality assessment, and quality improvement activities for business processes and support services.

AREAS TO ADDRESS

a. summary of process quality control and quality assessment activities for key business processes and support services: (1) how principal process quality requirements are set using customer requirements or the requirements of other company units served ("internal customers"); (2) how and how often process quality is measured; and (3) types and frequencies of quality assessments and who conducts them.
b. summary of quality improvement activities for key business processes and support services: (1) principal quality improvement goals and how they are set; (2) principal process evaluation and improvement activities, including how processes are simplified and response time shortened; (3) principal indicators used to measure quality; and (4) how and how often progress is reviewed.

Notes:

(1) *Business processes and support services might include activities and operations involving financial and accounting, software services, sales, marketing, information services, purchasing, personnel, legal services, plant and facilities management, research and development, and secretarial and other administrative services.*

(2) *The purpose of this item is to permit applicants to highlight separately the quality assurance, quality assessment, and quality improvement activities for functions that support the primary processes through which products and services are produced and delivered. Together, Items 5.1, 5.2, 5.3, 5.4, 5.5, 5. and 5.7 should cover all operations, processes, and activities of all work units. However, the selection of support services and business processes for inclusion in Item 5.6 depends on the type of business and quality system and should be made by the applicant.*

5.7 Supplier Quality
(20 pts.)
Describe how the quality of materials, components and services furnished by other business is assured, assessed and improved.

AREAS TO ADDRESS

a. approaches used to define and communicate the company's specific quality requirements to suppliers. Include: (1) the principal quality requirements for the company's most important suppliers; and (2) the principal quality indicators the company uses to communicate and monitor supplier quality.
b. methods used to assure that the company's quality requirements are met by suppliers. Methods may include audits, process reviews, receiving inspection, certification and testing.
c. strategy and current actions to improve the quality and responsiveness of suppliers. These may include partnerships, training, incentives and recognition and supplier selection.

Note: *The term "supplier" as used here refers to other company providers of goods and services. The use of these goods and services may occur at any stage in the production, delivery and use of the company's products and services. Thus, suppliers include businesses such as distributors, dealers and franchises as well as those that provide materials and components.*

6.0 QUALITY RESULTS (180 pts.)

The ***Quality Results*** category examines quality levels and quality improvement based upon objective measures derived from analysis of customer requirements and expectations and from analysis of business operations. Also examined are current quality levels in relation to those of competing firms.

6.1 Product and Service Quality Results *(90 pts.)*
Summarize trends in quality improvement and current quality levels for key product and service features; compare the company's current quality levels with those of competitors and world leaders.

AREAS TO ADDRESS

a. trends and current levels for all key measures of product and service quality.
b. current quality level comparisons with principal competitors in the company's key markets, industry averages, industry leaders and world leaders. Briefly explain bases for comparison such as: (1) independent surveys, studies, or laboratory testing; (2) benchmarks; and (3) company evaluations and testing. Describe how objectivity and validity of comparisons are assured.

Notes:

(1) Key product and service measures are measures relative to the set of all important features of the company's products and services. These measures, taken together, best represent the most important factors that predict customer satisfaction and quality in customer use. Examples include measures of accuracy, reliability, timeliness, performance, behavior, delivery, after-sales services, documentation and appearance. These measures are "internal" measures. Customer satisfaction or other customer data should not be included in response to this item.

(2) Results reported in Item 6.1 should reflect the key product and service features determined in Item 7.1, and be fullY consistent with key quality requirements for products and services.

6.2 Business Process, Operational and Support Service Quality Results *(50 pts.)*
Summarize trends in quality improvement and current quality levels for business processes, operations, and support services.

AREAS TO ADDRESS

a. trends and current levels for the most important measures of the quality and effectiveness of business processes, operations and support services.
b. comparison with industry averages, industry leaders and world leaders.

Notes:

(1) Key measures for business processes, operations and support services are the set of principal measurable characteristics that represent quality and effectiveness in company operations in meeting requirements of customers and of other company units. Examples include measures of accuracy, timeliness and effectiveness. Measures include error rates, defect rates, lead times, cycle times and use of manpower, materials, energy and capital as reflected in indicators such as repeat services, utilization rates and waste.

(2) The results reported in Item 6.2 derive from quality improvement activities described in Category 5 and Item 1.4, if appropriate. Responses should reflect relevance to the company's principal quality objectives and should also demonstrate the breadth of improvement results throughout all operations and work units.

6.3 Supplier Quality Results *(40 pts.)*
Summarize trends and levels in quality of suppliers and services furnished by other companies; compare the company's supplier quality with that of competitors and with key benchmarks.

AREAS TO ADDRESS

a. trends and current levels for the most important indicators of supplier quality.
b. comparison of the company's supplier quality with that of competitors and/or with benchmarks. Such comparisons could include industry averages, industry leaders, world leaders, principal competitors in the company's key markets and appropriate benchmarks. Describe the bases for comparisons.

Note: *The results reported in Item 6.3 derive from quality improvement activities described in Item 5.7. Results should be broken down by major groupings of suppliers and reported using the principal quality indicators described in Item 5.7.*

7.0 CUSTOMER SATISFACTION (300 pts.)

The ***Customer Satisfaction*** category examines the company's knowledge of the customer, overall customer service systems, responsiveness and its ability to meet requirements and expectations. Also examined are current levels and trends in customer satisfaction.

7.1 Determining Customer Requirements and Expectations *(30 pts.)* Describe how the company determines current and future customer requirements and expectations.

AREAS TO ADDRESS

a. how the company determines current and future requirements and expectations of customers. Include information on: (1) how market segments and customer groups are determined and how customers of competitors and other potential customers are considered; (2) the process for collecting information and data. This should include what information is sought, frequencies of surveys, interviews of other contacts and how objectivity is assured; (3) how other information and data are cross-compared to support determination of customer requirements and expectations. Such information and data might include performance information on the company's products and services, complaints, gains and losses of customers, customer satisfaction and competitors' performance.
b. process for determining product and service features and the relative importance of these features to customers and/or customer groups
c. how the company evaluates and improves its processes for determining customer requirements and expectations as well as the key product and service features.

Notes:

(1) Products and services may be sold to end users by intermediaries such as retail stores or dealers. Thus, determining customer groups should taken into account both the end users and the intermediaries.

(2) Product and service features refer to all important characteristics of products and services experienced by the customers throughout the overall purchase and ownership experiences. This includes any factors that bear upon customer preference or customer view of quality for example, those features that enhance them or differentiate them from competing offering.

(3) An applicant may choose to describe its offerings, part of its offerings, or certain of its activities as products or services irrespective of the SIC classification of the company. Such descriptions should then be consistent throughout the Application Report.

7.2 Customer Relationship Management *(50 pts.)* Describe how the company provides effective management of its relationship with its customers and uses information gained from customers to improve products and services as well as its customer relationship management practices.

AREAS TO ADDRESS

a. means for ensuring easy access for customers to seek assistance and to comment. Describe types of contact, such as telephone, personal and written, and how the company maintains easy access for each type of contact.
b. follow-up with customers on products and services to determine satisfaction with recent transactions and to seek data and information for improvement.
c. how the following are addressed for customer-contact personnel: (1) selection factors for customer-contact jobs; (2) career path; (3) special training to include: knowledge of products and services, listening to customer, soliciting comment from customers, how to anticipate and handle special problems or failures, and skills in customer retention; (4) empowerment and decision making; (5) attitude and morale determination; (6) recognition and reward; and (7) attrition
d. how the company provides technology and logistics support for customer-contact personnel to enable them to provide reliable and responsive services.
e. how the company analyzes key customer-related data and information to assess costs and market consequences for policy development, planning and resource allocation.
f. principal factors the company uses to evaluate its customer relationship management, such as response accuracy, timeliness and customer satisfaction with contacts. Describe how the factors or indicators are used to improve training, technology or customer-oriented management practices.

Notes:

(1) Other key aspects of customer relationship management are addressed in Items 7.3, 7.4 and 7.5.

(2) Item 7.2c addresses important human resource management requirements specifically for customer-contact personnel. This is included in Item 7.2 for special emphasis and coherence.

7.3 Customer Service Standards *(20 pts.)* Describe the company's standards governing the direct contact between its employees and customers and how these standards are set and modified.

AREAS TO ADDRESS

a. how well-defined service standards to meet customer requirements are set. List and briefly describe the company's most important customer service standards.
b. how standards requirements and key standards information are deployed to company units that support customer-contact personnel. Briefly describe how the company ensures that the support provided by these company units is effective and timely.
c. how service standards are tracked, evaluated and improved. Describe the role of customer-contact personnel in evaluating and improving standards.

Note: *Service standards are objectively measurable levels of performance that define quality for the overall service or for a part of a service. Examples include measures of response time, problem resolution time, accuracy and completeness.*

7.4 Commitment to Customers *(15 pts.)* Describe the company's commitment to customers on its explicit and implicit promises underlying its products and services.

AREAS TO ADDRESS

a. types of commitment the company makes to promote trust and confidence in its products, services and relationships. Include how the company ensures that these commitments: (1) address the principal concerns of customers; (2) are free from conditions that might weaken customer confidence; and (3) are understandable.
b. how improvements in the quality of the company's products and services over the past three years have been translated into stronger commitments. Compare commitments with those of competing companies.

Note: *Commitments may include product and service guarantees, product warranties and other understandings with the customer, expressed or implied.*

7.5 Compliant Resolution for Quality Improvement *(25 pts.)*

AREAS TO ADDRESS

a. how the company ensures that formal and informal complaints and feedback given to different company units are aggregated for overall evaluation and use wherever appropriate throughout the company.
b. how the company ensures that complaints are resolved promptly and effectively. Include: (1) trends and levels in indicators of response time; and (2) trends in percent of complaints resolved on first contact with customer-contact personnel.
c. how complaints are analyzed to determine underlying causes and how the findings are translated into improvements. This transition may lead to improvements such as in processes, service standards, training of customer-contact personnel and information to customers to help them make more effective use of products and/or services.
d. key indicators and methods the company uses to evaluate and improve its complaint-related processes. Describe how indicators and methods address effectiveness, response time improvement and translation of findings into improvements.

Notes:

(1) A major purpose of aggregation of complaint information is to ensure overall evaluation for policy development, planning, training and resource allocation. However, this does not imply that complaint resolution and quality improvement should await aggregation or that resolution and improvement are necessarily centralized within a company.

(2) Trends and current levels in complaints are requested in Item 7.7.

7.6 Determination Customer Satisfaction *(20 pts.)*
Describe the company's methods for determining customer satisfaction, how satisfaction information is used in quality improvement, and how methods for determining customer satisfaction are improved.

AREAS TO ADDRESS

a. how the company determines customer satisfaction for customer groups, Address: (1) brief description of market segments and customer groups; and (2) the process for determining customer satisfaction for customer groups. Include what information is sought, frequency of surveys, interviews or other contact, and how objectively is assured. Describe how the company sets the customer satisfaction measurement scale to adequately capture key information that accurately reflects customer preference.
b. how customer satisfaction relative to competitors is determined.
c. how customer satisfaction data a re analyzed and compared with other customer satisfaction indicators such as complaints and gains and losses of customers. Describe how such comparisons are used to improve customer satisfaction determination.
d. how the company evaluates and improves its overall methods and measurement scales used in determining customer satisfaction and customer satisfaction relative to competitors.

Notes:
(1) Information sought in determining customer satisfaction may include specific product and service features and the relative importance of these features to customers, thus supplementing information sought in determining customer requirements and expectations.
(2) The customer satisfaction measurement scale may include both numerical designators and the descriptors assigned to them. An effective scale is one that provides the company with accurate information about specific product and service features and about the customers' likely market behaviors.

7.7 Customer Satisfaction Results *(70 pts.)*
Summarize trends in the company's customer satisfaction and in indicators of adverse customer response.

AREAS TO ADDRESS

a. trends and current levels in indicators of customer satisfaction for products and services. Segment these results by customer groups, as appropriate.
b. trends and current levels in major adverse indicators. Adverse indicators include complaints, claims, refunds, recalls, returns, repeat services, litigation, replacements, downgrades, repairs, warranty costs and warrant work. If the company has received any sanctions under regulation or contract over the past three years, include such information in this item. Briefly describe how sanctions were resolved or current status.

7.8 Customer Satisfaction Comparison *(70 pts.)* Compare the company's customer satisfaction results and recognition with those of competitors that provide similar products and services.

AREAS TO ADDRESS

a. comparison of customer satisfaction results. Such comparisons should be made with principal competitors in the company's key markets, industry averages, industry leaders and world leaders.

b. surveys, competitive awards, recognition and ratings by independent organizations, including customers. Briefly describe surveys, awards, recognition and ratings. Include how quality and quality attributes are considered as factors in the evaluations of these independent organizations.

c. trends in gaining or losing customers and in customer and customer account retention. Briefly summarize gains and losses of customers, including those gained from or lost to competitors. Address customer groups or market segments, as appropriate.

d. trends in gaining and losing market share relative to major competitors, domestic and foreign. Briefly explain significant changes in terms of quality comparisons and quality trends.

APPENDIX C:

ACRONYMS

ASIC	Application Specific Integrated Circuits
CAD	Computer-Aided-Design
CMOS	Complementary Metal Oxide Semiconductor
DAR	Deficiency Area Reports
DESC	Defense Electronic Supply Center
DoD	Department of Defense
DSB	Defense Science board
EIA	Electronic Industry Association
Fat FET	Large Field Effect Transistor
FFRP	Field Failure Return Program
FSC	Federal Stock Code
GB	Ground Benign
GF	Ground Fixed
HDI	High Density Interconnect
IC	Integrated Circuit
ICWG	Industry Coordinating Working Group
JEDEC	Joint Electronic Device Engineering Circuit
MCM	Multichip Module
MIM	Metal Insulator Metal
MIMIC	Microwave and Millimeter-Wave Monolithic Integrated Circuit
NASA	National Aeronautics and space Administration
NECQ	National Electronic Components Quality Assessment
NEQPS	National Electronic Quality Process Standard
OEM	Original Equipment Manufacturers
PA	Preparing Activity
PM	Parametric Monitor
PROMS	Programmable Read Only Memories
PWA	Printed Wiring Assemblies
PWB	Printed Wiring Boards
QCI	Quality Conformance Inspection
QM	Quality Management
QML	Qualified Manufacturers List
QPL	Qualified Product List
RADC	Rome Air Development Center
RF	Radio Frequency
RHA	Radiation Hardness Assurance
RHACL	Radiation Hardened Assurance Capability Level
RL	Rome Laboratory
RWOH	Reliability without Hermeticity
SCD	Specification Control Drawing
SEC	Standard Evaluation Circuit
SMD	Standard Military Drawing
SPC	Statistical Process Control
SPO	System Program Offices
TCI	Technology Conformance Inspection

TCV	Technology Characterization Vehicle
TQM	Total Quality Management
TRB	Technology Review Board

APPENDIX D:

RAC PRODUCTS

RAC Product Order Form

		U.S.	Non-U.S.	Qty	Item Total
RELIABILITY HANDBOOKS					
RMST-91	Reliability and Maintainability Software Tools 1991	50.00	60.00		
TOOLKIT	RADC Reliability Engineer's ToolKit	10.00	20.00		
RDSC-1	Reliability Sourcebook	25.00	35.00		
MFAT-1	Microelectronics Failure Analysis Techniques - A Procedural Guide	140.00	180.00		
MFAT-2	GaAs Characterization and Failure Analysis Techniques - A Procedural Guide	100.00	130.00		
MFAT 1&2	Combined set of MFAT-1 and MFAT-2	200.00	300.00		
FTA	Fault Tree Analysis Application Guide	80.00	90.00		
NPS-1	Analysis Techniques for Mechanical Reliability	60.00	70.00		
PRIM-91	A Primer for DoD Reliability, Maintainability and Safety Standards	120.00	140.00		
RELIABILITY DATA					
NPRD-91	Nonelectronic Parts Reliability Data - 1991 (includes discrete electronic parts)	150.000	170.00		
NPRD-91P	Nonelectronic Parts Reliability Data - 1991 (IBM PC database)	400.00	440.00		
DSR-4	Discrete Semiconductor Device Reliability - 1988	100.00	120.00		
FMD-91	Failure Mode Distribution Critical Technology Review Assessment	100.00	120.00		
NONOP-1	Nonoperating Reliability Data - 1987	150.00	160.00		
MDR-22	Microcircuit Screening Analysis - 1987	125.00	135.00		
VZAP-90	Electrostatic Discharge Susceptibility Data	150.00	160.00		
VZAP-90P	VZAP-90 Data on diskette (IBM PC database)	350.00	380.00		
VZAP-90C	Complete VZAP package including VZAP-90 publication and VZAP-90P	450.00	480.00		
MDR-21	Trend Analysis Databook - 1985	100.00	110.00		
STATE-OF-THE-ART REPORTS AND SOFTWARE					
SOAR-2	Practical Statistical Analysis for the Reliability Engineer	40.00	50.00		
SOAR-3	IC Quality Grades: Impact on System Reliability and Life Cycle Cost	50.00	60.00		
SOAR-4	Confidence Bounds for System Reliability	50.00	60.00		
SOAR-5	Surface Mount Technology: A Reliability Review	60.00	70.00		
SOAR-6	ESD Control in the Manufacturing Environment	60.00	70.00		
SOAR-7	A Guide for Implementing Total Quality Management	75.00	85.00		
CRTA-PEM	Plastic Microcircuit Packages: A Technology Review	50.00	60.00		
CRTA-QML	Qualified Manufacturer's List: New Device Mfg. and Procurement Technique	50.00	60.00		
CRTA-GaAs	Assessment of GaAs Device Quality and Reliability	50.00	60.00		
VPRED	VHSIC Reliability Prediction Software	150.00	160.00		
RAC-NRPS	Nonoperating Reliability Prediction Software (Includes NONOP-1)	1400.00	1450.00		
RELIABILITY INDICES AND PROCEEDINGSs					
TRS-2	Search and Retrieval Index to IRPS Proceedings - 1968 to 1978	24.00	34.00		
TRS-2A	Search and Retrieval Index to IRPS Proceedings - 1979 to 1984	24.00	34.00		
TRS-3A	EOS/ESD Technology Abstracts - 1982	36.00	46.00		
TRS-4	Search and Retrieval Index to EOS/ESD Proceedings - 1979 to 1984	36.00	46.00		
TRS-5	Search and Retrieval Index to ISTFA Proceedings - 1978 to 1985	36.00	46.00		
MIL-HDBK-338	MIL-HDBK-338: Subject Index	25.00	35.00		
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Plastic Microcircuit Packages: A Technology Review

1992

Prepared by:

Reliability Analysis Center
PO Box 4700
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This report presents a critical review of the current information available on the reliability and related issues pertaining to plastic encapsulated microcircuits (PEMs). Numerous reports and studies have been published in scattered symposia and journals in this area since the RAC publication, *IC Quality Grades: Impact on System Reliability and Life Cycle Cost,* in 1985. This report will bring together in one reference a summary of the current state-of-the-art. The information presented is based upon the results of an extensive literature review and discussions with industry experts.

Included are sections on each of the following issues; cost, availability, quality, and reliability and failure mechanisms.

The annotated bibliography provides an extensive listing of over 200 references relating to this topic area.

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PREFACE

The purpose of this RAC CRTA - Critical Review and Technology Assessment is to revisit the available information on the reliability and related issues pertaining to plastic encapsulated microcircuits (PEMs). Specific areas addressed include:

- Availability
- Quality
- Reliability
- Cost

The last decade has brought about revolutionary changes in electronics technology in general, and plastic packaging in particular. Literally hundreds of studies have reported progress in plastic packaging integrity brought about by improvements in materials, increased purity of the plastics, high quality passivation layers processes, and major device manufacturer's quality programs. This report was prompted by the numerous changes in this technology in the last 5-10 years. An extensive annotated bibliography is provided to facilitate further research.

Plastic Microcircuit Packages: A Technology Review

1.0 INTRODUCTION

Todays emphasis on packaging from a reliability performance and cost aspect has resulted in a resurgence of organic encapsulation materials and techniques studies for microcircuit packaging. This report presents a critical review of the current information available on the reliability and related issues pertaining to plastic encapsulated microcircuits (PEMs). Numerous reports and studies have been published in scattered symposia and journals in this area since the RAC publication, *IC Quality Grades: Impact on System Reliability and Life Cycle Cost,* in 1985. Recent programs established to investigate this area represent a renewed interest in PEM technology, particularly for highly critical applications with the most scrutinous examination of this technology since the late sixties and early seventies. Important studies at that time were the RADC (now Rome Laboratory) effort "Can Plastic Encapsulated Microcircuits Provide Reliability With Economy" which studies screening and qualification procedures and the US Army LABCOM Panama Test Program which tested plastic devices in a worst case field environment. Appendix C presents a chronology of forementioned and other early studies concerning Plastic Encapsulated Semiconductor Technology. Reading of the Appendix C papers and this report should provide insight into a common question: "Why does the military limit the use of plastic packaged devices?" This report does not recommend or imply the use of PEM's in violation of present military requirements.

This report will bring together in one reference a summary of the current state-of-the-art. The information presented is based upon the results of an extensive literature review and conversations with industry experts.

"In order to present an unbiased view of the state-of-the-art of PEM's all references to efforts, studies and papers used in this document have been given equal weight. Their adequacy, correctness, testing and conclusions were neither questioned nor rated."

Included are sections addressing each of the following issues:

- Cost
- Availability
- Quality
- Reliability and failure mechanisms

The annotated bibliography in Appendix D provides an extensive listing of over 200 references on recent advances in this topic area to facilitate further research.

1.1 Background

Today's nearly exclusive use of hermetically sealed microcircuits in military, aerospace, and other high reliability, high criticality, rugged applications is a direct result of the early problems associated with plastic packaged integrated circuits that occurred during their introduction in the 60's and early 70's.

Early plastic molding compounds were plagued by a problem known as thermal intermittence. The differences between the Thermal Coefficients of Expansion (TCE) of the bond wires which expanded slowly and the plastic which expanded fairly rapidly at elevated temperatures, caused the bond wires to separate, thereby causing failure. When the device cooled down to room temperature, the bond often returned to its normal position and re-tested good.

Moisture was also a significant problem at that time. Devices were molded with significant amounts of moisture on the die surface. In addition, moisture penetrated the device packages fairly easily. Moisture reaching the chip carried with it manufacturing residues such as process-related chloride and phosphorus. Over time, the moisture would combine with these contaminants leading to corrosion. Poor adhesion of the molding material to the lead frame allowed migration of moisture and ionic contaminants along the lead frame and bond wires as well. Die glassivation often contained cracks and pinholes allowing easy access to the metallization, and to the unglassivated area of bonding pads. Early 85°C/85% testing in 1974 generally showed numbers in the 25% cumulative failures at 1000 hours (Ref. 1) compared with .1% today.

Problems with intermetallic compound formation between dissimilar metals at elevated temperatures often caused poor electrical conductivity, brittleness, reduced bond strength and eventual bond lifting. Kirkendall voiding occurred when the Au diffused into the Al faster than the Al in Au, thereby forming voids which would grow with continued exposure to temperature, leading to open circuit.

These early reliability problems associated with PEMs caused the reliability of these parts to be poor, particularly for use in rugged, highly critical applications. Use was thus limited to short term commercial applications where long term reliability was not an issue. Substantial improvements in the materials and processes of this technology have occurred since their introduction. Over the years the applicability of this technology has been periodically re-visited due primarily to cost and availability incentives. As improvements in the technology continue to be made reliability and quality issues which counter-balance cost and availability advantages continue to be re-evaluated.

1.2 Changing Trends

Interest in the applicability of these parts, even in military, aerospace and telecommunications areas, with their strict reliability requirements and severe environmental conditions, seems to have resurged ever more intently in the last few years. The appeal results from continued improvements in the technology, and a corresponding increase in the number of success stories, most notably the automotive industry. This interest is demonstrated by the increasing number of test methods, procedures and large programs investigating their applicability:

- JEDEC Standard No. 26-A, *Quality and Reliability Assurance of Plastic Encapsulated Microcircuits*, (PEMs) for use in rugged environments. This specification establishes uniform procedures and defines the general requirements for the quality and reliability assurance of plastic encapsulated (non-cavity) microcircuits used in ground, fixed or benign applications.

- JEDEC Standard JESD22-A100-A, *Cycled Temperature Humidity Bias Life Test* (January 1989), presents the Cycled Temperature

Humidity Bias Life Test performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments.

- JEDEC Test Method A110, *Highly-Accelerated Temperature and Humidity Stress Test (HAST)*, this test employs severe conditions of temperature, humidity and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.

- Proposed JEDEC Test Method A112, *Moisture Stress Sensitivity for Plastic Surface Mount Devices*, describes a test method to identify plastic surface mount devices which are sensitive to moisture-induced stress so they can be properly packaged, stored, and handled to avoid subsequent damage during solder reflow attachment and/or repair operation.

- MIL-I-38535A and proposed Amendment 1, *Integrated Circuits Manufacturing, General Specification For*, identifies the necessary criteria to allow a plastic device vendor to be included in the QML.

- Paragraph 5.4 of requirement 64 of MIL-STD-454M (Ref. 3), *Standard General Requirements for Electronic Equipment*, which covers requirements to be used in military specifications for electronic equipment states upon specific request and approval by the procuring activity to waive the requirements of 4.1, non-hermetic microcircuits may be considered for use in ground-fixed (GF) or ground benign (GB) environments as defined in MIL-HDBK-217, provided they meet all the requirements of the equipment specification, temperature and humidity are completely controlled in transit, storage, and application, and provisions have been made for logistic availability.

- The USAF Wright Laboratory has awarded a $4.2 million, four-year Manufacturing Science contract to the Microelectronics and Computer Technology Corporation (MCC), in conjunction with Lehigh University; and a $600K, 24 month contract to National Semiconductor in conjunction with Dow Corning Corp., for the Reliability Without Hermeticity (RwoH) Project. The long term goal of the project is to allow replacement of hermetic packages evaluation of organic and inorganic coatings that can be placed directly onto the semiconductor devices and multichip modules. MCC is investigating polymeric coatings, while National Semiconductor is working with the Dow Corning inorganic Surface Protection for Electronic Circuits (SPEC) coating for this purpose.

- The USAF Rome Laboratory at Griffiss AFB, NY is involved in evaluating innovative approaches for protecting microcircuits not contained in hermetically sealed packages. Technical guidance and monitoring was provided to the Defence Advanced Research Projects Agency (DARPA) funded research program to Dow Corning (contract #F49620-86-C-0110) to evaluate their SPEC coating. Additionally, a RL sponsored research program on packaging reliability entitled "Reliable Module for WSI" (contract #F30602-89-C-0195) with the Environmental Research Institute of Michigan (ERIM) is complete pending delivery of the final report.

- IIT Research Institute and Honeywell, Inc. have, under contract to the US Army Armament, Research, Development and Engineering Center (ARDEC) at Picatinny Arsenal in New Jersey, conducted a study comparing the performance of both EP/TAB ICs and hermetically sealed integrated circuits. The study was to determine if EP/TAB (Environmentally Protected Tape Automated Bonded) IC Packaging could be a viable alternative to hermetically sealed ICs presently used in military systems (Ref. 4). In addition, IITRI, also under contract to ARDEC, prepared specifications for the purchase and test of quality, highly reliable EP/TAB devices and for assuring the

integrity of EP/TAB IC's when included in the next level of assembly and incorporated EP/TAB IC requirements in proposed Amendment 1 to MIL-I-38535A.

- The Defense Science Board (DSB) 1986 Summer Study Group, "Use of Commercial Components in Military Equipment", reports dated January 1987 and June 1989 recommended the generation of a microcircuit selection guidebook. The US Army Electronics Laboratory Command was tasked to lead the effort. The effort is being overseen by Patrick Layden. The guidebook, which is nearing release at the time of this report, is to be used in conjunction with the QML and QPL for the selection of devices for military systems, based on cost-effective performance and reliability in a given application. Appropriate choices for packaging will be based on severity of the service environment and reliability criticality. An interesting observation in the guidebook concerning plastic encapsulated microcircuits indicates that the QML procedures will allow successful definition of their usage.

The key or perceived advantages of this technology which brings about it's continued interest, particularly in the last few years, include:

- Greater availability and mechanical shock resistance
- Reported improvements in reliability
- Reported improvements in manufacturer quality
- Lower acquisition cost

The current status of the technology in each of these four areas of the findings will be reviewed in the following sections.

2.0 ISSUES UPDATE

The last decade has brought about revolutionary changes in electronics technology in general and plastic packaging in particular. Literally hundreds of studies have reported progress in plastic package integrity brought about by improvements in materials, increased purity of the plastics, high quality passivation layer processes and major device manufacturer's quality programs. Interest in this packaging alternative is heightened by high shock resistance, greater availability, lighter weight and lower acquisition costs.

Additionally, performance parameters are dictating different packaging approaches i.e., speed. Discrete packaging and glue chips are being replaced with multichip modules i.e. ASIC's interconnected on large substrates. Hermetic packaging does not appear to have kept up with these technology advances in either a performance or a cost effective way. The following considerations must be given to alternate packaging approaches:

1. Performance should not be compromised by packaging.

2. High volume controlled process and materials are needed to insure quality.

3. Evaluation, qualification and test procedures must be developed and coordinated.

It is beyond the scope of this report to individually cite all references on PEMs in the last 5 years. However, some of the more recent industry trends which have had a significant effect in this technology area are discussed. The bibliography contains an extensive list of pertinent documents for further investigation. The issues of cost, availability, quality and reliability are discussed in the following sections of this report.

2.1 Cost

A hermetically packaged IC may cost (cost here refers to purchase cost opposed to life cycle cost) 3 to 10 times more than a plastic packaged IC.[1] It is often argued that this difference is largely due to added testing and screening of hermetic parts, and that much of the reported cost advantage of PEMs will be lost when subjected to individual testing to rigid user specifications. However, a study by ELDEC (Ref. 5) estimated that purchased component costs for plastic ICs are 12% less costly than their hermetic counterparts when both types are screened to customer requirements. Hermetic packages are usually constructed of more expensive materials and use costly, time consuming manufacturing processes. Since 80-90% of the IC market is plastic packaged, there are lower overhead costs per unit produced and savings from the low labor costs associated with off-shore manufacturing are not seen with hermetic parts. Present military requirements specify on-shore manufacturing. In the area of surface mount packaging, ceramic surface mount components are even more costly than ceramic dips, while there is little difference between cost of plastic surface mount components and plastic DIPs. As one example, Thomson-CSF reports (Ref. 6) a 45% purchase cost reduction for a manpack transceiver application implemented with PEMs instead of ceramic components for each of 12 printed circuit boards of the equipment. However, these cost benefits reported for PEMs become lower or nonexistent with higher integration, higher pin-count devices because of the high value of the die in relation to the total cost of the device. While these cost benefits may not be realized for complex monolithic IC's, large cost advantages may exist for complex package styles, such as multichip modules.

Reference 7 has reported the cost of the package alone for plastic and ceramic dips, Leadless Chip Carriers, and Pin Grid Arrays. These figures are shown in Table 1.

Plastic packaged parts lend themselves well to automatic assembly techniques, thereby eliminating manual handling and operator error, resulting in improved yields and and lower assembly cost. Automated assembly pick and place machines can crack hermetic seals or chip the package.

[1] RAC's SOAR-3, "IC Quality Grades: Impact on System Reliability and Life Cycle Cost.

Table 1: Ratio of Ceramic to Plastic Package Cost for Three Package Styles[1,2]

Package Style	8	16	18	20	24	28	40	48	68	84	120	168	208	256	Geometric Mean for Row
DIP	4.0	6.7	6.3	6.0	8.3	7.5	6.9								6.4
Chip Carrier			14.3	17.1	18.8	17.0	13.5	13.5	13.3	11.0					14.6
Pin Grid Array									1.6	1.9	2.5	3.5	2.6	2.5	2.4

(1) The above ratios are for the costs of empty packages and lid for large volumes.

(2) Semiconductor Economics Report, DM Data Inc., Scottsdale, AZ, Vol. 3, No. 9, May 1989, p. 8.

These reported cost savings do not reflect a total life cycle cost savings which considers the cost of any additional repair replacement costs. Total Life Cycle Cost (LCC) analysis ultimately is the only method of determining any true savings in any design technology trade-off decision. Section 2.4 on reliability issues provides additional information needed for a total LCC consideration. In it's most simplified form, the difference in life cycle cost between the packaging alternatives may be estimated as follows:

$$\Delta LCC = \Delta IC \text{ acquisition} + \Delta \text{cost of yield failures} + \Delta \text{cost of field failures} + \Delta \text{cost of inventory}$$

2.2 Availability

PEMs hold a definite advantage over hermetic devices with regard to availability. First, since plastic devices are built on continuous production lines, as opposed to an on-demand basis for hermetic parts, lead times are significantly shorter. In addition, start-up problems associated with the re-start of a hermetic line are not a problem with continuous production lines. Secondly, some parts are simply not available from major manufacturers in hermetic form. Most designs are developed first as a PEM. Approximately 30% more part numbers are available in plastic packages than hermetic at any one time. US Military electronics, the major purchaser of hermetic parts, has become a small portion of

the total electronics market, compared to nearly 80% of the total market in the 1960s.

2.3 Quality

Quality assurance provisions are not as standardized for PEMs as they are for hermetic devices. While hermetic devices are presently subjected to the rigors of the qualification and screening sequences of MIL-M-38510 and MIL-STD-883, the procedures available for insuring PEM robustness are just now starting to be addressed. Also some of the procedures currently used for insuring hermetic device reliability simply are not applicable to PEMs. There are however many efforts that have been and are being undertaken to develop such methodologies for PEMs. Initial efforts have focused on preconditioning requirements and on testing methodologies such as Highly Accelerated Stress Testing (HAST), autoclave and 85°C/85% RH tests. While the industry is using commonly accepted practices for some of these the level of standardization will undoubtedly increase as the technology and test equipment matures.

Tests for plastic devices, to accelerate known and possible failure mechanisms of PEMs, must be developed, validated, and standardized. Steps toward this have already been taken such as the JEDEC standard 26A, "General Specification for Plastic Encapsulated Microcircuits for Use in Rugged Applications." This specification establishes uniform procedures and defines the general requirements for the Quality and Reliability Assurance of plastic encapsulated (non-cavity) microcircuits used in ground, fixed or benign applications. Detail requirements, specific characteristics of microcircuits, and other provisions which are sensitive to the particular use intended shall be specified in the applicable detail specification.

With the increasing popularity of the QML (Qualified Manufacturers List) past arguments that plastic devices would loose some of their appeal if attempts were made to qualify individual plastic parts may disappear. Major manufacturers are keenly aware of the quality issue and have instituted programs such as Motorola's Six Sigma Program (Ref. 9). The recently issued MIL-I-38535A identifies some of the necessary criteria for a PEM vendor to be included in the

QML. (This inclusion does not, however, change the military usage requirements for PEMs).

Variability between manufacturers is a concern. Reference 10 presents extended temperature range testing of a plastic encapsulated CMOS micro-controller device from three manufacturer's. All three manufacturer's devices were specified to operate in the -40°C to +85°C range. However, manufacturer A's parts tested would not operate at -40°C. Also, manufacturer B's IC's were found to be electrically incompatible with the other two manufacturers, although this was not evident from the data sheets. For a user with consistently high device reliability needs, a strong relationship must exist with his supplier for both business and manufacturing processes. The use of statistical process control (SPC), where needed for measuring and controlling process and device quality and design of experiments (DOE) implementation to guide process and device quality improvement is necessary. Vendor and part certification/qualification and requalification of appropriate changes are required to ensure user/system needs. In essence strict manufacturer evaluation, selection and control procedures should be implemented.

Manufacturers should have data and documentation to substantiate claims of reliability and quality levels and process/test improvements and changes. An effective, on-going reliability program which demonstrates that the manufacturer understands the product and operating environment limitations is necessary.

2.4 Reliability

There have been several reports during the last decade of the reduced reliability gap between hermetic devices and PEMs. Manufacturing development efforts to improve performance and reliability in PEMs are continuing. Improvements in encapsulated materials such as:

- low ionic impurities
- low moisture adsorption
- better adhesion properties
- matching of thermal coefficients to die/lead frame
- high glass transition temperature

- higher thermal conductivity

and advances in passivations such as:

- better adhesion to die
- less pinholes or cracks
- low ionic impurity
- lower water vapor absorption
- thermal properties better matched to substrate
- spun-on-glass techniques

have caused dramatic improvements in the reliability of PEMs over the last several years. Figure 1 summarizes published improvements in PEM reliability between 1976 and 1990 which is representative of laboratory tests.

The automotive industry, consuming almost 3 million plastic ICs per day, has reported much success in its use of plastic parts in the severe automotive environment. ICs not hermetically sealed are reported to provide adequate reliability in the automotive environment. Chips under the hood control many engine functions including air/gas mixture and ignition control. Temperatures under the hood reach over 100°C and exposure to contaminants such as gasoline and motor oil is common. Table 2 cites some examples of the conditions in the automotive environment. These are only examples, and vary according to engine, vehicle, and application type.

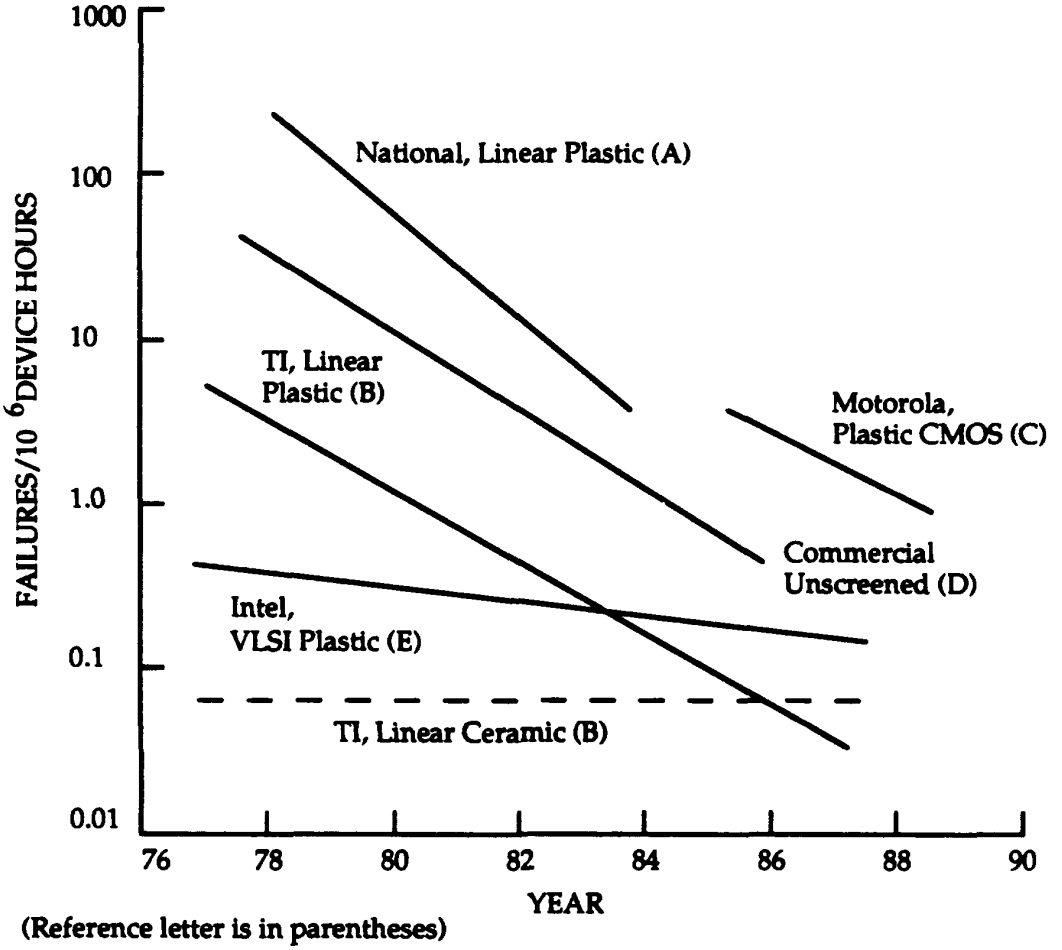
This section presents a discussion of the reliability concerns which currently are an issue with PEMs. The main failure mechanisms in relation to plastic encapsulation, as identified in discussions with manufacturers and a literature survey, are discussed.

Figure 2 shows failure mechanism data from Delco Electronics (Ref. 34) on 636 ICs (513 Bipolar and 123 MOS) analyzed. Bond/wire failure mechanisms account for almost 41% of failures analyzed, electrical overstress, a design-related problem accounted for 18.4% of the failures, approximately 12.5% of failures analyzed were quality-type defects such as masking or etching defects,

electrostatic discharge (ESD) failures accounted for 5% of failures (RAC publication VZAP-91 treats the problem of ESD), contamination/corrosion caused 2% of failures. The balance of failures analyzed resulted from mechanisms which accounted for < 1% of the total sample analyzed.

In Reference 34, Delco has also made projections of future defect rates (or failure rates) based on observed trends in historical data. The Delco data has indicated that the failure rate (in PPM per 5 year or 50,000 miles) was approximately 1,800 in 1986 and has decreased to approximately 650 in 1989. Based on the rate of decrease, an exponential regression suggests that a failure rate of .1 PPM per 5/50K in the year 2001 is a reasonable goal. Section 2.5 of this document presents a reliability model for automotive electronics based on a database separate from the Delco data. Section 2.5 also presents non-automotive data which indicates a trend similar to the Delco data. The absolute failure rate of the non-automotive data in Section 2.5 is however lower than the Delco data, most likely due to the more severe environmental stresses in automotive applications.

These results are consistent with findings in the literature. The main failure mechanisms reported for PEMs include: intermetallic formation, contamination, corrosion, filler particle induced stress effects and thermal mismatch. EOS has been excluded because it is not an exclusive plastic failure mechanism.



(Reference letter is in parentheses)

References:

(A) Pantic, D.M., "Maturity Factors in Predicting Failure Rate for Linear Integrated Circuits," IEEE Transactions on Reliability, Vol. R-33, No. 3., August 1984, pp. 208-211.

(B) Texas Instruments, Ceramic/Plastic Comparison Report to ELDEC, October 24, 1988.

(C) Fergus, K., "A Discussion on the Effectiveness of Better Level I (Temperature Cycling) and Level II (Burn-in) Screening," Motorola Reliability Report RIC-6086, January 1990.

(D) Frank, H., "Reliability and MIL-HDBK-217 Prediction," Reliability Review, Vol. 10, September 1990, pp. 7-9.

(E) Crook, D.L., "Evolution of VLSI Reliability Engineering," Proceedings of the 28th Annual IEEE Reliability Physics Symposium, 1990, pp. 2-11.

Figure 1: Microcircuit Reliability Improvement Trends

Condra, L. and Pecht, M., "Options for Commercial Microcircuits in Avionics Products," Defense Electronics, July 1991.

Table 2: Sample Environmental Conditions for Automotive Applications

LOCATION	TEMP. RANGE (°C)	RELATIVE HUMIDITY (% AT 40°C)	SALT SPRAY	VIBRATION & SHOCK
UNDER THE HOOD				
Above the exhaust	-40 - 650	80	YES	50 g to 1KHz
Intake manifold	-40 - 125	95	YES	Over 100 g
Fireproof wall	-40 - 140	80	YES	1 g to 600 Hz
Vehicle frontal zone	-40 - 85	98	YES	1 g to 600 Hz
ON THE CHASSIS				
Inside a wing	-40 - 85	98	YES	2 g to 2 KHz
Near the exhaust system	-40 - 125	98	YES	2 g to 2 KHz
Extreme conditions	-40 - 175	98	YES	Over 100g
WITHIN THE CAR INTERIOR				
Dashboard	-40 - 120	98	NO	1 g to 20Hz
Rear window	-40 - 104	98	NO	1 g to 20Hz

These figures are only an indication. Values differ according to engine and vehicle type.

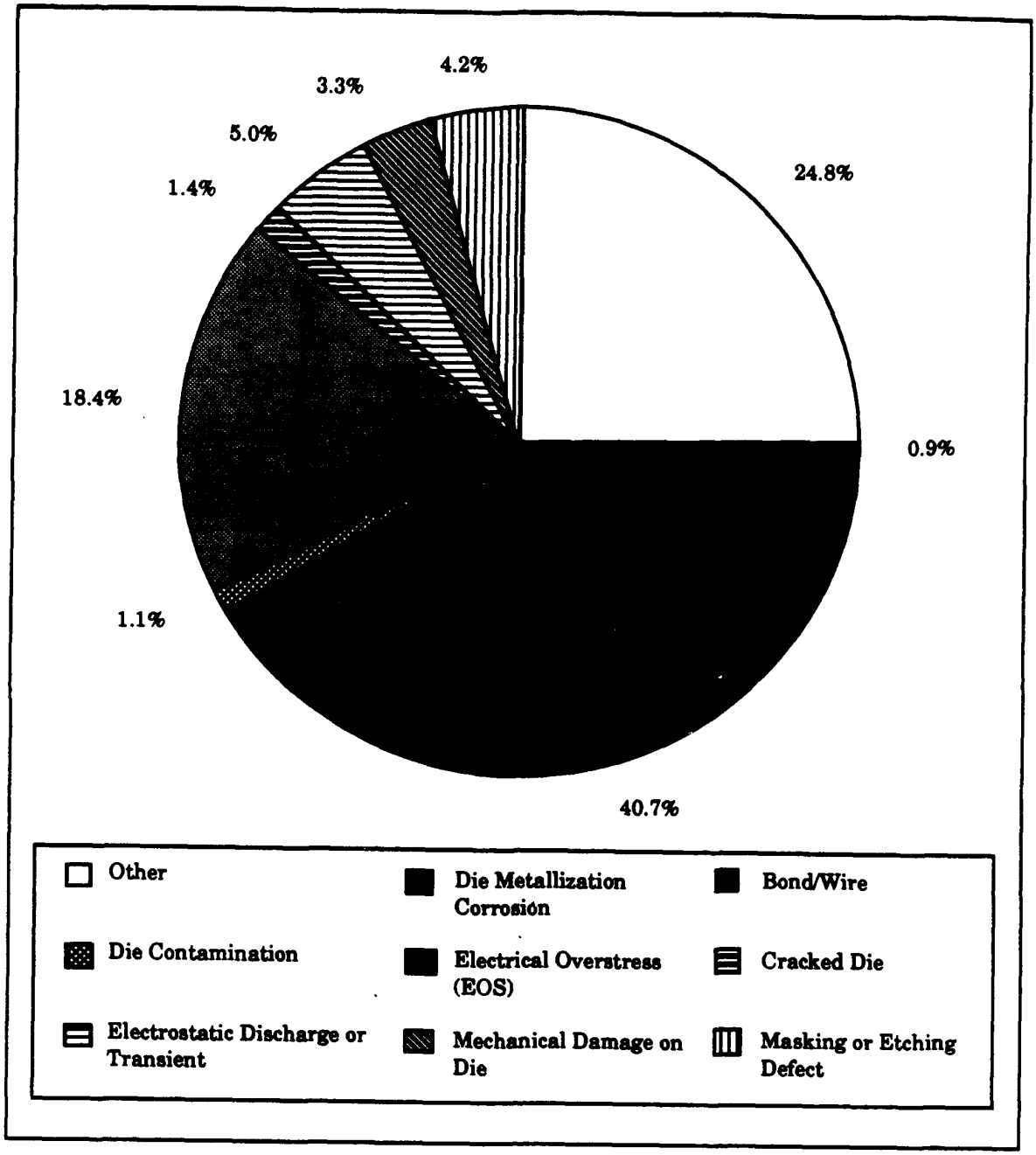


Figure 2: Failure Mechanisms Distribution

Straub, R.J., "Automotive Electronic IC Reliability," 1990 Custom IC Conference Proceedings.

2.4.1 Intermetallics

A traditional problem for plastic encapsulated ICs is the formation of intermetallic compounds at the interfaces of dissimilar metals. Plastic package technology utilizes gold wire bonded to aluminum bonding pads throughout the industry. Interfaces of Al and Au in the wire bond will form intermetallic compounds when exposed to high temperatures for a prolonged period due to the different mutual interdiffusion rates of gold and aluminum. The action of this mechanism is further enhanced by thermal cycling and moisture. Conceptually, the Arrehenius model is given by:

$$\text{Reaction Rate} \propto \exp(-E_a/KT)$$

where

E_a = activation energy (eV)

K = Boltzman's constant = 8.63×10^{-5} (eV/°K)

T = temperature (°K)

Under the assumption of the Arrehenius Model, every chemical reactions has a unique activation energy associated with it. Based on the results of almost ten (10) years of +125°C operating life testing, Motorola (Ref. 11) has developed the following specific Arrehenius equation to show the relationship between junction temperature and reliability:

$$(1) \quad T = (6.376 \bullet 10^{-9})e^{\left[\frac{11554.267}{273.15 + T_J}\right]}$$

where

T = Time in hours to 0.1% bond failure (1 failure per 1,000 bonds)

T_J = Device junction temperature, °C

and

$$(2) \quad T_J = T_A + P_D\theta J_A = T_A + \Delta T_J$$

where

T_J = Device junction temperature, °C

T_A = Ambient temperature, °C

P_D = Device power dissipation in watts

θ_{JA} = Device thermal resistance, junction to air, °C/watt

ΔT_J = Increase in junction temperature due to on-chip power dissipation

Activation energies between .8 to 1.4 have been reported in the literature. Table 3 shows the relationship between junction temperature, and continuous operating time to 0.1% bond failure, (1 failure per 1,000 bonds).

Table 3: Device Junction Temperature vs. Time to 0.1% Bond Failures

Junction Temperature (°C)	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

A host of catastrophic wirebond failures resulted from this mechanism. The failure mechanism became known as "Purple Plague" because of the presence of dark purple areas on the metallization surrounding the bond. This mechanism is associated with Kirkendall void formation at the bond/pad interface. This failure mechanism is increased by the presence of contaminants such as Bromine in flame retardant epoxies and residual chlorinated impurities.

This condition has not been considered a major problem for years due to such improvements as lower temperature assembly processes such as epoxy attachment of both die and substrate, however the only way to completely

eliminate the mechanism is to use a mono-metallic system, which is not available with plastic packages. However, Reference 12 reports the re-appearance of this mechanism in the industry, with examples and lists the following factors as leading to its reoccurrence:

- Tendency among manufacturers and users to disregard purple plague as a present day failure mechanism , forgetting that for purely thermodynamic reasons, intermetallics will always be formed when using the mixed metal system Al-Au...

- A neglect of the forgotten role of interface contamination...

- The use of epoxy attach arterials has led to the interesting suggestion that this is a source of contamination which enhances the intermetallic formation

- The presence of water in many of the plastics used for encapsulation, allowing hydrogen from the water to combine with oxygen along the bond interface and hence negate the latter's role in reducing the diffusion of the Al...

Conversations with reliability engineers at major IC manufacturers of PEMs, and examination of available data, confirm that intermetallic formation must be considered a primary failure mechanism for PEMs. Although this mechanism is under control within a specified temperature range, the manufacturer's curves for intermetallic formation must be consulted and compared with each individual mission profile with regard to temperature. If long exposure to high temperatures is essential, a monometallic system, provided in hermetic packages, will be essential for high reliability performance.

2.4.2 Moisture

Moisture related problems, ionic contamination and corrosion are also traditional failure mechanism of PEMs. Plastic packages are permeable to moisture because they are a retardant not a barrier. Moisture leachs impurities from the molding compound and carries contaminants from the packaging

surface to the die for moisture-related problems. In addition, moisture travels along the lead frame providing another path for impurities to the die. Figure 3 illustrates this process. The following advances in technology, often reported in the literature, have greatly improved moisture resistance by PEMs:

- Careful selection of materials for die attach and molding provide improved package integrity
- Molding characteristics such as:
  - low moisture adsorption compounds
  - low concentration of ionic impurities
  - low coefficient of thermal expansion
  - good adhesion properties
- Process cleanliness has been improved
- Passivation of the die with inert compounds such as silicon nitrides
- Chloride (Cl) content has been reduced during the manufacturing process
- Die planarization with spun-on-glass
- Phosphorous content of glassivation has also been reduced
- Lead-lock frames minimize separation of the plastic and the lead frame

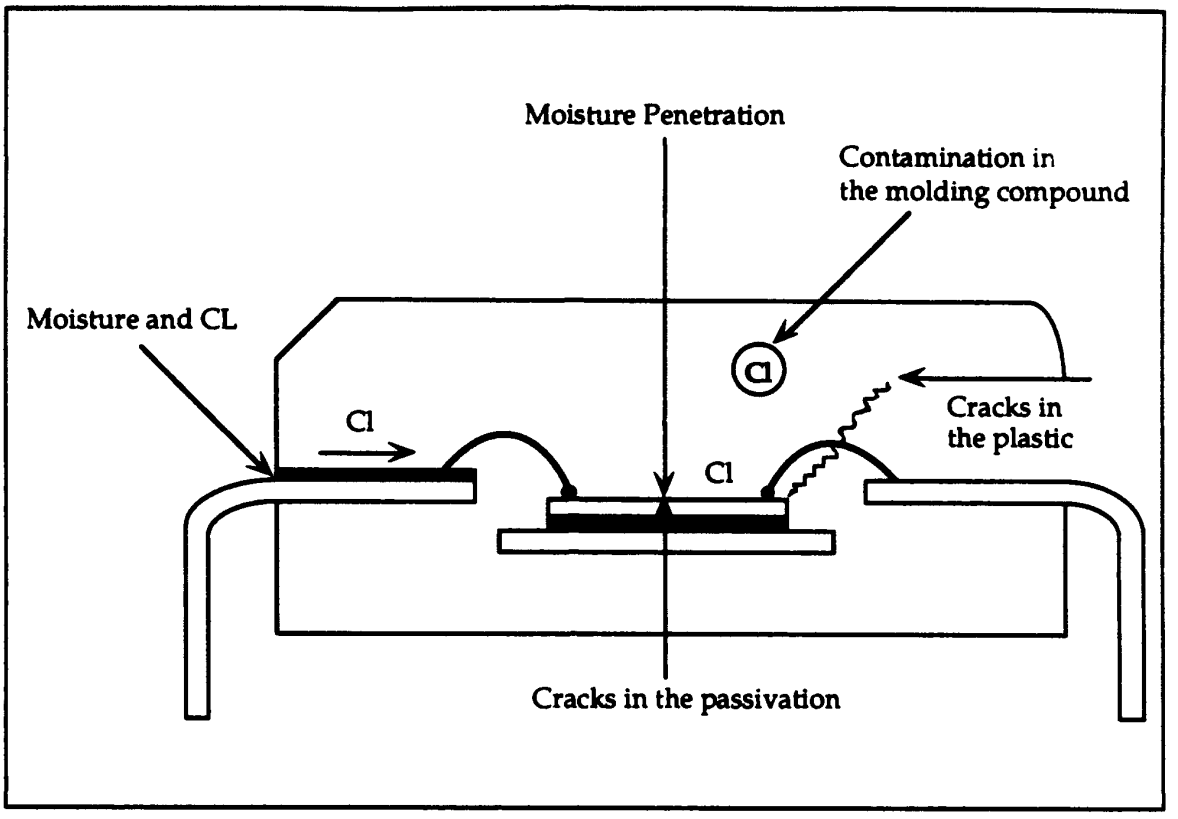


Figure 3: Mechanism of Moisture Related Problems

- **Cleaner die assembly processing**
- **Molding processes are improved resulting in better adherence to lead materials**

Figure 4 illustrates the results of these improvements for a major US IC manufacturer.

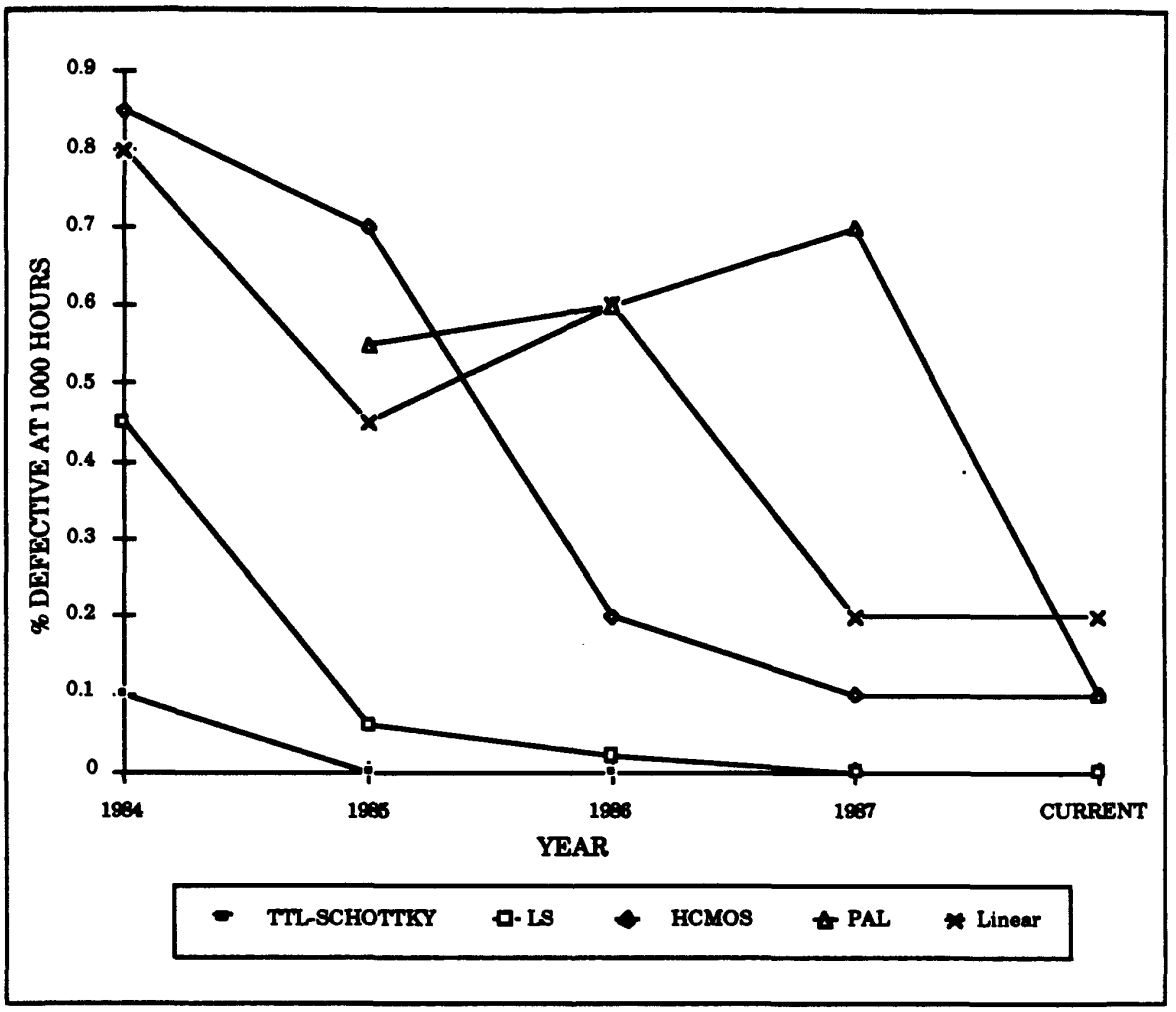


Figure 4: Moisture (85°C/85% RH) Performance of Plastic IC's for one Manufacturer 1984 to present

Condra, L., "Using Plastic-Packaged ICs in Avionics and Military Products," Technology Review Abstracts, 1991.

Despite all of these improvements, hermetic packages at the present remain the most reliable means of protecting an IC, provided the seal is intact, and no moisture is sealed in. The most frequent source of malfunction of semiconductors operating in a humid environment is electrochemical corrosion (Ref. 13). Hermetic packages protect the device from moisture intrusion and essentially eliminate corrosion failures.

Moisture, which permeates the plastic package, will transport impurities from the package surface, and leach impurities from the molding compound, causing electrochemical corrosion quickly once water and ionics reach the device metallization. Moisture can also degrade active devices. A defect-free passivation such as spun-on glass can protect the complete device, while a nitride passivation can protect all but the bonding pads and wires. However, if the passivation is cracked or has pinholes, permeation can occur. The basic conditions necessary for electrochemical corrosion is the presence of moisture, ionic contamination, and an electric field. With increasing integration, the interior metallization becomes finer, increasing the susceptibility to corrosion failure. Al metallization is even more prone to corrosion and chlorine contamination very significantly increases the rate of Al corrosion.

Several models describing the rate of degradation due to moisture are as follows:

(1) Peck (Bell Labs):

$$t = Ae^{(E_a/kT_a)}H^B$$

where

t	=	Time to 50% failure or mean time to failure
E_a	=	Thermal Activation Energy (eV)
T_a	=	Absolute temperature (°K)
K	=	Boltzman's Constant
H	=	Relative Humidity (%)
B	=	Constant

Peck, at the 1986 International Reliability Physics Symposium, after comparing all available literature, stated that he found excellent correlation between this equation and the data when he considered only corrosion failures. He later stated that he considered the best estimate of parameters B and E_a to be B = -2.66 and E_a = 0.81eV.

In 1978, Lycoudes of Motorola proposed a equation that added a voltage variable to Peck and Zierdt's expression, as follows:

(2) Lycoudes (Motorola):

$$t = Ae^{(E_a/kT_a)}\, e^{B/H_{E-1}}$$

where

E	=	Electric fields in the corrosion area
E_a	=	0.65 eV
B	=	304

Others, such as Lawson (British Telecom, 1984), Gunn (IBM, 1983), and others have proposed similar but different models that use Eyring Statistical Models to replace the basic Arrehenius Model generally used for temperature acceleration models.

The following model (Lawson) provides an acceleration factor for moisture and temperature. The basic form of the model is given by:

(3) Lawson:

$$t_m = t_0 \bullet \exp(C_T/T_a) \bullet \exp(-C_H \bullet H^2)$$

where

t	=	Median time to failure
t_0	=	Constant with dimension of time
T_a	=	Temperature in °K
C_T and C_H	=	Temperature and humidity constants
H	=	Relative humidity

Values of these constants have been reported for LSTTL[2].

$$C_T = 8.1 \cdot 10^3 \text{ (°K)}$$
$$C_H = 2.4 \cdot 10^{-4} \text{ (\%)}^{-2}$$

(4) Gunn (IBM):

$$R(T,RH,V) = V \cdot \exp\left[\frac{\Delta H}{kT}\right] \cdot \exp \beta(RH^{-1})$$

where

β	=	Humidity constant (%RH)
ΔH	=	Activation energy (electron volts)
RH	=	Relative Humidity (%)
k	=	Boltzman's constant
T	=	Temperature (°K)
V	=	Voltage (volts)

Reported activation energies range from .75 to 1.02 for chloride contamination and .3 for phosphorous. In systems predominantly in operation, the moisture induced failure mechanisms are reduced. Self heating of the components is an active protection against moisture because the relative humidity, which decreases as temperature increases, is the dominant parameter in moisture-induced failures (Ref. 14). A very careful analysis of operating conditions is necessary in the case of intermittent operation, however. Reference 14 concludes that:

> *MOISTURE induced failures in advanced plastic-encapsulated components are as infrequent as for ceramic packages with cavities if a chip excess temperature of 20°C is maintained compared to ambient temperature of the rack.*

The same benefits can not be expected in storage or intermittent operation. In storage, moisture can penetrate the package and when voltage is applied, failures will occur.

The Air Force is sponsoring an initiative to develop what is referred to as hermetic-equivalent packaging. "Hermetic-equivalent" packaging has attributes of both hermetic and non-hermetic approaches. Dense, inorganic materials (i.e, SPEC) are applied directly to the IC surface as a protective barrier. Similar to hermetic packages, chip protection is based upon preventing moisture and contaminants from passing through the barrier layer to the chip. Like traditional non-hermetic packages, however, these coatings do not have a cavity. Thus, MIL-STD-883 tests for seal and internal water vapor are not applicable. Additionally the initiative will develop and demonstrate a hermeticity equivalence test procedure. Guidelines targeted for assuring the integrity of packaging approaches utilizing surface coating materials to provide a moisture and ionic barrier is forthcoming.

An industry consortium, the IEEE Gel Task Force evaluated the reliability of silicon gel encapsulated devices in harsh environments and compared results with hermetically packaged devices. The silicon gel works by the attachment of the ends of the long chain silicone molecules to the surface of the silicon. If the resultant dense forest of molecules is tightly arrayed, no pools of water or water-filled voids would be formed. If there are no such water-filled voids, there would be no place for water to dissolve corrosive ions. If dense silicone molecules are attached everywhere to the chip surface, no water could collect, and no large size ions could penetrate (Ref. 15). The overall thrust of the Task Force was to determine whether a thin coating of silicone gel on the surface of the semiconductor chip would provide corrosion protection equal to a hermetically sealed package. The test sequence consisted of thermal shock, salt spray, and biased autoclave. Rome Laboratory failure analysis on these parts showed that corrosion of the die bond pads and metallization occurred even with the gel coatings. Pinholes in the primary passivation caused the gel to tent over and allow moisture to condense. The results reported in Reference 16 were that there were no hermetic failures and that none of the gel coated devices matched the performance of the hermetic devices.

The following summarize the final results of the task force:

- Gels should have quite low viscosity during application, and either be very thin or very soft in the cured state so that they do not exert destructive force on wire bonds
- An inorganic coating before gel application seems necessary to enhance the protection needed to survive testing
- If appropriate materials are applied properly, silicone gel coatings can be an alternate means of die protection instead of hermetic ceramic packages
- Some silicone gels afford corrosion protection
- Gel coatings can withstand forces up to 15,000g
- Thermal shock followed by salt spray followed by HAST can be used to test any coating for corrosion protection
- It seems possible to formulate and apply gel coatings to avoid wire bond breaks
- TAB bonding with its stronger leads might be particularly suitable for gel coatings
- A clean surface is essential to success

Other references (16, 17, 18, 19) have claimed success with silicon gels, and interest in this area is expected to continue.

The USAF's Wright Laboratory (WL) has awarded a four year contract to Microelectronics and Computer Technology Corporation (MCC) for the Reliability without Hermeticity (RwoH) project. This contract will expand on the work begun by an industry consortium including MCC, Lehigh University, and 20 commercial organizations, including IITRI/RAC who has been added to the team

to develop and coordinate the test plan. Support from the private sector is expected to continue. National Semiconductor in another WL contract is investigating the Dow Corning in-organic (SPEC) coating. Military organizations participating include: Army ETDL/LABCOM, Naval Weapons Support Center, USAF Rome Laboratory, and Sandia National Laboratories.

The RwoH mission is:

To advance US competitiveness by implementing electronic environmental protection technology which permits the replacement of classical hermetic packaging and enhances performance and reliability. (Ref. 20).

The program objectives are:

- To promote, demonstrate and obtain acceptance of non-hermetic electronic packaging technology for both commercial and military programs.
- To encourage the development of a common test methodology for qualifying non-hermetic electronic packaging.
- To provide fundamental understanding and technical guidance for advanced non-hermetic electronic packaging technology.
- To establish a replicable coating, processing and testing capability to qualify surface environmental protection systems.
- To promote the development of North American sources of materials

The US Army Armament, Munitions, and Chemical Command at Picatinny Arsenal in New Jersey (Contract DAA21-86-C-0043) sponsored a study to determine if EP/TAB (Environmentally Protected TAB) IC packaging could be a

viable alternative for hermetically sealed, integrated circuit packages presently used in military systems (Ref. 4).

Tape Automated Bonding (TAB) provides the following advantages:

- Component is testable compared to the free chip
- Repairs are easy through desoldering the component
- Transfer of the component to the substrate is easy to automate

The EP/TAB IC packaging configuration replaces the traditional hermetically sealed enclosure with a passivation and barrier layer metals and gold bumps which isolate susceptible portions of this device from the environment. The study was conducted by Honeywell (now Alliant Technology), Hopkins, Minnesota, and IIT Research Institute, Rome, NY, where bipolar and CMOS ICs were tested in both EP/TAB and hermetically sealed packages. Environmental tests were configured to verify that EP/TAB ICs could withstand prolonged exposure to hostile environments. Testing included salt atmosphere, 1100 temperature cycles, 90 cycles of thermal shock, moisture resistance, high temperature storage (no bias), humidity life (biased), low temperature storage (no bias), mechanical vibration, and mechanical shock (hot and cold). Preliminary results of the program are presented in Reference 4 and are:

- There was no evidence of corrosion observed on any of the EP/TAB ICs.
- There was no evidence of metal migration or metal whisker growth observed at the inter-lead-bonds on the EP/TAB ICs.
- The EP/TAB IC failures were the result of copper TAB leads. The open leads resulted from flexure fatigue of the copper leads after extended temperature and mechanical cycling.
- Shifts were observed in the electrical parameters of both the EP/TAB and LCC-packaged bipolar IE integrated circuits. The

electrical shifts occurred after 1000 hours of exposure to 85°C and 85% relative humidity. The electrical shifts were due to moisture penetration through the epoxy potting material. The moisture provided a current leakage path between the external leads of the test vehicle.

- The LCC-packaged integrated circuit failures were the result of solder fatigue at the lead-to-porcelain-coated-steel-board interface. This was the result of a thermal coefficient of expansion mismatch between the printed wire board and the ceramic LCC. The solder joint failures could be reduced significantly and possibly eliminated by using LCC packages with leads brazed to the top of the package rather than the bottom.

- A significant number of cracks was observed in the epoxy potting material of the test vehicle. Cracks occurred throughout the environmental testing. The cracks had a significant effect on the LCC-packaged integrated circuits and a very small effect on the EP/TAB IC.

  System operating conditions such as cycling rates, temperature, relative humidity and electric fields must be considered based upon all available data and information to properly assess the potential effects of these mechanisms for each application.

- The final step in implementing the EP/TAB IC technology into military systems requires the development of a reliability model and military specification for qualification testing and process control. The Product Assurance Group of Armament Research, Development and Engineering Center (ARDEC) at Picatinny Arsenal and IIT Research Institute/Reliability Analysis Center have developed the following:

  1. An EP/TAB IC reliability model for incorporation in the reliability handbook, MIL-HDBK-217.

2. An EP/TAB IC qualification specification which covers both the device qualification test methods and EP/TAB device-level-specific process controls. These requirements were used to prepare a draft amendment to MIL-I-38535A.

This specification establishes the general requirements for evaluating and qualifying the manufacturing processes used to produce unpackaged EP/TAB integrated circuits and specifies the quality and reliability assurance requirements to be met in the acquisition of such devices. Detail requirements, specific characteristics and other provisions which are sensitive to the particular use intended will be specified in the applicable device specification. This specification will be used to evaluate and qualify materials, processes, process controls and process stability used in the design and fabrication of wafers, gold bumping, inner lead bonding to tape and mounting on to singulated tape slide carriers, to achieve the prescribed level of quality and reliability. A single level of product assurance (including Radiation Hardness Assurance (RHA) if applicable) is provided for in this specification. This specification identifies additional test conditions and methods to be performed to satisfy process qualification, screening and quality conformance inspection of EP/TAB integrated circuits.

3. An EP/TAB IC board-level assembly qualification specification.

This specification establishes the general requirements for printed wiring assemblies (PWA) containing EP/TAB integrated circuits intended for U.S. Army munitions applications. It governs and provides general provisions for qualifying the processes used in their manufacture, the in-line process controls and quality assurance provisions necessary to assure that the printed wiring assembly processes do not adversely impact the inherent reliability properties of the EP/TAB integrated circuits used therein. Detail requirements, specific electrical and physical characteristics and other provisions which are sensitive

to the intended use shall be specified in the applicable detail PWA acquisition specification.

A paper prepared by working group 3, Assemblies and Miscellaneous Parts, of the Electronic/Electrical Parts Sub-Group of the Group on Standardization of Materiel and Engineering Practices (Ref. 21) summarizes the relation of Plastics to TAB as follows:

> *In general, it has been suggested that only the chip needs to be hermetic since no polymer meets the total requirements of a hermetic package. One method of achieving this might be to implement tape automated bonding (TAB). The die could be passivated with compressed silicon nitride, which if done properly should be impervious to moisture. In the TAB process, the reactive aluminum metallization at the bond pad openings would be covered with several layers of metal including an adhesion layer, a diffusion barrier, and an inert bonding layer. The critical areas of the chip would not be directly exposed to either moisture or contaminants. One difficulty with this proposal is that the transfer molding and TAB processes need further development in order to work well together. Injection molding Appears to be easily adapted to TAB. However, injection molding is relatively new to the encapsulation of electronic components and is normally used for thermoplastics rather than thermosets such as epoxy novolacs. It is likely these obstacles will soon be overcome. Another advantage to the TAB process is elimination of the wire bond problems including wire sweep, intermetallic failures, and wire shear.*

2.4.3 Thermal Mismatch

Thermal Coefficient of Expansion (TCE) mismatch problems have been identified by major PEM manufacturers as recently as this year (Ref. 22). In large die, stress-related passivation cracking, aluminum sliding, or poly cracking have been identified predominantly during temperature cycling. With the trend of integration continuing upward, with larger size dies and even finer

patterns, the problem is one which will continue to be addressed in the future. These occur as a result of the intimate interaction of the die surface and the molding compound due to mismatches in TCE between materials. Damage sites include:

- Delamination
- Chip cracking
- Cracks in the package
- Cleavage of wire bonding
- Passivation cracks
- Deformation and sliding of the metallization
- Polysilicon cracks

Cracking generally occurs near the corners of the chip. Resulting failure modes include functional failures, shorts, leakage, or opens.

Reference 22, by Foehringer, et al, of Intel Corporation, tabulated data on several plastic products to investigate this problem area. Four main factors including layout style, materials, die thickness and passivation type were investigated as to their impact on thin film cracking. Of the key variables examined, the layout style had the most influence on thin film cracking during thermal cycling. Thinner die and planarized passivation provided moderate improvements. Characterization of packaging materials was incomplete and not conclusive, and die size influences were not found to be significant, probably since results were dominated by other factors.

Reference 23 identified the following as contributors to this mechanism:

- **Die Topography**

  a) Number of metal and other interconnecting layers

  b) Interconnection metal hardness

  c) Strength of interlayer dielectrics

  d) Strength of protecting passivation layers

  e) Vertical height of overall topography

- **Die Layout**

  a) Relative proximity of metal interconnects to corners and edges of die

  b) Total area of interconnect "freeboard" around die periphery (including scribe line)

  c) Number and angle of crossover interconnects at or near die corners

  d) Relative distance to bonding pads from die corners

- **Die Size**

  Package stress increases exponentially from the package center along a radius line to the die corner. The longer the diagonal, the greater the stress.

- **Plastic Encapsulating Material/Assembly Processes**

  a) Residual stress of the plastic (in compression, as a function of ambient temperature)

  b) Adhesion of the plastic material to die and lead frame

  Because the damage to the die is fatigue related, the relative movement of the molding compound to the die surface is critical to the onset of damage, relative to any given die technology. We have learned that the level of delamination of the plastic to the die surface provides a clear correlation to the onset of fatigue related damage.

That paper also suggests that the greatest improvement to reduce thin film cracking can be gained by locating critical circuitry away from the die corners and filling the corner of the die with sacrificial anchoring structures. Modest improvements can be gained by thinning the die and using planarized passivation.

Plastic encapsulated moisture reliability is contingent on good passivation integrity. Planarizing the passivation with an intermediate Spin-On-Glass (SOG) layer was shown by Gaeta and Wu of Intel (Ref. 43) to reduce the long term steam failure rate by 3X and thus improve moisture performance.

Innovative low stress epoxies have been presented in the literature (Ref. 24, 25) for large and stress sensitive devices. These epoxies have a lower Young's Modulus and thermal coefficient of expansion. Other improvements include increased passivation strength, increased metallization hardness and changes in layout ground rules.

Reference 25 describes a method of screening these new plastics and quantifying the improvements in terms of device yield and performance. The method involves temperature cycling molded packages containing unpassivated test chips. The results of this particular study found several of the newer low stress epoxies gave metal deformation equal to or greater than the standard

formulations. Reference 24 investigates the effectiveness of both thermal shock and thermal cycling in the qualification of a package. A test chip using an all projection mask N-well CMOS process was used to compare thin film cracking and wire ball shear. Failure rates related to these failure mechanisms were found to have different dependence on thermal shock versus thermal cycling, and on lead frame material. One observation of this study is that thermal shock is far more complex than thermal cycling. Thermal shock introduces a failure mechanism not observed in thermal cycling which consisted of passivation cracking occurring with equal probability anywhere on the die. Corner passivation cracking was suppressed in thermal shock relative to thermal cycling for devices with Alloy 42 lead frames, but not for devices with copper lead frames. The authors conclude that thermal shock cannot be regarded as simply an acceleration of thermal cycling, and both are necessary to expose all failure mechanisms.

The dependence of thin film cracking and wire/bond failures on extended temperature cycling and thermal shock were also studied experimentally in Reference 44. Significant numbers of failures were generated after about 100 cycles of -55°C to 125°C temperature cycling. Failure modes included thin film cracking and bond shearing fracture, predominantly at the corners of a 252 mil x 252 mil die. It was noted that failed bonds exhibited resistances between 10 and 100 ohms. After decapsulation, zero pull strength was often observed due to fractures in the silicon beneath the bond pad. A "healing" phenomena which had sometimes been observed before decapsulation was thought to be related to mechanical movement re-establishing contact of fractured pieces held in close proximity by the encapsulant. Measurements of bond continuity with temperature excursions to detect intermittency (and bonds which remained "healed" at the test temperature) were not done in this study.

Koch, et. al. (Reference 45) discuss a PEM reliability improvement study which directly relates certain design and processing parameters to bond integrity in PEMs. They found that 1μm silicon precipitates in the aluminum metallization (required to control contact spiking during sintering) acted as stress points beneath gold ball bonds during bonding over dense PSG passivation. These stress points resulted in 1 micron pits extending 0.2 to 0.5 microns into the PSG. Large

area fractures which often extended into the silicon were found to be initiated at these pits in the PSG. These fractures resulted in intermittent bond continuity failures after molding and during reliability testing. They also studied plastic material flow and curing profiles during molding due to flow dynamics and temperature profiles. Basically, the material entering the cavity last flowed to the opposite end of the cavity and was heated by the exothermic reaction of curing material it flowed by. This apparently caused faster curing and more viscous material impacting on the bonds at the far side which failed much more often than those at the entry side. Removing the PSG beneath the pads and careful study and control of molding parameters were found to mitigate this problem.

Finite Element Analysis has been a major player in the reliability improvement of PEMs since it has been used to model the thermal and mechanical gradients in the package structure. The mechanical stresses due to TCE mismatch are modeled, resulting in better designs. This method has been extensively used to model and evaluate stress distribution in plastic, die and lead frame. Model parameters include resin material, lead frame material, adhesion between lead frame and plastic and others. Improvements resulting from this method include lead frames with lead locks, long humidity ingress paths, and end stress relief holes; and a package design with equal amounts of plastic on top of the chip and below the lead frame, minimizing cracking during temperature cycling.

With the increasing integration of circuits, power dissipation becomes and will continue to become a major reliability issue. In general, for similar pin counts, the package thermal resistance of ceramic packages is approximately half of that for a plastic package (Ref. 26). Toward this end, Reference 26 describes a heat spreader of SiC on graphite for Si chips. θ_{JA} reductions of 50% were reported for VLSI chips dissipating .5 watts.

2.4.4 SMT

Surface Mount Technology (SMT) is in major use today. A relatively new failure mechanism of PEMs is cracking of surface mount packages after exposure to moisture and elevated soldering temperatures during the board assembly process. The mechanism is described as follows:

> *Moisture inside that package vaporized and expands rapidly during elevated temperatures (220°C) such as vapor phase soldering or infrared soldering, or , if the package is submerged in molten solder, in wave soldering. The force resulting can cause package delamination, internal cracks, bond damage, or cratering beneath the bonds. In severe cases, external package cracks occur. This is commonly referred to as the "popcorn effect" due to the audible "pop" the package makes as it cracks. A TCE mismatch will also contribute to this problem, since the Tg for epoxy novolac (140-160°C) is less than the solder reflow temperatures. Moisture and contaminants then provided a clear path to the die. Figure 5 illustrates this mechanism.*

Surface mount devices are more susceptible to this phenomena because of the smaller minimum package thickness from the chip or mount pad interface to the outside package surface. JEDEC Test Method A112 "Moisture Induced Stress Sensitivity for Plastic Surface Mount Devices," presents a test method to identify plastic surface mount devices which are sensitive to this form of failure so that they can be properly packaged, stored, and handled to avoid subsequent damage. A preconditioning procedure must also be developed and used to determine device/manufacturing process compatibility.

Reference 27, "Recommended Procedures for Handling of Moisture Sensitive Plastic IC Packages," IPC Standard IPC-SM-786, dated 1990 is an extensive and most complete reference on this topic. The standard covers:

- Package types affected

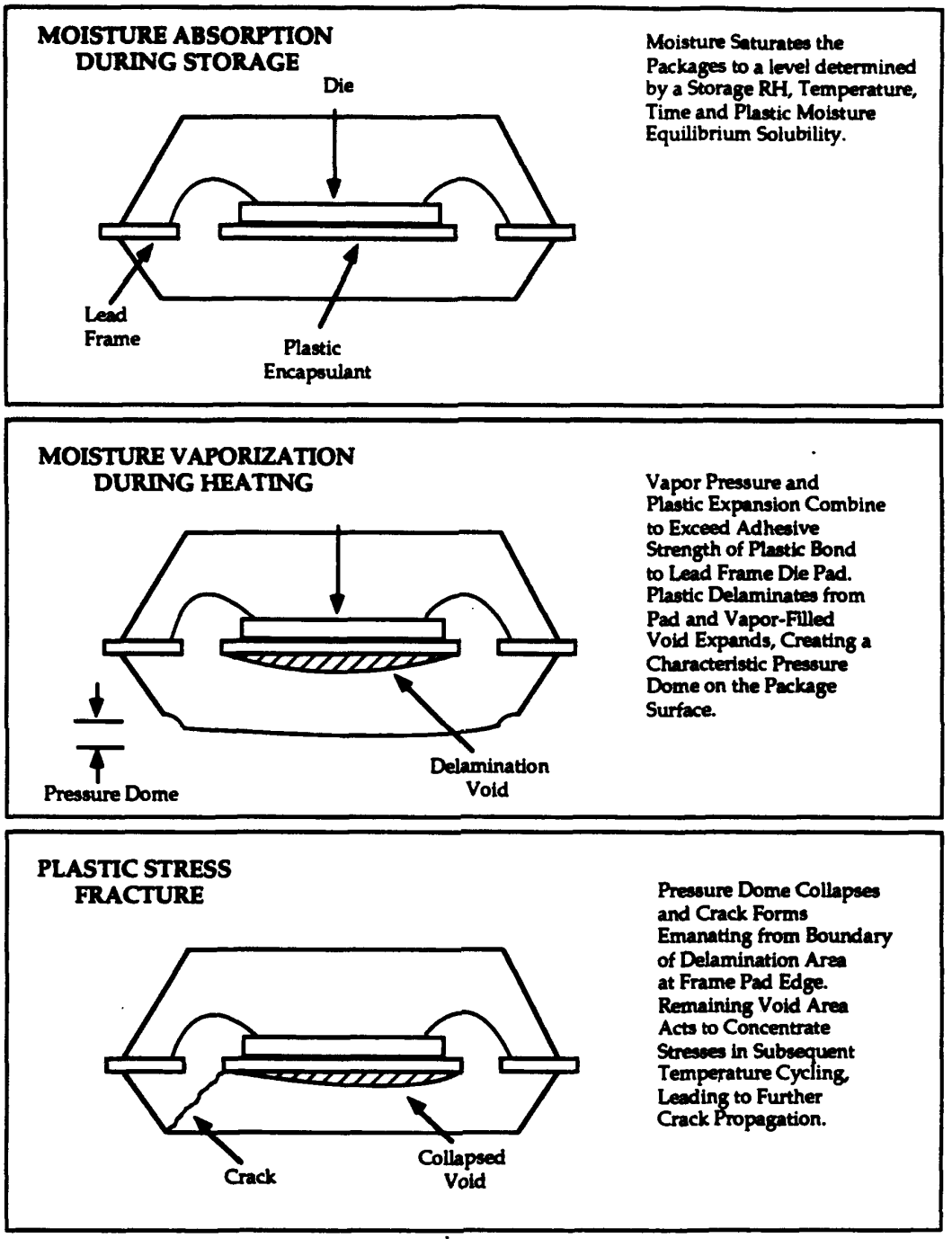


Figure 5: Plastic SMT Package Crack Mechanism

IPC Standard ANSI/IPC-SM-786, December 1990, p. 4.

- Variables that influence the failure mechanism
- Solutions to the problem
- Recommendations

Both C-Sam and Slam have been reported (Ref. 28) as extremely effective for inspection of internal package cracking.

The long term solutions to this problem are still being investigated and include improved molding compounds and lead frame designs. Presently manufacturers (Ref. 2) are providing dry packing for surface mount devices susceptible to cracking. Dry packaging consists of sealed vapor barrier bag with a desiccant. The bag may also specify a shelf life of the contained device based upon 55°C and 85% RH (worst case conditions) and will identify the parts as moisture sensitive.

2.4.5 Filler Induced Stress Effects

References 46 and 47 review a failure mechanism which is related to solid filler particles used in some plastic encapsulant compounds. It was found that the sharp edges and points of some filler particles touch the die surface. Both curing and aging cause the volume of the plastic to decrease and this results in increased stress in the silicon at the die surface, concentrated at those edges and points. The increased stress was found to result in increased junction leakage current and this in turn caused failures in certain DRAM sense amplifier circuits. High temperature storage tests were done at 125°C and above and it was found that 50% of the DRAMS failed at the time corresponding to 0.5% volume shrinkage of the encapsulant. The problem was cured by using a 2 micron particle free layer or by grinding the particles to less than five microns.

2.5 PEM Reliability Data

Failure rate and lifetime are two very different measures of reliability. The failure rate implies a random occurrence of failures and is a measure of the reliability of a part within its useful life. Failure mechanisms exhibiting this

randomness typically are manufacturing defect related mechanisms occurring in a relatively small percentage of the part population. These mechanisms are sometimes referred to a "special cause." The useful life of a part is a measure of the life time under a given set of conditions. Failure mechanisms which limit the life time of a part typically can affect the entire population of parts and are referred to as "common cause."

Much of the discussion and data in this document has focused on common cause type mechanisms. While the control of each mechanism is very important to insure that parts will operate reliably for a given period of time in specific applications, knowledge of a parts lifetime will provide very little information of the failure rate during its useful life.

The intent of this section is to present failure rate data collected by RAC on plastic encapsulated microcircuits. Since the data is representative of the first year of part operation, it will provide information on the failure rate during the early life of the part and will not provide end of life estimates. There are two sources of data provided;

1. A failure rate model for plastic microcircuits developed from field data on automotive electronics

2. Observed failure rates of PEMs over a 10 year time period from commercial equipment in ground applications.

2.5.1 Automotive PEM Failure Rate Model

An effort has been undertaken by the Society of Automotive Engineers (SAE) Reliability Standards committee to develop a reliability prediction methodology based solely on empirical data taken from automobile manufacturers and OEM warranty records. While the scope of that effort was for all electronic components, this section of the document only discusses the model developed for PEMs. Failure rate data was extracted from the warranty records and submitted to the RAC for data analysis and failure rate model development. Multiple linear regression was used to quantify parameters in a multiplicative model form. Several iterations of this process were necessary to insure only those variables

which are observed do significantly affect PEM field reliability. Reference 37 provides a more detailed discussion of the model development process and presents models for other electronic component types.

The failure rate model developed in that effort, as it appears in Ref. 37, is as follows,

$$\lambda_p = \lambda_b \pi_F \pi_S \pi_p \pi_T$$

where

π_p = predicted microcircuit failure rate (failures per 100 parts per 400 hours)

λ_b = microcircuit base failure rate

= .0038 Digital (.0016, .0140)

= .00023 Linear ($1.16 \cdot 10^{-5}$, .0046)

= .0038 Microprocessor (.0016, .0140)

π_F = Microcircuit family factor

= 1.00 MOS

= 1.62 Bipolar (.66, 3.96)

π_S = Screen factor

= 1.00 electrical and environmental

= 1.00 electrical

= 8.57 no screening (1.13, 64.71)

π_p = Module packaging factor

= 1.00 encapsulated

= 5.81 exposed (2.18, 15.46)

π_T = Temperature factor (given in Table 2 and 3)

$$= \exp\left(-A\left(\frac{1}{273 + T_j} - \frac{1}{287}\right)\right)$$

where

A = activation energy/Boltzman's constant (Ea/K)

= 4600, digital bipolar (Ea = .4)

= 8100, digital MOS (Ea = .7)

= 10400, linear bipolar (Ea = .9)

= 8100 microprocessor (MOS) (Ea = .7)

T_j = device junction temperature

= $T_A + \theta_{JC} P$

where

θ_{JC} = junction case thermal resistance

P = applied power

Several points should be noted when interpreting this model;

1. The failure rate units are failures per 100 components per year (400 operating hours), or failures per 40,000 operating hours. To convert to failures per 10^6 hours, multiply the predicted failure rate by 25. This failure rate was chosen since a typical automobile is operated for approximately 400 hours per year. It should also be noted that while it is an operating failure rate, it essentially includes dormant failures and therefore essentially predicts the number of failures per 100 components per year. To convert to FITS, multiply by 25,000 on to convert to %/1,000 hours, multiply by .0025.

2. The 95% confidence intervals are given in parenthesis for each factor, the R^2 value was .37 and the probability of F to enter was .3.

3. While it seems intuitive that there be a factor for the vehicle location (engine compartment, instrument panel, etc.), the data did not indicate that it is a statistically significant variable. However, since there was a correlation between quality (screening) level and environment, it was not possible to accurately quantify the effects of both. Therefore, only the effect of screening (quality) is included in the model and this factor inherently includes some location effects.

4. Although this model represents the most current effort by the SAE's committee, it was based on data collected in the 1982-1986 time period and is therefore representative of devices of that period.

2.5.2 Commercial PEM Data

RAC has collected a significant quantity of field failure rate data from various commercial and military sources. This section of the document presents a summary of one commercial source for which the devices are predominantly PEMs, although there is also a significant amount of data in the same source on hermetically packaged devices.

Figure 6 illustrate the observed failure rate over the ten year time period 1978 to 1988 for both PEM's and hermetic devices.

The database used to derive this data is from first year warranty data on commercial equipment operating primarily in ground based applications. These applications are primarily office and laboratory along with some transportable equipment.

Failure rate observances are for the same part (or part function) over time. For example, only those part numbers in the 84-88 data were used when they also appeared in the '78 - '84 data.

Over the ten year period of '78 - '88 there appears to be an order of magnitude improvement in both hermetic and nonhermetic devices. The data used is from first year warranty data and suggests that the early life failure rate has decreased by a factor of 10 over the period '78 - '88.

Similar trends have been observed by others collecting this kind of data. Additionally, there currently appears to be a very consistent value of failure rate between the various sources of data on plastic encapsulated microcircuits. This value is approximately .02 Failure/10^6 hours. It must be emphasized however that this failure rate is applicable to the ground application, early life situation discussed previously.

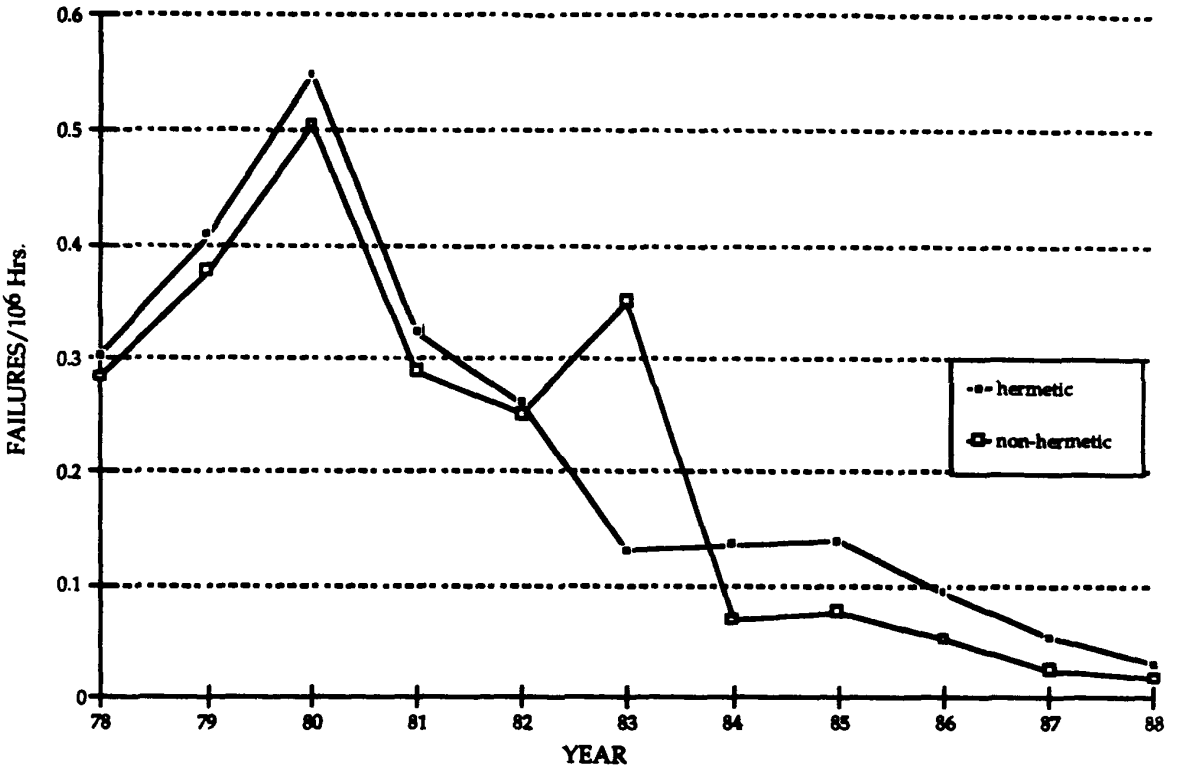


Figure 6: IC Failure Rate as a Function of Year

Earlier studies on plastic microcircuits have indicated that the variability in failure rates was much greater due primarily to the variation of encapsulant materials and vendors. This observed corroboration of failure rate data between several sources would seem to indicate that this variability has lessened. However, although the average failure rate for the various sources are similar, they are also based on the averaging of many different component types. The observed failure rates for specific PEM's still can vary significantly. Some of this variation is undoubtedly due to non-component failures such as design related problems.

The data appears to indicate that the average failure rates of hermetic and plastic devices are very close over the period 1978 to 1988. While the large increase in reliability predicted by many has occurred for PEM's, over this time frame, it appears that it has also occurred hermetic parts. However, the precise environments for each are not known and it is possible that the environment is more severe for the hermetic parts.

Unfortunately, the failure/data reported can typically not be traced back to its root cause, and hence failure causes cannot be traced to the package. The trend however has been that the failure rate related to the die has decreased over the last several years so that the percentage of all failures relating to the package has increased.

Based on this data, there is reason to believe that PEM's have the potential to operate very reliably, in their early life. However, the long term reliability of plastic IC's has not been established empirically, since all PEM data available has been from the parts early life.

2.6 Test and Evaluation

A critical player in moving into a new technology area, or expanding the applicability of one, such as non-hermetic packaging is the screening, qualification and in-process testing to assure reliability.

Die sizes and increased complexity of IC's have introduced new concerns in the reliability of plastic packages which have been discussed in the previous sections. Procedures for the identification of defects within a intact PEM have not been fully established. Traditional methods to inspection of plastic packages for defects, including X-ray radiography and cross-sectioning have significant limitations (Ref. 13).

Sonoscan, Inc., Bensenville, IL reports (Ref. 29) on their employment of Acoustic Microscopic Technologies (AMT) to characterize naturally occurring cracks, disbonds, and voids in PEMs. Acoustic Microscopy is a non-destructive method for locating internal flaws with high frequency, high resolution ultrasonic imaging. Two types of AMT are discussed: Scanning Laser Acoustic Microscopy (SLAM) and C-Mode Scanning Acoustic Microscopy (C-SAM).

With SLAM, a plane wave of ultrasound is passed through a PEM. Variations in the transmitted sound waves are then detected by a scanning laser beam on the other side of the sample. Air gaps within the sample block the transition from reaching the detector and will appear as dark areas in the transmitted image. SLAM's value is in determining that a defect exists, and is used by

manufacturers solely for quality control. The real time imaging capability of this technique lends it well to production line screening.

C-SAM operates in a reflection mode. A rapid mechanical scanner moves a pulse-echo transducer, which alternately transmits and receives ultrasound, over the area of interest and focuses on specific depths within the sample, thereby providing a depth-dependent profile of defects. C-SAM is geared toward analysis of defects because of its capability of imaging a PEM a slice at a time.

These techniques are being used by manufacturers to determine the effects of a particular manufacturing process or process change on the integrity of the package. They can also be used for lower volume screening applications. End users are employing the techniques to spot incoming defective parts.

Quality testing of devices for corrosion resistance has traditionally been 85°C and 85% Relative Humidity at ambient pressure testing i.e., JEDEC Standard A101. This testing has become too slow and impractical to determine the reliability of advanced IC's using ever improving materials. Typically, these tests must be performed for a minimum of 1000 hours, which necessitates a testing cycle of several weeks. Moreso, manufacturers are striving to improve their products, which can require as much as 5000 hours of 85/85 testing to ensure the desired quality level. This creates problems such as overly extended lead times, and increased costs.

A relatively new technique for quality testing is becoming rapidly adopted in response to these problems. Highly Accelerated Stress Testing (HAST) exposes IC's to high temperature and humidity under pressure. This method has been investigated by IBM, Intel, Hewlett-Packard, Sandia Labs, National Semiconductor, Xerox, AT&T, Allen Bradley, and many Japanese firms. JEDEC standard A110 describes a number of different temperature settings under which HAST testing can be performed. For example, HAST testing at 110 C can reduce the test time from 1000 as in 85/85 testing to 200 hours. Table 4 shows sample test times for various HAST temperatures per JEDEC A110. Several papers (Ref. 29, 30, 31, 32, 33) have investigated the correlation between 85/85 and HAST testing. A HAST test method should be coordinated for inclusion in MIL-STD-883.

HAST results exhibit two distinct failure regions. The early life failures are mainly caused by passivation defects, and process capability failures. The early life failures, which must be removed from the product during screening have reported acceleration factors from 30X to 100X when compared to 85/85 results. The intrinsic failure rate region, which should be used for qualification testing, shows HAST acceleration factors in the 30X to 60X region. These acceleration factors vary with RH and temperature, and device maturity and technology. Experimentation done by Intel, at two independent locations confirms the work of D.S. Peck (Ref. 12) and others, showing HAST to be an excellent evaluation tool for non-hermetic packaging. In all of the work published on HAST, no failure modes or mechanisms were found that did not exist in 85/85 tests for molded devices. Reference 33 determines that since there are several different mechanisms for device corrosion, such as Cl corrosion, P corrosion, etc., that there should not be expected to be a single correlation factor between 85/85 and HAST, but that the acceleration factors will be process and device dependent.

Investigation into the development of a MIL-STD-883 HAST test method, and HAST acceleration factors are currently on-going as part of the USAF Wright Laboratory's contract to Microelectronics and Computer Technology Corporation's (MCC) to operate the Reliability without Hermeticity (RwoH) program.

Table 4: HAST and 85/85 Test Time Comparisons

Test Parameters	Test Method				
	85/85 (JEDEC A101)	HAST (JEDEC A110)			
Temp. (°C)	85	110	120	130	140
Test Time (hr.)	1,000	200	100	50	25

Efforts continue in the area of test and evaluation techniques for PEMs. Such techniques may be the key to the acceptance of PEMs for critical applications.

3.0 SUMMARY

The potential for new applications of improved PEMs should be considered based on the evaluation of past and ongoing efforts to improve their materials and processing techniques and the development of improved test and evaluation procedures. The following summary is offered:

1. Plastic ICs are not as resistant as ceramic packaged ICs to moisture, operating temperature stress and thermal cycling, however, both have greatly improved and continue to improve. The applicability of PEMs for any product or equipment must be evaluated based upon empirical reliability testing and physics of failure methods with respect to

   - Known failure mechanisms
   - Field operating environment including temperature, thermal cycling, humidity, bias, etc.
   - Field reliability and maintenance cost requirements

   Estimates of part lifetimes for each application can be made based upon available information to facilitate an intelligent decision. Figure 7 illustrates this process.

2. This report does not specify what environment PEMs are suited for or specific procedures and environmental limits to employ in making that decision. What has been offered is a look at the important factors which must be considered, information on fielded PEM reliability trends and a decision process flow within which to work. Investigations of the long term reliability of PEMs in various military environments could provide the data to justify modification of existing environmental limitations.

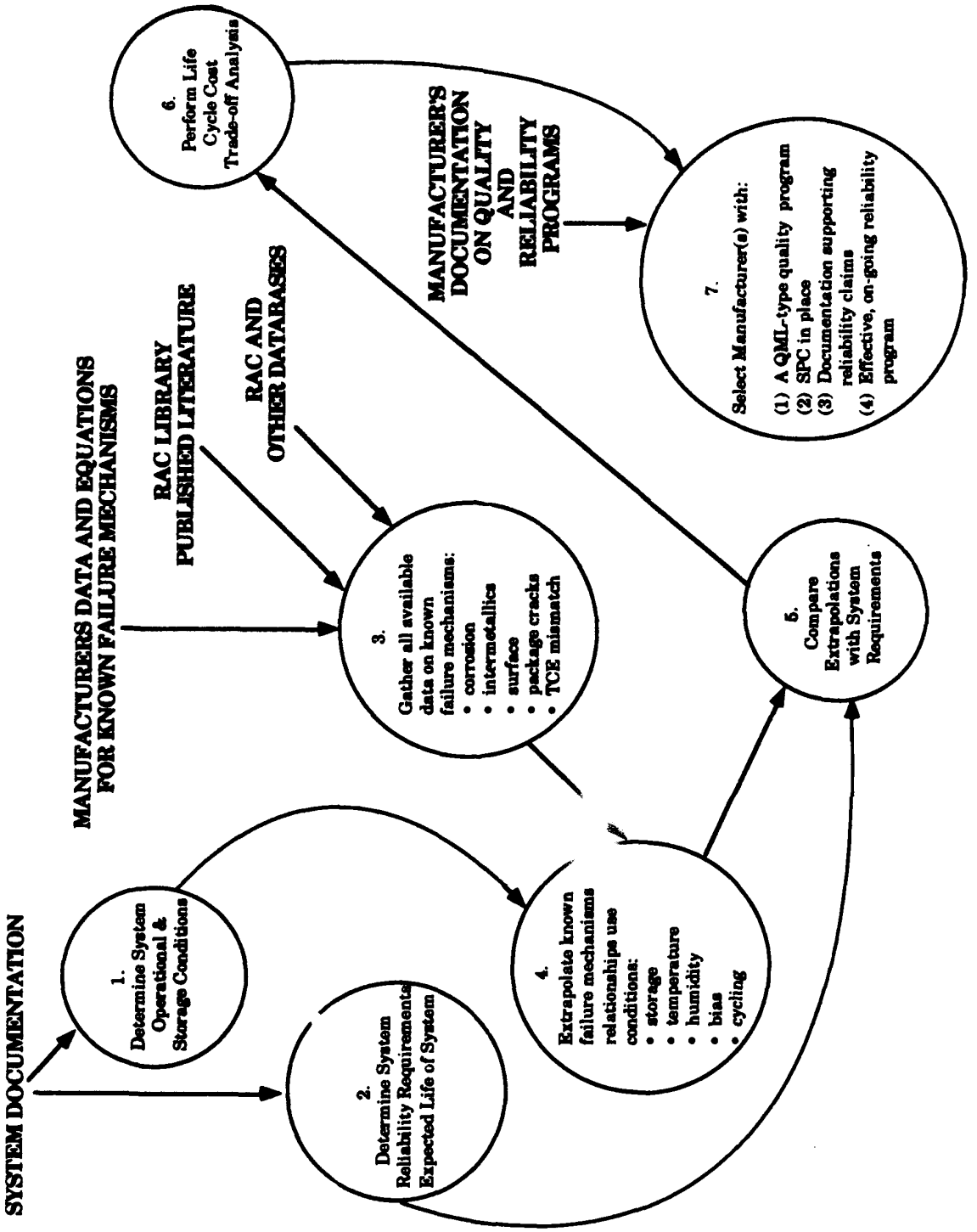


Figure 7: Process Flow for PEM Use Determination

3. System and equipment designers must take into account their product's functional requirements, operating, storage and transportation environments and customers' needs along with reliability, performance, size, weight and cost to make an intelligent decision about the best packaging method.

4. The difference in purchase price of plastic and hermetic parts is one of many factors which are considered when comparing plastic and hermetic parts. However, to determine the true purchase price of a particular package and die type all costs must be included i.e., reliability assurance, testing, field repair/warranty. Future die size and complexity increases could lead to higher die manufacturing and test costs and increase the impact of potential PEM failure mechanisms.

5. Moisture and temperature extremes are still problematic for PEMs, although existing field reliability data and high stress moisture resistance testing indicate that improvements have been made over previous incarnations. To date, organic coatings have not been developed which provide a long term moisture barrier. Factors which influence bond/wire integrity and failure mechanisms unique to plastic which were unknown ten years ago are clearly more widely discussed and understood today. This indicates the willingness and ability of PEM suppliers to make quality improvements.

6. Strict manufacturer selection and control procedures should be implemented. The manufacturer should have an established quality system in place, such as the process qualification procedures specified for the QML program which are presently being modified to include PEM's. This system must be supported by management and be able to provide data and documentation to substantiate claims of reliability and quality levels. The manufacturer should also have an effective, on-going reliability program which demonstrating understanding of the product and

operating environment limitations. This procedure has the potential to improve PEM reliability.

7. Research into the reliability and applicability of PEMs continues at a rapid pace. Results of on-going and new programs should be reviewed periodically to keep abreast of the state-of-the-art. Some programs to watch for include the following:

   a. Currently ELDEC Corporation of Bothell, Washington, R&D is in the process of evaluating both hermetic and plastic versions of the same IC on the same circuit card in the same application.

   b. The Reliability Analysis Center is planning a detailed state-of-the-art report on the reliability of PEMs. This report will present PEM reliability data both from the field and from testing, from a variety of data sources along with statistical analysis of this information.

   c. RWOH Program.

   Studies such as these will reveal how users can best take advantage of PEMs while maximizing the advantages and minimizing the risk.

8. Changes in PEM technology will continue to affect the failure mechanism distributions for these devices. For example, trends toward larger pieces of silicon surrounded by smaller amounts of molding compound will continue to drive the need for lower TCE toward that of the silicon. Smaller feature sizes will also further limit the amount of thermal stresses which can be withstood, and thermal conductivity of the molding compound will become increasingly important as power dissipation requirements continues to grow.

9. The major advantages of PEM's are:
   a. availability
   b. shock resistance
   c. weight

10. System cost savings may be achieved when the above features are considered in equipment design and fabrication where PEM's are demonstrated to produce the needed reliability.

11. QML additions and refinements for qualifying and procuring PEMs must be continued and should emphasize the study, optimization and assurance of PEM reliability performance. In particular, areas which must be addressed include: materials, die design and process factors which together determine susceptibility to thin film cracking, wire bond integrity and package cracking; methods of process control and monitoring for assuring consistent product; die coating materials, processes and inspection methods aimed at controlling surface passivation integrity; small sample high stress testing methods for objectively measuring package characteristics known to relate to field performance; and correlation of such stress tests to field reliability performance.

12. Finally, emphasis should be placed on knowing use environments and establishing firm reliability goals.

APPENDIX A:

LIST OF ACRONYMS

AMT	Acoustic Microscopic Technologies
CMOS	Complimentary Metalized Oxide Semiconductor
CRTA	Critical Review and Technology Assessment
DOE	Design of Experiments
DSB	Defense Science Board
EP/TAB	Environmentally Protected Tape Automated Bonded
ESD	Electrostatic Discharge
GB	Ground benign
GF	Ground Fixed
HAST	Highly Accelerated Stress Testing
LCC	Life Cycle Cost
PEM's	Plastic Encapsulated Microcircuits
PSG	Polysilicon Glass
PWA	Printed Wiring Assemblies
QML	Qualified Manufacturers List
QPL	Qualified Parts List
RHA	Radiation Hardness Assurance
RwoH	Reliability without Hermeticity

SLAM	Scanning Laser Acoustic Microscopy
SMT	Surface Mount Technology
SPC	Statistical Process Control
SPEC	Surface Protection for Electronic Circuits
TCE	Thermal Coefficient of Expansion

APPENDIX B:

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APPENDIX C:

CHRONOLOGY OF PLASTIC ENCAPSULATED SEMICONDUCTORS - 1966-1980

CHRONOLOGY OF A PLASTIC ENCAPSULATED SEMICONDUCTORS - 1966-1980

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APPENDIX D:

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910600	EXPERIMENTAL TECHNIQUES FOR ELECTRICAL TESTING OF MICROELECTRONIC COATINGS	TROYK, P.R. FRANKOVIC, R. ANDERSON, J.E.	IIT, PRITZKER INST. FOR MEDICAL ENGINEERING, RES. STAFF FORD MOTOR CO.	TRANSACTIONS, IEEE/CHMT, Vol. VOL. 14, No. 1, Pages PAGES 428-435	91-31
910600	POLYMER-COATED MICROELECTRONICS: COMPARISON OF BULK, SURFACE AND INTERPHASE CONDUCTIVITIES	ANDERSON, J.E., ADAMS, K.M. TROYK, P.R. FRANKOVIC, R.	RESEARCH STAFF, FORD MOTOR CO.,IIT, PRITZKER INSTITUTE FOR MEDICAL ENGINEERING	TRANSACTIONS, IEEE/CHMT, Vol. 14, No. 1, Pages 420-427	91-30
910400	DISTRIBUTOR REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE SENSITIVE (ESDS) DEVICES	ANON.	ELECTRONICS INDUSTRIES ASSOCIATION		25373-000
	THIS SPECIFICATION ESTABLISHES THE REQUIREMENTS FOR METHODS AND MATERIALS USED TO PROTECT ELECTRONIC DEVICES PROCESSED BY THE MANUFACTURER TO MEET EITHER MILITARY OR COMMERCIAL SPECIFICATIONS, WHICH ARE SUSCEPTIBLE TO DAMAGE OR DEGRADATION FROM ELECTROSTATIC DISCHARGE (ESD). THE ELECTROSTATIC CHARGES REFERRED TO IN THIS SPECIFICATION ARE GENERATED AND STORED ON SURFACES OF ORDINARY PLASTICS, MOSTCOMMON TEXTILE GARMENTS, UNGROUNDED HUMAN BODIES, AND MANY OTHER COMMONLY USED MATERIALS, NOT GENERALLY RECOGNIZED AS BEING ELECTROSTATIC GENERATORS.				
910400	ORIENTED WIRE-THROUGH CONNECTORS FOR HIGH DENSITY CONTACTS	YONEKURA,H.	FUJI POLYMER INDUSTRIES LTD	CONNECTION TECHNOLOGY, Vol. 7, No. 4, Pages 48-50	25333-003
	PRESENTLY, THE UTILIZATION OF SURFACE MOUNT TECHNOLOGY (SMT) REQUIRES VARIOUS HIGH DENSITY PACKAGING TECHNIQUES. THESE INCLUDE THE USE OF LEADLESS CERAMIC CHIP CARRIERS (LCC), PLASTIC LEADED CHIP CARRIERS (PLCC), SMALL OUTLINE PACKAGES (SOP), QUAD FLAT PACKAGES (QFP), PAD GRID ARRAYS (PGA) AND DISPLAYS WITH PAD AND MULTIPLE PARALLEL PADS AND VARIOUS OTHER HIGH DENSITY PAD CONFIGURATIONS.				
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	TODAY'S ELECTRONICS ARE MORE SENSITIVE TO MOISTURE CONTAMINATION EVEN WITH LITTLE OR NO PRESSURE DIFFERENTIAL PRESENT. CONSEQUENTLY, SEAL ENVIRONMENTAL SEALS NOW MUST USE A TRUE HERMETIC SEAL DESPITEDESIGN LIMITATIONS AND HIGHER COST.				
910300	PLCC PACKAGE CRACKING: IS PRE-ASSEMBLY BAKING THE ANSWER?	MORENCY, DANIEL		SURFACE MOUNT TECHNOLOGY, Pages 62-64	91-1
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910000	THIN FILM CRACKING IN PLASTIC PACKAGES-ANALYSIS, MODEL AND IMPROVEMENTS	FOEHRINGER, R. GOLWAKAR, S., ESKILDSEN, S. ALTIMAIR, S.	INTEL, (CHANDLER, AZ)	PROCEEDINGS, 41ST (1991) ECTC, Pages ####	91-18
910000	USE OF THE IN-PROCESS BOND SHEAR TEST FOR PREDICTING GOLD WIRE BOND FAILURE MODES IN PLASTIC PACKAGES	MAHNEY, M. SHELL, M. STRODE, R.	INTEL, (CHANDLER, AZ)	PROCEEDINGS, 29TH (1991) ANNUAL IRPS, Pages 44-51	91-13
910000	WIRE BONDER CHARACTERIZATION USING A "PN JUNCTION-BOND PAD" TEST STRUCTURE	GEE, S.A. NGUYEN, L.T. AKYLAS, V.R.	PHILIPS R&D CENTER, SIGNETICS, (SUNNYVALE, CA)	PROCEEDINGS, MEPPE FOCUS 91, Pages 156-170	91-3
901200	CORROSION CRITERIA FOR ELECTRONIC PACKAGING: PART II - CALCULATED CORROSION CURRENTS AND ACCELERATION FACTORS	HOGE, C.E.	WESTERN DIGITAL CORPORATION	TRANSACTIONS, IEEE/CHMT, Vol. 13, No. 4, Pages 1098-1104	90-21
901200	CORROSION CRITERIA FOR ELECTRONIC PACKAGING: PART III - CORROSION BY PACKAGE FAMILY	HOGE, C.E.	WESTERN DIGITAL CORPORATION	TRANSACTIONS, IEEE/CHMT, Vol. 13, No. 4, Pages 1105-1109	90-22

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901200	CORROSION CRITERIA FOR ELECTRONIC PACKAGING: PART I-A FRAMEWORK FOR CORROSION OF INTEGRATED CIRCUITS	HOGE, C.E.	WESTERN DIGITAL CORPORATION	TRANSACTIONS, IEEE/CHMT, Vol. 13, No. 4, Pages 1090-1097	90-20
901200	IN SITU CALIBRATION OF STRESS CHIPS	BASTAWROS, A.F. VOLOSHIN, A.S.	HOMER RESEARCH LABORATORIES,LEHIGH UNIVERSITY	TRANSACTIONS, IEEE/CHMT, Vol. 13, No. 4, Pages 888-892	90-17
901200	RELATION BETWEEN DELAMINATION AND TEMPERATURE CYCLING INDUCED FAILURES IN PLASTIC PACKAGED DEVICES	DOORSELAER, K.V. DEZEEUW, K.	PHILIPS RESEARCH LABS, (EINDHOVEN, THE NETHERLANDS)	TRANSACTIONS, IEEE/CHMT, Vol. 13, No. 4, Pages 879-882	90-15
901200	SILICONE DIE BOND ADHESIVE AND CLEAN IN-LINE CURVE FOR COPPER LEAD FRAME	SUZUKI, K., HIGASHINO, T. TSUBOSAKI, K., KABASHIMA, A. MINE, K., NAKAYOSHI, K.	HITACHI MICROCOMPUTER ENGINEERING,SEMI OR DESIGN, DOWN CORNING	TRANSACTIONS, IEEE/CHMT, Vol. 13, No. 4, Pages 883-887	90-16
901200	TEMPERATURE-HUMIDITY INDUCED MECHANISMS IN PLASTIC ENCAPSULATED BIPOLAR TRANSISTORS	MATTHAI,G.	GERMANY	QUALITY AND RELIABILITY ENGINEERING, Vol. 6, No. 5, Pages 317-321	24861-001
	IN THIS ARTICLE THE DISADVANTAGE OF WELL-KNOWN MODELS FOR TEMPERATURE-HUMIDITY INDUCED FAILURE MECHANISMS IN PLASTIC ENCAPSULATED MICROELECTRONIC DEVICES ARE SHOWN. IT IS NECESSARY TO RESTRICT THE VALIDITY OF THESE MODELS. THE ADVANTAGE OF BIPOLAR TRANSISTORS IS THAT THE FAILURE MECHANISMS CAN BE SEPARATED VERY EASILY. THE MOST SIGNIFICANT PROPERTIES OF POLYMERS, PLASTICATION AND GLASS TRANSITION,AND ALSO THE DIFFUSION OF MOISTURE WILL BE DESCRIBED.				
901200	THERMALLY INDUCED IC PACKAGE CRACKING	SUHL, D.	IC PACKAGE ENGINEERING, DEC	TRANSACTIONS, IEEE/CHMT, Vol. 13, No. 4, Pages 940-945	90-18
901200	TRANSIENT THERMAL STRAIN MEASUREMENTS IN ELECTRONIC PACKAGES	BASTAWROS, A.F. VOLOSHIN, A.S.	HOMER RESEARCH LAB, LEHIGH UNIVERSITY	TRANSACTIONS, IEEE/CHMT, Vol. 13, No. 4, Pages 961-966	90-19
901200	VOID FREE BONDING OF LARGE SILICON DICE USING GOLD-TIN ALLOYS	MATIJASEVIC, G.S. LEE, C.C. WANG, C.Y.	UC, (IRVINE, CA)	TRANSACTIONS, IEEE/CHMT, Vol. 13, No. 4, Pages 1128-1135	90-23
901106	NONDESTRUCTIVE INSPECTIONS FOR INTERNAL DEFECTS IN CFRP BY USING SLAM TECHNIQUES	YOSHIDA, H., URABE, K., WATABE, H.	INDUSTRIAL PRODUCTS RESEARCH INSTITUTE,JBOL TRADING CO.	PROCEEDINGS, 22ND INTERNATIONAL SAMPE TECHNICAL CON, Pages ####	90-26
901100	APPLICATIONS OF HIGH FREQUENCY ULTRASONIC IMAGING IN THE EVALUATION OF ELECTRONIC PACKAGING	GARTSIDE, C.S.	ULTRASONIC SCIENCES, INC., (UK)	PROCEEDINGS, CONFERENCE ON HIGH PERFORMANCE PACKAGING, Pages 178	90-59
901100	LONG TERM FIELD FAILURE MECHANISMS OF MICROELECTRONICS	EBEL,G.H.	IIT RESEARCH INSTITUTE	1990 DIGEST OF PAPERS, Pages 597-600	24777-149
	THERE HAVE BEEN SEVERAL PAPERS PRESENTED BY THE FIELD FAILURE RETURN PROGRAM (FFRP) ON THE DETAILED RESULTS OF FAILURE ANALYZED PARTS. THE SUBSTANTIAL PAYBACK OF THESE EFFORTS HAS BEEN WELL DOCUMENTED. THERE ARE MANY GLOBAL ISSUES WHICH CAN HAVE EVEN LARGER RETURNS ON THE INVESTMENT. THE PROGRAM ORIGINALLY WAS ESTABLISHED WHEN P.B. GHATE CHALLENGED THE INDUSTRY TO PRODUCE ONE ELECTROMIGRATION FIELD FAILURE. THIS CHALLENGE COULD BE EXTENDED TO OTHER AREAS SUCH AS THE LONG TERM HERMETIC INEGRITY OF MICROELECTRONIC PACKAGES AND ELECTRICAL INTERFACE STABILITY OF CONDUCTIVE EPOXIES.				
901100	RELIABILITY STUDY OF ENVIRONMENTALLY PROTECTED/TAPE AUTOMATED BONDED (EP/TAB) INTEGRATED CIRCUITS	NICOLAIDES,R.V. GOBLISH,B.E. BAKKE,S.J.	UNITED STATES ARMY	1990 DIGEST OF PAPERS, Pages 139-140	24777-030
	A RELIABILITY STUDY WAS CONDUCTED TO DETERMINE IF INTEGRATED CIRCUITS PACKAGED IN ENVIRONMENTALLY PROTECTED/TAPE-AUTOMATED-BONDED (EP/TAB) TECHNOLOGY COULD BE A VIABLE ALTERNATIVE TO HERMETICALLY SEALED ONES IN MILITARY SYSTEMS. THE EP/TAB IC IS NOT HOUSED IN A HERMETICALLY SEALED PACKAGE. THE MAJOR CONCERNS ARE DEGRADATION IN HARSH ENVIRONMENTS, SPECIFICALLY CORROSION OF THE ALUMINUM METALLIZATION AND METAL MIGRATION WHICH CAN OCCUR IF MOISTURE AND/OR CONTAMINATION CAN PENETRATE THE PROTECTIVE LAYER ON THE SILICON SURFACE CHIP.				
901100	ULTRASONIC MICROSCOPE USED IN THE REFLECTIVE AND THROUGH TRANSMISSION MODES IN THE FAILURE ANALYSIS OF ELECTRONIC PACKAGES	PFANNSCHMIDT, G.	SIEMENS AG, (MUNICH)	PROCEEDINGS, CONFERENCE ON HIGH PERFORMANCE PACKAGING, Pages 179-187	90-25
901029	ACOUSTIC MICROSCOPY TECHNOLOGY (AMT) ANALYSIS OF ADVANCED MATERIALS FOR INTERNAL DEFECTS AND DISCONTINUITIES	KESSLER, L.W. MARTELL, S.R.	SONOSCAN, (BENSENVILLE, IL)	PROCEEDINGS, (1990) ISTFA, Pages PAGES 491-504	90-51
901029	DEFECT DETECTION IN PLASTIC ENCAPSULATED ICS USING ACOUSTIC MICROSCOPY	IDE, J. ELLIS III, J.L.	DEC, (NORTHBORO, MA)	PROCEEDINGS, (1990) ISTFA, Pages 285-290	90-50
901029	LASER SCAN MICROSCOPY APPLICATIONS FOR MICROELECTRONIC FAILURE ANALYSIS	HUSSEY, K.P. SELESKY, S.L.	MOTOROLA, (AUSTIN, TX)	PROCEEDINGS, (1990) ISTFA, Pages 259-265	90-49

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901029	THE APPLICATION OF SCANNING ACOUSTIC MICROSCOPY TO CONTROL MOISTURE/THERMAL-INDUCED PACKAGE DEFECTS	MOORE, T.M. MCKENNA, R. KELSALL, S.	TI,TI/ COMPAQ,TI	PROCEEDINGS, (1990) ISTFA, Pages 251-258	90-48
901001	NONDESTRUCTIVE EVALUATION OF TAB BONDING BY MEANS OF ACOUSTIC MICROSCOPY: OVERVIEW OF PROGRESS USING C-MODE SCANNING ACOUSTIC MICROSCOPY	SEMMENS, J.E. KESSLER, L.W.	SONOSCAN, (BENSENVILLE, IL)	PROCEEDINGS, 9TH (1990) IEMTS, Pages 92-97	90-52
900919	RELIABILITY STUDY ON ENVIRONMENTALLY PROTECTED/TAPE-AUTOMATED-BONDED INTEGRATED CIRCUITS	GOBLISH,B.E. BAKKE,S.J. ARNO,R.G.	HONEYWELL, INC.	PREDICTIVE TECHNOLOGY SYMPOSIUM PROC, Pages 89-98	24867-011
	THIS PAPER DISCUSSES AN APPROACH USED TO COLLECT THE RELIABILITY DATA ON EP/TAB ICS AND THE RESULTS OBTAINED TO DATE. TWO TYPES OF INTEGRATED CIRCUITS, BIPOLAR AND COMPLEMENTARY-METAL-OXIDE SEMICONDUCTOR (CMOS), WERE TESTED. TEST VEHICLES CONSISTED OF BOTH EP/TAB ICS AND INTEGRATED CIRCUITS IN HERMETICALLY SEALED PACKAGES. ENVIRONMENTAL TESTS WERE CONFIGURED TO VERIFY THAT EP/TAB ICS COULD WITHSTAND PROLONGED EXPOSURE TO HOSTILE ENVIRONMENTS. ENVIRONMENTAL TESTING WAS PERFORMED IN ACCORDANCE WITH TEST METHODS OF MIL-STD-883, WERE APPLICABLE. RELIABILITY LEVELS WERE ESTABLISHED.				
900913	ESD POLYMER ALLOYS - AN ALTERNATIVE APPROACH FOR PRODUCING PERMANENTLY STATIC DISSIPATIVE POLYETHYLENE	MASS,T.R.	BF GOODRICH COMPANY	1990 EOS/ESD SYMPOSIUM PROCEEDINGS, Pages 237-244	24862-036
	THIS STUDY WAS CONDUCTED IN AN EFFORT TO APPLY THE ESD POLYMER ALLOYING TECHNOLOGY TO PRODUCE PERMAMENT AND RELIABLE STATIC DISSIPATIVE POLYETHYLENES. IN A PREVIOUS PUBLICATION, IT WAS DEMONSTRATED THAT THROUGH ESD POLYMER ALLOYING, STATIC DISSIPATIVE PROTECTION OF SOME SELECTED THERMOPLASTIC RESINS WAS OBTAINABLE WITH ONLY MINOR EFFECTS ON THE OVERALL MATRIX POLYMER'S PHYSICAL PROPERTIES. IT WASFURTEHR DEMONSTRATED THAT THE RESULTING ESD PROTECTION DISPLAYED EXCELLENT PERMANENCE CHARACTERISTICS AS WELL AS HUMIDITY INDEPENDENCE.				
900900	DRY PACKING FOR SURFACE MOUNT DEVICES			INTERNAL REPORT TOSHIBA CORPORATION, Vol. RIS0039B3	90-9
900828	RWOH - A CONSORTIUM APPROACH TO RELIABILITY WITHOUT HERMETICITY	PITTS,G.	MCC/LEHIGH UNIVERSITY		24676-000
	A CONSORTIUM APPROACH TO RELIABILITY WITHOUT HERMETICITY.				
900827	A PRACTICAL APPROACH TO DETERMINE PACKAGE CRACK SENSITIVITY IN A SMT ASSEMBLY ENVIRONMENT	PEREZ, R.	COMPAQ, HOUSTON, TX	PROCEEDINGS, TECHICAL PROGRAM, SURFACE MOUNT 90, Pages 1-11	90-28
900824	HITACHI INTERNAL REPORT: SOLDERING TECHNOLOGY OF FINE PITCH PACKAGE	YANO, H.	HITACHI IC PACKAGE ENG. DEVELOPMENT DEPARTMENT	HITACHI INTERNAL REPORT, Vol. REV. 5, PKG 90 056	90-7
900800	INSPECT PLASTIC IC PACKAGES WITH ULTRASOUND	ADAMS, T.E.		SEMICONDUCTOR INTERNATIONAL, Pages 88-91	90-27
900800	INSPECT PLASTIC IC PACKAGES WITH ULTRASOUND	ADAMS,T.	UNKNOWN	SEMICONDUCTOR INTERNATIONAL, Vol. 13, No. 9, Pages 88-91	24702-002
	ACOUSTIC MICROSCOPY DETECTS FAULTS IN MOLDED PLASTIC PACKAGES THAT MORE TRADITIONAL TECHNIQUES OFTEN OVERLOOK.				
900800	INTERPRETATION OF SCANNING ACOUSTIC MICROSCOPY MICROGRAPHS OF MOISTURE-INDUCED DAMAGE IN SURFACE MOUNT ICS	MOORE, T.M. MCKENNA, R. KELSALL, S.	TI, TI/COMPAQ,TI	PROCEEDINGS, TECHNICAL PROGRAM, SURFACE MOUNT 90, Pages 12-24	90-29
900800	SURVEY OF ACOUSTIC MICROSCOPY METHODS FOR IMPROVING THE RELIABILITY OF SURFACE MOUNT COMPONENTS AND ASSEMBLIES	KESSLER, L.W. SEMMENS, J.E.	SONOSCAN, (BENSENVILLE, IL)190-15	PROCEEDINGS, TECHNICAL PROGRAM, SURFACE MOUNT 90, Pages 33-41	90-30
900800	THIN SMALL OUTLINE PACKAGE (TSOP) APPLICATION NOTE		HITACHI SEMICONDUCTOR AND IC DIVISION	HITACHI SEMICONDUCTOR AND IC DIVISION, Vol. M10T001	90-8
900600	A MODEL FOR MOISTURE INDUCED CORROSION FAILURES IN MICROELECTRONIC PACKAGES	PECHT, M.	CALCE UNIVERSITY OF MARYLAND	TRANSACTIONS, IEEE/CHMT, Vol. 13, No. 2, Pages 383-389	90-12
900507	ADHESION BETWEEN MOULDING COMPOUND AND SUBSTRATE	BOGNER, M., HOLZAPFEL, W. MAIER, M., QUELLA, F. SCHWARZ, R.	SIEMENS, COMPONENT GRP & CENTRAL CORP. RES., (MUNCHE, FRG)	PROCEEDINGS, 8TH (1990) IEMTS, Pages 332-339	90-57

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900507	EVALUATION OF RELIABILITY AND PRODUCTION PARAMETERS USED IN NEW MATERIALS AND PROCESSING APPLICATIONS FOR SURFACE MOUNT TECHNOLOGY	MEERSMAN, E. HENTE, A. ALLAERT, K.	ALCATEL BELL TELEPHONE, (ANTWERPEN, BELGIUM)	PROCEEDINGS, 8TH (1990) IEMTS, Pages 322-331	90-56
900507	IR MICROSCOPIC OBSERVATION OF PLASTIC ENCAPSULATED TAB INNER LEAD BONDS DEGRADING DURING THERMAL CYCLING	ALPERN, P. TILGNER, R.	SIEMENS AG, (MUNCHEN, FRG)	PROCEEDINGS, 8TH (1990) IEMTS, Pages 306-312	90-54
900507	MEASUREMENT OF STRESS AND TEMPERATURE DISTRIBUTION IN LARGE AREA DIES	LANCHBERY, J.F. SHORTHOUSE, G.	ERA TECHNOLOGY,ERA JOHNSON MATTHEY TECH. CENTRE	PROCEEDINGS, 8TH (1990) IEMTS, Pages 287-295	90-53
900507	PLASTIC PACKAGE RELATED EFFECTS, MEASURED BY MEANS OF SILICON TEST PATTERNS	TIZIANI, R. MERMET-GUYENENET, M. MOTTA, V.	SGS-THOMSON MICRO, PKG. DEVELOP DEPT., ITALY, GRENOBLE, FR	PROCEEDINGS, 8TH (1990) IEMTS, Pages 340-450	90-58
900507	SCANNING ACOUSTIC MICROSCOPE: AN ATTRACTIVE TOOL FOR THE THICK FILM TECHNOLOGY CHARACTERIZATION	KRAUSE, J., OUSTEN, Y. FREMONT, H., DANTO, Y. SCHWIERZI	INSTITU FUR HALBLEITERTECHNOLOGIE UND WERKSTOFFE DER ELECTRO	PROCEEDINGS, 8TH (1990) IEMTS, Pages 313-321	90-55
900425	A STUDY ON THE DISCHARGE PHENOMENA OF VACCUUM REED SWITCH	OKHMICHI,T. KOBAYASHI,T. HINOHARA,K.	OKI ELECTRIC INDUSTRY CO., LTD.	38TH (1990) RELAY CONFERENCE PROCEEDINGS, Pages 6-1 THRU 6-4	25124-006
	REED SWITCHES HAVE CONTACTS HERMETICALLY SEALED TOGETHER WITH AN INACTIVE GAS; THEY ARE FREE FROM THE INFLUENCE OF DUST AND MOISTURE IN THE ENVIRONMENT. FOR THIS REASON, THEY HAVE BEEN WIDELY USED INVARIETY OF FIELDS SUCH AS MEASUREMENT AND CONTROL, WHERE HIGH RELIABILITY IS REQUIRED. THE RECENTLY EXPANDING APPLICATION MEAN THAT IMPROVEMENTS NEED TO BE MADE.				
900400	HERMETICITY IMPROVES PACKAGE RELIABILITY	DICKINSON,D. MOORE,D.	NONE	ELECTRONIC PACKAGING AND PRODUCTION, Vol. 30, No. 4, Pages 61-63	24385-001
	HIGH RELIABILITY CIRCUITS DEMAND THE MOST OF ELECTRONIC PACKAGES. GOOD HERMETICITY IS ONE FACTOR CONTRIBUTING TO CIRCUIT RELIABILITY. AS THE DEMANDS OF COMPLEX CIRCUITRY, ADVERSE OPERATING CONDITIONS,AND EXTENDED LIFETIMES INTENSIFY, HIGH RELIABILITY ELECTRONIC CIRCUIT PACKAGES WILL HAVE TO MEET INCREASINGLY STRINGENT STANDARDS. FOR A PACKAGE TO SURVIVE AND PERFORM FLAWLESSLY IN A HOSTILE ENVIRONMENT FOR MORE THAN 10 YEARS, MORE SOPHISTICATED MATERIALS AND BETTER CONTROL OF THE ASSEMBLY PROCESSES ARE NECESSARY.				
900300	BAKING ELIMINATES PLASTIC PACKAGE CRACKS	LACAP,E.M. KHAN,J.I.	NONE	SEMICONDUCTOR INTERNATIONAL, Vol. 13, No. 3, Pages 92-94	24408-001
	IT IS EXTREMELY IMPORTANT THAT TODAY'S FINE PITCH, THIN PACKAGES ARE RELIABLE. WE CAN UNDERSTAND THE NEED FOR THESE PACKAGES FOR SURFACE MOUNT APPLICATIONS. HOWEVER, ALONG WITH SURFACE MOUNT PACKAGES,USERS HAVE TO CONTEND WITH THE HIGH TEMPERATURES OF SOLDER REFLOW THAT CAN HAVE SEVERE EFFECTS OF ANY PACKAGE. INCREASING CHIP SIZES ARE ALSO AFFECTING PACKAGING. TODAY'S DESIGN AND PROCESS TECHNOLOGIES ARE INTEGRATING MORE FUNCTIONS ONTO A SINGLE CHIP, INCREASING CHIP SIZE AND POWER COMSUMPTION.				
900300	THE EFFECT OF HIGH-TEMPERATURE INTERMETALLIC GROWTH ON BALL-SHEAR INDUCED CRATERING	CLATTERBAUGH, G.V. CHARLES, H.K., JR.	APL, JOHN HOPKINS UNIVERSITY	TRANSACTIONS, IEEE/CHMT, Vol. 13, No. 1, Pages 167-175	90-10
900200	THOMAS: PUSHING THE PENTAGON TOWARD QML	ANON.	NONE	MILITARY & AEROSPACE ELECTRONICS, Pages 39-40	24321-000
	FIRST SILICON. THEN GALLIUM ARSENIDE. THEN CAPACITORS, RESISTORS, CONNECTORS, AND EVEN PLASTIC SUBSTRATES FOR HIGH-SPEED, HIGH-FREQUENCY INTERCONNECTION. IF ROBERT THAS HIS WAY, THERE WILL BE A QUALIFIED MANUFACTURING LINE STANDARD FOR ALL OF THESE - AND PLENTY OF OTHER THINGS AS WELL.				
900100	HIGH SPEED/HIGH DENSITY COPPER POLYIMIDE PACKAGE FOR GAAS DIGITAL CIRCUITS, FINAL TECHNICAL REPORT	PALMQUIST,S.L. SAINATI, R. MORAVEC,T.J.	HONEYWELL CO.		24444-000
	A NEW, HIGH-DENSITY, SINGLE-CHIP, SURFACE-MOUNT PACKAGE FOR DIGITAL GAAS ICS HAS BEEN DESIGNED AND FABRICATED. IT HAS 200 I/O OF WHICH 156 HAVE A BANDWIDTH OF 3GHZ AND 44 CAN PROVIDE 3 VOLTAGE LEVELSTO THE GAAS DIE. THE CERAMIC-BASED HERMETIC PACKAGE INCLUDES A NOVEL MICROSTRIP DESIGN WITH A POLYIMIDE DIELECTRIC AND INTEGRAL THIN FILM TERMINATION RESISTORS. EXTENSIVE TESTING UNDER MIL-STD-883C WAS PERFORMED TO ASSESS PACKAGE PERFORMANCE WITH ORGANIC MATERIALS AS PER MILITARY REQUIREMENTS FOR HERMETIC PACKAGES AND HIGH-RADIATION ENVIRONMENTS.				
900100	PLASTIC PACKAGING TECHNOLOGY - A USER'S PERSPECTIVE	ROBOCK, P.V.	IBM, (HOPEWELL JUNCTION, NY)	PROCEEDINGS, MEPPE FOCUS 90, Pages 95-103	90-24
900000	A STUDY OF LIFE ESTIMATION CONCERNED WITH ELECTRONIC PRODUCTS	ITOH, H. IWASHITA, S.	NIPPONDENSO CO., LTD.	PROCEEDINGS, INTER. SYM ON R & M, Pages 163-165	90-5
	TH CONNECTOR STRESSES ON SOLDER JOINTS				
900000	A STUDY OF THE RELIABILITY OF SURFACE MOUNT DEVICES	ISHIKAWA, T. TABE, N.	MATSUSHITA ELECTRONIC COMPONENTS, CO., INC.	PROCEEDINGS, INTER. SYM ON R & M, Pages 157-162	90-4

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900000	ANALYTICAL AND EXPERIMENTAL STUDY FOR DESIGNING MOLDING COMPOUNDS FOR SURFACE MOUNTING DEVICES	OHIZUMI, S., ITO, S. NAGASAWA, M., IGARASHI, K. KOHMOTO, M.	NITTO DENKO CORPORATION	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECT COMP & TECH, Pages 625-631	90-38
900000	APPLICATION OF ACOUSTIC MICROSCOPY TO ELECTRONIC PACKAGING PROBLEMS	KHURI-YAKUB, B.T. LIVESAY, B.R. NAGARKAR, M.D.	STANFORD UNIVERSITY	PROCEEDINGS ASM INTER 3RD ELECTRONIC MATERIALS AND PROCESSING, Vol. ISBN: 0-87170-396-3	90-11
900000	CALIBRATION CONSIDERATIONS FOR PIEZORESISTIVE-BASED STRESS SENSORS	BEATY, R.E., SUHLING, J.C. MOODY, C.A., BITTLE, D.A. JOHNSON, R.W., BUTLER, R.D.	AUBURN UNIVERSITY	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECT COMP & TECH, Pages 797-806	90-43
900000	DEVELOPMENT OF LOW ELASTIC MODULUS DIE ATTACH MATERIAL AND CLEAN CURE PROCESS	SUZUKI, K., HIGASHINO, T. TSUBOSAKI, K., KABASHIMA, A. MINE, K., NAKAYOSHI, K.	HITACHI MICROCOMPUTER ENG./HITACHI LTD/DOW CORNING TORAY	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECT COMP & TECH, Pages 835-839	90-47
900000	DEVELOPMENT OF ULTRA-THIN SURFACE MOUNTING IC PACKAGE (0.8 MM THICK TQFP)	FUJITA, K., OOMI, J. K. TOYOZAWA, S. MINAMIDE T. MAEDA	SHARP CORPORATION	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECT COM & TECH. CON, Pages 302-307	90-32
900000	EFFECT OF COMBINATION BETWEEN VARIOUS POLYIMIDE COATING MATERIALS AND MOLDING COMPOUNDS ON THE RELIABILITY OF INTEGRATED CIRCUITS (ICS)	TAKEUCHI, E. TAKEDA, T. HIRANO, T.	SUMITOMO BAKELITE COMPANY, LTD.	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECT COMP & TECH, Pages 818-823	90-46
900000	EXTREMELY RELIABLE BONDING OF LARGE SILICON DICE USING GOLD-TIN ALLOY	MATIJASEVIC, G.S., WANG, C.Y. LEE, C.C.	UNIVERSITY OF CALIFORNIA, IRVINE, CA	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECT COMP & TECH, Pages 7b9-790	90-41
900000	HIGH PERFORMANCE SCREEN-PRINTABLE SILICONE AS SELECTIVE HYBRID IC ENCAPSULANT	WONG, C.P.	AT&T BELL LABORATORIES	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECT. COMP & TECH, Pages 606-612	90-36
900000	IMPACT OF MOISTURE ON PLCC/PJQFP PACKAGE CRACKING	GROOVER, R.L. JOROSKI, J.H.	VLSI TECHNOLOGY (SAN JOSE STATE UNIVERSITY), LSI LOGIC	PROCEEDINGS, (1990) MRS MEETING, Pages 17	90-13
900000	IN-SITU CALIBRATION OF STRESS CHIPS	BASTATWROS, A.F. VOLOSHIN, A.S.	LEHIGH UNIVERSITY	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECT COMP & TECH, Pages 791-796	90-42
900000	LONG TERM FIELD FAILURE MECHANISMS OF MICROELECTRONICS	EBEL,G.H.	IITRI		24593-000
	THERE HAVE BEEN SEVERAL PAPERS PRESENTED BY THE FIELD FAILURE RETURN PROGRAM (FFRP) ON THE DETAILED RESULTS OF FAILURE ANALYZED PARTS. THE SUBSTANTIAL PAYBACK FOR THESE EFFORTS HAS BEEN WELL DOCUMENTED. THERE ARE MANY GLOBAL ISSUES WHICH CAN HAVE EVEN LARGER RETURNS ON THE INVESTMENT. THE PROGRAM ORIGINALLY WAS ESTABLISHED WHEN P.B. GHATE CHALLENGED THE INDUSTRY TO PRODUCE ONE ELECTROMIGRATION FIELD FAILURE. THIS CHALLENGE COULD BE EXTENDED TO OTHER AREAS SUCH AS THE LONG TERM HERMETIC INTEGRITY OF MICROELECTRONIC PACKAGES AND ELECTRICAL INTERFACE STABILITY OF CONDUCTIVE EPOXIES.				
900000	NONDESTRUCTIVE EVALUATION OF MICROELECTRONIC COMPONENTS BY ACOUSTIC MICROSCOPE	MARTELL, S.R. KESSLER, L.W. WEY, A.C.	SONOSCAN, (BENSENVILLE, IL)	PROCEEDINGS, 2ND (1990) NEPCON-SEMI, Pages 16	90-31
900000	PARAMETRIC SHIFTS IN DEVICES: ROLE OF PACKAGING, VARIABLES AND SOME NOVEL SOLUTIONS	PENDSE, R. JENNINGS, D.	HEWLETT-PACKARD CO./NATIONAL SEMICONDUCTOR CORP.	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECT COMP & TECH, Pages 322-326	90-34
900000	PROGRESSION OF DAMAGE CAUSED BY TEMPERATURE CYCLING ON A LARGE DIE IN A MOLDED PLASTIC PACKAGE	LESK, I.A., THOMAS, R.E. HAWKINS, G., REMMEL, T.P. RUGG, J.	MOTOROLA, INC.	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECT COMP & TECH, Pages 807-812	90-44
900000	RELATION BETWEEN DELAMINATION AND TEMPERATURE-CYCLING-INDUCED FAILURES IN PLASTIC PACKAGED DEVICES	VANDOORSELAER, K. DE ZEEUW, K.	PHILIPS RESEARCH LABORATORIES	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECT COMP & TECH, Pages 813-817	90-45

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900000	RELATION BETWEEN INNER VOIDS OF PLASTIC IC PACKAGES AND NON-NEWTONIAN FLOW CHARACTERISTICS OF RESIN ENCAPSULANT	ICHIMURA,S., KINASHI, K. URANO, T.	SHIMODATA RES. LAB,MINAMIYUKI WORKS, HITACHI CHEMICAL CO.	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECT COMP & TECH, Pages 641-645	90-40
900000	RELIABILITY OF ULTRA-THIN SURFACE MOUNTED PACKAGE (TQFP)	OMI, S. FUJITA, K. TOYOZAWA, K., MINAMIDE, S. TSUKA, T., MAEDA, T.	SHARP CORPORATION	PROCEEDINGS, INTER. SYM. ON RELIABILITY & MAINTAINABILITY, Pages 140-144	90-1
900000	ROBUST ENCAPSULATION OF HYBRID DEVICES	EMERSON, J.A. MARTIN, A.R., BONNEUA, M.R. BURKHART, D.A., SPARAPANY, J.J.	AT&T BELL LABS,AT&T MICRO.,DEXTER ELECT. MATERIALS	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECTR COMP & TECH, Pages 600-605	90-35
900000	SPECIAL PROPERTIES OF MOLDING COMPOUND FOR SURFACE MOUNTING DEVICES	NISHIOKA, T., ITO, S. NAGASAWA, M., IGARASHI, K. KOHMOTO, M.	NITTO DENKO CORPORATION	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECT COMP & TECH, Pages 632-640	90-39
900000	STRUCTURAL EFFECT OF IC PLASTIC PACKAGE ON RESIDUAL STRESS IN SILICON CHIPS	MIURA, H., NISHIMURA, A. KAWAI, S., MURAKAMI, G.	HITACHI LTD	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECT COMP & TECH, Pages 316-321	90-33
900000	STRUCTURE ANALYSIS OF SMD IN HYBRID IC BY COMPUTER SIMULATION	INOUE, K.	MITSUBISHI ELECTRIC CORPORATION	PROCEEDINGS, INTER. SYM ON RELIABILITY & MAINTAINABILITY, Pages 151-156	90-3
	THERMOMECHANICAL STRESS ON THE CHIP BY THE ENCAPSULATION				
900000	TEMPERATURE-CYCLING ACCELERATION FACTORS FOR ALUMINUM METALLIZATION FAILURE IN VLSI APPLICATIONS	DUNN, C.F. MCPHERSON, J.W.	TEXAS INSTRUMENTS	PROCEEDINGS, (1990) IRPS, Pages 252-258	90-14
900000	THE INFLUENCE ON SMD'S MOISTURE RESISTANCE BY PCT EQUIPMENT	MASUDA, H.	MATSUSHITA CORPORATION	PROCEEDINGS, INTER. SYM ON RELIABILITY & MAINTAINABILITY, Pages 145-150	90-2
900000	ULTRASONIC TESTING OF MATERIALS	KRAUTKRAMER, JOSEF KRAUTKRAMER, HERBERT SPRINGER-VERLAG		1990 TRANSLATION OF THE 5TH REVISED GERMAN (1986) EDITION, Vol. ISBN 0-387-51231-4	90-6
900000	UNIQUE POLYBUTADIENE RESIN: CHARACTERIZATION AFTER HARDENING AND APPLICATION TO IC	BATTISTI, A., HIRAYAMA, K. OKUNO, A.	JOHN C. DOLPH CO.,NIPPON MINING CO., LTD.,JAPAN REC. CO.	PROCEEDINGS, 40TH (1990) IEEE/CHMT ELECT COMP & TECH, Pages 620-624	90-37
891200	EFFECT OF LEAD FRAME MATERIAL ON PLASTIC-ENCAPSULATED IC PACKAGE CRACKING UNDER TEMPERATURE CYCLING	NISHIMURA, A. KAWAI, S. MURAKAMI, G.	HITACHI, MECH. ENG. RES. LAB, HITACHI SEMI DESIGN AND DEVELO	TRANSACTIONS, IEEE/CHMT, Vol. 12, No. 4, Pages 639-645	89-14
891110	DEGRADATION MECHANISMS OF GAAS MESFET DEVICES IN HIGH HUMIDITY CONDITIONS	MAGISTRALI,F. OGLIARI,D. SANGALLI,M.		PROCEEDINGS, (1989) ISTFA, Pages 141-151	24492-018
	GAAS MESFETS DEVICES OF DIFFERENT TECHNOLOGIES WERE AGED UNDER HIGH HUMIDITY TESTS, AIMING TO EVIDENCED RELIABILITY CONCERNS IN NON-HERMETIC APPLICATIONS. BY CONTINUOUSLY MONITORING A LARGE SET OF DCPARAMETERS, SIGNIFICANT DEGRADATIONS OF SOME OF THEM, SUCH AS IDSS, PINCH-OFF VOLTAGE AND SERIES RESISTANCES, WERE DETECTED. FAILURE ANALYSIS OF THE AGED DEVICES EVIDENCED MANY DIFFERENT MODIFICATIONS, ORIGINATED BY THE VARIOUS OCCURRENCE OF FOUR BASIC PHENOMENA: AL GATE CATHODIC CORROSION, AU ANODIC CORROSION IN OHMIC CONTACTS, AS DISSOLUTION AT THE EXPOSED GAAS SURFACE AND NI EXTRUSION.				
891110	IDENTIFICATION OF PACKAGE DEFECTS IN PLASTIC-PACKAGED SURFACE-MOUNT ICS BY SCANNING ACOUSTIC MICROSCOPY	MOORE,T.M.	TEXAS INSTRUMENTS	PROCEEDINGS, (1989) ISTFA, Pages 61-67	24492-008
	IN RECENT YEARS, THE DEVELOPMENT OF VERY LARGE SCALE INTEGRATION (VLSI) HAS PROMOTED SIGNIFICANT INCREASES IN THE RATIO OF FUNCTIONALITY-TO-COST IN MODERN INTEGRATED CIRCUITS AND COMPONENT ASSEMBLIES.THIS PROGRESSION HAS LED TO THE PACKAGING OF LARGER AREA AND HIGHER PIN-COUNT DIES IN MORE COMPACT AND CONVENTIONAL INSERTION MOUNTING, ONLY THE EXPOSED LEADS ARE DIRECTLY EXPOSED TO HIGH TEMPERATURE. IN SURFACE MOUNTING, HOWEVER, THE PACKAGE ITSELLF IS EXPOSED TO MOLTEN SOLDER TEMPERATURES. DURING THIS EXPOSURE, THE MECHANICAL TOLERANCES OF THE INTEGRATED CIRCUIT (IC) PACKAGE MAY BE EXCEEDED.				

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891110	PIN-HOLE FAILURE ANALYSIS OF PLASTIC-BASED MAGNETO-OPTICAL DISK	TAKEDA,Y. SAKAMOTO,S. SUMI,S.	SANYO ELECTRIC CO., LTD.	PROCEEDINGS, (1989) ISTFA, Pages 223-229	24492-027
	THE RELIABILITY OF AN ERASABLE OPTICAL MEMORY DISK CONSISTING OF AN AMORPHOUS FILM OF RARE-EARTH-TRANSITION METAL SANDWICHED BETWEEN PROTECTIVE FILMS HAS BEEN STUDIED. THE LIFE OF THIS DISK IS LIMITEDBY MICROSCOPIC CORROSION, A SO-CALLED PIN-HOLE DEFECT WHICH INCREASES THE RATE OF ERROR OF THE DISK. THE CAUSE OF THIS DEFECT WAS ANALYZED BY A NEW SEM OBSERVATION TECHNIQUE. THIS OBSERVATION TECHNIQUE UTILIZES THE DECREASED ELECTRICAL CONDUCTIVITY OF THE METAL FILM CAUSED BY CORROSION, AND PROJECTS A CHARGED CONTRAST IMAGE OF THE CORRODED REGION OF THE FILM.				
891106	IDENTIFICATION OF PACKAGE DEFECTS IN PLASTIC-PACKAGED SURFACE-MOUNT IC'S BY SCANNING ACOUSTIC MICROSCOPY	MOORE, T.M.	TI	PROCEEDINGS, (1989) ISTFA, Pages 61-67	89-20
891106	NON-DESTRUCTIVE FAILURE ANALYSIS OF IC'S USING SCANNING ACOUSTIC TOMOGRAPHY (SCAT) AND HIGH-RESOLUTION X-RAY MICROSCOPY (HRXM)	VAN DER WUK, A. VANDOORSELAER, K.	PHILIPS RESEARCH LABORATORIES, (EINDHOVEN, THE NETHERLANDS)	PROCEEDINGS, (1989) ISTFA, Pages 69-74	89-21
891100	Q-BAND FET POWER AMPLIFIERS, FINAL REPORT FOR PERIOD DECEMBER 1985 - MARCH 1989	CHYE,P. PRIORIELLO,R. MALBON,R.M.	AVANTEK, INC.		24452-000
	THIS FINAL REPORT DESCRIBES THE DESIGN, FABRICATION AND CHARACTERIZATION OF GAAS FETS, GAAS MMICS AND FULLY FUNCTIONAL HERMETICALLY SEALED POWER AMPLIFIERS FOR Q-BAND APPLICATIONS. BEST RESULTS INCLUDED A SATURATED OUTPUT POWER FOR THE AMPLIFIERS AT +26.9 DBM WITH A GAIN OF 30 DB IN THE BAND OF INTEREST. SIX ENGINEERING MODEL AMPLIFIERS WERE FABRICATED, CHARACTERIZED AND DELIVERED. THE OUTPUT POWER STAGE USED A PAIR OF GAAS MMIC CHIPS EACH WITH A GATE PERIPHERY OF 640 MICROMETERS. OUTPUT POWER DENSITY FOR THE MMIC CHIPS WAS 0.57 DBM/MM.				
891000	IMAGING OF PACKAGING-RELATED PROBLEMS IN ELECTRONIC COMPONENTS BY SCANNING ACOUSTIC MICROSCOPY	WILSON, K.J., SUTHERLAND, R.R. VIDELO, I.D.E. WAKEFIELD, B.	BRITISH TELECOM RESEARCH LABORATORIES, (IPSWICH,(SUFFOLK, UK)	QUALITY AND RELIABILITY ENGINEERING INTERNATIONAL, Vol. 5, No. 4, Pages 299-307	89-36
891000	MOISTURE INDUCED FAILURE IN PLASTIC SURFACE MOUNT PACKAGES	LEA, C. TILBROOK, D.	NATIONAL PHYSICAL LABORATORY, (TEDDINGTON, ENGLAND)	SOLDERING AND SURFACE MOUNT TECHNOLOGY, No. 3, Pages 30-34	89-6
890928	ESD POLYMER ALLOYS - A NOVEL APPROACH FOR PERMANENTLY STATIC DISSIPATIVE THERMOPLASTICS	MASS,T. WOODS,M. LEE,B.	UNKNOWN	1989 EOS/ESD SYMPOSIUM PROCEEDINGS, Pages 89-94	24310-015
	POLYMER ALLOYING IS STUDIED TO OVERCOME SOME OF THE PROPERTY TRADE-OFFS REPORTED FOR TRADITIONAL METHODS FOR MAKING PLASTICS STATIC DISSIPATIVE. RELIABILITY OF CURRENT STATIC DISSIPATIVE PLASTICS HASBEEN QUESTIONED IN PREVIOUS EOS/ESD PAPERS BECAUSE OF THE VOLATILITY AND SOLUBILITY OF THE CHEMICAL ANTISTATIC ADDITIVES. THE SLOUGHING OF CONDUCTIVE PARTICLES FROM FILLER LOADED PLASTICS CAUSES OTHERPROBLEMS.				
890925	NONDESTRUCTIVE EVALUATION OF DE-BONDING WITHIN PLASTIC INTEGRATED CIRCUIT PACKAGES USING DIFFERENT METHODS OF ACOUSTIC MICROSCOPY	SEMMENS, J.E. KESSLER, L.W.	SONOSCAN, (BENSENVILLE, IL)	PROCEEDINGS, 7TH (1989) IEMTS, Pages 322	89-9
890925	PLASTIC PACKAGE MOISTURE ABSORPTION HAZARDS IN SMT BOARD ASSEMBLY	SAINT-MARTIN, X. JOLY, J.	BULL SA	PROCEEDINGS, 7TH (1989) IEMTS, Pages PAGES 38-42	89-7
890900	ACOUSTIC MICROSCOPY: A KEY INSPECTION TOOL FOR IMPROVING THE RELIABILITY OF SURFACE MOUNT CAPACITORS AND PLASTIC IC PACKAGES	SANTANGELO, L.J. KESSLER, L.W.	SONOSCAN, (BENSENVILLE, IL)	SURFACE MOUNT TECHNOLOGY, Pages 39-43	89-8
890900	HIGH DENSITY PACKAGING TECHNOLOGY: ULTRA THIN PACKAGE AND NEW TAB PACKAGE	NAKAGAWA, O., SHIMAMOTO, H. UEDA, T., SHIMOMURA, K., HATA, T., TACHIKAWA, T.	MITSUBISHI ELECTRIC CORPORATION	J. ELECTRONIC MATERIALS, Vol. 18, Pages 633-643	89-15
890900	HIGHLY RELIABLE DIE ATTACHMENT ON POLISHED GAAS SURFACES USING GOLD-TIN EUTECTIC ALLOY	LEE, C.C. MATIJASEVIC, G.S.	UC, (IRVINE,CA)	TRANSACTIONS, IEEE/CHMT, Vol. 12, No. 3, Pages 406-409	89-17
890900	WATER SORPTION IN EPOXY THIN FILMS	MCMASTER, M.G. SOANE, D.S.	UC, (BERKELEY,CA)	TRANSACTIONS, IEEE/CHMT, Vol. 12, No. 3, Pages 373-386	89-22
890829	PRECONDITIONING OF PLASTIC SURFACE MOUNT COMPONENTS TO SIMULATE SOLDER REFLOW PRIOR TO RELIABILITY STRESSING	CLIFTON, L.	INTEL	PROCEEDINGS, SURFACE MOUNT '89, Pages 733-742	89-4

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890829	SURFACE MOUNT DEVICE PACKAGE CRACKING: AN OVERVIEW	MCKENNA, R.	TI	PROCEEDINGS, SURFACE MOUNT '89, Pages 711-722	89-3
890800	SCANNING ACOUSTIC TOMOGRAPHYC (SAT) - A NEW TECHNIQUE TO EVALUATE THE SI CHIP/PLASTIC ENCAPSULANT/LEADFRAME INTERFACES	BIRUDAVOUL, R.	NSC	PROCEEDINGS, SURFACE MOUNT '89, Pages 29-31	89-2
890700	CODES AND IC FIRE HAZARDS	CAMPBELL,R.J.	SANTA CLARA FIRE DEPARTMENT	SOLID STATE TECHNOLOGY, Vol. 32, No. 7, Pages 93-94	23687-008
	PREDICTABLE TRACK RECORDS HAVE BEEN ESTABLISHED FOR MANY OF THE HAZARDS PRESENT IN MANUFACTURING INTEGRATED CIRCUITS. FOR EXAMPLE, THE INDUSTRY'S TWO MOST FREQUENT FIRES OCCUR IN HEATED SINKS THAT DON'T HAVE PROPER PROTECTIVE DEVICES AND IN COMBUSTIBLE (PLASTIC) EXHAUST DUCTS USED TO CONVEY FLAMMABLE VAPORS. CODES AFFECTING THESE AND OTHER HAZARDS PRESENT IN I.C. FABS HAVE CHANGED DRASTICALLY INTHE PAST SEVERAL YEARS.				
890600	A PRACTICAL ASSESSMENT OF CURRENT PLASTIC ENCAPSULATED MICROELECTRONIC DEVICES	HUGHES,J.	BRITISH TELECON MATERIALS/COMPONENTS CTR	QUALITY AND RELIABILITY ENGINEERING, Vol. 5, No. 2, Pages 125-129	24303-004
	THE USE OF PLASTIC ENCAPSULATED DEVICES (PEDS) FOR A VARIETY OF MARKET SECTORS HAS BEEN THE SUBJECT OF MUCH DISCUSSION OVER THE PAST TWO DECADES. THE ADVANTAGES OF LOWER COST TOGETHER WITH THE INHERENT MECHANICAL RUGGEDNESS OF THESE NON-CAVITY PACKAGES HAVE BEEN WEIGHED AGAINST THE CONCERNS OVER QUALITY AND RELIABILITY AND, IN PARTICULAR, ELECTRICAL OPERATION AT EXTREMES OF TEMPERATURE. THIS PAPERPRESENTS THE RESULTS OF SOME PRACTICAL WORK UNDERTAKEN ON A MODERN LSI DEVICE IN A PLASTIC LEADED CHIP CARRIER PACKAGE.				
890522	DETERMINATION OF THERMALLY INDUCED DEFORMATIONS IN ELECTRONIC PACKAGES BY MOIRE' INTERFEROMETRY	BASTAWROS, A.F. VOLOSHIN, A.S. RODOGOVESKI, P.	LEHIGH UNIVERSITY	PROCEEDINGS, 39TH (1989) IEEE/CHMT ECC, Pages 864-868	89-33
890522	EFFECT OF LEAD FRAME MATERIAL ON PLASTIC-ENCAPSULATED IC PACKAGE CRACKING UNDER TEMPERATURE CYCLING	NISHIMURA, A. KAWAI, S. MURAKAMI, G.	HITACHI, LTD.	PROCEEDINGS, 39TH (1989) IEEE/CHMT ECC, Pages 524-530	89-31
890522	HIGH IMPACT BONDING TO IMPROVE RELIABILITY OF VLSI DIE IN PLASTIC PACKAGES	MCKENNA, R.G. MAHLE, R.L.	TI	PROCEEDINGS, 39TH (1989) IEEE/CHMT ECC, Pages 424-427	89-28
890522	HIGH-RELIABILITY EPOXY MOLDING COMPOUND FOR SURFACE-MOUNTED DEVICES	KUROKI, S. OOTA, K.	SUMITOMO BAKELITE COMPANY LIMITED	PROCEEDINGS, 39TH (1989) IEEE/CHMT ECC, Pages 885-891	89-35
890522	IMPROVEMENT OF MOISTURE RESISTANCE IN PLASTIC ENCAPSULANTS MOS-IC BY SURFACE FINISHING COPPER LEADFRAME	YOSHIOKA, O., OKABE, N. NAGAYAMA, S., YAMAGISHI, R. MURAKAMI, G.*	DENSEN WORKS, HITACHI CABLE, *MUSAHI WORKS, (TOKYO, JAPAN)	PROCEEDINGS, 39TH (1989) IEEE/CHMT ECC, Pages 464-471	89-30
890522	LOW-STRESS ENCAPSULATION RESIN FOR VLSI	NISHIOKA, T., SUZUKI, H. ADACHI, J., TAKI, H., IKO, K. YAMANAKA, K., SHIMIZU, M.,	NITTO DENKO CORPORATION	PROCEEDINGS, 39TH (1989) IEEE/CHMT ECC, Pages 881-884	89-34
890522	STRAIN GAUGE MAPPING OF DIE SURFACE STRESSES	GEE, S.A. VAN DEN BOGERT, W.F. AKYLAS, V.R., SHELTON, R.T.	SIGNETICS	PROCEEDINGS, 39TH (1989) IEEE/CHMT ELECT. COMP. CONFEREN, Pages 343-349	89-27
890522	STRESS EFFECTS OF PACKAGE PARAMETERS ON 4 MEGA DRAM WITH FRACTIONAL, FACTORIAL-DESIGNED FINITE ELEMENT ANALYSIS	ROMER, B. PAPE, H.	SIEMENS AG	PROCEEDINGS, 39TH (1989) IEEE/CHMT ELECT. COMP. CONFEREN, Pages 832-839	89-32
890522	THE INFLUENCE OF THE OPERATING MODE OF IC-DEVICES ON THEIR LIFETIME	JOHNSSON, P. VON SCHEELE, C.	THE SWEDISH INSTITUTE OF PRODUCTION ENGINEERING RESEARCH	PROCEEDINGS, 39TH (1989) IEEE/CHMT ELECT. COMP. CONFEREN, Pages 335-342	89-26
890522	THE STUDY OF PLASTIC PACKAGE CRACKING INDUCED BY THE MOISTURE/SOLDER REFLOW PROCESS	KITAGAWA, H., KIDO, Y. MAEDA, K., UMEDA, H. SANO, H., HASEGAWA, S.	TI, JAPAN LIMITED	PROCEEDINGS, 39TH (1989) IEEE/CHMT ELECT. COMP. CONFEREN, Pages 445-459	89-29

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890511	HIGH FREQUENCY ULTRASONIC VISUALIZATION AND CHARACTERIZATION OF MULTILAYER CERAMIC CAPACITORS BY MEANS OF SLAM	KESSLER, L.W. SEMMENS, J.E.	SONOSCAN, (BENSENVILLE, IL)	PROCEEDINGS, SYMPOSIUM ON MLC RELIABILITY	89-25
890500	CAN YOU FIND RELIABILITY IN A PLASTIC PIN GRID ARRAY?	WELLS,V.F.	INDY ELECTRONICS, INC.	SEMICONDUCTOR INTERNATIONAL, Vol. 12, No. 6, Pages 214-218	23682-002

WE SORTED THROUGH DOZENS OF COMBINATIONS OF PINS, LIDS, SUBSTRATES, WIRES, ENCAPSULANTS, AND PLATINGS TO DETERMINE WHICH PROVIDED THE BEST RELIABILITY. MANY DIFFERENT PACKAGE MATERIALS, METHODS AND VENDORS ARE AVAILABLE FOR PLASTIC PIN GRID ARRAYS (PPGAS). HERE, WE EXAMINE A NUMBER OF KEY OPTIONS FOR MATERIALS AND PROCESSES, TO DETERMINE WHICH COMBINATIONS PROVIDE RELIABILITY EQUAL TO OR BETTER THAN A PLASTIC LEADED CHIP CARRIER (PLCC).

890428	DESIGN FOR MANUFACTURABILITY IN HERMETIC PRODUCT DIE ATTACH	OWENS,N.L.	MOTOROLA, INC.	MICROELECT PKG TECH MAT & PROC CONF, Pages 67-71	23999-012

DIE ATTACHMENT FOR LARGE DIE IN HERMETIC PRODUCT IS REVIEWED AS A CASE STUDY IN DESIGN FOR MANUFACTURABILITY. PERFORMANCE GOALS ARE ESTABLISHED AS OPTIMUM THERMAL DISSIPATION AND MECHANICAL ADHESION MEETING MILITARY STANDARD 883, DIE SHEAR METHOD 2019, AS AN ADHESION BASELINE. A BREIF REVIEW OF MANUFACTURING GOALS IS COVERED. ADHESION MEASUREMENT TECHNOLOGIES ARE REVIEWED WITH EMPHASIS GIVEN TO PRACTICAL PRODUCTION APPLICATION. DIE ATTACHMENT TECHNOLOGY IS BREIFLY SURVEYED TO IDENTIFY PROCESS CHARACTERISTICS AMONG SOLDER, EUTECTIC, AND GLASS DIE ATTACHMENTS.

890428	NEW BONDING WIRE DEVELOPMENTS	DOUGLAS,P.	AMERICAN FINE WIRE CORPORATION	MICROELECT PKG TECH MAT & PROC CONF, Pages 31841	23999-002

RECENT DEVELOPMENTS IN THREE AREAS OF BONDING WIRE TECHNOLOGY ARE PRESENTED. BOND NECK GRAIN SIZE AND BOND PULL STRENGTH VALUES ARE REPORTED TO CHARACTERIZE THE PERFORMANCE OF THREE TYPES OF GOLD WIREBALL BONDED UNDER VARIOUS CONDITIONS. BALL MICROHARDNESS MEASUREMENTS FOR VARIOUS BALL-BONDED COPPER WIRES ARE PRESENTED IN COMPARISON TO TYPICAL VALUES FOR GOLD WIRES. THE PERFORMANCE UNDER "PRESSURE COOKER" CONDITIONS IS REPORTED FOR TWO NEW CORROSION RESISTANT ALUMINUM-BASED BONDING WIRES DEVELOPED FOR POWER DEVICES PACKAGED IN PLASTIC.

890428	ONE-STEP-MATCHED SEALS: A NEW PROCESS FOR MANUFACTURING HYBRID MICROCIRCUIT PACKAGES	BANDYOPADHYAY,N. TAMHANKAR,S. KIRSCHNER,M.	BOC GROUP TECHNICAL CENTER	MICROELECT PKG TECH MAT & PROC CONF, Pages 41-47	23999-008

CONVENTIONALLY, IN ORDER TO PRODUCE A SEAL WITH DESIRED ELECTRICAL, MECHANICAL AND HERMETIC PROPERTIES. KOVAR PARTS ARE FIRST DECARBURIZED, THEN A THIN OXIDE LAYER IS GROWN ON THEIR SURFACES. A SEAL IS THEN MADE BY FUSING THE THIN OXIDE LAYERS WITH MOLTEN GLASS. CURRENTLY THIS IS ACHIEVED THROUGH THREE CONSECUTIVE PROCESS STEPS, NAMELY DECARBURIZATION, OXIDATION AND SEALING. BY INVESTIGATING THESEPROCESS CONDITIONS, WE HAVE DISCOVERED A NOVEL PROCESS WHEREBY THE THREE CONVENTIONAL STEPS HAVE BEEN CONSOLIDATED INTO A SINGLE-FIRING, SINGLE-ATMOSPHERE SEALING PROCESS.

890428	ROOM TEMPERATURE LOW CYCLE FATIGUE OF A HIGH PB SOLDER (INDALLOY 151)	SOLOMON,H.D.	GENERAL ELECTRIC CO.	MICROELECT PKG TECH MAT & PROC CONF, Pages 135-146	23999-020

THIS PAPER DESCRIBES THE LOW CYCLE FATIGUE BEHAVIOR OF INDALLOY 151 SOLDER TESTED AT 35 DEGREES C. STRAIN CYCLING WAS DONE IN SIMPLE SHEAR WITH FIXED PLASTIC STRAIN. THIS DROP IN LOAD IS THUS A MEASURE OF THE FATIGUE PROCESS, WITH FAILURE VARIOUSLY DEFINED AS THE NUMBER OF CYCLES TO PRODUCE A 10, 25, 50 OR 90% DROP IN THE HYSTERSIS LOAD. THUS SEVERAL STRAIN LIFE CURVES ARE DEVELOPED, ONE FOR EACHDEFINITION OF FAILURE. THESE FATIGUE CURVES ARE DIFFERENT AND ARE DISPLACED ACCORDING TO THE DEFINITION OF FAILURE.

890428	USING DESIGNED EXPERIMENTS TO CONTROL SENSOR OUTPUT THROUGH PROCESS CONTROL	GEHMAN,R.W.	HONEYWELL CO.	MICROELECT PKG TECH MAT & PROC CONF, Pages 387-395	23999-049

WHEN USING HYBRID MICROELECTRONIC DEVICES AS SENSORS, THE PACKAGING DESIGN AND CONSTRUCTION HAVE A DIRECT AND SIGNIFICANT INFLUENCE ON SENSOR OUTPUT. MATERIALS, CONFIGURATION, AND PROCESSES ALL INTERACT IN DETERMINING BOTH SPECIFIC OUTPUT VALUES AND AMOUNT OF VARIANCE IN A NON-LINEAR OUTPUT. A RECENTLY DEVELOPED THIN FILM SENSOR WAS PACKAGED AS A THICK FILM HYBRID IN A PLASTIC PACKAGE. DURING DESIGN DEVELOPMENT WE FOUND THAT PACKAGE VARIABLES WERE DOMINANT OVER THIN FILM LOTS IN DETERMINING OUTPUT CHARACTERISTICS.

890426	MOISTURE RESISTANCE OF EPOXY RESIN USED FOR EXTREMELY LOW PROFILE IC MODULES	HIRAYAMA, H. TOTSUKA, N. NAMBU, S.	OKI ELECTRIC INDUSTRY COMPANY	PROCEEDINGS, 6TH (1989) IEMTS, Pages 325-328	89-10
890419	DESIGN OF A NEW TWIN-RELAY AND ITS PERFORMANCE FOR AUTOMOTIVE APPLICATIONS	IDE,T. GOTO,H. ONO,T.	NEC CORPORATION	PROCEEDINGS, 37TH (1989) RELAY CONFERENCE, Pages 6-1 THRU 6-9	25123-006

THE ADVANCING HIGH RELIABILITY TECHNOLOGY AND THE COST EFFECTIVE PRODUCTION FEASIBILITY IN RECENT YEARS FOR PLASTIC SEALED RELAYS TO BE MOUNTED ON PRINTED CIRCUIT BOARDS HAVE GREATLY PROMOTED THE USEFULNESS OF THESE RELAYS IN THE FIELDS OF COMMUNICATIONS, AUTOMOTIVE APPLICATIONS, AND HOME ELECTRONIC APPLIANCES.

890419	RESEARCH ON THE STANDARDIZATION OF HERMETIC CAPABILITY FOR HERMETICALLY SEALED RELAY	XIU-MING,H. ZHENG,H.	40TH RESEARCH INSTITUTE	PROCEEDINGS, 37TH (1989) RELAY CONFERENCE, Pages 7-1 THRU 7-4	25123-007

THIS PAPER STUDIES THE HERMETIC QUALITYI AND ITS INDEX OF HERMETICALLY SEALED RELAY. THROUGH THE PREDICTION OF GAS CHANGES INSIDE THE CAVITY OF HSR ON RELAY PRODUCTION LINE AND THE STUDY OF ORIGINAL TECHNOLOGICAL WATER VAPOR CONTENT AND ITS CHANGE, THE MUTUAL RELATIONS WITH REQUIREMENTS BETWEEN THE HERMETIC CAPABILITY, HERMETIC TECHNOLOGY AND THE RATIONAL INDEX OF HERMETIC CAPABILITY HAVE BEEN DEMONSTRATED.

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890413	IMPROVED EPROM MOISTURE PERFORMANCE USING SPIN-ON-GLASS (SOG) FOR PASSIVATION PLANARIZATION	GAETA,J.S. WU,K.J.	INTEL CORPORATION	PROCEEDINGS, 27TH (1989) ANNUAL RELIABILITY PHYSICS, Pages 122-126	24490-021

PLASTIC ENCAPSULATED EPROM MOISTURE RELIABILITY IS CONTINGENT ON GOOD PASSIVATION INTEGRITY. STEP COVERAGE OF PASSIVATION BECOMES AN ISSUE WHEN ARRAY METAL PITCH IS REDUCED IN HIGH DENSITY EPROMS. PLANARIZING THE PASSIVATION WITH AN INTERMEDIATE SPIN-ON-GLASS (SOG) LAYER IS SHOWN TO REDUCE THE LONG TERM STEAM FAILURE RATE BY 3X AND THUS IMPROVE EPROM PERFORMANCE IN MOISTURE.

890413	ON-CHIP MEASUREMENT OF PACKAGE-RELATED METAL SHIFT USING AN INTEGRATED SILICON SENSOR	BOSSCHEE,A.	DELFT UNIVERSITY OF TECHNOLOGY	PROCEEDINGS, 27TH (1989) ANNUAL RELIABILITY PHYSICS, Pages 127-130	24490-022

THE CONTINUAL TREND TO INCREASE THE SCALE OF INTEGRATION OF VLSI CIRCUITS FORCES THE DESIGN OF EVER LARGER SEMICONDUCTOR DEVICES WITH EVER FINER STRUCTURES. PLASTIC ENCAPSULATION OF THESE DEVICES IS ECONOMICALLY ATTRACTIVE BECAUSE OF THE LOWER COST. HOWEVER, THE LARGE MISMATCH IN THERMAL EXPANSION COEFFICIENTS OF SILICON AND THE AVAILABLE ENCAPSULANTS INTRODUCES SEVERE STRESSES ACTING AT THE CHIPSURFACE THAT MIGHT LEAD TO STRESS-INDUCED FAILURES.

890300	RELIABILITY OF PLASTIC-ENCAPSULATED LOGIC CIRCUITS	OLSSON,C.	ERICSSON DEFENSE & SPACE SYSTEMS	QUALITY AND RELIABILITY ENGINEERING, Vol. 5, No. 1, Pages 53-72	23459-008

FAMILIES OF PLASTIC-ENCAPSULATED LOGIC CIRCUITS HAVE BEEN SUBJECTED TO A QUALIFICATION PROCEDURE. THE AIM WAS TO QUALIFY THEM FOR USE IN TELECOMMUNICATION EQUIPMENT IN A CENTRAL OFFICE ENVIRONMENT. THE QUALIFICATION WAS BASED ON A LARGE NUMBER OF RELIABILITY TESTS PERFORMED BY THE EROCSSON FAILURE ANALYSIS LABORATORY AND BY THE VENDORS THEMSELVES. RELIABILITY MONITORING DATA FROM THE TESTING OF MORE THAN 150,000 DEVICES DURING THE PERIOD 1984 TO 1985 HAVE BEEN ANALYSED. LIFE TESTS, SUCH AS "HIGH TEMPERATURE OPERATING LIFE", "HIGH HUMIDITY OPERATING LIFE", & TEMPERATURE CYCLING WERE PERFORMED.

890300	VOID-FREE AU-SN EUTECTIC BONDING OF GAAS DICE AND ITS CHARACTERIZATION USING SCANNING ACOUSTIC MICROSCOPY	MATIJASEVIC, G.S. LEE, C.C.	UC, (IRVINE, CA)	J. ELECTRONIC MATERIALS, Vol. 18, No. 2, Pages 327-337	89-18
890210	COMPARING HAST RESULTS OF DIFFERENTLY PRETREATED PLASTIC ENCAPSULATED INTEGRATEDCIRCUITS	FOKKENS,K. LOUS,A.	UNKNOWN	MICROELECTRONICS AND RELIABILITY, Vol. 29, No. 6, Pages 1003-1009	24253-011

ACCELERATED MOISTURE TESTS ARE PERFORMED WITH A CMOS DEVICE. TEST RESULTS ARE COMPARED TO DEVICES PRETREATED WITH SOLDERDIPPING AND/OR THERMAL CYCLING AND UNTREATED PARTS. THE ONSET OF CORROSION AND OF ELECTRICAL DEGRADATION WAS DETERMINED. PRETREATING DID NOT APPRECIABLY ACCELERATE THE TESTS. IN ALL CASES CORROSION STARTED ABOUT 100 HOURS BEFORE NOTICEABLE ELECTRICAL DEGRADATION.

890200	ARE SMT SOLDER JOINTS RELIABLE?	MARKSTEIN,H.W.	NONE	ELECTRONIC PACKAGING AND PRODUCTION, Vol. 29, No. 2, Pages 66-69	23213-001

SOLDER-JOINT RELIABILITY IN ELECTRONICS ASSEMBLY HAS ALWAYS BEEN A TOPIC OF HIGH INTEREST, BUT FOR SURFACE-MOUNT TECHNOLOGY (SMT) THE SUBJECT HAS BECOME CRUCIAL. THE SHEAR STRESSES AND PLASTIC DEFORMATION UNDER THERMAL CYCLING CAUSE EVENTUAL CRACKING AND FAILURE OF SMT SOLDER JOINTS. ALTHOUGH LEADS ON CHIP CARRIERS, SOTS AND SOICS PROVIDE COMPLIANCE AND REDUCE THE MAGNITUDE OF THE SHEAR FORCES THAT WOULD BE INDUCED BY LEADLESS DEVICES, THERE WILL STILL BE SOME FORCES PRESENT THAT CAUSE CREEP STRAINS AND STRESS RELAXATION UNDER OF/OFF POWER CYCLING.

890200	TECHNIQUES IN THE DEVELOPMENT OF HIGH RELIABILITY, HIGH DENSITY SURFACE MOUNT PACKAGES, AND RECOMMENCATIONS FOR THEIR USE	NURSER, H.	MITSUBISHI SEMICONDUCTORS, UK	INTERNAL REPORT, Pages 13	89-11
890100	CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST (TEST METHOD A100-A)	ANON.	JEDEC (JESD22-A100-A)		22925-000

THE CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST IS PERFORMED FOR THE PURPOSE OF EVALUATING THE RELIABILITY OF NONHERMETIC PACKAGED SOLID-STATE DEVICES IN HUMID ENVIRONMENTS. IT EMPLOYS CONDITIONS OF TEMPERATURE CYCLING, HUMIDITY, AND BIAS WHICH ACCELERATE THE PENETRATION OF MOISTURE THROUGH THE EXTERNAL PROTECTIVE MATERIAL (ENCAPSULANT OR SEAL) OR ALONG THE INTERFACE BETWEEN THE EXTERNAL PROTECTIVEMATERIAL AND THE METALLIC CONDUCTORS WHICH PASS THROUGH IT.

890100	RELIABILITY OF PLASTIC-ENCAPSULATED LOGIC CIRCUITS	OLSSON, C.	ERICCSON TELECOM, (STOCKHOLM, SWEDEN)	QUALITY AND RELIABILITY ENGINEERING INTERNATIONAL, Vol. VOL. 5, No. 1, Pages 53-72	89-37
890100	TRANSMITTER AND RECEIVER FOR APF DATA LINKS	HARADA,Y. IWASHIMA,O. MARUME,M.	NIPPON ELECTRIC COMPANY, LTD.	NEC RESEARCH & DEVELOPMENT, No. 92, Pages 72-76	23460-011

LOW PRICE OPTICAL FIBER DATA LINKS HAVE BEEN USED IN VARIOUS SHORT DISTANCE COMMUNICATION SYSTEMS, MAKING THE BEST USE OF ELECTROMAGNETIC NOISE IMMUNITY, AND BEING GROUND POTENTIAL FREE. NEC HAS DEVELOPED THE LOW PRICE TRANSMITTER AND RECEIVER FOR ALL PLASTIC FIBER (APF) DATA LINKS. THE FEATURES OF THE TRANSMITTER AND THE RECEIVER ARE VERY SIMPLE STRUCTURE WITH TRANSPARENT RESIN MOLDED PACKAGE. THIS PAPER DESCRIBES THE CONFIGURATION AND PERFORMANCE OF THE TRANSMITTER AND THE RECEIVER.

890000	A RELIABILITY STUDY OF AU-SN EUTECTIC BONDING WITH GAAS DICE	MATIJASEVIC, G.S. LEE, C.C.	UC, IRVINE	PROCEEDINGS, IEEE/IRPS, Pages 137-140	89-19

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
890000	ACOUSTIC MICROSCOPY			METALS HANDBOOK, METHODS OF NONDESTRUCTIVE EVALUATION, Vol. 17, No. 9, Pages 465-482	89-1
890000	MOISTURE AND PLASTIC PACKAGE STABILITY	KINSMAN, K.R. JAHSMAN, W.E. SUNDAHL, R.C.	INTEL	ELECTRONIC PACKAGING MATERIALS SCIENCE, Vol. 134, No. 4, Pages 131-141	89-16
890000	MOISTURE CONTENT AND CRACKING OF PLASTIC SURFACE MOUNT PACKAGES	HAGEN, D. TRAN, Z. MIDDLETON, J., DODY, G.	MOTOROLA	SMT EXP '89, Pages 27-31	89-13
890000	PACKING	MINGES, M.L.		ELECTRONIC MATERIALS HANDBOOK, Vol. 1, No. 1	89-5
	SEE ACOUSTIC MICROSCOPY COMMENTS, SEVERAL.				
890000	QUALITY AND RELIABILITY HANDBOOK		SAMSUNG SEMICONDUCTOR	, Pages 78	89-12
890000	ULTRASONIC IMAGING AND DATA PROCESSING TECHNIQUES FOR SEMICONDUCTOR AND NEW MATERIALS	NONAKA, T., HAYAKAWA, Y. TAKEDA, S., IGARASHI, T. TAKISHITA, Y., MIYATA, T.	TECHNICAL RESEARCH LABORATORY, HITACHI CONSTRUCTION MACH.	PROCEEDINGS, 12TH WORLD CONFERENCE, Pages 784-789	89-23
881200	EXPERIMENTAL & STATISTICAL ANALYSES OF SURFACE-MOUNT TECHNOLOGY PLCC SOLDER-JOINT RELIABILITY	LAU,J.H. HARKINS,G. RICE,D.	HEWLETT-PACKARD CO.	IEEE TRANS ON RELIABILITY, Vol. 37, No. 5, Pages 524-530	23191-019
	THE MECHANICAL INTEGRITY OF SURFACE MOUNT TECHNOLOGY (SMT) PLASTIC LEADED CHIP CARRIER (PLCC) SOLDER JOINTS HAS BEEN STUDIED BY A 4-POINT MECHANICAL FLEXURE FATIGUE TEST. THE EFFECTS OF PRINED CIRCUITBOARD (PCB) PAD SURFACE COMPOSITION AND TESTING TEMPERATURE ON SOLDER JOINT RELIABILITY ARE EMPHASIZED. THREE SETS OF PCBS HAVE BEEN TESTED, ONE WITH CU-NI-SN PAD SURFACE METALLURGY, ONE WITH CU-NI-AU, AND ONE WITH SMOBC/SSC (SOLDER MASK OVER BARE COPPER/SELECTIVE SOLDER COATING, OR SIMPLY, SMOBC).				
881200	SCANNING ACOUSTIC MICROSCOPY	ANONYMOUS	SONOSCAN, (BENSENVILLE, IL)	RESEARCH AND DEVELOPMENT MAZAGINE, Pages 33-34	88-40
881104	CHARACTERIZATION OF DIE ATTACH INTEGRITY USING DESTRUCTIVE AND NONDESTRUCTIVE TECHNIQUES	MIRASOLE,M.J.	WESTERN DIGITAL CORP	PROCEEDINGS, (1988) ISTFA, Pages 77-88	23251-010
	NON-DESTRUCTIVE TECHNIQUES ARE OF EXTREME IMPORTANCE IN THAT THEY OFFER A PRACTICAL AND FAST WAY OF ANALYZING FULLY ENCAPSULATED PLASTIC AND CERAMIC CAVITY PACKAGES FOR DIE ATTACH ANOMALIES. THESE TECHNIQUES ARE, HOWEVER, LIMITED AND AT TIMES MUST BE SUPPLEMENTED BY THE DESTRUCTIVE TECHNIQUES DESCRIBED IN THIS PAPER. A COMPLETE DISCUSSION ABOUT EACH OF THE ANALYTICAL TECHNIQUES WITH ADVANTAGES, DISADVANTAGES AND EXPECTED RESULTS ARE DISCUSSED.				
881104	EXPANSION OF FRACTOGRAPHIC DATA BASE FOR CARBON FIBER REINFORCED PLASTICS (CFRP)	YAMASHITA,M.M. HUA,C.T. STUMPFF,P.	BOEING CO.	PROCEEDINGS, (1988) ISTFA, Pages 289-297	23251-038
	THE RESULTS OF THIS INVESTIGATION SHOWED THAT THE MACRO- AND MICROSCOPIC TOPOGRAPHICAL FEATURES ON THE FRACTURE SURFACES OF COMPOSITE LAMINATES CAN BE MODIFIED IN SOME INSTANCES AS A RESULT OF MATERIALS PROCESSING DEFICIENCIES AND EXPOSURE TO ADVERSE ENVIRONMENTAL CONDITIONS, PARTICULARLY AFTER FRACTURE HAD OCCURRED.				
881104	HIGHLY ACCELERATED STRESS TEST ON VLSI PLASTIC COMPONENTS	PEYRARD,O.	IBM CORP.	PROCEEDINGS, (1988) ISTFA, Pages 167-172	23251-022
	A HIGHLY ACCELERATED STRESS TEST (HAST), IS AN ENVIRONMENT OF HIGH TEMPERATURE (>100 DEGREES C) AND UNSATURATED VAPOR WAS COMPARED TO THE CONVENTIONAL TEMPERATURE AND HUMIDITY (TH) TEST. THE EXPERIMENTAL RESULTS DEMONSTRATE A GOOD CORRELATION BETWEEN TH AND HAST TESTING AS WELL FOR THE FAILURE MECHANISMS AS FOR THE KINETICS OF FAILURE APPEARANCES. CHIP CORROSION IN PLASTIC PACKAGE IS THE MAIN FAILURE MECHANISM FOUND. IN ADDITION, THIS METHOD ALLOWS TO DETECT, IN A QUICKER WAY, A SINGLE CELL FAILURE MODE ALSO OBSERVED DURING THE CONVENTIONAL STRESS.				
881104	INSTRUMENTED IMPACT TESTING OF COMPOSITE LAMINATES: DATA ANALYSIS AND INTERPRETATION	JANG,B.Z. CHEN,L.C. ZEE,R.H.	AUBURN UNIVERSITY	PROCEEDINGS, (1988) ISTFA, Pages 265-276	23251-036
	THE IMPACT RESPONSE, INCLUDING LOAD-TIME AND ENERGY-TIME TRACES, OF VARIOUS COMPOSITE LAMINATES WERE INVESTIGATED. IN GENERAL, EACH IMPACT LOAD-TIME CURVE FOR A PLATE-TYPE SPECIMEN, CAN BE DIVIDED INTO THREE STAGES BEYOND THE INITIAL ELASTIC DEFORMATION. THE PREDOMINANT DEFORMATION AND FAILURE MODES IN EACH STAGE OF IMPACT EVENT WERE CHARACTERIZED. THE MATERIALS UTILIZED INCLUDE BOTH THERMOSET ANDTHERMOPLASTIC COMPOSITES REINFORCED WITH VARIOUS HIGH PERFORMANCE FIBERS. SINGLE-COMPONENT LAMINATES AS WELL AS HYBRIDS WERE EXAMINED.				

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
881104	NON-DESTRUCTIVE INSPECTION OF VOIDS IN SILVER HARD SOLDER LAYER OF POWER TRANSISTOR	SHIRAI,K. KOBAYASHI,K. NOGUCHI,T.	FUJI ELECTRIC CO., LTD.	PROCEEDINGS, (1988) ISTFA, Pages 47-52	23251-007

IT IS VERY IMPORTANT TO ASSURE DIE MOUNTING ON METAL STEM OF THE HERMETIC SEAL TYPE POWER TRANSISTOR UNDER THE CONDITION OF TEMPERATURE CYCLING IN THE SPACE APPLICATION. TO REDUCE THE THERMAL STRESS,MOLYBDENUM DISC IS JOINTED ON THE METAL STEM BY USING SILVER HARD SOLDER, BEFORE DIE MOUNTING. SINCE THE EXISTENCE OF VOIDS IN THE SILVER SOLDER INCREASE THE THERMAL RESISTANCE BETWEEN A SILICON PELLET AND A STEM AND DEGRADE THE RELIABILITY OF THE DEVICE, EACH STEM HAS TO BE INSPECTED ACCURATELY FOR THE EXISTENCE OF VOIDS AFTER SOLDERING MOLYBDENUM DISC.

881104	NONDESTRUCTIVE EVALUATION OF THERMALLY SHOCKED PLASTIC INTEGRATED CIRCUIT PACKAGES USING ACOUSTIC MICROSCOPY	SEMMENS,J.E. KESSLER,L.W.	SONOSCAN, (BENSENVILLE, IL)	PROCEEDINGS, (1988) ISTFA, Pages 211-215	23251-028

CRITICAL DEFECTS IN PLASTIC ENCAPSULATED INTEGRATED CIRCUITS THAT HAVE BEEN EXPOSED TO THERMAL SHOCK ARE OBSERVED NONDESTRUCTIVELY WITH ACOUSTIC MICROSCOPY TECHNIQUES. SEPARATIONS OF THE MOLDING COMPOUND FROM THE LEAD FRAME, DIE, AND/OR THE PADDLE, ARE NONTRANSMISSIVE AND HIGHLY REFLECTIVE TO HIGH FREQUENCY ULTRASOUND AND THEREFORE, THEY APPEAR AS HIGH CONTRAST FEATURES IN THE IMAGE. TWO DIFFERENT TECHNIQUES ARE DISCUSSED FOR DETECTING MOLDING COMPOUND DEFECTS: THE TRANSMISSION MODE SCANNING LASER ACOUSTIC MICROSCOPE (SLAM), AND THE REFLECTION C-MODE SCANNING ACOUSTIC MICROSCOPE (C-SLAM).

881104	PLASTIC MOLD OPENER THAT USES FUMING NITRIC ACID AS DISSOLVING LIQUID	YOSHIDA,N. OHTA,H. KAWAI,H.	NIPPON SCIENTIFIC CO., LTD.	PROCEEDINGS, (1988) ISTFA, Pages 137-143	23251-018

DECAPSULATION OF IC/LSI HAS BECOME WIDELY POPULAR AS AN ANALYZING METHOD TO ENSURE THEIR RELIABILITY. HOWEVER, DECAPSULATING IC'S OF PLASTIC MOLD TYPE INVOLVES A VERY DANGEROUS PROCESS, THAT IS, DROPPING OF FUMING NITRIC ACID, AND REQUIRES A HIGH DEGREE OF SKILL TO AVOID INJURING SAMPLES TO BE ANALYZED. IN ORDER TO SOLVE THESE PROBLEMS, WE HAVE DEVELOPED EQUIPMENT THAT ENABLES AUTOMATED DECAPSULATION. WE HERE DESCRIBE THE USE OF THE DEVICE AND CARES TO BE TAKEN IN ITS USE, TOGETHER WITH SOME PROBLEMS IN INCORPORATING IT INTO A SYSTEM AND THEIR SOLUTIONS.

8810331	NONDESTRUCTIVE EVALUATION OF THERMALLY SHOCKED PLASTIC INTEGRATED CIRCUIT PACKAGES USING ACOUSTIC MICROSCOPY	SEMMENS, J.E. KESSLER, L.W.	SONOSCAN, (BENSENVILLE, IL)	PROCEEDINGS, (1988) ISTFA, Vol. 1, MICROELECTRONICS, Pages 211-215	88-27
881031	CHARACTERIZATION OF DIE ATTACH INTEGRITY USING DESTRUCTIVE AND NON-DESTRUCTIVE INSPECTION TECHNIQUES	MIRASOLE, M.J.	WESTERN DIGITAL CORP.	PROCEEDINGS, (1988) ISTFA, Vol. MICROELECTRONICS, Pages 77-88	88-29
881031	NON-DESTRUCTIVE INSPECTION OF VOIDS IN SILVER HARD SOLDER LAYER OF POWER TRANSISTOR	SHIRAI, K. KOBAYASHI, K. NOGUCHI, T., GOKA, T.	FUJI ELECTRIC, NATIONAL SPACE DEVELOPMENT AGENCY/JAPAN	PROCEEDINGS, (1988) ISTFA, Vol. MICROELECTRONICS, Pages 47-52	88-28
881019	PROCESS/PERFORMANCE COMPARISONS OF TWO ELECTRODING SYSTEMS FOR A PERFLUOROCARBONLIQUID/PLASTIC FILM CAPACITOR	HARRIS,J.O.,JR. DELANCY,R.W. FOSTER,J.C.	SANDIA NATIONAL LABORATORIES	CARTS - EUROPE 1988, Pages 155-159	25115-019

TWO ELECTRODING SYSTEMS FOR CAPACITOR ROLLS ARE COMPARED; ONE UTILIZED AG-EPOXY AND THE OTHER UTILIZED ARC-SPRAY TERMINATIONS. FOR THE REQUIRED HIGH-PEAK/HIGH-REVERSAL CURRENT DISCHARGES, THE ARC-SPRAY PROCESS WAS CLEARLY SUPERIOR IN BOTH PERFORMANCE (BASED ON DESTRUCTIVE TESTS) AND MANUFACTURABILITY/COSTS. THESE PERFORMANCE TRENDS WERE CONSISTENT FOR UNITS FABRICATED WITH A WIDE RANGE OF WINDINGTENSIONS AND DIFFERENT EDGE MARGINS.

881019	QUALITY MANAGEMENT FOR POLYESTER FILMS MANUFACTURED FOR THE ELECTRONICS INDUSTRY	HOVERMALE,R.A. SCHUTZ,R.J.	E.I. DU PONT DE NEMOURS AND COMPANY, INC	CARTS - EUROPE 1988, Pages 125-135	25115-015

FROM THE DISCOVERY OF CELLOPHANE BY THE FRENCH AND THE FUNDAMENTAL POLYMER WORK WITH NYLON BY CAROTHERS IN THE EARLY 1930S, A TREMENDOUS MARKET HAS DEVELOPED FOR PLASTICS IN ALL AREAS OF CONSUMER'S LIVES. PLASTIC PELLETS AND POWDERS ARE MOLDED INTO ALL MANNER OF SHAPES SUCH AS PIPES, TOYS, HOUSEHOLD GOODS, AUTOMOTIVE PARTS, APPAREL ITEMS AND THE LIKE. PLASTIC FILMS ARE FOUND IN SUCH ITEMS AS VIDEOTAPES, AUDIO TAPES, CAPACITORS, MOTORS, PACKAGING APPLICATIONS, AND WEATHER BALLOONS.

880929	CORROSION AND CONTAMINATION BY ANTISTATIC ADDITIVES IN PLASTIC FILMS	KOLYER,J.M. GUTTENPLAN,J.D.	ROCKWELL INTERNATIONAL CORP.	1988 EOS/ESD SYMPOSIUM PROCEEDINGS, Pages 99-102	22863-016

ONE COMMERCIAL BRAND OF MIL-B-81705, TYPE II FILM CONTAINED ORGANIC ACID AND CAUSED CORROSION OF SOLDER-COATED DEVICE LEADS ON CIRCUITRY. HOWEVER, SOLDERABILITY WAS UNAFFECTED IN ACCELERATED TESTS. EVEN ACID-FREE ANTISTATS CAN STRESSCRACK POLYCARBONATE, FOG INSTRUMENT MIRRORS, WEAKEN ADHESIVE BONDS, AND DISCOLOR EPOXY PAINT. THESE PROBLEMS ARE REDUCED BY A NEW GENERATION OF TYPE II FILMS.

880929	HOOD IONIZATION IN SEMICONDUCTOR WAFER PROCESSING: AN EVALUATION	MURRAY,K.D. AINSWORTH,G.F. GROSS,V.P.	IBM CORP.	1988 EOS/ESD SYMPOSIUM PROCEEDINGS, Pages 195-200	22863-030

IN A WAFER FABRICATION LINE, TYPICAL WORK STATIONS CONTAIN CHEMICAL RESISTANT PLASTICS, LOW RELATIVE HUMIDITY, AND ION DEPLETED, FILTERED AIR. WITH STATIONS UNDER FULL PRODUCTION, THESE CONDITIONS PROVIDE AN IDEAL ENVIRONMENT FOR ELECTROSTATIC DISCHARGE (ESD) AND ELECTROSTATIC ATTRACTION (ESA). IONIZATION VENDORS CLAIM THAT HIGH STATIC CHARGES ON NON-CONDUCTIVES INSIDE WET-STATION HOODS CAN BE ELIMINATED. THEY ALSO CLAIM THAT BY NEUTRALIZING OBJECTS IN THE WORK AREA AND BY MAINTAINING THE NEUTRALITY, PARTICULATE CONTAMINATION ON WAFERS THROUGH ESA CAN BE REDUCED WITH HIGH VOLTAGE DISCHARGE.

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
880929	TRIBOELECTRICITY AND SURFACE RESISTIVITY DO NOT CORRELATE	FOWLER,S.L.	W.R. GRACE CO.	1988 EOS/ESD SYMPOSIUM PROCEEDINGS, Pages 103-112	22863-017

TRIBOELECTRIC CHARGE GENERATION BY PLASTIC PACKAGING MATERIALS IS WIDELY BELIEVED TO BE DEPENDENT ON THE SURFACE RESISTIVITY OF THE MATERIALS IN QUESTION. IF A MATERIAL HAS A LOW RESISTIVITY IT IS SOMETIMES REGARDED AS HAVING A LOW PROPENSITY FOR CHARGE GENERATION. THIS PAPER PRESENTS DATA THAT CONTRADICTS THIS BELIEF. SURFACE RESISTIVITY AND CHARGE GENERATION CAN NOT BE CORRELATED. THE CONCEPT OFNON-CORRELATION OF RESISTIVITY AND TRIBOELECTRIC CHARGE GENERATION IS NOT NEW. MANY EXPERTS HAVE STATED THIS FACT IN THEIR PAPERS. HOWEVER, THE BELIEF OF A RELATION OF THESE TWO PARAMETERS PERSISTS.

880900	MOISTURE BARRIER BAG CHARACTERISTICS FOR PSMC PROTECTION	POPE, E.	INTEL	PROCEEDINGS, SEMICON-EAST, Pages 59-63	88-22
880900	NO FAILURES ALLOWED	CANNING,T.D.	ROCKWELL INTERNATIONAL CORP.	CIRCUITS MANUFACTURING	22877-000

SURFACE MOUNT TECHNOLOGY HAS BEEN INTRODUCED INTO AVIONICS PRODUCTS TO PROVIDE SMALLER, LIGHTER SYSTEMS WITH A DEGREE OF FUNCTIONAL INTEGRATION OVER PREVIOUS GENERATIONS. PLASTIC SMDS HAVE BEEN USED WHEREVER POSSIBLE, BUT CERTAIN APPLICATIONS IN THE AIR TRANSPORT MARKET REQUIRE THE USE OF HERMETICALLY SEALED SCREENED CERAMIC ICS. BECAUSE THEY WERE THE ONLY AVAILABLE CHOICE, LEADLESS CERAMIC CHIP CARRIERS (LCCS) HAVE BEEN USED TO INCORPORATE SMT IN AIR TRANSPORT PRODUCTS.

880700	STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST (TEST METHOD A101-A)	ANON.	JEDEC (JEDEC NO 22-A101-A)		25260-000

THE STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST IS IPERFORMED FOR THE PURPOSE OF EVALUATING THE RELIABILITY OF NON HERMETIC PACKAGED SOLID STATE DEVICES IN HUMID ENVIRONMENTS. IT EMPLOYS CONDITIONS OF TEMPERATURE, HUMIDITY, AND BIAS WHICH ACCELERATE THE PENETRATION OF MOISTURE THROUGH THE EXTERNAL PROTECTIVE MATERIAL OR ALONG THE INTERFACE BETWEEN THE EXTERNAL PROTECTIVE MATERIAL AND THE METALLIC CONDUCTORS WHICH PASS THROUGH IT.

880613	THE MECHANISM OF PLASTIC PACKAGE CRACKING IN SMT AND TWO SOLUTIONS	SUHL, D. KIRLOSKAR, M. STEINER, T.	DIGITAL EQUIPMENT CORPORATION	PROCEEDINGS, 4TH (1988) ANNUAL IEEE/IEMT/CHMT SYMP, Pages 129-132	88-26
880600	PACKAGING MATERIAL STANDARDS FOR ESD SENSITIVE ITEMS	MURELLO,A.	HARRIS	REVISION OF EIA/S S-A, -A-1	88-39
880600	PLASTIC PACKAGING FOR VLSI-BASED COMPUTERS	BREGMAN,M.F. KOVAC,C.A.	IBM CORP.	SOLID STATE TECHNOLOGY, Vol. 31, No. 6, Pages 75-80	22415-001

LOW-END COMPUTERS HAVE RECENTLY UNDERGONE RAPID GROWTH IN COMPLEXITY AND PERFORMANCE, LARGELY AS A RESULT OF THE INC REASED USE OF VLSI CIRCUITS. IN THIS PAPER, VLSI PACKAGING OPTIONS ARE REVIEWED ANDDISCUSSED IN TERMS OF THE REQUIREMENTS OF THE LOW-END SYSTEM: RELIABILITY, THERMAL REQUIREMENTS, I/O REQUIREMENTS, ELECTRICAL PERFORMANCE, AND COST.

880600	THE MECHANICS OF MOLDED PLASTIC PACKAGES	KINSMAN, K.R. METALS, J.		, Vol. 40, No. 6, Pages 23-29	88-30
880511	FINITE ELEMENT ANALYSIS OF COMPLIANT COATING	SHORAKA,F. GEALER,C. BETTEZ,E.	INTEL CORP.	PROCEEDINGS, 38TH (1988) ECC, Pages 461-467	23189-018

HISTORICALLY, COMPLIANT COATINGS HAVE ENHANCED PLASTIC PACKAGE RELIABILITY BY ACTING AS A BARRIER TO MOISTURE AND PARTICLES. MORE RECENTLY, COATINGS ARE BEING CONSIDERED AS A MEANS TO REDUCE DIE SURFACE STRESSES DUE TO THE MISMATCH OF THERMAL COEFFICIENTS OF EXPANSION OF THE PACKAGE MATERIALS. LOW STRESS MOLDING COMPOUND TECHNOLOGIES HAVE BEEN SUCCESSFUL IN REDUCING DIE SURFACE STRESSES AND IMPROVING PACKAGE CRACKING CHARACTERISTICS OF PLASTIC PACKAGES.

880511	MECHANICAL STRESS AND LIFE FOR PLASTIC-ENCAPSULATED, LARGE-AREA CHIP	LUNDSTROM,P. GUSTAFSSON,K.	ERICSSON DEFENSE & SPACE SYSTEMS	PROCEEDINGS, 38TH (1988) ECC, Pages 396-405	23189-016

IN ORDER TO DEVELOP TEST METHODS FOR QUALIFICATION OF COMMERCIALLY AVAILABLE PLCC PACKAGES, A SPECIAL TEST CIRCUIT HAS BEEN USED. THIS CIRCUIT CONTAINS PIEZO RESISTIVE SENSORS FOR MEASUREMENTS OF MECHANICAL STRESS, RESISTORS FOR POWER DISSIPATION AND DIODES FOR TEMPERATURE MEASUREMENTS. THE MECHANICAL STRESS HAS BEEN MEASURED AFTER DIE ATTACH ON DIFFERENT TYPES OF LEAD FRAMES AND AFTER ENCAPSULATION IN DIFFERENT MOULDING COMPOUNDS. ALLOY 42 LEAD FRAMES GAVE RISE TO LESS MECHANICAL STRESS THAN COPPER LEAD FRAMES.

880511	MOISTURE ABSORPTION AND MECHANICAL PERFORMANCE OF SURFACE MOUNTABLE PLASTIC PACKAGES	BHATTACHARYYA,B.K. HUFFMAN,W.A. JAHSMAN,W.E.	INTEL CORP.	38TH ELECTRONIC COMPONENTS CONF PROC, Pages 49-58	23189-006

SURFACE MOUNTABLE PLASTIC PACKAGES HAVE BEEN GAINING WIDE ACCEPTANCE BECAUSE OF THEIR REDUCED BOARD SPACE, LOWER COST AND EASE OF ASSEMBLY. HOWEVER, SINCE THESE PACAKGES ARE EXPOSED TO EXTREME TEMPERATURES DURING SOLDER REFLOW, THEY ARE SUSCEPTIBLE TO CRACKING IF THEIR MOISTURE CONTENT IS HIGH. THEREFORE, THERE IS A NEED FOR AN UNDERSTANDING OF THE LONG TERM MOISTURE RELIABILITY ISSUES BY BOTH VENDORS AND CUSTOMERS OF THESE PACKAGES.

880500	MOISTURE INDUCED PLASTIC PACKAGE CRACKING	PRASAD, R. NIXON, D. SPALIK, J., FEHR, G.	INTEL, AEROSPACE CORP., IBM, LSI LOGIC	WHITE PAPER, EIA/SPC SURFACE MOUNT COUNCIL	88-24
880500	PLASTIC SURFACE MOUNT COMPONENTS IN DESICCANT PACK FOR SURFACE MOUNT APPLICATIONS	CLIFTON,L., POPE, E. GRAF,C., WIENEKE, K. LEVY,I.	INTEL	INTERNAL DOCUMENT	88-38

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
880426	PACKAGE CRACKING AND MOISTURE ABSORPTION IN PLASTIC SURFACE MOUNT COMPONENTS	SWITKY, A.	NATIONAL SEMICONDUCTOR CORPORATION	INTERNAL DOCUMENT	88-23
880420	A STUDY ON THE DISCHARGE PHENOMENA OF RHODIUM CONTACT REED SWITCHES	YOKOKAWA,T. YANO,T. KAWAKITA,O.	OKI ELECTRIC INDUSTRY CO., LTD.	36TH RELAY CONFERENCE PROCEEDINGS, Pages 14-1-14-7	25122-014

REED SWITCHES HAVE A HERMETICALLY SEALED CONTACT AND SO ARE FREE FROM THE INFLUENCE OF DUST AND MOISTURE IN THE ENVIRONMENT. FOR THIS REASON, THEY HAVE BEEN WIDELY USED IN VARIOUS FIELDS SUCH AS MEASUREMENT AND CONTROL, WHICH REQUIRE HIGH RELIABILITY. ALONG WITH THE RECENT EXPANSION OF THEIR APPLICATIONS, VARIOUS IMPROVEMENTS ARE NOW HIGH BREAKDOWN VOLTAGE. TO ATTAIN HIGH BREAKDOWN VOLTAGE, THE INSIDE OF A GLASS TUBE IS PLACED UNDER HIGH PRESSURE OR IN A VACUUM, THEREBY INCREASING THE FIRING POTENTIAL. HOWEVER, CONTROLLING THE TUBE PRESSURE IS RATHER COMPLICATED AND RAISES COST.

880420	ENGINEERING PLASTICS FOR HIGH PERFORMANCE RELAYS	SOLENBERGER,J.C. PENN,R.E.	UNKNOWN	36TH RELAY CONFERENCE PROCEEDINGS, Pages 17-1 THRU 17-3	25122-017

MARKET NEEDS FOR SMALLER, HOTTER RUNNING COMPONENTS HAVING INCREASED RELIABILITY AND BETTER FLAME RESISTANCE HAVE FORCED SIGNIFICANT CHANGES IN ENGINEERING PLASTICS BEING USED IN HIGH PERFORMANCE RELAYS. WHERE 6.6 NYLON WAS ONCE THE PREDOMINANT PLASTIC USED IN RELAY COIL BOBBINS AND ENCLOSURES, NEW RELAY ASSEMBLIES ARE INCREASINGLY BEING SPECIFIED IN THERMOPLASTIC POLYESTERS, INITIALLY PBT POLYESTERS AND NOW PET POLYESTERS. ANOTHER TYPE OF POLYESTER, THE AMORPHOUS POLYVARYLATES, ARE ALSO UNDER STUDY AS A POSSIBLE CANDIDATE FOR SOLID STATE SYSTEMS.

880420	EVALUATION OF THE INFLUENCE OF ORGANIC VAPORS ON RELAY CONTACTS	GOTTERT,B. RAUTERBERG,U.	SIEMENS AG	36TH RELAY CONFERENCE PROCEEDINGS, Pages 15-1 THRU 15-9	25122-015

THIS PAPER DESCRIBES A METHOD WHICH PERMITS THE DETECTION OF VAPORS EXUDED FROM PLASTICS THAT ARE HARMFUL TO CONTACTS. A TEST APPARATUS WAS DEVELOPED FOR THIS PURPOSE. THE PLASTICS ARE INVESTIGATED ATA TEMPERATURE OF 100 DEGREES C IN RESPECT TO THEIR EFFECT ON AUAG8 CONTACTS WITH AN ELECTRICAL LOAD OF 6 V/100 MA AND ARE CLASSIFIED ON THE BASIS OF THEIR HARMFULNESS. IT CAN BE DEMONSTRATED THAT ADDITIVES HAVE A MAJOR INFLUENCE ON THE VAPOR EXUDATION BEHAVIOR AND THE CONTACT BEHAVIOR.

880400	NOVOLAC ADHESION PROMOTION	SUHL, D. KIRLOSKAR, M.	DEC, FRANKLIN, MA	IC PACKAGE ENGINEERING, Vol. IPC-TP-683	89-24
880331	TI FINDS A NEW WAY TO PREDICT PACKAGE RELIABILITY	LYMAN, J.		ELECTRONICS MAGAZINE, Pages 87-88	88-32

REFERENCES USE OF FINITE ELEMENT ANALYSIS

880310	ANALYSIS OF FILM CAPACITOR MILITARY SPECIFICATIONS	LAMPHIER,W.C.	COMPONENT RESEARCH COMPANY, INC.	CARTS 1988, Pages 21-24	25113-005

THIS PAPER WILL REVIEW AND SUMMARIZE EXISTING ESTABLISHED RELIABILITY MILITARY SPECIFICATIONS FOR HERMETICALLY SEALED FILM CAPACITORS. APPLICATION GUIDELINES WILL BE ESTABLISHED TO HELP THE ENGINEER SELECT THE RIGHT FILM CAPACITOR FOR A SPECIFIC APPLICATION. IN ADDITION SPECIFICATIONS THAT ARE UNDER DEVELOPMENT WILL ALSO BE DESCRIBED.

880310	MINIATURIZED HERMETICALLY SEALED FILM CAPACITORS - A NEW DESIGN	KELLERMAN,H.J.	COMPONENT RESEARCH COMPANY, INC.	CARTS 1988, Pages 178-182	25113-021

THIS PAPER DESCRIBES A NEW GENERATION HEREMTICALLY SEALED CAPACITOR WHICH HAS THE DUAL BENEFITS OF MINIATURE SIZE AND INCREASED HIGH TEMPERATURE PERFORMANCE.

880300	ULTRA LOW STRESS COMPOUND FOR VLSI			SUMITOMO INTERNAL REPORT	88-37
880200	MASTERING ESD PLASTICS IN STATIC CONTROL PRODUCT MARKETS	MOONEY,P.J.	BUSINESS COMMUNICATIONS CO., INC.	EMC TECHNOLOGY, Vol. 7, No. 1, Pages 14-16	21838-001

IT IS WELL KNOWN THAT WITH THE GROWTH OF THE WORLDWIDE MICROELECTRONICS INDUSTRY THERE HAS BEEN A CONCOMITANT GROWTH IN THE HAZARD TO ELECTRONIC EQUIPMENT POSED BY ELECTROSTATIC DISCHARGE (ESD). THISTHREAT TO ELECTRONIC EQUIPMENT HAS GIVEN RISE TO A WHOLE NEW MARKET FOR STATIC CONTROL PRODUCTS, NAMELY: FILM BAGS, CUSHIONING FOAM; RIGID CONTAINERS AND MATERIAL HANDLING EQUIPMENT; SPECIALLY CONSTRUCTED WORK BENCHES AND DESK TOPS; WRIST STRAPS AND HEEL GROUNDERS; AIR IONIZERS; SPECIALTY CLOTHING; AND OTHER SURFACES AND ITEMS THAT OPERATIVES CAN CONTACT ON THE FACTORY FLOOR AND IN THE WORKPLACE.

880000	A NEW BOND FAILURE 'WIRE CRATER' IN SMD	KOYAMA, H., SHIOZAKI, H. OKUMURA, I., MIZUGASHIRA, S. HIGUCHI, H., AJIKI, T.	MATSUSHITA/PANASONIC	PROCEEDINGS, (1988) IRPS, Pages 59-63	88-3
880000	ACOUSTIC MICROSCOPY- AN INDUSRTRIAL VIEW	KESSLER, LAWRENCE W.	SONOSCAN, BENSENVILLE, IL	PROCEEDINGS, (1988) IEEE/ULTRASONICS SYMPOSIUM, Pages 725-728	88-35
880000	ANALYSIS OF PACKAGE CRACKING DURING REFLOW SOLDERING PROCESS	KITANO, M., NISHIMURA, A. KAWAI, S. NISHI, K.	HITACHI MECHANICAL ENGINEERING RESEARCH LABORATORY	PROCEEDINGS, (1988) IRPS, Pages 90-95	88-5
880000	BOND PAD STRUCTURE RELIABILITY	CHING, T.B. SCHROEN, W.	TI	PROCEEDINGS, (1988) IRPS, Pages 64-70	88-21

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
880000	DESSICANT PACKAGING OF MOISTURE SENSITIVE ELECTRONIC DEVICES	WILLIAMS, J.M.	COMPAQ	PROCEEDINGS, SMART IV CONFERENCE, Pages 21-24	88-8
880000	EFFECT OF MOISTURE ON SUSCEPTIBILITY OF PLASTIC SMC TO PACKAGE CRACKING	CLIFTON, L. GORDON, S.	INTEL	PROCEEDINGS, (1988) WORKSHOP, IPC	88-2
880000	ELECTRONIC SCANNING OF 25 MHZ ULTRASOUND FOR IMAGING IC PACKAGES	KUBOTA,J. OKADA,H. MUSHA,Y.	HITACHI RESEARCH LAB.	IEEE/ULTRASONICS SYMPOSIUM, Pages 767-770	88-34
880000	FINITE ELEMENT ANALYSIS OF COMPLIANT COATING	SHORAKA, F. GEALER, C. BETTEZ, E.	INTEL	PROCEEDINGS, 38TH (1988) ECC, Pages 461-467	88-17
880000	HYBRID MICROCIRCUIT TECHNOLOGY HANDBOOK - MATERIALS, PROCESSES, DESIGN, TESTING AND PRODUCTION	LICARI,J.J. ENLOW,L.R.	ROCKWELL INTERNATIONAL CORP.		24415-000
	THE HYBRID MICROCIRCUIT TECHNOLOGY HANDBOOK INTEGRATES, FOR THE FIRST TIME, THE MANY DIVERSE TECHNOLOGIES USED IN THE DESIGN, FABRICATION, ASSEMBLY, AND TESTING OF HYBRID CIRCUITS. IT EMPHASIZES THOSETECHNOLOGY SEGMENTS CRUCIAL TO THE SUCCESS OF PRODUCING RELIABLE CIRCUITS IN HIGH YIELDS. AMONG THESE ARE: RESISTOR TRIMMING WIRE BONDING, DIE ATTACHMENT, CLEANING, HERMETIC SEALING, AND MOISTURE ANALYSIS. IN ADDITION TO THIN FILMS, THICK FILMS, AND ASSEMBLY PROCESSES, IMPORTANT CHAPTERS ON SUBSTRATE SELECTION, HANDLING, FAILURE ANALYSIS, AND DOCUMENTATION ARE INCLUDED.				
880000	LOW PROFILE PLASTIC QUAD FLAT PACKAGE (LPPQFP)	MCSHANE, M. CASTO, J. BIGLER, J., LIN, P.	MOTOROLA	PROCEEDINGS, 38TH (1988) ECC, Pages 411-419	88-15
880000	MECHANICAL STRESS AND LIFE FOR PLASTIC-ENCAPSULATED LARGE AREA CHIP	LUNDSTROM, P. GUSTAFSSON, K.	ERRICSSON TELECOM	PROCEEDINGS, 38TH (1988) ECC, Pages 396-405	88-14
880000	MOISTURE ABSORPTION AND MECHANICAL PERFORMANCE OF SURFACE-MOUNTABLE PLASTIC PACKAGES	BHATTACHARYYA, B.K. HUFFMAN, W.A., JAHSMAN, W.E. NATARAJAN, B.	INTEL	PROCEEDINGS, 38TH (1988) ECC, Pages 49-58	88-12
880000	MOISTURE EFFECTS ON SUSCEPTIBILITY TO PACKAGE CRACKING IN PLASTIC SURFACE MOUNT COMPONENTS	GORDON, S., HUFFMAN, W.A. PROUGH, S., SANDKUHLE, R. YEE, K.	INTEL	PROCEEDINGS, SMART IV CONFERENCE, Pages 1-25	88-7
880000	MOISTURE INDUCED PACKAGE CRACKING IN PLASTIC ENCAPSULATED SMC DURING SOLDER REFLOW PROCESS	LIN, R. SERISKY, P. BLACKSHEAR, E.	IBM	PROCEEDINGS, IRPS (1988), Pages 83-89	88-4
880000	OPTIMIZING BOND PARAMETERS TO MINIMIZE CRATING	MCKENNA,B.	TI	39TH (1988) ECC WORKSHOP, VLSI CHIP PACKAGING WORKSHIP	88-36
880000	PACKAGE CRACKING IN PLASTIC SURFACE MOUNT COMPONENTS AS A FUNCTION OF PACKAGE MOISTURE CONTENT AND GEOMETRY	POPE, D.E. CLIFTON, L.M.	INTEL	PROCEEDINGS, 5TH ANNUAL IEEE/EMT/CHMT SYMPOSIUM, Pages 89-92	88-1
880000	SELECTION CRITERIA FOR LIQUID ENCAPSULANTS IN NEW MICROELECTRONIC PACKAGES	COLLINS, W. BONNEAU, M.	HYSOL, DEXTER CORPORATION	PROCEEDINGS, 38th (1988) ECC, Pages 76-79	88-13
880000	SOCKETS: CONSIDERATIONS AS AN ALTERNATIVE TO DIRECT SURFACE MOUNTING OF COMPONENTS	PELLERITE, P. SUHL, D.	DIGITAL EQUIPMENT CORPORATION	PROCEEDINGS, 4TH (1988) ANNUAL IEEE/EMT/CHMT SYMP, Pages 89-91	88-25
880000	SPECIAL PROPERTIES OF MOLD COMPOUNDS FOR LARGE SURFACE MOUNTING DEVICES	ITO, S., OIZUMI, S. ADACHI, J., SHIMIZU, M. SUZUKI, H.	NITTO	PROCEEDINGS, 38TH (1988) ECC, Pages 486-492	88-18
880000	STRESS RELIEF IN PLASTIC-ENCAPSULATED INTEGRATED CIRCUIT DEVICES BY DIE COATING WITH PHOTODEFINABLE POLYIMIDE	KHAN, M.M. TARTER, T.S. FATEMI, H.	ADVANCED MICRO DEVICES, INC., (SUNNYVALE, CA)	PROCEEDINGS, 38TH (1988) ECC, Pages 425-431	88-16
880000	TEMPERATURE DISTRIBUTION IN IC PACKAGES IN THE REFLOW SOLDERING PROCESS	MIURA, H., NISHIMURA, A. KAWAI, S. NAKAYAMA, W.	HITACHI	PROCEEDINGS, I-THERM '88, IEEE/CHMT, Vol. IEEE CAT # 88CH2590-8, Pages 50-59	88-10

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
880000	THE ANALYSIS OF PACKAGE CRACKING PROBLEM UNDER VAPOUR PHASE REFLOW SOLDERING AND CORRECTIVE ACTION	ANJOH,I. NISHI,K. KITANO,M.	HITACHI	BRAZING AND SOLDERING, No. 14, Pages 48-51	88-33
880000	THERMAL CONDUCTIVITY OF BORON NITRIDE FILLED EPOXY RESINS: TEMPERATURE DEPENDENCE AND INFLUENCE OF SAMPLE PREPARATION	BUJARD, P.	CIBA-GIEGY	PROCEEDINGS, I-THERM '88, IEEE/CHMT, Vol. IEEE CAT #88CH2590-8, Pages 41-49	88-9
880000	THERMAL PHENOMENA DURING THE ENCAPSULATION OF ELECTRONIC DEVICES	EMERSON, J.A.	AT&T, (PRINCETON, NJ)	PROCEEDINGS, I-THERM '88, IEEE/CHMT, Vol. IEEE CAT # 88CH2590-8, Pages 190-192	88-11
880000	THERMOSONIC GOLD-WIRE BONDING TO PRECIOUS-METAL-FREE COPPER LEADFRAMES	LANG, B. PINAMANENI, S.	NATIONAL SEMICONDUCTOR, (SANTA CLARA, CA)	PROCEEDINGS, 38TH (1988) ECC, Pages 546-551	88-19
	DYE PENETRANT DISCLOSURE OF EXTERNAL CRACKS				
880000	VLSI PACKAGING THERMOMECHANICAL STRESSES TUTORIAL	EDWARDS, D.R. GROOTHUIS, S.K. MURTUZA, M.	TI	TUTORIAL NOTES, (1988) IRPS, Pages 8.1 THRU 8.39	88-6
880000	VOLUME PRODUCTION OF UNIQUE PLASTIC SURFACE-MOUNT MODULES FOR THE IBM 80-NS 1MBIT DRAM CHIP BY AREA WIRE BOND TECHNIQUE	WARD, W.C.	IBM, (ESSEX JUNCTION, VT)	PROCEEDINGS, 38TH (1988) ECC, Pages 552-557	88-20
	85/85/168 HOURS+ VPS + DYE PENETRANT DISCLOSURE OF EXTERNAL CRACKS				
871200	NONDESTRUCTIVE MOISTURE MEASUREMENT IN MICROELECTRONICS, FINAL TECHNICAL REPORT	KANE,D. DOMINGOS,H.	CLARKSON COLLEGE		21790-000
	THIS PROJECT WAS AIMED AT UNDERSTANDING MOISTURE INDUCED EFFECTS ON MATERIALS USED IN MICROELECTRONIC DEVICE MANUFACTURE. THE APPROACH CHOSEN HAS BEEN THE USE OF STATE-OF-THE-ART INTERDIGITATED SURFACE CONDUCTIVITY TEST STRUCTURES FOR CHARACTERIZING THE RESPONSES OF MICROELECTRONIC MATERIALS TO AMBIENT AND CONDENSED MOISTURE, BY PERFORMING NONDESTRUCTIVE MOISTURE MEASUREMENTS ON BOTH HERMETICALLYSEALED AND DELIDDED PACKAGES. A TEST CHAMBER AND AN APPROPRIATE ELECTRICAL TEST SETUP HAVE BEEN DEVELOPED FOR ASSESSING THE SPECIFICITY, REPRODUCIBILITY AND SENSITIVITY OF THESE EFFECTS.				
871200	SHEAR STRESS EVALUATION OF PLASTIC PACKAGES	EDWARDS,DARVIN R. HEINEN,K. GAIL MARTINEZ,J.E., GROOTHUIS, S.	TI	PROCEEDINGS, 37TH (1987) ECC, Pages 84-95	87-6
871126	LOAD-STRENGTH SIMULATION OF PLASTIC MOULDINGS	HOLL,V.	TERMA ELEKTRONIK AS, (DENMARK)	QUALITY AND RELIABILITY ENGINEERING, Vol. 4, No. 4, Pages 223-226	22743-003
	THE LOAD-STRENGTH THEORY IS USED TO SIMULATE THE RELATIONS BETWEEN THE RELIABILITY, THE SAFETY FACTORS USED IN THE MECHANICAL DESIGN AND THE DIFFERENT MATERIAL CONDITIONS CAUSED BY BATCH VARIATIONS INRAW MATERIAL, THE INJECTION MOULDING PROCESS AND THE MOULD DESIGN.				
871113	ACCELERATION FACTOR AT A PRESSURE COOKER TEST FOR THE SURFACE-MOUNT DEVICE	ITOBAYASHI, M. MIYAMOTO, K. KUROHUI, K.	MITSUBISHI ELECTRIC COMPANY	PROCEEDINGS, (1987) ISTFA, MICROELECTRONICS, Pages 283-289	87-26
871113	ACCELERATION FACTOR AT A PRESSURE COOKER TEST FOR THE SURFACE-MOUNT-DEVICE	ITOBAYASHI,M. MIYAMOTO,K. KUROHUI,M.	MITSUBISHI CORP.	PROCEEDINGS (1987) ISTFA, Pages 283-289	22862-037
	THE INFLUENCE OF THE HEAT STRESS ON THE LIFETIME OF SURFACE-MOUNT-DEVICES (SMDS) UNDER THE SATURATED PRESSURE COOKER TEST (PCT) HAS BEEN STUDIED. IT IS REVEALED THAT THE LIFETIME IN THE SATURATED PCTFOR THE SMDS, WHICH ARE SUBJECTED TO THE HEAT STRESS DURING SURFACE MOUNTING, BECOMES UNEXPECTEDLY SHORTER. THIS PHENOMENON CAN BE EXPLAINED BY THE GAP FORMATION BETWEEN LEAD FRAME AND PLASTIC RESIN IN THE DEVICES, AND THE HIGHER MOISTURE ABSORPTION RATE IN THE SATURATED PCT.				
871113	ACOUSTICAL MICROSCOPY AS A TOOL FOR NONDESTRUCTIVE TESTING OF FINISHED DEVICES	TATISTCHEFF, E.M. ELLIS, E. M.	DIGITAL EQUIPMENT CORPORATION	PROCEEDINGS, (1987) ISTFA, MICROELECTRONICS, Pages 21-24	87-23
871113	ACOUSTICAL MICROSCOPY AS A TOOL FOR NONDESTRUCTIVE TESTING OF FINISHED DEVICES	TATISTCHEFF,E.M. ELLIS,J.	DIGITAL EQUIPMENT CORP.	ISTFA 1987, Pages 21-24	22862-004
	TWENTY-SIX PLASTIC LEADED CHIP CARRIERS (PLCCS) WERE EXAMINED FOR PHYSICAL INTEGRITY USING SCANNING LASER ACOUSTIC MICROSCOPY (SLAM). TWENTY-ONE OF TWENTY-TWO DEVICES SUBJECTED TO VAPOR PHASE SOLDERING TEMPERATURE DEMONSTRATED LITTLE OR NO TRANSMISSION IN THE DIE AREA. CROSS SECTIONAL ANALYSIS REVEALED LATERAL DIE FRACTURE AS CAUSE OF THE POOR ACOUSTIC PROPERTIES. WHILE CHIP FRACTURE HAD BEEN SEENIN EARLIER CROSS SECTIONAL ANALYSIS, IT HAD BEEN ATTRIBUTED TO SECTIONING TECHNIQUE. SLAM SERVED TO BOTH IDENTIFY FRACTURED DEVICES AND TO VERIFY CROSS SECTIONAL TECHNIQUES.				
871113	ADVANCED FAILURE ANALYSIS TECHNIQUES FOR MULTILAYER CERAMIC CHIP CAPACITORS	BLOOMER, C. MEPHAM, R. SONNICKSEN, R. M.	MOTOROLA	PROCEEDINGS, (1987) ISTFA, MICROELECTRONICS, Pages 25-33	87-24

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
871113	DAMAGE ANALYSIS OF NOTCHED UNIDIRECTIONAL METAL MATRIX COMPOSITES	BAKUCKAS,J.G. LAU,C.W. AWERBUCH,J.	DREXEL UNIVERSITY	PROCEEDINGS, (1987) ISTFA, Pages 43-53	22861-005

THIS PAPER DESCRIBES RESULTS OF EXPERIMENTAL OBSERVATIONS OF FAILURE PROCESSES AND COMPUTATIONAL ANALYSIS OF MICROMECHANICS IN CENTER-NOTCHED UNIDIRECTIONAL METAL MATRIX COMPOSITES. IN PARTICULAR, THEEFFECT OF MATRIX PLASTIC PROPERTIES ON THE MECHANICS AND MECHANISMS LEADING TO ONSET OF MACROSCOPIC CRACK GROWTH IS INVESTIGATED. EXPERIMENTS WERE CONDUCTED ON CENTER-NOTCHED UNIDIRECTIONAL BORON/ALUMINUM COMPOSITE SPECIMENS UNDER QUASI-STATIC LOADING.

871113	ELECTROMIGRATION-ACCELERATE LIFE TEST OF AL-CONDUCTORS ENCAPSULATED IN PLASTIC AND CERAMIC	REVAY,L. EKLOF,E.	ERICSSON DEFENSE & SPACE SYSTEMS	PROCEEDINGS (1987) ISTFA, Pages 219-223	22862-030

WE HAVE STUDIED THE ELECTROMIGRATION PROPERTIES OF ALUMINUM ALLOY CONDUCTORS. THE CONDUCTOR MICROSTRUCTURE WAS DETERMINED BY TRANSMISSION ELECTRON MICROSCOPY (TEM). AN X-RAY DIFFRACTION SPECTRUM WAS OBTAINED FROM A MONITOR WAFER TO DETERMINE THE CRYSTALLOGRAPHIC AL-FILM TEXTURE. THE EM-TEST WAS PERFORMED TO DETERMINE THE MEDIAN FAILURE TIME BY VARYING THE CURRENT DENSITY AND AMBIENT TEMPERATURES.DURING THE TEST A CONSTANT CURRENT SUPPLY AND SCANNING DEVICE WAS USED TO SEQUENTIALLY READ THE VOLTAGE DROP ACROSS A LARGE STATISTICAL NUMBER OF ALUMINUM STRIPES.

871113	FAILURE ANALYSIS OF PRECISION BEARINGS	HOPPLE,G.	LOCKHEED AIRCRAFT CO.	PROCEEDINGS, (1987) ISTFA, Pages 201-208	22861-023

FAILURE ANALYSIS TECHNIQUES USED IN INVESTIGATING PRECISION AEROSPACE BEARING FAILURES ARE PRESENTED. SINCE BEARING ASSEMBLIES IN THESE CLOSE TOLERANCE SYSTEMS ARE HERMETICALLY SEALED, THE IMPORTANCEOF PROPER DISASSEMBLY METHODS AND THE USEFULNESS OF RESIDUAL GAS ANALYSIS IS EMPHASIZED. LUBRICANT EVALUATION METHODS FOR BOTH OILS AND GREASE COMPOUNDS ARE ALSO DETAILED. FOR THE LATTER MATERIALS, TECHNIQUES INVOLVING FREEZE-DRYING FOR SUBSEQUENT SEM EXAMINATION OF THICKENER STRUCTURE AND THE USE OF INFRARED ANALYSIS TO DETERMINE COMPOSITION AND THE PRESENCE OF CONTAMINATION IS REVIEWED.

871113	STRESS ANALYSIS FOR PASSIVATION AND INTERLEVEL-INSULATION FILM CRACKS IN MULTILAYEYR ALUMINUM STRUCTURES FOR PLASTIC-PACKAGED LSI	OKIKAWA,S. TOIDA,T. INATSU,M.	HITACHI CO.	PROCEEDINGS, (1987) ISTFA, Pages 75-81	22862-011

RECENTLY, MULTILAYER ALUMINUM METALLIZATION AND WIDER POWER LINES FOR SUPPLYING LARGER CURRENT HAVE BEEN INCREASINGLY USED TO REALIZE FASTER ICS INCORPORATING MORE AND MORE FUNCTIONS. HOWEVER, SUCH ALUMINUM WIRING TENDS TO CAUSE STRUCTURAL INSTABILITY IN DEVICES. SPECIFICALLY, IN PLASTIC-PACKAGED ICS, THERMAL STRESS ON THE PACKAGE MAY CAUSE THE PASSIVATION AND INTERLEVEL INSULATION FILM TO CRACK,RESULTING IN DEGRADED ELECTRICAL CHARACTERISTICS. TO ACHIEVE STABLE MULTILAYER ALUMINUM METALLIZATION, STRUCTURAL DESIGN CONSIDERATIONS ARE ESTABLISED.

871109	STRESS ANALYSIS FOR PASSIVATION AND INTERLEVEL-INSULATION FILM CRACKS IN MULTILAYER ALUMINUM STRUCTURES FOR PLASTIC-PACKAGED LSI	OKIKAWA, S. TOIDA, T. INATSU, M.	HITACHI	PROCEEDINGS, (1987) ISTFA MICROELECTRONICS, Pages 75-81	87-25
871100	ADVANCED SURFACE MOUNTABLE PACKAGES FOR VLSI DEVICES	BRADEN,J.S.	INDY ELECTRONICS, INC.	SEMICONDUCTOR INTERNATIONAL, Vol. 10, No. 12, Pages 82-85	21218-004

THE NEED FOR A LOW COST SURFACE MOUNTABLE PACKAGE HAS SPURRED INVESTIGATIONS INTO A NEW PACKAGE THAT WOULDD BE AN INDUSTRY STANDARD. UNTIL RECENTLY, VLSI DEVICES ABOVE 84 LEADS HAVE PREDOMINANTLY BEENASSEMBLED IN PIN GRID ARRAY (PGA) PACKAGES. THE HIGH COST OF THESE PACKAGES AND THE INDUSTRY TREND TO SURFACE MOUNT HAS NECESSITATED ALTERNATIVE PACKAGING TECHNOLOGIES. IN THE U.S. AND EUROPE, AVAILABLE SURFACE MOUNTABLE PACKAGES FOR VLSI DEVICES HAVE TYPICALLY INCLUDED PLASTIC LEADED CHIP CARRIERS (PLCCS), LEADED CERAMIC CHIP CARRIERS (LCCS), LEADLESS CERAMIC CHIP CARRIERS (LLCCS) AND CERQUADS.

871100	HERMETIC COATING OF OPTICAL FIBERS, FINAL TECHNICAL REPORT	RAYCHAUDHURI,S. LEVIN,P.S. SIERRA,R.	SPECTRAN CORP.		21085-000

HERMETICALLY COATED GRADED INDEX SILICA FIBERS WERE TO EXHIBIT PROOF TEST LEVELS GREATER THAN 200 KPSI OVER ONE KILOMETER LENGTH. FIBER WAS TO EXHIBIT A STRESS CORROSION FACTOR N GREATER THAN 100. THEDIELECTRIC COATING MATERIALS WERE TO INCLUDE, BUT NOT LIMITED TO DIAMOND - LIKE CARBON AND BORON NITRIDE. TECHNIQUES USING HOLLOW CATHODE DISCHARGE COATER PRODUCED COATED FIBER WITH N VALUE LESS THAN26. SEVERE ARCING PROBLEMS WERE FACED WITH THIS TECHNIQUE RESULTING IN LARGE CRACKS ON THE COATER ANODES.

871001	STATIC CONTROLLED THERMOFORMABLE SHEETS FROM ELECTRON BEAM CURING	KBOUGH,A.H.	METALLIZED PRODUCTS	PROCEEDINGS, (1987) EOS/ESD SYMPOSIUM, Pages 142-144	20884-023

THE PRINCIPLES OF ELECTRON BEAM RADIATION CURABLE STATIC CONTROLLED COATINGS HAVE NOW BEEN EXTENDED TO THERMOFORMABLE SHEET MATERIAL AS A LOGICAL NEXT STEP FOR RIGID PACKAGING. SUITABLE THERMOPLASTICSHEET MATERIAL SUCH AS POLYCARBONATE, POLYSTYRENE, AND GLYCOL MODIFIED POLYESTER (PET-G) HAVE BEEN COATED, RADIATION CURED, FORMED, AND AGED SHOWING PROMISING STABILITY AND FUNCTIONALITY FOR USE AS STATIC CONTROLLED RIGID PACKAGING.

871001	THERMOPLASTIC COMPOSITES FOR ESD PROTECTION	CROSBY,J.M. ADAMS,C.S.	LNP ENGINEERING PLASTICS	PROCEEDINGS (1987) EOS/ESD SYMPOSIUM, Pages 28-35	20884-005

ELECTROSTATIC DISCHARGE (ESD) HAS BEEN IDENTIFIED AS THE MAJOR SOURCE OF DAMAGE IN ELECTRONIC COMPONENTS. ALTHOUGH DESIGNS OFTEN PROVIDE PROTECTIVE CIRCUITRY, HANDLING AND SHIPPING GENERATE STATIC POTENTIALS THAT EXCEED THE LIMITS OF THE ESTABLISHED PROTECTION NETWORKS. THE INCREASING AMOUNT OF INTEGRATION IN CIRCUITS ALSO CONTRIBUTES TO THE PROBLEM, AS DISTANCES AN ELECTRIC POTENTIAL MUST TRAVELTO GROUND HAVE BEEN REDUCED.

871000	A MONOLITHIC 1 TO 90 MHZ CMOS CLOCK RECOVERY AND RETIMING CHIP	PRITCHETT,R.L. GUPTA,A. BAUMERT,R.J.	AT&T BELL LABORATORIES	1987 GOMAC DIGEST OF PAPERS, Pages 203-205	24776-045

THIS PAPER DESCRIBES A NOVEL SINGLE-CHIP DESIGN OF A CLOCK RECOVERY AND DATA RETIMING CIRCUIT. THE CHIP, WHEN USED ON THE RECEIVING END OF A SERIAL DATA LINK, RECOVERS A CLOCK FROM NRZ RANDOM DATA TRANSMITTED AT ANY BIT RATE BETWEEN 1 AND 50 MB/S AND SYNCHRONIZES THE CLOCK WITH THE DATA STREAM. THE CHIP HAS BEEN FABRICATED USING A 1.75 MICRON TWIN-TUB CMOS PROCESS, IS PACKAGED IN A 20 PIN PLASTICDIP, AND DISSIPATES 250 MW FROM A SINGLE 5.0V SUPPLY.

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
871000	HIGE PERMITTIVITY DIELECTRICS FOR ENERGY STORAGE	HILL,G.J. WORRELL,C.A.	ERA TECHNOLOGY LTD	CARTS - EUROPE 1987, Pages 70-73	25114-008

THIS PAPER WILL REVIEW THE PHYSICAL BACKGROUND TO THESE TWO LIMITATIONS AND SUGGEST MEANS BY WHICH THE ENERGY DENSITY ACHIEVABLE IN HIGH PERMITTIVITY MATERIALS MAY BE INCREASED TO A LEVEL IN EXCESS OFTHAT CURRENTLY ACHIEVED BY PLASTIC FILMS.

871000	TEN-WATT MONOLITHIC S-BAND TRANSCEIVER MODULES	JESSEN,D.N. BACHER,C.F. GRAY,E.S.	RAYTHEON COMPANY	1987 GOMAC DIGEST OF PAPERS, Pages 399-402	24776-090

LIGHTWEIGHT TEN-WATT S-BAND TRANSCEIVER MODULES HAVE BEEN BUILT COMBINING GAAS MMIC CHIPS WITH DISTRIBUTED MODULE CONTROL CIRCUITRY THE MICROWAVE CIRCUITS ARE CONTAINED IN A HERMETICALLY SEALED CERAMIC PACKAGE WHICH INCLUDES A PHASE SHIFTER, LOW-NOISE AMPLIFIER, DRIVE AMPLIFIER, AND TWO FINAL AMPLIFIER INTEGRATED CIRCUITS. A SEPARATELY PACKAGED CMOS GATE ARRAY PROVIDES BUILT-IN BEAM STEERING CAPABILITY.

871000	THE EVOLUTION OF METALLIZED FILM CAPACITORS TOWARDS SURFACE MOUNTING TECHNOLOGY	FABBRI,C. BERNARDI,A.	ARCOTRONICS ITALIA	CARTS - EUROPE 1987, Pages 31942	25114-001

AFTER THE FIRST EXPERIMENTAL PHASE, WE CAN SAY THAT SURFACE MOUNTING TECHNOLOGY (SMT) OF PLASTIC FILM CHIP CAPACITORS (MKT CHIP) HAS ALREADY BEEN INTRODUCED IN THE PRODUCTION ENVIRONMENT OF MANY COMPANIES

870911	NON-METAL HERMETIC ENCAPSULATION OF A HYBRID CIRCUIT	SCHNEIDER,G.	LGZ LANDIS AND GYR ZUG AG	MICROELECTRONICS AND RELIABILITY, Vol. 28, No. 1, Pages 75-92	20946-010

A CHEAP HERMETIC NON-METAL ENCAPSULATION WAS EVALUATED FOR USE WITH A HIGH RELIABILITY HYBRID CIRCUIT SUBJECT TO SEVERE CLIMATIC ENVIRONMENT FOR PRECISE MAGNETIC FIELD MEASUREMENTS OVER 20 YEARS LIFETIME. FOR THIS PURPOSE A LITERATURE SCAN HAS BEEN CARRIED OUT ESTABLISHING ROUGHLY THE FOLLOWING RESULTS: HUMIDITY IS THE LARGEST SINGLE RISK FACTOR CONCERNING RELIABILITY AND EXPECTED LIFE TIME OF THEDEVICE. PLASTIC SEALING DOES NOT PRESENT A BARRIER AGAINST HUMIDITY FOR A LONG TIME. THERE IS NO OFF-THE-SHELF SOLUTION AVAILABLE AS USUAL REAL HERMETIC ENCAPSULATIONS ARE RULED OUT.

870900	A NOVEL APPROACH - THERMOPLASTIC DIE ATTACH ADHESIVE	YING,L.	M&T CHEMICALS, INC.	SOLID STATE TECHNOLOGY, Vol. 30, No. 9, Pages 107-109	21136-002

A NOVEL APPROACH TO DIE BONDING USING A THERMOPLASTIC ADHESIVE IS DESCRIBED. THE THERMOPLASTIC ADHESIVE, WHICH REQUIRES NO CURE, OFFERS A NUMBER OF ADVANTAGES IN DIE ATTACH APPLICATIONS. THERE IS ALSOA DISCUSSION OF OTHER DIE BONDING MATERIALS SUCH AS GOLD-SILICON EUTECTIC, EPOXY AND POLYAMIC ACID PRODUCTS CURRENTLY AVAILABLE ON THE MARKET.

870900	A RAPID TECHNIQUE FOR ASSESSING THE MOISTURE INGRESS SUSCEPTIBILITY OF PLASTIC-ENCAPSULATED INTEGRATED CIRCUITS	CHWASTEK, E.J. SHAW, R.N.	BRITISH TELECOM RESEARCH LABORATORIES	QUALITY AND RELIABILITY ENGINEERING INTERNATIONAL, Vol. 3, No. 3, Pages 185-194	87-38
8706	USING THE PRECISION C-SAM FOR BILATERAL INSPECTION OF DIE ATTACH	ADAMS, T.E.	SONOSCAN, (BENSENVILLE, IL)	MICROELECTRONIC MANUFACTURING AND TESTING, Pages 32-34	87-37
870513	CHLORINE CONTENT IN AND LIFE OF PLASTIC ENCAPSULATED MICRO-CIRCUITS	GUSTAFSSON,K. LINDBORG,U.	ERICSSON DEFENSE & SPACE SYSTEMS	PROCEEDINGS, 37TH (1987) ECC, Pages 491-499	23188-017

A DIRECT CORRELATION BETWEEN CHLORINE CONTENT AND LIFE HAS BEEN FOUND DURING ACCELERATED HUMIDITY TESTS OF PLASTIC ENCAPSULATED MICRO-CIRCUITS. A METHOD HAS BEEN DEVELOPED WHICH PERMITS MEASUREMENTS OF THE CHLORINE CONTAMINATION WITHOUT REMOVING THE LEADFRAME AND THE CHIP IN AS-RECEIVED MICRO-CIRCUITS. FAILURE MECHANISMS CAUSED BY CHLORINE CONTAMINATION ARE MAINLY ALUMINUM CORROSION AND PURPLE PLAQUE AND, TO SOME EXTENT, GOLD MIGRATION FROM THE BOND WIRES. HOWEVER, DURING THE LAST FEW YEARS THE QUALITY OF PLASTIC ENCAPSULATED MICRO-CIRCUITS HAS BEEN CONSIDERABLY IMPROVED.

870513	HUMIDITY RESISTANCE IMPROVEMENT BY SPECIAL FORMULATION OF EPOXY MOLDING COMPOUNDS	SAMESHIMA,R. TANIMOTO,S. TANAKE,K.	SUMITOMO BAKELITE CO., LTD., (JAPAN)	PROCEEDINGS, 37TH (1987) ECC, Pages 181-186	23188-011

IN ORDER TO IMPROVE HUMIDITY RESISTANCE OF THE PLASTIC IC PACKAGES, STUDIES HAD BEEN MADE ON ANTI-CORROSIVES WHICH PREVENT CORROSION OF ALUMINUM, (AL CORROSION) BY THE MODEL TESTS AND THE DEVICE TESTS, TOGETHER WITH STUDIES OF THEIR ANTI-CORROSION MECHANISM. STUDIES WHICH COVERED THREE TYPES OF ANTICORROSIVES, I.E., (I) THOSE WHICH CATCH IMPURITY IONS, (II) THOSE WHICH NEUTRALIZE PH AND (III) THOSE WHICH COVER THE ALUMINUM SURFACE HAD PROVED THAT ANTICORROSIVES OF TYPE (I) ARE MOST EFFECTIVE FOR IMPROVEMENT OF HUMIDITY RESISTANCE.

870513	LIFE ESTIMATION FOR IC PLASTIC PACKAGES UNDER TEMPERATURE CYCLING BASED ON FRACTURE MECHANICS	NISHIMURA,A. TATEMICHI,A. MIURA,H.	HITACHI CO.	PROCEEDINGS, 37TH (1987) ECC, Pages 477-483	23188-015

THE STRENGTH OF PLASTIC ENCAPSULANTS IS ANALYZED FROM THE VIEWPOINT OF CRACK PROPAGATION. FATIGUE CRACK PROPAGATION RATES DA/DN OF ENCAPSULANTS CAN BE EXPRESSED AS FUNCTIONS OF THE STRESS INTENSITY FACTOR RANGE. THE CRACK PROPAGATION BEHAVIOR IN THE PACKAGE WAS ESTIMATED FROM THE DATA OF DA/DN AT THE LOWEST TEMPERATURE OF THE TEST CYCLES. REASONABLE CORRELATION IS FOUND BETWEEN THE ESTIMATED CRACKPROPAGATION BEHAVIOR AND THE OBSERVED ONE, AND THE APPLICABILITY OF FRACTURE MECHANICS TO THE PACKAGE CRACKING PROBLEM IS DEMONSTRATED.

870513	SHEAR STRESS EVALUATION OF PLASTIC PACKAGES	EDWARDS,D.R. HEINEN,K.G. MARTINEZ,J.E.	TEXAS INSTRUMENTS	PROCEEDINGS, 37TH (1987) ECC, Pages 84-95	23188-005

A STUDY HAS BEEN PERFORMED TO DETERMINE THE IMPACT OF PACKAGE ASSEMBLY ON SHEAR STRESS PHENOMENON IN PLASTIC ENCAPSULATED INTEGRATED CIRCUITS (IC'S). TEST STRUCTURES WERE USED WHICH ALLOWED QUANTITATIVE MEASUREMENTS OF COMPRESSIVE STRESSES ALONG WITH QUALITATIVE OBSERVATION OF SHEAR STRESS EFFECTS. RESULTS FROM EXPERIMENTS WITH VARIOUS MOLD COMPOUNDS, LEAD FRAME MATERIALS, AND MOUNT COMPOUNDS WILLBE PRESENTED. THE EXPERIMENTS LED TO THE DEVELOPMENT OF A SIMPLIFIED STRESS MODEL WHICH CAN BE APPLIED TO EVALUATING PACKAGE AND CHIP DESIGNS OF FUTURE PRODUCTS.

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
870513	STRESS-RELATED CORROSION FAILURE OF PLASTIC ENCAPSULATED IC'S DURING PTH RELIABILITY TESTS	BOLGER,J.C.	AMICON/GRACE ELECTRONIC MATERIALS	PROCEEDINGS, 37TH (1987) ECC, Pages 468-476	23188-014

THIS PAPER PROPOSES A NEW STRESS CORROSION MECHANISM TO EXPLAIN WHY SOME DIE ATTACH ADHESIVES PERFORM BETTER THAN OTHERS IN PTH (PRESSURE-TEMPERATURE-HUMIDITY) TESTS. EXTRACTABLE ION CONTENT IS GIVENFOR TEN WIDELY USED EPOXY AND POLYIMIDE DIE ATTACH ADHESIVES. AND FOR FOUR U.S. AND JAPANESE EPOXY MOLDING COMPOUNDS, AFTER EXTRACTION AT 100 DEGREES C, AND ALSO AFTER EXTRACTION OF 121 DEGREES C/15PSIG. PTH DIFFERENCES CANNOT BE EXPLAINED BY DIFFERENCES IN QUANTITY OR IDENTITY OF IONS EXTRACTED FROM THE DIFFERENT DIE ATTACH ADHESIVES.

870503	A MECHANICAL DECAPSULATION TECHNIQUE FOR EPOXIDE-PACKAGED SEMICONDUCTOR COMPONENTS	CHWASTEK,E.J. HOLLAND,I.A.	BRITISH TELECOM RESEARCH INC.	QUALITY AND RELIABILITY ENGINEERING, Vol. 4, No. 1, Pages 31967	22742-003

A NOVEL MECHANICAL TECHNIQUE FOR DECAPSULATING PLASTIC SEMICONDUCTOR COMPONENTS HAS BEEN DEVELOPED. THE TECHNIQUE IS EXTREMELY EASY TO USE, HAS A HIGH SUCCESS RATE, AND IS SUPERIOR IN ALL RESPECTS TOPREVIOUSLY-DESCRIBED MECHANICAL TECHNIQUES WHICH GIVE INCONSISTENT RESULTS. A SIGNIFICANT ADVANTAGE OVER ALTERNATIVE CHEMICAL TECHNIQUES IS THAT CORROSION PRODUCTS ON THE DIE SURFACE ARE RETAINED. THIS PAPER DESCRIBES THE NEW TECHNIQUE AND SHOWS EXAMPLES OF NEW AND CORRODED COMPONENTS THAT HAVE BEEN SUCCESSFULLY DECAPSULATED.

870500	STAINLESS STEEL FIBER SOLVES ESD PROBLEMS	GERTEISEN,S.	WILSON FIBERFIL INTERNATIONAL	EVALUATION ENGINEERING, Vol. 26, No. 4, Pages 124-132	21129-002

THE ELECTRICAL/ELECTRONICS INDUSTRY CONTINUES TO BE A LARGE MARKET FOR MOLDED PLASTIC PARTS. DESIGNERS SPECIFY PLASTICS OVER METAL BECAUSE OF SEVERAL ENGINEERING ADVANTAGES: GREATER FLEXIBILITY, LIGHTER WEIGHT, MOKRE PLEASING AESTHETICS, BETTER CORROSION RESISTANCE, AND LOWER FABRICATION COSTS. VERY OFTEN, ELECTRONICS APPLICATIONS MAKE USE OF THE EXCELLENT INHERENT ELECTRICAL INSULATION PROPERTIESOF PLASTICS. HOWEVER, SOMETIMES PROBLEMS CAN ARISE BECAUSE OF THE NONCONDUCTIVITY OF THE PLASTIC. ONE MAJOR PROBLEM AREA IS ELECTROSTATIC DISCHARGE (ESD).

870422	METHODS FOR THE ANALYSIS OF RELAY CONTAMINATION	REAGOR,B.T.	BELL COMMUNICATIONS RESEARCH, INC.	PROCEEDINGS, 35TH (1987) RELAY CONFERENCE, Pages 5-1 THRU 5-6	25121-005

FAILURES IN ELECTROMECHANICAL RELAYS ASSOCIATED WITH CHEMICAL CONTAMINATION CAN BE TRACED TO A VARIETY OF CAUSES. THE CONTAMINANTS CAN BE DERIVED FROM THE MANUFACTURING PROCESS, WEAR AND DETERIORATIONOF RELAY PARTS, FORES, FLOODS, OUTGASSING FROM PLASTIC PARTS, AS WELL AS CHEMICALS AND PARTICULATE SOURCES WITHIN THE OPERATING ENVIRONMENT. IN ATTEMPTING TO DETERMINE THE CAUSE OF THE FAILURE, WE MUST FIRST DETERMINE THE NATURE OF THE PROBLEM.

870406	A RAPID TECHNIQUE FOR ASSESSING THE MOISTURE INGRESS SUSCEPTIBILITY OF PLASTIC ENCAPSULATED INTEGRATED CIRCUITS	CHWASTEK,E.J. SHAW,R.N.	BRITISH TELECOM RESEARCH INC.	QUALITY AND RELIABILITY ENGINEERING, Vol. 3, No. 3, Pages 185-193	19722-006

THE EQUIPMENT AND ASSOCIATED METHODOLOGY OF A NEW TECHNIQUE FOR CHECKING THE SUSCEPTIBILITY OF PLASTIC ENCAPSULATED ICS TO MOISTURE INGRESS IS PRESENTED.

870403	CAPACITORS, FIXED, ELECTROLYTIC (SOLID ELECTROLYTE), TANTALUM, ESTABLISHED RELIABILITY, GENERAL SPECIFICATION FOR	ANON.	UNKNOWN		20760-000

THIS SPECIFICATION COVERS THE GENERAL REQUIREMENTS FOR ESTABLISHED RELIABILITY, INSULATED, TANTALUM, ELECTROLYTIC (SOLID ELECTROLYTE), FIXED CAPACITORS, HERMETICALLY SEALED 1/ IN METAL CASES. RATED VOLTAGES RANGE FROM 6 TO 100 VOLTS DC WITH SURGE VOLTAGES OF 8 TO 130 VOLTS DC, RESPECTIVELY. THESE CAPACITORS HAVE RELIABILITY RATINGS ESTABLISHED ON THE BASIS OF LIFE TESTS PERFORMED AT SPECIFIED VOLTAGE AT +85 DEGREES C FOR FAILURE RATE (FR) LEVELS.

870400	IC SURFACE MOUNTING GAINS WITH STANDARD PACKAGES	POUND,R.	NONE	ELECTRONIC PACKAGING AND PRODUCTION, Vol. 27, No. 4, Pages 46-49	21788-000

PROBLEMS OF COMPONENT AVAILABILITY AND PACKAGE STANDARDIZATION HAVE BEEN ON THE LIPS OF MANY SEEKING TO EXPLAIN THE "SLOW" ADOPTION OF SURFACE-MOUNT TECHNOLOGY IN THE UNITED STATES. BUT LISTEN NOW TOWHAT COMPONENT SUPPLIERS, AND EVEN SOME USERS, ARE SAYING ABOUT GETTING INTEGRATED CIRCUITS IN SURFACE-MOUNT, PLASTIC PACKAGES: A LARGE VARIETY OF IC DIE FABRICATION TECHNOLOGIES AND ELECTRONIC FUNCTIONS ARE AVAILABLE, AND IN STANDARD PLASTIC PACKAGES.

870324	SCANNING LASER ACOUSTIC MICROSCOPY (SLAM)	BLOOMER, C. MEPHAM, R. SONNICKSEN, R.M.	MOTOROLA	PROCEEDINGS, (1987) RELIABILITY: KEY TO INDUSTRIAL SUCCESS, Pages 157-164	87-35
870312	A NEW FILM CAPACITOR-POLYPHENYLENE SULFIDE	MANNHEIM,D.	SPRAGUE ELECTRIC COMPANY	CARTS 1987, Pages 41-49	25112-008

IN THIS PRESENTATION WE WILL INFORM YOU OF THE INHERENT, DESIRABLE PROPERTIES AND POTENTIAL ADVANTAGES OF THE NEW HIGH TEMPERATURE, LOW LOSS DIELECTRIC FILM AVAILABLE FOR CAPACITORS, POLYPHENYLENE SULFIDE (PPS). WITH THE USE OF SAMPLE TEST DATA, WE WILL HIGHLIGHT: POSSIBLE 150 DEGREES C OPERATING TEMPERATURE FOR DC APPLICATIONS; LOW LOSS AT HIGH FREQUENCY FOR AC APPLICATIONS; SIZE EFFICIENCY, PARTICULARLY VS. POLYSTYRENE AND POLYPROPYLENE; LOW MOISTURE ABSORPTION FOR NON-HERMETIC CAPACITORS; LOW CAPACITANCE CHANGE VS. TEMPERATURE FOR STABLE CAPACITANCE.

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
870310	A SOURCE OF CHLORIDE DEGRADATION OF ALUMINUM-METALLIZED, PLASTIC-ENCAPSULATED SEMICONDUCTOR DEVICES (AD-B109-944)	GABOR,K. ZSOLT,N.	NONE		22403-000

BY MEANS OF A PRESSURE COOKER TEST, A CLOSER INSIGHT IS GAINED INTO THE CHEMICAL DEFECT MECHANISMS OF PLASTIC-ENCAPSULATED SEMICONDUCTOR DEVICVES. AFTER SUMMARIZING THE HERETOFORE PUBLISHED SOURCES OFCHLORINE CONTAMINATION AND THE CAUSES OF DEGRADATION, WE PUBLISH OUR MORE RECENT RESEARCH FINDINGS, ACCORDING TO WHICH CHLORINE CONTAMINATION OF THE DEVICES ORIGINATES IN CERTAIN WASHING AND CLEANSING OPERATIONS.

870200	EVALUATION OF AEROSOL PARTICLE PENETRATION THROUGH PFA TUBING AND ANTISTATIC PFATUBING	BERGIN,M.H.	FLUOROWAVE, INC.	MICROCONTAMINATION, Vol. 5, No. 2, Pages 22-28	21228-002

THIS COLUMN FOCUSES ON A STUDY OF PFA AND ANTISTATIC PFA TUBING (SUPPLIED BY GALITEK CORPORATION, CHASKA, MN). THE ANTISTATIC PFA MATERIAL USED HAS A SURFACE RESISTIVITY OF 10TO THE ELEVENTH POWER -10 TO THE TWELVETH POWER MICROWAVES/SQ. FOR COMPARISON, PLASTICIZED PVC AND COPPER TUBING WERE ALSO TESTED. COPPER TUBING WAS TESTED BECAUSE OF ITS CONDUCTIVITY AND ITS MINIMAL PARTICLE LOSS DUE TO ELECTROSTATIC EFFECTS. TESTING WAS PERFORMED AT THE UNIVERSITY OF MINNISOTA'S PARTICLE TECHNOLOGY LABORATORY.

870200	RELIABLE PACKAGING ALTERNATIVES TO HERMETIC SEALING	KOOKOOTSEDES,G.	DOW CORNING CORP.		21475-000

BY COMBINING ECONOMICAL PACKAGES WITH SEMICONDUCTOR PROTECTIVE MATERIALS, RELIABILITY CAN BE ACHIEVED WITHOUT HERMETIC SEALING. THE GROWING USE OF MICROELECTRONICS IN EVERY PHASE OF LIFE TODAY, FROM BUSINESS MACHINES TO CONSUMER GOODS TO MILITARY EQUIPMENT, INCREASES THE PRESSURE ON MANUFACTURERS TO SUPPLY RELIABLE DEVICES. THIS RELIABILITY IS ALL THE MORE IMPORTANT AS DEVICES BECOME MORE COMPLEXAND EXPENSIVE. AT THE SAME TIME, DEVICES ARE EXPOSED MORE FREQUENTLY TO HARSH OPERATING ENVIRONMENTS.

870123	PACKAGE CRACK	UNO		NEC INTERNAL REPORT	87-09
870110	PURPLE PLAGUE: ELIMINATED OR JUST FORGOTTEN?	FOOTNER,P.K. RICHARDS,B.P. YATES,R.B.	GEC POWER ENGINEERING LTD (HIRST RESEARCH)	QUALITY AND RELIABILITY ENGINEERING, Vol. 3, No. 3, Pages 177-184	19722-005

THE REAPPEARANCE OF 'PURPLE PLAGUE' AS A RELIABILITY AND FAILURE RISK IN CURRENT IC DEVICES HAS LED TO RENEWED INTEREST IN THE PRECISE FAILURE MECHANISMS AND EVENTUAL FAILURE MODE. THESE ARE OUTLINEDAND ILLUSTRATED WITH EXAMPLES OF RECENT FAILURES IN PLASTIC ENCAPSULATED INTEGRATED CIRCUITS, HERMETICALLY SEALED INTEGRATED CIRCUITS AND HYBRIDS. THE REASONS FOR THE REAPPEARANCE OF THIS TYPE OF FAILURE ARE DISCUSSED, AND IT IS SHOWN THAT THE PROBLEM MAY BE EXPECTED TO INCREASE IN FUTURE GENERATION DEVICES.

870100	A REVIEW OF CORROSION FAILURE MECHANISMS DURING ACCELERATED TESTS: ELECTROLYTIC METAL MIGRATION	STEPPAN,J.J., JEANNOTTE, D.A. ROTH,J.A., CARBONE, S.P. HALL,L.C.	VANDERBILT UNIVERSITY, IBM	JOURNAL, ELECTROCHEMICAL SOCIETY, Vol. 134, No. 1, Pages 175-190	87-10
870100	CERAMIC QUAD PACKAGE MEETS HIGH-DENSITY SMT NEEDS	EASTMAN,K.	DIGITAL EQUIPMENT CORP.	ELECTRONIC PACKAGING AND PRODUCTION, Pages 70-81	21548-000

THE CERQUAD SEMICONDUCTOR PACKAGE FAMILY WAS DEVELOPED BY DIGITAL EQUIPMENT CORP.'S SEMICONDUCTOR OPERATIONS TO MEET THE COMPANY'S SURFACE-MOUNTING NEEDS. THIS PACKAGE IS SIMILAR IN CONSTRUCTION TO CERDIPS AND CERAMIC FLATPACKS, WHICH HAVE BEEN IN USE FOR OVER 20 YEARS. THE CERQUAD PACKAGE UTILIZES PROVEN PACKAGING TECHNOLOGIES WHICH HAVE BEEN ENHANCED AND REFORMATTED TO MEET CURRENT REQUIREMENTS.REQUIREMENTS PLACED ON CERQUAD INCLUDE: SURFACE-MOUNT, COST-EFFECTIVE, HERMETIC, POWER DISSIPATION GREATER THAN 1W, DEVICE SIZE UP TO 0.400 IN., AND LEAD COUNTS UP TO 164.

870100	MANUFACTURING METHODS AND TECHNOLOGY FOR SUPERPLASTIC FORMING OF ALUMINUM AIRFRAME COMPONENTS, FINAL REPORT FOR PERIOD 1982 - 1985	MCQUILKIN,F.T. STACHER,G.W.	ROCKWELL INTERNATIONAL CORP. (NA-86-1416)		19866-000

THE FABRICATION METHOD OF SUPERPLASTIC FORMING (SPF) HAS BEEN APPLIED TO THE SPECIALLY PROCESSED 7475 ALUMINUM ALLOY TO MAKE A COPILOT'S FLOOR/KEEL BEAM SECTION FOR THE AH-64 HELICOPTER. THIS REPORT COVERS THE DESIGN AND ANALYSIS OF THE FLOOR/KEEL BEAM SECTION, THE FABRICATION OF CHARACTERIZED 7475 ALUMINUM SHEET TO PRODUCE THE FLOOR/KEEL BEAM SECTIONS, AND FATIGUE DAMAGE TOLERANCE AND FULL SCALESTATIC TESTING OF THOSE PARTS.

870000	A RAPID TECHNIQUE FOR ASSESSING MOISTURE INGRESS SUSCEPTIBILITY OF PLASTIC ENCAPSULATED INTEGRATED CIRCUITS	CHWASTEK,E.J. SHAW,R.N.	BRITISH TELECOM	QUALITY AND RELIABILITY ENGINEERING INTERNATIONAL (GB), Vol. VOL. 3, Pages 185-193	87-08
870000	ANALYSIS OF REFLOW SOLDERING BY FINITE ELEMENT METHOD	OIZUMI, S. ITO, S. SUZUKI, H.	NITTO ELECTRIC INDUSTRIAL CO., LTD.	NITTO TR; SPECIAL #SEMICONDUCTOR ENCAPSULANT 1987, Pages 40-50	87-13
870000	CHLORINE CONTENT IN AND LIFE OF PLASTIC ENCAPSULATED MICRO-CIRCUITS	GUSTAFSSON, K. LINDBORG, U.	ERICSSON	PROCEEDINGS, 37TH (1987) ECC, Pages 491-499	87-20
870000	COMPARISON OF ULTRASONIC MICROSCOPE LASER THERMOGRAM, AND X-RAY FOR NDT (NON-DESTRUCTIVE TEST) INSPECTION OF SMA'S	PASCENTE, J.	LDI	PROCEEDINGS, EXPO SMT '87	87-30

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
870000	CONTROL OF PACKAGE CRACKING IN PLASTIC SMD DURING SOLDER REFLOW PROCESS	LIN, R. BLACKSHEAR, E. MAY, G.	IBM	PROCEEDINGS, (1987) IEPS, Pages 995-1010	87-01
870000	DEVELOPMENT OF EPOXY ENCAPSULANTS FOR SURFACE MOUNTED DEVICES	ITO, S. KITAYAMA, A. TABATA, H.	NITTO ELECTRIC INDUSTRIAL CO., INC.	NITTO TR; SPECIAL # SEMICONDUCTOR ENCAPSULANT 1987, Pages 78-82	87-16
870000	DEVELOPMENT OF ULTRA-LOW-STRESS RESIN ENCAPSULANTS FOR LARGE-CHIP SEMICONDUCTOR DEVICES	NAKAMURA,Y. UENISHI,S. KUNISHI,T.	NITTO ELECTRIC INDUSTRIAL CO., LTD.	NITTO TR; SPECIAL # SEMICONDUCTOR ENCAPSULANT 1987, Pages 23-31	87-11
870000	DIE ATTACH RELIABILITY PREDICTION	HEINEN, K.G.	TI	PROCEEDINGS, 1ST (1987) INT. ELECTR. CONF., SAMPE, Pages 264-274	87-32
870000	EVALUATION OF PLASTIC LEADED CHIP CARRIERS (PLCC) USING SCANNING LASER ACOUSTIC MICROSCOPY (SLAM)	TATISTCHEFF, E. M.	DEC	ACOUSTICAL IMAGING, Vol. 16	87-27
870000	HIGH THERMAL CONDUCTIVITY ENCAPSULANT	UHARA, Y. MIKI, K.	NITTO ELECTRIC INDUSTRIAL CO., LTD.	NITTO TR; SPECIAL # SEMICONDUCTOR ENCAPSULANT 1987, Pages 32-39	87-12
870000	HUMIDITY RESISTANCE IMPROVEMENT BY SPECIAL FORMULATION OF EPOXY MOLDING COMPOUNDS	SAMESHIMA, R. TANIMOTO, S. TANAKE, S.	SUMITOMO	PROCEEDINGS, 37TH (1987) ECC, Pages 181-186	87-18
870000	IMAGE ANALYSIS AS AN AID TO QUANTITATIVE INTERPRETATION OF ACOUSTIC IMAGES OF DIE ATTACH	SEMMENS, J. E. KESSLER, L. W.	SONOSCAN, (BENSENVILLE, IL)	ACOUSTICAL IMAGING, Vol. 16, Pages 129-136	87-28
870000	IMMERSION COOLING FOR HIGH DENSITY PACKAGING	YOKOUCHI, K. KAMEHARA, N. NIWA, K.	FUJITSU	PROCEEDINGS, 37TH (1987) ECC, Pages 545-549	87-21
870000	INTERACTION BETWEEN VOID PARAMETERS AND THE OUTPUTS OF THE SCANNING LASER ACOUSTIC MICROSCOPE	AL-SIKBAKHI, G.Z. HUSSAIN, M.G.M. SADEK,M.M.	KUWAIT UNIVERSITY, (KUWAIT)	PROCEEDINGS, ACOUSTICAL IMAGING, Vol. 16, Pages 147-164	87-39
870000	INTERNAL DEFECTS OBSERVATION OF IC PACKAGE BY SCANNING ACOUSTIC TOMOGRAPHY	TABATA, T. SUZUKI, H. HAMADA, T.	NITTO ELECTRIC INDUSTRIAL CO., LTD.	NITTO TR; SPECIAL # SEMICONDUCTOR ENCAPSULANT 1987, Pages 70-77	87-15
870000	INVESTIGATIONS OF LARGE PLCC PACKAGE CRACKING DURING SURFACE MOUNT EXPOSURE	STEINER,T.O. SUHL,D.	DEC	TRANSACTIONS, IEEE/CHMT, Vol. CHMT-10, No. 2, Pages 209-216	87-05
870000	LIFE ESTIMATION FOR IC PLASTIC PACKAGES UNDER TEMPERATURE CYCLING BASED ON FRACTURE MECHANICS	NISHIMURA,A. TATEMICHI,A. MIURA,H.	HITACHI	PROCEEDINGS, 37TH (1987) ECC, Pages 477-483	87-07
870000	LIQUID DROPPING RESIN FOR IC ENCAPSULANT	YAMAOKA, S. KUSUHARA, A. OKABE, A.	SUMITOMO	PROCEEDINGS, 37TH (1987) ECC, Pages 175-180	87-17
870000	MEASUREMENT OF DIE STRESS FROM PACKAGING AND EFFECTS OF THERMAL CYCLING	ROBINSON, M.J. TSAY, C. BUYNOSKI, M.	NATIONAL	ELECTRONIC PACKAGING MATERIALS SCIENCE III, Vol. VOL. 108, Pages 43-46	87-33
870000	MOISTURE SORPTION AND ITS EFFECT UPON THE MICROSTRUCTURE OF EPOXY MOLDING COMPOUNDS	BELTON,D.J. SULLIVAN,E.A. MOLTER,M.	SIGNETICS	PROCEEDINGS, IEEE/IEMT/CHMT SYMPOSIUM, Pages 158-169	87-03
870000	NEW PROFILE OF ULTRA-LOW-STRESS RESIN ENCAPSULANTS FOR LARGE CHIP SEMICONDUCTOR DEVICES	NAKAMURA, Y. UENISHI, S. KUNISHI, T.	NITTO	PROCEEDINGS, 37TH (1987) ECC, Pages 187-191	87-19
870000	NEW RELIABILITY ASPECTS OF SURFACE MOUNT DEVICES	MCSHANE,M.	MOTOROLA	PROCEEDINGS, IEEE/IEMT/CHMT SYMPOSIUM, Pages 87-88	87-02

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
870000	NONDESTRUCTIVE INSPECTION OF AG/GLASS DIE ATTACH BONDS	KESSLER, L. W. SEMMENS, J. E. WALTER, K.	SONOSCAN,QUANTUM MATERIALS, (BENSENVILLE, IL)	PROCEEDINGS, 37TH (1987) ECC, Pages 110-117	87-22
870000	NONDESTRUCTIVE SLAM EVALUATION OF CERAMIC CAPACITORS - AN OVERVIEW OF EXPERIENCES FROM 1980-1987	KESSLER, L.W. SEMMENS, J.E. RAMIREZ, P.	SONOSCAN, (BENSENVILLE, IL)	PROCEEDINGS, 1ST (1987) EUROPEAN CAPACITOR AND RESISTOR TECHNOLOGY SYMPOSIUM AND SEMINARS, Pages 91-104	87-36
870000	STRESS ANALYSIS OF SI-CHIP AND PLASTIC ENCAPSULANT INTERFACE	OIZUMI, S. IMAMURA, N. TABATA, H.	NITTO ELECTRIC INDUSTRIAL CO., LTD.	NITTO TR; SPECIAL # SEMICONDUCTOR ENCAPSULANT 1987, Pages 51-57	87-14
870000	STRESS RELATED FAILURES CAUSING OPEN METALLIZATION	GROOTHUIS, S.K. SCHROEN, W.H.	TI	PROCEEDINGS, 25TH (1987) ANNUAL IRPS, Pages 1-8	87-34
870000	THE ACCELERATED LIFE TESTING OF COPPER THICK FILM MULTILAYER MATERIAL	NEEDES,C.R.S.	E.I. DUPONT DE NEMOURS CO.	JOURNAL FOR HYBRID MICROELECTRONICS, Vol. 10, No. 2, Pages 27-35	20953-004

RELIABILITY DATA, OBTAINED FROM THE ACCELERATED LIFE TESTING OF COPPER MULTILAYER CIRCUITS, HAS BEEN ANALYZED STATISTICALLY BY THE USE OF THE WEIBULL DISTRIBUTION FUNCTION. THE ABOVE ANALYSIS WAS USEDTO REFINE A CORRELATION BETWEEN THE END-OF-LIFE RELIABILITY OF A MULTILAYER CIRCUIT AND THE HERMETICITY OF ITS DIELECTRIC MATERIAL. AN ADDITIONAL FEATURE OF THE REVISED CORRELATION IS THAT THE END-OF##

870000	THERMAL STRESS DEVELOPMENT IN THICK EPOXY COATINGS	KING, D. BELL, J.P.	UNIVERSITY OF CONNECTICUT	PROCEEDINGS, ACS POLYMERIC MATER.: SCIENCE & ENGINEERING, Vol. 56, Pages 441-445	87-29
870000	THERMAL STRESS IN SEMICONDUCTOR ENCAPSULATING MATERIALS	VAN DEN BOGERT,W., BELTON, D. MOLTER,M. SOANE, D., BIERNATH, R.	SIGNETICS, UNIVERSITY OF CALIFORNIA, (BERKELEY, CA)	PROCEEDINGS, IEEE/IEMT/CHMT SYMPOSIUM, Pages 170-177	87-04
870000	THIN FILM CRACKING AND WIRE BALL SHEAR IN PLASTIC DIPS DUE TO TEMPERATURE CYCLING AND THERMAL SHOCK	SHIRLEY, C. G. BLISH, R. C. II.	INTEL	PROCEEDINGS, 25TH (1987) IRPS, Pages 238-249	87-31
861100	RELIABILITY OF POWER GAAS FETS, FINAL TECHNICAL REPORT (AD-B112-779)	RAGLE,R.D. SHAW,D.S. OPP,F.	TEXAS INSTRUMENTS (U1-341610-F)		19186-000

THE OBJECTIVE OF THIS PROGRAM WAS TO ASSESS AND ESTABLISH THE RELIABILITY AND LIFE CHARACTERISTICS OF COMMERCIALLY AVAILABLE MEDIUM POWER GAAS MESFETS AND TO IDENTIFY ANY ASSOCIATED FAILURE MECHANISMS. THE DEVICES CHOSEN FOR THIS STUDY INCLUDED A TEXAS INSTRUMENTS 1200UM-CHIP DEVICE WHICH WAS HERMETICALLY SEALED IN A MICROWAVE PACKAGE, AND HERMETICALLY PACKAGED DEVICES FROM THREE OTHER DOMESTIC AND THREE JAPANESE VENDORS. TESTS PERFORMED INCLUDED CHARACTERIZATION AND STRESS TESTS OF ENVIRONMENTAL AND ELECTRICAL (CW AND PULSED) CONDITIONS.

861024	A NOVEL METHOD OF EVALUATION MOISTURE RESISTANCE OF SOLDERING PLASTIC ENCAPSULATED LSI BY A NEW ULTRASONIC INSPECTION SYSTEM	TANAKA,M. SAKIMOTO,M. OKIKAWA,S.	HITACHI CO.	PROCEEDINGS, (1986) ISTFA, Pages 173-177	22860-027

THE ULTRASONIC INSPECTION SYSTEM HAS DETECTED INTERNAL DEFECTS IN PLASTIC ENCAPSULATED LSI BY MEASURING REFLECTED ULTRASONIC WAVES. BUT WE HAVE HARDLY FOUND OUT A CRACK IN THE INTERNAL PARTS OF THE RESIN AND A SEPARATION BETWEEN CHIP AND RESIN BECAUSE OF POOR PERFORMANCE OF THE SYSTEM. RECENTLY A NEW ADVANCED ULTRASONIC INSPECTION SYSTEM (SCANNING ACOUSTIC IMAGING SYSTEM AT5000) HAS BEEN DEVELOPEDBY JOINT DEVELOPMENT OF HITACHI LTD. AND HITACHI CONSTRUCTION MACHINERY CO. LTD..

861024	A PROCEDURE FOR THE NONDESTRUCTIVE REMOVAL OF GLASSIVATION FROM INTEGRATED CIRCUITS	ABBOTT,J.	MARTIN MARIETTA CORP.	PROCEEDINGS, (1986) ISTFA, Pages 113-120	22860-018

A PROCEDURE HAS BEEN DEVELOPED WHICH REMOVES THE GLASSIVATION LAYER FROM THE DIE OF AN INTEGRATED CIRCUIT IN A HERMETIC PACKAGE USING A BARREL-GEOMETRY PLASMA REACTOR. THE CIRCUIT'S ELECTRICAL BEHAVIOR HAS BEEN SHOWN TO BE UNAFFECTED BY THE REMOVAL. THE GOLD DIE-BOND EUTECTIC TYPICALLY USED IN CERAMIC PACKAGES IS COVERED WITH PHOTORESIST PREVENTING DEPOSITION OF AUF2 OVER THE DIE SURFACE INHIBITING FURTHER ETCH. HYDROGEN IS ADDED TO THE CF4 ETCHANT GAS TO IMPROVE THE SIO2:SI ETCHING SELECTIVITY.

861024	FAILURE ANALYSIS OF SURFACE MOUNTED INTERCONNECTION	LAU,J.H. RICE,D.W.	HEWLETT-PACKARD CO.	PROCEEDINGS, (1986) ISTFA, Pages 73-82	22860-012

AN ELASTO-PLASTIC ANALYSIS OF THE THERMAL STRESSES AND STRAINS IN A SURFACE MOUNTED ASSEMBLY IS PRESENTED IN THIS PAPER. A NONLINEAR FINITE ELEMENT METHOD IS USED FOR THIS ANALYSIS. THE ASSEMBLY CONSISTS OF THREE MAJOR PARTS; A PLASTIC LEADED CHIP CARRIER (PLCC) WITH COPPER J-LEAD, A 63WT%SN-37WT%PB SOLDER JOINT, AND A FR-4 EPOXY/GLASS PRINTED CIRCUIT BOARD. BECAUSE OF THE GEOMETRY, THE STIFFNESSDIFFERENCE, AND THE THERMAL EXPANSION MISMATCH BETWEEN THESE PARTS, THE INTERCONNECTION (J-LEAD AND SOLDER) IS SUBJECTED TO A VERY COMPLEX STATE OF STRESS AND STRAIN.

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
861024	FRACTURE CHARACTERISTICS OF POLYCHLOROTRIFLUOROETHYLENE (PCTFE) AT CRYOGENIC ANDAMBIENT TEMPERATURES	SHOEMAKER,M. STERLING,P.	ROCKWELL INTERNATIONAL CORP.	PROCEEDINGS, (1986) ISTFA, Pages 251-259	22860-039

THE USE OF POLYCHLOROTRIFLUOROETHYLENE (PCTFE) THERMOPLASTIC RESIN AS AN AEROSPACE SEAL MATERIAL HAS INITIATED A SYSTEMATIC CORRELATION OF TYPICAL FAILURE MODES WITH OBSERVED FRACTURE SURFACES. TO SUPPORT THIS EFFORT, FRACTURE SURFACES WERE GENERATED AT CRYOGENUC AND AMBIENT TEMPERATURES UNDER STRAIN RATES RANGING FROM 4.2 TO 846.6 MICROMETERS/SEC (0.01 TO 2.0 IN./MIN) FOR FOUR BASIC FRACTURE MODES: TENSILE, SHEAR, FLEXURAL, AND COMPRESSIVE. SEM PHOTOS CLEARLY ILLUSTRATE THE SURFACE FEATURES CHARACTERISTIC OF EACH FAILURE ENVIRONMENT.

861024	MECHANISMS GOVERNING THE HIGH STRAIN FATIGUE BEHAVIOR OF AL-LI-X ALLOYS	SRIVATSAN,T.S. COYNE,E.J.,JR.	LOCKHEED AIRCRAFT CO.	PROCEEDINGS, (1986) ISTFA, Pages 281-295	22860-043

THIS PAPER COMPARES THE FATIGUE PROPERTIES, DEFORMATION AND CYCLIC STRESS RESPONSE OF THE COMMERCIAL AL-LI-CU-MN AND THE EXPERIMENTAL AL-LI-MN AND AL-LI-CU-MG-ZR ALLOYS CYCLED TO FAILURE OVER A RANGEOF PLASTIC STRAIN AMPLITUDES IN DIFFERENT ENVIRONMENTS. AN ABNORMAL PLASTIC STRAIN-FATIGUE LIFE BEHAVIOR WAS OBSERVED FOR ALL THE ALLOY SYSTEMS AND IS ATTRIBUTED TO DIFFERENCES IN THE DISTRIBUTION OFDEFORMATION AS A FUNCTION OF PLASTIC STRAIN AMPLITUDE AND TO A CHANGE IN THE RELATIVE AMOUNTS OF INTERGRANULAR AND TRANSGRANULAR FRACTURE AS A FUNCTION OF STRAIN AMPLITUDE.

861008	HERMETICITY MEASUREMENTS FOR LARGE MICROELECTRONIC PACKAGES	PINSKY,D.A.	RAYTHEON CO.	PROCEEDINGS, (1986) ISHM, Pages 379-382	18618-009

CHIP-TYPE MOISTURE SENSORS WERE MOUNTED IN A VARIETY OF LARGE MICROELECTRONIC PACKAGES. THE PACKAGES WERE SOLDER-SEALED AND WERE MONITORED FOR MOISTURE INTRUSION FOR SIX MONTHS. HELIUM FINE LEAK TESTING AND FLUOROCARBON GROSS LEAK TESTING WERE PERFORMED ON EACH PACKAGE. A CORRELATION BETWEEN HELIUM LEAK RATES AND MOISTURE INTRUSION RATES WAS OBSERVED. A NEW ACCEPT/REJECT LIMIT FOR HELIUM FINE LEAKTESTING IS PROPOSED.

860925	SHEET RESISTANCE MEASUREMENT OF BURIED SHIELDING LAYERS	UNGER,B.A. CHEMELLI,R.C. HART,D.L.	BELL COMMUNICATIONS RESEARCH	PROCEEDINGS, (1986) EOS/ESD SYMPOSIUM, Pages 59-61	20869-009

PLASTIC WRAP MATERIALS USED FOR ELECTRONIC ASSEMBLIES FREQUENTLY CONTAIN BURIED CONDUCTIVE LAYERS TO PROTECT OR SHIELD THE CONTENTS FROM ELECTROSTATIC DISCHARGE DAMAGE DURING HANDLING AND SHIPPING. THE THIN LAYERS ARE FREQUENTLY EVAPORATED AND LAMINATED IN A CONTINUOUS PROCESS MAKING THE DIRECT MEASUREMENT OF THICKNESS OR RESISTIVITY OF THE BURIED LAYER IMPOSSIBLE. THE SHIELDING EFFECTIVENESS OF THE LAYER IS INVERSELY PROPORTIONAL TO ITS RESISTIVITY.

860919	RELAYS, ELECTROMAGNETIC, ESTABLISHED RELIABILITY, GENERAL SPECIFICATION FOR	ANON.	UNKNOWN		19381-000

SPECIFICATION COVERS GENERAL REQUIREMENTS FOR ELECTROMAGNETIC, HERMETICALLY SEALED RELAYS FOR USE IN ELECTRONIC & COMMUNICATION-TYPE EQUIPMENT. THESE RELAYS ARE DESIGNED TO OPERATE OVER FULL RANGE FROM LOW LEVEL TO POWER SWITCHING WITH CONTACT RATINGS UP TO 10 AMPERES TO AC OR DC. FAILURE LEVEL IS ESTABLISHED AT CONFIDENCE LEVEL OF 90% OR QUALIFICATION & 60% FOR MAINTENANCE OF QUALIFICATION BASED ON 100,000 CYCLES AT 125C UNDER THE RATED LOAD CONDITIONS SPECIFIED HEREIN.

860900	EFFECT OF SCREEN TESTS AND BURN-IN ON MOISTURE CONTENT OF HYBRID MICROCIRCUITS	SWANSON,D.W. LICARI,J.J.	ROCKWELL INTERNATIONAL CORP.	SOLID STATE TECHNOLOGY, Vol. 29, No. 9, Pages 125-130	21146-001

CORRELATION OF THE PRESENCE AND AMOUNT OF MOISTURE WITH LEAK RATES OF HERMETICALLY SEALED HYBRID CIRCUITS IS INVESTIGATED. THE EFFECTS OF MIL-STD-883 SCREEN TESTS AND BURN-IN ON BOTH LEAK RATES AND MOISTURE GAS CONTENTS ARE DETERMINED. IT WAS FOUND THAT A DIRECT RELATIONSHIP EXISTS BETWEEN THE LEAK RATE AND THE MOISTURE, OXYGEN, AND ARGON CONTENTS OF A PACKAGE.

860800	DESIGN, MANUFACTURE, AND ASSEMBLY OF HIGH PIN COUNT PLASTIC PIN GRID ARRAY PACKAGES	BLACKSHAW,M.F. DANCE,F.J.	QUALITRON CORP.	SOLID STATE TECHNOLOGY, Vol. 29, No. 8, Pages 141-146	21147-004

THE PROLIFERATION OF VLSI TECHNOLOGY IN GATE ARRAY AND STANDARD CELL CUSTOM CHIP CONFIGURATIONS, AS WELL AS 32 BIT MICROPROCESSORS IS NECESSITATING THE DEVELOPMENT OF NEW, HIGH PERFORMANCE, HIGH PIN COUNT PACKAGING TECHNIQUES. THE USE OF PIN GRID ARRAYS AS AN IMMEDIATE PACKAGING SOLUTION IS ALREADY WIDELY EMPLOYED. THE DESIGN, MANUFACTURE, AND ASSEMBLY OF PLASTIC PIN GRID ARRAY PACKAGES ARE PROPOSED TO RESOLVE SOME OF THE CONCERNS WHICH ARISE WHEN THE TRADITIONAL ALUMINA CERAMIC WITH TUNGSTEN, MOLYBDENUM OR GOLD METALLIZATION IS EMPLOYED.

860701	XICOR X2404 RELIABILITY REPORT (RR-508)	SIGAL, J.	XICOR MILIPITAS, CA (RR-508)		17940-002

THE X2404 IS A 4096 BIT SERIAL EEPROM ORGANIZED AS TWO 256X8 BIT PAGES. THIS MEMORY OPERATES ON A SINGLE 5 V POWER SUPPLY OF ALL OPERATIONS. THIS RELIABILITY STUDYAND THE RESULTS PRESENTED ARE THOSEOF THE X2404 IN A PLASTIC PACKAGE.

860601	XICOR X2816A/X2864A RELIABILITY REPORT (RR-505)	HELFFRICH III, A.B.	XICOR MILIPITAS, CA (RR-505)		17940-005

THE X2804 AND X2816A ARE EEPROMS ORGANIZED 512 X 8 AND 2K X 8 BIT RESPECTIVELY. THIS REPORT IS BASED ON DATA COLLECTED USING THE X2816A IN BOTH PLASTIC AND CERAMIC DIP PACKAGES.

860601	XICOR X2864A RELIABILITY REPORT (RR-507)	PURVIS, L.J.	XICOR MILIPITAS, CA (RR-507)		17940-004

THE X2864A IS A 64K FIT ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY, EEPROM ORGANIZED 8K X 8. THE RELIABILITY STUDY AND RESULTS PRESENTED HERE ARE THOSE OF THE X2864A IN A PLASTIC PACKAGE.

860600	CORROSION FAILURE OF AL-MG ALLOY BONDING WIRES IN PLASTIC PACKAGES	RAMSEY,T.H. PETERSON,J. DOUGLAS,P.	TEXAS INSTRUMENTS	SOLID STATE TECHNOLOGY, Vol. 29, No. 7, Pages 181-185	21149-003

BONDING WIRE MADE FROM AL ALLOYED WITH MG IS NORMALLY USED TO MAKE THE ELECTRICAL INTERCONNECTIONS INSIDE HERMETIC SEMICONDUCTOR PACKAGES. THE USE OF AL WIRE AS A REPLACEMENT FOR GOLD IN NONHERMETIC PLASTIC PACKAGES WOULD BE A CONSIDERABLE ECONOMIC ADVANTAGE. AN AUTOMATED BALL-BONDING PROCESS WITH ELECTRONIC FLAME-OFF AND INITIALLY DESIGNED WITH AL/MG WIRE HAS BEEN DEVELOPED; HOWEVER, INTERGRANULAR CORROSION OF THE WIRE WAS DISCOVERED AFTER TESTING OF PLASTIC ENCAPSULATED DEVICES IN A PRESSURE COOKER ENVIRONMENT.

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
860600	NEGATIVE PRESSURE, SEALED NI-CD CELLS	ANON.	UNKNOWN		24921-000

FOR MORE THAN FOUR YEARS OF VENTED CELL PRODUCTION THE FNC NI-CD SYSTEM DEVELOPED BY DAUG AND MARKETED BY HOPPECKE HAS MADE A SIGNIFICANT STEP IN DIVERSIFICATION BY CREATION OF A SEALED, MAINTENANCE-FREE CELL TYPE. LIKE THE VENTED CELLS, THE SEALED VERSION IS BASED ON THE FIBRE ELECTRODE PLAQUE OF NICKEL COATED PLASTIC COMBINING THE EXCELLENT ACTIVE MASS CONTACT AND THE CYCLE LIFE OF SINTERED PLATES WITH THE DESIGN FLEXIBILITY OF ROLLED PLASTIC BONDED ELECTRODES.

860530	ELECTRICAL CHARACTERISTICS CHANGES IN THE HUMIDITY TEST	MAEDA,N. WADA,T.	MATSUSHITA ELECTRONICS CORPORATION	16TH (1986) SYMPOSIUM ON R & M, Pages 50-51	24604-026

SINCE THE TREND OF SEMICONDUCTOR DEVICES IS TOWARD FINER DIMENSION, HIGHER INTEGRATION AND SMALLER PACKAGE, THE MOISTURE RESISTANCE OF PLASTIC PACKAGE BECOMES THE MORE IMPORTANT. ELECTRICAL CHARACTERISTICS CHANGES ARE IMPORTANT FAILURE MODES OF THE PLASTIC ENCAPSULATED SEMICONDUCTOR DEVICES AS SAME AS ALIMINUM CORROSION WHEN ENCOUNTERED MOIST ENVIRONMENT. IN THIS REPORT FOR THE ELECTRICAL CHARACTERISTICS CHANGES CHANGES THE DEPENDENCE OF BIAS VOLTAGE, TEMPERATURE AND WATER VAPOR PRESSURE IS STUDIED.

860530	EQUIPMENT RELIABILITY IMPROVEMENT THROUGH ANALYSIS OF PLASTIC FILM CAPACITOR FAULTS	RYOKE,T. NISHIMURA,M. IWAOKA,M.	UNKNOWN	16TH (1986) SYMPOSIUM ON R & M, Pages 32029	24604-005

THIS REPORT DESCRIBES HOW THE RELIABILITY OF ELECTRONIC EQUIPMENT PRODUCED HAS BEEN IMPROVED BY DIMINISHING ITS SUCCESSIVE SAME-MODE FAULTS THROUGH A FAULT ANALYSIS INCLUDING A DESTRUCTIVE PHYSICAL ANALYSIS OF ITS COMPONENTS.

860530	HUMIDITY RESISTANCE OF SOP-ICS (SMALL OUTLINE PACKAGE ICS)	WATANABE,Y. YAMAMOTO,H. NAGO,N.	OKI ELECTRIC INDUSTRY CO., LTD.	16TH (1986) SYMPOSIUM ON R & M, Pages 48-49	24604-025

SMALL OUTLINE PACKAGE ICS HAVE BEEN ADAPTED FOR THE PURPOSE OF MINIATURIZATION OF ELECTRONIC EQUIPMENTS AND/OR SYSTEMS. THE ICS HAVE, HOWEVER, SOME PROBLEMS TO BE INVESTIGATED, FOR EXAMPLE, SOLDERINGCONDITIONS, ENVIRONMENTAL RESTRICTION IN PRACTICAL USAGE AND SO ON. THE OUTER DIMENSION OF SOP-ICS ARE GENERALLY ABOUT ONE-THIRD OF THOSE OF DIP ICS. PLASTIC PACKAGES RESULTED IN BOTH THINNER PROTECTIVE LAYERS FOR THE DEVICES BURIED AND SHORTER PATHS OF INERFACES BETWEEN PLASTIC AND LEAD FRAMES.

860530	PROBLEMS IN PRESSURE COOKER TEST	TOI,K. YAMAMOTO,T. YOSHIDA,H.	TABAI ESPEC CORPORATION	16TH (1986) SYMPOSIUM ON R & M, Pages 108-109	24604-054

THE PRESSURE COOKER TEST IS ONE METHOD USED TO EVALUATE RELIABILITY OF THE PLASTIC ENCAPSULATED ICS AND IS A HIGHLY ACCELERATED LIFE TEST TO CHECK HUMIDITY RESISTANCE. HOWEVER, THE PRESSURE COOKER TEST LEAVES A PROBLEM CONCERNING ITS REPRODUCIBILITY. TEST RESULTS DIFFER WITH DIFFERENT TEST APPARATUS AND IT HAS DOUBTS ABOUT RIGHTFULNESS AS TEST METHOD. THIS PAPER DESCRIBES RESULTS OF STUDIES AND TESTS CONDUCTED ON THE FOLLOWING PROBLEMS OF THE PRESSURE COOKER TEST.

860530	RELIABILITY EVALUATION BY INFRARED SPECTRUM ANALYSIS	AKIMOTO,R. EGUCHI,K. SUZUKI,Y.	HITACHI, LTD.	16TH (1986) SYMPOSIUM ON R & M, Pages 62-63	24604-032

PLASTICS TECHNOLOGY IS A KEY FACTOR IN THE IMPROVEMENT OF THE RELIABILITY OF MANUFACTURED GOODS THROUGH THE USE OF INTEGRATED MECHANISMS. IN ORDER TO ASSURE RELIABILITY WHERE ORGANIC MATERIALS LIKE ASPLASTICS ARE USED, INFRARED ANALYSIS IS HELPFUL IN ACCEPTANCNE INSPECTION AND FAILURE ANALYSIS. SEVERAL EXAMPLES AREE INVESTIGATED HERE.

860528	DEVELOPMENT OF EPOXY ENCAPSULANTS FOR SURFACE MOUNTED DEVICES	ITO, S., SUZUKI, H. KITAYAMA, A. TABATA, H.	NITTO ELECTRIC INDUSTRIAL CO., LTD.	PROCEEDINGS, IMC, Pages 462-469	86-09
860507	ACCELERATED CORROSION TESTING IN PRESSURE COOKER AT 130 DEGREES C.	BURGESS,J.F. YERMAN,A.J.	GENERAL ELECTRIC CO.	PROCEEDINGS, (1986) ECC, Pages 119-126	23187-008

THIS PAPER EXAMINES THE CRITICAL PART WHICH SURFACE CONTAMINATION PLAYS IN THE CORROSION PROCESS, PARTICULARLY WHERE CONDENSED WATER FILMS CAN FORM AT THE METAL SURFACE. THE EFFECTIVENESS OF VARIOUS PLASTIC COATING METHODS ARE VIEWED IN THE LIGHT OF THIS CONCEPT. ALUMINUM LEAD BONDS WERE MORE SUSCEPTABLE TO CORROSION THAN EXPECTED. A NUMBER OF MATERIALS WERE IDENTIFIED THAT SHOWED RESISTANCE TO PRESSURE COOKER CONDITIONS.

860507	DIE SURFACE STRESSES IN A MOLDED PLASTIC PACKAGE	NATARAJAN,B. BHATTACHARYYA,B.	INTEL CORP.	PROCEEDINGS, 36TH (1986) ECC, Pages 544-551	23187-018

EXCESSIVE STRESSES ON THE DEVICE SURFACE IN A MOLDED PLASTIC PACKAGE CAN CAUSE MECHANICAL AS WELL AS FUNCTIONAL FAILURES. DEVICE SURFACE RELATED FAILURE MODES AND CAUSAL RELATIONSHIPS ARE IN MANY CASES, NOT WELL QUANTIFIED, AND CONSEQUENTLY, THE MEANS OF IMPROVING THE PACKAGE DESIGN AND THE ASSEMBLY PROCESS TO DEVELOP MARGINS ARE KNOWN ONLY QUALITATIVELY. SINCE SUCH FAILURES MUST BE RELATED TO THESURFACE STRESSES ON THE DEVICE, THIS PAPER EXPLAINS THE STRESSES ON THE DEVICE AFTER DIE ATTACH AND AFTER PLASTIC ENCAPSULATION BY BOTH EXPERIMENTAL AND ANALYTICAL METHODS.

860507	FATIGUE OF 60/40 SOLDER	SOLOMON,H.D.	GENERAL ELECTRIC CO.	PROCEEDINGS, 36TH (1986) ECC, Pages 622-629	23187-023

PLASTIC STRAIN VS. FATIGUE LIFE DATA IS PRESENTED FOR TESTS RUN AT -50 DEGREES C, +35 DEGREES C, +125 DEGREES C, AND +150 DEGREES C. IT WAS FOUND THAT THIS DATA COULD BE CORRELATED BY THE COFFIN-MANSON FATIGUE LAW, WITH AN EXPONENT OF APPROXIMATELY 0.5 FOR THE TESTS RUN AT -35 DEGREES C TO +125 DEGREES C. AT +150 DEGREES C THE EXPONENT WAS REDUCED TO 0.37. THESE RESULTS WERE OBTAINED FOR PLASTIC STRAIN LIMITED TESTS. DIFFERENT RESULTS ARE OBTAINED WHEN TOTAL STRAIN LIMITS ARE EMPLOYED. THE DIFFERENCE IS DISCUSSED.

860507	FLUX PENETRATION AND PRESSURE COOKER FAIL MECHANISM IN PLASTIC IC PACKAGES	MURTUZA,M. LEE,J.C. TAN,R.	TEXAS INSTRUMENTS	PROCEEDINGS, 36TH (1986) ECC, Pages 616-621	23187-022

IN THIS STUDY, HUMIDITY TEST RESULTS OF PLASTIC PACKAGES WITH DIFFERENT METALLIC LEADFRAMES AND MOLDING COMPOUNDS WILL BE DISCUSSED. FAILURE ANALYSIS TO IDENTIFY THE CHEMICAL COMPOSITION AND THE MODEOF CONTAMINANT INGRESS WILL BE SHOWN. A MODEL FOR THE FAILURE MECHANISM WILL BE DISCUSSED. EVALUATIONS PERFORMED ON 16 PIN PLASTIC TEST PACKAGES REVEALED A MECHANISM WITH STRONG EVIDENCE RELATING TO THE ADHESIVE PROPERTIES OF THE LEADFRAME AND EPOXY MOLDING COMPOUND.

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
860507	NEW FAILURE MECHANISMS IN TEMPERATURE AND HUMIDITY STRESS	GUAN,D.Y. GUKELBERGER,T.F. CAHOON,E.C.	IBM CORP.	PROCEEDINGS, 36TH (1986) ECC, Pages 107-110	23187-006

NEW FAILURE MECHANISMS OTHER THAN METAL CORROSION WERE OBSERVED IN HIGH-TEMPERATURE, HIGH-HUMIDITY TESTING OF PLASTIC ENCAPSULATED VLSI MODULES. THE MECHANISMS WERE UNIQUE IN THAT PHYSICAL DEFECTS SUCH AS MICROCRACKS WERE ASSOCIATED WITH THE FAILURES. FAILURES APPEARED AS SINGLE-BIT, COLUMN, OR ROW FAILURES DEPENDING ON CIRCUIT DESIGNS AND PROCESS TECHNOLOGY. ADDITIONALLY, FOR ONE PROCESS DESIGN,IONIC ACCUMULATION CONTRIBUTED TO THE FAILURES. ELECTRICAL DIAGNOSIS, PHYSICAL ANALYSIS, AND FAILURE KINETICS WILL BE DISCUSSED.

860507	SOME PROBLEMS IN THE CORRECT FAILURE ANALYSIS OF PLASTIC ENCAPSULATED SEMICONDUCTOR DEVICES	WILSON,K.J. HENDERSON,J.C. SUTHERLAND,R.R.	BRITISH TELECOM RESEARCH INC.	PROCEEDINGS, 36TH (1986) ECC, Pages 132-137	23187-010

IT IS ESSENTIAL THAT FAILURE ANALYSIS OF SEMICONDUCTOR DEVICES IS ACCURATE, IN ORDER THAT CORRECTIVE EFFORT IS NOT MISDIRECTED. THE PRESENT INVESTIGATION CONCERNED THREE TYPES OF PLASTIC ENCAPSULATEDSEMICONDUCTOR DEVICES WHICH HAD FAILED IN WIDELY DIFFERING ENVIRONMENTS, BUT ALL HAVING SIMILAR FEATURES INCLUDING THE DISTRIBUTION OF BOTH GOLD AND A TRANSPARENT CRAZED FILM OF ALUMINUM CORROSION PRODUCTS ACROSS THE CHIP SURFACES.

860423	DEVELOPMENT OF PLASTIC-SEALED PROXIMITY SWITCH	WAKAMATSU,K. TAMURA,K.	NEC CORPORATION	PROCEEDINGS, 34TH (1986) RELAY CONFERENCE, Pages 4-1 THRU 4-9	25120-004

THE USE OF SENSITIVE SWITCHES TO DETECT LOCATIONS HAS INCREASED GREATLY. THE CONTACTS AND ACTUATORS OF THESE SWITCHES ARE ORDINARILY OPERATED BY TOUCHING AND NOT SEALED. THEREFORE, THESE SENSITIVE SWITCHES DON'T ALWAYS HAVE RESISTANCE TO HARSH ENVIRONMENT.

860411	FATIGUE ANALYSIS FOR CRACK INITIATION	YEN,C.C.S.	NONE	QUALITY AND RELIABILITY ENGINEERING, Vol. 2, No. 3, Pages 199-208	18914-007

FOR THE PREDICTION OF LIFE LEADING TO FATIGUE CRACK INITIATION, A METHOD FOR PERFORMING A CYCLE BY CYCLE LOCAL STRESS ANALYSIS AT THE STRESS CONCENTRATION AREA OF A STRUCTURAL COMPONENT WAS DEVELOPED.ELASTOPLASTIC STRESS STRAIN VALUES ALONG THE HYSTERESIS LOOP ARE TRACED FOR EACH LOAD REVERSAL IN MAKING THE LIFE PREDICTION CALCULATIONS. IN THIS MANNER, THE LOAD SEQUENCE EFFECT AND THE RESIDUAL STRESS DUE TO LOCAL YIELDING ARE INHERENTLY INCLUDED.

860403	INFRARED MICROSCOPY AS APPLIED TO FAILURE ANALYSIS OF P-DIP DEVICES	LEWIS,S.H.	IBM CORP.	PROCEEDINGS, 24TH (1986) ANNUAL RELIABILITY PHYSICS, Pages 99-101	20901-016

INFRARED MICROSCOPY IS AN IMPORTANT TOOL TO THE FAILURE ANALYST, AND ITS USES IN FAILURE MODE IDENTIFICATION ARE BECOMING MORE VARIED AND NUMEROUS. RECENT ADVANCES IN EQUIPMENT HAVE ENABLED HIGH MAGNIFICATION EXAMINATION WITH VERY GOOD RESOLUTION WHEN ANALYZING PLASTIC ENCAPSULATED DEVICES FROM THE BACKSIDE OF THE DIE. THIS PAPER WILL DISCUSS VARIOUS ANOMALIES OBSERVABLE WITH THIS TECHNIQUE AS WELL AS SAMPLE PREPARATION TECHNIQUES AND A DESCRIPTION OF THE IR EQUIPMENT USED.

860403	THE EFFECT OF LONG-TERM STRESS ON FILLER-INDUCED FAILURE IN HIGH DENSITY RAMS	MIYAMOTO,K. NAKAGAWA,O. MITSUHASI,J.	MITSUBISHI CORP.	PROCEEDINGS, 24TH (1986) ANNUAL RELIABILITY PHYSICS, Pages 51-54	20901-009

THE EFFECT OF LONG-TERM HIGH TEMPERATURE STRESS ON THE FILLER-INDUCED FAILURE IN HIGH DENSITY MOS RAMS WAS INVESTIGATED. HIGH TEMPERATURE STORAGE CAUSES VOLUME REDUCTION IN SOME PLASTIC RESINS WHICHENHANCES THE LOCAL STRONG STRESS TO RAM CHIP RESULTING IN THE FILLER-INDUCED FAILURE. THIS PHENOMENON IS WELL EXPLAINED BY THE INCREASE OF LEAKAGE CURRENT IN P-N JUNCTION UNDER LOCAL STRONG STRESS.

860126	MOISTURE PROOF PACKING FOR SURFACE MOUNT PACKAGES			HITACHI SEMICONDUCTOR TECHNICAL REPORT, ER PT 87002	86-01
860100	SURFACE MOUNTING FINE-PITCH CHIP CARRIERS	ROSENGARTH,K.W.,JR. WINKLER,R.R.	MOTOROLA, INC.	ELECTRONIC PACKAGING AND PRODUCTION, Pages 121-123	21539-000

THE SOLUTION TO VLSI LOGIC PACKAGING IS SIMILAR TO THE DESIGN ON THE CHIP ITSELF - A DESIGN INVOLVING MINIATURIZATION. A FINE-PITCH CHIP CARRIER, COUPLED WITH FINE-LINE CIRCUIT BOARD TECHNOLOGY AND COMPLIANT EDGE CLIPS, IS AN APPROACH TO HERMETIC PACKAGING WHICH SIMULTANEOUSLY ADDRESSES HIGHER LEAD COUNT AND THE COMPLIANT INTERCONNECTION REQUIRED FOR RELATIVELY LARGE PACKAGES.

860000	A BOND FAILURE MECHANISM	KOCH, T. RICHLING, W. WHITLOCK, J.		PROCEEDINGS, 24TH (1986) ANNUAL IRPS, Pages 55-60	86-06
860000	A NOVEL METHOD OF EVALUATING MOISTURE RESISTANCE OF SOLDERED PLASTIC ENCAPULATED LSI BY A NEW ULTRASONIC INSPECTION SYSTEM	TANAKA, M., SAKIMOTO, M. OKIKAWA, S., YOSHIDA, T., MUTOH, M., OKI, Y., ORII, Y.	HITACHI	PROCEEDINGS, (1986) ISTFA, Pages 173-177	86-4
860000	ACOUSTIC MICROSCOPY: NONDESTRUCTIVE BOND INSPECTION OF SURFACE MOUNTED COMPONENTS AND DEVICES	KESSLER, L.W. SEMMENS, J.E. CICHANSKI, F.	SONOSCAN, BENSENVILLE, IL	PROCEEDINGS, (1986) ISHM CONFERENCE, Pages 281-284	86-11
860000	COMPREHENSIVE MODEL FOR HUMIDITY TESTING CORRELATION	PECK, D.S.		PROCEEDINGS, 24TH (1986) ANNUAL IRPS, Pages 44-50	86-05

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
860000	DIE SURFACE STRESSES IN A MOLDED PACKAGE	NATARAJAN, B. BHATTACHARYYA, B.		PROCEEDINGS, 36TH (1986) ECC, Pages 544-551	86-7
860000	FLUX PENETRATION AND PRESSURE COOKER FAIL MECHANISM IN PLASTIC IC PACKAGES	MURTUZA, M., LEE, J.C. TAN, R. SCHROEN, W.H., BEDNARZ, G.	TI(SINGAPORE), TI	PROCEEDINGS, 36TH (1986) ECC, Pages 616-621	86-3
860000	PACKAGE AND MOLDING COMPOUND MECHANICS	SHORAKA, F. KINSMAN, K. NATARJAN, B.	INTEL	PROCEEDINGS, (1986) IEPS, Pages 294-312	86-10
860000	PRACTICAL APPLICATIONS OF ACOUSTIC MICROSCOPY IN NONDESTRUCTIVE TESTING OF SEMICONDUCTORS AND HYBRID CIRCUITS	BURTON, M.J. THAKER, D.M.	VG SEMICON, LTD., WEST SUSSEX, ENGLAND	PROCEEDINGS, (1986) ISHM CONFERENCE, Pages 253-258	86-12
860000	SPECIAL PROPERTIES OF MOLDING COMPOUNDS FOR SMALL OUTLINE PACKAGED DEVICES	ITO,S. UHARA,Y. TABATA,H.	NITTO	PROCEEDINGS, 36TH (1986) ECC, Pages 360-365	86-02
860000	STRESS ANALYSIS OF SILICON CHIP AND PLASTIC ENCAPSULANT	SUZUKI, H. TABATA, N. OIZUMI, INAMURA & S.	ELECTRO TECHNICAL RESEARCH LAB., NITTO DENKO,JAPAN	PROC. ACS POLYMERIC MATER: SCI. & ENG., Vol. 55, Pages 811-815	86-8
860000	TAB PACKAGING KEEPS COST LOW FOR HIGH-LEAD-COUNT DEVICES	LEVY,M.	NATIONAL SEMICONDUCTOR CORP.	NATIONAL ANTHEM, Pages 8	21618-000
	AN ADVANCED PACKAGING TECHNIQUE UNDER DEVELOPMENT BY NATIONAL USES TAPE AUTOMATED BONDING (TAB) TO ALLOW THE FABRICATION OF DEVICES WITH UP TO 300 LEADS IN A VERY SMALL AREA - AND WITHOUT COMPROMISINGPERFORMANCE. THE NEW METHOD, CALLED "TAPEPAK", IS DESIGNED FOR AUTOMATION OF THE SURFACE-MOUNT PROCESS. IT COMBINES HIGHLY RELIABLE TAB BONDING IN A LOW-COST MOLDED-PLASTIC PACKAGE WITH A UNIQUE BUILD-IN TEST RING. FEATURING ETCHED COPPER TAPE AS A LEADFRAME AND BONDING MEDIUM, TAPEPAK USES BONDING BUMPS ON THE TAPE'S INNER LEADS.				
851200	RELIABILITY REPORT UPDATE PLASTIC CHIP CARRIER (PCC) PACKAGE	ANON.	NATIONAL SEMICONDUCTOR CORP.		21749-000
	THIS RELIABILITY REPORT UPDATE PRESENTS ADDITIONAL DATA RECENTLY GATHERED ON NATIONAL'S FAMILY OF PLASTIC CHIP CARRIER PACKAGES WITH LEADCOUNTS OF 20, 28, 44, AND 68. THE DATA DEMONSTRATES THAT THE RELIABILITY PERFORMANCE OF PRODUCTS ASSEMBLED IN NATIONAL'S PLASTIC CHIP CARRIER PACKAGE IS EXCELLENT AND IS COMPARABLE TO THE RELIABILITY PERFORMANCE OF PRODUCT ASSEMBLED IN NATIONAL'S STANDARD DUAL-IN-LINE PACKAGE (DIP).				
851107	RELIABILITY EVALUATION OF PLASTIC PACKAGED DEVICES FOR LONG LIFE APPLICATIONS BY THE TEST	BRAMBILLA,P. CANALI,C. FANTINI,F.	TELETTRA, ITALY	MICROELECTRONICS AND RELIABILITY, Vol. 26, No. 2, Pages 365-384	18896-020
	THE RELIABILITY OF TRANSISTORS, BIPOLAR AND CMOS INTEGRATED CIRCUITS ENCAPSULATED IN DIFFERENT TYPES OF PLASTIC PACKAGES WAS INVESTIGATED BY USING THE 85 DEGREES C/85% R.H. TEST WITH APPLIED BIAS ANDRESULTS COMPARED WITH A LONG TERM OPERATING LIFE TEST. PARTICULAR ATTENTION WAS DEVOTED TO POINTING OUT THE INFLUENCE OF TECHNOLOGY, PROCESS CONTROL AND WORKING CONDITIONS ON DEVICE RELIABILITY AND FAILURE MECHANISMS.				
851100	PLASTIC CHIP CARRIER (PCC) TECHNOLOGY	ANON.	NATIONAL SEMICONDUCTOR CORP.		21767-000
	THE PLASTIC CHIP CARRIER (PCC) IS A MINIATURIZED LOW COST SEMICONDUCTOR PACKAGE DESIGNED TO REPLACE THE PLASTIC DUAL-IN-LINE PACKAGE (P-DIP) IN HIGH DENSITY APPLICATIONS. THE PCC UTILIZES A SMALLER LEAD-TO-LEAD SPACING - 0.050" VERSUS 0.100" - AND LEADS ON ALL FOUR SIDES TO ACHIEVE A SIGNIFICANT FOOTPRINT REDUCTION OVER THE P-DIP. FIGURE 1 OF THIS PAPER PROVIDES A REPRESENTATION OF THE PCC DEPICTING THE BASIC QUAD FORMAT WITH LEADS ON ALL FOUR SIDES AND THE REDUCED LEAD SPACING.				
851100	REEVALUATION OF THE EFFECTIVENESS OF THE CLASS S AND CLASS B SCREENING TESTS IN MIL-STD-883, FINAL REPORT - MARCH 1983 THROUGH SEPTEMBER 1985	ERICKSON,J.J.	HUGHES AIRCRAFT CO.		22463-000
	THE PURPOSE OF THIS PROGRAM WAS TO EVALUATE THE SCREENING TESTS USED IN MIL-STD-883 IN ACCORDANCE WITH EXHIBIT A. SCOPE OF WORK IN APPENDIX B. SPECIFICALLY, BURN-IN CIRCUITS AND CONDITIONS FOR VARIOUSINTEGRATED CIRCUIT TECHNOLOGIES WERE EVALUATED. ALSO, THE CONSTANT ACCELERATION SCREEN TEST AND HERMETIC SEAL TESTS WERE EVALUATED. THE METHODS USED TO EVALUATE THESE SCREENING TESTS INCLUDED LITERATURE REVIEWS, THEORETICAL EVALUATIONS, SURVEYS OF MANUFACTURERS, AND TESTING ON VARIOUS INTEGRATED CIRCUIT TECHNOLOGIES AND COMPLEXITIES.				
851023	A NOVEL TECHNIQUE OF EVALUATING A GAP BETWEEN LEAD AND RESIN FOR PLASTIC ENCAPSULATED DEVICES	SAKIMOTO,M. TANAKA,M. OKI,Y.	HITACHI CO.	PROCEEDINGS, (1985) ISTFA, Pages 120-125	18600-020
	THE FLUOROCARBON LEAK TEST USED FOR A GROSS LEAK TEST OF HERMETICALLY SEALED PACKAGES HAS BEEN STUDIED TO EVALUATE A GAP BETWEEN LEAD FRAME AND RESIN FOR PLASTIC ENCAPSULATED LSI IN CONJUNCTION WITH THE PRECONDITIONING OF 65 DEGREES C/95%RH SOAK FOR 168 HOURS.				
851023	AN IMPROVED DECAPSULIZATION TECHNIQUE FOR PLASTIC ENCAPSULATED OPTO COUPLER DEVICES	GORTNEY,B. KNAUS,K.	HEWLETT-PACKARD CO.	PROCEEDINGS, (1985) ISTFA, Pages 114-119	18600-019
	CURRENTLY, IF BOTH SECTIONS OF AN OPTOCOUPLER DEVICE (EMITTER AND DETECTOR) ARE TO BE EXAMINED AFTER DECAPSULATION, A CHEMICAL ETCHING TECHNIQUE IS REQUIRED. THIS TECHNIQUE HAS NUMEROUS DRAWBACKS. THIS WORK DEALS WITH THE ADVANTAGES AND DISADVANTAGES OF THIS DECAPSULATION TECHNIQUE, THE FIXTURE DESIGN ITSELF, AND PROCEDURES FOR DECAPSULATION.				

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
851023	EFFECT OF SPECIMEN GEOMETRY ON FRACTURE ELONGATION OF SUPERPLASTIC ZN-22% AL	SHARIAT,P. LANGDON,T.G.	UNIVERSITY OF SOUTHERN CALIFORNIA	PROCEEDINGS, (1985) ISTFA, Pages 289-298	18600-046

EXPERIMENTS WERE CONDUCTED TO INVESTIGATE THE EFFECT OF SPECIMEN GEOMETRY ON THE FRACTURE ELONGATIONS IN THE THREE REGIONS OF FLOW IN SUPERPLASTIC ZN-22% AL ALLOY. IT IS SHOWN THAT THE GAUGE WIDTH HASVERY LITTLE INFLUENCE ON THE FRACTURE ELONGATION, BUT IN THE SUPER-PLASTIC REGION II THE ELONGATION TENDS TO INCREASE AS THE GAUGE LENGTH IS DECREASED. THE FRACTURE ELONGATIONS ARE ALSO SUBSTANTIALLYREDUCED EITHER WHEN GAUGE LENGTH IS MACHINED INTO A TAPERED PROFILE OR WHEN IT CONTAINS A PREMACHINED NOTCH.

851023	HIGH-TEMPERATURE LONG-TERM RELIABILITY EVALUATION OF PLASTIC ENCAPSULATED LSI	MATSUMOTO,T. NAGANO,J.	NTT ATSUGI ELECTRICAL COMMUNICATIONS LAB	PROCEEDINGS, (1985) ISTFA, Pages 129-133	18600-022

STUDIES OF PLASTIC COMPOUND CHARACTERISTICS AT HIGH TEMPERATURES MAKE IT CLEAR THAT PLASTIC ENCAPSULATED MEMORY LSI FAILURES ARE CAUSED BY STRESS-INDUCED DEGRADATION OF PLASTIC COMPOUND THERMAL PROPERTIES. HIGH TEMPERATURE OPERATING TESTS AT 175 DEGREES C ARE SUPERIOR IN EVALUATING THE QUALITY AND RELIABILITY OF PLASTIC ENCAPSULATED LSIS IN A SHORT PERIOD OF TIME.

851023	TECHNIQUES AND NEW ETCH BLOCK DESIGN TO ENHANCE THE JET ETCH DECAPSULATION	TAN,P.	HEWLETT-PACKARD CO.	PROCEEDINGS, (1985) ISTFA, Pages 134-137	18600-023

THIS PAPER PRESENTS MASKING, ENCAPSULATING AND GRINDING METHODS TO PREPARE A SAMPLE. THESE METHODS ENABLE THE ORIGINAL JET ETCH METHOD TO DECAPSULATE PLASTIC PACKAGES OF ALMOST ANY GEOMETRICAL CONFIGURATIONS. WITHOUT THESE SAMPLE PREPARATION METHODS, THE ORIGINAL JET ETCH SYSTEM CANNOT RELIABLY DECAPSULATE PACKAGES WITH UNEVEN SURFACES, SMALL DIMENSIONS, DEEPLY BURIED DICE, OR DICE THAT ARE TOO CLOSE TO THE PACKAGE SIDE WALLS. ALSO PRESENTED IS A NEW JET ETCH BLOCK DESIGN. THIS IS AN IMPROVEMENT OVER THE ORIGINAL JET ETCH BLOCK DESIGN.

851023	THE EFFECT OF HUMIDITY AND ELECTRIC CURRENT ON THE FATIGUE BEHAVIOR OF ALUMINUM BONDED WIRE	MAGUIRE,D. LIVESAY,B.R. SRIVATSAN,T.S.	GEORGIA INSTITUTE OF TECHNOLOGY	PROCEEDINGS, (1985) ISTFA, Pages 372-380	18600-055

THE HIGH STRAIN, LOW CYCLE FATIGUE BEHAVIOR OF ALUMINUM - 1 PCT. SILICON WIRE BONDS USED IN MICROCIRCUITS WERE EVALUATED AT CYCLIC STRAIN AMPLITUDES GIVING LESS THAN 10 CUBED CYCLES TO FAILURE. THE EFFECTS OF CYCLIC PLASTIC STRAIN AMPLITUDE, HUMIDITY AND D.C. CURRENT WERE INVESTIGATED.

851023	ZYGLO PENETRANT TESTING OF PLASTIC PACKAGE INTEGRITY	TOMASI,D. BARTMESS,M.	IBM CORP.	PROCEEDINGS, (1985) ISTFA, Pages 126-128	18600-021

QUALIFYING PLASTIC DIPS WITH GOOD PACKAGE INTEGRITY IS A PRIME CONCERN FOR THE ELECTRONIC INDUSTRY DUE TO COST CONSIDERATIONS. ZYGLO PENETRANT TESTING SAVES WASTED QUALIFICATION EFFORT AND ALLOWS A PACKAGING ENGINEER TO MONITOR HIS PROCESS. ZYGLO PENETRATION TO THE CHIP SURFACE IS TYPICAL OF CORROSION FAILURES. FURTHERMORE, PDIPS WITH LITTLE OR NO ZYGLO PENETRATION HAVE LESS CORROSION FAILURESTHAN PDIPS WITH DEEP ZYGLO PENETRATION. THIS PAPER DISCUSSES ZYGLO PENETRATION AS A FUNCTION OF TEST PARAMETERS. AN ABBREVIATED PROCEDURE IS DISCUSSED FOR PERFORMING ZYGLO ANALYSIS.

851000	SCANNING LASER ACOUSTIC MICROSCOPY APPLIED TO THE EVALUATION OF MATERIAL INTERCONNECTIONS	DUNN, B.D. COLLINS, P.S.	NOORDWIJK	PROCEEDINGS, 3RD (1985) EUROPEAN SYMPOSIUM ON SPACECRAFT MATERIALS IN SPACE ENVIRONMENT, Pages 263-269	85-15
851000	THERMOPLASTIC SUBSTRATES	HASTIE,W.M.	NONE	CIRCUITS MANUFACTURING, Vol. 25, No. 10, Pages 31-32	21574-000

MOLDING PRINTED CIRCUITS FROM THERMOPLASTIC MATERIALS MOVED BEYOND THE EXPERIMENTAL STAGE IN 1985 AND NOW SEVERAL COMPANIES OFFER INJECTION MOLDED BOARDS ON A FULL PRODUCTION BASIS. EXPERTS SEE TREMENDOUS POTENTIAL FOR MOLDED BOARD DESIGNS INCLUDING RECESSED CIRCUITRY AND 3-D FEATURES SUCH AS COMPONENT SUPPORTS, STRUCTURAL RIBS, FASTENERS AND BATTERY CLIPS. FULLY 3-D CIRCUITRY CAN BE PRINTED ONTOPRODUCT HOUSINGS.

850912	MULTIPURPOSE BOMB FUSE WELL CORROSION PREVENTION INSERT - USAF PRAM PROGRAM FINAL REPORT	PETERS,W.	U.S. AIR FORCE		23337-029

THIS PRAM PROJECT WAS ESTABLISHED TO DEVELOP AN INSERTION PLUG AS A REPLACEMENT FOR THE PLASTIC SHIPPING CAP WHICH IS NOT EFFECTIVE IN PROTECTING FUSE WELLS OF GENERAL PURPOSE BOMBS FROM WATER INTRUSION. CORROSION IN THE FUSE WELL OF A GENERAL PURPOSE BOMB HAS THE GREATEST POTENTIAL OF RENDERING THE BOMB UNSERVICEABLE. THERE ARE APPROXIMATELY 1 1/4 MILLION GENERAL PURPOSE BOMBS IN THE INVENTORY. THE MAJORITY OF THESE ITEMS ARE IN UNCOVERED OUTDOOR STORAGE LOTS.

850900	ELECTRON BEAM RADIATION CURED COATINGS FOR STATIC CONTROL	KEOUGH,A.H.	METALLIZED PRODUCTS	EVALUATION ENGINEERING, Vol. 24, No. 9, Pages 50-56	18691-001

A STARTLING DISCOVERY WAS MADE THAT COATING ONE SIDE OF A PLASTIC FILM WITH AN ELECTRON BEAM CURABLE STATIC DISSIPATIVE COATING INDUCED STATIC DISSIPATIVE PROPERTIES ON THE UNCOATED SIDE OF THE FILM.THIS PHENOMENON HAS BEEN TERMED MASS TRANSPORT AND WILL BE DESCRIBED IN MORE DETAIL. ALSO A BRIEF DESCRIPTION OF ELECTRON BEAM PROCESSING IS INCLUDED TO ASSIST IN THE INTERPRETATION OF THE MASS TRANSPORT PHENOMENON.

850900	RESIDUAL STRESSES IN PLASTICALLY ENCAPSULATED MICROELECTRONIC DEVICES	LIECHTI, K.M.		EXPERIMENTAL MECHANICS, Pages 226-231	85-10
850830	HEAT TRANSFER & THERMAL STRESS ANALYSIS OF PLASTIC ENCAPSULATED ICS	MIYAKE,K. SUZUKI,H. YAMAMOTO,S.	NITTO ELECTRIC INDUSTRIAL CO.	IEEE TRANS ON RELIABILITY, Vol. 34, No. 5, Pages 402-409	18852-001

ANALYTIC APPROACHES OF THERMAL STRESS IN PLASTIC ENCAPSLATED ICS RELIABILITY HAVE BEEN STUDIED USING A SIMPLE, 2 DIMENSIONAL MODEL OF THE CROSS SECTION OF ICS BY THE FINITE ELEMENT METHOD.

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
850805	EPIC: A COST-EFFECTIVE PLASTIC CHIP CARRIER FOR VLSI PACKAGING	SINNADURAI,N.	BRITISH TELECOM RESEARCH INC.	IEEE TRANS ON COMPNT, HYB, & MFG TEC, Vol. 8, No. 3, Pages 386-390	21663-000

WITH THE CONTINUING GROWTH IN COMPLEXITY OF VERY LARGE-SCALE INTEGRATED (VLSI) CHIPS, THERE ARE INCREASING DEMANDS FOR HIGH-PERFORMANCE HIGH-PIN-COUNT MICROPACKAGES CAPABLE OF PROVIDING HIGH RELIABILITY PROTECTION OF THE CHIPS WITHOUT BEING UNDULY COSTLY. STUDIES HAVE CONFIRMED THAT PLASTIC ENCAPSULANTS, PARTICULARLY SILICONES, CAN PROVIDE VERY HIGH RELIABILITY PROTECTION INDEED. THESE OBSERVATIONS LED TO THE CONCEPT OF A NEW PLASTIC CHIP CARRIER, NAMED THE "EPIC," FABRICATED BY PRINTED CIRCUIT BOARD TECHNOLOGIES.

850708	STRESS-INDUCED DEFORMATION OF ALUMINUM METALLIZATION IN PLASTIC MOLDED SEMICONDUCTOR DEVICES	THOMAS,R.E.	MOTOROLA, INC.	IEEE TRANS ON COMPNT, HYB, & MFG TEC, Vol. 8, No. 4, Pages 427-434	21666-000

PLASTIC ENCAPSULATION OF LARGE SEMICONDUCTOR CHIPS HAS RESULTED IN INCREASED STRESS-RELATED FAILUERS SUCH AS CRACKED PASSIVATION, METAL DEFORMATION AND DELAMINATION, CRACKED CHIPS, CRACKED PACKAGES, AND PARAMETER SHIFTS. THE LARGE MISMATCH IN THE COEFFICIENT OF THERMAL EXPANSION BETWEEN THE SILICON CHIP AND THE PLASTIC ENCAPSULANT IS FELT TO BE THE MAJOR CONTRIBUTOR TO THESE FAILURES. IN AN EFFORTTO MINIMIZE STRESS PROBLEMS, MANY MOLD COMPOUND MANUFACTURERS HAVE MODIFIED THEIR FORMULATIONS AND EPOXY RESIN CHEMISTRIES.

850700	A CRITICAL REVIEW OF VLSI DIE-ATTACHMENT IN HIGH RELIABILITY APPLICATIONS	SHUKLA,R.K. MENCINGER,N.P.	INTEL CORP.	SOLID STATE TECHNOLOGY, Vol. 28, No. 7, Pages 67-74	21160-001

VLSI DIE BONDING MATERIALS AND PROCESSES FOR VLSI DIE-ATTACHMENT ARE REVIEWED, INCLUDING THE BONDING MECHANISM, METALLURGY, PROCESS VARIABLES, AND LIMITATIONS OF SOLDERS, ORGANIC ADHESIVES, AND GLASSADHESIVES. THE COMMON DIE BOND RELATED PROBLEMS, DISBONDING, AND DIE CRACKING ARE EXAMINED FROM A FUNDAMENTAL VIEWPOINT AS IS THE ROLE OF WAFER BACKSIDE IN OBTAINING RELIABLE DIE BONDING. IT IS CONCLUDED THAT TWO TECHNOLOGIES - EUTECTIC AND GLASS DIE BONDING - ARE WELL SUITED TO DEAL WITH LARGE DIE SIZES FOR VLSI APPLICATIONS IN HERMETIC PACKAGES.

850700	HERMETIC CHIP CARRIER COMPATIBLE PRINTED WIRING BOARD	HEMLER,P. WILLIAMSON,M. THOMPSON,D.	WESTINGHOUSE		19751-000

THE OBJECTIVE OF THIS PROGRAM WAS TO AID IN THE IDENTIFICATION AND UNDERSTANDING OF HCC TO PWB ATTACHMENT FAILURE MECHANISMS, TO FORMULATE CRITERIA FOR FUTURE PWB'S AND IDENTIFY NEW MATERIALS AND PROCESSES TO MEET THAT CRITERIA.

850700	SELECTION OF STATIC-ELIMINATING BENCHTOP MATERIALS	SAFEER,N.I. MILEHAM,J.R.	SPAULDING FIBRE CO., INC.	MICROCONTAMINATION, Pages 33-44	21470-000

IN THE MOVE TOWARD PARTICLE-FREE ENVIRONMENTS FOR SEMICONDUCTOR PROCESSING, IT HAS BECOME APPARENT THAT SOME OF THE STANDARD BENCHTOP MATERIALS USED FOR STATIC CONTROL ARE NOT ADEQUATE. YEAR ' AGO, THEUSE OF THERMOPLASTIC MATERIALS WAS THE ONLY POSITIVE WAY TO OBTAIN STATIC-DISSIPATIVE, NONMETALLIC TABLETOPS. THE MATERIALS WERE USUALLY PLACED OVER DECORATIVE LAMINATE BENCHTOPS. HOWEVER, THESE MATERIALS HAVE CLEANLINESS LIMITATIONS SINCE THEY TEND TO WEAR READILY, ARE HARD TO KEEP CLEAN, AND ARE VULNERABLE TO CLEANING SOLVENTS.

850600	ACOUSTIC MICROSCOPE FINDS TINY FLAWS IN LITTLE IC'S	AGRAMONTE, F.	SONOSCAN, (BENSENVILLE, IL)	INDUSTRIAL RESEARCH AND DEVELOPMENT MAGAZINE, Pages 132-138	85-17
850600	CHIP CARRIER DOUBLES PIN COUNT BUT KEEPS STANDARDE LEAD SPACING	ADAMS,T.	TEXAS INSTRUMENTS	ELECTRONIC PACKAGING AND PRODUCTION, Pages 142-143	21528-000

A NEW PLASTIC CHIP CARRIER JUST ABOUT DOUBLES THE PIN COUNT OF A PACKAGE WITHOUT INCREASING FOOTPRINT AREA OR REDUCING TRACE WIDTHS. A NEW SURFACE MOUNTING PLASTIC CHIP CARRIER SOON TO BE AVAILABLE FROM TEXAS INSTRUMENTS FOR HIGH PIN COUNT, HIGH DENSITY CUSTOM AND SEMICUSTOM VLSI CIRCUITS, WILL NEARLY DOUBLE THE NUMBER OF AVAILABLE PINS IN STANDARD-SIZED UNITS.

850600	CHIP-SIZE PLASTIC ENCAPSULATION ON TAPE CARRIER PACKAGE	FUJITA,K. ONISHI,T. WAKAMOTO,S.	SHARP CORP.	JOURNAL FOR HYBRID MICROELECTRONICS, Vol. 8, No. 2, Pages 32034	20993-002

TO MEET THE NEED FOR SMALLER SIZE, THINNESS, AND HIGH DENSITY OF ELECTRONIC EQUIPMENT, WE HAVE DEVELOPED A PLASTIC ENCAPSULATION TECHNOLOGY WHICH ACHIEVES OUTER DIMENSIONS OF PLASTIC ENCAPSULATION NEARLY AS SMALL AS THE CHIP IN TAPE CARRIER SYSTEMS. THIS PLASTIC ENCAPSULATED PACKAGE IS ULTRA-THIN AND SMALL WITH A DEVICE THICKNESS OF 500 MICROMETERS OR LESS AND AN ON-CHIP RESIN THICKNESS OF 100 MICROMETERS OR LESS. IN ADDITION, THE NEW PACKAGE EXHIBITS HIGH RELIABILITY OWING TO THE CONTRIVANCES AND IMPROVEMENTS IN PLASTIC ENCAPSULANT AND ENCAPSULATING TECHNOLOGY.

850600	RELIABILITY OF PLASTIC ENCAPSULATED INTEGRATED CIRCUITS IN MOISTURE ENVIRONMENTS	GALLACE, L. ROSENFIELD, M.	RCA, SOLID STATE DIV.	QUALITY AND RELIABILITY ENGINEERING INTERNATIONAL, Vol. 1, No. 2, Pages 105-118	85-16
850522	ELECTRONIC GRADE ADHESIVES, RELIABILITY AND PERFORMANCE	MOONEY,C.T.	EMERSON AND CUMING INC.	PROCEEDINGS, 35TH (1985) ECC, Pages 326-330	23186-033

ADHESIVE MANUFACTURERS HAVE BEEN PRODUCING ELECTRONIC GRADE MATERIALS FOR SEVERAL YEARS. MUCH LIKE THE ELECTRONICS INDUSTRY, TECHNOLOGY HAS EVOLVED RAPIDLY, PRODUCING NEWER, MORE ADVANCED ADHESIVE SYSTEMS FOR THE ELECTRONICS INDUSTRY. THIS PAPER REVIEWS THE INFORMATION AVAILABLE ON THE MECHANISMS BY WHICH AN ADHESIVE CAN CAUSE OR CONTRIBUTE TO THE FAILURE OF AN INTEGRATED CIRCUIT IN A PLASTIC OR CERAMIC PACKAGE.

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
850522	IMPROVED MOISTURE RESISTANCE IN PLASTIC PACKAGES	COLLINS,W.R. POWELL,D.B.	M&T CHEMICALS, INC.	PROCEEDINGS, 35TH (1985) ECC, Pages 14-17	23186-003

PLASTIC (EPOXY) PACKAGES OFFER MANY ADVANTAGES IN SEMICONDUCTOR AND HYBRID MANUFACTURE. HOWEVER, THE INGRESS OF WATER CAN CAUSE FAILURE OF THE DEVICE. MOLDING COMPOUND MANUFACTURERS HAVE DEVELOPED VERSIONS GIVING IMPROVED PERFORMANCE IN 85/85, PRESSURE POT AN BIASED PRESSURE POT TESTS COMPARED TO FIRST GENERATION COMPOUNDS. WE INVESTIGATED THE USE OF A SILOXANE POLYIMIDE AS A PROTECTIVE ENCAPSULANT. WE EMPLOYED A STANDARD OPERATIONAL AMPLIFIER DEVICE AND A LINEAR DEVICE AS THE TEST VEHICLES. THE CHIPS WERE BONDED WITH GOLD EUTECTIC AND WIRE BONDED WITH GOLD WIRE TO MINIMIZE SPURIOUS RESULTS.

850522	RELIABILITY TESTING OF THICK FILM MULTILAYER MATERIALS	NEEDES,C.R.S. BUTTON,D.P.	E.I. DUPONT DE NEMOURS CO.	PROCEEDINGS, 35TH (1985) ECC, Pages 505-511	23186-044

A CORRELATION HAS BEEN DEMONSTRATED BETWEEN THE RESULTS FROM THE ACCELERATED LIFE TESTING OF BOTH AIR- AND NITROGEN-FIREABLE THICK FILM DIELECTRIC MATERIALS AND DATA OBTAINED FROM AN ELECTROLYTIC HERMETICITY TEST. THE CORRELATION IS USEFUL BECAUSE A RAPID ASSESSMENT OF THE RELIABILITY OF A DIELECTRIC CAN BE ACHIEVED IN 1 TO 2 DAYS USING THE ELECTROLYTIC HERMETICITY TEST. THE CORRELATION IS USEFULBECAUSE A RAPID ASSESSMENT OF THE RELIABILITY OF A DIELECTRIC CAN BE ACHIEVED IN 1 TO 2 DAYS USING THE ELECTROLYTIC HERMETICITY TEST.

850522	STRESS-INDUCED DEFORMATION OF ALUMINUM METALLIZATION IN PLASTIC MOLDED SEMICONDUCTOR DEVICES	THOMAS,R.R.	MOTOROLA, INC.	PROCEEDINGS, 35TH (1985) ECC, Pages 37-45	23186-007

PLASTIC ENCAPSULATION OF LARGE SEMICONDUCTOR CHIPS HAS RESULTED IN INCREASED STRESS-RELATED FAILURES SUCH AS CRACKED PASSIVATION, METAL DEFORMATION AND DELAMINATION, CRACKED CHIPS AND PARAMETER SHIFTS. THE LARGE MISMATCH IN THE COEFFICIENT OF THERMAL EXPANSION BETWEEN SILICON AND THE PLASTIC IS FELT TO BE THE MAJOR CONTRIBUTOR TO THESE FAILURES. IN AN EFFORT TO MINIMIZE THE STRESS PROBLEMS, MANY OF THE MOLD COMPOUND MANUFACTURERS HAVE MODIFIED THEIR FORMULATIONS AND THE EPOXY RESIN CHEMISTRY. AS A RESULT, MANY "LOW-STRESS" MOLD COMPOUNDS HAVE BEEN INTRODUCED IN RECENT YEARS.

850522	THE DESIGN, MANUFACTURE, AND ASSEMBLY OF HIGH PIN COUNT PLASTIC PIN GRID ARRAY PACKAGES	BLACKSHAW,M.F. DANCE,F.J.	QUALITRON CORP.	PROCEEDINGS, 35TH (1985) ECC, Pages 199-205	23186-020

THE PROLIFERATION OF VLSI TECHNOLOGY IN GATE ARRAY AND STANDARD CELL CUSTOM CHIP CONFIGURATIONS, AS WELL AS 32 BIT MICROPROCESSORS, IS NECESSITATING THE DEVELOPMENT OF NEW, HIGH PERFORMANCE, HIGH PINGRID ARRAYS (PGAS) AS AN IMMEDIATE PACKAGING SOLUTION, IS ALREADY BEING WIDELY EMPLOYED. THIS PAPER WILL ATTEMPT TO RESOLVE CONCERNS BY REVIEWING THE DESIGN, MANUFACTURE, AND ASSEMBLY OF PLASTIC PIN GRID ARRAY PACKAGES. THIS TECHNOLOGY, BASED UPON ADVANCED PRINTED CIRCUIT BOARD PROCESSING TECHNIQUES, OFFERS IMPROVED ELECTRICAL AND THERMAL PERFORMANCE AND LOWER COST.

850500	MICROCIRCUIT CORROSION AND MOISTURE CONTROL	LOWRY,R.K.	NONE	MICROCONTAMINATION, Pages 63-100	21469-000

THIS ARTICLE DISCUSSES SOME CHEMICAL CONSIDERATIONS OF METALLIZED-IC CORROSION, INCLUDING THE CONTRIBUTORY ROLE OF RESIDUAL IONIC SPECIES. PRECAUTIONS FOR CORROSION PROTECTION AS WELL AS ANALYTICAL METHODS FOR MEASURING MOISTURE IN HERMETIC PACKAGING ARE ALSO DISCUSSED.

850424	HERMETIC SEALING - A SUCCESSFUL PROCESS	HUDSON,W.H.	COMMUNICATIONS INSTRUMENTS, INC.	PROCEEDINGS, 33RD (1985) RELAY CONFERENCE, Pages 3-1 THRU 3-4	25119-003

THIS PAPER WILL EXPLORE THE DEVELOPMENT OF A SUCCESSFUL HERMETIC SEALING PROCESS. I WILL DISCUSS AREAS THAT CAUSE HERMETIC SEAL PROBLEMS AND HOW TO CORRECT THEM. THE AUTHOR WILL PRESENT THE CRITERIA INVOLVED IN SELECTING THE BEST WELDING SYSTEM AND HOW TO USE IT TO GET GOOD SEALS WITHOUT THE USE OF ADJUNCT SEALERS. WHILE WE WILL USE THE HALF SIZE CRYSTAL CAN RELAY PROCESS IN OUR ANALYSIS, THESE OBSERVATIONS ALSO PERTAIN TO THE OTHER RELAYS IN THE CRYSTAL CAN FAMILY OF ELECTROMECHANICAL RELAYS.

850424	MYTH OF D.P.A.	BARLOW,D.A. HERRON,C.A.	GENICOM CORPORATION	PROCEEDINGS, 33RD (1985) RELAY CONFERENCE, Pages 19-1 THRU 19-6	25119-016

THE USE OF DESTRUCTIVE PHYSICAL ANALYSIS (DPA) ON HERMETICALLY SEALED RELAYS IS A VALUABLE PROCEDURE FOR FAILURE ANALYSIS STUDIES AND VERIFICATION OF INTERNAL CONSTRUCTION. HOWEVER, BASED ON THE FINDINGS PRESENTED IN THIS PAPER, DPA SHOULD NOT BE USED TO INSPECT FOR INTERNAL PARTICULATE CONTAMINATION. THE DISCUSSION OF THIS PAPER IS LIMITED TO RELAYS HERMETICALLY SEALED BY WELDING. VARIOUS METHODSOF RELAY EVALUATION AND THEIR RESPECTIVE INTRODUCTION OF PARTICLES INTERNAL TO THE RELAY WERE ANALYZED.

850424	QUALITY CONSISTENCY TEST FOR THE PROCUREMENT OF PLASTIC SEALED RELAYS	DESMET,H. SIMPSON,A.	NORTHERN TELECOM ELECTRONICS, LTD.	PROCEEDINGS, 33RD (1985) RELAY CONFERENCE, Pages 2-1 THRU 2-5	25119-002

THE QUALITY MAINTENANCE PROGRAM (QMP) IS INTENDED TO REDUCE THE USER'S RISK AGAINST CHANCE DEFECTS BY MEASURING THE CONSISTENCY OF PLASTIC SEALED RELAY LOTS. THE PAPER DESCRIBES A METHOD WHERE ONE PARAMETER, CONTACT RESISTANCE IS USED TO MEASURE THE LOT QUALITY AND RELIABILITY. IT FEATURES INCONSISTENCY INDICATORS BASED ON CONTACT RESISTANCE READINGS TAKEN DURING PREDETERMINED SEGMENTS OF THE RELIABILITY LIFE TEST, ECONOMICAL SAMPLE SIZE BASED ON PAST LOTS RESULTS AND LOT SIZE, ASSURED SPECIFIED FIELD PERFORMANCE, AND CONTINUING LOT UNIFORMITY.

850400	IMPLEMENTING COPPER THICK FILM SUBSTRATES FOR SURFACE MOUNTED TECHNOLOGY	ISAACSON,D.R. CASWELL,G.K.	TRACOR INC.	, Pages 1-10	21770-000

THIS PAPER PRESENTS THE IMPLEMENTATION OF LARGE AREA, MULTILAYER COPPER THICK FILM SUBSTRATES FOR INTERCONNECTING THE SURFACE MOUNTED HERMETIC CHIP CARRIERS OF HIGH RELIABILITY, MILITARY CPUS. RATIONALE IS PRESENTED FOR THE SELECTION OF THICK FILM TECHNOLOGY FOR SURFACE MOUNTING AND THE SELECTION OF THE PARTICULAR MATERIALS SYSTEM USED FOR THIS IMPLEMENTATION. THE THICK FILM PROCESS IS DESCRIBED INCLUDING PROCESS IMPROVEMENTS MADE TO INCREASE SUBSTRATE YIELD AND REDUCE THE AMOUNT OF REWORK REQUIRED DURING SUBSTRATE FABRICATION.

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
850400	SOCKETS FOR CHIP CARRIERS PAVE THE WAY TO SMT	BROWN,D. FREEDMAN,M.G.	D. BROWN ASSOCIATES, INC.	ELECTRONIC PACKAGING AND PRODUCTION, Pages 76-79	21440-000

DESIGNED TO COPE WITH A WIDE RANGE OF BURN-IN AND PRODUCTION NEEDS, THERE IS A SOCKET FOR ALMOST ANY PACKAGE OR BOARD DESIGN. ALTHOUGH THERE WILL BE MANY APPLICATIONS SERVED BY ALTERNATIVES LIKE THE PIN GRID ARRAY AND THE QUAD FLAT PACK, A VERY IMPORTANT SEMICONDUCTOR PACKAGE OF THE POST-DIP ERA FOR MSI, LSI AND VLSI SILICON IS GOING TO BE THE CHIP CARRIER. ANYONE WHO HAS USED THEM CAN ATTEST TOTHE FACT THAT THE CHIP CARRIER IS NOT ONE PACKAGE TECHNOLOGY, BUT SEVERAL, COMPRISING LEADED AND LEADLESS DESIGNS, CERAMICS, PRE-MOLDED AND POST-MOLDED PLASTICS AND A NUMBER OF CONTACT PITCHES.

850328	A HELIUM LEAK DETECTOR FOR SMALL COMPONENTS	BERGQUIST,L.E.	MARTIN MARIETTA CORP.	PROCEEDINGS, 23RD (1985) ANNUAL RELIABILITY PHYSICS, Pages 65-67	23195-012

A HELIUM LEAK DETECTION METHOD HAS BEEN DEVELOPED TO LEAK CHECK SMALL HERMETICALLY SEALED COMPONENTS WITH LEAK RATES FROM 2 TO 2 X 10 TO THE -12 POWER ATM CC/S. EQUIVALENT LEAK RATES FROM 2 TO 10 TO THE -6 POWER ATM CC/S CAN BE MEASURED IN A 0.4-CC VOLUME COMPONENT FILLED ONLY WITH ATMOSPHERIC AIR. USE OF A 1% HELIUM TRACER IN A 0.4-CC COMPONENT CAN MEASURE LEAK RATES FROM 2 TO 10 TO THE -8 POWERATM CC/S. A LEAK CHECKING CYCLE REQURIES LESS THAN 30 SECONDS. THE INLET PRESENTLY BEING USED HAS A VOLUME OF 80 CC WITH AN INSIDE DIAMETER OF 1 1/2 IN.

850328	COMPUTER AIDED STRESS MODELING FOR OPTIMIZING PLASTIC PACKAGE RELIABILITY	GROOTHUIS,S. SCHROEN,W. MURTUZA,M.	TEXAS INSTRUMENTS	PROCEEDINGS, 23RD (1985) ANNUAL RELIABILITY PHYSICS, Pages 184-191	23195-031

A COMPUTER-AIDED STRESS ANALYSIS PROGRAM HAS BEEN APPLIED TO RELIABILITY PREDICTION OF VLSI PLASTIC PACKAGES. THE PROCESS OF PLASTIC ENCAPSULATION AND THE TESTING BY TEMPERATURE CYCLING PRODUCE STRESSES IN THE SILICON CHIP AS WELL AS IN THE MOLDING MATERIAL. THESE STRESSES MUST BE MINIMIZED THROUGH SPECIFIC CHOICES OF MATERIAL AND PACKAGE DESIGN. FINITE ELEMENT STRESS MODELING IS USED TO QUANTIFYAND DISPLAY THE EFFECT OF MATERIAL CHOICES, FORM FACTORS, AND INNOVATE PROCESSING TECHNIQUES.

850328	MOISTURE RESISTANCE DEGRADATION OF PLASTIC LSIS BY REFLOW SOLDERING	FUKUZAWA,I. ISHIGURO,S. NANBU,S.	OKI ELECTRIC INDUSTRY CO., (JAPAN)	PROCEEDINGS, 23RD (1985) ANNUAL RELIABILITY PHYSICS, Pages 192-197	23195-032

THIS PAPER PRESENTS THE PROBLEMS ON LSIS THAT ARE MOUNTED BY REFLOW SOLDERING METHOD. THE MODELS FOR THESE PROBLEMS AND THE EVALUATION METHOD ARE PRESENTED. THE STRUCTURE AND RELIABILITY DATA FOR THEIMPROVED PACKAGES ARE PRESENTED.

850328	NEW FILLER-INDUCED FAILURE MECHANISM IN PLASTIC ENCAPSULATED VLSI DYNAMIC MOS MEMORIES	MATSUMOTO,H. YAMADA,M. FUKUSHIMA,J.	MITSUBISHI CORP.	PROCEEDINGS, 23RD (1985) ANNUAL RELIABILITY PHYSICS, Pages 180-183	23195-030

FILLERS IN PLASTIC RESIN CAN GIVE THE LOCAL STRESS TO THE CHIP, WHICH CAUSES A SINGLE-COLUMN-LINE FAILURE IN A SENSITIVE DYNAMIC RAM WITH MARGINAL SENSE AMPLIFIER CIRCUITS. THIS FAILURE CAN BE IMPROVED EFFECTIVELY BY EMPLOYING FILLERS OF SMALL SIZE AND/OR A BUFFER COATING OVER THE CHIP.

850314	PRODUCT EVALUATION OF MIL-C-39006/22 NONSOLID ELECTROLYTE TANTALUM CAPACITORS - DETERMINATION OF THE PERFORMANCE OF THESE CAPACITORS WHEN EXPOSED TO VIBRATION	DIFFOOT,R.O.	HUGHES AIRCRAFT COMPANY	CARTS (1985), Pages 133-140	25110-018

IN A TEST PROGRAM FOR NASA-MARSHALL SPACE FLIGHT CENTER, 90 WET TANTALUM CAPACITORS WERE SUBJECTED TO A PRODUCT EVALUATION TEST IN ORDER TO EVALUATE THEIR OPERATION UNDER VIBRATION. PARTS FROM THREE MANUFACTURERS, PURCHASED TO MIL-C-39006/22 (CLR79 STYLE), WERE SUBJECTED TO THE FOLLOWING TESTS: 1. ELECTRICAL MEASUREMENTS. 2. HERMETICITY. 3. SINUSOIDAL VIBRATION (20 AND 80 GS). 4. RANDOM VIBRATION(51 GS).

850314	SURFACE MOUNT PLASTIC FILM CAPACITORS	PRICE,R. BERNARDI,A.	WESTLAKE CAPACITORS, INC.	CARTS (1985), Pages 31795	25110-001

IN ORDER TO MEET THE CHANGING NEEDS OF ITS CUSTOMERS, THE PLASTIC FILM CAPACITOR INDUSTRY HAS BEEN DOING INTENSIVE RESEARCH AND DEVELOPMENT INTO THE PRODUCTION OF A "PRACTICAL" METALLIZED POLYESTER FILM CHIP CAPACITOR FOR USE IN SURFACE MOUNT APPLICATIONS. IN THE PAST, MULTILAYER CERAMIC CAPACITOR CHIPS HAVE BEEN VIRTUALLY THE ONLY TYPE OF CAPACITOR USED FOR SUCH APPLICATIONS. THE INTENT OF THIS PAPER IS TO PRESENT DETAILS ON THE VARIOUS CRITERIA OF POLYESTER FILM CHIP CAPACITORS AND TO MAKE SUGGESTIONS ON THEIR PROPER UTILIZATION.

850300	EVALUATION OF HERMETIC CHIP CARRIER TECHNOLOGY, FINAL REPORT	ANON.	U.S. ARMY (QE-84-702-31)		20584-000

HERMETIC CHIP CARRIERS (HCC) INCLUDE THE FAMILY OF LEADLESS, LEADED, AND GRIDED PIN ARRAYS (GPA) WHICH ARE DESIGNATED TO CONTAIN VERY LARGE SCALE INTEGRATED CIRCUITS (VLSI) AND VERY HIGH SPEED INTEGRATED CIRCUITS (VHSIC) AS WELL AS HYBRID MICROCIRCUIT CHIPS (RESISTORS, CAPACTIROS, INDUCTORS). THIS DOCUMENT IS AN ACCUMULATION OF THE STATE OF THE ART IN SURFACE MOUNTING TECHNIQUES, PROCEDURES, AND EXPERIENCES GLEANED FROM LITERATURE, GOVERNMENT DOCUMENTS, AND CONVERSATIONS WITH MAJOR USERS OF THESE DEVICES.

850200	ACOUSTIC MICROSCOPY IMPROVES INTERNAL RELIABILITY OF IC PACKAGING	ADAMS, T.E.		SEMICONDUCTOR INTERNATIONAL, Pages 100-104	85-12
850200	SMART WEAPONS RELIABILITY SUPPORT - FINAL REPORT, FEBRUARY 1985	DYLIS,D.F.	IITRI/RELIABILITY ANALYSIS CENTER		19889-000

THIS REPORT SUMMARIZES EFFORTS PERFORMED BY THE RELIABILITY ANALYSIS CENTER (RAC) FOR THE U.S. ARMY ARMAMENT RESEARCH AND DEVELOPMENT CENTER. IT WAS CONDUCTED DURING THE PERIOD MAY 1984 TO NOVEMBER 1984 IN SUPPORT OF THE SMART WEAPONS PROGRAM. THE EFFORTS REFLECT RECOMMENDATIONS OF AN ENVIRONMENTAL TEST PROGRAM FOR NON-HERMETIC ENVIRONMENTALLY PROTECTED TAPE AUTOMATED BONDED (EP/TAB) MICROCIRCUITS.

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
850200	TUNNEL DIODES COMPLEMENT HIGH-PERFORMANCE DETECTORS	TATUM,J. HINTON,K.	TRW INC.	MICROWAVES & RF, Vol. 24, No. 2, Pages 115-124	21166-002

A NEW PLANAR BLACK DOIDE PROCESSING TECHNOLOGY PRODUCES RUGGED, HIGHLY MATCHED DIODES IDEAL FOR USE IN AIRBORNE EW DETECTORS. THE DEVICES ARE AVAILABLE IN A VARIETY OF HERMETIC PACKAGES.

850118	IC QUALITY GRADES: IMPACT ON SYSTEM RELIABILITY & LIFE CYCLE COST	PRIORE,M.G.	IITRI/RELIABILITY ANALYSIS CENTER (SOAR-3)		20597-000

THIS TEXT PRESENTS THE MAIN FACTORS GOVERNING THE RELATIVE RELIABILITY AND APPLICABILITY OF PLASTIC COMMERCIAL (SCREENED AND UNSCREENED), HERMETIC COMMERCIAL, AND JANN-QUALIFIED INTEGRATED CIRCUITS (ICS). SPECIFIC AREAS ADDRESSED INCLUDE INITIAL COSTS AND PROCUREMENT LEAD TIMES, APPLICATION STRESSES OF PARTICULAR CONCERN WITH PLASTIC ENCAPSULATED ICS, PROCUREMENT PRACTICES FOR OBTAINING THE BEST AVAILABLE PLASTIC ICS, AND LIFE CYCLE COST ANALYSIS FOR ALTERNATIVE QUALITY GRADES.

850000	A NOVEL TECHNIQUE OF EVALUATING A GAP BETWEEN LEAD AND RESIN FOR PLASTIC ENCAPSULATED LSI	SAKIMOTO, M. TANAKA, Y. OKI, Y., ORII, Y.	HITACHI	PROCEEDINGS, (1985) ISTFA, Pages 120-125	85-03
850000	COMPUTER AIDED STRESS MODELLING FOR OPTIMIZING PLASTIC PACKAGE RELIABILITY	GROOTHUIS, S. SCHROEN, W.H. MURTUZA, M.	TI	PROCEEDINGS, 23RD (1985) IRPS, Pages 184-191	85-01
850000	LOW STRESS RESIN ENCAPSULANT FOR SEMICONDUCTOR DEVICES	KUWATA, K. IKO, K. TABATA, H.	KAMEYAMA PLANT, NITTO ELECTRIC INDUSTRIAL CO.	PROCEEDINGS, 35TH (1985) ECC, Pages 18-22	85-11
850000	MOISTURE RESISTANCE DEGRADATION OF PLASTIC LSI'S BY REFLOW SOLDERING	FUKUZAWA, I. ISHIGURO, S. NAMBU, S.	OKI ELECTRIC	PROCEEDINGS, 23RD (1985) IRPS, Pages 192-197	85-02
850000	NONDESTRUCTIVE DIE ATTACH BOND EVALUATION COMPARING SCANNING LASER ACOUSTIC MICROSCOPY (SLAM) AND X-RADIOGRAPHY	SEMMENS, J.E. KESSLER, L.W. AGRAMONTE, F.	SONOSCAN, (BENSENVILLE, IL)	PROCEEDINGS, 35TH (1985) ECC, Pages 250-258	85-14
850000	NONDESTRUCTIVE EVALUATION BY ACOUSTIC MICROSCOPY AS APPLIED TO THE FAILURE ANALYSIS OF MICROELECTRONICS	MICHAEL, J.A. FULTZ, W.W.	DELCO ELECTRONICS	PROCEEDINGS, (1985) ISTFA, Pages 181-186	85-05
850000	NONDESTRUCTIVE INSPECTION OF CERAMIC CAPACITORS: DETECTION OF APPARENT FLAW GROWTH IN PARTS SUBMITTED TO LOW-VOLTAGE HUMIDITY EXPOSURE	SEMMENS, J.E. KESSLER, L.W. EWELL, G.	SONOSCAN (BENSENVILLE, IL), THE AEROSPACE CORP.	PROCEEDINGS, (1985) ISTFA, Pages 193-201	85-07
850000	PLASTIC PACKAGING, ALL THERE IS TO KNOW	SCHROEN,W.H.	TEXAS INSTRUMENTS INCORPORATED	IRPS (1985) TUTORIAL NOTES, Pages 4.1-4.18	24868-004

THIS TUTORIAL PRESENTATION REVIEWS THE MOST IMPORTANT CONTRIBUTIONS TO PLASTIC PACKAGE RELIABILITY: DESIGN OF PACKAGES FOR VARIOUS SIZE SILICON CHIPS (ESPECIALLY OF THE SURFACE MOUNT VARIETY), SELECTION OF MATERIALS FOR PLASTIC COMPOUNDS AND LEADFRAMES, AND IMPACT OF ASSEMBLY AND PACKAGING PROCESSES AND THEIR CONTROL. EXAMPLES WILL BE SHOWN OF COMPUTER-SIMULATED STRESS DISTRIBUTIONS IN PLASTIC PACKAGES, AND HOW THEY ARE VERIFIED BY STRAIN GAUGE MEASUREMENTS. MOISTURE AND STRESS TEST STRUCTURES ARE DESCRIBED WHICH CHARACTERIZE PLASTIC MATERIALS AND SERVE AS PROCESS CONTROLS.

850000	PRACTICAL APPLICATIONS OF ACOUSTIC MICROSCOPY IN FAILURE ANALYSIS	BURTON, N.J. THAKER, D.M.	VG SEMICON, LTD, (WEST SUSSEX, ENGLAND)	PROCEEDINGS, (1985) ISTFA, Pages 187-192	85-06
850000	SCANNING LASER ACOUSTIC MICROSCOPY STUDY OF DIE ATTACH INTEGRITY	PRASAD, S.K.	INTEL	PROCEEDINGS, (1985) ISTFA, Pages 202-209	85-08
850000	SELECTION OF LEADFRAME MATERIALS FOR PLASTIC PACKAGE	SAJJA, V. DIORIO, M. BELANI, J.		PROCEEDINGS, 5TH (1985) ANNUAL IEPS, Pages 50-54	85-13
850000	STRESS-INDUCED DEFORMATION OF ALUMINIUM METALLIZATION IN PLASTIC MOLDED SEMICONDUCTOR DEVICES	THOMAS, R.E.		PROCEEDINGS, 35TH (1985) ECC, Pages 37-45	85-09
850000	ZYGLO PENETRANT TESTING OF PLASTIC INTEGRITY	TOMASI, D. BARTMESS, M.	IBM	PROCEEDINGS, (1985) ISTFA, Pages 126-128	85-04
840000	CURING STRESSES IN AN EPOXY POLYMER	SRIVASTAVA, A.K. WHITE, J.R.	DEPARTMENT OF METALLURGY & ENGINEERING MATERIALS	J. APP POLYMER SCI., Vol. 29, Pages 2155-2161	84-5
840000	FAILURE MECHANISM OF DIE CRACKING DUE TO IMPERFECT DIE ATTACHMENT	CHIANG, S.S. SHUKLA, R.K.		PROCEEDINGS, 34TH (1984) ECC, Pages 195-202	84-4
840000	LOW STRESS EPOXY MOLDING COMPOUNDS FOR VLSI DEVICES	KAKEI, M. IKEDA, Y. KOSHIBE, S.	NIKKEI ELECTRONICS MICRODEVICES	, Vol. 6.11, Pages 82-92	84-2

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
840000	SCANNING LASER ACOUSTIC MICROSCOPY WITH SOME APPLICATIONS TO ADHESION	ARNOLD, W. REITER, H.	FRAUENHOFER-INST. FOR NON-DESCTRUCTIVE TESTING (FDR)	PROCEEDINGS, INTERNATIONAL CONFERENCE ON ADHESION	84-6
840000	THE DETERMINATION OF FABRICATION STRESSES IN MICROELECTRONIC DEVICES	LIECHTI, K.M. THEOBALD, P.		PROCEEDINGS, 34TH (1984) ECC, Pages 203-208	84-3
840000	THE DEVELOPMENT OF MINI PLASTIC IC PACKAGING FOR DIP SOLDERING	SASAKI, S. SERIZAWA, K. ISHI, I.	HITACHI	PROCEEDINGS, 34TH (1984) ECC	84-1
830000	STRESS ANALYSIS OF PASSIVATION FILM CRACK FOR PLASTIC MOLDED LSI CAUSED BY THERMAL STRESS	OKIKAWA, S. SAKIMOTO, M. TANAKA, M.		PROCEEDINGS, (1983) ISTFA, Pages 275-280	83-1
830000	THE QUALITY OF DIE-ATTACHMENT AND ITS RELATIONSHIP TO STRESSES AND VERTICAL DIE-CRACKING	VAN KESSEL, C.G.M. GEE, S.A. MURPHY, J.J.		TRANS. IEEE/CHMT, Vol. CHMT-6, No. 4, Pages 414-420	83-2
820900	LEADFRAME MATERIALS FOR PACKAGING SEMICONDUCTORS	ZARLINGO, S.P. SCOTT, J.R.	BRASS GROUP, OLIN CORP.	SEMICONDUCTOR INTERNATIONAL, Pages 111-124	82-5
820900	NONDESTRUCTIVE TESTING OF INTERCONNECT WELDS USING THE SCANNING LASER ACOUSTIC MICROSCOPE	VORRES, C.L., ORAVEZ, M.G. YUHAS, D.E. SEMMENS, J.E.	SONOSCAN, (BENSENVILLE, IL)	PROCEEDINGS, 16TH (1982) IEEE PHOTOVOLTAIC SPEC. CONF., Pages 102-107	82-6
820000	FLUORESCENT PENETRATION TESTING FOR FAILURE ANALYSIS ON PLASTIC ENCAPSULATED INTEGRATED CIRCUITS	OKIKAWA, S. MIKINO, H. SUZUKI, H.	HITACHI	PROCEEDINGS, (1982) ISTFA, Pages 125-132	82-1
820000	FUNDAMENTALS OF ACOUSTICS	KINSLER, L.E. FREY, A.R. COPPENS, A.B.		JOHN WILEY & SONS (PUBLISHER), Vol. 3RD, Pages 124-137	82-3
820000	METHOD FOR USING LIQUID PENETRANTS, NONDESTRUCTIVE TESTING HANDBOOK		AMERICAN SOCIETY FOR NONDESTRUCTIVE TESTING/ASM INTERNATIONAL	NONDESTRUCTIVE TESTING HANDBOOK, Vol. 2, No. 2	82-2
820000	NON-DESTRUCTIVE TESTING OF ADHESIVELY BONDED STRUCTURES WITH ACOUSTIC METHODS	CURTIS, G.J. SZILARD, J.	ULTRASONIC TESTING	JOHN WILEY & SONS (PUBLISHER), Pages 495-553	82-4
810000	EXPERIMENTAL AND MATHEMATICAL DETERMINATION OF MECHANICAL STRAINS WITHIN PLASTIC IC PACKAGES AND THEIR EFFECTS ON DEVICES DURING ENVIRONMENTAL TESTS	USELL, R.J. SMILEY, S.A.	BURROUGHS CORP.	PROCEEDINGS, (1981) IRPS, Pages 65-73	81-1
810000	LOWER STRESS ENCAPSULANTS	JORDAN, R.B.	HYSOL DIVISION, DEXTER CORPORATION	PROCEEDINGS, 31ST (1981) ECC, Pages 130-135	81-6
810000	MICROELECTRONICS FAILURE ANALYSIS TECHNIQUES	DOYLE, B. MORRIS, W.L.	G.E. CO. (SYRACUSE, NY), RADC (GAFB, NY) RELIABILITY ANALYSIS CENTER, (ROME, NY)	MFAT-1	81-4
810000	NEW QUANTITATIVE MEASUREMENTS OF IC STRESS INTRODUCED BY PLASTIC PACKAGES	SPENCER, J.L., SCHROEN, W.H. BEDNARZ, G.A., BRYAN, J.A. METZGAR, T.D., CLEVELAND, R.D., EDWARDS, D.R.	TI	PROCEEDINGS, (1981) IRPS, Pages 74-80	81-2
810000	ON THE PREDICTION OF RESIDUAL STRESSES IN POLYMERS	WILLIAMS, J.C.		PLASTIC AND RUBBER PROCESSING AND APPLICATIONS, Vol. 1, No. 4, Pages 369-377	81-5
810000	RELIABILITY STUDY OF PLASTIC ENCAPSULATED COPPER LEAD FRAME/EPOXY DIE ATTACH PACKAGING SYSTEM	HOWELL, J.R.		PROCEEDINGS, 19TH (1981) IRPS, Pages 104-110	81-7
810000	RELIABILITY TESTS AND STRESS IN PLASTIC INTEGRATED CIRCUITS	SCHROEN, W.H. SPENCER, J.L. BRYAN, J.A.	TI	PROCEEDINGS, (1981) IRPS, Pages 81-87	81-3

Date	Title	Author(s)	Performing Agency	Journal	RAC DAN
800000	DEFORMATION OF AL METALLIZATION IN PLASTIC ENCAPSULATED SEMICONDUCTOR DEVICES CAUSED BY THERMAL SHOCK	ISAGAWA, M. IWASAKI, Y. SUTOH, T.		PROCEEDINGS, 18TH (1980) ANNUAL IRPS, Pages 171-177	80-1
780000	SWELLING AND GLASS TRANSITION RELATIONS FOR EPOXY MATRIX MATERIAL IN HUMID ENVIRONMENT	MCKAGUE, JR., E.L. REYNOLDS, J.D. HALKIAS, J.E.		J. APPLIED POLYMER SCIENCE, Vol. 22, Pages 1643-1654	78-2
780000	THE MECHANISMS OF ELEVATED TEMPERATURE PROPERTY LOSSES IN HIGH PERFORMANCE STRUCTURAL EPOXY RESIN MATRIX MATERIALS AFTER EXPOSURES TO HIGH HUMIDITY ENVIRONMENTS	BROWNING, C.E.		POLYMER ENGINEERING AND SCIENCE, Vol. 18, Pages 16-24	78-1

APPENDIX E:

RAC PRODUCTS

RAC Product Order Form

(DP92-1)

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CRTA-PEM	Plastic Microcircuit Packages: A Technology Review	50.00	60.00		
CRTA-QML	Qualified Manufacturer's List: Device Manufacturing Procurement Technique	50.00	60.00		
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DSR-4	Discrete Semiconductor Device Reliability	100.00	120.00		
FMD-91	Failure Mode/Mechanism Distributions 1991	100.00	120.00		
FTA	Fault Tree Analysis Application Guide	80.00	90.00		
MDR-21	Microcircuit Device Reliability Trend Analysis Databook	100.00	120.00		
MDR-22	Microcircuit Screening Analysis	125.00	145.00		
MFAT-1	Microelectronics Failure Analysis Techniques - A Procedural Guide	140.00	180.00		
MFAT-2	GaAs Microcircuit Characterization & Failure Analysis Techniques	100.00	120.00		
MFAT-1&2	Combined set of MFAT-1 and MFAT-2	200.00	260.00		
NONOP-1	Nonoperating Reliability Databook	150.00	170.00		
NPRD-91	Nonelectronic Parts Reliability Data 1991	150.00	170.00		
NPRD-91P	Nonelectronic Parts Reliability Data 1991 (IBM PC database)	400.00	440.00		
NPS-1	Analysis Techniques for Mechanical Reliability	60.00	70.00		
PRIM-92	A Primer for DoD Reliability, Maintainability ,Safety and Logistics Stds	120.00	140.00		
RAC-NRPS	Nonoperating Reliability Prediction System (Includes NONOP-1)	1400.00	1450.00		
RDSC-1	Reliability Sourcebook	25.00	35.00		
RMST-91	Reliability and Maintainability Software Tools 1991	50.00	60.00		
RQ	RAC Quarterly (Subscription for four issues/one year)	30.00	35.00		
SOAR-2	Practical Statistical Analysis for the Reliability Engineer	40.00	50.00		
SOAR-4	Confidence Bounds for System Reliability	50.00	60.00		
SOAR-5	Surface Mount Technology: A Reliability Review	60.00	70.00		
SOAR-6	ESD Control in the Manufacturing Environment	60.00	70.00		
SOAR-7	A Guide for Implementing Total Quality Management	75.00	85.00		
SOAR-8	Process Action Team (PAT) Handbook	80.00	90.00		
TOOLKIT	RADC Reliability Engineer's Toolkit	10.00	20.00		
VPRED	VHSIC Reliability Prediction Software	150.00	170.00		
VZAP-91	Electrostatic Discharge Susceptibility Data 1991	150.00	170.00		
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TESTABILITY DESIGN AND ASSESSMENT TOOLS

1991

Prepared by:

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13. ABSTRACT (Maximum 200 words)

This Critical Review and Technology Assessment (CRTA) on testability provides basic definitions for testability and describes the benefits of performing design-for-testability (DFT) principles early in a systems design phase. Having defined testability and DFT, three of the most common testability assessment methodologies are described in detail. The three methods are controllability/observability (C/O), heuristic scoring techniques, and dependency modeling.

The last part of the CRTA provides detailed descriptions of available testability assessment tools that are based on one or more of the three described methodologies. The tools are neither compared nor rated, and the information provided is on capabilities and outputs. A total of ten (10) tools are described, and information is provided on who to contact for further information on each tool.

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FOREWORD

Welcome to the field of testability analysis. This Critical Review and Technology Assessment (CRTA) has been designed to provide both the beginning and experienced analyst with information on the following items:

- Testability definitions, concepts and benefits
- Evolution of testability analysis tools
- Information on available testability analysis tools
- Explanations of analysis methodologies employed in the most common testability analysis tools
- Examples of how the tools can be used in compliment to address testability design and specific parts of MIL-STD-2165; "Testability Program for Electronic Systems and Equipments."

The objective of this CRTA is to make the reader aware of the tools that have been specifically developed to aid a testability analysis, the application and limitation of these tools, and the methodology that the tools employ. Tools that are digital automatic test program generators (DATPGs) that provide some testability measures are not detailed in this report.

The purpose of this document is to provide information that will give the reader the necessary background to both understand the intent of testability, and to make a sound decision in acquiring the tool(s) that best fit their needs. Information regarding the cost of testability tools and licensing agreements can be found in the RAC publication on Reliability & Maintainability Software Tools, RAC order no. RMST-91.

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ACRONYMS AND ABBREVIATIONS

A/D	-	Analog-to-Digital
ACE-APT	-	APT Computational Environment - Alphatech Program for Testability
A_o	-	Operational Availability
ASIC	-	Application Specific Integrated Circuit
ASTEP	-	Advanced System Testability Evaluation Program
ATE/ETE	-	Automatic Test Equipment/External Test Equipment
ATG	-	Automatic Test Generator
BCS	-	Bench Check Serviceable
BIT	-	Built-In-Test
BITE	-	Built-In-Test Equipment
C/O	-	Controllability/Observability
CAD	-	Computer Aided Design
CAE	-	Computer Aided Engineering
CAFIT	-	Computer Aided Fault Isolation/Testability
CAMELOT	-	Computer Aided Measure for Logic Testability
CDDB	-	Computer Diagnostic Data Base
CFBD	-	Component Feedback Dominance
CND	-	Cannot Duplicate
CODMOD	-	Consolla and Danner Model
COMET	-	Controllability Observability - Measure for Testability
COP	-	Controllability/Observability Program
COPTER	-	Controllability - Observability - Predictability - Testability Report
CRTA	-	Critical Review and Technology Assessment
D/A	-	Digital-to-Analog
DATPGs	-	Digital Automatic Program Generators
DEP	-	Dependency
DFR	-	Detected Failure Rate
DFT	-	Design for Testability
DOE	-	Department of Energy
DTA	-	Daisy Testability Analyzer
EXDEP	-	External Dependency
FAT	-	False Alarm Tolerance
FBD	-	Functional Block Diagram
FD/FI	-	Fault Detection/Fault Isolation
FFM	-	False Failure Measure

FIG	-	Fault Isolation Group
FIR	-	Fault-Isolation Indicator Report
FLC	-	Feedback Loop Complexity
FMEA	-	Failure Mode Effects Analysis
FMIL	-	Feedback Modified Isolation Level
FMTL	-	Feedback Modified Test Leverage
FOM	-	Figure of Merit
FQ	-	Fault Quantum
FR	-	Fault Resolution
HAT	-	Heuristic Advisor for Testability
HECTOR	-	Heuristic Controllability & Observability Analysis
HFM	-	Hidden Failure Measure
I-CAT	-	Interactive Computer Aided Testability
I/O	-	Input/Output
IC	-	Integrated Circuit
ID	-	Interface Device
IDSS	-	Integrated Diagnostic Support System
IL	-	Isolation Level
IMFFM	-	Input Modified False Failure Measure
IMHFM	-	Input Modified Hidden Failure Measure
IMPHFM	-	Input Modified Percent Hidden Failure Measure
ITFOM	-	Inherent Testability Figure of Merit
ITTAP	-	Interactive Testability Analysis Program
ITTTR	-	Intrinsic Test Time to Repair
JTAG	-	Joint Test Action Group
LCC	-	Life Cycle Cost
LONGMOD	-	Longendorfer Model
LRU	-	Line Replaceable Unit
LSAR	-	Logistic Support Analysis Record
MILMOD	-	Military Model
NDP	-	Nondetection Percentage
NRTL	-	Nonredundant Test Leverage
P&ID	-	Piping & Instrumentation Diagram
PC	-	Personal Computer
PCB	-	Printed Circuit Board
PFD	-	Probability of Fault Detection
PHFM	-	Percent Hidden Failure Measure
PREDICT	-	Probabilistic Estimation of Digital Circuit Testability

PROTEST - Probabilistic Testability Analysis
RAC - Reliability Analysis Center
RADC - Rome Air Development Center
REFDES - Reference Designator
RI - Replaceable Item
RISP - Reduced Intrusion Scan Path
RMST - Reliability & Maintainability Software Tools
RTOK - Retest OK
SAG - Suspect Ambiguity Group
SCOAP - Sandia Controllability Observability Analysis Program
SNL - Sandia National Laboratories
SRU - Shop Replaceable Unit
SSM - Standard System Model
STAMP - System Testability and Maintenance Program
STAT - System Testability Analysis Tool
TCE - Test Coverage Estimate
TDEP - Test Dependency
TEST - Time Efficient Sequence of Tests
TFBD - Test Feedback Dominance
TFOM - Testability Figure of Merit
TIDEP - Test Interdependency
TL - Test Leverage
TLMAX - Maximum Test Leverage
TLMIN - Minimum Test Leverage
TMEAS - Testability Measurement
TP - Test Point
TPS - Test Program Set
TR - Test Redundancy
TU - Test Uniqueness
UUT - Unit Under Test
VHDL - VHSIC Hardware Description Language
VHSIC - Very High Speed Integrated Circuit
VICTOR - VLSI Identifier of Controllability, Testability, Observability, Redundancy
WSTA - Weapon System Testability Analyzer
XM - Excess Test Measure

1.0 TESTABILITY AND DESIGN - AN INTRODUCTION

1.1 What is Testability?

Testability is the extent to which a system or unit design supports fault detection and fault isolation (FD/FI) within the bounds of specific time, confidence, complexity, and cost effectiveness limits. A system developed using Design for Testability (DFT) criteria will provide the necessary test points to facilitate the incorporation of Built-In-Test (BIT) and support Automated/External Test Equipment (ATE/ETE) while meeting FD/FI requirements. Testability by design will achieve the required FD/FI goals and help to meet Operational Availability (Ao) within complexity and cost constraints. A design methodology utilizing DFT techniques to achieve a high level of testability must be considered early in the design phase.

The goal of testability by design is to assure that all levels of a system meet the requirements of Controllability, Observability, and Accessibility. Controllability is the ability to externally control the functions of a unit to provide test stimuli, disable clocks or break-up chains and feedback loops. Observability is the ability to observe the functions of a unit through BIT/ETE provided by adequate test points and integrated diagnostics. Accessibility is the ability to access the unit's internal structure depending on mission requirements and limited test point placement.

1.2 What is Design for Testability (DFT)?

DFT is a design process intended to achieve a high level of testability by incorporation, early in the design phase, of the following circuit/module/equipment/system characteristics:

- Initialization - The ability to initialize a system with external stimuli to the operating characteristics of the system. For digital systems, this includes being able to disable internal clocks.

- Controllability - The ability to control the functions of the system with external test stimuli, including clocks, and the ability to break up chains and feedback loops.

- Observability - The ability to observe the functions of the system through adequate test points (0-100%) using integrated diagnostics, (i.e., BIT/ETE/ATE/Manual test/etc.)

- Accessibility - The ability to have 0-100% access to the unit's internal part structures and partitions, depending on mission requirements and limited test point placement.

The means by which DFT is implemented will require the ability to analyze the above characteristics for a given system to identify where improvements are necessary to provide adequate initialization, controllability, observability and accessibility. The analysis can take several forms depending on the type of system and the testability requirements. There are several tools and methods available to the analyst that will provide the necessary information needed to implement DFT principles. This CRTA will identify and describe the most commonly used tools and will attempt to give some guidance on how they can be used alone or together, as in many instances, one tool or method may not sufficiently address all requirements.

1.3 Design for Testability Objectives

As one may have gathered from the definition of DFT, the goals and objectives of any DFT program are to minimize the costs associated with testing for equipment malfunctions while maximizing system Ao. More specifically, these objectives are met by using DFT techniques to help determine where functional test and condition monitoring are needed to assure Ao requirements, and what strategies (i.e., best mix of BIT/ETE/ATE etc. and optimum test performance sequence) are needed to maximize malfunction detection and isolation and decrease test times. In meeting DFT objectives, the benefits of lower Test Program Set (TPS) development costs and lower system life cycle support costs will more than outweigh the cost of implementation.

1.4 Testability Requirements

One of the keys to understanding DFT is to understand the basic requirements of testability. For DFT to be successful and most cost effective, it must be implemented at the earliest design stages. Early implementation will guarantee that adequate

testability is an inherent part of the hardware design. Late incorporation of DFT usually generates extra costs and is much less effective.

Program management must provide for active representation of testability concerns in all program life cycle phases. This means that testability goals are established and monitored and that a testability program plan is developed and adhered to. Part of the program plan should be to evaluate the testability posture at the end of each development phase, before entering the next acquisition phase. This requires that, testability be tracked and demonstrated such that problems can be identified and corrected in a timely and cost effective manner similar to other assurance disciplines

Testability and DFT techniques should be applied at all hardware indenture levels and at all maintenance levels whenever possible or practical. To decrease test costs in production phases, testability should be considered in a bottom up approach. The bottom up approach will help to facilitate a top down look at testing and testability that is required for operation and maintenance. The various testability tools described herein can be implemented to facilitate a top down, bottom up or combined approach to testability analysis. It is important to remember that applying DFT at all levels of hardware indenture and maintenance will go a long way in maximizing system Availability while minimizing test resource consumption.

1.5 Effective Testability Design Considerations

While the goals, objectives, and requirements of testability and a DFT program have been introduced, the path that one must take to achieve DFT goals, objectives, and requirements has not. For any DFT effort to be successful, certain characteristics of system design must be considered and, if necessary, modified to meet FD/FI requirements. Below is a list of testability design considerations that must be addressed under any DFT program. Keep in mind that some of the listed characteristics may be specific to a particular system technology.

- Provide for initialization of sequential circuits
- Control oscillator and clock circuits
- Minimize the number of fan-in and fan-out situations
- Minimize ambiguity group sizes

- Design a high % of accessible input and output nodes
- Limit the number of feedback loops
- Eliminate digital race problems
- Generate accurate documentation
- Eliminate excessive or redundant tests
- Eliminate undetectable failures to meet FD requirements

To properly affect the inherent testability of a design, each of the above characteristics needs to be addressed. The available testability tools and techniques that are discussed in this CRTA will provide the means to achieve these objectives.

1.6 Benefits of DFT and Testability Analysis

It is generally accepted that the testability characteristics of a system are the direct result of the design of that system. Providing desirable supportable features that yield acceptable operational readiness and reduced operating and support costs can only result when sound engineering design principles are applied.

Although testability analyses are called for in some system procurements, there is currently no common standard, or handbook, that completely defines the methodology or tools to be used. MIL-STD-2165, "Testability Program for Electronic Systems and Equipment," is a good foundation, as a testability standard, but does not adequately address testability analysis techniques and their applications. This CRTA provides an overview of commonly accepted techniques and focuses on the most widely used methods.

When testability requirements are not addressed during the conceptual phase of system development, or are postponed until after the advanced development phase, the results are poor operational readiness, long maintenance times and high support costs. The maintainability benefits that can be derived by incorporating testability analysis in the system development are:

- A system design that fits the established maintenance concept
- Effective fault detection through the proper allocation of potential test points to BIT, ETE, and manual test

- Efficient test strategy to fault isolate down to the replaceable unit, at each maintenance level
- Manageable ambiguity group sizes at all maintenance levels
- Feedback loop identification at each maintenance level
- Reduced time and cost for acceptance testing and fault isolation
- Decreased RTOK's (Retest OKs), CND's (Cannot Duplicates) and BCS's (Bench Check Serviceables)
- Lower cost and more precise test program sets (TPS's)
- More exact ATE/ETE specifications
- Reduced Life Cycle Cost (LCC)

1.7 MIL-STD-2165, "Testability Program for Electronic Systems and Equipment"

MIL-STD-2165 is a tri-service approved document used by all branches of the military in the specification and acquisition of quality-assured electronic systems and equipment. The current version is the initial release dated January 26, 1985. The preparing activity is:

Department of Navy
Space and Naval Warfare Systems Command
Attn: SPAWAR 003-121
Washington, DC 20363-5100

MIL-STD-2165 is composed of seven testability related "tasks" contained in its nineteen pages. There are also three supporting appendices: Appendix A, "Testability Program Application Guidance," Appendix B, "Inherent Testability Assessment," and Appendix C, "Glossary of Terms." The three appendices contain an additional fifty-five pages. It defines methodology for the incorporation of

adequate and cost-effective testability and BIT features into the equipment design. It sets the requirements and establishes guidelines for assessing the extent to which a system or a unit supports fault detection and fault isolation. Three different types of tasks are addressed: 1) program monitoring and control tasks, 2) design and analysis tasks and 3) test and evaluation tasks. These three types of tasks may be defined as follows:

1) Program monitoring and control tasks focus on providing the information essential to the acquisition, operation and support management of the system/equipment. They relate more to the management responsibilities dealing with the program and less to the technical details.

2) Design and analysis tasks focus on the establishment of specific requirements, design practices, the prediction and analysis of testability parameters and other related engineering tasks.

3) Test and evaluation tasks are those that determine compliance with specified requirements and assess the validity of the previously made predictions.

The following is a listing of the tasks contained in MIL-STD-2165:

Task 101: Testability Program Planning
Task 102: Testability Reviews
Task 103: Testability Data Collection and Analysis Planning
Task 201: Testability Requirements
Task 202: Testability Preliminary Design and Analysis
Task 203: Testability Detail Design and Analysis
Task 301: Testability Inputs to Maintainability Demonstration

2.0 TESTABILITY DESIGN AND ANALYSIS TECHNIQUES

Many testability design and analysis techniques have been available for quite some time. For instance, while a failure mode effects analysis (FMEA) is primarily considered a reliability design technique, it is also one of the primary means to identify which system or component failure modes require detection and where such failure modes can be detected. This information is paramount to the design of Built-In-Test (BIT). While an FMEA is probably one of the oldest techniques, there are others, such as the D-algorithm used for automatic test generation, that have been in existence for nearly 30 years. It is only recently, within the last 15 years, that testability analysis techniques, and tools based on those techniques, have emerged. Wide use of testability analysis tools has not been prevalent until the last 5 years. Testability techniques and tools are now widely accepted and have matured to the point where they have been applied to help meet testability requirements. Much of what has been developed was done so to address testability problems in the digital electronics area. As a result, many of the tools available today are applicable primarily to digital electronic technology at the component or circuit card level.

2.1 Basic Techniques

There are presently three basic techniques for which testability design and analysis tools are available.

- Controllability/Observability (C/O)
- Heuristic scoring
- Dependency Modeling

While there are definitely more techniques than the three listed, nearly all of the available tools are based on one or more of these three. Information on other techniques can be found in references [1] and [2].

Of the three techniques listed above, two of them address primarily digital systems. Only dependency modeling can be effectively applied to other system types such as analog, mechanical, electro-mechanical and fluid or process control systems. Dependency modeling does, however, have other limitations as will be explained.

The three basic techniques can be used to develop one or more testability metric of the system being analyzed. These metrics range from a single number, or figure of merit (FOM), that indicates the ease of item test, to other statistical measures such as fault coverage and percent of faults isolatable to a specific ambiguity group size. More detail on specific testability measures provided by each technique can be found in the individual technique descriptions.

The key to using analysis techniques that provide a single FOM is the quality of the measure obtained from the analysis. However, a single measure, while giving an indication of the overall ease or difficulty of test, does not provide a good indication of the testability of the individual nodes or even specific signal paths. Thus, if the testability analyst uses proper judgement and some caution in the interpretation, a single FOM can provide useful information relating to the testability of an item. One must keep in mind that in nearly all cases, each technique provides more than just a single measure. Areas where testability needs to be improved are indicated differently by all of the techniques.

2.1.1 Controllability and Observability (C/O) Techniques

2.1.1.1 Sandia Controllability Observability Analysis Program (SCOAP)

Much of the early work in testability analysis centered on efforts to deterministically estimate the difficulty of justifying a specific logic value on a node and propagating this logic value to an output where it can be identified. The terms controllability and observability were borrowed from control theory to denote these quantities. The most widely known testability analysis tool of this type is probably SCOAP (Sandia Controllability Observability Analysis Program), which is based on the pioneering work of Lawrence Goldstein at Sandia National Laboratories. While SCOAP is a testability analysis tool, many other tools are based on the SCOAP principle making SCOAP a basic testability technique itself. SCOAP attempts to relate the C/O measures to the minimum number of node assignments necessary to control and observe that node.

The SCOAP algorithm is based on developing six functions to characterize the C/O properties of the internal nodes of a digital circuit. The measures are based on circuit topology alone, and do not consider the particular sequences of input and

state vectors. The types of circuits analyzed are composed of standard combinational and sequential cells that would be available in a standard cell library. The basic elements of the library would include AND gates, OR gates, inverters, buffers, flip-flops, and more complex cells that are combinations of the basic elements.

2.1.1.1.1 Definitions

The C/O functions to be developed are divided into combinational functions and sequential functions. These can each be further divided into combinational and sequential 0 and 1 controllabilities of a node N ($CC^0(N)$, $CC^1(N)$, $SC^0(N)$, $SC^1(N)$) and combinational and sequential observabilities of N (CO(N), SO(N)).

$CC^0(N)$ and $CC^1(N)$ are related to the minimum number of combinational node assignments in a circuit required to justify a 0 or a 1 on node N, where a node is defined here as either a primary input or output of a standard combinational cell. CO(N) is related to the number of standard combinational cells between node N and a primary output and the minimum number of combinational node assignments required to propagate a logical value on N to a primary output.

$SC^0(N)$ and $SC^1(N)$ are related to the minimum number of sequential nodes that must be set to specified logical values to justify 0 or 1 on node N. $SC^0(N)$ and $SC^1(N)$ represent an upper bound measure of the number of time frames required to control nodes that are deeply buried in a digital network from the primary outputs. SO(N), like CO(N), is related to the number of standard sequential cells between N and a primary output and the number of cells that must be controlled to propagate a logical value of N to an output.

2.1.1.1.2 Quantitative Definitions

2.1.1.1.2.1 Primary Inputs and Outputs

If I is a primary input node of a digital circuit, then the controllabilities of node I are defined as follows:

$$CC^0(I) = 1$$
$$CC^1(I) = 1$$

$SC^0(I) = 0$
$SC^1(I) = 0$

where $SC^0(I)$ and $SC^1(I)$ are 0 since it is not necessary to control any sequential nodes in the justification of a primary input.

If U is a primary output node of a digital circuit, then:

$CO(U) = 0$
$SO(U) = 0$

since a primary output can be observed without any need to effect the information in a sequential or combinational circuit.

2.1.1.1.2.2 Standard Cells

To compute the controllability of a standard cell output node, a number equal to the sum of the controllabilities associated with each of the input assignments that accomplish the desired output node justification is computed. The minimum of these numbers incremented by cell depth, is defined to be the output node controllability, where cell depth is the combinational or sequential depth of the cell. For this algorithm, combinational depth of a combinational cell is 1, and 0 for a sequential cell; sequential depth of a combinational cell is 0, and 1 for a sequential cell.

To compute the observability of a standard cell input node, the observability of the easiest to observe sensitized output (where sensitized refers to all of the cell input assignments that sensitize one or more cell outputs to changes in the specified input) plus the sum of the controllabilities of the minimum cost sensitizing input assignment plus cell depth is calculated.

Consider as an example a 3-input NAND combinational cell with output Y and inputs X_1, X_2, and X_3. In order to assign Y to 1, any of three combinations is required: $X_1 = 0$, $X_2 = d$, $X_3 = d$; $X_1 = d$, $X_2 = 0$, $X_3 = d$; or $X_1 = d$, $X_2 = d$, $X_3 = 0$; where d = don't care. Therefore,

$$CC^1(Y) = \min [CC^0(X_1), CC^0(X_2), CC^0(X_3)] + 1$$
$$SC^1(Y) = \min [SC^0(X_1), SC^0(X_2), SC^0(X_3)]$$

where the combinational depth of the NAND gate equals 1 and its sequential depth 0. The output Y can be set to 0 only by setting all three inputs to 1. Therefore:

$$CC^0(Y) = CC^1(X_1) + CC^1(X_2) + CC^1(X_3) + 1$$
$$SC^0(Y) = SC^1(X_1) + SC^1(X_2) + SC^1(X_3)$$

To observe any one of the inputs (X_i) requires observing output Y while the other two inputs are maintained at logical 1. This makes the observability equations for this example as follows:

$$CO(X_i) = CO(Y) + CC^1(X_j) + CC^1(X_k) + 1$$
$$SO(X_i) = SO(Y) + SC^1(X_j) + SC^1(X_k)$$

where i, j, k are elements of the set {1, 2, 3}

If the inputs to the 3-input NAND gate were primary inputs, and Y a primary output, the previous equations would provide the following values:

$CC^1(Y) = 2$
$CC^0(Y) = 4$
$SC^1(Y) = 0$
$SC^0(Y) = 0$

$CO(X_i) = 3$
$SC(X_i) = 0$

where the lower values indicate better controllability and observability.

For a second example, consider the C1490, a resettable negative-edge-triggered *D*-flip-flop sequential standard cell. In order to set the output *Q* of a C1490 to 1, it is necessary to set the *D* input to 1, hold the reset line *R* at 0 and generate a falling edge on the clock line, *C*. Therefore, the 1 controllability equations for *Q* can be written:

$$CC^1(Q)=CC^1(D)+CC^1(C)+CC^0(C)+CC^0(R)$$

$$SC^1(Q)=SC^1(D)+SC^1(C)+SC^0(C)+SC^0(R)+1$$

Notice that the difficulty of generating a falling edge on the clock line is represented by $CC^1(C)+CC^0(C)$, since it is necessary first to set the clock line to 1, then force it to 0.

There are two distinct mechanisms for setting *Q* to 0. Either the reset line can be used while maintaining the clock line at a logical 0, or a 0 value can be clocked into the flip-flop from the *D*-input line. Consequently, the controllability equations for *Q* can be written:

$$CC^0(Q)=\min [\ CC^1(R)+CC^0(C),\ CC^0(D)+CC^1(C)+CC^0(C)+CC^0(R)\ ]$$

$$SC^0(Q)=\min [\ SC^1(R)+SC^0(C),\ SC^0(D)+SC^1(C)+SC^0(C)+SC^0(R)\ ]+1$$

The *D*-input line value can be observed at the *Q* output of the flip-flop by generating a falling edge on the clock line while holding the reset line low.

$$CO(D)=CO(Q)+CC^1(C)+CC^0(C)+CC^0(R)$$

and

$$SO(D)=SO(Q)+SC^1(C)+SC^0(C)+SC^0(R)+1$$

The reset line *R* can be observed at *Q* by setting the flip-flop to a logical 1 and then using the reset line to force it to a logical 0.

$$CO(R)=CO(Q)+CC^1(Q)+CC^0(C)+CC^1(R)$$

and

$$SO(R)=SO(Q)+SC^1(Q)+SC^0(C)+SC^1(R)+1$$

Finally, the clock line can be indirectly observed at the flip-flop output by either setting the flip-flop to 1 and clocking in a 0 or resetting the flip-flop to 0 and clocking in a 1.

$$CO(C)=\min [\ CO(Q)+CC^0(R)+CC^1(C) + CC^0(C)+CC^0(D)+CC^1(Q),$$
$$CO(Q)+CC^0(R)+CC^1(C) + CC^0(C)+CC^1(D)+CC^0(Q)\ ]$$

and

$$SO(C)=1+ \min [\ SO(Q)+SC^0(R)+SC^1(C) + SC^0(C)+SC^0(D)+SC^1(Q),$$
$$SO(Q)+SC^0(R)+SC^1(C) + SC^0(C)+SC^1(D)+SC^0(Q)\ ]$$

Where once again if the flip-flop inputs and outputs were primary:

$CC^1(Q)=4$
$CC^0(Q)=2$
$SC^1(Q)=SC^0(C)=1$
$CO(D)=CO(R)=3$
$SO(D)=SO(R)=1$
$CO(C)=6$
$SO(C)=2$

2.1.1.1.3 Implementation of the Algorithm for a Circuit

The above examples were simplified by considering each element as a stand-alone circuit where each input and output was primary. To implement this methodology for a complete circuit, a generalized description is presented here.

Calculate circuit node controllabilities.
Initializations: For all primary input nodes *I*, set

$$CC^0(I)=CC^1(I)=1$$

$$SC^0(I)=SC^1(I)=0.$$

For all other nodes *N*, set

$$CC^0(N)=CC^1(N)=\infty$$

$SC^0(N)=SC^1(N)=\infty$.

Working from primary inputs to circuit outputs, use standard cell controllability equations to map cell input node controllabilities into cell output node controllabilities.

Iterate on the above step until the controllability numbers stabilize (to handle feedback loops external to standard cells, etc.).

Since this is an integer algorithm, and the controllability numbers are monotonically nonincreasing from iteration to iteration, there is always a guarantee that the algorithm converges. Practically, only two or three iterations are usually necessary for the controllability numbers to stabilize.

Calculate circuit node observabilities.
Initializations: For all primary output nodes *U*, set

$CO(U)=0$
$SO(U)=0$

For all other nodes *N*, set

$CO(N)=SO(N)=\infty$.

Working from primary outputs to circuit inputs, use standard cell observability equations together with the previously computed node controllabilities to map cell output node observabilities into cell input node observabilities. Note that the observability of a fanout point is by definition, equal to the minimum observability of the nodes to which it fans out.

Iterate on the above steps until the observability numbers stabilize.

If after application of the above algorithm to a given digital circuit, there remains a node *N* with an infinite *e*-controllability number, $e \in \{0,1\}$, then that node is *e*-uncontrollable. $CC^e=\infty$ or $SC^e(N)=\infty$ is a sufficient but not necessary condition for the *e* uncontrollability of *N*. Similarly, $CO(N)=\infty$ or $SO(N)=\infty$ is a sufficient but not

necessary condition for the unobservability of node *N*. This limitation in testability results from the existence in the circuit of nodes which are not properly connected to either primary inputs or outputs.

The above algorithm was initially implemented on a DEC-10 computer system with typical initial run-times on the order of .75 minutes for 30 cell circuits and 3.5 minutes for 200 cell circuits. Since the source code for the program, SCOAP, was developed by the Department of Energy (DOE), it has been acquired and used by several companies both internally and in other available testability analysis tools.

2.1.2 Heuristic Scoring Technique

2.1.2.1 Design Guide Checklist

In 1979, under contract to Rome Air Development Center (RADC), Grumman Aerospace Corp. developed "An Objective Printed Circuit Board (PCB) Testability Design Guide and Rating System" (reference [3]). The design guide and rating system was one of the earliest available methods of testability analysis for digital electronic systems. Like SCOAP, the Grumman method is both a tool and a technique, that technique being a combination design guide checklist and heuristic scoring method. Several companies utilize this technique and the MIL-STD-2165, Appendix B, checklist is based on it.

The Grumman design guide checklist technique is divided into three areas:

1. A PCB testability design guide that presents examples of testability corrective methods and techniques that are used to eliminate PCB test deficiencies.

2. A checklist of system/management factors that are applicable to a group of PCBs or a system, and may be related to specific ATE.

3. A PCB testability evaluation system that develops a Figure-of-Merit (FOM) and identifies areas where design corrections are needed.

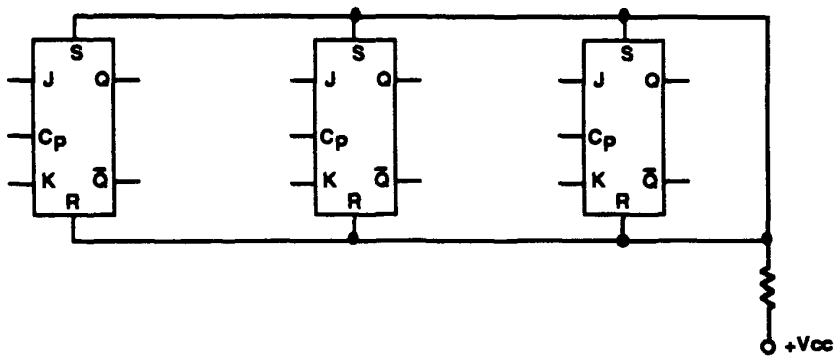
The testability design guide of the checklist technique provides information on the dos and don'ts for digital PCB testability. The areas covered in the design guide are:

- Proper initialization of sequential circuits
- Breaking up high ambiguity groups
  - Breaking up common reset lines
  - Use of common integrated circuit packages for related/ redundant gate logic
  - Breaking up high fan-in/fan-out logic
- Clock line and oscillator problems
  - Provide proper access to continuously running oscillators, clocks, or pulse generators
- Handling of feedback loops
- Resolving "buried logic" clusters and "bottlenecks"
- Testing counters
  - Modify circuit to gain access to buried counters
- Testability documentation requirements
  - Assigning proper logic symbols
  - Cross referencing of drawings
  - Non-standard parts
  - I/O pin designations
  - Proper page connections

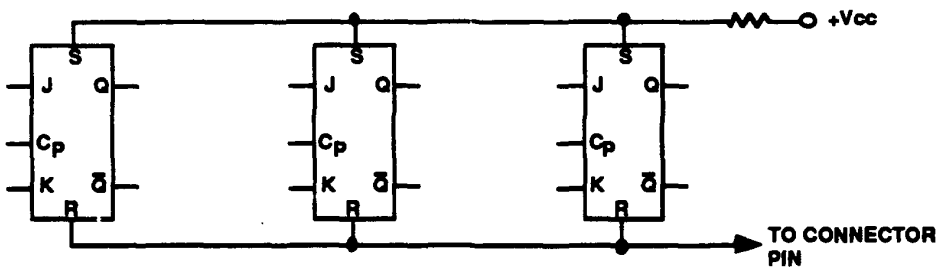
- Application of power loads
  - Supply voltage sequencing
  - Uniform power pins
- Miscellaneous
  - Clock race problems
  - Avoidance of monostable multivibrators
  - Use of high frequencies
  - Use of potentiometers
  - Test point isolation
  - Orientation of integrated circuit packages
  - Testing of microprocessors, memories, and other complex components

For each item covered, there are detailed explanations of why designing one way is better than another from an ease of test viewpoint. In many cases, figures are used to help in the explanation. Some of the figures used are reprinted on the following pages.

The design in Circuit A denies the test engineer the use of an alternate reset approach for the JK flip/flop. By returning the R inputs to an external pin in Circuit A-1, the stages can be reset while the Cp fault is being simulated. This allows detection and isolation of the simulated fault.



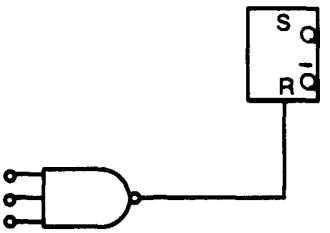
Circuit A: Poor Design of Flip/Flop Reset Lines



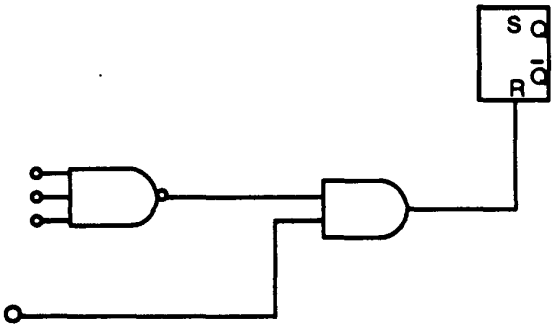
Circuit A-1: Good Testability Reset Design for Flip/Flop

Figure 2-1: Testability Practices for Flip/Flop Reset Lines

For cases where flip/flops are reset from an uncontrolled internal circuit point such as shown in Circuit B, the logic should be redesigned to permit a state change from the primary input to reset the flip/flop.



Circuit B: Uncontrolled Internal Flip/Flop Reset Line

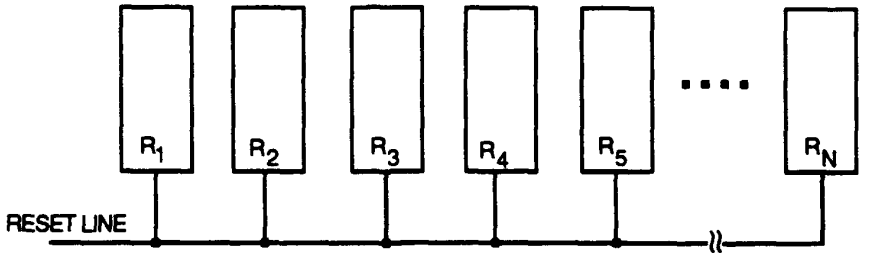


Circuit B-1: Logic for Testable Flip/Flop Reset Line

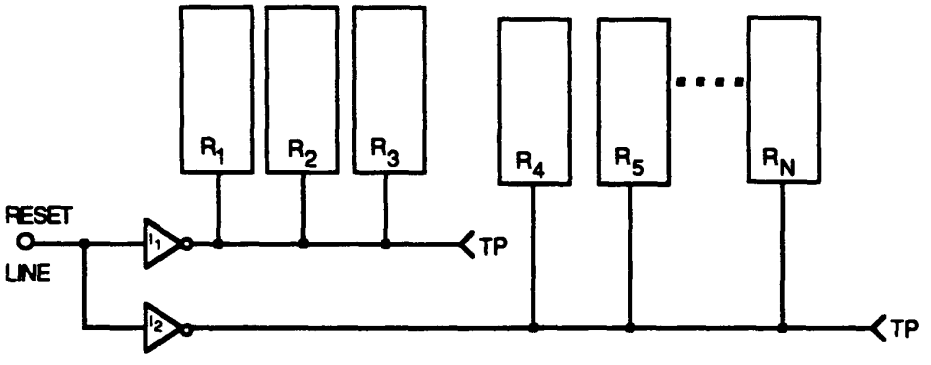
Figure 2-2: Additional Consideration for Flip/Flop Resets

When a reset can be accomplished using only the "R" input, there is a natural tendency to tie the one reset line to all flip/flop resets (Circuit C).

This design practice presents a high ambiguity problem to the test engineer. Reset lines of this type should be broken into groups, with the reset line buffered by logic into each group (Circuit C-1).



Circuit C: High Ambiguity Reset Line



Circuit C-1: Design for Testability Break Up High Ambiguity Reset Line

Figure 2-3: Testability Practices for Ambiguity Group Resolution

Whenever possible, groups of combinational gates should be from the same IC package as demonstrated below. This holds true for the situation presented in Figure 2-3, where stages R1 and R2 (shown in Circuit C-1), or other pairs connected to the same reset branch, should be from the same IC package to further reduce ambiguity.

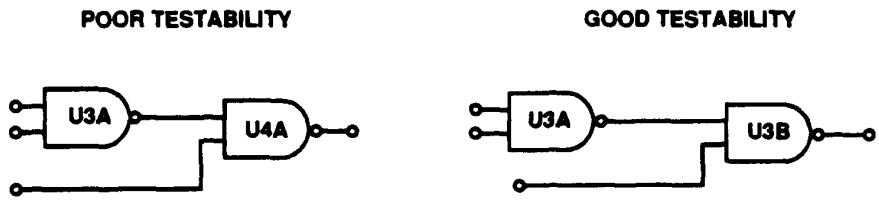
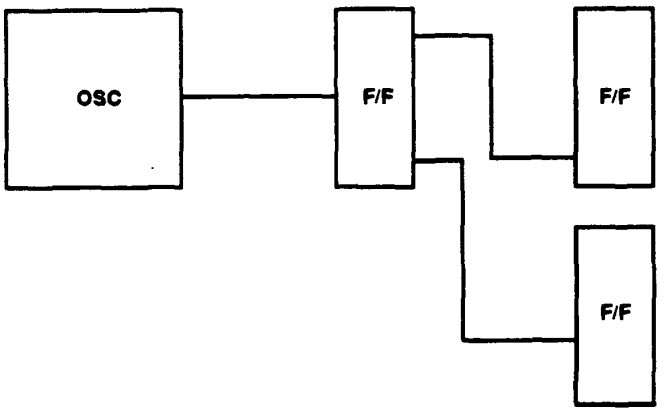
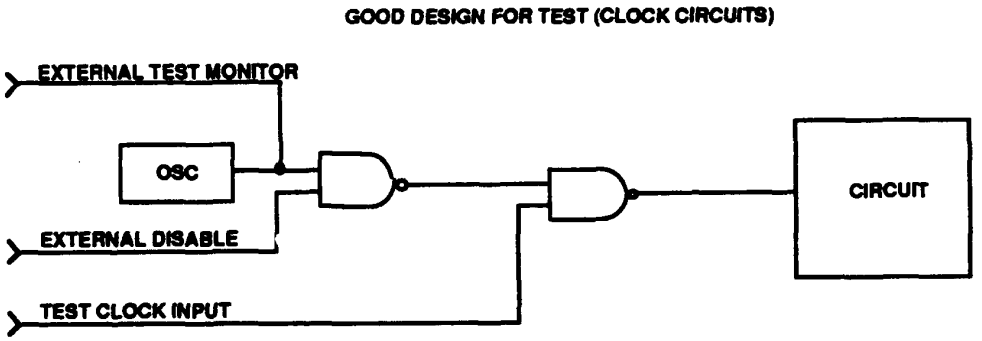


Figure 2-4: Packaging Solutions to Ambiguity Resolution

Circuits that contain continuously running oscillators, clocks, or pulse generators without access to external PCB inputs or outputs present an unacceptable design for test (Circuit D). This design practice makes it difficult to synchronize the ATE with the UUT. There are several alternative design for testability techniques that can overcome this difficulty. One approach is to bring the oscillator output directly to a primary output pin. This will permit a direct check of whether the oscillator is functioning. Another approach is to add gates between the clock and its destination. This will allow the ATE to disable the clock and supply its own test clock (Circuit D-1). An alternative would be to use a socket for the oscillator so it can be removed during test, and an alternate signal supplied from the ATE.



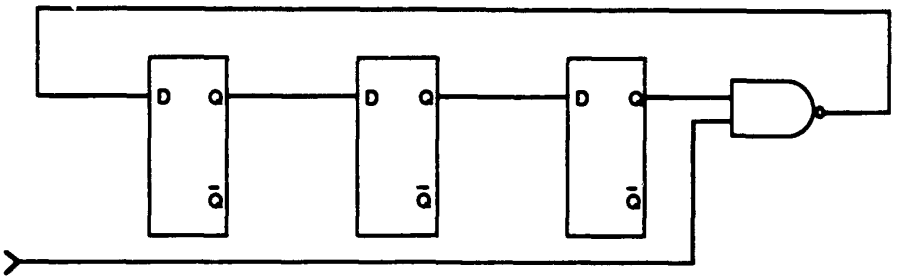
Circuit D: Unacceptable Design



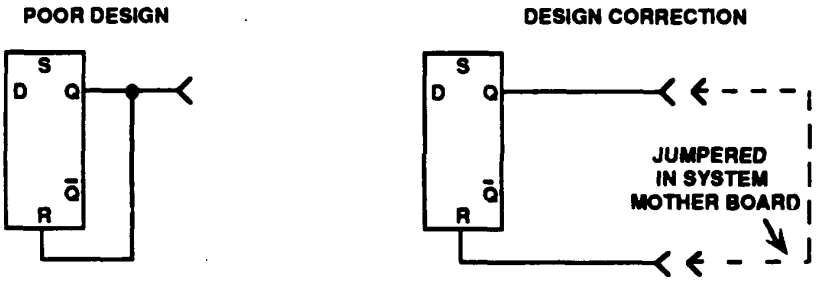
Circuit D-1: Design for Testability Oscillator Circuit

Figure 2-5: Testability Design for Clock Lines & Oscillators

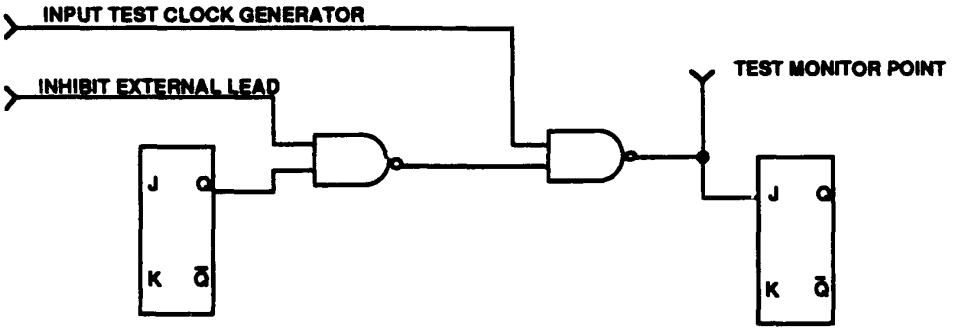
Feedback loops present a difficult problem to the test engineer. If feedback loops are unavoidable, testability design enhancements, such as shown in Circuits E and E-1, should be added. There are other instances where the logic circuits of a PCB become "buried" when several sequential stages are interconnected with no access to primary inputs or outputs. Circuit E-2 is an example of how to deal with breaking up buried sequential logic and improve testability.



Circuit E: Externally Controlled Gate Breaks Feedback Loop



Circuit E-1: Feedback Loop Broken for PCB Test - Connected in System Interconnected Harness



Circuit E-2: Logic to Break Sequential Feedback Loop

Figure 2-6: Testability Design for Feedback Loops

One of the keys to being able to perform accurate testability analysis using the tools described in this document is that of good documentation. Figure 2-7 presents several examples of preferred and unacceptable means of documentation.

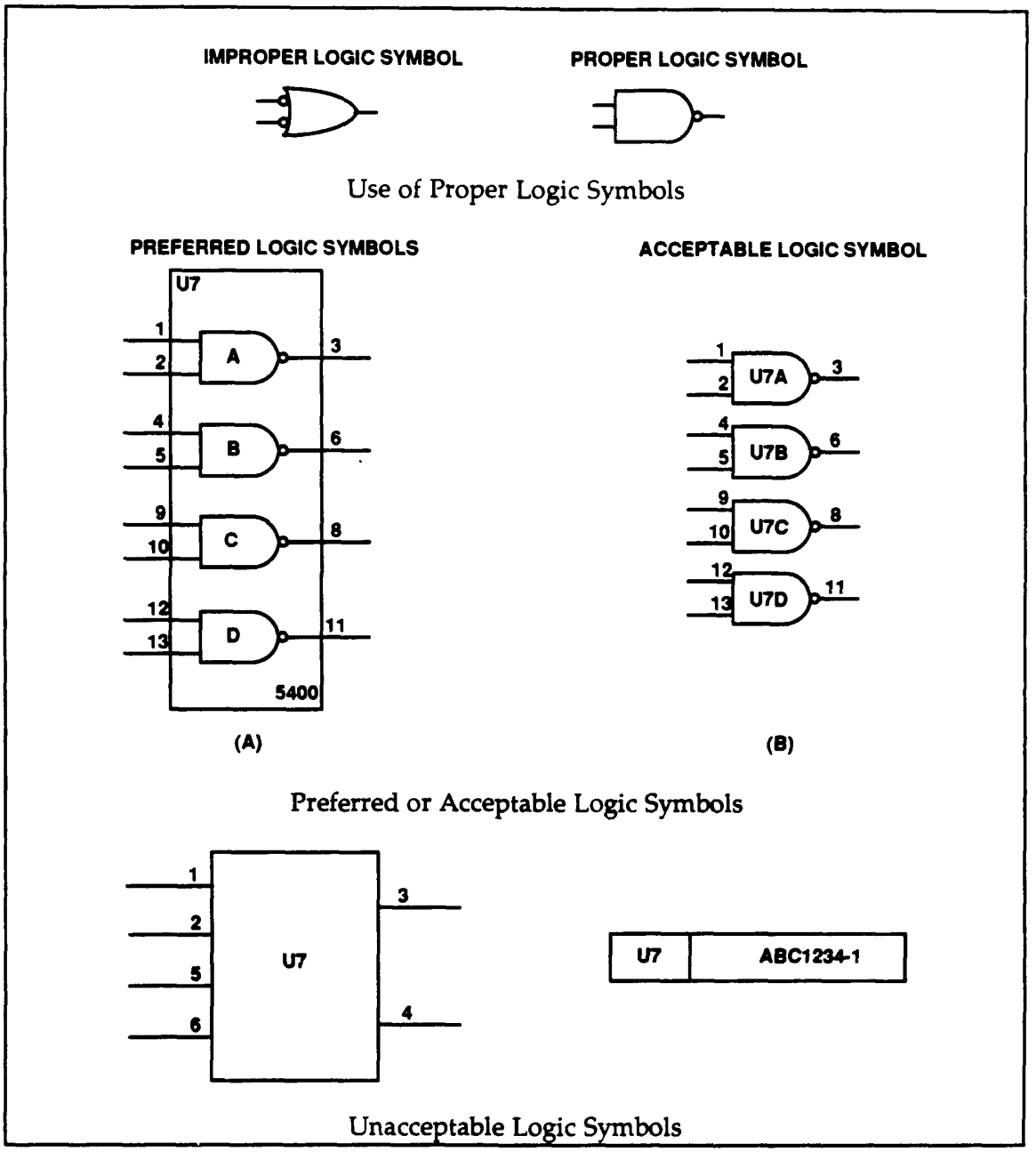


Figure 2-7: Examples of Good and Bad Documentation for Testability

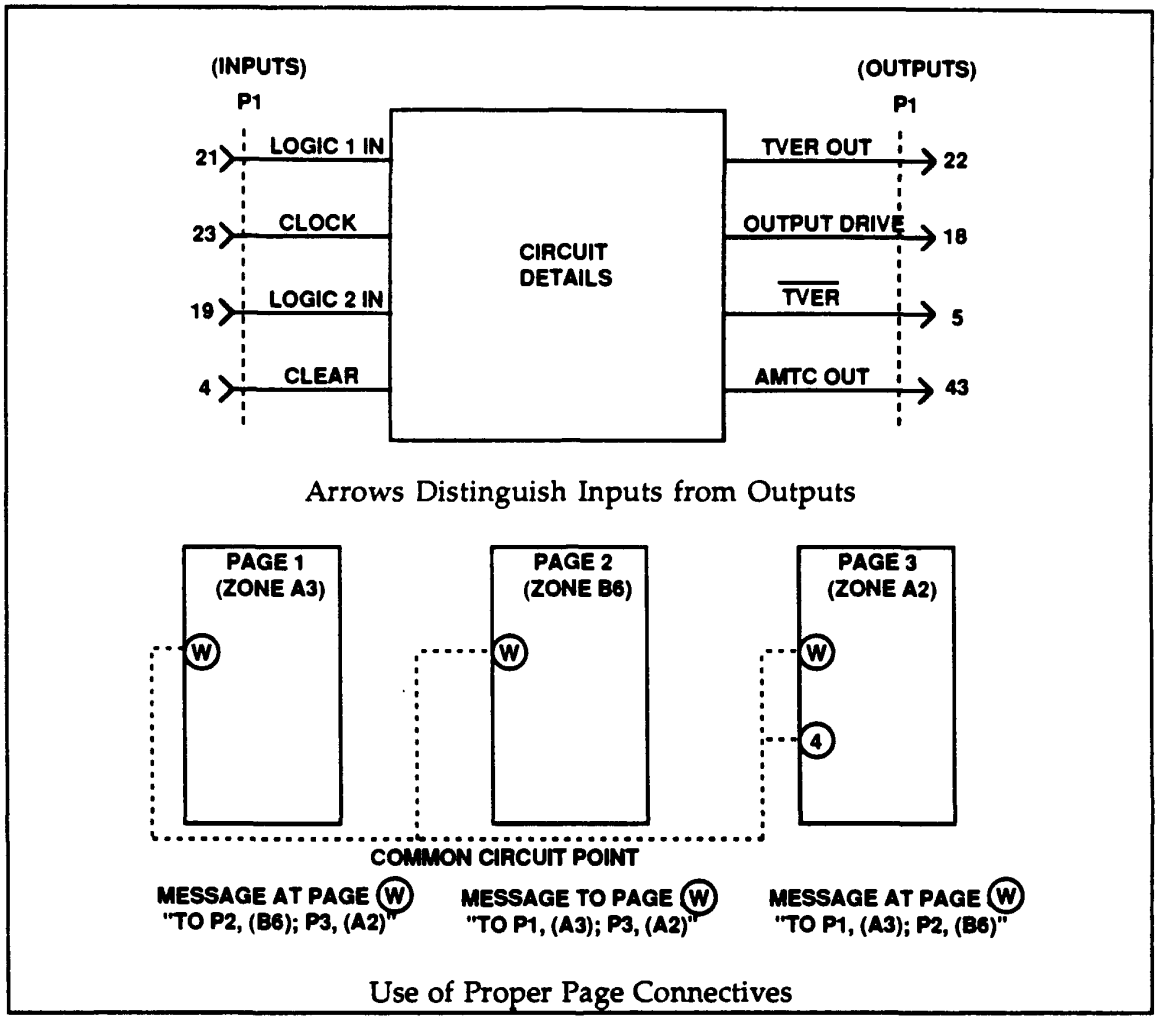


Figure 2-7: Examples of Good and Bad Documentation for Testability (CONT'D)

2.1.2.2 System/Management Factors

This part of the Grumman guide/checklist technique provides a checklist for system level considerations, where the system comprises several PCB's. Note that while there is a rating system on the PCB level (see next subsection), Grumman felt it impractical to develop something similar at the system level due to the numerous variations in systems designs. The checklist presented in this part of the overall guide is more qualitative than the previous section on PCB design practices in that

specific examples, with figures, are not presented. Specifically, the system level checklist covers four areas that are outlined below:

- System Interface Factors Checklist

  - Limit the Number of Different Part Types Used
  - Limit Types of Logic Families
  - Fail Safe Design - UUT I/O Lines
  - System Clock - External Disable
  - Functional Packaging
  - Proper BIT Application
  - Feedback Loops Open for Test
  - Well Chosen Test Detect/Isolate Levels
  - No Reconvergent Fanout Between LRUs
  - Design for ATG Compatibility

- Management Factors Checklist

  - System Configuration Control
  - Use a Test System With Real Time Compiler
  - Use of Proper Test Diagrams
  - Proper System Labeling

- System Hardware Checklist

  - Use a Common PCB Connector
  - Use a Common Interface Device (ID) for the Maximum Number of PCBs

- System Power Checklist

  - Power Supply Sequencing
  - Common Pins for Power/Ground Leads
  - Standard Grounding Philosophy

An explanation for each checklist factor is presented in the guide report.

2.1.2.3 PCB Testability Evaluation System

To better explain the guide/checklist technique, refer to Appendix A which is an excerpt from RADC-TR-79-327 which documents this method. Note that this particular rating system, while being somewhat out-of-date for specific kinds of components, is still very useful. To address newer technologies, Raytheon Corporation, under contract to Rome Laboratory, is in the process of updating the design guide and rating system.

To obtain information on the update effort, contact Dr. Roy Stratton at Rome Laboratory, Griffiss AFB, New York. A copy of the Grumman Report may be ordered from the National Technical Information Service (NTIS) located in Philadelphia, PA. The report number is RADC-TR-79-327.

2.1.3 Nodal Dependency Technique

2.1.3.1 Dependency Modeling

A majority of the testability analysis tools that benefit fault isolation through test point placement and the identification of ambiguity groups can be classified as dependency modeling tools. That is, they perform their analyses with reference to the relationship of the inputs of an item (components, PWAs, SRUs, etc.), the item itself and the outputs of the designated item. The output then becomes the input to another item and in this manner the dependency relationships of the items are established through an algorithm to form a dependency model. Dependency modeling has its roots in the principle that all events (potential tests) within a design are either depended on, or dependent upon, some other event or set of events. Separating all events are modifiers (replaceable items). Within the boundary of a Unit Under Test (UUT), regardless of its indenture level (PWA, sub-assembly, assembly or system), there are three types of events. These are initial, intermediate, and terminal events. Initial events are those supplied to the UUT, and with which it performs its intended function. Intermediate events are those that are completely within the boundary of the UUT and occur as a result of the specific functional operations being performed by the UUT. Terminal events are the expected output of the UUT. With this basic knowledge, any electronic, mechanical, or hydraulic design can be analyzed. The depth of the analysis hinges on the

amount of design data available and the required isolation level for the item being analyzed. A fully detailed analysis requires that full disclosure of design detail be made available to the testability analyst.

When performing a dependency modeling analysis, using a dependency based automated tool, the testability design analyst will assign each event and replaceable item a unique identifier, such as a number or alphanumeric code. The analyst then has a means to identify each event and replaceable item in the resulting logical model of the particular unit being analyzed. In some tools, the pertinent design data can also be keyed to a unique event and replaceable item identifier. The analysis of each system unit is performed at one level below the required fault isolation level. This provides the dependency modeling tool with the necessary relational information required to produce the model for the desired level of fault isolation. Dependency modeling is a versatile methodology that is applicable to a wide variety of system types and structures. Most automated dependency based modeling tools provide the capability to manage the model databases so that iterations of the system can be quickly produced for comparative analyses.

2.1.3.2 Benefits and Capabilities Offered By Dependency Modeling

The dependency modeling technique, and those tools based on this technique, are most useful in determining where testing is required for fault-isolation. Because dependency modeling provides a topological connectivity map of the system being analyzed, algorithms have been written that use this information to identify the following kinds of fault-isolation related items for a given set of tests and/or test points:

- Identification of ambiguity groups and the items within
- Identification of feedback loops and the items within
- Fault-isolation percentage to an ambiguity group size of n (where n = 1, 2, 3, ...)
- Tests not required for fault-isolation
- Fault-isolation or diagnostic strategy tree; A go-no/go path showing test order required for efficient fault-isolation that, in most tools, can be weighted by failure rate, test cost, test time, etc.

The benefits of knowing the above kinds of information are as follows:

- Identification of re-packaging needs to reduce ambiguity groups
- Where more tests are required to meet fault-isolation requirements
- Where tests are not needed for fault-isolation resulting in a minimum number of tests that meet requirements
- Identification of feedback loops that can be eliminated or broken up via hardware and software techniques
- A test strategy that can be tailored to match real world test situations and maintenance requirements
- By having a computerized model, a simple means for making trade-off analyses before design change decisions are made.

While a testability analysis via dependency modeling techniques does not solve all testability problems, it does provide a road map that can be used in concert with other testability tools and techniques.

2.1.3.3 The Basics of Dependency Modeling

2.1.3.3.1 Partitioning the System

The first step when performing a testability analysis of a system, using the dependency modeling technique, is to determine the structure of the system using functional block diagrams, or upper level maintenance diagrams. These diagrams will provide the necessary information to be used in concert with the requirements acquired during preliminary discussions with the customer. The specified level of isolation will be the guiding requirement at this time. The general rule to be followed is to divide the system into manageable pieces along any physical breakpoints. These pieces may be Line Replaceable Units (LRUs) in a large system, or Shop Replaceable Units (SRUs) in smaller systems. The normal sequence for the breakdown of an equipment would be system, subsystem, assembly, subassembly, and component. However, it should be remembered that unique designations may be encountered for specialized equipments or systems of types or pu s other than electronics.

2.1.3.3.2 An Example - Building The Model

Figure 2-8 shows a simple system that will be used to demonstrate the basic principles of dependency modeling. The initial step in any dependency modeling analysis is to create a functional flow chart of the system, or item, to be analyzed. This can be, for example, a block diagram, such as the one depicted in Figure 2-8, a schematic, or a piping and instrumentation diagram (P&ID). Basically any diagram that relates the functional interconnections of the system may be used. A basic understanding of how the system functions is also required. Once the diagram is obtained, the first step is to label the direction of information flow in the system, and to label both replaceable items and potential test nodes. All of this has been done for the UUT shown in Figure 2-8. Once the labeling step is complete, the dependency model can then be developed. In dependency modeling, only tests have dependencies. Therefore, dependency statements are developed for each individually defined test. The dependency statements for the UUT of Figure 2-8 are shown in Table 2-1.

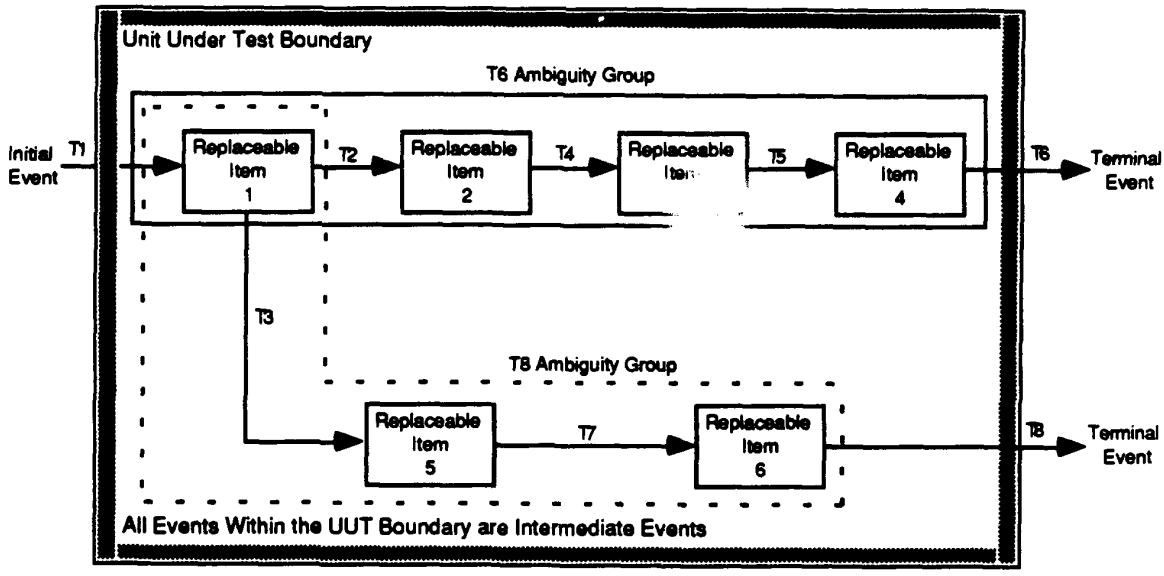


Figure 2-8: Example of Basic Dependency Modeling

Table 2-1: Dependency Statements for UUT of Figure 2-8

TEST	DEPENDENCY
T1	None
T2	RI1, T1
T3	RI1, T1
T4	RI2, T2
T5	RI3, T4
T6	RI4, T5
T7	RI5, T3
T8	RI6, T7

RI = Replaceable Item

Note that the dependency statements shown in Table 2-1 are considered first order dependencies. For most, if not all, of the dependency modeling tools, this is all that is required as initial input. You will note that the first order dependency of a test only considers the item or items that feed the test, and any test (or tests) that is a direct input to the item. Most algorithms automatically determine all "higher order" dependencies. Obviously, for the system depicted in Figure 2-8, one does not require a computer to determine the higher order dependencies. However, as systems become more complex, computer programs are absolutely necessary.

Before continuing, some points need to be addressed regarding model development and the simplicity of the Figure 2-8 UUT. The UUT in Figure 2-8 shows that each item has only one input and one output. Further, there are no feedback loops and all information flows in one direction. This is not to say that dependency modeling is applicable only to simple systems. On the contrary, dependency modeling can handle sophisticated situations very effectively. However, defining the dependencies correctly is the key. Consider, for example, the component shown in Figure 2-9, which is a data latch having twelve (12) inputs and eight (8) outputs. Note also that the component diagram has already been labeled for dependency modeling.

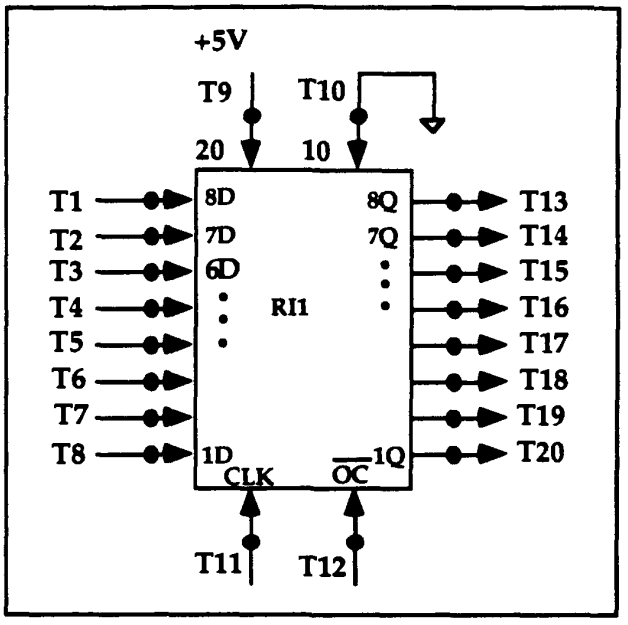


Figure 2-9: Data Latch

In order to write the dependency statements for each of the eight outputs of the latch (T13 - T20), some knowledge of which inputs effect which outputs, or, in other words, which outputs depend upon which inputs, must be known to the testability analyst. This means that information on the schematic for the latch must be consulted. Otherwise the dependency statement for each output test would have to include all inputs, creating large ambiguity groups that aren't really there. This further illustrates that the dependency modeling analysis takes place at one level below the level that is being modeled. Note that there are times when the lower level information may not be available. In these cases, one usually has to create a worst case model where all inputs feed all outputs. This, however, should be a last resort and avoided at all cost.

2.1.3.3.3 Using the Model Information

Some of the types of information that can be derived using dependency model information are listed in subsection 2.1.3.2 - Benefits and Capabilities. One of the more unique features of dependency modeling tools, is the capability to automatically provide fault isolation trees, that show a streamlined test order and

identify, based on test results, the failed replaceable item or items. Referring once again to Figure 2-8 will point out how this can be done.

To review, Figure 2-8 shows a UUT consisting of 6 replaceable items and 8 potential tests. This example portrays dependency modeling in a most simplistic manner to convey the basic tenents that apply to the technique. The first fact that can be seen in the example is that, both terminal events will be affected by the single initial event. The second recognizable fact is that, each terminal event will be affected by a different set of replaceable items. These sets of replaceable items are called an ambiguity group. Performing a test at the beginning and at the end of a set, (where a set is an individual string of items between UUT input and output), may not provide enough information to determine which item in the set is faulty. (Note, however, for this particular example, you may be able to isolate to replaceable item 1 by only testing at the input and outputs of the UUT.) The size of the ambiguity group can be reduced if the potential tests available at the intermediate events can be performed. It should also be noted that, if the reliability of the individual replaceable item is taken into account, certain potential tests within the group might be more likely to isolate the fault sooner than the others.

If the goal of the testability assessment is to reduce the size of the ambiguity groups in a UUT, most dependency modeling tools will provide the necessary insight, so that the analyst can recommend which of the potential tests should be made available. The manner in which the tests will be accessed will involve the participation of the design engineer, test engineer and the testability analyst.

Fault isolation is easily addressed by most automated dependency modeling tools. The basic procedure of fault isolation is to alternately test the inputs and outputs of a UUT that has been identified as functioning incorrectly. If all factors were considered to be equal, a logical scheme to follow when fault isolating to a defective item, among a set of items, would be the classic divide and conquer using the split half theory. If the output of a set is bad and the input is good a logical next step would be to perform a test in the center of the set. This is a very basic fault isolation strategy, but it will work. A split half test strategy for a failure at T6, in Figure 2-8 would be: perform T1, go to T4, if T4 bad - test T2, if T4 good - test T5. However, in real world situations, all factors are not equal and this can be compensated for when producing a test strategy using todays dependency modeling testability tools. The

sequence for testing the UUT can also be influenced by the involvement of a specific replaceable item in the various possible failures that can occur. This is illustrated in Figure 2-8 by the fact that replaceable item 1 is in the ambiguity group for both outputs. If replaceable item 1 fails, the failure would propagate to both outputs.

Even based on single failure assumptions these could be several test sequences for isolating replaceable item 1 (RI1). Keeping in mind that Figure 2-8 is a simple system, the problem of test sequence for efficient fault isolation multiplies as more parallel paths, fan-outs, fan-ins, feedback loops, etc. are part of the system being modeled. Having a dependency model to work from allows most dependency modeling tools to choose the best path for any given set of factors, automatically. Referring back to isolating RI1 in Figure 2-8, and given that T6 is bad, the tools would most likely choose T1 next, and if T1 was good, then go to T8. If T8 is bad, RI1 is isolated as the common element to T6 and T8 (based on the single failure assumption). It is easy to see how someone else may choose to perform T1, then T2 & T3, which is one more step than an automated tool might choose. Some tools do, to some extent, factor in the possibility of multiple failures, which further complicates the ability to choose a test path using manual methods.

Fault detection can also be addressed through dependency modeling. If the model of the UUT contains the data defined in the proceeding paragraph, the tests available can be ranked in order from the most likely to fail to the least likely to fail. Those tests with a high potential for failure can be selected for any functional monitoring capability built into the system. This would generally be useful to those designers responsible for the system BIT development. Furthermore, most tools will identify the minimum number of tests necessary to meet fault isolation requirements. This test set can form the basis for fault detection testing, and fault simulation points during test development.

2.1.3.4 Building the System Model

Until now we have considered only component and unit level analysis. This section discusses how the technique can be applied to the system level as well. The dependency logic models created by the analysis of units within the system are joined together by using system interconnect data. The external input events of each unit are linked to the external terminal events of the source units, thus

creating the next higher level of the system. The dependencies of the units comprising any assembly/sub-assembly group will uncover any inter-unit feedback loops that might otherwise go unnoticed. At this level of the system modeling the units effectively become the replaceable items in the assembly groupings. The linking continues until the highest level of the system is attained.

Dependency modeling is very effective for analyzing an equipment design at several different levels of detail. If the analysis is intended to provide an assessment of the fault isolation capabilities, or aid in the selection of testpoints for BIT and fault detection at a major level of assembly, the analyst can create unit models that do not have lower level detail. The resulting unit models would contain the dependency relationships of the inputs and outputs of the unit, all of which would be used to indicate the status (good or bad) of the operation of the unit. These unit models, when grouped together, would represent an assembly, within the equipment, that contains an assortment of replaceable items. Although these unit models would not provide the detail required to fault isolate a component within the unit, they will allow the analyst to develop a strategy to isolate to the unit when it has failed. If the components of a unit must also be isolatable at some stage of the repair cycle, it would be necessary to model the units with the interior detail included. There are automated tools available that allow the analyst to include the detail in the unit model, and then make a copy which removes those details resulting in a less complex model for use in higher level strategy development. The analyst would then continue with the upper level "system modeling" of the equipment.

The more sophisticated automated tools have the capability necessary to allow the analyst to perform the "modeling" at any desired level within the equipment and then manipulate the models so that fault isolation at other levels can be developed using a single database of information. Some of these automated tools provide an audit trail, that the analyst would use to determine the steps performed to develop a particular "system model".

A "system model" is assembled from an assortment of "unit models" in much the same manner as the actual equipment is assembled from an assortment of parts. The modeling of an equipment is conducted from the bottom up, much as the equipment is built up from ever larger pieces until the full assembly is attained.

The assembly of the "system model" must be done carefully, so that the resulting model is representative of the particular equipment configuration being analyzed.

2.2 Summary

A review of the literature (see references [1], [2]) will reveal that several techniques for performing testability analysis have been introduced within the last 20 years. However, of the testability tools that are readily available and have been used on actual systems, the three basic techniques discussed is Section 2.1 are the most commonly employed.

A review of the three techniques discussed reveals the following:

- The SCOAP program was one of the first programs to implement C/O methods to determine node testability. While SCOAP is limited to strictly digital circuits, several companies have used it in-house and have been able to modify it to handle re-convergent fan-out and to predict things such as the cost of testing a node. This C/O method is still in use today in tools such as Daisy Testability Analyzer (DTA) (see Section 3.0) but each of the C/O based tools remains limited to digital circuits at the PCB level or lower.

- The heuristic scoring and design guide technique developed by Grumman is probably the only technique, (because part of it is a design guide), that actually shows design methods for improving testability. Most other tools only indicate where improvement should be made. While the Grumman technique is somewhat outdated, it is being brought up-to-date by Raytheon Corporation who themselves have used the Grumman technique as have several other manufacturing firms. The major limitation of this technique is that it is mostly applicable to digital circuits at the PCB level.

- The last technique discussed, dependency modeling, is probably the most versatile in that it is applicable at all levels of design and all kinds of technology (i.e., digital, analog, mechanical, electro-

hydraulic, fluid systems, etc.). The tools based on this technique provide information on where testing is, and is not, required for fault-isolation, and what areas of a design needs addressing to improve testability. These tools also provide optimal diagnostic trees that can be weighted by one or more factors (see Section 3.0). Lastly, when combined with any of the tools based on the other techniques discussed, the testability analyst has a powerful means for implementing DFT principles.

3.0 TESTABILITY EVALUATION AND ANALYSIS TOOLS

A brief synopsis of several of the tools that have been investigated as part of this program are listed on the following pages. These reports contain a brief description of their capabilities. A more detailed description of the tools that are available to the reader is provided in Section 3.1.1. For information on those tools that are listed, but not available, consult the noted references contained in the bibliography.

3.1 Testability Tools Overview

There are a number and a variety of testability evaluation and analysis tools that can be used on a multitude of system scenarios. They are described as functional and logical modeling techniques. They provide either quantitative or qualitative analysis, depending on the results desired. The functional models are used typically for analyzing electronic configurations and the logic models are used for modeling all other configurations besides electronic, such as mechanical, electro-mechanical hydraulic, etc.

Testability tools are available in both manual and automated forms. In general, automated tools are used to perform quantitative testability analyses while manual tools are mostly used to perform qualitative testability analyses. Figures 3-1 and 3-2 provide the breakdown of both available and non-available tools, their functions and developers.

Automated testability tools are available from both commercial and government sources. The commercial tools listed are proprietary to their respective companies. Typically, they can be licensed from the originator or the originator can, in some cases, be contracted to perform the analysis. The automated and manual tools developed by the government are available at no cost to qualified users.

1. Checklist Tools

- CODMOD (Consolla and Danner; RADC PCB Checklist)*
- MILMOD (Military Model; MIL-STD-2165 Appendix B)*

2. Controllability/Observability Tools

Deterministic:

- TESTSCREEN (Testability Analysis Program; Sperry Research Center)*
- TMEAS (Testability Measurement Program; AT&T)*
- SCOAP (SANDIA Controllability/Observability Analysis Program; SANDIA Labs)
- ITFOM (Inherent Testability Figure of Merit; Sperry-Univac)*
- CAMELOT (Computer Aided Measure for Logic Testability; Cirrus Computers)*
- ITTAP (Interactive Testability Analysis Program; ITT)*
- COMET (Controllability and Observability-Measure for Testability - United Technologies)*
- VICTOR (VLSI Identifier of Controllability, Testability, Observability and Redundancy; University of California)*
- COPTER (Controllability-Observability-Predictability-Testability Report; CALMA)*
- HECTOR (Heuristic Controllability & Observability Analysis; Siemans)*
- A Calculas of Testability at the Functional Level (Nippon Electric)*
- INTELLIGEN (Developed by RACAL-REDAC)
- Daisy Testability Analyzer (DTA) (Daisy Systems Corp.)

Probabilistic:

- COP (Controllability/Observability Program; BNR)*
- PREDICT (Probabilistic Estimation of Digital Circuit Testability; AT&T)*
- PROTEST (Probabilistic Testability Analysis; University of Karlsruhe)*

3. Dependency Modeling Tools:

- LONGMOD (Longendorfer Model; Northrop)*
- STAMP (System Testability and Maintenance Program; ARINC)
- STAT (System Testability Analysis Tool; DETEX)
- WSTA (Weapons System Testability Analyzer; NAVSEA)
- I-CAT (Interactive Computer Aided Testability; Automated Systems Technology Corporation)

Other Testability Assessment Tools:

- ASTEP (Advanced System Testability Evaluation Program; BITE Corporation)
- TRI-MOD (Mission Effectiveness Testability Analysis; GAI)
- HAT (Heuristic Advisor for Testability; University of Illinois)*
- ACE-APT (Computational Environment/APT; ALPHATECH, Inc.)
- CAFIT (Computer Aided Fault Isolation/Testability; NOSC)

* Not available to public domain, consult references for further information.

Figure 3-1: Testability Analysis Tools & The Developers

TOOL	DATE	TYPE OF SYSTEM			LEVEL WITHIN SYSTEM			
		Analog	Digital	Other	CHIP	BOARD	SUBSYSTEM	SYSTEM
CODMOD	1980		X			X		
MILMOD	1985	X	X		X	X	X	X
TEST SCREEN	1979		X		X	X		
TMEAS	1979		X		X	X	X	X
SCOAP	1980		X		X	X	X	X
ITFOM	1981		X		X	X	X	X
CAMELOT	1981		X		X	X	X	X
ITTAP	1982		X		X	X	X	X
COMET	1982		X		X			
VICTOR	1982		X		X			
COPTR	1983		X		X			
HECTOR	1984		X		X			
INTELLIGEN	1989		X		X	X		
DTA	1984		X		X	X		
COP	1984		X		X			
PREDICT	1984		X		X			
PROTEST	1985		X		X			
LONGMOD	1982	X	X		X	X	X	X
STAMP	1984	X	X	X	X	X	X	X
WSTA	1988	X	X	X	X	X	X	X
STAT	1988	X	X	X	X	X	X	X
I-CAT	1989	X	X	X	X	X	X	X
ASTEP	1988	X	X	X	X	X	X	X
TRI-MOD	1984	X	X		X	X	X	X
HAT	1985		X		X	X	X	X
CAFIT	1988	X	X		X	X		
ACE-APT	1986	X	X		X	X		

Figure 3-2: Breakdown of Testability Tools & Their System Applicability

3.2 Automated Testability Analysis Tools Description

In this section, a description of those automated tools that are available to the public domain is provided. A description for those tools that are labeled with an asterisk (*) in Table 3-1 will not be described as they are not readily available to the public domain.

The tools to be described are:

1. STAT (System Testability Analysis Tool) - DETEX Systems, Inc. Orange, CA (Proprietary)

2. STAMP (System Testability and Maintenance Program) - ARINC Corporation, Annapolis, MD (Proprietary)

3. WSTA (Weapon System Testability Analyzer) - US Navy (NAVSEA) developed by Harris Corporation, Syosset, NY

4. I-CAT (Intelligent Computer Aided Testability) - Automated Technology Systems Corporation, Hauppauge, NY

5. CAFIT (Computer Aided Fault Isolation and Testability) - US Navy (NOSC) developed by ATAC Corporation, Mountain View, CA

6. DTA (Daisy Testability Analyzer) Daisy Systems Corporation, Sunnyvale, CA

7. SCOAP (SANDIA Controllability/Observability Analysis Program; SANDIA Laboratories, Albuquerque, NM)

8. INTELLIGEN (Developed by RACAL-REDAC, Westford, MA)

9. ASTEP (Advanced System Testability Evaluation Program; BITE Corporation, Manasass, VA)

10. ACE-APT (APT Computational Environment - Alphatech Program for Testability; Alphatech Incorporated, Burlington, MASS)

All manual tools are based primarily on the Grumman developed PCB Design Guide and Rating System described in Section 2.1.2 and, therefore, will not be described here.

The tools to be described will be grouped according to the analysis technique they are based on.

3.2.1 C/O Based Tools

The C/O based tools to be described are: SANDIA Controllability/Observability Analysis Program (SCOAP), Daisy Testability Analyzer (DTA), and INTELLIGEN.

3.2.1.1 Sandia Controllability/Observability Analysis Program (SCOAP)

Background: The SCOAP is one of the better known testability analysis tools. It was first published by Lawrence Goldstein of Sandia Laboratories in 1979. Being public domain, several commercial software vendors have used copies or enhanced versions of SCOAP for their testability analysis lines. GENRAD, CALMA, and DAISY have CAE workstation versions with complete IC model libraries. The most powerful of these is the DAISY Testability Analyzer (DTA) (described elsewhere in this report), because of its unique "auto insert" mode. This mode recommends optimum test point (TP) locations based upon calculations of every node's TP impact on the design. Other SCOAP enhanced venders do not have this feature.

SCOAP cannot detect re-convergent fan-outs, the SCOAP is limited to digital, and IC level use. It is also not applicable as a mixed technology system level tool. The primary goal of SCOAP is to provide a quantitative measure of the difficulty for controlling and observing the logical values of internal nodes of a network. This is accomplished by considering the circuit topology alone without analyzing sequences of input and state vectors or assuming any particular test methodology.

The SCOAP provides the following:

1) Computes estimates of combinational and sequential controllability for each node in the network.

2) Computes estimates of combinational and sequential observability for each node in the network.

3) Identifies controllable loops and/or nodes that cannot be observed at a primary output.

A large controllability/observability number at an identified node indicates that the node is difficult to control/observe.

The SCOAP uses a deterministic approach to estimating controllability and observability of each internal node in a digital system. This is accomplished by considering only the topology of the network. That is, the network is viewed as an interconnection of standard cells (combination or sequential).

Equations derived for each standard cell are used to compute controllability numbers for each cell output node and observability of each cell input node. The combination numbers at an identified node are an estimate of the minimum number of node assignments that must be made to control and observe the node. The sequential numbers at the identified node are an estimate of how many time frames are required to control and observe the node.

3.2.1.1.1 Algorithms and Heuristics

Controllability estimates for all nodes in a network are obtained by:

1) Initializing CC^0 and CC^1 to 1 at primary inputs

2) Initializing SC^0 and SC^1 to 0 at the primary inputs

3) Initializing CC^0, CC^1, SC^0, and SC^1 to infinity at all other nodes, and

4) Using standard cell controllability equations to map cell input node controllabilities to cell output node controllabilities along signal paths in the network.

Iterations are necessary around feedback loops external to standard cells until the controllability numbers stabilize.

Observability estimates for all nodes in a network are obtained by:

1) Initializing CO and SO to 0 at the primary inputs

2) Initializing CO and SO to infinity at all other nodes, and

3) Using standard cell observability equations to map cell output node observabilities into cell input node observabilities (observability of fan-out point is defined to be equal to the minimum of the observabilities of the nodes to which it fans out). Iterations are necessary around feedback loops external to standard cells until the observability numbers stabilize.

Measures developed: SCOAP computes six quantities for each internal node in a combinational or sequential network which provide a measure of testability for the network. These quantities are:

1) $CC^0(N)$, combinational 0-controllability: An estimate of the minimum number of combinational node assignments required to set node N to 0. (A combinational node is defined as either a primary input node or an output node of a combinational standard cell).

2) $CC^1(N)$, combinational 1-controllability: An estimate of the minimum number of combinational node assignments required to set node N to 1.

3) CO(N), combinational observability: An estimate of the number of combinational standard cells between node N and a primary output and the minimum number of combinational node assignments required to propagate the value at node N to a primary output.

4) $SC^1(N)$, sequential 1-controllability: An estimate of the minimum number of sequential nodes that must be set to specified values in order to set N to O. (A sequential node is defined as an output node of a sequential standard cell).

5) $SC^0(N)$, sequential 0-controllability: An estimate of the minimum number of sequential nodes that must be set to specified values in order to set N to O.

6) SO(N), sequential observability: Is an estimate of the number of sequential standard cells between node N and a primary output and the minimum number of sequential node assignments required to propagate the value at node N to a primary output.

The combinational numbers (CC^0, CC^1, and CO) at node N are estimates of spatial complexity (the minimum number of node assignments) required to control or observe node N.

The sequential numbers (SC^0, SC^1, and SO) at node N are estimates of temporal complexity (the number of time frames) required to control or observe node N.

Interaction with other methods: SCOAP provides the designer with controllability and observability information on a proposed design; this enables the designer to identify nodes that are difficult to control so that design changes can be made to improve testability. There is no direct interaction with other methods for establishing testability of a proposed design.

3.2.1.1.2 Additional Information

SCOAP was developed at Sandia National Laboratories (SNL) in Albuquerque, New Mexico.

Since SNL is a Department of Energy (DOE) function, the SCOAP source code is available to the public domain for little to no cost. Several vendors have acquired SCOAP and have used it in their own testability analysis tools. For more information on SCOAP and how it might be obtained, contact SNL at the following address:

SNL
Albuquerque, NM
Phone: (505) 844-5678

3.2.1.2 Daisy Testability Analyzer

The Daisy Testability Analyzer (DTA) is one of several testability analysis tools that is based on the SCOAP algorithm developed at Sandia Labs. While DTA does not solve the problem that SCOAP has with reconvergent fanout, it does improve upon SCOAP with something called the "auto-insert" mode. When used in this mode, DTA will recommend optimum test point (TP) locations based upon calculations of every node's TP impact on the design.

DTA will quantify testability factors such as sequential and combinational controllability and observability throughout a circuit and report the results to the user. DTA calculates six testability functions for each circuit under analysis. The six functions are:

1) combinational 0 - controllability (CC^0)
2) combinational 1 - controllability (CC^1)
3) sequential 0 - controllability (SC^0)
4) sequential 1 - controllability (SC^1)
5) combinational observability (CO)
6) sequential observability (SO)

CC^0, CC^1, SC^0, SC^1, CO and SO are defined and discussed in Section 2.0 and in the above description of SCOAP.

DTA evaluates the above functions at each node in the circuitry. A node is either a primary circuit input or a logic cell output. A node can be considered a combinational node if it is a circuit input or output from a combinational cell. It can be considered a sequential node if it is the output from a sequential cell. Sequential cells are clocked devices and combination cells are logic gates.

Combinational controllability (CC^0, CC^1) of a node, determines the number of combinational nodes in the circuit that must be controlled, to control the logic gate at the node. The combinational observability (CO) of a node determines the number of combinational nodes in a circuit that must be controlled, to propagate the logic value at the node to an observable circuit output. These values, together, indicate how difficult it will be to generate test patterns to test the node because, they

measure the complexity of the circuit logic. The values are also a secondary indicator of the time required to run a test on the finished circuitry.

Similarly, sequential controllability (SC0, SC1) of a node measures the number of sequential cells that must be controlled to create a 0 or 1 at the node. Sequential observability (SO) measures the number of sequential cells that must be controlled to propagate the logic value at the node to a circuit output. These values together, give an indication of the number of time frames required to test a node. They actually represent a worst case scenario, since it may be possible to exploit parallelism in the circuit to control more than one sequential node at a given time.

DTA provides a report showing CC0, CC1, SC0, SC1, CO and SO values for each node in a circuit and an example of the measures report is provided in Figure 3-3. The report lists each node in the far left column, and provides the listed testability measures listed across the top. Negative numbers indicate nodes that are difficult to control or observe and require testability improvement.

When run in the "auto-insert" mode, DTA will automatically insert test points required to improve the controllability and observability of the nodes in a circuit. The test point recommendations are based on user inputs for how many input only tests, output only tests, and input-output tests are required. The optional test points matching the three user selected criteria are provided in a summary output report. Figure 3-4 shows an example of this report before and after the "auto-insert" mode was invoked for a sample circuit. Note that the DTA Optimal Testability shows the percent improvement in the six testability measures over the baseline assessment.

3.2.1.2.1 DTA Input/Hardware

DTA operates on a Daisy Logician Workstation. There is a Computer Aided Engineering (CAE) workstation version with complete IC model libraries. Figure 3-5 shows the sequence of the daisy software for DTA.

NAME	CC0	CC1	SC0	SC1	CO	SO
@Pages/1:A1057	1	1	0	0	8	0
@Pages/1:A1059	1	1	0	0	31	0
@Pages/1:A1062	1	1	0	0	-1	-1
@Pages/1:A1065	1	1	0	0	-1	-1
@Pages/1:A1153	1	1	0	0	-1	-1
@Pages/1:A1233	1	1	0	0	-1	-1
@Pages/1:A1240	1	1	0	0	-1	-1
@Pages/1:A1687	1	1	0	0	-1	-1
@Pages/1:A1764	1	1	0	0	-1	-1
@Pages/1:A1824	1	1	0	0	-1	-1
@Pages/3:A2550	1	1	0	0	1	0
@Pages/3:A2555	1	1	0	0	-1	-1
@Pages/3:A2568	1	1	0	0	2	0
@Pages/3:A2626	1	1	0	0	-1	-1
@Pages/2:AZ21	1	1	0	0	-1	-1
@Pages/2:AZ27	1	1	0	0	-1	-1
@Pages/1:GTD34	1	1	0	0	64	0
@Pages/3:OPGEARBXSW	1	1	0	0	-1	-1
@Pages/3:OPGTDSW	1	1	0	0	-1	-1
@Pages/4:SLANTANGLEINPUT	1	1	0	0	-1	-1
@Pages/5:TEST27	1	1	0	0	-1	-1
@Pages/5:TEST28	1	1	0	0	-1	-1
@Pages/5:TEST29	1	1	0	0	-1	-1
@Pages/5:TEST30	1	1	0	0	-1	-1
@Pages/5:TEST31	1	1	0	0	-1	-1
@Pages/5:TEST32	1	1	0	0	-1	-1
@Pages/5:TEST33	1	1	0	0	-1	-1
@Pages/5:TEST34	1	1	0	0	-1	-1
@Pages/5:TEST35	1	1	0	0	-1	-1
@Pages/5:TEST36	1	1	0	0	-1	-1
@Pages/5:TEST37	1	1	0	0	-1	-1
@Pages/5:TEST38	1	1	0	0	-1	-1
@Pages/5:TEST39	1	1	0	0	-1	-1
@Pages/5:TEST40	1	1	0	0	-1	-1
@Pages/5:TEST41	1	1	0	0	-1	-1
@Pages/5:TEST42	1	1	0	0	-1	-1
@Pages/5:TEST43	1	1	0	0	30	0
@Pages/5:TEST51	1	1	0	0	-1	-1
@Pages/5:TEST52	1	1	0	0	-1	-1
@Pages/5:TEST53	1	1	0	0	-1	-1
@Pages/5:TO22	1	1	0	0	-1	-1
@Pages/5:TO27	1	1	0	0	-1	-1
@Pages/3:XWINDVELOCITYIN	1	1	0	0	26	0
@Pages/1:A1837	2	2	0	0	-1	-1
@Pages/1:TEST54	4	3	0	0	-1	-1
@Pages/1:A2671	3	3	0	0	31	0
@Pages/1:SXIG380	5	30	0	0	-1	-1
@Pages/1:A1768	3	3	0	0	29	0
@Pages/1XSIG330	2	2	0	0	30	0
@Pages/1:TEST25	4	-1	0	-1	-1	-1
@Pages/1:A2669	2	2	0	0	26	0
@Pages/1:A3200	2	2	0	0	18	0
@Pages/1:XSIG430	2	2	0	0	7	0
@Pages/1:A2590	3	3	0	0	6	0
@Pages/1:A1790	5	5	0	0	-1	-1
@Pages/1:XSIG477	6	6	0	0	13	0
@Pages/1:XSIG484	6	6	0	0	29	0
@Pages/1:XSIG487	4	21	0	0	-1	-1
@Pages/1:XSIG493	30	30	0	0	-1	-1
@Pages/1:A2076	7	7	0	0	12	0
@Pages/1:A2652	5	22	0	0	-1	-1

Note the "-1" unable to be observed or controlled signals

Figure 3-3: Example of DTA Output Values Report

**** DTA TESTABILITY REPORT ****

	Maximum Value	Count Max Val	Average Vale	% Improvement	Count Untestable
Combinational 0-Controllability (CC0)	34	5	8	0	0
Combination 1-Controllability (CC1)	82	1	11	0	55
Sequential 0-Controllability (SC0)	0	321	0	0	0
Sequential 1-Controllability (SC1)	0	274	0	0	55
Combinational Observability (CO)	64	1	16	0	240
Sequential Observability (SO)	0	89	0	0	240
Mean	-	-	5	0	-
Standard Deviation	-	-	6	0	-

**** DTA OPTIMAL TESTABILITY REPORT ****

	Maximum Value	Count Max Val	Average Vale	% Improvement	Count Untestable
Combinational 0-Controllability (CC0)	20	1	5	45	0
Combination 1-Controllability (CC1)	30	1	6	50	55
Sequential 0-Controllability (SC0)	0	321	0	0	0
Sequential 1-Controllability (SC1)	0	274	0	0	55
Combinational Observability (CO)	16	2	4	80	240
Sequential Observability (SO)	0	89	0	0	240
Mean	-	-	3	54	-
Standard Deviation	-	-	2	67	-

The auto insert (input output I/O) number is (2 8 2)

The optimal input points are
@PAGES/7:xCMP43.T1
@PAGES/6:XSIG20

The optimal output points are
@PAGES/1:AZ30
@PAGES/1:A2679
@PAGES/5:CLK
@PAGES/5:A3206
@PAGES/1:A2080
@PAGES/5:A2057
@PAGES/1:A2675
@PAGES/1:A2076

The optimal I/O points are
@PAGES/6:XCMP78.T1
@PAGES/7:XCMP44.T1

Figure 3-4: DTA Normal (Top Third)/Auto-Insert (Lower Two-Thirds) Test Reports. Note Combinational Improvements.

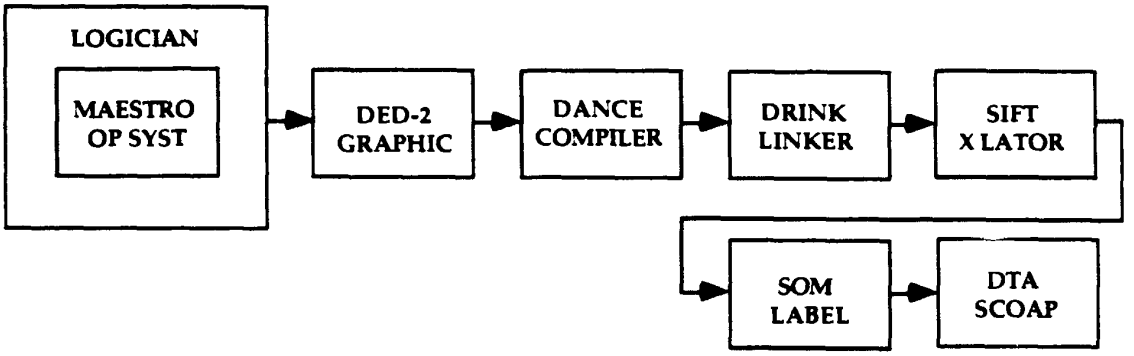


Figure 3-5: Sequence of Daisy Software for DTA

3.2.1.2.2 Additional Information

At the time of this report, the RAC has been unable to determine the point of contact for the DTA software. Anyone having such information is encouraged to contact the RAC at the phone or address provided in the front of this document.

3.2.1.3 INTELLIGEN

Intelligen, developed by HHB Systems, a subsidiary of Racal-Redac, Inc., is primarily an automatic test generation (ATG) tool for application specific integrated circuits (ASICs), that uses testability analysis techniques to determine where test points are required for effective fault coverage. Intelligen has been used by several manufacturers as documented in References [6], [7] and [8].

The best description of the tool's capabilities was found in an article on Software Support for Boundary-Scan Techniques in the June, 1990 issue of Electronics Test (Reference [6]). The following write-up is taken from the referenced article:

3.2.1.3.1 Making Faults Visible

In the typical design cycle, the user finds the best locations for the T-Cells using the Racal-Redac INTELLIGEN design-for-testability system. The system is built upon an

ATG program geared for complex sequential circuits with feedback loops, asynchronous logic, and complex clocking structures.

Though it runs on a workstation, the program is a batch processing job and requires successive passes. It requires the user-a design engineer (perhaps collaborating with a test engineer) - to provide a complete net list for the circuit from which a fault list can be generated. In its operation, the ATG attempts to generate tests for every one of the faults listed. Its output is a list of both successes and failures. The successes are usable test stimulus vectors. The failures are analyzed to produce recommendations about where testability could be improved by the insertion of a T-Cell. The program can generate Joint Test Action Group (JTAG)-compatible test vectors designed to take advantage of these inserted structures.

As a first step, the program performs a testability analysis, analyzing each circuit node for observability and controllability. This is followed by an "observability" analysis that works backward from the outputs of a circuit to its inputs. This analysis is intended to reveal major testability problems. The static testability analysis doesn't tell how difficult it will be to generate tests for the circuit, nor what kind of fault coverage will be obtained. Outputs of the testability analysis include the extent of uncontrollable nodes, unobservable nodes, uninitializable loops, and some ATG decision priorities.

To generate tests, the ATG program within INTELLIGEN selects a fault from its fault list and attempts to build a test specifically for that fault. If it is successful, the set of test vectors generated gets passed to an online fault simulator, which runs the test to see if those vectors will reveal other faults as well. Those successfully tested faults are eliminated from the fault list. When this operation is complete, the control program accesses the database again and selects another undetected fault. This process continues until all the faults on the list are processed.

In the selection of a fault, the static testability information helps select a path through the circuit that offers the best means of observability for that fault. The algorithm determines the best path working backward from a primary output through the fanouts of a logic device. The backtrace algorithm works backward through the logic, relating output sensitivity to inputs (path sensitization), until it comes to a fault site.

Nodal values that are calculated to sensitize the path and exercise the fault are also driven backwards through the circuit by a process called justification. The backtracing processes are designed for sequential logic so that all necessary circuit initialization is automatically generated. The resulting vectors drive the circuit through a state sequence necessary to exercise the target fault and propagate the fault effect to an external pin.

The process completes itself for "testable" circuits. Complex circuits, however, are not always testable. Where the process is incomplete, the "blocking nodes" are identified. These are the nodes that have prevented a complete test from being constructed. Where this occurs, the representative fault on the fault list is marked.

The process is retried for the next fault on the list in the ATG database. Blocking nodes are once again identified, and these are compared with the blocking nodes identified in the test generation process for the first fault. Typically, only a few nodes contribute to most of the blocked test generation attempts. ***Where these nodes can be identified, testability improvements can be made at these strategic locations.***

Each vector produced in this way specifies the signals on the actual functional pins of the chip as well as the state that has to be loaded into the T-Cells. A programmable post processor takes vectors produced in this form and establishes the proper protocol to drive the external pins and serially load the scan chains. These vectors can be output in 1149.1 or any other user-defined protocol.

ATG program geared for complex sequential circuits with feedback loops, asynchronous logic, and complex clocking structures.

Though it runs on a workstation, the program is a batch processing job and requires successive passes. It requires the user-a design engineer (perhaps collaborating with a test engineer) - to provide a complete net list for the circuit from which a fault list can be generated. In its operation, the ATG attempts to generate tests for every one of the faults listed. Its output is a list of both successes and failures. The successes are usable test stimulus vectors. The failures are analyzed to produce recommendations about where testability could be improved by the insertion of a T-Cell. The program can generate Joint Test Action Group (JTAG)-compatible test vectors designed to take advantage of these inserted structures.

> ***As a first step, the program performs a testability analysis, analyzing each circuit node for observability and controllability. This is followed by an "observability" analysis that works backward from the outputs of a circuit to its inputs. This analysis is intended to reveal major testability problems. The static testability analysis doesn't tell how difficult it will be to generate tests for the circuit, nor what kind of fault coverage will be obtained. Outputs of the testability analysis include the extent of uncontrollable nodes, unobservable nodes, uninitializable loops, and some ATG decision priorities.***

To generate tests, the ATG program within INTELLIGEN selects a fault from its fault list and attempts to build a test specifically for that fault. If it is successful, the set of test vectors generated gets passed to an online fault simulator, which runs the test to see if those vectors will reveal other faults as well. Those successfully tested faults are eliminated from the fault list. When this operation is complete, the control program accesses the database again and selects another undetected fault. This process continues until all the faults on the list are processed.

3.2.1.3.2 Additional Information

Intelligen accepts as input EDIF 200 or circuit netlist descriptions, optional functional vectors and optional behavioral data. Intelligen integrates the power of sequential circuit automatic test pattern generation and the Reduced Intrusion Scan Path (RISP™) methodology into a tool that handles designs without scan built in.

RISP is a process of selectively inserting testability enhancement logic into a circuit based on feedback from an ATG. Partial scan path circuitry can be automatically implanted in a logic circuit where indicated by the INTELLIGEN software. The purpose of a partial scan technique such as Reduced Intrusion Scan Path (RISP) is to minimize intrusion into an ASIC by using a test cell, or testability cell (referred to as a "T-cell"), with abbreviated flip-flop chains to access a node in a sequential circuit.

Since the T-Cell method is compatible with IEEE standard 1149.1, the Joint Test Action Group (JTAG) boundary-scan-interface standard, any test vectors created by INTELLIGEN can be applied at the board level to test each ASIC device separately, by using the four pin test bus defined by the JTAG standard.

To obtain more information on INTELLIGEN, contact Racal-Redac at the following address:

Westford Regency Park, 238 Littleton Road
Westford, MA 01886
Tel: (508) 692-4900 Fax: (508) 692-4725

For information on scan techniques as a means of implementing test design see reference [6] in the bibliography.

3.2.2 Dependency Modeling Based Tools

The dependency modeling based tools to be described are: System Testability Analysis Tool (STAT), System Testability and Maintenance Program (STAMP), Intelligent-Computer Aided Testability (I-CAT), and Weapon System Testability Analyzer (WSTA).

3.2.2.1 The System Testability Analysis Tool (STAT)

STAT is an advanced version of the LOGMOD (Logical Modeling) testability analysis tool that had its beginnings in 1968. STAT, as with other dependency model based tools, can be used to model electronic, mechanical, hydraulic and other kinds of systems and equipments. The dependency modeling is performed manually through coded designations that identify the items being modeled and their dependencies (inputs and outputs). The dependencies are then converted into dependency statements that are used as inputs into STAT. Using this input, STAT provides a dependency chart, or topological "roadmap", of the system/equipment being modeled and prints out several testability reports. The processing of the models and testability reports are performed automatically by a PC, VAX or SUN computer.

Current versions of STAT require that the model information be entered via the key board. However, the program has a good graphical interface for inputting dependency model and other information related to the test point and specific items. Copies of the input screens are shown in Figures 3-6 and 3-7.

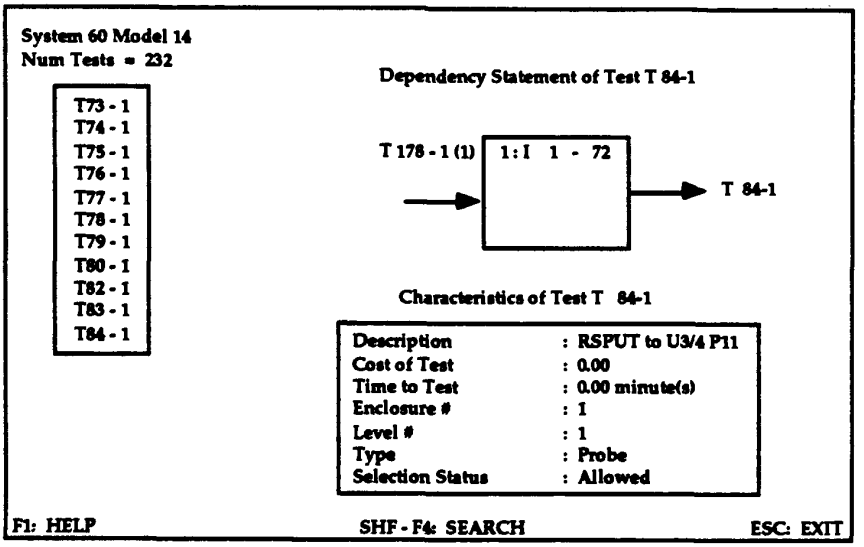


Figure 3-6: STAT Model Input Screen-Tests and Dependencies

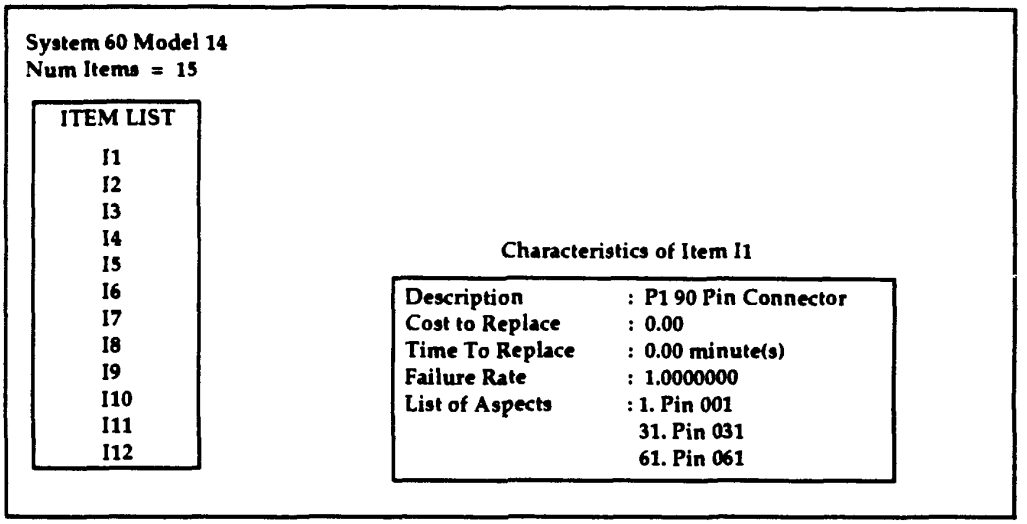


Figure 3-7: STAT Model Input Screen-Item Information

The STAT program also allows you to equate a single test to several other tests. This comes in quite useful in situations where several inputs, such as +5V, ground, address or data buses, are available at several locations on, say, a PCB design. Instead of typing in each individual test input over and over, the equate functions lets you enter only one test input over and over, saving model input time and reducing room for possible input error.

Once the initial model is entered, this becomes the base model from which several cases can be derived to analyze a design and make testability trade-off decisions. Cases of the base model are made quite easily in STAT using the case model editor, wherein test points can be turned on or off without having to delete or add tests as you go along. After a case model is developed, the system processes the information, checking for any errors and identifying fan-out points and feedback loop information.

3.2.2.1.1 STAT Output Reports

Once a model is processed, STAT allows you to develop a number of output reports described briefly below:

1. **Topological Indicator Report:** Provides for both a summary and detailed analysis of the topological information contained in the model. Included in the summary analysis report are the topological complexity chart, test and test aspect statistics, item and item aspect statistics, and inherent ambiguity group statistics.

   The topological complexity chart is based on the number of tests, number of dependencies per test, and the number of dependents per test. The results of the chart can be used as a relative comparison of model complexity, and as a gauge in the complexity of performing tests and the cost of TPS development.

   The test and test aspect statistics reported reflect the total number of tests, the average number of aspects per test, average number of tests in a system fanout and the average number of 1st order dependents and dependencies for a test. Similar information is produced for item and item aspect statistics. The inherent ambiguity group statistics are based on the connectivity of the system and do not reflect the application of any fault-isolation algorithm. The ambiguity group statistics produced are the total ambiguity group size(s), total unique and non-unique ambiguity groups and relative isolation levels, weighted (by failure rate) and un-weighted.

   The detailed report provides a recap of the ambiguity group statistics, an ambiguity group reference list, item and test data, and test fan-out data.

2. **Feedback Loop Indicator Report:** There is a summary and detailed analysis output of this report. The summary analysis provides the total number of feedback loops, probability of failure within a feedback loop, percent of all items involved in feedback loop(s), feedback loop complexity chart, and aggregate item characteristics per feedback loops.

   Of the data provided in the summary, only the feedback loop complexity (FLC) chart warrants further explanation. The FLC chart

reflects the relative effect that feedback loops within the processed system or model have upon the total design. A HIGH FLC indicates that the fault-isolation process can be expected to produce adverse effects, due to the high level of influence of feedback loops within the design. These adverse effects will be manifest as increases in ambiguity group sizes, cost and time to isolate a primary failure, etc. As the FLC approaches 0.0, these adverse effects are minimized. This can be accomplished by enhancing the input data base design using Feedback Loop Breakpoints or by re-evaluating the design. If the FLC cannot be reduced by either of these means, then an increase in ambiguity group sizes will result. In this case, it should be obvious that "availability" (on-line) will then be subject to the reliability of the hardware contained in the Feedback Loops.

The detailed analysis report provides the following for each identified feedback loop: Input test(s), Internal test(s), Controllable system/model input test(s), Observable system/model output test(s), standard characteristics for item(s) in feedback loop, and any user-defined characteristics for each item.

Also as part of the Feedback Loop Indicator Report, a Breakpoint Analysis report can be generated. The following data for each feedback loop is provided: Possible breakpoints, Path reference number(s) broken by each possible breakpoint, Path reference number definitions, Reference number(s) for ambiguity groups created by each possible breakpoint, and the corresponding ambiguity group reference list. Note that a breakpoint represents a node in the system where a feedback loop could be physically broken to eliminate the ambiguity and testing problems created by a feedback loop. The same analysis is available interactively in STAT, wherein the possible breakpoints are presented and the user can choose a point and see the effects on-line. Once the user decides on the best possible breakpoint, the model can be modified automatically and a new system/model level analysis can be performed.

3. **Fault-Isolation Indicator Report (FIR):** Aside from the Feedback Loop Indicator Report, the FIR is the most important data output of the STAT program. There is a summary and detailed analysis output of the FIR. The summary analysis provides: Listings of operated selected fault-isolation parameters and weighting factors, statistics to isolate a primary failure, dynamic ambiguity group statistics, suggested test type selections in hierarchical order, and tests not utilized during fault-isolation strategy. Each of the summary outputs is explained below.

Before continuing, the FIR is generated as a result of STAT applying its test-strategy algorithm. This algorithm calculates, based primarily on the dependency model information, an optimal order of test performance for a failure detected at a primary system output. In the process of doing this, STAT calculates not only test order, but all possible ambiguity groups that will result for a given set of tests. Other information derived: statistics on the minimum and maximum number of tests to fault-isolate a failure, and percentage of time an isolation to a specific ambiguity group size will occur.

Detailed Description of FIR Summary Analysis Data

Operator Selected Fault-Isolation Parameters

There are two parameters that can be pre-selected by the user in influencing the fault-isolation strategy algorithm: Test Strategy Cut-off and Test Type Selection Cut-Offs.

There are three types of cut-off parameters that, in combination, determine the depth of the fault-isolation strategy:

1) Acceptable Ambiguity Group Size
2) Acceptable Ambiguity Group Replacement Time
3) Acceptable Ambiguity Group Replacement Cost

The test type selection cut-offs allow the user to choose the criteria for STAT to use when determining the kind of test to be performed at a particular node. In STAT, there are three kinds of tests to consider, Built-In-Test/Built-In-Test Equipment

(BIT/BITE), External Tests, and Probe Tests. When designing a system for testability, therefore, the user can input what percentage of tests (or nodes) they want available for BIT/BITE and what the maximum number of external tests node available is. Based on user input, STAT will recommend which tests should be used for BIT/BITE, External, or Probe.

Weighting Factors

There are currently thirteen different weighting factors available in STAT for influencing the fault-isolation strategy. They are:

- Test Cost
- Test Time
- Test User Function
- Enclosure Cost
- Enclosure Time
- Enclosure User Function
- Level Cost
- Level Time
- Level User Function
- Probability that test will be good
- Ambiguity Group Replacement Cost
- Ambiguity Group Replacement Time
- Ambiguity Group User Function

Any of the above factors can be used and ranked as to relative importance to the user. Interesting to note here are the enclosure and level factors. The test strategy can be structured to reflect the physical location of a test point and, therefore, the cost and/or time penalty that may be associated with accessing a particular test point. The user functions allow for adding weights such as safety or risk associated with performing a test, or the skill level required.

Statistics to Isolate a Primary Failure

This section provides statistics derived from the fault isolation paths resultant from applying the strategy (with assigned Cut-Offs) to the processed system or model

(with or without calculated Test Weightings). STAT provides minimum, maximum and average statistics for the following data:

- Number of Tests to isolate a failure(s)
- Test Cost in isolating a failure(s)
- Test Time to isolate a failure(s)
- Number of Enclosure transitions that must be made to isolate a failure

The statistics can be used for trade-off analyses, and as input to logistical and maintainability analyses.

Dynamic Ambiguity Group Statistics

This section of the report provides information on the number and size of ambiguity groups that exist based on applying the isolation strategy (with selected ambiguity group cut-offs) to the model information. Also provided are statistics on the percentage of ambiguity that are less than or equal to an indicated size. Such measurements include the MIL-STD-2165 calculation for fault-resolution.

Suggested Test Type Selections

Based on the user selected test-type cut-offs, STAT produces a list of all available tests, in a hierarchical order, and suggestions for the type of test (BIT, BITE, External, or Probe). The tests are listed in three separate groups, Internal tests, System Input tests, and System Output tests. The hierarchical order is based on an inherent rank and usage rank for each test. The inherent rank is based on the ability of a test to break up ambiguities within the system, and the usage rank is based on the frequency a test appears in different fault-isolation paths.

Test(s) Not Utilized During Fault-Isolation

STAT identifies and outputs those tests in the model that are not required for the level of fault-isolation reported in the Dynamic Ambiguity Group Statistics. The tests not utilized are dependent on which tests are available for fault-isolation. Therefore, as you add and/or delete tests, the tests not utilized list will, in most cases, change. The importance of this information is that STAT identifies those test

points that do not require associated test procedures, or the development and life cycle costs associated with the test procedures.

Detailed Description of FIR Detailed Analysis Data

The information provided in the detailed analysis report is: Diagnostic Flow Diagram, and Suspect Ambiguity Group Reference List.

The diagnostic flow diagram can be produced in tabular or graphical format. The diagram represents the test sequence required for fault-isolation based on STAT's inherent algorithm and all user selected cut-offs and weighting parameters. The test order is based on being able to determine if a test result is "good" or "bad". Figure 3-8 shows an example of the tabular diagnostic flow diagram. Note that the information shown for each test can be tailored, depending on what information is needed. Therefore all or none of the associated parameters shown need to be in the printout. Note also that the diagnostic diagram identifies when an isolation will occur, and lists an associated suspect ambiguity reference number (Sus AG Ref #).

The suspect ambiguity group (SAG) reference outputs list all suspect ambiguity groups by reference number as listed in the diagnostic flow diagram. The following information can be tailored for each STAT report, and an example printout corresponding to the flow diagram in Figure 3-8 is shown in Figure 3-9.

- Input test(s) of SAG
- Output test(s) of SAG
- Controllable system/model input test(s) of SAG
- Observable system/model output test(s) of SAG
- Standard characteristics for item(s) in SAG
- User-defined characteristics for item(s) in SAG

Each of the above listed data allow the analyst to quickly assess where the SAG is located in the system and where additional testing may be required to break up a particular SAG.

SYSTEM 1: Bad Actor Boards
MODEL 14: Receiver Status PWA CASE 5: Final Ver w/levls

FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Diagnostic Flow Table

	Record	Cfg-Test	-Asp	Previous Record	Next Diagnostic Step	(Record)
*	1.	1-T175	-1		GOOD: Goto 1-T162 -1	(30)
					BAD: Goto 1-T39 -1	(2)
	2.	1-T39	-1	1	GOOD: Goto 1-T38 -1	(3)
					BAD: Faulty Input	
	3.	1-T38	-1	2	GOOD: Goto 1-T2 -3	(4)
					BAD: Faulty Input	
	4	1-T2	-3	3	GOOD: Goto 1-T2 -2	(5)
					BAD: Faulty Input	
	5	1-T2	-2	4	GOOD: Goto 1-T2 -1	(6)
					BAD: Faulty Input	
	6	1-T2	-1	5	GOOD: Goto 1-T1 -3	(7)
					BAD: Faulty Input	
	7	1-T1	-3	6	GOOD: Goto 1-T1 -2	(8)
					BAD: Faulty Input	
	8	1-T1	-2	7	GOOD: Goto 1-T1 -1	(9)
					BAD: Faulty Input	
	9	1-T1	-1	8	GOOD: Goto 1-T65 -1	(10)
					BAD: Faulty Input	
	10	1-T65	-1	9	GOOD: Goto 1-T104 -1	(12)
					BAD: Goto 1-T64 -1	(11)
	11	1-T64	-1	10	GOOD: Replace SAG Ref #2	
					BAD: Replace SAG Ref #1	
	12	1-T104	-1	10	GOOD: Goto 1-T103 -1	(13)
					BAD: Replace SAG Ref #3	
	13.	1-T103	-1	12	GOOD: Goto 1-T162 -1	(14)
					BAD: Replace SAG Ref #4	
	14	1-T162	-1	13	GOOD; Replace SAG Ref. #6	
					BAD: Goto 1-T162 -1	(15)

Figure 3-8: Diagnostic Flow Table

SYSTEM 1: Bad Actor Boards
MODEL 14: Receiver Status PWA CASE 5: Final Ver w/levls

FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Suspect Ambiguity Group Reference List

Suspect AG Ref Number: 1 Suspect AG Size: 1

Input Test(s) of Suspect Ambiguity Group: [3]
1-T1-1 1-T1-2 1-T1-3

Output Test(s) of Suspect Ambiguity Group: [1]
1-T64-1

Standard Characteristics for Item(s) in Suspect Ambiguity Group:

Cfg-Item -Aspect	Item/Aspect Description		Cost to Replace		Time to Replace	Failure Probability
1-I1	P1 90 Pin Connector	++	0.00	++	0.00	++0.11402509
-1	Pin 001					
-31	Pin 031					
-61	Pin 061					
	TOTALS:		0.00		0.00	0.11402509

Figure 3-9: Suspect Ambiguity Group Reference List

4. **Management Model Report:** There are two outputs for this report: A summary analysis and a topological dependency graph.

   The summary analysis provides the following, in a tailored format. Number of original test(s), number of original input test(s) and output test(s), number of feedback loop test breakpoints, number of items and item aspects. The number of original test(s) does not include any added test breakpoints.

An example of the topological dependency graph is provided in Figure 3-10. This graph is a visual representation of the dependency model. It may be used for a quality assurance check of the dependency model and a quick means of locating where in the system a feedback loop is located.

In the graph shown in Figure 3-10, a Test is represented by the symbol "#". An Item is represented by the symbol "0". The dependence of one Test upon another is represented by either the symbol "<" or ">". The ">" symbol represents a "normal" dependency, while the "<" symbol represents a dependency that comprises part of a feedback loop.

In addition to the STAT features described, STAT also has a feature called "linking". This feature allows you to model parts of a system, independently, and then link the parts together to create a system level model.

An example of how this works would be to consider a system that comprises several modules, or subsystems, that are made up by several PCBs each. Using STAT, you can first model the PCBs to the component level. Once this is done, each PCB model can be "collapsed" by STAT wherein the PCB becomes an individual replaceable item with inputs and outputs that retain the connectivity information provided in the lower level model. Each collapsed PCB model can then be linked with other collapsed PCB models to form a module-level model. The module-level models can then be collapsed themselves, and linked together to form a system model.

Such a linking process allows testability analysis to all levels, and makes STAT applicable to each phase of development.

3.2.2.1.2 Additional Information

The STAT program is available on a lease/license arrangement and operates on a pc or vax computer. A unix version of the software may be available by mid-1991.

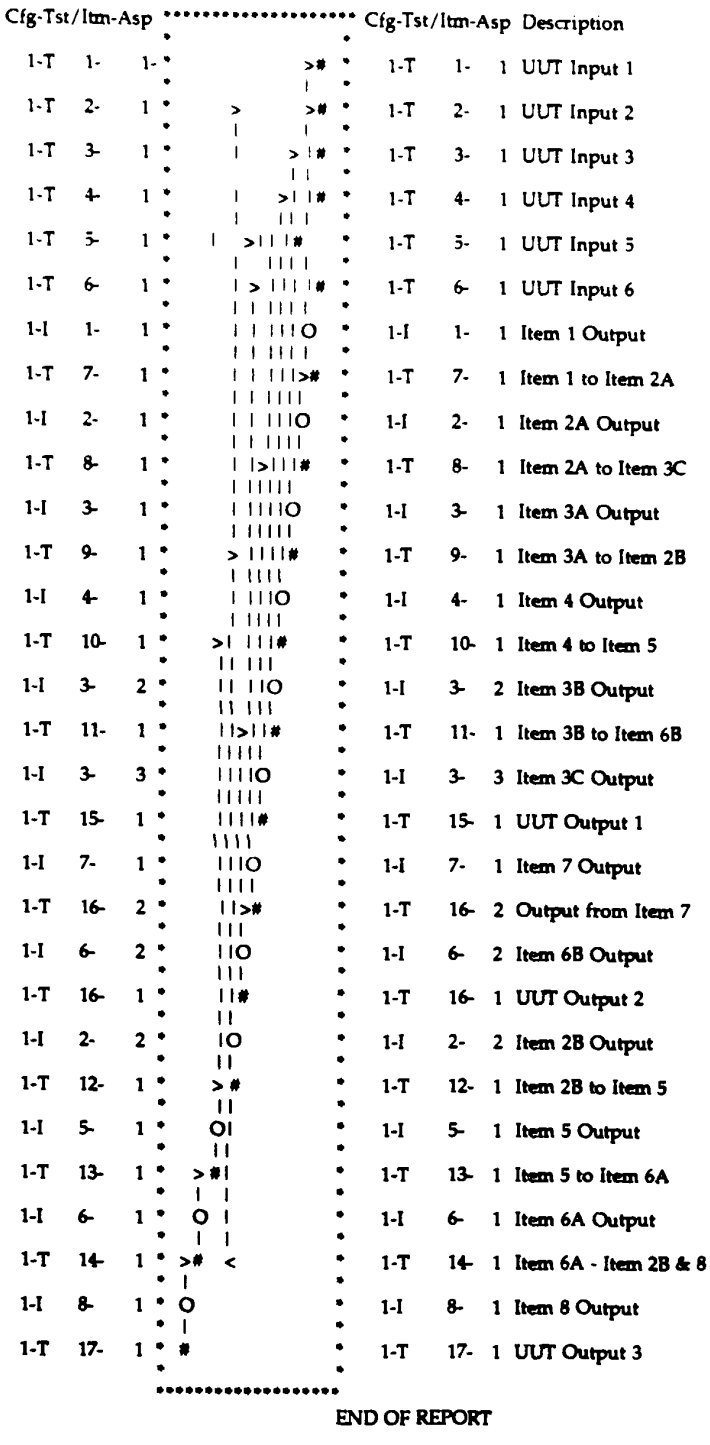


Figure 3-10: Management Model Report
Topological Dependency Graph

For further information on the STAT program, contact DETEX Systems, Inc. at the address below:

1574 N. Batavia
Suite 4
Orange, CA 92667

Phone: 714/637-9325
Fax: 714/998-4875

3.2.2.2 Weapon System Testability Analyzer (WSTA)

WSTA (pronounced WISTA) is another dependency modeling analysis tool and was developed by Harris Corporation as part of the US Navy's Integrated Diagnostic Support System (IDSS) program. While the name implies that this tool is for weapon systems, WSTA is applicable to most any kind of system, as are most dependency modeling tools.

A flow diagram of the WSTA program is shown below in Figure 3-11.

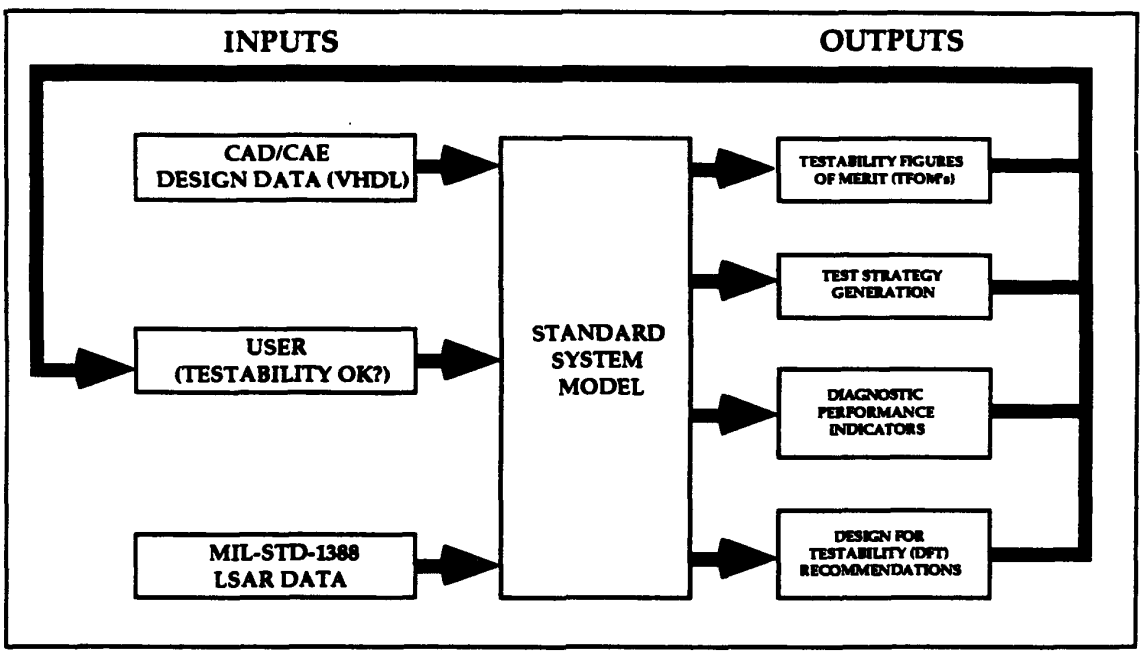


Figure 3-11: Testability Analysis Using WSTA

Referring to the above figure, the Standard System Model (SSM) block contains a subprogram that generates a dependency model based on the input data depicted. Where possible, the topological design data can be created with a Computer-Aided Design/Computer-Aided Engineering (CAD/CAE) tool in the Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL). This data, in the form of a net list and signal flow information goes into the common diagnostic database (CDDB), that also contains logistical data (the Logistic Support Analysis Record (LSAR) block in Figure 3-11) such as component failure rates, component replacement time, etc. The data contained in the CDDB can then, if necessary, be modified by the user through the WSTA model editor prior to model compilati For systems that cannot be designed in VHDL the topological dependency mo information can be entered manually by the user via the model editor.

As shown in Figure 3-11 there are four types of analysis outputs in WSTA. Each of these are described in the following paragraphs.

3.2.2.2.1 Testability Figures of Merit (TFOMs) - Static Analysis

The static analysis provides:

- Ambiguity Group Distribution Data
- Inherent Fault Isolation Levels
- Component Involvement Ratios
- Feedback Loop Data

As implied, the above data are TFOM's that indicate how well the inherent testability of the design is. Inherent fault-isolation levels are used to evaluate the percent of time an isolation to a specified ambiguity group level will occur (e.g., 95% isolation to 2 or fewer components). If requirements are not met, the data such as ambiguity group distribution and feedback loops are indications of where improvement is required to meet fault-isolation requirements. Component involvement ratio is a relative measure that reflects the involvement of a particular component in multiple fault-isolation paths. While this is not necessarily a testability measure, it is an indication of where reliability may need to be improved. Any component having a high involvement ratio, should be reviewed for

reliability, based on the premise that if the component has low reliability, its probable effect on system level failures is high, and should therefore be reduced.

3.2.2.2.2 Test Strategy Generation

The Test Strategy Generation creates a diagnostic fault tree. As with all other dependency model tools described in this document, the fault tree algorithm provides an optimized sequence of diagnostic tests for isolating each replaceable component(s). The diagnostic tree is based on standard pass/fail or good/bad criteria for each test, and identifies the failed component or group of components (ambiguity group) based on the assumption of a single failure.

The diagnostic tree produced by WSTA can be weighted by the following user selected factors: test time, test cost, user defined function, component replacement time, component replacement cost, and component failure probability. The tree can be produced in either tabular or graphical format.

3.2.2.2.3 Diagnostic Performance Indicators

The performance indicators provided by WSTA represent the testability performance that may be expected during an actual, on-line fault diagnosis session for the system being analyzed. A description of each indicator follows.

- **Isolation Penalties:** Mean/Maximum/Minimum-Time-To-Isolate and mean-cost-to-isolate any faulty component in the UUT. WSTA provides a graphical analysis of these factors that can be used to predict maintenance performance, compare designs for testability, and to improve the cost of fault isolation, such as increasing the reliability of components that have larger fault-isolation times.

- **Repair Penalties:** Mean/Maximum/Minimum-Time-To-Repair based on individual isolation times calculated automatically from the logistics data stored in the CDDB, coupled with individual component replacement times, and mean-cost-to-repair. A graphical analysis is provided and this information can be used to improve repair costs by reducing the replacement cost (time) of

unreliable components and increasing the reliability of components with large repair cost (time).

- **Replacement/Isolation Tradeoff-Data:** Provides the user with visibility into the overall testing picture for the UUT by calculating for each node in the diagnostic tree the expected repair time if the tree is followed and a complete replacement time.

- **Test Point Utilization Data:** Provides an expected number of times each test point appears in a given test strategy. This information is used to identify test points having low utilization and thus a smaller impact on ambiguity group sizes if they are removed. This analysis also identifies those test points not used for fault-isolation, the importance of which was explained in the description of STAT.

- **Test Point Criticality:** Provides a measure of aggregate criticality of the components associated with a given node in the test strategy. Every component has a criticality value (e.g., P {mission failure/ component failed and was not replaced prior to the mission}). The test point criticality is the sum of the component criticalities for those components that are isolated by each test point in the diagnostic strategy produced by WSTA. Test points with low criticality that are removed, have less impact on mission success since the larger ambiguities that result (from removal of a test point) are less critical.

3.2.2.2.4 Design for Testability (DFT) Recommendations

WSTA provides an analysis of the static and dynamic testability indicators and provides the user with a comprehensive set of recommendations for improving the testability of the UUT. The major recommendations provided are as follows:

- **Loop-Breaking Recommendations:** The optimal point to break each feedback loop, including an ordered list of alternatives.

- **Test/Test Point Recommendations:** Provides three types of recommendations:

  - Test/Test Point BIT Recommendations: Recommends a set of BIT tests/test points required to certify a UUT as being operational.

  - Test/Test Point Deletion Recommendations: Provides a list of tests/test points that are redundant in the current design.

  - Test/Test Point Addition Recommendations: Provides a list of those nodes that will, if made accessible as test points, improve the overall testability of the UUT.

3.2.2.2.5 Additional Information

WSTA is available free to any qualified government agency or government contractor. To obtain a copy of WSTA, contact Mr. Don Fromm at the following address:

SEA 04-DS2
Naval Sea Systems Command
Washington, DC 20362
Phone: (703) 602-2765

To obtain additional information on WSTA, contact Mr. Brian Kelly or Bob Pahl of Harris Corporation - GSSD at the following address:

6801 Jericho Turnpike
Syosset, NY 11791
Phone: (516) 677-3369

3.2.2.3 Intelligent-Computer Aided Troubleshooting (I-CAT)

I-CAT is a tool that was developed primarily as a model based expert system fault diagnostic aid. As such, I-CAT can be used in the following ways:

- Manual Bench-Top Testing - Directs a technician step-by-step in hands-on diagnosis. In this mode I-CAT acts like a master technician, telling the technician what to do next.

- Automatic Test Equipment (ATE)* - I-CAT can be connected to ATE, or other testing hardware, to direct the automatic testing in an optimal way.

- Diagnostic Fault Trees - I-CAT automatically produces diagnostic fault trees that can be used in both the design process and in maintenance.

- Testability Design* - I-CAT determines the number and placement of testpoints or sensors for optimal testability design. It can also determine where new testpoints and sensors need to be added, or where they are unnecessary.

- Automatic Source Code Generator* - I-CAT produces program shells in common computer languages including BASIC, C, PASCAL, etc., which can be used to develop software for stand-alone ATE applications.

- Technical Publications/Logistics - Documentation can be integrated within I-CAT so that technicians have the precise information required to test or repair a system available on-line.

The asterisked (*) items above are available only as optional advanced development tools.

3.2.2.3.1 The Basic I-CAT System

With the basic I-CAT System, referred to in the I-CAT User's Guide as the I-CAT Basic Development System, a user can build a dependency model of a system, subsystem, or component. The model built is a functional model that is created using a graphics package that is an inherent part of the I-CAT tool. An example of a functional block diagram created in I-CAT is shown in Figure 3-12.

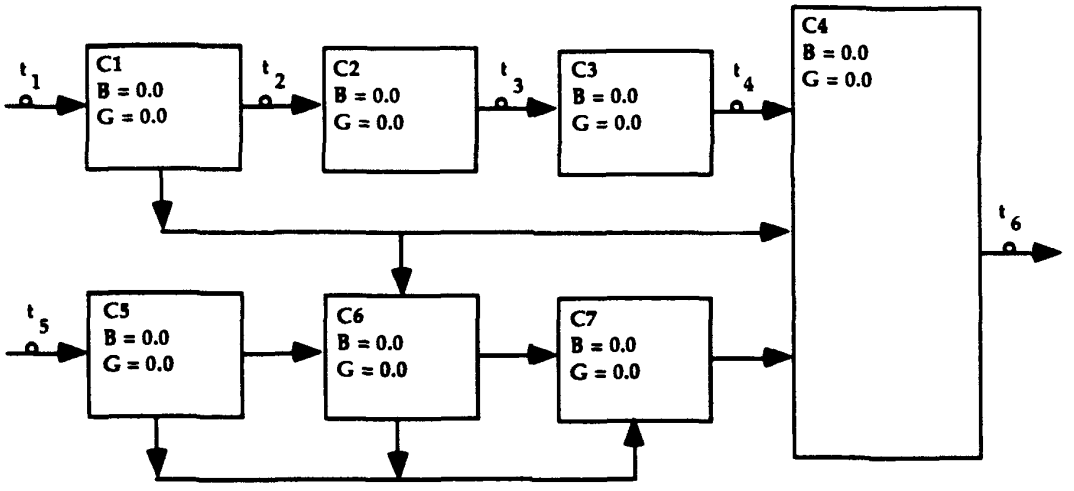


Figure 3-12: Example I-CAT Functional Block Diagram

Each box in the figure above is considered a module to which the following information can be added as weighting factors:

- Module Failure Rates
- Module Cost
- Module Retest OK (RTOK) Rates
- Testpoint Cost
- Module Substructure
- Supporting Text
- Supporting Pictures
- Expert Rules

The expert rules are added to the module using I-CATs rule editor.

3.2.2.3.2 I-CAT as a Testability Analysis Tool

Although I-CAT is primarily an expert diagnostic aid, it will produce testability data as part of its advanced development tools package. The following testability analysis data is output as part of the Fault Tree & Analysis Report:

- Average Cost To Diagnose
- Average Ambiguity Group Size

- Average Replacement Cost
- Unnecessary Testpoints
- Testpoints Required
- Feedback Loops

An example output of the Fault Tree Analysis Report is shown in Figure 3-13. Some general comments about the figure are:

- Although the figure shows feedback loops as none, I-CAT does identify all tests and components contained in a feedback loop.

- If all modes were accessible, additional testpoints required would be none. However, this does not necessarily mean that additional access to the system being analyzed is not required.

- I-CAT only prints out average ambiguity group size, but the actual groups and sizes can be taken from the fault tree printout. Therefore, if the user wants to compute fault resolution (i.e., % of time you can fault-isolate to n or fewer replaceable units (n = 1, 2, 3, . . .)) it must be done by hand.

- I-CAT can only recommend additional testpoints if they were originally defined when the model was created and then made "invisible," (or declared inaccessible), prior to running the Fault Tree & Analysis Report.

- It is assumed that if additional tests are required, the recommendation is based on the number of testpoints needed to achieve the lowest possible level of fault-isolation based on the model. It does not appear that one can pre-select the level of isolation and have I-CAT recommend what additional points are required to meet the pre-selected level.

```
FAIL:
    |     -Replace (UUT:input)
|   -Test:t1
|   |     |   -Replace (C1)
|   |     -Test:t6
|         |   -Replace (C8)
|   -Test:t2
|   |     -Replace (C2)
-Test:t3
|         |   -Replace (UUT:input)
|   |     -Test:t5
|   |     |   |   -Replace (C3)
|   |     |   -Test:t4:Frequency
|   |         |   |   -Dead-Replace (C3)
|   |         |   |   -High-Replace (C3)
|   |         |   |   -Low-Replace (C3)
|   |         |   Remove access cover:-
Test:t4:Voltage
|   |             |           |   -Replace (C9)
|   |             |       |   -Test:t20
|   |             |       |   |   -Replace (J21)
|   |             |   |   -Test:t19
|   |             |   |   |   |   -Replace (C5)
|   |             |   -Test:t15
|   |                 |           |   -Replace (C9)
|   |                 |       |   -Test:t20
|   |                 |       |   |   -Replace (J21)
|   |                 |   |   -Test:t19
|   |                 |   |   |   |   -Replace (C5)
|   |                 |   |   |   -Test:t14
|   |                 |   |       |   -Replace (C6)
|   |                 |   -Test:t22
t18, t17, t19, t20, t22, t23
|   |                     |           |   -Replace (C5)
|   |                     |       |   -Test:t23
|   |                     |       |   |   -Replace (J24)
|   |                     |   |   -Test:t18
|   |                     |   |   |   -Replace (C7)
|   |                     |   -Test:t16
|   |                         |       |   -Replace (C9)
|   |                         |   |   -Test:t20
|   |                         |   |   |   -Replace (J21)
|   |                         |   -Test:t17
|   |                             |   -Replace (C4)
|   -Test:Audio Out
    |     -UUT:ok

PASS:
```

Costs of Diagnosis:

Average:	24380.696
Variance:	415829718.633
Std. Deviation:	20391.903
Minimum:	2.000
Maximum:	50001.000

Replacement Costs:

Average:	22.522
Variance:	1667.467
Std. Deviation:	40.835
Minimum:	1.000
Maximum:	100.000

Ambiguity Group Size:

Average:	1.000
Std. Deviation:	0.000
Minimum:	1.000
Maximum:	1.000

Testpoints:
t3,t1,t4,t5,t2,t6, Audio Out
Used: Audio Out, t1, t2, t4, t5, t3, t6
Not Used: None
Additional Required: t14, t15, t16,

Feedback Loops: None

Figure 3-13: Example I-CAT Fault Tree & Analysis Report

3.2.2.3.3 Additional Information

The I-CAT program will run on the following hardware platforms:

1. Macintosh - Mac II Computers, System 6.0.2 or later. 4-8 Mbytes of memory recommended.

2. SUN Workstations - Any SUN 3 Computer, 8 Mbytes of solid state memory recommended.

3. APOLLO Workstations - Any APOLLO Computer, 8 Mbytes of solid state memory recommended.

4. UNIX 386/ix - Any Intel 386 computer running interactive 386/ix, 8 Mbytes of solid state memory is recommended, and a floppy drive and Version 2.0 or later of Interactive 386/ix, with X Window System is required.

For additional information on I-CAT and its capabilities as an expert diagnostic aid, contact:

Automated Technology Systems Corporation
25 Davids Drive
Hauppauge, NY 11788
Phone: (516) 231-7777
FAX: (516) 231-7075

3.2.2.4 System Testability and Maintenance Program (STAMP)

STAMP is a computer-aided tool for the analysis of system testability and the development of fault isolation strategies. It is based on the dependency model concept and provides a number of measures of system testability such as; guidance for re-design to improve testability, and detailed fault isolation procedures.

The information required by STAMP consists of a description of the system under study in terms of its components, inputs, tests, and their interdependencies. This information must be prepared by a person who has a working knowledge of the system to be analyzed.

3.2.2.4.1 STAMP Output Reports

STAMP performs two types of analyses that produce a testability report and a fault isolation strategy report. The testability report provides 24 normalized measures of system testability and their interpretation. It also provides tables of component ambiguities (components whose failures are indistinguishable given the current set of tests) and test point redundancies (tests that provide the same information). It also identifies functional feedback loops and identifies where re-design or additional tests would enhance testability.

More specifically, the following information is provided in a STAMP Testability Report:

- Basic Testability Measures:
  - Isolation level (IL)
  - Test leverage (TL)
  - Test uniqueness (TU)
  - Nondetection percentage (NDP)
  - Hidden failure measure (HFM)
  - False-failure measure (FFM)
  - False-alarm tolerance (FAT)
  - Maximum test leverage (TLMAX)
  - Minimum test leverage (TLMIN)
  - External dependency (EXDEP)
  - Excess-test measure (XM)

- Extended Testability Measures:
  - Feedback-modified isolation level (FMIL)
  - Nonredundant test leverage (NRTL)
  - Feedback-modified test leverage (FMTL)
  - Test redundancy (TR)
  - Test feedback dominance (TFBD)
  - Component feedback dominance (CFBD)
  - Input-modified hidden-failure measure (IMHFM)
  - Percent-hidden-failure measure (PHFM)
  - Input-modified percent-hidden-failure-measure (IMPHFM)

- Input-modified false-failure measure (IMFFM)
- Dependency (DEP)
- Test interdependency (TIDEP)
- Test dependency (TDEP)

The user can tailor each output report to include some, all,or none of the above measures, as not all of the measures will be relevant to each analysis. Most of the above measures are calculated based on a single failure assumption, except HFM, IMHFM, PHFM, IMPHFM, FFM, and IMFFM which are multiple failure testability measures. Each of the above measures is explained in detail in the STAMP User's Guide.

Additional information provided in the testability report is:

- **Operational Isolation to n Units** - represents the percentage of observed fault isolations that isolate to n replaceable units. This measure is equivalent to the MIL-STD-2165 measure for fault-resolution (FR) and is provided weighted or unweighted with component failure rates.

- **Component Ambiguity Table** - Provides in a tabular format all ambiguity groups, and components within, that will result for a defined number of tests.

- **Excess Tests** - Provides a list of excessive tests. Tests that may not be necessary to isolate faults in a system under the single-failure assumption are identified. Therefore, if 2 or more tests are listed together in this output, at least one of the tests is not required for fault-isolation. If excess tests exist, STAMP will provide an excess tests analysis and recommend elimination based on user criteria.

- **Feedback Loops** - Lists each feedback loop and all tests and components comprising the loop.

- **Test Redundancy Table** - Lists tests that are redundant to other tests. Therefore, if test A is redundant to test B, (i.e., test B provides identical information to test A) either one can be eliminated based on user criteria.

- **Subsignature Table** - Provides a list of possible hidden failures in a multiple-failure situation. An example of this table is shown below in Figure 3-14. In considering the table shown, if CP1 failed, that failure could mask any of the components listed. If components in the Failure Indicator column are preceded by an asterisk, this is an indication that if the listed hidden components were failed in certain combinations, such a situation could make the asterisked component look as if it has failed, resulting in a false failure indication.

- **Single-Failure Modified FMEA** - Provides a table showing all possible component failures in the system and lists each of the tests that will appear bad.

Subsignature Table

Failure Indicator	Hidden Components		
cp1	cp2	cp3	cp4
	cp5	cp6	
cp2	cp4	cp5	
cp3	cp4	cp5	cp6
cp4	cp5		
cp6	cp5		
ui1	cp1	cp2	cp3
	cp4	cp5	cp6

* Leading asterisk indicates a False Failure indication is possible

Figure 3-14: Example STAMP Subsignature Table

The STAMP testability measures and testability outputs provide enough data to allow the analyst to identify where testability needs to be improved through re-packaging, adding tests, or deleting tests.

STAMP also provides a fault-isolation strategy report that is an ordered list of tests to perform for fault diagnosis. The test order is optimized based on the dependency model itself, information theoretics, and user defined weighting criteria. The information theoretic algorithm used by STAMP provides an optimized test order. This adaptive fault-isolation strategy can be summarized as:

- For each test, how much information can be inferred from either a "good" or "bad" result?
- Select a test to optimize the answer to the above question.

STAMPs fault-isolation strategy can take into consideration the following factors:

- Test cost
- Test time
- Skill level
- Component failure rate
- User selected weights for tests and components
- Use of initial conditions (e.g., Provide a fault strategy based on known good, known bad, or known unavailable tests)
- Forced path inputs wherein the user specifies a test path (a list of tests to be performed sequentially) and STAMP builds a strategy around the path.
- Associated test groups (e.g., tests are grouped according to common set-up procedures, or physical locations)
- Associated component groups (e.g., the user may only want to isolate down to groups of components)

- Minimum RTOK path wherein STAMP creates the most efficient system verification path before proceeding to normal fault-isolation calculation.

In addition to test order, STAMP also produces in its fault-tree report: a component ambiguity table, summary statistics including maximum, minimum and average number of steps to fault-isolate, and tests not used for fault-isolation. An example STAMP fault-tree analysis report is shown in Figure 3-15.

3.2.2.4.2 Additional Information

STAMP takes as input a first-order dependency model comprising each defined tests and those components and other tests that immediately feed it. Most of the data is inputted manually to STAMP via a keyboard. STAMP is compatible however, with the Schema software package, a CAD program used to create schematics.

STAMP was originally written for an Apple Computer and then upgraded to run on an HP-1000/A-900 Computer. Recent efforts have been made for STAMP to run on IBM Compatible 386 PC's. RAC does not currently know what the minimum configuration requirements are for the HP-1000 or the soon to be released PC version.

For further information on STAMP, contact Mr. Randy Pizzi at the following address:

ARINC Research Corporation
2551 Riva Road
Annapolis, MD 21401
Phone: (301) 266-4000

Decision Tree Analysis
Component Ambiguity Groups

Group	Components			
1	cp5	(.5000)	cp8	(.5000)
2	cp3	(.3333)	cp7	(.3333)
	cp9	(.3333)		

Decision Tree Analysis
Fault Tree Table

Step	Test	Prev Step	Good	Bad
1	te6	0	Step 2	Step 5
2	te4	1	Step 3	Step 4
3	te8	2	No Fault (RTOK)	Comp Group 1
4	te3	2	cp4	cp2
5	te3	1	Step 6	Step 7
6	te4	5	cp6	Comp Group 2
7	te1	5	cp1	ui1

Decision Tree Analysis

Summary statistics

Isolation Sequences =	8
Maximum number of steps to isolate fault =	3
Minimum number of steps to isolate fault =	3
Average number of steps to isolate fault =	3.0000
Standard Deviation of Number Tests =	0.0000
Sum of Failure Frequencies for this tree =	0.000000

Fault tree choice criterion (Normal, Fast, Xtrafast) = Normal

These tests are available, but were not used in this tree:
te2 te5
te7

Figure 3-15: Sample STAMP Fault-Tree Analysis Report

3.2.3 Other Testability Analysis Tools

The additional tools described, that do not clearly fit into either of the preceding categories are: Computer Aided Fault Isolation and Testability (CAFIT), Advanced System Testability Evaluation Program (ASTEP), and APT Computational Environment - Alphatech program for Testability (ACE-APT).

3.2.3.1 Computer Aided Fault Isolation and Testability (CAFIT)

CAFIT was developed by ATAC Corporation for the U.S. Government and is a combination C/O based and dependency model based tool. It is primarily used to analyze digital PCB systems but allows the creation of analog components making it applicable to both. A system overview of CAFIT is shown in Figure 3-16.

CAFIT uses a net list produced from schematic capture software to produce a network model from which testability analysis can be performed. The software allows the creation of a device library that, for digital devices must contain pin, attribute, and logic data. Digital device attributes include name, number of devices per package, failure rate, etc. Analog devices are represented as pure topological models, (i.e., only inputs and outputs are represented, the function is not taken into account). CAFIT also allows the creation of A/D and D/A devices including a function table, as shown in Figure 3-17.

Once a schematic of the system is created and a net list generated, CAFIT processes the net list information and produces three specific testability analyses:

- Testability Inhibiting Factors
- Test Site Location Analysis
- Signal Coverage Estimation

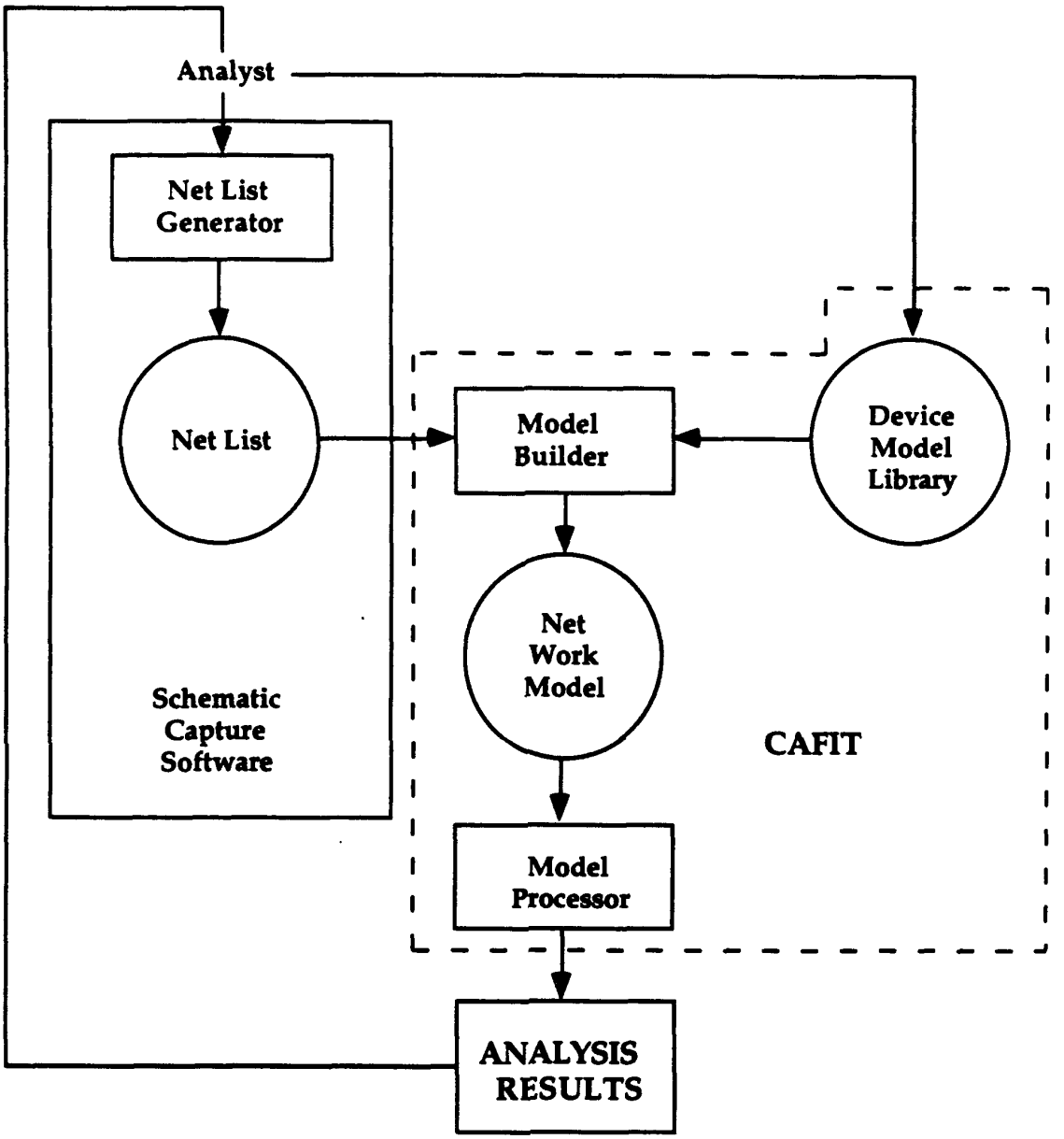


Figure 3-16: CAFIT System Overview

A/D

I1	O1	O2	O3	O4
A	H	X	X	X
A	L	X	X	X
A	X	H	X	X
A	X	L	X	X
A	X	X	H	X
A	X	X	L	X
A	X	X	X	H
A	X	X	X	L

ANALOG INPUT DIGITAL OUTPUT



D/A

I1	I2	I3	I4	O1
H	X	X	X	A
L	X	X	X	A
X	H	X	X	A
X	L	X	X	A
X	X	H	X	A
X	X	L	X	A
X	X	X	H	A
X	X	X	L	A

DIGITAL INPUT ANALOG OUTPUT

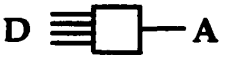
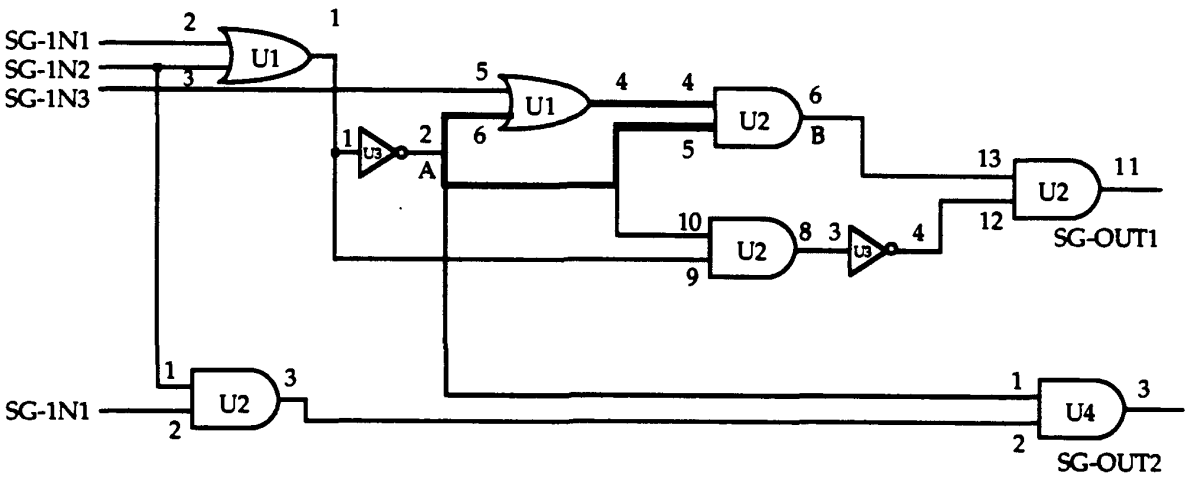


Figure 3-17: CAFIT Function Table for A/D and D/A Converters

3.2.3.1.1 Testability Inhibiting Factors

This analysis locates network logic and design elements that prevent fault detection including: feedback loops, negative reconvergence, and logic redundancy. Whenever it identifies feedback loops, CAFIT also produces a feedback loop report showing components within each loop and recommended feedback loop break points. In identifying negative reconvergence, CAFIT is able to do what other SCOAP based tools can't. An example of a reconvergent fan-out is shown in Figure 3-18. In this condition, a reconvergent fan-out causes the value of a pin to always be the same, thus inhibiting the ability to control the fan-in.



U1 SN5402J QUAD 2-INPUT POSITIVE-NOR GATE
U2 SN5408J QUAD 2-INPUT POSITIVE-NOR GATE
U3 SN5405J HEX INVERTERS
U4 SN5409J QUAD 2-INPUT POSITIVE-NOR GATE

Figure 3-18: Example of Logic Reconvergence

The logic redundancy report lists locations of logic redundancy in the schematic. An example is provided in Figure 3-19.

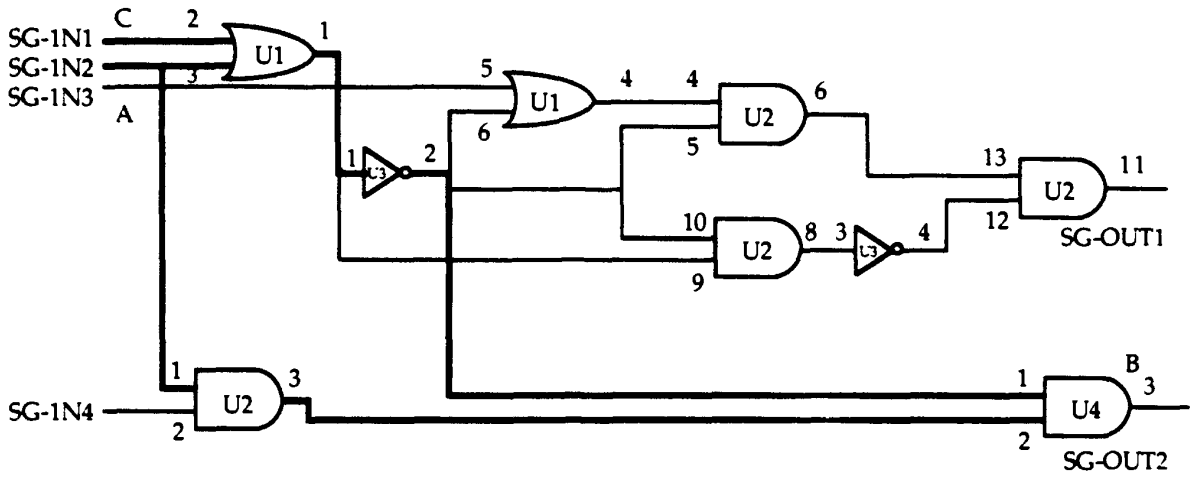


Figure 3-19: Example of Logic Redundancy

Figure 3-19 is another example of reconvergent fan-out, however in this condition, a reconvergent fan-out causes the value of the pin at fan-in to be dependent only on the value of the pin at the fan-out. This condition causes other signals that fan-in to the reconvergent logic to be redundant to the value at the fan-out.

3.2.3.1.2 Test Site Location Analysis

This analysis identifies optimal test sites, where the identified pin permits control or observations of the largest number of network devices. This analysis also takes into account the degree of controllability or observability permitted by the test sight with the complexity of the test programs required.

3.2.3.1.3 Signal Coverage Estimation

Using information from the previous analysis, this analysis calculates the extent to which a network is both controllable and observable.

3.2.3.1.4 CAFIT Reports

Some of the reports produced are described in the analysis descriptions above. A complete list of reports and outputs is provided below:

- Tied Low and Tied High Signal Report - Lists the total number of pin values set by "tied low" and "tied high" signals.

- Negative Reconvergence Report - See previous description.

- Logic Redundancy Report - See previous description.

- External Controllability Report - Shows the percentage of the network that can be controlled through network inputs as a whole, based on the maximum number of test signals specified and on designed-in test sites.

- Input Test Site List - Lists the optimal input test sites that contribute maximum controllability including number of pins controllable at each site.

- External Observability Report - Contains measures of network signal coverage for network outputs showing the percentage of the network that can be observed from each output.

- Output Test Site List - Lists the optimal output test sites that contribute to maximum network observability.

- Device Signal Coverage Report - Shows signal coverage or the percentage of stuck-at-faults in the device that can be tested for, including the location of the device.

- Feedback Loop Report - See previous description

3.2.3.1.5 Additional Information

The following minimum hardware/software requirements are needed to run CAFIT:

- IBM PC-AT or compatible with MS-DOS 3.X or higher
- 512K RAM

- 20 Mbyte hard disk drive recommended; CAFIT requires 2 Mbytes
- 1 double-density, 5.25 inch floppy disk drive
- EGA color graphics terminal card

To view analysis results in the form of color coded schematics, a CT-2000 workstation and schematic capture software is required. CAFIT is a government owned tool available to government employees and qualified government contractors. For additional information on CAFIT, contact

ATAC
1200 Villa Street
Mountain View, CA 94041
Phone: (415) 965-8801

3.2.3.2 Advanced System Testability Evaluation Program (ASTEP)

The ASTEP, produced by BITE Corporation, is more of a test effectiveness tracking system rather than a pure testability analysis tool. Written in Foxbase+™, ASTEP will run on any IBM XT, AT, 80386 or compatible computers with a minimum hardware requirement of 512K of memory and a hard disk.

In ASTEP, there are three kinds of input data to define a system: System Definition Data, Fault Quantum (FQ) Definition Data, and Test Coverage Estimates.

System Definition Data - Defines maintenance levels, hardware levels, repair times and system defaults. Hardware levels are used to define the system hierarchy when replaceable unit information is entered. There can be up to 8 levels of hardware. Maintenance levels refer to maintenance scenarios. Four different maintenance scenarios can be defined in ASTEP and for each scenario a particular hardware level is defined as the default replaceable unit.

Fault Quantum (FQ) Data - This data forms the actual model of the hardware to be assessed. A testability assessment, or test effectiveness assessment is provided for each particular FQ. A FQ can be an actual piece part including connector pins and cables, or a complete subsystem within a system. The FQ definition is also the means for relating the physical structure to the functional structure. FQ definitions

are hierarchical in nature, with each successive level a refinement of the level above. The primary data related to a given FQ is:

- Reference Designator (REFDES) - reference designators (up to eight levels) of the physical hardware
- Part ID/FBDID: a part ID of the hardware or the functional block diagram (FBD)ID.
- The failure rate of the FQ
- The fraction of the FQ that is built-in-test-equipment (BITE) hardware
- The fraction of the FQ that is mission essential
- The fraction of the FQ that is operational hardware

Test Coverage Estimate - This data comprises a test identification (Test ID), the FQ covered by the Test ID, and the probability of fault detection (PFD) of that test on the given FQ.

Other input data such as component failure rates and a part dictionary can also be entered into the database. From the FQ, TCE, and system definition data, the following reports are generated:

- Performance Report - There are several ways a performance report can be generated depending on the information one wishes to see. Reports are generated by the following specific identifiers: part ID, FQ, or test ID. The following kinds of information are listed in the report:
  - probability of fault detection
  - mean prioritized replacement position of the identifier
  - mean fault isolation group (FIG) replacement size
  - intrinsic test time to repair (ITTTR)

- total failure rate (FR) of a particular identifier
- detected failure rate (DFR) = total FR*PFD
- % BITE FR which is the percentage of BITE hardware as a percentage of total identifier FR.

- Replacement FIG Size Distribution Report - gives the distribution of the FIG list sizes for each hierarchy level and item identified (i.e., FQ, REFDES, or PARTID/FBDID). Information is presented cumulatively or discretely as the probability that the FIG replacement size is *N* (discrete) or *N* or less (cumulative) for each particular identifier.

- Prioritized Replacement Position Report - information can be provided for a FQ, REFDES or PARTID/FBDID. Information provided is the mean prioritized replacement position, and probability the replacement position of the identifier is *N* (discrete) or *N* or less ((cumulative).

- FIG List Report - Provides for each defined maintenance scenario a list of expected fault isolation groups, by REFDES, for each particular TESTID, including the detected failure rate (DFR) of the FIG, and the probability of a successful repair of each REFDES in a FIG which is equal to the DFR (of the individual FIG) divided by the DFR of all REFDES in the FIGs.

- Non-Detect Report - lists the percentage of failure rate in a FQ that is untested, and therefore, undetectable.

3.2.3.2.1 Additional Information

All of the examples used in the ASTEP demo package were of digital systems, but it appears that ASTEP is applicable to any type of system. The apparent limitations are that much of the input data, such as test coverage estimates and probability of fault detection, must be available for ASTEP to be most effective.

For additional information on ASTEP contact BITE, Incorporated at the following address:

9254 Center Street
Manassas, VA 22110
Phone: (703) 361-7050

3.2.3.3 APT Computational Environment - Alphatech Program for Testability (ACE-APT)

ACE-APT was developed under contract to the Army by Alphatech Incorporated and is based on the Time Efficient Sequencer of Tests (TEST) algorithm introduced by Alphatech at AUTOTESTCON '85. The program is mainly applicable to digital PCB-level systems, is based on failure modes, and it tries to emulate how a technician would diagnose a fault.

ACE-APT input is created as a block diagram by using schematic capture software that is custom-made by Alphatech to develop a block diagram of the system to be analyzed. Once the system is created, test points are added at applicable nodes, including test cost information, which is used to indicate accessibility to testing. The model created by ACE-APT from a schematic has "connectivity" information, but not dependency information as described in Section 2.2.

Additional information that can be entered includes failure modes for each box in the block diagram and failure rates.

Based on the model information, ACE-APT produces the following testability related reports:

- Tree - This report provides a diagnostic decision tree showing a test order for fault diagnosis. The report also includes a list of ambiguity groups that will occur for a given set of tests.

- Cost QA - Provides a component group histogram with the size of the ambiguity groups and number of occurrence, total expected test

cost per diagnostic session, and the number of tests in a RTOK or "go chain".

- Cost DFT - Provides a list of failure modes that are in ambiguity groups. If only one failure mode is entered per function block, this list will match the list provided in the TREE report. This output also lists how much each test point is used and which test points are not used at all.

3.2.3.3.1 Additional Information

At last report, ACE-APT had not yet been completely released for general use within government agencies but was expected to be very soon. For information on this tool contact Alphatech Incorporated at:

111 Middlesex Turnpike
Burlington, MASS 01803
Phone: (617) 273-3388

APPENDIX A

The following is an excerpt from Technical Report RADC-TR-79-327 entitled "An Objective Printed Circuit Board Testability Design Guide and Rating System" prepared by Grumman Aerospace Corporation for the Rome Air Development Center dated January 1980. It is reprinted here for the purpose of providing the reader with a means to implement the scoring technique on their own design.

1.0 PCB-TESTABILITY EVALUATION SYSTEM

The Testability Evaluation System rates PCBs in terms of four basic test factors and 30 negative testability factors. Basic test factors define a score on a positive scale of 0 to 100%. This represents how closely the generic design of the PCB approaches optimum testability. The negative testability factors are penalties for bad design practices. The total negative score is subtracted from the total positive score to produce a net total score. The net total score is the measure of PCB testability.

Negative factors can usually be reduced by the designer using the testability design methods recommended in this guide. The process used to identify and correct testability problems is based on objective mathematical standards. The rating process is designed to require less than eight working hours per PCB evaluated. The evaluation system takes into account known factors relating to the cost of testing. Automatic testing considerations and proper documentation are also key inputs to the evaluation process.

Examples of remedial testability design methods are divided into five main areas; circuit structure (with sequential circuit and ATG factors), special parts (microprocessors, memories, VLSI, etc.), documentation, power application, and miscellaneous (tolerance, adjustments, high frequency, fail safe, mechanical, etc.). In each area, specific design corrections are recommended to reduce the difficulty of testing.

1.1 Use of the PCB Testability Evaluation System

When initiating a testability evaluation, the following is mandatory:

- Schematic/logic diagram
- Parts list
- Specifications and internal logic of all PCB parts
- All documents must be legible
- Configuration of the PCB and its documents must be clearly stated and identical.

Do not proceed with the evaluation unless all of the above items are present and accounted for.

The following provides a step-by-step procedure to conduct a PCB testability evaluation. The evaluator will require the following:

- A Node Accessibility Score Sheet (Figure A-1)
- The PCB Testability Evaluation Score Sheet (Figure A-2)
- The PCB Testability Evaluation System (Subsection 4.4)

1.2 Compilation of Basic (Positive) Factors

Step 1: Use the Node Accessibility Score Sheet (Figure A-1) and the schematic/logic diagram, to trace each primary input lead to all its termination points in the circuit. Place a mark in the score sheet box for each case which corresponds to the number of components tied to that lead under the appropriate column in the top half (Access) part of the form. When five or more parts are connected to a single input, circle that input lead on the schematic with a red pencil. Put a pencil check on each termination point so the same path will not be retraced later. Group the marks made in the numbered boxes by multiples of five or ten to make counting up the total easy.

Step 2: Repeat Step 1 for each output lead.

Step 3: Count the number of parts connected to each internal node (wiring junction point) and place a mark in the score sheet box which represents the number of parts connected to each node. (Since the internal nodes are inaccessible, these marks are made on the lower half of the form). When four or more parts are connected to the same node, circle the node at a convenient point with a red pencil. Place a pencil check on each termination point to prevent retracing the line later.

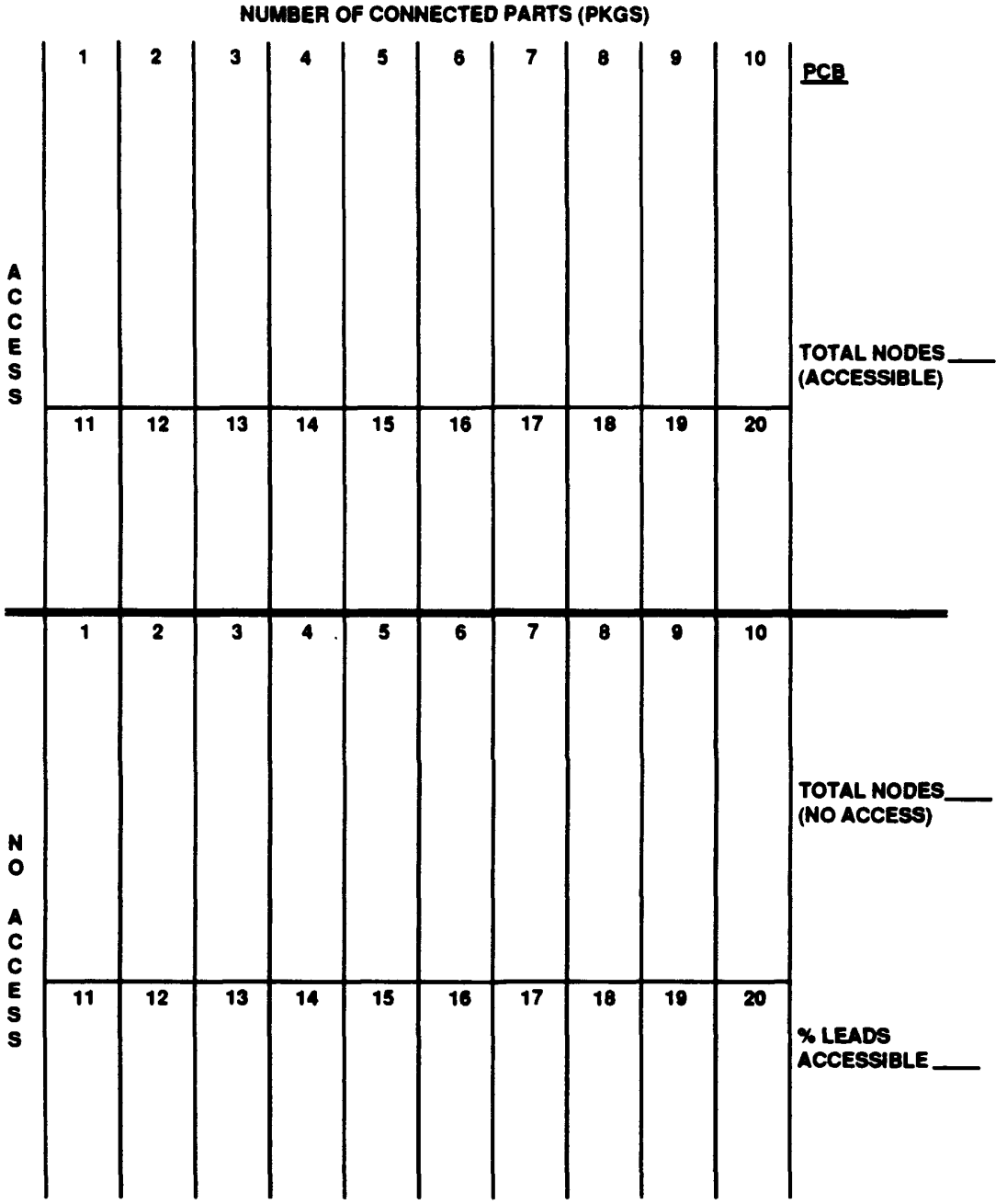


Figure A-1: Node Accessibility Score Sheet

FACTOR	DESCRIPTION	SCORE	POSSIBLE RATING	ACTUAL RATING	COMMENTS
B1	Percent Nodes Accessible		30%		
B2	Proper Documentation		25%		
B3	% of Sequential Ckts		25%		
B4	PCB Complexity Count		20%		
	Total Basic Score		100%		
N1	Monostable Ckt		-%/Inst		
N2	Counters (Pkgs x Stgs)		-%/Inst		
N3	Max. No. Function Blocks/ Node (No Access)		-%/Inst		
N4	Max. No. Function Blocks/ Node (Accessible)		-%/Inst		
N5	Seq. Supply Voltages		-10%		
N6	Non-Remov. Memories		-%/Inst		
N7	Non-Rem. Buried Memory		-%/Inst		
N8	Removable Complex Part		-%/Inst		
N9	Non-Rem. U-Proc. VLSI		-10%/Inst		
N10	Init. of Seq. CKTS		-%/Inst		
N11	Ext. Loading Req'd		-5%		
N12	Different Logic Types		-%/Inst		
N13	Buried Seq. Logic		-%/Inst		
N14	I/O Pins Distinguished		-3%		
N15	Excess Warm-up Time		-3%		
N16	Tolerance		-%/Inst		
N17	High Power		-%/Inst		
N18	Critical Frequency		-5%		
N19	Clock Lines		-20%		
N20	Ext. Test Equipment		-%/Inst		
N21	Environmental		-10%		
N22	Adjustments		-%/Inst		
N23	Complex Signal Inputs		-%/Inst		
N24	Redundant Logic		-%/Inst		
N25	No. of Logic Voltages		-1%/L.V.		
N26	No. of Power Supplies		-1%/P.S.		
N27	Schematic Connectives		-20%		
N28	I/O Pin - Schematic		-5%		
N29	Dual Pin Designations		-3%/Inst		
N30	Symbols on Schematic		-5%		
	Total Negative Score				
	Net Total Score				

Figure A-2: PCB Testability Evaluation Score Sheet

The procedure will refer to the above as needed in the evaluation.

Step 4: Total up the number of "Accessible" nodes and record their number in the Nodes Accessible blank of the Score Sheet.

Step 5: Total up the number of "No Access" nodes excluding those which connect only one or two parts. Record this total in the Node Inaccessible blank on the Score Sheet.

Step 6: Calculate the percent of nodes accessible:

$$\% \text{ nodes accessible} = \frac{\text{Total Count - Step 4}}{\text{Total Current - Step 4 \& Step 5}} \bullet 100\%$$

Record this result on the Score Sheet. Also, enter this result on the PCB Testability Evaluation Score Sheet (Figure A-2) as the score for the first rating factor. Convert this score to an actual rating by using the PCB testability evaluation system (Subsection 4.4) which converts the raw score to a weighted percentage. Enter the weighted percentage in the rating column of the PCB Testability Evaluation Score Sheet.

Step 7: Proceed to Factor B2 of the PCB Testability Evaluation System (Subsection 4.4) and total up the percentage points for documentation items (a) through (f). Points are awarded if requirements are met or exceeded. Enter total percentage in actual rating column of PCB Testability Evaluation Score Sheet.

Step 8: Proceed to Factor B3 of the PCB Testability Evaluation System (Subsection 4.4). Using the PCB parts list, add up the total number of sequential IC packages. Divide the number of sequential packages by the total of all IC packages. (If discrete parts are used on the PCB, only count functional groups of discretes as equivalent to one IC). Score Sequential Groups and Combinational Groups in appropriate areas. Enter the percent of sequential circuits in the "Score" column of the Score Sheet and convert this value using Subsection 4.4 scale factors to get the actual percentage rating. Enter actual percentage on the Score Sheet.

Step 9: Using the B4 instructions of Subsection 4.4, add up the total counts of all sequential circuit parts. Convert this total count to an actual rating percentage using the table in Subsection 4.4. Enter this actual percentage on the Score Sheet.

Step 10: Add the actual ratings for Basic Factors B1 through B4 to arrive at the "Total Basic" score and enter this on the Score Sheet.

1.2.1 Complication of Negative Factors

Step 11: Check PCB to see if there are any monostable circuits. Assess how these must be tested, and assign appropriate penalties as per the N1 section of the PCB Testability Evaluation System (Subsection 4.4).

Step 12: Using the N2 factors of the PCB Testability Evaluation System, evaluate possible penalties and make the appropriate entries on the Score Sheet. Counters are considered accessible if a signal can be directly input. The count of stages starts from each direct input and continues until the final stage of the counter is reached, or until a point where another input can be injected is reached. If there are test points within the counter, the penalty is reduced (see N2 (a) and (c) factors).

Step 13: Using the filled out Node Accessibility Score Sheet, add up the total instances of inaccessible (bottom half of chart) nodes for groups of 4, 5, 6, ---N packages separately by group. Using the PCB Testability Evaluation System assign penalties shown for each group and add the total negative points. Record this total on the Score Sheet under N3.

Step 14: Repeat the Step 13 procedure for all accessible nodes with 5 or more packages tied together. Record this result on the Score Sheet for N4.

Step 15: For factors N5 through N9, assign penalties if undesirable design factors are present and enter these in the appropriate places on the Score Sheet. Show 0% if a factor is not a problem to indicate that each factor was considered.

Step 16: Check each sequential circuit to see if it can be initialized in two ways; using the direct set/reset inputs, and using signal input patterns with a clock line. Penalize (per the Evaluation System) in each case where initialization cannot be accomplished in two ways, and enter these under N10.

Step 17: For factors N11 and N12 assign possible penalties and enter results on Score Sheet.

Step 18: For N13 start with any sequential circuit (count of 1) and count each sequential stage directly connected to one of its inputs or to one of its outputs. If an output lead from an otherwise unconnected sequential circuit is connected to the clock input of a sequential circuit in the above cluster, it should also be counted. Expand the count in all directions until all signal leads from all circuits in the cluster reach combinational circuits or a PCB input/output lead. Assess penalties for each cluster of three or more sequential circuits as shown in the Evaluation System. Continue this process until all sequential circuits have been checked. Total up and record the penalty in the Score Sheet.

Step 19: For factors N14 through N30 assign possible penalties as per the Evaluation System and record the results on the Score Sheet.

Step 20: Total up all negative percentage points and record the total negative score. Subtract the total negative score from total basic score to obtain the final PCB rating.

1.2.2 Relationship of PCB Rating to Actual Test Difficulty

In order to determine how the final PCB Testability Rating correlates with actual difficulty-to-test, the average rating limits for typical PCBs are presented below:

PCB Rating	Circuit Test Difficulty
+81% to +100%	Very easy
+66% to +80%	Easy
+46% to +65%	Medium/Easy
+31% to +45%	Medium
+11% to +30%	Hard
+1% to +10%	Very Hard
-100% to 0%	Impossible to test without extreme cost penalties

1.3 PCB Testability Evaluation Scoring System

1.3.1 Basic Factors

B1 - Percent of Nodes Accessible

An accessible wiring node is one which is connected to an external connector pin.

Percent Accessible Nodes	Actual Rating (%)
(a) 91 to 100	(30)
(b) 81 to 90	(27)
(c) 71 to 80	(24)
(d) 61 to 70	(21)
(e) 51 to 60	(18)
(f) 41 to 50	(15)
(g) 31 to 40	(12)
(h) 21 to 30	(8)
(i) 11 to 20	(4)
(j) 0 to 10	(0)

B2 - Proper Documentation

1) Mandatory Requirements

a) Schematic/Logic Diagram provided
b) Parts List provided
c) Equivalent logic diagrams of all integrated circuit parts
d) All documents must be legible
e) Configuration of the Schematic/Assembly Group must be clearly stated

2) Basic Items	Actual Rating (%)
a) Logic diagrams or schematics (of all detailed parts) provided either on overall print or as individual part specs	4
b) Detailed performance spec with signal I/O tolerance provided	8
c) Truth table for each digital IC circuit type shown on schematic or on detailed part drawing provided	3
d) Functional designations should be shown next to each pin number of all logic packages on the schematic	5
e) Power circuits shown in a single location on the schematic and with voltages labeled	3
f) Schematic shows reference to corresponding assembly print and part number of next higher assembly	2

B3 - Percent of Sequential Circuits

Each integrated circuit package on the schematic is counted as a single sequential or combination circuit regardless of its individual complexity.

Percent of Sequential Circuits	Actual Rating (%)
(a) < 15%	25
(b) ≥ 15 but < 25	20
(c) ≥ 25 but < 40	10
(d) ≥ 40 but < 50	5
(e) ≥ 50	0

B4 - Complexity Count

The complexity count is made for sequential circuits only. Combinational ICs are ignored. Use the following list to determine the total count for each type of circuit configuration.

Total Counts

a)	Flip Flop	7
b)	Latch	7
c)	4-BIT Shift Register	35
d)	Memory Chip	2^n (n = number of inputs)
e)	Microprocessor	1,000
f)	VLSI Chip	1,000
g)	All other sequential ICs	See Notes 1 and 2

PCB Complexity Count		Actual Rating (%)
a)	Less than 300	20
b)	301 to 500	16
c)	501 to 800	12
d)	801 to 1200	8
e)	1201 to 1800	4
f)	1801 and higher	0

Note 1: For complex IC circuits with sequential sections, add the count of internal combination gates and inverters to the total based on:

- Gate = number of input leads plus one
- Inverter = 3

Note 2: Total count for other sequential ICs is determined by summing the counts of each internal gate with the counts of logic types (a) through (e) above

1.3.2 Negative Factors

N1 - Monostable Circuits

Classify each monostable into one of the three categories listed below and assess the appropriate scoring penalties.

	Scoring Factors	Actual Rating (%)
a)	Is tested by analog techniques not requiring digital ATG processing	(-1) per instance
b)	Accessible monostable output driving sequential circuits	(-2) per instance
c)	Inaccessible monostable output driving sequential circuits	(-5) per instance

N2 - 2^n Sequential Counters

Multiply the number of IC packages by the number of internal sequential stages. The scoring factor is equal to the product. Stop count when a combinational circuit is reached.

	Scoring Factors	Actual Rating (%)
a)	5 to 10 with monitor lead only	(-2) per instance
b)	5 to 10 not accessible	(-3) per instance

c)	10 or more with monitor lead only	(-4 plus (-0.05(N-10)) per instance
d)	10 or more not accessible	(-5 plus (-0.1 • (N-10)) per instance

N3 - Maximum Number of Function Blocks per Inaccessible Node

Count the number of different function blocks (circuit packages) connected to the same wiring junction (node). This procedure pinpoints areas of the circuit design where high internal fanouts make fault isolation difficult.

Inaccessible Nodes	Actual Rating (%)
a) 4	(-0.1) per instance
b) 5	(-0.2) per instance
c) 6	(-0.5) per instance
d) 7	(-1.0) per instance
e) 8	(-1.3) per instance
f) 9	(-1.7) per instance
g) 10 and higher	(-2.0) per instance

N4 - Maximum Number of Function Blocks per Accessible Node

Same procedure as N3 but with smaller penalties for high fanout.

Accessible Nodes	Actual Rating (%)
a) 5	(-0.1) per instance
b) 6	(-0.2) per instance
c) 7	(-0.5) per instance
d) 8	(-0.6) per instance
e) 9	(-0.8) per instance
f) 10 and higher	(-1.0) per instance

N5 - Supply Voltage Sequencing Requirements

Two or more supply voltages which require a turn-on and/or turn-off sequence. Assess a -10% penalty for any PCB with this requirement.

N6 - Non-removable Memories (I/O leads accessible)

Any type of memory permanently wired to the PCB with all I/O leads accessible.

Memory Size (BITS)	Actual Rating (%)
a) 100K and over	(-10) per instance
b) 32K to 99K	(-6) per instance
c) 8K to 31K	(-4) per instance
d) 1K to 7K	(-2) per instance

N7 - Non-removable Buried Memory

Any memory permanently wired to the PCB with one or more of its leads not connected to I/O pins.

Memory Size (BITS)	Actual Rating (%)
a) Under 1K	(-5) per instance
b) $\geq$ 1K	(-10) per instance

N8 - Removable Complex Part

If the part is mounted in a socket or the equivalent and must be extracted prior to test access a -1% penalty per instance.

Scoring Factors	Actual Rating (%)
a) All leads accessible to I/O pins	(-3) per instance
b) One or more leads not accessible to I/O pins	(-10) per instance

N9 - Non-Removable Microprocessor, VLSI Chip or Other Complex Parts

Scoring Factors	Actual Rating (%)
a) All leads accessible to I/O pins	(-3) per instance
b) One or more leads not accessible to I/O pins	(-10) per instance

N10 - Initialization of Sequential Circuits

Sequential circuits should be resettable from an external connector pin (either set or reset) and by applying a digital stimulus of less than 16 patterns to the PCB. Penalties are assessed if either type of reset is absent, and a severe penalty is given for no reset capability.

Scoring Factors	Actual Rating (%)
a) Direct set and <16 pattern reset	No penalty
b) Direct set but no pattern reset	(-0.05) per instance
c) No direct set but <16 pattern reset	(-0.1) per instance
d) No direct set and ≥16 pattern reset	(-2) per instance

N11 - External Loading Required

Components which must be added to the ID to perform test (e.g., pullup resistors).

Scoring Factors	Actual Rating (%)
a) 10 resistive loads	(-2)
b) 50 and over resistive load	(-3)
c) > 5 Reactive Loads	(-5)

N12 - Diversity of IC Type Numbers

Scoring Factors	Actual Rating (%)
a) 7 types	No Penalty
b) 10 types	(-1)
c) > 10 types	(-1) for each additional 3 types

N13 - Buried Sequential Logic

Do not count 2^n buried counters under this step.

Scoring Factors	Actual Rating (%)
a) Cluster of 3 or 4 sequential circuits	(-0.1)
b) Cluster ≥ 5	-0.2 [1 + (N-5)] per instance

N14 - Input - Output Pins Distinguished on Schematic

This makes tracing of signal paths easier.

Scoring Factors	Actual Rating (%)
a) Direction arrows not different for input pins versus output pins	(-3)

N15 - Excess Warm-up Time

Time required to stabilize card should not exceed 3 minutes.

Scoring Factors	Actual Rating (%)
a) Over 3 minutes	(-3)

N16 - Tolerance (Perform if information on test equipment is known)

Scoring Factors	Actual Rating (%)
a) Measurement capability at least 10 times more accurate than PCB requirement	No penalty
b) Measurement capability 3 times more accurate than PCB requirement	(-2) per instance
c) Measurement capability less than 3 times more accurate than PCB requirement	(-5) per instance

N17 - High Power

Scoring Factors	Actual Rating (%)
a) More than 5 amps of current required	(-5) per instance
b) High voltage >300Vpp	(-2) per instance
c) Multiple parallel pins for high current	(-1) per instance

N18 - Frequency Critical

Scoring Factors	Actual Rating (%)
a) Requires co-ax in ID	(-5)
b) Over 10 MHz	(-3)
c) Over 4 MHz	(-2)
d) Over 1 MHz	(-1)

N19 - Clock Lines

Scoring Factors	Actual Rating (%)
a) One, externally controlled	(-1)
b) Multiphase, externally controlled	(-2)
c) Single clock, monitor only	(-3)
d) Multiple clocks, monitor only	(-5)
e) Inaccessible free-running clock	(-20)

N20 - External Test Equipment

Test equipment other than that contained in the automatic test equipment.

Scoring Factors	Actual Rating (%)
a) 2 Power supplies or more	(-2)
b) Oscilloscope	(-2)
c) Function Generator	(-4)

N21 - Environmental

Special chambers or areas required to perform test.

Scoring Factors	Actual Rating (%)
a) Forced air, ambient or chilled	(-2)
b) Heat, altitude, EMI (chamber)	(-10)

N22 - Adjustments

Trimpots, variable caps, etc.

Scoring Factors	Actual Rating (%)
a) per instance	(-2)
b) per interactive adjustment	(-4)

N23 - Complex Signal Inputs/Outputs

Signals where interpretation by the test operator is required where complex or non-periodic waveshapes are used.

Scoring Factors	Actual Rating (%)
a) 2 coincident unusual wave forms	(-5 per instance)
b) 1 unusual wave form	(-2 per instance)

N24 - Redundant Logic

Logic which because of being in parallel prevents fault isolation and/or detection of individual logic failures. No penalty if built-in-test permits fault isolation of redundant elements.

Scoring Factors	Actual Rating (%)
a) 2 parallel logic functions - inseparable	(-2) per instance
b) 3 and over parallel logic functions -	(-3) per instance inseparable

N25 - Number of Logic Voltages

Scoring Factors	Actual Rating (%)
a) 4	No Penalty
b) > 4	(-1 per logic voltage)

N26 - Number of Power Supplies

Number of separate power supplies which must be supplied by the test station.

Scoring Factors	Actual Rating (%)
a) 3	No Penalty
b) > 3	(-1 each additional supply)

N27 - Connectives for Schematic Diagram

The aim of this factor is to guarantee that the schematic/logic diagrams do not impose hardship on the test design engineer.

Scoring Factors	Actual Rating (%)
a) Schematic on single page	No Penalty
b) If schematic on multiple pages with connecting leads between pages - then all interpage connectives are numbered showing other page numbers and zones	No Penalty
c) If neither a) or b) conditions are met	(-20)

N28 - I/O Pins on Schematic

I/O pins located in the center of prints cause extra work for test designer.

Scoring Factors	Actual Rating (%)
a) All I/O pins not brought to edges of schematic diagram or to a common dotted line	(-5)

N29 - Dual I/O Pin Designation

Scoring Factors	Actual Rating (%)
a) If dual designation of an I/O pin is in different areas of print with no cross reference	(-3) per instance

N30 - Logic Symbols on Schematic

Only a single symbol should be used to describe a specific hardware part. Multiple symbols for identical parts make it difficult to check ATG bit propagation and to design key manual patterns to supplement tests.

Scoring Factors	Actual Rating (%)
a) IC Logic Symbols used are not identical to detail part drawing symbols	(-5)

APPENDIX B:

REFERENCES

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APPENDIX C:

RAC PRODUCTS

RAC Product Order Form

		U.S.	Non-U.S.	Qty	Item Total
RELIABILITY HANDBOOKS					
RMST-91	Reliability and Maintainability Software Tools 1991	50.00	60.00		
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RDSC-1	Reliability Sourcebook	25.00	35.00		
MFAT-1	Microelectronics Failure Analysis Techniques - A Procedural Guide	140.00	180.00		
MFAT-2	GaAs Characterization and Failure Analysis Techniques - A Procedural Guide	100.00	130.00		
MFAT 1&2	Combined set of MFAT-1 and MFAT-2	200.00	300.00		
FTA	Fault Tree Analysis Application Guide	80.00	90.00		
NPS-1	Analysis Techniques for Mechanical Reliability	60.00	70.00		
PRIM-91	A Primer for DoD Reliability, Maintainability and Safety Standards	120.00	140.00		
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DSR-4	Discrete Semiconductor Device Reliability - 1988	100.00	120.00		
FMD-91	Failure Mode Distribution Critical Technology Review Assessment	100.00	120.00		
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