

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP USA, INC.,
Petitioner,

v.

BELL SEMICONDUCTOR, LLC,
Patent Owner.

IPR2024-00168
Patent 7,345,245 B2

Before JEFFREY W. ABRAHAM, JOHN D. HAMANN, and
BRIAN D. RANGE, *Administrative Patent Judges*.

RANGE, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

NXP USA, Inc. (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–12 of U.S. Patent No. 7,345,245 B2 (Ex. 1001, “the ’245 patent”). Paper 1 (“Pet.”). Bell Semiconductor, LLC (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). Patent Owner disclaimed claims 7 and 9–12. Prelim. Resp; 2, Ex. 2002.

Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in the petition “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” The following findings of fact and conclusions of law are not final, but are made for the sole purpose of determining whether Petitioner meets the threshold for initiating review. Any final decision shall be based on the full trial record, including any response timely filed by Patent Owner. Any arguments not raised by Patent Owner in a timely-filed response may be deemed waived.

For the reasons stated below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one claim. We hereby institute an *inter partes* review as to claims 1–6 and 8 of the ’245 patent based upon Petitioner’s asserted grounds of unpatentability.

II. BACKGROUND

A. *Real Parties in Interest*

Petitioner identifies itself as the real party in interest, as well as NXP Semiconductors N.V., NXP B.V., and Freescale Semiconductor Holdings V, Inc. Pet. 1. Patent Owner identifies itself as the real party in interest, as well as Hilco Patent Acquisitions 56, LLC; Hilco IP Merchant Capital, LLC;

Hilco, Inc.; Vulcan Ventures Inc.; CDPQ Investments (U.S.) Inc.; and KLIM AIV, LP. Paper 5, 1.

B. Related Matters

The parties identify the following matter as related to this proceeding: *Bell Semiconductor, LLC v. NXP USA, Inc.*, No. 8:22-cv-02133-HDV-ADS (C.D. Cal.) (filed Nov. 23, 2022). Pet. 1; Paper 5, 1.

C. The '245 patent

The '245 patent, titled “Robust High Density Substrate Design for Thermal Cycling Reliability,” issued March 18, 2008, with claims 1–12. Ex. 1001, codes (45), (54), 4:10–65. The '245 patent generally relates to a “semiconductor package for a die with improved thermal cycling reliability.” *Id.* at code (57).

The '245 patent explains that “[r]ecent silicon technology advances have placed increased demand for high density signal routing on organic BGA [ball grid array] substrates,” and that “[p]ackages with a full area ball array are also being used to reduce the package body size and provide a high input/output (IO) signal density.” *Id.* at 1:7–12. The patent notes that “an improved package is needed which will reduce cracks in the signal traces and therefore avoids functional failures caused by stresses under the die corner.” *Id.* at 2:16–18. Specifically, the '245 patent discloses “an improved package in which a high stress area associated with the die corner is defined and in which the signal traces are routed away from the high stress areas at the die corner.” *Id.* at 2:32–36.

Figure 4, reproduced below, is a diagram of a portion of a substrate package from above.

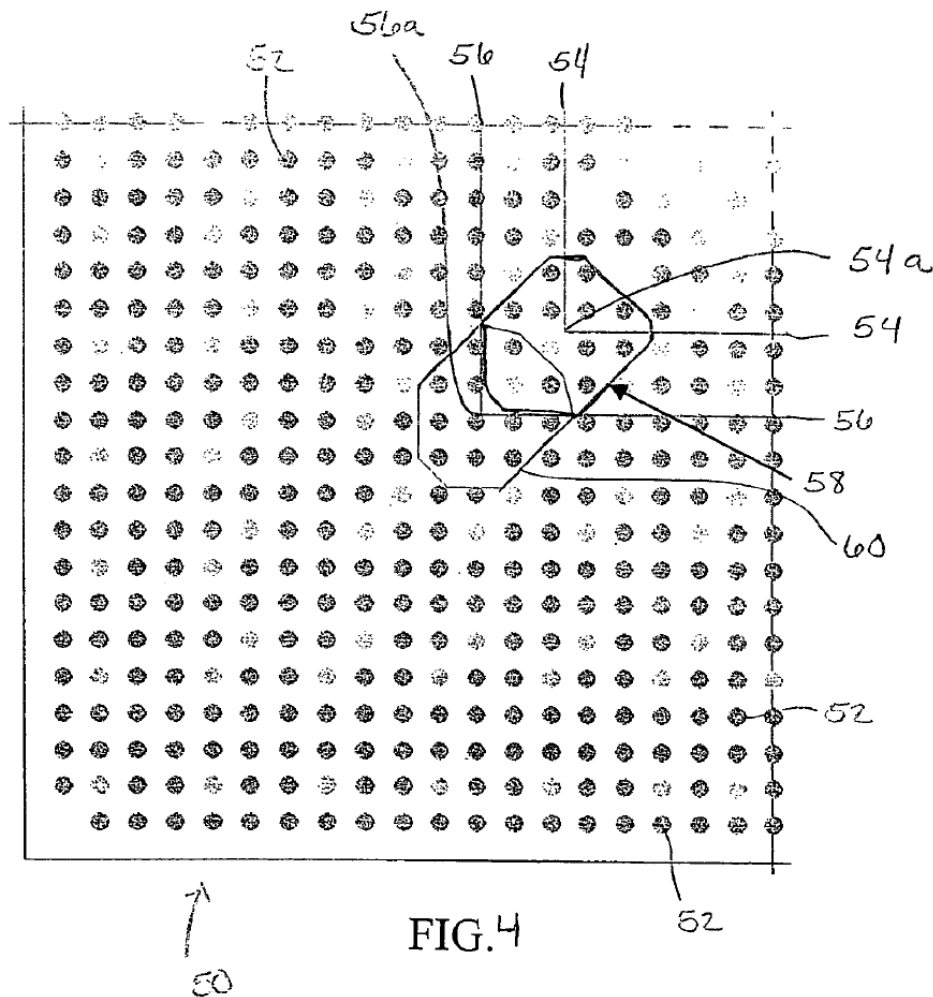


FIG. 4

Figure 4 illustrates L9 layer 50, of a 9-layer stackup, ball pads 52, lines 54 and 56, corners 54a and 56a, and high-stress zones 58 and 60. *Id.* at 3:10–22. A portion of high stress zone 58 overlaps a portion of high stress zone 60. *Id.* at 3:23–24. The '245 patent discloses that the “high stress zone 58 extends approximately two ball pitches away from the die corner 54a in each direction,” and the “high stress zone 60 extends approximately two ball pitches away from the die corner 56a in each direction.” *Id.* at 3:24–28. In addition, “[s]everal ball pads 52 are provided within the high stress zone 58 and several ball pads are provided within the high stress zone 60.” *Id.* at 3:28–30.

Referencing Figure 5 (not reproduced here), the '245 patent discloses that “[s]ignal traces 64 and other metal structures are provided throughout layer L8, however, within the high stress area 58, the signal traces 64 and other metal structures, for example, voltage bus bars, are routed away from the die corner 54a.” *Id.* at 3:39–43. Therefore, according to the '245 patent, “[b]ecause the signal traces 64 and other metal structures are not provided over the ball pads 52, cracks initiated from the ball pad edges during thermal cycling do not affect the traces 64 and other metal structures and therefore thermal cycling reliability of the package is improved.” *Id.* at 3:55–59.

D. Illustrative Claims

Claims 1, 7, and 8, reproduced below with Petitioner’s annotations, are illustrative. Patent Owner filed a statutory disclaimer of claims 7 and 9–12. Ex. 2002. Challenged claims 2–6 depend from claim 1. Challenged claim 8 depends from disclaimed independent claim 7. *See* Ex. 1001, 4:10–65. We reproduce claims 1, 7, and 8 below while modifying the formatting to match Petitioner’s use of lettering (a, b, c, d) to identify different portions of the claims.

- 1a) A semi-conductor package comprising:
 - a top layer having a die mounted thereon, said die having a corner; and
 - b) a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces thereon,
 - c) and a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads,
 - d) wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die.

- 7a). A semi-conductor package comprising:
a top layer having a die mounted thereon, said die having a corner defining a surrounding area of increased stress;
and
b) a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces thereon,
c) and a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads dispersed thereon,
d) wherein none of the signal traces of the bottom routing layer are located within the area of increased stress defined by the corner of the die.
- 8a) A package as recited in claim 7, wherein none of the signal traces of the bottom routing layer are located within two ball pad pitches of the corner of the die.

Ex. 1001, 4:10–20, 4:38–51; Pet. 17, 27, 36.

E. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability (Pet. 2–4) and cites the declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 1002) for support:¹

Petitioner Ground #	Claims Challenged	35 U.S.C. §	References/Basis
1	7, 8, 10, 11	103(a) ²	Devnani ³ , AAPA ⁴

¹ The relevant sections of the Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, took effect on March 16, 2013. The ’245 patent was filed before this date. *See* Ex. 1001, code (22). For the purposes of this Decision, pre-AIA statutes apply.

² We do not address disclaimed claims 7, 10, and 11.

³ US 2003/0183919 A1, published Oct. 2, 2003, Ex. 1005 (“Devnani”).

⁴ For brevity, the phrase “applicant’s admitted prior art” as set forth in the specification is abbreviated as “AAPA.”

Petitioner Ground #	Claims Challenged	35 U.S.C. §	References/Basis
2	9	103(a) ⁵	Devnani, AAPA, Pillai ⁶
3	12	103(a) ⁷	Devnani, AAPA, Tanahashi ⁸
4	1, 2, 4, 5	103(a)	Devnani, AAPA
5	3	103(a)	Devnani, AAPA, Pillai
6	6	103(a)	Devnani, AAPA, Tanahashi
7	1, 2, 5	103(a)	Chung ⁹ , Celeron ¹⁰
8	3	103(a)	Chung, Celeron, Pillai
9	4	103(a)	Chung, Celeron, AAPA
10	6	103(a)	Chung, Celeron, Tanahashi
11	1, 2, 5	103(a)	Devnani, Celeron
12	6	103(a)	Devnani, Celeron, Tanahashi
13	7	103(a) ¹¹	Dunkerton ¹² , Devnani, CRTA ¹³

⁵ We do not reach the ground because claim 9 is disclaimed.

⁶ US 6,680,530 B1, issued Jan. 20, 2004, Ex. 1007 (“Pillai”).

⁷ We do not reach the ground because claim 12 is disclaimed.

⁸ US 6,172,305 B1, issued Jan. 9, 2001, Ex. 1009 (“Tanahashi”).

⁹ US 2003/0003705 A1, published Jan. 2, 2003, Ex. 1006 (“Chung”).

¹⁰ “Mobile Intel Celeron Processor (0.13 μ) in Micro-FCBGA and Micro-GCPGA Packages,” Datasheet, Intel Corp., April 2003, Ex. 1008 (“Celeron”).

¹¹ We do not reach the ground, because claim 7 is disclaimed.

¹² Dunkerton, et al., “A Review of Ball Grid Arrays for Electronic Assembly,” The 1998 International Conference on Advances in Welding Technology, Sept. 30–Oct. 2, 1998, Ex. 1018 (“Dunkerton”).

¹³ “Critical Review and Technology Assessments ’91–’92,” Reliability Analysis Center, AD-A278 419, 1994, Ex. 1016 (“CRTA”).

III. ANALYSIS

A. *Legal Standard*

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and “the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. *Level of Ordinary Skill in the Art*

In order to determine whether an invention would have been obvious at the time the application was filed, we consider the level of ordinary skill in the pertinent art at the critical time. *Graham*, 383 U.S. at 17. The resolution of this question is important because it allows us to “maintain[] objectivity in the obviousness inquiry.” *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991). In assessing the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (quotation omitted). Generally, it is easier to

establish obviousness under a higher level of ordinary skill in the art. *Innovention Toys, LLC v. MGA Entm't, Inc.*, 637 F.3d 1314, 1323 (Fed. Cir. 2011) (“A less sophisticated level of skill generally favors a determination of nonobviousness . . . while a higher level of skill favors the reverse.”).

Petitioner contends that a person of ordinary skill in the art “would have had a bachelor’s degree in a field relating to the semiconductor manufacturing process, such as materials science, physics, electrical engineering, and/or other related subjects, and at least two to three years of experience with fabrication of integrated circuits.” Pet. 4 (citing Ex. 1002 ¶ 20). Petitioner also contends “[m]ore education can supplement practical experience and vice versa.” *Id.* Patent Owner does not dispute the level of ordinary skill in the art. Prelim. Resp. 4–5.

For purposes of this Decision, we adopt Petitioner’s proposal as reasonable and consistent with the ’245 patent specification and the prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art may reflect an appropriate level of skill in the art).

C. Claim Construction

In *inter partes* reviews, the Board interprets claim language using the same standard as a district court, as described in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b). Under that standard, we generally give claim terms their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history. *See Phillips*, 415 F.3d at 1313–14. Although extrinsic evidence, when available, may also be useful when

construing claim terms under this standard, extrinsic evidence should be considered in the context of the intrinsic evidence. *See id.* at 1317–19.

Petitioner “believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims.” Pet. 10. Patent Owner “does not propose any express claim constructions.” Prelim. Resp. 5.

We address claim 1’s recitation of “wherein none of the signal traces . . . are located over ball pads of the ball pad layer which are disposed in an area” when addressing the parties’ arguments concerning this claim because the parties’ arguments appear to depend on different meanings of this claim term. Aside from this recitation, for purposes of this Decision, we do not discern a need to construe explicitly any claim language because doing so would have no effect on our analyses below of Petitioner’s asserted grounds, and will not assist in resolving the present controversy between the parties. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

D. Overview of the Asserted Art

1. Devnani (Exhibit 1005)

Devnani generally relates to an integrated circuit (IC) die with signal and signal complement traces positioned relative to each other to maximize broadside coupling for a matching impedance, for high-speed signal transmission. Ex. 1005, code (57). Devnani indicates, “[u]se of a broadside coupled trace configuration alleviates routing congestion in an IC package

and permits an IC to accommodate a greater number of channels within a given surface area than is possible under the prior art.” *Id.*

Figure 3, reproduced below, “is a plan view representation of an IC package according to the teachings of the present invention and utilizing signal and signal complement traces on internal layers of the IC package.” *Id.* ¶ 10.

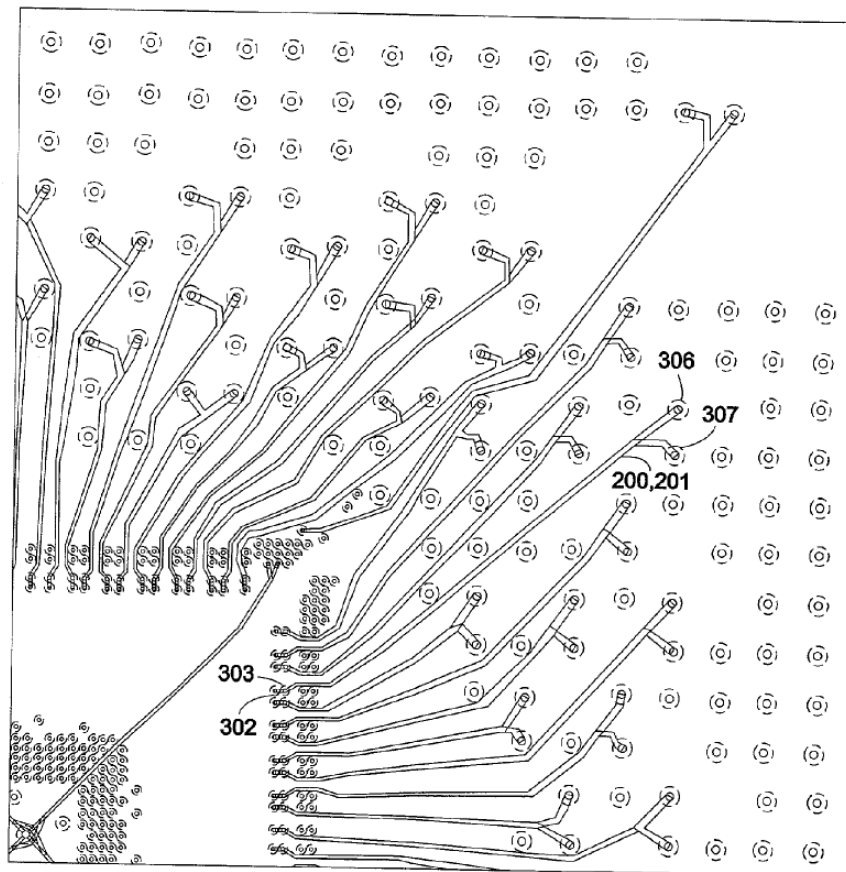


Figure 3 illustrates a corner of an IC package 300, with signal and signal complement flip-chip pads 302, 303, signal trace 200, signal complement trace 201, signal package via 306, and signal complement package via 307. *Id.* ¶¶ 22–23.

Figure 4, reproduced below, is a side view of Devnani’s package.

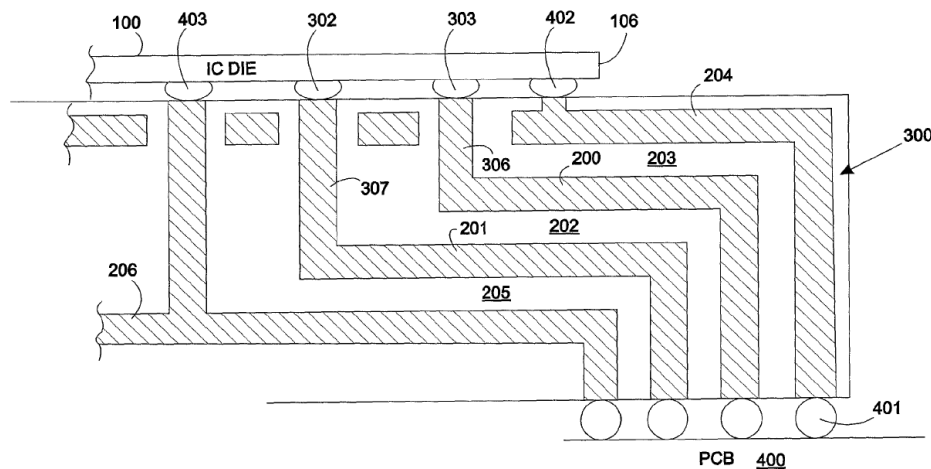


Figure 4 is a side view of the integrated circuit, additionally illustrating printed circuit board 400, interconnection ball 401, reference potential bump 402, bias potential bump 403, signal trace conductive reference plane 204, signal complement trace conductive reference plane 206, and integrated circuit die edge 106. *Id.* ¶¶ 20, 23.

2. Pillai (*Exhibit 1007*)

Pillai generally relates to packaging integrated circuits for high-speed applications. Ex. 1007, 1:6–7. Pillai describes that in prior art technology, “it is not possible to run signals in the gigabit range through the bulk of a ceramic chip carrier with acceptable frequency response.” *Id.* at 1:32–35. Instead, it “has been required to use connectors attached to transmission lines running in a single plane, at considerable cost and subject to tight space limits.” *Id.* at 1:35–38. Further, “[e]dge or surface mount connectors have been used to provide acceptable performance, but cost more to implement and only a very limited number can be used due to real estate constraints on the top surface.” *Id.* at 1:39–43.

To address this, Pillai discloses “a multi-layer chip carrier that makes vertical transitions in signal paths through a number of small steps, rather than a single larger step.” *Id.* at 3:46–48. Figure 1, reproduced below, is a

side view of Pillai's integrated circuit.

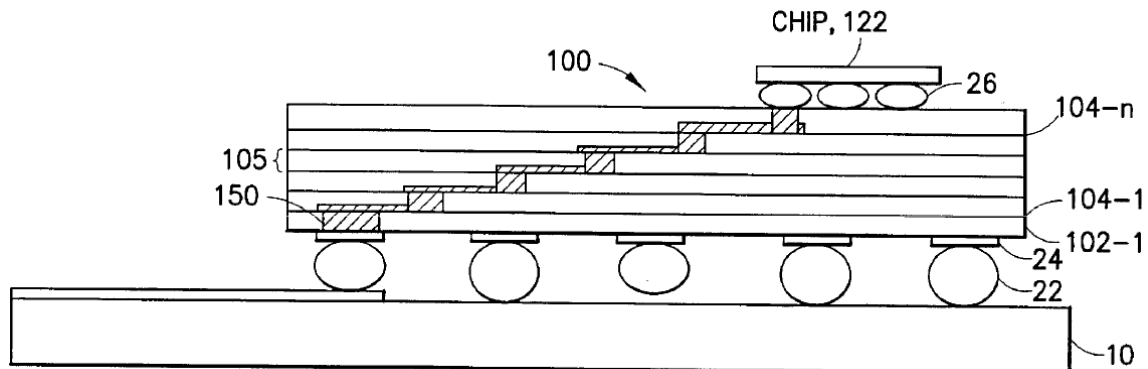


Figure 1 illustrates ceramic chip carrier 100, positioned on substrate 10, with integrated circuit 122 at the top, a bottom ball grid array of balls 22, which interfaces between the substrate and chip carrier, bond pads 24, a top ball grid array of balls 26, and via 150, which traverses horizontal layers 102-1 and 104-1 to 104-n. *Id.* at 2:2–17.

According to Pillai, “substantial improvement in signal quality is possible if the signal is run through a ‘staircase’ structure such as that shown in FIGS. 1 and 2, in which a set of evenly divided vertical steps substitute for the single step of the prior art.” *Id.* at 2:42–46. Pillai discloses “a typical run between the substrate and the chip connection of 25 to 15 mm will have at least 12 horizontal runs and 11 vertical steps, including the steps connecting the top and bottom ball grid arrays.” *Id.* at 2:46–49. Pillai explains, “increasing the number of steps does not cause an adverse effect either since the small reflections at each step are attenuated on their return to the chip driver circuit.” *Id.* at 2:52–55.

3. *Tanahashi (Ex. 1009)*

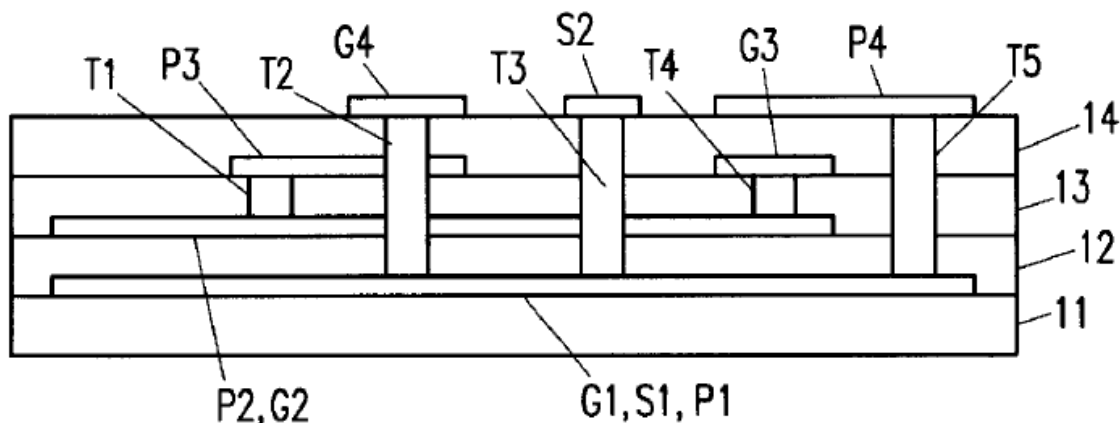
Tanahashi generally relates to the structure of a conductive layer for electric wiring in a multilayer circuit board used for an electrical circuit board. Ex. 1009, 1:6–9. Tanahashi describes problems with multilayer

circuit boards, where the power wiring conductor, ground wiring conductor, and signal wiring conductor are formed in the same layer, and the signal wiring conductor is arranged between the power wiring conductor and the ground wiring conductor to form a coplanar line structure. *Id.* at 1:48–2:45.

Tanahashi is:

directed to a multilayer circuit board in which a capacitance is made between a power wiring conductor and a ground layer while keeping a characteristic impedance of a signal wiring conductor to uniform, whereby a power supply can be arranged close to a semiconductor device, as well as characteristic impedances of the power wiring conductor and the ground layer and then a composite characteristic impedance of a power supply path are decreased to provide a stable power supply to the semiconductor device and prevent the erroneous operation of the semiconductor device.

Id. at 2:59–3:3. Figure 3B, reproduced below, is a side view diagram of one embodiment of Tanahashi.



In Figure 3B:

the first ground wiring conductor G1, the first power wiring conductor P1, and the first signal wiring conductor S1 provided between them are placed substantially in parallel to each other on the first insulating layer I1, and the first power wiring conductor P1 has an end for connecting via the through-hole conductor T5

with the fourth power wiring conductor P4 placed upward, outside the right angle formed thereby.

Id. at 13:29–37.

4. *Chung (Ex. 1006)*

Chung generally relates to integrated circuit packages having bond pads that are directly connected with vertically-oriented conductive layers, rather than with vias or horizontally-oriented conductive layers. Ex. 1006 ¶ 1. Chung describes that the pads dedicated to input-output operations are typically located only at the outer edge rows of ball pads. *Id.* ¶ 6. Chung describes the use of decoupling capacitors to reduce noise. *Id.* ¶ 8. Chung discloses that “what are needed are packages that can provide higher levels of decoupling capacitance, without increased package sizes, and at reduced inductance levels.” *Id.* ¶ 13.

Figure 2, reproduced below, illustrates a three-dimensional diagram of one of Chung’s embodiments.

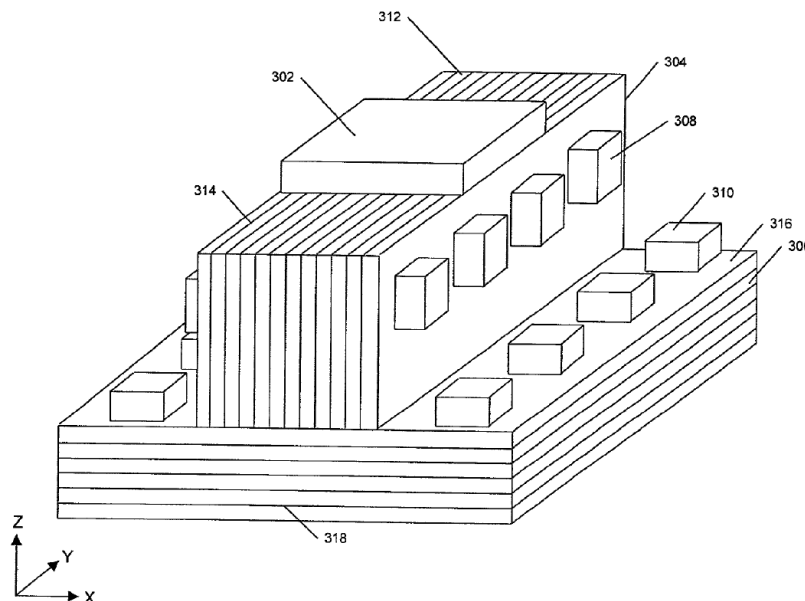


Figure 3 shows integrated circuit 302, with a package consisting of a vertical package section 304, horizontal package section 306, first level

decoupling capacitors 308, and second level decoupling capacitors 310. *Id.* ¶ 27.

5. *Celeron (Ex. 1008)*

Celeron is a Datasheet of several processor packages available from the Intel Corporation. Ex. 1008, 10. Celeron covers the electrical, thermal, and mechanical specifications of the processors and packages. *Id.*

The Datasheet also describes that the Celeron Processor will be available in a 479-ball surface-mount package. *Id.* at 69. The Datasheet describes that the package may have “capacitors placed in the area around the die.” *Id.* Figure 28, reproduced below, shows isometric diagrams of the top and bottom of the package.

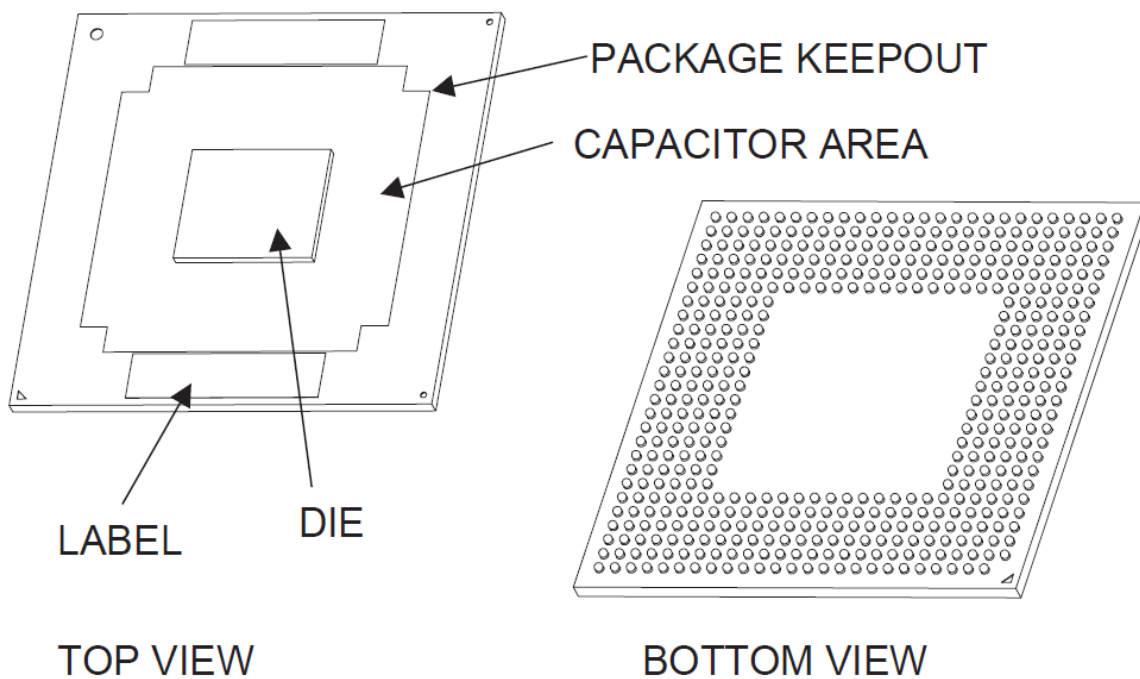


Figure 28 shows isometric views of the top and bottom of the chip, showing the die and capacitor area around it on the top, and, on the bottom, a surface full of ball pads with an area clear of ball pads in the center. *Id.*, Fig. 29, 30.

E. Unpatentability Grounds

1. Unpatentability over Devnani and AAPA (Grounds 1 and 4)

Petitioner asserts that claims 1, 2, 4, 5, and 8 are unpatentable under 35 U.S.C. § 103(a) as obvious over Devnani in view of AAPA, citing the Declaration of Dr. R. Jacob Baker for support (Ex. 1002). Pet. 16, 27–29, 35–44 (citing Ex. 1002). Patent Owner disputes Petitioner’s assertions as to claim 8. Prelim. Resp. 6–39. We address Petitioner’s assertions and Patent Owner’s arguments below.

Ground 1. We first address Petitioner’s ground one, which addresses claim 8. Claim 8 depends from claim 7, so we address the recitations of claims 7 and 8. Petitioner argues that Devnani discloses the recitations of claim 7. Pet. 16–27. Petitioner argues that to the extent Devnani does not disclose “wherein none of the signal traces of the bottom routing layer are located within the area of increased stress defined by the corner of the die,” the AAPA discloses this recitation. *Id.* at 22. As to claim 8, Petitioner admits “Devnani does not explicitly state the signal traces that are not near the corner of the die are farther than ‘two ball pad pitches’ [as claim 8 recites].” *Id.* at 27. Petitioner argues, however, that this recitation would have been obvious to a person having ordinary skill in the art implementing a packaging according to the combined teachings of Devnani and the AAPA. *Id.* Petitioner also argues a person having ordinary skill in the art would have combined the teachings of Devnani and the AAPA. *Id.* at 24–29.

Patent Owner argues that Devnani does not teach or suggest a die having “a corner defining a surrounding area of increased stress” as claim 7 recites. Prelim. Resp. 14. Petitioner identifies Devnani’s teaching of a die

corner and provides evidence that a person having ordinary skill in the art would have understood that such die corners undergo increased stress. Pet. 18–19 (citing Ex. 1005, Fig. 3; Ex. 1002 ¶¶ 52–58). Neither party addresses the metes and bounds of this recitation in a fulsome manner. Based on the current record, we determine that the information presented sufficiently supports, for purposes of institution, Petitioner’s assertions that Devnani teaches or suggests this recitation. *See* Pet. 16–27. To the extent Patent Owner maintains that Devnani does not teach this recitation in a Patent Owner Response, we invite the parties to further address at trial the meaning of this recitation and how it compares to Devnani.¹⁴

Patent Owner further argues that claim 8’s “two ball pad pitches” recitation would not have been obvious in view of Devnani and “Purported AAPA.” Prelim. Resp. 16. Patent Owner emphasizes that “Petitioner has not shown a reasonable likelihood that the disadvantages of the purported AAPA solution were known in the prior art.” *Id.* To provide guidance for the parties at trial, we preliminarily address the scope of the ’245 Patent’s admitted prior art.¹⁵

¹⁴ We remind Petitioner that “[i]t is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify ‘with particularity’ the ‘evidence that supports the grounds for the challenge to each claim.’” *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (quoting 35 U.S.C. § 312(a)(3)).

¹⁵ We note that the Patent Office Director has addressed use of AAPA in IPR proceedings, and our decision is consistent with that guidance. *See* Updated Guidance on the Treatment of Statements of the Applicant in the Challenged Patent in Inter Partes Reviews Under § 311 (June 9, 2022 (“AAPA Guidance”)).

Figures 1–3 of the '245 patent are each labeled “(Prior Art).” Ex. 1001, Figs. 1–3. These figures depict a single device with Figure 1 providing an overview, Figure 2 showing a portion of layer L9, and Figure 3 showing a portion of layer L8. *Id.* at 1:23–2:2. The '245 patent indicates that this device is “an example” of a package “in wide use.” *Id.* at 1:22–28. Thus, it is reasonably clear, on this record, that the device depicted in Figures 1–3, and the specification’s description of those figures, is admitted prior art.

The '245 patent also states that this typical package has edges of ball pads that “act as stress concentration points,” which may initiate cracks under temperature cycling conditions. *Id.* at 1:61–2:2. The '245 patent explains that cracks extending through traces can “cause failures.” *Id.* The '245 patent then identifies a first “existing solution” and second “existing solution” to this problem. *Id.* at 2:3–15. Patent Owner argues that these “existing solutions” are not admitted prior art known to others. Prelim. Resp. 8. We are skeptical of Patent Owner’s argument in this regard for three reasons. First, the '245 patent refers to these solutions as “existing” and discusses these solutions as “BACKGROUND OF THE INVENTION.” Ex. 1001, 1:5, 2:3–9. *See* AAPA Guidance at 4 (“Admissions . . . may describe technology as “prior art,” “conventional,” or “well-known.”) Second, we note that Figure 3, labeled “prior art,” depicts a lack of traces overlapping corner 38a. *Id.* Fig. 3. Third, the evidence of record indicates that persons of skill in the art understood that the die corner and solder balls could be points of high stress. Pet. 39; Ex. 1002 ¶¶ 46, 47, 52–57 (citing Exs. 1010, 1011, 1016, 1017). Given this context, it is reasonable that these “existing solutions” and the problem these existing solutions address *may* constitute admitted prior art. We reserve final resolution of this fact question for trial.

Finally, the '245 patent states disadvantages of the first and second “existing solution[s].” Ex. 1001, 2:3–15. With regard to the second existing solution, the '245 patent states “[a] disadvantage of having a one (1) millimeter radius region under the die corner 38*a* is that it is not sufficient to avoid trace cracks in the layer L8 under temperature cycling conditions for all packaging technologies.” *Id.* at 2:11–15. The '245 patent does not teach that recognition of the problems with these “existing solution[s]” were known in the art. Rather, the '245 patent identifies these problems and then suggests that “[t]he present invention” will address solutions to these problems. *Id.* at 2:16–22. Based on the present record, we are skeptical of Petitioner’s position to the extent Petitioner argues that recognition of problems with the two “existing solution[s]” are admitted prior art. We emphasize that our findings regarding the scope of admitted prior art is preliminary and based on the current record.

Petitioner relies on recognition by the prior art of problems with the second “existing solution” as reason to reach the recitations of claim 8. Pet. 27–38. We reserve final consideration of whether Petitioner’s rationale for reaching claim 8 is adequately supported after development of a full trial record.

Ground 4. Petitioner argues that Devnani teaches most of the recitations of claim 1 for the same reasons that Petitioner expresses when addressing claim 7. Pet. 36. Patent Owner argues that Petitioner’s cross-referencing is inappropriate and does not meet the requirements for *inter partes* review. Prelim. Resp. 21–25. We disagree. Many of the recitations of claim 1 are identical to the recitations of claim 7. It is appropriate for

Petitioner to refer back to its arguments for claim 7 when addressing identical or substantially identical recitations of claim 1.

As to claim 1's recitation of "wherein none of the signal traces . . . are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die," Petitioner argues that Devnani teaches this as an "inherent feature" because Devnani Figure 3 shows all signal traces 200 being routed away from the high stress zone. Pet. 37 (citing Ex. 1005, Fig. 3; Ex. 1002 ¶ 105). Petitioner admits that "Devnani does not explicitly disclose that high stress area is defined by 'two ball pad pitches of the corner of the die.'" *Id.* Petitioner argues that the AAPA renders this claim element obvious. *Id.* Petitioner argues that the AAPA includes a teaching of a one-millimeter radius around the die corner without routing traces on layer L8. *Id.* at 38. Petitioner further argues that a person having ordinary skill in the art "would have known that the die corner and the underlying solder balls near the die corner would be high stress points" and presents evidence persuasively supporting this argument. *Id.* at 39 (citing Ex. 1002 ¶¶ 46–47, 52–57). Petitioner argues that the two ball pad pitch recitation is merely a change in shape and that a person having ordinary skill in the art would have known to use a larger area to achieve a known result. *Id.* at 41.

Patent Owner again argues that the '245 patent's reference to two "existing" solutions is not admitted prior art. Prelim. Resp. 27. As we explain above, we are skeptical of Patent Owner's argument as applied to the '245 patent's explanation of "existing" solutions, but we will consider the issue at trial on a full record if Patent Owner raises it in its Patent Owner Response.

Patent Owner also argues that Devnani does not render obvious the “two ball pitches” recitation. Prelim. Resp. 30. In particular, Patent Owner argues that claim 1 requires that the package have ball pads within two ball pad pitches of the corner of the die. Prelim. Resp. 32. On this record, we disagree with this claim interpretation.

Claim 1 affirmatively recites, for example, “a plurality of layers under the top layer.” Ex. 1001, 4:13. Claim 1 also affirmatively recites that the “plurality of layers compris[es] a bottom routing layer having signal traces thereon.” *Id.* at 4:14–15. So, claim 1 requires a bottom routing layer having signal traces. Claim 1 then recites “where[] none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die.” *Id.* at 4:17–20. This recitation serves to describe the “signal traces of the bottom routing layer.” The recitation does not affirmatively recite a required location of any ball pads. Likewise, the claim as a whole also does not state that the ball pad layer comprises ball pads disposed within two ball pad pitches of the corner of the die. Rather, the claim recites “said ball pad layer having a plurality of ball pads” without affirmatively indicating where those ball pads must be located within the ball pad layer.

Thus, on the present record, we interpret claim 1’s recitation of “none of the signal traces . . . within two ball pad pitches of the corner of the die” as requiring that no signal traces of the bottom routing layer be located over ball pads of the ball pad layer disposed within two ball pad pitches of the corner of the die if any such ball pads exist in this location. We do not interpret claim 1 as affirmatively requiring ball pads disposed within two ball pad pitches of the corner of the die. To the extent Patent Owner

maintains arguments regarding this recitation in a Patent Owner Response, we invite the parties to further address this claim construction issue at trial to the extent permitted by our rules.

Ground 4 also addresses dependent claims 2, 4, and 5. Petitioner provides argument addressing the recitations of these claims. Pet. 42–44. Patent Owner disputes Petitioner’s argument for claim 2 for reasons similar to those Patent Owner raises with respect to claim 8. Prelim. Resp. 38. Patent Owner does not substantively argue with respect to the recitations of claims 4 and 5 at this time. We defer further consideration of the dependent claims until after the parties develop a full record at trial.

2. *Unpatentability over Devnani, AAPA, and Pillai*
(Ground 5)

Petitioner asserts claim 3 is unpatentable under 35 U.S.C. § 103(a) as obvious over Devnani in view of AAPA, and further in view of Pillai. Pet. 45 (citing Ex. 1002). Patent Owner argues that Pillai does not overcome the deficiencies with regard to claim 1. Prelim. Resp. 40. We defer further consideration of the dependent claim 3 until after the parties develop a full record at trial.

3. *Unpatentability over Devnani, AAPA, and Tanahashi*
(Ground 6)

Petitioner asserts that claim 6 is unpatentable under 35 U.S.C. § 103(a) as obvious over Devnani in view of AAPA, and further in view of Tanahashi. Pet. 45 (citing Ex. 1002). Patent Owner argues that Tanahashi does not overcome the deficiencies with regard to claim 1. Prelim. Resp. 40–41. We defer further consideration of the dependent claim 6 until after the parties develop a full record at trial.

4. *Unpatentability over Chung and Celeron (Ground 7)*

Petitioner asserts claims 1, 2, and 5 are unpatentable under 35 U.S.C. § 103(a) as obvious over Chung in view of Celeron. Pet. 45–55 (citing Ex. 1002). Petitioner argues that Chung teaches most of claim 1’s recitations. *Id.* at 45–48. Petitioner states that “Chung does not explicitly show that ‘none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within an area within two ball pad pitches of the corner of the die’ as required by the last element of claim 1.” *Id.* at 48. Petitioner argues, however, that Celeron teaches such a configuration. *Id.* at 48–53. Petitioner argues that a person implementing Chung’s package would have had good reasons to look to Celeron because Celeron is in the same field, because implementation would be straightforward because there is no change of function, and because routing layers in the clear area of Celeron would “prevent damage to signal traces of the bottom routing layer during thermal cycling.” *Id.* (citing, for example, Ex. 1002 ¶ 141).

We have reviewed Petitioner’s contentions for all of the elements of independent claim 1, as well as the supporting evidence. Pet. 45–55. Based on the record before us, we are persuaded that Petitioner’s discussion of the particular structures and methods in Chung and Celeron establishes a reasonable likelihood of prevailing at trial on the issue of whether the combined teachings of Chung and Celeron teach or suggest all of the limitations of independent claim 1. *Id.* Also, based on the present record, we are persuaded that Petitioner adequately establishes that a person having ordinary skill in the art would have had reason to combine the teachings of Chung and Celeron.

Patent Owner argues that Celeron lacks ball pads near its die corners. Prelim. Resp. 41–42. As we explain above, however, we disagree with Patent Owner that claim 1 requires ball pads within two ball pad pitches of the corner of the die. *See* Section III(E)(1), *supra*. Patent Owner’s argument, therefore, does not, based on the present record, persuasively undermine Petitioner’s showing.

Patent Owner also argues that Chung and Celeron fail to show the signal traces. Prelim. Resp. 42. Petitioner adequately establishes that Chung teaches conductive layer 544 (which Petitioner identifies as a “bottom routing layer”) including signal traces. Pet. 47; Ex. 1006 ¶¶ 38, 50, Fig. 5. We agree with Patent Owner that Petitioner does not identify how Chung or Celeron teach where signal traces are within the bottom routing layer. Petitioner, however, adequately establishes that Celeron teaches no ball pads at all in its clear area near the die corners. Pet. 48–53. Thus, Petitioner adequately establishes that regardless of where the signal traces are located in Chung or Celeron, the traces would necessarily meet claim 1’s requirement that “none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die.” *Id.*

Patent Owner also argues that Petitioner has not adequately established that Celeron is prior art. Prelim. Resp. 43–44. We disagree. Petitioner identifies Exhibit 1008 as being the Celeron reference. Pet. 3. Exhibit 1008 includes a copyright page suggesting the Celeron reference was publicly available by 2002. Ex. 1008, 2. For example, Celeron states that “[i]nformation in this document is provided in connection with Intel products” and provides information on how the public may obtain Intel

literature. *Id.* These indicia are sufficient to establish that Petitioner has a reasonable likelihood of showing at trial that Celeron was publicly available by 2002. *See Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 at 13 (PTAB Dec. 20, 2019) (precedential) (stating that, “at the institution stage, the petition must identify, with particularity, evidence sufficient to establish a reasonable likelihood that [a] reference was publicly accessible before the critical date of the challenged patent and therefore that there is a reasonable likelihood that it qualifies as a printed publication”). Patent Owner presents no countervailing evidence at this time. As such, Patent Owner’s argument does not persuasively undermine Petitioner’s showing.

Ground 7 also addresses dependent claims 2 and 5. Petitioner provides argument addressing the recitations of these claims. Pet. 53–55. Patent Owner does not substantively argue with respect to the recitations of claims 2 and 5 at this time. Prelim. Resp. 43–44. We defer further consideration of the dependent claims until after the parties develop a full record at trial.

5. *Unpatentability over and Chung, Celeron, and Pillai*
(Ground 8)

Petitioner asserts claim 3 is unpatentable under 35 U.S.C. § 103(a) as obvious over Chung, Celeron, and Pillai. Pet. 55–56 (citing Ex. 1002). Patent Owner does not substantively argue with respect to the recitations of claim 3 at this time. Prelim. Resp. 44. We defer further consideration of dependent claim 3 until after the parties develop a full record at trial.

6. *Unpatentability over Chung, Celeron, and AAPA*
(Ground 9)

Petitioner asserts claim 4 is unpatentable under 35 U.S.C. § 103(a) as obvious over Chung in view of Celeron, and further in view of AAPA.

Pet. 57–58 (citing Ex. 1002). Patent Owner does not substantively argue with respect to the recitations of claim 4 at this time. Prelim. Resp. 44. Patent Owner does argue that the purported AAPA is not prior art. *Id.* Petitioner, however, relies on ’245 patent Figure 1 and related text for this particular ground. Pet. 57–58. As we explain above, it is reasonably clear that ’245 patent Figure 1 is admitted prior art. *See* Section III(E)(1), *supra*. We defer further consideration of dependent claim 4 until after the parties develop a full record at trial.

7. *Unpatentability over Chung, Celeron, and Tanahashi (Ground 10)*

Petitioner asserts claim 6 is unpatentable under 35 U.S.C. § 103(a) as obvious over Chung in view of Celeron, and further in view of Tanahashi. Pet. 58–60 (citing Ex. 1002). Patent Owner does not substantively argue with respect to the recitations of claim 6 at this time. Prelim. Resp. 45–46. We defer further consideration of dependent claim 6 until after the parties develop a full record at trial.

8. *Unpatentability over Devnani and Celeron (Ground 11)*

Petitioner asserts claims 1 and 5 are unpatentable under 35 U.S.C. § 103(a) as obvious over Devnani in view of Celeron. Pet. 60–62 (citing Ex. 1002). As to claim 1, Petitioner relies on Devnani in the same way it does for grounds one and four. *Id.* at 60. With respect to claim 1’s “wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die” recitation, Petitioner relies on Celeron in a manner similar to ground 7. *Id.* at 61. Petitioner’s stated reason and motivation to combine is similar to the rationale for combining Chung and

Celeron. *Id.* We have reviewed Petitioner’s contentions for all of the elements of independent claim 1, as well as the supporting evidence. *Id.* at 60–62. Based on the record before us, we are persuaded that Petitioner’s discussion of the particular structures and methods in Devnani and Celeron establishes a reasonable likelihood of prevailing at trial on the issue of whether the combined teachings of Devnani and Celeron teach or suggest all of the limitations of independent claim 1. *Id.* Also, based on the present record, we are persuaded that Petitioner adequately establishes that a person having ordinary skill in the art would have had reason to combine the teachings of Devnani and Celeron.

Patent Owner argues that the Petition is too conclusory, that the proposed combination would not have had ball pads near the corner of the die, and that Celeron is not shown to be prior art. Prelim. Resp. 46–48. For the reasons we explain above, none of these arguments persuasively undermine Petitioner’s showing of unpatentability. *See* Sections III(E)(1), (4), *supra*.

Petitioner also asserts claim 5 is unpatentable under 35 U.S.C. § 103(a) as obvious over Devnani and Celeron. Pet. 61. Patent Owner does not substantively argue with respect to the recitations of claim 5 at this time. Prelim. Resp. 49. On the present record, we are persuaded that Petitioner’s discussion of the particular structures and methods in Devnani and Celeron establishes a reasonable likelihood of prevailing at trial on the issue of whether the combined teachings of Devnani and Celeron teach or suggest all of the limitations of dependent claim 5.

9. *Unpatentability over Devnani, Celeron, and Tanahashi*
(Ground 12)

Petitioner asserts claim 6 is unpatentable under 35 U.S.C. § 103(a) as obvious over Devnani in view of Celeron, and further in view of Tanahashi. Pet. 62–63 (citing Ex. 1002). Patent Owner does not substantively argue with respect to the recitations of claim 6 at this time. Prelim. Resp. 49–50. We defer further consideration of dependent claim 6 until after the parties develop a full record at trial.

IV. CONCLUSION

For the reasons above, we determine that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail with respect to one or more challenged claims of the '245 patent. At this juncture in the proceeding, we have not made a final determination with respect to the patentability of the challenged claims, or with respect to claim construction.

V. ORDER

For the foregoing reasons, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–6 and 8 of the '245 patent is hereby instituted with respect to all grounds of unpatentability set forth in the Petition that address those claims¹⁶; and

¹⁶ We will not further address grounds that only address disclaimed claims 7 and 9–12.

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FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this Decision.

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