

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP USA, Inc.

Petitioner

v.

Bell Semiconductor, LLC

Patent Owner

Case: IPR2024-00168

Patent No. 7,345,245

DECLARATION OF JUNE ANN MUNFORD

Mail Stop PATENT BOARD
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

1. My name is June Ann Munford. I am over the age of 18, have personal knowledge of the facts set forth herein, and am competent to testify to the same.
2. I earned a Master of Library and Information Science (MLIS) from the University of Wisconsin-Milwaukee in 2009. I have over ten years of experience in the library/information science field. Beginning in 2004, I have served in various positions in the public library sector including Assistant Librarian, Youth Services Librarian and Library Director. I have attached my Curriculum Vitae as Appendix CV.
3. During my career in the library profession, I have been responsible for materials acquisition for multiple libraries. In that position, I have cataloged, purchased and processed incoming library works. That includes purchasing materials directly from vendors, recording publishing data from the material in question, creating detailed material records for library catalogs and physically preparing that material for circulation. In addition to my experience in acquisitions, I was also responsible for analyzing large collections of library materials, tailoring library records for optimal catalog

search performance and creating lending agreements between libraries during my time as a Library Director.

4. I am fully familiar with the catalog record creation process in the library sector. In preparing a material for public availability, a library catalog record describing that material would be created. These records are typically written in Machine Readable Catalog (herein referred to as “MARC”) code and contain information such as a physical description of the material, metadata from the material’s publisher, and date of library acquisition. In particular, the 008 field of the MARC record is reserved for denoting the date of creation of the library record itself. As this typically occurs during the process of preparing materials for public access, it is my experience that an item’s MARC record indicates the date of an item’s public availability.
5. Typically, in creating a MARC record, a librarian would gather various bits of metadata such as book title, publisher and subject headings among others and assign each value to a relevant numerical field. For example, a book’s physical description is tracked in field 300 while title/attribution is tracked in field 245. The 008 field of the MARC record is reserved for denoting the creation of the library record itself. As this is the only date reflecting the inclusion of said materials within the library’s collection, it is my experience

that an item's 008 field accurately indicates the date of an item's public availability.

6. I am familiar with the Internet Archive, a digital library formally certified by the State of California as a public library. Among other services that the Internet Archive makes available to the general public is the Wayback Machine, an online archive. The Internet Archive's Wayback Machine service archives webpages as of a certain capture date to track changes in the web over time. The Internet Archive has been in operation as a nonprofit library since 1996 and has hosted the Wayback Machine service since its inception in 2001. During my time as a librarian, I frequently used the Internet Archive's Wayback Machine for research and instruction purposes. This includes teaching instructional classes on using the Wayback Machine to library patrons and using the Wayback Machine to research reference inquiries that require hard-to-find online resources. I consider the Internet Archive's recordskeeping to be as rigorous and detailed as other formal library recordskeeping practices such as MARC records, OCLC records and Dublin Core.
7. I have reviewed Exhibit 1008, a datasheet entitled *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages At 1.33*

GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003) by Intel. A copy of this reference was provided to me by council. The metadata contained within the PDF file provided to me as Exhibit-1008 indicates the file was first created as of March 26, 2003 and most recently updated as of August 19, 2016.

8. Attached hereto as Appendix INTEL2003-01 is a screen capture of a web page entitled “Mobile Intel Celeron Processor Datasheets” hosted on the Intel website. I secured these captures myself from <https://www.intel.com/content/www/us/en/support/articles/000006672/processors.html>. Appendix INTEL2003-01 also contains a PDF copy of *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003)*, secured from a link available on page 1 of Appendix INTEL2003-01.
9. In comparing Exhibit 1008 to Appendix INTEL2003-01, it is my determination that Exhibit 1008 is a true and correct copy of *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA*

Packages At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003).

10. The PDF copy of *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003)* listed on this web page includes a 'Date' field indicating this document was first published as of April 2003. This date matches the April 2003 date present on page 1 of the PDF document. Page 4 of Appendix INTEL2003-01 displays the document properties of the PDF listed on the Intel website, indicating this document was first created as of March 26, 2003 and most recently updated as of August 19, 2016.

11. Attached hereto as Appendix INTEL2003-02 is a PDF copy of *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003)* as hosted on the Internet Archive website. I secured this file myself from

<https://ia804508.us.archive.org/16/items/manualzilla-id-7136606/7136606.pdf>.

12. Pages 1-9 and 65-73 of *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003)* as contained within Appendix INTEL2003-02 appear to be identical to the copies present in Exhibit 1008 and Appendix INTEL2003-01. Page 2 of Appendix INTEL2003-02 displays the document properties of the PDF listed on the Internet Archive website, indicating this document was first created as of March 26, 2003 and most recently updated as of March 26, 2003.

13. Attached hereto as Appendix INTEL2003-03 is a series of screen captures, including the Internet Archive Wayback Machine entry for <http://developer.intel.com/design/mobile/datashts/298517.htm>. I secured these screen captures myself from <https://web.archive.org/web/20030803150718/http://developer.intel.com:80/design/mobile/datashts/298517.htm> and is a true and correct copy of the Internet Archive record for this webpage. Pages 1-3 were captured by the

Internet Archive as of August 3, 2003. Page 4 was captured as of August 6, 2003, Page 5 was captured as of August 10, 2003, Page 6 was captured as of August 10, 2003, Page 7 was captured as of August 10, 2003, Page 6 was captured as of August 10, 2003, Page 8 was captured as of June 4, 2003, Page 9 was captured as of June 4, 2003, Page 10 was captured as of August 3, 2003 and page 11 was captured as of November 1, 2004.

14. Appendix INTEL2003-03 is a capture of a web page entitled “Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages at 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 733 MHz, 650 MHz; and Ultra Low Voltage 733 MHz, 700 MHz, 667 MHz, and 650 MHz” as published on the Intel website as of August 3, 2003. This page accurately describes *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003)* as present in Exhibit 1008, Appendix INTEL2003-01 and Appendix INTEL2003-02.

15. Page 2 of Appendix INTEL2003-03 also offers three different download links for this datasheet, indicating that interested users navigating the Intel

website in August 2003 would have been able to discover and download *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003)*. As illustrated on pg. 3 of Appendix INTEL2003-03, inspecting the web page's code or hovering over a link on this page displays a file name, with each download link on this page displaying the file name '29851706.pdf'. '29851706.pdf' matches the file description on page 4 of Appendix INTEL2003-01 and the URL present on page 10 of Appendix INTEL2003-03.

16. Appendix INTEL2003-03 also contains a series of screen captures from the Internet Archive illustrating one path that an interested member of the public could have followed as of 2003 to discover *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003)* on the Intel website. I secured the screen captures of each Internet Archive page discussed hereto. As demonstrated in

pages 4 – 11 of this Appendix, a user beginning on the homepage of Intel could click on the link entitled ‘Support’ to find a technical support page. This home page is a true and correct copy of the Internet Archive record for https://web.archive.org/web/20030806043441/http://www.intel.com/index.htm?iid=Corporate+Header_Intel_logo&, can be found on page 4 of Appendix INTEL2003-03 and was captured as of August 6, 2003.

17. From this technical support page, a user could click on the link entitled ‘receive technical support’ to find a site map. This technical support page is a true and correct copy of the Internet Archive record for https://web.archive.org/web/20030810185734/http://intel.com/support/index.htm?iid=Homepage+Header_Support&, can be found on page 5 of Appendix INTEL2003-03 and was captured as of August 10, 2003.

18. From this site map, a user could click on the link entitled ‘Processors’ to find a page describing various Intel processors. This site map page is a true and correct copy of the Internet Archive record for <https://web.archive.org/web/20030810213653/http://intel.com/support/sitemap.htm>, can be found on page 6 of Appendix INTEL2003-03 and was captured as of August 10, 2003.

19. From this page describing Intel processors, a user could click on the link entitled 'Mobile Intel Celeron processors' to find a page describing the mobile Intel Celeron processors. This page describing Intel processors is a true and correct copy of the Internet Archive record for <https://web.archive.org/web/20030810013242/http://support.intel.com/support/processors/index.htm>, can be found on page 7 of Appendix INTEL2003-03 and was captured as of August 10, 2003.

20. From this mobile Intel Celeron processors page, a user could click on the link entitled 'Datasheets' to find a page containing several mobile processor datasheets. This page describing mobile Intel Celeron processors is a true and correct copy of the Internet Archive record for <https://web.archive.org/web/20031003184919/http://support.intel.com/support/processors/mobile/celeron/>, can be found on page 8 of Appendix INTEL2003-03 and was captured as of June 4, 2003.

21. From this mobile processor datasheet page, a user could click on the link entitled 'Mobile Intel Celeron Processor (0.13u) in Micro-FCPGA and Micro-FCBGA Packages' to discover a page describing *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz;*

Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003). This mobile processor datasheet page is a true and correct copy of the Internet Archive record for

<https://web.archive.org/web/20031011093308/http://developer.intel.com/design/mobile/datashts/>, can be found on page 9 of Appendix INTEL2003-03 and was captured as of June 4, 2003.

22. Finally, a user could download a PDF copy of this datasheet from the page describing *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003)* by clicking the link entitled ‘U.S. Web Server’. The page describing this datasheet is a true and correct copy of the Internet Archive record for <https://web.archive.org/web/20030803150718/http://developer.intel.com/design/mobile/datashts/298517.htm>, can be found on page 10 of Appendix INTEL2003-03 and was captured as of August 3, 2003.

23. The PDF copy of *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages At 1.33 GHz, 1.26 GHz, 1.20 GHz,*

1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003) found by the clicking the 'U.S. Web Server' link is a true and correct copy of the Internet Archive record for

<https://web.archive.org/web/20041101063418/http://developer.intel.com/design/mobile/datashts/29851706.pdf>, can be found on page 11 of Appendix

INTEL2003-03 and was captured as of November 1, 2004.

24. I have inspected pages 1-9 and 65-73 of Exhibit 1008, Appendix

INTEL2003-01 and Appendix INTEL2003-02 and as such, it is my determination that each of these documents are functionally identical copies of *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003)*. These different files contain the same title, revision month, order number and copyright dates.

25. Exhibit 1008, Appendix INTEL2003-01, and Appendix INTEL2003-02

contain metadata within their file properties indicating multiple copies of *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-*

FCPGA Packages At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003) were in existence as of March 26, 2003.

26. Appendix INTEL2003-01 indicates this datasheet was first published as of April 2003. Appendix INTEL2003-03 indicates that visitors to the Intel website were able to download a full and complete copy of *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003)* as of August 3, 2003 if not earlier. Considering this evidence, it is my determination that *Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz (April 2003)* was first made available to the public as of August 3, 2003 via the Internet Archive and likely prior to August 3, 2003 via other outlets.

27. I have reviewed Exhibit 1010, “The effects of in-plane orthotropic properties in a multi-chip ball grid array assembly” by Thomas D. Moore and John L. Jarvis as published in *Microelectronics Reliability*, June 2002.

28. Attached hereto as Appendix MOORE01 is a true and correct copy of the MARC record for *Microelectronics Reliability* as held by the Penn State University library. I secured this record myself from the library’s public catalog. The MARC record contained within Appendix MOORE01 accurately describes the title, author, publisher, and ISSN number of *Microelectronics Reliability*. The ‘Availability’ field of this record visible on page 4 indicates this collection includes the June 2002 edition of *Microelectronics Reliability* containing “The effects of in-plane orthotropic properties in a multi-chip ball grid array assembly”. In comparing Exhibit 1010 to Appendix MOORE01, it is my determination that Exhibit 1010 is a true and correct copy of “The effects of in-plane orthotropic properties in a multi-chip ball grid array assembly” by Thomas D. Moore and John L. Jarvis as published in *Microelectronics Reliability* June 2002.

29. The 008 field of the MARC record in Appendix MOORE01 indicates the date of record creation. The 008 field of Appendix MOORE01 indicates the Penn State University library first acquired this journal as of June 18, 1982

and held the journal in perpetuity until 2004. Considering this information, it is my determination that *Microelectronics Reliability* June 2002 and therefore “The effects of in-plane orthotropic properties in a multi-chip ball grid array assembly” was made available to the public shortly after its initial publication in June 2002.

30. I have reviewed Exhibit 1011, “Process capability study and thermal fatigue life prediction of ceramic BGA solder joints” by D.J. Xie and Z.P. Wang as published in *Finite Elements in Analysis and Design*, July 1998.

31. Attached hereto as Appendix XIE01 is a true and correct copy of the MARC record for *Finite Elements in Analysis and Design* as held by the Penn State University library. I secured this record myself from the library’s public catalog. The MARC record contained within Appendix XIE01 accurately describes the title, author, publisher, and ISSN number of *Finite Elements in Analysis and Design*. The ‘Availability’ field of this record visible on page 3 indicates this collection includes the July 1998 edition of *Finite Elements in Analysis and Design* containing “Process capability study and thermal fatigue life prediction of ceramic BGA solder joints”. In comparing Exhibit 1011 to Appendix XIE01, it is my determination that Exhibit 1011 is a true and correct copy of “Process capability study and thermal fatigue life

prediction of ceramic BGA solder joints” by D.J. Xie and Z.P. Wang as published in *Finite Elements in Analysis and Design* July 1998.

32. The 008 field of the MARC record in Appendix XIE01 indicates the date of record creation. The 008 field of Appendix XIE01 indicates the Penn State University library first acquired this journal as of November 11, 1985 and held the journal in perpetuity until 2004. Considering this information, it is my determination that *Finite Elements in Analysis and Design* July 1998 and therefore “Process capability study and thermal fatigue life prediction of ceramic BGA solder joints” was made available to the public shortly after its initial publication in July 1998.

33. I have reviewed Exhibit 1016, *Critical Review and Technology Assessments '91-'92* by the Reliability Analysis Center.

34. Attached hereto as Appendix RAC01 is a true and correct copy of the MARC record for *Critical Review and Technology Assessments '91-'92* as held by the Linda Hall library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix RAC01 accurately describes the title, author, publisher, and ISBN number of *Critical Review and Technology Assessments '91-'92*. In comparing Exhibit 1016 to

Appendix RAC01, it is my determination that Exhibit 1016 is a true and correct copy of *Critical Review and Technology Assessments '91-'92* by the Reliability Analysis Center.

35. The 008 field of the MARC record in Appendix RAC01 indicates the date of record creation. The 008 field of Appendix RAC01 indicates the Linda Hall library first acquired this book as of January 19, 1993. Considering this information, it is my determination that *Critical Review and Technology Assessments '91-'92* was made available to the public shortly after its initial acquisition as of January 19, 1993.

36. I have reviewed Exhibit 1017, a document entitled "Performance Characteristics of IC Packages" as published in *2000 Packaging Databook* by Intel.

37. Attached hereto as Appendix INTEL2000 is a screen capture of the Internet Archive Wayback Machine entry for http://developer.intel.com/design/packtech/ch_04.pdf. I secured these screen captures myself from https://web.archive.org/web/20000901000000*/http://developer.intel.com/de

sign/packtech/ch_04.pdf. This web page contains a file named “ch_04.pdf”, a copy of “Performance Characteristics of IC Packages”.

38. In comparing Appendix INTEL2000 to Exhibit 1017, it is my determination that Exhibit 1017 is a true and correct copy of “Performance Characteristics of IC Packages” as published in *2000 Packaging Databook* by Intel.

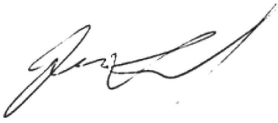
Considering Appendix INTEL2000 indicates “ch_04.pdf” was first preserved by the Internet Archive as of August 16, 2000, it is also my determination that “Performance Characteristics of IC Packages” was first available to the public by the Internet Archive as of August 16, 2000 if not earlier via the manufacturer.

39. I have been retained on behalf of the Petitioner to provide assistance in the above-illustrated matter in establishing the authenticity and public availability of the documents discussed in this declaration. I am being compensated for my services in this matter at the rate of \$200.00 per hour plus reasonable expenses. My statements are objective, and my compensation does not depend on the outcome of this matter.

40. I declare under penalty of perjury that the foregoing is true and correct. I hereby declare that all statements made herein of my own knowledge are

true and that all statements made on information and belief are believed to be true; and further that these statements were made the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: 6/4/2024

A handwritten signature in black ink, appearing to read 'June Ann Munford', with a stylized, flowing script.

June Ann Munford

APPENDIX CV

Education

University of Wisconsin-Milwaukee - MS, Library & Information Science, 2009
Milwaukee, WI

- Coursework included cataloging, metadata, data analysis, library systems, management strategies and collection development.
- Specialized in library advocacy, cataloging and public administration.

Grand Valley State University - BA, English Language & Literature, 2008
Allendale, MI

- Coursework included linguistics, documentation and literary analysis.
- Minor in political science with a focus in local-level economics and government.

Professional Experience

Researcher / Expert Witness, October 2017 – present
Freelance ● Pittsburgh, Pennsylvania & Grand Rapids, Michigan

- Material authentication and public accessibility determination. Declarations of authenticity and/or public accessibility provided upon research completion. Experienced with appeals and deposition process.
- Research provided on topics of public library operations, material publication history, digital database services and legacy web resources.
- Past clients include Alston & Bird, Arnold & Porter, Baker Botts, Fish & Richardson, Erise IP, Irell & Manella, O'Melveny & Myers, Perkins-Coie, Pillsbury Winthrop Shaw Pittman and Slayden Grubert Beard.

Library Director, February 2013 - March 2015
Dowagiac District Library ● Dowagiac, Michigan

- Executive administrator of the Dowagiac District Library. Located in

Southwest Michigan, this library has a service area of 13,000, an annual operating budget of over \$400,000 and total assets of approximately \$1,300,000.

- Developed careful budgeting guidelines to produce a 15% surplus during the 2013-2014 & 2014-2015 fiscal years while being audited.
- Using this budget surplus, oversaw significant library investments including the purchase of property for a future building site, demolition of existing buildings and building renovation projects on the current facility.
- Led the organization and digitization of the library's archival records.
- Served as the public representative for the library, developing business relationships with local school, museum and tribal government entities.
- Developed an objective-based analysis system for measuring library services - including a full collection analysis of the library's 50,000+ circulating items and their records.

November 2010 - January 2013

Librarian & Branch Manager, Anchorage Public Library ● Anchorage, Alaska

- Headed the 2013 Anchorage Reads community reading campaign including event planning, staging public performances and creating marketing materials for mass distribution.
- Co-led the social media department of the library's marketing team, drafting social media guidelines, creating original content and instituting long-term planning via content calendars.
- Developed business relationships with The Boys & Girls Club, Anchorage School District and the US Army to establish summer reading programs for children.

June 2004 - September 2005, September 2006 - October 2013

Library Assistant, Hart Area Public Library

Hart, MI

- Responsible for verifying imported MARC records and original MARC

cataloging for the local-level collection as well as the Michigan Electronic Library.

- Handled OCLC Worldcat interlibrary loan requests & fulfillment via ongoing communication with lending libraries.

Professional Involvement

Alaska Library Association - Anchorage Chapter

- Treasurer, 2012

Library Of Michigan

- Level VII Certification, 2008
- Level II Certification, 2013

Michigan Library Association Annual Conference 2014

- New Directors Conference Panel Member

Southwest Michigan Library Cooperative

- Represented the Dowagiac District Library, 2013-2015

Professional Development

Library Of Michigan Beginning Workshop, May 2008

Petoskey, MI

- Received training in cataloging, local history, collection management, children's literacy and reference service.

Public Library Association Intensive Library Management Training, October 2011

Nashville, TN

- Attended a five-day workshop focused on strategic planning, staff management, statistical analysis, collections and cataloging theory.

Alaska Library Association Annual Conference 2012 - Fairbanks, February 2012

Fairbanks, AK

- Attended seminars on EBSCO advanced search methods, budgeting, cataloging, database usage and marketing.

Depositions

2019 ● Fish & Richardson

Apple v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282 and 39521-00421IP2)

2019 ● Erise IP

Implicit, LLC v. Netscout Systems, Inc (Civil Action No. 2:18-cv-53-JRG)

2019 ● Perkins-Coie

Adobe Inc. v. RAH Color Technologies LLC (Cases IPR2019-00627, IPR2019-00628, IPR2019-00629 and IPR2019-00646)

2020 ● O'Melveny & Myers

Maxell, Ltd. v. Apple Inc. (Case No. 5:19-cv-00036-RWS)

2021 ● Pillsbury Winthrop Shaw Pittman LLP

Intel v. SRC (IPR2020-1449)

2022 ● Perkins-Coie

Realtek v. Future Link (IPR2021-01182)

2023 ● Fish & Richardson

Neuroderm Ltd. v. Abbvie, Inc (Case No. PGR2022-00040)

2023 ● Fish & Richardson

Nearmap US Inc. v. Pictometry International Corp. (IPR2022-00735)

2023 ● Fish & Richardson

Samsung Electronics v. MemoryWeb LLC (Case No. 39843-0136PS1)

2023 ● Pillsbury Winthrop Shaw Whitman LLP

Gravel Rating Systems v. Costco Wholesale Corp. (Civil Action No. 4:21-cv-149-ALM)

Limited Case and Clientele History

Alston & Bird

- Ericsson

v. Collision Communications (IPR2022-01233)

- Nokia

v. Neptune Subsea, Xtera (Case No. 1:17-cv-01876)

- Universal Electronics Inc

v. Roku Inc (IPR2022-00818)

Arnold & Porter

- Ivantis

v. Glaukos (Case No. 8:18-cv-00620)

- Samsung

v. Jawbone (Case No. 2:21-cv-00186)

Benesch Friedlander Coplan & Aronoff

- Voyis

v. Cathx (Case No. 5:21-cv-00077-RWS)

Erise I.P.

- Apple

- v. Ericsson Inc. (IPR2022-00715)
- v. Future Link Systems (IPRs 6317804, 6622108, 6807505, and 7917680)
- v. INVT (Case No. 20-1881)
- v. Navblazer LLC (IPR2020-01253)
- v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)
- v. Quest Nettech Corp (Case No. 2:19-cv-00118-JRG)
- v. Telefonaktiebolaget LM Ericsson (IPR2022-00275)

- Fanduel

- v. CGT (Case No. 19-1393)

- Garmin

- v. Phillips North America LLC (Case No. 2:19-cv-6301-AB-KS)

- Netscout

- v. Longhorn HD LLC (Case No. 2:20-cv-00349)
- v. Implicit, LLC (Civil Action No. 2:18-cv-53-JRG)

- Sony Interactive Entertainment LLC

- v. Bot M8 LLC (IPR2020-01288)
- v. Infernal Technology LLC (Case No. 2:19-CV-00248-JRG)

- Unified Patents

v. GE Video Compression (Civil Action No. 2:19-cv-248)

Fish & Richardson

- Apple

v. AliveCor (3:21-cv-03958)

v. LBS Innovations (Case No. 2:19-cv-00119-JRG-RSP)

v. Koss Corporation (IPR2021-00305)

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v. TQ Delta LLC (Case No. 18-1798)

- Evapco Dry Cooling

v. SPG Dry Cooling (IPR2021-00688)

- Genetec

v. Sensormatic Electronics (Case No. 1:20-CV-00760)

- Huawei

v. Bell Northern Research LLC (IPR2019-01174)

- Kianxis

v. Blue Yonder (Case No. 3:20-cv-03636)

- LG Electronics

v. Bell Northern Research LLC (Case No. 3:18-cv-2864-CAB-BLM)

- Metaswitch

v. Sonus Networks (IPR2018-01719)

- Microsoft

v. Throughputer Inc (IPR2022-00757)

- Mom Enterprises

v. Ddrops Company (Case No. 1:22-cv-00332)

- MLC Intellectual Property

v. MicronTech (Case No. 3:14-cv-03657-SI)

- Nearmap Inc

v. EagleView Technologies (IPR2022-01009)

- Neuroderm Ltd.

v. Abbvie, Inc (Case No. PGR2022-00040)

- Realtek Semiconductor

v. Future Link (IPR2021-01182)

- Quectel

v. Koninklijke Philips (Case No. 1:20-cv-01710)

- Samsung

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v. Jawbone Innovations (IPR2022-00865)

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- Curium

O'Melveny & Myers

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APPENDIX INTEL2000



INTERNET ARCHIVE

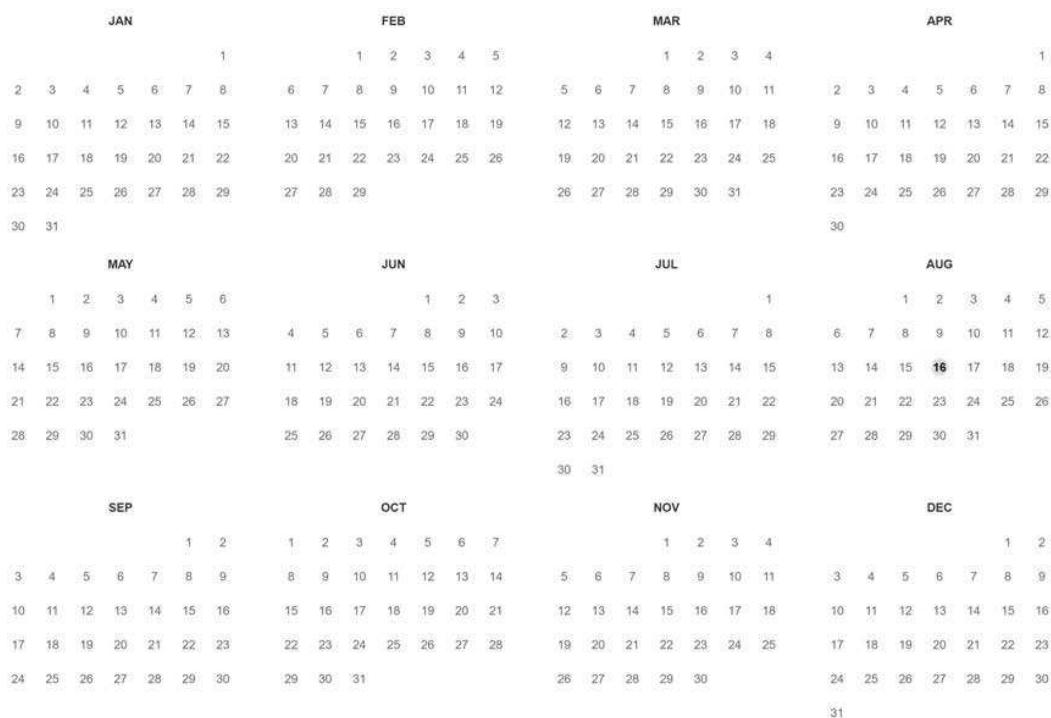
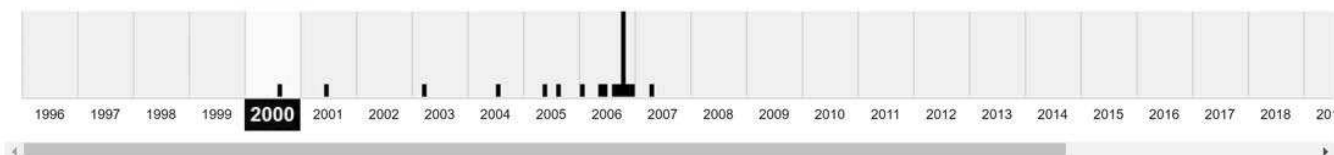
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Performance Characteristics of IC Packages

4

4.1 IC Package Electrical Characteristics

As microprocessor speeds have increased and power supply voltages have decreased, the function of the microprocessor package has transitioned from that of a mechanical interconnect which provides protection for the die from the outside environment to that of an electrical interconnect that affects microprocessor performance and which must be properly understood in an electrical context. Inherent in understanding the electrical performance effects of the package is the need for electrical characterization of the package. The package is a complex electrical environment and the characterization of this environment is a multi-faceted task that consists of models constructed from both theoretical calculations and experimental measurements.

In simple terms, a package electrical model translates the physical properties of a package into electrical characteristics that are usually combined into a circuit representation. The typical electrical circuit characteristics that are reported are DC resistance (R), inductance (L), capacitance

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In simple terms, a package electrical model translates the physical properties of a package into electrical characteristics that are usually combined into a circuit representation. The typical electrical circuit characteristics that are reported are DC resistance (R), inductance (L), capacitance (C), and characteristic impedance (Z_o) of various structures in the package. A package model consists of two parts, both of which are necessary for fully understanding the electrical performance effects of the package environment on Intel's microprocessors.

The first is an I/O lead model that describes the signal path from the die to the board. Depending upon the complexity of the model required for simulation purposes, the I/O lead model can take the form of a simple lumped circuit model, a distributed lumped circuit model, a single-conductor transmission-line model, or a multiple-conductor transmission-line model. While lumped models can adequately model simple effects, such as DC resistive voltage drop, more sophisticated models like the multiple-conductor transmission-line model include effects such as time delay and crosstalk.

The second part of a package model is a power-distribution network that describes the power scheme of the package. Like the I/O lead model, the sophistication of the power-distribution network can vary from a simple distributed lumped model to a complex circuit network called a PEEC (partial-element equivalent circuit) network. The simpler models can describe gross electrical characteristics of the power-distribution network, such as DC resistive drop for the entire package, whereas the more complex models enable the analysis of the effects of the power-distribution topology.

Experimental characterization of the package can include measurements of trace characteristics and power loop parasitics, to name a few of the package aspects that can be characterized. Experimental characterization is usually the final, validation stage of the package-design process. Care must be taken in determining the characteristics that are measured. If a comparison between measured and modeled data is to be made, then the same assumptions used in obtaining the theoretical package model must be replicated in the test environment.

The following sections provide an overview of basic package modeling terminology and methodology, an overview of experimental characterization, and modeled data for the packages that Intel uses for its most advanced microprocessors. These products are housed in packages representative of a broad spectrum of package technologies, including CPGA (ceramic pin-grid array), PPGA (plastic pin-grid array), H-PBGA (high thermal plastic ball grid array), TCP (tape carrier package), OLGA (organic land-grid array), and FC-PGA (flip-chip pin-grid array). For the

sake of completeness, package parasitics data for older package technologies are included in the final part of this section. The package types included are multilayer molded (MM-PQFP), ceramic quad flatpack (CQFP), plastic leaded chip carrier (PLCC), quad flatpack (QFP, SQFP, TQFP), and small outline packages (TSOP, PSOP). These packaging technologies are no longer used for Intel's leading-edge microprocessors but are still used for other products.

Since the packages used for Intel's microprocessors are custom designed for each product, the parameters given in the following sections may not reflect the actual values for a particular product. The actual parameters can be obtained by contacting a local Intel sales office. For electrical parameters of packages not listed, please contact your local Intel field sales office.

4.1.1 Terminology

4.1.1.1 DC Resistance (R)

The DC resistance (R) is normally the cause of IR voltage drops in the package. Reduction of DC resistance is particularly important in the power and ground paths. DC resistance is determined by the cross-sectional dimensions (width and thickness), material, and length of the lead. The DC resistance of an I/O lead with cross-sectional area, A, length, L, and resistivity, ρ , can be calculated using:

Equation 4-1.

$$R = \frac{\rho L}{A}$$

Ceramic packages have relatively high resistance because of the high resistivity of the tungsten alloy metallization used with ceramic technology. Plastic/organic packages have much lower resistance because the metallization used is either copper or a copper alloy. The resistivity of copper or copper alloys is approximately a factor of 6-12 lower than that of tungsten alloys.

4.1.1.2 Capacitance (C)

Capacitance (C) is determined by the lead length and cross-sectional dimensions, the spacing between leads, the spacing between the lead and the power or ground plane, the dielectric constant of the surrounding material, and the number of leads involved. The relative dielectric constant of the material used for ceramic packages is in the range of 8–10. The dielectric constant of the material used for plastic packages is in the range of 4–6. There are formulas for the capacitance of classic geometries; however, the capacitance for a particular structure in a package must usually be calculated using a software modeling tool. The formula for the capacitance of a parallel plate capacitor can be used to deduce the general relationship between geometry and capacitance. The capacitance for this structure, neglecting fringing fields, is:

Equation 4-2.

$$C = \frac{\epsilon A}{t}$$

where A is the area of one of the plates, ϵ is the permittivity of the material separating the plates, and t is the thickness of the material.

Capacitances which are important to package electrical performance are “loading” capacitance, “lead-to-lead” capacitance, and “decoupling” capacitance. The loading capacitance is the total capacitance of a lead with respect to all surrounding conductors. The lead-to-lead capacitance is the mutual capacitance between the two leads. The loading capacitances are the diagonal terms in the so-called “short-circuit” capacitance matrix, and the lead-to-lead capacitances are the off-diagonal terms. The lead-to-lead capacitance and the mutual inductance determine the extent of electromagnetic coupling between the two leads. Decoupling capacitance is the total capacitance between the power leads and the ground leads. In a ceramic PGA with power/ground planes, the decoupling capacitance is due to the capacitance between power and ground planes, as well as added discrete capacitors to the package. In plastic PGA packages, decoupling capacitance is usually provided by adding discrete capacitors to the package. Decoupling capacitance serves as a reservoir which provides part of the energy required when buffers switch. This reduces the AC voltage drop, also called the switching noise or the ground bounce, of the power/ground path.

4.1.1.3 Inductance

A simple definition of inductance (L) is the property of a conductor that describes the proportionality between current change and induced voltage. An inductor is any conductor across which there is a voltage drop when there is a time-varying current present. This aspect of a package is important in determining the extent of the effects of crosstalk and simultaneous switching noise. The classical definition of inductance implies that the inductance is that of a current loop, however, a loop can be segmented, and partial-self and partial-mutual inductances can be attributed to each segment. This is a useful concept for analyzing package AC noise and is widely used today. For example, a pin inductance is a partial-self inductance.

Another useful term is the “open-loop” inductance which is the inductance of a loop with gaps at two ends. We can visualize a segment of a transmission line as an open-loop and the total inductance of that segment as the open-loop inductance. Inductances used in analyzing behavior such as propagation delay and crosstalk of electrical interconnects are, in general, open-loop inductances.

When partial inductances are used in package electrical performance analysis, it is essential to understand the current direction in each segment. Wrong assumptions on current directions can lead to erroneous results. The term “current return path” is widely used to stress the importance of understanding the current direction in each segment involved.

The inductance values are determined by the lead length and cross-sectional dimensions, the spacing between leads, the spacing between the power or ground plane, the permeability of the conductor, and the number of leads involved. A general rule of thumb is that the smaller the entire current loop involved the lower the inductance. This is an important concept to be aware of when designing packages and systems, in general. Each signal needs to have a nearby, well-defined, and continuous return path. There are few simple formulas for inductance because the inductance is dependent upon both the physical geometry of the structure and the current return path. A few classic problems have been solved in closed form. Software codes that use electromagnetic analysis techniques are usually used to compute the inductance of the complex structures in packages.

4.1.1.4 Characteristic Impedance (Z_o)

Characteristic impedance (Z_o) is one parameter that is used to describe transmission-line structures, which are any structures consisting of two conductors - a signal conductor (lead) and a reference conductor, typically a power/ground plane. In package modeling, traces are usually described in terms of transmission-line parameters because this type of description inherently incorporates time delay. A model that consists of lumped circuit components cannot account for the time delay of the signal through the package.

The characteristic impedance of a line can be found using:

Equation 4-3.

$$Z_o = \sqrt{\frac{L}{C}}$$

L and C are per-unit-length values of the inductance and capacitance of the line, so Z_o is independent of line length.

Z_o is an important factor in determining the amount of signal reflection that will occur at the boundary between the die and the package and at the boundary between the package and the board. The amount of reflection and, thus signal distortion, is directly proportional to the amount of mismatch between Z_o 's at these boundaries. As an example, the Z_o of traces in FR-4 boards typically used for motherboards is around 50 ohms, so typical packaging technologies attempt to match this impedance as closely as possible. For example, a typical CPGA package has a 42-ohm trace impedance and a typical PPGA package has a 47-ohm impedance.

4.1.1.5 Crosstalk

Crosstalk refers to unwanted signal coupling between lines. It is a complex function of the driver and receiver characteristics, trace characteristics, and switching patterns. Some generalities regarding package design and its relationship to crosstalk can be made. Crosstalk in a package is dependent upon the stack-up, just as is characteristic impedance; however, crosstalk is primarily affected by the distance between traces and the amount of parallelism between them. The longer the parallel distance between two or more lines, the higher the crosstalk between them. Also, the closer the lines are to one another, the higher the crosstalk. The proximity of power/ground planes to the traces can help reduce crosstalk. That is, crosstalk is directly proportional to the distance between the planes above and below the trace. There are no simple formulas for predicting crosstalk. Models of the traces, with the mutual inductance and capacitance calculated, must be generated and simulations run using buffer models and models representing the system loads to correctly determine the amount of crosstalk in a package design or system.

4.1.1.6 Simultaneous Switching

A final concern in package and system design is the effect of simultaneous switching of signals. There are two items of concern when many signals switch simultaneously: noise generated on the power/ground planes and timing pushout of signals. The first item, power/ground noise, is usually referred to as "SSN", simultaneous switching noise, and is the noise generated in power/ground structures due to a changing current and inductive elements in the power delivery system. The second item is usually referred to as "SSO (simultaneous switching output) pushout." This is the difference in timing between single-bit and multiple-bit switching. System designers must budget for the worst-case switching case upfront in their design to insure a design that is robust enough to handle all switching cases. Analyses of SSN and SSO are very complex but critical to the overall design process. The general guideline to mitigate the impact of simultaneous switching is to insure that all signals have well-defined return paths with low inductance and to insure that the power delivery network has a low inductance. Models and simulations for simultaneous switching phenomenon are very complex and product dependent and, thus, will not be included in this document. Please contact your Intel field sales office for product-specific models.

4.1.2 Modeling Methodology

The exact format for a package model depends upon the model usage. For analyzing specific critical signals, it is necessary to model only a few I/O signal leads in a small section of the package. For designing a power supply scheme, it is necessary to model the power supply loop for the entire package. A complete package model consists of an I/O signal lead for a typical lead geometry plus power loop models for each isolated power supply in the package. The amount of detail included in the model and the exact format of the model are items that the packaging engineer must determine based upon assessments of the model usage and the system characteristics. The next few sections outline some of the issues that the packaging engineer must consider in creating an appropriate package electrical model.

4.1.2.1 I/O Signal Lead Model

The I/O signal lead model consists of the parasitics for a particular signal path in the package. For a wirebond, pin-grid array (PGA) package, the signal path includes the bondwire, the trace, vias, the pin, and the plating bar. Intel has migrated to flip-chip packaging (OLGA and FC-PGA) for its higher performance products. For these types of packages, the signal path includes the solder bump connection between the die and package, the trace, vias, and the pins or lands. If crosstalk is to be considered, then the cross-coupling parasitics for the nearest leads should also be included in the model. Ordinarily it is useful to analyze the lead both in isolation and in conjunction with the nearest traces on either side of the lead.

The key to providing an accurate I/O signal lead model is to identify the return current paths. For example, in analyzing the I/O signal lead bondwire inductance, the closest current return path is the nearest power or ground bondwire. If the effect of this bondwire is not included in the analysis, then the calculated I/O signal lead bondwire inductance will be higher than it actually is because the mutual effects of nearby wires have not been included. In analyzing the signal trace, it is necessary to identify the nearest current-carrying package planes that provide a current return path. In effect, signal traces are usually modeled as microstripline or stripline structures, where a microstripline structure is defined as a trace with one current-carrying plane in close proximity and a stripline structure is defined as a trace sandwiched between two current-carrying planes.

Unless a highly accurate model for a particular critical signal is required, the I/O signal lead model for a package is usually based upon the typical lead geometry. Crosstalk parameters are usually based upon the worst-case crosstalk scenario, i.e., the minimum trace spacing. Typically, the individual components comprising the signal lead are modeled individually using two and three dimensional solutions obtained using electromagnetic field-solving software. The primary parasitics of interest are the line characteristic impedance (Z_o), the line inductance (L), the line resistance (R), the line capacitance (C), and cross-coupling L and C matrices for crosstalk analysis. SSO models usually include mutual effects between signal lines and include the power distribution network effects. To obtain the level of accuracy and complexity required for SSO modeling, three-dimensional fully coupled models are necessary.

4.1.2.2 Power Loop Models

The power loop model consists of the structures used for power delivery in the package. Typically, all power and ground bondwires, vias, planes, and pins must be included along with mutual effects between structures in close proximity to one another. The format for the power loop model is not as straightforward as for the I/O signal lead model because of the complexity of the system. To accurately model the power loop, the entire package structure must be comprehended. This is an unwieldy task, so the packaging engineer must use approximations and partitioning of the package structure to simplify the model. The amount of complexity that is included depends upon the usage. A simple distributed lumped model may be sufficient for certain analyses; however, a more

complex model is usually required for making power distribution design decisions, such as determining the quantity and location of power and ground pins and bondwires and the quantity and location of decoupling capacitors.

A simple distributed model usually consists of a single resistor/inductor element to represent each major structure in the package. For example, all the power bondwires are considered to be parallel, equivalent resistive/inductive structures, so their parasitics are lumped into one resistor/inductor element. Similarly, all the pins and vias are lumped together, and each plane is represented as a single resistor and inductor. This is a highly simplistic model which assumes equal current flow through each pin. Although this is not a very accurate model, it is quite useful for obtaining an approximation for the total package resistance and inductance. To more accurately model the intricacies of the power distribution in the package, all elements must be represented by circuits that contain both self and mutual inductance and capacitance terms. This type of representation is typically called a PEEC (partial-element equivalent circuit) network and must be generated using software tools that solve electromagnetic field equations. The drawback of this type of model is that it consists of a large, complex circuit with many individual elements. The effects of various elements are not intuitively obvious, so circuit simulations must be run. Since the network is large, much computer memory and simulation time is required for this type of analysis.

4.1.2.3 Trade-Offs Between Accuracy and Complexity

Package modeling is both a science and an art. Ideally, one would like to be able to exactly and entirely model the package; however, this is extremely impractical, if not impossible. Both the amount of computational resources and the complexity of the final package model are prohibitive. On the other hand, using a very convenient approach of modeling the entire package as an R, L, C circuit whose parameter values are determined from closed form formulas is crudely simplistic. Somewhere between these extremes lies the realm in which the packaging engineer realistically must develop electrical models for the package.

Inherent in this development is the decision of how much loss in accuracy is acceptable in order to provide a convenient and usable model. This is a decision that is best made after experimentation to test for convergence of a model and, ideally, after comparison to measured data. In general, a single I/O lead model can be quite accurately constructed using two-dimensional approximations for the trace itself and even for the bondwire. Three-dimensional modeling is usually required for the pin and via. All these structures can be easily created and accurately analyzed using commercial software tools for solving electromagnetic field equations. Because of its complexity, there are more engineering approximations that must be made in constructing a model for the power supply loop. For example, a power plane may have a hundred vias connected to it; however, inputting this complex geometry into a software tool would be a time-consuming task. In addition, analyzing this type of geometry would require large quantities of computer memory and time. The accuracy lost in grouping vias together may be very small, i.e., one via could be used to represent ten vias in close proximity. After some practice and experimentation, one can learn to recognize opportunities for model simplification which will not overly compromise accuracy.

4.1.2.4 Lumped-Element Models versus Transmission-Line Models

One key choice that must be made in creating a package model is whether to represent package structures as lumped circuit elements or as transmission-line elements. The general guideline that is given throughout packaging literature is that a transmission-line model should be used if:

Equation 4-4.

$$t_r < 2t_o l$$

where $2t_o l$ is the round-trip delay in the medium in which the signal path lies and t_r is the risetime of the signal. As an example, a typical package trace in a ceramic package is around 1 inch long. Using a dielectric constant of 10 for ceramic, the round-trip delay is:

Equation 4-5.

$$2t_o l = 2 \times \sqrt{\epsilon_r \epsilon_o \mu_o} \times l = 2 \times \frac{\sqrt{\epsilon_r}}{c} \times l = 2 \times \frac{\sqrt{10}}{3 \times 10^{10} \text{ cm/s}} \times 2.54 \text{ cm/in.} \times 1 \text{ in.} = 0.54 \text{ ns}$$

This is the order of the risetimes for signals in today's microprocessors. Therefore, using a transmission-line model for traces in a package is an appropriate modeling decision.

Typically, a transmission-line model should be used for the trace and lumped models for the bondwires, pins, and vias. Most of the time delay in the package is due to the trace delay, and a transmission-line model for the trace will appropriately account for the time delay. A lumped model cannot account for time delay and should only be used when the delay through a structure is not a significant portion of the overall signal propagation delay. As risetimes decrease and propagation delays through the package become more critical, transmission-line models will be necessary for many structures in the package.

4.1.2.5 Frequency-Dependent Effects

Another choice that must be made in creating a package model is whether or not to include frequency-dependent effects. To briefly summarize the issue, at DC, current is evenly distributed across the cross-section of a conductor. At high-frequencies, the current is confined to the surface of the conductor. At frequencies in between DC and high-frequency, the current is confined to an area defined as the skin depth of the conductor. Skin depth is material-, geometry-, and frequency-dependent and decreases with increasing frequency. Because of the frequency dependence of the skin depth, the resistance and inductance of a conductor vary with frequency. The cross-sectional area through which current flows in a conductor is also affected by the presence of other conductors. This phenomenon is called the proximity effect.

It is usually adequate to simply model the DC resistance of a conductor in a package and to use high-frequency, or quasi-static inductance calculations to model the inductance. Because signal risetimes are decreasing with each new generation of microprocessor, however, the spectral content of typical signal waveforms is increasing and frequency-dependent effects are becoming more critical to accurate package analysis. For this reason, future package models should include both frequency-dependent resistance and inductance values. These parameters must be calculated using software tools which accurately perform a full-wave solution to Maxwell's equations, the equations which describe electromagnetic field interactions.

4.1.2.6 Power-Distribution Design Concepts

There are many applications for a complete and accurate package model. The obvious use is in analyzing signal distortion and delay through the package environment. A second area which is very important, but not as obvious, is in designing the power decoupling scheme for a package. For power-distribution design, there are a few general guidelines that should be mentioned. First, there

are two types of decoupling: low and high-frequency. Low-frequency decoupling is used on the board to typically control the noise from the power supply entering the board. High-frequency decoupling is used on the package and chip to control simultaneous switching noise.

When decoupling capacitors are placed on the package, they should be placed as close as possible to the die to minimize stray inductance associated with the connection between the capacitor and the die. It is important in using any type of decoupling capacitor to try to minimize the stray resistance and inductance associated with the interconnect and the capacitor itself. This is more important for high-frequency decoupling than low-frequency. In general, low-frequency decoupling schemes require large values of capacitance. Larger inductances are usually associated with larger capacitors. High-frequency capacitance values should be small to reduce the associated stray inductance.

The placement of decoupling capacitors affects the overall effective inductance; therefore, a fairly complex package model that allows analysis of the effects of capacitor placement is usually necessary for power-distribution design. The package model for this use, therefore, should take the form of a complex distributed model, or partial-element equivalent circuit (PEEC) model.

4.1.2.7 Modeling Tools

The theoretical values for package parameters are obtained at Intel by using in-house and commercial two-dimensional and three-dimensional modeling tools. The software calculates the inductance, capacitance, resistance, and characteristic impedance values based upon physical design parameters, such as geometry information and material properties, which are input using a CAD-based graphical interface. The user can usually input this information manually or use interface modules which can convert physical design databases for the package geometry into the appropriate format for the modeling tool.

Most of these tools are based upon numerical solutions of electromagnetic field equations, i.e., Maxwell's equations. The techniques used vary according to the software vendor. Some of the most common solution techniques include moment method, finite-element method, finite-difference time-domain technique, and boundary-element method. Although one need not be an expert, using commercially available software tools which use these techniques usually requires that one be somewhat knowledgeable about the basic theory behind the technique because additional user input is usually required to accurately solve for the parasitics. For example, the user is usually required to specify the meshing scheme used to divide the geometry for numerical analysis. One should also be aware of the limitations and requirements of the tool and technique used for solving for package parasitics or one could inadvertently produce data that is not useful or accurate. Some of the issues that should be understood are the limits on the types of geometries that can be analyzed, the assumptions concerning return-current paths, the assumptions concerning ground planes and ground conductors, and the underlying analysis algorithms.

4.1.3 Experimental Characterization Methodology

4.1.3.1 Equipment

The equipment necessary for characterizing the parasitics of a package falls into three categories. The first is measurement equipment, which is standard and available from several companies which specialize in the design and manufacture of this equipment. A well equipped laboratory should contain a D.C.-ohmmeter, an impedance analyzer, a network analyzer for frequency-domain characterization, and a time-domain reflectometry (TDR) set-up for time-domain characterization. The second category is test fixtures. These must be specially designed for the package and structure being characterized. Methods for de-embedding the test fixture from the

measurement must be devised. The third category is probes. Most package measurements involve probing very small structures with fixed pitches. Probes and calibration standards for these probes are available from companies which specialize in this area.

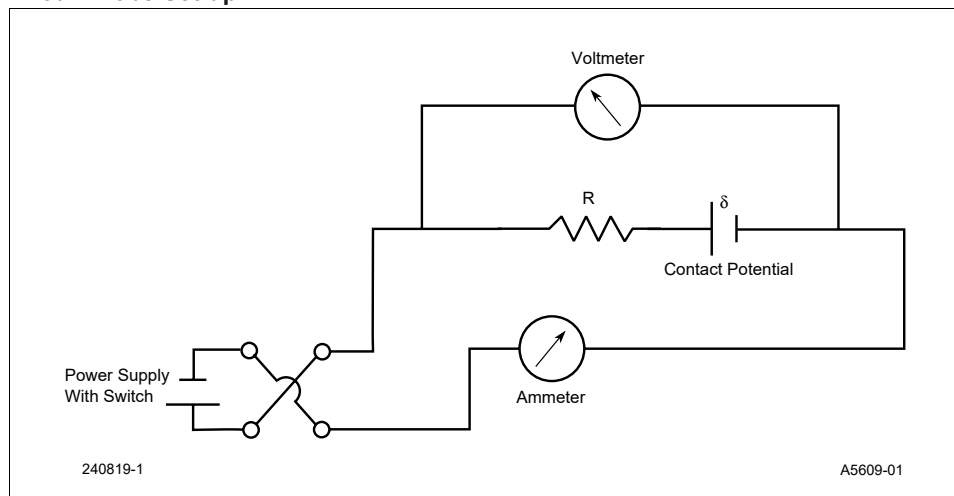
The following sections outline some of the basics for measuring I/O signal lead and power loop parasitics. It is impossible to cover the intricacies of measurement technique adequately in such a small space. Measurement methodology is continually evolving, and packaging engineers should remain in close contact with measurement equipment representatives and should keep up with conference proceedings and technical journals so that they are well informed concerning the latest and most accurate techniques. Regardless of the measurement technique, the packaging engineer should take care to model and measure the same scenarios if reliable validation data is to be obtained.

4.1.3.2 I/O Signal Lead Characterization

4.1.3.2.1 DC Resistance

The resistance for a given CPGA package is measured from the tip of the bond finger to the pin braze pad. The lead resistance for plastic packages is measured from tip to tip. Figure 4-1 shows the four-probe setup used to measure resistance values. Two sets of readings are taken by reversing the direction of current to eliminate the contact potential. The average value is considered the resistance of the sample.

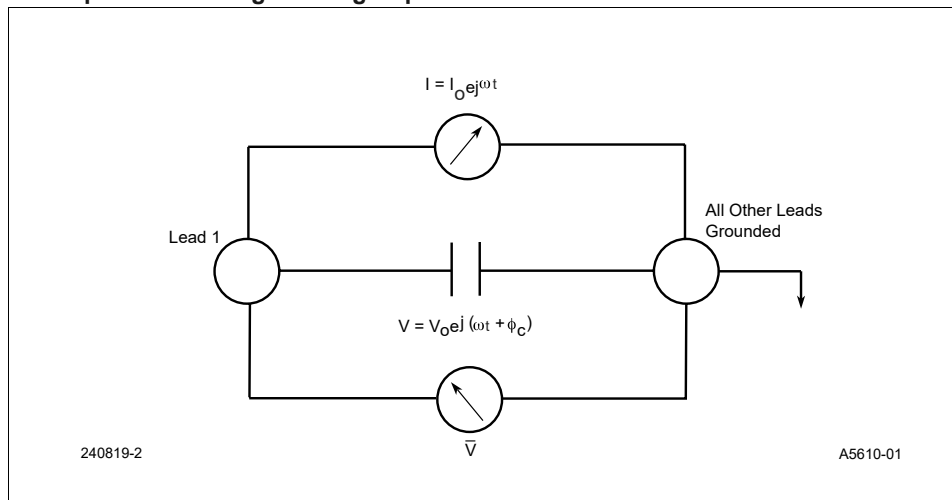
Figure 4-1. Four-Probe Set-up



4.1.3.2.2 Capacitance

Loading capacitances are measured using an impedance analyzer. The setup for measuring loading capacitance is shown symbolically in Figure 4-2. In this setup, all leads except the lead of interest are grounded. The capacitance is measured between this lead and ground. Decoupling capacitance is measured between a power lead and a ground lead.

Figure 4-2. Set-up for Measuring Loading Capacitance



4.1.3.2.3 Inductance

Like capacitances, inductances are measured using an impedance analyzer. The inductance measurement is a rather complicated process which involves sophisticated fixturing and de-embedding techniques. Typically, measuring inductance is quite difficult because the test method and fixture can affect the outcome of the measurement. One method of indirectly extracting the inductance is to measure the characteristic impedance (Z_0) and self-capacitance, which can be more accurately measured, and to determine the inductance using:

Equation 4-6.

$$L = C \times Z_0^2$$

4.1.3.2.4 Characteristic Impedance

Characteristic impedance (Z_0) for a signal trace can be measured using time-domain reflectometry (TDR). It is important in performing this measurement to identify the return-current path. If the proper return path is identified and incorporated into the measurement, this technique is highly accurate and can be used to extract the trace inductance.

4.1.3.3 Power Loop Characterization

Power loop characterization typically requires special test fixtures and de-embedding techniques. The standard characterization method is to use an impedance analyzer; however, inductance measurements using this technique are not very accurate. Newer techniques are being developed which involve using a network analyzer to perform frequency-domain characterization. Curve-fitting is used to match an equivalent circuit model to the frequency-domain response. In this way, package parasitics can be extracted. Regardless of the measurement equipment, the methodology usually involves shorting all the power elements together and shorting all the ground elements together using a test fixture designed for the particular package that is being characterized. In this way, the parasitics for the entire power supply loop can be extracted.

4.1.4 Product Package Models for Intel's Leading-Edge Microprocessors

The following sections contain data describing the parasitics for the packages for Intel's most recent microprocessors. The I/O signal lead, power loop, and crosstalk models for TCP, CPGA, PPGA, H-PBGA, OLGA, and FC-PGA packages are given. All values are calculated values based upon the final package design and calculated using commercially available software tools. The values given for the I/O signal lead models are given as ranges of values for the bondwires and as per-unit-length parasitics for the traces. The ranges for trace lengths in the package are also given. The power loop model is based upon the typical package and microprocessor design. Crosstalk models account for coupling between the closest signals on either side of the signal of interest. All transmission-line models and inductance values are calculated assuming high-frequency conditions, i.e., assuming that current flows on the exterior of the conductor only. Resistance values are calculated at DC. Transmission line models are used where necessary, and mutual effects of nearby current-return paths are incorporated into the final parasitic values. For example, the inductance of a bondwire is calculated by considering the particular location of the bondwire with respect to current-return paths. The inductance is not calculated assuming an isolated bondwire. For assistance in constructing models for specific leads in a package, contact your local Intel field sales office for information pertaining to the lead of interest.

4.1.4.1 I/O Signal Lead Models

A single I/O lead in a package is modeled as a circuit consisting of representative elements for the bondwire, the trace, the pin or land, and the plating trace. Bondwires, pins, and lands are modeled as series resistors and inductors. The signal and plating traces are represented by transmission lines with per-unit-length resistance (R), inductance (L), and capacitance (C) or with characteristic impedance (Z_0). Figure 4-3 illustrates the generic I/O lead model for any multilayer package technology. This circuit can be used to describe a specific package technology by changing the parasitic values to match the technology. Table 4-1 lists the typical parasitics for the CPGA, PPGA, H-PBGA, OLGA, and FC-PGA packages. The values listed assume that the package is mounted on the motherboard using a socket, so the pin/land parasitics include the socket effects as well as connecting via parasitics inside the package. For flip-chip packages (OLGA and FC-PGA), the bondwire is replaced by the die bump and connecting via and there are no plating traces. The values given in this section are for typical cases only. For more accurate data for simulations for specific signals on specific products of interest, contact your local Intel field sales office.

Figure 4-3. Package I/O Signal Lead Model for Multilayer Packages

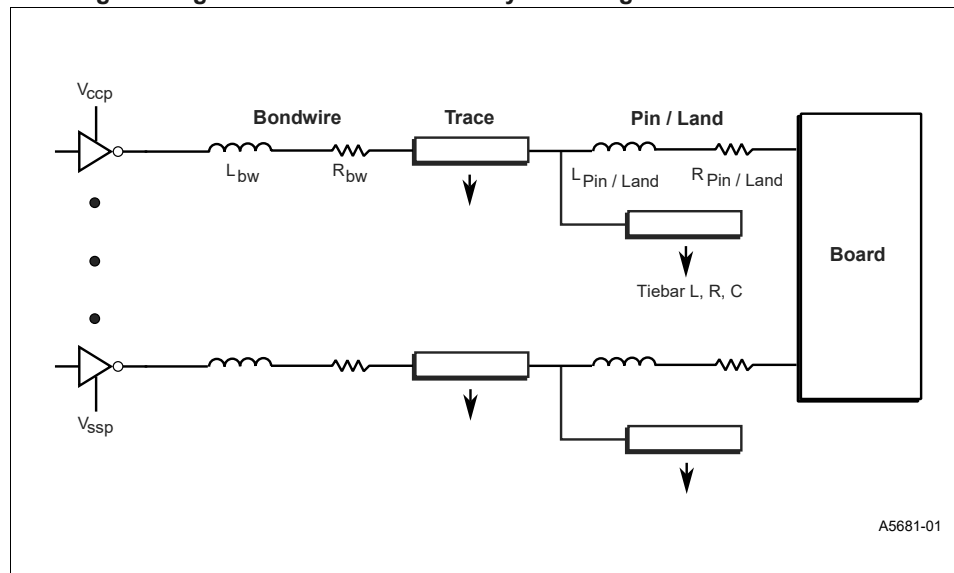


Table 4-1. Summary of Package I/O Lead Electrical Parasitics for Multilayer Packages

Electrical Parameter	Wirebond Package Type			Flip-chip Package Type	
	CPGA	PPGA	H-PBGA	OLGA	FC-PGA
Bondwire/Die bump R (mohms)	126 - 165	136 - 188	114 - 158	2	0.06
Bondwire/Die bump L (nH)	2.3 - 4.1	2.5 - 4.6	2.1 - 4.1	0.02	0.013
Trace R (mohms/cm)	1200	66	66	590	120
Trace L (nH/cm)	4.32	3.42	3.42	3.07	2.329
Trace C (pF/cm)	2.47	1.53	1.53	1.66	1.707
Trace Z ₀ (ohms)	42	47	47	43	38.5
Pin/Land R (mohms)	20	20	0	8	20
Pin/Land L (nH)	4.5	4.5	4.0	0.75	2.9
Plating Trace R (mohms/cm)	1200	66	66	N/A	N/A
Plating Trace L (nH/cm)	4.32	3.42	3.42	N/A	N/A
Plating Trace C (pF/cm)	2.47	1.53	1.53	N/A	N/A
Plating Trace Z ₀ (ohms)	42	47	47	N/A	N/A
Trace Length Range (mm)	8.83 - 26.25	6.60 - 42.64	4.41 - 22.24	3.0 - 18.0	10.0 - 42.6
Plating Trace Length Range (mm)	1.91 - 10.50	1.91 - 16.46	0.930 - 8.03	N/A	N/A

Because the geometry of TCP packages is very different from that of multilayer packages, another circuit representation for the package model must be used. This is shown in Figure 4-4. The model consists of three transmission lines with different parasitics that represent different portions of the signal path through the package. Typical TCP parasitics are given in Table 4-2.

Figure 4-4. Package I/O Signal Lead Model for TCP Packages

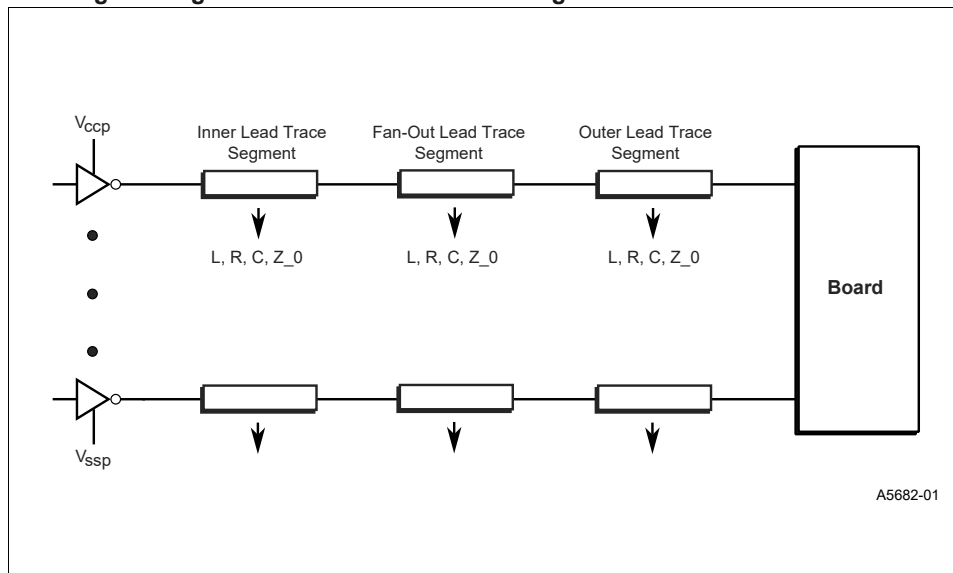


Table 4-2. Summary of Package I/O Lead Electrical Parasitics for TCP Packages

Electrical Parameter	Trace Segment		
	Inner Lead Segment	Fan-Out Lead Segment	Outer Lead Segment
Trace Segment R (mohms/cm)	352	290	144
Trace Segment L (nH/cm)	6.48 - 8.84	6.43 - 8.81	7.56 - 9.77
Trace Segment C (pF/cm)	0.58 - 0.83	0.13 - 0.19	0.12 - 0.16
Trace Segment Z_0 (ohms)	89 - 124	183 - 256	220 - 288
Trace Segment Length Range (mm)	0.90 - 4.0	0.05 - 11.8	0.91 - 3.25

4.1.4.2 Power Loop Models

There are many different methods of representing the power loop parasitics in a package model. As a general rule, the more distributed the model, the more accurate the model. As a comparative tool, however, this type of model is not very useful. To provide a simple model by which the overall power loop parasitics of different packaging technologies can be compared, the model shown in Figure 4-5 is used here. The overall inductance and resistance of the power loop for the core (V_{cc} and V_{ss}) power supply have been calculated and are given in Table 4-3. As in the previous section, the parasitic values for the multilayer packages include the effects of a socket. This is a highly simplistic model but a good one for comparing the different packaging types. For more accurate data for simulations, contact your local Intel field sales office

Figure 4-5. Package Core Power Loop Model

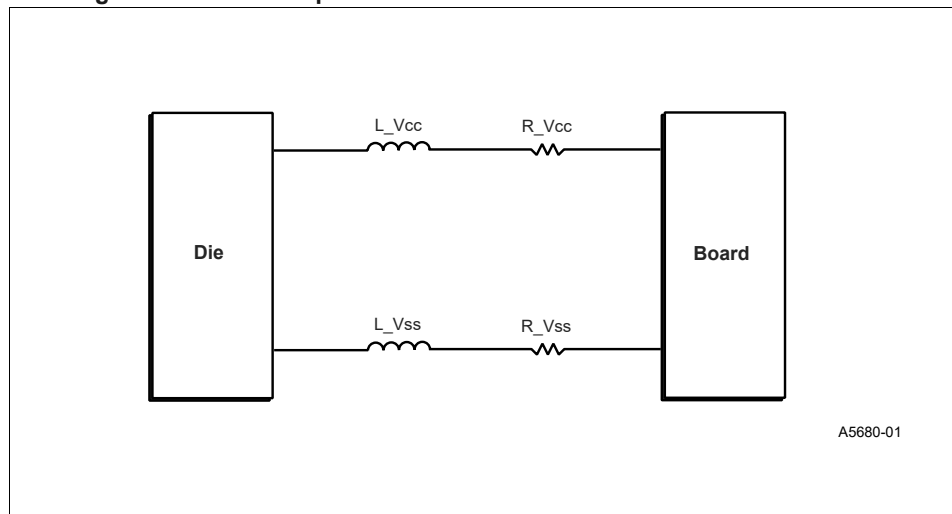


Table 4-3. Summary of Package Core Power Loop Electrical Characteristics

Electrical Parameter	Package Type					
	CPGA	PPGA	TCP	H-PBGA	OLGA	FC-PGA
R_Vcc (mohms)	5.5	2.0	6.0	4.1	0.5	1.2
L_Vcc (pH)	150	150	150	217	15	64.4
R_Vss (mohms)	5.5	2.0	6.0	4.1	0.5	1.2
L_Vss (pH)	150	150	150	198	15	64.4

4.1.4.3 Cross Talk Models

As devices migrate to lower voltage designs and smaller packages, the detrimental effects of crosstalk become more pronounced. Care must be taken in package design to minimize and quantify crosstalk. To simulate the effects of crosstalk, an appropriate model is needed. The model included in this handbook, Figure 4-6, is for coupling between three parallel signal leads located at minimum spacing for the package technology from one another. Figure 4-6 illustrates the numbering convention and placement of the signal leads. Table 4-4 gives the inductive coupling coefficients, and Table 4-5 gives the capacitive coupling coefficients for the CPGA, PPGA, TCP, H-PBGA, OLGA, and FC-PGA packages. Note that the mutual terms have negative signs, which is the convention for the “short-circuit” matrix representation. These values are for typical cases only. For more accurate data for simulations for specific signals of interest, contact your local Intel field sales office.

Figure 4-6. Package Crosstalk Model

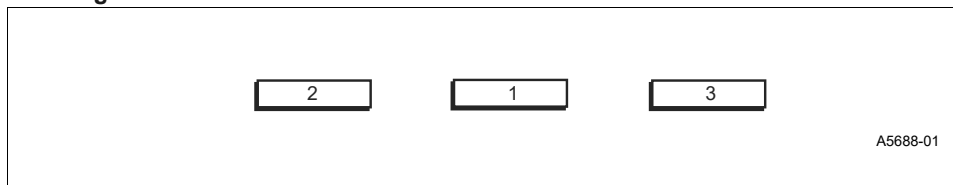


Table 4-4. Summary of Package Crosstalk Inductive Coupling Coefficients

Electrical Parameter	Package Type					
	CPGA	PPGA	TCP	H-PBGA	OLGA	FC-PGA
L11 (nH/cm)	4.26	3.39	5.71	3.39	3.2	2.329
L22 (nH/cm)	4.30	3.42	4.94	3.42	3.15	2.329
L33 (nH/cm)	4.30	3.42	4.94	3.42	3.15	2.329
L12 (nH/cm)	0.79	0.46	2.43	0.46	0.85	0.214
L13 (nH/cm)	0.79	0.46	2.43	0.46	0.85	0.214
L23 (nH/cm)	0.18	0.082	1.33	0.082	0.31	0.055
L31 (nH/cm)	0.79	0.46	2.43	0.46	0.85	0.214
L21 (nH/cm)	0.79	0.46	2.43	0.46	0.85	0.214
L32 (nH/cm)	0.18	0.082	1.33	0.082	0.31	0.055

Table 4-5. Summary of Package Crosstalk Capacitive Coupling Coefficients

Electrical Parameter	Package Type					
	CPGA	PPGA	TCP	H-PBGA	OLGA	FC-PGA
C11 (pF/cm)	2.80	1.60	1.25	1.60	1.65	1.707
C22 (pF/cm)	2.68	1.56	1.23	1.56	1.75	1.707
C33 (pF/cm)	2.68	1.56	1.23	1.56	1.75	1.707
C12 (pF/cm)	-0.49	-0.21	-0.48	-0.21	-0.33	-0.126
C13 (pF/cm)	-0.49	-0.21	-0.48	-0.21	-0.33	-0.126
C23 (pF/cm)	-0.022	-0.0092	-0.094	-0.0092	-0.001	-0.008
C31 (pF/cm)	-0.49	-0.21	-0.48	-0.21	-0.33	-0.126
C21 (pF/cm)	-0.49	-0.21	-0.48	-0.21	-0.33	-0.126
C32 (pF/cm)	-0.022	-0.0092	-0.094	-0.0092	-0.001	-0.008

4.1.4.4 SSO Models

Models and simulations for simultaneous switching phenomenon are very complex and product dependent and, thus, will not be included in this document. Please contact your Intel field sales office for product-specific models.

4.1.5 Package Models for Mature Package Technologies

To meet the performance requirements of Intel's microprocessors for future silicon technology generations, Intel's package technologies are evolving toward complex, multilayer plastic structures with copper traces and planes. Some of Intel's older microprocessor products do not require these advanced package technologies. For many embedded microcontroller applications

involving mature silicon technologies, older, more mature package technologies are the appropriate choice. Table 4-6 through Table 4-12 give the package parasitics for some of the older packages. Although they are not used for Intel's leading-edge microprocessors, they are routinely used for other Intel products. As with all the packages discussed in this chapter, the parameters given in the following sections may not reflect the actual values for a particular product. These are typical values only. The actual parameters for a particular product can be obtained by contacting a local Intel sales office. For electrical parameters of packages not listed, contact your local Intel field sales office.

Table 4-6. Summary of CQFP Electrical Data

Electrical Parameter	Lead Count	
	164L	196L
L_{lead} (nH)	3.3	3.3
R_{lead} (Ω)	0.004	0.004
$L_{\text{Trace(I/O)}}$ (nH)	5.0	6.0
$R_{\text{Trace(I/O)}}$ (Ω)	0.8	0.9
C_{load} (pF)	4.0	5.0
$L_{\text{Trace(Vcc/Vss)}}$ (nH)	1.5	2.5
$R_{\text{Trace(Vcc/Vss)}}$ (nH)	0.2	0.4
L_{wire} (nH)	3.0	3.0
R_{wire} (W)	0.08	0.08
$C_{\text{(Vcc Plane to Vss Plane)}}$ (pF)	170.0	240.0

Table 4-7. Summary of MM Packages

Electrical Parameter	Lead Count			
	132 Lead MM		196 Lead MM	
	Min	Max	Min	Max
I/O				
$R_{\text{Wire + Lead}}$ (m Ω)	81	106	83	115
$L_{\text{Wire + Lead}}$ (nH)	6.6	8.3	7.6	10.2
C_{Load} (pF)	0.5	1.3	0.7	2.2
Vss and Vcc				
$R_{\text{Vss db Wire}}$ (m Ω)	34	34	34	34
$L_{\text{Vss db Wire}}$ (nH)	1.1	1.1	1.1	1.1
$L_{\text{Vss Plane}}$ (nH)	0.2	0.2	0.3	0.3
C_{Plane} (nF)	0.090	0.090	0.210	0.210
$R_{\text{Vcc db Wire}}$ (m Ω)	55	55	55	55
$L_{\text{Vcc db Wire}}$ (nH)	1.9	1.9	1.9	1.9
$L_{\text{Vcc Plane}}$ (nH)	0.2	0.2	0.3	0.3
$R_{\text{Lead to Pin}}$ (m Ω)	9	10	10	12
$L_{\text{Lead to Pin}}$ (m Ω)	3.8	4.2	4.7	5.3

NOTE: db = Down bond

Table 4-8. Summary of PQFP Electrical Data

Electrical Parameter	Lead Count							
	84 Lead PQFP		100 Lead PQFP		132 Lead PQFP		164 Lead PQFP	
	Min	Max	Min	Max	Min	Max	Min	Max
R _{Wire + Lead} (mΩ)	62.9	106.4	64.9	108.8	63.2	112.8	65.8	116.9
L _{Wire + Lead} (nH)	5.3	9.8	5.9	10.6	5.4	11.9	6.2	13.2
C _{Load} (pF)	0.2	0.6	0.3	0.7	0.2	0.9	0.3	1.0

Table 4-9. Summary of PLCC Electrical Data

Electrical Parameter	Lead Count							
	28 Lead PLCC		32 Lead PLCC		44 Lead PLCC		68 Lead PLCC	
	Min	Max	Min	Max	Min	Max	Min	Max
R _{Wire + Lead} (mΩ)	56.7	74.0	56.9	74.3	57.7	75.6	57.7	78.4
L _{Wire + Lead} (nH)	4.1	7.1	4.2	7.3	5.0	8.4	5.0	10.3
C _{Load} (pF)	0.2	0.6	0.2	0.7	0.3	0.8	0.3	1.2

Table 4-10. Summary of QFP Electrical Data

Electrical Parameter	Lead Count					
	44 Lead PLCC		64 Lead PLCC		80 Lead PLCC	
	Min	Max	Min	Max	Min	Max
R _{Wire + Lead} (mΩ)	60.9	102.3	60.9	102.0	61.8	108.6
L _{Wire + Lead} (nH)	4.8	8.7	4.8	8.6	5.1	10.8
C _{Load} (pF)	0.1	0.4	0.1	0.4	0.1	0.6

Table 4-11. Summary of SQFP/TQFP Electrical Data

Electrical Parameter	Lead Count									
	80 Lead SQFP		100 Lead SQFP		144 Lead TQFP		176 Lead TQFP		208 Lead SQFP	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
R _{Wire + Lead} (mΩ)	61.5	82.6	61.8	84.6	69.5	98.1	69.5	103.7	69.5	122.6
L _{Wire + Lead} (nH)	4.0	6.4	4.1	6.9	5.2	8.7	5.2	9.8	6.3	12.6
C _{Load} (pF)	0.2	0.4	0.2	0.5	0.3	0.7	0.3	0.8	0.4	1.0

Table 4-12. Summary of SOP Electrical Data

Electrical Parameter	Lead Count / Package Type					
	32L TSOP			40L TSOP	56L TSOP	44L PSOP
	28F010	28F001BX	28F020	28F008SA	28F016	28F008SA
L (nH)	6.86 - 7.84		5.05 - 5.95	3.62 - 4.28	4.44 - 5.39	6.57 - 11.05
Pin C (pF)	8 - 12					
Lead-to-Lead C (pF)	0.80 - 0.94		0.59 - 0.73	0.38 - 0.40	0.45 - 0.50	2.09 - 3.32

4.2 IC Package Mechanical Characteristics

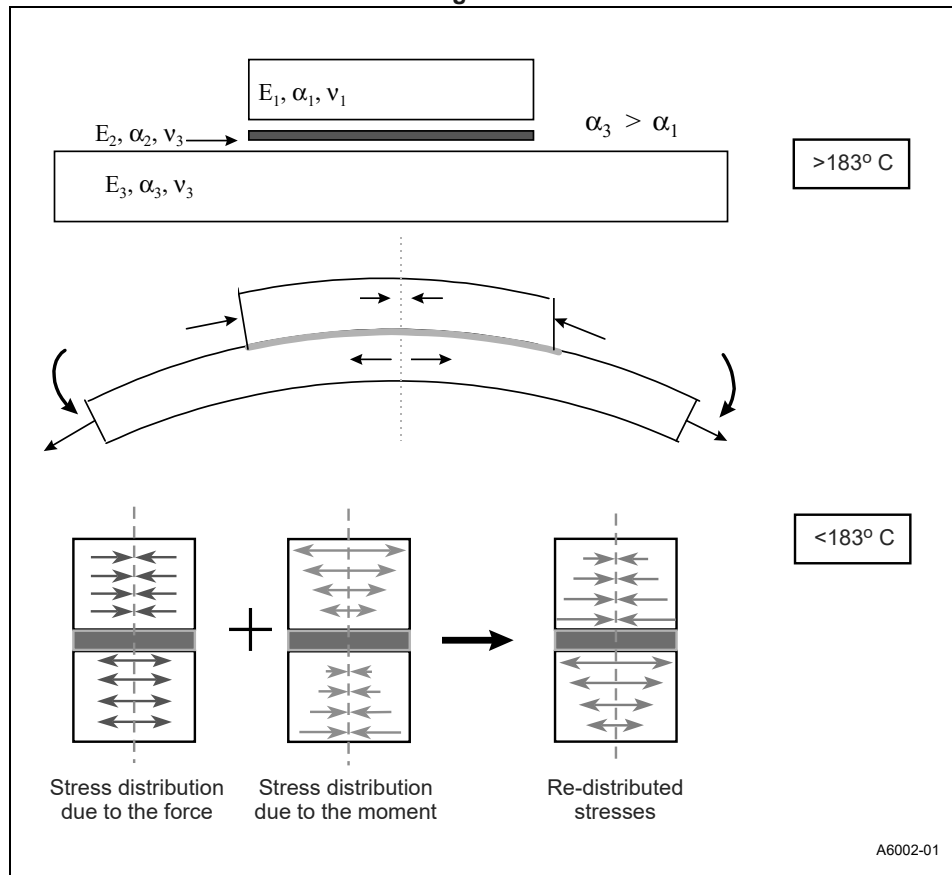
A typical electronic package assembly consists of different materials which are attached together in a variety of ways. The coefficient of thermal expansion mismatch between these different materials induces stresses in the attached components during manufacture and in operation. Flexing of a card, or other types of mechanical loads on the card with surface mounted components attached to it causes stresses to be induced in the surface mounted joints. Irrespective of the origin of the stress, when these stresses exceed the strength of the material, a crack initiates at the weakest point. After initiation, the crack propagates until complete failure occurs. Depending on the material and the location at which failure initiates, loss of functionality of the component (electrical or mechanical) can take different periods of time. The manufacturing process typically introduces many small flaws at different regions of the component. Crack initiation usually occurs at these pre-existing flaws at high stress locations in the component. Typical causes of failure of electronic packages are briefly discussed below.

Intel optimizes its packages through design, construction, material selection, and processes to insure that mechanical characteristics are acceptable. Packages then go through extensive testing and qualification.

4.2.1 Stresses generated during a thermal excursion

Structures used in microelectronic assemblies are constructed from materials that have a wide range of thermal expansion properties. This thermal expansion mismatch at an interface of two or more materials of different CTE's cause stresses to be developed in the materials during a thermal excursion. At the device level, oxide passivation layers and metallic interconnect lines on silicon are good examples of multi-material interfaces. The oxidation and deposition temperatures used to construct these structures are different from the temperatures at which subsequent fabrication steps are carried out, and different from the temperature at which the device will be operated. The packaging of fabricated devices introduces similar problems at a different scale. Ceramics or organics used as chip carriers to provide a stable operating environment for the active elements of a structure, introduce stresses due to a CTE mismatch with the silicon.

Figure 4-7. Schematic of Thermal Stresses During Reflow



Consider the simplified case of attaching a silicon die to an organic substrate using a thin layer of eutectic lead tin solder, as depicted in Figure 4-7. The melting temperature of eutectic lead tin is about 183°C . Therefore, at 183°C or higher, the individual materials are free to expand independently. While cooling the assembly down (at temperatures below 183°C), the solder layer solidifies, adhering the silicon and the organic substrate rigidly at the mating surfaces. Relative motion is thereby prevented between the mating surface of the silicon and the substrate, forcing them to contract together. However, the organic substrate which has a larger CTE than the silicon, would want to contract more. Compressive forces are therefore, induced on the die and tensile forces on the substrate. These opposing forces constitute a moment forcing the assembly to bend in a convex shape when viewed from the top. This bending has a significant effect on the distribution of stresses in the attached layers. Due to the bending, tensile stresses are introduced on the top of the die and compressive stresses on the bottom of the substrate. For elastic layers, the stress distribution can easily be calculated. The location along the thickness where the direction of the stress changes would depend upon the relative magnitudes to the two components of the stress. In some cases, there are actually more than one neutral axis along the thickness. The actual stress distribution in the assembly may vary from those calculated from an elastic model due to the viscoelastic nature of the adhesive layer. Further die edge shear stresses are present to balance the forces on the center regions of the assembly. As a result high stresses occur locally at the die edges.

In general, there are three primary stresses that exist at the interfaces of the assembly after reflow—normal stresses, shear stresses, and peeling stresses. All these stresses vary along the length of the interface, and their magnitudes depend upon the stiffnesses of the individual components being attached. Normal stresses have a maximum value almost over the entire center regions of the assembly, and drop to zero at the edges. Shear stresses have a maximum magnitude at the edges of the die. Peeling stresses change directions along the length of the die, and have a maximum magnitude close to the edge of the die. There are a number of analytical formulations based on Timoshenko's theory of bi-metallic thermostats, that predict the stress distribution for a tri-material assembly. Most of these formulations (though some account for limited adhesive non-linearity) are derived for elastic material behavior. However, these analytical relations are very useful to understand the fundamentals of thermal stresses in a tri-material assembly, and the relative influences of different design parameters and material properties on their stress state.

One set of analytical relations developed by Suhir E. [1], for a tri-material assembly when the thickness or the modulus of the adhesive material is small are of the form:

Equation 4-7.

$$\begin{aligned}\sigma_{die} &= \frac{F_{die,max}}{h_{die}} + \frac{6M_{die,max}}{h_{die}^2} = -\frac{\Delta\alpha\Delta T}{\lambda h_{die}} \left(1 + 3\frac{h}{h_{die}} \frac{D_{die}}{D}\right) \chi(x) \\ \sigma_{sub} &= -\frac{F_{sub,max}}{h_{sub}} - \frac{6M_{sub,max}}{h_{sub}^2} = -\frac{\Delta\alpha\Delta T}{\lambda h_{sub}} \left(1 + 3\frac{h}{h_{sub}} \frac{D_{sub}}{D}\right) \chi(x) \\ \tau_{sol} &= \kappa \frac{\Delta\alpha\Delta T}{\lambda} \chi'(x)\end{aligned}$$

where:

F_{die} , F_{sub} , M_{die} and M_{sub} are the forces and moments acting on the die and the substrate due to the CTE mismatch between them.

E , G , and ν , are the elastic modulus, shear modulus, and the poisson's ratio of the three materials.

$\Delta\alpha$ is the CTE mismatch between the die and the substrate ($\alpha_{sub} - \alpha_{die}$).

h_{die} , h_{sub} , and h are thickness of die, substrate and the assembly ($h_{die} + h_{sol} + h_{sub}$).

λ is the axial compliance of the assembly.

Equation 4-8.

$$\lambda = \frac{1-\nu_{die}}{E_{die}h_{die}} + \frac{1-\nu_{sub}}{E_{sub}h_{sub}} + \frac{h^2}{4D}, \quad D = \frac{E_{die}h_{die}^3}{12(1-\nu_{die}^2)} + \frac{E_{sub}h_{sub}^3}{12(1-\nu_{sub}^2)}$$

Here, D is the flexural rigidity of the assembly and k is the interfacial compliance of the assembly

Equation 4-9.

k is a parameter of the assembly stiffness which is a function of the axial and the interfacial compliances.

$$\kappa = \frac{h_{die}}{3G_{die}} + \frac{2h_{sol}}{3G_{sol}} + \frac{h_{sub}}{3G_{sub}}$$

Equation 4-10.

$$k = \sqrt{\frac{\lambda}{k}}$$

The functions $\chi^{(x)} = 1 - \frac{\cosh(kx)}{\cosh(kl)}$, and $\chi^{(x)} = \frac{\sinh(kx)}{\cosh(kl)}$ characterizes the longitudinal distribution of forces from the center to the edge of the interface(l).

Figure 4-8. Comparison of analytically and numerically calculated stresses along the length of the die.

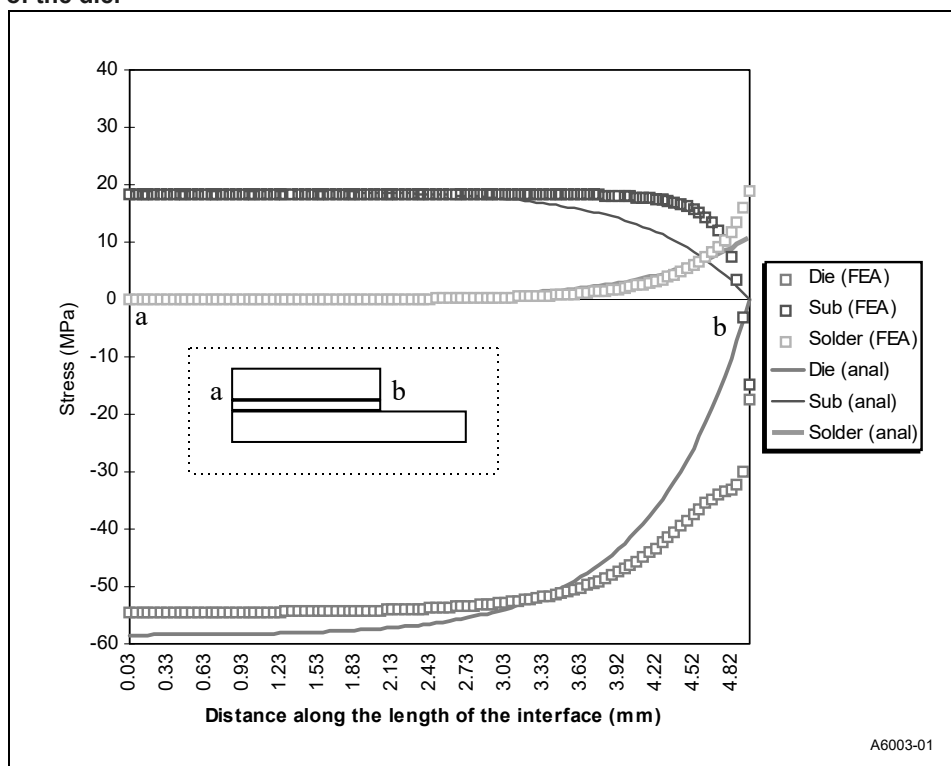


Figure 4-8 compares the normal stress in the die and the substrate, and the shear stress in the solder joint, obtained using these relations to those obtained numerically using a finite element model. The material properties and the design dimensions used for this comparison are listed in Table 4-13.

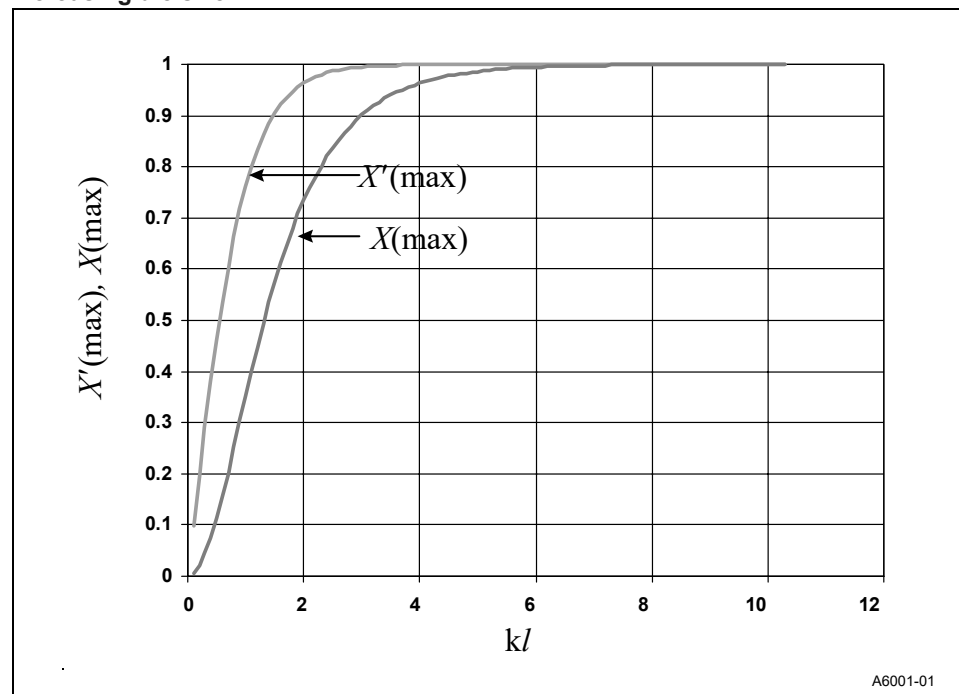
Table 4-13.

	E (GPa)	α (ppm/°C)	ν	Thickness (mm)	Half Length (mm)
Die	130	3.2	0.3	0.7	5
Solder	6.2	27	0.3	0.05	5
Substrate	17	16	0.3	1.65	10

Note that for the most part, the results match well.

The following general conclusions can be made from the analytical equations for the stresses in the assembly.

Figure 4-9. Variation of the maximum shear stress and normal stress with increasing die size



- The factors $\chi'(x)$ and $\chi(x)$ describes the longitudinal distribution of shear and normal stresses along the length of the interface. The maximum shear stresses occur at the end (at $x = l$) where the function $\chi'(x)$ has the value:

$$\chi'(l) = \chi'(max) = \frac{\sinh(kl)}{\cosh(kl)} = \tanh(kl)$$

and the maximum normal stress occurs at the center where:

$$\chi(0) = \chi(max) = 1 - \frac{1}{\cosh(kl)}$$

Figure 4-9 shows the variation of these two factors for increasing values of kl . From Figure 4-9, it is evident that increases with kl , for values of kl less than 3.5, and increases with kl for

values of k/l less than about 7.5. This indicates that for the die/solder/substrate assembly considered, σ_{die} and $\sigma_{\text{substrate}}$ increases with increasing die size for $k/l < 7.5$ (ie $2/l < 19.5$ mm), and t_{solder} increases with die size for $k/l < 3.5$ (ie $2/l < 5.5$ mm). For die sizes greater than 19.5 mm square (and 5.5 mm square for shear stress), the normal stress in the die and the substrate, and the shear stress in the solder layer will remain unchanged. For die and substrates of different thicknesses and properties than that considered here, the size of the die beyond which the stresses will remain unchanged, will be different.

- The coefficient of thermal expansion of the attachment material does not enter into the relations for the stresses in the assembly. This means that the CTE of the solder material does not affect the thermally induced stresses in the assembly, as long as the thickness and/or the modulus of the adhesive are small compared to that of the adherents.

However, the modulus and the melting temperature of the adhesive layer plays an important part in the magnitude and distribution of the stresses. Lower the modulus of the solder, lower will be the amount of stresses transmitted to the attached components. Also, lower melting temperature solders decrease the stresses in the assembly by lowering the temperature differential between reflow and room temperature. However, low melting temperature solders are at high homologous temperatures (T/T_{melting} in the absolute scale) during the range of operating temperatures of an electronic package, leading to inelastic strain accumulation in the solder material. This accumulation of inelastic strain in the material could lead to fatigue failure of the material during operation.

Eutectic lead tin solder melts at 183°C, and therefore, is at about 65% ($0.65T_M$) of its melting temperature in the absolute scale, at room temperature. In general, creep becomes significant in materials at homologous temperatures above $0.5T_M$. Therefore, inelastic strain gets accumulated in the eutectic lead-tin solder after reflow and during subsequent thermal cycles in operation.

In addition to these primary failure mechanisms, manufacturing processes induce numerous defects in a package, which typically becomes the preferred site for failure initiation. For example, sawing a die from a wafer introduces numerous micro-cracks at the edges of the die, which can propagate due to the stresses induced in the die during operation.

4.2.2 Temperature Cycles in Operation

A microprocessor package is subjected to numerous heating and cooling cycles in operation. When the device is powered up, its temperature rises, and when it is shut down, its temperature drops. The magnitude of the maximum temperature on the die surface depends on the thermal solution employed, and is usually between 80 to 125°C. In addition to these power on and power off cycles (maxi-cycles), the microprocessor is cycled between different intermediate temperature values depending upon processor usage (mini-cycles) in any application program. The Institute for Interconnecting and Packaging Electronic Circuits [2] lists the typical worst case usage conditions for personal computers and consumer electronics as given below. This table is intended only as a guideline, and individual companies use different field use conditions based on their research.

Table 4-14. Worst Case Use Environment

Category	Worst case use environment					
	T _{min} °C	T _{max} °C	ΔT °C	Dwell (hrs)	Cycle/yr	Approx. Years in Service
Consumer	0	+60	35	12	365	1-3
Computers	+15	+60	20	2	1460	5

To investigate the reliability of a microprocessor package during the intended life of the package, they are subjected to temperature and power cycling tests.

4.2.3 Delamination of bi-material interfaces

As mentioned previously, an electronic package consists of many multi-material interfaces. Mechanical bonding is the primary bonding mechanism at many of these interfaces. Delamination can occur at these interfaces during temperature excursions in manufacture or operation. The primary cause of delamination of interfaces are manufacturing defects compounded by the shear stresses acting at these interfaces due to a CTE mismatch. One of the common interface seen in a package is an organic material (like an epoxy or an encapsulant) bonded to a metallic or a ceramic surface. There are a number of publications in literature that describe mechanisms associated with delamination of an interface from the elements in the package. The key events or process steps leading up to delamination can be incorporated into a reasonably coherent picture on the basis of information presented in these references.

4.2.4 Shock and vibratory loads

The increasing speed requirements of modern day microprocessor packages has resulted in packaging memory components along with the CPU, leading to larger sizes of packages. Cantilevered and lightly restrained structures are regions of concern in shock and vibratory loading environments. The dynamic response of a package can introduce high frequency cyclic stresses in some components of the package leading to the possibility of high cycle fatigue. As an example, consider the stresses that occur when a computer is subjected to vibrations. Repeated flexure of a structure within the package will put the copper lines and solder joints through a fully traversed stress cycle. If the package has a resonant frequency at 10 Hz and an expected service life of 4000 hrs, the circuit lines and solder bumps would have to survive a minimum of 100 million cycles of stress reversals.

The ability of a package to survive these stress-inducing environments is governed by the properties of the materials used in its construction, as well as by its design.

4.2.5 Typical Analysis Methodologies

Finite element analysis along with suitable experiments, is the most common technique used to determine the behavior and the reliability of a package to various stress inducing environments. Due to the complex structure of packages, geometric and analysis simplifications are often utilized in these analyses. To ensure that all relevant interactions are accounted for, and the model accurately captures the behavior of the real structure, model validation experiments are carried out. The experimental results are used to calibrate the model to ensure the validity of the model predictions.

In recent years, extremely sensitive, full-field optical interference techniques have been extensively used to calibrate and compare numerical predictions to actual behavior. Some of the commonly employed "opto-mechanical tools" that produce high-resolution, full-field contour maps of thermo-mechanical deformation within an electronic package are Moiré Interferometry, Infrared (IR) Fizeau Interferometry and Shadow Moiré [3-5]. While Moire interferometry measures the in-plane deformation, Fizeau interferometry and Shadow moire are used to map the out of plane deformation (warpage) of packages. In addition to model validation, these tools by itself can be used to study the effect of design changes on the behavior of the package quickly.

4.2.5.1 Numerical analysis and model validation examples

Figure 4-10 shows a finite element model and the out of plane displacement of a C4 die bonded to a substrate after assembly. Since there is a CTE mismatch between the silicon, substrate, and the die attach materials, the assembly warps after cool-down from the reflow temperature. For the size of the assembly modeled, the out of plane displacement on the surface of the die is predicted to be 39.45 microns. Figure 4-11 shows the Fizeau measurement of the die warpage after manufacture. The fringe sensitivity of this measurement is 2.65 um/fringe, which gives the total warpage (measured from center to corner) on the die surface to be 39.4 microns. Note that there is a good correlation between the numerical prediction and the experimental measurement, thereby, validating the general behavior of the finite element model.

Figure 4-10. Finite element model and out of plane displacement of a die C4 attached to a substrate

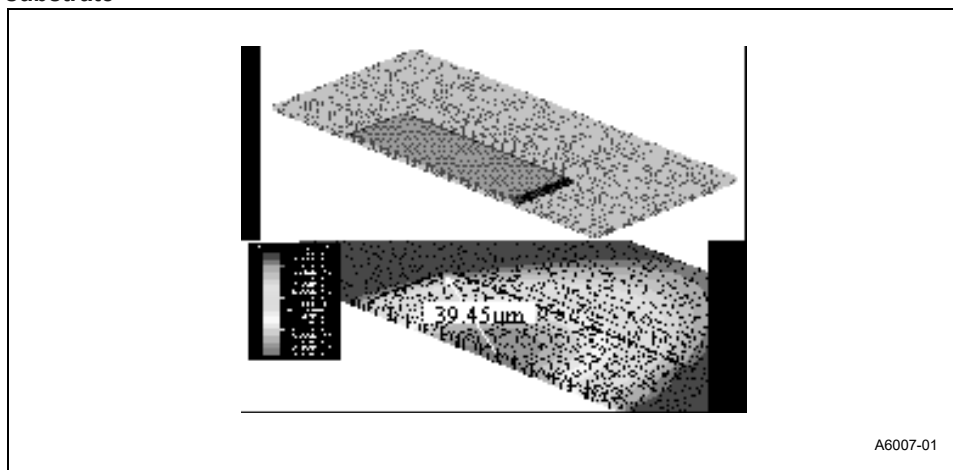
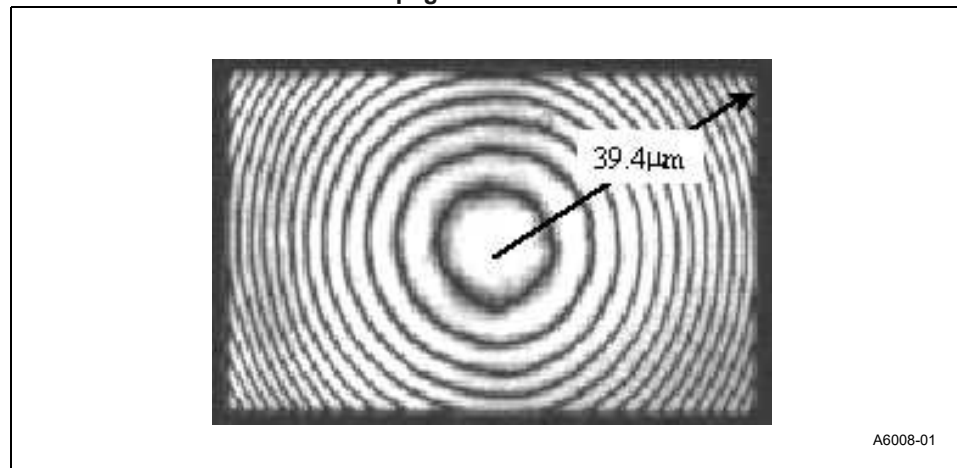


Figure 4-11. Fizeau measurement of die warpage

However, before this model can be used for stress predictions in microscopic regions of the package, this model has to be further validated. Figure 4-12 and Figure 4-13 compare the inplane displacements in the fillet region of the underfill. The fringe constant for the fringe patterns shown in these figures is 0.417 mm/fringe. For comparison purposes, an image analysis software has been used to depict the displacements in a selected region of the fillet as a displacement contour pattern having the same scale as the numerical contour pattern. Note that the results match well. This validated model is now used for stress and life predictions. Typically, the properties of materials used in these packages are not well characterized. Therefore, a number of iterations of model calibration using the experimental results are required before the model can be used for stress predictions.

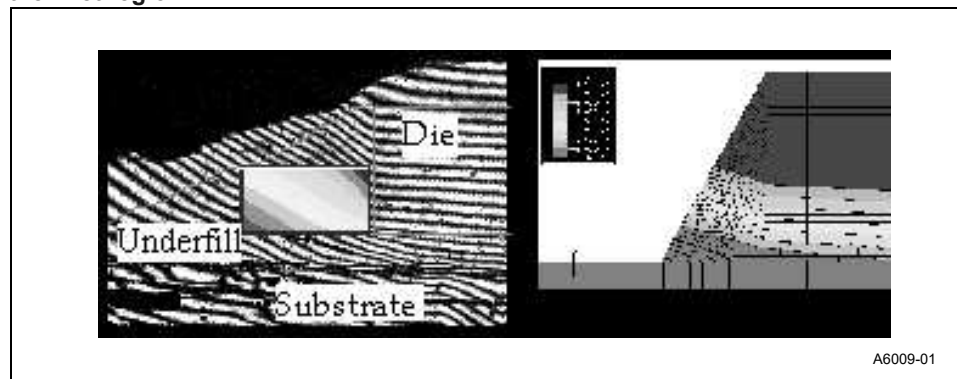
Figure 4-12. Comparison of model prediction and moire results of horizontal displacement in the fillet region

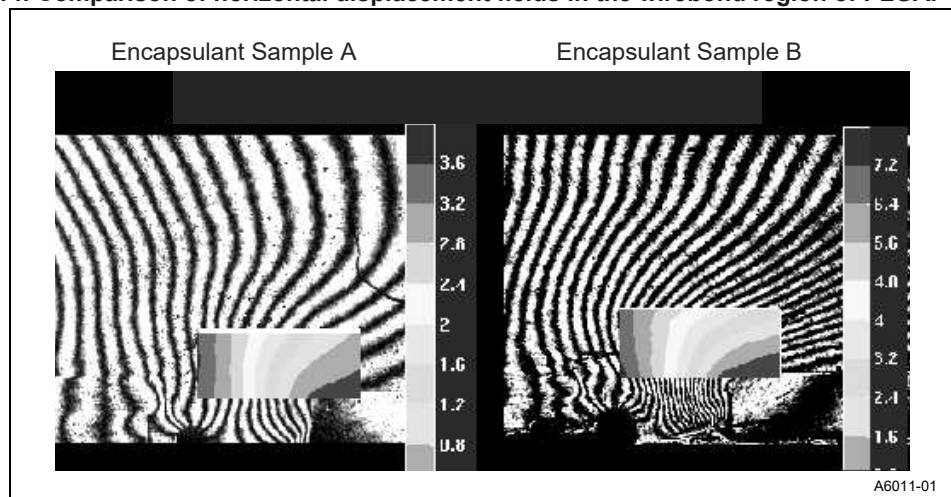
Figure 4-13. Comparison of model prediction and moire results of verticle displacement in the fillet region



Besides its use as model validation tools, these interferometric techniques are also used to compare materials and design options, due to its relatively short time-to-data. Two epoxy samples proposed to be used as the encapsulant material in PLGA (Plastic Land Grid Array) packages were compared using Moiré interferometry. In PLGA packages, the silicon die is covered with the encapsulated. This epoxy not only covers the active surface of the silicon, but also the wire-to-pad interconnects. Therefore, these two epoxy samples were compared from a wire bond reliability perspective.

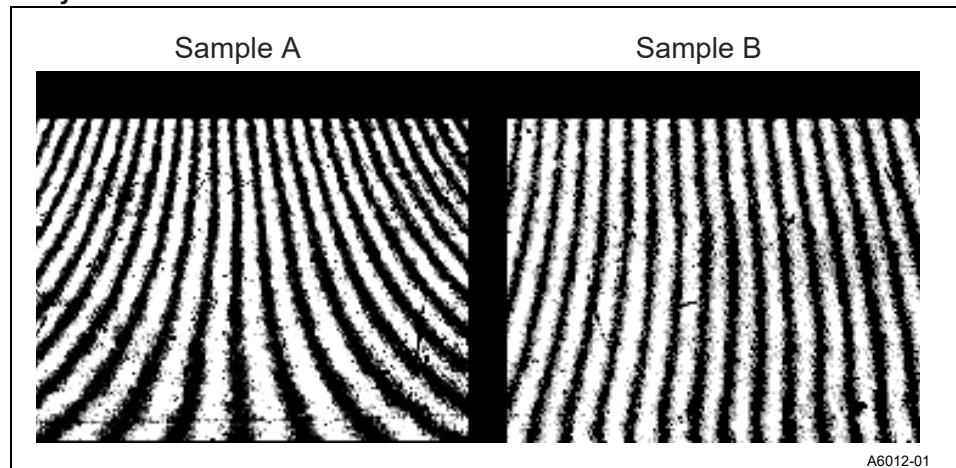
Figure 4-14 compares the Moiré U-field displacement patterns (horizontal fields) of the wire heel region (at the wire to die interface) using the two different encapsulant materials. Fringe gradients in any direction would indicate relative motion between the encapsulant and the die in that direction, increasing the likelihood of failure during temperature excursions. V-field images (vertical field) revealed almost no fringe gradients in the wire heel region indicating negligible relative motion between the die and the encapsulant in that direction.

Figure 4-14. Comparison of horizontal displacement fields in the wirebond region of PLGA.



Note the higher density of fringes in the right image

Figure 4-15. Comparison of free expansions of the two encapsulant materials used in the study



However as shown in Figure 4-14, the horizontal displacement of the the encapsulant in wire heel area of the sample using encapsulant B is twice that in the case of the package using sample A. This difference in behavior between encapsulant A and B was confounding since both encapsulants had nearly identical bulk CTE's in the horizontal direction. The encapsulant material in the heel area of both packages were seperated and moire performed. Figure 4-15 shows the horizontal displacement fields obtained from both encapsulant materials. Figure 4-15 indicates that encapsulant B has a much larger CTE at the interface that encapsulant A. This was later determined to be due to a lower filler content at the interface.

4.2.6 Surface Mounted Lead Packages

4.2.6.1 Bond Stresses

In addition to the mechanical and metallurgical stresses developed during the wire-bonding process, encapsulation and environmental stresses subsequent to bonding can contribute to degradation of the interconnection. Reliable first and second bonds can be ensured by bonding within the process windows for force, power, time, and temperature. Excursions beyond these windows are minimized through regular process monitors such as bond pulls. Both pull strength and failure mechanism criteria must meet specifications. In particular, no cratering failures are acceptable even if pull strength criteria are met, since craters indicate excessive force during bonding which could lead to reliability problems in the field.

During encapsulation, wire sweep may occur if wire lengths are too great or if drag during molding flow is excessive. Current mold gate designs provide low drag flow patterns, and X-ray monitors are used to confirm process stability. Wire diameter and length design rules are strictly enforced to ensure that there is adequate mechanical stability of the bond arch to resist drag forces. Development of new package designs includes analysis and experiment to ensure that wire sweep is minimized.

In plastic packages, delamination at the interface between molding compound and silicon or lead frame can cause high stresses at the first or second bond location, because the differential thermal expansions must be accommodated across the bond itself. The delamination generally results from temperature cycling of packages with trapped moisture. To suppress the adverse effects of delamination, selection of materials with enhanced interfacial adhesion and the design of lead

frames that feature additional mold compound locking characteristics have proven to be effective. Finite element models are used to guide and optimize designs. For packages that are particularly moisture-sensitive, shipment of prebaked product in sealed moisture-proof bags with desiccant ensures that delamination is minimized and operation of the assembled part will be reliable.

4.2.6.2 Compliant Leads and Solder Joint Fatigue

With the advent of surface mounted packages, solder joint integrity became an issue of considerable concern. It was found that solder joints on leadless ceramic packages measuring more than 0.5 inch on a side could survive only a few hundred temperature cycles (Condition B, -55°C to $+125^{\circ}\text{C}$) when the packages were surface mounted to FR-4-type circuit boards. The addition of compliant leads to these packages has extended the life considerably and is now used in the design of all new surface mounted packages.

As a means of experimentally evaluating the in situ stiffnesses of leads on packages surface-mounted to boards, the straddle board method has proven to be a very useful tool. As shown in Figure 4-16 and Figure 4-17, the straddle board consists of a slotted, double-sided epoxy-glass FR-4 board that is patterned for corner leads. All other package leads are removed.

Figure 4-16. Lead Stiffness Straddle Board

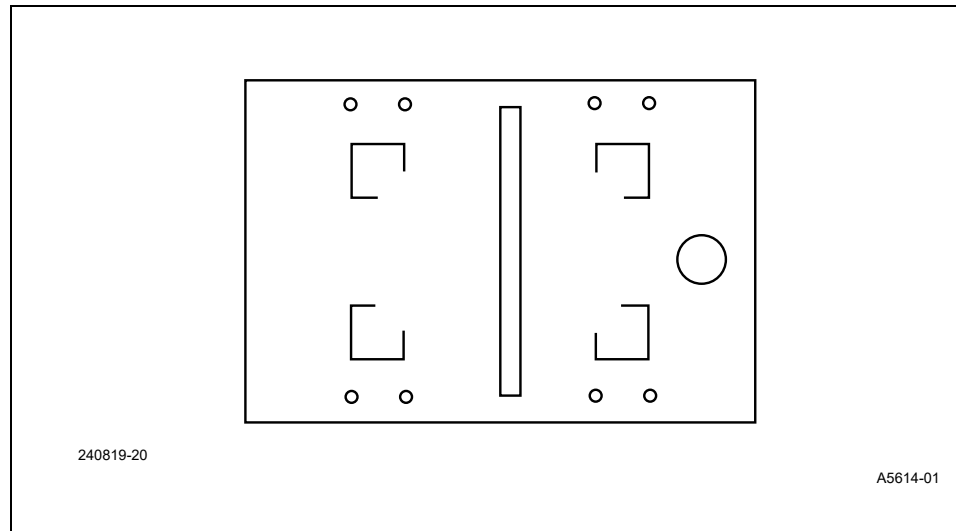
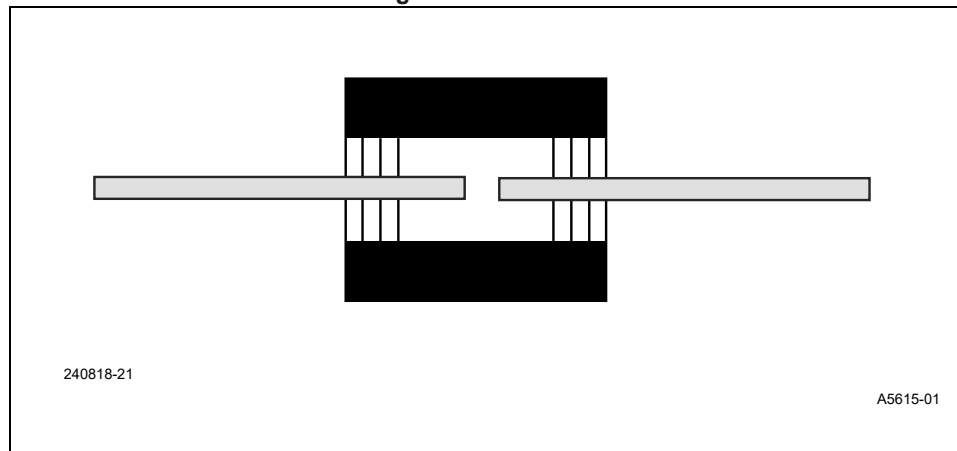


Figure 4-17. Straddle Board with Two Packages in Place

Units are mounted on both sides of the board using production-level processes and specifications for each package. The board is mounted vertically in a tensile test set-up such as a materials test system (MTS), and the narrow sides of the slot are cut, separating the two ends of the package. The MTS is fitted with a 200 lb. load cell and a 6 inch displacement actuator. This allows the straddle board to be tested with a 0.020 inch displacement, 0.010 inch in the tensile cycle and 0.010 inch in the compressive cycle. These values were chosen to span the lead displacement experienced during temperature excursions from -65°C to $+150^{\circ}\text{C}$ (MIL-STD-883C T/C [C]).

A total cycle time of five seconds was used with a maximum load range of 0.8-8 lbs., depending on the package type and lead count. As Figure 4-18 shows, leads are loaded in both lateral and transverse directions (i.e. in the plane and normal to the plane of the lead bend). Twenty-five samples per lead count per direction were evaluated. Once the board was mounted, three full cycles were run, and the force versus deflection curve was recorded. The linear portions of the loading and unloading curves were used to determine the lead stiffness. A typical hysteresis curve is shown in Figure 4-19.

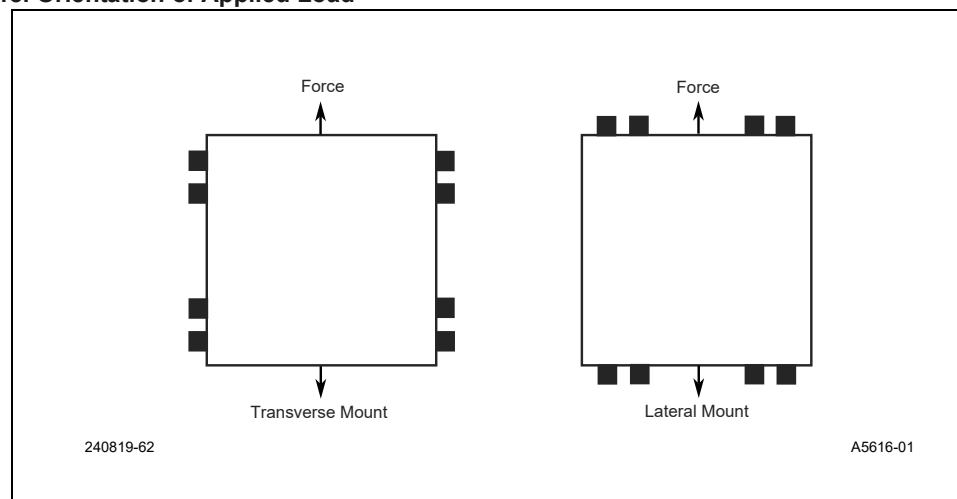
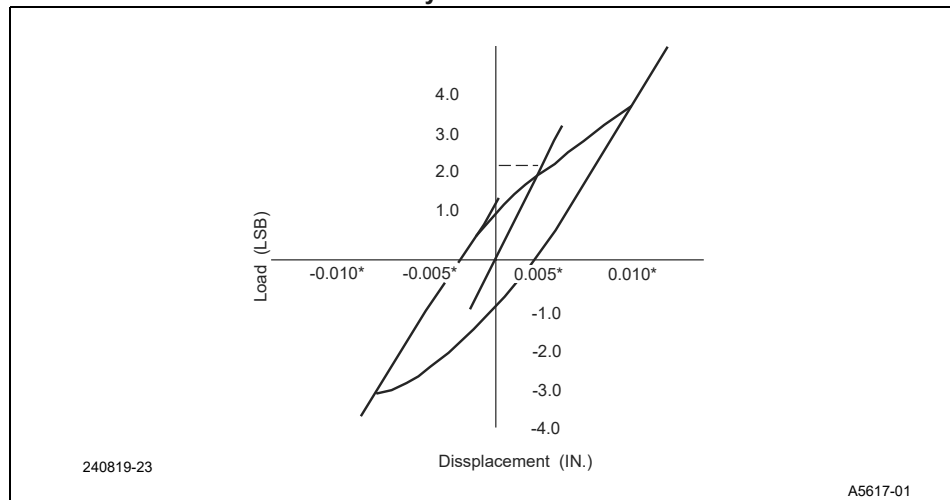
Figure 4-18. Orientation of Applied Load

Figure 4-19. Lead Stiffness Determined from Hysterisis



Designing leads with adequate compliance is now recognized as an important element of overall product design, and mechanical modeling has proven to be a useful design tool. Lateral and transverse lead stiffnesses were calculated for PLCC, and PQFP packages using the ANSYS 3-D elastic beam element option. The calculated stiffness for each type of package was matched to the value obtained from the straddle board measurements by locating the point on the lead where agreement was reached. In all cases, the point lay within the solder joint, in agreement with physical expectations.

Of particular interest were the boundary conditions imposed by the solder joint on the foot of the lead. In the lateral direction, the solder volume is adequate for the joint to provide built-in support to the lead foot (zero rotation). However, in the transverse direction for the PLCC and cerquad packages, the J-bend lead stiffnesses are large enough to produce inelastic deformations in the solder joint. As a result, the joint acts like a pinned support (free rotation). In all cases, the PQFP gull-wing leads are sufficiently compliant for the solder joint to act as a built-in support. This result suggests that reducing lead stiffness will significantly reduce solder joint stresses and associated creep and fatigue. Experimental data recently reported in supports this hypothesis.

Because of the contribution of lead stiffness to the level of stress in the solder joint when there is thermal mismatch between package and board, a comprehensive list of in situ lead stiffness values is provided in Figure 4-21. All surface mounted packages currently used for Intel products (TSOP, PLCC, PQFP and CQFP) are listed in Table 4-15. For these packages both translational and rotational stiffness components are given. The translational stiffness is defined as the force in pounds created by a displacement in inches applied at the solder joint in the direction of interest, the remaining force and rotation components being zero. These stiffness components are important when the thermal mismatch creates differential displacements which must be accommodated along the leads. The rotational stiffness is defined as the moment in inch-pounds created by a rotation in radians applied at the solder joint about the axis of interest, all other moments and displacement components being zero. These stiffness components are important when thermally induced differential rotations are imposed at the ends of the leads.

The magnitude of the stiffness components are useful in making comparisons of the level of stress or strain induced in the solder joint by various package types; high lead stiffness will generate high solder stresses, etc. Experience to date indicates that in situ translational lead stiffnesses on the order of 100 lb./in. or less produce excellent joint reliability. Even lead stiffnesses above this level are acceptable although they have less margin than the more compliant leads. With reference to

Figure 4-21, the x- and y-components of the gull-wing leads on 0.025 in. centers (PQFP and CQFP) fall into this category. The z-components are always large and demonstrate the importance of minimizing board flexing, which generates these z-components.

To assist in visualizing the stiffness and stress entries in Table 4-15, Figure 4-21 has been prepared. The gull-wing lead of the PQFP has been used for reference. In all entries, the center line represents the lead profile in the plane of interest. The heavy line represents the displacement profile associated with the displacement or rotation component indicated at the point on the lead connected to the solder. The line connected by shading to the undeflected profile shows the distribution of the bending stress along the lead. In general, the maximum value is at or near the solder connection point; however, for displacements along (or rotations about) the z-axis, the bending stress maximizes at the package body. As mentioned previously, z-component displacements may generate high lead stresses. Figure 4-21 suggests that the package body is the site of maximum stress and damage in the lead.

Table 4-15. Surface Mount Package Lead Stiffness

Package	Lead Stiffness Components						Maximum Lead Stresses					
	Trans. Stiffness (lb/in.)			Rotation Stiffness (in.-lb/rad.)			Trans. Stresses (Ksi/m in.)			Rot. Stresses (Ksi/m rad.)		
Type	K _x	K _y	K _z	K _{θx}	K _{θy}	K _{θz}	σ _x	σ _y	σ _z	σ _{θx}	σ _{θy}	σ _{θz}
TSOP(I)	1900	2560	9730	0.579	0.435	0.115	514	521	1660*	7.89	9.55	1.78*
TSOP(II)	3820	18800	19500	4.42	0.869	0.704	514	990	1660*	15.1	9.55	2.86*
PLCC 44L	323	1250	7750	1.82	0.379	1.03	43.3	59.1	335	1.81+	6.65	1.56+
PLCC 68L	187	1190	8813	1.03	0.166	0.641	43.7	89.1	474	3.08+	6.99	2.60+
PQFP	39.8	85.9	955	0.245	0.133	0.0468	30.4	35.9	281*	1.98	2.05	0.438*
CQFP	9.05	23.0	250	0.361	0.0132	0.0232	16.6	24.8	173*	2.39	1.62	0.342*

DEFINITIONS:

K_α = Force in lbs. needed to produce a displacement in inches in the α direction at the solder joint, all other forces and rotations = 0.

K_{θα} = Moment in in.-lbs. needed to produce a rotation in rad. about the α axis at the solder joint, all other moments and displacements = 0.

σ_α = Maximum lead stress in Ksi due to a 0.001 in. displacement in the α direction at the solder joint, all other forces and rotations = 0. Unless otherwise noted, maximum stress occurs at the solder joint.

σ_{θα} = Maximum lead stress in Ksi due to a 0.001 rad. rotation about the α axis at the solder joint, all other forces and rotations = 0. Unless otherwise noted, maximum stress occurs at the solder joint.

x = Outward normal to the edge of the package in the plane of the unformed leadframe.

y = Tangent to the edge of the package in the plane of the unformed leadframe.

z = Perpendicular to the plane of the unformed leadframe.

NOTES:

1. * Maximum at the package body.

2. + Maximum at the site of lead width reduction.

Under certain conditions, stresses in the lead may be large enough to cause reliability problems in the lead as well as in the solder joint. The figures of merit presented in Table 4-16 extracted from Table 4-15, provides indicators of lead compliance and lead stress levels for current Intel package types. All the lead compliance and stress of various packages and lead designs are normalized upon the lead configuration of a 68L PLCC package. The first two columns give the level of lead compliance along the lateral and transverse directions as compared to that of a 68L PLCC package. The lead stress is estimated by applying a unit displacement (1 mil) along the lateral or the transverse direction, the third and fourth columns provide the level of lead stress produced by the proposed lead displacement. A correlation between the lead stiffness and the lead stress is observed; the greater the lead stiffness, the higher the lead stress. A plot of log [lead stress] verses log [lead stiffness] is shown in Figure 4-20. The trend of the lead stress dependence on lead stiffness is linear on a log-log plot for most of the Intel packages except the TSOP I and TSOP II packages which show much stiffer lead response because of their low profile and short lead design. In general, a stiffer lead will introduce higher stress at the solder joint during temperature cycle (T/

C) stressing and subsequently degrades the solder joint fatigue performance. To assess solder joint reliability, a methodology is described in the following paragraphs to investigate the solder joint fatigue performance at various lead displacement amplitudes and frequencies.

Table 4-16. Figures of Merit for Lead Compliance and Lead Stress Package

Package	Compliance FOM ¹		Stress FOM ²	
	Lateral	Transverse	Lateral	Transverse
TSOP I	0.098	0.46	0.085	0.17
TSOP II	0.049	0.06	0.085	0.09
44L PLCC	0.58	0.95	1.01	1.51
68L PLCC ³	1.00	1.00	1.00	1.00
100L PQFP	4.70	13.85	1.44	2.48
CQFP	20.66	51.74	2.73	3.59

NOTES:

1. Compliance FOM = (Package Compliance) / (68L PLCC Compliance).
2. Stress FOM = (68L PLCC Lead Stress) / (Package Lead Stress).
3. 68L PLCC: Lateral Lead Stiffness = 187 lbf/in, Transverse Lead Stiffness = 1190 lbf/in.
4. Lateral Lead Stress = 43.7 Kpsi/mil, Transverse Lead Stress = 89.1 Kpsi/mil.

Figure 4-20. Lead Stress Dependence on Lead Stiffness for Various Lead Designs

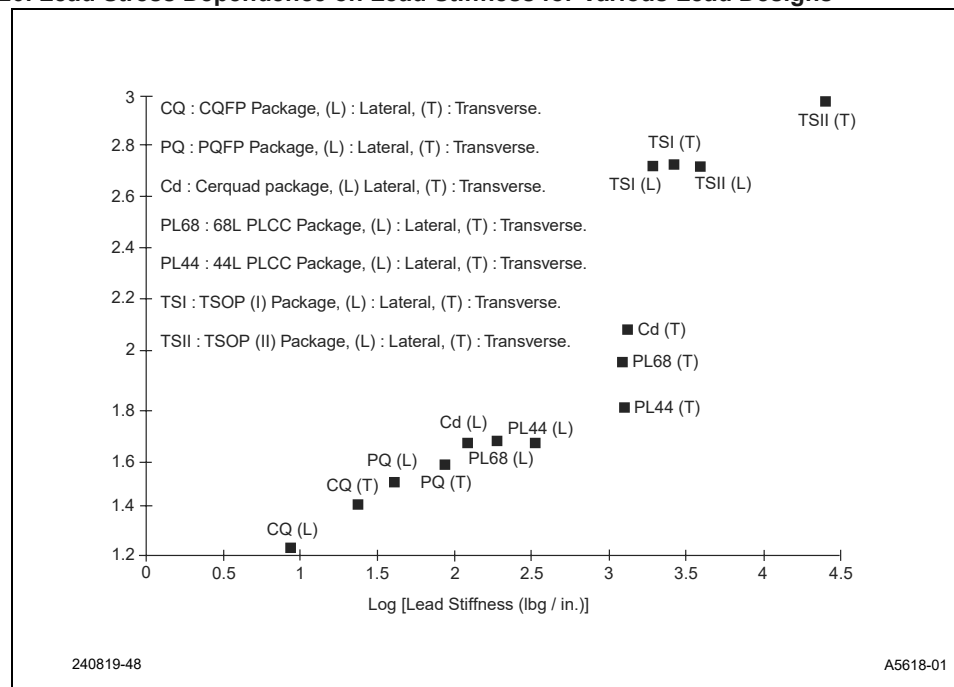


Figure 4-21. Stress Distribution along a PQFP Lead

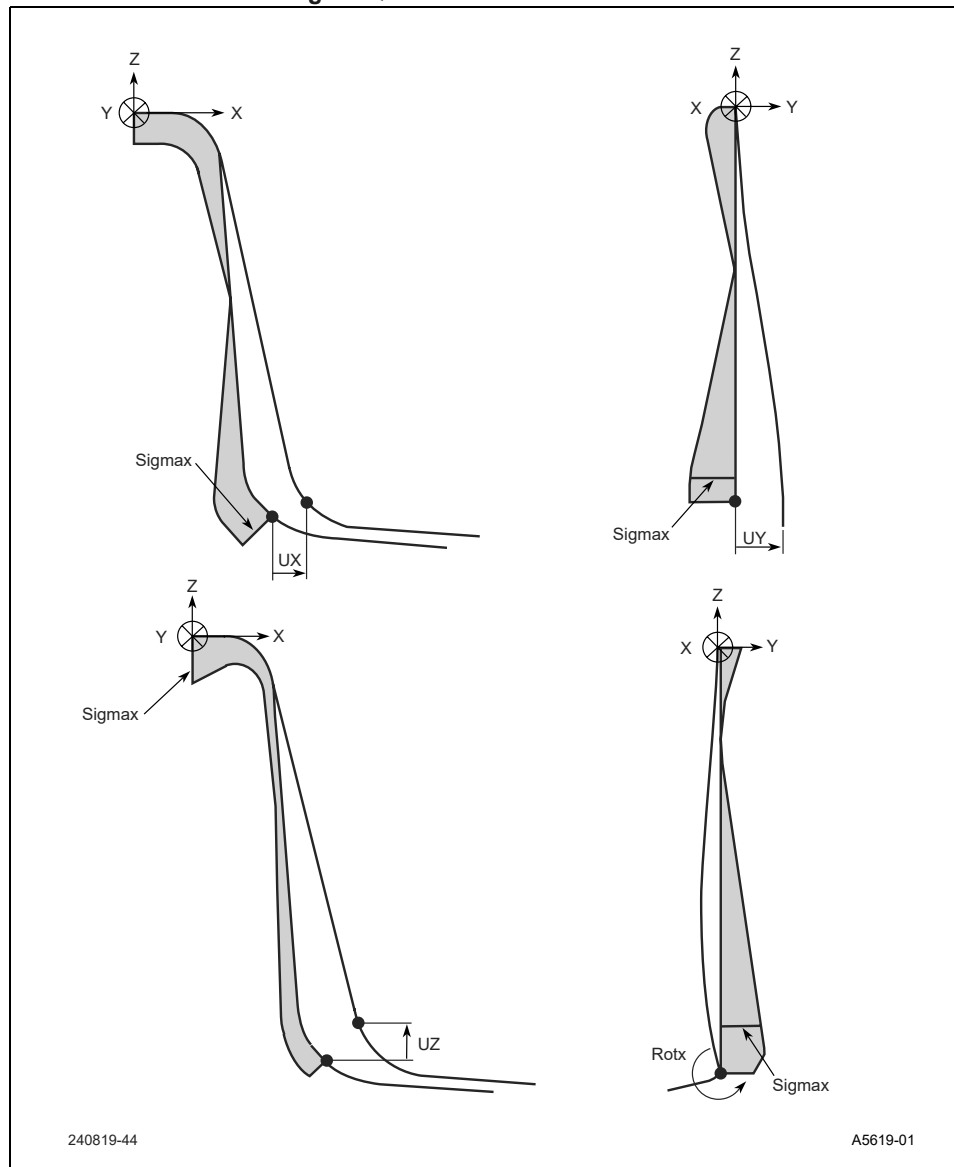
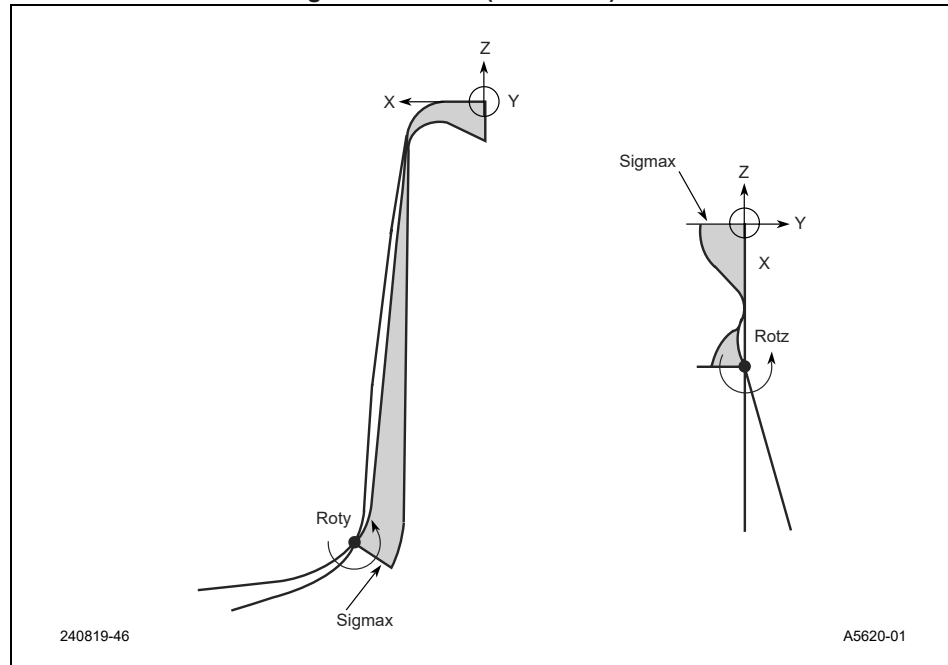


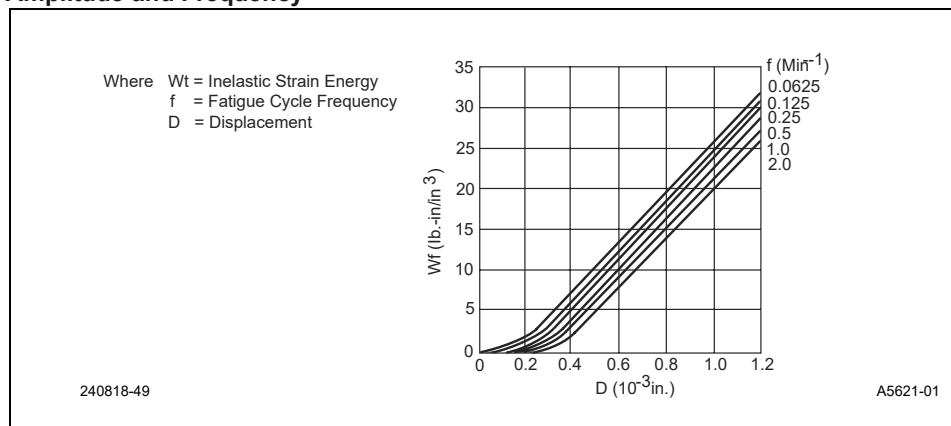
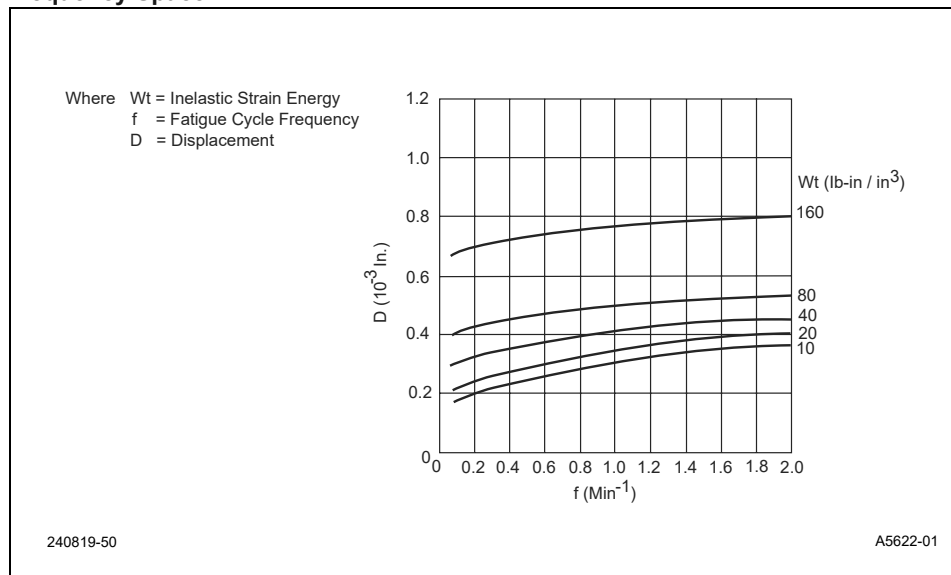
Figure 4-22. Stress Distribution Along a PQFP Lead (continued)



4.2.6.3 Effects of Loading Frequency and Amplitude on Solder Joint Damage

Cyclic strain energy dissipation, W , was analyzed for a simple two segment structure consisting of solder exhibiting elastic, plastic and creep behavior connected in series with copper exhibiting elastic behavior only. The structure is fixed at one end and subjected to a 'square wave' displacement at the other. The total strain energy consists of plastic and creep components, the magnitudes of which depend on the amplitude and frequency of the square wave. The plastic components arise during the instantaneous changes in displacement while the creep components occur during the dwell periods. At very low frequencies (long dwell times), the creep component provides maximum contribution to the total, in the range of 15-50% for the examples considered. At very high frequencies (very short dwell times), only the plastic component contributes and is smaller than its low-frequency counterpart. This is because the creep relaxation during the long dwell period at the low frequency end enables a large value of plastic strain to be generated during the instantaneous change in displacement following the dwell.

A quantitative picture of the dependence of the total strain energy dissipation, W , per cycle on displacement amplitude and frequency is shown in Figure 4-23 and re-mapped to Figure 4-24. These iso-strain energy dissipation contours per cycle show strong dependence on the displacement amplitude and weaker dependence on the cyclic frequency. The use of the cumulated total energy could provide reasonably good prediction on the solder joint fatigue life. The use of this methodology to predict a 68 L PLCC solder joint reliability is described in the next section.

Figure 4-23. Dependence of Total Strain Energy Dissipation per Cycle on Displacement Amplitude and Frequency**Figure 4-24. Isocontours of Strain Energy Dissipation in Displacement Amplitude and Frequency Space**

4.2.6.4 Dependence of J-Lead Solder Joint Reliability on Lead Displacement Amplitude and Frequency

A 68L PLCC configuration was selected to study the J-lead solder joint reliability as a function of lead displacement amplitude (d) and frequency (t) (period of fatigue cycle). The general form of the constitutive relations for the solder and the lead is given elsewhere. A “square wave” displacement amplitude of 1.25-5 mils and periods of 0-30 minutes were applied to the end of the lead, the total inelastic energy dissipation (plastic and creep) in the solder joint was analyzed and displayed in Figure 4-25. The total energy, W , exhibits a monotonically increasing dependence on the lead displacement (d) and frequency (t) (period of fatigue cycle). In addition, it appears that for a given displacement, the total energy, W , asymptotically approaches a maximum value which is reasonably well approximated by W at $t = 30$ minutes.

Considering the solder joint fatigue life is governed by the total inelastic energy dissipation during fatigue stressing, estimations of its life expectancy may be conservative. Even though solder fatigue life predictions based on inelastic strain energy density buildup to a critical level alone might be conservative, it is still useful to examine the consequences of postulating a critical strain energy density buildup level and examining its impact on the life prediction. For example, if 100 cycles count is the cycle count for a critical strain energy density buildup for the displacement of 5 mils and a period of 30 minutes, then based on the data in Figure 4-25, the corresponding cycle count for various amplitude and period combinations to reach the same level of energy dissipation (damage) could be calculated (in a case of fatigue displacement of 5 mils and period of 30 minutes, if 100 cycles is the critical count to fracture, then, with data given in Figure 4-25, the corresponding critical cycle counts for various fatigue conditions to fail could be estimated). The plot of various cycle count in the form of $\log(d)$ versus $\log(N/100)$, where N is the total cycle counts for solder joint fatigue failures, is given in Figure 4-26. Common practice when displaying fatigue curves whose appearance is similar to Figure 4-26 is to obtain the slope for a fit to the Coffin-Manson relation. In this case, the exponent varies from -0.667 for $t = 0$ minutes to -0.786 for $t = 30$ minutes. Hence, although each curve appears linear, the slopes show a dependence on the period (inverse frequency) of the cycle. For the displacement amplitude ranges investigated, these values are close to those reported from experimental investigations. The consistency between the model and the experiments suggest that the critical strain energy density buildup criterion may be a useful approach for the development of a comprehensive failure prediction methodology for solder. However, it should be pointed out that for displacement amplitude larger than those shown in Figure 4-26, it is likely that the curves merge. Moreover, at very low displacement amplitude, the curves should become horizontal (asymptotically approach the cycle to failure axis) since negligible strain energy density buildup is possible and the solder should survive almost unlimited cycling.

Figure 4-25. Cyclic Strain Energy Dependence on Displacement Period

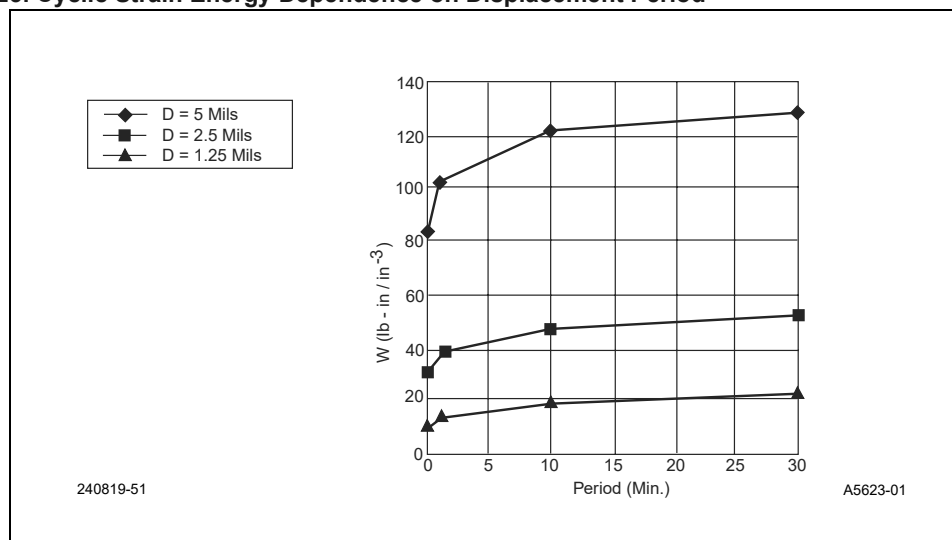
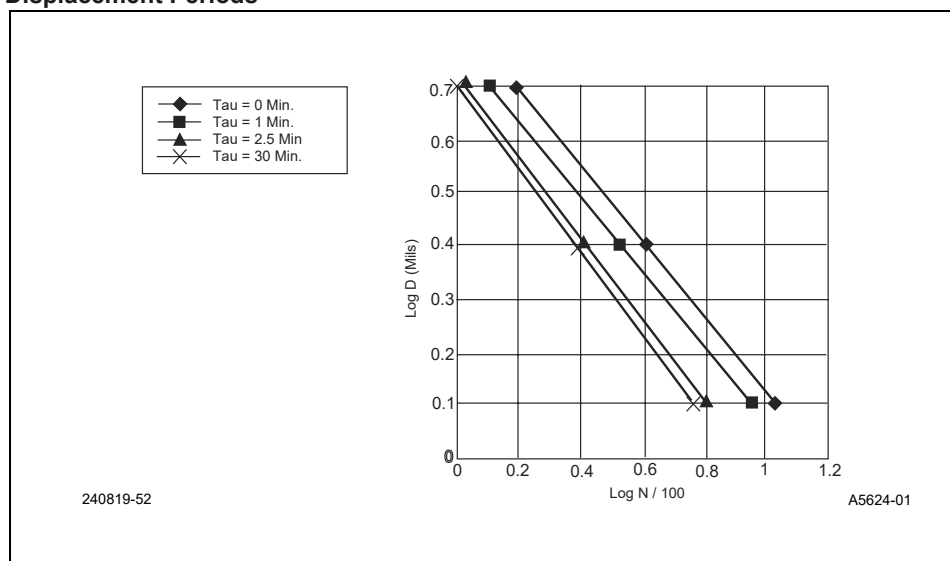


Figure 4-26. Dependence of Log of Displacement Amplitude on Log of (N/100) for Different Displacement Periods

4.3 IC Package Thermal Characteristics

4.3.1 Importance of Thermal Management

Thermal management of an electronic system encompasses all the thermal processes and technologies that must be utilized to move and transport heat from individual components to the system thermal sink in a controlled manner.

Thermal management has two primary objectives. The first is to ensure that the temperature of each component is maintained within both its functional and maximum allowable limit. The functional temperature limit defines the maximum temperature up to which the electrical circuits may be expected to meet their specified performance targets. Operation of the circuits at temperatures higher than the functional limit may result in performance degradation or logic errors. The maximum allowable temperature limit is the highest temperature to which a component or part thereof may be safely exposed. Operation of the component at temperatures higher than the maximum allowable temperature limit may cause irreversible changes in its operating characteristics or may even cause physical destruction of the component.

The second objective of thermal management is to ensure that the temperature distribution in each component satisfies reliability objectives. Failure mechanisms encountered in electronic components are kinetic in nature and depend exponentially on the device operating temperature. The exact relationship between the failure rate and temperature depends upon the thermophysical properties of the packaging materials and the failure mechanism in operation. The relationship between the normalized failure rate and temperature, for changes in the device operating characteristics resulting from chemical or diffusive processes, can be defined by an Arrhenius equation as follows:

Equation 4-11.

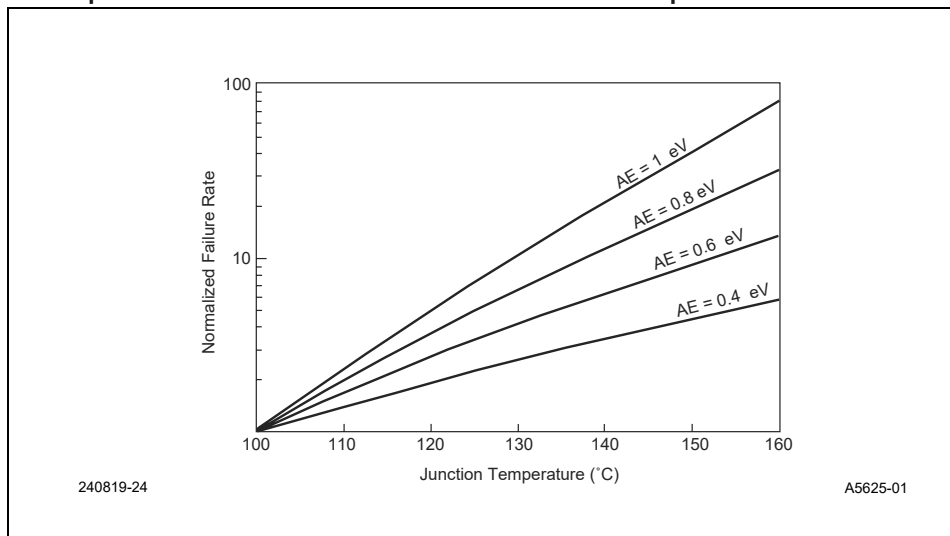
$$\theta_n = \frac{\theta_T}{\theta_{Tr}} = \text{Exp} \left[\left(\frac{E_A}{k} \right) \left(\frac{1}{Tr} - \frac{1}{T} \right) \right]$$

Where:

- θ = Failure rate
- θ_n = Normalized failure rate
- T = Absolute junction temperature (K)
- Tr = Reference temperature (K)
- E_A = Activation energy (eV)
- k = Boltzmann's constant: 8.616×10^{-5} (eV/K)

Figure 4-27 shows a plot of Equation 4-11 for a reference temperature of 100 °C and activation energies of 0.4 eV to 1.0 eV. The figure shows that for activation energies between 0.6 eV to 0.8 eV, a 25 °C increase in the operating temperature, above the reference temperature, results in an approximately five to six fold increase in the failure rate. Thus, precise control of component operating temperatures is absolutely essential to ensure product reliability.

Figure 4-27. Component Failure Rate as a Function of Junction Temperature



4.3.2 Heat Transfer Modes

To understand the thermal characteristics of electronic components and packages, it is necessary to briefly review the processes by which heat is transferred from one point to another. Heat transfer occurs via one or more of three modes: conduction, convection, and radiation.

4.3.2.1 Conduction

Conduction is a mode of heat transfer in which heat flows from a region of higher temperature to one of lower temperature within a medium (solid, liquid, or gaseous) or media in direct physical contact. In conductive heat flow, the energy is transmitted by direct molecular communication without appreciable displacement of the molecules.

In a one-dimensional system (see Figure 4-22), conductive heat transfer is governed by the following relation:

Equation 4-12.

$$q = -kA \frac{\Delta T}{L} = -kA \frac{T_1 - T_2}{L}$$

where:

- q = Heat flow rate (W)
- k = Material thermal conductivity (W/mC)
- A = Cross-sectional area (m²)
- Δ T = Temperature difference, T₁-T₂, between the hot and cold regions (K or °C)
- L = Linear distance between the locations of T₁-T₂ (m)

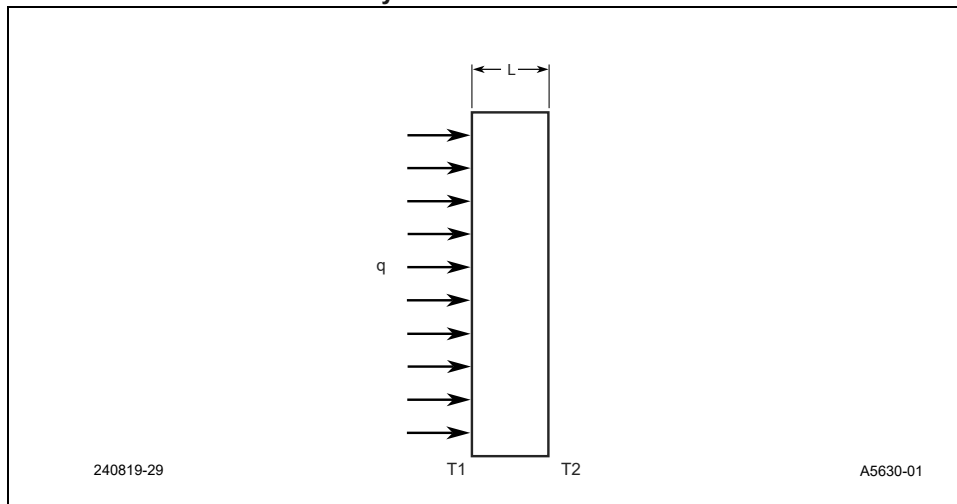
Equation 4-12 indicates that in conduction, the heat flow rate is directly proportional to material thermal conductivity, temperature gradient, and cross-sectional area. Equation 4-12 can be written as:

Equation 4-13.

$$q = \frac{\Delta T}{L/kA}$$

Using an electrical analogy, if q and Δ T are analogous to current and voltage respectively, L/kA is analogous to electrical resistance. According to Equation 4-13, thermal resistance can be expressed in terms of material thermal conductivity and geometrical parameters and is independent of the power dissipation.

Figure 4-28. One-Dimensional Heat Flow by Conduction



4.3.2.2 Convection

Convection is a mode of heat transport from a solid surface to a fluid and occurs due to the bulk motion of the fluid. The basic relation that describes heat transfer by convection from a surface presumes a linear dependence on the surface temperature rise over the ambient, and is referred to as Newton's law of cooling:

Equation 4-14.

$$q_c = h_c A (T_s - T_a)$$

where:

- q_c = Convective heat flow rate from a surface to ambient (W)
- A = Surface area (m^2)
- T_s = Surface temperature (C)
- T_a = Average convective heat transfer coefficient
- h_c = Average convective heat transfer coefficient (W/m^2C)

Equation 4-14 can also be written as:

Equation 4-15.

$$q_c = \frac{T_s - T_a}{1/h_c A}$$

Comparing Equation 4-15 to Equation 4-14, it is apparent that the convective thermal resistance can be defined as $1/h_c A$.

In forced convection, fluid flow is created by an external factor such as a fan. In free or natural convection, fluid motion is induced by density variations resulting from temperature gradients in the fluid. Under the influence of gravity or other body forces, these density differences give rise to buoyancy forces that circulate the fluid and convect heat toward or away from surfaces wetted by the fluid.

4.3.2.3 Radiation

Radiation heat transfer occurs as a result of radiant energy emitted from a body by virtue of its temperature. Radiation heat transport occurs without the aid of any intervening medium. Radiant energy is sometimes envisioned to be transported by electromagnetic waves, at other times by photons. Neither viewpoint completely describes the nature of all observed phenomena.

The amount of heat transferred by radiation, between two surfaces at temperatures T_1 and T_2 respectively, is governed by the following expression:

Equation 4-16.

$$q = \epsilon \sigma A (T_1^4 - T_2^4) F_{12}$$

where:

- q = Amount of heat transfer by radiation (W)
- ϵ = Emissivity ($0 < \epsilon < 1$)
- σ = Stefan-Boltzmann constant, 5.67×10^{-8} (W/m² K⁴)
- A = Area (m²)
- F_{12} = Shape factor between surfaces 1 and 2 (A fraction of surface 1 radiation seen by surface 2)
- T_1, T_2 = T_1, T_2 = Surface temperatures (K)

Note that the temperatures T_1 and T_2 in Equation 4-16 are absolute temperatures.

For radiation to make a rather significant contribution compared to either natural convection or forced convection mechanisms, a relatively large temperature difference must exist between T_1 and T_2 . In the case of most low-power electronic applications, these temperature differences are relatively small and, therefore, radiation effects are normally neglected. But for power application, heat transfer by radiation should be considered. To compare radiative and convective effects, a radiation heat transfer coefficient is defined as:

Equation 4-17.

$$h_r = \epsilon \sigma F_{12} (T_1^2 - T_2^2) (T_1 + T_2)$$

where h_r is a radiative heat transfer coefficient.

4.3.3 Thermal Resistance in Packaging Design

The thermal performance of IC packages is typically measured using the junction-to-ambient and junction-to-case thermal resistance values. These parameters are defined by the following relations:

Equation 4-18.

$$\theta_{jc} = \frac{T_j - T_c}{P}$$

$$\theta_{ca} = \frac{T_c - T_a}{P}$$

$$\theta_{ja} = \theta_{jc} + \theta_{ca}$$

Where:

- θ_{ja} = Junction-to-ambient thermal resistance (C/W)
- θ_{jc} = Junction-to-case thermal resistance (C/W)
- θ_{ca} = Case-to-ambient thermal resistance (C/W)
- T_j = Average die temperature (C)
- T_c = Case temperature at a predefined location (C)
- P = Device Power dissipation (W)
- T_a = Ambient temperature (C)

The junction-to-case thermal resistance, θ_{jc} , is a measure of the internal thermal resistance of the package from the silicon die to the package exterior. θ_{jc} is strongly dependent on the thermal properties (i.e. thermal conductivities) of the packaging materials and on the package geometry. The junction-to-ambient thermal resistance, θ_{ja} , includes not only the package internal thermal resistance, but also the conductive and convective thermal resistance from package exterior to the ambient. θ_{ja} values depend on material thermal conductivities, package geometry as well as ambient conditions such as coolant flow rates and the thermophysical properties of the coolant.

To guarantee component functionality and long-term reliability, the maximum device operating temperature is bounded by setting constraints on either the ambient temperature or the package exterior temperature measured at predefined locations. Ambient temperature is most often measured at an undisturbed location at a certain distance away from the package. As defined in Intel experiments, the case temperature is measured at the center of the top surface of the package. Depending on the environment (ambient and board temperatures) within the computer system, thermal enhancements such as fins or forced air cooling may be necessary to meet requirements on the package case temperature, " T_c ".

4.3.4 Factors Impacting Package Thermal Resistance

The thermal resistance of a package is not a constant. Package mounting configuration and many packaging and environmental parameters have an impact on the thermal resistance values. The following is a summary of some parameters which affect thermal resistance.

4.3.4.1 Package Size

As shown by the one-dimensional conductive and convective thermal resistance expressions (see Equation 4-14 and Equation 4-16), thermal resistance is inversely proportional to area. This means that as the package gets larger, the thermal resistance becomes smaller due to an increase in the

heat transfer area. Figure 4-29 through Figure 4-31 show typical junction-to-ambient thermal resistance values as a function of lead count for different package families. According to this figure, thermal resistance is lower for packages with higher lead counts (i.e. larger package size) within the same package family.

Figure 4-29. Effect of Package Size on Thermal Resistance of PLCC, PQFP, and PGA Packages

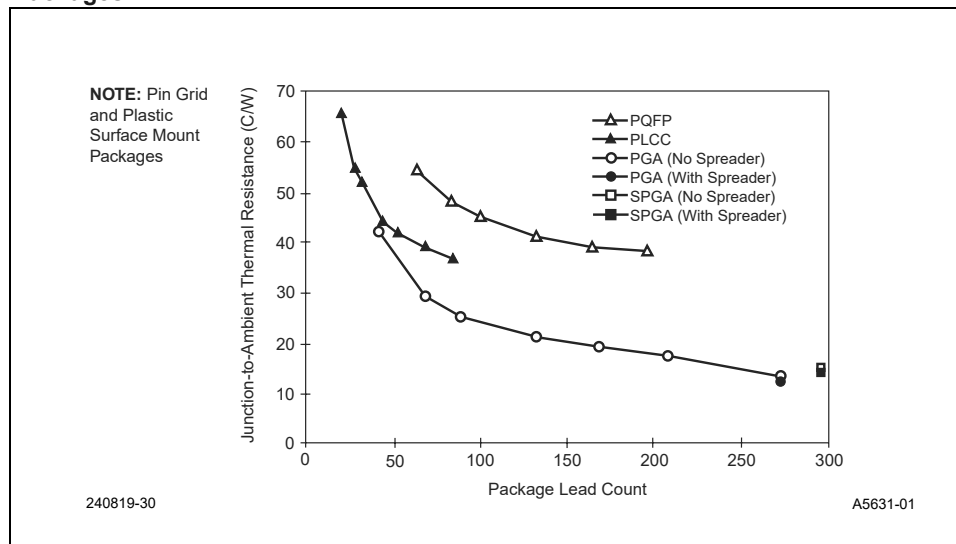


Figure 4-30. Effect of Package Size on Thermal Resistance of Plastic and Ceramic Dual-In-Line Packages

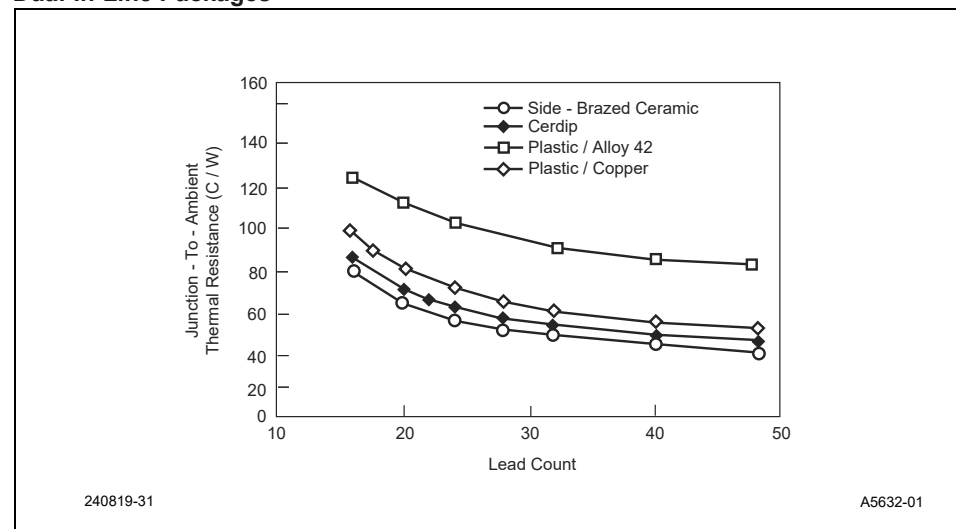
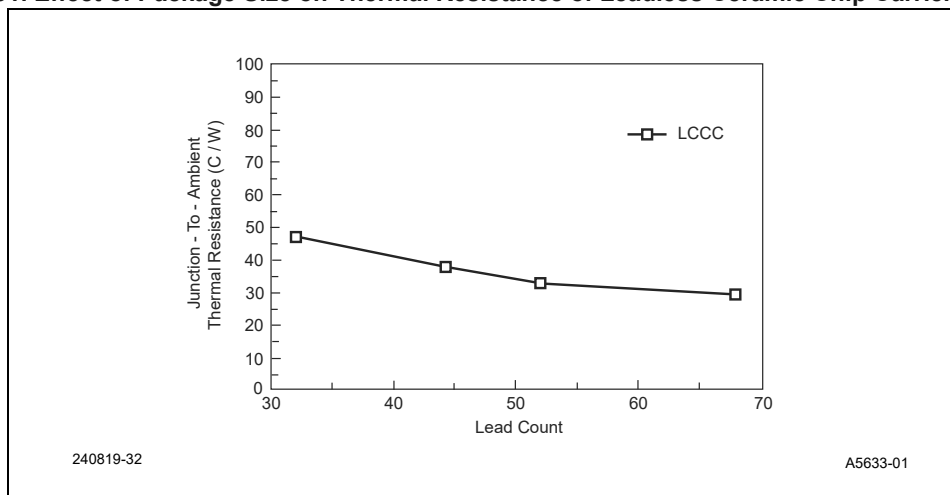


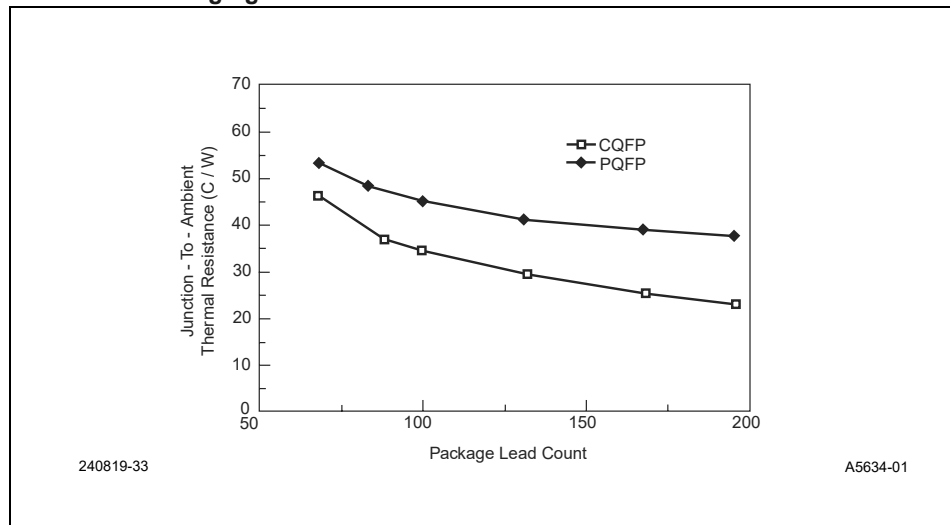
Figure 4-31. Effect of Package Size on Thermal Resistance of Leadless Ceramic Chip Carrier



4.3.4.2 Packaging Material Thermal Conductivity

Again, the one-dimensional conductive thermal resistance expression shows that thermal resistance is inversely proportional to the thermal conductivity of the packaging material. For example, aluminum oxide, the most commonly used ceramic material, has a thermal conductivity that is an order of magnitude larger than plastic materials. As a result, the internal resistance of a ceramic package is substantially lower than a plastic package from the same package family, resulting in lower overall thermal resistance (see Figure 4-32, CQFP versus PQFP).

Figure 4-32. Effect of Packaging Material on Thermal Resistance



4.3.4.3 Heat Spreader And Heat Slug

Heat spreaders and heat slugs are commonly used to improve the heat spreading effect which results in lower package internal thermal resistance. For leadframe type packages (such as PQFP and SQFP) the heat spreader plate is typically made out of Copper or Aluminum and is attached to the bottom surface of the leadframe. For CPGA type packages, the heat spreader is typically made out of Copper or Copper-Tungsten alloy and is attached to the top surface of the ceramic packages. For both types of packages, the heat slug is a metal block which on the one side is attached to the die and on the other side is exposed to the outside environment. Figure 4-33 shows the difference of thermal resistance for different PQFP package types. Figure 4-34 shows the reduction of θ_{ja} for CPGA packages by using heat spreader and heat slug when compared to standard packages. It can be seen that the effect of heat spreaders and heat slugs on thermal performance is more significant for smaller die sizes.

Figure 4-33. Effect of Heat Spreader and Heat Slug on Thermal Performance

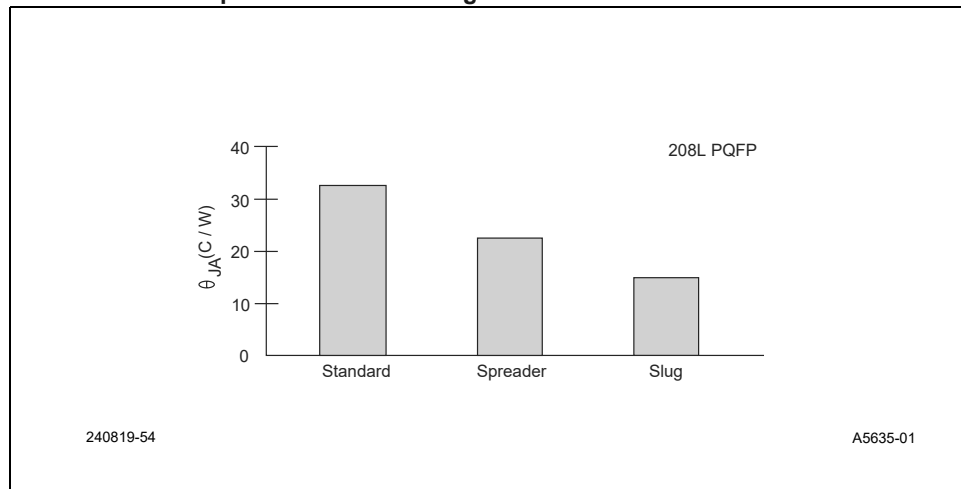
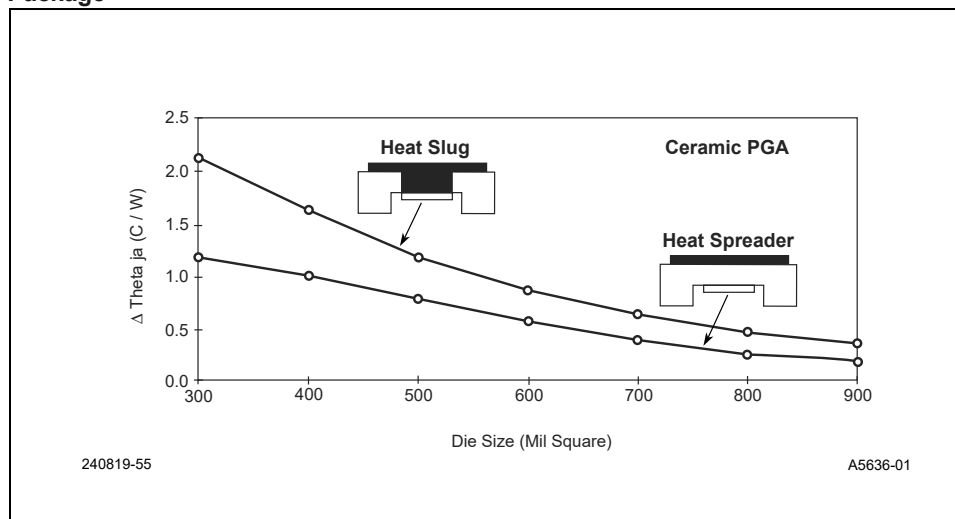


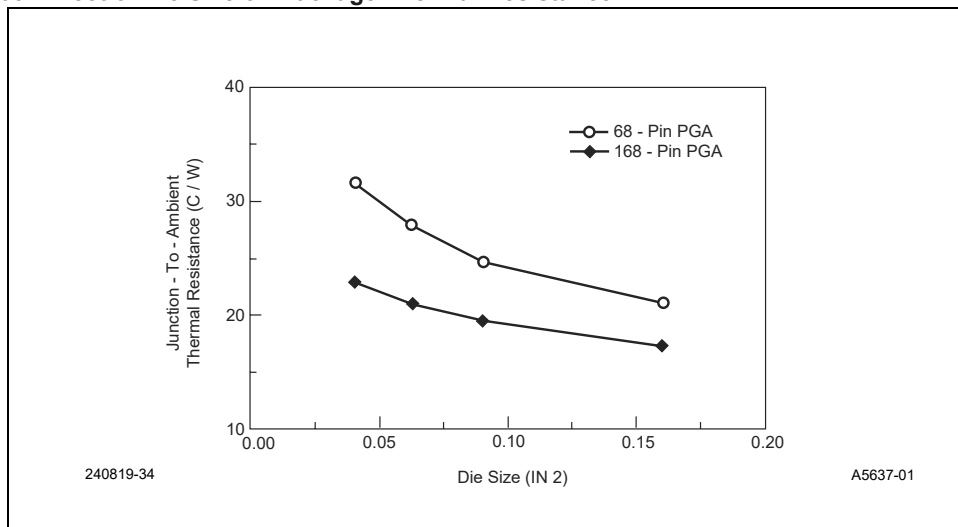
Figure 4-34. Reduction of θ_{ja} by Heat Spreader and Heat Slug when Compared to Standard Package



4.3.4.4 Die Size

As shown in Figure 4-35, thermal resistance decreases as the die sizes increases. Increase in die size results in lower power density and larger effective heat transfer area. The changes in thermal resistance are sharper at smaller die sizes, and as the die size approaches packages size, they become less significant.

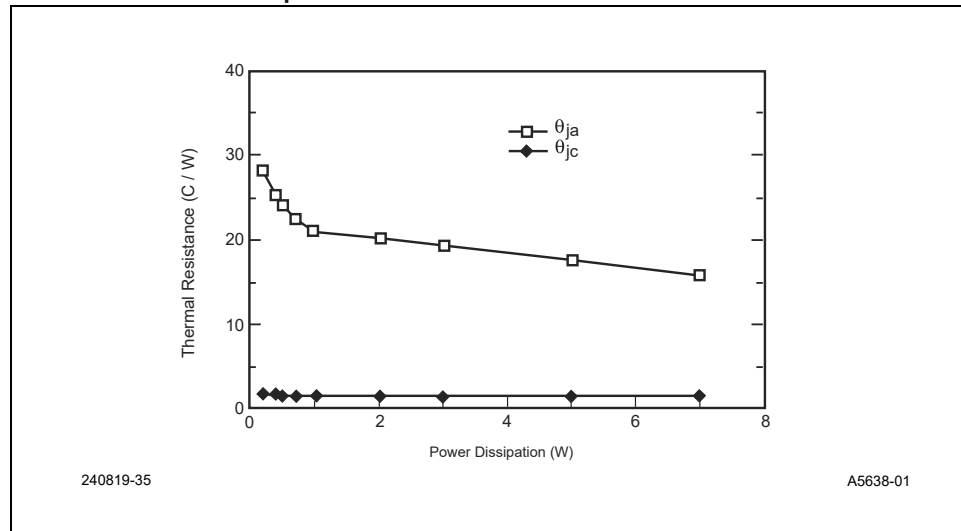
Figure 4-35. Effect of Die Size on Package Thermal Resistance



4.3.4.5 Device Power Dissipation

An increase in device power, which will raise the temperature of the package, results in lower junction-to-ambient thermal resistance (θ_{ja}) values in natural convection, while not affecting θ_{ja} in forced convection. The values of θ_{jc} do not change significantly as a function of the device power both in natural and forced convection (see Figure 4-36). In natural convection, the convective heat transfer coefficient is proportional to the temperature difference between the case and the ambient, raised to the power n , where $n = 0.25$ for laminar flow and $n = 0.33$ for turbulent flow. Therefore, the case-to-ambient thermal resistance will be inversely proportional to this temperature difference raised to the power n , and as a result, to the device power.

Figure 4-36. Effect of Power Dissipation on Thermal Resistance



It should be noted that the error in θ_{ja} also increases at lower power levels, because both temperature and power measurements are less accurate.

In the case of forced convection, the heat transfer coefficient does not depend on temperature explicitly. Dependency on temperature is only due to changes in material properties. The material properties for air do not vary significantly within the temperature ranges normally encountered. However, at low flow rates, natural and forced convection may have effects that are of the same order of magnitude (mixed convection). A small dependency on power may be observed in mixed convection heat transfer. However, as the flow rate increases the power dependency disappears.

4.3.4.6 Air Flow Rate

In forced convection, case-to-ambient thermal resistance is a function of the air flow rate, as shown by Equation 4-19:

Equation 4-19.

$$\theta_{ca} = K/V^m$$

Where:

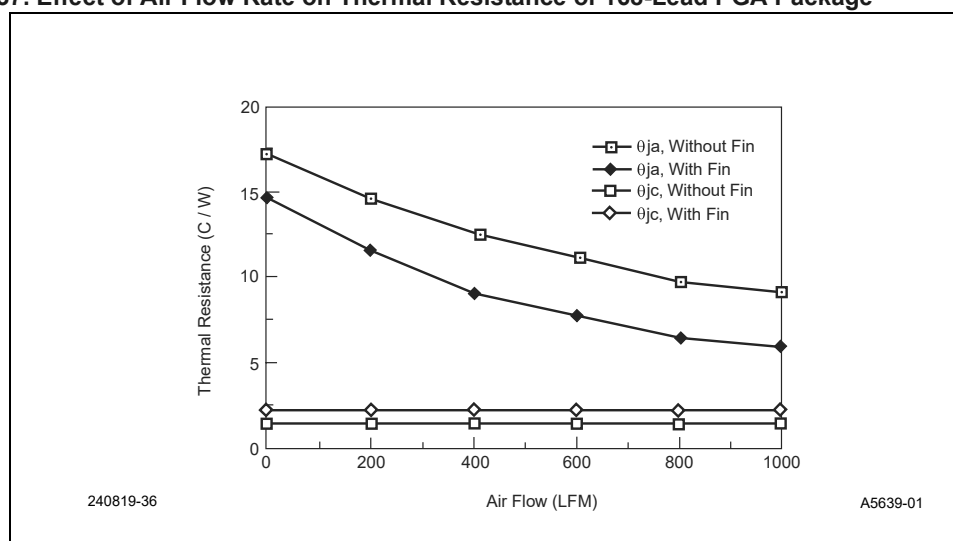
K = Constant depending on air properties as well as package geometry

V = Air velocity (m/s)
m = $1/2$ and $4/5$ for laminar and turbulent flow respectively

Figure 4-37 shows how θ_{ja} varies as a function of air flow rate for 168-lead PGA with and without heat fins. At lower air flow rates, there is a strong dependency of θ_{ja} on the air flow rate, but as the air flow rate increases, θ_{ja} values become less sensitive to the changes in the flow rate.

$$\theta_{ja} = \theta_{jc} + K/V^m$$

Figure 4-37. Effect of Air Flow Rate on Thermal Resistance of 168-Lead PGA Package



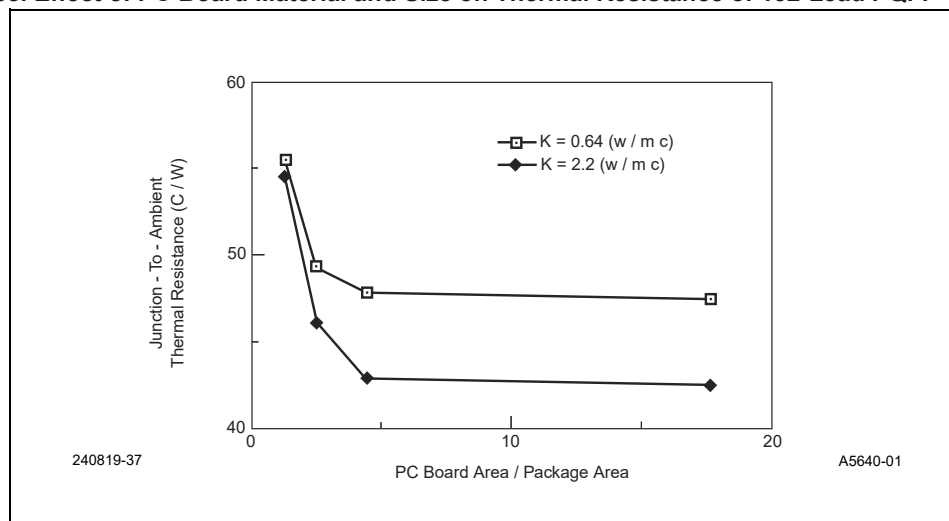
4.3.5 Mounting Parameters

4.3.5.1 PC Board Size And Thermal Conductivity

The printed circuit board on to which components are mounted can act as a fin by virtue of its thermal conductivity. The effect of conduction in the printed circuit board is illustrated in Figure 4-38. The effect of the board size on overall thermal resistance may vary, depending on the thermal resistance between the junction and the board compared to the resistance between the case and the ambient. Smaller packages with a relatively high case-to-ambient thermal resistance value are more dependent on the board for transfer of heat to ambient than are the larger size packages. Consequently, board size will have a much larger impact on the junction-to-ambient thermal resistance for such packages.

Another factor that impacts the thermal resistance from board to ambient is board thermal conductivity. As board thermal conductivity or board thickness increases, the spreading resistance for lateral conduction of heat within the board decreases. As a result a larger board area becomes available for heat transfer to the ambient.

Figure 4-38. Effect of PC Board Material and Size on Thermal Resistance of 132-Lead PQFP

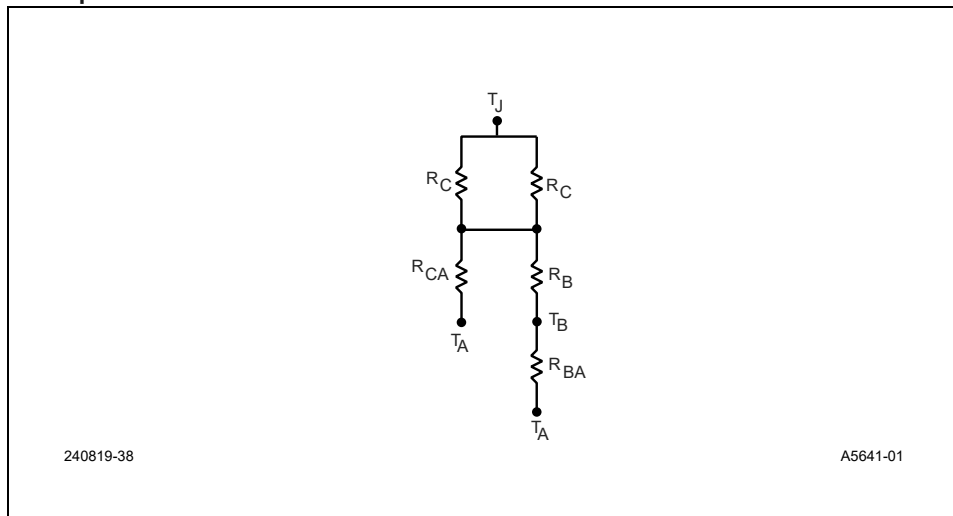


4.3.5.2 PC Board Temperature

The temperature of the printed circuit board may significantly impact package thermal resistance but is normally ignored in thermal packaging design. A board of specific size and material properties, with only the component under consideration mounted on it, will have a unique equilibrium temperature distribution under fixed environmental and mounting conditions. However, if there are other components on the board, or the board is attached to a heat sink, the maximum board temperature, T_b , may increase or decrease. A change in board temperature will affect the junction temperature and consequently the junction-to-ambient thermal resistance. The junction-to-ambient thermal resistance, θ_{ja} , measured when the board is influenced by other heating or cooling factors, is referred to as the apparent thermal resistance or systems-level thermal resistance $\theta_{ja,s}$.

In almost all practical applications, printed circuit boards are populated by many components, and heating of one package influences the thermal performance of other packages. In order to get a relatively good estimate of system thermal resistance, $\theta_{ja,s}$ and θ_{ja} values must be correlated through another parameter. As it turns out, this parameter is T_b . A simple resistor network shown in Figure 4-39 can be used to obtain this correlation. In this model, it is assumed that the heat flows from the junction to the package boundary, and from there a portion of the heat is transferred directly to the ambient, while the rest goes into the board and is distributed and transferred to the ambient.

Figure 4-39. Simplified Resistor Network



It should be noted that the model shown in Figure 4-39 is simplified, and the actual package resistor network model can be more complex. The following expression shows the relation between $\theta_{ja,s}$ and θ_{ja} and board temperature rise ($T_b - T_a$):

Equation 4-20.

$$\theta_{ja,s} = \theta_{ja} + S \left(\frac{T_b - T_a}{P} \right) \frac{SR_a R_b}{(R_a + R_b + R_{ba})}$$

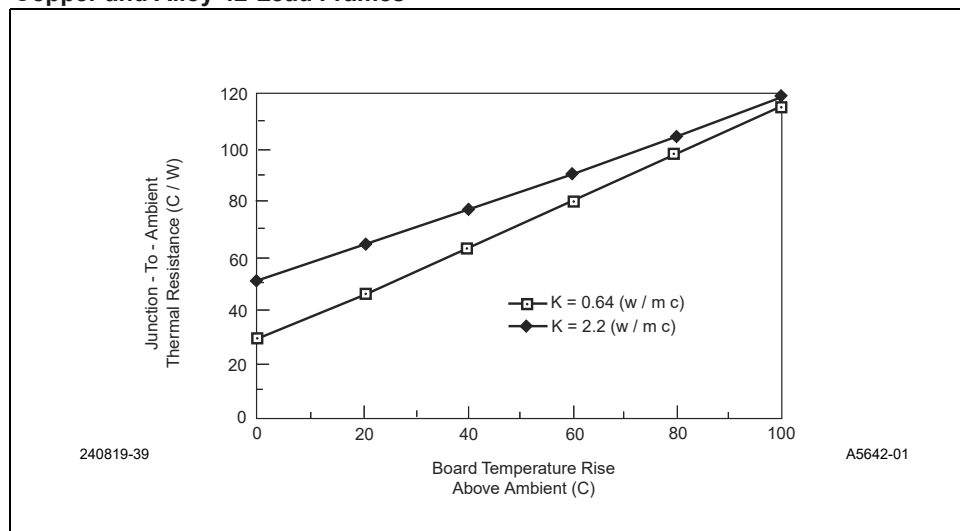
where:

$$S = \frac{R_a}{R_a + R_b}$$

- P = Power dissipation (W)
- R_a = Case-to-ambient resistance (C/W)
- R_b = Case-to-board resistance (C/W)
- R_{ba} = Board-to-ambient resistance (C/W)
- R_c = Junction-to-case resistance (C/W)
- S = Sensitivity parameter, $R_a/(R_a + R_b)$ ($0 < S < 1$)
- $T_b - T_a$ = Board temperature rise over ambient (C)

Equation 4-20 shows a linear dependence of $\theta_{ja,s}$ on board temperature rise; as the board temperature increases or decreases, the system thermal resistance will increase or decrease. The rate of these changes is dictated by sensitivity parameter S , which in turn depends on R_a/R_b . As R_a/R_b increases, thermal resistance becomes more sensitive to board temperature rise; in other words, the packages becomes more thermally coupled with other components on the board. Large values of R_a/R_b indicate that the package depends more on the board for transfer of heat to the ambient than on direct heat transfer to the ambient (larger packages vs. smaller packages). On the other hand, as R_a/R_b decreases, S decreases. Smaller R_a/R_b means a higher degree of insulation between the package and the board. For example, the thermal resistance of a package with a copper lead frame is more sensitive to board temperature rise than its counterpart with an Alloy 42 lead frame, as shown in Figure 4-40.

Figure 4-40. Effect of Board Temperature Rise on Thermal Resistance of 132-Lead PQFP with Copper and Alloy 42-Lead Frames

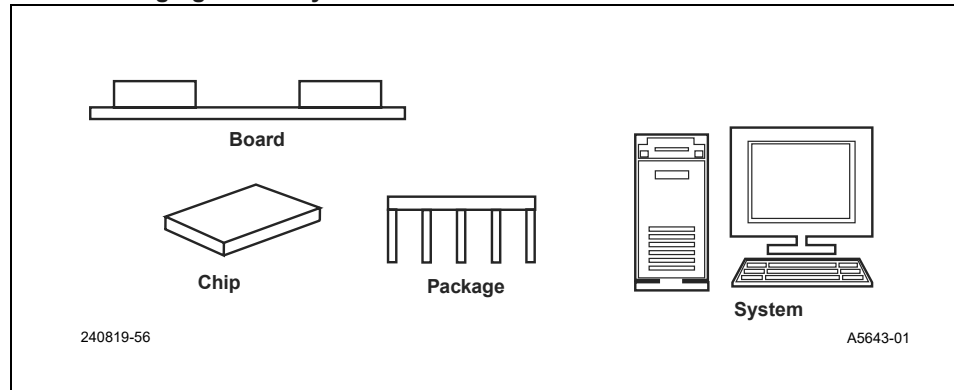


To determine sensitivity factors and intercept in expression 12, the package system thermal resistance can be measured under two different board temperature conditions (θ_{ja} is assumed to be known).

4.3.5.3 System Thermal Design

As shown in Figure 4-41, the packaging of an electronic system starts with the design or selection of the structure that houses the silicon integrated circuit or chip, proceeds to the chip-to-chip interconnect, continues to the board-to-board level and concludes at the box or cabinet, which houses the complete system.

Figure 4-41. The Packaging Hierarchy



4.3.6 Typical Configuration of PCs

PC chassis are divided into two categories: desktops and notebooks. Desktops have two major categories: LPX (Low Profile) and Baby AT. A typical LPX PC is 17" x 16" X 4". Figure 4-42 shows a general configuration. The add-in boards are inserted horizontally into the slots connected to the mother board. There are two fans, one for the power supply and one for general cooling. The total system power is usually around 100 Watts.

Figure 4-42. The Configuration of the LPX PCs

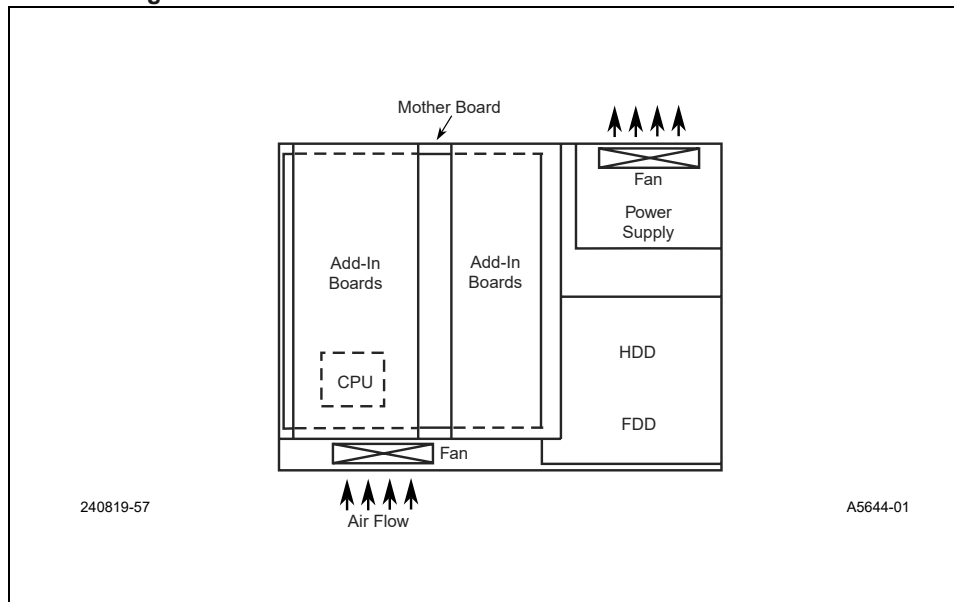


Figure 4-43 shows the configuration of the Baby AT PC. Its typical size is 20" x 17" x 6". Because of the larger available space, more add-in boards can be inserted into the mother board vertically. A typical system power is around 120 Watts.

Figure 4-44 shows the configuration of a notebook with a typical size of 11" x 9" x 2". The CPU typically consumes 4-8 Watts depending on the products used. Other components including the mother board, HDD, FDD and screen use about 6-10 Watts. The total system power is around 12-15 Watts.

Figure 4-43. The Configuration of a Typical Baby AT PC

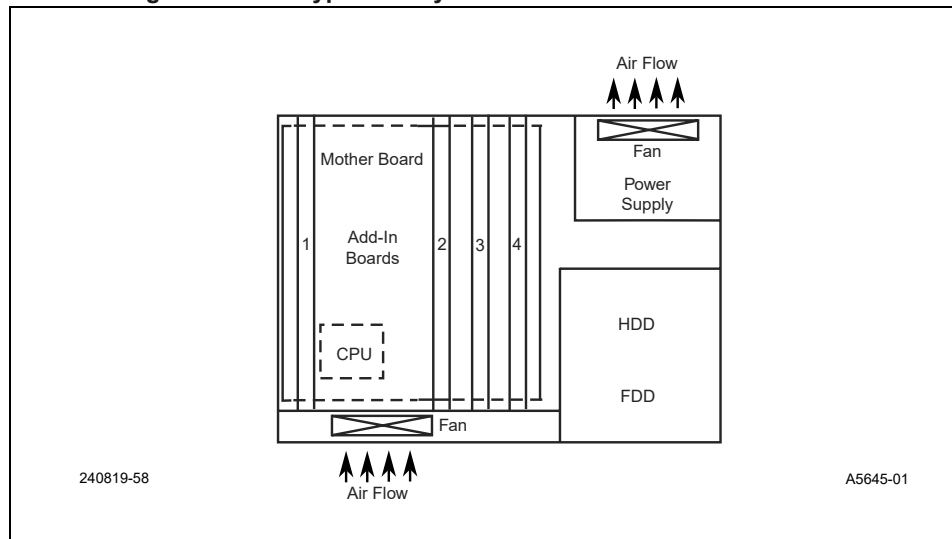
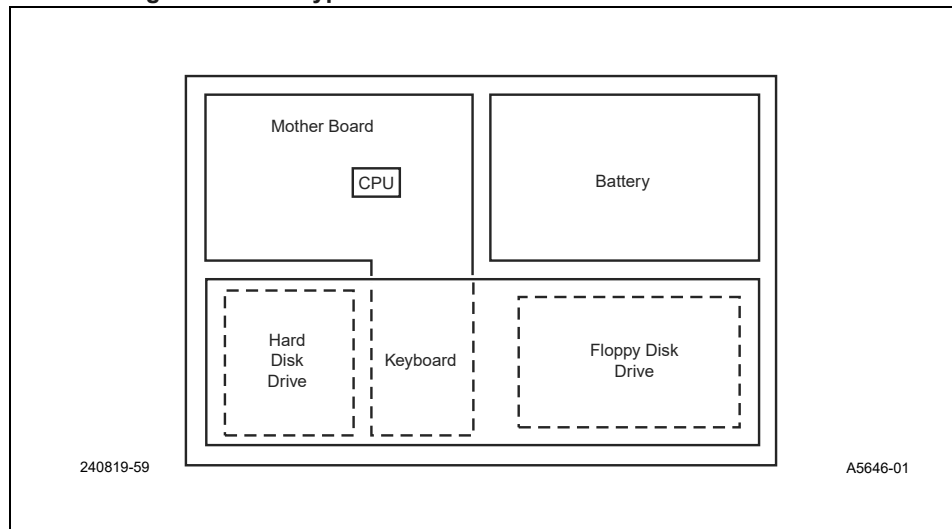


Figure 4-44. The Configuration of a Typical Notebook



4.3.6.1 Worst Case Design Methodology

For electronic systems to function properly under any circumstances, thermal designs must be obtained under the worst case scenario. These worst case conditions are briefly discussed in this section.

CPU power: The use of the maximum CPU power is recommended for system thermal design purposes. The power dissipation values for the Intel family of processors are the maximum power levels for the corresponding processors.

Component power: The thermal impact of components such as the hard disk drive, video and memory cards, and PCMCIA must be taken into account for system level thermal design. In prototype testing, load boards with simulated components can be used to generate the maximum component heat dissipation to investigate the thermal performance of the system.

Ambient temperature: Although most electronic systems work at room temperatures (25 °C), the thermal design must consider the extreme environments which the system may experience. Normally an ambient temperature of 35 °C to 40 °C is used by most system designers.

4.3.6.2 System Thermal Designs

As the total system level power dissipation increases and the system size decreases, designing a cost-effective thermal solution which satisfies all requirements is an increasingly challenging job. In general, thermal management can be divided into internal and external thermal management. Internal thermal management handles the thermal resistance from the junction to the package case, while the external thermal management handles the thermal resistance from the package case to the ambient. For a general thermal system design problem, three factors namely Budgeting, Internal Thermal Management and External Thermal Management should be considered.

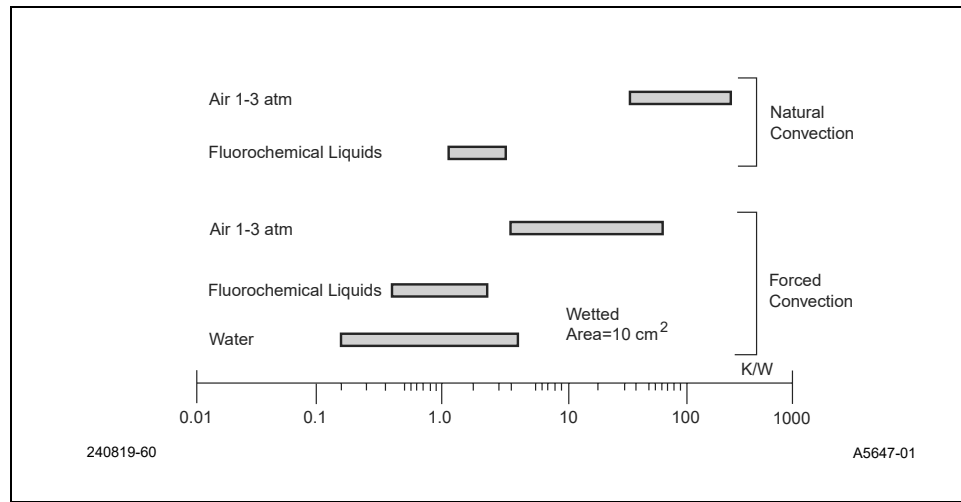
Budgeting: The total junction-to-ambient thermal resistance must be distributed among the various sections of the thermal path; from chip-to-package, package-to-heat-sink and heat-sink-to-inside-ambient and inside-ambient-to-outside ambient. The thermal resistance in each section must then be managed to meet the assigned thermal budget.

Internal thermal management: This involves selection of thermal interface materials, package type, bonding techniques, and via design. The design must also meet constraints of cost, available technologies, reliability, manufacturing processes, and yield.

External thermal management. This involves selection of the cooling mode (i.e. conduction, natural or forced convection, or radiation), heat sink design, and heat sink attachment process. Figure 4-45 shows the typical convective thermal resistance values obtained using various coolants and cooling modes.

When the component is cooled directly by contact with a gas or liquid, the resistance to the convective heat removal from the surface is inversely proportional to the product of the heat transfer coefficient and the wetted area, $1/(hA)$, where h is the convective heat transfer coefficient and A is the wetted area. As shown in Figure 4-45, the convective coefficients range from 100 K/W for natural convection of air, to 33 K/W of forced air convection, to 1 K/W in fluorochemical liquid forced convection.

When direct cooling of the package surface is inadequate to maintain the chip temperature below desired levels, a heat sink can be attached to the package. A heat sink provides a significantly larger wetted area for the heat transfer. In addition, the extended surfaces of the heat sink help to spread the heat. However, the presence of the heat sink may increase the overall pressure drop in the system, and the thermal interface between the package and the heat sink will introduce additional thermal conductive resistance. Proper management of the heat sink design and the heat sink attach method is required to achieve maximum thermal performance benefits from the use of a heat sink. Typical air-cooled heat sinks can reduce the external thermal resistance to values less than 15 K/W in natural convection and as low as 5 K/W for moderate forced convection. Liquid cooled heat sinks can further reduce the external resistance to below 1 K/W. Once the cooling mode has been selected, heat sinks, fans, and the heat sink attachment process must be optimized for the system level thermal solution.

Figure 4-45. Typical Convective Thermal Resistances for Various Coolants and Cooling Modes

4.3.6.2.1 Thermal Enhancement Options

There are many thermal enhancement options available to the package and system designer to reduce both the internal package thermal resistance as well as the package-to-ambient thermal resistance. Some of the commonly used enhancement techniques are summarized below.

Heat slug/spreader: In order for the heat to spread efficiently from the silicon die to the package, heat slugs or spreaders are used in the thermal design of many packages. The primary goal is to allow the heat to conduct from the die and spread into the heat spreader or slug. Since the heat transfer area provided by the slug is larger, it helps to reduce the thermal resistance. However, the use of heat slugs and spreaders present several design challenges; thermally induced stresses resulting from a mismatch between the coefficient of thermal expansion between the package and the heat slug or spreader, reliability of the attachment between the die and the slug, and manufacturability issues.

Thermal via and board design: Thermal vias are often used to reduce the thermal resistance of materials with low thermal conductivity like printed circuit boards or substrates. Via designs are divided into two configurations: stacked and staggered. In a stacked via design, successive via layers are stacked with vias on top of each other. In the staggered configuration, the vias are not stacked directly on top of vias in another layer.

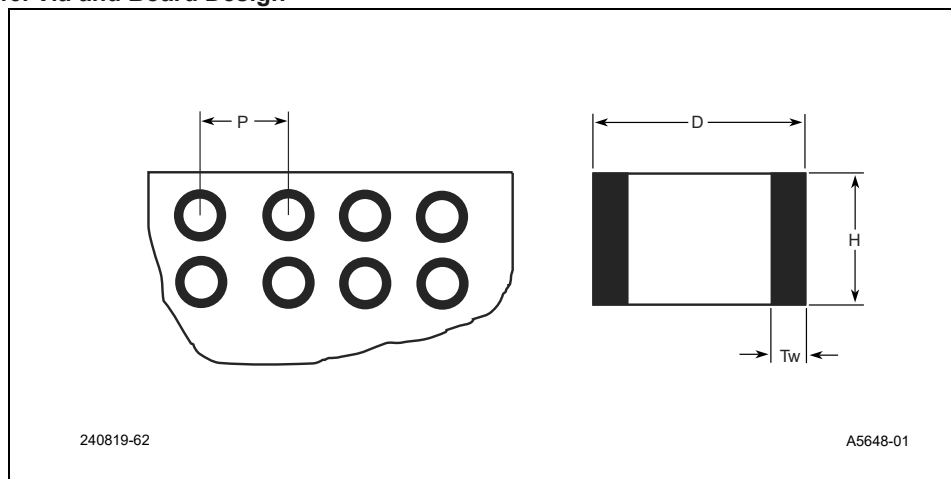
Figure 4-46 shows an example of the stacked via designs on PCB. The via has an outside diameter D , height H and is plated with copper of thickness T_w . The thermal resistance of the n vias can be approximately estimated using one dimensional heat conduction analysis:

Equation 4-21.

$$R_v = H / K n \pi (D T_w - T_w^2)$$

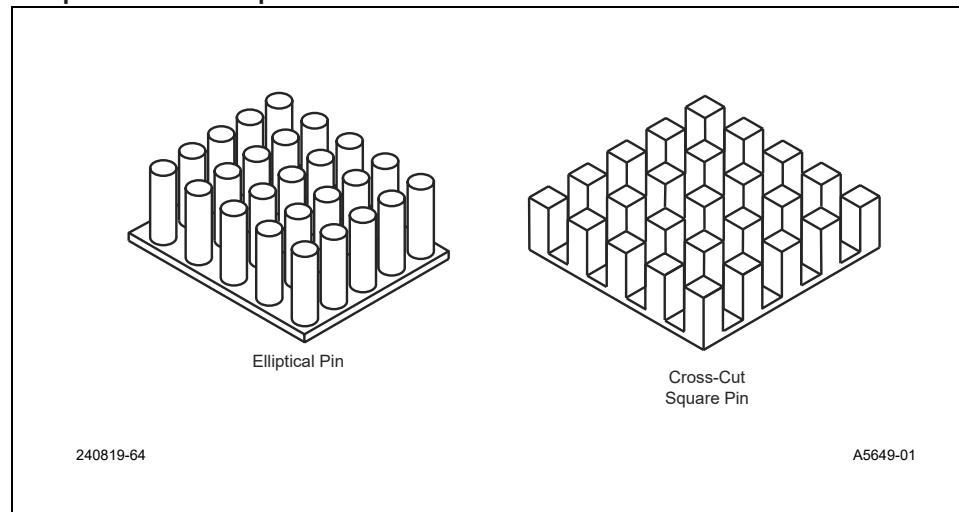
where R_v is the total thermal resistance of the number (n) of vias and K is the thermal conductivity of the via plating material. Vias reduce the thermal resistance but increase the electrical routing difficulty. The density and size of the vias depends on many factors in the design criteria: electrical routing, thermal performance requirements, cost, etc. The final design is usually a trade-off among various considerations. For a fixed pitch to diameter (say, $P/D = 2$), the criterion favors vias with small diameters. However, when the pitch is fixed, the minimum thermal resistance is obtained with larger via diameters.

Figure 4-46. Via and Board Design



Heat sinks: Heat sinks vary in shape, size and material depending on applications. Figure 4-47 shows a regular cross cut pin fin heat sink and elliptical pin fin heat sink. The purpose of heat sinks is to spread the heat and to increase the heat transfer area wetted by the coolant. Although heat sinks help in heat spreading, the presence of the fins presents a blockage to the coolant flow causing an increase in the system level pressure drop. Increased pressure drop would require a larger fan to drive the required coolant flow through the computer chassis. The heat sink design (i.e. number, shape and size of fins) must be optimized in order to maximize the heat transfer from the heat sink with the smallest possible increase in the pressure drop.

Figure 4-47. Square Pin and Elliptical Pin Heat Sinks



Metal plate or rod: Heat spreading should be considered in the thermal design of the system to minimize the temperature drop on the heat dissipating surfaces when: (1) concentrated heat must be transferred to places where space is available for more enhancements like heat sinks or fans, or simply where the thermal environment is more favorable; and (2) if a large surface area is required for heat dissipation. Table 4-17 compares the temperature drops at the ends of a 10" long 1" diameter rod with 1 Watt passing through the rod. Results show that the use of copper or aluminum decreases the thermal resistance by nearly two orders of over the typical PCB. In portable computer systems, flexible laminated copper foils called "flexible heat sinks" can be used in order to satisfy space and weight constraints.

Table 4-17. Comparison of Spreading Efficiency of Different Rods

	PCB	Aluminum	Copper	Heat pipe
Temperature Drop (°C)	251	2.51	1.26	0.034
Thermal conductivity (W/m.K)	2	200	400	14800 (equivalent)

Heat pipes: An increase in the cross-sectional area of a spreader plate made out of copper or aluminum can reduce the spreading thermal resistance. However, this approach is often constrained by the space and weight limitations of the system. Under such circumstances, heat pipes can be used for heat transfer. A typical heat pipe consists of an enclosed, partially evacuated chamber containing a small amount of liquid. The liquid evaporates in the heat pipe section in contact with a hot surface such as the processor package. The vapor travels to the colder sections of the heat pipe and condenses. The internal surface of the heat pipe consists of a mesh or sintered porous wick which transports the condensed liquid, via capillary fluid flow, to the hot section of the heat pipe. Thus, the heat pipe provides an enclosed, phase-change based system for transporting heat from hot to cold regions. Since heat removal in the hot section of the heat pipe, and condensation in the cold sections of the heat pipe involve phase change, there is almost no temperature gradient associated with transferring heat along the heat pipe. This is apparent from the temperature drop value for a heat pipe listed in Table 4-17. Heat pipe designs utilizing water, freons and dielectric fluorinert liquids are commercially available in a variety of configurations.

Fans: Fans provide forced air flow, which improves the convection coefficient significantly. Fans are widely used in desktop computers. However, their use in notebooks will require the resolution of issues typical of portables: power consumption (reducing battery life), space limitations, noise

and reliability. In spite of these constraints, the use of fans in high performance notebooks is gaining acceptance because of the steady increase of CPU power and the fact that alternative non-fan solutions are becoming increasingly complicated and expensive.

Fan-sinks. Fans are most effective when combined with heat sinks. Fan-sinks have emerged to provide an integrated solution in improving the thermal performance while achieving smaller overall size and higher efficiency.

Active thermal feedback (ATF). The worst case design methodology often creates products that are “over-designed.” With the increasing complexity of thermal solutions, in many applications it may not be economical to design products for the worst thermal case, which happens only to a very small portion of the products. Rather ATF can be implemented to deal with those extreme occasions. When the temperature of main components (say, CPU) reach certain threshold, ATF will throttle the clock speed to reduce the power consumption of the system until the temperature of the system decreases to a safe level.

It should be noted that when developing a thermal management strategy for the electronic system, it is no longer sufficient to focus only on temperature. Rather, the thermal/packaging engineer has to understand, control and ultimately eliminate the thermally induced failures present throughout the electronic system. The attainment of that goal, accompanied by the severe electrical, manufacturing, cost and reliability constraints, demands better collaboration of engineers with various backgrounds to better the design of the system so that it can provide all the desired functions reliably and inexpensively.

4.3.7 Design Methodology

Thermal packaging design at the component and system level may involve both experimental validation and modeling. The following sections describe the test methodology which can be used to determine various package level thermal resistances.

4.3.7.1 Junction Temperature Measurements

In order to calculate thermal resistance values, the junction temperature is measured using the temperature- sensitive parameter (TSP) method. This method employs special test structures which are the same size as the actual device. The test structure typically consists of a resistive heater to simulate device power dissipation. The temperature sensors, located at different points on the test structure, may either be temperature sensitive diodes or resistors. Temperature measurements from these on-die temperature sensors are used to obtain an accurate estimate of the junction temperature.

A single package is mounted either directly or via a socket on a thermal test board. Different test board designs, are used for surface mount and through-hole mount packages(see Figure 4-48 and Figure 4-49 respectively). The test chamber volume is 1ft³, and the ambient temperature is measured 12 inches away from the package (see Figure 4-50). In order to obtain accurate temperature measurements from the temperature sensing diodes/resistors, the diode output voltage or sensor resistance must first be correlated to the temperature. This is done using a three point calibration technique. For calibration purposes, the test board assembly is immersed in a constant, uniform temperature dielectric fluid bath. The temperature of the dielectric fluid in the bath is measured using an RTD probe. The dielectric fluid in the bath is continuously stirred in order to maintain temperature uniformity. If the temperature sensors are diodes, they are forward-biased using a 100 mA constant current source and the voltage drop across the diode is measured at 3 different bath temperatures. If the temperature sensors are resistors, a four wire resistance measurement is obtained at 3 different bath temperatures. A linear best fit straight line correlation is usually obtained to relate the diode voltage drop or sensor resistance to the measured bath temperature.

After calibration, the test structure is powered up to the desired power level. The on-die temperature sensors are continuously monitored until no change is detected in the temperature level, indicating an equilibrium state. At this stage, the chip surface temperatures, ambient and case temperatures, and device voltage drop and current are recorded. The device voltage drop and current are used to estimate the actual power dissipated in the test structure. When measuring thermal resistance under forced convection conditions, the test board assembly is exposed to a developed air flow. In this case, air velocity is measured at a location 12 inches upstream from the leading edge of the test board, using a hot wire anemometer. Air temperature is also measured at the same location.

Figure 4-49. Typical Thermal Test Board for Through Surface Mount Component

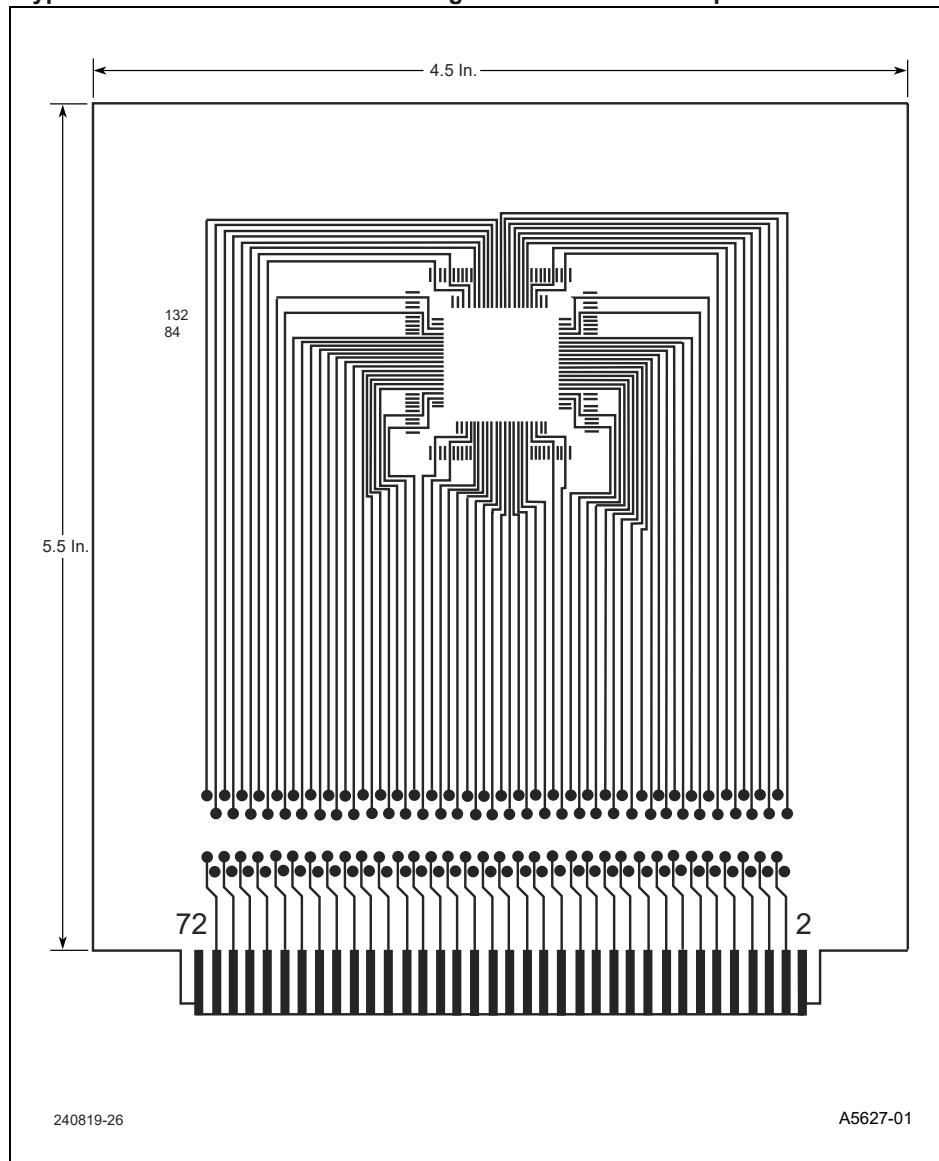
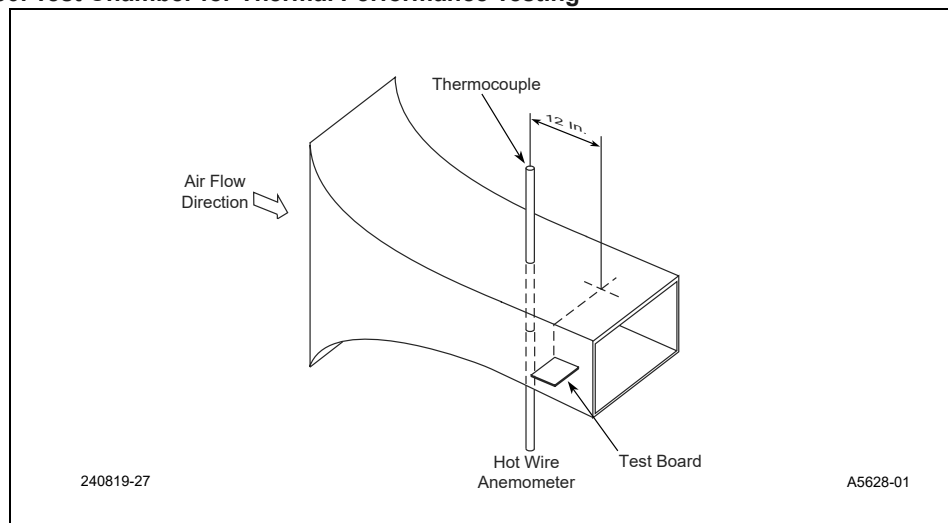


Figure 4-50. Test Chamber for Thermal Performance Testing

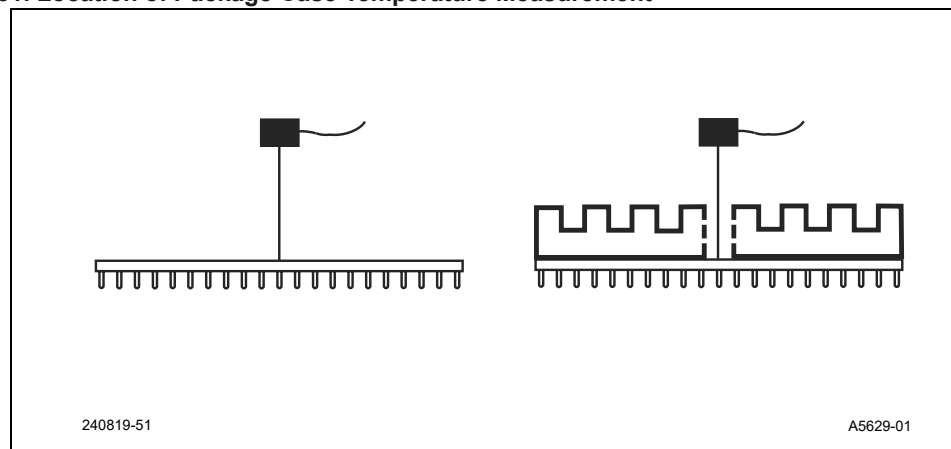


4.3.7.2 Case Temperature Measurement

Case temperature, " T_c ", is measured at the center of the top surface of the package. This is typically the location with the highest temperature on the package case. Special care is required when measuring the case temperature to ensure an accurate temperature measurement. Usually, a thermocouple attached to the top surface of the package is used to measure T_c . Thermocouples must be calibrated before making temperature measurements. Moreover, different types of measurement errors are introduced when measuring the temperature of a surface which is at a temperature different from that of the surrounding ambient air. These errors could be caused due to poor thermal contact between the thermocouple junction and the package case, and due to heat loss by radiation or by conduction through the thermocouple leads. To minimize measurement errors, the following approach is recommended:

- Use 36 gauge or finer diameter, type K, T, or J thermocouples. Intel laboratory testing is performed using type K thermocouples made by Omega (part number: 5TC-TTK-36-36).
- Attach the thermocouple bead to the center of the package top surface using high thermal conductivity cements. The laboratory testing is performed by using Omega Bond (part number: OB-101).
- The thermocouple should be attached at a 90° angle as shown in Figure 4-51.
- If the case temperature is measured with a heat sink attached to the package, drill a hole (no larger than 0.15 inches) through the heat sink to route the thermocouple wire out Figure 4-51.

Figure 4-51. Location of Package Case Temperature Measurement



4.3.7.3 Numerical Modeling

During the initial phases of the thermal design, numerical modeling can be very effectively used to investigate feasibility of the design. Numerical modeling provides significant savings because it eliminates the need for expensive prototype fabrication and time consuming experimental measurements. Package level numerical models, validated using experimental measurements, can be incorporated in system level models to compare various system level design options. A large selection of very sophisticated computational tools for thermal and fluid flow analysis are available commercially. Some of the tools like ANSYS, PATRAN/ABAQUS, and Ideas are suitable for detailed investigations of heat conduction within a board or a component. Other tools like IcePak, Flotherm, Ideas-TMG, Coolit etc. provide the ability to solve conjugate problems involving fluid flow and heat transfer. These tools provide sophisticated, easy to use graphic interfaces and can be used very effectively to analyse the fluid flow and heat transfer phenomena within complete electronic systems.

Numerical models usually incorporate highly simplified representations of electronic components. Additionally, detailed modeling of components results in large computational times but seldom adds much value to the thermal performance trends. The thermal properties of commonly encountered materials such as Silicon or Aluminum are well known and can be directly inserted in the thermal model. However, components like the printed circuit boards and substrates are made out of many layers of and other insulating materials. Moreover, the copper layers are not single sheets of copper; they have cutouts due to the presence of traces, vias and other electrical structures. Due to the complexity of the actual substrate construction, it is difficult to estimate the effective thermal properties with a high degree of accuracy. In almost all cases, these thermal properties must be determined by using experimental measurements to validate the model predictions.

For validation purposes, the component and test board are instrumented with thermocouples to measure the temperature distribution within and on the component and on the substrate. Thermocouples are also used to measure case and ambient temperatures. The experiments are conducted using a partial factorial design. A factorial design involves independently powering up individual components. Powering up a single component allows the ability to monitor the heat spreading inside the component and also within the substrate. This data is very useful to determine

the thermal properties for simplified component representations. Such experimental data can be used to determine the thermal properties which when used in the numerical model would provide temperature predictions to a reasonable degree of accuracy.

4.4 References

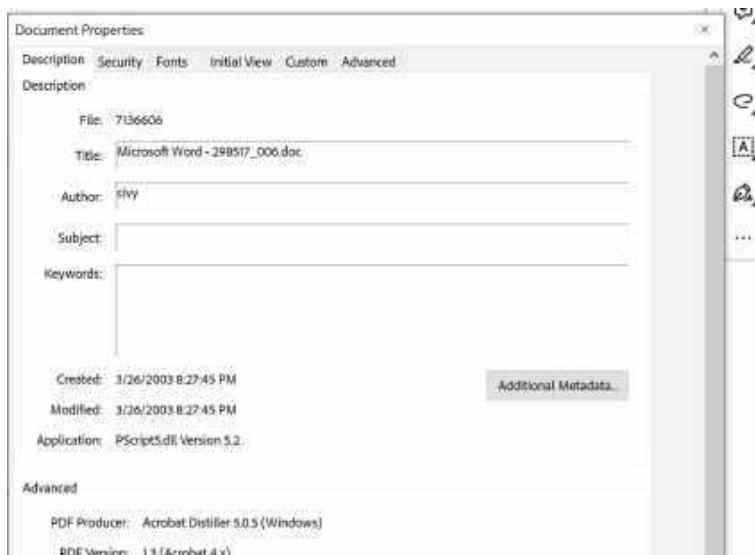
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4.5 Revision Summary

- Re-wrote section 4.2
- Re-wrote several portions of section 4.3
- Added a section on numerical modeling
- General edit of all other sections

APPENDIX INTEL2003-02





Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages

At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz

[Datasheet](#)

April 2003



Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages

At 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 866 MHz, 733 MHz, 650 MHz; and Ultra Low Voltage 800 MHz, 733 MHz, 700 MHz, and 650 MHz

Datasheet

April 2003



Order Number: 298517-006

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Contents

1.	Introduction	10
1.1	Overview	10
1.2	State of the Data	11
1.3	Terminology	11
1.4	References	12
2.	Mobile Intel Celeron Processor Features	13
2.1	New Features in the Mobile Intel Celeron Processor	13
2.1.1	133-MHz PSB With AGTL Signaling	13
2.1.2	256-K On-die Integrated L2 Cache	13
2.1.3	Data Prefetch Logic	13
2.1.4	Differential Clocking	13
2.1.5	Signal Differences Between the Mobile Intel Celeron Processor (0.18 μ) (in BGA2 and Micro-PGA2 Packages) and the Mobile Intel Celeron Processor (0.13 μ) (in Micro-FCBGA and Micro-FCPGA Packages)	14
2.2	Power Management	14
2.2.1	Clock Control Architecture	14
2.2.2	Normal State	14
2.2.3	Auto Halt State	14
2.2.4	Quick Start State	15
2.2.5	HALT/Grant Snoop State	16
2.2.6	Deep Sleep State	16
2.2.7	Operating System Implications of Low-power States	17
2.3	AGTL Signals	17
2.4	Mobile Intel Celeron Processor CPUID	17
3.	Electrical Specifications	19
3.1	Processor System Signals	19
3.1.1	Power Sequencing Requirements	20
3.1.2	Test Access Port (TAP) Connection	20
3.1.3	Catastrophic Thermal Protection	21
3.1.4	Unused Signals	21
3.1.5	Signal State in Low-power States	21
3.1.5.1	System Bus Signals	21
3.1.5.2	CMOS and Open-drain Signals	21
3.1.5.3	Other Signals	22
3.2	Power Supply Requirements	22
3.2.1	Decoupling Guidelines	22
3.2.2	Voltage Planes	22
3.2.3	Voltage Identification	23
3.2.4	VTPWRGD Signal Quality Specification	24
3.2.4.1	Transition Region	24
3.2.4.2	Transition Time	24
3.2.4.3	Noise	25
3.3	System Bus Clock and Processor Clocking	25
3.4	Maximum Ratings	26
3.5	DC Specifications	26

3.6	AC Specifications	41
3.6.1	System Bus, Clock, APIC, TAP, CMOS, and Open-drain AC Specifications	41
4.	System Signal Simulations	58
4.1	System Bus Clock (BCLK) and PICCLK DC Specifications and AC Signal Quality Specifications	58
4.2	AGTL AC Signal Quality Specifications	60
4.3	Non-AGTL Signal Quality Specifications	61
4.3.1	PWRGOOD, VTPWRGD Signal Quality Specifications	62
4.3.1.1	VTPWRGD Noise Parameter Specification	62
4.3.1.2	VTPWRGD Transition Parameter Recommendation	63
4.3.1.2.1	Transition Region	63
4.3.1.2.2	Transition Time	63
4.3.1.2.3	Noise	63
5.	Mechanical Specifications	65
5.1	Socketable Micro-FCPGA Package	65
5.2	Surface Mount Micro-FCBGA Package	69
5.3	Signal Listings	73
6.	V _{CC} Thermal Specifications	80
6.1	Thermal Diode	82
7.	Processor Initialization and Configuration	83
7.1	Description	83
7.1.1	Quick Start Enable	83
7.1.2	System Bus Frequency	83
7.1.3	APIC Enable	83
7.2	Clock Frequencies and Ratios	83
8.	Processor Interface	84
8.1	Alphabetical Signal Reference	84
8.2	Signal Summaries	94
Appendix A.	PLL RLC Filter Specification	96
A1.	Introduction	96
A2.	Filter Specification	96
A3.	Recommendation for Mobile Systems	97
A4.	Comments	98

Figures

Figure 1. Clock Control States.....	15
Figure 2. PLL RLC Filter.....	23
Figure 3. VTTTPWRGD System-Level Connections.....	24
Figure 4. Noise Estimation	25
Figure 5. Illustration of V_{CC} Static and Transient Tolerances ($V_{ID} = 1.15$ V)	37
Figure 6. Illustration of Deep Sleep V_{CC} Static and Transient Tolerances (V_{ID} Setting = 1.15 V)	37
Figure 7. Illustration of V_{CC} Static and Transient Tolerances ($V_{ID} = 1.40$ V)	38
Figure 8. Illustration of Deep Sleep V_{CC} Static and Transient Tolerances (V_{ID} Setting = 1.40 V)	39
Figure 9. BCLK (Single Ended)/PICCLK/TCK Generic Clock Timing Waveform.....	49
Figure 10. Differential BCLK/BCLK# Waveform (Common Mode).....	49
Figure 11. BCLK/BCLK# Waveform (Differential Mode)	50
Figure 12. Valid Delay Timings.....	50
Figure 13. Setup and Hold Timings.....	51
Figure 14. Cold/Warm Reset and Configuration Timings.....	51
Figure 15. Power-on Sequence and Reset Timings.....	52
Figure 16. Power Down Sequencing and Timings (V_{CC} Leading)	53
Figure 17. Power Down Sequencing and Timings (V_{CCT} Leading).....	54
Figure 18. Test Timings (Boundary Scan).....	55
Figure 19. Test Reset Timings	55
Figure 20. Quick Start/Deep Sleep Timing (BCLK Stopping Method).....	56
Figure 21. Quick Start/Deep Sleep Timing (DPSLP# Assertion Method)	57
Figure 22. BCLK (Single Ended)/PICCLK Generic Clock Waveform	59
Figure 23. Maximum Acceptable Overshoot/Undershoot Waveform	60
Figure 24. VTTTPWRGD Noise Specification	64
Figure 25. Socketable Micro-FCPGA Package - Top and Bottom Isometric Views.....	66
Figure 26. Socketable Micro-FCPGA Package - Top and Side View	67
Figure 27. Socketable Micro-FCPGA Package - Bottom View	68
Figure 28. Micro-FCBGA Package – Top and Bottom Isometric Views.....	70
Figure 29. Micro-FCBGA Package – Top and Side Views.....	71
Figure 30. Micro-FCBGA Package - Bottom View	72
Figure 31. Pin/Ball Map - Top View.....	73
Figure 32. PLL Filter Specifications.....	97

Tables

Table 1. New and Revised Mobile Intel Celeron Processor (0.13 μ) Signals	14
Table 2. Clock State Characteristics	17
Table 3. Mobile Intel Celeron Processor CPUID	18
Table 4. Mobile Intel Celeron Processor CPUID Cache and TLB Descriptors	18
Table 5. System Signal Groups	19
Table 6. Recommended Resistors for Mobile Intel Celeron Processor Signals	20
Table 7. Mobile Intel Celeron Processor VID Values	23
Table 8. VTPWRGD Noise Specification	24
Table 9. VTPWRGD Transition Time Specification	24
Table 10. Mobile Intel Celeron Processor Absolute Maximum Ratings	26
Table 11. Power Specifications for Mobile Intel Celeron Processor ¹	27
Table 12. V_{CC} Tolerances for the Low Voltage Mobile Intel Celeron Processor: VID = 1.15 V	28
Table 13. V_{CC} Tolerances for the Low Voltage Mobile Intel Celeron Processor in the Deep Sleep State: VID = 1.15 V	29
Table 14. V_{CC} Tolerances for the Ultra Low Voltage Mobile Intel Celeron Processor: VID = 1.1 V	29
Table 15. V_{CC} Tolerances for the Ultra Low Voltage Mobile Intel Celeron Processor in the Deep Sleep State: VID = 1.1 V	30
Table 16. V_{CC} Tolerances for the Mobile Intel Celeron Processor: VID = 1.40 V	31
Table 17. V_{CC} Tolerances for the Mobile Intel Celeron Processor in the Deep Sleep State: VID = 1.40 V	32
Table 18. V_{CC} Tolerances for the Mobile Intel Celeron Processor: VID = 1.45 V	33
Table 19. V_{CC} Tolerances for the Mobile Intel Celeron Processor in the Deep Sleep State: VID = 1.45 V	34
Table 20. V_{CC} Tolerances for the Mobile Intel Celeron Processor: VID = 1.50 V	35
Table 21. V_{CC} Tolerances for the Mobile Intel Celeron Processor in the Deep Sleep State: VID = 1.50 V	36
Table 22. AGTL Signal Group DC Specifications	40
Table 23. AGTL Bus DC Specifications	40
Table 24. CLKREF, APIC, TAP, CMOS, and Open-drain Signal Group DC Specifications	41
Table 25. System Bus Clock AC Specifications (Differential)	42
Table 26. System Bus Clock AC Specifications (133 MHz, Single Ended)	43
Table 27. System Bus Clock AC Specifications (100 MHz, Single Ended)	43
Table 28. Valid Mobile Intel Celeron Processor Frequencies	44
Table 29. AGTL Signal Groups AC Specifications	45
Table 30. CMOS and Open-drain Signal Groups AC Specifications	45
Table 31. Reset Configuration AC Specifications and Power On/Power Down Timings	46
Table 32. APIC Bus Signal AC Specifications	47
Table 33. TAP Signal AC Specifications	48
Table 34. Quick Start/Deep Sleep AC Specifications	48
Table 35. BCLK (Differential) DC Specifications and AC Signal Quality Specifications	58
Table 36. BCLK (Single Ended) DC Specifications and AC Signal Quality Specifications	58
Table 37. PICCLK DC Specifications and AC Signal Quality Specifications	59
Table 38. 133-MHz AGTL Signal Group Overshoot/Undershoot Tolerance at the Processor Core	61
Table 39. 100-MHz AGTL Signal Group Overshoot/Undershoot Tolerance at the Processor Core	61
Table 40. Non-AGTL Signal Group Overshoot/Undershoot Tolerance at the Processor Core	62
Table 41. VTPWRGD Noise Parameter Specification	62



Table 42. VTPWRGD Transition Parameter Recommendation	63
Table 43. Socketable Micro-FCPGA Package Specification	65
Table 44. Micro-FCBGA Package Mechanical Specifications.....	69
Table 45. Signal Listing in Order by Pin/Ball Number	74
Table 46. Signal Listing in Order by Signal Name.....	77
Table 47. Voltage and No-Connect Pin/Ball Locations	79
Table 48. Power Specifications for Mobile Intel Celeron Processor	81
Table 49. Thermal Diode Interface	82
Table 50. Thermal Diode Specifications	82
Table 51. BSEL[1:0] Encoding	86
Table 52. Input Signals	94
Table 53. Output Signals	94
Table 54. Input/Output Signals (Single Driver).....	95
Table 55. Input/Output Signals (Multiple Driver)	95
Table 56. PLL Filter Inductor Recommendations	97
Table 57. PLL Filter Capacitor Recommendations.....	97
Table 58. PLL Filter Resistor Recommendations.....	98

Revision History

Date	Revision	Updates
October 2001	298517-001	Initial release
January 2002	298517-002	Updates include: - Added new processor speeds 1.2 GHz, 1.13 GHz, and 1.06 GHz at 1.45V. - Added new Low Voltage 667 MHz - Added new Ultra Low Voltage 650 MHz - Updated Processor Specifications (Tables 9, 12-15, 40) - Added Specification Clarification for VTPWRGD in Table 25, Figure 21 and Section 4.3.1 - Added note 5 CMOSREF resistor divider recommendations to Table 24. - Updated references
June 2002	298517-003	Updates include: - Targeted processor frequencies updated - Updated Tables 3, 9, 12 - 19, 29, and 44 - Updated/corrected Tables 39 and 40 - Updated Figure 5- Figure 7 - Updated Section 5 - Updated CMOSREF description in Section 8.1 - Added Section 3.2.4
August 2002	298517-004	Updates include: - Added new processor frequencies - Updated Table 11 and Table 48
December 2002	298517-005	Updates include: - Added new processor frequencies - Updated Table 11 and Table 48
April 2003	298517-006	Updates include: - Added new processor frequencies (1.26 GHz) - Updated Table 11 and Table 48

Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages

Product Features

- Mobile Intel® Celeron® Processor with the following Processor core/bus speeds:
 - 1.333 GHz/133 MHz at 1.50 V
 - 1.200 GHz/133 MHz at 1.45 V
 - 1.133 GHz/133 MHz at 1.45 V
 - 1.066 GHz/133 MHz at 1.45 V
 - 1.266 GHz/133 MHz at 1.40 V
 - 1.000 GHz/133 MHz at 1.40 V
- Low Voltage Mobile Intel Celeron Processor (0.13 μ) with the following Processor core/bus speeds:
 - 866/133 MHz at 1.15 V
 - 733/133 MHz at 1.15 V
 - 650/100 MHz at 1.15 V
- Ultra Low Voltage Mobile Intel Celeron processor (0.13 μ) with the following Processor core/bus speeds:
 - 800/133 MHz at 1.10V
 - 733/133 MHz at 1.10V
 - 700/100 MHz at 1.10V
 - 650/100 MHz at 1.10 V
- Supports the Intel Architecture with Dynamic Execution
- On-die primary 16-Kbyte instruction cache and 16-Kbyte write-back data cache
- On-die second level cache (256-Kbyte) with Advanced Transfer Cache Architecture
- Data Prefetch Logic
- Integrated AGTL termination
- Integrated math co-processor
- Micro-FCPGA and Micro-FCBGA packaging technologies
 - Supports thin form factor notebook designs
 - Exposed die enables more efficient heat dissipation
 - Mobile ULV and LV Celeron processor (0.13 μ) are available only in Micro-FCBGA package.
 - Mobile Intel Celeron processors at 1.45 V and 1.50 V are available only in Micro-FCPGA package.
- Fully compatible with previous Intel microprocessors
 - Binary compatible with all applications
 - Support for MMX™ technology
 - Support for Streaming SIMD Extensions
- Power Management Features
 - Quick Start and Deep Sleep modes provide low power dissipation
- On-die thermal diode

1. Introduction

Using Intel's advanced 0.13-micron process technology with copper interconnect, the Mobile Intel Celeron Processor offers high-performance and low-power consumption. The Mobile Intel Celeron Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA packages (hereafter referred to as "the Mobile Intel Celeron Processor") is based on the same core as existing mobile Intel® Pentium® III Processor-M. Key performance features include Internet Streaming SIMD instructions, an Advanced Transfer Cache architecture, and a processor system bus speed of 133 MHz. The Low Voltage and Ultra Low Voltage Mobile Intel Celeron Processors will support both a 133-MHz and 100-MHz bus speed. These features are offered in Micro-FCPGA packages for socketable boards and Micro-FCBGA packages for surface mount boards. The Low Voltage and Ultra Low Voltage Mobile processors will be available only in the Micro-FCBGA package. The Mobile Intel Celeron processors at 1.45 V and at 1.50 V are available only in the Micro-FCPGA package. All of these technologies make outstanding performance possible for mobile PCs in a variety of shapes and sizes.

The 256-KB integrated L2 cache based on the Advanced Transfer Cache architecture runs at full speed and is designed to help improve performance. It complements the system bus by providing critical data faster and reducing total system power consumption. The processor also features Data Prefetch Logic that speculatively fetches data to the L2 cache, resulting in improved performance. The Mobile Intel Celeron Processor's 64-bit wide Assisted Gunning Transceiver Logic (AGTL) system bus provides a glue-less, point-to-point interface for a memory controller hub.

This document covers the electrical, mechanical, and thermal specifications for the following:

- The Mobile Intel Celeron Processor at the following frequencies and voltages: 1.33 GHz at 1.50 V; 1.2 GHz, 1.13 GHz, 1.06 GHz at 1.45 V; and 1.266GHz, 1 GHz at 1.40 V.
- The Low Voltage Mobile Intel Celeron Processor at the following frequencies and voltages: 866 MHz, 733 MHz and 650 MHz at 1.15 V.
- The Ultra Low Voltage Mobile Intel Celeron Processor at the following frequencies and voltages: 800 MHz, 733 MHz, 700 MHz, and 650 MHz at 1.10 V.
- Unless explicitly stated, all references to the Mobile Intel Celeron Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA packages in this document also apply to the Low Voltage and Ultra Low Voltage Mobile Intel Celeron Processor (0.13 μ) in the Micro-FCBGA package.

1.1 Overview

- Performance features
 - Supports the Intel Architecture with Dynamic Execution
 - Supports the Intel Architecture MMX™ technology
 - Supports Streaming SIMD Extensions for enhanced video, sound, and 3D performance
 - Integrated Intel Floating Point Unit compatible with the IEEE 754 standard
 - Data Prefetch Logic
- On-die primary (L1) instruction and data caches
 - 4-way set associative, 32-byte line size, 1 line per sector
 - 16-Kbyte instruction cache and 16-Kbyte write-back data cache
 - Cacheable range controlled by processor programmable registers

- On-die second level (L2) cache
 - 8-way set associative, 32-byte line size, 1 line per sector
 - Operates at full core speed
 - 256-Kbyte ECC protected cache data array
- AGTL system bus interface
 - 64-bit data bus, 100-MHz and 133-MHz operation
 - Uniprocessor, two loads only (processor and chipset)
 - Integrated termination
- Processor clock control
 - Quick Start for low power, low exit latency clock “throttling”
 - Deep Sleep mode for lower power dissipation
- Thermal diode for measuring processor temperature

1.2 State of the Data

All information in this document is the best available information at the time of publication. Revisions of this document will be provided on an as-required basis until the Mobile Intel Celeron Processor is released for production orders.

1.3 Terminology

Term	Definition
#	A “#” symbol following a signal name indicates that the signal is active low. This means that when the signal is asserted (based on the name of the signal) it is in an electrical low state. Otherwise, signals are driven in an electrical high state when they are asserted. In state machine diagrams, a signal name in a condition indicates the condition of that signal being asserted
!	Indicates the condition of that signal not being asserted. For example, the condition “!STPCLK# and HS” is equivalent to “the active low signal STPCLK# is unasserted (i.e., it is at 1.5V) <i>and</i> the HS condition is true.”
L	Electrical low signal levels
H	Electrical high signal levels
0	Logical low. For example, BD[3:0] = “1010” = “HLHL” refers to a hexadecimal “A,” and D[3:0]# = “1010” = “LHLH” also refers to a hexadecimal “A.”
1	Logical high. For example, BD[3:0] = “1010” = “HLHL” refers to a hexadecimal “A,” and D[3:0]# = “1010” = “LHLH” also refers to a hexadecimal “A.”
TBD	Specifications that are yet to be determined and will be updated in future revisions of the document.
X	Don’t care condition

1.4 References

- *P6 Family of Processors Hardware Developer's Manual* (Order Number 244001-001)
- *Intel® Architecture Optimization Reference Manual* (Order Number 245127-001)
- *Intel® Architecture Software Developer's Manual*
 - Volume I: Basic Architecture (Order Number 245470)
 - Volume II: Instruction Set Reference (Order Number 245471)
 - Volume III: System Programming Guide (Order Number 245472)
- *CK-408 (CK-Titan) Clock Synthesizer/Driver Specification* (Contact your Intel Field Sales Representative)
- *Mobile Intel® Pentium® III Processor-M I/O Buffer Models*, IBIS Format (Contact your Intel Field Sales Representative)
- *Intel® 830 Chipset Family: 82830 Graphics and Memory Controller Hub (GMCH-M) Datasheet* (Order Number 298338-003)
- *Intel® 830 Chipset Family: Intel® 830 Chipset Platform Design Guide* (Order Number 298339-003)
- *Intel® 830 Chipset Family: Intel® 82801CAM I/O Controller Hub 3 (ICH3-M) Datasheet* (Order Number 290716-001)
- *Intel® Mobile Voltage Positioning -II (IMVP-II) Design Guide* (Contact your Intel Field Sales Representative)
- *Mobile Intel® Pentium® III Processor-M /440MX Platform Design Guide* (Contact your Intel Field Sales Representative)
- *Intel Processor Identification and the CPUID Instruction Application Note AP-485* (Order Number 241618-020)

2. Mobile Intel Celeron Processor Features

2.1 New Features in the Mobile Intel Celeron Processor

2.1.1 133-MHz PSB With AGTL Signaling

The Mobile Intel Celeron Processor uses Assisted GTL (AGTL) signaling on the PSB interface. The main difference between AGTL and GTL+ used on previous Intel processors is $V_{CCT} = 1.25$ V for AGTL versus 1.5 V for GTL+. The lower voltage swing enables high performance at lower power. The Low Voltage and Ultra Low Voltage Mobile Celeron Processors will also support a 100-MHz PSB.

2.1.2 256-K On-die Integrated L2 Cache

The 256-K on die integrated L2 cache on the Mobile Intel Celeron Processor is double the L2 cache size on the Mobile Intel Celeron Processor (0.18 μ). The L2 cache runs at the processor core speed and the increased cache size provides superior processing power.

2.1.3 Data Prefetch Logic

The Mobile Intel Celeron Processor features Data Prefetch Logic that speculatively fetches data to the L2 cache before an L1 cache request occurs. This reduces transactions between the cache and system memory reducing or eliminating bus cycle penalties, resulting in improved performance. The processor also includes extensions to memory order and reorder buffers that boost performance.

2.1.4 Differential Clocking

Differential clocking requires the use of two complementary clocks: BCLK and BCLK#. Benefits of differential clocking include easier scaling to lower voltages, reduced EMI, and less jitter. All references to BCLK in this document apply to BCLK# also even if not explicitly stated. The Mobile Intel Celeron Processor will also support Single Ended Clocking. The processor will configure itself for Differential or Single Ended Clocking based on the waveforms detected on the BCLK and BCLK#/CLKREF signal lines.

2.1.5 Signal Differences Between the Mobile Intel Celeron Processor (0.18 μ) (in BGA2 and Micro-PGA2 Packages) and the Mobile Intel Celeron Processor (0.13 μ) (in Micro-FCBGA and Micro-FCPGA Packages)

A list of new and changed signals is shown in Table 1.

Table 1. New and Revised Mobile Intel Celeron Processor (0.13 μ) Signals

Signals	Function
BCLK, BCLK#	Differential host clk signals.
CLKREF	Host Clock reference signal in Single Ended Clocking mode.
BSEL[1:0]	Signals are output only instead of I/O. Please refer to the Appendix for details.
DPSLP#	Deep Sleep pin (replaces SLP# pin on the mobile Celeron processor (0.18 μ))
NCTRL	AGTL output buffer pull down impedance control.
VID[4:0]	Voltage Identification (different implementation from mobile Celeron processor (0.18 μ)). Please refer to Section 3.2.3 for details.
VTPWRGD	Power Good signal for VCCT, which indicates that, the VID signals are stable. Please refer to Figure 3 for VTPWRGD system level connections.

2.2 Power Management

2.2.1 Clock Control Architecture

The Mobile Intel Celeron Processor clock control architecture (Figure 1) has been optimized for leading edge mobile computer designs. The clock control architecture consists of six different clock states: Normal, Auto Halt, Quick Start, HALT/Grant Snoop and Deep Sleep states. The Auto Halt state provides a low-power clock state that can be controlled through the software execution of the HLT instruction. The Quick Start state provides a very low power and low exit latency clock state that can be used for hardware controlled “idle” computer states. The Deep Sleep state provides extremely low-power states that can be used for “Power-On-Suspend” computer states, which is an alternative to shutting off the processor’s power. The exit latency of the Deep Sleep state is 30 msec in the Mobile Intel Celeron Processor. Performing state transitions not shown in Figure 1 is neither recommended nor supported. Figure 2 provides the clock state characteristics, which are described in detail in the following sections.

2.2.2 Normal State

The Normal state of the processor is the normal operating mode where the processor’s core clock is running and the processor is actively executing instructions.

2.2.3 Auto Halt State

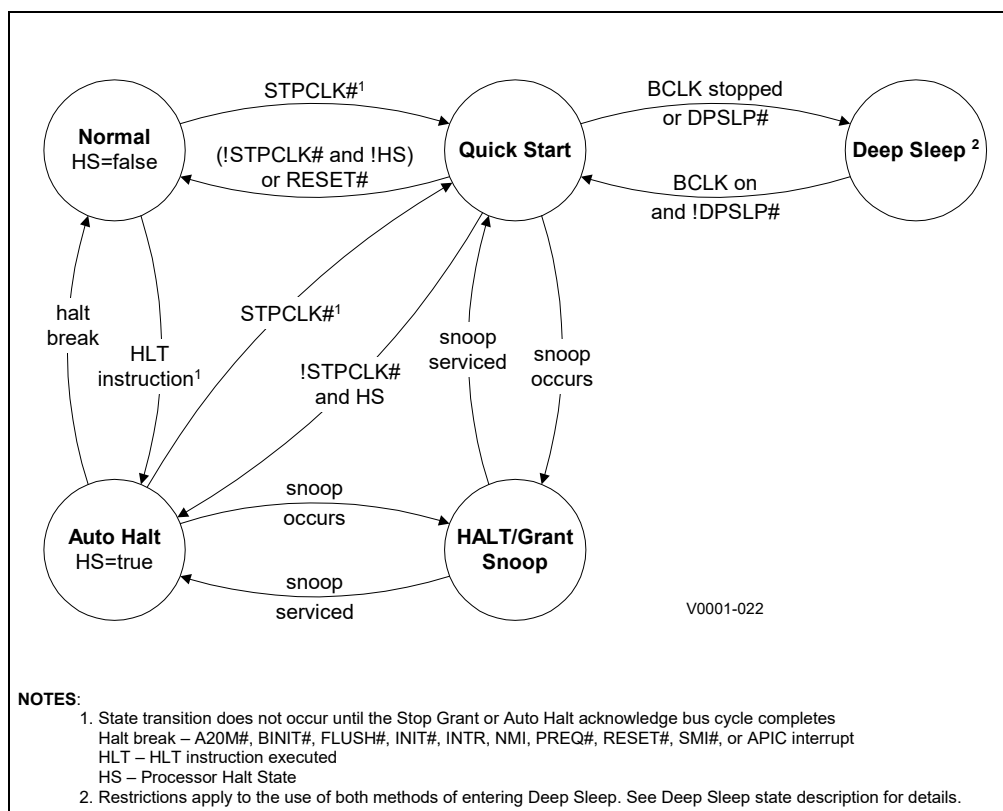
This is a low-power mode entered by the processor through the execution of the HLT instruction. A transition to the Normal state is made by a halt break event (one of the following signals going active: NMI, INTR, INIT#, INIT#, RESET#, FLUSH#, or SMI#).

Asserting the STPCLK# signal while in the Auto Halt state will cause the processor to transition to the Quick Start state. Deasserting STPCLK# will cause the processor to return to the Auto Halt state without issuing a new Halt bus cycle.

The SMI# interrupt is recognized in the Auto Halt state. The return from the System Management Interrupt (SMI) handler can be to either the Normal state or the Auto Halt state. See the *Intel® Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information. No Halt bus cycle is issued when returning to the Auto Halt state from the System Management Mode (SMM).

The FLUSH# signal is serviced in the Auto Halt state. After the on-chip and off-chip caches have been flushed, the processor will return to the Auto Halt state without issuing a Halt bus cycle. Transitions in the A20M# and PREQ# signals are recognized while in the Auto Halt state.

Figure 1. Clock Control States



2.2.4 Quick Start State

The processor is required to be configured for the Quick Start state by strapping the A15# signal low. In the Quick Start state the processor is only capable of acting on snoop transactions generated by the system bus priority device. Because of its snooping behavior, Quick Start can only be used in a uniprocessor (UP) configuration.

A transition to the Deep Sleep state can be made by stopping the clock input to the processor or asserting the DPSLP# signal. A transition back to the Normal state (from the Quick Start state) is made only if the STPCLK# signal is deasserted.

While in this state the processor is limited in its ability to respond to input. It is incapable of latching any interrupts, servicing snoop transactions from symmetric bus masters, or responding to FLUSH# or BINIT# assertions. While the processor is in the Quick Start state, it will not respond properly to any input signal other than STPCLK#, RESET#, or BPRI#. If any other input signal changes, then the behavior of the processor will be unpredictable. No serial interrupt messages may begin or be in progress while the processor is in the Quick Start state.

RESET# assertion will cause the processor to immediately initialize itself, but the processor will stay in the Quick Start state after initialization until STPCLK# is deasserted.

2.2.5 HALT/Grant Snoop State

The processor will respond to snoop transactions on the system bus while in the Auto Halt or Quick Start state. When a snoop transaction is presented on the system bus the processor will enter the HALT/Grant Snoop state. The processor will remain in this state until the snoop has been serviced and the system bus is quiet. After the snoop has been serviced, the processor will return to its previous state. If the HALT/Grant Snoop state is entered from the Quick Start state, then the input signal restrictions of the Quick Start state still apply in the HALT/Grant Snoop state, except for those signal transitions that are required to perform the snoop.

2.2.6 Deep Sleep State

The Deep Sleep state is a very low power state that the processor can enter while maintaining its context. The Deep Sleep state is entered by stopping the BCLK and BCLK# inputs to the processor or by asserting the DPSLP# signal, while it is in the Quick Start state. Note that either one of the methods can be used to enter Deep Sleep but **not both** at the same time. When BCLK and BCLK# are stopped, they must obey the DC levels specified in Table 38 and Table 39.

The processor will return to the Quick Start state from the Deep Sleep state when the BCLK and BCLK# inputs are restarted or the DPSLP# signal is deasserted. Due to the PLL lock latency, there is a delay of up to 30 μ sec after the clocks have started before this state transition happens. PICCLK may be removed in the Deep Sleep state. PICCLK should be designed to turn on when BCLK and BCLK# turn on or DPSLP# is deasserted when transitioning out of the Deep Sleep state.

Table 2. Clock State Characteristics

Clock State	Exit Latency	Snooping?	System Uses
Normal	N/A	Yes	Normal program execution
Auto Halt	10 μ sec	Yes	S/W controlled entry idle mode
Quick Start	Through snoop, to HALT/Grant Snoop state: immediate Through STPCLK#, to Normal state: 10 μ sec	Yes	H/W controlled entry/exit mobile throttling
HALT/Grant Snoop	A few bus clocks after snoop completion	Yes	Supports snooping in the low power states
Deep Sleep	30 μ sec	No	H/W controlled entry/exit mobile powered-on suspend support

2.2.7 Operating System Implications of Low-power States

The time-stamp counter and the performance monitor counters are not guaranteed to count in the Quick Start state. The local APIC timer and performance monitor counter interrupts should be disabled before entering the Deep Sleep state or the resulting behavior will be unpredictable.

2.3 AGTL Signals

The Mobile Intel Celeron Processor system bus signals use a variation of the low-voltage swing GTL signaling technology. The AGTL system bus depends on incident wave switching and uses flight time for timing calculations of the AGTL signals, as opposed to capacitive derating. Intel recommends analog signal simulation of the system bus including trace lengths. Contact your field sales representative to receive the IBIS models for the Mobile Intel Celeron Processor.

The AGTL system bus of the Mobile Intel Celeron Processor is designed to support high-speed data transfers with multiple loads on a long bus that behaves like a transmission line. However, in mobile systems the system bus only has two loads (the processor and the chipset) and the bus traces are short. It is possible to change the layout and termination of the system bus to take advantage of the mobile environment using the same AGTL I/O buffers. This termination is provided on the processor core (except for the RESET# signal).

2.4 Mobile Intel Celeron Processor CPUID

When the CPUID version information is loaded with EAX=01H, the EAX and EBX registers contain the values shown in Table 3. After a power-on RESET, the EDX register contains the processor version information (type, family, model, stepping). Table 4 shows the CPUID Cache and TLB descriptor values after the L2 cache is initialized. See the *Intel Processor Identification* and the *CPUID Instruction Application Note AP-485* for further information.



Table 3. Mobile Intel Celeron Processor CPUID

EAX[31:0]					EBX[7:0]
Reserved [31:14]	Type [13:12]	Family [11:8]	Model [7:4]	Stepping [3:0]	Brand ID
X	0	6	B	X	07

Table 4. Mobile Intel Celeron Processor CPUID Cache and TLB Descriptors

Cache and TLB Descriptors	01H, 02H, 03H, 04H, 08H, 0CH, 83H
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3. Electrical Specifications

3.1 Processor System Signals

Table 5 lists the processor system signals by type. All AGTL signals are synchronous with the BCLK and BCLK# signals. All TAP signals are synchronous with the TCK signal except TRST#. All CMOS input signals can be applied asynchronously.

Table 5. System Signal Groups

Group Name	Signals
AGTL Input	BPRI#, DEFER#, RESET#, RSP#
AGTL Output	PRDY#
AGTL I/O	A[35:3]#, ADS#, AERR#, AP[1:0]#, BERR#, BINIT#, BNR#, BP[3:2]#, BPM[1:0]#, BREQ0#, D[63:0]#, DBSY#, DEP[7:0]#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#, RP#, RS[2:0]#, TRDY#
1.5 V CMOS Input	A20M#, DPSLP#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, SMI#, STPCLK#
1.8 V CMOS Input	PWRGOOD
1.5 V Open Drain Output	FERR#, IERR#
3.3 V Open Drain Output	BSEL[1:0], VID[4:0]
1.25 V input	VTPWRGD
Clock	BCLK, BCLK# (Differential Mode)
2.5 V Clock Input	BCLK (Single Ended Mode)
APIC Clock	PICCLK
APIC I/O	PICD[1:0]
Thermal Diode	THERMDC, THERMDA
TAP Input	TCK, TDI, TMS, TRST#
TAP Output	TDO
Power/Other	CLKREF, CMOSREF, EDGECTRLP, NC, NCTRL, PLL1, PLL2, RTTIMPEDP, V _{CC} , V _{CCT} , V _{REF} , V _{SS}

NOTES:

1. VCC is the power supply for the core logic.
2. PLL1 and PLL2 are power/ground for the PLL analog section. See Section 3.2.2 for details.
3. VCCT is the power supply for the system bus buffers.
4. VREF is the voltage reference for the AGTL input buffers.
5. VSS is system ground.

The APIC data and TAP outputs are Open-drain and should be pulled up to 1.5 V using resistors with the values shown in Table 6. If Open-drain drivers are used for input signals, then they should also be pulled up to the appropriate voltage using resistors with the values shown in Table 6.

Table 6. Recommended Resistors for Mobile Intel Celeron Processor Signals

Recommended Resistor Value (Ω)	Mobile Intel Celeron Processor Signal ^{1,2}
10 pull-down	BREQ0# ³
14 pull-up	NCTRL
39 pull-up	TMS
39 pull-down	TCK
56.2 pull-up	PRDY#, RESET# ⁴
56.2 pull-down	RTTIMPEDP
110 pull-down	EDGECTRLP
150 pull-up	PICD[1:0], TDO
200-300 pull-up	PREQ#, TDI
500 pull-down	TRST#
1K pull-up	BSEL[1:0], TESTHI, VID[4:0], VTPWGRGD
1K pull-down	TESTLO
1.5k pull-up	FERR#, IERR#, PWRGOOD
3K pull-up	FLUSH#
Additional Pullup/Pulldown Resistor Recommendations⁶	
270 pull-up	SMI#
680 pull-up	STPCLK#
1.5k pull-up	A20M#, DPSLP#, INIT#, IGNNE#, LINT0/INTR, LINT1/NMI

NOTES:

1. The recommendations above are only for signals that are being used. These recommendations are maximum values only; stronger pull-ups may be used. Pull-ups for the signals driven by the chipset should not violate the chipset specification. Refer to Section 3.1.4 for the required pull-up or pull-down resistors for signals that are not being used.
2. Open-drain signals must never violate the undershoot specification in Section 4.3. Use stronger pull-ups if there is too much undershoot.
3. A pull-down on BREQ0# is an alternative to having the central agent to drive BREQ0# low at reset.
4. A 56.2 Ω 1% terminating resistor connected to V_{CCT} is required.
5. The following signals are actively driven high by the ICH3-M component and do not need external pull up resistors on ICH3-M based platforms: A20M#, DPSLP#, INIT#, IGNNE#, LINT0/INTR, LINT1/NMI, SMI#, STPCLK#.
6. These pull up recommendations apply to systems on which these signals are not actively pulled high such as those utilizing the 82443MX chipset.

3.1.1 Power Sequencing Requirements

Unlike the Mobile Intel Celeron Processor (0.18 μ), the Mobile Intel Celeron Processor (0.13 μ) does have specific power sequencing requirements. The power on sequencing and timings are shown in Figure 15 and Table 31. Power down timing requirements are shown in Figure 16, Figure 17, and Table 31. The V_{CC} power plane must not rise too fast. At least 200 μ sec (T_R) must pass from the time that V_{CC} is at 10% of its nominal value until the time that V_{CC} is at 90% of its nominal value. For more details, please refer to the *Intel® Mobile Voltage Positioning -II (IMVP-II) Design Guide* (contact your Field Sales Representative).

3.1.2 Test Access Port (TAP) Connection

The TAP interface is an implementation of the IEEE 1149.1 (“JTAG”) standard. Due to the voltage levels supported by the TAP interface, Intel recommends that the Mobile Intel Celeron Processor and the

other 1.5-V JTAG specification compliant devices be last in the JTAG chain after any devices with 3.3-V or 5.0-V JTAG interfaces within the system. A translation buffer should be used to reduce the TDO output voltage of the last 3.3/5.0 V device down to the 1.5-V range that the Mobile Intel Celeron Processor can tolerate. Multiple copies of TMS and TRST# must be provided, one for each voltage level.

A Debug Port and connector may be placed at the start and end of the JTAG chain containing the processor, with TDI to the first component coming from the Debug Port and TDO from the last component going to the Debug Port. There are no requirements for placing the Mobile Intel Celeron Processor in the JTAG chain, except for those that are dictated by voltage requirements of the TAP signals.

3.1.3 Catastrophic Thermal Protection

The Mobile Intel Celeron Processor does not support catastrophic thermal protection or the THERMTRIP# signal. An external thermal sensor must be used to protect the processor and the system against excessive temperatures. If the external thermal sensor detects a processor junction temperature of 101 °C (maximum), both the V_{CC} and V_{CCT} supplies to the processor must be reduced to at least 50% of the nominal values within 500 ms and are recommended to be turned off completely within 1 second to prevent damage to the processor. Processor temperature must be monitored in all states including low power states.

3.1.4 Unused Signals

All signals named NC must be unconnected. Unused AGTL inputs, outputs, and bi-directional signals should be unconnected. Unused CMOS active low inputs should be connected to 1.5 V and unused active high inputs should be connected to V_{SS} . Unused Open-drain outputs should be unconnected. When tying any signal to power or ground, a resistor will allow for system testability. For unused signals, Intel suggests that 1.5-k Ω resistors are used for pull-ups and 1.0-k Ω resistors are used for pull-downs.

PICCLK must be driven with a clock that meets specification and the PICD[1:0] signals must be pulled up **separately** to 1.5 V with 150- Ω resistors, even if the local APIC is not used.

If the TAP signals are not used then the inputs should be pulled to ground with 1-k Ω resistors and TDO should be left unconnected.

3.1.5 Signal State in Low-power States

3.1.5.1 System Bus Signals

All of the system bus signals have AGTL input, output, or input/output drivers. Except when servicing snoops, the system bus signals are tri-stated and pulled up by the termination resistors. Snoops are not permitted in the Deep Sleep state.

3.1.5.2 CMOS and Open-drain Signals

The CMOS input signals are allowed to be in either the logic high or low state when the processor is in a low-power state. In the Auto Halt state these signals are allowed to toggle. These input buffers have no internal pull-up or pull-down resistors and system logic can use CMOS or Open-drain drivers to drive them.

The Open-drain output signals have open drain drivers and external pull-up resistors are required. One of the two output signals (IERR#) is a catastrophic error indicator and is tri-stated (and pulled-up) when the processor is functioning normally. The FERR# output can be either tri-stated or driven to V_{SS} when the processor is in a low-power state depending on the condition of the floating-point unit. Since this signal is a DC current path when it is driven to V_{SS} , Intel recommends that the software clears or masks any floating-point error condition before putting the processor into the Deep Sleep state.

3.1.5.3 Other Signals

The system bus clocks (BCLK, BCLK#) must be driven in all of the low-power states except the Deep Sleep state. The APIC clock (PICCLK) must be driven whenever BCLK and BCLK# are driven. Otherwise, it is permitted to turn off PICCLK by holding it at V_{SS} . BCLK and BCLK# should be obey the DC levels in Table 38 (for Differential Clocking) and Table 39 (for Single Ended Clocking).

In the Auto Halt state, the APIC bus data signals (PICD[1:0]) may toggle due to APIC bus messages. These signals are required to be tri-stated and pulled-up when the processor is in the Quick Start or Deep Sleep states.

3.2 Power Supply Requirements

3.2.1 Decoupling Guidelines

The Mobile Intel Celeron Processor in Micro-FCPGA package has twelve 0805IDC, 1- μ F surface mount decoupling capacitors. Eight capacitors are on the V_{CC} supply and four capacitors are on V_{CCT} . For the Micro-FCBGA package, there are six 0.68- μ F capacitors on V_{CC} and two 0.68- μ F capacitors on V_{CCT} . In addition to the package capacitors, sufficient board level capacitors are also necessary for power supply decoupling. The guidelines are as follows:

- High and Mid Frequency V_{CC} decoupling – Place twenty-four 0.22- μ F 0603 capacitors directly under the package on the solder side of the motherboard using at least two vias per capacitor node. Ten 10- μ F X7 6.3V 1206-size ceramic capacitors should be placed around the package periphery near the balls. Trace lengths to the vias should be designed to minimize inductance. Avoid bending traces to minimize ESL.
- High and Mid Frequency V_{CCT} decoupling – Place ten 1- μ F X7R 0603 ceramic capacitors close to the package. Via and trace guidelines are the same as above.
- Bulk V_{CC} decoupling – Minimum of 1200- μ F capacitance with Equivalent Series Resistance (ESR) less than or equal to 3.5 m Ω .
- Bulk V_{CCT} decoupling – Platform dependent but recommendation is minimum of 660 μ F with ESR less than or equal to 7 m Ω .

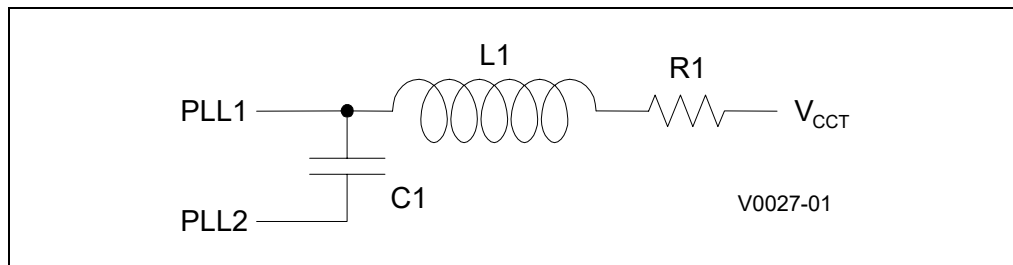
Please refer to the appropriate platform design guidelines for bulk decoupling recommendations.

3.2.2 Voltage Planes

All V_{CC} and V_{SS} pins/balls must be connected to the appropriate voltage plane. All V_{CCT} and V_{REF} pins/balls must be connected to the appropriate traces on the system electronics. In addition to the main V_{CC} , V_{CCT} , and V_{SS} power supply signals, PLL1 and PLL2 provide analog decoupling to the PLL

section. PLL1 and PLL2 should be connected according to Figure 2. Do not connect PLL2 directly to V_{SS} . Appendix A contains the RLC filter specification.

Figure 2. PLL RLC Filter



3.2.3 Voltage Identification

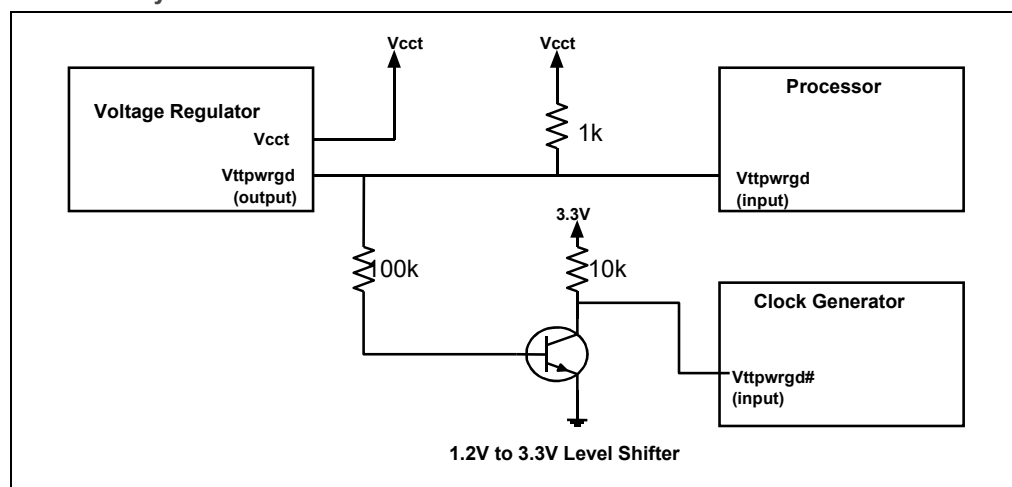
There are five voltage identification balls/pins on the Mobile Intel Celeron Processor. These signals can be used to support automatic selection of V_{CC} voltages. They are needed to cleanly support voltage specification variations on current and future processors. VID[4:0] are defined in Table 7. The voltages specified in the VID table are the Battery Optimized Mode V_{CC} voltages. The VID[4:0] signals are open drain on the processor and need pull-up resistors to 3.3 V on the motherboard. Please refer to the mobile VR guidelines provided by Intel for additional information.

Table 7. Mobile Intel Celeron Processor VID Values

VID[4:0]	V_{CC} (V)	VID[4:0]	V_{CC} (V)	VID[4:0]	V_{CC} (V)	VID[4:0]	V_{CC} (V)
00000	1.750	01000	1.350	10000	0.975	11000	0.775
00001	1.700	01001	1.300	10001	0.950	11001	0.750
00010	1.650	01010	1.250	10010	0.925	11010	0.725
00011	1.600	01011	1.200	10011	0.900	11011	0.700
00100	1.550	01100	1.150	10100	0.875	11100	0.675
00101	1.500	01101	1.100	10101	0.850	11101	0.650
00110	1.450	01110	1.050	10110	0.825	11110	0.625
00111	1.400	01111	1.000	10111	0.800	11111	0.600

Figure 3 shows the system level connections for the VTTPWRGD signal. Please refer to the appropriate VR and system level guidelines provided by Intel for more details.

Figure 3. VTTWRGD System-Level Connections



3.2.4 VTTWRGD Signal Quality Specification

The VTTWRGD signal is an input to the processor used to determine that the VTT power is stable and the VID and BSEL signals should be driven to their final state by the processor. To ensure the processor correctly reads this signal, it must meet the following requirement while the signal is in its transition region of 300 mV to 900 mV. Also, VTTWRGD should only enter the transition region once, after VTT is at nominal values, for the assertion of the signal.

Table 8. VTTWRGD Noise Specification

Parameter	Specification
Amount of noise (glitch)	Less than 100 mV

In addition, the VTTWRGD signal should have reasonable transition time through the transition region. A sharp edge on the signal transition will minimize the chance of noise causing a glitch on this signal. Intel recommends the following transition time for the VTTWRGD signal.

Table 9. VTTWRGD Transition Time Specification

Parameter	Recommendation
Transition time (300 mV to 900 mV)	Less than or equal to 100 μ s

3.2.4.1 Transition Region

The transition region covered by this requirement is 300 mV to 900 mV. Once the VTTWRGD signal is in that voltage range, the processor is more sensitive to noise, which may be present on the signal. The transition region when the signal first crosses the 300 mV voltage level and continues until the last time it is below 900 mV.

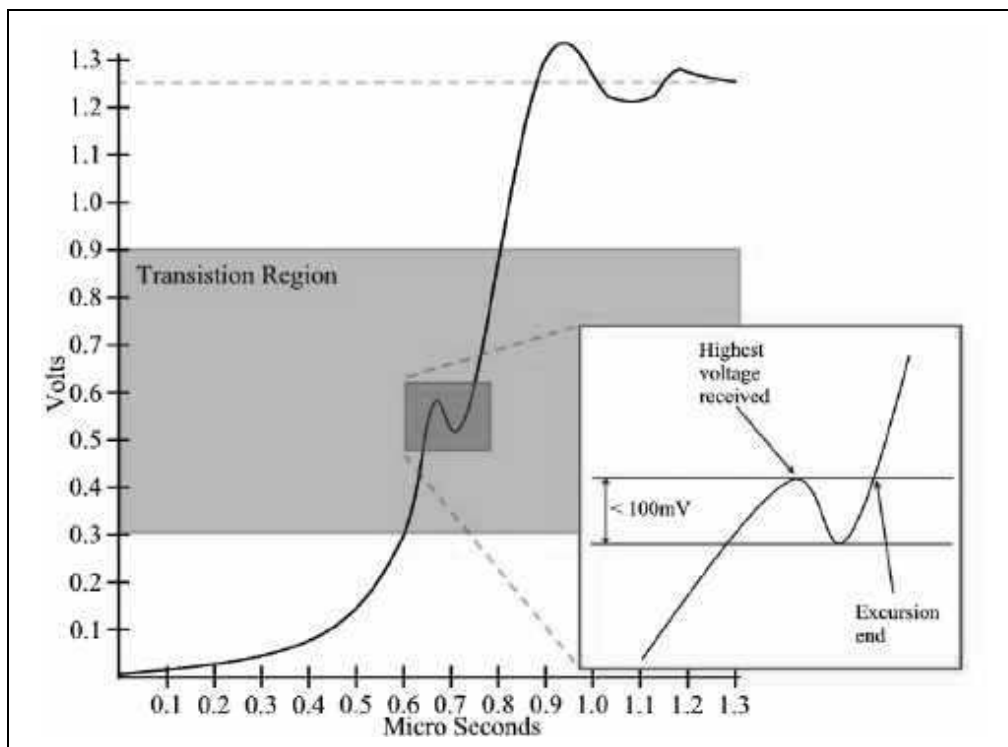
3.2.4.2 Transition Time

The transition time is defined as the time the signal takes to move through the transition region. A 100- μ s transition time will ensure that the processor receives a good transition edge.

3.2.4.3 Noise

The signal quality of the VTPWRGD signal is critical to the correct operation of the processor. Every effort should be made to ensure this signal is monotonic in the transition region. If noise or glitches are present on this signal, it must be kept to less than 100 mV of a voltage drop from the highest voltage level received to that point. This glitch must remain less than 100 mV until the excursion ends by the voltage returning to the highest voltage previously received. Please see Figure 4 for an example graph of this situation and requirements.

Figure 4. Noise Estimation



3.3 System Bus Clock and Processor Clocking

The BCLK and BCLK# clock inputs directly control the operating speed of the system bus interface. All system bus timing parameters are specified with respect to the crossing point of the rising edge of the BCLK input and falling edge of the BCLK# input. The Mobile Intel Celeron Processor core frequency is a multiple of the BCLK frequency. The processor core frequency is configured during manufacturing. The configured bus ratio is visible to software in the Power-on configuration register. See Section 7.2 for details.

Multiplying the bus clock frequency is necessary to increase performance while allowing for easier distribution of signals within the system. Clock multiplication within the processor is provided by the internal Phase Lock Loop (PLL), which requires constant frequency BCLK and BCLK# inputs. During Reset or on exit from the Deep Sleep state, the PLL requires some amount of time to acquire the phase of BCLK and BCLK#. This time is called the PLL lock latency, which is specified in Section 3.6, AC timing parameters T18 and T47.

3.4 Maximum Ratings

Table 10 contains the Mobile Intel Celeron Processor stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating conditions are provided in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 10. Mobile Intel Celeron Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T _{Storage}	Storage Temperature	-40	85	°C	Note 1
V _{CC(Abs)}	Supply Voltage with respect to V _{SS}	-0.5	1.75	V	
V _{CCT}	System Bus Buffer Voltage with respect to V _{SS}	-0.3	1.75	V	
V _{IN GTL}	System Bus Buffer DC Input Voltage with respect to V _{SS}	-0.3	1.75	V	Notes 2, 3
V _{IN125}	1.25 V Buffer DC Input Voltage with respect to V _{SS}	-0.3	1.75	V	Note 4
V _{IN15}	1.5 V Buffer DC Input Voltage with respect to V _{SS}	-0.3	2.0	V	Note 5
V _{IN18}	1.8 V Buffer DC Input Voltage with respect to V _{SS}	-0.3	2.0	V	Note 6
V _{IN20}	2.0 V Buffer DC Input Voltage with respect to V _{SS}	-0.3	2.4	V	Note 7
V _{IN25}	2.5 V Buffer DC Input Voltage with respect to V _{SS}	-0.3	3.3	V	Note 9
V _{INVID}	VID ball/pin DC Input Voltage with respect to V _{SS}	—	3.465	V	Note 8
I _{VID}	VID Current	-0.3	3.6	mA	Note 8

NOTES:

1. The shipping container is only rated for 65°C.
2. Parameter applies to the AGTL signal groups only. Compliance with both V_{IN GTL} specifications is required.
3. The voltage on the AGTL signals must never be below -0.3 V or above 1.75 V with respect to ground.
4. Parameter applies to CLKREF, TESTHI, VTTTPWRGD signals.
5. Parameter applies to CMOS, Open-drain, APIC, TESTLO and TAP bus signal groups only.
6. Parameter applies to PWRGOOD signal.
7. Parameter applies to PICCLK signal.
8. Parameter applies to each VID pin/ball individually.
9. Parameter applies to BCLK signal in Single Ended Clocking Mode.

3.5 DC Specifications

Table 11 through Table 24 list the DC specifications for the Mobile Intel Celeron Processor. Specifications are valid only while meeting specifications for the junction temperature, clock frequency, and input voltages. The junction temperature range for all DC specifications is 0°C to 100°C unless otherwise noted. Care should be taken to read all notes associated with each parameter. Unlike the Mobile Intel Pentium III Processor, the V_{CC} tolerances for the Mobile Intel Celeron Processor are not specified as a percentage of nominal. The tolerances are instead specified in the form of load lines for the static and transient cases in Table 12 through Table 21. Illustration of the load lines is shown in Figure 5 through Figure 8.

Table 11. Power Specifications for Mobile Intel Celeron Processor¹

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CC}	Transient V_{CC} for core logic		1.10 1.15 1.40 1.45 1.50		V V V V V	Note 11 Notes 9, 10 Notes 9, 10 Notes 9, 10 Notes 9, 10
$V_{CC,DC}$	Static V_{CC} for core logic		1.10 1.15 1.40 1.45 1.50		V V V V V	Note 11 Notes 9, 10 Notes 9, 10 Notes 9, 10 Notes 9, 10
V_{CCT}	V_{CC} for System Bus Buffers, Transient tolerance	1.138	1.25	1.362	V	± 9%, Notes 7,10
$V_{CCT,DC}$	V_{CC} for System Bus Buffers, Static tolerance	1.188	1.25	1.312	V	±5%, Notes 2,10
I_{CC}	Current for V_{CC} at core frequency 800 MHz & 1.10V 733 MHz & 1.10 V 700 MHz & 1.10 V 650 MHz & 1.10 V 650 MHz & 1.15 V 667 MHz & 1.15 V 733 MHz & 1.15 V 866 MHz & 1.15 V 1.00 GHz & 1.40 V 1.26 GHz & 1.40V 1.06 GHz & 1.45 V 1.13 GHz & 1.45 V 1.20 GHz & 1.45 V 1.33 GHz & 1.50 V			7.58 7.98 7.89 7.58 10.52 10.68 11.27 10.03 18.27 18.75 18.67 19.14 19.63 15.90	A	Notes 4, 11 Notes 4, 11 Notes 4, 11 Notes 4, 11 Note 4 Note 4 Note 4 Note 4
I_{CCT}	Current for V_{CCT}			2.7	A	Notes 3, 4
$I_{CC,AH}$	Processor Auto Halt current at 1.10 V 1.15 V 1.40 V 1.45 V 1.50 V			3.09 5.42 8.85 10.20 10.73	A	Note 4 Notes 4, 11
$I_{CC,QS}$	Processor Quick Start current at 1.10 V 1.15 V 1.40 V 1.45 V 1.50 V			2.91 5.16 8.53 9.80 9.90	A	Note 4 Notes 4, 11
$I_{CC,DSLP}$	Processor Deep Sleep Leakage current at 1.10 V 1.15 V 1.40 V 1.45 V 1.50 V			2.65 4.79 8.04 9.20 9.20	A	Note 4 Notes 4, 11
I_{LVID}	VID leakage current			0.5	mA	Note 8
dl_{CC}/dt	V_{CC} power supply current slew rate			400	A/ μ s	Notes 5, 6

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. Processors will comply with the $I_{CCX,max}$ specification for the current mode of operation.
2. Static voltage regulation includes: DC output initial voltage set point adjust, output ripple and noise, temperature and warm up.
3. I_{CCT} is the current supply for the system bus buffers, including the on-die termination.

4. $I_{CCx,max}$ specifications are specified at V_{CC} static (typical) derived from the tolerances in Table 12 through Table 19, $V_{CCT,max}$, T_{jmax} , and under maximum signal loading conditions.
5. Based on simulations and averaged over the duration of any change in current. Use to compute the maximum inductance and reaction time of the voltage regulator. This parameter is not tested.
6. Maximum values specified by design/characterization at nominal V_{CC} and V_{CCT} .
7. V_{CCx} must be within this range under all operating conditions, including maximum current transients. V_{CCx} must return to within the static voltage specification, $V_{CCx,DC}$, within 100 μ s after a transient event.
8. VID leakage current is < 100 μ A for VID voltages under 3.0 V.
9. Typical V_{CC} indicates the VID encoded voltage. Voltage supplied must conform to the load line specification shown in Table 12 through Table 19.
10. Voltages are measured at the processor socket pin for the Micro-FCPGA part and at the package ball on the Micro-FCBGA part.
11. This specification applies only to the Ultra Low Voltage Mobile Intel Celeron Processor.

Table 12. V_{CC} Tolerances for the Low Voltage Mobile Intel Celeron Processor: VID = 1.15 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.150	1.125	1.175	1.105	1.195
1.0	1.146	1.121	1.171	1.101	1.191
2.0	1.142	1.117	1.167	1.097	1.187
3.0	1.138	1.113	1.163	1.093	1.183
4.0	1.134	1.109	1.159	1.089	1.179
5.0	1.130	1.105	1.155	1.085	1.175
6.0	1.126	1.101	1.151	1.081	1.171
7.0	1.122	1.097	1.147	1.077	1.167
8.0	1.118	1.093	1.143	1.073	1.163
9.0	1.114	1.089	1.139	1.069	1.159
10.0	1.110	1.085	1.135	1.065	1.155
11.0	1.106	1.081	1.131	1.061	1.151
12.0	1.102	1.077	1.127	1.057	1.147
13.0	1.098	1.073	1.123	1.053	1.143
14.0	1.094	1.069	1.119	1.049	1.139
15.0	1.090	1.065	1.115	1.045	1.135

Table 13. V_{CC} Tolerances for the Low Voltage Mobile Intel Celeron Processor in the Deep Sleep State: VID = 1.15 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.114	1.089	1.139	1.069	1.159
1.0	1.110	1.085	1.135	1.065	1.155
2.0	1.106	1.081	1.131	1.061	1.151
3.0	1.102	1.077	1.127	1.057	1.147
4.0	1.098	1.073	1.123	1.053	1.143
5.0	1.094	1.069	1.119	1.049	1.139
6.0	1.090	1.065	1.115	1.045	1.135

Table 14. V_{CC} Tolerances for the Ultra Low Voltage Mobile Intel Celeron Processor: VID = 1.1 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.100	1.075	1.125	1.055	1.145
1.0	1.096	1.071	1.121	1.051	1.141
2.0	1.092	1.067	1.117	1.047	1.137
3.0	1.088	1.063	1.113	1.043	1.133
4.0	1.084	1.059	1.109	1.039	1.129
5.0	1.080	1.055	1.105	1.035	1.125
6.0	1.076	1.051	1.101	1.031	1.121
7.0	1.072	1.047	1.097	1.027	1.117
8.0	1.068	1.043	1.093	1.023	1.113
9.0	1.064	1.039	1.089	1.019	1.109
10.0	1.060	1.035	1.085	1.015	1.105
11.0	1.056	1.031	1.081	1.011	1.101
12.0	1.052	1.027	1.077	1.007	1.097
13.0	1.048	1.023	1.073	1.003	1.093



Table 15. V_{CC} Tolerances for the Ultra Low Voltage Mobile Intel Celeron Processor in the Deep Sleep State: VID = 1.1 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.068	1.043	1.093	1.023	1.113
1.0	1.064	1.039	1.089	1.019	1.109
2.0	1.060	1.035	1.085	1.015	1.105
3.0	1.056	1.031	1.081	1.011	1.101
4.0	1.052	1.027	1.077	1.007	1.097
5.0	1.048	1.023	1.073	1.003	1.093

Table 16. V_{CC} Tolerances for the Mobile Intel Celeron Processor: VID = 1.40 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.400	1.375	1.425	1.355	1.445
1.0	1.396	1.371	1.421	1.351	1.441
2.0	1.392	1.367	1.417	1.347	1.437
3.0	1.388	1.363	1.413	1.343	1.433
4.0	1.384	1.359	1.409	1.339	1.429
5.0	1.380	1.355	1.405	1.335	1.425
6.0	1.376	1.351	1.401	1.331	1.421
7.0	1.372	1.347	1.397	1.327	1.417
8.0	1.368	1.343	1.393	1.323	1.413
9.0	1.364	1.339	1.389	1.319	1.409
10.0	1.360	1.335	1.385	1.315	1.405
11.0	1.356	1.331	1.381	1.311	1.401
12.0	1.352	1.327	1.377	1.307	1.397
13.0	1.348	1.323	1.373	1.303	1.393
14.0	1.344	1.319	1.369	1.299	1.389
15.0	1.340	1.315	1.365	1.295	1.385
16.0	1.336	1.311	1.361	1.291	1.381
17.0	1.332	1.307	1.357	1.287	1.377
18.0	1.328	1.303	1.353	1.283	1.373
19.0	1.324	1.299	1.349	1.279	1.369
20.0	1.320	1.295	1.345	1.275	1.365
21.0	1.316	1.291	1.341	1.271	1.361
22.0	1.312	1.287	1.337	1.267	1.357
23.0	1.308	1.283	1.333	1.263	1.353



Table 17. V_{CC} Tolerances for the Mobile Intel Celeron Processor in the Deep Sleep State: VID = 1.40 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.338	1.313	1.363	1.293	1.383
1.0	1.334	1.309	1.359	1.289	1.379
2.0	1.330	1.305	1.355	1.285	1.375
3.0	1.326	1.301	1.351	1.281	1.371
4.0	1.322	1.297	1.347	1.277	1.367
5.0	1.318	1.293	1.343	1.273	1.363
6.0	1.314	1.289	1.339	1.269	1.359
7.0	1.310	1.285	1.335	1.265	1.355
8.0	1.306	1.281	1.331	1.261	1.351

Table 18. V_{CC} Tolerances for the Mobile Intel Celeron Processor: VID = 1.45 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.450	1.425	1.475	1.405	1.495
1.0	1.446	1.421	1.471	1.401	1.491
2.0	1.442	1.417	1.467	1.397	1.487
3.0	1.438	1.413	1.463	1.393	1.483
4.0	1.434	1.409	1.459	1.389	1.479
5.0	1.430	1.405	1.455	1.385	1.475
6.0	1.426	1.401	1.451	1.381	1.471
7.0	1.422	1.397	1.447	1.377	1.467
8.0	1.418	1.393	1.443	1.373	1.463
9.0	1.414	1.389	1.439	1.369	1.459
10.0	1.410	1.385	1.435	1.365	1.455
11.0	1.406	1.381	1.431	1.361	1.451
12.0	1.402	1.377	1.427	1.357	1.447
13.0	1.398	1.373	1.423	1.353	1.443
14.0	1.394	1.369	1.419	1.349	1.439
15.0	1.390	1.365	1.415	1.345	1.435
16.0	1.386	1.361	1.411	1.341	1.431
17.0	1.382	1.357	1.407	1.337	1.427
18.0	1.378	1.353	1.403	1.333	1.423
19.0	1.374	1.349	1.399	1.329	1.419
20.0	1.370	1.345	1.395	1.325	1.415
21.0	1.366	1.341	1.391	1.321	1.411
22.0	1.362	1.337	1.387	1.317	1.397
23.0	1.358	1.333	1.383	1.313	1.393



Table 19. V_{CC} Tolerances for the Mobile Intel Celeron Processor in the Deep Sleep State: VID = 1.45 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.388	1.363	1.413	1.343	1.433
1.0	1.384	1.359	1.409	1.339	1.429
2.0	1.380	1.355	1.405	1.335	1.425
3.0	1.376	1.351	1.401	1.331	1.421
4.0	1.372	1.347	1.397	1.327	1.417
5.0	1.368	1.343	1.393	1.323	1.413
6.0	1.364	1.339	1.389	1.319	1.409
7.0	1.360	1.335	1.385	1.315	1.405
8.0	1.356	1.331	1.381	1.31	1.401

Table 20. V_{CC} Tolerances for the Mobile Intel Celeron Processor: VID = 1.50 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.50	1.475	1.525	1.455	1.545
1.0	1.496	1.471	1.521	1.451	1.541
2.0	1.492	1.467	1.517	1.447	1.537
3.0	1.488	1.463	1.513	1.443	1.533
4.0	1.484	1.459	1.509	1.439	1.529
5.0	1.480	1.455	1.505	1.435	1.525
6.0	1.476	1.451	1.501	1.431	1.521
7.0	1.472	1.447	1.497	1.427	1.517
8.0	1.468	1.443	1.493	1.423	1.513
9.0	1.464	1.439	1.489	1.419	1.509
10.0	1.460	1.435	1.485	1.415	1.505
11.0	1.456	1.431	1.481	1.411	1.501
12.0	1.452	1.427	1.477	1.407	1.497
13.0	1.448	1.423	1.473	1.403	1.493
14.0	1.444	1.419	1.469	1.399	1.489
15.0	1.440	1.415	1.465	1.395	1.485
16.0	1.436	1.411	1.461	1.391	1.481
17.0	1.432	1.407	1.457	1.387	1.477
18.0	1.428	1.403	1.453	1.383	1.473
19.0	1.424	1.399	1.449	1.379	1.469
20.0	1.420	1.395	1.445	1.375	1.465
21.0	1.416	1.391	1.441	1.371	1.461
22.0	1.412	1.387	1.437	1.367	1.457
23.0	1.408	1.383	1.433	1.363	1.453



Table 21. V_{CC} Tolerances for the Mobile Intel Celeron Processor in the Deep Sleep State: VID = 1.50 V

I_{CC} (A)	V_{CC} (V)				
	Static			Transient	
	Typ	Min	Max	Min	Max
0.0	1.438	1.413	1.463	1.393	1.483
1.0	1.434	1.409	1.459	1.389	1.479
2.0	1.430	1.405	1.455	1.385	1.475
3.0	1.426	1.401	1.451	1.381	1.471
4.0	1.422	1.397	1.447	1.377	1.467
5.0	1.418	1.393	1.443	1.373	1.463
6.0	1.414	1.389	1.439	1.369	1.459
7.0	1.410	1.385	1.435	1.365	1.455
8.0	1.406	1.381	1.431	1.361	1.451

Figure 5. Illustration of V_{CC} Static and Transient Tolerances (VID = 1.15 V)

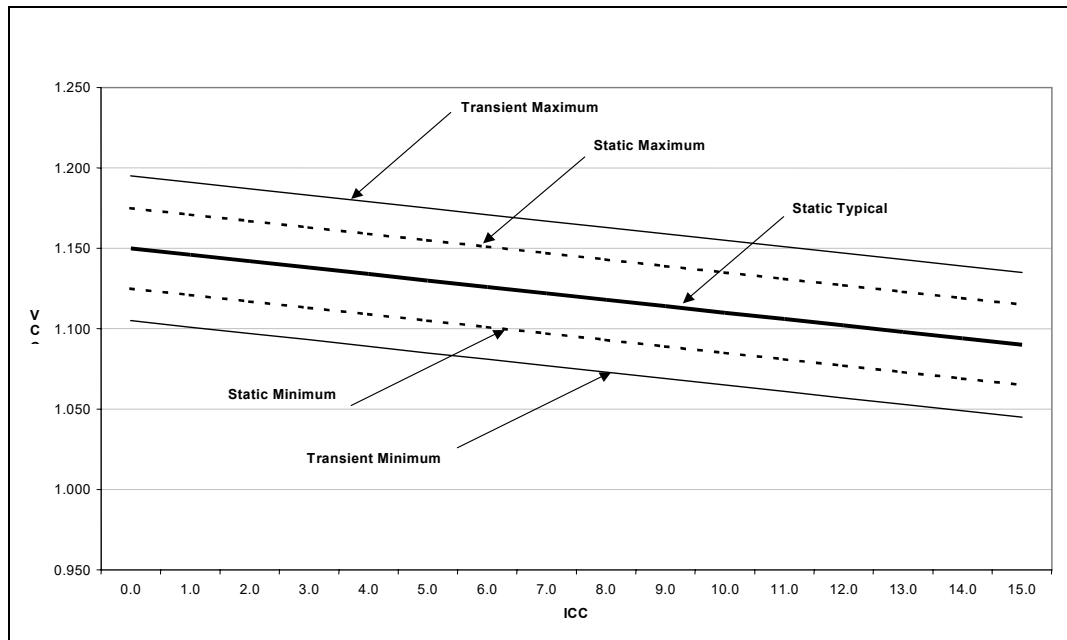


Figure 6. Illustration of Deep Sleep V_{CC} Static and Transient Tolerances (VID Setting = 1.15 V)

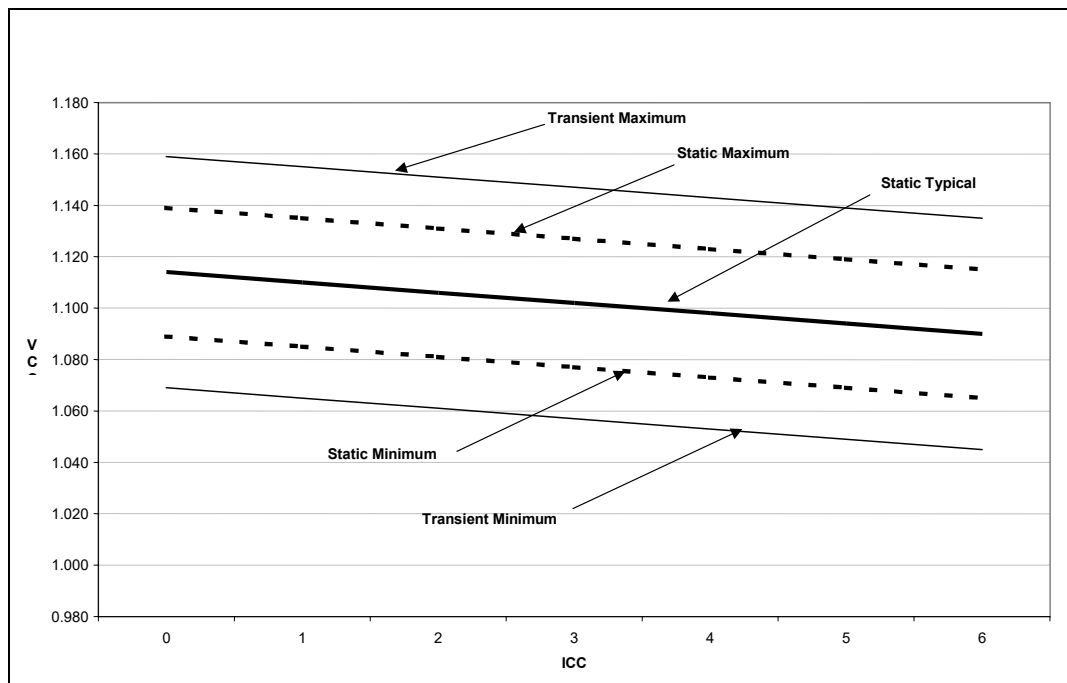




Figure 7. Illustration of V_{CC} Static and Transient Tolerances (VID = 1.40 V)

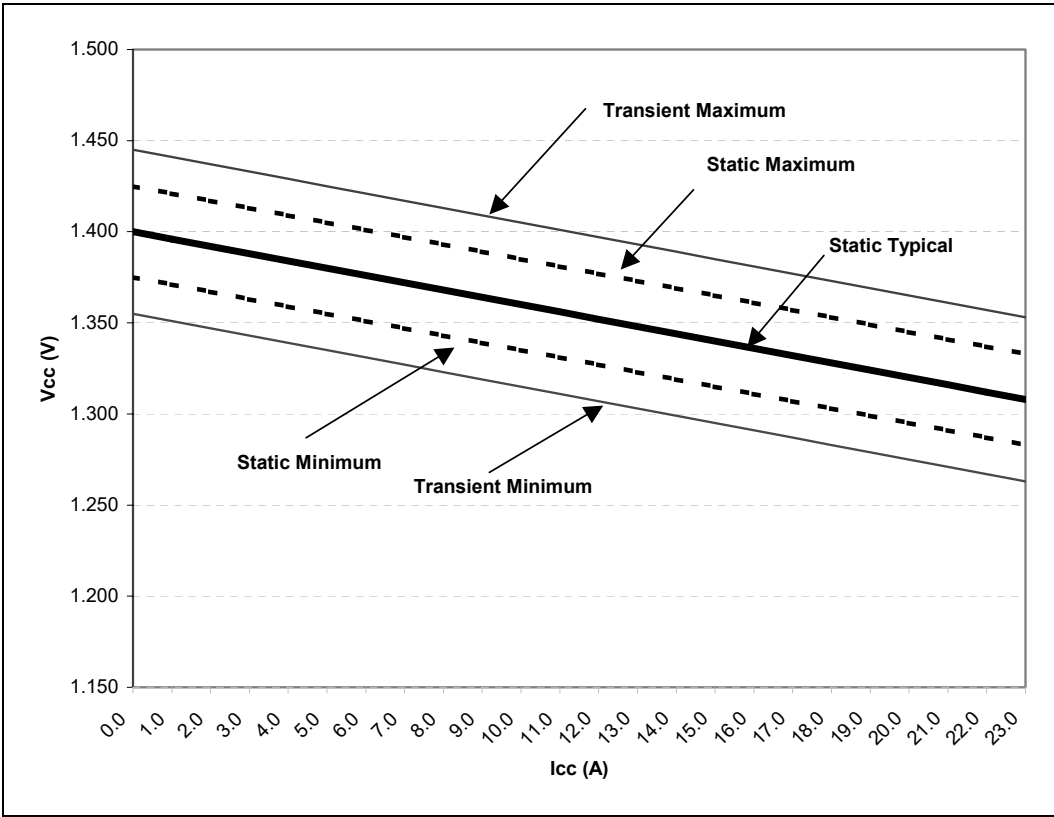


Figure 8. Illustration of Deep Sleep V_{CC} Static and Transient Tolerances (VID Setting = 1.40 V)

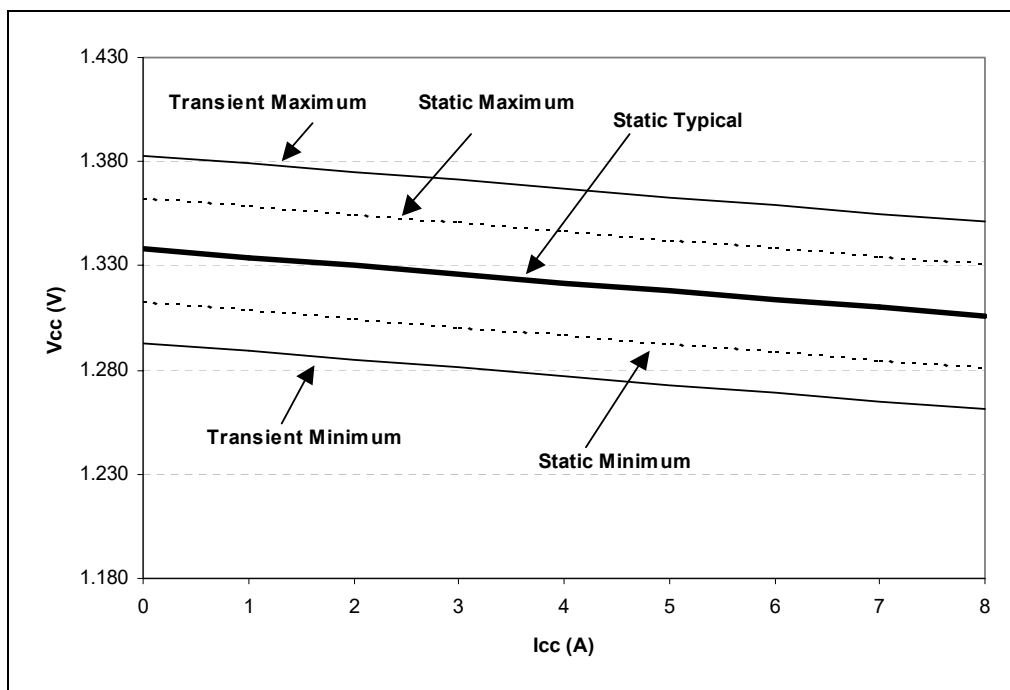


Table 22. AGTL Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	-0.15	$V_{REF}-0.2$	V	
V_{IH}	Input High Voltage	$V_{REF}+0.2$	V_{CCT}	V	See $V_{CCT,max}$ in Table 11
V_{OH}	Output High Voltage	—	—	V	See $V_{CCT,max}$ in Table 11
R_{ON}	Output Low Drive Strength		16.67	Ω	Note 2
I_L	Leakage Current for Inputs, Outputs and I/Os		100	μA	Note 1

NOTES:

1. Specification applies to leakage high only, for pins with on die R_{TT} , ($0 < V_{IN/OUT} \leq V_{CCT}$).
2. Refer to IBIS models for I/V characteristics.

Table 23. AGTL Bus DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CCT}	Bus Termination Voltage		1.25		V	Note 1
V_{REF}	Input Reference Voltage	$\frac{2}{3}V_{CCT} - 2\%$	$\frac{2}{3}V_{CCT}$	$\frac{2}{3}V_{CCT} + 2\%$	V	$\pm 2\%$, Note 2
R_{TT}	Bus Termination Strength	50	56	65	Ω	On-die R_{TT} , Note 3

NOTES:

1. Please refer to Table 11 for minimum and maximum values.
2. V_{REF} should be created from V_{CCT} by a voltage divider.
3. The RESET# signal does not have an on-die R_{TT} . It requires an off-die $56.2 \Omega \pm 1\%$ terminating resistor connected to V_{CCT} .

Table 24. CLKREF, APIC, TAP, CMOS, and Open-drain Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V _{IL15}	Input Low Voltage, 1.5 V CMOS	−0.15	V _{CMOSREFmin} − 300 mV	V	
V _{IL18}	Input Low Voltage, 1.8 V CMOS	−0.36	0.36	V	Notes 1, 2
V _{IH15}	Input High Voltage, 1.5 V CMOS	V _{CMOSREFmax} + 250 mV	2.0	V	Note 10
V _{IH15PICD}	Input High Voltage, 1.5 V PICD[1:0]	V _{CMOSREFmax} + 200 mV	2.0	V	Note 11
V _{IH18}	Input High Voltage, 1.8 V CMOS	1.44	2.0	V	Notes 1, 2
V _{OH15}	Output High Voltage, 1.5 V CMOS	N/A	1.615	V	All outputs are Open-drain
V _{OH33}	Output High Voltage, 3.3 V signals	2.0	3.465	V	3.3V + 5%
V _{OL33}	Output Low Voltage, 3.3 V signals		0.8	V	
V _{OL}	Output Low Voltage		0.3	V	Note 8
V _{CMOSREF}	CMOSREF Voltage	0.90	1.10	V	Note 4
V _{CLKREF}	CLKREF Voltage	1.187	1.312	V	Note 9
V _{ILVTPWR}	Input Low Voltage, VTPWRGD		0.4	V	Note 7
V _{IHVTPWR}	Input High Voltage, VTPWRGD	1.0		V	Note 7
R _{ON}			30	Ω	Note 3
I _{OL}	Output Low Current	10		mA	Note 6
I _L	Leakage Current for Inputs, Outputs and I/Os		±100	μ A	Note 5

NOTES:

- Parameter applies to the PWRGOOD signal only.
- V_{ILx,min} and V_{IHx,max} only apply when BCLK, BCLK# and PICCLK are stopped. PICCLK should be stopped in the low state. See Table 33 and Table 34 for DC levels when BCLK and BCLK# are stopped.
- Measured at 9 mA.
- V_{CMOSREF} should be created from a stable 1.5-V supply using a voltage divider. It must track the voltage supply to maintain noise immunity. The same 1.5-V supply should be used to power the chipset CMOS I/O buffers that drive these signals.
- (0 ≤ V_{IN/OUT} ≤ V_{IHx,max}).
- Specified as the minimum amount of current that the output buffer must be able to sink. However, V_{OL,max} cannot be guaranteed if this specification is exceeded.
- Parameter applies to VTPWRGD signal only.
- Applies to non-AGTL signals except BCLK, PWRGOOD, PICCLK, BSEL[1:0], VID[4:0].
- ±5% DC tolerance. CLKREF must be generated from the 2.5-V supply used to generate the BCLK signal. AC Tolerance must be less than −40 dB @ 1 MHz.
- Applies to all TAP and CMOS signals (not to APIC signals).
- Applies to PICD[1:0].

3.6 AC Specifications

3.6.1 System Bus, Clock, APIC, TAP, CMOS, and Open-drain AC Specifications

All system bus AC specifications for the AGTL signal group are relative to the crossing point of the rising edge of the BCLK input and falling edge of the BCLK# input. All AGTL timings are referenced to V_{REF} for both “0” and “1” logic levels unless otherwise specified. All APIC, TAP, CMOS, and Open-drain signals except PWRGOOD are referenced to 1.0 V. All minimum and maximum specifications are at points within the power supply ranges shown in Table 12 through Table 21 and junction temperatures

(Tj) in the range 0°C to 100°C unless otherwise noted. Tj **must** be less than or equal to 100°C (or the otherwise-noted given value) for all functional processor states.

Table 25. System Bus Clock AC Specifications (Differential) ¹

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes
	System Bus Frequency		133		MHz		
T1	BCLK Period – average	7.5		7.7	ns	8	Note 2
T1abs	BCLK Period – Instantaneous minimum	7.3			ns	8	Note 2
T2	BCLK Cycle to Cycle Jitter			200	ps	8	Notes 2, 3, 4
T5	BCLK Rise Time	175		467	ps	8	Notes 2, 6, 8
		175		550			Notes 2, 6, 9
T6	BCLK Fall Time	175		467	ps	8	Notes 2, 6, 8
		175		550			Notes 2, 6, 9
	Vcross for 1-V swing	0.51		0.76	V	7	Note 7
	Rise/Fall Time Matching			325	ps	7	Note 5
	BCLK Duty Cycle	45%		55%		8	Note 2

NOTES:

1. All AC timings for AGTL and CMOS signals are referenced to the BCLK and BCLK# crossing point.
2. Measured on differential waveform: defined as (BCLK – BCLK#).
3. Not 100% tested. Specified by design/characterization.
4. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that the clock driver be designed to meet a period stability specification into a test load of 10 pF to 20 pF. This should be measured on the rising edge of adjacent BCLKs at the BCLK, BCLK# crossing point. The jitter present must be accounted for as a component of BCLK skew between devices. Period difference is measured around 0-V crossing points.
5. Measurement taken from common mode waveform, measure rise/fall time from 0.41 to 0.86 V. Rise/fall time matching is defined as “the instantaneous difference between maximum BCLK rise (fall) and minimum BCLK# fall (rise) time, or minimum BCLK rise (fall) and maximum BCLK# fall (rise) time”. This parameter is designed to guard waveform symmetry.
6. Rise time is measured from –0.35 V to 0.35 V and fall time is measured from 0.35 V to –0.35 V.
7. Measured on common mode waveform – includes every rise/fall crossing.
8. Measured at the package ball for the Micro-FCBGA package.
9. Measured at the socket pin for the Micro-FCPGA package.

Table 26. System Bus Clock AC Specifications (133 MHz, Single Ended) ¹

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	System Bus Frequency		133		MHz	
T1S	BCLK Period	7.5	7.65	ns	6	Note 2
T1Sabs	BCLK Period – Instantaneous Minimum	7.25				Note 2
T2S	BCLK Period Stability		± 250	ps		Notes 2, 3, 4
T3S	BCLK High Time	1.4		ns	6	at>2.0 V
T4S	BCLK Low Time	1.4		ns	6	at<0.5 V
T5S	BCLK Rise Time	0.4	1.6	ns	6	Note 5
T6S	BCLK Fall Time	0.4	1.6	ns	6	Note 5

NOTES:

1. All AC timings for AGTL and CMOS signals are referenced to the BCLK rising edge at 1.25 V.
2. Period, jitter, skew and offset measured at 1.25 V.
3. Not 100% tested. Specified by design/characterization.
4. Measured on the rising edge of adjacent BCLKs at 1.25 V. The jitter present must be accounted for as a component of BCLK skew between devices.
5. Measured between 0.5 V and 2.0 V.

Table 27. System Bus Clock AC Specifications (100 MHz, Single Ended)¹

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes
	System Bus Frequency		100		MHz		
T1S1	BCLK Period		10		ns	6	Note 2
T1S1abs	BCLK Period – Instantaneous Minimum	9.75			ns		Note 2
T2S1	BCLK Period Stability			± 250	ps		Notes 2, 3, 4
T3S1	BCLK High Time	2.70			ns	6	at>2.0 V
T4S1	BCLK Low Time	2.45			ns	6	at<0.5 V
T5S1	BCLK Rise Time	0.4		1.6	ns	6	Note 5
T6S1	BCLK Fall Time	0.4		1.6	ns	6	Note 5

NOTES:

1. All AC timings for AGTL and CMOS signals are referenced to the BCLK rising edge at 1.25 V.
2. Period, jitter, skew and offset measured at 1.25 V.
3. Not 100% tested. Specified by design/characterization.
4. Measured on the rising edge of adjacent BCLKs at 1.25 V. The jitter present must be accounted for as a component of BCLK skew between devices.
5. Measured between 0.5 V and 2.0 V.



Table 28. Valid Mobile Intel Celeron Processor Frequencies

BCLK Frequency (MHz)	Frequency Multiplier	Core Frequency (MHz)	Power-on Configuration bits [27,25:22]
100	6.5	650	0, 1111
133	5.5	733	0, 0100
133	7.5	1000	0, 1101
133	8	1066	0, 1010
133	8.5	1133	1, 0110
133	9	1200	1, 0000
133	10	1333	1, 1011

NOTE: While other combinations of bus and core frequencies are defined, operation at frequencies other than those listed above will not be validated by Intel and are not guaranteed. The frequency multiplier is programmed into the processor when it is manufactured, and it cannot be changed.

Table 29. AGTL Signal Groups AC Specifications¹

$R_{TT} = 56\Omega$ internally terminated to V_{CCT} ; $V_{REF} = \frac{2}{3}V_{CCT}$; load = 50 ohms

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T7	AGTL Output Valid Delay	0.40	3.25	ns	9	
T8	AGTL Input Setup Time	0.95 1.30		ns	10	Notes 2, 3, 6 Note 7
T9	AGTL Input Hold Time	1		ns	10	Note 4
T10	RESET# Pulse Width	1		ms	11,12	Note 5

NOTES:

1. All AC timings for AGTL signals are referenced to the crossing point of the BCLK rising edge and the BCLK# falling edge for Differential Clocking and to the BCLK rising edge at 1.25 V for Single Ended Clocking. All AGTL signals are referenced at V_{REF} . Unless other specified, all timings apply to both 100-MHz and 133-MHz bus frequencies.
2. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
3. Specification is for a minimum 0.40-V swing from $V_{REF}-200$ mV to $V_{REF}+200$ mV.
4. Specification is for a maximum 0.8-V swing from $V_{CCT}-0.8$ V to V_{CCT} .
5. After V_{CC} , V_{CCT} , and BCLK, BCLK# become stable and PWRGOOD is asserted.
6. Applies to all processors supporting 133-MHz bus clock frequency except Ultra Low Voltage processors.
7. Applies to all processors supporting 100-MHz bus clock frequency and Ultra Low Voltage processors supporting 133-MHz bus clock frequency.

Table 30. CMOS and Open-drain Signal Groups AC Specifications^{1, 2}

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T14	1.5V Input Pulse Width, except PWRGOOD and LINT[1:0]	2		BCLKs	9	Active and inactive states
T14B	LINT[1:0] Input Pulse Width	6		BCLKs	9	Note 3
T15	PWRGOOD Inactive Pulse Width	2		μ s	12	Note 4,5

NOTES:

1. All AC timings for CMOS and Open-drain signals are referenced to the crossing point of the BCLK rising edge and BCLK# falling edge for Differential Clocking and to the rising edge of BCLK at 1.25 V for Single Ended Clocking. All CMOS and Open-drain signals are referenced at 1.0 V.
2. Minimum output pulse width on CMOS outputs is 2 BCLKs.
3. This specification only applies when the APIC is enabled and the LINT1 or LINT0 signal is configured as an edge triggered interrupt with fixed delivery, otherwise specification T14 applies.
4. When driven inactive, or after V_{CC} , V_{CCT} and BCLK, BCLK# become stable. PWRGOOD must remain below $V_{IL18,MAX}$ until all the voltage planes meet the voltage tolerance specifications in Table 12 through Table 21 and BCLK, BCLK# have met the BCLK, BCLK# AC specifications in Table 35 and Table 36 for at least 2 μ s. PWRGOOD must rise error-free and monotonically to 1.8 V.
5. If the BCLK Settling Time specification (T60) can be guaranteed at power-on reset then the PWRGOOD Inactive Pulse Width specification (T15) is waived and BCLK may start after PWRGOOD is asserted. PWRGOOD must still remain below $V_{IL25,max}$ until all the voltage planes meet the voltage tolerance specifications.

Table 31. Reset Configuration AC Specifications and Power On/Power Down Timings

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes
T16	Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT#, PICD0) Setup Time	4			BCLKs	11	Before deassertion of RESET#
T17	Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT#, PICD0) Hold Time	2		20	BCLKs	11	After clock that deasserts RESET#
T18	RESET#/PWRGOOD Setup Time	1			ms	12	Before deassertion of RESET# ¹
T18A	VCCT to VTPWRGD Setup Time	1			ms	12	
T18B	VCC to PWRGOOD Setup Time		10		ms	12	
T18C	BSEL, VID valid time before VTPWRGD assertion	1			μ s	12	
T18D	RESET# inactive to Valid Outputs	1			BCLK	11	
T18E	RESET# inactive to Drive Signals	4			BCLKs	11	
T19A	Time from VCC(nominal)-12% to PWRGOOD low			0	ns	13	VCC(nominal) is the VID voltage setting
T19B	All outputs valid after PWRGOOD low	0			ns	13	
T19C	All inputs required valid after PWRGOOD low	0			ns	13	
T20A	Time from VCCT-12% to VTPWRGD low			0	ns	14	
T20B	All outputs valid after VTPWRGD low	0			ns	14	
T20C	All inputs required valid after VTPWRGD low	0			ns	14	
T20D	VID, BSEL signals valid after VTPWRGD low	0			ns	14	
T20E	VTPWRGD Transition Time			100	μ s		Measurement from 300 mV to 900 mV. Amount of noise (glitch) less than 100 mV. See Section 4.3.1 for details

NOTE: At least 1 ms must pass after PWRGOOD rises above $V_{IH18min}$ and BCLK, BCLK# meet their AC timing specification until RESET# may be deasserted.

Table 32. APIC Bus Signal AC Specifications ¹

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T21	PICCLK Frequency	2	33.3	MHz		Note 2
T22	PICCLK Period	30	500	ns	6	
T23	PICCLK High Time	10.5		ns	6	at >1.6 V
T24	PICCLK Low Time	10.5		ns	6	at <0.4 V
T25	PICCLK Rise Time	0.25	3.0	ns	6	(0.4 V – 1.6 V)
T26	PICCLK Fall Time	0.25	3.0	ns	6	(1.6 V – 0.4 V)
T27	PICD[1:0] Setup Time	8.0		ns	9	Note 3
T28	PICD[1:0] Hold Time	2.5		ns	9	Note 3
T29	PICD[1:0] Valid Delay (Rising Edge)	1.5	8.7	ns	8	Notes 3, 4
	PICD[1:0] Valid Delay (Falling Edge)	1.5	12.0			

NOTES:

1. All AC timings for APIC signals are referenced to the PICCLK rising edge at 1.0 V. All CMOS signals are referenced at 1.0 V.
2. The minimum frequency is 2 MHz when PICD0 is at 1.5 V at reset Referenced to PICCLK Rising Edge.
3. For Open-drain signals, Valid Delay is synonymous with Float Delay.
4. Valid delay timings for these signals are specified into 150 Ω to 1.5 V and 0 pF of external load. For real system timings these specifications must be derated for external capacitance at 105 ps/pF.

Table 33. TAP Signal AC Specifications¹

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T30	TCK Frequency	—	16.67	MHz		
T31	TCK Period	60	—	ns	6	
T32	TCK High Time	25.0		ns	6	$\geq V_{CMOSREF}+0.2V$, Note 2
T33	TCK Low Time	25.0		ns	6	$\leq V_{CMOSREF}-0.2V$, Note 2
T34	TCK Rise Time		5.0	ns	6	$(V_{CMOSREF}-0.2V) - (V_{CMOSREF}+0.2V)$, Notes 2, 3
T35	TCK Fall Time		5.0	ns	6	$(V_{CMOSREF}+0.2V) - (V_{CMOSREF}-0.2V)$, Notes 2, 3
T36	TRST# Pulse Width	40.0		ns	16	Asynchronous, Note 2
T37	TDI, TMS Setup Time	5.0		ns	15	Note 4
T38	TDI, TMS Hold Time	14.0		ns	15	Note 4
T39	TDO Valid Delay	1.0	10.0	ns	15	Notes 5, 6
T40	TDO Float Delay		25.0	ns	15	Notes 2, 5, 6
T41	All Non-Test Outputs Valid Delay	2.0	25.0	ns	15	Notes 5, 7, 8
T42	All Non-Test Outputs Float Delay		25.0	ns	15	Notes 2, 5, 7, 8
T43	All Non-Test Inputs Setup Time	5.0		ns	15	Notes 4, 7, 8
T44	All Non-Test Inputs Hold Time	13.0		ns	15	Notes 4, 7, 8

NOTES:

1. All AC timings for TAP signals are referenced to the TCK rising edge at 1.0 V. All TAP and CMOS signals are referenced at 1.0 V.
2. Not 100% tested. Specified by design/characterization.
3. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16 MHz.
4. Referenced to TCK rising edge.
5. Referenced to TCK falling edge.
6. Valid delay timing for this signal is specified into 150 Ω terminated to 1.5 V and 0 pF of external load. For real system timings these specifications must be derated for external capacitance at 105 ps/pF.
7. Non-Test Outputs and Inputs are the normal output or input signals (except TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
8. During Debug Port operation use the normal specified timings rather than the TAP signal timings.

Table 34. Quick Start/Deep Sleep AC Specifications¹

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T45	Quick Start Cycle Completion to Clock Stop or DPSP# assertion	100		BCLKs	17, 18	
T46	Quick Start Cycle Completion to Input Signals Stable		0	μ s	17, 18	
T47	Deep Sleep PLL Lock Latency	0	30	μ s	17, 18	Note 2
T48	STPCLK# Hold Time from PLL Lock	0		ns	17, 18	
T49	Input Signal Hold Time from STPCLK# Deassertion	8		BCLKs	17, 18	

NOTES:

1. Input signals other than RESET# and BPRI# must be held constant in the Quick Start state.
2. The BCLK, BCLK# Settling Time specification (T60) applies to Deep Sleep state exit under all conditions.

Figure 9. BCLK (Single Ended)/PICCLK/TCK Generic Clock Timing Waveform

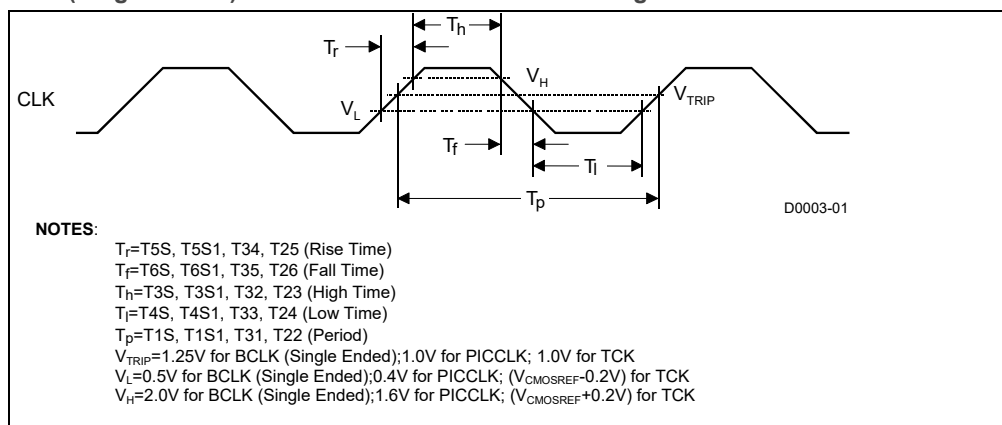


Figure 10. Differential BCLK/BCLK# Waveform (Common Mode)

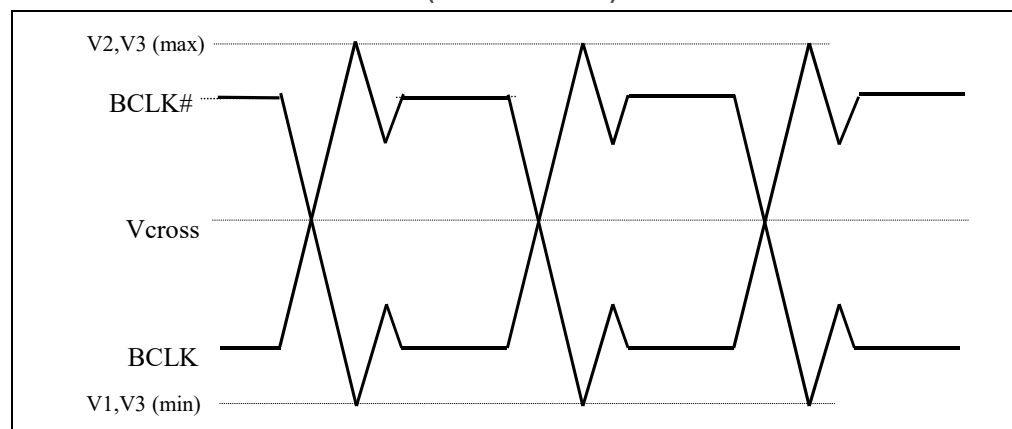


Figure 11. BCLK/BCLK# Waveform (Differential Mode)

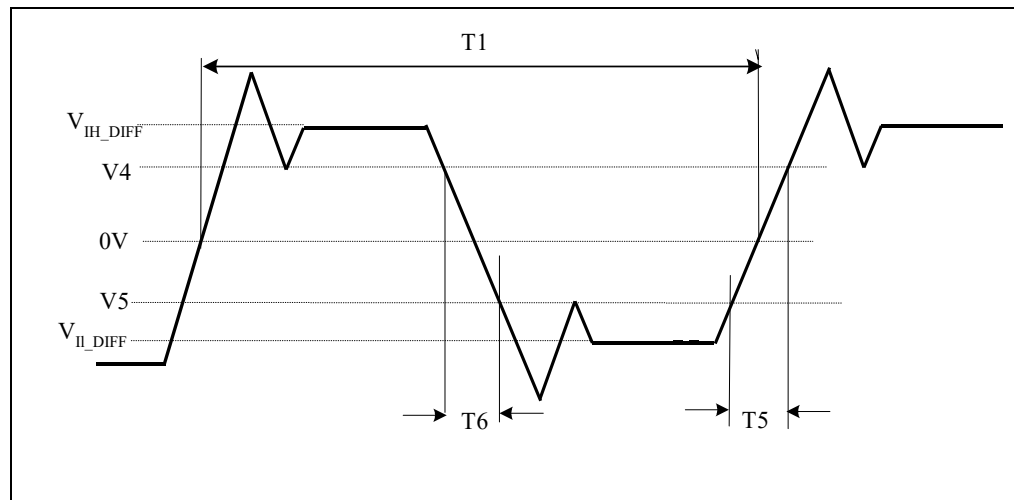


Figure 12. Valid Delay Timings

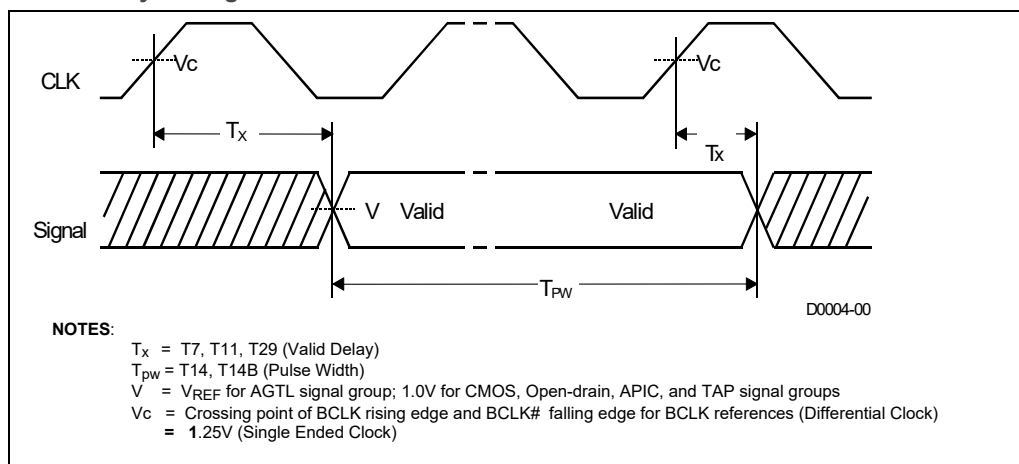


Figure 13. Setup and Hold Timings

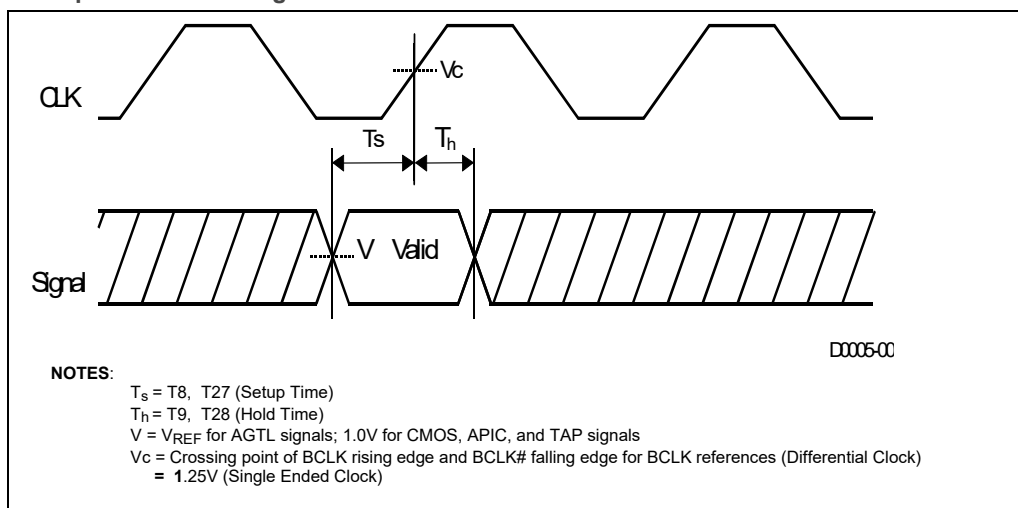


Figure 14. Cold/Warm Reset and Configuration Timings

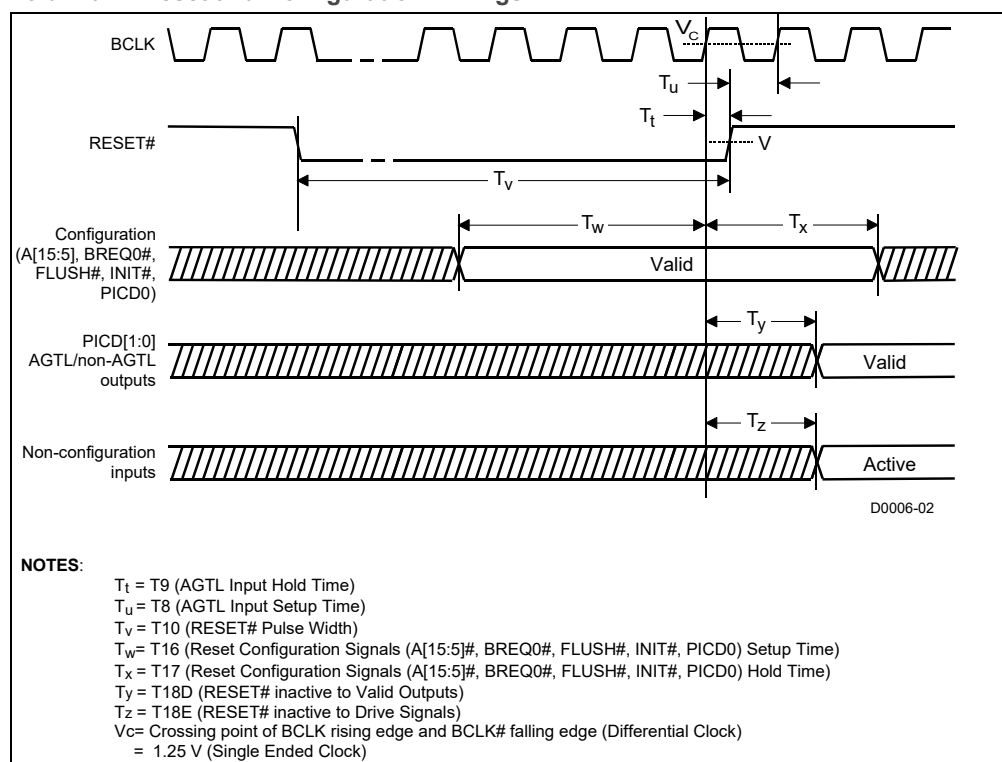


Figure 15. Power-on Sequence and Reset Timings

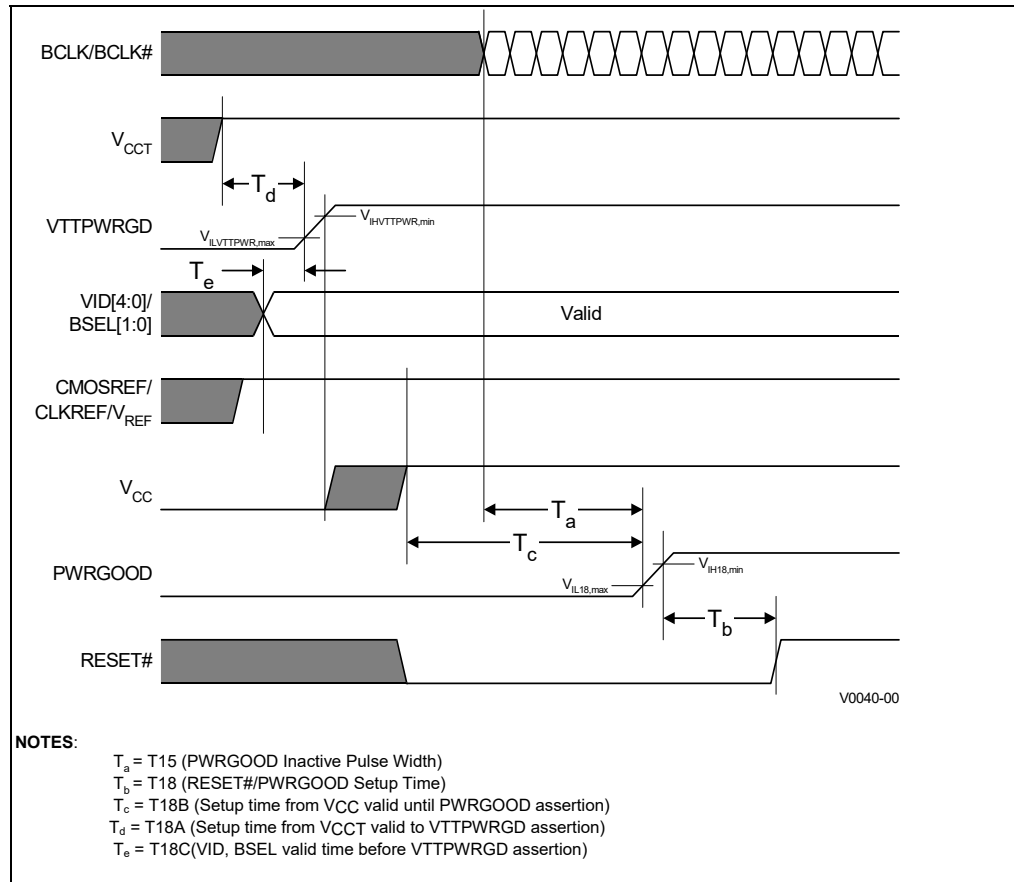




Figure 16. Power Down Sequencing and Timings (VCC Leading)

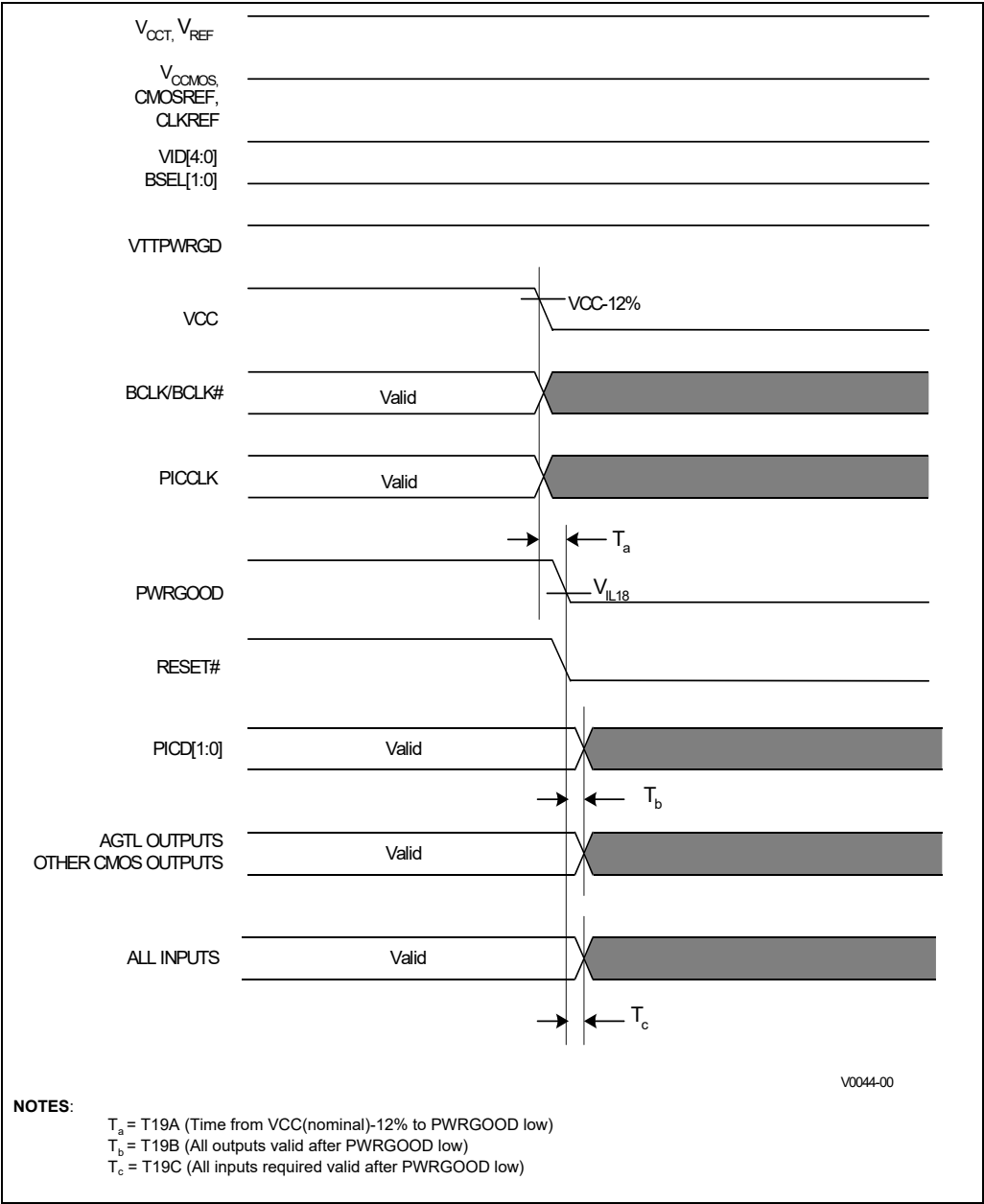


Figure 17. Power Down Sequencing and Timings (V_{CCT} Leading)

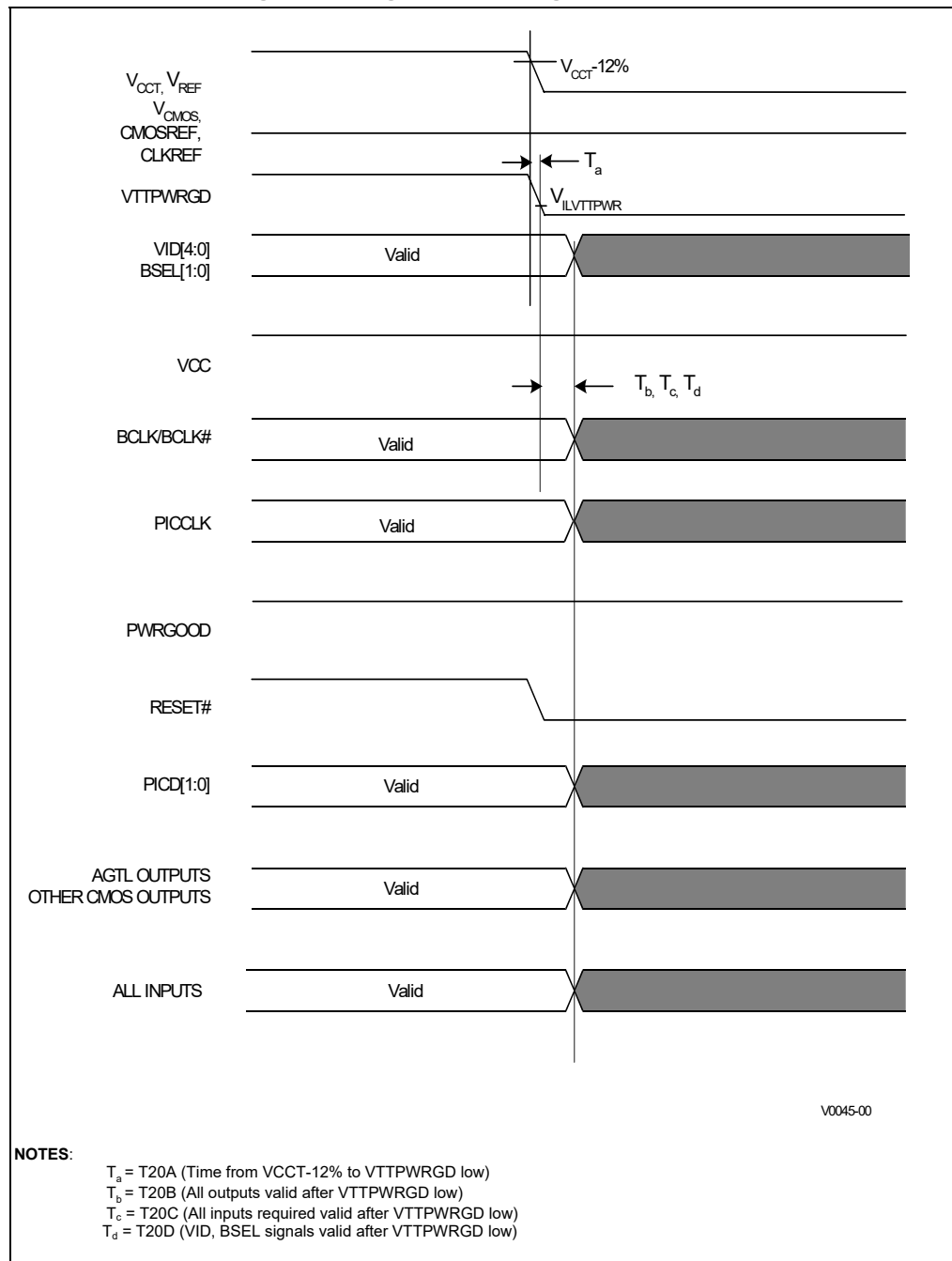


Figure 18. Test Timings (Boundary Scan)

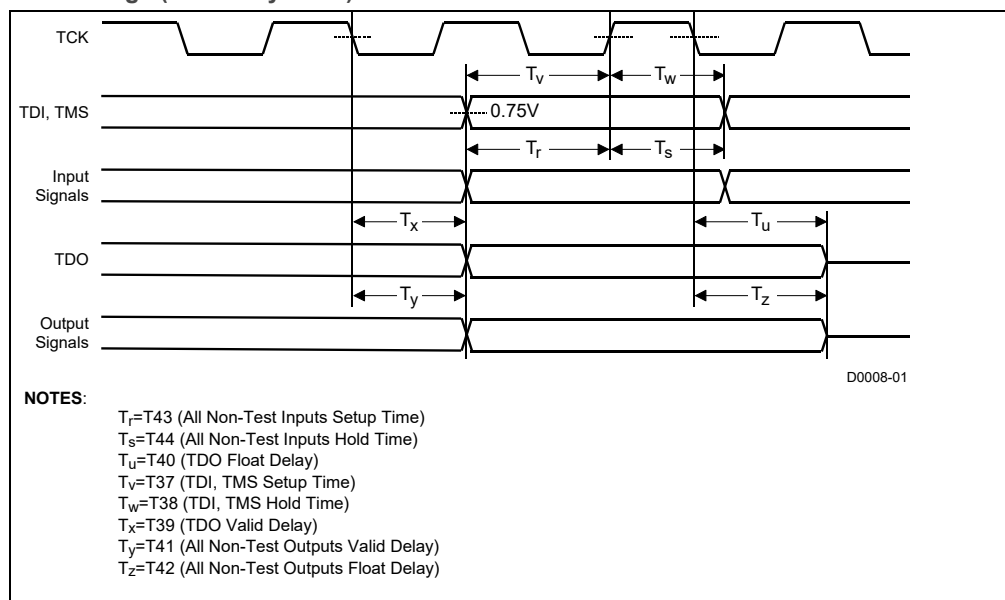


Figure 19. Test Reset Timings

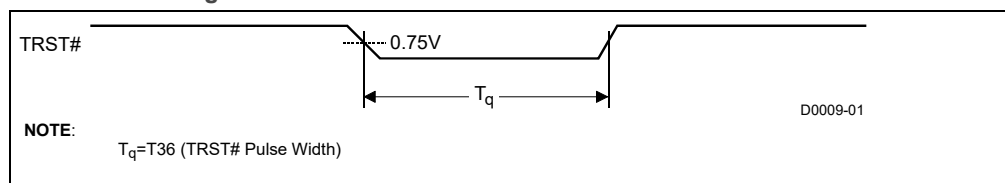




Figure 20. Quick Start/Deep Sleep Timing (BCLK Stopping Method)

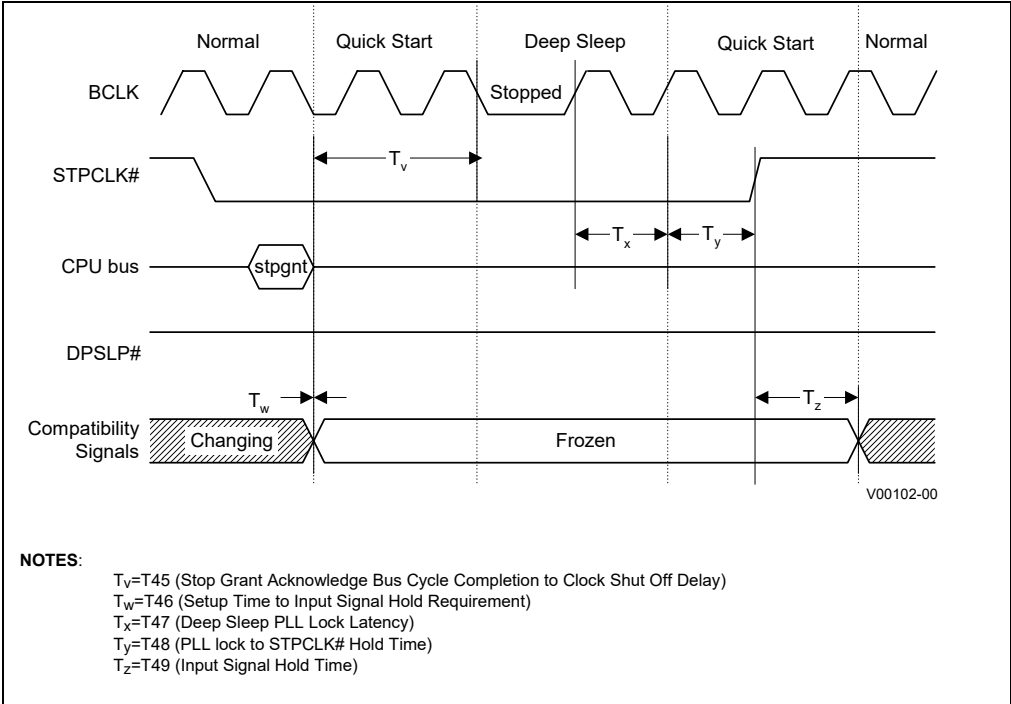
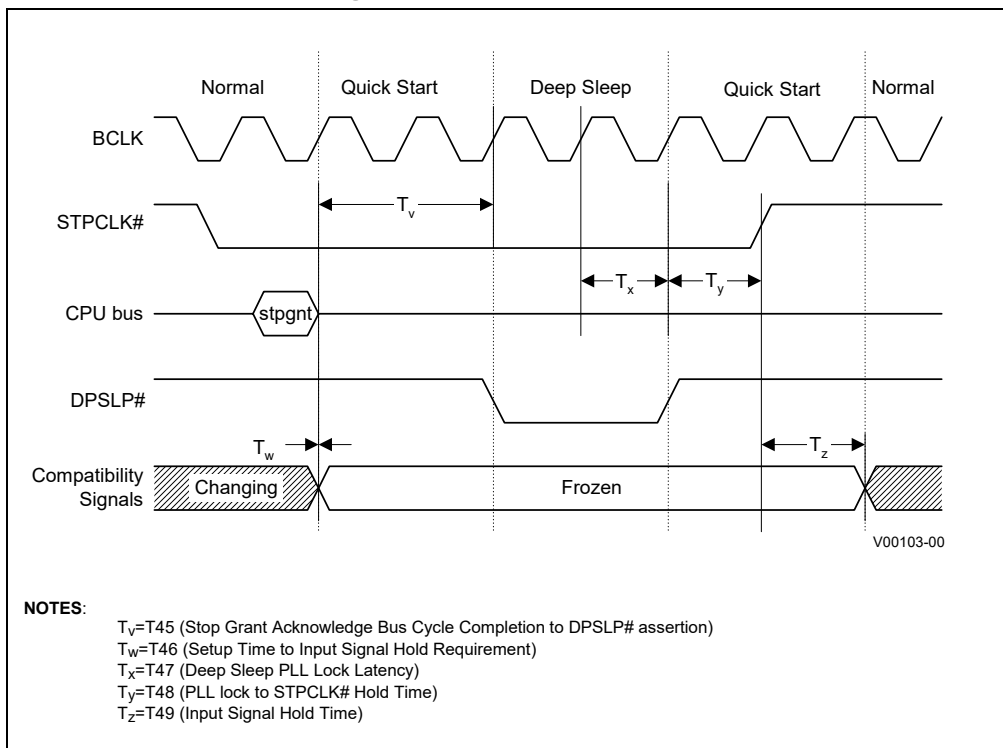


Figure 21. Quick Start/Deep Sleep Timing (DPSLP# Assertion Method)



4. System Signal Simulations

Systems must be simulated using IBIS models to determine if they are compliant with this specification. All references to BCLK signal quality also apply to BCLK# for Differential Clocking.

4.1 System Bus Clock (BCLK) and PICCLK DC Specifications and AC Signal Quality Specifications

Table 35. BCLK (Differential) DC Specifications and AC Signal Quality Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
V1	$V_{IL,BCLK}$	-0.2	0.35	V	7	Note 1
V2	$V_{IH,BCLK}$	0.92	1.45	V	7	Note 1
V3	V_{IN} Absolute Voltage Range	-0.2	1.45	V	7	Undershoot/Overshoot, Note 2
V4	BCLK Rising Edge Ringback	0.35		V	8	Note 3
V5	BCLK Falling Edge Ringback		-0.35	V	8	Note 3
V_{BCLK_DPSLP}	BCLK Voltage in Deep Sleep State	0.4	1.45	V		Note 4
$V_{BCLK\#_DPSLP}$	BCLK# Voltage in Deep Sleep State	0	V_{BCLK_DPSLP} - 0.2 V	V		Note 4

NOTES:

1. The clock must rise/fall monotonically between $V_{IL,BCLK}$ and $V_{IH,BCLK}$.
2. These specifications apply only when BCLK, BCLK# are running.
3. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) voltage the differential waveform can go to after passing the V_{IH_DIFF} (rising) or V_{IL_DIFF} (falling) levels. V_{IL_DIFF} (max) = -0.57 V, V_{IH_DIFF} (min) = 0.57 V.
4. Applies when BCLK and BCLK# are stopped in Deep Sleep State.

Table 36. BCLK (Single Ended) DC Specifications and AC Signal Quality Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
V1	$V_{IL,BCLK}$		0.3	V	20	Note 1
V2	$V_{IH,BCLK}$	2.2		V	20	Note 1
V3	V_{IN} Absolute Voltage Range	-0.5	3.1	V	20	Undershoot/Overshoot, Note 2
V4	BCLK Rising Edge Ringback	2.0		V	20	Absolute Value, Note 3
V5	BCLK Falling Edge Ringback		0.5	V	20	Absolute Value, Note 3

NOTES:

1. The clock must rise/fall monotonically between $V_{IL,BCLK}$ and $V_{IH,BCLK}$. BCLK must be stopped in the low state.
2. These specifications apply only when BCLK is running. BCLK may not be above $V_{IH,BCLK,max}$ or below $V_{IL,BCLK,min}$ for more than 50% of the clock cycle.
3. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can go to after passing the $V_{IH,BCLK}$ (rising) or $V_{IL,BCLK}$ (falling) voltage limits.

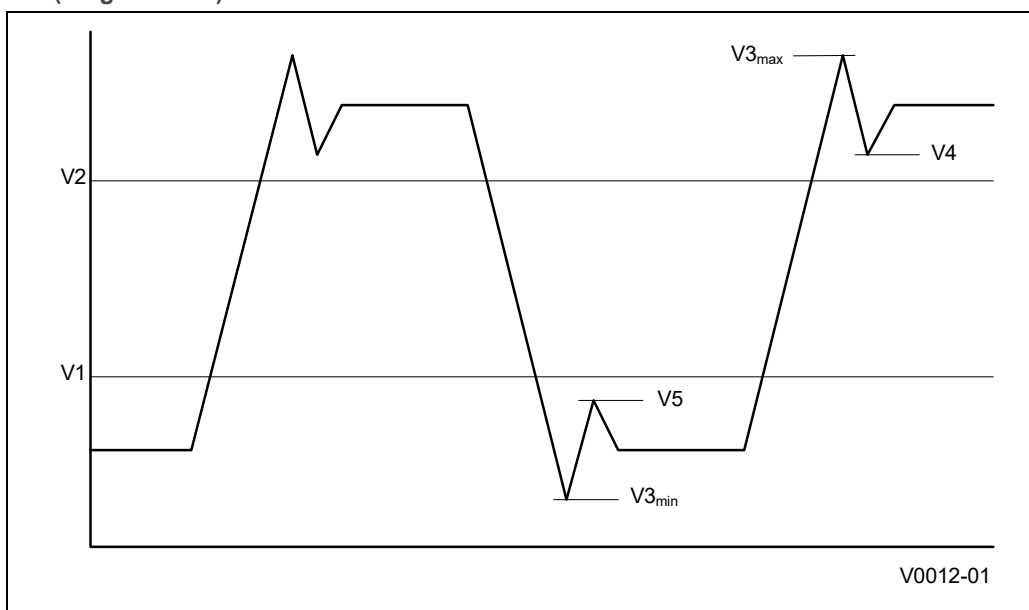
Table 37. PICCLK DC Specifications and AC Signal Quality Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
V1	V_{IL20}		0.4	V	20	Note 1
V2	V_{IH20}	1.6		V	20	Note 1
V3	V_{IN} Absolute Voltage Range	-0.5	2.4	V	20	Undershoot, Overshoot, Note 2
V4	PICCLK Rising Edge Ringback	1.6		V	20	Absolute Value, Note 3
V5	PICCLK Falling Edge Ringback		0.4	V	20	Absolute Value, Note 3

NOTES:

1. The clock must rise/fall monotonically between V_{IL20} and V_{IH20} .
2. These specifications apply only when PICCLK is running. See the DC specifications for when PICCLK is stopped. PICCLK may not be above $V_{IH20,max}$ or below $V_{IL20,min}$ for more than 50% of the clock cycle.
3. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the PICCLK signal can go to after passing the V_{IH20} (rising) or V_{IL20} (falling) voltage limits.

Figure 22. BCLK (Single Ended)/PICCLK Generic Clock Waveform



4.2 AGTL AC Signal Quality Specifications

Ringback specifications for the AGTL signals are as follows: Ringback below $V_{REF,max} + 200$ mV is not authorized during low to high transitions. Ringback above $V_{REF,min} - 200$ mV is not authorized during high to low transitions.

Overshoot and undershoot specifications are documented in Table 38 and Table 39 and illustrated in Figure 23.

Figure 23. Maximum Acceptable Overshoot/Undershoot Waveform

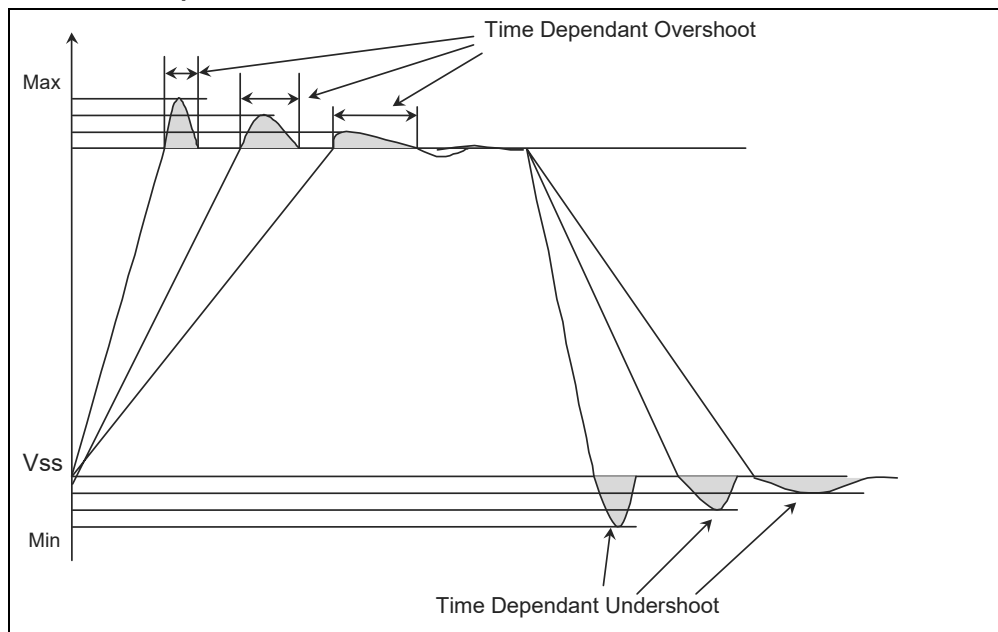


Table 38. 133-MHz AGTL Signal Group Overshoot/Undershoot Tolerance at the Processor Core

Max V_{CCT} + Overshoot/Undershoot Magnitude (volts)	Allowed Pulse Duration (ns) [Tj=100C (see Note 7)]		
	Activity Factor = 0.01	Activity Factor = 0.1	Activity Factor = 1
1.78	1.5	0.15	0.015
1.73	3.5	0.35	0.035
1.68	7.2	0.72	0.072
1.63	15	1.5	0.15
1.58	15	3.2	0.32
1.53	15	6.5	0.65
1.48	15	14	1.40

NOTES:

1. Under no circumstances should the sum of the Max V_{CCT} and absolute value of the Overshoot/Undershoot voltage exceed 1.78 V.
2. Activity factor of 1 represents the same toggle rate as the 133-MHz clock.
3. Ringbacks below V_{CCT} cannot be subtracted from overshoots. Lesser undershoot does not allocate longer or larger overshoot.
4. Ringbacks above ground cannot be subtracted from undershoots. Lesser overshoot does not allocate longer or larger undershoot.
5. System designers are encouraged to follow Intel provided AGTL layout guidelines.
6. All values are specified by design characterization and are not tested.
7. Tj = 85°C for 1.33 GHz.

Table 39. 100-MHz AGTL Signal Group Overshoot/Undershoot Tolerance at the Processor Core

Max V_{CCT} + Overshoot/Undershoot Magnitude (volts)	Allowed Pulse Duration (ns) [Tj=100C (see Note 7)]		
	Activity Factor = 0.01	Activity Factor = 0.1	Activity Factor = 1
1.78	1.6	0.16	0.016
1.73	4.5	0.45	0.045
1.68	9.5	0.95	0.095
1.63	20	2.0	0.2
1.58	20	4.2	0.42
1.53	20	8.5	0.85
1.48	20	19	1.9

NOTES:

1. Under no circumstances should the sum of the Max V_{CCT} and absolute value of the Overshoot/Undershoot voltage exceed 1.78 V.
2. Activity factor of 1 represents the same toggle rate as the 100-MHz clock.
3. Ringbacks below V_{CCT} cannot be subtracted from overshoots. Lesser undershoot does not allocate longer or larger overshoot.
4. Ringbacks above ground cannot be subtracted from undershoots. Lesser overshoot does not allocate longer or larger undershoot.
5. System designers are encouraged to follow Intel provided AGTL layout guidelines.
6. All values are specified by design characterization and are not tested.
7. Tj = 85°C for 1.33 GHz.

4.3 Non-AGTL Signal Quality Specifications

Signals driven to the Mobile Intel Celeron Processor should meet signal quality specifications to ensure that the processor reads data properly and that incoming signals do not affect the long-term reliability of the processor. The overshoot and undershoot specifications for non-AGTL signals are shown in Table 40. Ringback must not exceed the CMOS V_{IH} and V_{IL} specification levels in Table 24.

Table 40. Non-AGTL Signal Group Overshoot/Undershoot Tolerance at the Processor Core

Max V_{CMOS} + Overshoot/Undershoot Magnitude (volts)	Allowed Pulse Duration (ns) [Tj=100C (see note 6)]		
	Activity Factor = 0.01	Activity Factor = 0.1	Activity Factor = 1
2.38	6.5	0.65	0.065
2.33	13	1.3	0.13
2.28	29	2.9	0.29
2.23	60	6	0.6
2.18	60	12	1.2
2.13	60	26	2.6
2.08	60	56	5.6

NOTES:

1. $V_{CMOS}(\text{nominal}) = 1.5 \text{ V}$.
2. Under no circumstances should the sum of the Max V_{CMOS} and absolute value of the Overshoot/Undershoot voltage exceed 2.38 V.
3. Activity factor of 1 represents a toggle rate of 33 MHz.
4. System designers are encouraged to follow Intel provided non-AGTL layout guidelines.
5. All values are specified by design characterization, and are not tested.
6. Tj = 85°C for 1.33 GHz.

4.3.1 PWRGOOD, VTT PWRGD Signal Quality Specifications

The processor requires PWRGOOD to be a clean indication that clocks and the power supplies (V_{CC} , V_{CCT} , etc.) are stable and within their specifications. Clean implies that the signal will remain below V_{IL18} and without errors from the time that the power supplies are turned on, until they come within specification. The signal will then transition monotonically to a high (1.8 V) state. The VTT PWRGD signal must also transition monotonically.

The VTT PWRGD signal is an input to the processor used to determine that the VTT power is stable and the VID and BSEL signals should be driven to their final state by the processor. To ensure the processor correctly reads this signal, the processor must meet the requirement shown in Table 41 while the signal is in its transition region of 300 mV to 900 mV. Also, VTT PWRGD should only enter the transition region once, after VTT is at nominal values, for the assertion of the signal.

4.3.1.1 VTT PWRGD Noise Parameter Specification

Table 41. VTT PWRGD Noise Parameter Specification

Parameter	Specification
Amount of noise (glitch)	Less than 100 mV

In addition, the VTT PWRGD signal should have reasonable transition time through the transition region. A sharp edge on the signal transition will minimize the chance of noise causing a glitch on this signal. Intel recommends the following transition time for the VTT PWRGD signal.

4.3.1.2 VTT_PWRGD Transition Parameter Recommendation

Table 42. VTT_PWRGD Transition Parameter Recommendation

Parameter	Recommendation
Transition time (300 mV to 900 mV)	Less than or equal to 100 μ s

In addition, the VTT_PWRGD signal should have reasonable transition time through the transition region. A sharp edge on the signal transition will minimize the chance of noise causing a glitch on this signal. Intel recommends the following transition time for the VTT_PWRGD signal.

4.3.1.2.1 Transition Region

The transition region covered by this requirement is 300 mV to 900 mV. Once the VTT_PWRGD signal is in that voltage range, the processor is more sensitive to noise, which may be present on the signal. The transition region when the signal first crosses the 300-mV voltage level and continues until the last time it is below 900 mV.

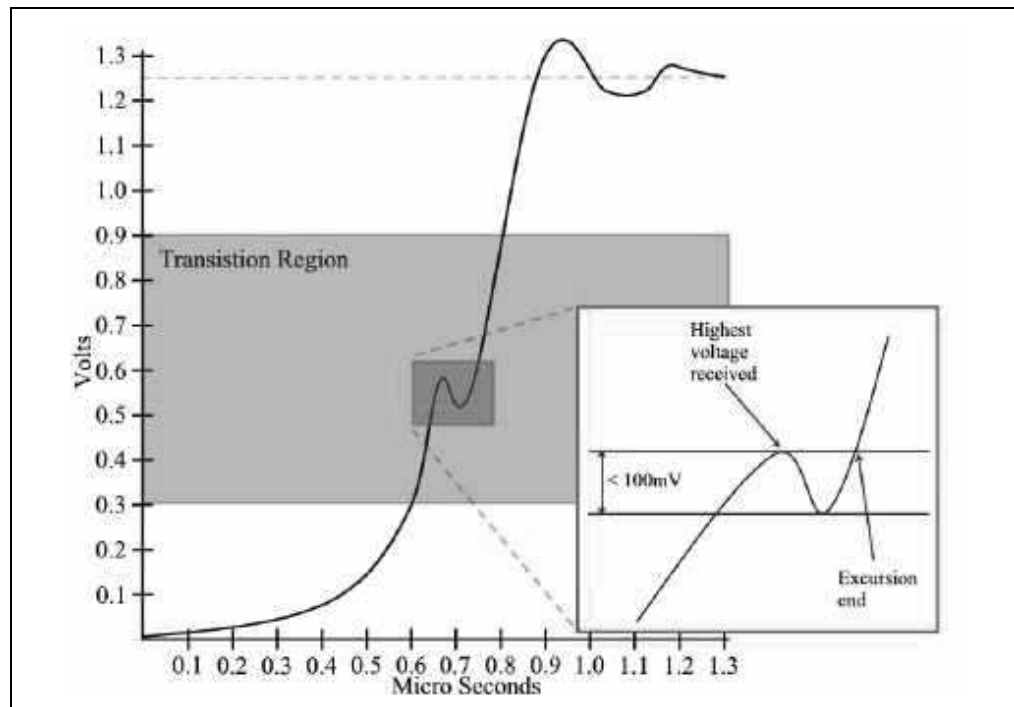
4.3.1.2.2 Transition Time

The transition time is defined as the time the signal takes to move through the transition region. A 100- μ s transition time will ensure that the processor receives a good transition edge.

4.3.1.2.3 Noise

The signal quality of the VTT_PWRGD signal is critical to the correct operation of the processor. Every effort should be made to ensure this signal is monotonic in the transition region. If noise or glitches are present on this signal, the noise or glitches must be kept to less than 100 mV of a voltage drop from the highest voltage level received to that point. This glitch must remain less than 100 mV until the excursion ends by the voltage returning to the highest voltage previously received. Please see Figure 24 for an example graph of this situation and requirements.

Figure 24. VTPWRGD Noise Specification



5. Mechanical Specifications

5.1 Socketable Micro-FCPGA Package

The Mobile Intel Celeron Processor is packaged in a 478-pin Micro-FCPGA package. The Low Voltage and Ultra Low Voltage processors will not be available in this package. The mechanical specifications for the socketable package are provided in Table 43. Figure 25 through Figure 27 illustrate different views of the package.

Table 43. Socketable Micro-FCPGA Package Specification

Symbol	Parameter	Min	Max	Unit
A	Overall height, top of die to package seating plane	1.81	2.03	mm
-	Overall height, top of die to PCB surface, including socket(1)	4.69	5.15	mm
A1	Pin length	1.95	2.11	mm
A2	Die height	0.854		mm
B	Pin diameter	0.28	0.36	mm
D	Package substrate length	34.9	35.1	mm
E	Package substrate width	34.9	35.1	mm
D1	Die length	11.18 ³ 10.82 ⁴		mm
E1	Die width	7.20 ³ 6.85 ⁴		mm
e	Pin pitch	1.27		mm
K	Package edge keep-out	5		mm
K1	Package corner keep-out	7		mm
K3	Pin-side capacitor boundary	14		mm
-	Pin tip radial true position	<=0.254		mm
N	Pin count	478		each
Pdie	Allowable pressure on the die for thermal solution	-	689	kPa
W	Package weight	4.5		g
	Package surface Flatness	0.286		mm

NOTES:

1. All dimensions are subject to change.
2. Overall height with socket is based on design dimensions of the Micro-FCPGA package and socket with no thermal solution attached. Values were based on design specifications and tolerances. This dimension is subject to change based on socket design, OEM motherboard design, or OEM SMT process.
3. Dimension for CPUID = 0x06B1.
4. Dimension for CPUID = 0x06B4.

Figure 25. Socketable Micro-FCPGA Package - Top and Bottom Isometric Views

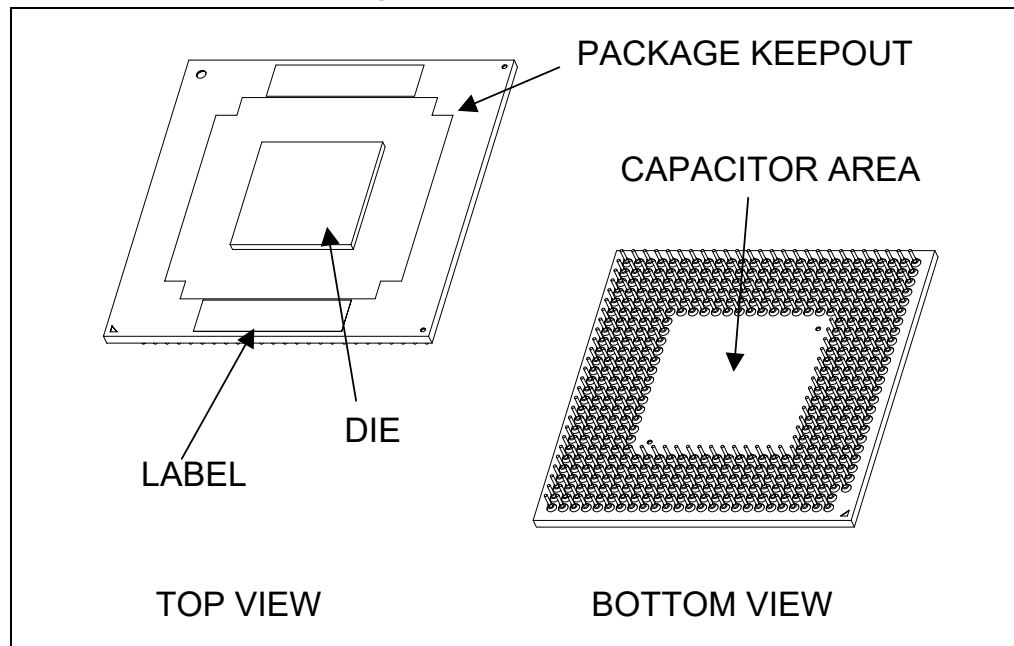


Figure 26. Socketable Micro-FCPGA Package - Top and Side View

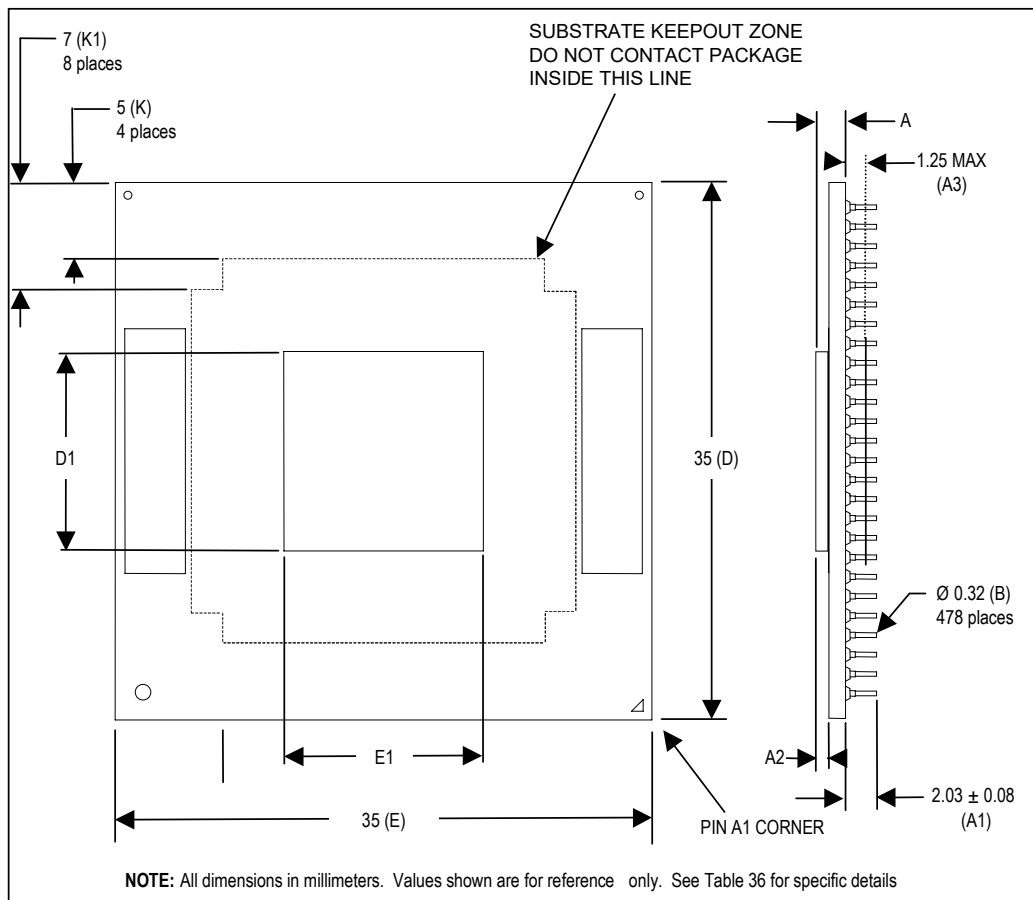
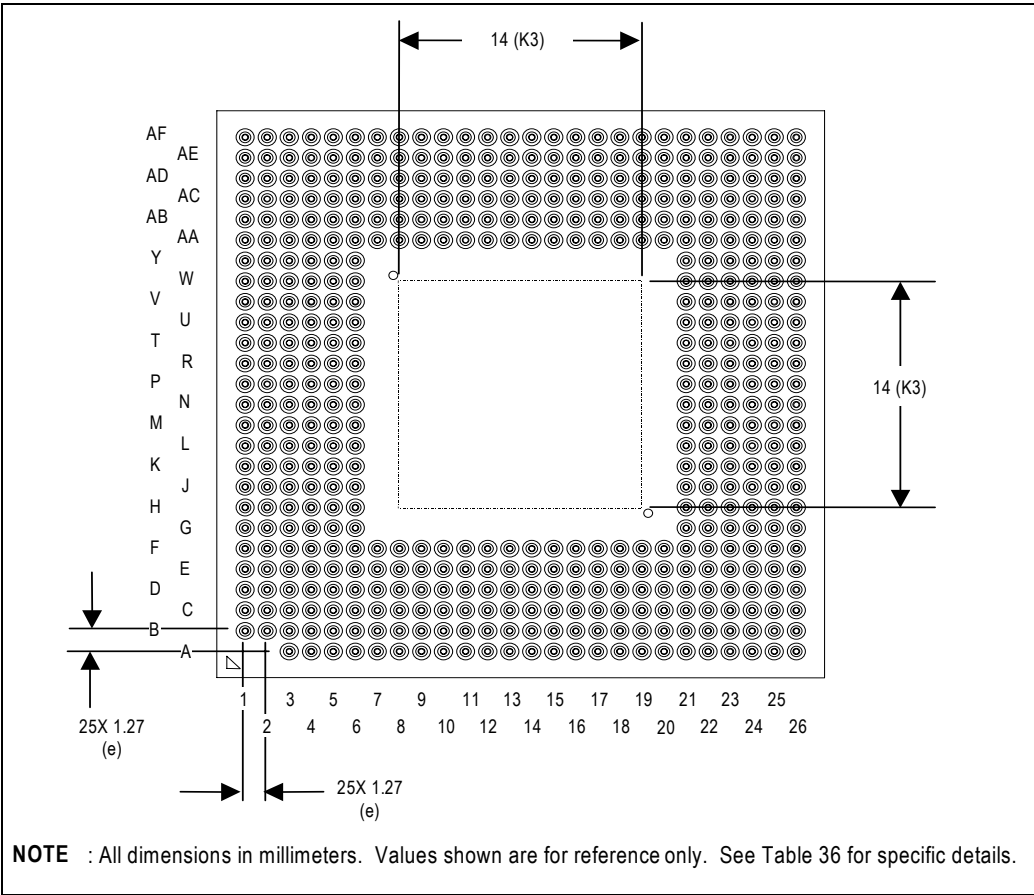


Figure 27. Socketable Micro-FCPGA Package - Bottom View



5.2 Surface Mount Micro-FCBGA Package

The Mobile Intel Celeron Processor will also be available in a surface mount, 479-ball Micro-FCBGA package. The Low Voltage and Ultra Low Voltage processors will be available only in this package. The Mobile Intel Celeron processors at 1.45V and 1.5V will not be available in this package. Mechanical specifications are shown in Table 44. Figure 28 through Figure 30 illustrate different views of the package.

The Micro-FCBGA package may have capacitors placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors, and possibly damage the device or render it inactive. The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting.

Table 44. Micro-FCBGA Package Mechanical Specifications

Symbol	Parameter	Min	Max	Unit
A	Overall height, as delivered (1)	2.27	2.77	mm
A2	Die height	0.854		mm
b	Ball diameter	0.78		mm
D	Package substrate length	34.9	35.1	mm
E	Package substrate width	34.9	35.1	mm
D1	Die length	11.18 ³ 10.82 ⁴		mm
E1	Die width	7.20 ³ 6.85 ⁴		mm
e	Ball pitch	1.27		mm
N	Ball count	479		each
K	Keep-out outline from edge of package	5		mm
K1	Keep-out outline at corner of package	7		mm
K2	Capacitor keep-out height	-	0.7	mm
S	Package edge to first ball center	1.625		mm
--	Solder ball coplanarity	0.2		mm
Pdie	Allowable pressure on the die for thermal solution	-	689	kPa
W	Package weight	4.5		g

NOTES:

1. All dimensions are subject to change.
2. Overall height as delivered. Values were based on design specifications and tolerances. Final height after surface mount depends on OEM motherboard design and SMT process.
3. Dimension for CPUID = 0x06B1.
4. Dimension for CPUID = 0x06B4.

Figure 28. Micro-FCBGA Package – Top and Bottom Isometric Views

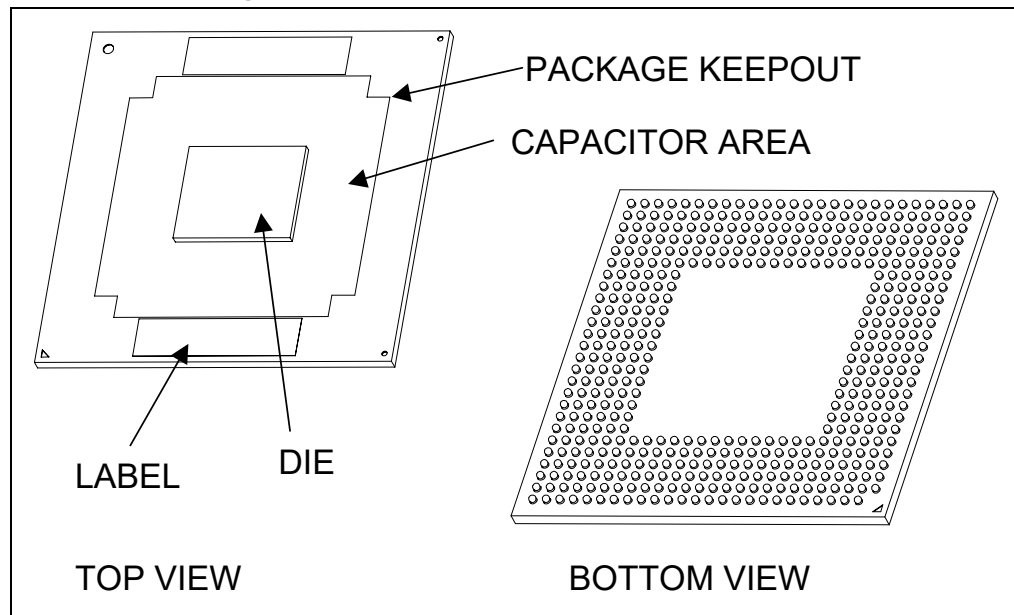


Figure 29. Micro-FCBGA Package – Top and Side Views

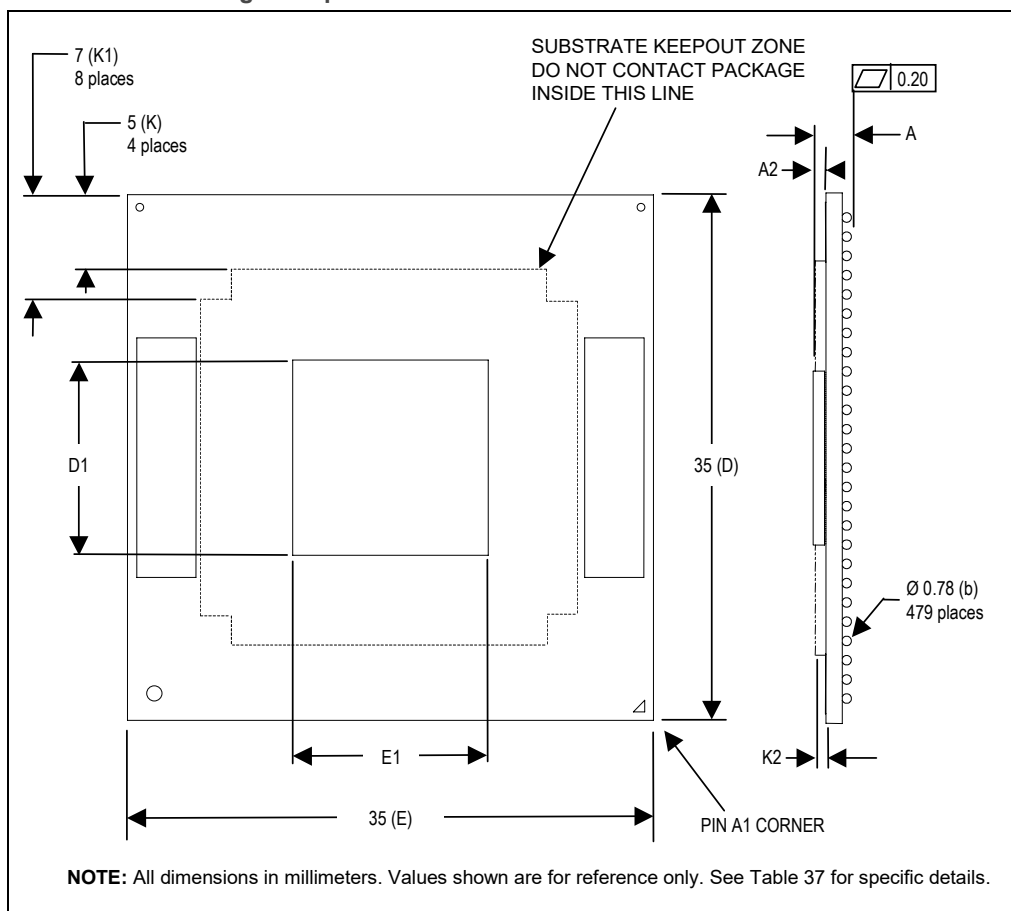
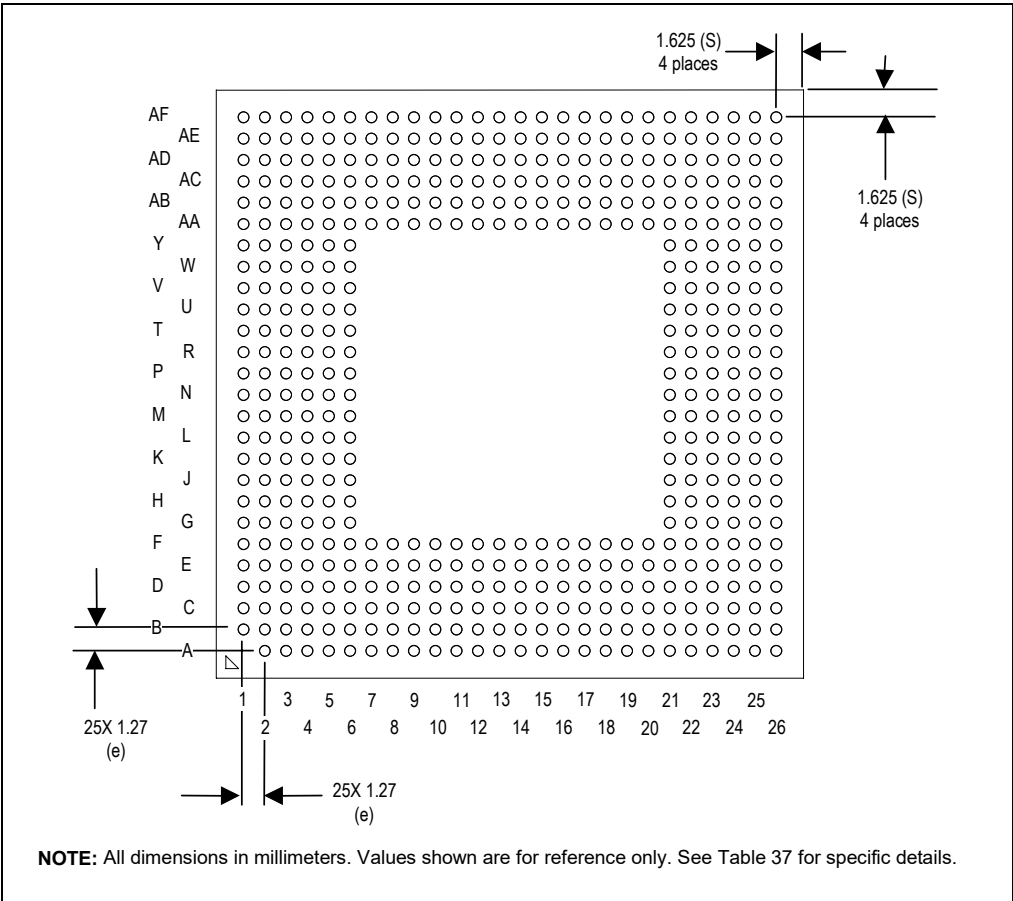




Figure 30. Micro-FCBGA Package - Bottom View



5.3 Signal Listings

Figure 31 is a top-side view of the ball or pin map of the Mobile Intel Celeron Processor with the voltage balls/pins called out. Table 45 lists the signals in ball/pin number order. Table 46 lists the signals in signal name order.

Figure 31. Pin/Ball Map - Top View

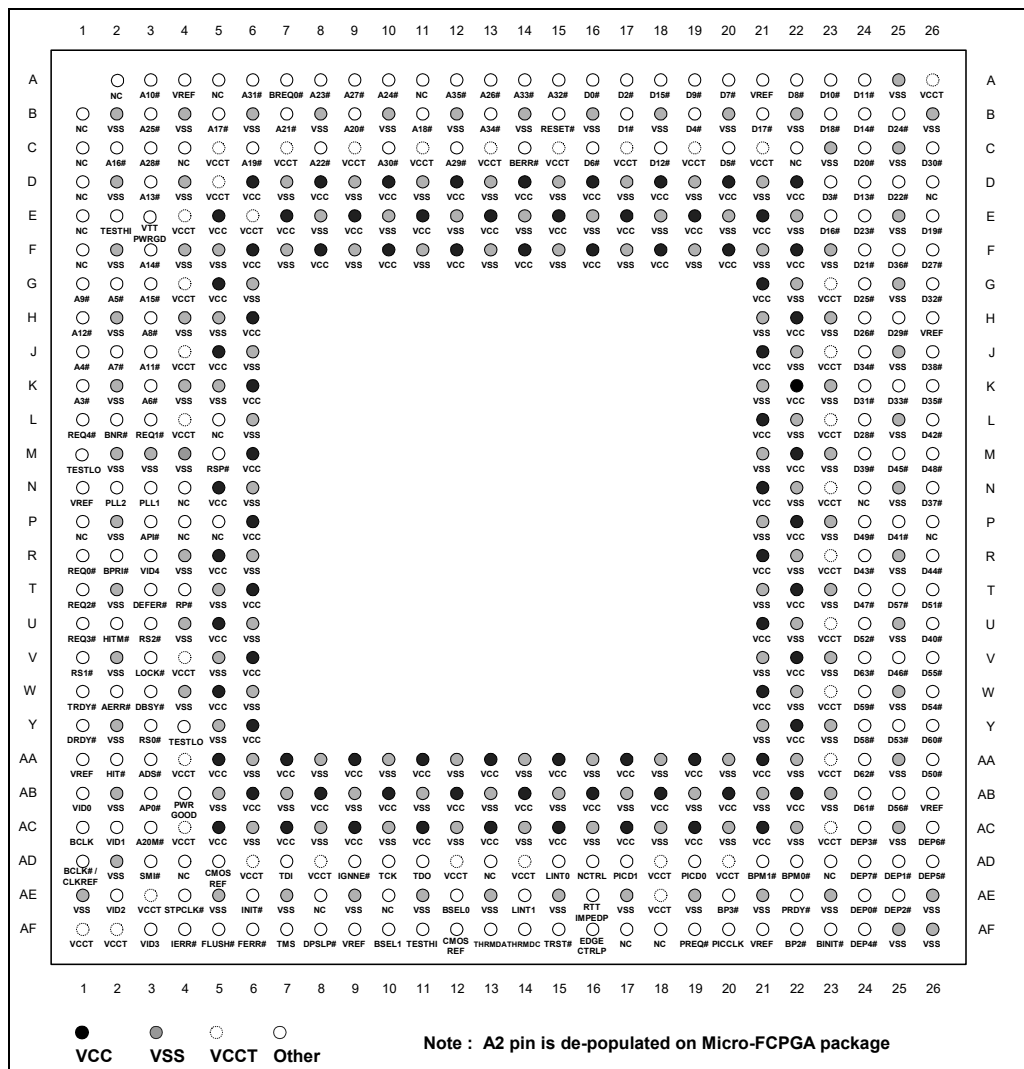


Table 45. Signal Listing in Order by Pin/Ball Number

No.	Signal Name	No.	Signal Name	No.	Signal Name	No.	Signal Name
A3	A10#	B18	VSS	D7	VSS	E22	VSS
A4	VREF	B19	D4#	D8	VCC	E23	D16#
A5	NC	B20	VSS	D9	VSS	E24	D23#
A6	A31#	B21	D17#	D10	VCC	E25	VSS
A7	BREQ0#	B22	VSS	D11	VSS	E26	D19#
A8	A23#	B23	D18#	D12	VCC	F1	NC
A9	A27#	B24	D14#	D13	VSS	F2	VSS
A10	A24#	B25	D24#	D14	VCC	F3	A14#
A11	NC	B26	VSS	D15	VSS	F4	VSS
A12	A35#	C1	NC	D16	VCC	F5	VSS
A13	A26#	C2	A16#	D17	VSS	F6	VCC
A14	A33#	C3	A28#	D18	VCC	F7	VSS
A15	A32#	C4	NC	D19	VSS	F8	VCC
A16	D0#	C5	VCCT	D20	VCC	F9	VSS
A17	D2#	C6	A19#	D21	VSS	F10	VCC
A18	D15#	C7	VCCT	D22	VCC	F11	VSS
A19	D9#	C8	A22#	D23	D3#	F12	VCC
A20	D7#	C9	VCCT	D24	D13#	F13	VSS
A21	VREF	C10	A30#	D25	D22#	F14	VCC
A22	D8#	C11	VCCT	D26	NC	F15	VSS
A23	D10#	C12	A29#	E1	NC	F16	VCC
A24	D11#	C13	VCCT	E2	TESTHI	F17	VSS
A25	VSS	C14	BERR#	E3	VTTTPWRGD	F18	VCC
A26	VCCT	C15	VCCT	E4	VCCT	F19	VSS
B1	NC	C16	D6#	E5	VCC	F20	VCC
B2	VSS	C17	VCCT	E6	VCCT	F21	VSS
B3	A25#	C18	D12#	E7	VCC	F22	VCC
B4	VSS	C19	VCCT	E8	VSS	F23	VSS
B5	A17#	C20	D5#	E9	VCC	F24	D21#
B6	VSS	C21	VCCT	E10	VSS	F25	D36#
B7	A21#	C22	NC	E11	VCC	F26	D27#
B8	VSS	C23	VSS	E12	VSS	G1	A9#
B9	A20#	C24	D20#	E13	VCC	G2	A5#
B10	VSS	C25	VSS	E14	VSS	G3	A15#
B11	A18#	C26	D30#	E15	VCC	G4	VCCT
B12	VSS	D1	NC	E16	VSS	G5	VCC
B13	A34#	D2	VSS	E17	VCC	G6	VSS
B14	VSS	D3	A13#	E18	VSS	G21	VCC
B15	RESET#	D4	VSS	E19	VCC	G22	VSS
B16	VSS	D5	VCCT	E20	VSS	G23	VCCT
B17	D1#	D6	VCC	E21	VCC	G24	D25#

No.	Signal Name	No.	Signal Name	No.	Signal Name	No.	Signal Name
G25	VSS	L4	VCCT	P23	VSS	V2	VSS
G26	D32#	L5	NC	P24	D49#	V3	LOCK#
H1	A12#	L6	VSS	P25	D41#	V4	VCCT
H2	VSS	L21	VCC	P26	NC	V5	VSS
H3	A8#	L22	VSS	R1	REQ0#	V6	VCC
H4	VSS	L23	VCCT	R2	BPRI#	V21	VSS
H5	VSS	L24	D28#	R3	VID4	V22	VCC
H6	VCC	L25	VSS	R4	VSS	V23	VSS
H21	VSS	L26	D42#	R5	VCC	V24	D63#
H22	VCC	M1	TESTLO	R6	VSS	V25	D46#
H23	VSS	M2	VSS	R21	VCC	V26	D55#
H24	D26#	M3	VSS	R22	VSS	W1	TRDY#
H25	D29#	M4	VSS	R23	VCCT	W2	AERR#
H26	VREF	M5	RSP#	R24	D43#	W3	DBSY#
J1	A4#	M6	VCC	R25	VSS	W4	VSS
J2	A7#	M21	VSS	R26	D44#	W5	VCC
J3	A11#	M22	VCC	T1	REQ2#	W6	VSS
J4	VCCT	M23	VSS	T2	VSS	W21	VCC
J5	VCC	M24	D39#	T3	DEFER#	W22	VSS
J6	VSS	M25	D45#	T4	RP#	W23	VCCT
J21	VCC	M26	D48#	T5	VSS	W24	D59#
J22	VSS	N1	VREF	T6	VCC	W25	VSS
J23	VCCT	N2	PLL2	T21	VSS	W26	D54#
J24	D34#	N3	PLL1	T22	VCC	Y1	DRDY#
J25	VSS	N4	NC	T23	VSS	Y2	VSS
J26	D38#	N5	VCC	T24	D47#	Y3	RS0#
K1	A3#	N6	VSS	T25	D57#	Y4	TESTLO
K2	VSS	N21	VCC	T26	D51#	Y5	VSS
K3	A6#	N22	VSS	U1	REQ3#	Y6	VCC
K4	VSS	N23	VCCT	U2	HITM#	Y21	VSS
K5	VSS	N24	NC	U3	RS2#	Y22	VCC
K6	VCC	N25	VSS	U4	VSS	Y23	VSS
K21	VSS	N26	D37#	U5	VCC	Y24	D58#
K22	VCC	P1	NC	U6	VSS	Y25	D53#
K23	VSS	P2	VSS	U21	VCC	Y26	D60#
K24	D31#	P3	API#	U22	VSS	AA1	VREF
K25	D33#	P4	NC	U23	VCCT	AA2	HIT#
K26	D35#	P5	NC	U24	D52#	AA3	ADS#
L1	REQ4#	P6	VCC	U25	VSS	AA4	VCCT
L2	BNR#	P21	VSS	U26	D40#	AA5	VCC
L3	REQ1#	P22	VCC	V1	RS1#	AA6	VSS

No.	Signal Name	No.	Signal Name	No.	Signal Name	No.	Signal Name
AA7	VCC	AB22	VCC	AD11	TDO	AE26	VSS
AA8	VSS	AB23	VSS	AD12	VCCT	AF1	VCCT
AA9	VCC	AB24	D61#	AD13	NC	AF2	VCCT
AA10	VSS	AB25	D56#	AD14	VCCT	AF3	VID3
AA11	VCC	AB26	VREF	AD15	LINT0	AF4	IERR#
AA12	VSS	AC1	BCLK	AD16	NCTRL	AF5	FLUSH#
AA13	VCC	AC2	VID1	AD17	PICD1	AF6	FERR#
AA14	VSS	AC3	A20M#	AD18	VCCT	AF7	TMS
AA15	VCC	AC4	VCCT	AD19	PICD0	AF8	DPSLP#
AA16	VSS	AC5	VCC	AD20	VCCT	AF9	VREF
AA17	VCC	AC6	VSS	AD21	BPM1#	AF10	BSEL1
AA18	VSS	AC7	VCC	AD22	BPM0#	AF11	TESTHI
AA19	VCC	AC8	VSS	AD23	NC	AF12	CMOSREF
AA20	VSS	AC9	VCC	AD24	DEP7#	AF13	THRMDA
AA21	VCC	AC10	VSS	AD25	DEP1#	AF14	THRMDC
AA22	VSS	AC11	VCC	AD26	DEP5#	AF15	TRST#
AA23	VCCT	AC12	VSS	AE1	VSS	AF16	EDGECTRLP
AA24	D62#	AC13	VCC	AE2	VID2	AF17	NC
AA25	VSS	AC14	VSS	AE3	VCCT	AF18	NC
AA26	D50#	AC15	VCC	AE4	STPCLK#	AF19	PREQ#
AB1	VID0	AC16	VSS	AE5	VSS	AF20	PICCLK
AB2	VSS	AC17	VCC	AE6	INIT#	AF21	VREF
AB3	AP0#	AC18	VSS	AE7	VSS	AF22	BP2#
AB4	PWRGOOD	AC19	VCC	AE8	NC	AF23	BINIT#
AB5	VSS	AC20	VSS	AE9	VSS	AF24	DEP4#
AB6	VCC	AC21	VCC	AE10	NC	AF25	VSS
AB7	VSS	AC22	VSS	AE11	VSS	AF26	VSS
AB8	VCC	AC23	VCCT	AE12	BSEL0		
AB9	VSS	AC24	DEP3#	AE13	VSS		
AB10	VCC	AC25	VSS	AE14	LINT1		
AB11	VSS	AC26	DEP6#	AE15	VSS		
AB12	VCC	AD1	BCLK#/CLKREF	AE16	RTTIMPEDP		
AB13	VSS	AD2	VSS	AE17	VSS		
AB14	VCC	AD3	SMI#	AE18	VCCT		
AB15	VSS	AD4	NC	AE19	VSS		
AB16	VCC	AD5	CMOSREF	AE20	BP3#		
AB17	VSS	AD6	VCCT	AE21	VSS		
AB18	VCC	AD7	TDI	AE22	PRDY#		
AB19	VSS	AD8	VCCT	AE23	VSS		
AB20	VCC	AD9	IGNNE#	AE24	DEP0#		
AB21	VSS	AD10	TCK	AE25	DEP2#		

Table 46. Signal Listing in Order by Signal Name

No.	Signal Name	Signal Buffer Type	No.	Signal Name	Signal Buffer Type
K1	A3#	AGTL I/O	AF23	BINIT#	AGTL I/O
J1	A4#	AGTL I/O	L2	BNR#	AGTL I/O
G2	A5#	AGTL I/O	AF22	BP2#	AGTL I/O
K3	A6#	AGTL I/O	AE20	BP3#	AGTL I/O
J2	A7#	AGTL I/O	AD22	BPM0#	AGTL I/O
H3	A8#	AGTL I/O	AD21	BPM1#	AGTL I/O
G1	A9#	AGTL I/O	R2	BPRI#	AGTL Input
A3	A10#	AGTL I/O	A7	BREQ0#	AGTL I/O
J3	A11#	AGTL I/O	AE12	BSEL0	3.3 V CMOS Output
H1	A12#	AGTL I/O	AF10	BSEL1	3.3 V CMOS Output
D3	A13#	AGTL I/O	AD5	CMOSREF	CMOS Reference Voltage
F3	A14#	AGTL I/O	AF12	CMOSREF	CMOS Reference Voltage
G3	A15#	AGTL I/O	A16	D0#	AGTL I/O
C2	A16#	AGTL I/O	B17	D1#	AGTL I/O
B5	A17#	AGTL I/O	A17	D2#	AGTL I/O
B11	A18#	AGTL I/O	D23	D3#	AGTL I/O
C6	A19#	AGTL I/O	B19	D4#	AGTL I/O
B9	A20#	AGTL I/O	C20	D5#	AGTL I/O
B7	A21#	AGTL I/O	C16	D6#	AGTL I/O
C8	A22#	AGTL I/O	A20	D7#	AGTL I/O
A8	A23#	AGTL I/O	A22	D8#	AGTL I/O
A10	A24#	AGTL I/O	A19	D9#	AGTL I/O
B3	A25#	AGTL I/O	A23	D10#	AGTL I/O
A13	A26#	AGTL I/O	A24	D11#	AGTL I/O
A9	A27#	AGTL I/O	C18	D12#	AGTL I/O
C3	A28#	AGTL I/O	D24	D13#	AGTL I/O
C12	A29#	AGTL I/O	B24	D14#	AGTL I/O
C10	A30#	AGTL I/O	A18	D15#	AGTL I/O
A6	A31#	AGTL I/O	E23	D16#	AGTL I/O
A15	A32#	AGTL I/O	B21	D17#	AGTL I/O
A14	A33#	AGTL I/O	B23	D18#	AGTL I/O
B13	A34#	AGTL I/O	E26	D19#	AGTL I/O
A12	A35#	AGTL I/O	C24	D20#	AGTL I/O
AC3	A20M#	1.5V CMOS Input	F24	D21#	AGTL I/O
AA3	ADS#	AGTL I/O	D25	D22#	AGTL I/O
W2	AERR#	AGTL I/O	E24	D23#	AGTL I/O
AB3	AP0#	AGTL I/O	B25	D24#	AGTL I/O
P3	AP1#	AGTL I/O	G24	D25#	AGTL I/O
AC1	BCLK	Clock Input	H24	D26#	AGTL I/O
AD1	BCLK#/CLKREF	Clock Input	F26	D27#	AGTL I/O
C14	BERR#	AGTL I/O	L24	D28#	AGTL I/O

No.	Signal Name	Signal Buffer Type	No.	Signal Name	Signal Buffer Type
H25	D29#	AGTL I/O	AF24	DEP4#	AGTL I/O
C26	D30#	AGTL I/O	AD26	DEP5#	AGTL I/O
K24	D31#	AGTL I/O	AC26	DEP6#	AGTL I/O
G26	D32#	AGTL I/O	AD24	DEP7#	AGTL I/O
K25	D33#	AGTL I/O	Y1	DRDY#	AGTL I/O
J24	D34#	AGTL I/O	AF8	DPSLP#	1.5 V CMOS Input
K26	D35#	AGTL I/O	AF16	EDGECTRLP	AGTL Control
F25	D36#	AGTL I/O	AF6	FERR#	1.5 V Open Drain Output
N26	D37#	AGTL I/O	AF5	FLUSH#	1.5 V CMOS Input
J26	D38#	AGTL I/O	AA2	HIT#	AGTL I/O
M24	D39#	AGTL I/O	U2	HITM#	AGTL I/O
U26	D40#	AGTL I/O	AF4	IERR#	1.5 V Open Drain Output
P25	D41#	AGTL I/O	AD9	IGNNE#	1.5 V CMOS Input
L26	D42#	AGTL I/O	AE6	INIT#	1.5 V CMOS Input
R24	D43#	AGTL I/O	AD15	INTR/LINT0	1.5 V CMOS Input
R26	D44#	AGTL I/O	V3	LOCK#	AGTL I/O
M25	D45#	AGTL I/O	AE14	NMI/LINT1	1.5 V CMOS Input
V25	D46#	AGTL I/O	AD16	NCTRL	AGTL impedance control
T24	D47#	AGTL I/O	AF20	PICCLK	1.8 V APIC Clock Input
M26	D48#	AGTL I/O	AD19	PICD0	1.5 V Open Drain I/O
P24	D49#	AGTL I/O	AD17	PICD1	1.5 V Open Drain I/O
AA26	D50#	AGTL I/O	N3	PLL1	PLL Analog Voltage
T26	D51#	AGTL I/O	N2	PLL2	PLL Analog Voltage
U24	D52#	AGTL I/O	AE22	PRDY#	AGTL Output
Y25	D53#	AGTL I/O	AF19	PREQ#	1.5 V CMOS Input
W26	D54#	AGTL I/O	AB4	PWRGOOD	1.8 V CMOS Input
V26	D55#	AGTL I/O	R1	REQ0#	AGTL I/O
AB25	D56#	AGTL I/O	L3	REQ1#	AGTL I/O
T25	D57#	AGTL I/O	T1	REQ2#	AGTL I/O
Y24	D58#	AGTL I/O	U1	REQ3#	AGTL I/O
W24	D59#	AGTL I/O	L1	REQ4#	AGTL I/O
Y26	D60#	AGTL I/O	B15	RESET#	AGTL Input
AB24	D61#	AGTL I/O	T4	RP#	AGTL I/O
AA24	D62#	AGTL I/O	Y3	RS0#	AGTL I/O
V24	D63#	AGTL I/O	V1	RS1#	AGTL I/O
W3	DBSY#	AGTL I/O	U3	RS2#	AGTL I/O
T3	DEFER#	AGTL Input	M5	RSP#	AGTL Input
AE24	DEP0#	AGTL I/O	AE16	RTTIMPEDP	AGTL Pull-up Control
AD25	DEP1#	AGTL I/O	AD3	SMI#	1.5 V CMOS Input
AE25	DEP2#	AGTL I/O	AE4	STPCLK#	1.5 V CMOS Input
AC24	DEP3#	AGTL I/O			

No.	Signal Name	Signal Buffer Type	No.	Signal Name	Signal Buffer Type
AD10	TCK	1.5V JTAG Clock Input	AC2	VID1	Voltage Identification
AD7	TDI	JTAG Input	AE2	VID2	Voltage Identification
AD11	TDO	JTAG Output	AF3	VID3	Voltage Identification
E2	TESTHI	Test Use Only	R3	VID4	Voltage Identification
AF11	TESTHI	Test Use Only	A4	VREF	AGTL Reference Voltage
M1	TESTLO	Test Use Only	A21	VREF	AGTL Reference Voltage
Y4	TESTLO	Test Use Only	N1	VREF	AGTL Reference Voltage
AF13	THERMDA	Thermal Diode Anode	AF9	VREF	AGTL Reference Voltage
AF14	THERMDC	Thermal Diode Cathode	AF21	VREF	AGTL Reference Voltage
AF7	TMS	JTAG Input	AA1	VREF	AGTL Reference Voltage
W1	TRDY#	AGTL I/O	AB26	VREF	AGTL Reference Voltage
AF15	TRST#	JTAG Input	H26	VREF	AGTL Reference Voltage
AB1	VID0	Voltage Identification	E3	VTTTPWRGD	VCCT power good signal

Table 47. Voltage and No-Connect Pin/Ball Locations

Signal Name	Pin/Ball Numbers
NC	A2, A5, A11, B1, C1, C4, C22, D1, D26, E1, F1, L5, N4, N24, P1, P4, P5, P26, AD4, AD13, AD23, AE8, AE10, AF17, AF18
VCC	D6, D8, D10, D12, D14, D16, D18, D20, D22, E5, E7, E9, E11, E13, E15, E17, E19, E21, F6, F8, F10, F12, F14, F16, F18, F20, F22, G5, G21, H6, H22, J5, J21, K6, K22, L21, M6, M22, N5, N21, P6, P22, R5, R21, T6, T22, U5, U21, V6, V22, W5, W21, Y6, Y22, AA5, AA7, AA9, AA11, AA13, AA15, AA17, AA19, AA21, AB6, AB8, AB10, AB12, AB14, AB16, AB18, AB20, AB22, AC5, AC7, AC9, AC11, AC13, AC15, AC17, AC19, AC21
VCCT	A26, C5, C7, C9, C11, C13, C15, C17, C19, C21, D5, E4, E6, G4, G23, J4, J23, L4, L23, N23, R23, U23, V4, W23, AA4, AA23, AC4, AC23, AD6, AD8, AD12, AD14, AD18, AD20, AE3, AE18, AF1, AF2
VSS	A25, B2, B4, B6, B8, B10, B12, B14, B16, B18, B20, B22, B26, C23, C25, D2, D4, D7, D9, D11, D13, D15, D17, D19, D21, E8, E10, E12, E14, E16, E18, E20, E22, E25, F2, F4, F5, F7, F9, F11, F13, F15, F17, F19, F21, F23, G6, G22, G25, H2, H4, H5, H21, H23, J6, J22, J25, K2, K4, K5, K21, K23, L6, L22, L25, M2, M3, M4, M21, M23, N6, N22, N25, P2, P21, P23, R4, R6, R22, R25, T2, T5, T21, T23, U4, U6, U22, U25, V2, V5, V21, V23, W4, W6, W22, W25, Y2, Y5, Y21, Y23, AA6, AA8, AA10, AA12, AA14, AA16, AA18, AA20, AA22, AA25, AB2, AB5, AB7, AB9, AB11, AB13, AB15, AB17, AB19, AB21, AB23, AC6, AC8, AC10, AC12, AC14, AC16, AC18, AC20, AC22, AC25, AD2, AE1, AE5, AE7, AE9, AE11, AE13, AE15, AE17, AE19, AE21, AE23, AE26, AF25, AF26

NOTE: A2 pin is de-populated on the Micro-FCPGA package.

6. V_{CC} Thermal Specifications

In order to achieve proper cooling of the processor, a thermal solution (e.g., heat spreader, heat pipe, or other heat transfer system) must make firm contact to the exposed processor die. The processor die must be clean before the thermal solution is attached or the processor may be damaged.

Table 48 provides the Thermal Design Power (TDP) dissipation and the minimum and maximum T_J temperatures for the Mobile Intel Celeron Processor. The thermal solution should be designed to ensure the junction temperature never exceeds the specified value while operating at the Thermal Design Power. Additionally, a secondary failsafe mechanism in hardware should be provided to shutdown the processor at 101°C to prevent permanent damage, as described in Section 3.1.3. TDP is a thermal design power specification based on the worst case power dissipation of the processor while executing publicly available software under normal operating conditions at nominal voltages. Contact your Intel Field Sales Representative for further information.

Table 48. Power Specifications for Mobile Intel Celeron Processor

Symbol	Core Frequency/Voltage	Thermal Design Power		Unit	Notes	
TDP	650 MHz & 1.10 V	7.0		W	At 100°C, Note 1	
	700 MHz & 1.10 V	7.0				
	733 MHz & 1.10 V	7.0				
	800 MHz & 1.10V	7.0				
	650 MHz & 1.15 V	10.6		W	At 85°C, Note 4	
	733 MHz & 1.15 V	11.2				
	866 MHz & 1.15 V	9.61				
	1.000 GHz & 1.40 V	22.0				
	1.266 GHz & 1.40 V	22.0				
	1.066 GHz & 1.45 V	23.2				
	1.133 GHz & 1.45 V	23.8				
	1.200 GHz & 1.45 V	24.4				
	1.333 GHz & 1.50 V	19.0				
Symbol	Parameter	Min	Max	Unit	Notes	
P _{AH}	Auto Halt power at			W	At 50°C, Note 2	
	1.10 V		1.9			
	1.15 V		3.6			
	1.40 V		7.0			
	1.45 V		8.2			
P _{QS}	Quick Start power at			W	At 50°C, Note 2	
	1.10 V		1.7			
	1.15 V		3.2			
	1.40 V		6.5			
	1.45 V		7.6			
P _{DSLP}	Deep Sleep power at			W	At 35°C, Note 2	
	1.10 V		1.6			
	1.15 V		2.4			
	1.40 V		4.8			
	1.45 V		5.6			
T _J	1.50 V		6.8	°C	Note 3	
	Junction Temperature					
	For all processors except 1.33 GHz		0			100
	For 1.33 GHz processor only		0			85

NOTES:

1. TDP is defined as the worst case power dissipated by the processor while executing publicly available software under normal operating conditions at nominal voltages that meet the load line specifications. The TDP number shown is a specification based on I_{cc} (maximum) and indirectly tested by I_{cc} (maximum) testing. TDP definition is synonymous with the Thermal Design Power (typical) specification referred to in previous Intel datasheets. The Intel TDP specification is a recommended design point and is not representative of the absolute maximum power the processor may dissipate under worst case conditions.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. T_J is measured with the on-die thermal diode.
4. T_J at 85°C only applies to 1.33 GHz processor. Intel recommends that the notebook thermal management system include full-speed fan activation at no higher than 55°C to provide adequate cooling.

6.1 Thermal Diode

The Mobile Intel Celeron Processor has an on-die thermal diode that should be used to monitor the die temperature (T_J). A thermal sensor located on the motherboard, or a stand-alone measurement kit, should monitor the die temperature of the processor for thermal management or instrumentation purposes. Table 49 and Table 50 provide the diode interface and specifications.

Note: The reading of the thermal sensor connected to the thermal diode will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time based variations in the die temperature measurement. Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the T_J temperature can change.

Table 49. Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
THERMDA	AF13	Thermal diode anode
THERMDC	AF14	Thermal diode cathode

Table 50. Thermal Diode Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
n	Diode Ideality Factor (5-150uA)	1.0011	1.0067	1.0122		Notes 1, 2, 3, 4, 6
n	Diode Ideality Factor (5-300uA)	1.0003	1.0091	1.0178		Notes 1, 2, 3, 5, 6

NOTES:

- Intel does not support or recommend operation of the thermal diode under reverse bias. Intel does not support or recommend operation of the thermal diode when the processor power supplies are not within their specified tolerance range.
- Characterized at 100°C.
- Not 100% tested. Specified by design/characterization.
- Specified for Forward Bias Current = 5 μA (min) and 150 μA (max).
- Specified for Forward Bias Current = 5 μA (min) and 300 μA (max).
- The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:
Where I_s = saturation current, q = electronic charge, V_d = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).

$$I_{FW} = I_s \cdot \left(e^{\frac{qV_d}{nkT}} - 1 \right)$$

7. Processor Initialization and Configuration

7.1 Description

The Mobile Intel Celeron Processor has some configuration options that are determined by hardware and some that are determined by software. The processor samples its hardware configuration at reset on the active-to-inactive transition of RESET#. The *P6 Family of Processors Developer's Manual* describes these configuration options. Some of the configuration options for the Mobile Intel Celeron Processor are described in the remainder of this section.

7.1.1 Quick Start Enable

Quick Start enabling is mandatory on the Mobile Intel Celeron Processor by strapping A15# low. When the STPCLK# signal is asserted it will enter the Quick Start state when A15# is sampled active on the RESET# signal's active-to-inactive transition. The Quick Start state supports snoops from the bus priority device but it does not support symmetric master snoops nor is the latching of interrupts supported. A "1" in bit position 5 of the Power-on Configuration register indicates that the Quick Start state has been enabled.

7.1.2 System Bus Frequency

The current generation Mobile Intel Celeron Processor will only function with a system bus frequency of 133 MHz. The Low Voltage and Ultra Low Voltage Mobile Intel Celeron Processors will support both 100-MHz and 133-MHz bus frequencies. Bit positions 18 to 19 of the Power-on Configuration register indicates at which speed a processor will run.

7.1.3 APIC Enable

The processor APIC must be hardware enabled by pulling the PICD[1:0] signals separately up to 1.5 V and supplying an active PICCLK to the processor. Software can be used to disable the APIC if it is not being used, after PICD[1:0] are sampled high when RESET# is deasserted and the processor has started executing instructions.

7.2 Clock Frequencies and Ratios

The Mobile Intel Celeron Processor uses a clock design in which the bus clock is multiplied by a ratio to produce the processor's internal (or "core") clock. The ratio used is programmed into the processor during manufacturing. The bus ratio programmed into the processor is visible in bit positions 22 to 25 and 27 of the Power-on Configuration register. Table 28 shows the 5-bit codes in the Power-on Configuration register and their corresponding bus ratios.

8. Processor Interface

8.1 Alphabetical Signal Reference

A[35:3]# (I/O – AGTL)

The A[35:3]# (Address) signals define a 2^{36} -byte physical memory address space. When ADS# is active, these signals transmit the address of a transaction; when ADS# is inactive, these signals transmit transaction information. These signals must be connected to the appropriate pins/balls of both agents on the system bus. The A[35:24]# signals are protected with the AP1# parity signal, and the A[23:3]# signals are protected with the AP0# parity signal.

On the active-to-inactive transition of RESET#, each processor bus agent samples A[35:3]# signals to determine its power-on configuration. See *P6 Family of Processors Developer's Manual* for details.

A20M# (I - 1.5V Tolerant)

If the A20M# (Address-20 Mask) input signal is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in Real mode.

ADS# (I/O - AGTL)

The ADS# (Address Strobe) signal is asserted to indicate the validity of a transaction address on the A[35:3]# signals. Both bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop or deferred reply ID match operations associated with the new transaction. This signal must be connected to the appropriate pins/balls on both agents on the system bus.

AERR# (I/O - AGTL)

The AERR# (Address Parity Error) signal is observed and driven by both system bus agents, and if used, must be connected to the appropriate pins/balls of both agents on the system bus. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction.

If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the error handling architecture of the system.

AP[1:0]# (I/O - AGTL)

The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:3]#, REQ[4:0]# and RP#. AP1# covers A[35:24]#. AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals is low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should be connected to the appropriate pins/balls on both agents on the system bus.

BCLK, BCLK# (I)

The BCLK and BCLK# signals determines the system bus frequency.

On systems with Differential Clocking, both system bus agents must receive these signals to drive their outputs and latch their inputs on the BCLK rising edge and BCLK# falling edge. All external timing parameters are specified with respect to the crossing point of the BCLK rising edge and BCLK# falling edge.

On systems with Single Ended Clocking, both system bus agents must receive the BCLK signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal. The BCLK# signal functions as the CLKREF input.

BERR# (I/O - AGTL)

The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by either system bus agent and must be connected to the appropriate pins/balls of both agents, if used. However, the Mobile Intel Celeron Processors do not observe assertions of the BERR# signal.

BERR# assertion conditions are defined by the system configuration. Configuration options enable the BERR# driver as follows:

- Enabled or disabled
- Asserted optionally for internal errors along with IERR#
- Asserted optionally by the request initiator of a bus transaction after it observes an error
- Asserted by any bus agent when it observes an error in a bus transaction

BINIT# (I/O - AGTL)

The BINIT# (Bus Initialization) signal may be observed and driven by both system bus agents and must be connected to the appropriate pins/balls of both agents, if used. If the BINIT# driver is enabled during the power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information.

If BINIT# is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after reset, and internal count information is lost. The L1 and L2 caches are not affected.

If BINIT# is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the Machine Check Architecture (MCA) of the system.

BNR# (I/O - AGTL)

The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

Since multiple agents may need to request a bus stall simultaneously, BNR# is a wired-OR signal that must be connected to the appropriate pins/balls of both agents on the system bus. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.

BP[3:2]# (I/O - AGTL)

The BP[3:2]# (Breakpoint) signals are the System Support group Breakpoint signals. They are outputs from the processor that indicate the status of breakpoints.

BPM[1:0]# (I/O - AGTL)

The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

BPRI# (I - AGTL)

The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the system bus. It must be connected to the appropriate pins/balls on both agents on the system bus. Observing BPRI# active (as asserted by the priority agent) causes the processor to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed and then releases the bus by deasserting BPRI#.

BREQ0# (I/O - AGTL)

The BREQ0# (Bus Request) signal is a processor Arbitration Bus signal. The processor indicates that it wants ownership of the system bus by asserting the BREQ0# signal.

During power-up configuration, the central agent must assert the BREQ0# bus signal. The processor samples BREQ0# on the active-to-inactive transition of RESET#. Optionally, this signal may be grounded with a 10-ohm resistor.

BSEL[1:0] (O – 3.3V Tolerant)

The BSEL[1:0] (Select Processor System Bus Speed) signal is used to configure the processor for the system bus frequency. The chipset and system clock generator also uses the BSEL signals. The VTTPWRGD signal informs the processor to output the BSEL signals. During power up the BSEL signals will be indeterminate for a small period of time. The chipset and clock generator should not sample the BSEL signals until the VTTPWRGD signal is asserted. The assertion of the VTTPWRGD signal indicates that the BSEL signals are stable and driven to a final state by the processor. Please refer to Figure 15 for the timing relationship between the BSEL and VTTPWRGD signals.

Table 51 shows the encoding scheme for BSEL[1:0]. The only supported system bus frequency for the Mobile Intel Celeron Processor is 133 MHz. The Low Voltage and Ultra Low Voltage Mobile Intel Celeron Processors will support both 100-MHz and 133-MHz bus frequencies. If another frequency is used then the processor is not guaranteed to function properly.

Table 51. BSEL[1:0] Encoding

BSEL[1:0]	System Bus Frequency
01	100 MHz
11	133 MHz

CLKREF (Analog)

The CLKREF (System Bus Clock Reference) signal provides a reference voltage to define the trip point for the BCLK signal on platforms supporting Single Ended Clocking. This signal should be connected to

a resistor divider to generate 1.25 V from the 2.5-V supply. A minimum of 1- μ F decoupling capacitance is recommended on CLKREF. On systems with Differential Clocking, the CLKREF pin functions as the BCLK# input.

CMOSREF (Analog)

The CMOSREF (CMOS Reference Voltage) signal provides a DC level reference voltage for the CMOS input buffers. CMOSREF must be generated from a stable 1.5V supply (830 chipset family), 2.5 V (440MX chipset family) and must meet the VCMOSREF specification. The same 1.5 V (830 chipset family) or 2.5 V (440MX chipset family) supply should be used to power the chipset CMOS I/O buffers that drive the CMOS signals. The Thevenin equivalent impedance of the VCMOSREF generation circuits must be less than 0.5 K Ω /1 K Ω (i.e., top resistor 500 Ω , bottom resistor 1 K Ω) for the Intel 830 Chipset family. The Thevenin equivalent impedance of the VCMOSREF generation circuits must be less than 0.75 K Ω /0.5 K Ω (i.e., top resistor 750 Ω , bottom resistor 500 Ω) for the Intel 440MX chipset family.

D[63:0]# (I/O - AGTL)

The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between both system bus agents, and must be connected to the appropriate pins/balls on both agents. The data driver asserts DRDY# to indicate a valid data transfer.

DBSY# (I/O - AGTL)

The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must be connected to the appropriate pins/balls on both agents on the system bus.

DEFER# (I - AGTL)

The DEFER# (Defer) signal is asserted by an agent to indicate that the transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory agent or I/O agent. This signal must be connected to the appropriate pins/balls on both agents on the system bus.

DEP[7:0]# (I/O - AGTL)

The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and must be connected to the appropriate pins/balls on both agents on the system bus if they are used. During power-on configuration, DEP[7:0]# signals can be enabled for ECC checking or disabled for no checking.

DRDY# (I/O - AGTL)

The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# can be deasserted to insert idle clocks. This signal must be connected to the appropriate pins/balls on both agents on the system bus.

DPSLP# (I - 1.5 V Tolerant)

The DPSLP# (Deep Sleep) signal, when asserted in the Quick Start state, causes the processor to enter the Deep Sleep state. In order to return to the Quick Start state BCLK, BCLK# must be running and the DPSLP# pin must be deasserted.

EDGCTRLP (I-Analog)

The EDGCTRLP (Edge Rate Control) signal is used to configure the edge rate of the AGTL output buffers. Connect the signal to V_{SS} with a 110- Ω , 1% resistor.

FERR# (O - 1.5 V Tolerant Open-drain)

The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and it is included for compatibility with systems using DOS-type floating-point error reporting.

FLUSH# (I - 1.5 V Tolerant)

When the FLUSH# (Flush) input signal is asserted, the processor writes back all internal cache lines in the Modified state and invalidates all internal cache lines. At the completion of a flush operation, the processor issues a Flush Acknowledge transaction. The processor stops caching any new data while the FLUSH# signal remains asserted.

On the active-to-inactive transition of RESET#, each processor bus agent samples FLUSH# to determine its power-on configuration.

HIT# (I/O - AGTL), HITM# (I/O - AGTL)

The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must be connected to the appropriate pins/balls on both agents on the system bus. Either bus agent can assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.

IERR# (O - 1.5 V Tolerant Open-drain)

The IERR# (Internal Error) signal is asserted by the processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system logic. The processor will keep IERR# asserted until it is handled in software or with the assertion of RESET#, BINIT, or INIT#.

IGNNE# (I - 1.5 V Tolerant)

The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor freezes on a non-control floating-point instruction if a previous instruction caused an error. IGNNE# has no affect when the NE bit in control register 0 (CR0) is set.

INIT# (I - 1.5 V Tolerant)

The INIT# (Initialization) signal is asserted to reset integer registers inside the processor without affecting the internal (L1 or L2) caches or the floating-point registers. The processor begins execution at the power-on reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous input.

If INIT# is sampled active on RESET#'s active-to-inactive transition, then the processor executes its built-in self-test (BIST).

INTR (I - 1.5 V Tolerant)

The INTR (Interrupt) signal indicates that an external interrupt has been generated. INTR becomes the LINT0 signal when the APIC is enabled. The interrupt is maskable using the IF bit in the EFLAGS register. If the IF bit is set, the processor vectors to the interrupt handler after completing the current instruction execution. Upon recognizing the interrupt request, the processor issues a single Interrupt Acknowledge (INTA) bus transaction. INTR must remain active until the INTA bus transaction to guarantee its recognition.

LINT[1:0] (I - 1.5 V Tolerant)

The LINT[1:0] (Local APIC Interrupt) signals must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC component. When APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the same signals for the Pentium processor. Both signals are asynchronous inputs.

Both of these signals must be software configured by programming the APIC register space to be used either as NMI/INTR or LINT[1:0] in the BIOS. If the APIC is enabled at reset, then LINT[1:0] is the default configuration.

LOCK# (I/O - AGTL)

The LOCK# (Lock) signal indicates to the system that a sequence of transactions must occur atomically. This signal must be connected to the appropriate pins/balls on both agents on the system bus. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction through the end of the last transaction.

When the priority agent asserts BPRI# to arbitrate for bus ownership, it waits until it observes LOCK# deasserted. This enables the processor to retain bus ownership throughout the bus locked operation and guarantee the atomicity of lock.

NCTRL (I - Analog)

The NCTRL signal provides the AGTL pull down impedance control. The processor samples this input to determine the N-channel pull-down device strength when it is the driving agent. An external 14 ohm (1% tolerance) pull-up resistor to V_{CCT} is required for this signal. Please refer to platform design guide for implementation details.

NMI (I - 1.5 V Tolerant)

The NMI (Non-Maskable Interrupt) indicates that an external interrupt has been generated. NMI becomes the LINT1 signal when the APIC is disabled. Asserting NMI causes an interrupt with an internally supplied vector value of 2. An external interrupt-acknowledge transaction is not generated. If NMI is asserted during the execution of an NMI service routine, it remains pending and is recognized after the IRET is executed by the NMI service routine. At most, one assertion of NMI is held pending. NMI is rising edge sensitive.

PICCLK (I – 2.0 V Tolerant)

The PICCLK (APIC Clock) signal is an input clock to the processor and system logic or I/O APIC that is required for operation of the processor, system logic, and I/O APIC components on the APIC bus.

PICD[1:0] (I/O - 1.5 V Tolerant Open-drain)

The PICD[1:0] (APIC Data) signals are used for bi-directional serial message passing on the APIC bus. They must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC components. If the PICD0 signal is sampled low on the active-to-inactive transition of the RESET# signal, then the APIC is hardware disabled. For the Mobile Intel Celeron Processor, the APIC is required to be hardware enabled as described in Section 7.1.3.

PLL1, PLL2 (Analog)

The PLL1 and PLL2 signals provide isolated analog decoupling is required for the internal PLL. See Section 3.2.2 for a description of the analog decoupling circuit.

PRDY# (O - AGTL)

The PRDY# (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.

PREQ# (I - 1.5 V Tolerant)

The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processor.

PWRGOOD (I – 1.8 V Tolerant)

PWRGOOD (Power Good) is a 1.8-V tolerant input. The processor requires this signal to be a clean indication that clocks and the power supplies (V_{CC} , V_{CCT} , etc.) are stable and within their specifications. Clean implies that the signal will remain low, (capable of sinking leakage current) and without glitches, from the time that the power supplies are turned on, until they come within specification. The signal will then transition monotonically to a high (1.8 V) state. Figure 15 through Figure 17 illustrate the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before the rising edge of PWRGOOD. It must also meet the minimum pulse width specified in Table 30 (Section 3.6) and be followed by a 1 ms RESET# pulse.

The PWRGOOD signal, which must be supplied to the processor, is used to protect internal circuits against voltage sequencing issues. The PWRGOOD signal should be driven high throughout boundary scan operation.

REQ[4:0]# (I/O - AGTL)

The REQ[4:0]# (Request Command) signals must be connected to the appropriate pins/balls on both agents on the system bus. They are asserted by the current bus owner when it drives A[35:3]# to define the currently active transaction type.

RESET# (I - AGTL)

Asserting the RESET# signal resets the processor to a known state and invalidates the L1 and L2 caches without writing back Modified (M state) lines. For a power-on type reset, RESET# must stay active for at least 1 ms after V_{CC} and BCLK, BCLK# have reached their proper DC and AC specifications and after PWRGOOD has been asserted. When observing active RESET#, all bus agents will deassert their outputs within two clocks. RESET# is the only AGTL signal that does not have on-die AGTL termination. A 56.2 Ω 1% terminating resistor connected to V_{CCT} is required.

A number of bus signals are sampled at the active-to-inactive transition of RESET# for the power-on configuration. The configuration options are described in Section 4 and in the *P6 Family of Processors Developer's Manual*.

Unless its outputs are tri-stated during power-on configuration, after an active-to-inactive transition of RESET#, the processor optionally executes its built-in self-test (BIST) and begins program execution at reset-vector 000FFFF0H or FFFFFFF0H. RESET# must be connected to the appropriate pins/balls on both agents on the system bus.

RP# (I/O - AGTL)

The RP# (Request Parity) signal is driven by the request initiator and provides parity protection on ADS# and REQ[4:0]#. RP# should be connected to the appropriate pins/balls on both agents on the system bus.

A correct parity signal is high if an even number of covered signals is low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.

RS[2:0]# (I/O - AGTL)

The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction) and must be connected to the appropriate pins/balls on both agents on the system bus.

RSP# (I - AGTL)

The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#. RSP# provides parity protection for RS[2:0]#. RSP# should be connected to the appropriate pins/balls on both agents on the system bus.

A correct parity signal is high if an even number of covered signals are low, and it is low if an odd number of covered signals are low. During Idle state of RS[2:0]# (RS[2:0]#=000), RSP# is also high since it is not driven by any agent guaranteeing correct parity.

RTTIMPEDP (I-Analog)

The RTTIMPEDP (R_{TT} Impedance/PMOS) signal is used to configure the on-die AGTL termination. Connect the RTTIMPEDP signal to V_{SS} with a 56.2- Ω , 1% resistor.

SMI# (I - 1.5 V Tolerant)

The SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.

STPCLK# (I - 1.5 V Tolerant)

The STPCLK# (Stop Clock) signal, when asserted, causes the processor to enter a low-power Quick Start state. The processor issues a Stop Grant Acknowledge special transaction and stops providing internal clock signals to all units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in the Quick Start state. When STPCLK# is deasserted and

other conditions in are met, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no affect on the bus clock.

TCK (I - 1.5 V Tolerant)

The TCK (Test Clock) signal provides the clock input for the test bus (also known as the test access port).

TDI (I - 1.5 V Tolerant)

The TDI (Test Data In) signal transfers serial test data to the processor. TDI provides the serial input needed for JTAG support.

TDO (O - 1.5 V Tolerant Open-drain)

The TDO (Test Data Out) signal transfers serial test data from the processor. TDO provides the serial output needed for JTAG support.

TESTHI[2:1] (I - 1.25 V Tolerant)

The TESTHI[2:1] (Test input High) signals are used during processor test and need to be pulled high during normal operation.

TESTLO[2:1] (I - 1.5 V Tolerant)

The TESTLO[2:1] (Test input Low) signals are used during processor test and needs to be pulled to ground during normal operation.

THERMDA, THERMDC (Analog)

The THERMDA (Thermal Diode Anode) and THERMDC (Thermal Diode Cathode) signals connect to the anode and cathode of the on-die thermal diode.

TMS (I - 1.5 V Tolerant)

The TMS (Test Mode Select) signal is a JTAG support signal used by debug tools.

TRDY# (I/O - AGTL)

The TRDY# (Target Ready) signal is asserted by the target to indicate that the target is ready to receive write or implicit write-back data transfer. TRDY# must be connected to the appropriate pins/balls on both agents on the system bus.

TRST# (I - 1.5 V Tolerant)

The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. The Mobile Intel Celeron Processors do not self-reset during power on; therefore, it is necessary to drive this signal low during power-on reset.

VID[4:0] (O – Open-drain)

The VID[4:0] (Voltage ID) pins/balls can be used to support automatic selection of power supply voltages. Please refer to Section 3.2.3 for details.

VREF (Analog)

The VREF (AGTL Reference Voltage) signal provides a DC level reference voltage for the AGTL input buffers. A voltage divider should be used to divide V_{CCT} by $2/3$. Resistor values of 1.00 k Ω and 2.00 k Ω are recommended. Decouple the VREF signal with three 0.1- μ F high-frequency capacitors close to the processor.

VTPWRGD (I – 1.25 V)

The VTPWRGD signal informs the processor to output the VID signals. During power up, the VID signals will be in an indeterminate state for a small period of time. The voltage regulator should not sample and/or latch the VID signals until the VTPWRGD signal is asserted. The assertion of the VTPWRGD signal indicates that the VID signals are stable and are driven to the final state by the processor. Please refer to Figure 15 for the power up sequence. (Also see Section 4.3.1.)

8.2 Signal Summaries

Table 52. Input Signals

Name	Active Level	Clock	Signal Group	Qualified
A20M#	Low	Asynch	CMOS	Always
BCLK	High	—	System Bus	Always
BCLK#	Low	—	System Bus	Always
BPRI#	Low	BCLK	System Bus	Always
DEFER#	Low	BCLK	System Bus	Always
FLUSH#	Low	Asynch	CMOS	Always
IGNNE#	Low	Asynch	CMOS	Always
INIT#	Low	Asynch	System Bus	Always
INTR	High	Asynch	CMOS	APIC disabled mode
LINT[1:0]	High	Asynch	APIC	APIC enabled mode
NMI	High	Asynch	CMOS	APIC disabled mode
NCTRL	High	Asynch		
PICCLK	High	—	APIC	Always
PREQ#	Low	Asynch	Implementation	Always
PWRGOOD	High	Asynch	Implementation	Always
RESET#	Low	BCLK	System Bus	Always
RSP#	Low	BCLK	System Bus	Always
SMI#	Low	Asynch	CMOS	Always
STPCLK#	Low	Asynch	Implementation	Always
TCK	High	—	JTAG	
TDI		TCK	JTAG	
TMS		TCK	JTAG	
TRST#	Low	Asynch	JTAG	
VTTTPWRGD	High	Asynch	Power/Other	

Table 53. Output Signals

Name	Active Level	Clock	Signal Group
BSEL[1:0]	High	Asynch	Open-drain
FERR#	Low	Asynch	Open-drain
IERR#	Low	Asynch	Open-drain
PRDY#	Low	BCLK	Implementation
TDO	High	TCK	JTAG
VID[4:0]	High	Asynch	Power/Other

Table 54. Input/Output Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
A[35:3]#	Low	BCLK	System Bus	ADS#, ADS#+1
ADS#	Low	BCLK	System Bus	Always
AP[1:0]#	Low	BCLK	System Bus	ADS#, ADS#+1
BREQ0#	Low	BCLK	System Bus	Always
BP[3:2]#	Low	BCLK	System Bus	Always
BPM[1:0]#	Low	BCLK	System Bus	Always
D[63:0]#	Low	BCLK	System Bus	DRDY#
DBSY#	Low	BCLK	System Bus	Always
DEP[7:0]#	Low	BCLK	System Bus	DRDY#
DRDY#	Low	BCLK	System Bus	Always
LOCK#	Low	BCLK	System Bus	Always
REQ[4:0]#	Low	BCLK	System Bus	ADS#, ADS#+1
RP#	Low	BCLK	System Bus	ADS#, ADS#+1
RS[2:0]#	Low	BCLK	System Bus	Always
TRDY#	Low	BCLK	System Bus	Response phase

Table 55. Input/Output Signals (Multiple Driver)

Name	Active Level	Clock	Signal Group	Qualified
AERR#	Low	BCLK	System Bus	ADS#+3
BERR#	Low	BCLK	System Bus	Always
BINIT#	Low	BCLK	System Bus	Always
BNR#	Low	BCLK	System Bus	Always
HIT#	Low	BCLK	System Bus	Always
HITM#	Low	BCLK	System Bus	Always
PICD[1:0]	High	PICCLK	APIC	Always

Appendix A. PLL RLC Filter Specification

A1. Introduction

All Mobile Intel Celeron Processors have internal PLL clock generators, which are analog in nature and require quiet power supplies for minimum jitter. Jitter is detrimental to a system; it degrades external I/O timings as well as internal core timings (i.e. maximum frequency). The PLL RLC filter specifications for the Mobile Intel Celeron Processor are the same as those for the mobile Intel Pentium III Processor-M. The general desired topology is shown in Figure 2. Excluded from the external circuitry are parasitics associated with each component.

A2. Filter Specification

The function of the filter is two fold. It protects the PLL from external noise through low-pass attenuation. It also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter.

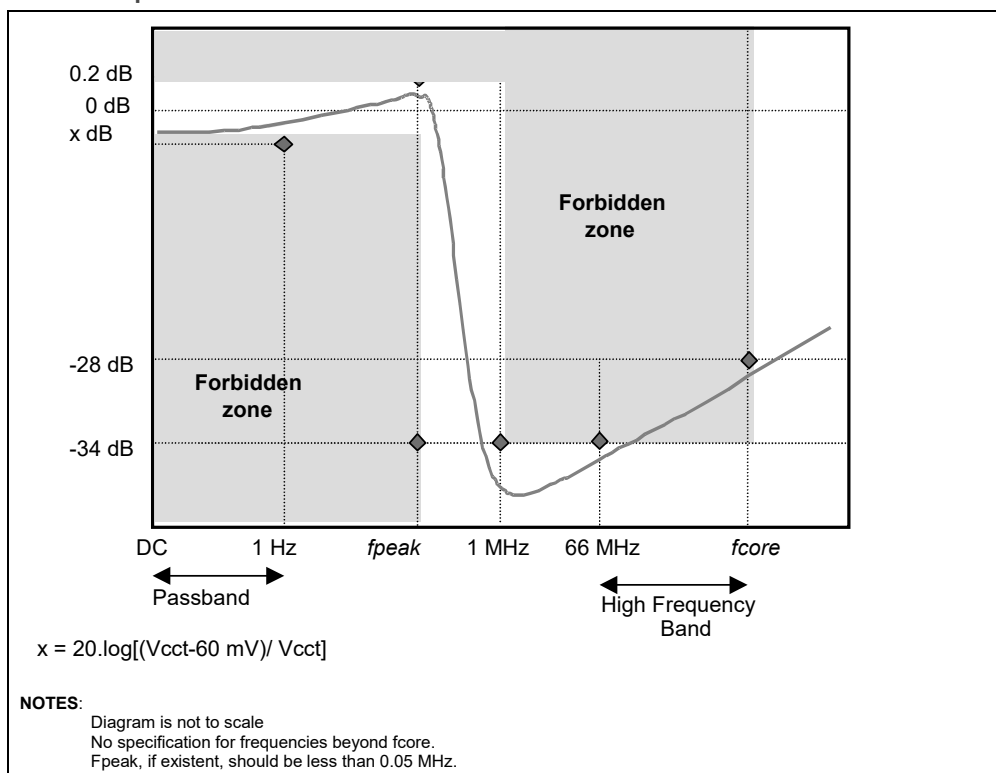
The AC low-pass specification, with input at V_{CCT} and output measured across the capacitor, is as follows:

- < 0.2-dB gain in pass band
- < 0.5-dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- 34-dB attenuation from 1 MHz to 66 MHz
- 28-dB attenuation from 66 MHz to core frequency
- The filter specification (AC) is graphically shown in Figure 32.

Other requirements:

- Use a shielded type inductor to minimize magnetic pickup
- The filter should support a DC current of at least 30 mA
- The DC voltage drop from V_{CCT} to PLL1 should be less than 60 mV, which in practice implies series resistance of less than 2 Ω . This also means that the pass band (from DC to 1 Hz) attenuation below 0.43 dB for $V_{CCT} = 1.25$ V.

Figure 32. PLL Filter Specifications



A3. Recommendation for Mobile Systems

The following LC components are recommended. The tables will be updated as other suitable components and specifications are identified.

Table 56. PLL Filter Inductor Recommendations

Inductor	Part Number	Value	Tol	SRF	Rated I	DCR	Min Damping R Needed
L1	TDK MLF2012A4R7KT	4.7 μ H	10%	35 MHz	30 mA	0.56 Ω (1 Ω max)	0 Ω
L2	Murata LQG21N4R7K10	4.7 μ H	10%	47 MHz	30 mA	0.7 Ω (+/-50%)	0 Ω
L3	Murata LQG21C4R7N00	4.7 μ H	30%	35 MHz	30 mA	0.3 Ω max	0.2 Ω (assumed)

NOTE: Minimum damping resistance is calculated from $0.35 \Omega - DCR_{min}$. From vendor provided data, L1 and L2 DCR_{min} is 0.4 Ω and 0.5 Ω respectively, qualifying them for zero required trace resistance. DCR_{min} for L3 is not known and is assumed to be 0.15 Ω . Products with equivalent specifications may also be used.

Table 57. PLL Filter Capacitor Recommendations

Capacitor	Part Number	Value	Tolerance	ESL	ESR
C1	Kemet T495D336M016AS	33 μ F	20%	2.5 nH	0.225 Ω
C2	AVX TPSD336M020S0200	33 μ F	20%	unknown	0.2 Ω

Table 58. PLL Filter Resistor Recommendations

Resistor	Part Number	Value	Tolerance	Power
R1	Various	1 Ω	10%	1/16W

To satisfy damping requirements, total series resistance in the filter (from V_{CCT} to the top plate of the capacitor) must be at least 0.35 Ω . This resistor can be in the form of a discrete component, or routing, or both. For example, if the picked inductor has minimum DCR of 0.25 Ω , then a routing resistance of at least 0.10 Ω is required. Be careful not to exceed the maximum resistance rule (2 Ω). For example, if using discrete R1, the maximum DCR of the L should be less than $2.0 - 1.1 = 0.9 \Omega$, which precludes using L2 and possibly L1.

Other routing requirements include:

- The capacitor should be close to the PLL1 and PLL2 pins, with less than 0.1 Ω per route (These routes do not count towards the minimum damping resistance requirement).
- The PLL2 route should be parallel and next to the PLL1 route (minimize loop area).
- The inductor should be close to the capacitor; any routing resistance should be inserted between V_{CCT} and the inductor.
- Any discrete resistor should be inserted between V_{CCT} and the inductor.

A4. Comments

- A magnetically shielded inductor protects the circuit from picking up external flux noise. This should provide better timing margins than with an unshielded inductor.
- A discrete or routed resistor is required because the LC filter by nature has an under-damped response, which can cause resonance at the LC pole. Noise amplification at this band, although not in the PLL-sensitive spectrum, could cause a fatal headroom reduction for analog circuitry. The resistor serves to dampen the response. Systems with tight space constraints should consider a discrete resistor to provide the required damping resistance. Too large of a damping resistance can cause a large IR drop, which means less analog headroom and lower frequency.
- Ceramic capacitors have very high self-resonance frequencies, but they are not available in large capacitance values. A high self-resonant frequency coupled with low ESL/ESR is crucial for sufficient rejection in the PLL and high frequency band. The recommended tantalum capacitors have acceptably low ESR and ESL.
- The capacitor must be close to the PLL1 and PLL2 pins; otherwise the value of the low ESR tantalum capacitor is wasted. Note the distance constraint should be translated from the 0.1- Ω requirement.

APPENDIX INTEL2003-03



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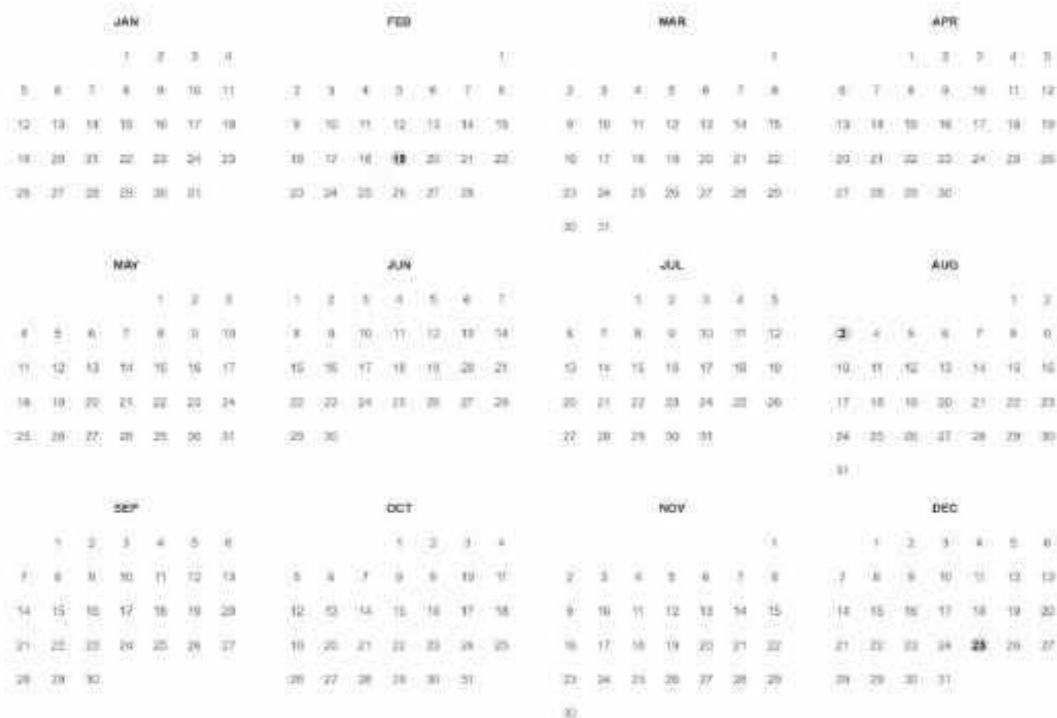
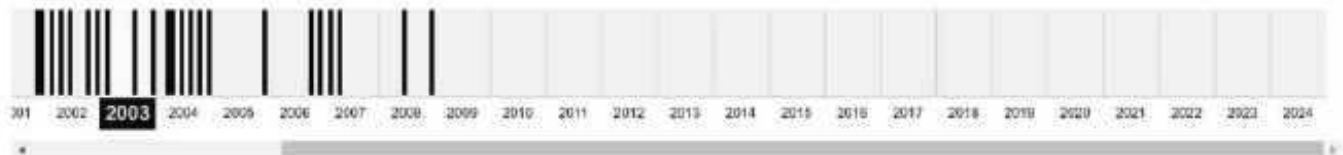
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Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages at 1.33 GHz, 1.26 GHz, 1.20 GHz, 1.13 GHz, 1.06 GHz, 1.00 GHz; Low Voltage 733 MHz, 650 MHz; and Ultra Low Voltage 733 MHz, 700 MHz, 667 MHz, and 650 MHz

Using Intel's advanced 0.13-micron process technology with copper interconnect, the Mobile Intel® Celeron® Processor offers high-performance and low-power consumption. The Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA packages (hereafter referred to as "the Mobile Intel® Celeron® Processor") is based on the same core as existing mobile Intel® Pentium® III Processor-M. Key performance features include Intel® Streaming SIMD instructions, an Advanced Transfer Cache architecture, and a processor system bus speed of 133 MHz. The Low Voltage and Ultra Low Voltage Mobile Intel® Celeron® Processors will support both a 133-MHz and 100-MHz bus speed. These features are offered in Micro-FCPGA packages for socketable boards and Micro-FCBGA packages for surface mount boards. The Low Voltage and Ultra Low Voltage Mobile processors will be available only in the Micro-FCBGA package. The Mobile Intel® Celeron® processors at 1.45 V and at 1.50 V are available only in the Micro-FCPGA package. All of these technologies make outstanding performance possible for mobile PCs in a variety of shapes and sizes.

The 256-KB integrated L2 cache based on the Advanced Transfer Cache architecture runs at full speed and is designed to help improve performance. It complements the system bus by providing critical data faster and reducing total system power consumption. The processor also features Data Prefetch Logic that speculatively fetches data to the L2 cache, resulting in improved performance. The Mobile Intel® Celeron® Processor's 64-bit wide Assisted Gunning Transceiver Logic (AGTL) system bus provides a glue-less, point-to-point interface for a memory controller hub.

This document covers the electrical, mechanical, and thermal specifications for the following:

- The Mobile Intel® Celeron® Processor at the following frequencies and voltages: 1.33 GHz at 1.50 V; 1.2 GHz; 1.13 GHz; 1.06 GHz at 1.45 V; and 1.26 GHz; 1 GHz at 1.40 V.
- The Low Voltage Mobile Intel® Celeron® Processor at the following frequencies and voltages: 666 MHz, 733 MHz and 650 MHz at 1.15 V.
- The Ultra Low Voltage Mobile Intel® Celeron® Processor at the following frequencies and voltages: 600 MHz, 733 MHz, 700 MHz, 667 MHz and 650 MHz at 1.10 V.
- Unless explicitly stated, all references to the Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA packages in this document also apply to the Low Voltage and Ultra Low Voltage Mobile Intel® Celeron® Processor (0.13 μ) in the Micro-FCBGA package.

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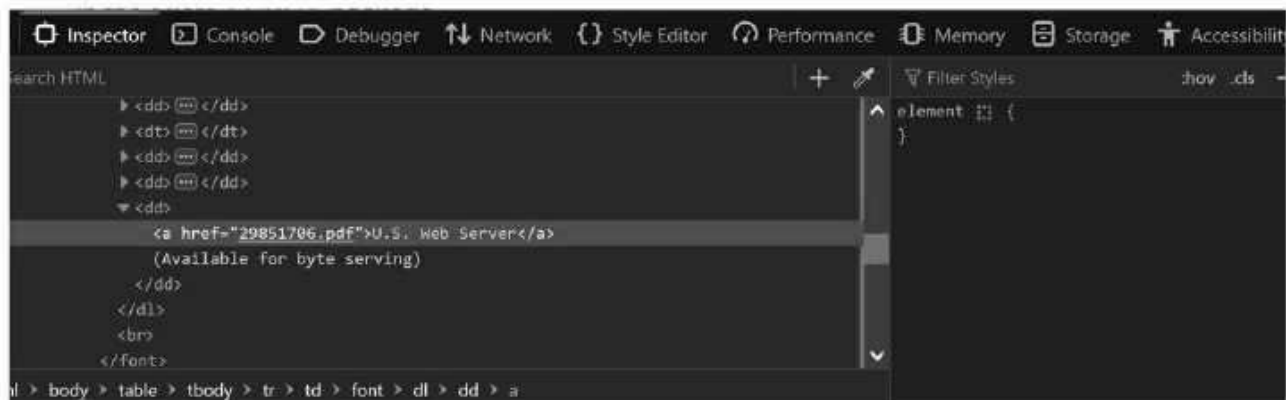
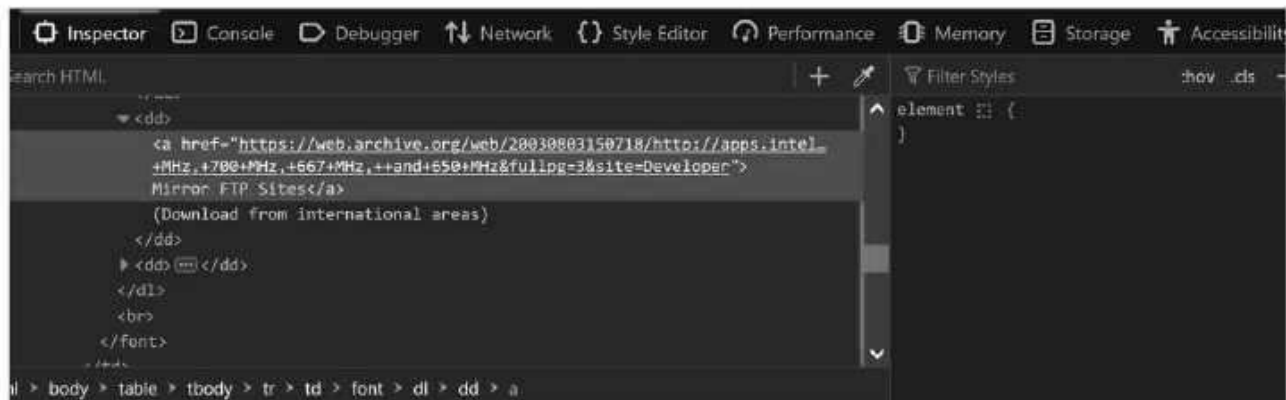
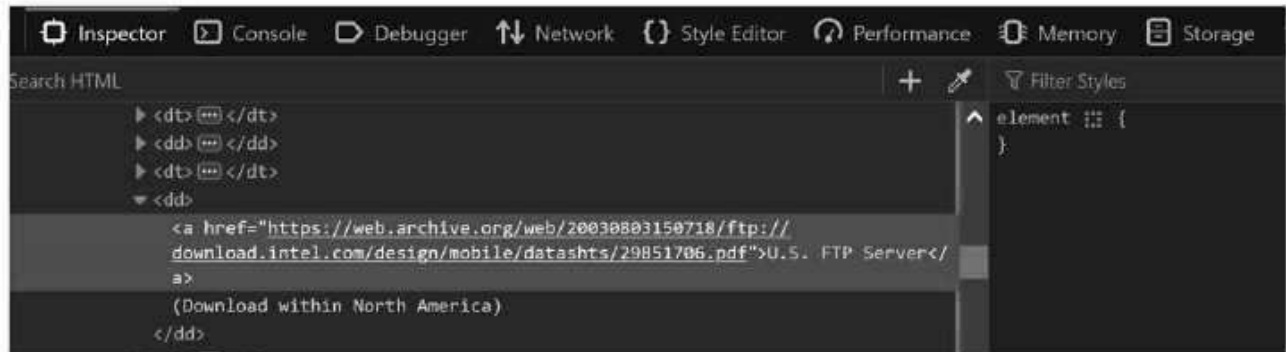
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[Advanced Search](#)

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- Pentium® 4 processors
- Intel® Xeon™ processors
- Pentium® III processors
- Pentium® III Xeon™ processors
- Intel® Celeron® processors
- Intel® Itanium® processors

Mobile processors

- Intel® Pentium® M processors
- Mobile Intel® Pentium® 4 processors - M
- Mobile Intel® Pentium® 4 processors
- Mobile Intel® Pentium® III processors
- Mobile Intel® Celeron® processors**

Archived Products

- Intel® Celeron® processors - PGA
- Intel® Celeron® processors - SEPP
- Pentium® II processors
- Pentium® II Xeon™ processors
- Pentium® Pro processors
- Pentium® processors with MMX™ technology
- Pentium® processors
- Mobile Pentium® processors
- Mobile Pentium® II processors
- OverDrive® processors
- Itanium® processors
- Embedded Pentium® processors and processor modules
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- Intel® Pentium® EX Evaluation processors
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- Intel® Processor Frequency ID Utility
- Processor Package Type Guide

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- Processor Spec Finder tool
- Start here for help with your Pentium® 4 processor supporting Hyper-Threading Technology.

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- Warranty Information
- RMA Request Form

back to top

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NAD/Initiatives

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United States Home

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Site Map

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Mobile Intel® Pentium® M Processor

Mobile Intel® Pentium® M Processor Datasheet

Mobile Intel® Pentium® 4 Processor - M

Mobile Intel® Pentium® 4 Processor - M Datasheet

Mobile Intel® Pentium® III Processor - M

Mobile Intel® Pentium® III Processor - M Datasheet

Mobile Intel® Pentium® III Processor

Mobile Intel® Pentium® III Processor in BGA2 and Micro-PGA2 Packages Featuring Enhanced Intel SpeedStep® Technology at 1 GHz, 900 MHz, 800 MHz, 750 MHz, 700 MHz, Low-voltage 700MHz, Low-voltage 600 MHz, and Ultra Low-voltage 500 MHz

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Mobile Intel® Celeron® Processor on 13 Micron Process in Micro-FCPGA Package Datasheet

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Mobile Chipsets

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DEC 03 2002

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245 0 0 a| Microelectronics and reliability.

246 1 0 a| Microelectronics reliability

246 1 i| Issues for 1998- have title: a| Microelectronics reliability

247 1 0 f| v.1-2, 1962-1963, a| Electronics reliability and microminiaturization.

260 a| Oxford ; a| New York : b| Pergamon Press, c| 1964-

300 a| v. : b| ill. ; c| 26-27 cm.

310 a| Monthly. b| <1997->.

321 a| Frequency varies. b| 1964-

362 0 a| v. 1- jan./Mar. 1962 -

500 a| Title from cover.

650 0 a| Electronic apparatus and appliances x| Reliability v| Periodicals.

650 0 a| Miniature electronic equipment v| Periodicals.

949 a| TK7870.E56 v.18-19 1978/79 w| LCPER c| 1 i| 000057535494 d| 4/27/2006 l| ACAD-BLDG m| UP-ANNEX q| 2 r| Y s| Y t| PERIODICAL u| 10/4/2001 z| 793

949 a| PO-775 w| LCPER c| 1 i| 916043-66001 l| ON-ORDER m| ONLINE r| Y s| Y t| ONLINE u| 7/1/2004

949 a| TK7870.E56 v.17 1978 w| LCPER c| 1 i| 000060047991 d| 6/10/2005 l| ACAD-BLDG m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 6/10/2005 z| 793

949 a| TK7870.E56 v.1 1962 w| LCPER c| 1 i| 000061828292 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/13/2007 z| 5408

949 a| TK7870.E56 v.2 1963 w| LCPER c| 1 i| 000061828308 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/13/2007 z| 5408

949 a| TK7870.E56 v.3 1964 w| LCPER c| 1 i| 000068982461 d| 4/25/2011 e| 3/24/2011 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/13/2007 z| 5408

949 a| TK7870.E56 v.4-5 1965/66 w| LCPER c| 1 i| 000060048042 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/13/2007 z| 5408

949 a| TK7870.E56 v.6-7 1967/68 w| LCPER c| 1 i| 000060048059 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/13/2007 z| 5408

949 a| TK7870.E56 v.8-9 1969/70 w| LCPER c| 1 i| 000060048066 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/14/2007 z| 5408

949 a| TK7870.E56 v.10 1971 w| LCPER c| 1 i| 000060048127 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/14/2007 z| 5408

949 a| TK7870.E56 v.11 1972 w| LCPER c| 1 i| 000060048134 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/14/2007 z| 5408

949 a| TK7870.E56 v.12 1973 w| LCPER c| 1 i| 000060048158 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/14/2007 z| 5408

949 a| TK7870.E56 v.13 1974 w| LCPER c| 1 i| 000060048141 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/14/2007 z| 5408

949 a| TK7870.E56 v.14-15 1975/76 w| LCPER c| 1 i| 000061828117 l| ACAD-BLDG m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/14/2007 z| 793

949 a| TK7870.E56 v.16 1977 w| LCPER c| 1 i| 000060047984 l| ACAD-BLDG m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/14/2007 z| 793

949 a| TK7870.E56 v.20 1980 w| LCPER c| 1 i| 000060047953 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/18/2007 z| 6644

949 a| TK7870.E56 v.21 1981 w| LCPER c| 1 i| 000059403050 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/18/2007 z| 6644

949 a| TK7870.E56 v.22 1982 w| LCPER c| 1 i| 000059403067 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/18/2007 z| 6644

949 a| TK7870.E56 v.23 1983 w| LCPER c| 1 i| 000051833626 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 4/8/2003 z| 7737

949 a| TK7870.E56 v.24 1984 w| LCPER c| 1 i| 000051833633 l| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 4/8/2003 z| 7737

949 a| TK7870.E56 v.25 no.1-3 1985 w| LCPER c| 1 i| 000051833640 d| 2/14/2006 l| CATO-2 m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 4/8/2003 z| 7737



949	a TK7870.E56 v.25 no.4-6 1985 w LC PER c 1 i 000051833657 I CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7737
949	a TK7870.E56 v.26 no.1-3 1986 w LC PER c 1 i 000051833664 I CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7738
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949	a TK7870.E56 v.28 no.1-3 1988 w LC PER c 1 i 000051833701 I CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7738
949	a TK7870.E56 v.28 no.4-6 1988 w LC PER c 1 i 000051833718 I CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7738
949	a TK7870.E56 v.29 no.1-3 1989 w LC PER c 1 i 000051833725 d 3/18/2005 I CATO-2 m UP-ANNEX q 1 r Y s Y t PERIODICAL u 4/8/2003 z 7738
949	a TK7870.E56 v.29 no.4-6 1989 w LC PER c 1 i 000051833732 d 4/1/2004 I CATO-2 m UP-ANNEX q 1 r Y s Y t PERIODICAL u 4/8/2003 z 7738
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949	a TK7870.E56 v.33 no.10-12 1993 w LC PER c 1 i 000051833855 I CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7738
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949	a TK7870.E56 v.38 no.4-9 1998 w LC PER c 1 i 000051834036 I CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7743
949	a TK7870.E56 v.38 no.1-3 1998 w LC PER c 1 i 000051834029 I CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7743
949	a TK7870.E56 v.37 no.10-12 1997 w LC PER c 1 i 000051834012 I CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7743

7743	
949	a TK7870.E56 v.37 no.7-9 1997 w LCPER c 1 i 000051834005 l CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7743
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949	a TK7870.E56 v.36 no.10-12 1996 w LCPER c 1 i 000051833978 l CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7743
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949	a TK7870.E56 v.36 no.7-9 1996 w LCPER c 1 i 000051833961 l CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7743
949	a TK7870.E56 v.36 no.4-6 1996 w LCPER c 1 i 000051833954 d 12/3/2003 l CATO-2 m UP-ANNEX q 2 r Y s Y t PERIODICAL u 4/8/2003 z 7738
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949	a TK7870.E56 v.35 no.4-6 1995 w LCPER c 1 i 000051833923 l CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7738
949	a TK7870.E56 v.35 no.1-3 1995 w LCPER c 1 i 000051833916 l CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7738
949	a TK7870.E56 v.34 no.10-12 1994 w LCPER c 1 i 000051833909 l CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7738
949	a TK7870.E56 v.34 no.7-9 1994 w LCPER c 1 i 000051833893 l CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7738
949	a TK7870.E56 v.34 no.4-6 1994 w LCPER c 1 i 000051833886 d 4/1/2004 l CATO-2 m UP-ANNEX q 1 r Y s Y t PERIODICAL u 4/8/2003 z 7738
949	a TK7870.E56 v.34 no.1-3 1994 w LCPER c 1 i 000051833879 d 9/1/2005 e 8/10/2005 l CATO-2 m UP-ANNEX n 1 q 1 r Y s Y t PERIODICAL u 4/8/2003 z 7738
949	a TK7870.E56 v.33 no.13-15 1993 w LCPER c 1 i 000051833862 l CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/8/2003 z 7738
949	a TK7870.E56 v.42 no.4-8 2002 w LCPER c 1 i 000051858520 l CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 4/14/2003 z 7744
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949	a TK7870.E56 v.43 no.1-4 2003 w LCPER c 1 i 000052801600 d 6/16/2004 l CATO-2 m UP-ANNEX q 1 r Y s Y t PERIODICAL u 2/16/2004 z 7744
949	a TK7870.E56 v.43 no.5-8 2003 w LCPER c 1 i 000052801594 l CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 2/16/2004 z 7744
949	a TK7870.E56 v.43 no.9-12 2003 w LCPER c 1 i 000052800085 l CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 2/16/2004 z 7744
949	a TK7870.E56 v.44 no.1-4 2004 w LCPER c 1 i 000055139465 l CATO-2 m UP-ANNEX r Y s Y t PERIODICAL u 8/21/2006 z 7744
852	0 1 a PSt b UP-ANNEX c ANNEX h TK7870 i .E56
866	0 8 0 a v.1(1962)-v.41:no.4(2001), v.41:no.6(2001)-v.44:no.4(2004)



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TK7870.E56 v.39 no.8-12 1999	Bound Journal	Annexed Material
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TK7870.E56 v.38 no.10-12 1998	Bound Journal	Annexed Material
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TK7870.E56 v.32 no.10-12 1992	Bound Journal	Annexed Material
TK7870.E56 v.32 no.7-9 1992	Bound Journal	Annexed Material
TK7870.E56 v.32 no.4-6 1992	Bound Journal	Annexed Material
TK7870.E56 v.32 no.1-3 1992	Bound Journal	Annexed Material
TK7870.E56 v.31 no.4-6 1991	Bound Journal	Annexed Material
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TK7870.E56 v.16 1977	Bound Journal	Annexed Material
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TK7870.E56 v.13 1974	Bound Journal	Annexed Material
TK7870.E56 v.12 1973	Bound Journal	Annexed Material
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TK7870.E56 v.4-5 1965/66	Bound Journal	Annexed Material
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TK7870.E56 v.1 1962	Bound Journal	Annexed Material

Dates of Publication and/or Sequential Designation:

v. 1- Jan./Mar. 1962 -

Subject(s):

Electronic apparatus and appliances—Reliability—Periodicals

Miniature electronic equipment—Periodicals

ISSN:

0026-2714

Publication Frequency:

Monthly, <1997->.

Frequency varies, 1964-

Note:

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050 00$aTK7874 $b.C74 1992
245 00$aCritical review and technology assessments '91-'92.
260 ##$aRome, NY (P.O. Box 4700, Rome 33440-8200) : $bReliability Analysis Center, $c1992.
300 ##$a1 v. (various paging) : $bill. ; $c30 cm.
504 ##$aIncludes bibliographical references.
505 00$aContents: Assessment of gallium arsenide device quality and reliability -- Plastic microcircuit packages -- Qualified manufacturer's list
599 31$aDonated by Nortel Networks, April 1999.
650 00$aMicroelectronics $xReliability
650 00$aGallium arsenide semiconductors $xReliability.
650 00$aMicroelectronic packaging $xReliability.
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Identifier OCLC : (OCoLC)27728514

Contents Contents: Assessment of gallium arsenide device quality and reliability -- Plastic microcircuit packages -- Qualified manufacturer's list -- Reliability and maintainability software tools, 1991 -- Testability design and assessment tools.

Publisher Rome, NY P.O. Box 4700, Rome 13440-8200 : Reliability Analysis Center

Creation date 1992

Format 1 v. (various paging) : ill. : 30 cm.

General notes Includes bibliographical references.

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260 a| Amsterdam : b| North-Holland, c| c1985-
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949 a| TA347.F5F6 v.37 no.8-12 2001 w| LCPER c| 1 i| 000048277792 I| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 2/27/2002 z| 6320
949 a| TA347.F5F6 v.37 no.1-7 2001 w| LCPER c| 1 i| 000048277815 I| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 2/27/2002 z| 6320
949 a| TA347.F5F6 v.36 2000 w| LCPER c| 1 i| 000048277808 d| 11/2/2004 e| 11/2/2004 I| CATO-2 m| UP-ANNEX n| 1 r| Y s| Y t| PERIODICAL u| 2/27/2002 z| 6320
949 a| TA347.F5F6 v.34-35 2000 w| LCPER c| 1 i| 000051705589 I| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/4/2002 z| 6320
949 a| TA347.F5F6 v.32-33 1999 w| LCPER c| 1 i| 000051705572 I| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/4/2002 z| 6320
949 a| TA347.F5F6 v.30-31 1998/99 w| LCPER c| 1 i| 000051705565 I| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/4/2002 z| 6320
949 a| TA347.F5F6 v.28-29 1997/98 w| LCPER c| 1 i| 000051705558 I| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/4/2002 z| 6320
949 a| TA347.F5F6 v.26-27 1997 w| LCPER c| 1 i| 000051705541 d| 5/2/2003 I| CATO-2 m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 9/4/2002 z| 6320
949 a| TA347.F5F6 v.24-25 1996/97 w| LCPER c| 1 i| 000051705534 I| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/4/2002 z| 6320
949 a| TA347.F5F6 v.22-23 1996 w| LCPER c| 1 i| 000051705527 d| 11/2/2004 e| 11/2/2004 I| CATO-2 m| UP-ANNEX n| 1 r| Y s| Y t| PERIODICAL u| 9/4/2002 z| 6320
949 a| TA347.F5F6 v.20-21 1995/96 w| LCPER c| 1 i| 000051705510 I| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/4/2002 z| 6320
949 a| TA347.F5F6 v.18-19 1994/95 w| LCPER c| 1 i| 000051705503 I| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/4/2002 z| 6320
949 a| TA347.F5F6 v.16-17 1994 w| LCPER c| 1 i| 000051705497 I| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/4/2002 z| 6320
949 a| TA347.F5F6 v.14-15 1993/94 w| LCPER c| 1 i| 000051705480 I| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/4/2002 z| 6320
949 a| TA347.F5F6 v.13 1993 w| LCPER c| 1 i| 000051705473 I| CATO-2 m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/4/2002 z| 6320



949	a	TA347.F5F6 v.12 1992 w	LCPER c	1 i	000051705466 l	CATO-2 m	UP-ANNEX r	Y s	Y t	PERIODICAL u	9/4/2002 z	6320				
949	a	TA347.F5F6 v.11 1992 w	LCPER c	1 i	000051705459 l	CATO-2 m	UP-ANNEX r	Y s	Y t	PERIODICAL u	9/4/2002 z	6320				
949	a	TA347.F5F6 v.9-10 1991/92 w	LCPER c	1 i	000051705442 l	CATO-2 m	UP-ANNEX r	Y s	Y t	PERIODICAL u	9/4/2002 z	6320				
949	a	TA347.F5F6 v.8 1990 w	LCPER c	1 i	000051705435 l	CATO-2 m	UP-ANNEX r	Y s	Y t	PERIODICAL u	9/4/2002 z	6320				
949	a	TA347.F5F6 v.6-7 1989-91 w	LCPER c	1 i	000051705428 d	8/21/2007 e	7/7/2003 l	CATO-2 m	UP-ANNEX n	1 q	1 r	Y s	Y t	PERIODICAL u	9/4/2002 z	6320
949	a	TA347.F5F6 v.5 1989 w	LCPER c	1 i	000051705411 l	CATO-2 m	UP-ANNEX r	Y s	Y t	PERIODICAL u	9/4/2002 z	6320				
949	a	TA347.F5F6 v.4 1988/89 w	LCPER c	1 i	000051705404 l	CATO-2 m	UP-ANNEX r	Y s	Y t	PERIODICAL u	9/4/2002 z	6320				
949	a	TA347.F5F6 v.3 1987 w	LCPER c	1 i	000051705398 d	6/30/2004 e	6/30/2004 l	CATO-2 m	UP-ANNEX n	1 r	Y s	Y t	PERIODICAL u	9/4/2002 z	6320	
949	a	TA347.F5F6 v.2 1986 w	LCPER c	1 i	000051705381 l	CATO-2 m	UP-ANNEX r	Y s	Y t	PERIODICAL u	9/4/2002 z	6320				
949	a	TA347.F5F6 v.1 1985 w	LCPER c	1 i	000051705374 d	5/30/2006 l	CATO-2 m	UP-ANNEX q	1 r	Y s	Y t	PERIODICAL u	9/4/2002 z	6320		
852	0	1 a	PSt b	UP-ANNEX c	ANNEX h	TA347.F5 i	F6									
866	0	8	0 a	v.1(1985)-v.40:no.8(2004)												



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Dates of Publication and/or Sequential Designation:

Vol. 1, no. 1 (Apr. 1985)-

Subject(s):

Finite element method—Periodicals

Engineering design—Data processing—Periodicals

Computer-aided design—Periodicals

ISSN:

0168-874X

Publication Frequency:

Quarterly.

Note:

"The international journal of applied finite elements and computer aided engineering."

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