UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP USA, INC.,
Petitioner,

v.

BELL SEMICONDUCTOR, LLC,
Patent Owner

Case: IPR2024-00168

U.S. Patent No. 7,345,245

EXPERT DECLARATION OF DR. JOSEPH BERNSTEIN IN SUPPORT OF PATENT OWNER'S RESPONSE

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I. INTRODUCTION

1. My name is Dr. Joseph Bernstein and I have been retained as a technical expert by counsel for Patent Owner Bell Semiconductor, LLC ("Bell Semic" or "Patent Owner") to provide expert opinion testimony in the above captioned matter.

2. I have been asked to render opinions on Petitioner's unpatentability arguments regarding U.S. Patent No. 7,345,245 ("the '245 Patent") that have been identified in the Petition. Specifically, I have been asked to consider whether certain references disclose or suggest the features recited in claims 1–6, and 8 of the '245 patent.

3. This report contains statements of my opinions formed to date regarding these references and the '245 Patent and the bases and reasons for those opinions. I may offer additional opinions based on further review of materials in this case, including opinions and/or testimony of other expert witnesses.

4. Based upon the materials that I have considered, and the arguments made by Petitioner and Dr. Baker, as explained below it is my opinion that Petitioner has failed to meet its burden to show that any challenged claim of the '245 Patent is unpatentable.

II. QUALIFICATIONS

5. This is a summary of my background and qualifications. I set forth my background in more detail in my Curriculum Vitae ("CV"), below.

6. I graduated *Summa Cum Laude* from Union College in Schenectady, NY with a Bachelor of Science degree in Electrical Engineering in 1984. Subsequently, I attended the Massachusetts Institute of Technology (MIT), where I earned a Master of Science degree in Electrical Engineering and Computer Science in 1986, an Electrical Engineering degree in 1987, and a Doctor of Philosophy in Electrical Engineering and Computer Science in 1990.

7. After earning my Ph.D., I worked at MIT Lincoln Laboratory as a senior research staff member, during which time I taught at Boston University as an Adjunct Professor. My first position at Lincoln Labs was as a senior research staff in the Wafer Scale Integration group. This group was responsible for developing technologies to allow programming and packaging of wafer scale integrated circuits. Technologies we developed included mounting, wiring, routing, programming, packaging, and reliability for very large wafer scale integrated circuits. This is where I developed laser programmable interconnect technology which was my first set of patents and was the basis for my first start-up company, Lightspeed Semiconductor, and my introduction to the field of

Microelectronics Reliability. I have a book from that era: Hoang, H.H., Schutz, R., Bernstein, J.B., Vasquez, B., *Multi-level Interconnection: Issues that Impact Competitiveness*, Proceedings of SPIE 2090, 1993.

8. From 1995 to 2007, I was first an Assistant and then Associate Professor of Engineering at the University of Maryland (UMD) while acting as co-founder and chief scientist of Lightspeed, a Silicon Valley company relating to high performance, metal-configurable gate arrays using laser anti-fuses. Upon arriving at UMD as a professor of Microelectronics Reliability, I was soon invited by the head of the Packaging Reliability Center (CALCE), Professor Michael Pecht, to lead a group of industry packaging experts to investigate the emerging Korean electronics industry. This experience led to my complete immersion and familiarity with the latest packaging techniques in the world, primarily those happening in South Korea. This led to my next book as a co-author: Pecht, M., Bernstein, J.B., Searls, D., and Peckerar, M., *The Korean Electronics Industry*, CRC Press, 1997.

9. Thus, my background started from my collaborations at UMD and my work with the industry. My research programs brought me close with many companies around the world looking into better, cheaper, and more reliable packaging techniques for the latest industrial technologies. I have several journal

publications from that era in the field of electronic packaging from my research and student supervision in industry. Some more appropriate publications from the time include the following:

- Gershman and J. B. Bernstein, "*Structural health monitoring of solder joints in QFN package,"* Microelectronics Reliability, Volume 52, Issue 12, Pages 3011–3016 (2012).
- L. Yang and J. Bernstein, *"Reliability Evaluation and Modeling of High Density Electronic Packages,"* Microelectronics International, vol. 29, no. 1, pp. 15-21 (2012).
- Gershman and J. B. Bernstein, *"Solder-Joint Quantitative Crack Analysis—Ohmic Resistance Approach,"* IEEE Transaction on Components, Packaging and Manufacturing Technology, vol. 2, no. 5, pp. 748 - 755 (2012).
- L.-S. Yang and J.B. Bernstein, *"Encapsulation Process Development for Flexible Circuit Based Chip Scale Packages,"* IEEE Trans. Electronics Packaging Manufacturing, vol. 25, no. 4, pp. 344-354 (October 2002).
- L.-S. Yang, J.B. Bernstein and K.C. Leong, *"Effect of the Plasma Cleaning Process on Plastic Ball Grid Array Package Assembly Reliability,"* IEEE Trans. Electronics Packaging Manufacturing, vol. 25, no. 2, pp. 91-99 (April 2002).
- Yang, L., Bernstein, J.B., Chung, K, *"The Impact of Lead-free Soldering on Electronics packages,"* Microelectronics International, vol. 18, no. 3, pp. 20-26 (2001).

10. Many more of my publications and patents (including my work on electronic packaging and testing) are listed in my CV.

11. While at the University of Maryland, I taught in the Reliability program as the specialist in microelectronics device reliability. In the summer of 1998, I joined the Jet Propulsion Laboratories as a NASA Summer Faculty

Research Fellow. At UMD, I was promoted from Assistant to Associate Professor with tenure in 2001. From 2003 to 2005, I was a Professor of Engineering at Tel-Aviv University on Sabbatical from the University of Maryland and as a Fulbright Fellow lecturer, and researcher. During my tenure at Maryland, I had many programs also sponsored at the National Institute of Standards and Technology (NIST), where I worked directly with the semiconductor industry by means of the connection with NIST. This group acted as a government liaison with semiconductor manufacturing companies and often was the center for Joint Electron Device Engineering Council (JEDEC) roundtables and committee groups focused on reliability and standards for the semiconductor industry.

12. I am currently employed at Ariel University of Israel. At Ariel, a large focus of my research is on issues related to chip and packaging reliability, including links between reliability, power, and thermal behavior. My current research focuses on packaged devices at the board level. We look at the functionality and performance of system-level reliability boards and packages, including FPGAs embedded with DRAM and Flash memory. We look at all the failure mechanisms that can affect the reliability of the circuits and systems and model these mechanisms to derive a complete reliability prediction methodology.

13. I also work with several consulting clients in the semiconductor field

that apply my methodologies, as well as system level customers and various smaller companies and startups.

14. I have published several books, one new one is completed and expected to be published in 2024. I have published more than 120 refereed journal publications and conference papers, a more complete list of which is included in my CV. In addition to my publications, I have given numerous tutorials, talks, presentations, and lectures, in both academic and corporate settings, on semiconductor devices and reliability. For at least the past five years, I am the first or second most referenced author in the field of Microelectronics Reliability as listed by Google Scholar.

15. I have been affiliated with the Reliability Program of the Mechanical Engineering Department, the Electrical and Computer Engineering Department, and the Institute for Research in Electronics and Applied Physics at the University of Maryland. I was also affiliated with the Nano-Science and Nano-Technology Center at Tel-Aviv University, which I headed during my Sabbatical there. I also served as the Founder and Faculty advisor for the Israel Electronics Manufacturers Working Group on Reliability (ILTAM), and I lead the Laboratory for Reliable Electronics Systems at Ariel University.

16. I currently supervise two Ph.D. candidates and one post-doc. I have

served as the advisor or co-advisor for twenty Ph.D. graduates in electrical and electronic engineering, many of whom graduated in the materials and mechanical engineering departments through the Reliability Program at the University of Maryland and several more in Israel.

17. I teach classes at Ariel University that include undergraduate and graduate courses in Electrical Engineering. Some courses I have taught include VLSI Design, Reliability Engineering Fundamentals, Microelectronics Device Reliability, Advanced Reliability Engineering, and Quality Engineering Fundamentals. I have also developed coursework and curriculum on Reliability Engineering and Electronic Device Reliability.

18. I am a named inventor on at least eight issued U.S. utility patents in fields including electrical interconnections and repairable systems in microelectronics packaging technology.

III. PRIOR TESTIMONY

19. I have served as a testifying expert in litigation in ten district court cases. I have also served as an expert in several matters at the Patent Trial and Appeal Board, including *inter partes* reviews and patent reexaminations.

20. I have also served as a technical consultant for electronics and computer systems companies on issues including testing and reliability.

21. A list of all such cases in which I have consulted or testified as an expert at trial or by deposition can be found in my CV.

IV. COMPENSATION

22. I am being compensated for my services in this proceeding. This compensation is not contingent upon my performance, the outcome of this case, or any issues involved in or related to this case. I have no financial interest in this matter.

V. MATERIALS CONSIDERED

23. My opinions are based on my experience in this field, and are necessarily formed by my own experiences, materials I have read over the years, and discussions I have had with colleagues during my career. I have also considered the understanding of a person of ordinary skill ("POSITA") around the time of the invention of the '245 Patent. In addition, I have reviewed and considered the following materials in forming my opinion:

- The '245 Patent (EX1001);
- File History of the '245 Patent (EX1004);
- The Devnani reference, US Patent Pub. 2003/0183919 to Devnani et al. (EX1005);
- The Chung reference, US Patent Pub. 2003/0003705 to Chung, et al.

(EX1006);

- The Pillai reference, U.S. Patent No. 6,680,530 to Pillai et al. (EX1007);
- The Celeron reference, Mobile Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA and Micro-FCPGA Packages Datasheet (EX1008);
- The Tanahashi reference, U.S. Patent No. 6,172,305 to Tanahashi (EX1009);
- Thomas D. Moore, et al., "The effects of in-plane orthotropic properties in a multi-chip ball grid array assembly, Microelectronics Reliability, Volume 42, Issue 6, pages 943-949 (EX1010);
- D.J. Xie et al, "Process capability study and thermal fatigue life prediction of ceramic BGA solder joints, Finite Elements in Analysis and Design, Vol. 30, Issues 1-12, pages 31-45 (EX1011);
- Critical Review and Technology Assessments '91-'92, Reliability Analysis Center, AD-A278 419 (EX1016);
- 2000 Packaging Handbook, Chapter 4: Performance Characteristics of IC Packages, pages 1-6 (EX1017); and
- "A Review of Ball Grid Arrays for Electronic Assembly," SB Dunkerton et al. (EX1018).

- August 15, 2024 Deposition Transcript of R. Jacob Baker, Ph.D. (EX2004)

VI. UNDERSTANDING OF THE LAW

24. I am not an attorney. For the purposes of this declaration, Patent Owner's counsel has informed me about certain aspects of the law that are relevant to my opinions. I have applied those legal principles in arriving at my conclusions expressed in this declaration.

25. I understand that the first step in performing a validity analysis of the patent claims is to interpret the meaning and scope of the claims by construing the terms and phrases found in those claims. I understand that a determination of the meaning and scope of the claims is a matter of law. I have been informed that to determine the meaning of the claims, courts consider the intrinsic evidence, which includes the patent's claims, written description, prosecution history, materials incorporated by reference in the patent, and prior art cited in the patent or its prosecution history. Courts give claim terms their ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the content of the entire patent. A patentee may also define his or her own terms to disavow claim scope. Normally, embodiments and examples appearing in the specification will not generally be read into the claims. However,

the intrinsic record may resolve ambiguous claims terms where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone. A term's context in the claims can also be helpful. Differences among the claim terms can also assist in understanding a term's meaning.

26. I have been informed that extrinsic evidence can also be useful in determining the meaning of claims, however, it is less significant than the intrinsic record. Technical dictionaries may be useful to show the way one skilled in the art might use claim terms, but technical dictionaries may provide definitions that are too broad or may not be indicative of how the term is used in the patent.

27. I understand that the claim terms of a patent are to be construed from the point of view of a hypothetical person of ordinary skill in the art (POSITA) in the time frame of the patent's priority date. (At times I may refer to a person of skill in the art as simply "a skilled person.") For the purpose of assessing the level of ordinary skill of such an individual, I have considered the types of problems encountered in the art, the prior solutions to those problems found in the literature, the speed with which innovations were made in the time relevant time frame, and the level of education and expertise of active workers in the field.

28. It is my opinion that a POSITA at the time of the invention of the '245

Patent would have had a minimum of a bachelor's degree in a field relating to semiconductor packaging, such as mechanical, electrical, or computer engineering, along with at least two years of experience in semiconductor packaging (or additional education substituting for professional experience and/or significant experience in the field substituting for formal education). Given the above description of a POSITA, and based on my education and advanced experience, I believe that I at least meet or even exceed the necessary qualifications in the timeframe of the invention.

A. Legal Standards for Prior Art

29. I understand that a patent or other publication must first qualify as prior art before it can be used to invalidate a patent claim.

30. I understand that a U.S. or foreign patent qualifies as prior art to an asserted patent if the date of issuance of the patent is prior to the invention of the asserted patent. I further understand that a printed publication, such as an article published in a magazine or trade publication, qualifies as prior art to an asserted patent if the date of publication is prior to the invention of the asserted patent.

31. I understand that a U.S. or foreign patent also qualifies as prior art to an asserted patent if the date of issuance of the patent is more than one year before the filing date of the asserted patent. I further understand that a printed

publication, such as an article published in a magazine or trade publication, constitute prior art to an asserted patent if the publication occurs more than one year before the filing date of the asserted patent.

32. I understand that a U.S. patent qualifies as prior art to the asserted patent if the application for that patent was filed in the United Stated before the invention of the asserted patent.

B. Legal Standard for Obviousness

33. I understand that even if a patent is not anticipated, it is still invalid if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person of ordinary skill in the art.

34. I understand that a person of ordinary skill in the art provides a reference point from which the prior art and claimed invention should be viewed. This reference point prevents one from using his (or her) own insight or hindsight in deciding whether a claim is obvious.

35. I also understand that an obviousness determination includes the consideration of various factors such as:

a. the scope and content of the prior art,

b. the differences between the prior art and the asserted claims,

c. the level of ordinary skill in the pertinent art, and

d. the existence of secondary considerations such as commercial success, long-felt but unresolved needs, failure of others, etc.

36. I understand that an obviousness evaluation can be based on a combination of multiple prior art references. I understand that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but other times the nexus linking two or more prior art references is just common sense. I further understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may be supplied by the direction of the marketplace.

37. I understand that if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

38. I also understand that practical and common-sense considerations should guide a proper obviousness analysis, because familiar items may have obvious uses beyond their primary purposes. I further understand that a person of ordinary skill in the art looking to overcome a problem will often be able to fit

together the teachings of multiple publications. I understand that obviousness analysis therefore considers the inferences and creative steps that a person of ordinary skill in the art would employ under the circumstances.

39. I understand that a particular combination may be proven obvious merely by showing that it was obvious to try the combination. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

40. The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, the patent claim is likely obvious.

41. It is further my understanding that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill in the art, not just the patentee. Accordingly, I understand that any need or problem known in

the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

42. I understand that a claim can be obvious through consideration of a single reference, without the need to combine references, if the elements of the claim that are not found explicitly or inherently in the reference can be supplied by the common sense of one of skill in the art.

43. I understand that secondary indicia of non-obviousness may include:

a. a long felt but unmet need in the prior art that was satisfied by the invention of the patent;

b. commercial success of processes covered by the patent;

c. unexpected results achieved by the invention;

d. praise of the invention by others skilled in the art;

e. taking of licenses under the patent by others;

f. deliberate copying of the invention;

g. failure of others to find a solution to the long-felt need; and

h. skepticism by experts.

44. I also understand that there must be a relationship between any such secondary considerations and the invention.

45. I further understand that contemporaneous and independent invention

by others is a secondary consideration supporting an obviousness determination.

46. In summation, my understanding is that prior art teachings are properly combined where a person of ordinary skill in the art having the understanding and knowledge reflected in the prior art and motivated by the general problem facing the inventor, would have been led to make the combination of elements recited in the claims. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of multiple prior art references in the claimed manner.

47. I understand that obviousness in an *inter partes* review must be shown by a preponderance of the evidence, which is a higher standard than the reasonable likelihood standard for instituting *inter partes* review.

VII. OPINION

48. The ’245 Patent, entitled “Robust High Density Substrate Design for Thermal Cycling Reliability,” has a priority date of October 8, 2003, and relates to a semiconductor package for a die with improved thermal cycling reliability. (EX1001, Abstract.)

49. The development of the semiconductor package claimed in the ’245 Patent represented an important advancement related to the design of a

semiconductor device.

50. Specifically, the ’245 Patent discloses an improved signal trace routing in the high stress area under the die corner that accommodates a range of die sizes. (EX1001 at 2:36–39.)

51. This responds to the increased demand for high density signal routing on organic BGA substrates based on advances in semiconductor technology.

52. Packages with a full area ball array were also adopted to reduce the package body size and provide a high input/output (IO) signal density. (*Id.* at 1:8–13.)

53. In the prior art, signal traces on the bottom routing layer were routed over the ball pads of the underlying layer. (*See id.* at 1:24–26, 1:57–58.)

54. The die corner is associated with a surrounding area of high stress, which also affects the ball pads positioned under the surrounding area.

55. The edges of those ball pads act as stress concentration points and, under temperature cycling conditions associated with typical use of semiconductor device, cracks are initiated from the edges of the ball pads and extend into the dielectric layer above. (*Id.* at 1:58–65.)

56. One solution to overcoming this problem is to place metal planes below the bottom routing layer under the die corner 28; however, this causes a

reduction in signal density. (*Id.* at 2:3–6.)

57. Another solution is to define a circular area with a one-millimeter radius around the die corner and avoiding routing traces within this region on the bottom routing layer. (*Id.* at 2:6–9.)

58. However, these solutions are not sufficient to avoid trace cracks in the bottom routing layer under temperature cycling conditions for all packaging technologies. (*See id.* at 2:16–18.)

59. Inventors Anand Govind, Zafer Kutlu, and Farshad Ghahghahi ("the '245 Inventors"), understood these issues and set out to develop an improved method for designing a semiconductor package that eliminates the occurrences of cracks in the signal traces.

60. The '245 Inventors ultimately conceived of a methodology for signal trace routing in the high stress area under the die corner that accommodates a range of die sizes. (*Id.* at 2:36–39.)

61. One such embodiment of the invention provides an improved package in which a high stress area associated with the die corner is defined as an area within two ball pad pitches of the die corner and in which the signal traces are routed so as to preferably be outside the high stress area or, if they cannot be moved outside the high stress area, to avoid being over ball pads within the high

stress area. (*Id.* at 2:32–36; 3:45–50.)

A. Cited Art

The Petition cites the following art:

1. U.S. Patent No. 7,345,245 to Govind et al. (Purported "AAPA") (EX1001)

62. FIGS. 1–3 of the '245 Patent are labeled "prior art" and show a full area ball array package described in the Background of the Invention as being "currently in wide use." (EX1001 at 1:23–2:2.)

63. The prior art full area ball array package design is described as a "multi-layer organic BGA flip chip substrate that uses a 9-layer stackup 20 with a thin core," in which "[n]umerous signal traces 36 and other metal structures extend across the layer L8 proximate the die corner 38a" and "[t]he signal traces 36 of layer L8 are routed over the ball pads 34 of layer L9." (*Id*.)

64. The Background of the Invention also identifies a problem with such full area ball array packages and two "existing" solutions to the problem. (*Id.* at 1:58–2:15.)

65. The problem is that "areas of high stress are associated with the die corner 38a and in particular the ball pads which are positioned under the area surrounding the die corner 38a. The edges of the ball pads 34, which are

associated with the die corner 38a act as stress concentration points and under thermal cycling conditions, cracks are initiated from the edges of the ball pads 34 and extend into the dielectric layer above layer L9. If traces 36 are routed or other metal structures are provided on layer L8 over the ball pads 34 associated with the die corner 38a, the cracks can extend through the traces 36 and cause failures due to trace cracks under cycled stress conditions." (*Id*. at 1:58–2:2.)

66. The first "existing" solution is to place metal planes on the layer L9 under the die corner. (*Id*. at 2:3–6.)

67. The second "existing" solution is to define "a circular shaped area with a one (1) millimeter radius using placement of the die corner 38a as the center of the circle" and not routing traces "within the circular region." (*Id*. at 2:6–15.)

68. Neither the problem nor the "existing" solutions are described in the '245 Patent as being in the prior art or known by others.

69. Without providing any analysis or evidence to support its position, Petitioner makes a conclusory allegation that both the problem identified in the '245 Patent and the two "existing" solutions are admitted prior art. (Pet. at 5–8.)

70. Here, the Background did not state that the problem was known in the prior art, nor did the Background describe the second "existing" solution as "prior art," and Petitioner has not presented any analysis or evidence to show that either

the problem or the "existing solution" should be considered admitted prior art.

71. In fact, there is ample evidence that the problem and "existing" solution should not be considered admitted prior art.

72. First, while Applicant clearly labeled the package design in FIGS. 1–3 as "prior art" and described it as being "currently in wide use," it consciously avoided using similar terminology to describe the problem with the package design and "existing" solutions to the problem.

73. Instead, Applicant merely explained the problem without characterizing it in any way (i.e., without any admission) and referred to the solutions as "existing" (which is not the same as 'prior art' or 'currently in wide use').

74. The lack of any admission with respect to the problem and the use of different terminology with respect to the solutions evidence an intent on the part of the Applicant to distinguish these statements in the patent from the prior art.

75. Second, the invention is described throughout the patent in a way that encompasses the second "existing" solution.

76. For example, in the Abstract, the Applicant describes the invention generally as defining "a high stress area associated with the corner of the dies" and "routing [signal traces] away from the high stress area," and uses the term

"preferably" when describing the embodiment wherein the high stress area is defined as "two ball pitches away from the corner of the die." (*Id.* at Abstract.)

77. Similarly, in the Objects and Summary of the Invention, Applicant states "an embodiment of the present invention provides an improved package in which a high stress area associated with the die corner is defined and in which the signal traces are routed away from the high stress areas at the die corner." (*Id.* at 2:32–39.)

78. The Detailed Description also refers to the invention broadly as a package "in which signal traces are routed away from the high stress area associated with the ball pads and the corner of the die." (*Id.* at 3:6–9.)

79. Finally, it should be noted that independent claim 7 of the '245 patent (which was statutorily disclaimed) is in fact broader than the "existing" solution because it does not specify a specific size or shape of the "surrounding area of increased stress." (*Id.* at 4:38–48.)

80. Thus, it is evident that the Applicant did not consider the problem or the "existing" solution to be in the prior art.

2. US Patent Pub. 2003/0183919 to Devnani et al. ("Devnani") (EX1005)

3. **US Patent Pub. 2003/0003705 to Chung, et al. ("Chung") (EX1006)**

4. **US Patent No. 6,680,530 to Pillai et al. ("Pillai") (EX1007)**

5. **Mobile Intel® Celeron® Processor (0.13 µ) in Micro-FCBGA and Micro-FCPGA Packages Datasheet (April 2003) ("Celeron") (EX1008)**

6. **U.S. Patent No. 6,172,305 to Tanahashi ("Tanahashi") (EX1009)**

VIII. CLAIM CONSTRUCTION

81. Petitioner does not specify what constitutes the plain and ordinary meaning of any term and believes that "no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims." (Pet. at 10.)

82. The Petition fails to specify the meaning of three claim terms that are critical to this proceeding:

1. "wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die" (Claim 1);

2. "area of increased stress defined by the corner of the die" (Claims 7/8); and

3. "within two ball pad pitches of the corner of the die" (Claims 1 and 8).

A. "wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die" (Claim 1)

83. I understand that the Patent Owner Response construes the term "wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die" in claim 1 to mean "wherein the plurality of ball pads includes ball pads disposed in an area within two ball pad pitches of the corner of the die and wherein none of the signal traces of the bottom routing layer are located over the ball pads in the area." I agree with this construction of the term.

84. I agree that the phrase "which are disposed in an area within two ball pad pitches of the corner of the die" is a restrictive relative clause that limits the meaning of the noun "ball pads of the ball pad layer."

85. I agree that the restrictive relative clause "which are disposed in an area within two ball pad pitches of the corner of the die" modifies the subject "ball pads of the ball pad layer," at least because the subject "ball pads of the ball pad

layer" is immediately antecedent to the restrictive relative clause, there is no other subject next to the restrictive relative clause, and they are written together without any comma between them.

86. I agree that a mapping of the nouns and verbs in the limitation further supports this conclusion because the verb "disposed" is clearly associated with the state of the immediately antecedent noun "ball pads of the ball pad layer," whereas the verb "located" is clearly associated with the state of the immediately antecedent noun "signal traces."

87. Thus, I agree that the only reading of this limitation that makes sense grammatically is that it requires ball pads of the ball pad layer to be disposed in an area within two ball pad pitches of the corner of the die.

88. The intrinsic evidence suports the proposed construction.

89. First, the proposed construction is consistent with the stated purpose of the invention to solve a problem arising from "increased demand for high density signal routing," (EX1001 at 1:8-10), which results in ball pads being disposed in the area surrounding the die corner (e.g., in a full area ball array) to "provide a high input/ouput (IO) signal density." (EX1001 at 1:10–12.)

90. The '245 Patent states that "[p]roblems exist with the packages which are currently in wide use" in which "signals are typically routed directly over the

ball pads under the die corner on the bottom routing layer." (EX1001 at 1:23–26.)

91. The '245 Patent explains that this is a problem because "[a]reas of high stress are associated with the die corner 38a and in particular the ball pads which are positioned under the area surrounding the die corner" and "edges of the ball pads 34 which are associated with the die corner 38a act as stress concentration points and under temperature cycling conditions, cracks are initiated from the edges of the ball pads 34 and extend into the dielectric layer above [the ball pad layer]." (EX1001 at 1:57–64.)

92. The '245 Patent goes on to explain that "[i]f traces 36 are routed or other metal structures are provided on layer L8 over the ball pads 34 associated with the die corner 38a, the cracks can extend through the traces 36 and cause failures due to trace cracks under cycled stress conditions." (EX1001 at 1:64–2:2.)

93. Two "existing" solutions are discussed in the '245 Patent, together with their disadvantages, and an improved package according to the invention is disclosed. (EX1001 at 2:3–44.)

94. In light of the specification, I agree that the limitation must be construed in the context of solving the problem of reliably routing signal traces in a high density substrate in which ball pads are disposed in the high stress area around the die corner.

95. Second, the specific embodiment described in the '245 Patent includes ball pads disposed within the high stress area around the corner of the die. (*See, e.g.*, EX1001 at 3:6-9 ("An embodiment of the present invention provides a substrate package in which signal traces are routed away from the ***high stress area*** associated with ***the ball pads and the corner of the die***."); EX1001 at 3:28–30 ("Several ball pads 52 are provided within the high stress zone 58 and several ball pads are provided within the high stress zone 60."); EX1001 at 3:46–50 ("If, however, the traces 64 cannot be moved outside the high stress zone 58, the traces 64 are routed so as to avoid routing the traces 64 over the ball pads 52 of layer L9 within the high stress area 58."); EX1001 at 3:55–59 ("Because the signal traces 64 and other metal structures are not provided over the ball pads 52, cracks initiated from the ball pad edges during thermal cycling do not affect the traces 64 and other metal structures and therefore thermal cycling reliability of the package is improved.").

96. Similarly, in Figure 4 of the '245 Patent (reproduced below), several ball pads 52 are illustrated in the high stress areas 58 and 60 surrounding corners 54a and 56a of two dies 54 and 56.

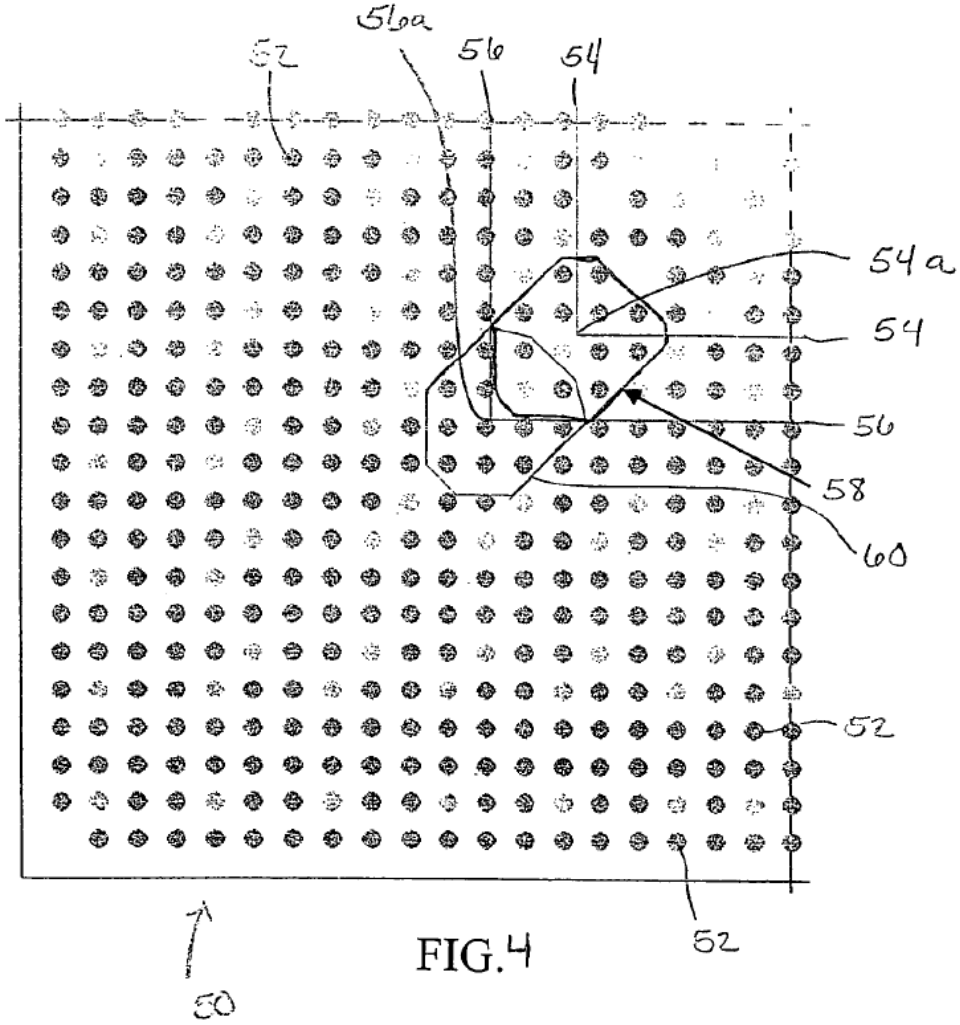


FIG.4

(EX1001 at FIG. 4.)

97. Thus, Patent Owner's proposed construction comports with the only embodiment shown and described in the '245 Patent.

98. Third, the '245 Patent disavows embodiments in which there is no high stress area associated with ball pads under the die corner.

99. The illustrated embodiment, in which ball pads are disposed in a high

stress zone two ball pad pitches from the die corner in each direction, (EX1001 at 3:26–30), is referred to in the '245 patent as "the present invention," (EX1001 at 2:43–44.)

100. As opposed to eliminating the high stress area by removing ball pads under the area surrounding the die corner, which would require custom designed high density ball grid arrays for every type of die, the '245 Patent explains that "***[t]he invention*** describes a methodology for signal trace routing ***in the high stress area*** under the die corner that incorporates a range of die sizes," (EX1001 at 2:36–39 (emphasis added).)

101. The '245 Patent defines "[a]reas of high stress" as those "associated with the die corner 38a and ***in particular the ball pads which are positioned under the area surrounding the die corner 38a***." (EX1001 at 1:57-59 (emphasis added); *see also* EX1001 at 1:18-21 and 3:6-9.)

102. By providing a methodology for signal trace routing in the high stress area associated with ball pads under the area surrounding the die corner, the present invention makes it possible to reliably use high density ball grid arrays (i.e., packages with ball pads dispersed throughout the ball pad layer) with dies of various sizes.

103. It is my understanding that such statements are disavowals that further

confirm the propriety of Patent Owner's proposed construction.

104. Fourth, it is my understanding that embodiments without ball pads under the corner of the die were disavowed during prosecution of the application that issued as the '245 Patent, when applicant's attorney expressly argued that "[p]roviding that none of the signal traces of the bottom routing layer are located over ***the*** ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die ***is the essence of the present invention*** . . .," (EX1004 at 298 (emphasis added).)

105. By expressly referring to "***the*** ball pads . . . which are disposed in a area within two ball pad pitches of the corner of the die" in characterizing "the essence of the present invention," the applicant confirmed that the invention includes ball pads disposed in an area within two ball pad pitches of the corner of the die, and disavowed packages in which there are no ball pads within two ball pad pitches of the corner of the die.

106. For at least these reasons, I agree that this limitation should be construed to mean "wherein the plurality of ball pads includes ball pads disposed in an area within two ball pad pitches of the corner of the die and wherein none of the signal traces of the bottom routing layer are located over the ball pads in the area" is submitted to be correct and should be adopted by the Board.

B. "said die having a corner defining a surrounding area of increased stress" (Claims 7/8)

107. I understand that the Patent Owner Response construes the term "said die having a corner defining a surrounding area of increased stress" in claim 8 (by virtue of its dependence on statutorily disclaimed independent claim 7) to mean "said die having a corner defining a surrounding area of increased stress associated with ball pads under the area." I agree with that construction.

108. The '245 Patent defines "[a]reas of high stress" as those "***associated with*** the die corner 38a and in particular ***the ball pads which are positioned under the area surrounding the die corner 38a***." (EX1001 at 1:57-59 (emphasis added); *see also* EX1001 at 1:18-21 and 3:6-9.)

109. Petitioner's expert agreed with the general proposition that a corner with ball pads underneath it has more stress than a corner without:

Q. Well, all other things being the same, would a corner with ball pads under it define a high stress area than a corner without ball pads under it?

MR. TAYLOR: Objection, form.

A. If I understand what you're asking, I think the answer is yes, you would have more stress in a corner with ball pads than one without. However, it's

very - - it just depends on the - - you know, the sizes and the thicknesses and all that. But, I mean, in general I would say yes, but not always.

(EX2004 at 60:15–61:4.)

110. Therefore, it is appropriate to construe "area of increased (i.e., high) stress" in accordance with the meaning provided in the specification of the '245 Patent.

111. Patent Owner's proposed construction is also correct because the '245 Patent disavows embodiments in which there is no high stress area associated with ball pads under the die corner.

112. Furthermore, embodiments without ball pads under the corner of the die were disavowed during prosecution.

113. Additionally, Patent Owner's proposed construction comports with the only illustrated embodiment of the '245 Patent.

114. Finally, Patent Owner's proposed construction is correct when viewed in the context of the '245 Patent's purpose of solving the problem of reliably routing signal traces in a high density substrate in which ball pads are disposed in the area around the die corner.

115. For at least these reasons, I agree with Patent Owner's proposed

construction of this limitation to mean "said die having a corner defining a surrounding area of increased stress associated with ball pads under the area" is submitted to be correct and should be adopted by the Board.

C. "within two ball pad pitches of the corner of the die" (Claims 1 and 8)

116. I understand that the Patent Owner Response construes the term "within two ball pad pitches of the corner of the die" in claims 1 and 8 to mean "within two ball pad pitches of the corner of the die in each routing direction defined by the ball pads." (EX1001 at 4:46–51.) I agree with this construction.

117. As noted above, it is my understanding that claim limitations should be construed in the context of the purpose of the invention.

118. Here, the purpose of the invention is to solve the problem of reliably routing signal traces in a high density substrate in which ball pads are disposed in the area around the die corner.

119. The invention solves the problem by defining an area of high stress of a specific size and shape around the die corner and either routing all signal traces outside the high stress area or making sure signal traces routed through the high stress area are not located over the ball pads in the area. (*See, e.g.*, EX1001 at 3:45–50.)

120. However, to ensure high density signal routing, it is important that the

high stress area be no larger than required to eliminate the occurrence of cracks in the signal traces.

121. As illustrated in FIGS. 4 and 5 of the '245 Patent (reproduced below), the aforementioned goal is realized by defining the high stress area as two ball pitches from the corner of the die in each routing direction defined by the ball pads.

122. Routing directions refers to the directions signal traces can be routed from one ball pad to another ball pad.

123. In the embodiment illustrated in FIGS. 4 and 5, it can be seen that the routing directions defined by the ball pads are horizontal, vertical, and diagonal.

124. That is, signal traces may be routed in a horizontal, vertical, or diagonal direction between two ball pads.

125. More specifically, the disclosed area of high stress extends *horizontally* from two ball pad pitches to the left of the die corner to two ball pad pitches to the right of the die corner, *vertically* from two ball pitches below the die corner to two ball pitches above the die corner, *diagonally* from two ball pad pitches to the northwest of the die corner to two ball pad pitches to the southeast of the die corner, and *diagonally* from two ball pad pitches to the southwest of the die corner to two ball pad pitches to the northeast of the die corner.

126. The resulting area of high stress is therefore a polygon in the illustrated embodiment.

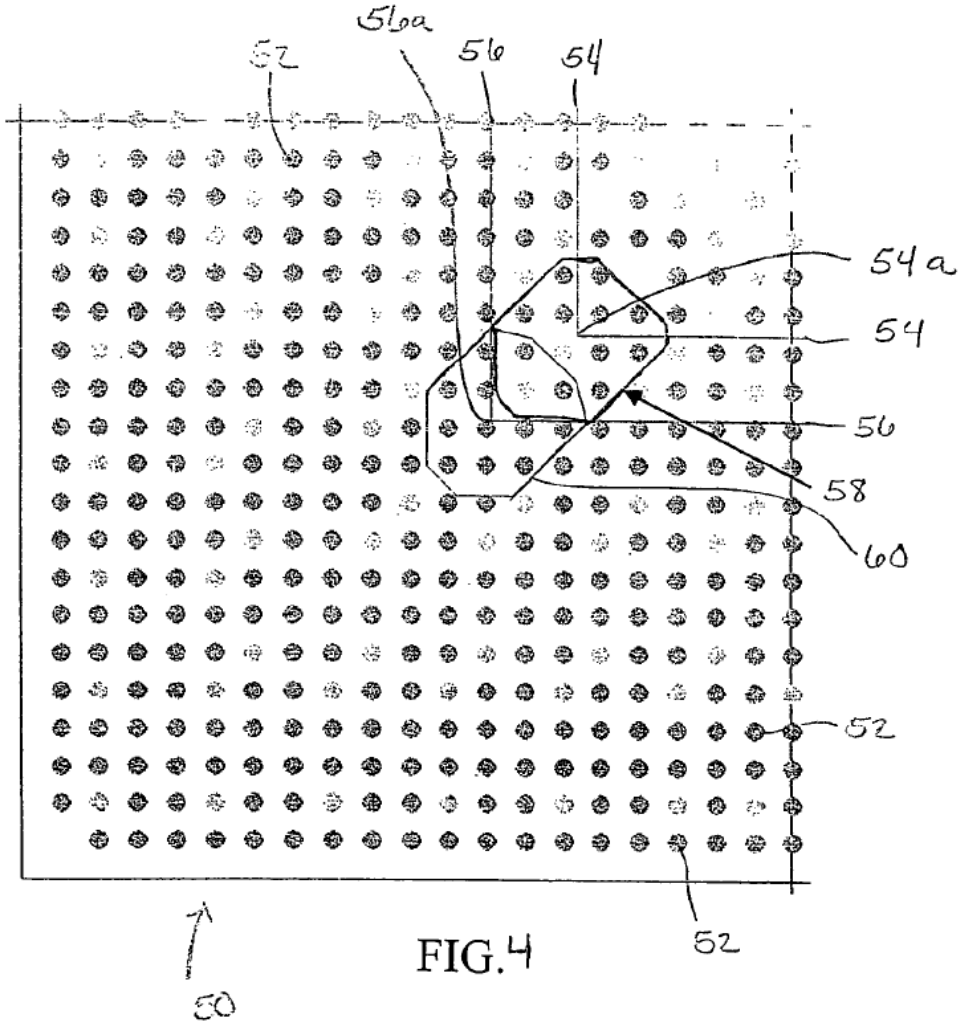


FIG.4

(EX1001 at FIG. 4.)

127. By defining the area of high stress as two ball pad pitches from the die corner in each routing direction defined by the ball pads, the '245 Patent ensures that the high stress area is no larger than required to solve the problem of reliably

routing signal traces in a high density substrate in which ball pads are disposed in the area around the die corner.

128. If, for example, the high stress area was defined as a circle large enough to circumscribe the polygon shown in FIGS. 4 and 5, restrictions on signal routing would be imposed in certain areas of the circle outside the polygon that would needlessly reduce signal density without increasing reliability.

129. Conversely, if the high stress area was defined as a circle small enough to fit inside the polygon shown in FIGS. 4 and 5, cracking of signal traces routed outside the circle but within two ball pad pitches of the die corner would occur.

130. Thus, Patent Owner's proposed construction is correct when viewed in the context of the purpose of the invention.

131. Patent Owner's proposed construction is also supported by the only disclosed embodiment of the '245 Patent, which clearly shows the high stress areas bounded in the horizontal, vertical, and diagonal directions corresponding to signal trace routing directions defined by the ball pads. (*See, e.g.*, EX1001 at FIGS. 4 and 5; *see also* EX1001 at 3:24–8.)

132. Additionally, Patent Owner's proposed construction is correct because the '245 Patent disparages the "existing solution" in which a circular shaped area

with a one millimeter radius is defined using the die corner as the center and traces are routed around the circular region. (EX1001 at 2:6–15 ("A disadvantage of having a one (1) millimeter radius region under the die corner 38a is that it is not sufficient to avoid trace cracks in the layer L8 under temperature cycling conditions for all packaging technologies.").)

133. In contrast, the size of the high stress area in the '245 Patent is based on ball pad pitch and the shape is based on routing directions defined by the ball pads, thereby establishing an area that is no larger than required to eliminate cracking of signal traces and accommodating a range of die sizes.

134. For at least these reasons, I agree with Patent Owner's proposed construction of this limitation to mean "within two ball pad pitches of the corner of the die in each routing direction defined by the ball pads."

IX. ARGUMENT

A. PETITIONER HAS FAILED TO SATISFY ITS BURDEN UNDER 35 U.S.C. § 316(e)

1. Ground 4: Devnani-AAPA Does Not Render Obvious Claims 1, 2, 4, and 5

135. Ground 4 of the Petition alleges that the combination of Devnani (EX1005) and AAPA (EX1001) ("Devnani-AAPA") renders claims 1, 2, 4, and 5 obvious.

136. However, I disagree that Devnani-AAPA renders claims 1, 2, 4, and 5 obvious because, as noted above, Petitioner has not shown that the purported AAPA is in fact prior art nor has Petitioner shown that Devnani by itself renders claims 1, 2, 4, and 5 obvious.

137. Furthermore, even if the purported AAPA is considered prior art, Petitioner has not shown by a preponderance of evidence that the proposed combination of Devnani and AAPA renders claims 1, 2, 4, and 5 obvious.

a. Devnani-AAPA Fails to Render Obvious Claim 1

138. Claim 1 is directed to a semiconductor package comprising, among other things, an area "wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die." (EX1001 at 4:17–20.)

139. As noted above, the term "wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die" should be construed to mean "wherein the plurality of ball pads includes ball pads disposed in an area within two ball pad pitches of the corner of the die and wherein none of the signal traces of the bottom routing layer are located over the ball pads in the area."

140. Furthermore, as noted above, the term "within two ball pad pitches of the corner of the die" in claim 1 should be construed to mean "within two ball pad pitches of the corner of the die in each routing direction defined by the ball pads."

141. The proposed Devnani-AAPA combination fails to render obvious claim 1 for at least the following reasons.

(i) The Proposed Devnani-AAPA Combination Lacks Ball Pads Within the Alleged High Stress Area

142. As noted above, when properly construed, claim 1 requires ball pads to be disposed in an area within two ball pad pitches of the corner of the die.

143. Petitioner identified an alleged high stress zone in the proposed Devnani-AAPA combination, (*see, e.g.*, Pet. at 36–42), but presented no evidence that ball pads are disposed within the alleged high stress zone.

144. The thrust of Petitioner's argument is that Devnani-AAPA shows all of the signal traces being routed away from a high stress zone associated with the corner of the die; and, with all signal traces being routed away from the high stress zone, the claim limitation "none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer" is met. (*Id*..)

145. Petitioner then goes on to talk about the limitation "two ball pad pitches of the corner of the die" and how the purported AAPA renders it obvious.

(*Id*. at 37–41.)

146. What Petitioner doesn't mention is that it deliberately parsed the claim language to leave out the phrase—"which are disposed in an area within"—that connects the former limitation with the latter limitation.

147. As noted above, when the phrases are read together, the full limitation reads "wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die."

148. This conveys a much different meaning, as it refers to "ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die," meaning the package ***must have ball pads in the defined area***.

149. The lack of ball pads in the alleged high stress zone in the proposed Devnani-AAPA combination is manifest in annotated Figure 3 of Devnani (reproduced below) that is "annotated to illustrate where a die quadrant resides when the IC die is mounted upon the package 300 and to identify the AAPA high stress zone associated with the corner of the die. . . . signal traces 200 of the bottom routing layer are routed from edges of the die and around an area (e.g., the AAPA high stress zone) associated with the die corner." (Pet. at 36.)

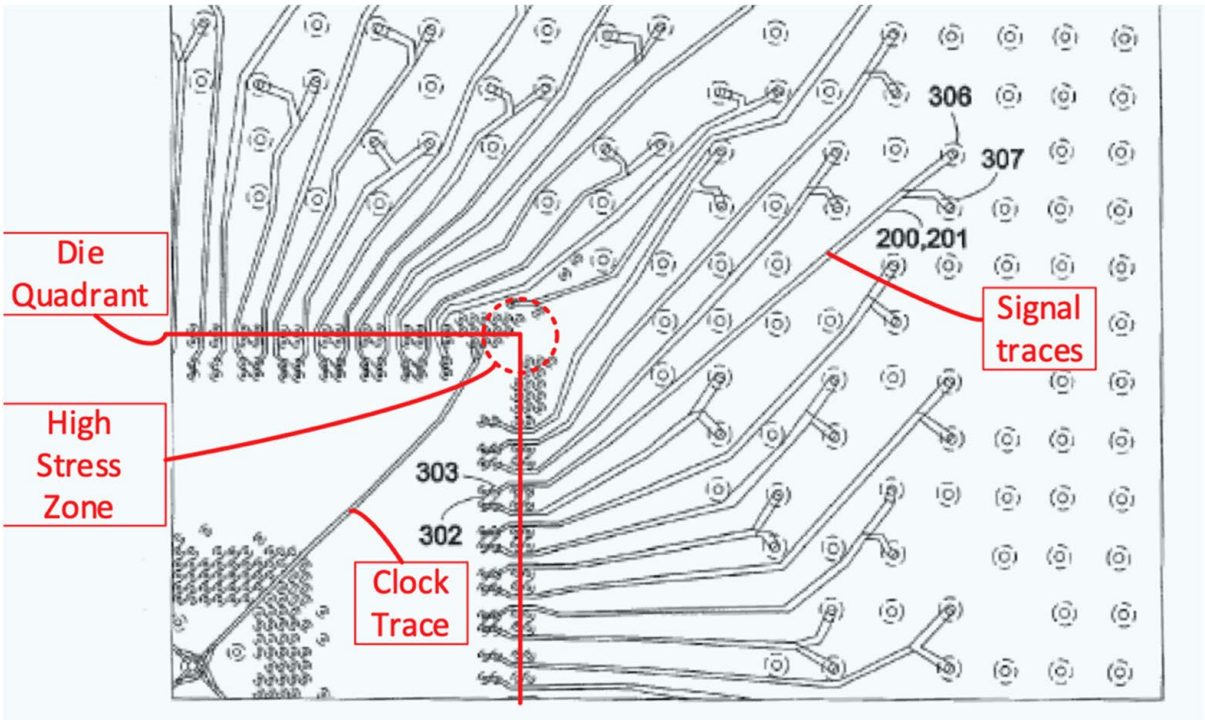
150. Devnani explains that elements 306, 307 in Figure 3 are vias that

connect to solder balls 401 (not shown). (EX1005 at ¶[0023].)

151. Each of the vias is depicted as a circular hole surrounded by a phantom circle.

152. There are numerous vias depicted in Figure 3, but they are all located far away from the die.

153. None of the vias (and, thus, none of the solder balls on the bottom layer) are located below the die, much less in an area within two ball pitches of the die corner.



Devnani Figure 3 (Annotated by Petitioner)

(Pet. at 37 (EX1005, FIG. 3 annotated.)

154. No ball pads are highlighted or annotated by Petitioner. (Pet. at 37–42.)

155. In fact, Petitioner's expert admitted that he doesn't know if there are ball pads disposed in the alleged high stress zone identified by Petitioner:

> Q. Are there any ball pads under the alleged high-stress zone in the annotated version of Figure 3 of Devnani?
>
> MR. TAYLOR: Objection, form.
>
> A. I - - I don't know. I do know there's no signal traces routed there, and that's what the claim is requiring. So the signal traces be routed away from the high-stress corners.

(EX2004, 49:22–50:8.)

156. Since the alleged high stress zone of the proposed Devnani-AAPA combination includes no ball pads, Petitioner has failed to show by a preponderance of evidence that claim 1 is obvious over Devnani-AAPA.

(ii) The Alleged High Stress Zone in the Proposed Devnani-AAPA Combination Is Not an Area Within Two Ball Pad Pitches of the Die

Corner in Each Routing Direction Defined by the Ball Pads

157. As noted above, when properly construed, claim 1 defines an area of increased stress within two ball pad pitches of the corner of the die in each routing direction defined by the ball pads.

158. In the '245 patent, the routing directions defined by the ball pads are horizontal, vertical, and diagonal, and that's why the area of increased stress in the illustrated embodiment of the claimed invention is polygonal in shape.

Petitioner's expert admitted as much during his deposition:

Q: Okay. Would you agree that the shape of
the high-stress zone 58 in Figures 4 and 5 [of the '245 Patent] is
polygonal?
MR. TAYLOR: Objection, form.
A: Is that maybe -- is that what they call it
in the patent and I just don't recall?
Q: I'm asking you if you think it would be
fair to characterize the shape that's shown in
Figures 4 and 5 as polygonal?
MR. TAYLOR: Objection, form.

A: I don't recall what that word means. Are

you talking polygonal?

Q: Yeah.

A Oh. Yeah. I think so.

(EX2004, 78:10–79:1.)

Petitioner's expert also admitted that the shape of the high stress zone in Figures 4 and 5 of the '245 Patent is different than the circularly shaped high stress zones of the alleged AAPA and the proposed Devnani-AAPA combination:

Q. But you agree that the high-stress zone 58 in Figures 4 and 5 of the '245 patent is not a circular shape?

A. What they've labeled there for 58 and 60 are not circles, no.

(EX2004, 81:4–8.)

159. Petitioner fails to explain why the shape of the high stress area in the illustrated embodiment of the '245 Patent differs from the circular high stress area in the alleged AAPA, much less provide a claim construction analysis proving that the two ball pad limitation covers a circularly shaped high stress area like the

alleged AAPA or the proposed Devnani-AAPA combination.

160. Petitioner simply alleges in a conclusory manner that claim 1 does not require a particular shape of a high stress zone. (Pet. at 40–41.)

161. As explained above, this is not true.

162. Claim 1 defines an area within two ball pad pitches of the corner of the die, which when read in light of the specification would be understood by a POSITA to mean two ball pad pitches in each routing direction defined by the ball pads.

163. No evidence has been presented that the routing directions defined by the ball pads of the alleged AAPA or Devnani would constitute a circle.

164. In fact, the circular shape of the alleged AAPA is disavowed by the '245 Patent and none of the illustrated embodiments of the '245 patent show a circular high stress area. (EX1001 at 1:11–15 ("A disadvantage of having a one (1) millimeter radius region under the die corner 38a is that it is not sufficient to avoid trace cracks in the layer L8 under temperature cycling conditions for all packaging technologies.") 3:22–30 ("Each high stress zone 58, 60 is similarly shaped . . . ", FIG. 4, FIG. 5.)

165. For these additional reasons, Petitioner has failed to show by a preponderance of evidence that claim 1 is obvious over Devnani-AAPA.

(iii) It Would Not Have Been Obvious For The Alleged High Stress Zone in the Proposed Devnani-AAPA Combination To Have a Radius of Two Ball Pad Pitches

166. Even if the Board rejects Patent Owner's proposed constructions relating to the term "wherein none of the signal traces in the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die," Petitioner has not proven by a preponderance of evidence that it would have been obvious to define a high stress zone in the proposed Devnani-AAPA combination within two ball pad pitches of the corner of the die.

167. Petitioner concedes that Devnani does not explicitly define an area of high stress within "two ball pad pitches of the corner of the die," as claimed. (Pet. at 37.)

168. For this element, Petitioner relies exclusively on AAPA.

169. However, a consequence of there being no ball pads under the corner of Devnani is that, even if the purported AAPA is prior art, there would have been no reason for a POSITA to look to the purported AAPA for a solution.

170. That is, since Devnani Figure 3 does not have ball pads of the ball pad layer disposed in the area surrounding the die corner where they can cause

cracking, there would be no reason to look to the purported AAPA for a solution because the problem the alleged AAPA is purported to solve is ball pads causing cracking.

171. In particular, there is no basis for Petitioner's addition of a high stress zone defined by a one millimeter circle centered on the corner of the die in Devnani Figure 3.

172. As explained above, the two ball pad pitch implementation of claim 1 differs from the fixed one (1) millimeter radius in that, among other things, the two ball pad pitch implementation is not fixed in size and can therefore accommodate a variety of dies and ball pad pitch sizes.

173. Even though Petitioner mischaracterizes the two ball pad pitch implementation as merely being a larger version of the 1 mm solution, the actual size depends on the ball pad pitch of the package.

174. As the '245 Patent explains, the two ball pad pitch implementation depends on the size of the die and how the ball pads are dispersed. ('245 Patent at 2:36–39; 3:10–30; FIG. 4.)

175. The Petition fails to account for this key fact.

176. The two ball pad pitch implementation of claim 1 (as opposed to hard-coding a 1 mm circle) is critical to the invention to "reduce cracks in the signal

traces and therefore avoids functional failures caused by stresses under the die corner." ('245 Patent at 2:16–18.)

177. Contrary to Petitioner's assertions, the size or shape of the high stress zone is clearly defined by the language of claim 1 and in view of the '245 Patent's specification. ('245 Patent at 4:10–20, 2:36–39, 3:10–30, FIGS. 4, 5.)

178. Petitioner also presents contradictory obviousness arguments.

179. For example, Petitioner contradicts itself within the same paragraph by stating in one sentence that "a POSITA would naturally select [] ***any size or shaped area*** they believe would result in reducing failures due to trace cracks[]" and in the next sentence stating that "a POSITA would have anticipated success in reducing the number of stress cracks in signal traces by routing signal traces around a ***larger area than 1 mm*** from the corner of the die . . . " (Pet. at 41.)

180. Petitioner's obviousness ground on claim 1 cannot stand on such contradictory positions where on one hand the high stress zone can be anything a POSITA believes is correct and on the other hand, it must be an area larger than 1 mm.

181. The configuration of the claimed "area within two ball pad pitches of the corner of the die" is significant because it reduces cracks in the signal traces and avoids functional failures caused by stresses under the die corner for all

packaging technologies. ('245 Patent at 2:16–19, 37–39.)

182. The one-size-fits-all approach of the 1 mm radius does not. ('245 Patent at 2:12–15.)

183. Furthermore, there is no evidence that the high stress zone drawn by Petitioner in annotated FIG. 3 of Devnani-AAPA has a radius of two ball pad pitches.

184. In fact, Petitioner's expert admits that he doesn't know the size of the alleged high stress zone Petitioner identified in Devnani-AAPA Figure 3:

> Q. So how large is the high-stress zone in the annotated version of Figure 3 of Devnani?
>
> MR. TAYLOR: Objection, form.
>
> A. I mean, it would be whatever size it needs to be. I was just highlighting the corner of the chip, or the die, to show that's where the high-stress region was. It would depend on the size of the die, the thickness of the die. It's - - the ***whole point of the circle was just to show the corner of the die***, which is where the claim requires or defines the high - - increased area of high stress or area of increased stress. And

> so, I mean, I could shrink it, and I don't think it would change my opinion. It's just I wanted to show the signals were routed away from that corner.

(EX2004, 45:2–18.)

185. Petitioner argues that a POSITA would have been motivated to use a larger area based on the discussion in the '245 Patent about the disadvantages of the purported AAPA solution. (Pet. at 27–28.)

186. According to Petitioner, such larger area "would include an area defined by 2 ball pad pitches from the corner of the die." (Pet. at 28.)

187. There are at least two major problems with these arguments.

188. First, Petitioner has not shown that the disadvantages of the purported AAPA solution were known in the prior art.

189. In full, the '245 Patent merely states "[a] disadvantage of having a one (1) millimeter radius region under the die corner 38a is that it is not sufficient to avoid trace cracks in the layer L8 under temperature cycling conditions for all packaging technologies." (EX1001 at 1:11–15.)

190. The '245 Patent does not say the disadvantage was known in the prior art, or common knowledge, or otherwise, and there is absolutely no analysis in the

Petition showing that the disadvantages were known in the prior art.

191. It's simply assumed by Petitioner. Therefore, it's improper for Petitioner to rely on the stated disadvantage for motivation to modify the purported AAPA solution.

192. At deposition, Petitioner's expert was evasive on whether he agreed with the Board that there is no disclosure in the '245 Patent that the disadvantages associated with the existing solutions were known in the art:

> Q: So do you disagree or agree with the statement in the Institution Decision on page 20 at lines 6 through 13?
>
> MR. TAYLOR: Objection, form.
>
> A: I don't -- I don't disagree with what the APJs had written there, but I don't necessarily agree.

(EX2004, 20:8–14.)

193. Second, even if the disadvantage was known in the prior art (which Petitioner has not even tried to show), there's simply no support for Petitioner's argument that "an area larger than 1 mm from the corner of the die . . . would

include an area defined by 2 ball pad pitches from the corner of the die."

194. Petitioner has not proffered any evidence to support the notion that any high stress zone larger than the purported AAPA solution would encompass the "two ball pad pitches" limitation.

195. Third, with regard to Petitioner's allegation that "there is no specific disclosure regarding any advantages, criticality, or unexpected results related to [the "two ball pitch" limitation]," this is provably false.

196. In fact, the '245 Inventors stated that the purported AAPA solution is "not sufficient to avoid trace cracks . . . under temperature cycling conditions for all packaging technologies," (EX1001 at 2:11–15), that "an improved package is needed," (*id.* at 2:16–18), and that "[t]he present invention provides such a package," (*id.* at 2:19).

197. In other words, the inventors believed that, unlike the purported AAPA solution, the claimed invention was sufficient to avoid trace cracks under temperature cycling conditions ***for all packaging technologies***.

198. This is certainly an advantage and a significant improvement over the purported AAPA solution.

199. A POSITA reading the '245 Patent would also understand that the "two ball pad pitch" limitation is advantageous and significant in that it provides

an adjustable solution suitable "for all packaging technologies" (e.g., the "area of increased stress" adjusts to accommodate packages having ball grids with different ball pitches) as opposed to a one-size-fits-all fixed radius area like the purported AAPA solution.

200. The invention of claim 1 is thus distinguishable from the cases cited by Petitioner relating to simple changes in size/proportion and shape. (*See* Pet. at 8–9.)

201. Claim 8 does not recite a change in the size of the semiconductor package, and the "two ball pad pitch" limitation of claim 8 differs from the fixed one (1) millimeter radius in that it is not fixed in size and can therefore accommodate a variety of ball pad pitch sizes.

202. The size of the zone in the alleged prior art was fixed regardless of the size of the die (i.e., not scalable).

203. The claimed package performs differently from the alleged prior art in being less prone to cracking and more reliable "for all packaging technologies" due to the adjustability of the "two ball pad pitches" limitation.

204. Finally, I understand that, in the case cited by Petitioner (i.e., *In re Dailey*, 357 F.2d 669 (C.C.P.A. 1966)), there was no evidence that the particular configuration of the claimed disposable plastic nursing container was significant.

Here, the configuration of the claimed package is significant because it is less prone to cracking than alleged prior art packages and is more reliable "for all packaging technologies" due to the adjustability of the "two ball pad pitches" limitation.

205. For at least the foregoing reasons, it is my opinion that claim 1 is patentable over the proposed Devnani-AAPA combination.

b. Ground 4 Fails to Render Obvious Claim 2

206. Dependent claim 2 recites a package as recited in claim 1, wherein:

> none of the signal traces of the bottom routing layer are located within two ball pad pitches of the corner of the die.

(EX1001 at 4:21–23.)

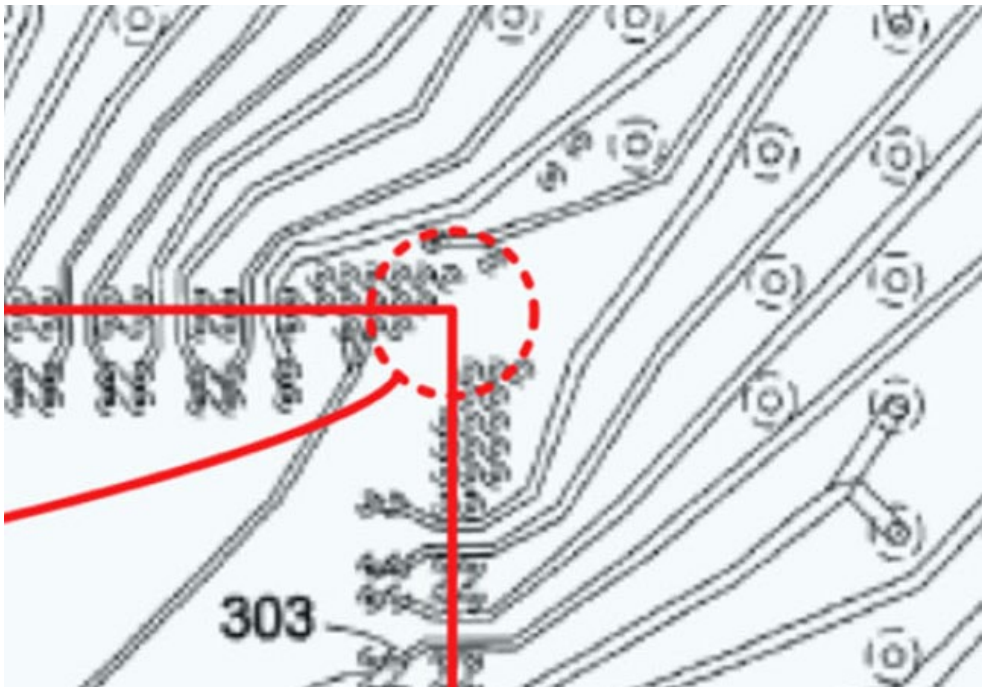
207. It is my understanding that a dependent claim contains all of the limitations of the claim or claims from which it depends.

208. Therefore, claim 2 distinguishes over Devnani-AAPA for at least all of the reasons discussed in above with regard to claim 1.

209. Nor has Petitioner shown that the combination of Devnani-AAPA would exhibit a complete lack of signal traces in the area located within two ball

pad pitches of the corner of the die.

210. On the contrary, even in Petitioner's annotated version of Figure 3 of Devnani reproduced below, the alleged high stress zone encompasses a signal trace (near an upper portion of the circle) and therefore does not meet the claim limitation "wherein none of the signal traces of the bottom routing layer are located within two ball pad pitches of the corner of the die."



(Pet. at 22 (Annotation by Petitioner) (enlarged).) This is not surprising since Petitioner's expert admitted that he does not even know where the ball pads are located in Devnani.

Q. Are there any ball pads under the alleged high-stress zone in the annotated version of Figure 3 of Devnani?

MR. TAYLOR: Objection, form.

A. I - - I don't know. I do know there's no signal traces routed there, and that's what the claim is requiring. So the signal traces be routed away from the high-stress corners.

(EX2004, 49:22–50:8.)

211. Thus, it is my opinion that claim 2 is patentable over Devnani-AAPA for this additional reason.

c. Ground 4 Fails to Render Obvious Claim 4

212. Dependent claim 4 recites a package as recited in claim 1, wherein:

> the package comprises nine layers with the routing layer being the eighth layer and the ball pad layer being the ninth layer, on a bottom of the package.

(EX1001 at 4:28–31.)

213. It is my understanding that a dependent claim contains all of the limitations of the claim or claims from which it depends.

214. Therefore, claim 4 distinguishes over Devnani-AAPA for at least all

of the reasons discussed above with regard to claim 1.

215. Moreover, Devnani does not disclose a package with the routing layer being the eighth layer and the ball pad layer being the ninth layer.

216. Aside from a conclusory statement that "[a] POSITA would have been motivated to combine the AAPA 9-layer stackup 20 with the package 30 of Devnani to route signals, power, and ground between a die and PCB," (Pet. at 43-44), Petitioner has not shown that it would be obvious to modify Devnani to include these additional limitations of claim 4. As such, it is my opinion that claim 4 is patentable over Devnani-AAPA for this additional reason.

d. Ground 4 Fails to Render Obvious Claim 5

217. Dependent claim 5 recites a package as recited in claim 1, wherein:

> the die is mounted to the top layer in an arrangement other than a pin connection.

(EX1001 at 4:32–34.)

218. It is my understanding that a dependent claim contains all of the limitations of the claim or claims from which it depends.

219. Therefore, claim 5 distinguishes over Devnani-AAPA for at least all of the reasons discussed above with regard to claim 1.

2. Ground 1 Fails to Render Obvious Claim 8 Over Devnani-AAPA

220. With regard to claim 8, it is my opinion that Petitioner has failed to show by a preponderance of evidence that Devnani-AAPA renders obvious claim 8 because, as noted above, Petitioner has not shown that the purported AAPA is in fact prior art nor has the Petitioner shown that the differences between Devnani and claim 8 would have been obvious.

221. Furthermore, even if the purported AAPA is considered prior art, Petitioner has not shown that claim 8 would have been obvious over the proposed Devnani-AAPA combination.

222. Claim 7, from which claim 8 depends, recites a semiconductor package comprising the following limitations:

> a top layer having a die mounted thereon, ***said die having a corner defining a surrounding area of increased stress***;
>
> and
>
> a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces thereon, and ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads

> dispersed thereon, ***wherein none of the signal traces of the bottom routing layer are located within the area of increased stress defined by the corner of the die***.

(EX1001 at 4:38–48 (emphasis added).)

223. Claim 8 further recites:

> ***wherein none of the signal traces of the bottom routing layer are located within two ball pad pitches of the corner of the die***.

(EX1001 at 4:49–51 (emphasis added).)

224. With regard to the claimed "area of increased stress," the '245 Patent explains that "[a]reas of high stress are associated with the die corner . . . and in particular ***the ball pads which are positioned under the area surrounding the die corner*** . . . ." (EX1001 at 1:58–60 (emphasis added); *see also id*. at 3:6–9, 28–30, and 45–50.)

225. The edges of the ball pads on the bottom-most layer under the area surrounding the die corner act as stress concentration points that, under temperature cycling conditions, may initiate cracks that can extend upward through the dielectric layer and damage signal traces on the bottom routing layer above the ball pads. (*Id*. at 1:61–2:2.)

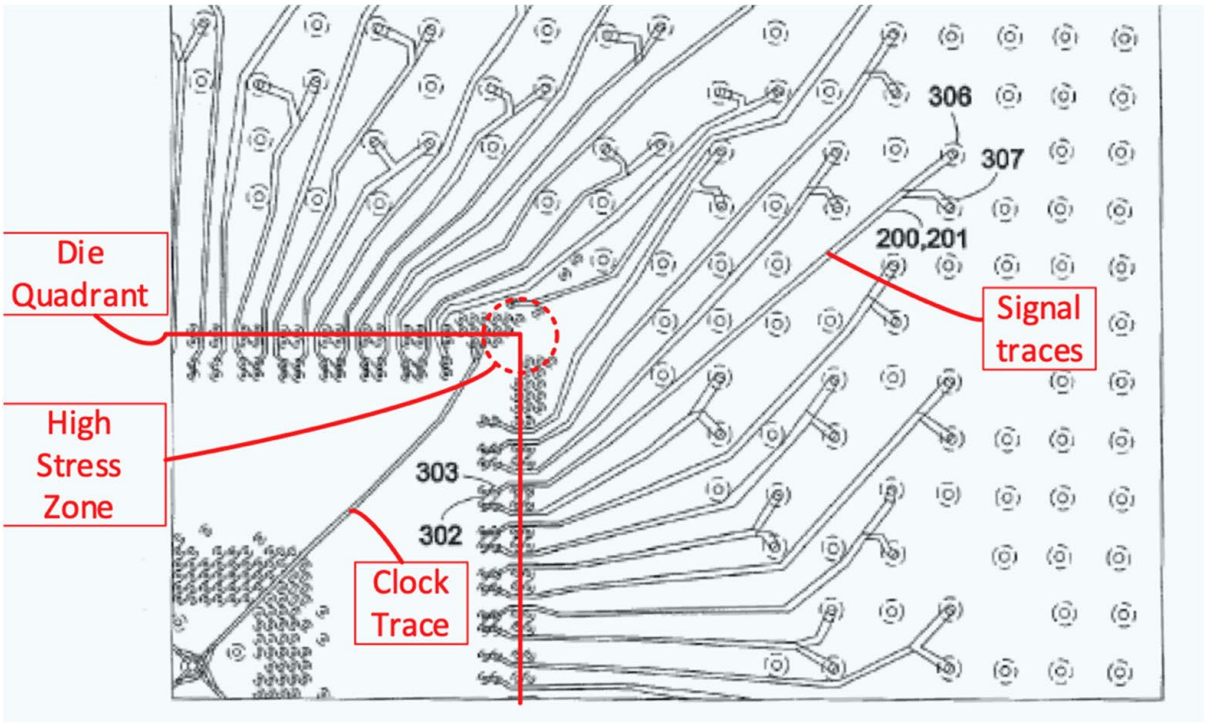
226. The invention of claim 8 solves this problem by routing signal traces such that "none of the signal traces of the bottom routing layer are located within two ball pad pitches of the corner of the die." (*Id*. at 4:49–51.)

227. Even if the purported AAPA is considered prior art, the invention of claim 8 would not be obvious over Devnani in view of AAPA for at least the following reasons.

228. Petitioner relies heavily on an annotated version of Figure 3 of Devnani-AAPA (reproduced below) to attack claim 8.

229. While Petitioner admits that Devnani does not ***explicitly*** state that the die corner in the figure defines a surrounding area of increased stress, it is argued that there is implicitly an area of increased stress near the die corner due to different thermal expansion characteristics. (Pet. at 18.)

230. As illustrated below, Petitioner annotated Figure 3 to show an alleged high stress zone of circular shape centered on the die corner. (*Id*.)



231. Petitioner argues that Devnani-AAPA Figure 3 shows all of the signal traces routed outside the alleged high stress zone. (Pet. at 22.)

232. As backup, Petitioner argues that a POSITA implementing the semiconductor package of Devnani would look to the purported AAPA to route signal traces away from the alleged high stress zone in Figure 3. (*Id.*)

233. What Petitioner doesn't say about Figure 3 of Devnani is important—there are no ball pads on the bottom layer below the alleged area of increased stress surrounding the corner of the die.

234. Devnani explains that elements 306, 307 in Figure 3 are vias that connect to solder balls 401 (not shown). (EX1005 at ¶[0023].)

235. Each of the vias is depicted as a circular hole surrounded by a phantom circle.

236. There are numerous vias depicted in Figure 3, but they are all located far away from the die.

237. None of the vias (and, thus, none of the solder balls on the bottom layer) in Petitioner's annotated Figure 3 are located below the alleged area of increased stress surrounding the die corner.

238. As explained above, when properly construed, the claimed "area of increased stress" in claim 8 is associated with ball pads below an area surrounding the die corner—not just thermal cycling.

239. The ball pads act as "stress concentration points." (EX1001 at 1:61–65.)

240. Because there are no ball pads around the corner acting as stress concentration points, Devnani does not have "a corner defining a surrounding area of increased stress" as claimed.

241. The consequences of this omission by Petitioner are two-fold.

242. First, since Devnani does not have "a corner defining a surrounding area of increased stress" as claimed, there would be no reason to look to the purported AAPA for a solution to a non-existent problem.

243. Second, even if Devnani is considered to have a corner defining a surrounding area of increased stress due solely to different thermal characteristics between the die and substrate, Petitioner has not shown that a POSITA would look to the purported AAPA for a solution, since the purported AAPA is focused on a different problem due to ball pads under an area surrounding the corner causing cracking, and there are no ball pads within Petitioner's alleged high stress zone around the die corner in Devnani.

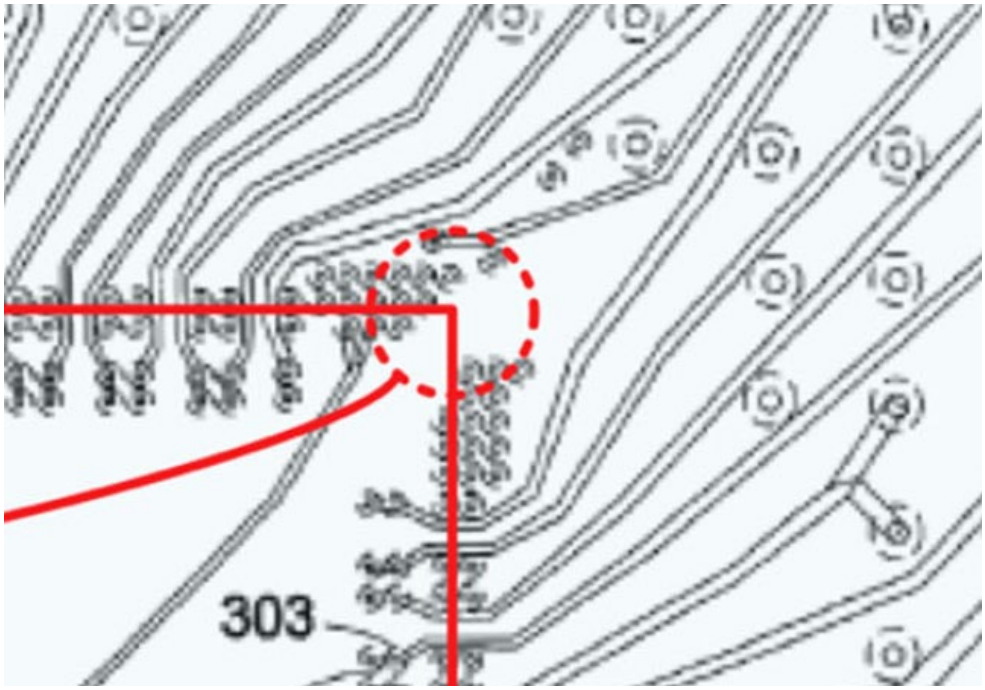
244. In particular, there is no basis for Petitioner's addition of a high stress zone defined by a one millimeter circle centered on the corner of the die in Figure 3 of Devnani.

245. Furthermore, as explained previously, the term "within two ball pad pitches of the corner of the die" in claim 8 should be construed to mean "within two ball pad pitches of the corner of the die in each routing direction defined by the ball pads."

246. No evidence has been presented that two ball pad pitches in each routing direction defined by the ball pads of the alleged AAPA or Devnani would result in a circular region as proposed by Petitioner.

247. Finally, it should be noted that, even in Petitioner's annotated version of Figure 3 of Devnani reproduced below, the alleged circular high stress zone

encompasses a signal trace (near an upper portion of the circle) and therefore does not meet the claim limitation "wherein none of the signal traces of the bottom routing layer are located within the area of increased stress defined by the corner of the die."



(Pet. at 22 (Annotation by Petitioner) (enlarged).)

248. Even if the Board rejects Patent Owner's proposed constructions relevant to claim 8, in my opinion Petitioner has not proven that it would have been obvious to define the surrounding area of increased stress in the proposed Devnani-AAPA combination as an area within two ball pad pitches of the corner of the die.

249. Petitioner concedes that Devnani does not explicitly define an area of high stress within "two ball pad pitches of the corner of the die," as claimed. (Pet. at 27.)

250. For this element, Petitioner relies exclusively on AAPA. (*Id*.)

251. However, a consequence of there being no ball pads under the corner of Devnani is that, even if the purported AAPA is considered prior art (which it should not be), there would have been no reason to look to the purported AAPA for a solution.

252. That is, since Devnani Figure 3 does not have ball pads of the ball pad layer disposed in the area surrounding the die corner where they can cause cracking, there would be no reason to look to the purported AAPA for a solution because the problem the alleged AAPA is purported to solve is ball pads causing cracking.

253. Petitioner argues that a POSITA would have been motivated to use a larger area based on the discussion in the '245 Patent about the disadvantages of the purported AAPA solution. (Pet. at 27–28.)

254. According to Petitioner, such larger area "would include an area defined by 2 ball pad pitches from the corner of the die." (Pet. at 28.)

255. There are at least three major problems with these arguments.

256. First, Petitioner has not shown that the disadvantages of the purported AAPA solution were known in the prior art.

257. In full, the ’245 Patent merely states “[a] disadvantage of having a one (1) millimeter radius region under the die corner 38a is that it is not sufficient to avoid trace cracks in the layer L8 under temperature cycling conditions for all packaging technologies.” (EX1001 at 1:11–15.)

258. The ’245 Patent does not say the disadvantage was known in the prior art, or common knowledge, or otherwise, and there is absolutely no analysis in the Petition showing that the disadvantages were known in the prior art.

259. It’s simply assumed by Petitioner. Therefore, it’s improper for Petitioner to rely on the stated disadvantage for motivation to modify the purported AAPA solution.

260. At deposition, Petitioner’s expert was evasive on whether he agreed with the Board that there is no disclosure in the ‘245 Patent that the disadvantages associated with the existing solutions were known in the art:

Q: So do you disagree or agree with the statement in the Institution Decision on page 20 at lines 6 through 13?

MR. TAYLOR: Objection, form.

A: I don't -- I don't disagree with what the APJs had written there, but I don't necessarily agree.

(EX2004, 20:8–14.)

261. Second, even if the disadvantage was known in the prior art (which Petitioner has not even tried to show), there's simply no support for Petitioner's argument that "an area larger than 1 mm from the corner of the die . . . would include an area defined by 2 ball pad pitches from the corner of the die." (Pet. at 28.)

262. This is nothing more than hindsight analysis. Petitioner has not proffered any evidence to support the notion that any high stress zone larger than the purported AAPA solution would encompass the "two ball pad pitches" limitation.

263. Third, with regard to Petitioner's allegation that "there is no specific disclosure regarding any advantages, criticality, or unexpected results related to [the "two ball pitch" limitation]," (Pet. at 28), this allegation is provably false.

264. In fact, the '245 Inventors stated that the purported AAPA solution is "not sufficient to avoid trace cracks . . . under temperature cycling conditions for all packaging technologies," (EX1001 at 2:11–15), that "an improved package is needed," (*id.* at 2:16–18), and that "[t]he present invention provides such a

package," (*id.* at 2:19).

265. In other words, the inventors believed that, unlike the purported AAPA solution, the claimed invention was sufficient to avoid trace cracks under temperature cycling conditions ***for all packaging technologies***.

266. This is certainly an advantage and a significant improvement over the purported AAPA solution.

267. A POSITA reading the '245 Patent would also understand that the "two ball pad pitch" limitation is advantageous and significant in that it provides an adjustable solution suitable "for all packaging technologies" (e.g., the "area of increased stress" adjusts to accommodate packages having ball grids with different ball pitches) as opposed to a one-size-fits-all fixed radius area like the purported AAPA solution.

268. Furthermore, there is no evidence that the high stress zone drawn by Petitioner in annotated FIG. 3 of Devnani-AAPA has a radius of two ball pad pitches.

269. In fact, Petitioner's expert admits that he doesn't know the size of the alleged high stress zone Petitioner identified in Devnani-AAPA Figure 3:

Q. So how large is the high-stress zone in the annotated version of Figure 3 of Devnani?

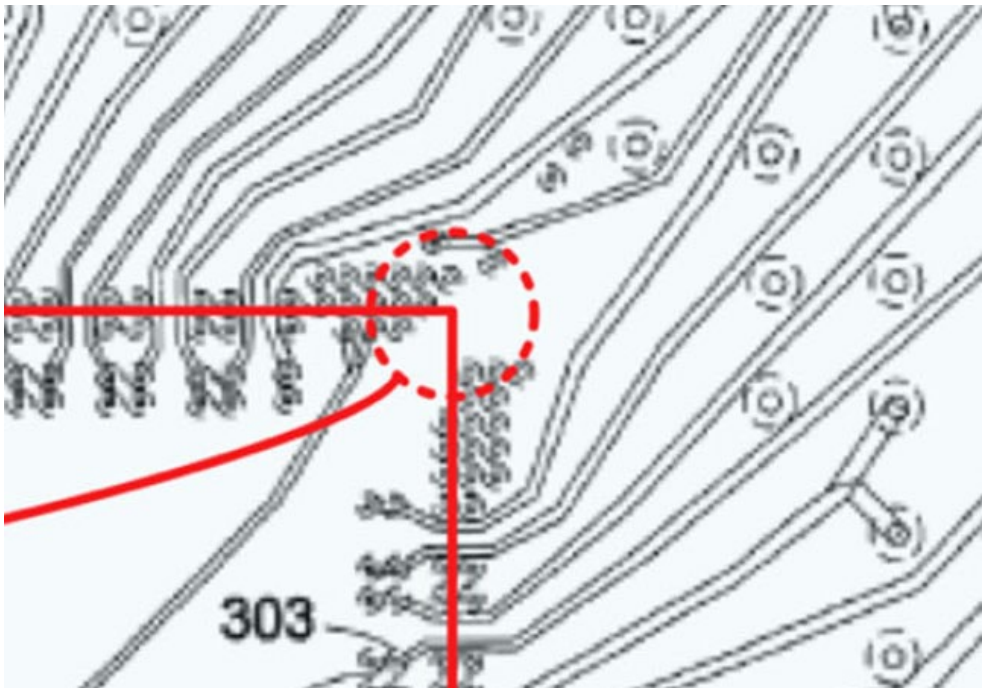
MR. TAYLOR: Objection, form.

A. I mean, it would be whatever size it needs to be. I was just highlighting the corner of the chip, or the die, to show that's where the high-stress region was. It would depend on the size of the die, the thickness of the die. It's - - the ***whole point of the circle was just to show the corner of the die***, which is where the claim requires or defines the high - - increased area of high stress or area of increased stress. And so, I mean, I could shrink it, and I don't think it would change my opinion. It's just I wanted to show the signals were routed away from that corner.

(EX2004, 45:2–18.)

270. Indeed, even in Petitioner's annotated version of Figure 3 of Devnani reproduced below, the alleged high stress zone "as disclosed by AAPA" (Pet. at 22) encompasses a signal trace (near an upper portion of the circle) and therefore does not meet the claim limitation "wherein none of the signal traces of the bottom routing layer are located within the area of increased stress defined by the corner of the die."

271. If the alleged high stress zone in Petitioner's annotated version of Figure 3 was made to have a radius larger than 1mm, it could encompass additional signal traces, thereby further distancing the proposed combination from claim 8.



(Pet. at 22 (Annotation by Petitioner) (enlarged).

3. Ground 5 Fails to Render Obvious Claim 3 Over Devnani-AAPA-Pillai

272. Dependent claim 3 recites a package as recited in claim 1, wherein:

> said ball pad layer has a plurality of ball pads dispersed thereon and no metal traces on the ball pad layer which are connected to the ball pads.

(EX1001 at 4:24-27.)

273. It is my understanding that a dependent claim contains all of the limitations of the claim or claims from which it depends.

274. Ground 5 does not rely on Pillai to overcome the deficiencies of Devnani-AAPA noted above in Ground 4 with respect to claim 1, from which claim 3 depends.

275. Therefore, claim 3 distinguishes over Devnani-AAPA for at least the same reasons noted above in the discussion of claim 1 with regard to Ground 4.

276. Indeed, there is no analysis of Pillai in any respect in Ground 5—only a reference to a different section of the Petition and the Baker Declaration. (Pet. at 45.)

277. In any event, Devnani, AAPA, and Pillai are all silent regarding metal traces being connected to bond pads on the bond pad layer.

278. The vias in Pillai are for connecting the ball pads to other layers of the package.

279. The partial cross-section in FIG. 1 of Pillai, by itself, is insufficient to prove that Pillai lacks metal traces connected to bond pads anywhere else on the bond pad layer or to provide motivation to forego metal traces on the bond pad layer.

280. Thus, it is my opinion that claim 3 is patentable over Devnani-AAPA-Pillai for this additional reason.

4. Ground 6 Fails to Render Obvious Claim 6 Over Devnani-AAPA-Tanahashi

281. Dependent claim 6 recites a package as recited in claim 1, wherein:

> the signal traces on the bottom routing layer comprise at least one voltage bus bar.

(EX1001 at 4:35–37.)

282. Claim 6 depends from claim 1.

283. Since a dependent claim contains all of the limitations of the claim or claims from which it depends, claim 6 distinguishes over Devnani-AAPA for at least the same reasons discussed above in with regard to claim 1.

284. Petitioner relies on Tanahashi for allegedly disclosing the additional limitations of claim 6, not for overcoming the deficiencies of Devnani-AAPA with respect to claim 1, from which claim 6 depends.

285. Therefore, claim 6 is patentable over Devnani-AAPA-Tanahashi for at least the same reasons discussed above with regard to claim 1.

286. In my opinion, claim 6 is further patentable over Devnani-AAPA-Tanahashi for the additional limitations it recites because Petitioner's annotations

of Figure 3B of Tanahashi, by themselves, are insufficient to prove that the power wiring conductor P1 in FIG. 3C of Tanahashi is a voltage bus bar on the bottom routing layer.

5. Ground 7: Chung-Celeron Does Not Render Obvious Claims 1, 2, and 5

287. Claim 1 recites, among other things, that "none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die." (EX1001 at 4:17–20.)

288. As explained previously, the proper construction of this claim term requires ball pads to be disposed in an area within two ball pad pitches of the corner of the die.

289. Petitioner alleges that claim 1 would have been obvious over Chung in view of Celeron ("Chung-Celeron").

290. More specifically, without citing any evidence regarding the purpose of the clear area in Celeron, Petitioner alleges that a POSITA would have been motivated to combine the multiple routing layers of Chung with the clear area of Celeron to prevent damage to signal traces of the bottom routing layer during thermal cycling. (Pet. at 52.) I disagree.

291. First, as shown in FIG. 3 of Chung (reproduced below with Petitioner's annotations), the electrical assembly of Chung includes an integrated circuit 302 (IC) mounted on a top surface 312 of a vertical section 304 that includes "multiple conductive layers arranged in parallel with a vertical plane." (EX1006 at [0026].)

292. The vertical section is arranged on top of a horizontal section 306 that includes "conductive layers arranged in parallel with a horizontal plane." (EX1006 at [0026].)

293. Thus, the conductive layers of the vertical section are arranged perpendicular to the conductive layers of the horizontal section.

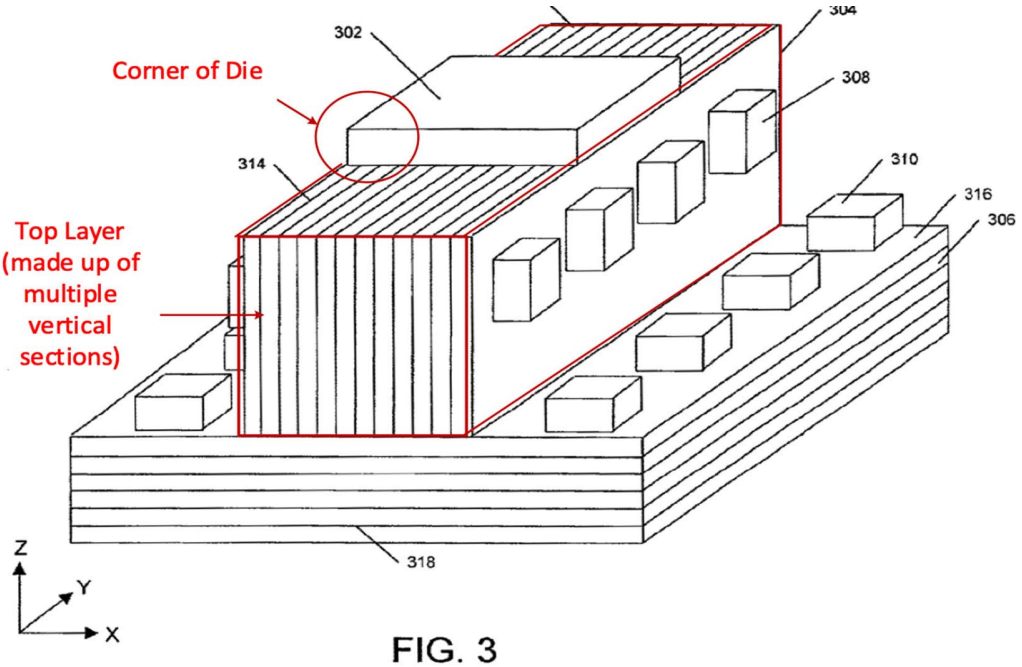


FIG. 3

(EX1006, Fig. 3 annotated.)

294. During his deposition, Petitioner's expert agreed that the layers of the vertical section in Chung are perpendicular to the layers of the horizontal section:

> Q: And the layers of the vertical package section in Chung are oriented perpendicular to the horizontal package section, correct?
>
> Mr. Taylor: Objection, form.
>
> A: Yeah. The portion that is made up of the vertical package section 304 is perpendicular to the horizontal packaging Section 306.

(EX2004, 83:20–84:4.)

295. As shown in Fig. 5 of Chung (reproduced below with Petitioner's annotations), Petitioner identifies the conductive layer 544 in the horizontal section of Chung as corresponding to the bottom routing layer of claim 1.

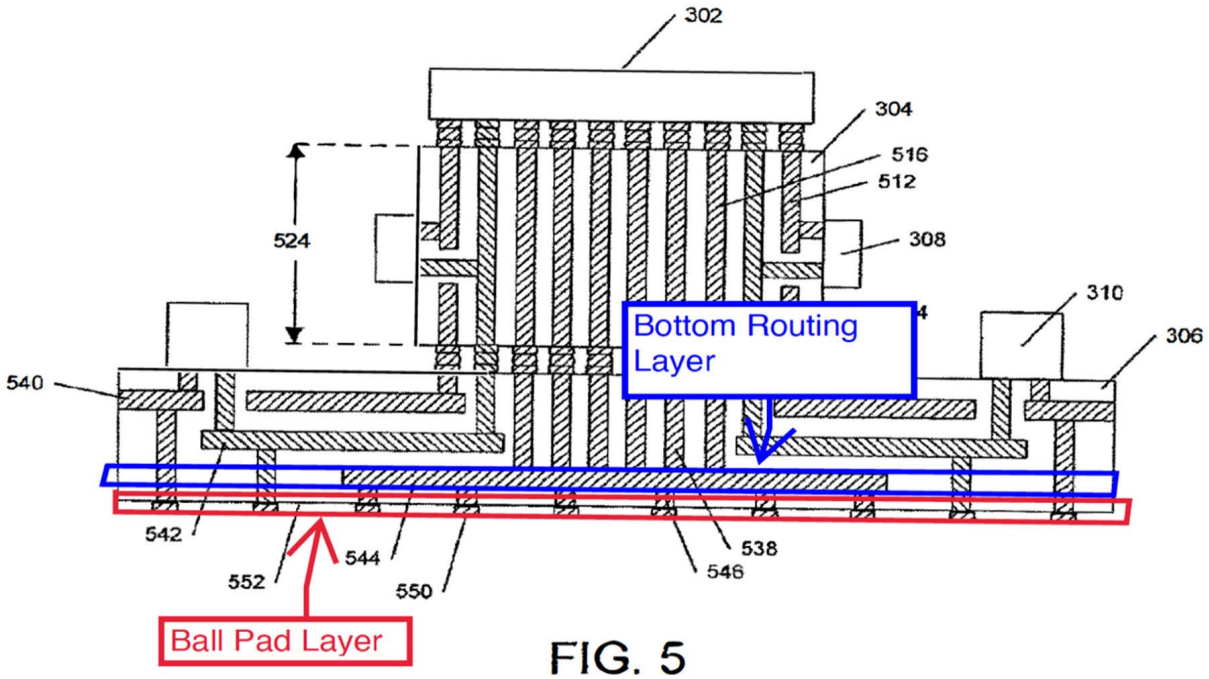


FIG. 5

296. However, Petitioner provides no evidence that forming a clear area in the center of the bond pad layer 550 in Chung is necessary to prevent damage to a signal trace of a conductive layer in the horizontal package section during thermal cycling.

297. Neither Celeron nor any of the other references cited in the Petition teach that the corner of a die mounted on top of vertical layers would be associated with increased stress in horizontal layers disposed perpendicularly below the vertical layers.

298. Absent evidence showing same, there would be no motivation to combine Chung and Celeron in the manner proposed.

299. In fact, since one of the functions of the horizontal section in Chung can be to convert the pitch along the x-axis from the bond pad pitch of the IC to a larger bond pad pitch in the bond pad layer[1], (EX1006 at [0038]), and whereas forming a clear area in the bond pad layer like Celeron would tend to reduce pitch by reducing the area available for the bond pads, a POSITA would actually be motivated not to combine Chung and Celeron as proposed.

300. Even if there were motivation to combine Chung and Celeron as proposed, the proposed Chung-Celeron combination would not include ball pads in an area within two ball pad pitches of the of the corner of the die as required by claim 1.

301. In the proposed combination of references in Ground 7, Petitioner admits that Chung does not explicitly show that "none of the signal traces of the

[1] Petitioner alleges that bond pads 550 in Figure 5 of Chung correspond to the ball pad layer of claim 1. (Pet. at 48.) However, it should be noted that, contrary to Petitioner's assertions, bond pads are not the same as ball pads. Ball pads serve as mounts for solder balls, whereas bond pads form connections with solder balls. (EX1006 at [0053) The proposed combination fails for this reason as well.

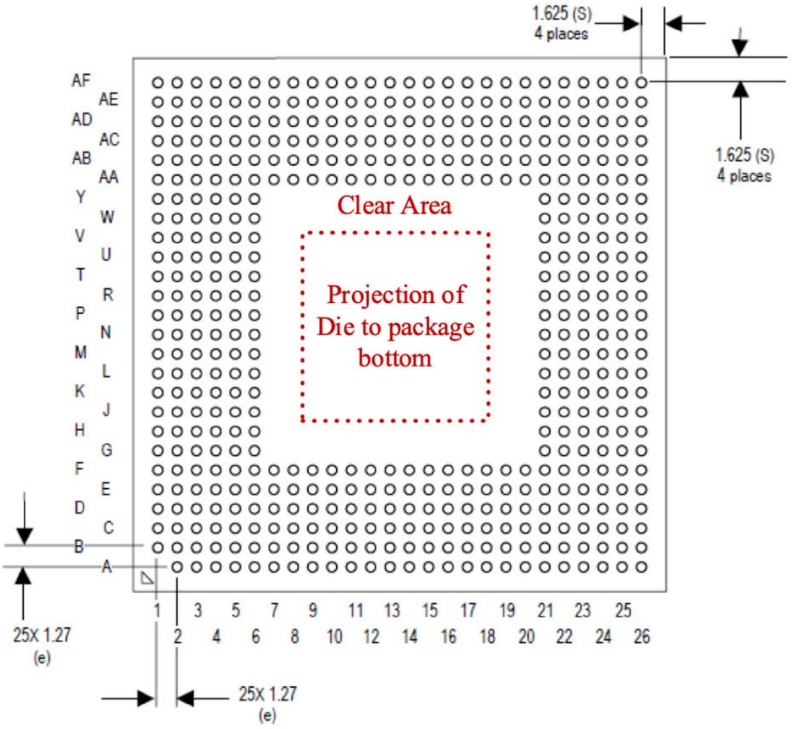
bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die," (Pet. at 48), and relies on Celeron for this limitation, (*id.* at 48–53).

302. However, as admitted by Petitioner, "Celeron discloses that there are no ball pads in the ball pad layer 'disposed in an area within two ball pad pitches of the corner of the die.'" (Pet. at 52.)

303. Thus, the proposed combination would not have "ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die."

304. This deficiency is clearly shown in annotated Figure 30 of Celeron (Pet. at 51), reproduced below, in which a large area surrounding the corner of the die is free of ball pads.

305. Petitioner even labels the area around the die without ball pads as "Clear Area."



306. Moreover, Chung and Celeron both fail to show the signal traces, so even if there were ball pads in the "Clear Area," it has not been proven that they meet the claim limitation "wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die," in claim 1.

307. Petitioner's expert confirmed that the Chung-Celeron combination lacks important limitations:

> Q: And does the combination proposed in paragraph 141 of your declaration include ball pads within two ball pad pitches of the corner of the die?

MR. TAYLOR: Objection, form.

A: The ball pads in the combination are not within two ball pad pitches of the corner of the die. They would be outside the corner of the die as I discussed in paragraphs 140 and 141.

(EX2004, 94:12–20.)

308. For at least the above reasons, the proposed Chung-Celeron combination fails to render claim 1 obvious.

309. Claims 2 and 5 depend from claim 1.

310. It is my understanding that a dependent claim contains all of the limitations of the claim or claims from which it depends.

311. Therefore, claims 2 and 5 distinguish over Chung-Celeron for at least the same reasons discussed above with regard to claim 1.

6. Ground 8: Chung-Celeron-Pillai Do Not Render Obvious Claim 3

312. Claim 3 depends from claim 1.

313. It is my understanding that a dependent claim contains all of the

limitations of the claim or claims from which it depends.

314. Ground 8 does not rely on Pillai to overcome the deficiencies of Chung-Celeron noted above with respect to claim 1, from which claim 3 depends.

315. Therefore, claim 3 distinguishes over Chung-Celeron for at least the same reasons noted above in the discussion of claim 1 with regard to Ground 7.

316. In any event, Chung, Celeron, and Pillai are all silent regarding metal traces being connected to bond pads on the bond pad layer.

317. The vias in Pillai are for connecting the ball pads to other layers of the package.

318. The partial cross-section in FIG. 1 of Pillai, by itself, is insufficient to prove that Pillai lacks metal traces connected to bond pads anywhere else on the bond pad layer or to provide motivation to forego metal traces on the bond pad layer.

319. For these reasons, it is my opinion that Petitioner has not met its burden with respect to claim 3.

7. Ground 9: Obviousness of Claim 4 Over Chung in View of Celeron and AAPA

320. Claim 4 depends from claim 1.

321. It is my understanding that a dependent claim contains all of the

limitations of the claim or claims from which it depends.

322. Ground 9 does not rely on the purported AAPA to overcome the deficiencies of Chung-Celeron with respect to claim 1, from which claim 4 depends.

323. Therefore, it is my opinion that claim 4 is patentable over Chung-Celeron-AAPA for at least the same reasons discussed above with regard to claim 1 and Chung-Celeron.

8. Ground 10: Obviousness of Claim 6 over Chung in view of Celeron and Tanahashi

324. Claim 6 depends from claim 1.

325. Since it is my understanding that a dependent claim contains all of the limitations of the claim or claims from which it depends, claim 6 distinguishes over Chung-Celeron for at least the same reasons discussed above with regard to claim 1.

326. Petitioner relies on Tanahashi for allegedly disclosing the additional limitations of claim 6, not for overcoming the deficiencies of Chung-Celeron with respect to claim 1, from which claim 6 depends.

327. Therefore, it is my opinion that claim 6 is patentable over Chung-Celeron-Tanahashi for at least the same reasons discussed above with regard to

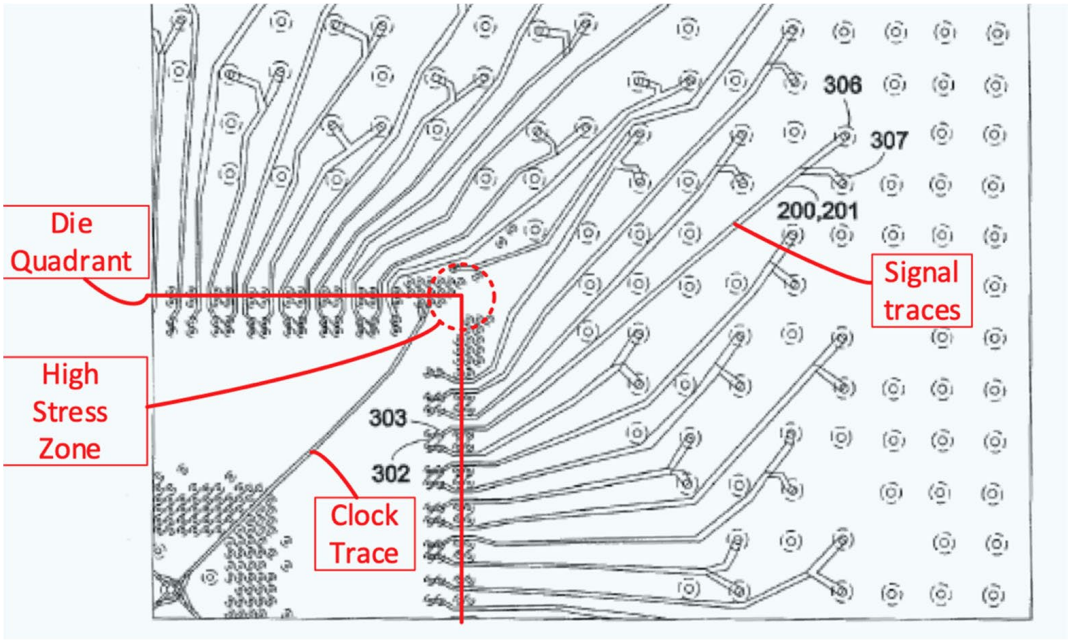
claim 1.

328. In my opinion, claim 6 is also patentable over Chung-Celeron-Tanahashi for the additional limitations it recites because Petitioner's annotations of Figure 3B of Tanahashi, by themselves, are insufficient to prove that the power wiring conductor P1 in FIG. 3C of Tanahashi is a voltage bus bar on the bottom routing layer.

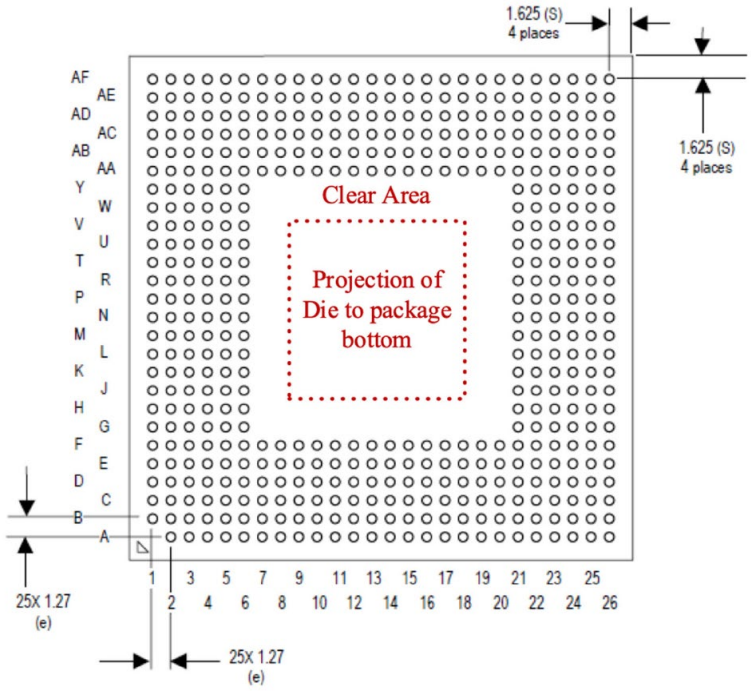
9. Ground 11: Obviousness of Claims 1 and 5 Over Devnani in View of Celeron

329. Petitioner fails to show that Devnani-Celeron would render claim 1 obvious because, as noted above, (Ground 4) and (Ground 7), the limitation "ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die" in claim 1 should be construed to mean "wherein the plurality of ball pads includes ball pads disposed in an area within two ball pad pitches of the corner of the die and wherein none of the signal traces of the bottom routing layer are located over the ball pads in the area," and neither Devnani Figure 3 nor Figure 30 of Celeron have ball pads within such an area relative to the die corner.

330. *See* Petitioner's Annotated Figure 3 of Devnani (EX1005) and Petitioner's Annotated Figure 30 of Celeron (EX1008) reproduced below.



(Devnani, Figure 3 (Annotated by Petitioner).)



(Celeron, Figure 30 (Annotated by Petitioner).)

331. As such, neither Devnani nor Celeron would experience the problem described in the '245 Patent and, even if combined, the proposed combination would not have ball pads in Petitioner's alleged high stress zone around the corner of the die.

332. Therefore, the proposed combination would not include all the limitations of claim 1, which require ball pads in such a zone around a corner of a die.

333. Claim 5 depends from claim 1.

334. Since it is my understanding that a dependent claim contains all of the limitations of the claim or claims from which it depends, claim 5 distinguishes over Devnani-Celeron for at least the same reasons discussed immediately above in this Section with regard to claim 1.

10. Ground 12: Claim 6 Is Not Rendered Obvious by Devnani-Celeron-Tanahashi

335. Claim 6 depends from claim 1. Since it is my understanding that a dependent claim contains all of the limitations of the claim or claims from which it depends, claim 6 distinguishes over Devnani-Celeron for at least the same reasons discussed above in with regard to claim 1.

336. Petitioner relies on Tanahashi for allegedly disclosing the additional limitations of claim 6, not for overcoming the deficiencies of Devnani-Celeron with respect to claim 1, from which claim 6 depends.

337. Therefore, it is my opinion that claim 6 is patentable over Devnani-Celeron-Tanahashi for at least the same reasons discussed above with regard to claim 1.

338. In my opinion, claim 6 is further patentable for the additional limitations it recites because Petitioner's annotations of Figure 3B of Tanahashi, by themselves, are insufficient to prove that the power wiring conductor P1 in FIG. 3C of Tanahashi is a voltage bus bar on the bottom routing layer.

339. I reserve the right to revise, supplement, and/or amend my opinions in this declaration based on future positions taken by Petitioner and/or their experts, additional documents, testimony, or other information provided by Petitioner or its witnesses, any orders from the Court, or as I may otherwise find necessary and to offer rebuttal analyses and/or opinions to any such positions of the Petitioner.

340. I expect to continue to develop my opinions discussed in this report. I also reserve the right to supplement my opinions based on information obtained from additional discovery or from Petitioner's experts, as indicated above.

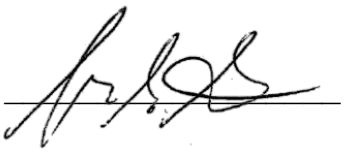
341. When called upon to do so, I will offer testimony at trial or otherwise

regarding these opinions and will offer rebuttal testimony as appropriate throughout the remainder of this proceeding.

342. I currently hold the opinions expressed in this declaration, but my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

343. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code and that any such willful false statements may jeopardize the validity of the patent at issue in this proceeding.

Dated: August 21, 2024



Dr. Joseph Bernstein

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Professional Summary

Professor Bernstein's expertise lie in several areas of micro-electronic devices, packaging and system reliability, including failure analysis, process variations and reliability prediction. He is a world recognized expert in GaN and SiC power device reliability and on advanced electronic packaging. He has worked directly with companies producing DRAM and SDRAM, SRAM and Flash memory. He has worked also with MEMS and laser programmable metal interconnect. Included in electronic systems are Power Electronic devices, flip-chip devices, packaging and physics of failure research including memory devices, gate oxide integrity and radiation effects. He has licensed his own technology and consulted for RFID, Flash, and other memory related companies including Sandisk, Cypress and Freescale. He directs the Laboratory for Failure Analysis and Reliability of Electronic Systems, teaches VLSI design courses and heads the VLSI program at Ariel University. His Laboratory is a center of research activity dedicated to serving the needs of manufacturers of highly reliable electronic packaging and systems using commercially available off the shelf parts. Research areas include thermal, mechanical, and electrical interactions of failure mechanisms of ultra-thin gate dielectrics, Non-Volatile memory, advanced metallization and power devices. He also works extensively with the semiconductor industry on projects relating to failure analysis, defect avoidance, programmable interconnect used in Field Programmable Gate Arrays and repair in microelectronic circuits and packaging. He has developed an important method for predicting device failure rates based on new JEDEC standards for multiple failure rate-based prediction. Professor Bernstein was a Fulbright Senior Researcher/Lecturer at Tel Aviv University in the Department of Electrical Engineering, Honored lecturer at "Nanorun," and at IEEE Summer-School in Toulouse, France. Professor Bernstein is a senior member of IEEE.

Expertise

- Microelectronics and Electronic Device and System Design and Reliability
- Power Electronics Devices and Architecture
- Advanced Packaging of Electronic Devices
- SiC and GaN Power Device Reliability
- DRAM, SDRAM, SRAM & Flash (NAND and NOR) Memory Cells
- Electronics Lifetime Prediction
- Failure Analysis of Electronic Circuits
- Fuse Processing for Redundancy and Memory Repair
- Gate Oxide Integrity of in Ultra-Thin Gate Dielectrics
- Hot Carrier Degradation of Nanometer Scale Devices
- Processing of Semiconductor Devices and Wafers and Packaging (Ball Grid Array).
- Materials Processing for Advanced Semiconductor Devices
- Materials Processing for MEMS Applications
- Multiple Failure Rate Modeling and Lifetime Prediction
- Programmable Gate array architecture, layout and redundancy
- Semiconductor Device Processing Materials and Technologies
- Thermal Fatigue of Electronic Circuit Boards
- GaN Power Semiconductor Devices

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Education

Year	College or University	Degree
1990	Massachusetts Institute of Technology	Ph.D., Electrical Engineering and Computer Science, GPA: 5.0/5.0
1987	Massachusetts Institute of Technology	E.E., Electrical Engineer, GPA: 5.0/5.0
1986	Massachusetts Institute of Technology	M.S., Electrical Engineering and Computer Science, GPA: 5.0/5.0
1984	Union College, Schenectady, NY	B.S., Electrical Engineering, GPA: 3.9/4.0 Summa Cum Laude

Professional Experience

From: 2012
To: Present
Organization: Ariel University, Israel
Title: Professor, Faculty of Engineering

From: 2009
To: Present
Organization: Reliability International Associates LLC, Reliability consulting company
Title: Founder and Owner

From: 2007
To: 2012
Organization: Bar Ilan University, Israel
Title: Professor, Faculty of Engineering

From: 2003
To: 2005
Organization: Tel-Aviv University, Israel
Summary:

2003 – 2005 Visiting Associate Professor of Engineering, Faculty of Engineering

2004 – 2005 Fulbright Senior Scholar

From: 1995
To: 2008
Organization: University of Maryland

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Summary:

2001 – 2007 Associate Professor, Mechanical Engineering

1995 – 2001 Assistant Professor of Reliability, Materials and Nuclear Engineering Dept.

Summer 1998 NASA/ASEE Summer Faculty Research Fellow, JPL, Pasadena, CA.

From: 2002
To: 2006
Organization: LaserLink Technology, LLC (Maryland based)
Title: Owner

From: 1995
To: 1997
Organization: Lightspeed Semiconductor, Inc.
Title: Founder and Chief Scientist

From: 1991
To: 1993
Organization: Boston University
Title: Adjunct Professor

From: 1990
To: 1995
Organization: MIT Lincoln Library, Lexington, MA
Title: Research Staff

Litigation Support Experience

Expert Engagement:

Type of Matter: Jury Trial for Trade Secret Violation under and NDA
Law Firm: Bejin Bieneman PLC | 2000 Town Center, Suite 800 | Southfield, MI 48075 313-528-4882 | www.b2iplaw.com
Case Name: **MERSEN USA EP CORP., v. TDK ELECTRONICS INC.**
UNITED STATES DISTRICT COURT
SOUTHERN DISTRICT OF NEW YORK **Case No. 21-cv-00763**
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and testimony for the plaintiff, Mersen USA
Disposition: Settled highly favorably for the Plaintiff!
Date: 2023

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Expert Engagement:

Type of Matter:	Jury Trial for Reliability fraud
Law Firm:	ORRICK HERRINGTON & SUTCLIFFE 405 Howard Street San Francisco, California 94105-2675
Case Name:	**Allied Telesis K.K. v. Micron Technology, Inc.** **Santa Clara County, CA Case No. 2015-1-CV-282977**
Services Provided:	Engaged as Expert providing expert reports, depositions, expert analysis and testimony for the defendant, Micron Technology, Inc.
Disposition:	Settled favorably for the Defendant
Date:	2021-2022

Expert Engagement:

Type of Matter:	Due-Diligence Consulting and Patent Analysis
Law Support Firm:	Papst Licensing Gmbh, Germany and Detroit
Case Name:	Trolling software development
Services Provided:	Engaged as Expert providing consulting and analysis of a portfolio of IBM patents in order to validate a developing software and provide due-diligence support.
Disposition:	Found none of hundreds of patents useful to pursue.
Date:	2021-2022

Expert Engagement:

Type of Matter:	Inter-Parte Review defending patent owner.
Law Firm:	SKIERMONT DERBY LLP
Case Name:	ADVANCED SEMICONDUCTOR ENGINEERING, INC.,PETITIONER, V. BELL SEMICONDUCTER LLC, PATENT OWNER. Case No. IPR2021-00180, U.S. Patent No. 6,624,007
Services Provided:	Engaged as Expert providing expert reports, depositions, expert analysis and testimony.
Disposition:	Patent was found unpatentable.
Date:	2021-2022

Expert Engagement:

Type of Matter:	Inter-Parte Review defending patent owner.
Law Firm:	Mishcon De Reya New York, LLP
Case Name:	RPX CORPORATION and AMD, INC. vs. IYM Technologies, LLC. IPR2017-01886 and 88
Services Provided:	Engaged as Expert providing expert reports, depositions, expert analysis and testimony. Patent was found unpatentable. 2018

Expert Engagement:

Type of Matter:	Patent Infringement defending patent owner.
Law Firm:	Lowenstein and Weatherwax, LLP
Case Name:	KINGSTON Technology v. POLARIS Innovations
Services Provided:	Engaged as Expert providing expert reports, depositions, expert analysis and testimony.

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Disposition: 01623 resolved as NOT un-patentable.
Date: 2017

Expert Engagement:
Type of Matter: Patent Infringement defending patent owner.
Law Firm: TENSEGRITY LAW GROUP, LLP
Case Name: KINGSTON Technology v. POLARIS Innovations
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and testimony.
Disposition: Case was dropped after IPR results
Date: 2017

Expert Engagement:
Type of Matter: Patent Infringement defending patent owner.
Law Firm: DLA Piper
Case Name: MIPOX Corp. v. International Test Solutions, Inc. Inter Partes Reviews of US patents 8,801,869; 7,202683; and 6,777,966
Services Provided: Engaged as Expert providing expert reports, expert analysis and testimony.
Disposition: Brought to successful settlement and non-institution of necessary claims.
Date: 2017

Expert Engagement:
Type of Matter: Patent Infringement and validity
Law Firm: Dowling Aaron Incorporated
Case Name: *Beco Dairy Automation, Inc. v. Global Tech Systems, Inc.* (Eastern District of California; 1:12-cv-01310-LJO-SMS
Services Provided: Engaged as Expert providing expert reports, expert circuit analysis and testimony, Claim chart construction and expert testimony covering 8 patents
Disposition: Brought to successful and beneficial settlement
Date: 2016

Expert Engagement:
Type of Matter: Patent Infringement
Law Firm: Nix Patterson, LLP
Case Name: DSS Technology Management, LLC v. Intel Corp., Hynix, Samsung.
Services Provided: Engaged as Expert providing expert reports, expert circuit analysis and testimony.
Disposition: Client pulled out after institution at IPR
Date: 2015

Expert Engagement:
Type of Matter: Patent Infringement
Law Firm: Desmarais, LLP
Case Name: Round Rock Research, LLC v. ACER, INC., and Gateway, Inc.,
Services Provided: Engaged as Expert providing expert reports, expert circuit analysis and testimony, these cases successfully, were settled out of court.
Disposition: Settled
Date: 2014

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Expert Engagement:

Type of Matter:	Patent Interference
Law Firm:	Oblong, Spivak, McClelland, Maier, & Neustadt, PC, for Defendant
Case Name:	Yunlong Sun, Edward J. Swenson and Richard S. Harris v. Donald V. Smart
Services Provided:	Engaged as Expert for over 6 years supporting patent interferences cases involving laser processing in semiconductor devices. Numerous expert reports and depositions as well as interviews at the patent office and testimony.
Disposition:	Company was purchased by the competition.
Date:	2008-2012

Expert Engagement:

Type of Matter:	Patent Re-Examination
Law Firm:	Law Office of Andrew D. Fortney
Case Name:	MIT/UMD appeal to USPTO
Services Provided:	Engaged as Expert writing expert testimony in defense of a patent in the semiconductor field
Disposition:	Successful defense of patent
Date:	2012

Expert Engagement:

Type of Matter:	Patent Infringement
Law Firm:	Townsend Townsend and Crew, LLC
Case Name:	Agere v. Samsung
Services Provided:	Engaged as Expert providing expert reports and testimony, the case was successfully settled out of court.
Disposition:	Settled
Date:	2006

Expert Engagement:

Type of Matter:	Patent Infringement
Law Firm:	Brown & Bain, PA, for Defendant
Case Name:	EMI Group North America, Inc. v. Cypress Semiconductor Corporation
Services Provided:	Engaged as Expert over 3 years providing numerous expert reports and trial testimony defending the company's use of technology in alleged violation of a patent, which we proved in court to have been invalid.
Disposition:	We defeated the patent at trial and sustained on appeal
Date:	2001, 2003

Expert Engagement:

Type of Matter:	Patent Infringement
Law Firm:	Choate Hall & Stewart
Case Name:	GSI v. A-B Lasers
Services Provided:	Engaged as Expert providing hands-on consulting, expert testimony and reports relating to laser processing of silicon wafers for marking technology.
Disposition:	Settled
Date:	2001

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Industrial Consultation and Involvement

Consulting Project:
Client: EPC Corporation
Services Provided: GaN Power Circuit Design, Evaluation and Qualification

Consulting Project:
Client: Sandisk
Services Provided: Test and Reliability Consultant.

Consulting Project:
Client: Maradin Corp.
Services Provided: Accelerated Reliability and Qualification Consulting.

Consulting Project:
Client: Camtek Corp.
Services Provided: Reliability Testing and Qualification Consulting.

Consulting Project:
Client: Essence Corp.
Services Provided: Test and Reliability Consultant providing device lifetime characterization.

Consulting Project:
Client: Marvel Corp.
Services Provided: Test and Reliability Consultant providing important device lifetime characterization.

Consulting Project:
Client: Veraz Telecommunication
Services Provided: System Reliability Consultant providing models and accelerated tests

Consulting Project:
Client: Israel Aircraft Industries
Services Provided: Lecturer and Consultant

Consulting Project:
Client: Cypress Semiconductor
Services Provided: Laser processing consultation and trial expert witness

Consulting Project:
Client: Teradyne Corporation
Services Provided: Device and system reliability consultant

Consulting Project:
Client: Freescale Semiconductor
Services Provided: Device qualification and reliability testing and modeling

Consulting Project:
Client: GSI Lumonics
Services Provided: Improving laser cut and link technologies and expert witness

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Professional Affiliations, Achievements & Awards

Laboratory and Programmatic Affiliations

- Laboratory for Reliability of Advanced Microelectronic Systems, Ariel University – current head
- Laboratory for Reliable Electronic Systems at Ariel University, in collaboration with Israeli industry consortium and Bar Ilan University. (2007-2012).
- Founder and Faculty Advisor: Israel Electronics Manufacturers Working Group on Reliability, ILTAM. (2005-present).
- Assoc. Director, University Research Institute for Nanoscience and Nanotechnology at Tel-Aviv University. (2003-2005).

Awards and Honors

- Expert Panelist and Invited Lecturer for GaN and SiC Power MOSFET, ISTFA 2023
- Excellence in Teaching Award, Ariel University 2021
- 32nd MIEL Serbia, Best Paper Award, 2021
- Tech-Connect Innovation Award 2018 (Through Ariel Scientific Innovations)
- Nanorun, distinguished lecturer and contributor, IRT-Saint Exupery, Feb. 2016
- Windows on Science researcher/lecturer, US Air Force, March 2015
- ChipEx 2014, best paper/lecturer award 2014
- Fulbright Senior Researcher. Lecturer, 2004 – 2005
- IEEE Senior Member, 2003

Teaching and Advising

- Courses Taught in the Last 5 Years
  - Reliability Prediction based on Multiple Accelerated Life Tests – Hobbs, IEEE, NASA, STMicro
  - Why Weibull, Why Not! – Hobbs, IEEE Summer School, Toulouse
  - VLSI Design – Ariel University (Advanced Undergraduate)
  - Reliability Engineering Fundamentals - Ariel University
  - Microelectronics Device Reliability – Ariel University
  - VLSI Analog (1 semester) and Digital VLSI (1 semester) Laboratories – Ariel University

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Project Title	Organization	PI or Co-PI	Funding Amount	Year
Reliability of V-GaN	US ONR	PI	**$400,000**	2023-2026
Microwave GaN Rel	MAFAT (Isr.)	PI	**$60,000**	2023-2024
Power SOC	Israel Innov.	PI/2	**$400,000**	2022-2025
Gate Drive for SiC	US ONR	PI/2	**$450,000**	2021-2024
DSM/WBG Reliability	IRT Saint-Exupery	PI	**$200,000**	2018-2020
GaN Class-D Amplifier	Kamin Israel	PI/2	**$200,000**	2019-2021
GaN Microwave Device	Israel DOD	PI	**$150,000**	2018-2022
GaN Device Reliability	ONR	PI	**$500,000**	2015-2019
Wide Bandgap Device	AFOSR	PI	**$135,000**	2015-2018
FPGA Reliability	USAF	PI	**$150,000**	2014-2015
System Reliability	Magneton Israel	PI	**$100,000**	2012-2013
Power Electronic System Reliability	ONR	PI	**$200,000**	2010-2011
Systems Reliability in Nanotechnology	ONR	PI	**$200,000**	2009-2010
Methods to Account for Early Wear-out	AVSI consortium	PI	**$286,000**	2007 - 2010
MIL HDBK 217 Replacement	Wyle Labs	PI	**$86,608**	2007
Advanced Gate Dielectric Reliability	NIST	PI	**$69,965 (1st year)**	2006-2009
JPL NASA Research Program	JPL	PI	**$65,000**	2006-2007
Microelectronic Systems Reliability	AVSI (Aerospace Corporations)	PI	**$180,000 (5th year)**	2006
Ultra Thin Dielectric Metrology	NIST	PI	**$56,000**	2005
Microelectronic Systems Reliability	AVSI (Aerospace Corporations)	PI	**$210,000 (4th year)**	2005
EDCOT Research Consortium	MAGNET (Tel-Aviv Univ.)	Co-PI (50%)	**$100,000**	2004-2005
Laser programmable device design	NSA	PI	**$50,000**	2004-2005
Microelectronic Systems Reliability	AVSI (Aerospace Corporations)	PI	**$157,000 (3rd year)**	2004
Power Device Reliability	ONR	Co-PI (60%)	**$150,000 per year**	2004-2008
Microelectronic Systems Reliability	AVSI (Aerospace Corporations)	PI	**$198,000 (2nd year)**	2003
Laser programmable device design	NSA	PI	**$50,000**	2002-2003
Place and Route for LPAA	Mission Research Corporation	PI	**$198,000**	2002-2003
Laser MAKELINK development	MIPS (Matrics Corporation)	PI	**$77,000**	2001-2002
Alternate Gate Dielectric Analysis	NIST	PI	**$150,000**	2001-2005
Microelectronic Systems Reliability	AVSI (Aerospace Corporations)	PI	**$175,000 (1st year)**	2002

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Design and Layout of LPGA: Phase I.	BAE Systems Co.	PI	**$43,070**	2000-2001
Wide band-gap power device reliability	ONR	Co-PI (50%)	**$314,804**	2000 - 2003
Laser Process Development	DOD - NSA	PI	**$75,000**	2000 - 2001
Thin Dielectric Metrology	NIST	PI	**$234,000**	1999 - 2005
Laser Process Development	DOD - NSA	PI	**$146,680**	1999 - 2000
Power Semiconductor	NIST	PI	**$42,300**	1999 - 2000
Dielectric Metrology	NIST	PI	**$39,231**	1999 - 2000
Laser Process Reliability	NASA / JPL	PI	**$54,080**	1998
Metrology for Power Device Reliability	COMM - NIST	PI	**$6,000**	1998
W Contact evaluation	DOD - NSA	PI	**$5,270**	1998
Power Device Reliability	ONR	PI	**$150,000**	1997 - 2000
Metal Cut Evaluation	General Scanning	PI	**$25,000**	1997
Gate-Oxide Metrology	NIST	PI	**$124,330**	1996 - 1999
Laser Restructuring / Evaluation	DOD - NSA	PI	**$200,000**	1996 - 1997
Atomic Microscopy and Surface Science	NSA	Co-PI	**$122,810**	1994 - 1997

Equipment Donated:

Donated Item	Donating Agency	Value of Donation
Cold/Hot Burn-In Ovens	Anonymous	$200,000
Laser Timing Probe Microscope	Semicaps	$3.5 Million
Laser Semiconductor Process Equipment	XRL Corporation	$300,000
Laser Semiconductor Process Equipment	Electro Scientific Industries	$700,000
Electromigration Test Equipment	Aetrium Corporation	$150,000

Patents & Publications

Patent	Date	Description
US17626857	9/15/2022	Power converter suitable for high frequencies
US202063039002P	15/06/2020	Control circuit for ring oscillator-based power controller
US 10,746,781	18/08/2020	Ring oscillator test circuit
PCT/IL2016/050476	05/01/2017	Enhancement mode only ring oscillator test circuit
US2014/0052392	02/20/2014	Solder joint life measurement for prognostics
US2015/0039244	02/15/2015	Failure Rate Estimation from Multiple Mechanisms
6,541,868	04/01/2003	Interconnecting Conductive Links
6,057,221	05/02/2000	Laser-Induced Cutting of Metal Interconnect
5,920,727	07/06/1999	Technique for Producing Interconnecting Conductive Links
5,920,789	07/06/1999	Technique for Producing Interconnecting Conductive Links
5,861,325	01/19/1999	Technique for Producing Interconnecting Conductive Links
5,585,602	12/17/1996	Structure for Providing One or More Conductive Paths

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Publications

Book Authorship and Editorship

1. Joseph B. Bernstein, *Reliability Prediction from Burn-In Data Fit to Reliability Models*, Academic Press, 2014, ISBN: 978-0-12-800747-1
2. Joseph B. Bernstein et.al, *Physics-of-Failure Based Handbook of Microelectronic Systems,* Reliability Information Analysis Center, Utica, NY, 2008, ISBN-10: 1-933904-29-1.
3. Mark White, Joseph B. Bernstein, Microelectronics Reliability: Physics-of-Failure Based Modeling and Lifetime Evaluation, NASA JPL Publication, 2008.
4. Mark White, Joseph B. Bernstein, *Microelectronics Reliability Modeling and Lifetime Evaluation Handbook: Derating and Reliability Prediction Guidelines*, NASA JPL Publication, 2007.
5. Pecht, M., Bernstein, J.B., Searls, D., and Peckerar, M., *The Korean Electronics Industry*, CRC Press, 1997 and 2020
6. Hoang, H.H., Schutz, R., Bernstein, J.B., Vasquez, B., *Multi-level Interconnection: Issues that Impact Competitiveness*, Proceedings of SPIE 2090, 1993.

Book Chapters

1. Alain Bensoussan, Joseph B. Bernstein and Alain Bravix, Chapter 1, *Basic Reliability Tools for SHM Protocols*, in "Reliability and Physics-of-Healthy in Mechatronics, Volume 15 - Reliability of Multiphysical Systems Set." ISBN : 978-178-63-0881-8, November 2022.
2. Alain Bensoussan, Joseph B. Bernstein and Alain Bravix, Chapter 2, *Applied Engineering on Physics-of-Healthy and SHM of Microelectronic Equipment for Aeronautic, Space, Automotive and*
3. *transport operations*, in "Reliability and Physics-of-Healthy in Mechatronics, Volume 15 - Reliability of Multiphysical Systems Set." ISBN : 978-178-63-0881-8, November 2022.
4. Joseph B. Bernstein, *Reliability Prediction Considering Multiple Failure Mechanisms,* Chapter in "System Reliability", INTECH Publication, 2017, ISBN 978-953-51-5532-4.
5. Bernstein, J.B., "Laser Link-Making," in *LIA Handbook of Laser Materials Processing*, Magnolia Publishing, 2001.
6. Stark, B., Bernstein, J.B., "Reliability Overview," *MEMS Reliability Assurance Guidelines for Space Applications*, NASA Publication, 1998.

Articles in Refereed Journals

1. *A Chaturvedi, M Sarma, SK Chaturvedi, J Bernstein, "*Performance assessment and RUL prediction of power converters under the multiple components degradation," Microelectronics Reliability Vol.144, (2023) pp. 144958

2. *E Bender, JB Bernstein, DS Boning,* "Mitigation of Thermal Stability Concerns in FinFET Devices," Electronics 11 (20), (2022) pp.3305

3. Clay Mayberry, Joseph Bernstein, "*Reliability and Survivability of Advanced Electronics Technologies,"* AFRL Space Vehicles Directorate, (2022) 3/1

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

4. *E Bender, JB Bernstein, "*Microchip Health Monitoring System Using the FLL Circuit," Sensors vol.7, (2021) pp.2285
5. *E Bender, JB Bernstein, A Bensoussan, "Reliability prediction of FinFET FPGAs by MTOL," Microelectronics Reliability, vol.*114, *(2020)* pp.113809
6. *S. Shaheen, G. Golan, M. Azoulay, J. B. Bernstein, "*A COMPARATIVE STUDY OF RELIABILITY FOR FINFET," *Facta Universitatis, Series: Electronics and Energetics Vol. 31, No 3, September 2018, pp. 343-366*
7. *G. Golan, M. Azoulay, T. Avraham, I. Kremenetsky, J. B. Bernstein, "An improved reliability model for Si and GaN power FET," Microelectronics Reliability Vol. 81 pp. 77-89 (2018)*
8. *J. B. Bernstein, A. Bensoussan, E. Bender, "Reliability Prediction with MTOL," Microelectronics Reliability Vol. 68 pp. 91–97 (2017)*
9. *J. B. Bernstein, M. Gabbay, O. Delly, "Reliability matrix solution to multiple mechanism prediction*," Microelectronics Reliability pp. 2951–2955 (2014).
10. Chung, Kuan-Jung, Martin Peckerar, and Joseph B. Bernstein*. "Design Optimization of Laser-Induced Microbridges for Low Resistance Interline Connections in ICs."* Microelectronic Engineering, Vol. 103, Pages 70–75 (2013).
11. I. Gershman and J. B. Bernstein, "*Structural health monitoring of solder joints in QFN package,"* Microelectronics Reliability, Volume 52, Issue 12*,* Pages 3011–3016 (2012).
12. L. Yang and J. Bernstein, *"Reliability Evaluation and Modeling of High Density Electronic Packages,"* Microelectronics International, vol. 29, no. 1, pp. 15-21 (2012).
13. I. Gershman and J. B. Bernstein, *"Solder-Joint Quantitative Crack Analysis—Ohmic Resistance Approach,"* IEEE Transaction on Components, Packaging and Manufacturing Technology, vol. 2, no. 5, pp. 748 - 755 (2012).
14. L. Yang, R. Niu, J. Xie, B. Qian, B. Song, Q. Rong, J.B. Bernstein, *"Design-for-reliability implementation in microelectronics packaging development,"* Microelectronics International, vol. 28, no. 1, pp. 29-40 (2011).
15. B. Huang, M. Rodriguez, M. Li, J.B. Bernstein, C.S. Smidts, *"Hardware Error Likelihood Induced by the Operation of Software,"* IEEE Trans. on Reliability, vol. 60, no. 3, pp. 622-639 (2011).
16. Kuan-Jung Chung and J.B. Bernstein, *"Experimental investigation of the optimal laser-induced microbridges,"* Precision Engineering, vol. 34, no. 3, pp. 578-585 (2010).
17. B. Yan, J. Qin, J. Dai, Q. Fan, and J.B. Bernstein*, "Reliability Simulation and Circuit-Failure Analysis in Analog and Mixed-Signal Applications,"* IEEE Trans. on Device and Mat. Rel., vol. 9, no. 3, pp. 339-347 (2009).
18. M. Gurfinkel, P. Livshits, A. Rozen, J.B. Bernstein, *"Local Oscillations of On-Die Supply Voltage-A Reliability Issue,"* IEEE Trans. on Device and Mat. Rel., vol. 9, no. 3, pp. 476-482 (2009).
19. L. Yang, Joseph B. Bernstein, T. Koschmieder, *"Assessment of acceleration models used for BGA solder joint reliability studies,"* Microelectronics Reliability Vol. 49, pp. 1546–1554 (2009).
20. L. Yang, Joseph B. Bernstein, *"Failure rate estimation of known failure mechanisms of electronic packages,"* Microelectronics Reliability Vol. 49, pp. 1563-1572 (2009).
21. *X. Li, J. Qin,* and J.B. Bernstein, *"Compact Modeling of MOSFET Wearout Mechanisms for Circuit-Reliability Simulation,"* IEEE Trans. on Device and Mat. Rel., vol. 8, no. 1, pp. 98-121 (2008).

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

22. M. Gurfinkel, H.D. Xiong, K.P. Cheung, J.S. Suehle, J.B. Bernstein, Y. Shapira, A.J. Lelis, D. Habersat, N. Goldsman, *"Characterization of Transient Gate Oxide Trapping in SiC MOSFETs Using Fast I-V Techniques,"* IEEE Transactions on Electron Devices, vol. 55, no.8, pp. 2004-12 (2008).
23. L. Yang, J.B. Bernstein, *"Reliability Study of High-Density EBGA Packages Using the Cu Metalized Silicon,"* IEEE Transaction on Components and Packaging Technology, vol. 31, no. 3, pp. 702-11 (2008).
24. M. Gurfinkel, J.C. Horst, J.S. Suehle, J.B. Bernstein, Y. Shapira, K.S. Matocha, G. Dunne, R.A. Beaupre, *"Time-Dependent Dielectric Breakdown of 4H-SiC/SiO_2 MOS Capacitors,"* IEEE Trans. on Device and Mat. Rel., vol. 8, no. 4, pp. 635-641 (2008).
25. D. Heh, C.D. Young, G.A. Brown, P.Y. Hung, A. Diebold, E. Vogel, J.B. Bernstein, and G. Bersuker, *"Spatial Distributions of Trapping Centers in $Hf0_2/SiO_2$ Gate Stack,"* IEEE Transactions on Electron Devices, vol. 54, no.6, pp. 1338-45 (2007).
26. Joseph B. Bernstein, Moshe Gurfinkel, Xiaojun Li, Jörg Walters, Yoram Shapira and Michael Talmor, *"Electronic circuit reliability modeling,"* Microelectronics Reliability, vol. 46, pp. 1957-1979 (2006).
27. Heh D, Young CD, Brown GA, Hung PY, Diebold A, Bersuker G, Vogel EM, Bernstein JB, *"Spatial distributions of trapping centers in HfO2/SiO2 gate stacks,"* Applied Physics Letters, vol. 88, no.15, pp. 152907 (2006).
28. X. Li, J. Qin, B. Huang, X. Zhang, and J.B. Bernstein, *"SRAM Circuit Failure Modeling and Reliability Simulation with SPICE,"* IEEE Trans. on Device and Mat. Rel., vol. 6, no. 2, pp.235-246 (2006).
29. X. Li, J. Qin, B. Huang, X. Zhang, and J.B. Bernstein, *"A New SPICE Reliability Simulation Method for Deep Submicron VLSI Circuits,"* IEEE Trans. on Device and Mat. Rel., vol. 6, no. 2, pp. 247-257 (2006).
30. J.S. Suehle, B. Zhu, Y. Chen and J.B. Bernstein, *"Detailed study and projection of hard breakdown evolution in ultra-thin gate oxides,"* Microelectronics Reliability, vol. 45, pp. 419-426 (2005).
31. J. Lee, W. Zhang, J.B Bernstein, *"Analysis of Energy Process Window of Laser Metal Pad Cut Link Structure,"* IEEE Transactions on Semiconductor Manufacturing, vol. 16, no. 2, pp. 299-307 (2003).
32. L. Yang, C.K. King, J.B. Bernstein, *"Liquid Dispensing Encapsulation in Semiconductor Packaging,"* Microelectronics International, vol. 20, no. 3, pp. 29-35 (2003).
33. D.W. Heh, E.M. Vogel, J.B. Bernstein, *"Impact of Substrate Hot Hole Injection on Ultra-thin Silicon-dioxide Breakdown,"* Applied Physics Letters, vol. 82, no. 19, pp. 3242-3244 (2003).
34. J.S. Suehle, E.M. Vogel, P. Roitman, J.F. Conley Jr., A.H. Johnston, B. Wang, J.B. Bernstein, and C.E. Weintraub, *"Observation of Latent Reliability Degradation in Ultra-Thin Oxides after Heavy-Ion Irradiation,"* Applied Physics letters, vol. 80, no. 7, pp. 1282-4 (18 Feb 2002).
35. E.M., Vogel, D. Heh, J.B. Bernstein, *"Interaction between low-energy electrons and defects created by hot holes in ultrathin Silicon Dioxide,"* Applied Physics letters, vol. 80, no. 18, pp. 3343-5 (6 May 2002).
36. L.-S. Yang and J.B. Bernstein, *"Encapsulation Process Development for Flexible-Circuit Based Chip Scale Packages,"* IEEE Trans. Electronics Packaging Manufacturing, vol. 25, no. 4, pp. 344-354 (October 2002).

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

37. L.-S. Yang, J.B. Bernstein and K.C. Leong, *"Effect of the Plasma Cleaning Process on Plastic Ball Grid Array Package Assembly Reliability,"* IEEE Trans. Electronics Packaging Manufacturing, vol. 25, no. 2, pp. 91-99 (April 2002).
38. E.M., Vogel, D. Heh, J.B. Bernstein, J.S. Suehle, *"Impact of the Trapping of Anode Holes in Silicon Dioxide Breakdown,"* IEEE Electron Device Letters, vol. 23, no. 11, pp. 667-669 (November 2002).
39. Yang, L., Bernstein, J.B., Chung, K, *"The Impact of Lead-free Soldering on Electronics packages,"* Microelectronics International, vol. 18, no. 3, pp. 20-26 (2001).
40. Wang, B., Suehle J.S. ,Vogel E.M., Bernstein, J.B., *"Time-Dependent Breakdown of Ultra-thin SiO_2 Gate Dielectrics under Pulsed Biased Stress,"* IEEE Electron Device Letters, vol. 22, no. 5, pp. 224-226 (2001).
41. Zhang, W., J.-H. Lee, Bernstein, J.B, *"Energy Effect of the Laser Induced Vertical Metallic Link,"* IEEE Transactions on Semiconductor Manufacturing, vol. 14, no. 2, pp. 163-169 (2001).
42. J.F. Conley Jr., J.S. Suehle, A.H. Johnston, B.Wang, T. Miyahara, E.M. Vogel, J.B. Bernstein, *"Heavy-Ion Induced soft breakdown of thin gate oxides,"* IEEE Transactions on Nuclear Science, vol. 48, no. 6, pp. 1913-16 (Dec. 2001).
43. Shen, C.C., Hefner, A.R., Jr., Berning, D.W., Bernstein, J.B., *"Failure Dynamics of the IGBT During Turn-off For Unclamped Inductive Loading Conditions,"* IEEE Transactions on Industry Applications, Vol. 36, no.2, pp.614-24 (2000).
44. Bernstein, J.B., Lee, J., Yang, G., Dahmas, T., *"Analysis of Laser Metal-Cut Energy Process Window,"* IEEE Transactions on Semiconductor Manufacturing, vol.13, no. 2, pp. 228-34 (2000).
45. Vogel, E., Suehle, J.S., Edelstein, M.D., Wang, B., Chen, Y., Bernstein, J.B., *"Reliability of Ultra-thin Silicon Dioxide Under Combined Substrate Hot Electron and Constant Voltage Tunneling Stress,"* IEEE Transactions on Electron Devices, vol. 47, no.6, pp.1183-91 (2000).
46. Lee, J., Zhang, W., Bernstein, J.B., *"Scalability Study of Laser-induced Vertical Make-link Structure,"* IEEE Transactions on Semiconductor Manufacturing, vol. 13, no. 4, pp. 442-447 (2000).
47. Zhang, W., Lee, J.H., Chen, Y., Bernstein, J.B., Suehle, J.S., *"Reliability of laser-induced metallic vertical links,"* IEEE Transactions on Advanced Packaging, vol. 22, no.4, pp. 614-19 (1999).
48. Bernstein, J.B., Hua, Y., Zhang, W., *"Laser energy limitation for buried metal cuts,"* IEEE Electron Device Letters, vol. 19, no. 1, pp. 4-6 (1998).
49. Bernstein, J.B., Zhang, W., Nicholas, C.H., *"Laser formed metallic connections,"* IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, vol. 21, no. 2, pp. 194-8 (1998).
50. Chen, Y., Suehle, J.S., Shen, C.C., Bernstein, J.B., Messick, C., Chaparala, P., *"A new technique for determining long-term TDDB acceleration parameters of thin gate oxides,"* IEEE Electron Device Letters, vol. 19, no. 7, pp. 218-21 (1998).
51. Shen, Y-L, Suresh, S., Bernstein, J.B., *"Laser linking of metal interconnect: analysis and design considerations,"* IEEE Transactions on Electron Devices, vol. 43, no. 3, pp. 402-10 (1996).
52. Rasera, R.L., Bernstein, J.B., *"Laser linking of metal interconnect: linking dynamics and failure analysis,"* IEEE Transactions on Components, Packaging, and Manufacturing Technology, vol. 19, no. 4, pp. 554-61 (1996).

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

53. Bernstein, J.B., Ventura, T.M., Radomski, A.T., *"Laser induced microfracture leading to high density metal-to-metal connections,"* Proceedings of the SPIE, The International Society for Optical Engineering, vol. 2335, pp. 165-76 (1995).
54. Bernstein, J.B., Colella, B.D., *"Laser-formed metallic connections employing a lateral link structure,"* IEEE Transaction on Components, Packaging, and Manufacturing Technology, Part A, vol. 18, no. 3, pp.690-2 (1995).
55. Bernstein, J.B., Ventura, T.M., Radomski, A.T., *"Laser induced microfracture leading to high density metal-to-metal connections,"* Proceedings of the SPIE, The International Society for Optical Engineering, vol. 2335, pp. 165-76 (1995).
56. Bernstein, J.B., Colella, B.D., *"Laser-formed metallic connections employing a lateral link structure,"* IEEE Transaction on Components, Packaging, and Manufacturing Technology, Part A, vol. 18, no. 3, pp.690-2 (1995).
57. Bernstein, J.B., Ventura, T.M., Radomski, A.I., *"High-density laser linking of metal interconnect,"* IEEE Transactions on Components, Packaging and Manufacturing Technology, Part A, vol. 17, no.4, pp. 590-3 (1994).
58. Murguia, J.E., Bernstein, J.B., *"Short-time failure of metal interconnect caused by current pulses,"* IEEE Electron Device Letters, vol. 14, no. 10, pp. 481-3 (1993).
59. Bernstein, J.B., *"Improvements to the Electrically Stimulated Acoustic Wave method for analyzing bulk space charge,"* IEEE Transactions on Electrical Insulation, vol. 27, no.1, pp. 152-61 (1992).
60. Bernstein, J.B., Cohen, S.S., Wyatt, P.W., *"Metal wire cutting by repeated application of low-power laser pulses,"* Review of Scientific Instruments, vol. 63, no. 6, pp. 3516-18 (1992).
61. Cohen, S.S., Bernstein, J.B., Wyatt, P.W., *"The effect of multiple laser pluses on damage to thin metallic films,"* Journal of Applied Physics, vol. 71, no. 2, pp. 630-7 (1992).
62. Cohen, S.S., Bernstein, J.B., Wyatt, P.W., *"Laser-induced line melting and cutting,"* IEEE Transactions on Electron Devices, vol. 39, no. 11, pp. 2480-5 (1992).
63. Bernstein, J.B., *"Analysis of the electrically stimulated acoustic-wave method for observing space charge in semi-insulating films,"* Physical Review B (Condensed Matter), vol.44, no.19, pp. 10804-14 (1991).
64. Bernstein, J.B., Cooke, C.M., *"Bulk space charge behavior in polymethylethacrylate under an imposed virtual cathode condition,"* IEEE Transactions on Electrical Insulation, vol. 26, no. 6, pp. 1080-6 (1991).
65. Bernstein, J.B., Cooke, C.M., *"Electric poling behavior of polymethylmethacrylate,"* IEEE Transactions on Electrical Insulation, vol. 26, no. 6, pp. 1087-93 (1991).
66. Cohen, S.S., Wyatt, P.W., Bernstein, J.B., *"Laser-induced melting of thin conducting films. II. Heat-dissipating substrates,"* IEEE Transactions on Electron Devices, vol.38, no.9 pp. 2051-7 (1991).
67. Cohen, S.S., Wyatt, P.W., Burns, J.A., Bernstein, J.B., *"The mechanism of laser-induced vertical links,"* Journal of the Electrochemical Society, vol.138, no.10, pp. 3013-18 (1991).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Refereed Conference Proceedings

1. E Bender, JB Bernstein, DS Boning, *"The Effects of Process Variations and BTI in Packaged FinFET Devices,"* IEEE International Reliability Physics Symposium (IRPS), 1-5 Monterey, CA (2023)
2. JB Bernstein, E Bender, A Bensoussan, *"The Correct Hot Carrier Degradation Model,"* 2023 IEEE International Reliability Physics Symposium (IRPS), 1-5 Monterey, CA (2023)
3. E. Bender and J. B. Bernstein, "Self-heating Effects Measured in Fully Packaged FinFET Devices," 32ND INTERNATIONAL CONFERENCE ON MICROELECTRONICS, Serbia (2021)
4. I Aharn, Y Shalom, Y Dromi, A Shemaryahu, JB Bernstein, "*GaN based Ring Oscillator PWM Generator*," IEEE 12th Energy Conversion Congress & Exposition-Asia (ECCE-Asia 2021)
5. E Bender, JB Bernstein, A Bensoussan, *"Reliability prediction of FinFET FPGAs by MTOL," Microelectronics Reliability, ESREF (2020)*
6. I Aharon, M Sitbon, J Bernstein, "*Design Considerations for GaN Based Converters,*" 8th International Conference on Renewable Energy Research and Applications (ICRERA 2019)
7. G Golan, M Azoulay, J Bernstein, *"On the Ballistic Transport in Si Nano-Devices," IEEE 31st International Conference on Microelectronics (MIEL), 55-58 (Sept. 2019)*
8. M Musil, A Bensoussan, J Bernstein, F Coccetti, "Synopsis of Multiphysics Deep Sub-Micron Failure Rate Modeling Technique for CFR and EOL Prediction," 2018 IEEE 13th Nanotechnology Materials and Devices Conference (NMDC) (Nov 2018)
9. G Golan, M Azoulay, S Shaheen, JB Bernstein, "A Novel Reliability Model For GaN Power FET," 2018 IEEE International Conference on the Science of Electrical Engineering {Dec 2018)
10. J.B Bernstein, "Aerospace electronics reliability: Could it be predicted in a cost-effective fashion?," IEEE Aerospace Conference, Colorado (Feb 2015)
11. J.B. Bernstein, O. Delly, M. Gabbay, "Combination of Multiple Mechanism for Post-Silicon Reliability Prediction," ChipEx 2014, Tel Aviv (April 2014)
12. J.B. Bernstein, "Multiple Accelerated Test Matrix for Reliability Prediction," SemIsrael Expo, Airport City, Israel (Nov 2013)
13. J.B. Bernstein and Y. Bot, "Physics Based Reliability Qualification," IEEE-IRIC, (March 2013)
14. J.B. Bernstein, "Physics of Failure Based Reliability Qualification," Proceedings of 19th International Conference of the Israel Society for Quality, pres. 7.1.4 Tel Aviv (October 2012).
15. Hava, F. Barmoav, C. Moulton, B. Kowalski, E. Ribak and J.B. Bernstein, "Prediction of Earpiece field failure rate based on accelerated Life test," 2012 IEEE 27-th Convention, Eilat (2012).
16. J. Qin, M. White, J.B. Bernstein, "A Study of Scaling Effect on DRAM Reliability," Annual Reliability and Maintainability Symposium (RAMS), Final Report, pp. 9C-4 (January 2011).
17. J. Qin, A. Hava, J.B. Bernstein, "FaRBS: a New PoF Based VLSI Reliability Prediction Method," Annual Reliability and Maintainability Symposium (RAMS), pp. 9D-3 (January 2011).
18. M. Gurfinkel, P. Livshits, A. Rozen, Y. Fefer, J.B. Bernstein, Y. Shapira, "Supply signal

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

fluctuations due to chip power grid resonance — a new reliability concern," Proc. of the IEEE International Reliability Physics Symposium, (April-May 2008).

19. J. Qin, B. Yan, Y. Shoshany, R. Druker, H. Rahamim, H. Marom, J.B. Bernstein, "Study of Transistor and Product NBTI Lifetime Distributions (A)," International Integrated Reliability Workshop (IIRW) Final Report, pp. 1-16 (October 2008).
20. J. Qin, B. Yan, Y. Shoshany, R. Druker, H. Rahamim, H. Marom, J.B. Bernstein, "Study of Transistor and Product NBTI Lifetime Distributions (B)," International Integrated Reliability Workshop (IIRW) Final Report, pp. 64-67 (October 2008).
21. B. Yan, J. Qin, J. Dai, Q. Fan, J.B. Bernstein, "Reliability Simulation and Design Consideration of High Speed ADC Circuits." International Integrated Reliability Workshop (IIRW) Final Report, pp. 125-128 (October 2008).
22. L. Condra, J. Qin and J.B. Bernstein, **"**State of the Art Semiconductor Devices in Future Aerospace Systems," Proceedings of the FAA/NASA/DoD Joint Council on Aging Aircraft Conference, Palm Springs, CA (April 2007).
23. M. Gurfinkel, J. Suehle, J.B. Bernstein, Yoram Shapira, A.J. Lelis, D. Habersat, N. Goldsman, "Ultra-fast Characterization of Transient Gate Oxide Trapping in SiC MOSFETs," Proc. of the IEEE International Reliability Physics Symposium 2007.
24. J. Qin, X. Li, J.B. Bernstein, "SRAM Stability Analysis Considering Gate Oxide SBD, NBTI and HCI," 2007 International Integrated Reliability Workshop (IIRW) Final Report, 2.2, (October 2007).
25. M. Gurfinkel, et. al., "Characterization of Interface and Bulk Oxide Traps in SiC MOSFETs with Epitaxialy grown and implanted channels," 2007 International Integrated Reliability Workshop (IIRW) Final Report, 8.3 (October 2007).
26. L. Yang, J.B. Bernstein, D. Gajewski and J. Walls, "Predictive Reliability Assessment and Failure Rate Modeling for Electronic Packages," IMAPS 40th International Symposium on Microelectronics, Final Report, WA5 (November 2007).
27. M. Gurfinkel, J. Suehle, J.B. Bernstein, Y. Shapira, A.J. Lelis, D. Habersat, N. Goldsman, "Ultra-Fast Measurement of Vth Instability in SiC MOSFETs due to Positive and Negative Constant Bias Stress," 2006 International Integrated Reliability Workshop (IIRW) Final Report, pp. 49-53 (October 2006).
28. M. White, C. Vu, C. Nguyen, R. Ruiz, Y. Chen, J.B. Bernstein, "Product Reliability Trends, Derating Considerations and Failure Mechanisms with Scaled CMOS," 2006 International Integrated Reliability Workshop (IIRW) Final Report, pp. 156-159 (October 2006).
29. J. Qin, J.B. Bernstein, "Non-Arrhenius Temperature Acceleration and Stress-Dependent Voltage Acceleration for Semiconductor Devices Involving Multiple Failure Mechanisms," 2006 International Integrated Reliability Workshop (IIRW) Final Report, pp. 93-97 (October 2006).
30. Bernstein, J. B., "Reliability Qualification at the Maryland-Israel Center for Product Realization," Proceedings of 16th International Conference of the Israel Society for Quality, pp.

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

9.2.01 Tel Aviv (November 2006).

31. M. Gurfinkel, J. Suehle, J.B. Bernstein, Y. Shapira, "Enhanced Gate Induced Leakage Current in HfO2 MOSFETs due to Remote Interface Trap-Assisted Tunneling," 2006 International Electron Devices Meeting (IEDM) technical digest, pp. 755-758, (Dec 2006).
32. Xiaojun Li; Walter, J.D.; Bernstein, J.B.; "Simulating and Improving Microelectronic Device Reliability by Scaling Voltage and Temperature," Quality of Electronic Design, 2005. ISQED 2005. Sixth International Symposium, pp.496 - 502 (March 2005).
33. Xiaojun Li; Huang, B.; Qin, J.; Zhang, X.; Talmor, M.; Gur, Z.; Bernstein, J.B.; "Deep Submicron CMOS Integrated Circuit Reliability Simulation with SPICE," Quality of Electronic Design, 2005. ISQED 2005. Sixth International Symposium on, pp. 382 - 389 (March 2005).
34. Zhu, B.; Suehle, I.S.; Vogel, E.; Bernstein, J.B.; "The contribution of HFO_2 bulk oxide traps to dynamic NBTI in pMOSFETs," IEEE International Reliability Physics Symposium 2005 Proceedings, pp. 533 – 537 (April 2005).
35. Kuan-Jung Chung; Bernstein, J.B.; Ji Luo; Tuchman, J.A.; Ma, Z.K.; "Experimental Study for Low Resistance Interline Connections Using Pulsed Laser Techniques," Quantum Electronics and Laser Science 2005, Conference Volume 3, pp.1564 - 1566 (May 2005).
36. Bing Huang; Xiaojun Li; Ming Li; Bernstein, J.; Smidts, "Study of the impact of hardware fault on software reliability," Proceedings. 16th IEEE International Symposium on Software Reliability Engineering. Chicago, IL, USA (Nov. 2005).
37. B. Zhu, J.S. Suehle, J.B. Bernstein, "Mechanism for reduced NBTI effect under pulsed bias stress conditions," Proceedings of Integrated Reliability Workshop, Phoenix (Arizona 2004).
38. J.S. Suehle, B. Zhu, Y. Chen, J.B. Bernstein, "Acceleration factors and mechanistic study of progressive breakdown in small area ultra-thin gate oxides," Proceedings of Integrated Reliability Workshop, Phoenix (Arizona 2004).
39. Ji Luo; Bernstein, J.B.; Tuchman, J.A.; Hu Huang; "A high performance radiation-hard field programmable analog array." Proceedings. 5th International Symposium on Quality Electronic Design. p. 522-7. (Los Alamitos, CA, 2004).
40. Hu Huang, Joseph B. Bernstein, Martin Peckerar, Ji Luo; "Combined Channel Segmentation and Buffer Insertion for Routability and Performance Improvement of Field Programmable Analog Arrays," Proceedings of the IEEE International Conference on Computer Design (October 2004).
41. X. Zhang, N. Goldsman, J.B. Bernstein, J.M. McGarrity, "Numerical and Experimental Characterization of 4H-SiC Schottky Diodes," Proceedings of IEEE International Semiconductor Device Research Symposium, p. 120-1 (2003).
42. M. White, M. Cooper, Y. Chen, J. Bernstein, "Impact of Junction Temperature on Microelectronic Device Reliability and Considerations for Space Applications," Proceedings of Integrated Reliability Workshop, p. 133-6 (Nevada 2003).
43. B. Zhu, J.B. Bernstein, J. Suehle, "Negative bias temperature instability of deep sub-micron p-MOSFETs under pulsed bias stress," Proceedings of Integrated Reliability Workshop, pp. 125-9 (Nevada 2003).

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

44. Y. Chen, D. Nguyen, S. Guertin, J.B. Bernstein, M. White, R. Menke, S. Kayali, "A Reliability Evaluation Methodology for Memory Chips for Space Applications when Sample Size is Small," Proceedings of Integrated Reliability Workshop, Lake Tahoe (Nevada 2003).

45. Ji Luo, Kuan-Jung Chung, Hu Huang, J.B. Bernstein, "Temperature Dependence of R(on,sp) in Silicon Carbide and GaAs Schottky diodes," Proceedings of IEEE International Reliability Physics Symposium, 40th annual (New Jersey 2002).

46. Zhuo Gao, Ji Luo, Hu Huang, Wei Zhang, J.B. Bernstein, "Reliable laser programmable gate array technology," Proceedings International Symposium on Quality Electronic Design, p. 252-6, Los Alamitos (California 2002).

47. D. Heh, J.B. Bernstein, E.M. Vogel, "Defect generation in ultra-thin oxide over large fluence ranges," Proceedings of Integrated Reliability Workshop, Lake Tahoe (Nevada 2002).

48. Z. Gao, J. Luo, Hu Huang, W. Zhang, J.B. Bernstein, "Reliable laser programmable gate array technology," Proceedings of International Symposium on Quality Electronic Design, pp. 252-256 (Californinia 2002).

49. J.S. Suehle, et.al … J.B. Bernstein, "Challenges of high-k gate dielectrics for future MOS devices," 6th International Symposium on Plasma and Process Induced Damage, pp. 90-93 (California 2001).

50. B. Wang, J.B. Bernstein, "Latent Reliability Degradation of Ultra-Thin Oxides after Heavy Ion and Gamma Irradiation," Proceedings of Integrated Reliability Workshop (California 2001).

51. Bernstein, J.B. and Lee, J, "A Laser Formed MakeLink for Customization and Repair," Proceedings of IEEE International Symposium on Semiconductor Manufacturing, pp. 347-350 (California 2001).

52. Ji Luo, K. Chung, Hu Huang, J.B. Bernstein, "Comparison of Silicon Carbide Schottky diodes," Proceedings of 2001 GaAs Reliability Workshop (Virginia 2001).

53. Suehle, J.S., Vogel, E., Wang, B., Bernstein, J.B., "Temperature Dependence of Soft Breakdown and Wear-Out in Sub-3 nm SiO_2 Films," International Reliability Physics Symposium - Conference Proceedings, pp. 33-9 (California 2000).

54. E. M. Vogel, M. D. Edelstein, C. A. Richter, N. V. Nguyen, I. Levin, D. L. Kaiser, H. Wu, and J. Bernstein, **"**Issues in High-κ Gate Dielectrics for Future MOS Devices," Proceedings of IEEE Microelectronics Reliability Qualification Workshop (California 2000).

55. B. Wang, J. Suehle, E.M. Vogel, J.B. Bernstein, "The Effect of Stress Interruption and pulsed bias stress on Ultra-Thin Gate Dielectric Reliability," Proceedings of Integrated Reliability Workshop (California 2000).

56. J. Lee, G. Zhuo and J.B. Bernstein, "Laser Programmable Multichip Module using Vertical Make-link," Proceedings of the IEEE Electronic Components and Technology Conference, pp 932-936 (Nevada 2000).

57. Vogel, E., Suehle, J.S., Edelstein, M.D., Wang, B., Chen, Y., Bernstein, J.B., "Degradation of Ultra-thin SiO_2 Under Combined Substrate Hot Electron and Tunneling Stress," Semiconductor Interface Specialists Conference, (California 2000).

58. Shen, C.C., Kefner, A.R., Jr., Berning, D.W., Bernstein, J.B., "Failure dynamics of the IGBT during turn-off for unclamped inductive loading conditions," Conference Record of 1998 IEEE Industry Applications Conference, p. 3, vol. xxx+2410, 831-9, vol. 2 (New York 1999).

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

59. Zhang, W., Bernstein, J.B., "Electromigration simulation under DC/AC stresses considering microstructure," Proceedings of the IEEE 1999 International Interconnect Technology Conference, pp. 295, 41-3 (California 1999).

60. Chen, Y., Suehle, J.S., Shen, C.C., Bernstein, J.B., Messick, C., Chaparala, P., "The correlation of highly accelerated Q_{bd} tests to TDDB life tests for ultra-thin gate oxides," 1998 IEEE International Reliability Physics Symposium Proceedings. 36thAnnual, pp. 87-91 (California 1998).

61. Bernstein, J.B., Zhang, W., Nicholas, C.H., "Laser formed connections for programmable wiring," Proceedings of the IEEE 1998 Custom Integrated Circuits Conference, pp. 608, 163-5 (California 1998).

62. Bernstein, J.B., Zhang, W., Nicholas, C.H., "Laser programmable metallic vias," Proceedings of the IEEE 1998 International Interconnect Technology Conference, pp. 304, 205-7 (New York 1998).

63. Chen, Y, Suehle, J.S., Shen, C.C., Bernstein, J.B., Messick, C., Chaparala, P., "The correlation of highly accelerated Q_{bd} tests to TDDB life tests for ultra-thin gate oxides," 1998 IEEE International Reliability Physics Symposium Proceedings. 36th Annual, pp. vii+421, 87-91 (Nevada 1998).

64. Chen, Y., Suehle, J.S., Shen, C.C., Bernstein, J.B., Messick, C., "A New Technique to Extract TDDB Acceleration Parameters from Fast Qbd Tests," Proceedings of International Integrated Reliability Workshop, pp. 67-69, (Nevada 1997).

65. Bernstein, J.B., "Laser Formed Lateral Metallic Connections," Proceedings of the Second International Conference on Beam Processing of Advanced Materials, pp. 101-104 (Ohio 1995).

66. Bernstein, J.B., "Dielectric fracture leading to metallic connections employing a lateral link structure," Thin Films: Stresses and Mechanical Properties V. Symposium, MRS pp. 833-7 (Massachusetts 1994).

67. Bernstein, J.B., Ventura, T.M., Radomski, A.T., "Laser induced microfracture leading to high density metal-to-metal connections," Proceedings of the SPIE, The International Society for Optical Engineering, pp. 165-76 (Texas 1994).

68. Bernstein, J.B., Gleason, E.F., Wetsel, A.E., Liu, E.Z., Wyatt, P.W., "Anomalous Behavior of Semi-insulating Silicon Rich Amorphous Silicon Nitride," Amorphous Insulating Thin Films Symposium, MRS pp. 113-18 (Massachusetts 1993).

69. Bernstein, J.B., Gleason, E.F., Wyatt, P.W., "A thermally stable silicon rich amorphous silicon nitride alloy for electronic device applications," Amorphous Silicon Technology Symposium, MRS pp. 667-72 (California 1992).

70. Bernstein, J.B., Gleason, E.F., Wyatt, P.W., "High density metal cross-point laser linking," International Conference on Wafer Scale Integration Proceedings, pp. 176-81 (California 1992).

71. Bernstein, J.B., Cohen, S.S., Wyatt, P.W., "Fatigue of aluminum films leading to melting by multiple laser pulses," Phase Formation and Modification by Beam-Solid Interactions Symposium,MRS pp. 589-93 (Boston 1991).

72. Cooke, C.M., Wright, K.A., Takasu, N., Bernstein, J.B., Gollin, E., "Calibration of Volume Charge Measurements By Use of Electron Beam Implantation," 1989 Annual Report. Conference on Electrical Insulation and Dielectric Phenomena, pp. 508, 435-41 (Virginia 1989).

73. Bernstein, J.B., Bahl, S., Schlecht, M.F., "A Low Capacitance Power MOSFET with an Integral Gate Driver," Proceeding of the 18th Annual IEEE Power Electronics Specialists Conference, PESC vol. 87, pp. 704, 61-8 (Virginia 1987).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Magazine Articles

1. J.B. Bernstein, "Engineering through Torah," Et Lachshov, Vol. 96, pp. 16-19 (Aug-Sep. 2008).
2. J.B. Bernstein, "The Power of Three" (Hebrew), Et Lachshov, Vol. 89, pp. 32-37 (Jul-Aug 2007).
3. J.B. Bernstein, "Scientific Exploration," Et Lachshov, Vol. 87, pp. 12-15 (May-June 2007).
4. J.B. Bernstein, "Reliable Truth" (In Hebrew), Et Lachshov, Vol. 86, pp. 16-18 (Mar-Apr 2007).
5. J.B. Bernstein, "Good and Bad" (In Hebrew), Et Lachshov, Vol. 82, pp. 16-18 (Dec. 2006).
6. J.B. Bernstein, "Limitations" (In Hebrew), Et Lachshov, Vol. 80, pp. 22-24 (Sep.-Oct. 2006).
7. J.B. Bernstein, "Computers and the Jewish Soul" (In Hebrew), Et Lachshov, Vol. 79, pp. 22-24 (Jul.-Aug. 2006).
8. J.B. Bernstein, "Chess and Free Choice," Et Lachshov, Vol. 76, pp. 14-17 (May 2006).
9. J.B. Bernstein, "Truth through the Scientific Method" (In Hebrew), Et Lachshov, Vol. 74, pp. 25-27 (Feb. 2006).
10. J.B. Bernstein, "Education and Technology," Et Lachshov, Vol. 67, pp. 22-25 (June 2005).
11. J.B. Bernstein, "The Wonders of Silicon," Et Lachshov, Vol. 66, pp. 28-30 (May 2005).
12. J.B. Bernstein, "The Moon" (In Hebrew), Et Lachshov, Vol. 64, pp. 30-32 (March 2005).
13. J.B. Bernstein, "Halacha and Engineering Design" Et Lachshov, Vol. 63, pp. 36-37 (Feb. 2005).
14. J.B. Bernstein, "Statistical Logic" (In Hebrew), Et Lachshov, Vol. 62, pp. 20-22 (Jan. 2005).
15. J.B. Bernstein, "That we should not know from failures…" (In Hebrew), Et Lachshov (time to think), Vol. 61, pp. 32-33 (Oct. – Dec. 2004).
16. J.Lee, J. Ehrmann, D. Smart, J. Griffiths, and J.B. Bernstein, "Analyzing the process window for laser copper-link processing," Solid State Technology, (December 2002).
17. Pecht, M., Bernstein, J.B., Searls, D., Peckerar, M., Karulkar, P., "Korea's Focus on Market Dominance," Semiconductor International, pp. 118-22 (1998).
18. Kump, H.J., Bernstein, J.B., "The Deal fast-surface states are probably deep-level impurities in the semiconductor," IEEE Circuits and Devices Magazine, vol. 1, no. 6, pp. 17-22 (1985).