

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DELTA ELECTRONICS, INC.
Petitioner,

v.

VICOR CORPORATION,
Patent Owner.

Case IPR2024-00187

U.S. PATENT NO. 9,166,481

**DECLARATION OF DOUGLAS CHARLES HOPKINS, PH.D. IN
SUPPORT OF PETITION FOR *INTER PARTES* REVIEW**

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DECLARATION OF DOUGLAS CHARLES HOPKINS, PH.D

1. I, Douglass Charles Hopkins, make this declaration in connection with the proceedings identified above.

2. I have been retained on behalf of Petitioner Delta Electronics, Inc. (“Delta”) to offer my expert opinions in connection with the above-captioned proceeding relating to U.S. Patent 9,166,481 (the “’481 Patent”).

3. I am being compensated for my time in connection with this *inter partes* review (IPR) at my standard consulting rate. No part of my compensation depends on the outcome of this proceeding.

4. I have been asked to provide my opinions as to whether claims 1, 22, and 31-35 (the “Challenged Claims”) of the ’481 Patent are invalid to a person having ordinary skill in the art at the time of the alleged invention.

5. In preparing this declaration, I have reviewed the ’481 Patent (Ex. 1001),¹ the file history of the ’481 Patent (Ex. 1002), various pieces of prior art (Exs. 1005-1015 and 1017-1020), and all other materials referenced in this declaration.

¹ All citations to exhibit numbers in this declaration are to the exhibits attached to the accompanying IPR Petition for the ’481 Patent.

6. In forming the opinions expressed in this declaration, I relied upon my education, training, knowledge, and experience in the art, and have considered the viewpoint of an ordinary artisan at the time of the invention.

I. BACKGROUND AND QUALIFICATIONS

7. I summarize in this section my educational background, career history, and other relevant qualifications. My full resume is attached as Exhibit 1004 to the accompanying IPR Petition.

8. I earned a Bachelor of Science in Electrical Engineering and a Master of Science in Electrical Engineering from the State University of New York at Buffalo in 1975 and 1977, respectively. I earned a Ph.D. in Electrical Engineering from Virginia Polytechnic Institute and State University (Virginia Tech) in 1989, with a focus on Power Electronics and Energy Systems.

9. I am currently a Professor in the Department of Electrical and Computer Engineering at North Carolina State University—a position I’ve held since August 2011 to the present. I have also served as Director of the Laboratory for Packaging Research in Electronic Energy Systems at North Carolina State University since September 2011 to the present.

10. Prior to my position at North Carolina State University, I was a Professor in the Electrical Engineering Department of the State University of New York at Buffalo, from 1997 to 2011. I was also Director of the Electronic Power

and Energy Research Laboratory at the the State University of New York at Buffalo during that same timeframe. In 2008, during my time at the State University of New York at Buffalo, I founded a company called DensePower, LLC (involved in developing power control modules for power supplies), and I served as its President from 2008 until 2014.

11. From 1994-1998, I was an Assistant Professor in the Department of Electrical Engineering at the State University of New York at Binghamton, and my teaching and research were in the area of electronic energy systems and electronic packaging. Prior to that, from 1993-1994, I was a Research Assistant Professor at the State University of New York Research Foundation in Binghamton, New York, with research in the area of electronic energy systems.

12. From 1988 to 1992, I was an Assistant Professor in the Department of Electrical Engineering at Auburn University. In that role, my teaching and research were in the area of power electronics and power packaging.

13. From 1983 to 1988, while I was a Doctoral Student at Virginia Tech, I was also an Instructor in the Department of Electrical Engineering at Virginia Tech.

14. Prior to my time in academia, and before I began pursuit of my Ph.D. in 1983, I worked as an Electrical Engineer in the Corporate Research and Development Center at General Electric Company from 1977-1982. I also worked

as a Senior Engineer in the Research and Development Center at Carrier Corporation from 1982-1983.

15. I have been a Senior Member of the Institute of Electrical and Electronics Engineers (“IEEE”) since 1992, and have participated in a number of the IEEE Societies, including the Components, Packaging and Manufacturing Technology Society, the Electron Devices Society, the Industry Applications Society, the Industrial Electronics Society, the Power Electronics Society, the Power & Energy Society, and the Vehicular Technology Society. I am also a Fellow of the International Microelectronics and Packaging Society.

II. LEGAL STANDARDS

16. I am not a lawyer or legal expert, and I do not offer any opinions regarding applicable legal standards. Below, I set forth my understanding of the law as it has been explained to me, and I have applied this understanding in forming my opinions in this declaration.

A. Priority Date and Prior Art

17. I am informed that for these proceedings, the prior art to the challenged patent includes patents and printed publications in the relevant art that predate the priority date of the patent.

18. The '481 Patent issued on October 20, 2015 from U.S. Patent Application No. 13/830,262 filed on March 14, 2013. Ex. 1001, Cover. The '481 Patent is not a continuation or divisional of any earlier applications.

19. I understand that the '481 Patent claims priority on its face to March 14, 2013. I have also been told that Patent Owner has contended in a related ITC proceeding that the '481 Patent was conceived in April 2010. My opinions in this declaration with respect to Ground I of the related Petition are applicable if the March 14, 2013 priority date applies to the '481 Patent, and my opinions with respect to Grounds II-VII of the related Petition are applicable regardless of which priority date applies to the '481 Patent. I offer no opinions in this declaration as to which priority date is correct, but reserve the right to do so should the Patent Owner allege a priority date earlier than March 14, 2013 in this IPR proceeding.

B. Claim Interpretation

20. I understand that in construing or interpreting a patent claim, the words of the claim are generally given their ordinary and customary meaning, which is the meaning that words would have had to a person of ordinary skill in the art in question at the time of the invention. The person of ordinary skill in the art is deemed to read the claim term in the context of not only the particular claim in which the disputed term appears, but also in the context of the entire patent, including the other claims and the specification, as well as the prosecution history of the patent. For purposes

of this proceeding, I understand the claim terms of the '481 Patent to have their ordinary and customary meaning.

C. Anticipation

21. To invalidate a patent claim as anticipated in the context of IPR, the petitioner bears the burden of showing by a preponderance of the evidence that a single prior art reference discloses every element required by the claim.

22. An element need not be expressly disclosed if it is inherent in the prior art, but the allegedly inherent characteristic must necessarily flow from the teachings of the applied prior art—in other words, the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic.

D. Obviousness

23. To invalidate a patent claim as obvious in the context of an IPR proceeding, the petitioner bears the burden of showing by a preponderance of the evidence that the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art to which the subject matter pertains at the time the claimed invention was made. Factors relevant to the determination of obviousness include (1) the scope and content of the prior art, (2) the level of ordinary skill in the art at the time of the invention, (3) differences between the claimed invention and the prior art, and

(4) “secondary considerations” or objective evidence of obviousness or nonobviousness.

24. I am informed that some non-exclusive rationales that may support a conclusion of obviousness include:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of known technique to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- "Obvious to try" – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art;

- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

25. **Reason to Combine.** Obviousness can be established by showing that a person of ordinary skill in the art would have combined or modified the teachings of the prior art to produce the claimed invention and would have had a reasonable expectation of success in achieving the claimed subject matter. There is no requirement that the prior art provide an express teaching, suggestion, or motivation to combine elements of the prior art, but a determination of obviousness requires more than showing that each element of a patent claim was independently known in the prior art. Rather, the petitioner in an IPR must identify some apparent reason why a person of ordinary skill in the art would have combined the elements or concepts from the prior art in the same way as in the claimed invention when considered as a whole. The motivation to combine may be implicit and may be found in the knowledge of a person of ordinary skill in the art, from the nature of the problem to be solved, market demand, or common sense.

26. **Hindsight.** A determination regarding obviousness must be based on the knowledge possessed by a person of ordinary skill in the art at the time when the invention was made, and one should not consider in hindsight what is known today or what is learned from the teachings of the patent. Thus, it is inappropriate to use

hindsight reconstruction of references to reach the claimed invention without any explanations as to how or why the references would be combined to produce the claimed invention.

27. **Analogous Art.** An obviousness analysis cannot be based on nonanalogous art. The rationale behind this rule is that when art is directed to a different purpose than a claimed invention, an inventor would have less motivation or occasion to consider it. Art is analogous when it is from the same field of endeavor as the claimed invention, or if the art is not from the same field of endeavor, when it is reasonably pertinent to the particular problem faced by the inventor. To be “reasonably pertinent,” art must “logically commend itself” to an inventor’s attention in considering his problem.

III. PERSON OF ORDINARY SKILL IN THE ART

28. I have been advised that there are multiple factors relevant to determining a person having a level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.

29. I have been informed that Patent Owner has contended in a related ITC proceeding that a person of ordinary skill in the art (“POSITA”) with respect to the ’481 Patent would have at least a Master’s degree in electrical engineering and two

or more years of work experience relating to power electronics and the design and control of switching power converters, with more experience potentially substituting for education, or vice-versa. I have adopted this understanding of the level of ordinary skill in the art for purposes of this Declaration.

30. I have been qualified as at least a person of ordinary skill in the art since well before 2010, and each of my opinions set forth in this declaration are presented from the standpoint of one skilled in the art. Thus, where I specify in the analysis below that I am rendering my opinion, it should be understood that my opinion is from the perspective of a person having the level of ordinary skill in the art that I have described at the time of the invention.

IV. OVERVIEW OF THE '481 PATENT

31. The '481 Patent is directed to a method for digital control of a resonant power converter. Ex. 1001, Abstract. The patent relates to a method for “digital control of resonant zero-current and zero-voltage switching resonant power converters.” *Id.* 1:6-9.

32. The patent describes one implementation of the invention as “a method of synchronously operating a power converter in a series of converter operating cycles includes providing an oscillator for generating clock signals at an oscillator frequency and generating timing control signals for each of a plurality of events based upon the clock signals in a standard converter operating cycle having a

standard operating period and frequency. The timing and control signals may turn a primary switch ON and OFF at times when essentially zero voltage is impressed across and essentially zero resonant current is flowing in the primary switch and turn a secondary switch ON and OFF at times when essentially zero current is flowing in and essentially zero voltage is impressed across the secondary switch. The oscillator frequency may be preset and the timing of the timing control signals for one or more selected events may be set independently of other timing control signals and events.” *Id.* 2:26-41. This description corresponds to claim 1 of the ’481 Patent, which is the patent’s only independent claim. *Id.*, Claim 1.

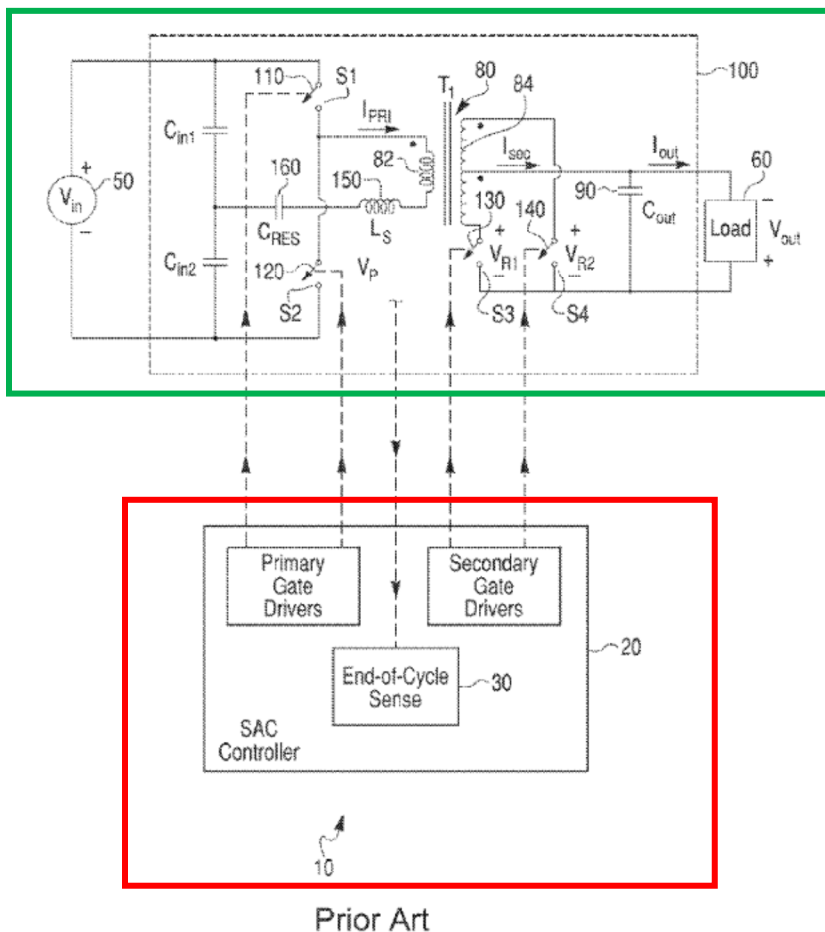
33. Specifically, claim 1 of the ’481 Patent claims, “a method of synchronously operating a power converter in a series of converter operating cycles, the converter having at least one primary switch to drive a resonant power train and at least one secondary switch, the resonant power train including a transformer and having a characteristic resonant frequency and period, the method comprising: providing an oscillator for generating clock signals at an oscillator frequency; generating timing control signals for each of a plurality of events based upon the clock signals in a (A) standard converter operating cycle, having a standard operating period and frequency, to: (i) turn the at least one primary switch ON and OFF at times when essentially zero voltage is impressed across the respective at least one primary switch and essentially zero resonant current is flowing in the respective

at least one primary switch; and (ii) turn the at least one secondary switch ON and OFF at times when essentially zero current is flowing in the respective at least one secondary switch and essentially zero voltage is impressed across the respective at least one secondary switch; and wherein the oscillator frequency is preset, and the timing of the timing control signals for one or more selected events may be set independently of other timing control signals and events.” *Id.*, Claim 1. The features described in claim 1 were well known to those skilled in the art at the time of the priority date of the ’481 Patent.

34. The dependent claims of the ’481 Patent add nothing inventive, in my opinion, including the use of a gate drive circuit to operate the converter switches (claim 22), generating the timing control signals by counting the clock signals from the oscillator and setting a count threshold for each event (claim 31), having the oscillator and timing events be open-loop with respect to the power train (claim 32), having the oscillator or timing events adjusted with feedback from measurements in the power train (claim 33), having the feedback measurements and adjustments performed during the manufacturing process (claim 34), and having the feedback measurements and adjustments performed during operation as part of a closed-loop feedback system (claim 35). Each of these features were also well known to those skilled in the art at the time of the priority date of the ’481 Patent.

35. In reading the specification, the '481 Patent expressly admits that resonant power converters with zero-current and zero voltage switching were known in the art at the time of filing. The converter and controller configuration in Figure 1 of the '481 Patent (copied below) is labeled as “Prior Art” and is described as a “block diagram of a half-bridge sine amplitude converter 10” that “comprises SAC power conversion circuitry 100 . . . and a SAC controller 20 which controls the turning ON and OFF of the switches within the power conversion circuitry 100.” Ex. 1001, 1:20-25; Fig. 1.

Fig. 1



Prior Art

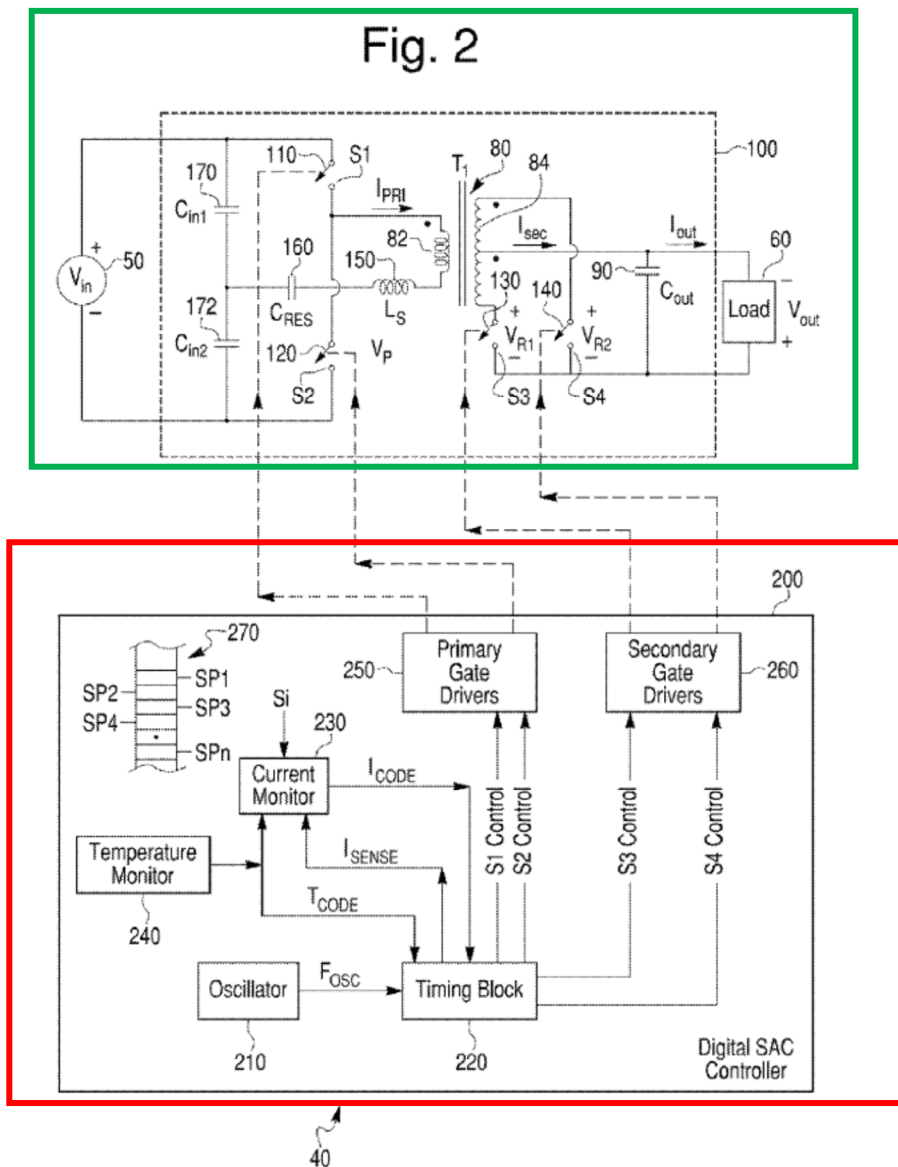
Ex. 1001, Fig. 1 (“Prior Art”).²

36. The green box in Figure 1 represents the prior art “SAC power conversion circuitry 100”, and the red box represents the prior art “SAC controller 20 which controls the turning ON and OFF of the switches within the power conversion circuitry 100”. *Id.* 1:20-25. The ’481 Patent further admits that the prior

² All colors and colored annotations to figures in this declaration have been added.

art was capable of performing zero-voltage switching (“ZVS”) and zero-current switching (“ZCS”). *Id.* 1:13-2:7.

37. The purported “invention” of the ’481 Patent replaced the conventional SAC controller 20 of Figure 1 with a digital SAC controller 200 of Figure 2, shown below.



Ex. 1001, Fig. 2.

38. The '481 Patent states that “the SAC power conversion circuitry 100 shown in Fig. 2 is essentially the same as shown in Fig. 1.” *Id.* 4:29-35. A comparison of the SAC power conversion circuitry 100 (the green boxes) in both Figure 1 (admitted prior art) and Figure 2 ('481 Patent) confirms that they are identical. The '481 Patent goes on to describe the operation of digital SAC controller 200. But as I discuss in detail in Section VI below, use of a digital controller to control zero-voltage and zero-current switching in a resonant power converter was well known at the time of the '481 Patent's priority date. The prior art references discussed in Section VI render the Challenged Claims of the '481 Patent unpatentable.

39. I have reviewed the '481 Patent in its entirety, and neither the specification nor claims describe anything innovative in the art at the priority date of the '481 Patent.

V. OVERVIEW OF THE PRIOR ART

A. McDonald (Ex. 1005)

40. McDonald is a paper from the 2012 Texas Instruments Power Supply Design Seminar entitled “Design and Optimization of a High Performance LLC Converter.” Ex. 1005, Cover.

41. McDonald describes the design of a resonant LLC converter that uses a digital controller to control the primary and secondary switches of the converter,

including at zero voltage and zero current switching conditions. Ex. 1005, Abstract, 5-3, Fig. 1. McDonald notes that Figure 1 (depicted below) “illustrates the basic schematic for a half-bridge LLC power stage as well as the critical operating variables in the system.” Ex. 1005, 5-3.

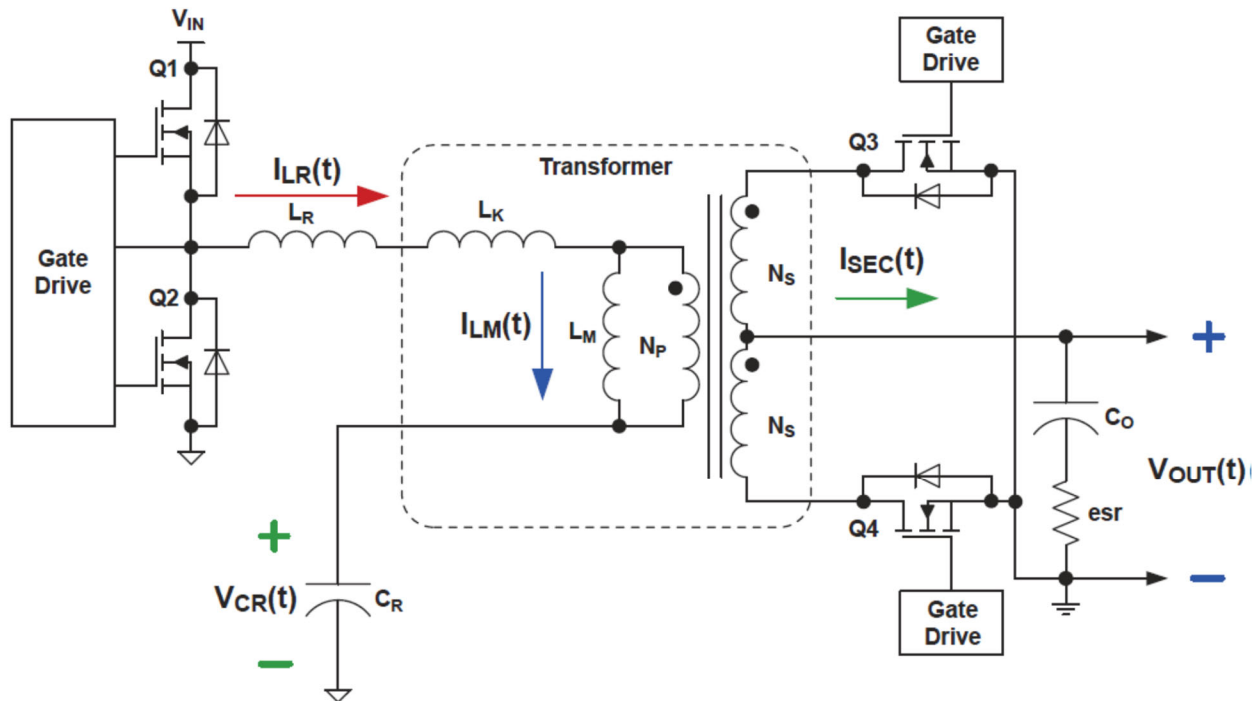


Figure 1 – Basic LLC schematic.

Ex. 1005, Figure 1.

42. The resonant LLC converter shown in Figure 1 of McDonald contains: two primary side MOSFET switches (Q1 and Q2); two secondary side MOSFET switches (Q3 and Q4); a resonant tank on the primary side depicted by two inductors (L_R and L_M) and a capacitor (C_R); a transformer; and gate drive circuitry (Gate Drive) for controlling the converter. *Id.*

43. McDonald acknowledges that the converter depicted therein uses “a Texas Instruments UCD3138 digital controller” to facilitate “easy optimization and evaluation of the various control features” discussed. Ex. 1005, 5-22. The TI UCD3138 digital controller is discussed in greater detail below as another prior art reference. This digital controller contains an oscillator for generating clock signals for the controller, and also generates the various timing signals to control the switching of the switches in the resonant power converter.

B. TI UCD3138 (Ex. 1006)

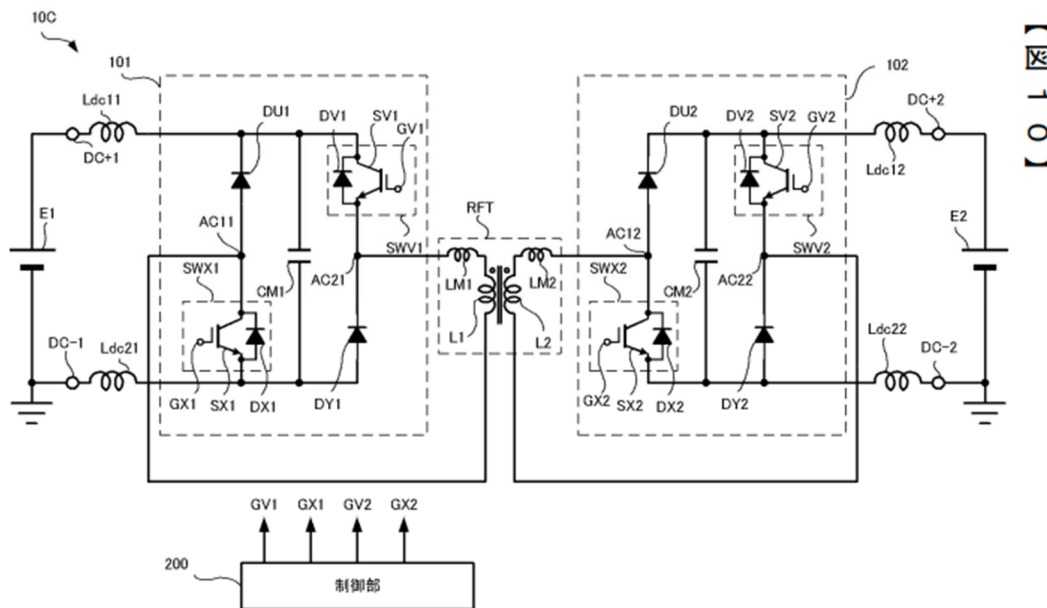
44. TI UCD3138 is a data manual from Texas Instruments for the UCD3138 Highly Integrated Digital Controller for Isolated Power. Ex. 1006, Cover. The manual discusses that the UCD3138 is a digital power supply controller that is “suitable for a wide variety of power conversion applications. Ex. 1006, 7.

45. The manual also discusses that specific power management peripherals have been added to the controller to allow for a variety of operating features, including “LLC and phase shifted full bridge mode switching,” which refers to zero voltage and zero current switching. *Id.* The manual further discusses that the device’s “topology support has been optimized” for a variety of configurations, including “LLC half bridge and full bridge.” Ex. 1006, 7.

C. Shimada (Ex. 1007 (original), Ex. 1008 (certified translation))

46. Shimada is a Japanese patent entitled “Current-Fed Series Resonance DC/DC Converter and Power Conversion Control Method.” Ex. 1008, Cover. Shimada discloses a series resonant converter that “can supply bi-directional DC power and soft switching with simple control regardless of the output voltage of the power supply.” *Id.*, Abstract.

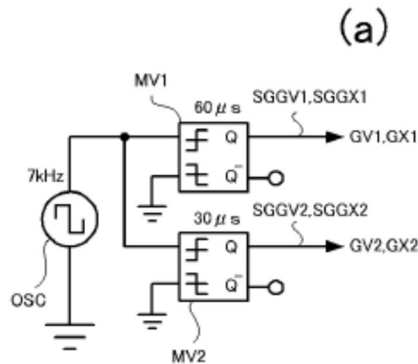
47. Figure 10 of Shimada (copied below) shows a converter with: two primary side switches (SWV1 and SWX1); two secondary side switches (SWV2 and SWX2); a resonant tank circuit on the primary side; a transformer (RFT); and a digital control unit (200) for controlling the converter.



Ex. 1007, Fig. 10.

48. The digital control unit (200) of Shimada is shown in Figure 23(a) (copied below) and includes an oscillator (OSC) for generating clock signals at a preset oscillatory frequency of 7kHz.

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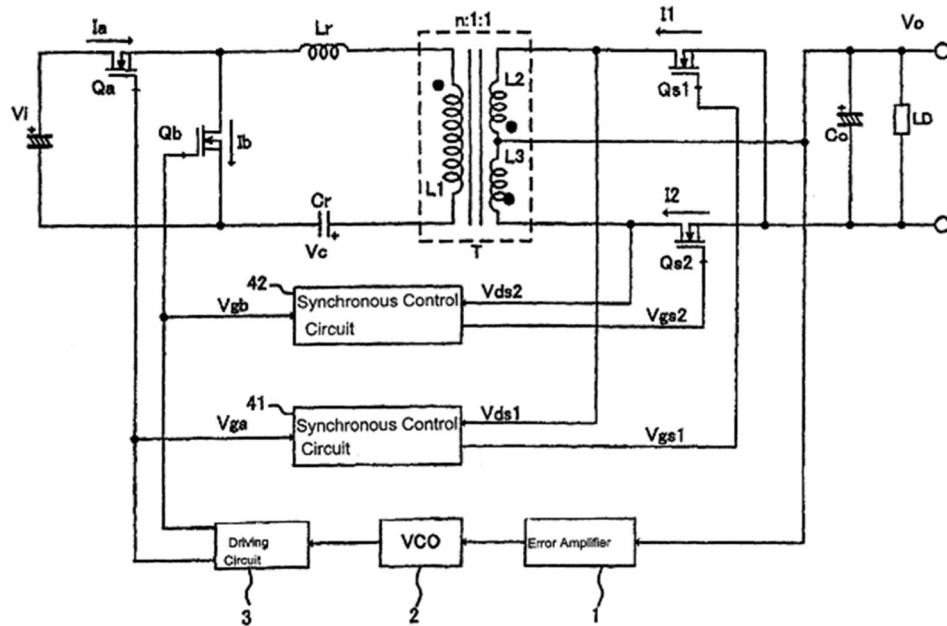
Id., Fig. 23(a); Ex. 1008, ¶ [0137].

D. Chen (Ex. 1010)

49. Chen is a U.S. patent entitled “Switching Power Supply Device and Switching Power Supply Control Circuit.” Ex. 1010, Cover. Chen discloses a series resonant switching power supply device that utilizes a synchronous control circuit for controlling the primary and secondary switches of the power supply device. *Id.*, Abstract, 7:23-34.

50. Figure 1 of Chen (copied below) shows a power supply converter with: two primary side MOSFET switches (Qa and Qb); two secondary side MOSFET switches (Qs1 and Qs2); a resonant circuit on the primary side (Lr, Cr); a transformer (T); and control circuitry for controlling the converter. The control circuitry includes

an oscillator (VCO), a gate drive circuit (Driving Circuit), and control signals (V_{ga} , V_{gb} , V_{gs1} , and V_{gs2}) for controlling the switches in the converter.



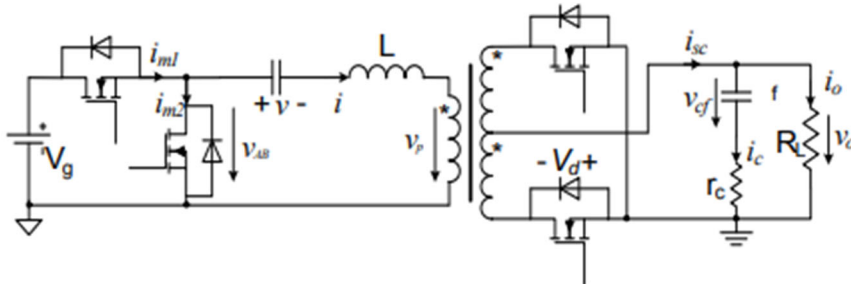
Ex. 1010, Fig. 1.

E. Pan (Ex. 1011)

51. Pan is a conference paper from the 2008 IEEE Power Electronics Specialists Conference entitled “Secondary-side Adaptive Digital Controlled Series Resonant DC-DC Converters for Low Voltage High Current Applications.” Ex. 1011, Cover.

52. Pan discloses a series resonant converter that utilizes a digital controller for controlling the primary and secondary switches of the converter. Ex. 1011, § II, Fig. 1, Fig. 11. Figure 1 of Pan (copied below) shows a series resonant converter with: two primary side MOSFET switches (M1 and M2); two secondary side

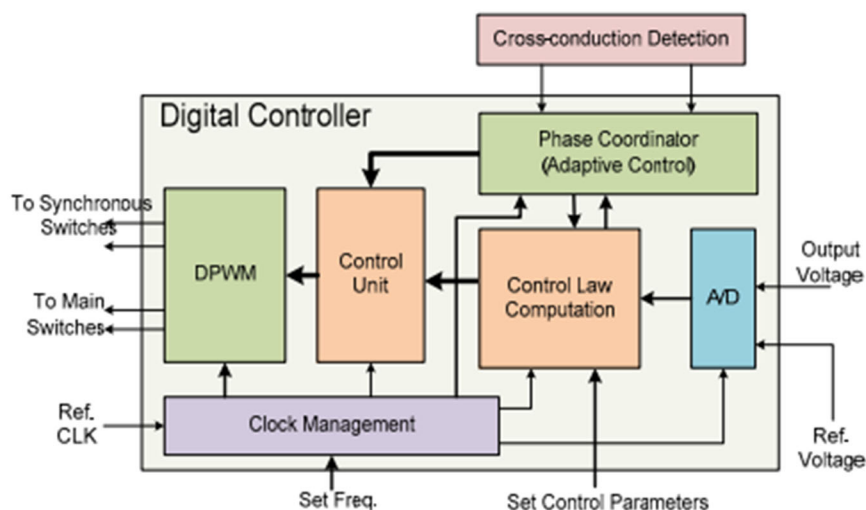
MOSFET switches (S1 and S2); a resonant circuit on the primary side; and a transformer.



Ex. 1011, Fig. 1, 712.

53. The description of the converter in Pan states that “[t]he main stage on the primary side of the transformer could be either half bridge or full bridge with L-C series resonant tank” and further that “[t]he main switches (M1 & M2) operate in complementary mode against input voltage variations. The rectifier switches (S1 & S2) operate in PWM control mode against load variations.” *Id.* 712.

54. Figure 11 of Pan shows the architecture of the digital controller used to control the series resonant converter in Pan.



Ex. 1011, Fig. 11. The digital controller includes a control unit, a digital pulse width modulator (DPWM), and clock management.

F. Peng (Ex. 1012)

55. Peng is a U.S. patent entitled “Isolated and Soft-Switched Power Converter.” Ex. 1012, Cover. Peng discloses a soft-switched power converter with resonant tank circuits on either side of an isolation transformer. *Id.*, Abstract.

56. Figure 6 of Peng (copied below) shows a power converter with: primary side MOSFET switches (S1 and S2), secondary side switches (S3 and S4), a transformer (104), and resonant tank circuits on the primary side and secondary sides of the transformer.

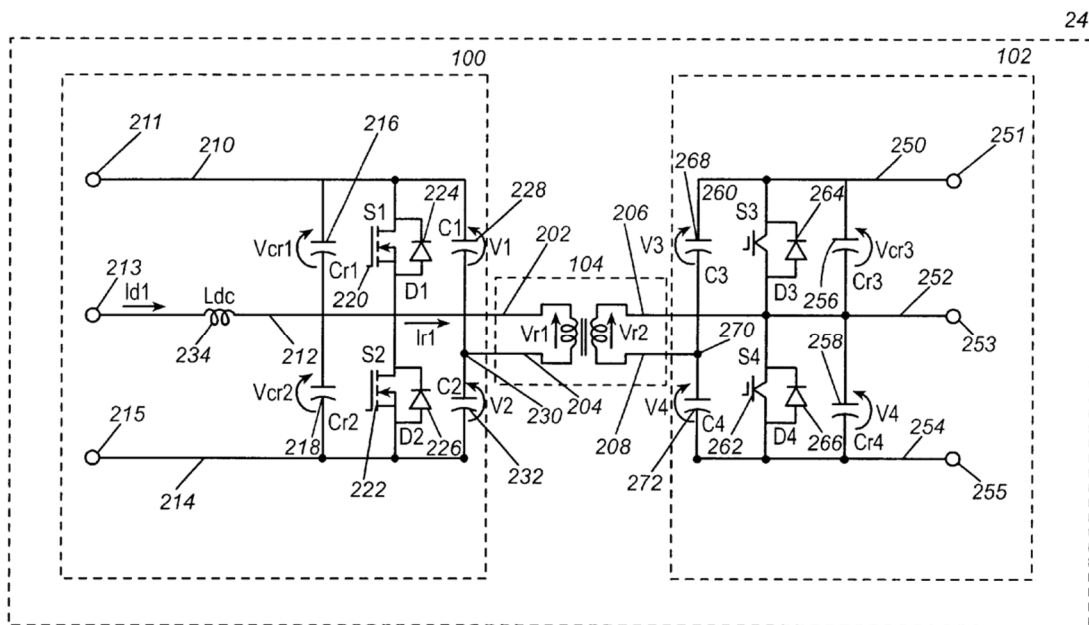


FIG. 6

Ex. 1012, Fig. 6.

57. Figure 5 of Peng (copied below) is a block diagram of the power converter, which shows the switching controller (160) for controlling the primary and secondary switches. Peng explicitly states that “[m]any suitable computing stations and circuits may serve as the switching controller 160, including personal computers, workstations, minicomputers, application-specific digital/analog integrated circuits, and so forth.” *Id.*, 14:54-58.

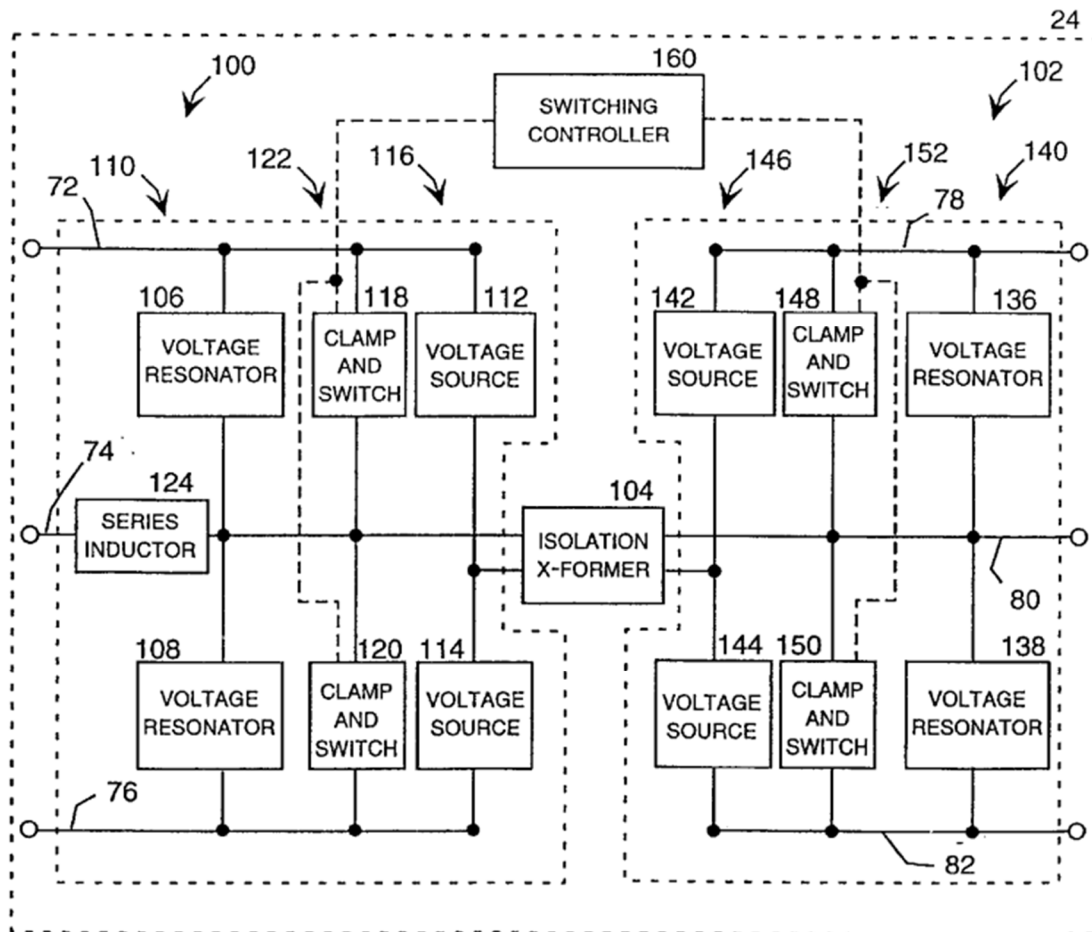


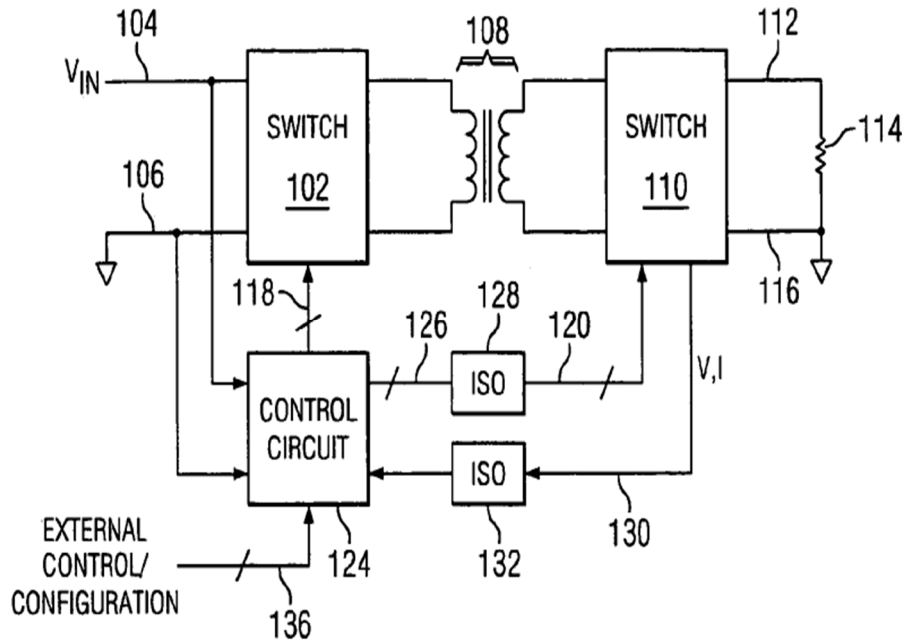
FIG. 5

Ex. 1012, Fig. 5.

G. Leung (Ex. 1013)

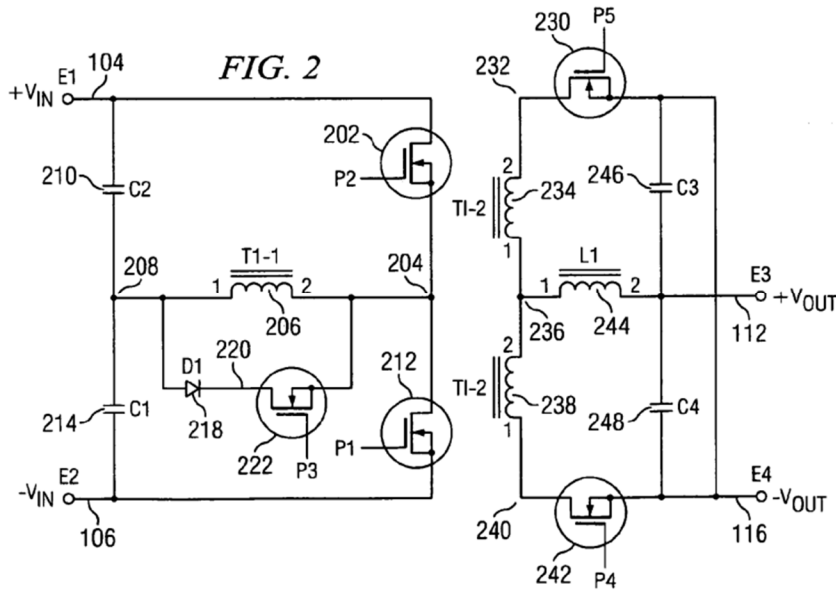
58. Leung is a U.S. patent application entitled “Digital PWM Controller.”

Ex. 1013, Cover. Figure 1 of Leung (below) shows a power converter with: a primary switch group (102), a secondary switch group (110); a transformer (108); and a digital control circuit (124).



Ex. 1013, Fig. 1

59. Figure 2 of Leung (below) shows a more detailed schematic diagram of the primary switch group (102), the secondary switch group (110), and the isolation transformer (108).



Ex. 1013, Fig. 2

60. Figure 4 of Leung (below) shows a block diagram of the digital controller 124 in Figure 1.

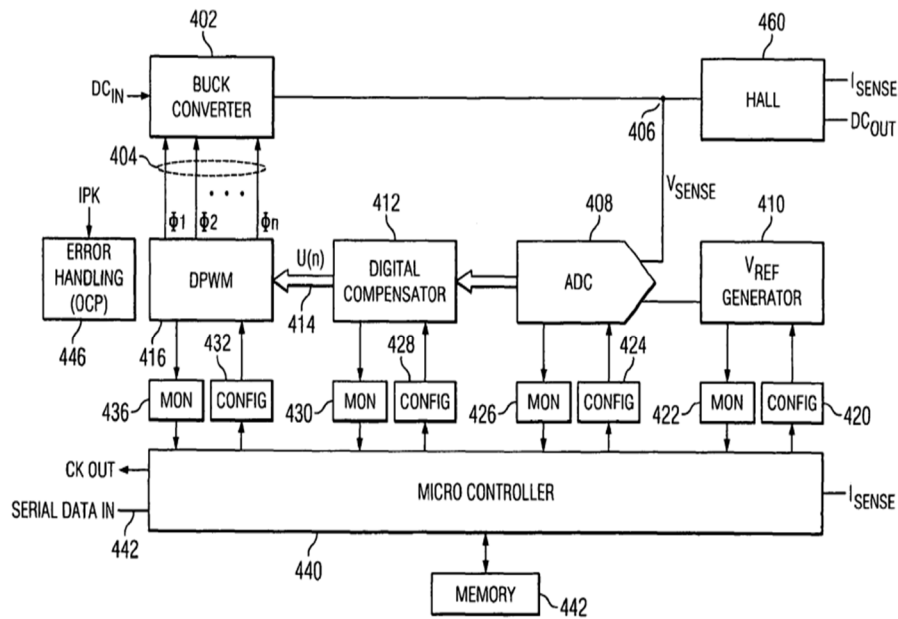


FIG. 4

Ex. 1013, Fig. 4.

H. TI UCD3040 (Ex. 1018)

61. TI UCD3040 is a datasheet from Texas Instruments for the UCD3040, UCD3028, and UCD3020 Digital Power Controllers. Ex. 1018, 1. The datasheet states that UCD3040 is suitable for “isolated AC/DC and DC/DC power supplies.” *Id.* The datasheet also states that it supports a wide range of topologies, including “half-bridge, phase-shifted full bridge, active clamp, and resonant LLC.” *Id.* at 2. This indicates that it can be used to control zero voltage and zero current switching.

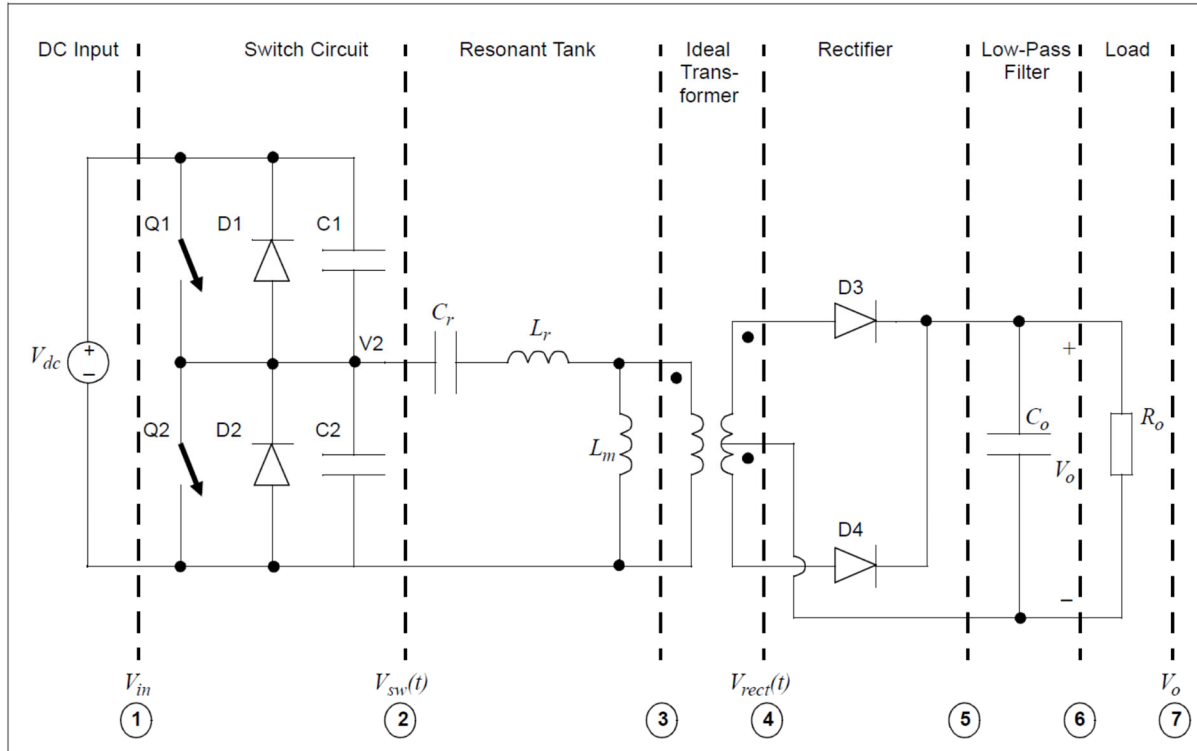
I. AN1336 (Ex. 1019)

62. AN1336 is Microchip datasheet for the AN1336 DC/DC LLC Reference Design Using the dsPIC DSC. Ex. 1019, 1. The datasheet discusses LLC resonant converters and control thereof using Microchip’s dsPIC digital signal controllers. *Id.*

63. AN1336 states that its converter “permits the implementation of control and supervision/management tasks with a small pin count dsPIC DSC from Microchip. Sophisticated control is possible, using the DSP capabilities of dsPIC DSC devices.” *Id.*

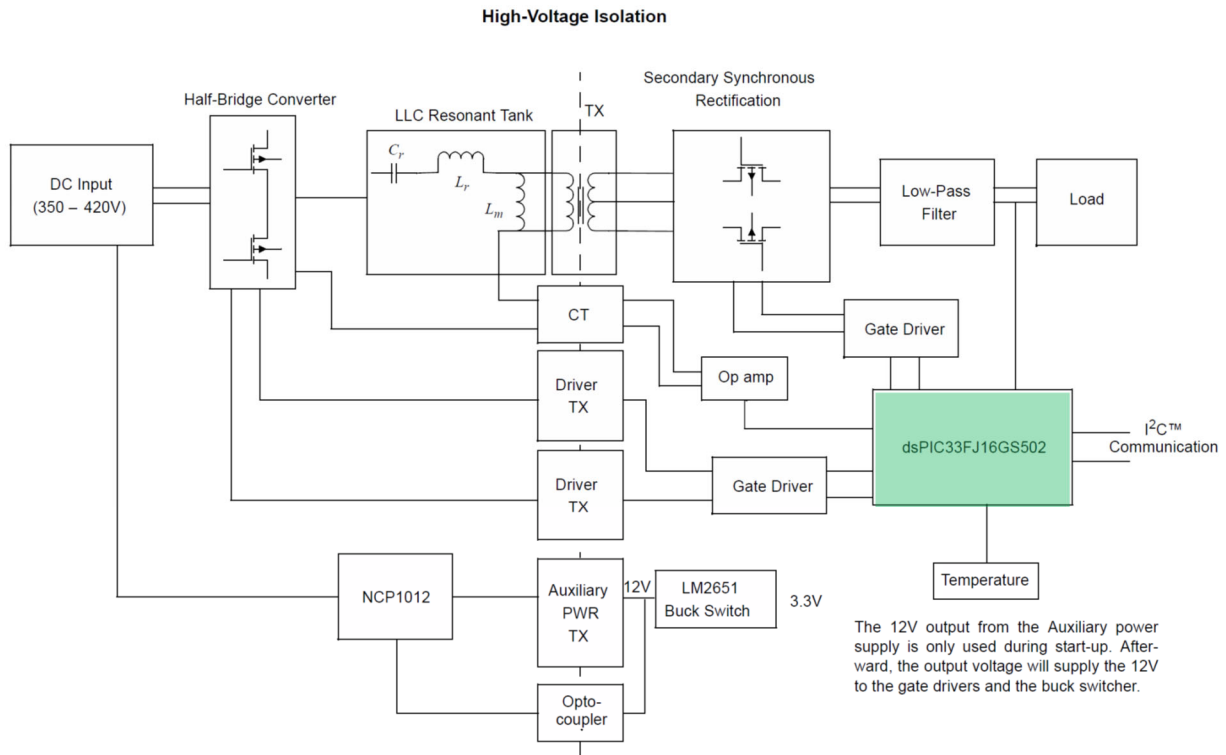
64. Figure 10 of AN1336 (copied below) shows a schematic diagram of the resonant converter, including primary switches (Q1 and Q1), the LLC resonant tank on the primary side (consisting of inductor L_r , inductor L_m , and capacitor C_r), the secondary switches (D3 and D4), and the transformer.

FIGURE 10: LLC CIRCUIT COMPONENTS AND SECTIONS



Ex. 1019, Figure 10.

65. Figure 46 of AN1336 (copied below) shows a schematic diagram of the Microchip dsPIC controller (in green) that controls the resonant converter.



Ex. 1019, 36 (Fig. 46).

J. dsPIC33FJ06GS101 (Ex. 1020)

66. dsPIC33FJ06GS101 is a datasheet from Microchip for the dsPIC33FJ06GS101 Digital Signal Controller. Ex. 1020. The datasheet states that it provides high-speed PWM “with independent timing” and an internal oscillator.

Id., 1.

K. AAPA (Exs. 1001, 1009)

67. The '481 Patent discloses several instances of Applicant Admitted Prior Art ("AAPA") related to zero voltage switching and zero current switching. For example, the '481 Patent states that the prior art (as depicted in Figure 1) discloses that "switches S1 110 and S3 130 are closed when the voltages across switches S1

110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero, initiating a power transfer interval.” Ex. 1001, 1:28-32.

68. The '481 Patent also states that the prior art discloses that “when the sinusoidal current flow completes half-cycle, and the current I_{pri} returns substantially to zero, switches S1 110 and S3 130 are opened.” *Id.*, 1:36-39. And further that “an energy recycling interval following the opening of switches S1 110 and S3 130, allows the transformer 80 magnetizing current to charge and discharge circuit parasitic capacitances such that the voltages across switches S2 120 and S4 140 decline toward zero.” *Id.*, 1:39-43.

69. The '481 Patent also states that in the prior art, “the voltage across one or more of the switches may be monitored to establish the timing of a zero-voltage switching or zero-current switching event.” *Id.* 1:66-2:3.

70. The '481 Patent also explicitly references and incorporates by reference U.S. Patent No. 6,984,965 (“the '965 Patent”) (Ex. 1009), which is another Vicor patent with the same named inventor as the '481 Patent. *Id.* 1:14-20. The '965 Patent states that “the VTM may include secondary switches turned on and off essentially at times of zero voltage to rectify power from the transformer. The VTM may include secondary switches on and off essentially at times of zero current to rectify power from the transformer.” Ex. 1009, 9:25-29.

VI. THE CHALLENGED CLAIMS ARE UNPATENTABLE

71. It is my opinion that a person of ordinary skill in the art would have considered the Challenged Claims of the '481 Patent unpatentable, over either: (A) McDonald and TI UCD3138; (B) Shimada and AAPA; (C) Chen and AAPA; (D) Pan, TI UCD3138 (or, alternatively, TI UCD3040), and AAPA; (E) Peng, TI UCD3138 (or, alternatively, TI UCD3040), and AAPA; (F) Leung and AAPA; and (G) AN1336, dsPIC33FJ06GS101, and AAPA. I explain my opinions in detail below, on a claim-by-claim basis.

A. The Challenged Claims are Obvious over McDonald in view of TI UCD3138.

72. It is my opinion that McDonald (Ex. 1005) combined with TI UCD3138 (Ex. 1006) renders obvious claims 1, 22, and 31-35 of the '481 Patent.

73. A POSITA would have been motivated to combine McDonald with TI UCD3138 because McDonald states that the converter depicted therein uses “a Texas Instruments UCD3138 digital controller” to facilitate “easy optimization and evaluation of the various control features.” Ex. 1005, 5-22. A POSITA would therefore have understood and expected that TI UCD3138 and the teachings discussed therein could be used as the digital controller for the converter disclosed in McDonald, such that modifying the converter disclosed in McDonald to utilize the TI UCD3138 digital controller would have been obvious to a POSITA.

1. Claim 1

- a. “A method of synchronously operating a power converter in a series of converter operating cycles the converter having at least one primary switch to drive a resonant power train and at least one secondary switch, the resonant power train including a transformer and having a characteristic resonant frequency and period, the method comprising:”**

74. McDonald discloses this limitation. McDonald discloses a method of synchronously operating a half-bridge power converter, where the converter has at least one primary switch that drives a resonant circuit, at least one secondary switch, and a transformer. Ex. 1005, 5-3 (“Figure 1 illustrates the basic schematic for a half-bridge LLC power stage as well as the critical operating variables in the system.”).

75. Figure 1 of McDonald (copied below) discloses a half-bridge converter having primary switches Q1 and Q2 (in blue), a resonant circuit (LLC) on the primary side consisting of inductor L_R , inductor L_M , and capacitor C_R , secondary switches Q3 and Q4 (in pink), and a transformer (in yellow).

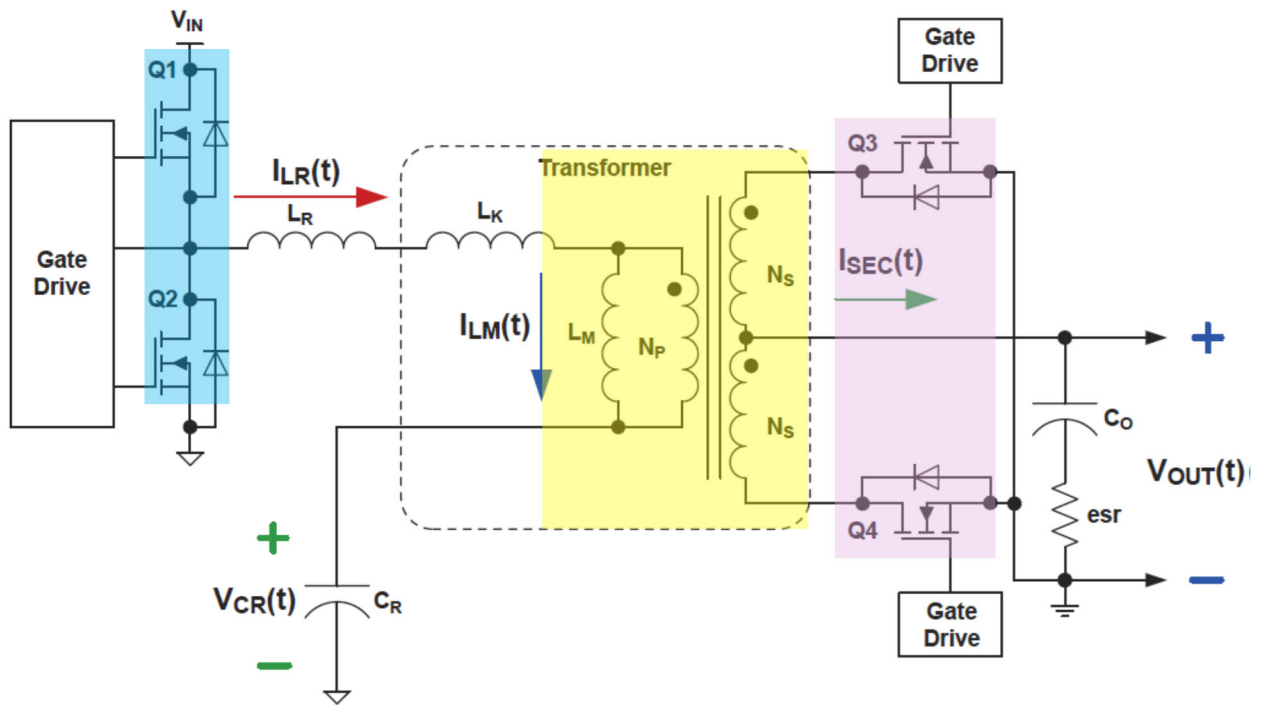


Figure 1 – Basic LLC schematic.

Ex. 1005, Fig. 1. The resonant circuit, by its nature, has a resonant frequency and period.

b. “providing an oscillator for generating clock signals at an oscillator frequency;”

76. McDonald in combination with TI-UCD3138 (“McDonald-TI UCD3138”) renders this limitation obvious. Figure 1 of McDonald (copied below) discloses that the switches Q1, Q2, Q3, and Q4 are controlled by a Gate Drive controller (shown in red).

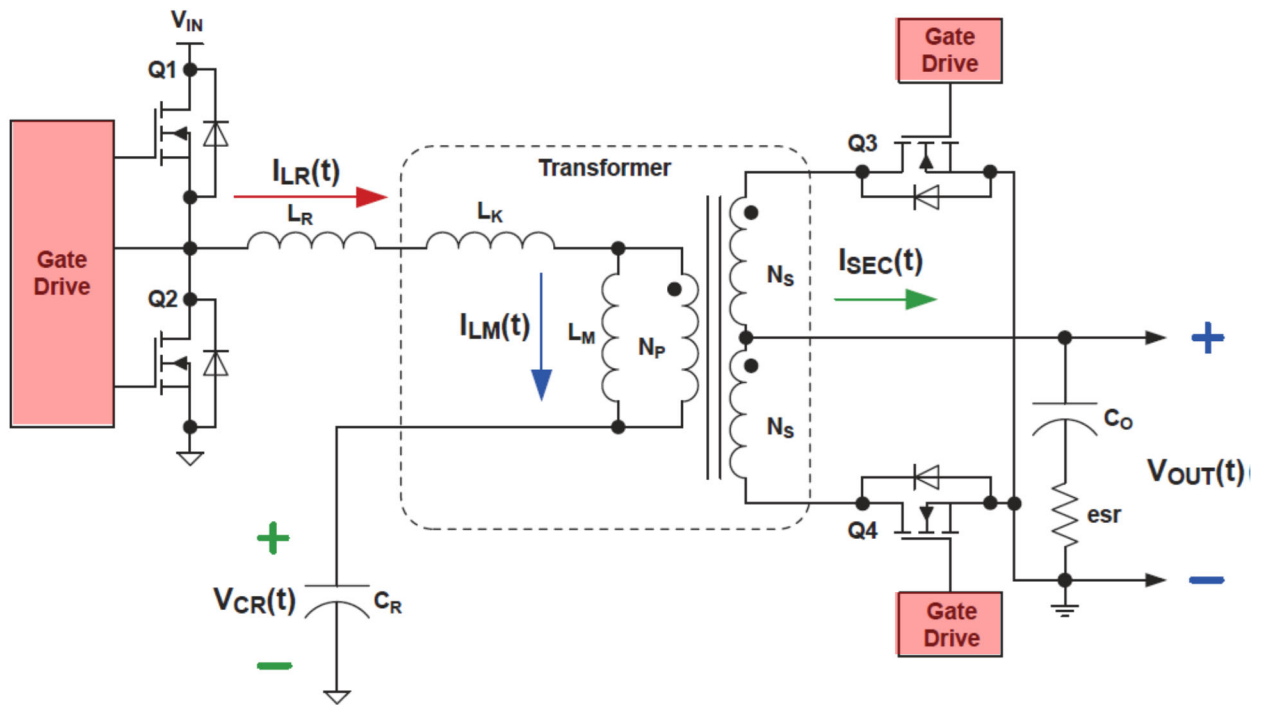
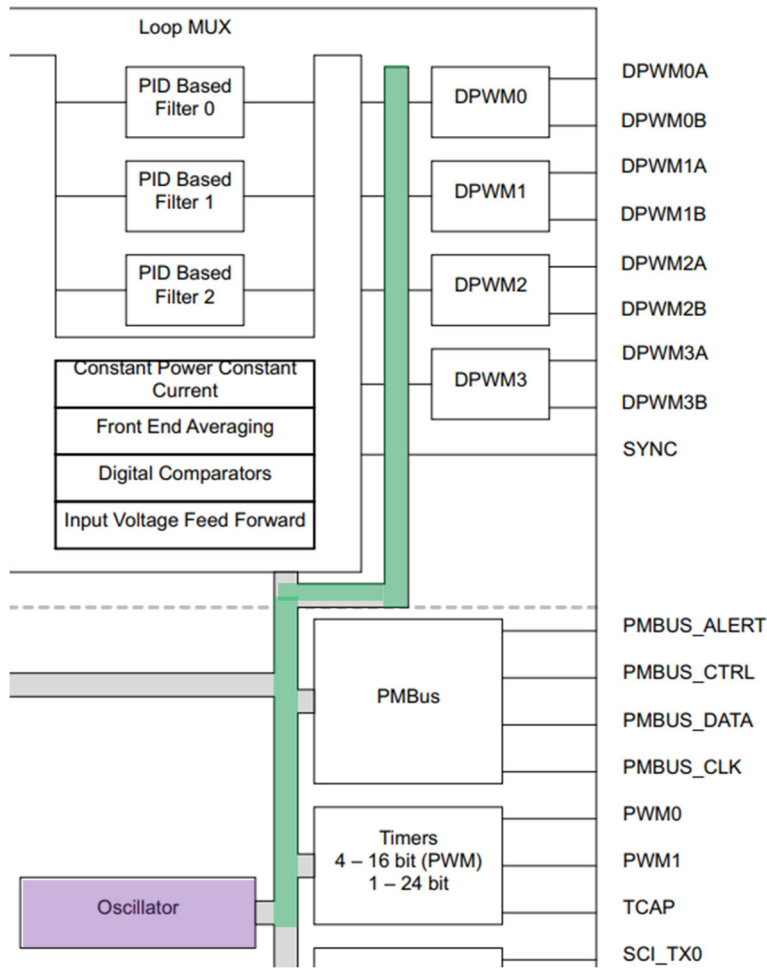


Figure 1 – Basic LLC schematic.

Ex. 1005, Figure 1. McDonald also states that its converter uses “a Texas Instruments UCD3138 digital controller” to facilitate “easy optimization and evaluation of the various control features.” Ex. 1005, 5-22. Therefore, TI UCD3138 operates as the controller for all the Gate Drives in McDonald.

77. TI UCD3138 discloses an oscillator with an oscillator frequency that generates clock signals. Ex. 1006, 9 (Fig. 2.4), 17. Figure 2.4 of TI UCD3138 (copied below) shows an Oscillator (in purple) that generates several clock signals (in green).



Ex. 1006, Fig. 2.4. The oscillator in TI UCD3138 has an internal oscillator frequency $f_{(PCLK)}$ with a typical frequency of 250 MHz. *Id.*, 17.

78. TI UCD3138 also teaches that its oscillator generates clock signals.

4.4.1.4 High Resolution DPWM

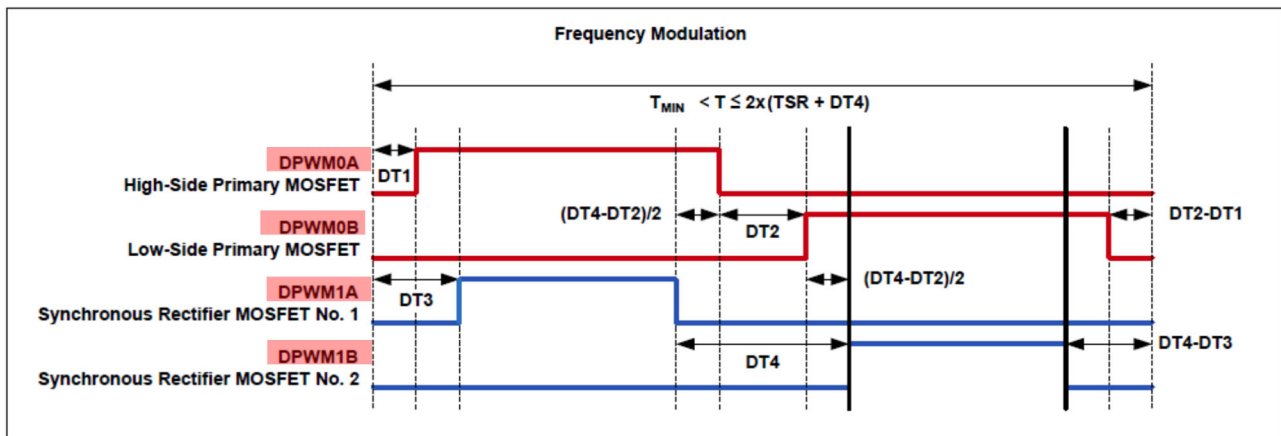
Unlike conventional PWM controllers where the frequency of the clock dictates the maximum resolution of PWM edges, the UCD3138 DPWM can generate waveforms with resolutions as small as 250 ps. This is 16 times the resolution of the clock driving the DPWM module.

This is achieved by providing the DPWM mechanism with 16 phase shifted clock signals of 250 MHz each. The high resolution section of DPWM can be enabled or disabled, also the resolution can be defined in several steps between 4ns to 250ps. This is done by setting the values of PWM_HR_MULTI_OUT_EN, HIRES_SCALE and ALL_PHASE_CLK_ENA inside the DPWM Control Register 1. See the Power Peripherals programmer's manual for details.

Id., 30.

- c. “generating timing control signals for each of a plurality of events based upon the clock signals in a (A) standard converter operating cycle, having a standard operating period and frequency, to:”

79. McDonald-TI UCD3138 renders this limitation obvious. Figure 25 of McDonald (copied below) discloses use of timing control signals DPWM0A, DPWM0B, DPWM1A, and DPWM1B (highlighted in red) to control both the primary switches (High-Side Primary MOSFET and Low-Side Primary MOSFET) and the secondary switches (Synchronous Rectifier MOSFET No. 1 and Synchronous Rectifier MOSFET No. 2).



Ex. 1005, Figure 25; *Id.*, 5-17 (“Figure 25 illustrate the exact timing relationships between the primary-side MOSFET control signals and the synchronous-rectifier control signals.”).

80. In addition, TI UCD3138 discloses that each DPWM can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

81. When TI UCD3138 is combined with McDonald, the timing control signals are based on clock signals in the resonant converter operating cycle, having a resonant period and frequency. Ex. 1005, 5-4 (“the operating frequency is exactly equal to the dominant frequency of the resonant tank.”). The resonant period and frequency is what the ’481 Patent refers to as the “standard” operating period and frequency.

- d. **“(i) turn the at least one primary switch ON and OFF at times when essentially zero voltage is impressed across the respective at least one primary switch and essentially zero resonant current is flowing in the respective at least one primary switch; and”**

82. McDonald-TI UCD3138 renders this limitation obvious. McDonald discloses that the primary switches Q1 and Q2 turn on and off with zero voltage switching (ZVS). Ex. 1005, 5-3 (“Figure 2 illustrates how this system achieves zero

voltage switching (ZVS) on Q1 and Q2. . . . State 1 shows that V_{DS} of Q2 is charged all the way to V_{IN} , with the inductor current flowing through the channel of Q1. When Q1 turns off, the current that was flowing through Q1's channel diverts and flows through the two capacitors, as shown in state 2.³ This state continues until the V_{DS} of Q2 has dropped low enough to forward-bias the diode across Q2. At this point operation transitions to state 3. Now the system is free to turn on Q2 with a near zero voltage, thus achieving the so-called ZVS, as shown in state 4.”)

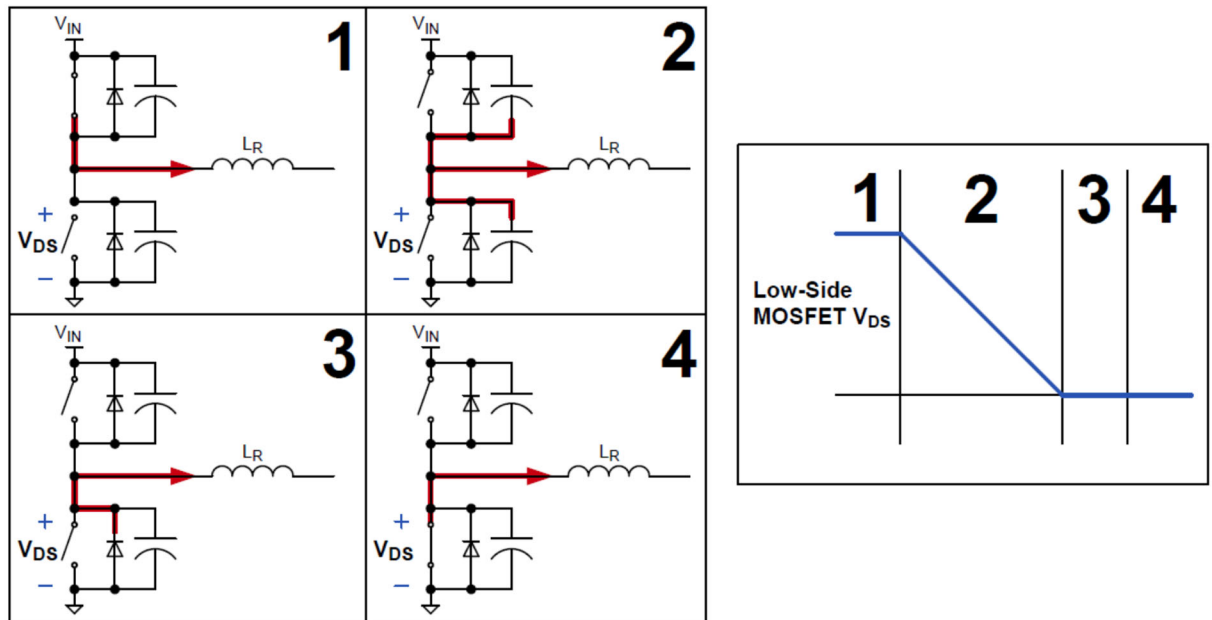


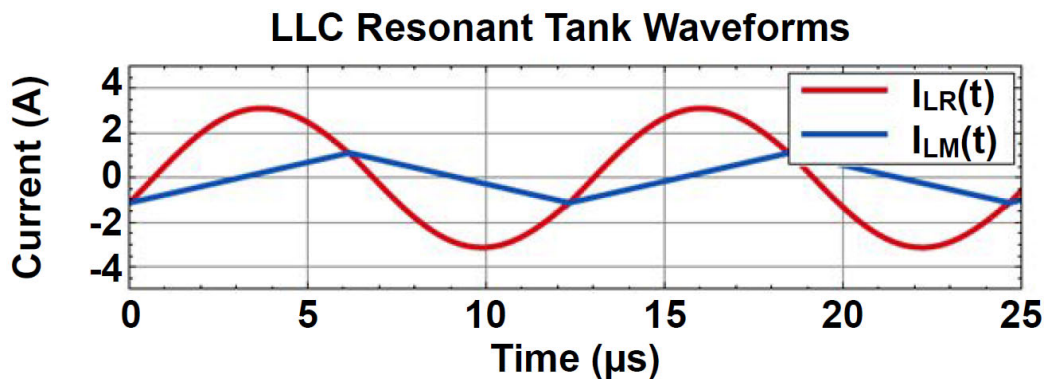
Figure 2 – Zero voltage switching.

Ex. 1005, 5-4.

³ The V_{DS} of Q2 remains at V_{IN} and thus Q1 has turned off with essentially zero voltage impressed across it.

83. McDonald also teaches that primary switches Q1 and Q2 turn on and off when zero resonant current is flowing in the switch. McDonald discloses a primary winding current I_{LR} , which is equal to the primary magnetizing current I_{LM} plus the resonant current I_{RES} ; in other words $I_{LR} = I_{LM} + I_{RES}$.⁴ Therefore, the resonant current is equal to the primary winding current minus the primary magnetizing current ($I_{RES} = I_{LR} - I_{LM}$). This means that the resonant current is zero when the primary winding current I_{LR} and primary magnetizing current I_{LM} are the same.

84. Figure 3 of McDonald (copied below) shows that the resonant current is zero at the points where I_{LR} (red waveform) and I_{LM} (blue waveform) are the same (i.e. at the minimum and maximum points of blue waveform I_{LM}).



⁴ This is the same equation disclosed in the '481 Patent, which states that “Fig. 3B shows the primary winding current, comprising both the resonant current (solid line) and the primary magnetizing current (dashed line).” Ex. 1001, 6:24-27.

85. McDonald also states that primary switches Q1 and Q2 are operated to generate a square wave, which produces the triangular-shaped magnetizing current I_{LM} in Figure 3.

To visualize this, recognize that Q1 and Q2 generate a square wave at the input to L_R . This square wave is filtered to produce a sine wave in $I_{LR}(t)$. The voltages across $L_R + L_K$ and C_R are 180 degrees out of phase and equal and opposite in magnitude. These voltages cancel out one another and produce a square wave voltage across L_M . This square wave produces the triangular-shaped current $I_{LM}(t)$ shown in Figure 3.

The input voltage is now reduced so that the system control effort changes the frequency to something below the resonant frequency, as defined by Equation 2.

$$f_i < \frac{1}{2\pi\sqrt{(L_R + L_K)C_R}} \quad (2)$$

Ex. 1005, 5-5. This means that the switches are switching on and off at the minimum and maximum points of the magnetizing current I_{LM} (blue waveform), and as I stated above there is zero resonant current at these points.

- e. **“(ii) turn the at least one secondary switch ON and OFF at times when essentially zero current is flowing in the respective at least one secondary switch and**

essentially zero voltage is impressed across the respective at least one secondary switch; and”

86. McDonald-TI UCD3138 renders this limitation obvious. McDonald teaches that secondary switches Q3 and Q4 turn on and off with zero current switching. Ex. 1005, 5-5 (“In Figures 3 and 4, notice that the current through Q3 and Q4 naturally decays to 0 A, providing zero current switching (ZCS) for these devices.”)

87. Figure 29 of McDonald (copied below) also shows zero current turn on and off of the secondary switches Q3 and Q4 because the secondary current I_{SEC} starts at zero and ends at zero.

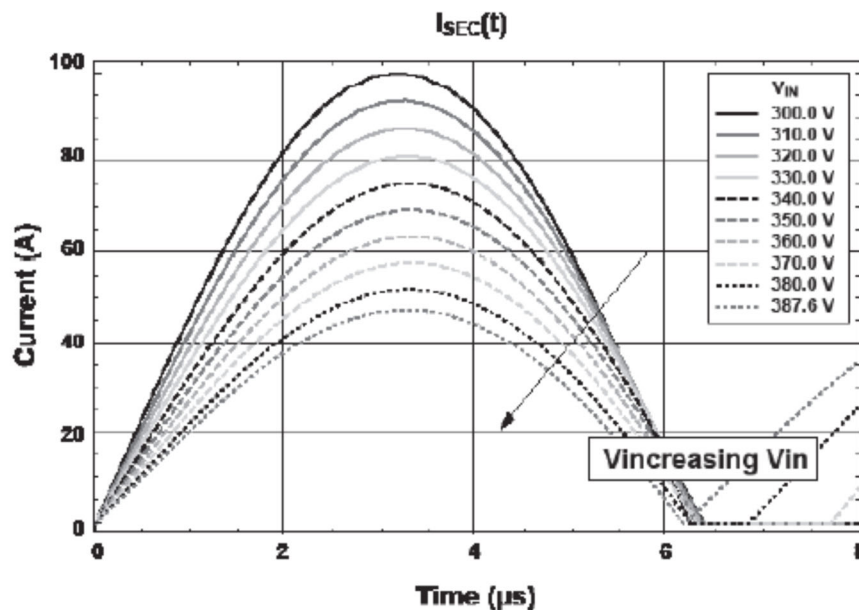


Figure 29 – Synchronous rectifier current and input voltage.

Ex. 1005, 5-19.

88. McDonald teaches that secondary switches Q3 and Q4 turn on and off with zero voltage switching. Ex. 1005, 5-21 (“Figures 32, 33 and 34 illustrate this

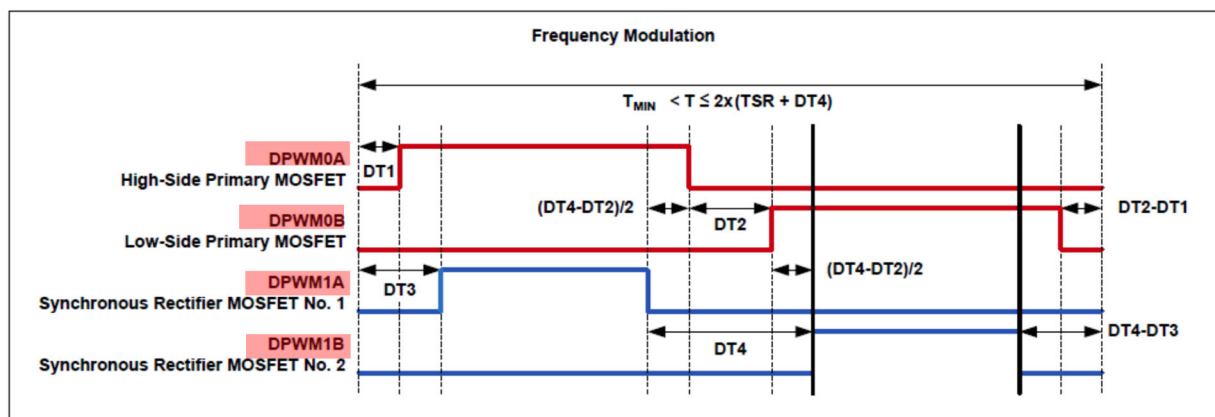
feature in action. . . . Notice that in all cases, the body-diode conduction time across the synchronous rectifiers is very close to minimum.”). A POSITA would understand that MOSFET switches inherently achieve zero voltage at turn off because when a MOSFET switch is on it has zero volts across it, and in the short time it takes to turn off, the voltage does not change significantly because the inherent capacitance of the device mitigates fast changes in voltages.

f. “wherein the oscillator frequency is preset, and”

89. McDonald-TI UCD3138 renders this limitation obvious. The oscillator in TI UCD3138 has an internal oscillator frequency $f_{(PCLK)}$ that is preset and has a typical frequency of 250 MHz. Ex. 1006, 17.

g. “the timing of the timing control signals for one or more selected events may be set independently of other timing control signals and events.”

90. McDonald-TI UCD3138 renders this limitation obvious. Figure 25 of McDonald (copied below) indicates that the timing of the timing control signals DPWM0A, DPWM0B, DPWM1A, and DPWM1B are set independently.



Ex. 1005, 5-18.

91. TI UCD3138 also discloses that timing of the timing control signals are independent, stating that the “DPWM module represents one complete PWM channel with 2 independent outputs, A and B.”

4.4.1.2 DPWM Module

The DPWM module represents one complete PWM channel with 2 independent outputs, A and B. Multiple DPWM modules within the UCD3138 system can be configured to support all key power topologies. DPWM modules can be used as independent PWM outputs, each controlling one power supply output voltage rail. It can also be used as a synchronized PWM—with user selectable phase shift between the PWM channels to control power supply outputs with multiphase or interleaved PWM configurations.

Ex. 1006, 27.

92. TI UCD3138 further discloses that the timing of the timing control signals for various events are independent of each other, by indicating that each DPWM can control different timing events.

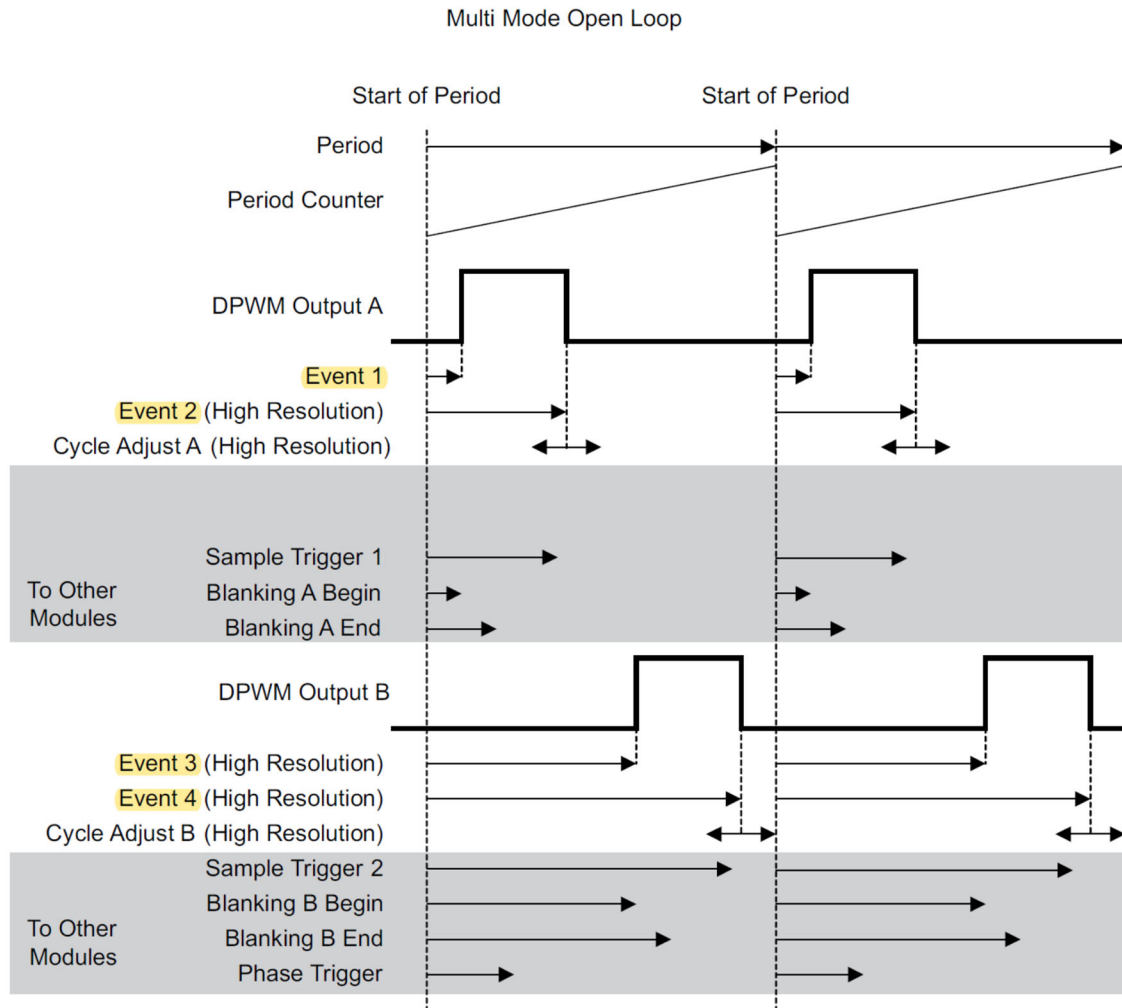
4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28. As can be seen in the Multi-Mode Open Loop figure (below) in TI UCD3138, the timing of the timing control signals is set independently because each

rising edge and falling edge of DPWM A and DPWM B are independent events (Event 1, Event 2, Event 3, and Event 4) and are not dependent on the timing of other events.



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
 DPWM A Falling Edge = Event 2 + Cycle Adjust A
 DPWM B Rising Edge = Event 3
 DPWM B Falling Edge = Event 4 + Cycle Adjust B
 Phase Trigger = Phase Trigger Register value

Ex. 1006, 29.

2. Claim 22

a. “The method of claim 1 further comprising”

93. See § VI.A.1 above.

b. “providing a gate drive circuit for operating selected switches in the converter and generating timing control signals based upon the clock signals to (a) initiate a transition of the selected switches from ON to OFF or OFF to ON, (b) hold the selected switches ON, and (c) hold the selected switches OFF.”

94. McDonald-TI UCD3138 renders this limitation obvious. Figure 1 of McDonald (copied below) shows use of Gate Drive circuits (in red), which are controlled by TI UCD3138, to control the switches Q1, Q2, Q3, and Q4. *Id.*

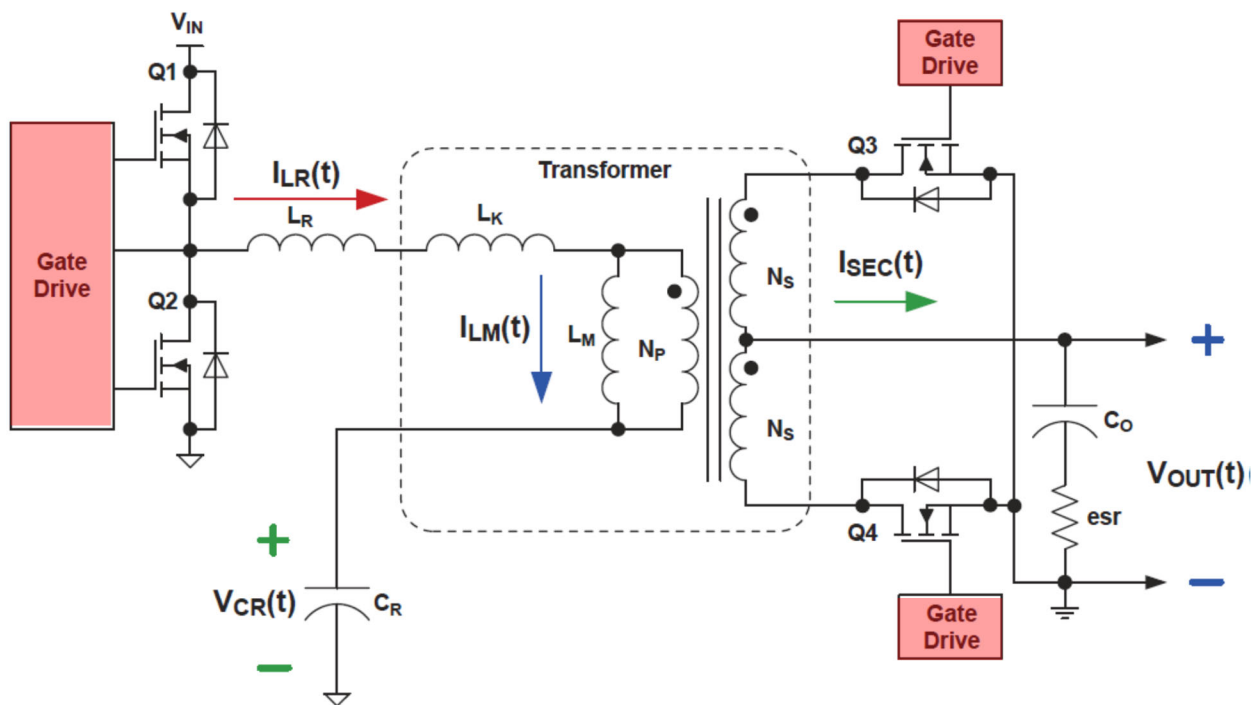
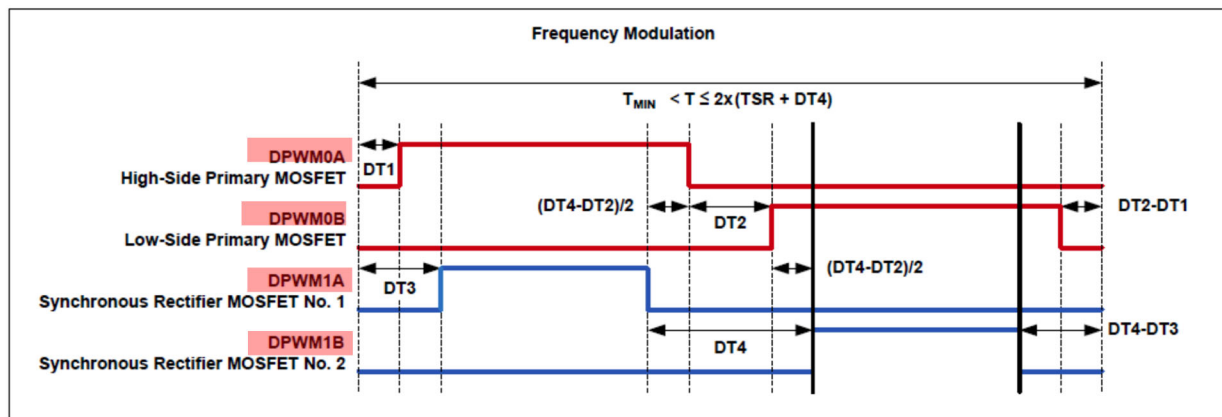


Figure 1 – Basic LLC schematic.

Ex. 1005, Figure 1.

95. Figure 25 of McDonald (copied below) also shows use of timing control signals DPWM0A, DPWM0B, DPWM1A, and DPWM1B (highlighted in red) to control both the primary switches Q1 and Q2 (High-Side Primary MOSFET and Low-Side Primary MOSFET) and the secondary switches Q3 and Q4 (Synchronous Rectifier MOSFET No. 1 and Synchronous Rectifier MOSFET No. 2).



Ex. 1005, 5-18.

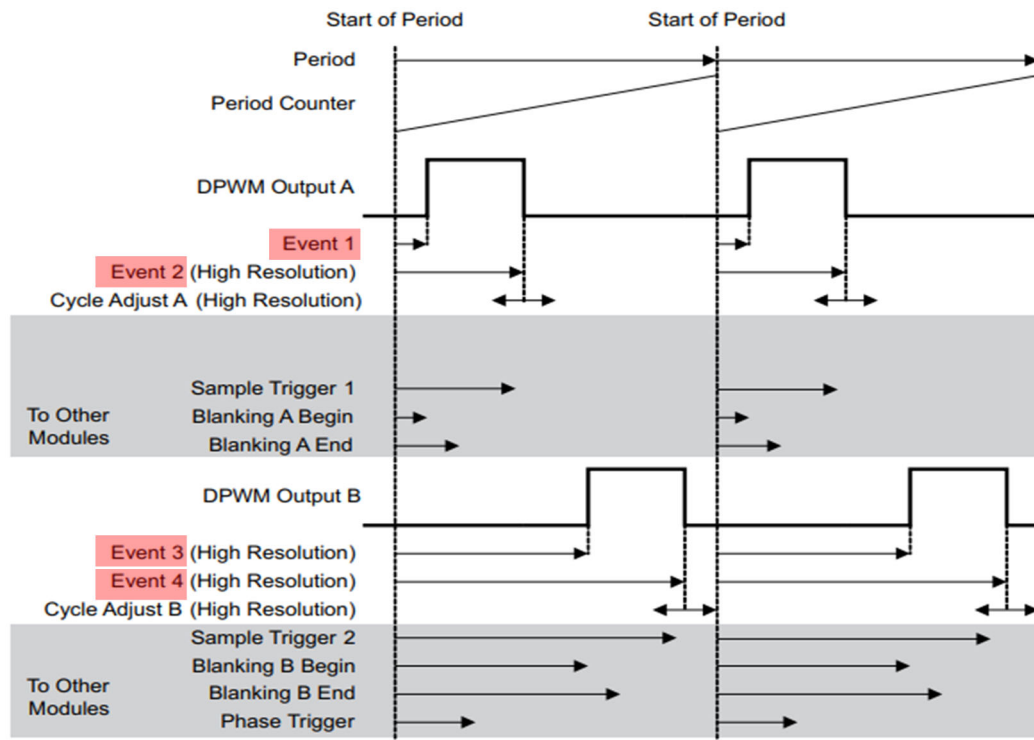
96. TI UCD3138 also discloses that each timing control signal DPWM can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28; *Id.*, 29 (figure below showing timing signals for different events).



Ex. 1006, 29.

3. Claim 31

- a. “The method of claim 1 wherein the generating timing control signals based upon the clock signals further comprises:”

97. See § VI.A.1.

- b. “counting the clock signals from the oscillator;”

98. McDonald-TI UCD3138 renders this limitation obvious. TI UCD3138 discloses that the DPWM’s control of the various timing events involves counting the clock signals from the oscillator.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

- c. “setting a count threshold for each event;”

99. McDonald-TI UCD3138 renders this limitation obvious. TI UCD3138 discloses that the DPWM sets a count threshold for each event.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

- d. **“generating the respective timing control signal for each event as the counting matches the respective count threshold.”**

100. McDonald-TI UCD 3138 renders this limitation obvious. TI UCD3138 discloses that the DPWM generates timing control signals for each event when the counting matches the count threshold.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Basic comparisons between the programmed registers and the DPWM counter can create the desired edge placements in the DPWM. High resolution edge capability is available on Events 2, 3 and 4.

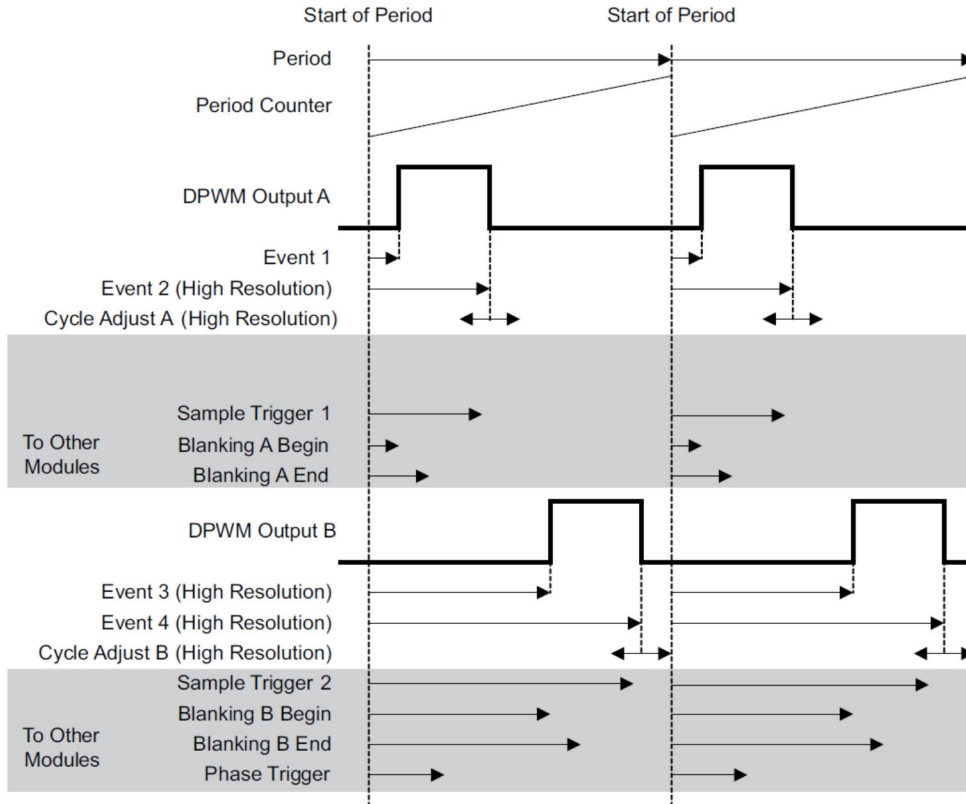
Ex. 1006, 28. *See also id.*, 31, 4.5 DPWM Modes of Operation (“... The DPWM logic causes transitions in many digital signals when the period counter hits the target value for that signal.”).

4. Claim 32

- a. **“The method of claim 31 wherein the oscillator and timing events are open-loop with respect to the power train.”**

101. McDonald-TI UCD3138 renders this limitation obvious. *See* § VI.A.3 above. TI UCD3138 shows a Multi-Mode Open Loop figure (below), stating that the DPWM is controlled entirely by its own registers, not by the filter output.

Multi Mode Open Loop



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
 DPWM A Falling Edge = Event 2 + Cycle Adjust A
 DPWM B Rising Edge = Event 3
 DPWM B Falling Edge = Event 4 + Cycle Adjust B
 Phase Trigger = Phase Trigger Register value

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

The drawing above is for multi-mode, open loop. Open loop means that the DPWM is controlled entirely by its own registers, not by the filter output. In other words, the power supply control loop is not closed.

Ex. 1006, 29.

5. Claim 33

- a. “The method of claim 31 wherein the oscillator or timing events are adjusted with feedback from measurements in the power train.”

102. McDonald-TI UCD3138 renders this limitation obvious. *See* § VI.A.3 above. McDonald discloses adjusting the oscillator and timing events with feedback from measurements in the power train. Ex. 1005, 5-19 (“Traditionally, you can solve this problem by using some kind of current sensing circuitry to determine when the synchronous rectifier should be on and off.”). TI UCD3138 also discloses this limitation of adjusting timing events with feedback, where the Filter provides the feedback function for the DPWM timing control signals.

These can be connected in many different combinations, with multiple filters and DPWMs. They are capable of supporting functions like input voltage feed forward, current mode control, and constant current/constant power, etc.. The simplest configuration is shown in the following figure:



Ex. 1006, 26.

6. Claim 34

- a. **“The method of claim 33 wherein the measurements and adjustments are performed during the manufacturing process.”**

103. McDonald-TI UCD3138 renders this limitation obvious. *See* § VI.A.4 above. TI UCD3138 discloses use of firmware data for certain measurements. Firmware is set during the manufacturing process. Ex. 1006, 22, 4.2 Memory (“Within the UCD31xx architecture, there is a 1024x32-bit Boot ROM that contains the initial firmware startup routines for PMBUS communication and non-volatile (FLASH) memory download. This boot ROM is executed after power-up-reset

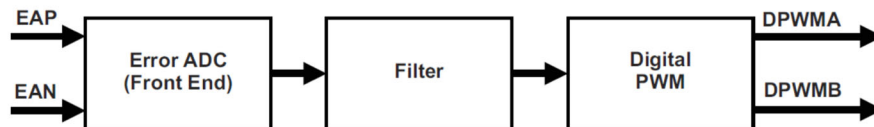
checks if there is a valid FLASH program written.”); Ex. 1006, 55, 4.23 Temperature Reference (“The temperature reference register (TEMPREF) provides the ADC12 count when ADC12 measures the internal temperature sensor (channel 14) during the factory trim and calibration. This information can be used by different periodic temperature compensation routines implemented in the firmware. But it should not be overwritten by firmware, otherwise this factory written value will be lost.”).

7. Claim 35

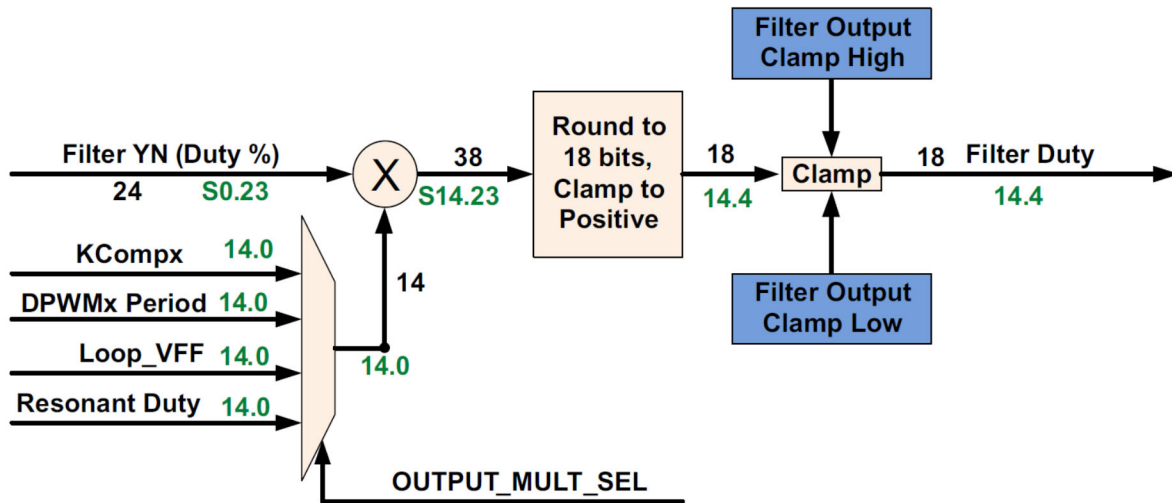
- a. **“The method of claim 33 wherein the measurements and adjustments are performed during operation as part of a closed-loop feedback system.”**

104. McDonald-TI UCD3138 renders this limitation obvious. *See* § VI.A.4 above. TI UCD3138 discloses that the measurements and adjustments are performed during operation of the device as part of a closed-loop feedback system, where the Filter provides the feedback.

These can be connected in many different combinations, with multiple filters and DPWMs. They are capable of supporting functions like input voltage feed forward, current mode control, and constant current/constant power, etc.. The simplest configuration is shown in the following figure:



Ex. 1006, 26.

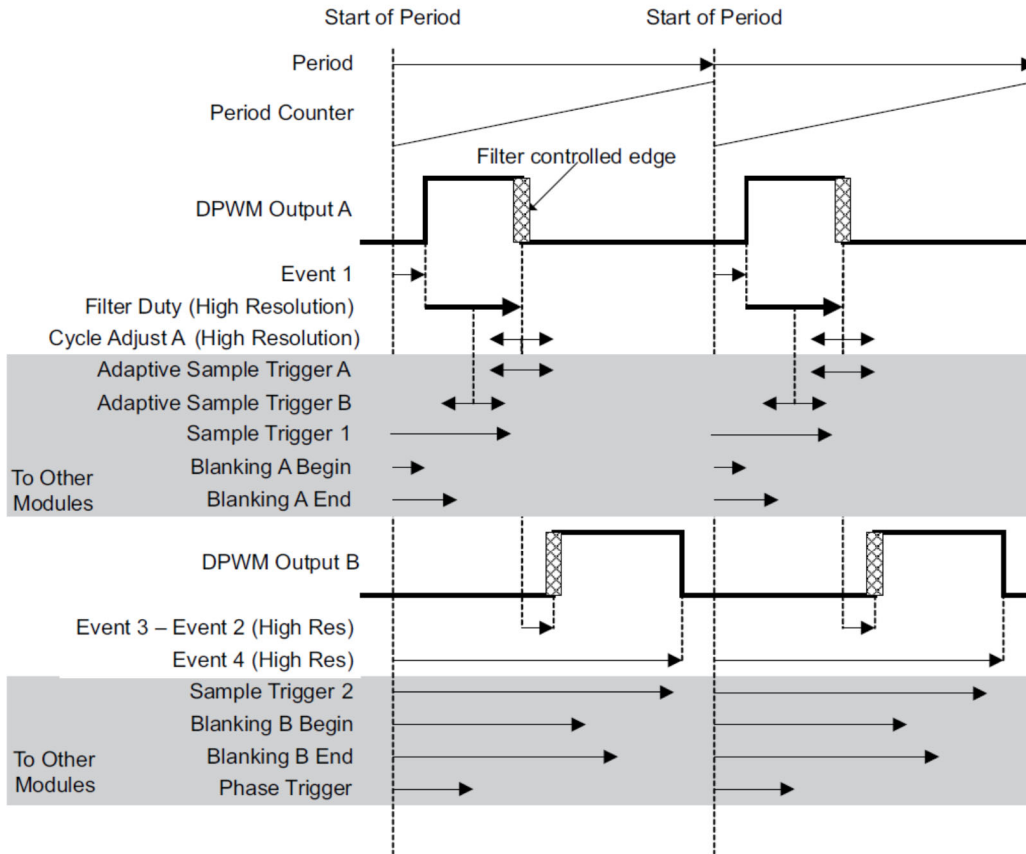


This permits the filter output to be multiplied by a variety of correction factors to match the DPWM Period, to provide for Voltage Feed Forward, or for other purposes. After this, there is another clamp. For resonant mode, the filter can be used to generate both period and duty cycle.

Ex 1006, 46.

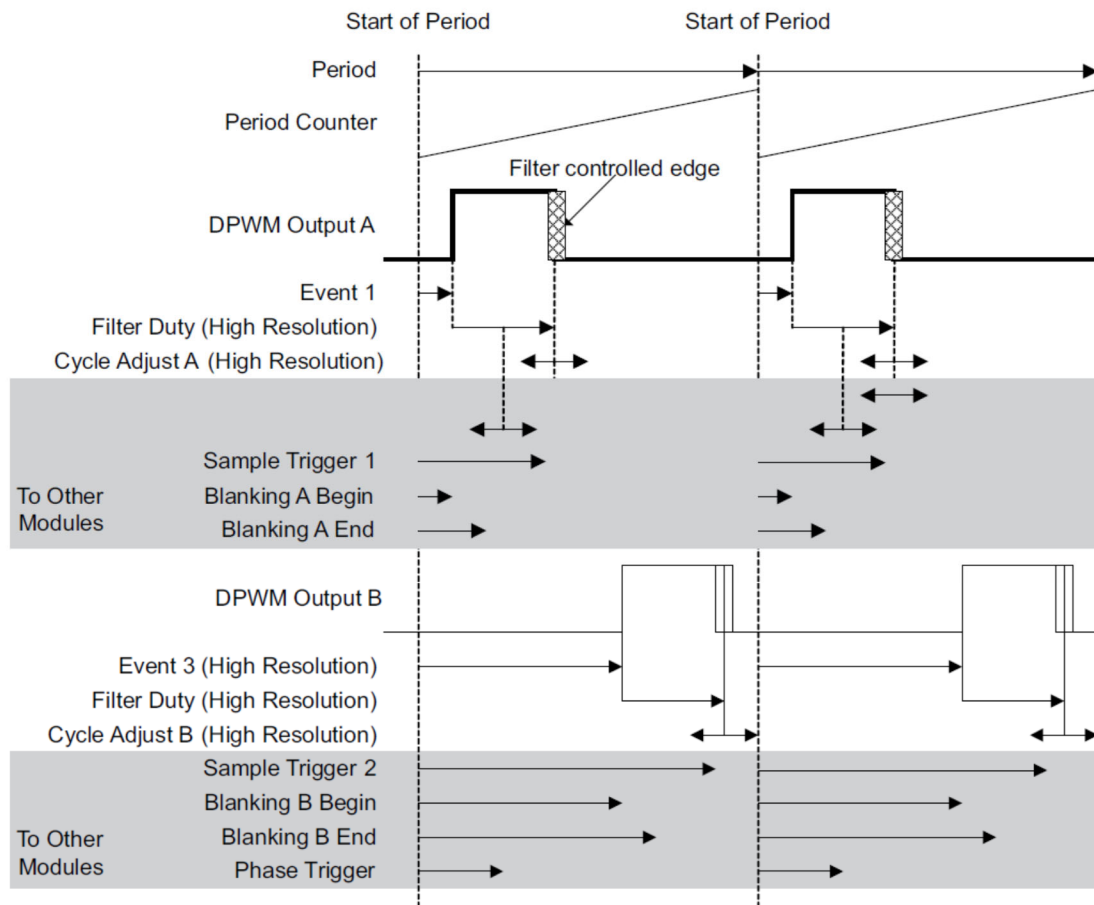
105. TI UCD3138 has several figures that disclose closed loop operation, as shown below.

Normal Mode Closed Loop

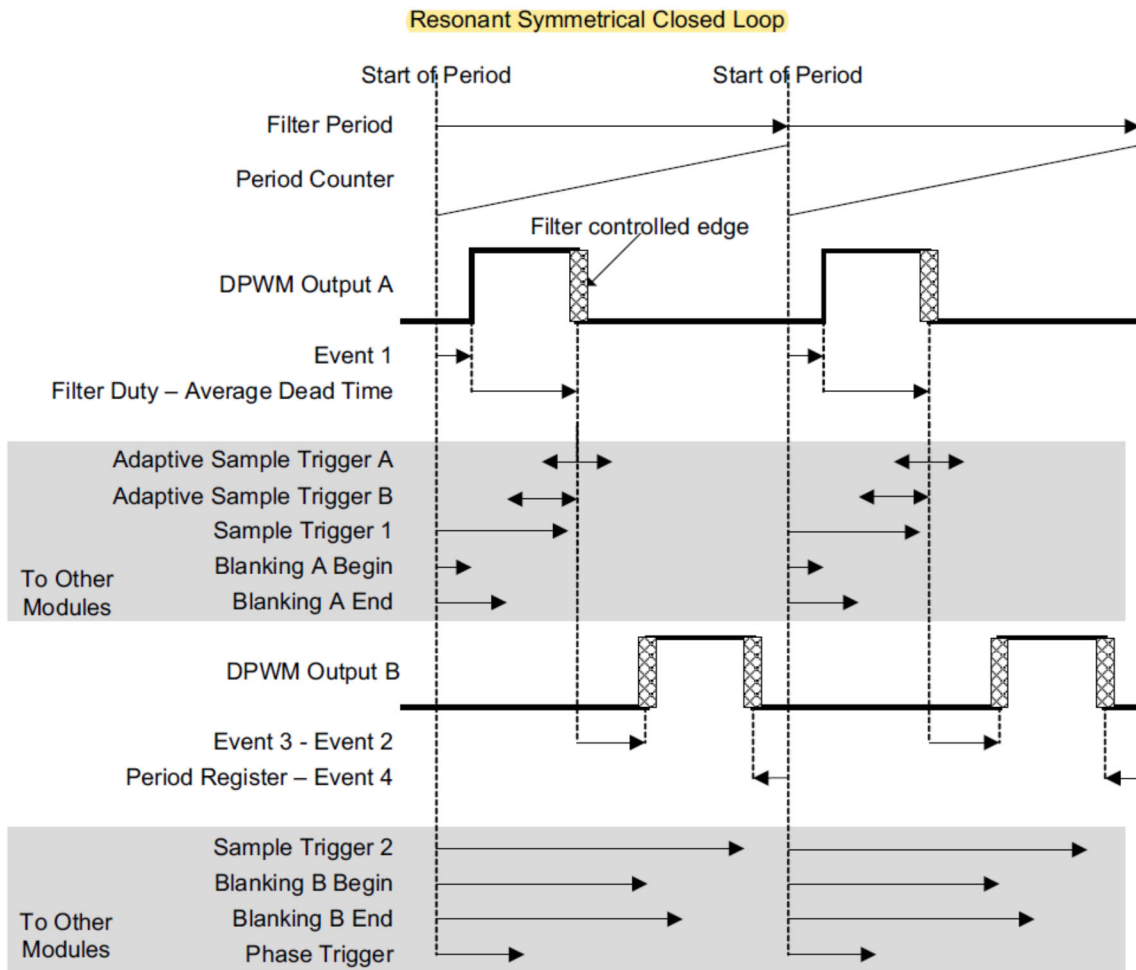


Id., 32.

Multi Mode Closed Loop



Id., 34.



Id., 36. See also, *Id.*, 37, 39.

B. The Challenged Claims are Obvious over Shimada in view of AAPA.

106. It is my opinion that Shimada (Exs. 1007-1008) combined with the AAPA renders obvious claims 1, and 22 of the '481 Patent.

107. A POSITA would have been motivated to combine Shimada with the AAPA for purposes of zero current and zero voltage switching because both are related to resonant converters, and Shimada contemplates zero current and zero voltage switching, which the AAPA explicitly teaches. A POSITA would therefore

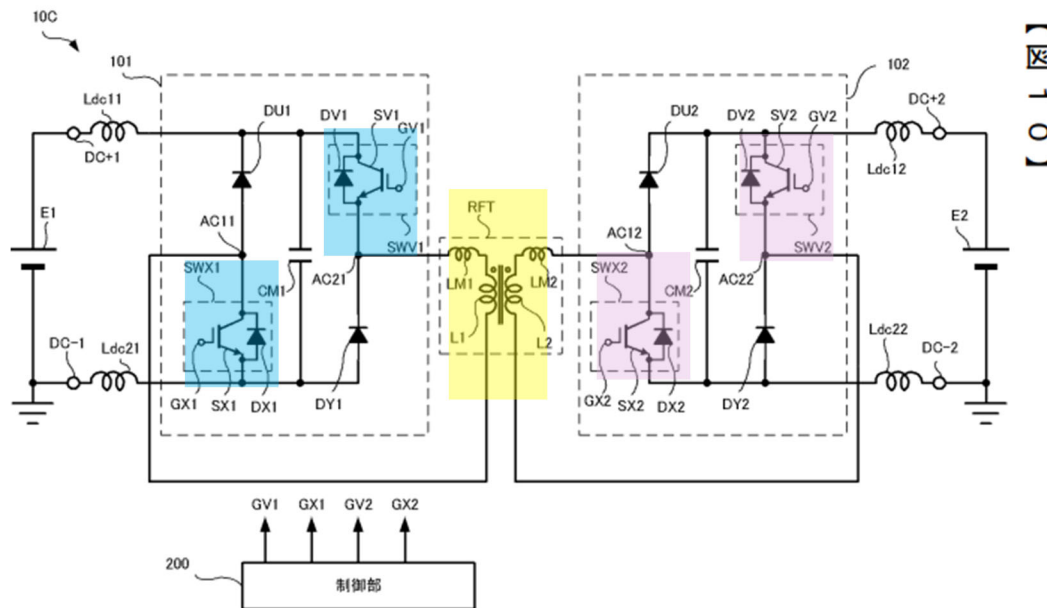
have understood and expected that the AAPA's teachings, which were generally known in the prior art, would apply to Shimada's resonant converter, and would have looked to the AAPA for additional details related to zero current and zero voltage switching.

1. Claim 1

- a. “A method of synchronously operating a power converter in a series of converter operating cycles the converter having at least one primary switch to drive a resonant power train and at least one secondary switch, the resonant power train including a transformer and having a characteristic resonant frequency and period, the method comprising:”**

108. Shimada discloses this limitation. Shimada discloses a method of synchronously operating a half-bridge power converter, where the converter has at least one primary switch that drives a resonant circuit, at least one secondary switch, and a transformer. Exs. 1007-1008, [0012], Fig. 10.

109. Figure 10 of Shimada (copied below) shows a half-bridge converter having primary switches SWV1 and SWX1 (in blue), a resonant circuit (LLC) on the primary side consisting of inductor L_{dc11} , inductor L_{dc21} , and capacitor C_{M1} , secondary switches SWV2 and SWX2 (in pink), and a transformer RFT (in yellow).



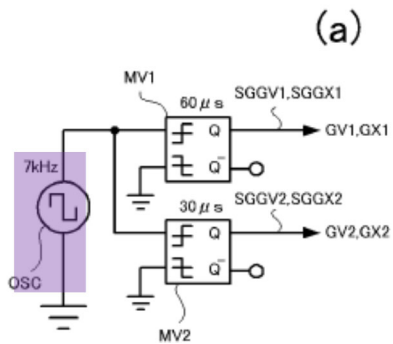
Exs. 1007-1008, Fig. 10. The resonant circuit has a resonant frequency and period.

b. “providing an oscillator for generating clock signals at an oscillator frequency;”

110. Shimada discloses an oscillator OSC for generating clock signals at an oscillator frequency f_1 . Exs. 1007-1008, [0137] (“Fig. 23(a) shows a control circuit that outputs gate signals SGGV1, SGGX1, SGGV2, and SGGX2 of the DC-DC converter using the one-directional MERS⁵ described above. This circuit is equipped with an oscillator OSC [shown in purple below] and one-shot multivibrators MV1 and MV2. The oscillator OSC outputs clock pulses with a frequency 7kHz (frequency f_1).”).

⁵ Magnetic Energy Recovery Switch

【 2 3 】



Exs. 1007-1008, Fig. 23(a).

- c. “generating timing control signals for each of a plurality of events based upon the clock signals in a (A) standard converter operating cycle, having a standard operating period and frequency, to:”

111. Shimada discloses that controller 200 generates timing control signals (gate signals) to control the primary and secondary switches. Exs. 1007-1008, [0031] (indicating that control unit 200 generates gate signals).

(0031)

Before the start of operation, the control unit 200 outputs all of the gate signals SGGV1, SGGX1, SGGV2, and SGGX2 as off signals and repeats the next cycle C1 on the basis of the pre-stored times d1 and d2 and the frequency f1 in response to a user instruction, for example.

In the cycle C1, the control unit 200 simultaneously switches all of the gate signals SGGV1, SGGX1, SGGV2, and SGGX2 from the off signal to the on signal. Then, time d2 after switching to the on signals, the gate signals SGGV2 and SGGX2 are switched from on signals to off signals, and then after another time (d1-d2) elapses, the gate signals SGGV1 and SGGX1 are switched from the on signals to the off signals.

The control unit 200 repeats this cycle C1 at the frequency f1.

Exs. 1007-1008, [0031].

112. A POSITA would understand that in Shimada, the converter operating cycle would have a standard operating period and frequency, which is the resonant period and frequency of the resonant converter, because Shimada discusses achieving ZVS and ZCS, and this requires a resonant frequency.

- d. **“(i) turn the at least one primary switch ON and OFF at times when essentially zero voltage is impressed across the respective at least one primary switch and essentially zero resonant current is flowing in the respective at least one primary switch; and”**

113. Shimada in combination with the AAPA (“Shimada-AAPA”) renders this limitation obvious. Shimada discusses zero voltage and zero current switching on the primary switches.

(0127)

As can be seen from FIG. 20A to 20C, when switching the gate signals from the on signal to the off signal, the capacitor voltage of that MERS is almost zero, and when switching the gate signals from the off signal to the on signal, the current flowing in the inductor L_m is almost zero. Therefore, the switching of each switch is at zero voltage or zero current, and soft switching is achieved with both high and low charges per time.

Exs. 1007-1008, [0127].

114. The AAPA discloses that zero voltage and zero current switching can be used to turn the primary switches on and off. For example, the AAPA discloses turning on (closing) a primary switch (S1) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32.

115. The AAPA also discloses turning off (opening) a primary switch S1 “when the sinusoidal current flow completes half-cycle, and the current I_{pri} returns substantially to zero” and “the voltages across switches S2-120 and S4-140 decline toward zero.” *Id.*, 1:36-43.

- e. **“(ii) turn the at least one secondary switch ON and OFF at times when essentially zero current is flowing in the respective at least one secondary switch and**

essentially zero voltage is impressed across the respective at least one secondary switch; and”

116. Shimada-AAPA renders this limitation obvious. Shimada discusses zero voltage and zero current switching on the secondary switches.

(0127)

As can be seen from FIG. 20A to 20C, when switching the gate signals from the on signal to the off signal, the capacitor voltage of that MERS is almost zero, and when switching the gate signals from the off signal to the on signal, the current flowing in the inductor L_m is almost zero. Therefore, the switching of each switch is at zero voltage or zero current, and soft switching is achieved with both high and low charges per time.

Exs. 1007-1008, [0127].

117. The AAPA discloses that zero voltage and zero current switching can be used to turn the secondary switches on and off. For example, the AAPA discloses that “the VTM may include secondary switches turned on and off essentially at times of zero voltage to rectify power from the transformer. The VTM may include secondary switches on and off essentially at times of zero current to rectify power from the transformer.” Ex. 1009, 9:25-29.

118. The AAPA also discloses turning on (closing) a secondary switch (S3) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32.

119. The AAPA further discloses that “the voltage across one or more of the switches may be monitored to establish the timing of a zero-voltage switching or zero-current switching event.” *Id.* 1:66-2:3.

120. The AAPA further discloses that “the timing architecture of the SAC topology supports . . . ZCS and ZVS operation of the secondary switches.” Ex. 1009, 18:49-56.

f. “wherein the oscillator frequency is preset, and”

121. Shimada discloses that the oscillator frequency f_1 is preset. Exs. 1007-1008, [0137] (“The oscillator OSC outputs clock pulses with the frequency 7kHz (frequency f_1).”).

g. “the timing of the timing control signals for one or more selected events may be set independently of other timing control signals and events.”

122. Shimada teaches that timing of the timing control signals (gate signals) are independent. Exs. 1007-1008, [0028]-[0029].

(0028)

The control unit 200 is configured from a computer provided with, for example, a processor such as a central processing unit (CPU) and a memory device such as a random access memory (RAM) or a read only memory (ROM).

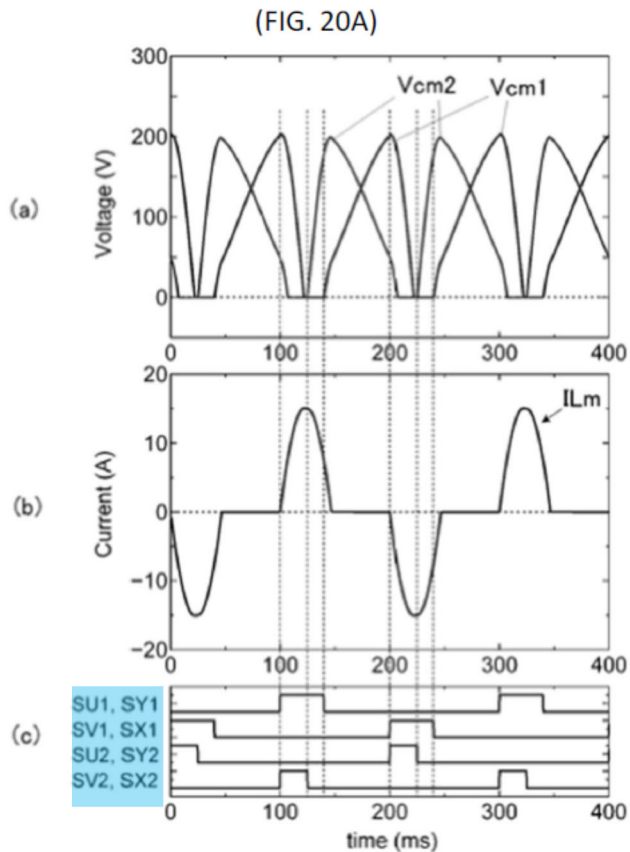
The control unit 200 uses the processor to read and execute, for example, a program stored in advance in the memory device, and by repeating the processing described below, e.g., the cycle described below, supplies the gate signals SGGV1, SGGX1, SGGV2, and SGGX2 to the gates GV1, GX1, GV2, and GX2, respectively.

(0029)

Each gate signal indicates on or off for a semiconductor switch provided with a gate to which the gate signal is supplied. For example, a gate signal that indicates on (on signal) has a voltage high enough to turn on the semiconductor switch (high level voltage), and a gate signal that indicates off (off signal) has a voltage low enough to turn off the semiconductor switch (low level voltage).

Ex. 1008, [0028]-[0029].

123. Figure 20A of Shimada also shows independent timing signals (in blue) for various events.



Ex. 1008, Fig. 20A.

2. Claim 22

a. “The method of claim 1 further comprising”

124. *See* § VI.B.1.

b. “providing a gate drive circuit for operating selected switches in the converter and generating timing control signals based upon the clock signals to (a) initiate a transition of the selected switches from ON to OFF or OFF to ON, (b) hold the selected switches ON, and (c) hold the selected switches OFF.”

125. Shimada discloses this limitation. Shimada discloses that “Fig. 23(b) shows a control circuit that outputs gate signals SGGU1, SGGV1, SGGX1, SGGY1, SGGU2, SGGV2, SGGX2, AND SGGY2 of the DC/DC converter using the

bidirectional MERS described above. The circuit is equipped with one-shot multivibrators MU1 and MU2 in addition to the control section 200 described in FIG. 23(a). . . . The one-shot multivibrator MU1 responds to the rising clock pulse output by the oscillator OSC by switching the off signal to the on signal, holding the on signal for 60 microsecond, and then switching to the off signal. . . . The one-shot multivibrator MU2 responds to the rising clock pulse output by the oscillator OSC, switches the off signal to the on signal, holds the on signal for 30 microseconds, and then switches to the off signal.”). Exs. 1007-1008, [0138].

C. The Challenged Claims are Obvious over Chen in view of AAPA

126. Chen (Ex. 1010) combined with the AAPA renders obvious claims 1, and 22 of the '481 Patent.

127. A POSITA would have been motivated to combine Chen with the AAPA for purposes of zero current and zero voltage switching because both are related to resonant converters, and Chen contemplates zero current and zero voltage switching, which the AAPA explicitly teaches. A POSITA would therefore have understood and expected that the AAPA's teachings, which were generally known in the prior art, would apply to Chen's resonant converter, and would have looked to the AAPA for additional details related to zero current and zero voltage switching.

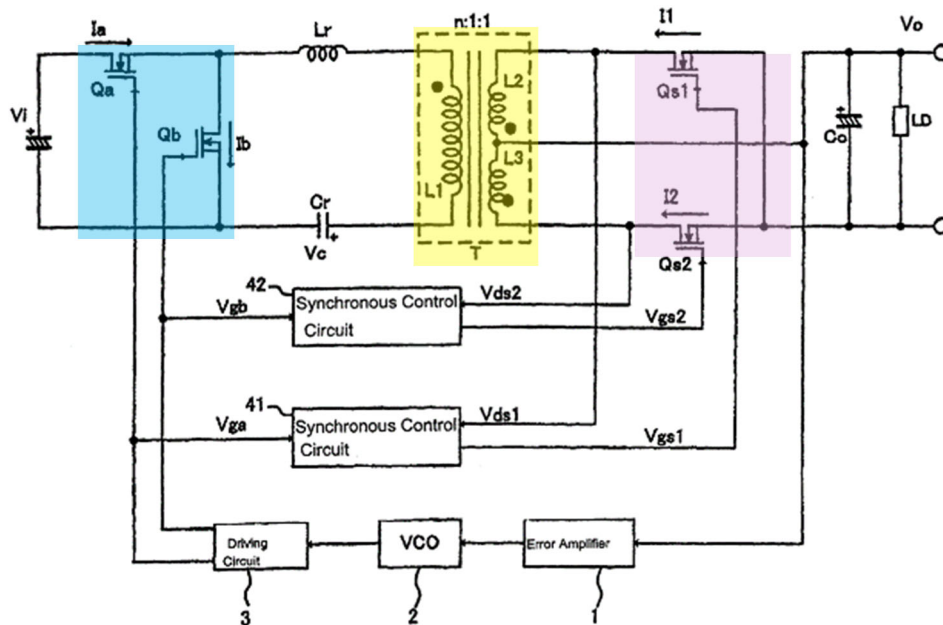
1. Claim 1

- a. “A method of synchronously operating a power converter in a series of converter operating cycles the**

converter having at least one primary switch to drive a resonant power train and at least one secondary switch, the resonant power train including a transformer and having a characteristic resonant frequency and period, the method comprising:”

128. Chen discloses this limitation. Chen teaches a method of synchronously operating a half-bridge power converter, where the converter has at least one primary switch that drives a resonant circuit, at least one secondary switch, and a transformer. Ex. 1010, 9:25-28 (“MOSFETs Qa, Qb are main switching elements which switch the current path to the series resonance circuit by switching in alternation on the primary side of the transformer T”); *Id.*, 9:43-47 (“The other end of secondary windings L2 and tertiary windings L3 are connected, via synchronous rectification MOSFETs Qs1 and Qs2 respectively, to the other ends on the ground side of the output capacitor Co and the load L.”).

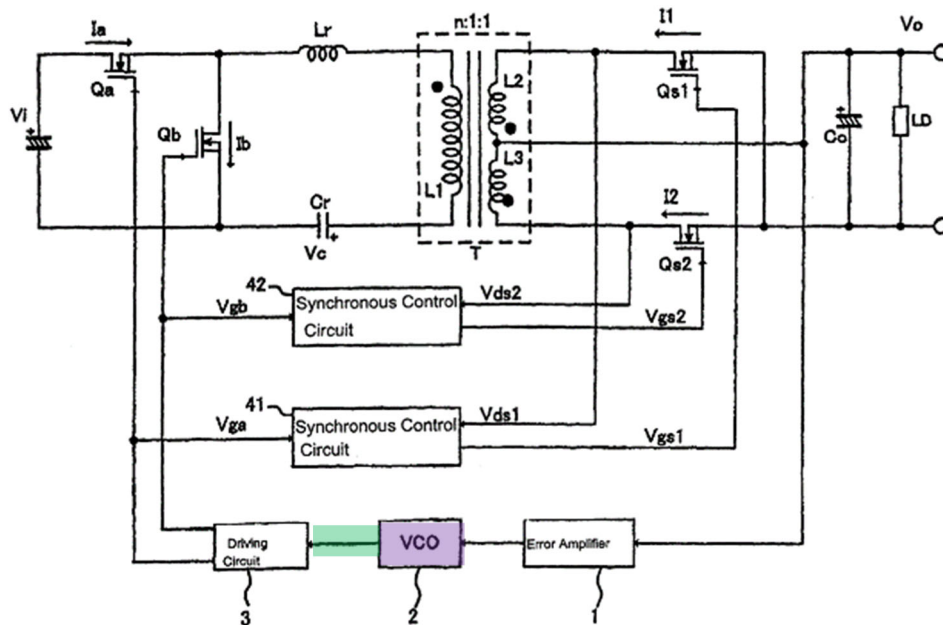
129. Figure 1 of Chen (copied below) shows a half-bridge converter having primary MOSFET switches Qa and Qb (in blue), a resonant circuit on the primary side consisting of inductor L_r and capacitor C_r , secondary switches Qs1 and Qs2 (in pink), and a transformer T (in yellow).



Ex. 1010, Fig. 1. The resonant circuit has a resonant frequency and period.

b. “providing an oscillator for generating clock signals at an oscillator frequency;”

130. Chen discloses an oscillator VCO for generating clock signals at an oscillator frequency. Ex. 1010, 9:57 (noting that VCO is a “voltage controlled oscillator circuit.”). Figure 1 of Chen (below) shows oscillator VCO (in purple), which inherently generates clock signals (in green) at the oscillator frequency. *Id.*



Ex. 1010, Fig. 1.

- c. “generating timing control signals for each of a plurality of events based upon the clock signals in a (A) standard converter operating cycle, having a standard operating period and frequency, to:”

131. Chen discloses this limitation. Chen shows that the Driving Circuit generates timing control signals (gate signals and synchronous driving signals) to control primary switches Qa and Qb and secondary switches Qs1 and Qs2.

The output voltage V_O supplied to the load LD is fed back 55
to the driving circuit 3 of the MOSFETs Qa, Qb via the error
amplifier 1 and a VCO (voltage controlled oscillator circuit)
2. Here, gate signals Vga, Vgb which are turned on and off in
alternation with prescribed timing are generated in the driving
circuit 3, and the currents Ia, Ib of the MOSFETs Qa, Qb are 60
controlled so as to flow in the directions of the arrows with
prescribed timing. The current Ib flows in the direction oppo-
site the arrow depending on operating conditions. Here, the
output frequency of the VCO 2 is changed to be higher when
it is judged from the output of the error amplifier 1 that the 65
output voltage V_O is higher than a preset voltage, or that the
load LD is a light load. Conversely, when it is judged that the

Ex. 1010, 9:58-62; *Id.*, 10:10-14 (“And, synchronous driving signals Vgs1, Vgs2
which control the on periods of the synchronous rectification MOSFETs Qs1, Qs2
are output from these synchronous control circuits 41, 42 respectively.”); *Id.* Fig. 1.

132. A POSITA would understand that in Chen the converter operating cycle
would have a standard operating period and frequency, which is the resonant period
and frequency of the resonant converter, because Chen discusses achieving ZCS,
and this requires a resonant frequency.

- d. **“(i) turn the at least one primary switch ON and OFF
at times when essentially zero voltage is impressed
across the respective at least one primary switch and
essentially zero resonant current is flowing in the
respective at least one primary switch; and”**

133. Chen in combination with the AAPA (“Chen-AAPA”) renders this
limitation obvious. Chen discusses zero current switching on the secondary
switches. Ex. 1010, 5:51-63 (“When the secondary current Is decreases and

becomes zero . . . Then, the comparison signal V_{dsc} is inverted, the MOSFET is turned off By this means, the comparison signal V_{dsc} is again inverted, the MOSFET is again turned on . . .”).

134. The AAPA discloses that zero voltage and zero current switching can be used to turn the primary switches on and off. For example, the AAPA discloses turning on (closing) a primary switch (S1) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32.

135. The AAPA also discloses turning off (opening) a primary switch S1 “when the sinusoidal current flow completes half-cycle, and the current I_{pri} returns substantially to zero” and “the voltages across switches S2-120 and S4-140 decline toward zero.” *Id.*, 1:36-43.

- e. **“(ii) turn the at least one secondary switch ON and OFF at times when essentially zero current is flowing in the respective at least one secondary switch and essentially zero voltage is impressed across the respective at least one secondary switch; and”**

136. Chen-AAPA renders this limitation obvious. The AAPA discloses that zero voltage and zero current switching can be used to turn the secondary switches on and off. For example, the AAPA discloses that “the VTM may include secondary switches turned on and off essentially at times of zero voltage to rectify power from

the transformer. The VTM may include secondary switches on and off essentially at times of zero current to rectify power from the transformer.” Ex. 1009, 9:25-29.

137. The AAPA also discloses turning on (closing) a secondary switch (S3) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32.

138. The AAPA further discloses that “the voltage across one or more of the switches may be monitored to establish the timing of a zero-voltage switching or zero-current switching event.” *Id.* 1:66-2:3.

139. The AAPA further discloses that “the timing architecture of the SAC topology supports . . . ZCS and ZVS operation of the secondary switches.” Ex. 1009, 18:49-56.

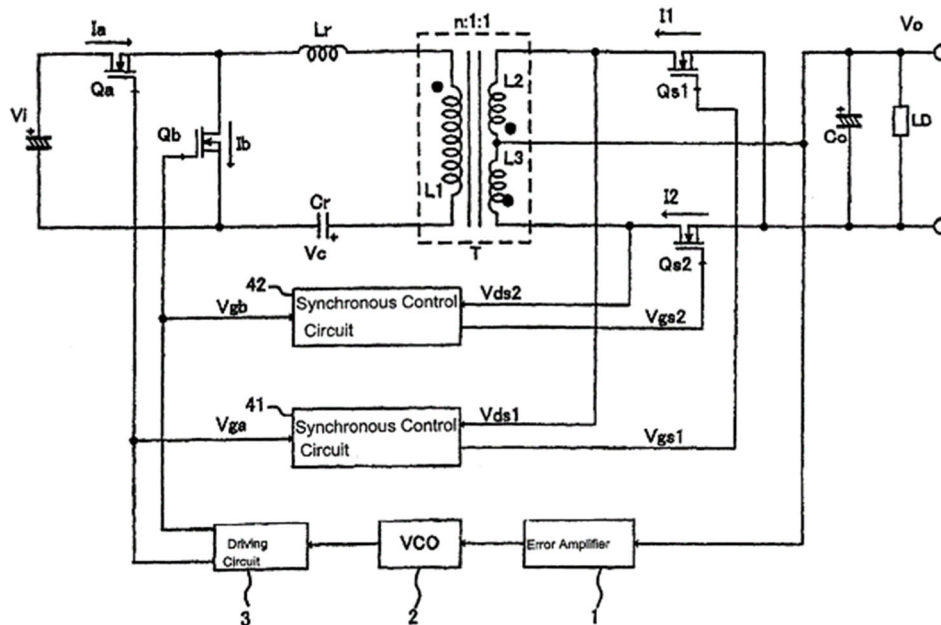
f. “wherein the oscillator frequency is preset, and”

140. Chen discloses that the oscillator frequency from VCO has 2 preset frequencies, a higher frequency and a lower frequency, depending on conditions from the error amplifier. Ex. 1010, 9:64-10:5 (“Here, the output frequency of the VCO 2 is changed to be higher when it is judged from the output of the error amplifier 1 that the output voltage V_o is higher than a preset voltage, or that the load LD is a light load. Conversely, when it is judged that the output voltage V_o is lower than the preset voltage, or that the load LD is heavy, the VCO 2 functions to the lower output frequency.”).

- g. “the timing of the timing control signals for one or more selected events may be set independently of other timing control signals and events.”

141. Chen discloses that the timing of the timing control signals for the secondary switches (synchronous driving signals V_{gs1} and V_{gs2}) are independent of the timing control signals of the primary switches. Ex. 1010, 10:15-18 (“As explained below, these synchronous driving signals V_{gs1} , V_{gs2} turn on the MOSFETs Q_{s1} , Q_{s2} respectively synchronized to the slower timing among the on timing of the MOSFETs Q_a , Q_b .”).

142. Figure 1 of Chen (below) further shows that synchronous driving signals V_{gs1} and V_{gs2} are output from Synchronous Control Circuits 41 and 42, which makes them independent of gate signals V_{ga} and V_{gb} which are generated directly by the Driving Circuit 3.



Ex. 1010, Fig. 1.

2. Claim 22

a. “The method of claim 1 further comprising”

143. See § VI.C.1.

b. “providing a gate drive circuit for operating selected switches in the converter and generating timing control signals based upon the clock signals to (a) initiate a transition of the selected switches from ON to OFF or OFF to ON, (b) hold the selected switches ON, and (c) hold the selected switches OFF.”

144. Chen discloses this limitation. Chen discloses that “gate signals Vga, Vgb which are turned on and off in alternation with prescribed timing are generated in the Driving Circuit 3, and the currents Ia, Ib of the MOSFETs Qa, Qb are controlled so as to follow in the directions of the arrows with prescribed timing.”

Ex. 1010, 9:58-62.

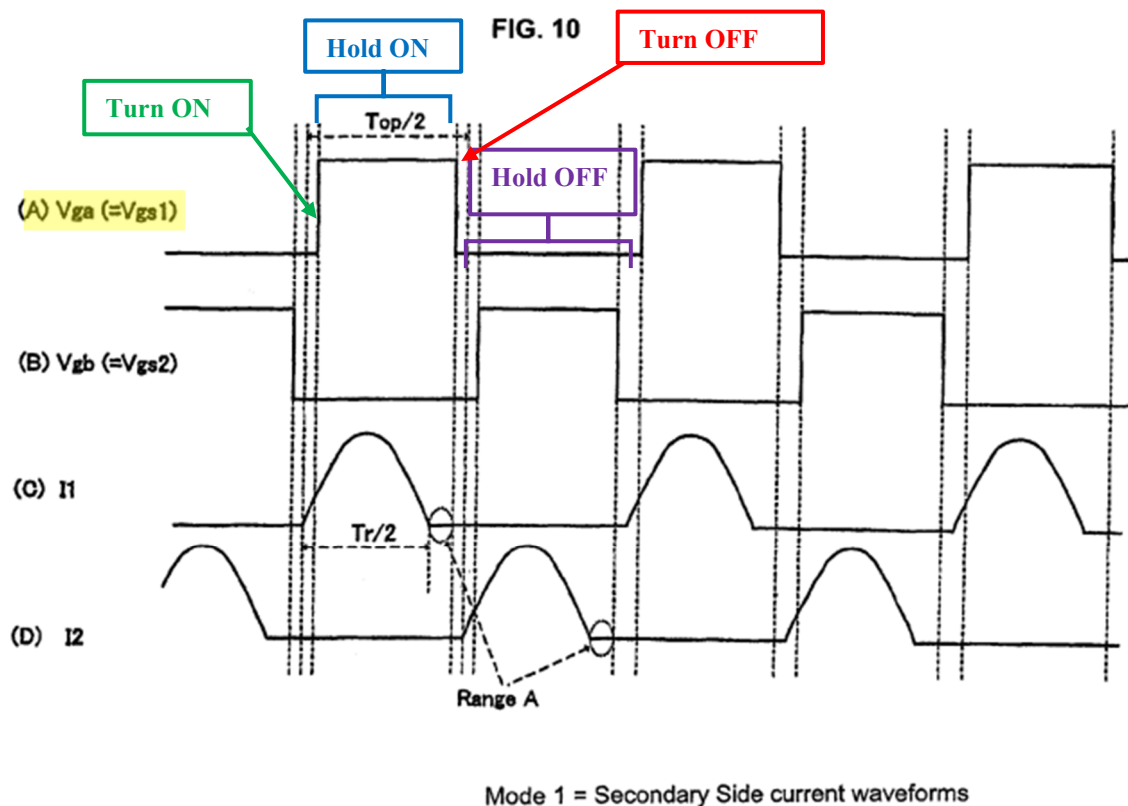
145. Chen also discloses that the Driving Circuit 3 generates synchronous driving signals Vgs1, Vgs2 to control on and off periods of the synchronous rectification MOSFETs Qs1, Qs2.

5 Synchronous control circuits 41 and 42, to which the gate signals V_{ga} and V_{gb} generated by the driving circuit 3 are respectively input, are provided in the switching power supply device. These synchronous control circuits 41, 42 further take as inputs the cross-terminal voltage signals V_{ds1} , V_{ds1} across the sources and drains of the synchronous rectification MOSFETs Q_{s1} , Q_{s2} . And, synchronous driving signals V_{gs1} , V_{gs2} which control the on periods of the synchronous rectification MOSFETs Q_{s1} , Q_{s2} are output from these synchronous control circuits 41, 42 respectively. As explained below, these synchronous driving signals V_{gs1} , V_{gs2} turn on the MOSFETs Q_{s1} , Q_{s2} respectively synchronized to the slower timing among the on timing of the MOSFETs Q_a , Q_b , or the conduction timing of the internal diodes D_s (see FIG. 2) detected from the cross-terminal voltage signals V_{ds1} , V_{ds2} of the MOSFETs Q_{s1} , Q_{s2} . Hence in this switching power

Id., 10:4-16. A POSITA would understand that “control the on periods” means that V_{gs1} , V_{gs2} control when the Q_{s1} , Q_{s2} turn on and turn off, which defines the “on periods.”

146. Chen further discloses that “in the first operating mode (Mode 1), the synchronous driving signal V_{gs} turns off the MOSFET Q_s in synchronization with the earlier timing among the turn-off timing of the gate signal V_{gp} . . . Further, in the second and fifth operating modes (Modes 2 and 5), the synchronous driving signal V_{gs} turns on the MOSFET Q_s in synchronization with the later timing among the timing with which the maximum on-width signal T_{mot} indicates the on state”. *Id.*, 16:5-23.

147. The timing waveform for V_{gs} in Figure 10 of Chen (copied below) shows that in addition to turning the MOSFET switches on (green) and off (red), they can also hold the MOSFETs on (blue) and hold the MOSFETs off (purple).



Ex. 1010, Fig. 10.

D. The Challenged Claims are Obvious over Pan in view of TI UCD3138 (or, in the alternative, TI UCD3040) and AAPA

148. It is my opinion that Pan (Ex. 1011) combined with TI UCD3138 (Ex. 1006) (or, alternatively, TI UCD3040 (Ex. 1018)) and further combined with the AAPA renders obvious claims 1, 22, and 31-35 of the '481 Patent.

149. A POSITA would have been motivated to combine Pan with TI UCD3138 or TI UCD3040 because Pan discloses a digital controller that includes a

control unit, a digital PWM (DPWM), and clock management. Ex. 1011, 716, Fig. 11. TI UCD3138 and TI UCD3040 are both digital controllers that have all of the features of the digital controller in Pan, including DPWM.

150. The TI UCD3138 Datasheet also states that its “Topology support has been optimized for . . . LLC half bridge and full bridge” converters. Ex. 1006, 7. TI UCD3040 states that it supports “half-bridge, phase-shifted full bridge, active clamp, and resonant LLC” converters. Ex. 1018, 2. Pan discloses a series resonant converter that can be either half bridge or full bridge. Ex. 1011, 712 (“Series resonant DC/DC converters with constant switching frequency control are utilized. The main stage on the primary side of the transformer could be either half bridge or full bridge with L-C series resonant tank.”) This presents a POSITA with further motivation to combine.

151. A POSITA would also have been motivated to combine Pan with the AAPA for purposes of zero current and zero voltage switching because both are related to resonant converters, and Pan contemplates zero current and zero voltage switching, which the AAPA explicitly teaches. A POSITA would therefore have understood and expected that the AAPA’s teachings, which were generally known in the prior art, would apply to Pan’s resonant converter, and would have looked to the AAPA for additional details related to zero current and zero voltage switching. TI UCD3138 also relates to series resonant converters and contemplates zero current

and zero voltage switching by referencing “LLC and phase shifted full bridge mode switching.” Ex. 1006, 7. Similarly, TI UCD3040 discusses resonant LLC converters and contemplates zero current and zero voltage switching. Ex. 1018, 2.

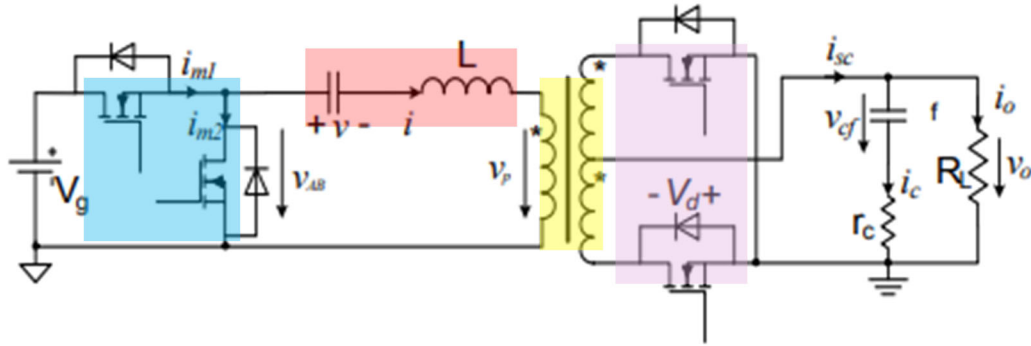
1. Claim 1

- a. “A method of synchronously operating a power converter in a series of converter operating cycles the converter having at least one primary switch to drive a resonant power train and at least one secondary switch, the resonant power train including a transformer and having a characteristic resonant frequency and period, the method comprising:”**

152. Pan discloses this limitation. Pan teaches a method of synchronously operating a half-bridge power converter, where the converter has at least one primary switch that drives a resonant circuit, at least one secondary switch, and a transformer. Ex. 1011, 712 (“The main switches (M_1 & M_2) operate in complementary mode against input voltage variations. The rectifier switches (S_1 & S_2) operate in PWM control mode against load variations.”); *Id.* (“Series resonant DC/DC converters with constant switching frequency control are utilized. The main stage on the primary side of the transformer could be either half bridge or full bridge with L-C series resonant tank.”).

153. Figure 1 of Pan (below) shows a half-bridge converter having primary MOSFET switches M_1 & M_2 (in blue), a resonant circuit on the primary side

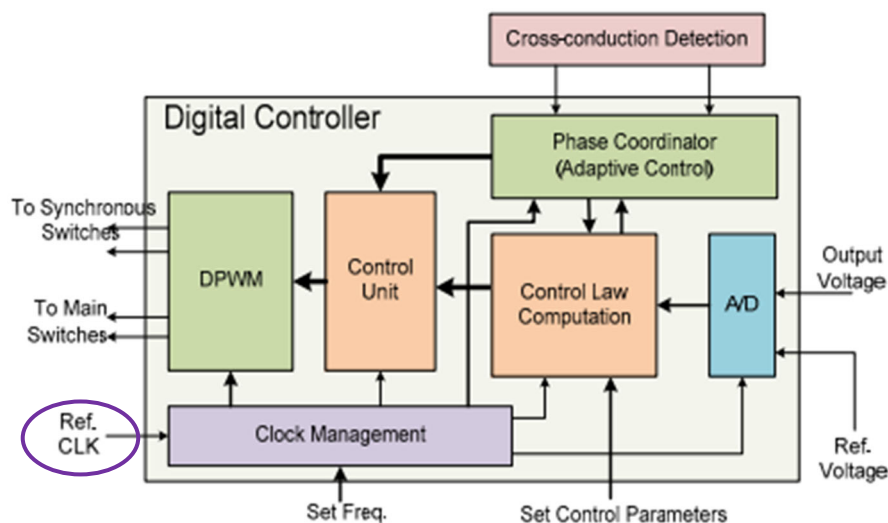
consisting of inductor L and capacitor C (in red), secondary MOSFET switches S_1 & S_2 (shown in pink), and a transformer (in yellow).



Ex. 1011, Figure 1. The resonant circuit has a resonant frequency and period.

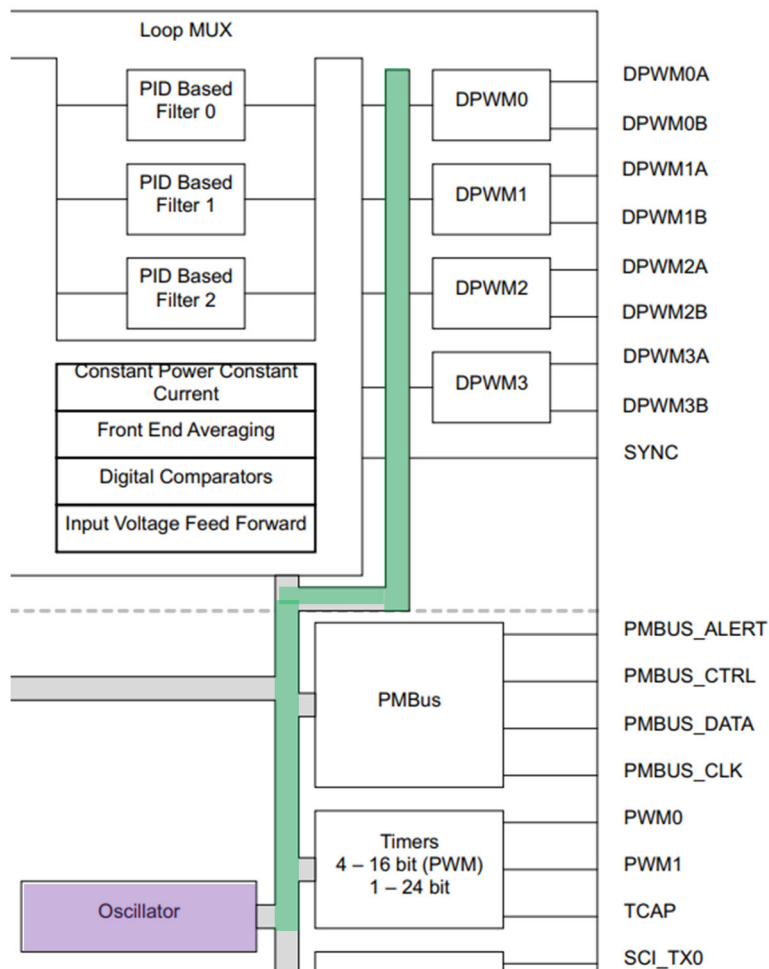
b. “providing an oscillator for generating clock signals at an oscillator frequency;”

154. Pan in combination with the TI UCD3138 (“Pan-TI UCD3138”) (or, alternatively, Pan in combination with TI UCD3040, “Pan-TI UCD3040”) renders this limitation obvious. Figure 11 of Pan (below) discloses an oscillator (Ref. CLK, circled in purple) for generating clock signals at an oscillator frequency.



Ex. 1011, Figure 11.

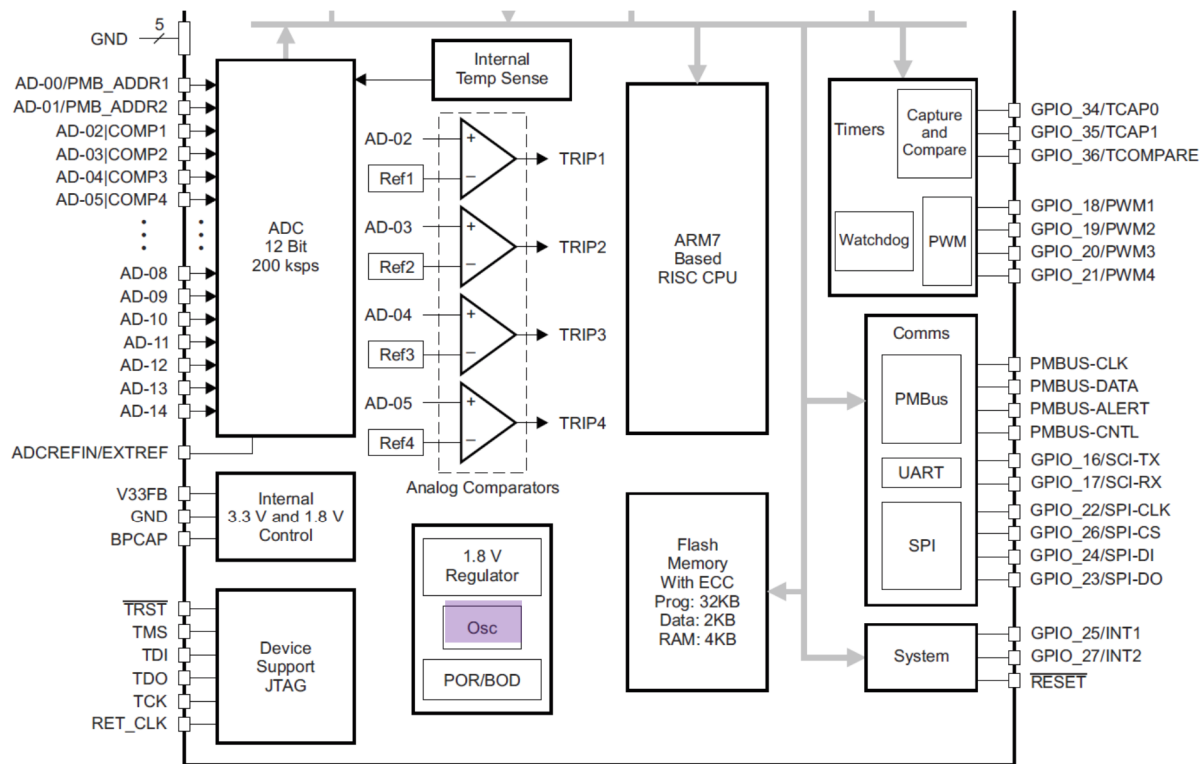
155. TI UCD3138 also discloses an oscillator with an oscillator frequency that generates clock signals. Ex. 1006, 9 (Fig. 2.4), 17. Figure 2.4 of TI UCD3138 (below) shows an Oscillator (in purple) that generates several clock signals (in green).



Ex. 1006, 9. The oscillator in TI UCD3138 has an internal oscillator frequency $f_{(PCLK)}$, having a typical frequency of 250 MHz. *Id.*, 17.

156. TI UCD3138 also teaches that its oscillator generates clock signals. *Id.*, 30, 4.4.1.4 High Resolution PWM (“This is achieved by providing the DPWM mechanism with 16 phase shifted clock signals of 250 MHz each.”).

157. TI UCD3040 also teaches an oscillator with an oscillator frequency that generates clock signals. Ex. 1018, 4, 18. The figure below shows an oscillator OSC (in purple).

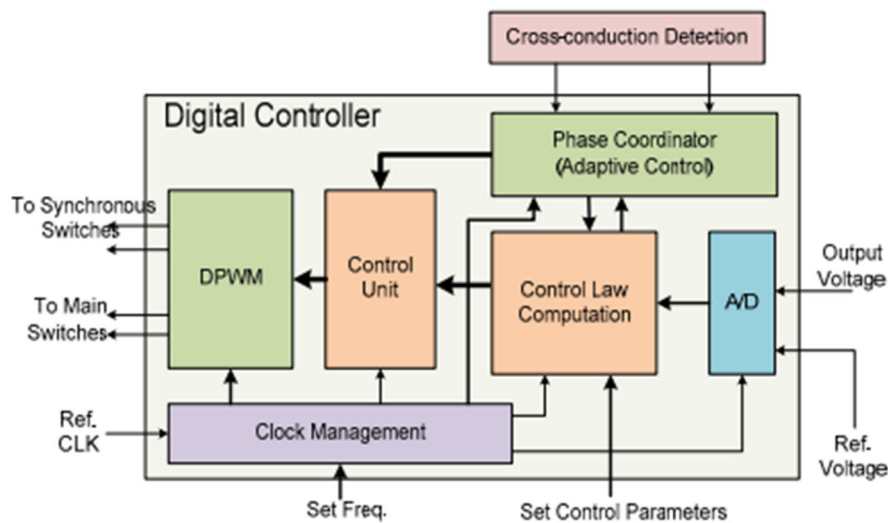


Ex. 1018, 4. The oscillator in TI UCD3040 has an internal oscillator frequency $f_{(PCLK)}$ of 250 MHz. *Id.*, 18.

- c. “generating timing control signals for each of a plurality of events based upon the clock signals in a (A)

standard converter operating cycle, having a standard operating period and frequency, to:”

158. Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. Figure 11 of Pan (copied below) shows use of timing control signals (DPWM) to control both the primary switches (Main Switches) and the secondary switches (Synchronous Switches).



Ex. 1011, Figure 11.

159. TI UCD3138 and TI UCD3040 both teach that each DPWM can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

160. A POSITA would understand that in Pan the converter operating cycle would have a standard operating period and frequency, which is the resonant period and frequency of the resonant converter, because Pan discusses achieving ZVS, and this requires a resonant frequency.

- d. “(i) turn the at least one primary switch ON and OFF at times when essentially zero voltage is impressed across the respective at least one primary switch and essentially zero resonant current is flowing in the respective at least one primary switch; and”**

161. Pan in combination with the AAPA (“Pan-AAPA”) renders this limitation obvious. Pan discusses zero voltage switching on the primary switches. Ex. 1011, 712 (“At t_3 , M_2 is turned on to achieve zero voltage switching (ZVS)”); *Id.*, 713 (“At t_8 , M_1 is turned on to achieve zero voltage switching (ZVS)”).

162. The AAPA discloses that zero voltage and zero current switching can be used to turn the primary switches on and off. For example, the AAPA discloses turning on (closing) a primary switch (S1) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32.

163. The AAPA also discloses turning off (opening) a primary switch S1 “when the sinusoidal current flow completes half-cycle, and the current I_{pri} returns substantially to zero” and “the voltages across switches S2-120 and S4-140 decline toward zero.” *Id.*, 1:36-43.

- e. “(ii) turn the at least one secondary switch ON and OFF at times when essentially zero current is flowing in the respective at least one secondary switch and**

essentially zero voltage is impressed across the respective at least one secondary switch; and”

164. Pan-AAPA renders this limitation obvious. Pan discusses switching of the secondary switches when the resonant current is near zero. Ex. 1011, 713 (“At t_5 , the resonant current i is going across zero. Current through the body diode of S_2 is diminished to zero.”); *Id.* (“At t_0 , the resonant current i goes across zero. Current through the body diode of S_1 is diminished to zero.”).

165. The AAPA also discloses that zero voltage and zero current switching can be used to turn the secondary switches on and off. For example, the AAPA discloses that “the VTM may include secondary switches turned on and off essentially at times of zero voltage to rectify power from the transformer. The VTM may include secondary switches on and off essentially at times of zero current to rectify power from the transformer.” Ex. 1009, 9:25-29.

166. The AAPA also discloses turning on (closing) a secondary switch (S_3) “when the voltages across switches S_1 110 and S_3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32.

167. The AAPA further discloses that “the voltage across one or more of the switches may be monitored to establish the timing of a zero-voltage switching or zero-current switching event.” *Id.* 1:66-2:3.

168. The AAPA further discloses that “the timing architecture of the SAC topology supports . . . ZCS and ZVS operation of the secondary switches.” Ex. 1009, 18:49-56.

f. “wherein the oscillator frequency is preset, and”

169. Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. Figure 11 of Pan shows that the frequency of the oscillator (Ref. CLK) can be preset to a set frequency (Set Freq). Ex. 1011, Figure 11.

170. In addition, the oscillator in TI UCD3138 has an internal oscillator frequency $f_{(PCLK)}$ that is preset, having a typical frequency of 250 MHz. Ex. 1006, 17.

171. The oscillator in TI UCD3040 has a preset oscillator frequency $f_{(PCLK)}$ of 250 MHz. Ex. 1018, 18.

g. “the timing of the timing control signals for one or more selected events may be set independently of other timing control signals and events.”

172. Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. TI UCD3138 and TI UCD3040 both disclose that timing of the timing control signals are independent.

4.4.1.2 DPWM Module

The DPWM module represents one complete PWM channel with 2 independent outputs, A and B. Multiple DPWM modules within the UCD3138 system can be configured to support all key power topologies. DPWM modules can be used as independent PWM outputs, each controlling one power supply output voltage rail. It can also be used as a synchronized PWM—with user selectable phase shift between the PWM channels to control power supply outputs with multiphase or interleaved PWM configurations.

Ex. 1006, 27.

DPWM Module

Programmers' Reference Manual: UCD30xx Fusion Digital Power Peripherals Programmer's Manual

The DPWM module represents one complete DPWM channel with two independent outputs, A and B. Multiple DPWM modules within the UCD30xx system can be configured to support all key power topologies. DPWM modules can be used as independent DPWM outputs, each controlling one power-supply output-voltage rail. A DPWM module can also be used as a synchronized DPWM, with user-selectable phase shift between the DPWM channels, in order to control power-supply outputs with multiphase or interleaved DPWM configurations.

Ex. 1018, 30.

173. TI UCD3138 and TI UCD3040 both further disclose that the timing of the timing control signals for various events are independent of each other, by indicating that each DPWM can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

DPWM Events

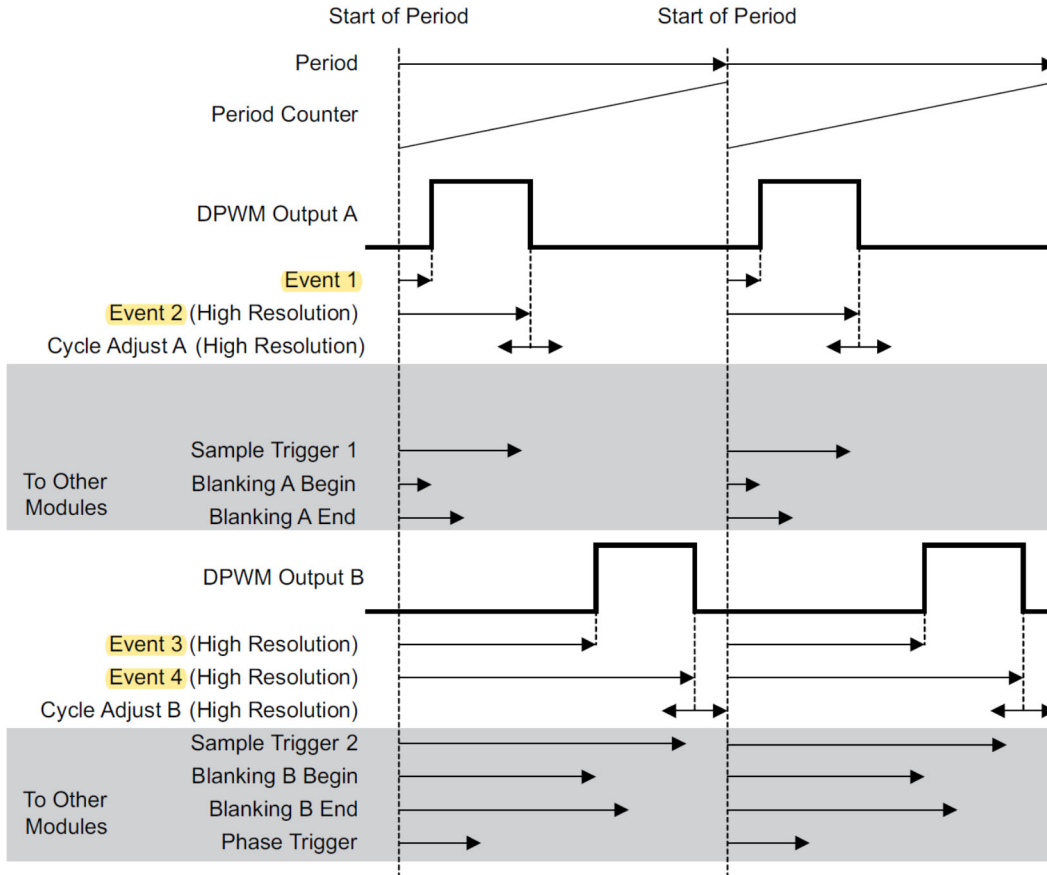
Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

174. As can be seen in the Multi-Mode Open Loop figure (below) in TI UCD3138, the timing of the timing control signals are set independently because each rising edge and falling edge of DPWM A and DPWM B are independent events (Event 1, Event 2, Event 3, and Event 4) and are not dependent on the timing of other events.

Multi Mode Open Loop



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
 DPWM A Falling Edge = Event 2 + Cycle Adjust A
 DPWM B Rising Edge = Event 3
 DPWM B Falling Edge = Event 4 + Cycle Adjust B
 Phase Trigger = Phase Trigger Register value

Ex. 1006, 29.

2. Claim 22

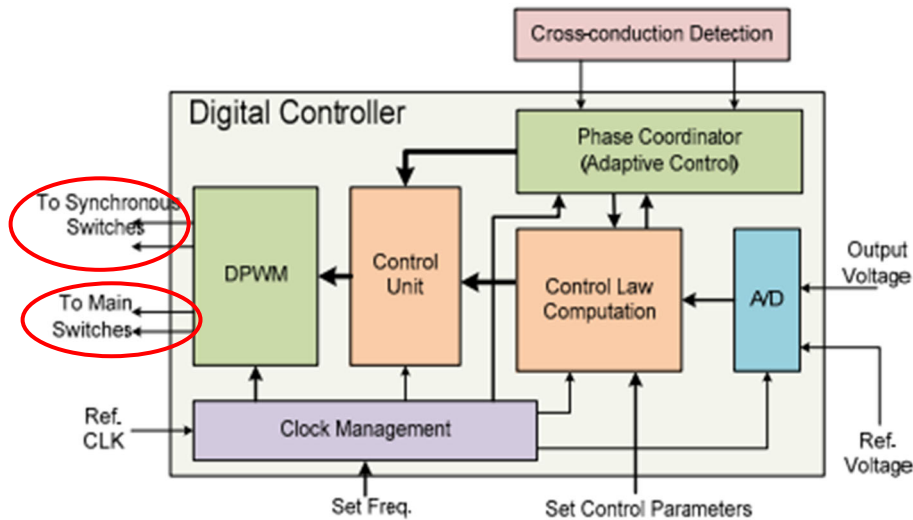
a. “The method of claim 1 further comprising”

175. See §V1.D.1.

b. “providing a gate drive circuit for operating selected switches in the converter and generating timing control signals based upon the clock signals to (a) initiate a transition of the selected switches from ON to OFF or

OFF to ON, (b) hold the selected switches ON, and (c) hold the selected switches OFF.”

176. Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. Figure 11 of Pan (below) shows use of a gate drive circuit (Control Unit) to generate timing control signals (DPWM) to control the primary (Main) and secondary (Synchronous) switches.



Ex. 1011, Figure 11.

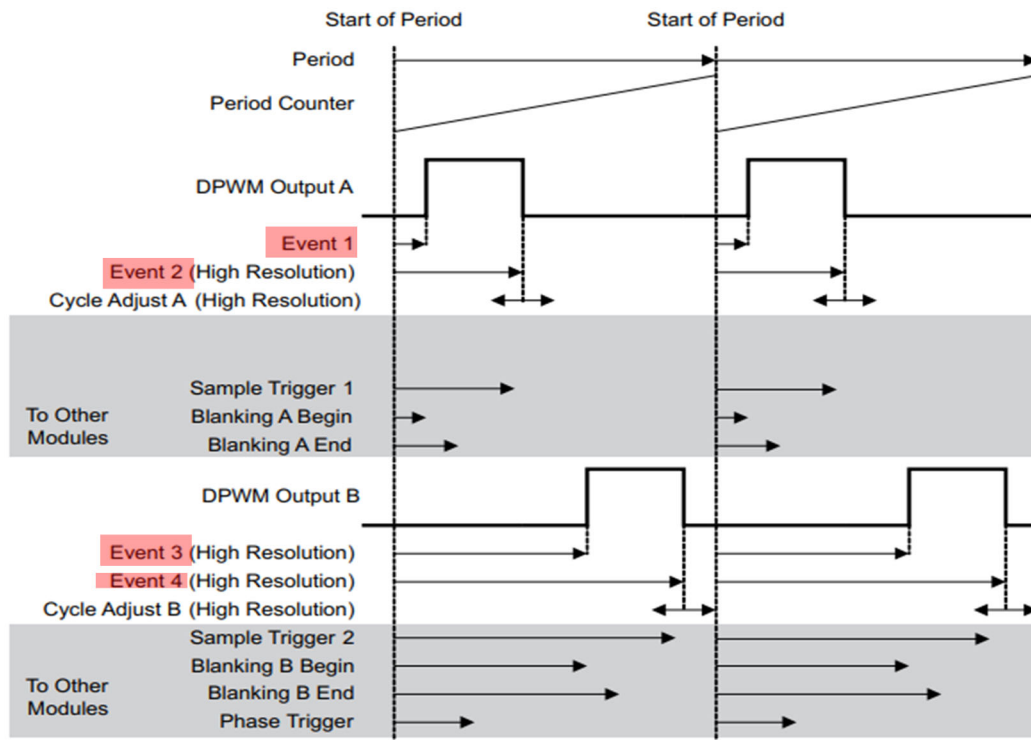
177. TI UCD3138 and TI UCD3040 both disclose that each timing control signal DPWM can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28; *Id.*, 29 (figure below showing timing signals for different events).



Ex. 1006, 29.

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

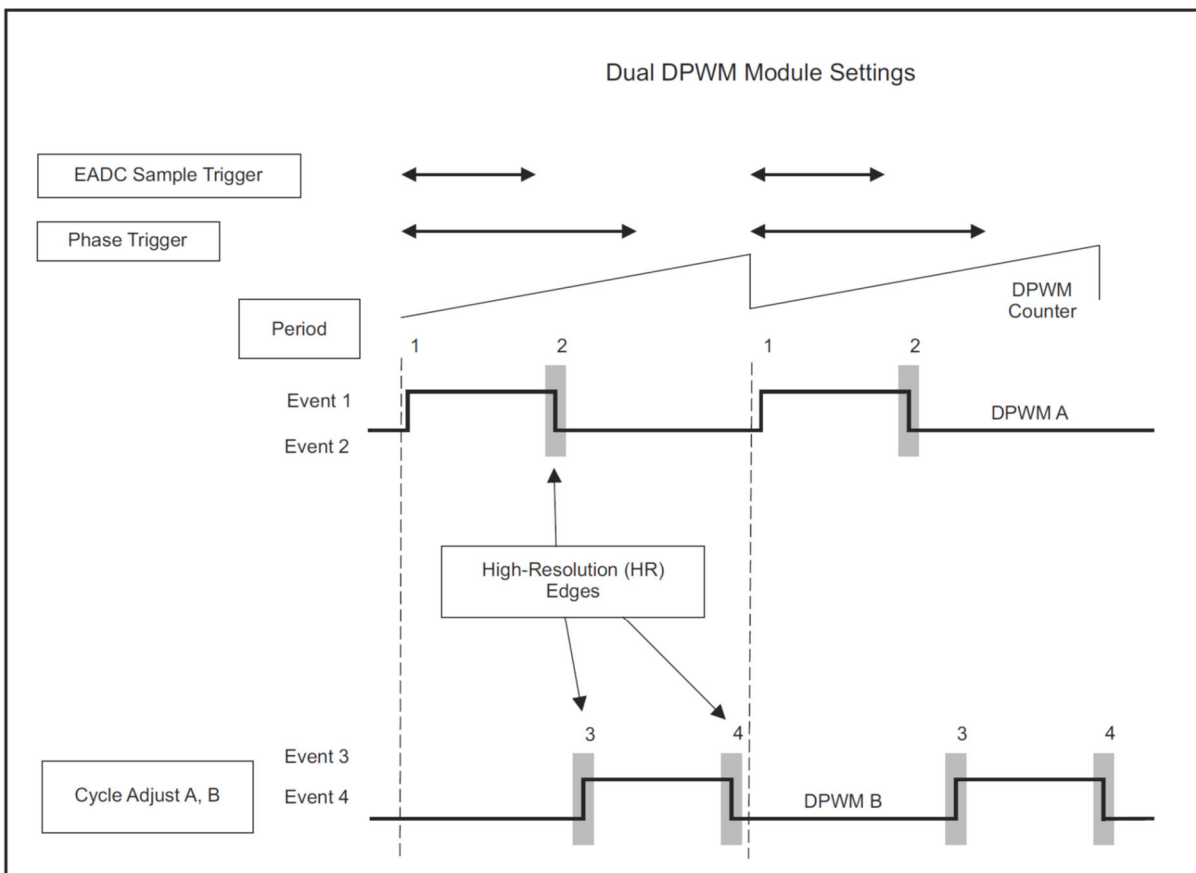


Figure 7. DPWM Events

Ex. 1018, 32 (showing timing signals for different events).

3. Claim 31

- a. “The method of claim 1 wherein the generating timing control signals based upon the clock signals further comprises:”

178. See § V1.D.1.

- b. “counting the clock signals from the oscillator;”

179. Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. TI UCD3138 and TIUCD3040 both disclose that the DPWM’s control of the various timing events involves counting the clock signals from the oscillator.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

c. “setting a count threshold for each event;”

180. Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. TI UCD3138 and TI UCD3040 both disclose that the DPWM sets a count threshold for each event.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

- d. **“generating the respective timing control signal for each event as the counting matches the respective count threshold.”**

181. Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. TI UCD3138 and TI UCD3040 both teach that the DPWM generates timing control signals for each event when the counting matches the count threshold.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28. *See also id.*, 32, 4.5 DPWM Modes of Operation (“... The DPWM logic causes transitions in many digital signals when the period counter hits the target value for that signal.”).

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

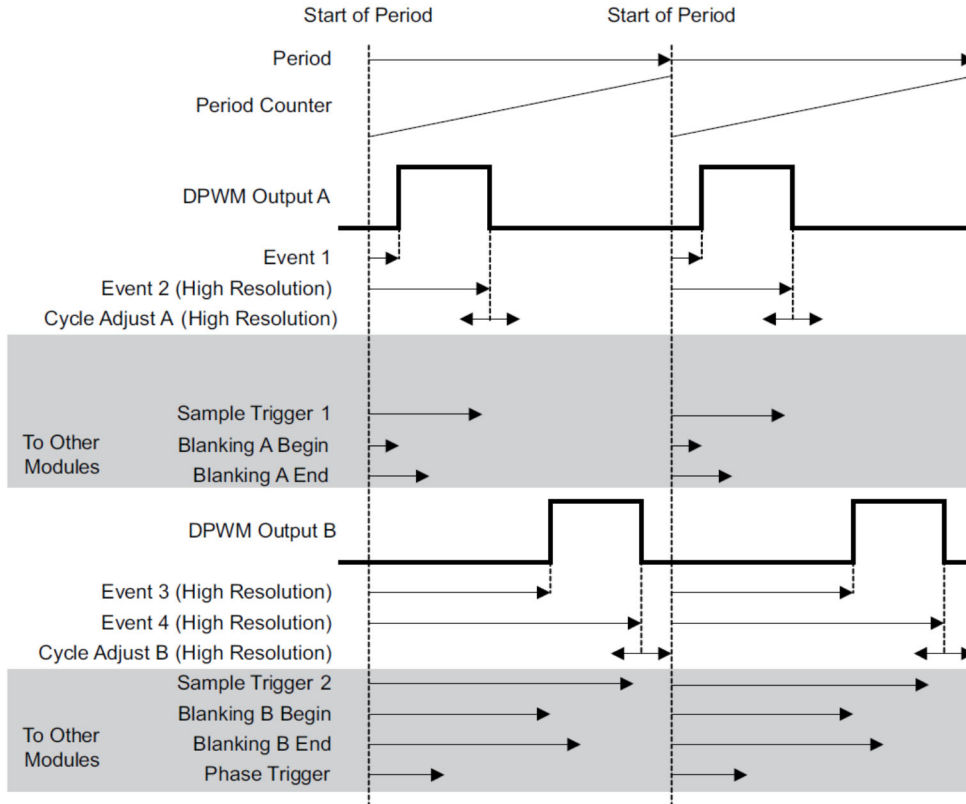
Ex. 1018, 31.

4. Claim 32

- a. “The method of claim 31 wherein the oscillator and timing events are open-loop with respect to the power train.”**

182. Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. *See* § VI.D.3. TI UCD3138 shows a Multi-Mode Open Loop figure (below), stating that the DPWM is controlled entirely by its own registers and not by the filter output.

Multi Mode Open Loop



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
 DPWM A Falling Edge = Event 2 + Cycle Adjust A
 DPWM B Rising Edge = Event 3
 DPWM B Falling Edge = Event 4 + Cycle Adjust B
 Phase Trigger = Phase Trigger Register value

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

The drawing above is for multi-mode, open loop. Open loop means that the DPWM is controlled entirely by its own registers, not by the filter output. In other words, the power supply control loop is not closed.

Ex. 1006, 29.

183. TI UCD3140 also discloses an open-loop mode (below).

Ex. 1006, 26.

185. TI UCD3040 also discloses this limitation of adjusting timing events with feedback provided by the compensator.

PERIPHERALS

Fusion Digital Power Peripherals

At the core of the UCD30xx controller are its four Fusion Digital Power peripherals (FDPP). Each FDPP can be configured to drive from one to eight DPWM outputs. Each FDPP consists of a differential input error ADC (EADC), a hardware-accelerated digital three-pole/three-zero (3p/3z) compensator, and a digital PWM module.

Ex. 1018, 25.

6. Claim 34

- a. **“The method of claim 33 wherein the measurements and adjustments are performed during the manufacturing process.”**

186. Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. *See* § VI.D.4. TI UCD3138 and TI UCD3040 both teach use of firmware data for certain measurements. Firmware is set during the manufacturing process. Ex. 1006, 22, 4.2 Memory (“Within the UCD31xx architecture, there is a 1024x32-bit Boot ROM that contains the initial firmware startup routines for PMBUS communication and non-volatile (FLASH) memory download. This boot ROM is executed after power-up-reset checks if there is a valid FLASH program written.”); Ex. 1018, 20, Memory (“Within the UCD30xx architecture, there is a 1024x32-bit Boot ROM that contains the initial firmware startup routines for PMBUS communication and non-volatile (flash) memory download. This boot ROM is executed after power-up-reset checks if there is a valid flash program

written.”); Ex. 1006, 55, 4.23 Temperature Reference (“The temperature reference register (TEMPREF) provides the ADC12 count when ADC12 measures the internal temperature sensor (channel 14) during the factory trim and calibration. This information can be used by different periodic temperature compensation routines implemented in the firmware. But it should not be overwritten by firmware, otherwise this factory written value will be lost.”).

7. Claim 35

- a. **“The method of claim 33 wherein the measurements and adjustments are performed during operation as part of a closed-loop feedback system.”**

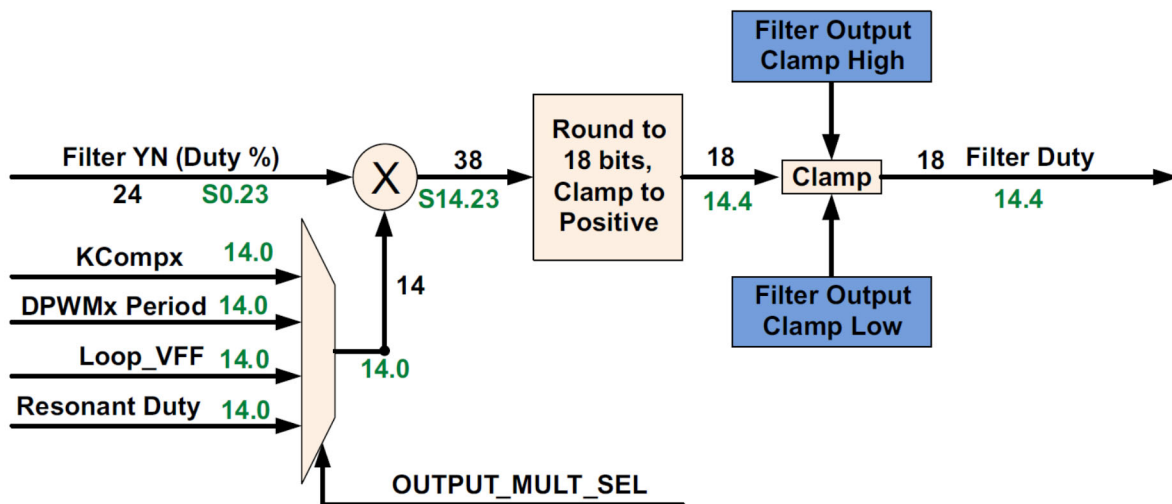
187. Pan-TI UCD3138 (or, alternatively, Pan-TI UCD3040) renders this limitation obvious. *See* § VI.D.4. Figure 11 of Pan shows that the measurements and adjustments are performed during operation as part of a closed-loop feedback system. The “Output Voltage” is measured and input into the A/D (Analog to Digital Converter) and is used to adjust the DPWM output signals to the primary and secondary switches. This closed-loop control is used to maintain a DC-DC Converter Output Voltage relative to the “Ref Voltage.” Ex. 1011, Fig. 11.

188. TI UCD3138 also discloses that the measurements and adjustments are performed during operation of the device as part of a closed-loop feedback system, where the Filter provides the feedback.

These can be connected in many different combinations, with multiple filters and DPWMs. They are capable of supporting functions like input voltage feed forward, current mode control, and constant current/constant power, etc.. The simplest configuration is shown in the following figure:



Ex. 1006, 26.

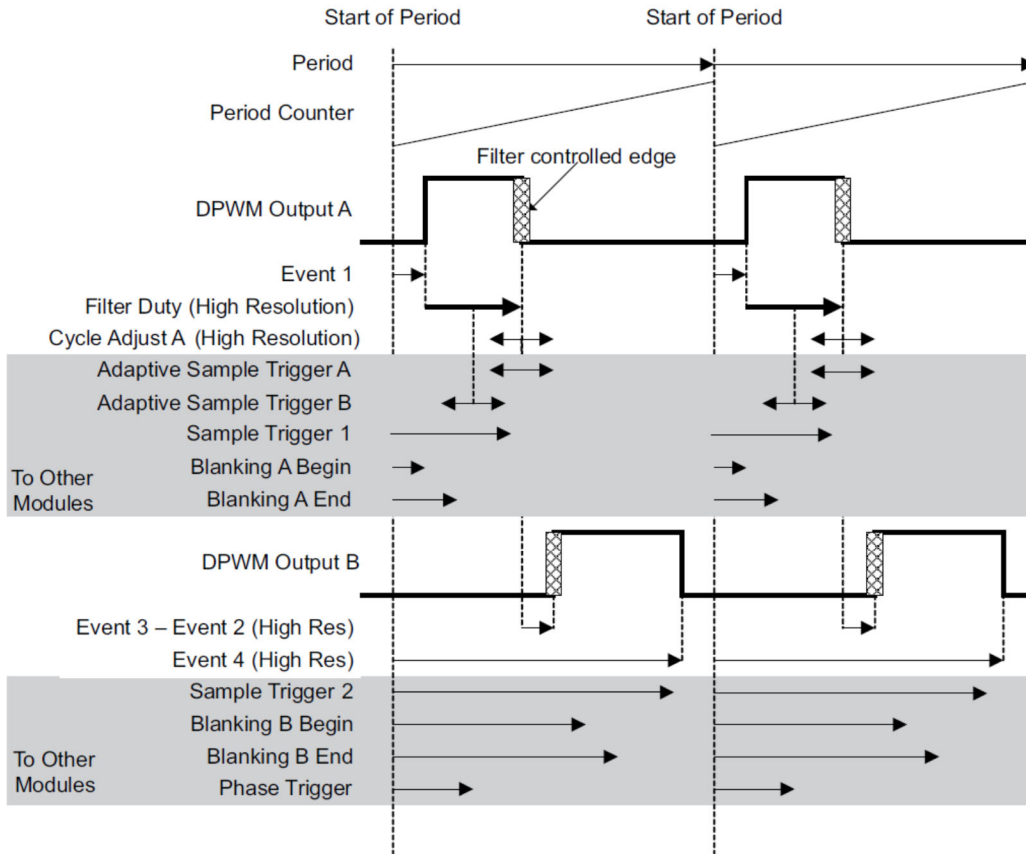


This permits the filter output to be multiplied by a variety of correction factors to match the DPWM Period, to provide for Voltage Feed Forward, or for other purposes. After this, there is another clamp. For resonant mode, the filter can be used to generate both period and duty cycle.

Ex. 1006, 46.

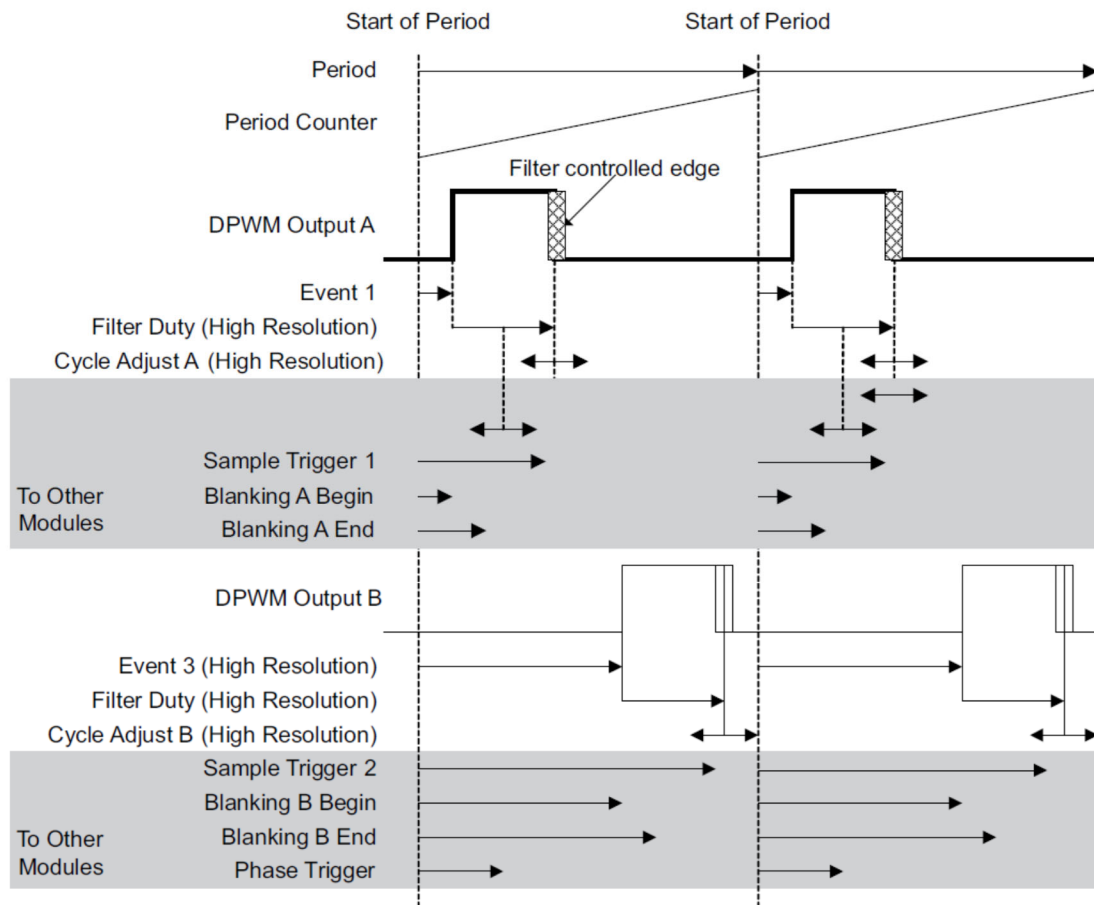
189. TI UCD3138 also has several figures showing closed loop operation.

Normal Mode Closed Loop

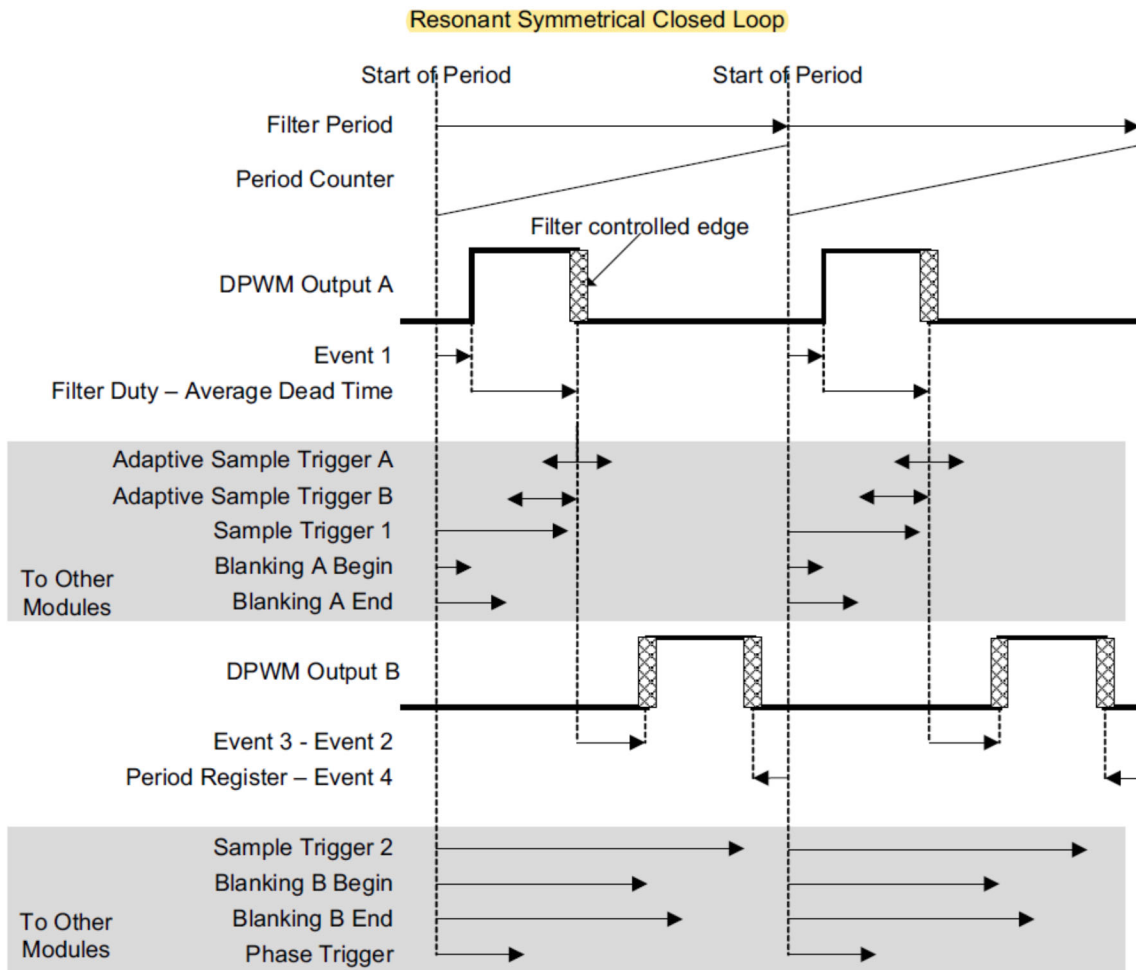


Id., 32.

Multi Mode Closed Loop



Id., 34.



Id., 36. See also, *Id.*, 37, 39.

190. TI UCD3040 also teaches that the measurements and adjustments are performed during operation of the device as part of a closed-loop feedback system, where the compensator provides the feedback.

PERIPHERALS

Fusion Digital Power Peripherals

At the core of the UCD30xx controller are its four Fusion Digital Power peripherals (FDPP). Each FDPP can be configured to drive from one to eight DPWM outputs. Each FDPP consists of a differential input error ADC (EADC), a hardware-accelerated digital three-pole/three-zero (3p/3z) compensator, and a digital PWM module.

Ex. 1018, 25.

191. TI UCD3140 also has several figures showing closed loop operation.

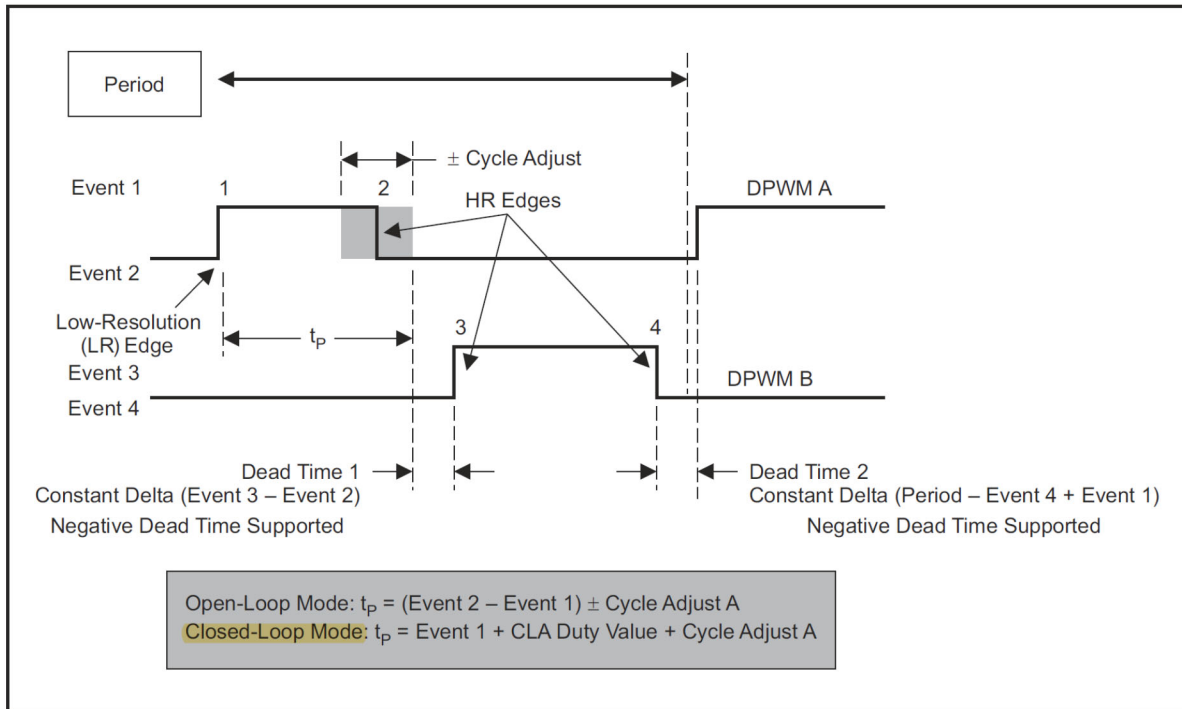


Figure 8. Normal Mode (Duty-Ratio Control) – DPWM Timing Diagram

Ex. 1018, 34.

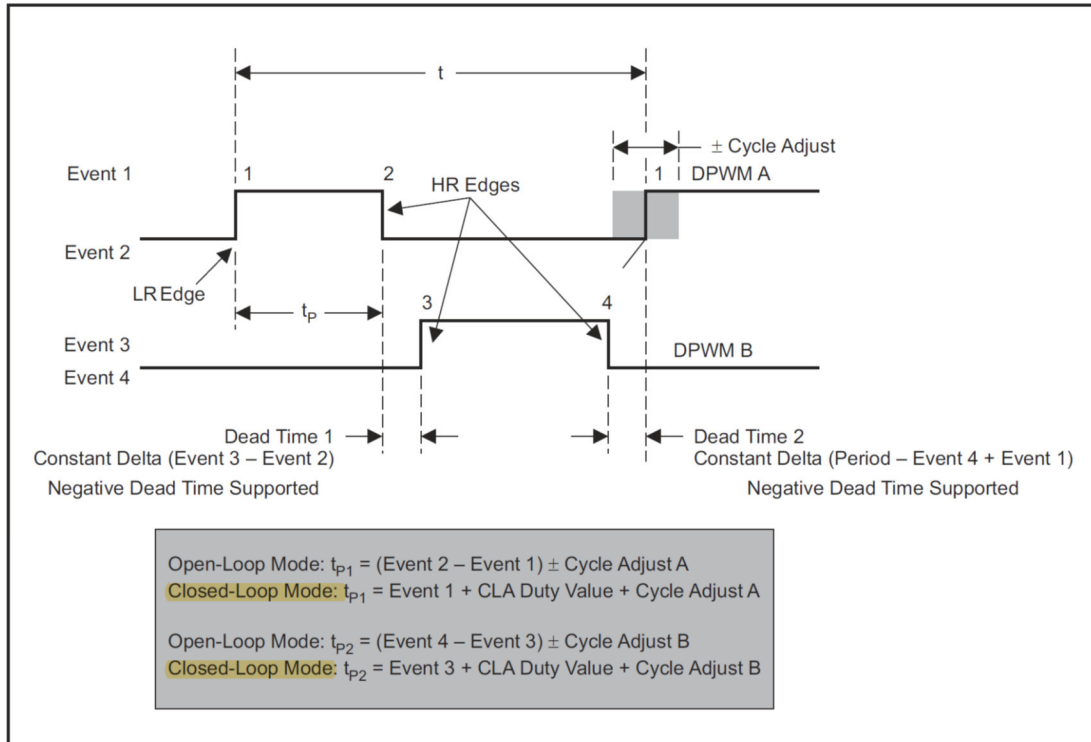


Figure 10. Resonance Mode (Constant-On Duty Ratio With Variable Period) – DPWM Timing Diagram

Ex. 1018, 36.

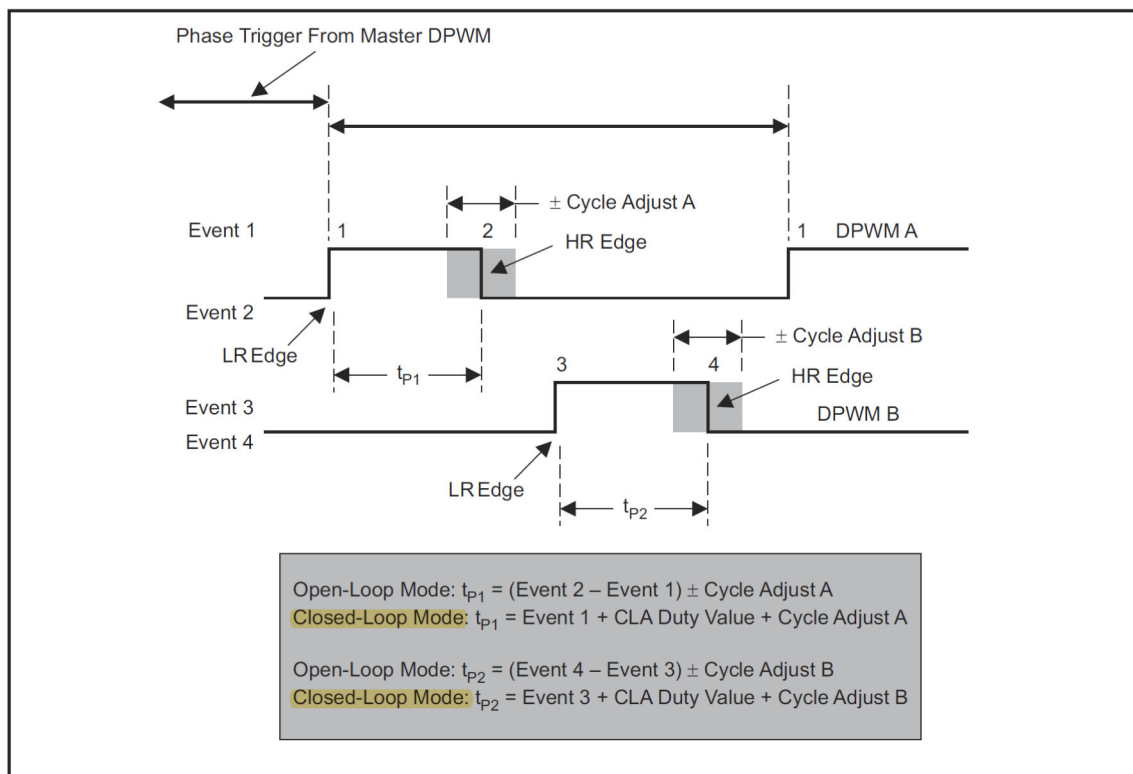


Figure 11. Multi-Output Mode – DPWM Timing Diagram

Ex. 1018, 37.

E. The Challenged Claims are Obvious over Peng in view of TI UCD3138 (or, in the alternative, TI UCD3040) and AAPA

192. It is my opinion that Peng (Ex. 1011) combined with TI UCD3138 (Ex. 1006) (or, alternatively, TI UCD3040 (Ex. 1018)) and further combined with the AAPA renders obvious claims 1, 22, and 31-35 of the '481 Patent.

193. A POSITA would have been motivated to combine Peng with TI UCD3138 or TI UCD3040 because Peng explicitly states that “[m]any suitable computing stations and circuits may serve as the switching controller 160, including . . . application-specific digital/analog integrated circuits.”. Ex. 1012, 14:54-58. TI

UCD3138 and TI UCD3040 are both digital controllers as described in Peng. TI UCD3138 states that its “Topology support has been optimized for . . . LLC half bridge and full bridge” converters. Ex. 1006, 7. TI UCD3040 states that it supports “half-bridge, phase-shifted full bridge, active clamp, and resonant LLC” converters. Ex. 1018, 2. Peng discloses a series resonant LCC half-bridge converter. Ex. 1012, Fig. 6, 16:10-15. This presents a POSITA with further motivation to combine.

194. A POSITA would also have been motivated to combine Peng with the AAPA for purposes of zero current and zero voltage switching because both are related to resonant converters, and Peng contemplates zero current and zero voltage switching (Ex. 1012, 16:23-29), which the AAPA explicitly teaches. A POSITA would therefore have understood and expected that the AAPA’s teachings, which were generally known in the prior art, would apply to Peng’s resonant converter, and would have looked to the AAPA for additional details related to zero current and zero voltage switching. TI UCD3138 also relates to resonant converters and contemplates zero current and zero voltage switching. Ex. 1006, 7. Similarly, TI UCD3040 discusses resonant LLC converters and contemplates zero current and zero voltage switching. Ex. 1018, 2.

1. Claim 1

- a. “A method of synchronously operating a power converter in a series of converter operating cycles the converter having at least one primary switch to drive a resonant power train and at least one secondary**

switch, the resonant power train including a transformer and having a characteristic resonant frequency and period, the method comprising:”

195. Peng discloses this limitation. Peng teaches a method of synchronously operating a half-bridge power converter, where the converter has at least one primary switch that drives a resonant circuit, at least one secondary switch, and a transformer.

Ex. 1012, 15:8-15, 15:28-32, 15:58-63.

196. Figure 6 of Peng (copied below) shows a half-bridge converter having primary MOSFET switches S1 and S2 (in blue), a resonant circuit on the primary side consisting of inductor L_{dc} and capacitors C_{r1} and C_{r2} , secondary IGBT switches S3 and S4 (shown in pink), and a transformer 104 (in yellow).

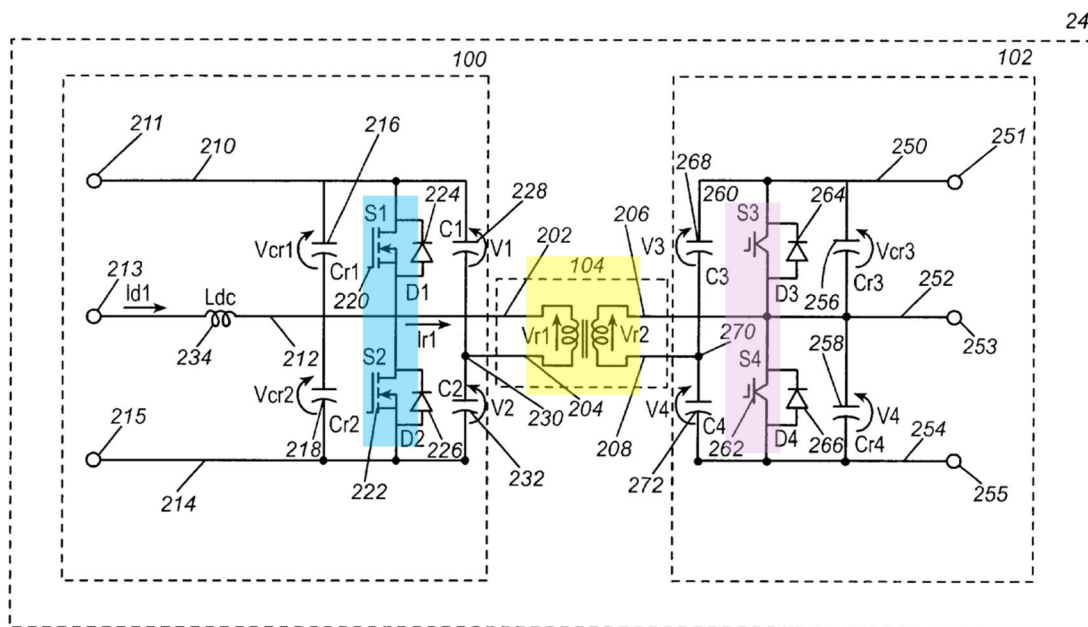


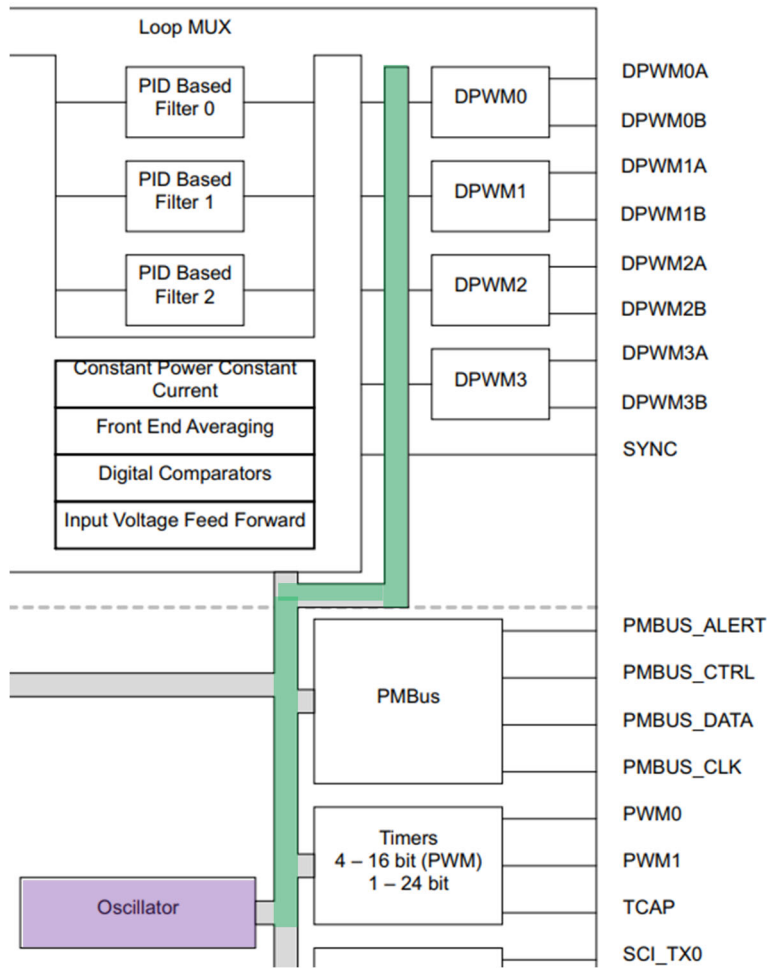
FIG. 6

Ex. 1012, Figure 6. The resonant circuit has a resonant frequency and period.

b. “providing an oscillator for generating clock signals at an oscillator frequency;”

197. Peng in combination with the TI UCD3138 (“Peng-TI UCD3138”) (or, alternatively, Peng in combination with TI UCD3040, “Peng-TI UCD3040”) renders this limitation obvious. Peng states that its switching controller 160 can be implemented using a digital integrated circuit. Ex. 1012, 14:54-58. TI UCD3138 is a digital integrated circuit, and discloses an oscillator with an oscillator frequency that generates clock signals. Ex. 1006, 9 (Fig. 2.4), 17.

198. Figure 2.4 of TI UCD3138 (below) shows an Oscillator (in purple) that generates several clock signals (in green).



Ex. 1006, 9. The oscillator in TI UCD3138 has an internal oscillator frequency $f_{(PCLK)}$, with a typical frequency of 250 MHz. *Id.*, 17.

199. TI UCD3138 also teaches that its oscillator generates clock signals.

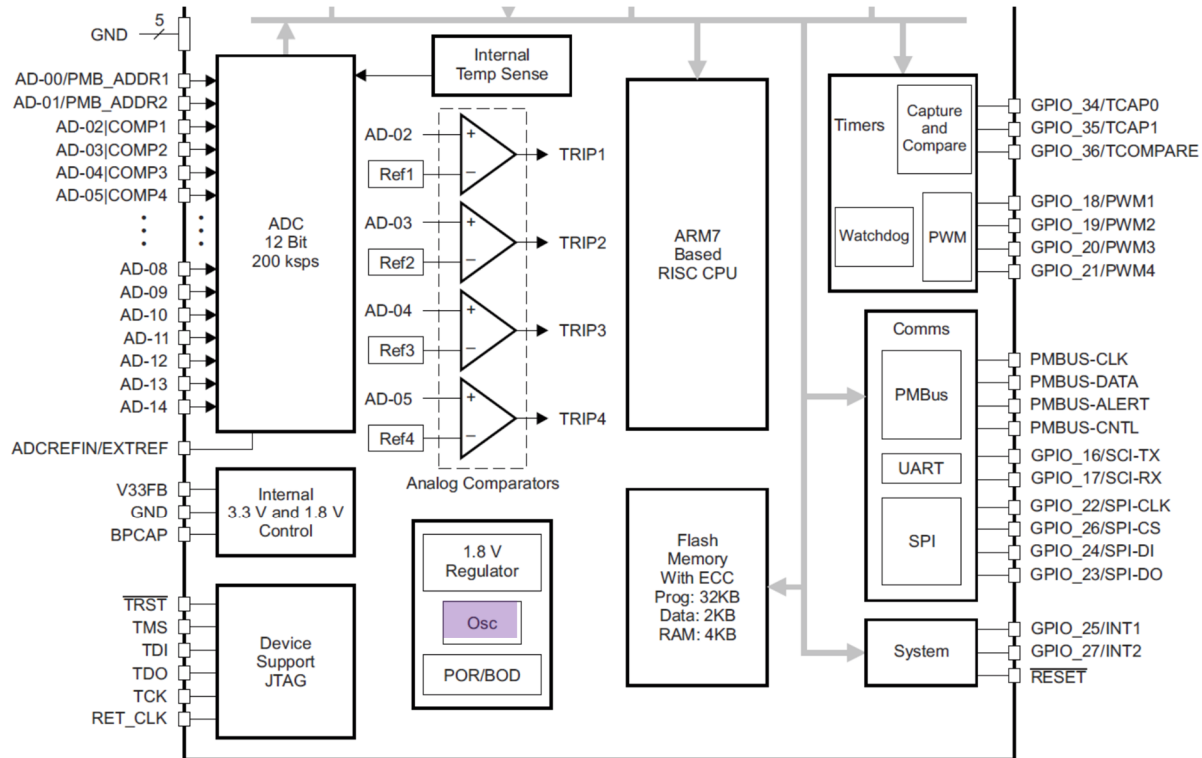
4.4.1.4 High Resolution DPWM

Unlike conventional PWM controllers where the frequency of the clock dictates the maximum resolution of PWM edges, the UCD3138 DPWM can generate waveforms with resolutions as small as 250 ps. This is 16 times the resolution of the clock driving the DPWM module.

This is achieved by providing the DPWM mechanism with 16 phase shifted clock signals of 250 MHz each. The high resolution section of DPWM can be enabled or disabled, also the resolution can be defined in several steps between 4ns to 250ps. This is done by setting the values of PWM_HR_MULTI_OUT_EN, HIRES_SCALE and ALL_PHASE_CLK_ENA inside the DPWM Control Register 1. See the Power Peripherals programmer's manual for details.

Id., 30.

200. TI UCD3040 discloses an oscillator with an oscillator frequency that generates clock signals. Ex. 1018, 4, 18. The figure below shows an oscillator OSC (in purple).



Ex. 1018, 4. The oscillator in TI UCD3040 has an internal oscillator frequency $f_{(PCLK)}$ of 250 MHz. *Id.*, 18.

- c. “generating timing control signals for each of a plurality of events based upon the clock signals in a (A) standard converter operating cycle, having a standard operating period and frequency, to:”

201. Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this limitation obvious. Peng teaches use of a switching controller 160 to generate gating signals to control the switching elements. Ex. 1012, 14:37-42 (“The power converter

24 also includes a switching controller 160 for gating the switching elements 118, 120, 148, and 150. The switching controller may 160 may be a circuit to generate a proper gating sequence to achieve soft-switching and output power (or voltage) control.”); Fig. 5. As discussed above, TI UCD3138 and TI UCD3040 are both digital controllers that can be used in Peng’s switching controller 160, and both teach that each DPWM can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

202. A POSITA would understand that in Peng the converter operating cycle would have a standard operating period and frequency, which is the resonant period and frequency of the resonant converter because Peng discusses achieving ZVS and ZCS, and this requires a resonant frequency.

- d. **“(i) turn the at least one primary switch ON and OFF at times when essentially zero voltage is impressed across the respective at least one primary switch and essentially zero resonant current is flowing in the respective at least one primary switch; and”**

203. Peng in combination with the AAPA (“Peng-AAPA”) renders this limitation obvious. Peng discusses zero voltage and zero current switching on the primary switches. Ex. 1012, 16:27-29 (“The switches S1 and S2 are zero-voltage turn-off and zero-current zero-voltage turn-on.”).

204. The AAPA further discloses that zero voltage and zero current switching can be used to turn the primary switches on and off. For example, the AAPA discloses turning on (closing) a primary switch (S1) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32.

205. The AAPA also discloses turning off (opening) a primary switch S1 “when the sinusoidal current flow completes half-cycle, and the current I_{pri} returns substantially to zero” and “the voltages across switches S2-120 and S4-140 decline toward zero.” *Id.*, 1:36-43.

- e. **“(ii) turn the at least one secondary switch ON and OFF at times when essentially zero current is flowing in the respective at least one secondary switch and essentially zero voltage is impressed across the respective at least one secondary switch; and”**

206. Peng-AAPA renders this limitation obvious. Peng discusses achieving soft-switching of its switches, which a POSITA understands is turning devices on and off at zero or nearly zero voltage or current. Ex. 1012,14:37-42.

207. The AAPA also teaches that zero voltage and zero current switching can be used to turn the secondary switches on and off. For example, the AAPA discloses that “the VTM may include secondary switches turned on and off essentially at times of zero voltage to rectify power from the transformer. The VTM

may include secondary switches on and off essentially at times of zero current to rectify power from the transformer.” Ex. 1009, 9:25-29.

208. The AAPA also discloses turning on (closing) a secondary switch (S3) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32.

209. The AAPA further discloses that “the voltage across one or more of the switches may be monitored to establish the timing of a zero-voltage switching or zero-current switching event.” *Id.* 1:66-2:3.

210. The AAPA further discloses that “the timing architecture of the SAC topology supports . . . ZCS and ZVS operation of the secondary switches.” Ex. 1009, 18:49-56.

f. “wherein the oscillator frequency is preset, and”

211. Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this limitation obvious. Peng teaches that the oscillator frequency in the switching controller can be preset to “a single resonant frequency.” Ex. 1012, 26:38-45.

212. The oscillator in TI UCD3138 has an internal oscillator frequency $f_{(PCLK)}$ that is preset, with a typical frequency of 250 MHz. Ex. 1006, 17. The oscillator in TI UCD3040 has a preset oscillator frequency $f_{(PCLK)}$ of 250 MHz. Ex. 1018, 18.

- g. “the timing of the timing control signals for one or more selected events may be set independently of other timing control signals and events.”

213. Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this limitation obvious. TI UCD3138 and TI UCD3040 both disclose that timing of the timing control signals are independent.

4.4.1.2 DPWM Module

The DPWM module represents one complete PWM channel with 2 independent outputs, A and B. Multiple DPWM modules within the UCD3138 system can be configured to support all key power topologies. DPWM modules can be used as independent PWM outputs, each controlling one power supply output voltage rail. It can also be used as a synchronized PWM—with user selectable phase shift between the PWM channels to control power supply outputs with multiphase or interleaved PWM configurations.

Ex. 1006, 27.

DPWM Module

Programmers' Reference Manual: UCD30xx Fusion Digital Power Peripherals Programmer's Manual

The DPWM module represents one complete DPWM channel with two independent outputs, A and B. Multiple DPWM modules within the UCD30xx system can be configured to support all key power topologies. DPWM modules can be used as independent DPWM outputs, each controlling one power-supply output-voltage rail. A DPWM module can also be used as a synchronized DPWM, with user-selectable phase shift between the DPWM channels, in order to control power-supply outputs with multiphase or interleaved DPWM configurations.

Ex. 1018, 30.

214. TI UCD3138 and TI UCD3040 both further disclose that the timing of the timing control signals for various events are independent of each other, by indicating that each DPWM can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

DPWM Events

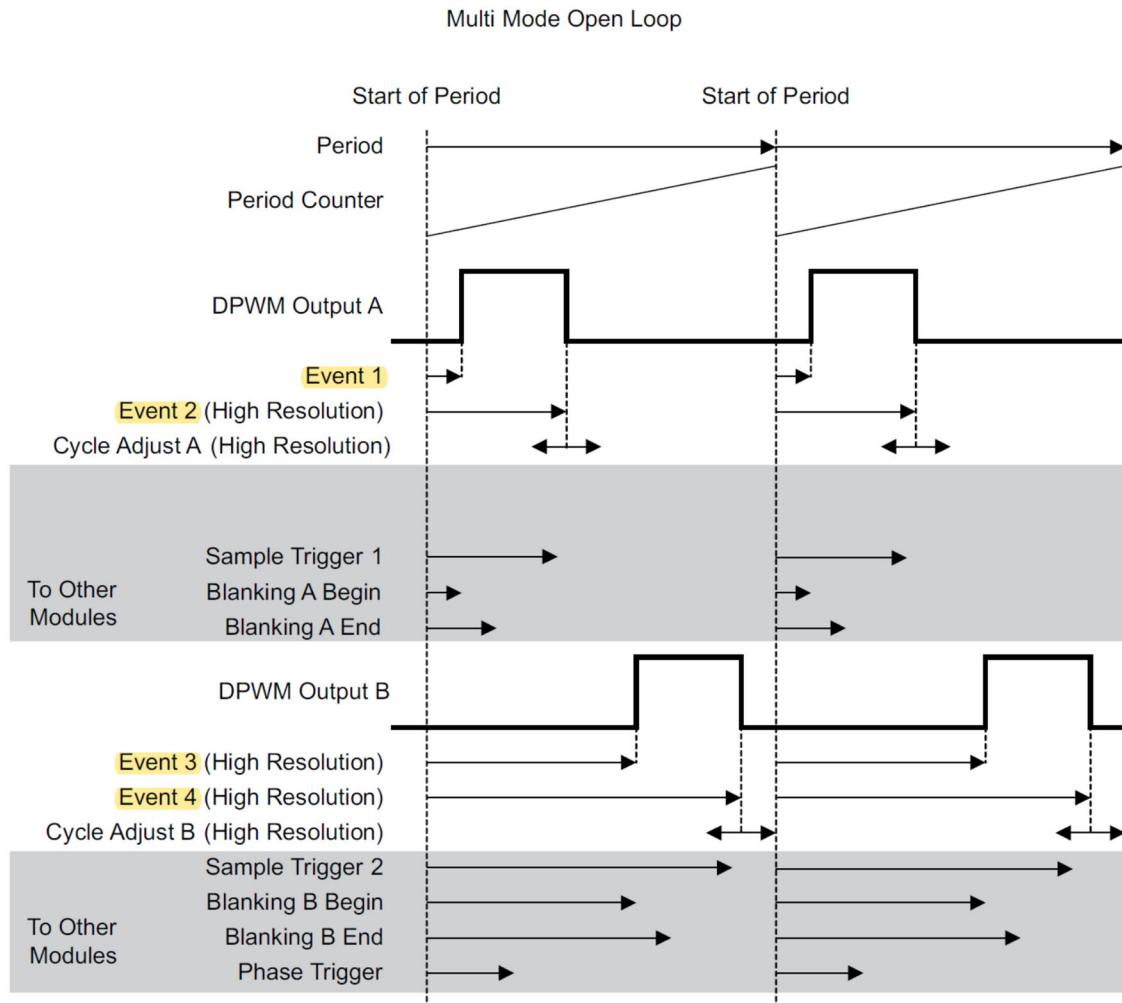
Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

215. As can be seen in the Multi-Mode Open Loop figure (below) in TI UCD3138, the timing of the timing control signals are set independently because each rising edge and falling edge of DPWM A and DPWM B are independent events

(Event 1, Event 2, Event 3, and Event 4) and are not dependent on the timing of other events.



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
 DPWM A Falling Edge = Event 2 + Cycle Adjust A
 DPWM B Rising Edge = Event 3
 DPWM B Falling Edge = Event 4 + Cycle Adjust B
 Phase Trigger = Phase Trigger Register value

Ex. 1006, 29.

2. Claim 22

a. “The method of claim 1 further comprising”

216. See § VI.E.1.

- b. **“providing a gate drive circuit for operating selected switches in the converter and generating timing control signals based upon the clock signals to (a) initiate a transition of the selected switches from ON to OFF or OFF to ON, (b) hold the selected switches ON, and (c) hold the selected switches OFF.”**

217. Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this limitation obvious. Peng discloses that its switching converter 160 is used for “gating the switching elements” and includes “a circuit to generate a proper gating sequence to achieve soft switching and output power (or voltage) control.” Ex. 1012, 14:37-42.

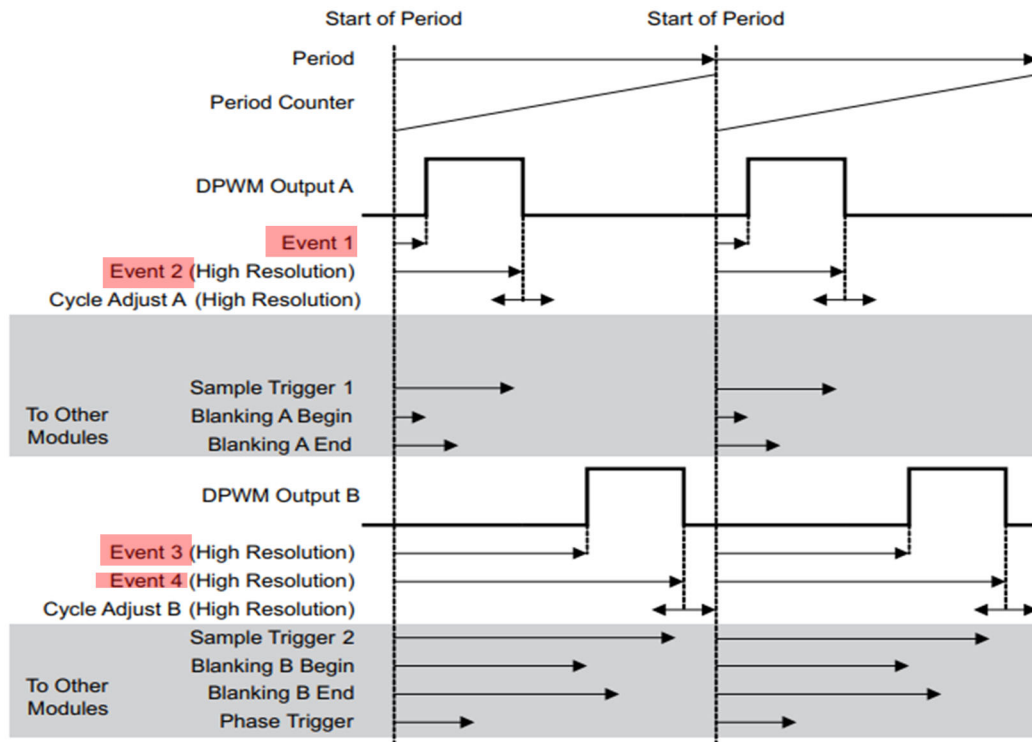
218. TI UCD3138 and TI UCD3040 both disclose that each DPWM timing control signal can control different timing events.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.



Ex. 1006, 29 (showing timing signals for different events).

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

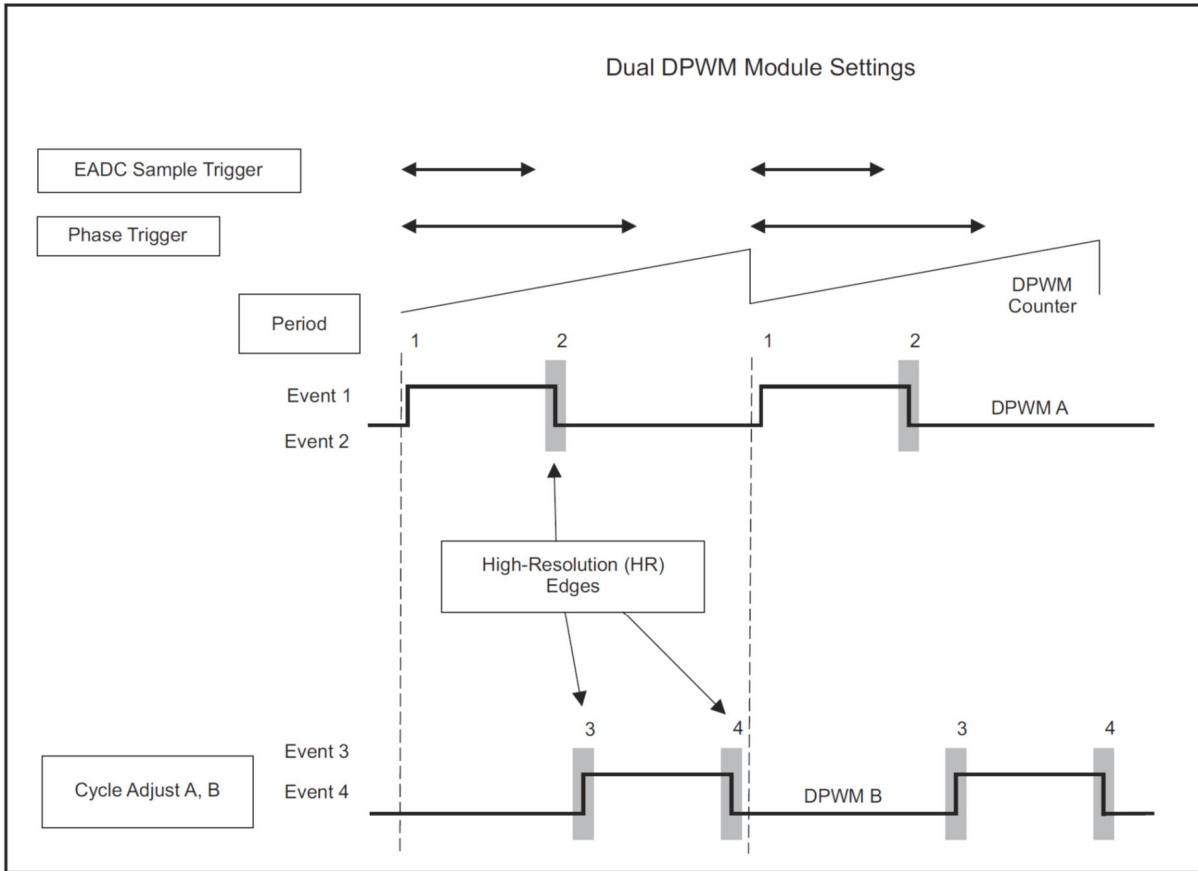


Figure 7. DPWM Events

Ex. 1018, 32 (showing timing signals for different events).

3. Claim 31

- a. **“The method of claim 1 wherein the generating timing control signals based upon the clock signals further comprises:”**

219. *See* § VI.E.1.

- b. **“counting the clock signals from the oscillator;”**

220. Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this limitation obvious. TI UCD3138 and TIUCD3040 both disclose that the DPWM’s

control of the various timing events involves counting the clock signals from the oscillator.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

c. “setting a count threshold for each event;”

221. Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this limitation obvious. TI UCD3138 and TI UCD3040 both disclose that the DPWM sets a count threshold for each event.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28.

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Ex. 1018, 31.

- d. “generating the respective timing control signal for each event as the counting matches the respective count threshold.”

222. Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this limitation obvious. TI UCD3138 and TI UCD3040 both disclose that the DPWM generates timing control signals for each event when the counting matches the count threshold.

4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Ex. 1006, 28. *See also id.*, 32, 4.5 DPWM Modes of Operation (“... The DPWM logic causes transitions in many digital signals when the period counter hits the target value for that signal.”).

DPWM Events

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

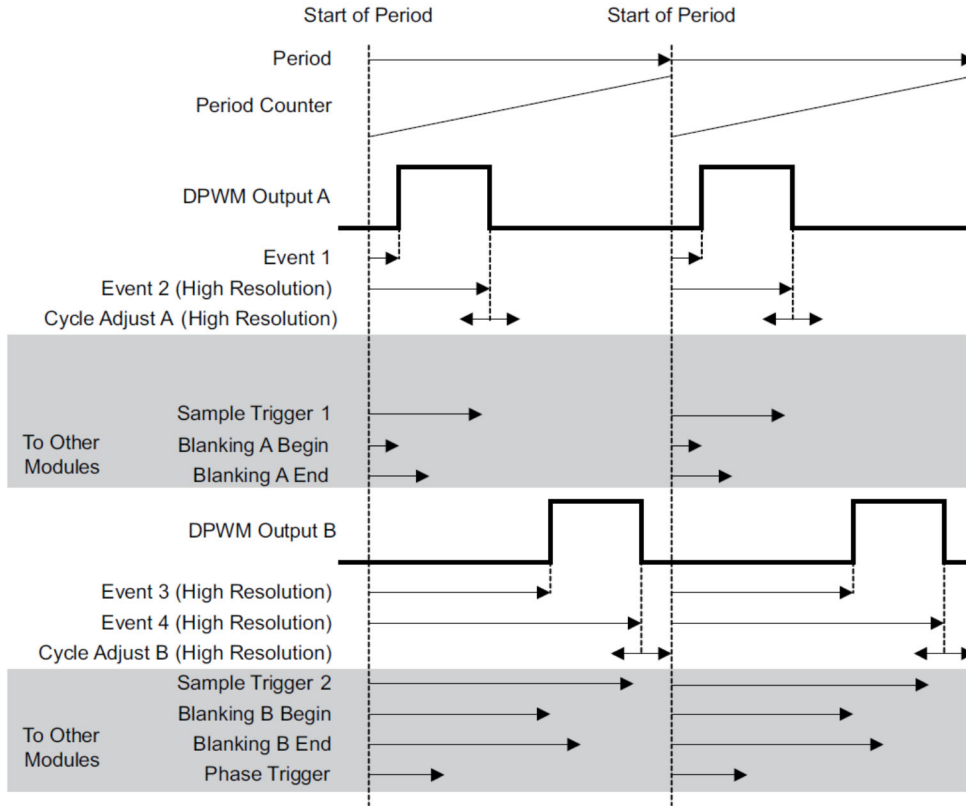
Ex. 1018, 31.

4. Claim 32

- a. **“The method of claim 31 wherein the oscillator and timing events are open-loop with respect to the power train.”**

223. Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this limitation obvious. *See* § VI.E.3. TI UCD3138 shows a Multi-Mode Open Loop figure (below), stating that the DPWM is controlled entirely by its own registers, not by the filter output.

Multi Mode Open Loop



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
 DPWM A Falling Edge = Event 2 + Cycle Adjust A
 DPWM B Rising Edge = Event 3
 DPWM B Falling Edge = Event 4 + Cycle Adjust B
 Phase Trigger = Phase Trigger Register value

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

The drawing above is for multi-mode, open loop. Open loop means that the DPWM is controlled entirely by its own registers, not by the filter output. In other words, the power supply control loop is not closed.

Ex. 1006, 29.

224. TI UCD3140 also discloses an open-loop mode (shown below).

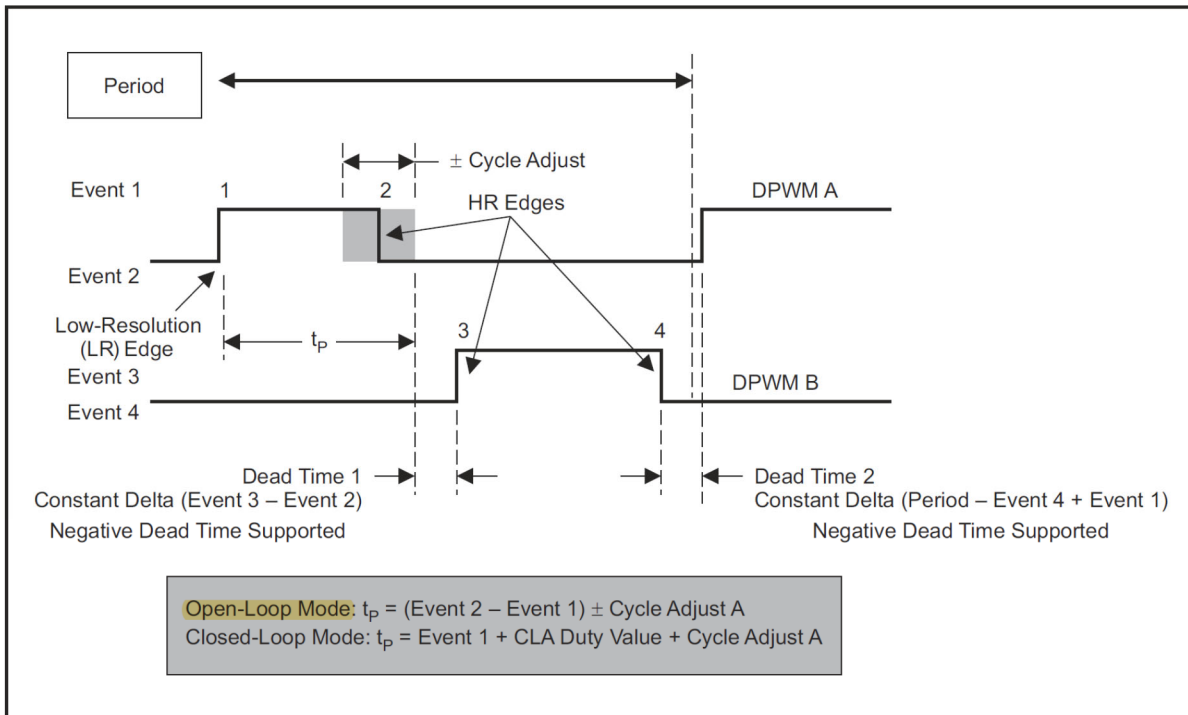


Figure 8. Normal Mode (Duty-Ratio Control) – DPWM Timing Diagram

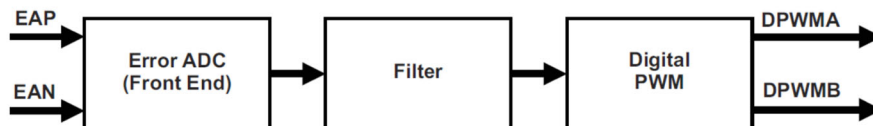
Ex. 1018, 34.

5. Claim 33

- a. “The method of claim 31 wherein the oscillator or timing events are adjusted with feedback from measurements in the power train.”

225. Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this limitation obvious. *See* § VI.E.3 above. TI UCD3138 discloses this limitation of adjusting timing events with feedback provided by the Filter.

These can be connected in many different combinations, with multiple filters and DPWMs. They are capable of supporting functions like input voltage feed forward, current mode control, and constant current/constant power, etc.. The simplest configuration is shown in the following figure:



Ex. 1006, 26.

226. TI UCD3040 also teaches this limitation of adjusting timing events with feedback from by the compensator.

PERIPHERALS

Fusion Digital Power Peripherals

At the core of the UCD30xx controller are its four Fusion Digital Power peripherals (FDPP). Each FDPP can be configured to drive from one to eight DPWM outputs. Each FDPP consists of a differential input error ADC (EADC), a hardware-accelerated digital three-pole/three-zero (3p/3z) compensator, and a digital PWM module.

Ex. 1018, 25.

6. Claim 34

- a. **“The method of claim 33 wherein the measurements and adjustments are performed during the manufacturing process.”**

227. Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this limitation obvious. *See* § VI.E.4. TI UCD3138 and TI UCD3040 both disclose use of firmware data for certain measurements, which is set during the manufacturing process. Ex. 1006, 22, 4.2 Memory (“Within the UCD31xx architecture, there is a 1024x32-bit Boot ROM that contains the initial firmware startup routines for PMBUS communication and non-volatile (FLASH) memory download. This boot ROM is executed after power-up-reset checks if there is a valid FLASH program written.”); Ex. 1018, 20, Memory (“Within the UCD30xx architecture, there is a 1024x32-bit Boot ROM that contains the initial firmware startup routines for PMBUS communication and non-volatile (flash) memory download. This boot ROM is executed after power-up-reset checks if there is a valid flash program written.”); Ex. 1006, 55, 4.23 Temperature Reference (“The temperature reference

register (TEMPREF) provides the ADC12 count when ADC12 measures the internal temperature sensor (channel 14) during the factory trim and calibration. This information can be used by different periodic temperature compensation routines implemented in the firmware. But it should not be overwritten by firmware, otherwise this factory written value will be lost.”).

7. Claim 35

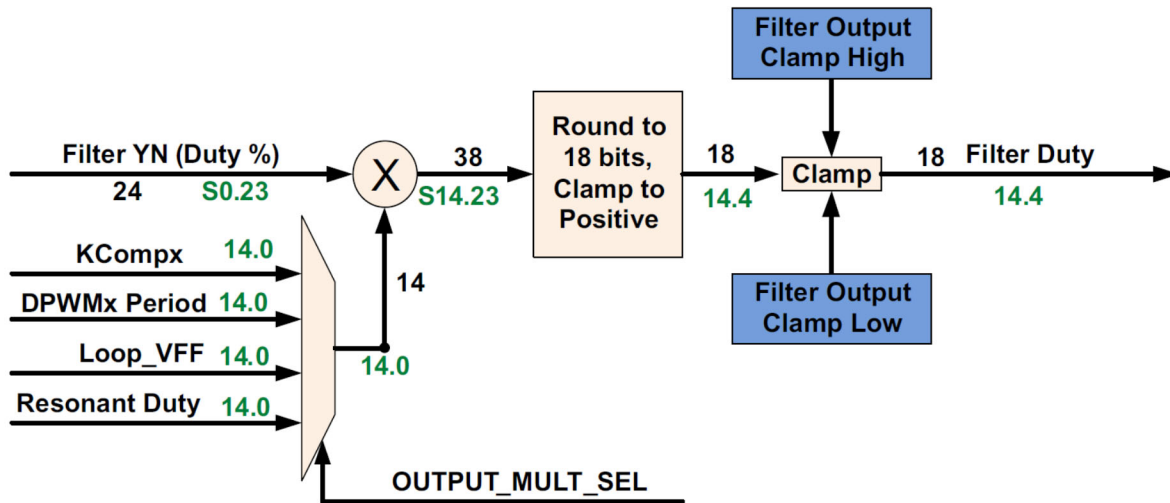
- a. **“The method of claim 33 wherein the measurements and adjustments are performed during operation as part of a closed-loop feedback system.”**

228. Peng-TI UCD3138 (or, alternatively, Peng-TI UCD3040) renders this limitation obvious. *See* § VI.E.4. TI UCD3138 teaches that the measurements and adjustments are performed during operation of the device as part of a closed-loop feedback system, where the Filter provides the feedback.

These can be connected in many different combinations, with multiple filters and DPWMs. They are capable of supporting functions like input voltage feed forward, current mode control, and constant current/constant power, etc.. The simplest configuration is shown in the following figure:



Ex. 1006, 26.

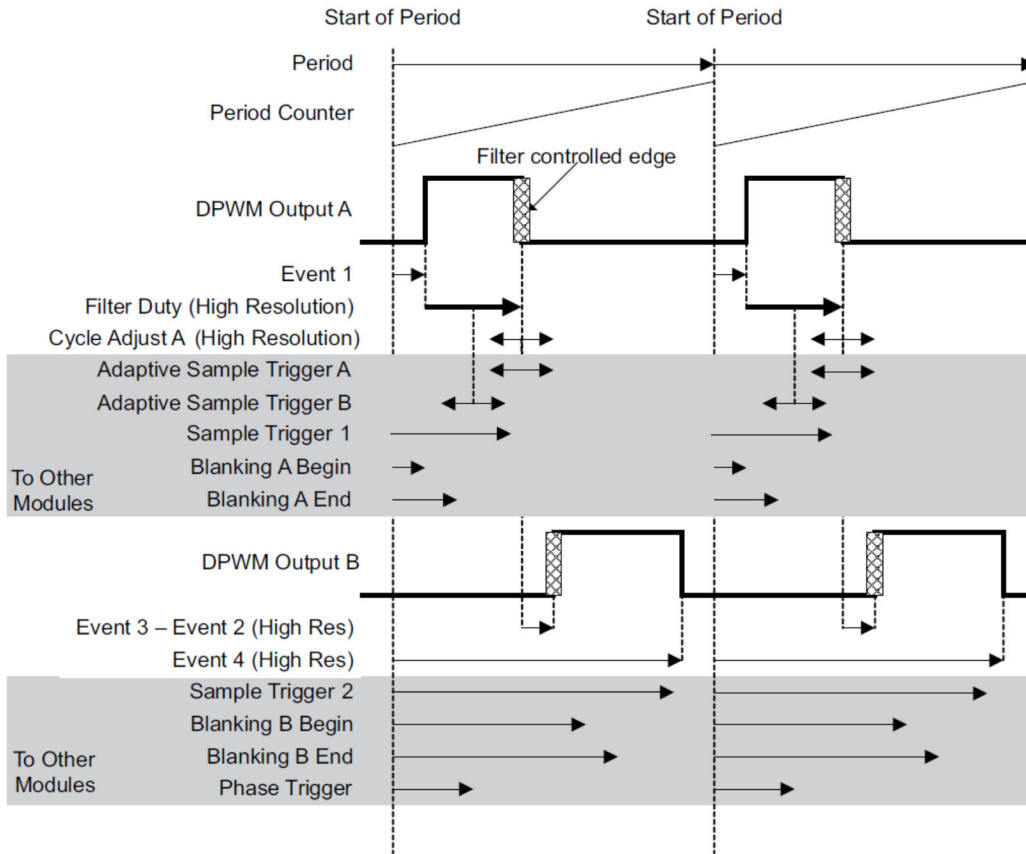


This permits the filter output to be multiplied by a variety of correction factors to match the DPWM Period, to provide for Voltage Feed Forward, or for other purposes. After this, there is another clamp. For resonant mode, the filter can be used to generate both period and duty cycle.

Ex. 1006, 46.

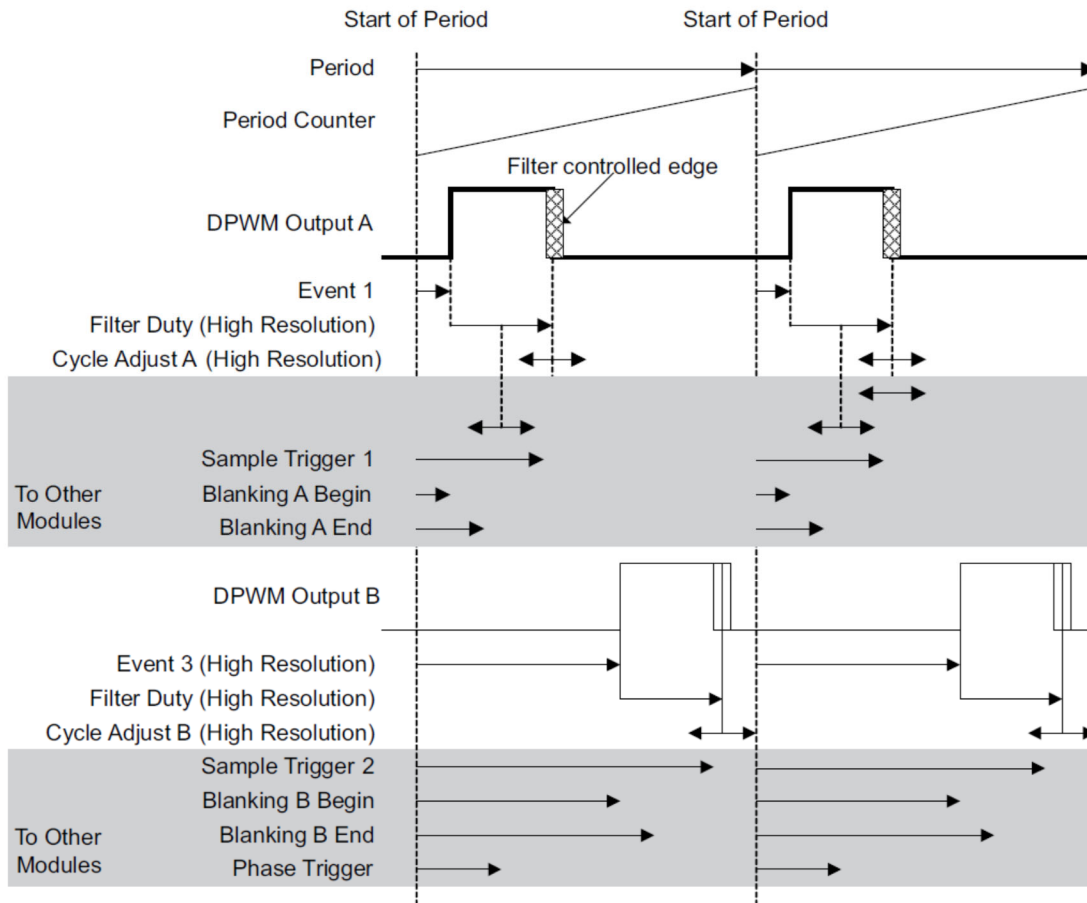
229. TI UCD3138 also has several figures disclosing closed loop operation.

Normal Mode Closed Loop

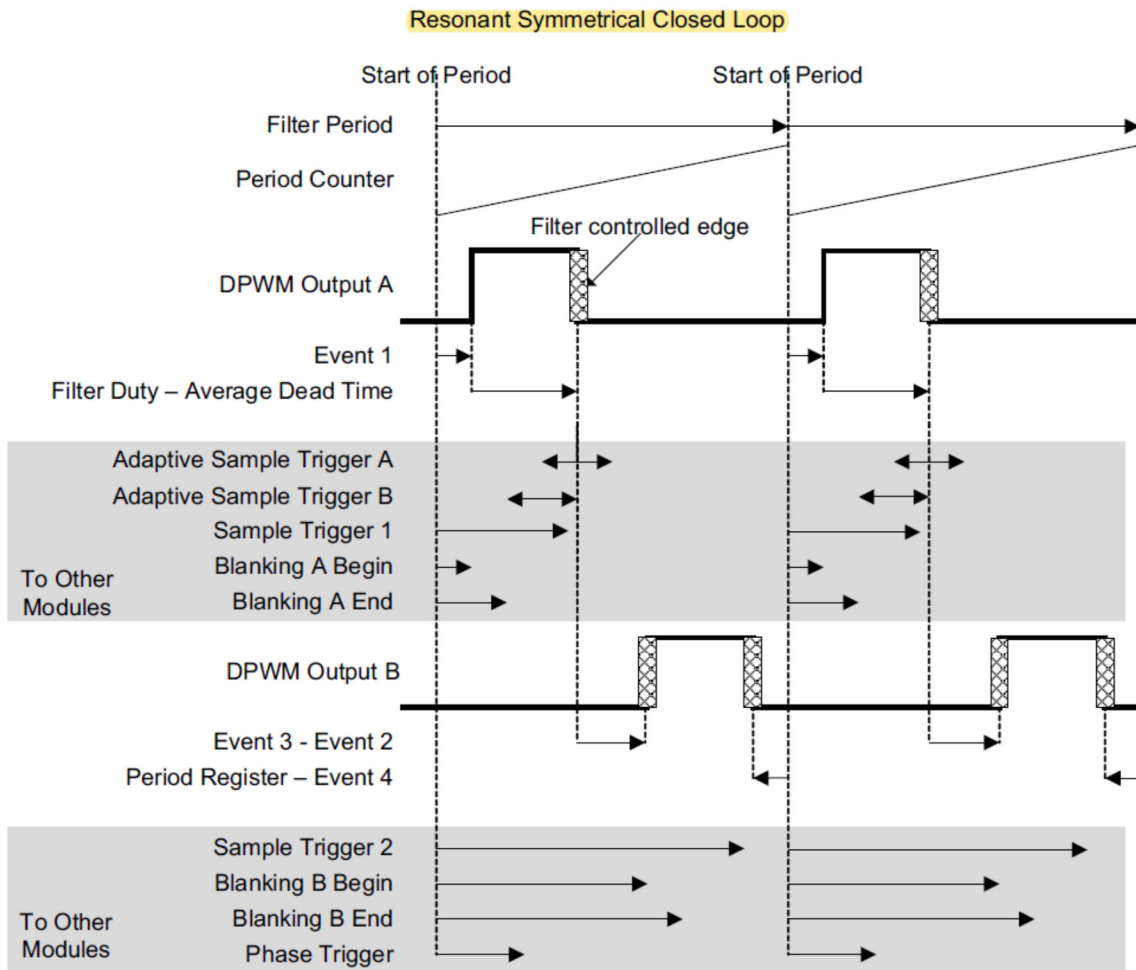


Id., 32.

Multi Mode Closed Loop



Id., 34.



Id., 36. See also, *Id.*, 37, 39.

230. TI UCD3040 also teaches that the measurements and adjustments are performed during operation of the device as part of a closed-loop feedback system, with the compensator providing the feedback.

PERIPHERALS

Fusion Digital Power Peripherals

At the core of the UCD30xx controller are its four Fusion Digital Power peripherals (FDPP). Each FDPP can be configured to drive from one to eight DPWM outputs. Each FDPP consists of a differential input error ADC (EADC), a hardware-accelerated digital three-pole/three-zero (3p/3z) compensator, and a digital PWM module.

Ex. 1018, 25.

231. TI UCD3140 also has several figures disclosing closed loop operation.

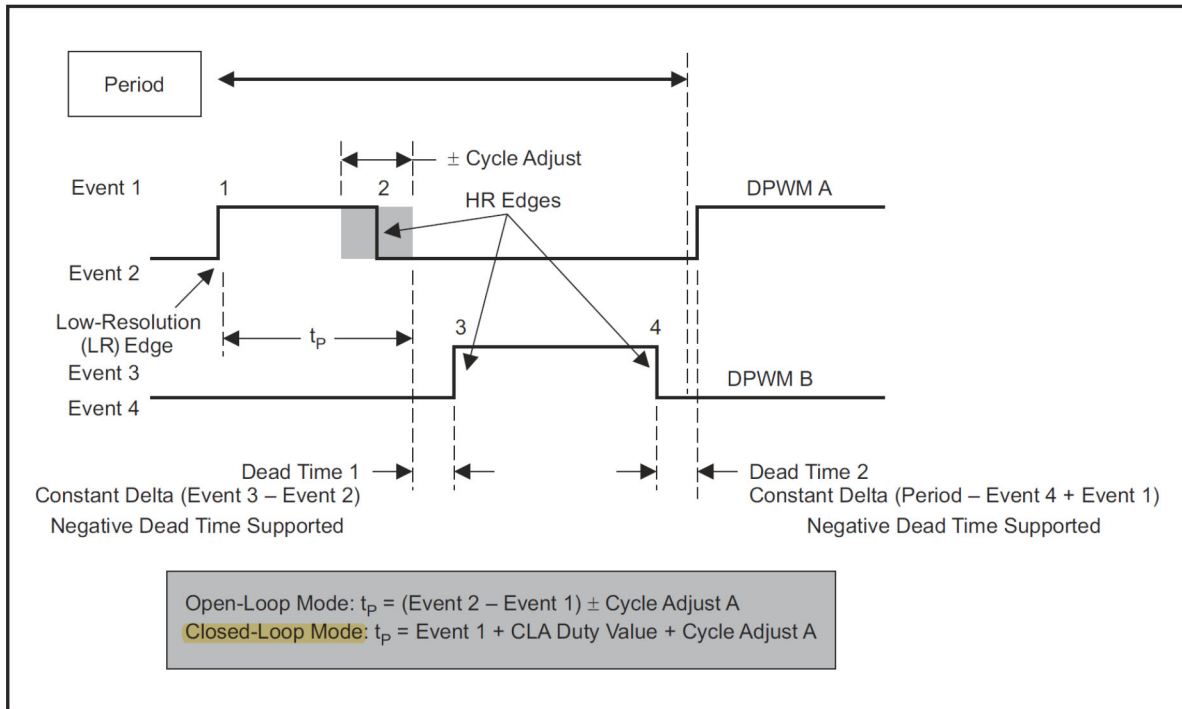


Figure 8. Normal Mode (Duty-Ratio Control) – DPWM Timing Diagram

Ex. 1018, 34.

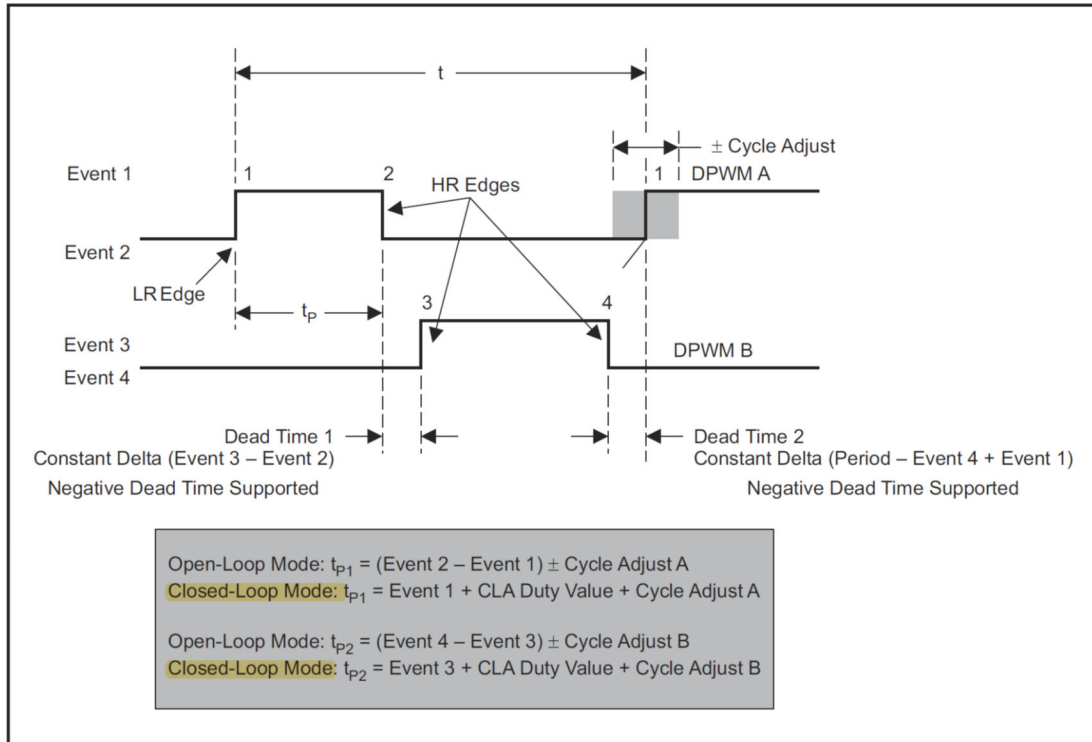


Figure 10. Resonance Mode (Constant-On Duty Ratio With Variable Period) – DPWM Timing Diagram

Ex. 1018, 36.

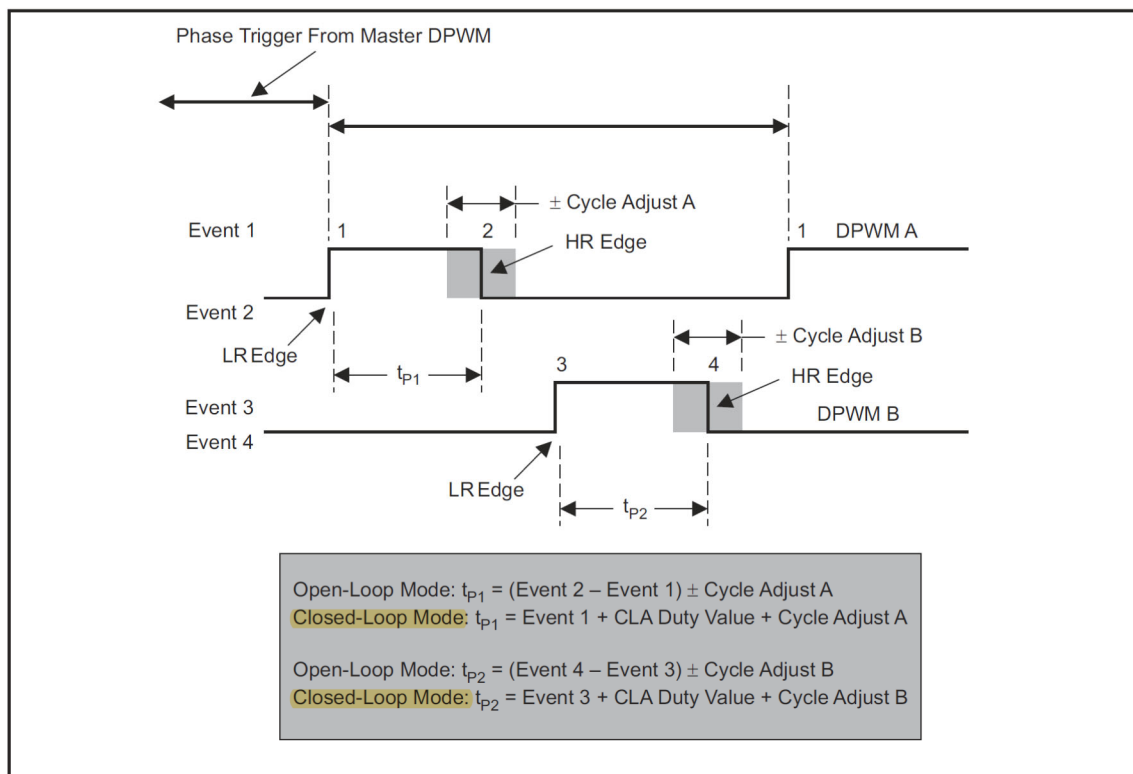


Figure 11. Multi-Output Mode – DPWM Timing Diagram

Ex. 1018, 37.

F. The Challenged Claims are Obvious over Leung in view of AAPA

232. It is my opinion that Leung (Ex. 1013) combined with the AAPA renders obvious claims 1 and 22 of the '481 Patent.

233. A POSITA would have been motivated to combine Leung with the AAPA for purposes of zero current and zero voltage switching because both are related to half-bridge converters, and zero current and zero voltage switching was well known in the art, which the AAPA explicitly teaches. A POSITA would therefore have understood and expected that the AAPA's teachings, which were generally known in the prior art, would apply to Leung's half-bridge converters, and

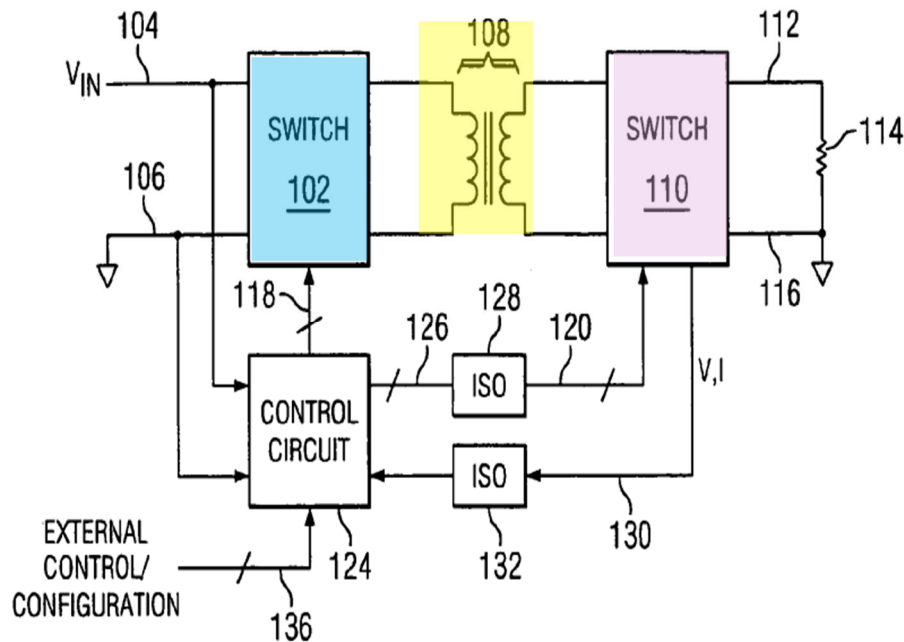
would have looked to the AAPA for additional details related to zero current and zero voltage switching.

1. Claim 1

- a. “A method of synchronously operating a power converter in a series of converter operating cycles the converter having at least one primary switch to drive a resonant power train and at least one secondary switch, the resonant power train including a transformer and having a characteristic resonant frequency and period, the method comprising:”**

234. Leung in combination with the AAPA (“Leung-AAPA”) renders this limitation obvious. Leung discloses a method of synchronously operating a half-bridge power converter, where the converter has at least one primary switch, at least one secondary switch, and a transformer. Ex. 1013, [0062]. The AAPA makes clear that resonant half-bridge converters were well known in the prior art (Ex. 1001, 1:13-59, Fig. 1). A POSITA would have known that a resonant circuit could be added the Leung’s half-bridge converter.

235. Figure 1 of Leung (copied below) shows a half-bridge converter having a primary switch group 102 (in blue), a secondary switch group 110 (in pink), and a transformer 108 (in yellow).



Ex. 1013, Fig.1. With the addition of a resonant circuit to Leung's half-bridge converter as discussed above, the resonant circuit would have a resonant frequency and period.

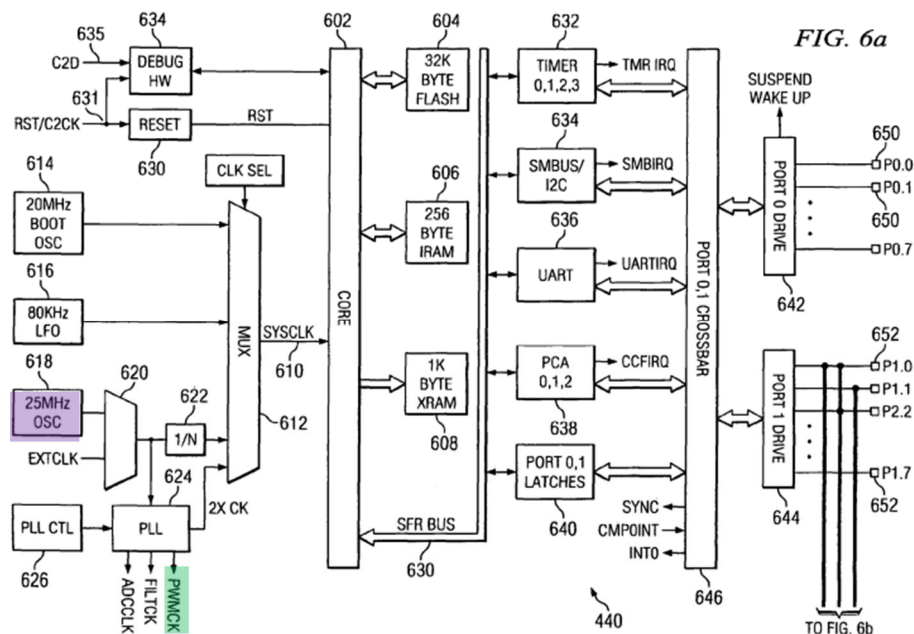
b. “providing an oscillator for generating clock signals at an oscillator frequency;”

236. Leung discloses an oscillator OSC for generating clock signals at an oscillator frequency.

clock, if necessary. Additionally, an external clock is input to the other input of multiplexer 620, such that either the internally generated 25 MHz clock can be utilized or an external clock can be utilized. A phase lock loop 624 is provided which is controlled by a PLL control block 626 and this utilizes the 25 MHz clock 618 as a reference and then multiplies this clock up to as high as 400 kHz. This provides an output to one end of the multiplexer 612 for selection as the SYSCLK. This PLL 624 is operable to generate the other clocks associated with the operation of a digital controller, the clock for the DPWM 416, PWMCK, the filter clock, FILTCLK, and the ADC clock, ADCCLK. This will be described hereinbelow.

[0083] The core 602 is also operable to receive a Reset signal on a block 630, which is operable to generate a reset when it is not in a debug operating mode. In a debug

Ex. 1013, [0082].



Id., Fig. 6a (oscillator shown in purple, and clock signals shown in green).

- c. “generating timing control signals for each of a plurality of events based upon the clock signals in a (A)

standard converter operating cycle, having a standard operating period and frequency, to:”

237. Leung-AAPA discloses that the digital controller generates timing control signals (switching phases 404) from the DPWM to control the primary and secondary switches. Ex. 1013, [0071]-[0072].

Digital Controller—Overall

[0071] Referring now to **FIG. 4**, there is illustrated a block diagram of the digital controller **124** of **FIG. 1**. As described hereinabove, the switching converter is generally realized with a half bridge converter, but a simpler buck converter **402** is illustrated in this figure. This requires a plurality of phases **404** for controlling the switches internal to the buck

converter **402**. This will allow a DC input voltage to be converted to a DC output voltage on output **406**. The digital controller senses the output voltage on the output **406** as a sense voltage, V_{SENSE} , and inputs this to one input of a differential analog-to-digital converter (ADC) **408**. The other input of the ADC **408** is connected to an analog or reference voltage generated by a V_{REF} generator **410** that, as will be described hereinbelow, comprises a digital-to-analog converter (DAC).

Ex. 1013, [0071].

[0072] The output of the ADC 408 is a digital output that represents the difference between the analog output voltage on the DC output 406 and the “set point” generated by V_{REF} generator 410. The output of the V_{REF} generator 410 is typically the desired output voltage. As such, the operation of the control loop at regulation will typically result in a “0” output from the ADC 408. As will be described hereinbelow, this is the “0” code for the ADC 408. This is input to a digital compensator 412, which is operable to provide some phase lead in the loop. The buck converter 402 is comprised of a combination of a series inductor and shunt capacitor that forms an LC network, which provides a phase lag of 180° . The control loop will typically be provided by a negative feedback loop and will result in an additional negative phase shift of 180° . If the loop were allowed to operate in this manner, this would result in a 0° total phase change which would be an unstable loop. As such, the digital compensator 412 provides some phase lead to stabilize the loop. The output of digital compensator 412 provides the digital control value $u(n)$ on a digital output bus 414 for input to a digital pulse width modulator (DPWM) 416. This provides the various clock signals which provide the switching phases 404 to the buck converter 402 (or to a half bridge converter described herein above).

Ex. 1013, [0072].

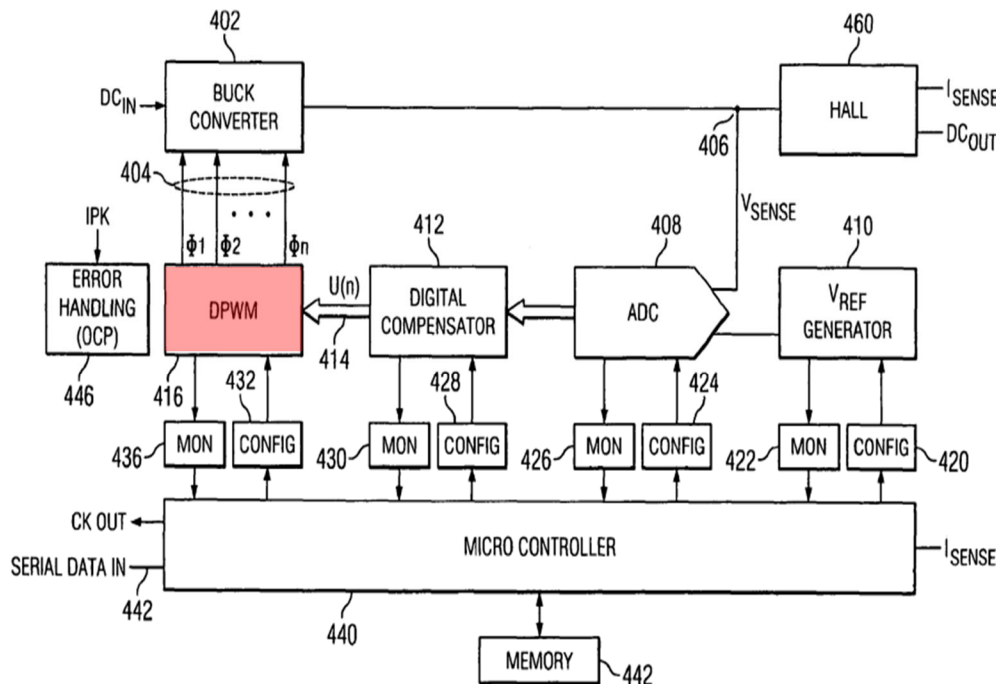


FIG. 4

Id., Fig. 4 (showing switching phases 404 (in red) coming from DPWM). A POSITA would understand that Leung-AAPA's converter operating cycle would have a standard operating period and frequency, which is the resonant period and frequency of the resonant converter because the AAPA discusses achieving ZVS and ZCS, and this requires a resonant frequency.

- d. **“(i) turn the at least one primary switch ON and OFF at times when essentially zero voltage is impressed across the respective at least one primary switch and essentially zero resonant current is flowing in the respective at least one primary switch; and”**

238. Leung-AAPA renders this limitation obvious. Leung discloses that the digital control circuit 124 “is operable to control the operation of the primary switch group 102 and the secondary switch group 110. Ex. 1013, [0063].

239. The AAPA teaches that zero voltage and zero current switching can be used to turn the primary switches on and off. For example, the AAPA discloses turning on (closing) a primary switch (S1) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32. It also discloses turning off (opening) a primary switch S1 “when the sinusoidal current flow completes half-cycle, and the current I_{pri} returns substantially to zero” and “the voltages across switches S2-120 and S4-140 decline toward zero.” *Id.*, 1:36-43.

- e. **“(ii) turn the at least one secondary switch ON and OFF at times when essentially zero current is flowing**

in the respective at least one secondary switch and essentially zero voltage is impressed across the respective at least one secondary switch; and”

240. Leung-AAPA renders this limitation obvious. The AAPA discloses that zero voltage and zero current switching can be used to turn the secondary switches on and off. For example, the AAPA discloses that “the VTM may include secondary switches turned on and off essentially at times of zero voltage to rectify power from the transformer. The VTM may include secondary switches on and off essentially at times of zero current to rectify power from the transformer.” Ex. 1009, 9:25-29.

241. The AAPA also discloses turning on (closing) a secondary switch (S3) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32.

242. The AAPA further discloses that “the voltage across one or more of the switches may be monitored to establish the timing of a zero-voltage switching or zero-current switching event.” *Id.* 1:66-2:3.

243. The AAPA further discloses that “the timing architecture of the SAC topology supports . . . ZCS and ZVS operation of the secondary switches.” Ex. 1009, 18:49-56.

f. “wherein the oscillator frequency is preset, and”

244. Leung discloses that the frequency of oscillator OSC is preset at 25 MHz. Ex. 1013, [0082] (“The 25 MHz oscillator is the primary oscillator at the operating frequency of the core 602.”).

g. “the timing of the timing control signals for one or more selected events may be set independently of other timing control signals and events.”

245. Leung discloses that timing of the timing control signals (switching phases 404) are independent. Ex. 1013, [0068] (“Referring now to Fig. 3, there is illustrated a timing diagram for generating the switching pulses to operate the switch of Fig. 2.”). As shown in Figure 3 of Leung (below), each timing pulse P1-P5 correlate to various switching transistors, and are all different, which ensures independent timing control signals.

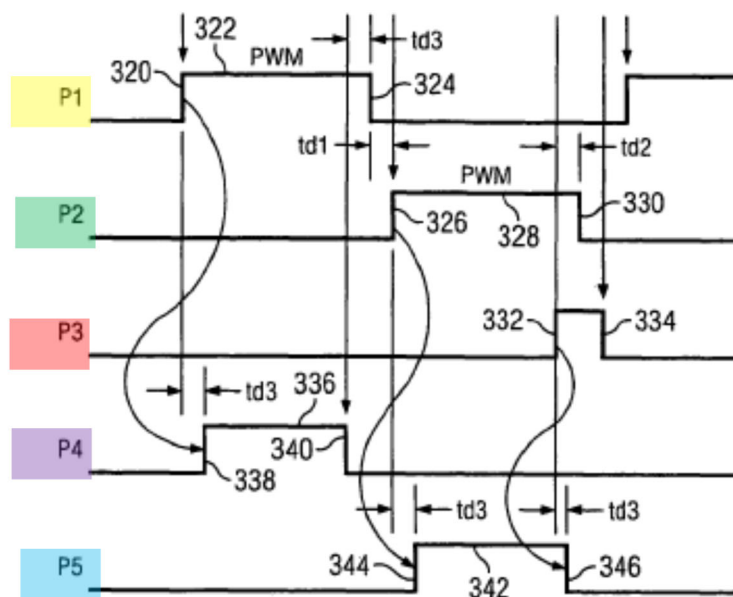


FIG. 3

Ex. 1013, Fig. 3.

2. Claim 22

a. “The method of claim 1 further comprising”

See § VI.F.1.

b. “providing a gate drive circuit for operating selected selected switches in the converter and generating timing control signals based upon the clock signals to (a) initiate a transition of the selected switches from ON to OFF or OFF to ON, (b) hold the selected switches ON, and (c) hold the selected switches OFF.”

246. Leung discloses this limitation. Leung discloses that the DPWM generates timing control signals (switching phases 404) based on clock signals to control the converter switches.

[0072] The output of the ADC 408 is a digital output that represents the difference between the analog output voltage on the DC output 406 and the “set point” generated by V_{REF} generator 410. The output of the V_{REF} generator 410 is typically the desired output voltage. As such, the operation of the control loop at regulation will typically result in a “0” output from the ADC 408. As will be described hereinbelow, this is the “0” code for the ADC 408. This is input to a digital compensator 412, which is operable to provide some phase lead in the loop. The buck converter 402 is comprised of a combination of a series inductor and shunt capacitor that forms an LC network, which provides a phase lag of 180°. The control loop will typically be provided by a negative feedback loop and will result in an additional negative phase shift of 180°. If the loop were allowed to operate in this manner, this would result in a 0° total phase change which would be an unstable loop. As such, the digital compensator 412 provides some phase lead to stabilize the loop. The output of digital compensator 412 provides the digital control value $u(n)$ on a digital output bus 414 for input to a digital pulse width modulator (DPWM) 416. This provides the various clock signals which provide the switching phases 404 to the buck converter 402 (or to a half bridge converter described herein above).

Ex. 1013, [0072].

[0139] Referring now to **FIG. 34**, there is illustrated a general block diagram of the DPWM **416**. As noted hereinabove, the DPWM **416** is a state machine that is operable to generate up to six phases for use in driving external drivers that will control switches on the switching power converter. Each of these phases will be defined by a leading edge and a trailing edge, either leading or trailing edge being rising or falling. Either the u(n) signal from the digital

See also, id., [0139] (further describing switching phases 404).

G. The Challenged Claims are Obvious over AN1336 in view of dsPIC33FJ06GS101 and AAPA

247. It is my opinion that AN1336 (Ex. 1019) combined with dsPIC33FJ06GS101 (Ex. 1020) and further combined with the AAPA renders obvious claims 1 and 22 of the '481 Patent.

248. A POSITA would have been motivated to combine AN1336 with dsPIC33FJ06GS101 because the AN1336 datasheet states that its converter “permits the implementation of control and supervision/management tasks with a small pin count dsPIC DSC from Microchip. Sophisticated control is possible, using the DSP capabilities of dsPIC DSC devices.” Ex. 1019, 1.

249. A POSITA would also have been motivated to combine AN1336 with the AAPA for purposes of zero current and zero voltage switching because both are related to half-bridge resonant converters, and AN1336 discusses zero current and zero voltage switching, which the AAPA explicitly teaches. A POSITA would therefore have understood and expected that the AAPA’s teachings, which were

generally known in the prior art, would apply to AN1336's resonant converters, and would have looked to the AAPA for additional details related to zero current and zero voltage switching.

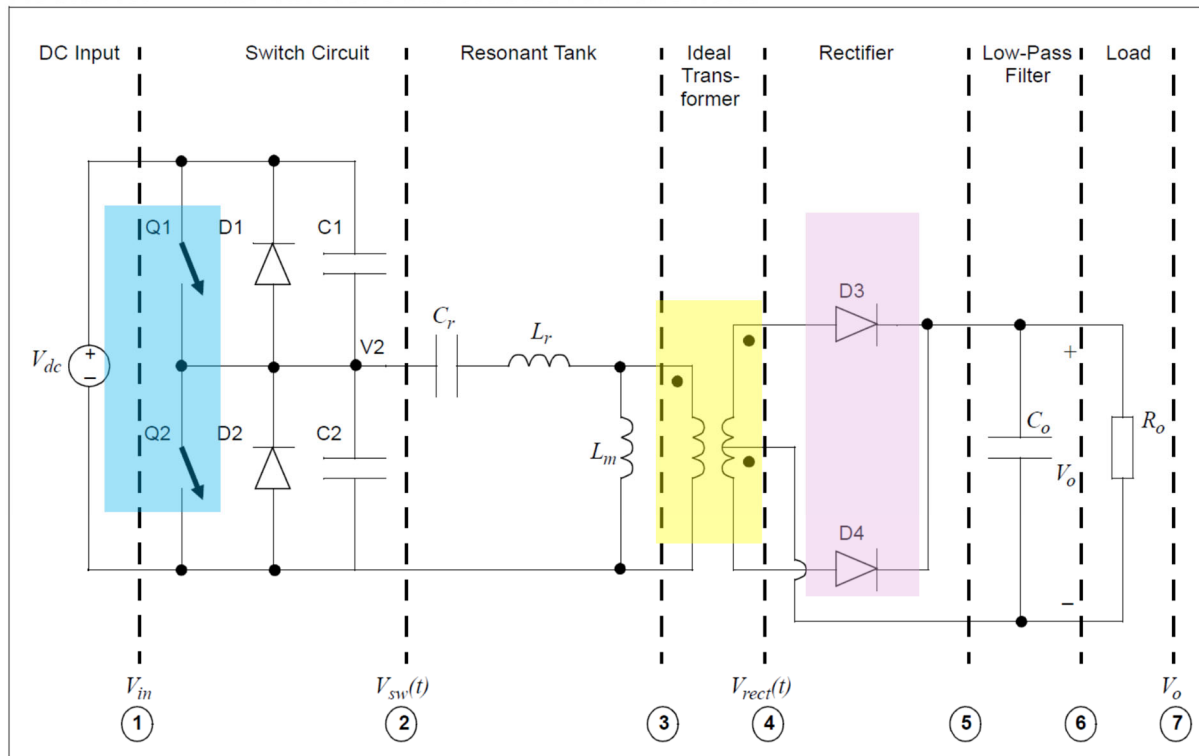
1. Claim 1

- a. “A method of synchronously operating a power converter in a series of converter operating cycles the converter having at least one primary switch to drive a resonant power train and at least one secondary switch, the resonant power train including a transformer and having a characteristic resonant frequency and period, the method comprising:”**

250. AN1336 discloses this limitation. AN1336 teaches a method of synchronously operating a half-bridge power converter, where the converter has at least one primary switch that drives a resonant circuit, at least one secondary switch, and a transformer. Ex. 1019, 8.

251. Figure 10 of AN1336 (copied below) discloses a half-bridge converter having primary switches Q1 and Q2 (in blue), a resonant circuit (LLC) on the primary side consisting of inductor Lr, inductor Lm, and capacitor Cr, secondary switches D3 and D4 (in pink), and a transformer (in yellow). The text describing Figure 10 notes that “a diode-based full-wave rectifier is shown” but that “[a] number of different topologies can be used” including a “synchronous rectifier.” The synchronous rectifier would consist of a circuit containing MOSFET switches being used in place of the diode-based rectifier circuit shown in Figure 10. *Id.*

FIGURE 10: LLC CIRCUIT COMPONENTS AND SECTIONS



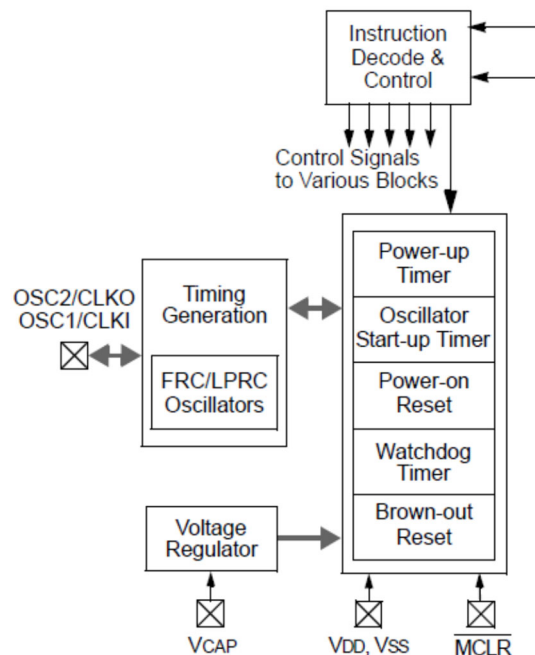
Ex. 1019, Fig. 10.

252. AN1336 also teaches that the converter operates at a resonant frequency and period. Ex. 1019, 28 (“This section describes the operation of the LLC converter at resonance, which is when the MOSFETs are operated at the same frequency as the resonant frequency, as set by the selected components.”).

b. “providing an oscillator for generating clock signals at an oscillator frequency;”

253. AN1336 in combination with dsPIC33FJ06GS101 (“AN1336-dsPIC33FJ06GS101”) renders this limitation obvious. Figure 1-1 of

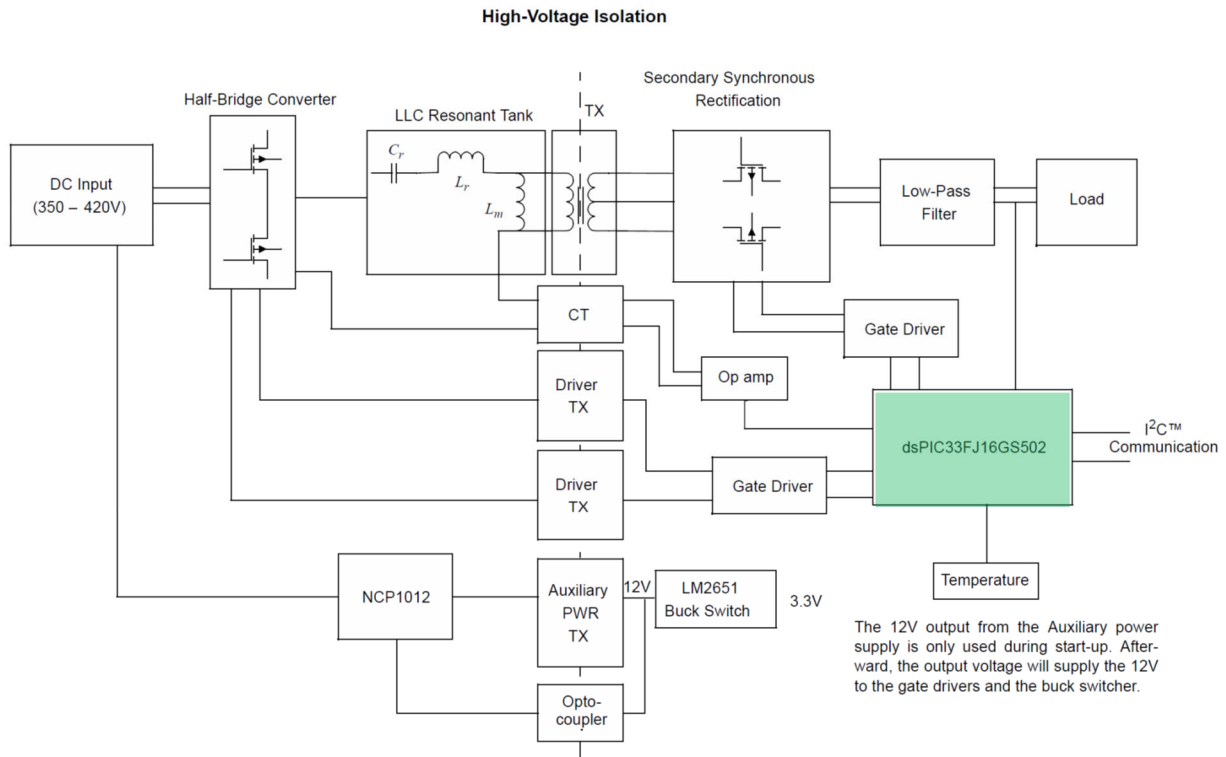
dsPIC33FJ06GS101 (below) discloses an oscillator (OSC1 or OSC2) for generating clock signals at an oscillator frequency.



Ex. 1020, 6 (Fig. 1-1). *See also, id.*, 133 (“The oscillator system provides external and internal oscillator options as clock sources.”).

- c. **“generating timing control signals for each of a plurality of events based upon the clock signals in a (A) standard converter operating cycle, having a standard operating period and frequency, to:”**

254. AN1336-dsPIC33FJ06GS101 renders this limitation obvious. Figure 46 of AN1336 (below) shows a dsPIC controller (in green) that generates timing control signals to control the primary and secondary switches of the converter.



Ex. 1019, 36 (Fig. 46).

255. In addition, dsPIC33FJ06GS101 discloses that its timing control signals (PWM outputs) can control different timing events (“The high-speed PWM module incorporates . . . individual time base and duty cycle for each of the eight PWM outputs.”). Ex. 1020, 195.

256. AN1336 also teaches that the converter operates and controls the switches at a resonant frequency and period. Ex. 1019, 28 (“This section describes the operation of the LLC converter at resonance, which is when the MOSFETs are operated at the same frequency as the resonant frequency, as set by the selected components.”).

- d. **“(i) turn the at least one primary switch ON and OFF at times when essentially zero voltage is impressed across the respective at least one primary switch and essentially zero resonant current is flowing in the respective at least one primary switch; and”**

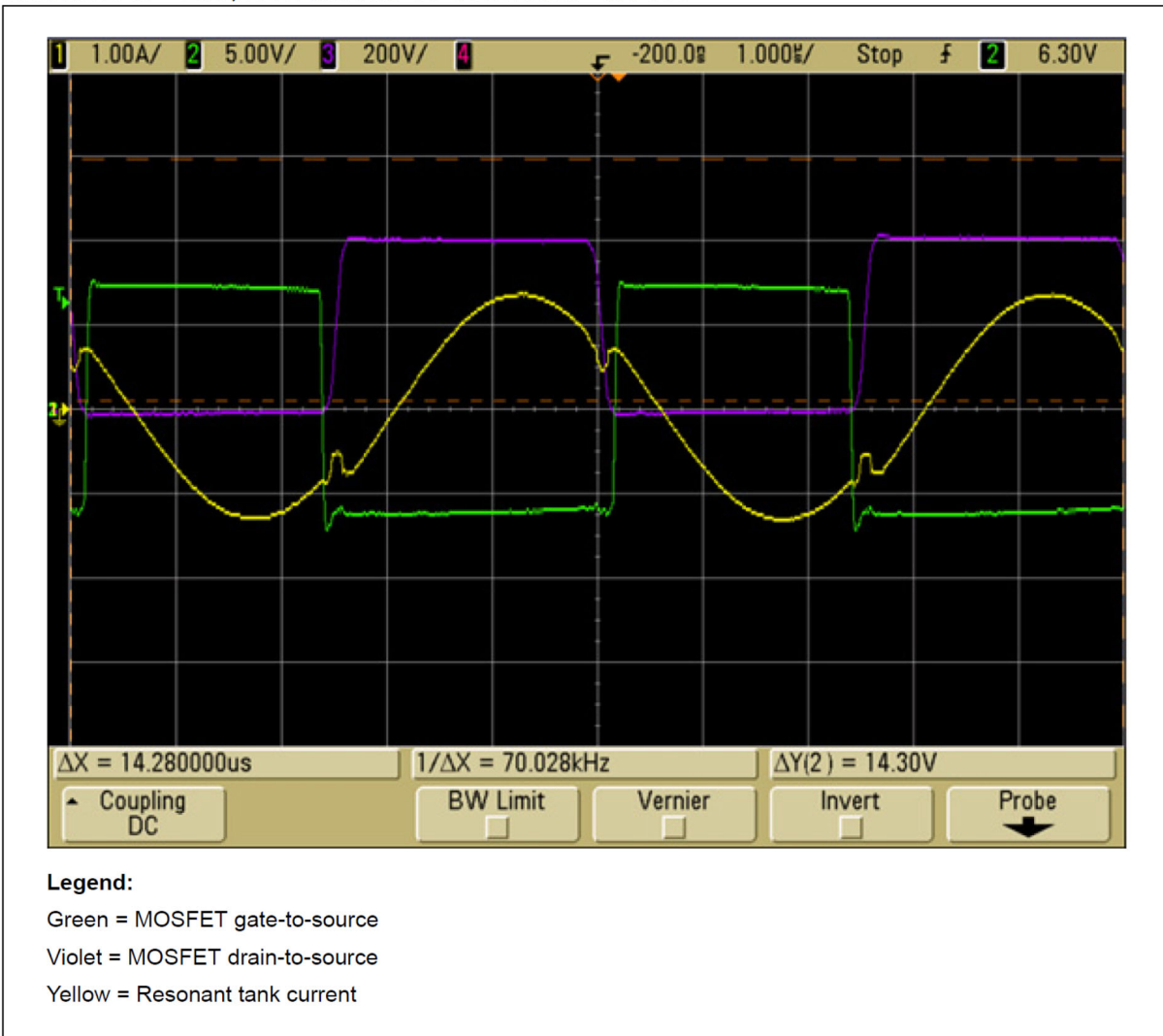
257. AN1336 in combination with the AAPA (hereinafter “AN1336-AAPA”) renders this limitation obvious. AN1336 discloses that the primary switches turn on and off with zero voltage switching.

B.6 Zero Voltage Switching

Due to the phase shift between the resonant tank current and voltage the half-bridge MOSFETs are able to switch without any turn on losses. Figure B-9 and Figure B-10 demonstrate zero voltage switching on the low-side MOSFET.

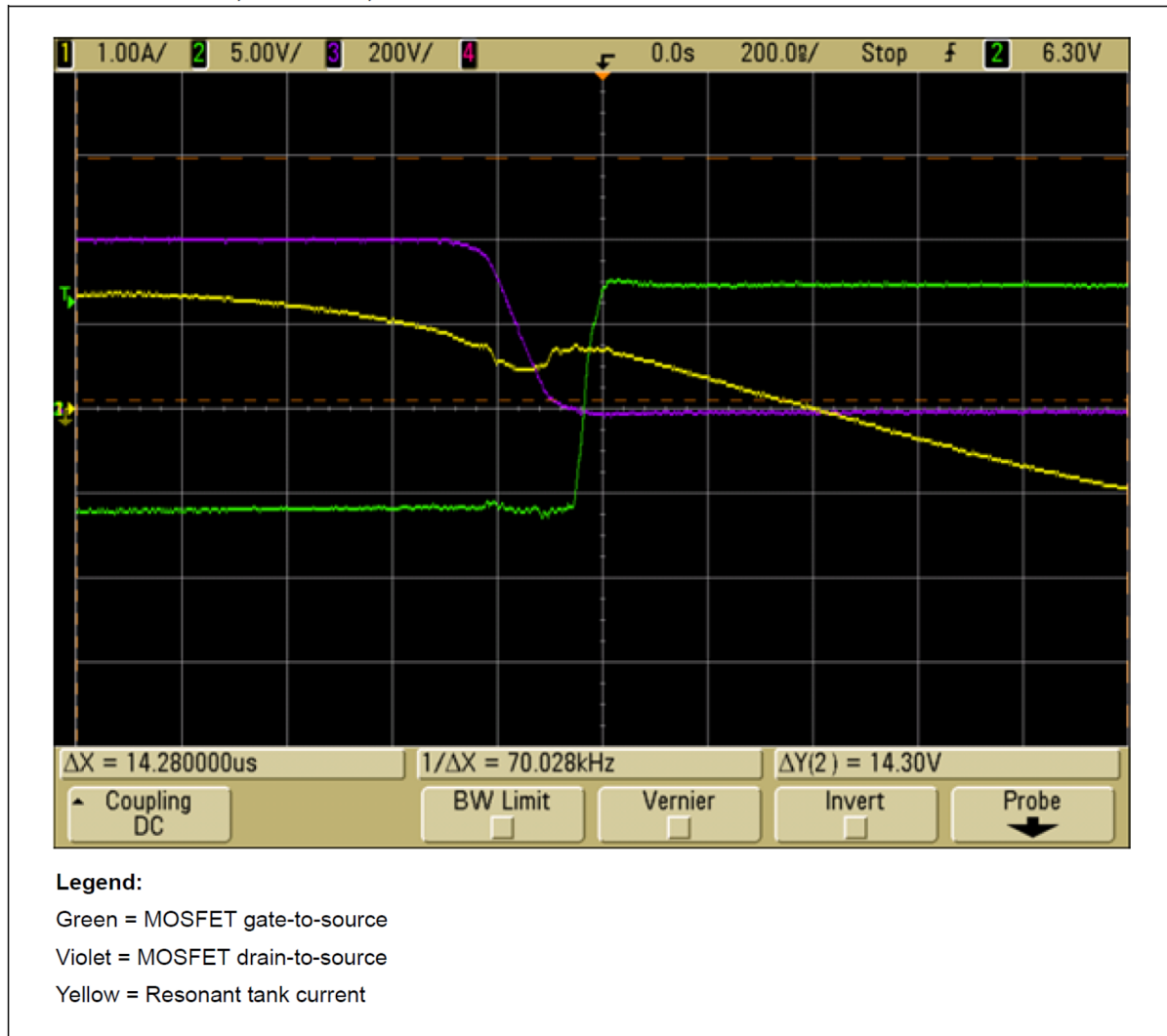
Ex. 1019, 59.

FIGURE B-9: ZVS, I_{OUT} : 8.5A INPUT VOLTAGE: ~400 Vdc



Ex. 1019, 59 (Fig. B-9).

FIGURE B-10: ZVS, I_{OUT} : 8.5A, INPUT VOLTAGE: ~400 VDC



Ex. 1019, 59 (Fig. B-9). AN1336 also discloses that “MOSFET Q1 can be closed at any time during this interval: the voltage drop on it is almost zero, so that the turn-on losses are pretty close to zero. Zero Voltage Switching ZVS is obtained.” *Id.*, 28.

258. AN1336 further discloses that “at resonance . . . the tank current exactly equals the magnetizing current. This, then, is the current flowing into Q1 when it opens. This current should be as small as possible to have low turn off switching

losses.” *Id.*, 29. This means that the resonant current in Q1 is zero at that time when the magnetizing current and tank current are equal, because the resonant current equals tank current minus the magnetizing current. *Id.*, 32 (Fig. 43).

259. The AAPA discloses that zero voltage and zero current switching can be used to turn the primary switches on and off. For example, the AAPA discloses turning on (closing) a primary switch (S1) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32. It also discloses turning off (opening) a primary switch S1 “when the sinusoidal current flow completes half-cycle, and the current I_{pri} returns substantially to zero” and “the voltages across switches S2-120 and S4-140 decline toward zero.” *Id.*, 1:36-43.

- e. **“(ii) turn the at least one secondary switch ON and OFF at times when essentially zero current is flowing in the respective at least one secondary switch and essentially zero voltage is impressed across the respective at least one secondary switch; and”**

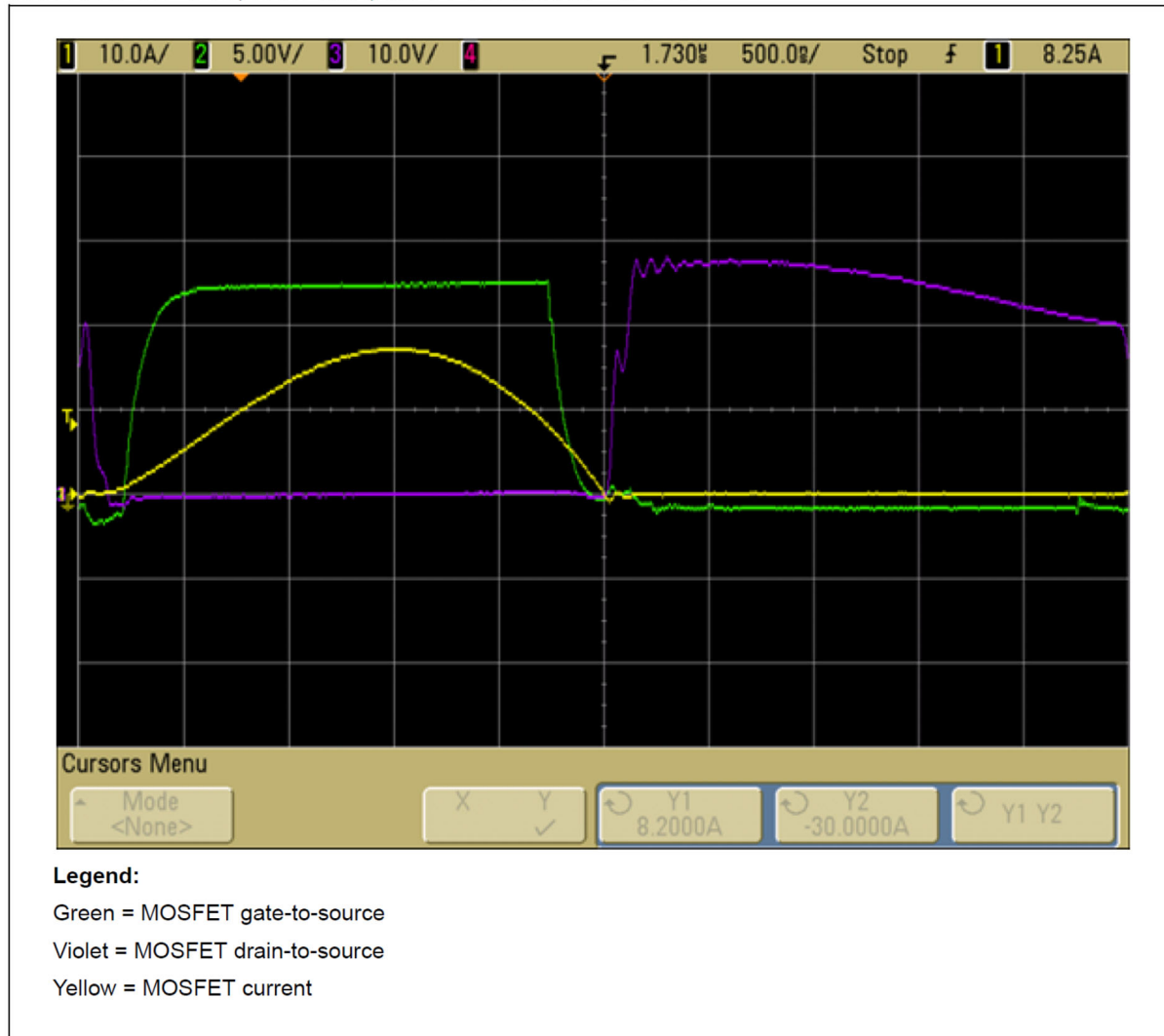
260. AN1336-AAPA renders this limitation obvious. AN1336 discloses that the secondary switches turn on and off with zero current switching.

B.7 Zero Current Switching

Figure B-11 demonstrates zero current switching on the secondary rectifier. As the MOSFET current becomes zero the MOSFETs Drain-to-Source Voltage begins to rise. This eliminates any turn-off losses.

Ex. 1019, 61.

FIGURE B-11: ZCS, I_{out} : 8.5A, INPUT VOLTAGE: ~400 Vdc



Id. (Fig. B-11).

261. The AAPA discloses that zero voltage and zero current switching can be used to turn the secondary switches on and off. For example, the AAPA discloses that “the VTM may include secondary switches turned on and off essentially at times of zero voltage to rectify power from the transformer. The VTM may include

secondary switches on and off essentially at times of zero current to rectify power from the transformer.” Ex. 1009, 9:25-29.

262. The AAPA also discloses turninf on (closing) a secondary switch (S3) “when the voltages across switches S1 110 and S3 130, and the resonant portion of the primary current I_{pri} , are each substantially zero.” Ex. 1001, 1:28-32.

263. The AAPA further discloses that “the voltage across one or more of the switches may be monitored to establish the timing of a zero-voltage switching or zero-current switching event.” *Id.* 1:66-2:3.

264. The AAPA further discloses that “the timing architecture of the SAC topology supports . . . ZCS and ZVS operation of the secondary switches.” Ex. 1009, 18:49-56.

f. “wherein the oscillator frequency is preset, and”

265. AN1336-dsPIC33FJ06GS101 renders this limitation obvious. dsPIC33FJ06GS101 discloses that the primary oscillator has a frequency “in the range of 10 MHz to 40 MHz,” which can be preset by the user. Ex. 1020, 134.

g. “the timing of the timing control signals for one or more selected events may be set independently of other timing control signals and events.”

266. AN1336-dsPIC33FJ06GS101 renders this limitation obvious. dsPIC33FJ06GS101 discloses that the timing of its timing control signals (PWM outputs) are set independently of other timing control signals. Ex. 1020, 195 (“The

high-speed PWM module incorporates . . . individual time base and duty cycle for each of the eight PWM outputs.”); *id.* (“Independent fault/current-limit inputs for each of the eight PWM outputs.”); *id.*, 1 (“Up to four PWM pairs with independent timing.”).

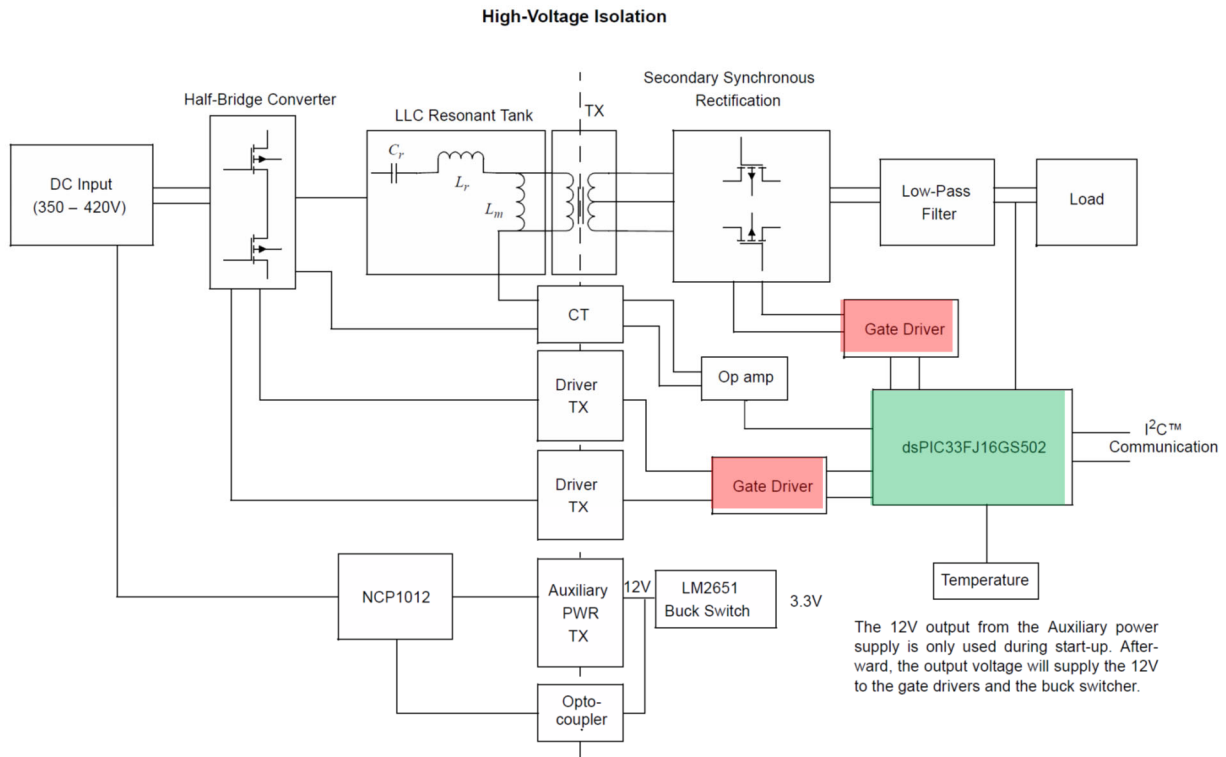
2. Claim 22

a. “The method of claim 1 further comprising”

See § VI.G.1.

b. “providing a gate drive circuit for operating selected selected switches in the converter and generating timing control signals based upon the clock signals to (a) initiate a transition of the selected switches from ON to OFF or OFF to ON, (b) hold the selected switches ON, and (c) hold the selected switches OFF.”

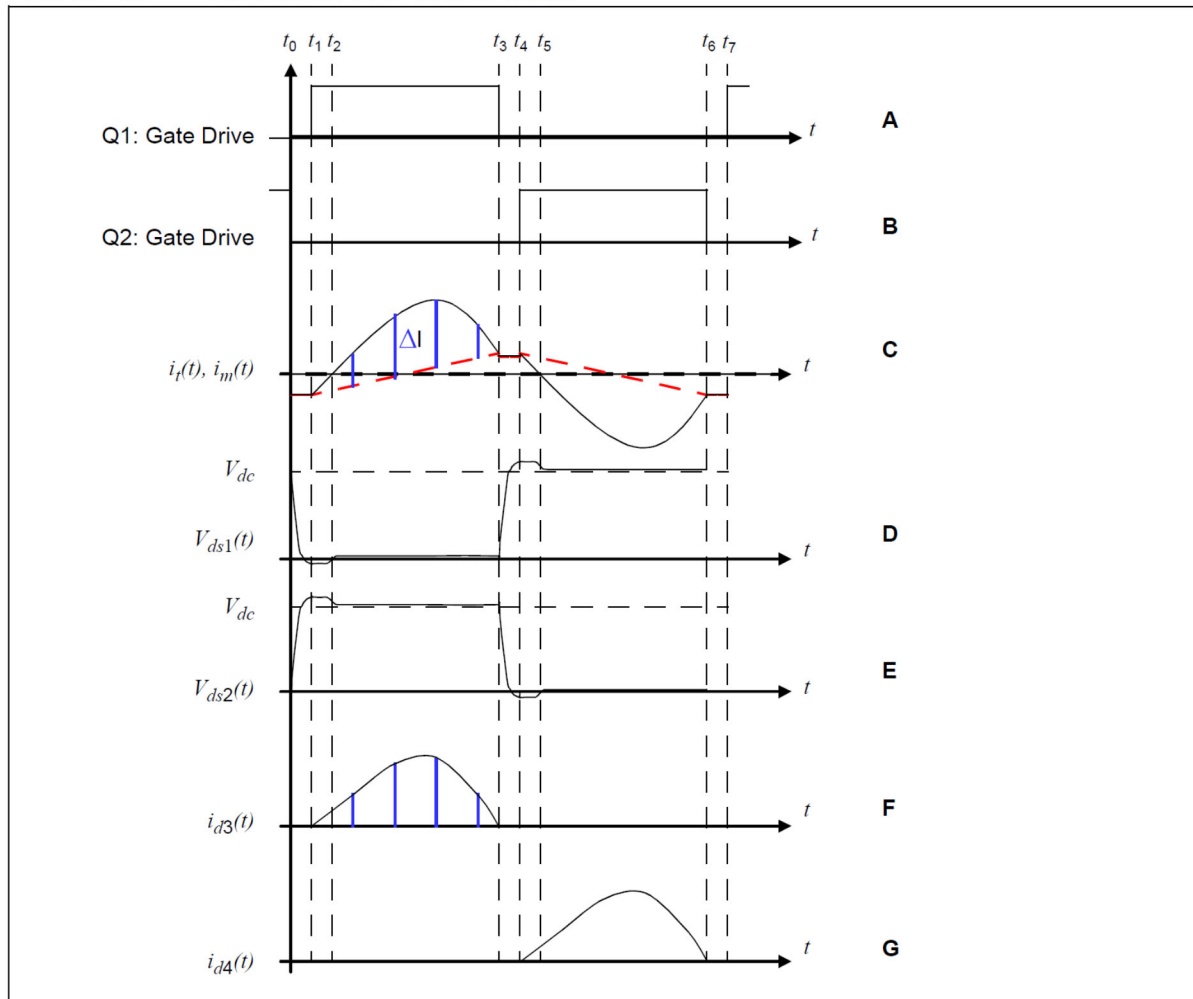
267. AN1336-dsPIC33FJ06GS101 renders this limitation obvious. Figure 46 of AN1336 (copied below) discloses a dsPIC digital controller (in green) that controls Gate Drive circuits (in red) for operating the primary and secondary switches of the converter.



Ex. 1019, 36 (Fig. 46).

268. Figure 43 (below) shows the relevant waveforms of the converter circuit operating at resonance, including the transitions for turning the selected switches from on to off or off to on, holding the selected switches on, or holding the selected switches off.

FIGURE 43: RELEVANT LLC WAVEFORMS



Ex. 1019, 32 (Fig. 43); *see also* Figs. 37-42 (showing the converter circuit at various time intervals).

269. In addition, dsPIC33FJ06GS101 discloses that the PWM module generates timing control signals (PWM outputs) to control the converter switches.

Ex. 1020, 195 (“The high-speed PWM module incorporates . . . individual time base and duty cycle for each of the eight PWM outputs.”).

VII. SECONDARY CONSIDERATIONS

270. There are no secondary considerations of non-obviousness with a nexus to the claimed invention of the '481 Patent.

VIII. CONCLUSION

271. Based on the above, it is my opinion that the Challenged Claims of the '481 Patent are invalid and unpatentable. Each of the claims was obvious over the prior art, and a POSITA would have readily appreciated that the claims were not inventive.

I hereby declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements are punishable by fine or imprisonment or both. *See* 18 U.S.C. § 1001.

Date: November 13, 2023

Respectfully submitted,

A handwritten signature in black ink that reads "Dr. Douglas C. Hopkins". The signature is written in a cursive style with a horizontal line extending to the right.

Douglas Charles Hopkins, Ph.D.