# UCD3138
## Highly Integrated Digital Controller for Isolated Power

# Data Manual

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Literature Number: SLUSAP2 A
March 2012–Revised March 2012

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# Highly Integrated Digital Controller for Isolated Power

Check for Samples: UCD3138

## 1 Introduction

### 1.1 Features

- Digital Control of up to 3 Independent Feedback Loops
  - Dedicated PID based hardware
  - 2-pole/2-zero configurable
  - Non-Linear Control
- Up to 16MHz Error Analog to Digital Converter (EADC)
  - Configurable Resolution as Small as 1mV/LSB
  - Automatic Resolution Selection
  - Up to 8x Oversampling
  - Hardware Based Averaging (up to 8x)
  - 14 bit Effective DAC
- Up to 8 High Resolution Digital Pulse Width Modulated (DPWM) Outputs
  - 250ps Pulse Width Resolution
  - 4ns Frequency Resolution
  - 4ns Phase Resolution
  - Adjustable Phase Shift Between Outputs
  - Adjustable Dead-band Between Pairs
  - Up to 2MHz Switching Frequency
- Configurable PWM Edge Movement
  - Trailing Modulation
  - Leading Modulation
  - Dual Edge Modulation
- Configurable Feedback Control
  - Voltage Mode
  - Average Current Mode
  - Peak Current Mode Control
  - Constant Current
  - Constant Power
- Configurable Modulation Methods
  - Frequency Modulation
  - Phase Shift Modulation
  - Pulse Width Modulation
- Fast, Automatic and Smooth Mode Switching
  - Frequency Modulation and PWM
  - Phase Shift Modulation and PWM
- High Efficiency and Light Load Management
  - Burst Mode
  - Ideal Diode Emulation
  - Synchronous Rectifier Soft On/Off
  - Low IC Standby Power
- Soft Start / Stop with and without Pre-bias
- Fast Input Voltage Feed Forward Hardware
- Primary Side Voltage Sensing
- Copper Trace Current Sensing
- Flux and Phase Current Balancing for Non-Peak Current Mode Control Applications
- Current Share Bus Support
  - Analog Average
  - Master/Slave
- Feature Rich Fault Protection Options
  - 7 High Speed Analog Comparators
  - Cycle-by-Cycle Current Limiting
  - Programmable Fault Counting
  - External Fault Inputs
  - 4–10 Digital Comparators
  - Programmable blanking time
- Synchronization of DPWM waveforms between multiple UCD313x devices
- 14 channel, 12 bit, 265 ksps General Purpose ADC with integrated
  - Programmable averaging filters
  - Dual sample and hold
- Internal Temperature Sensor
- Fully Programmable High-Performance 31.25MHz, 32-bit ARM7TDMI-S Processor
  - 32 kByte (kB) Program Flash
  - 2 kB Data Flash with ECC
  - 4 kB Data RAM
  - 4 kB Boot ROM Enables Firmware Boot-Load in the Field via $I^2C$ or UART
- Communication Peripherals
  - $I^2C$/PMBus
  - 2 UARTs
- JTAG Debug Port
- Timer capture with selectable input pins
- Up to 5 Additional General Purpose Timers
- Built In Watchdog: BOD and POR
- 64-pin QFN and 40-pin QFN packages
- Operating Temperature: –40°C to 125°C
- Fusion Digital Power GUI Support

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### 1.2 Applications

- **Power Supplies and Telecom Rectifiers**
- **Power Factor Correction**
- **Isolated dc-dc Modules**

## 2 Overview

### 2.1 Description

The UCD3138 is a digital power supply controller from Texas Instruments offering superior levels of integration and performance in a single chip solution. The flexible nature of the UCD3138 makes it suitable for a wide variety of power conversion applications. In addition, multiple peripherals inside the device have been specifically optimized to enhance the performance of ac/dc and isolated dc/dc applications and reduce the solution component count in the IT and network infrastructure space.

The UCD3138 is a fully programmable solution offering customers complete control of their application, along with ample ability to differentiate their solution. At the same time, TI is committed to simplifying our customer's development effort through offering best in class development tools, including application firmware, Code Composer Studio™ software development environment, and TI's Fusion Power Development GUI which enables customers to configure and monitor key system parameters.

At the core of the UCD3138 controller are the digital control loop peripherals, also known as Fusion Digital Power Peripherals (FDPP). Each FDPP implements a high speed digital control loop consisting of a dedicated Error Analog to Digital Converter (EADC), a PID based 2 pole–2 zero digital compensator and DPWM outputs with 250 ps pulse width resolution. The device also contains a 12-bit, 265ksps general purpose ADC with up to 14 channels, timers, interrupt control, JTAG debug and PMBus and UART communications ports. The device is based on a 32-bit ARM7TDMI-S RISC microcontroller that performs real-time monitoring, configures peripherals and manages communications. The ARM microcontroller executes its program out of programmable flash memory as well as on-chip RAM and ROM.

In addition to the FDPP, specific power management peripherals have been added to enable high efficiency across the entire operating range, high integration for increased power density, reliability, and lowest overall system cost and high flexibility with support for the widest number of control schemes and topologies. Such peripherals include: light load burst mode, synchronous rectification, LLC and phase shifted full bridge mode switching, input voltage feed forward, copper trace current sense, ideal diode emulation, constant current constant power control, synchronous rectification soft on and off, peak current mode control, flux balancing, secondary side input voltage sensing, high resolution current sharing, hardware configurable soft start with pre bias, as well as several other features. Topology support has been optimized for voltage mode and peak current mode controlled phase shifted full bridge, single and dual phase PFC, bridgeless PFC, hard switched full bridge and half bridge, and LLC half bridge and full bridge.

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## 2.2 Ordering Information

| PART NUMBER | PIN COUNT | PACKAGE | SUPPLY | TOP SIDE MARKING | OPERATING TEMPERATURE RANGE, $T_A$ |
|---|---|---|---|---|---|
| UCD3138RGCT | 64 | QFN | 250 (Small Reel) | UCD3138 | –40°C to 125°C |
| UCD3138RGCR | 64 | QFN | 2000 (Large Reel) | UCD3138 | –40°C to 125°C |
| UCD3138RHAT | 40 | QFN | 250 (Small Reel) | UCD3138 | –40°C to 125°C |
| UCD3138RHAR | 40 | QFN | 2500 (large Reel) | UCD3138 | –40°C to 125°C |

## 2.3 Product Selection Matrix

| FEATURE | UCD3138 64 PIN | UCD3138 40 PIN |
|---|---|---|
| ARM7TDMI-S Core Processor | 31.25 MHz | 31.25 MHz |
| High Resolution DPWM Outputs (250ps Resolution) | 8 | 8 |
| Number of High Speed Independent Feedback Loops (# Regulated Output Voltages) | 3 | 3 |
| 12-bit, 265ksps, General Purpose ADC Channels | 14 | 7 |
| Digital Comparators at ADC Outputs | 4 | 4 |
| Flash Memory (Program) | 32 KB | 32 KB |
| Flash Memory (Data) | 2 KB | 2 KB |
| Flash Security | √ | √ |
| RAM | 4KB | 4 KB |
| DPWM Switching Frequency | up to 2 MHz | up to 2 MHz |
| Programmable Fault Inputs | 4 | 1 + 2(1) |
| High Speed Analog Comparators with Cycle-by-Cycle Current Limiting | 7(2) | 6(2) |
| UART (SCI) | 2 | 1 + 1(1) |
| PMBus | √ | √ |
| Timers | 4 (16 bit) and 1 (24 bit) | 4 (16 bit) and 1 (24 bit) |
| Timer PWM Outputs | 2 | 1 |
| Timer Capture Inputs | 1 | 1(1) |
| Watchdog | √ | √ |
| On Chip Oscillator | √ | √ |
| Power-On Reset and Brown-Out Reset | √ | √ |
| JTAG | √ | √ |
| Package Offering | 64 Pin QFN (9mm x 9mm) | 40 Pin QFN (6mm x 6mm) |
| Internal Reference (Tolerance) | ±1% | ±1% |
| Sync IN and Sync OUT Functions | √ | √ |
| Total GPIO (includes all pins with multiplexed functions such as, DPWM, Fault Inputs, SCI, etc.) | 30 | 17 |
| External Interrupts | 1 | 0 |

(1) This number represents an alternate pin out that is programmable via firmware. See the Peripherals Programming manual for details.
(2) To facilitate simple OVP and UVP connections both comparators B and C are connected to the AD03 pin.


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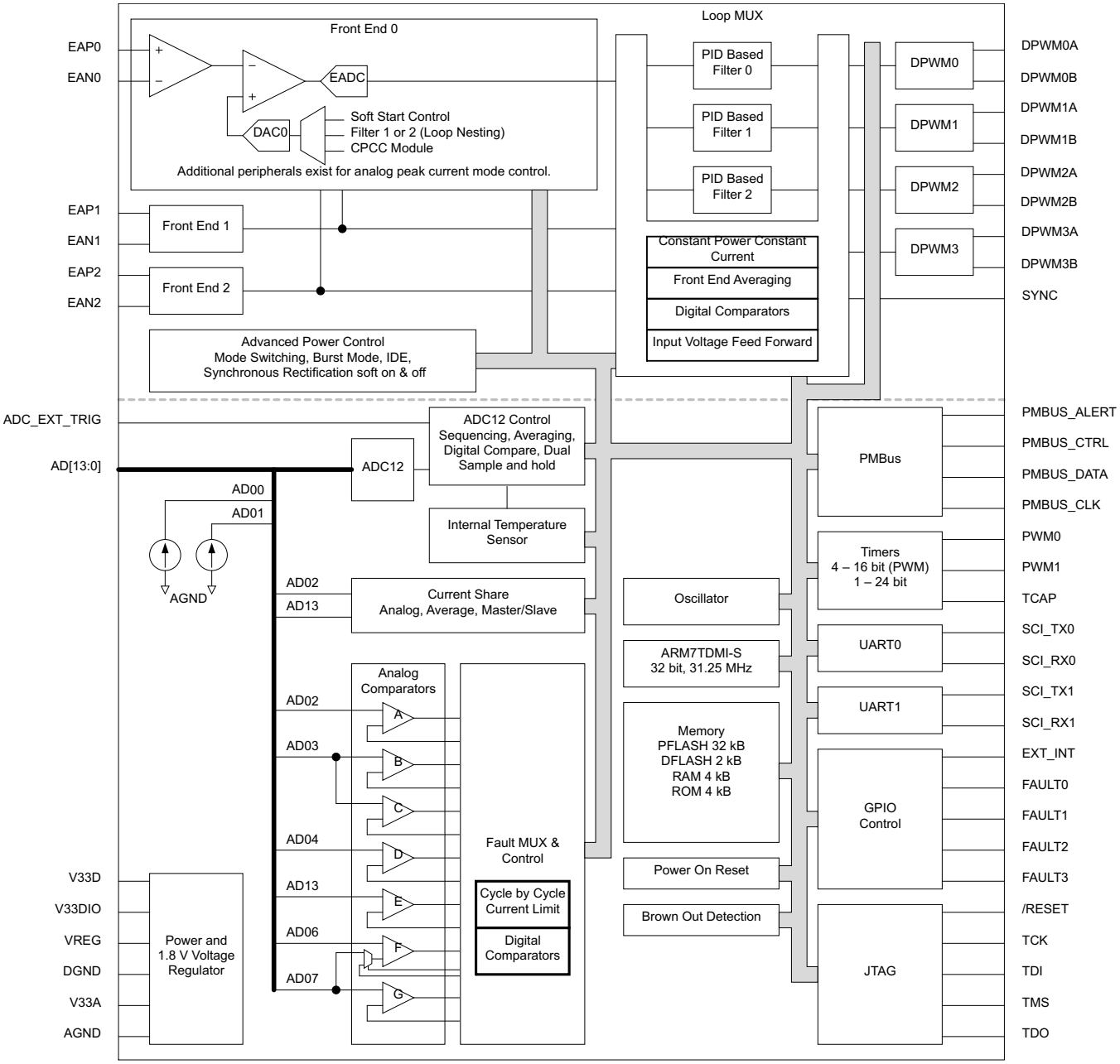
## 2.4 Functional Block Diagram

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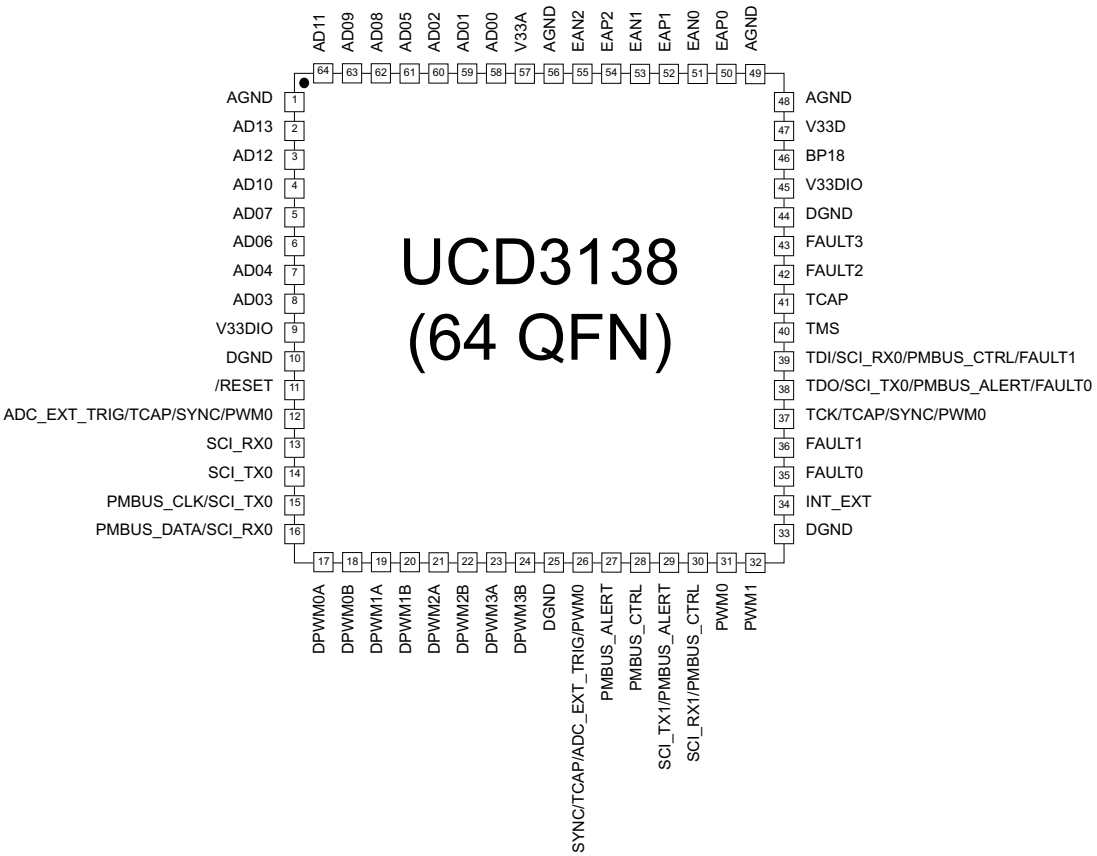
## 2.5 UCD3138 64 QFN – Pin Assignments





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## 2.6 Pin Functions

Additional pin functionality is specified in the following table.

**Table 2-1. Pin Functions**

| PIN | NAME | PRIMARY ASSIGNMENT | ALTERNATE ASSIGNMENT | | | CONFIGURABLE AS A GPIO? |
|---|---|---|---|---|---|---|
| | | | NO. 1 | NO. 2 | NO. 3 | |
| 1 | AGND | Analog ground | | | | |
| 2 | AD13 | 12-bit ADC, Ch 13, comparator E, I-share | | | | |
| 3 | AD12 | 12-bit ADC, Ch 12 | | | | |
| 4 | AD10 | 12-bit ADC, Ch 10 | | | | |
| 5 | AD07 | 12-bit ADC, Ch 7, Connected to comparator G | | | | |
| 6 | AD06 | 12-bit ADC, Ch 6, Connected to comparator F | | | | |
| 7 | AD04 | 12-bit ADC, Ch 4, Connected to comparator D | | | | |
| 8 | AD03 | 12-bit ADC, Ch 3, Connected to comparator B & C | | | | |
| 9 | V33DIO | Digital I/O 3.3V core supply | | | | |
| 10 | DGND | Digital ground | | | | |
| 11 | $\overline{\text{RESET}}$ | Device Reset Input, active low | | | | |
| 12 | ADC_EXT_TRIG | ADC conversion external trigger input | TCAP | SYNC | PWM0 | Yes |
| 13 | SCI_RX0 | SCI RX 0 | | | | Yes |
| 14 | SCI_TX0 | SCI TX 0 | | | | Yes |
| 15 | PMBUS_CLK | PMBUS Clock (Open Drain) | SCI TX 0 | | | Yes |
| 16 | PMBUS_DATA | PMBus data (Open Drain) | SCI RX 0 | | | Yes |
| 17 | DPWM0A | DPWM 0A output | | | | Yes |
| 18 | DPWM0B | DPWM 0B output | | | | Yes |
| 19 | DPWM1A | DPWM 1A output | | | | Yes |
| 20 | DPWM1B | DPWM 1B output | | | | Yes |
| 21 | DPWM2A | DPWM 2A output | | | | Yes |
| 22 | DPWM2B | DPWM 2B output | | | | Yes |
| 23 | DPWM3A | DPWM 3A output | | | | Yes |
| 24 | DPWM3B | DPWM 3B output | | | | Yes |
| 25 | DGND | Digital ground | | | | |
| 26 | SYNC | DPWM Synchronize pin | TCAP | ADC_EXT_TRIG | PWM0 | Yes |
| 27 | PMBUS_ALERT | PMBus Alert (Open Drain) | | | | Yes |
| 28 | PMBUS_CTRL | PMBus Control (Open Drain) | | | | Yes |
| 29 | SCI_TX1 | SCI TX 1 | PMBUS_ALERT | | | Yes |
| 30 | SCI_RX1 | SCI RX 1 | PMBUS_CTRL | | | Yes |
| 31 | PWM0 | General purpose PWM 0 | | | | Yes |
| 32 | PWM1 | General purpose PWM 1 | | | | Yes |
| 33 | DGND | Digital ground | | | | |
| 34 | INT_EXT | External Interrupt | | | | Yes |
| 35 | FAULT0 | External fault input 0 | | | | Yes |
| 36 | FAULT1 | External fault input 1 | | | | Yes |
| 37 | TCK | JTAG TCK | TCAP | SYNC | PWM0 | Yes |
| 38 | TDO | JTAG TDO | SCI_TX0 | PMBUS_ALERT | FAULT0 | Yes |
| 39 | TDI | JTAG TDI | SCI_RX0 | PMBUS_CTRL | FAULT1 | Yes |
| 40 | TMS | JTAG TMS | | | | Yes |
| 41 | TCAP | Timer capture input | | | | Yes |
| 42 | FAULT2 | External fault input 2 | | | | Yes |
| 43 | FAULT3 | External fault input 3 | | | | Yes |

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**Table 2-1. Pin Functions (continued)**

| PIN | NAME | PRIMARY ASSIGNMENT | ALTERNATE ASSIGNMENT | | | CONFIGURABLE AS A GPIO? |
|---|---|---|---|---|---|---|
| | | | NO. 1 | NO. 2 | NO. 3 | |
| 44 | DGND | Digital ground | | | | |
| 45 | V33DIO | Digital I/O 3.3V core supply | | | | |
| 46 | BP18 | 1.8V Bypass | | | | |
| 47 | V33D | Digital 3.3V core supply | | | | |
| 48 | AGND | Substrate analog ground | | | | |
| 49 | AGND | Analog ground | | | | |
| 50 | EAP0 | Channel #0, differential analog voltage, positive input | | | | |
| 51 | EAN0 | Channel #0, differential analog voltage, negative input | | | | |
| 52 | EAP1 | Channel #1, differential analog voltage, positive input | | | | |
| 53 | EAN1 | Channel #1, differential analog voltage, negative input | | | | |
| 54 | EAP2 | Channel #2, differential analog voltage, positive input | | | | |
| 55 | EAN2 | Channel #2, differential analog voltage, negative input | | | | |
| 56 | AGND | Analog ground | | | | |
| 57 | V33A | Analog 3.3V supply | | | | |
| 58 | AD00 | 12-bit ADC, Ch 0, Connected to current source | | | | |
| 59 | AD01 | 12-bit ADC, Ch 1, Connected to current source | | | | |
| 60 | AD02 | 12-bit ADC, Ch 2, Connected to comparator A, I-share | | | | |
| 61 | AD05 | 12-bit ADC, Ch 5 | | | | |
| 62 | AD08 | 12-bit ADC, Ch 8 | | | | |
| 63 | AD09 | 12-bit ADC, Ch 9 | | | | |
| 64 | AD11 | 12-bit ADC, Ch 11 | | | | |


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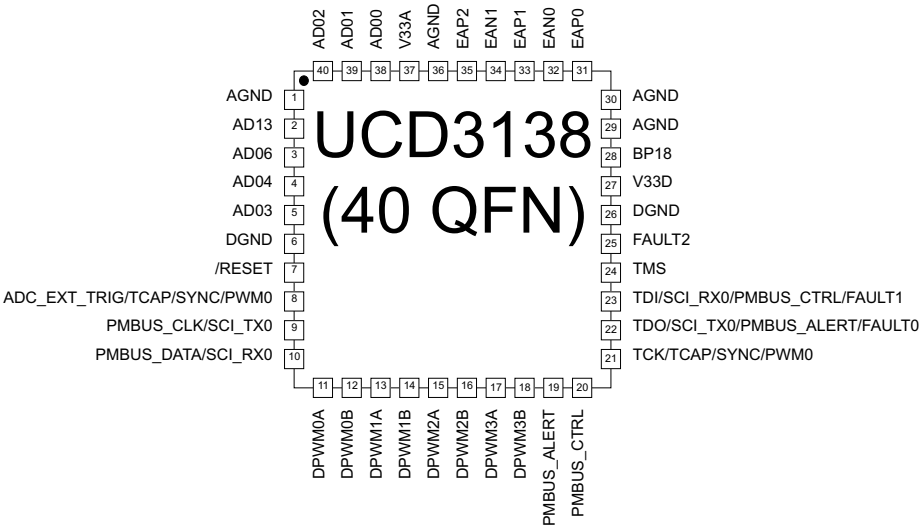
## 2.7 UCD3138 40 QFN – Pin Assignments



## 2.8 Pin Functions

Additional pin functionality is specified in the following table.

**Table 2-2. Pin Functions**

| PIN | NAME | PRIMARY ASSIGNMENT | ALTERNATE ASSIGNMENT | | | CONFIGURABLE AS A GPIO? |
|---|---|---|---|---|---|---|
| | | | NO. 1 | NO. 2 | NO. 3 | |
| 1 | AGND | Analog ground | | | | |
| 2 | AD13 | 12-bit ADC, Ch 13, Connected to comparator E, I-share | | | | |
| 3 | AD06 | 12-bit ADC, Ch 6, Connected to comparator F | | | | |
| 4 | AD04 | 12-bit ADC, Ch 4, Connected to comparator D | | | | |
| 5 | AD03 | 12-bit ADC, Ch 3, Connected to comparator B & C | | | | |
| 6 | DGND | Digital ground | | | | |
| 7 | $\overline{\text{RESET}}$ | Device Reset Input, active low | | | | |
| 8 | ADC_EXT_TRIG | ADC conversion external trigger input | TCAP | SYNC | PWM0 | Yes |
| 9 | PMBUS_CLK | PMBUS Clock (Open Drain) | SCI_TX0 | | | Yes |
| 10 | PMBUS_DATA | PMBus data (Open Drain) | SCI_RX0 | | | Yes |
| 11 | DPWM0A | DPWM 0A output | | | | Yes |
| 12 | DPWM0B | DPWM 0B output | | | | Yes |
| 13 | DPWM1A | DPWM 1A output | | | | Yes |
| 14 | DPWM1B | DPWM 1B output | | | | Yes |
| 15 | DPWM2A | DPWM 2A output | | | | Yes |
| 16 | DPWM2B | DPWM 2B output | | | | Yes |
| 17 | DWPM3A | DPWM 3A output | | | | Yes |
| 18 | DPWM3B | DPWM 3B output | | | | Yes |
| 19 | PMBUS_ALERT | PMBus Alert (Open Drain) | | | | Yes |
| 20 | PMBUS_CTRL | PMBus Control (Open Drain) | | | | Yes |
| 21 | TCK | JTAG TCK | TCAP | SYNC | PWM0 | Yes |
| 22 | TDO | JTAG TDO | SCI_TX0 | PMBUS_ALERT | FAULT0 | Yes |
| 23 | TDI | JTAG TDI | SCI_RX0 | PMBUS_CTRL | FAULT1 | Yes |
| 24 | TMS | JTAG TMS | | | | Yes |
| 25 | FAULT2 | External fault input 2 | | | | Yes |
| 26 | DGND | Digital ground | | | | |
| 27 | V33D | Digital 3.3V core supply | | | | |
| 28 | BP18 | 1.8V Bypass | | | | |
| 29 | AGND | Substrate analog ground | | | | |
| 30 | AGND | Analog ground | | | | |
| 31 | EAP0 | Channel #0, differential analog voltage, positive input | | | | |
| 32 | EAN0 | Channel #0, differential analog voltage, negative input | | | | |
| 33 | EAP1 | Channel #1, differential analog voltage, positive input | | | | |
| 34 | EAN1 | Channel #1, differential analog voltage, negative input | | | | |
| 35 | EAP2 | Channel #2, differential analog voltage, positive input | | | | |
| 36 | AGND | Analog ground | | | | |
| 37 | V33A | Analog 3.3V supply | | | | |
| 38 | AD00 | 12-bit ADC, Ch 0, Connected to current source | | | | |
| 39 | AD01 | 12-bit ADC, Ch 1, Connected to current source | | | | |
| 40 | AD02 | 12-bit ADC, Ch 2, Connected to comparator A, I-share | | | | |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# 3 Electrical Specifications

## 3.1 ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range (unless otherwise noted)

| | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| V33D | V33D to DGND | –0.3 | 3.8 | V |
| V33DIO | V33DIO to DGND | –0.3 | 3.8 | V |
| V33A | V33A to AGND | –0.3 | 3.8 | V |
| \|DGND – AGND\| | Ground difference | 0.3 | | V |
| All Pins (2) | Voltage applied to any pin | –0.3 | 3.8 | V |
| $T_{OPT}$ | Junction Temperature | –40 | 125 | °C |
| $T_{STG}$ | Storage temperature | –55 | 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Referenced to DGND

## 3.2 THERMAL INFORMATION

| THERMAL METRIC | | UCD3138 64 PIN QFN | UCD3138 40 PIN QFN | UNITS |
|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 25.1 | 31.8 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 10.5 | 18.5 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 4.6 | 6.8 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | 0.2 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 4.6 | 6.7 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 1.2 | 1.8 | |

## 3.3 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| V33D | Digital power | 3.0 | 3.3 | 3.6 | V |
| V33DIO | Digital I/O power | 3.0 | 3.3 | 3.6 | |
| V33A | Analog power | 3.0 | 3.3 | 3.6 | V |
| $T_J$ | Junction temperature | -40 | - | 125 | °C |

## 3.4 ELECTRICAL CHARACTERISTICS

V33A = V33D = V33DIO = 3.3V; 1µF from VREG to DGND, $T_J$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | |
| I33A | | | 6.3 | | mA |
| I33DIO | All GPIO and communication pins are open | | 0.35 | | mA |
| I33D | ROM program execution | | 60 | | mA |
| I33D | Flash programming in ROM mode | | | 70 | mA |
| I33 | Total supply current with all peripherals operating. | | | 100 | mA |

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## ELECTRICAL CHARACTERISTICS *(continued)*

V33A = V33D = V33DIO = 3.3V; 1µF from VREG to DGND, $T_J$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ERROR ADC INPUTS EAP, EAN** | | | | | | |
| | EAP-AGND | | –0.15 | | 1.998 | V |
| | EAP-EAN | | -0.256 | | 1.848 | V |
| | Error range | AFE = 0 | –256 | | 248 | mV |
| | EAP-EAN Error voltage digital resolution | AFE = 3 | 0.95 | 1 | 1.20 | mV |
| | | AFE = 2 | 1.90 | 2 | 2.30 | mV |
| | | AFE = 1 | 3.72 | 4 | 4.45 | mV |
| | | AFE = 0 | 7.3 | 8 | 9.10 | mV |
| $R_{EA}$ | Input impedance | AGND reference | 0.5 | | | MΩ |
| $I_{OFFSET}$ | Input offset current | | –5 | | 5 | µA |
| | EADC Offset | Input voltage = 0 V at AFE = 0 | –2 | | 2 | LSB |
| | | Input voltage = 0 V at AFE = 1 | -2.5 | | 2.5 | LSB |
| | | Input voltage = 0 V at AFE = 2 | -3 | | -3 | LSB |
| | | Input voltage = 0 V at AFE = 3 | -4 | | 4 | LSB |
| | Sample Rate | | | | 16 | MHz |
| | Analog Frond End Amplifier Bandwidth | | | 100 | | MHz |
| $A_0$ | Gain | | | 1 | | V/V |
| | Minimum output voltage | | | | 100 | mV |
| **EADC DAC** | | | | | | |
| | DAC range | | 0 | | 1.6 | V |
| | VREF DAC reference resolution | 10 bit, No dithering enabled | | 1.56 | | mV |
| | VREF DAC reference resolution | With 4 bit dithering enabled | | 97.6 | | µV |
| | INL | | –3.0 | | 3.0 | LSB |
| | DNL | Does not include MSB transition | –2.1 | | 1.6 | LSB |
| | DNL at MSB transition | | | -1.4 | | LSB |
| | DAC reference voltage | | 1.58 | | 1.61 | V |
| τ | Settling Time | From 10% to 90% | | 250 | | ns |
| **ADC12** | | | | | | |
| $I_{BIAS}$ | Bias current for PMBus address pins | | 9.5 | | 10.5 | µA |
| | Measurement range for voltage monitoring | | 0 | | 2.5 | V |
| | Internal ADC reference voltage | –40°C to 125°C | 2.475 | 2.500 | 2.525 | V |
| | Internal ADC reference from 25°C reference voltage(1) | 25°C to –40°C | | -0.4 | | mV |
| | | 25°C to 85°C | | -1.8 | | |
| | | 25°C to 125°C | | -4.2 | | |
| | ADC12 INL integral nonlinearity(1) | ADC_SAMPLINGSEL = 6 for all ADC12 data, 25 °C to 125 °C | | +/-2.5 | | LSB |
| | ADC12 DNL differential nonlinearity(1) | | | -0.7/+2.5 | | LSB |
| | ADC Zero Scale Error | | -4 | | 4 | mV |
| | ADC Full Scale Error | | -35 | | 35 | mV |
| | Input bias | 2.5 V applied to pin | | | 400 | nA |
| | Input leakage resistance | | | 1 | | MΩ |
| | Input Capacitance | | | 10 | | pF |
| | ADC single sample conversion time | | | 3.9 | | µs |

(1) As designed and characterized. Not 100% tested in production.


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## ELECTRICAL CHARACTERISTICS *(continued)*

V33A = V33D = V33DIO = 3.3V; 1µF from VREG to DGND, $T_J$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DIGITAL INPUTS/OUTPUTS (2) (3)** | | | | | | |
| $V_{OL}$ | Low-level output voltage (4) | $I_{OH}$ = 6 mA, V33DIO = 3 V | | DGND + 0.25 | | V |
| $V_{OH}$ | High-level output voltage (4) | $I_{OH}$ = –6 mA, V33DIO = 3 V | V33DIO – 0.6 | | | V |
| $V_{IH}$ | High-level input voltage | V33DIO = 3 V | 2.1 | | | V |
| $V_{IL}$ | Low-level input voltage | V33DIO = 3 V | | | 1.1 | V |
| $I_{OH}$ | Output sinking current | | | | 4 | mA |
| $I_{OL}$ | Output sourcing current | | -4 | | | mA |
| **SYSTEM PERFORMANCE** | | | | | | |
| | Time to disable DPWM output based on active FAULT pin signal | High level on FAULT pin | | 70 | | ns |
| | Processor master clock (MCLK) | | | 31.25 | | MHz |
| $t_{Delay}$ | Digital compensator delay (5) | (1 clock = 32ns) | 6 | | | clocks |
| $V_{DD}$ | Slew minimum VDD slew rate | VDD slew rate between 2.3 V and 2.9 V | 0.25 | | | V/ms |
| $t_{(reset)}$ | Pulse width needed at reset | | 10 | | | µs |
| | Retention period of flash content (data retention and program) | $T_J$ = 25°C | 100 | | | years |
| | Program time to erase one page in data flash or program flash | $T_J$ = 25°C | | 20 | | ms |
| | Program time to write one word n data flash or program flash | $T_J$ = 25°C | | 25 | | µs |
| $f_{(PCLK)}$ | Internal oscillator frequency | | 240 | 250 | 260 | MHz |
| | Sync-in/sync-out pulse width | | | 256 | | ns |
| | Flash Read | | | 1 | | MCLKs |
| | Flash Write | | | 30 | | µs |
| | Block Erase | | | 20 | | ms |
| $I_{SHARE}$ | Current share current source | | 238 | | 259 | µA |
| $R_{SHARE}$ | Current share resistor | | 9.75 | | 10.3 | kΩ |
| **POWER ON RESET AND BROWN OUT** | | | | | | |
| VGH | | Voltage good High | | 2.7 | | V |
| VGL | | Voltage good Low | | 2.5 | | V |
| $V_{res}$ | | Voltage at which IReset signal is valid | | 0.8 | | V |
| $T_{POR}$ | | Time delay after Power is good or RESET* relinquished | | 1 | | ms |
| | Brownout | Internal signal warning of brownout conditions | | 2.9 | | V |
| **TEMPERATURE SENSOR (6)** | | | | | | |
| $V_{TEMP}$ | | Voltage range of sensor | 1.46 | | 2.44 | V |
| | Voltage resolution | Volts/°C | | 5.9 | | mV/ºC |
| | Temperature resolution | Degree C per bit | | 0.7 | | ºC/LSB |
| | Accuracy (6) (7) | -40°C to 125°C | -10 | ±5 | 10 | ºC |
| | Temperature range | -40°C to 125°C | –40 | | 125 | ºC |

(2) DPWM outputs are low after reset. Other GPIO pins are configured as inputs after reset.
(3) On the 40 pin package V33DIO is connected to V33D internally.
(4) The maximum total current, IOHmax and IOLmax for all outputs combined, should not exceed 12 mA to hold the maximum voltage drop specified. Maximum sink current per pin = –6 mA at $V_{OL}$; maximum source current per pin = 6 mA at $V_{OH}$.
(5) Time from close of error ADC sample window to time when digitally calculated control effort (duty cycle) is available. This delay must be accounted for when calculating the system dynamic response.
(6) Characterized by design and not production tested.
(7) Ambient temperature offset value should be used from the TEMPSENCTRL register to meet accuracy.

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## ELECTRICAL CHARACTERISTICS *(continued)*

V33A = V33D = V33DIO = 3.3V; 1µF from VREG to DGND, $T_J$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{TEMP}$ | | Current draw of sensor when active | | 30 | | µA |
| $T_{ON}$ | | Turn on time / settling time of sensor | | 100 | | µs |
| $V_{AMB}$ | Ambient temperature | Trimmed 25°C reading | | 1.85 | | V |
| **ANALOG COMPARATOR** | | | | | | |
| DAC | Reference DAC Range | | 0 | | 2.5 | V |
| | Reference Voltage | | 2.478 | 2.5 | 2.513 | V |
| | Bits | | | 7 | | bits |
| | INL (6) | | -0.42 | | 0.21 | LSB |
| | DNL (6) | | 0.06 | | 0.12 | LSB |
| | Offset | | -5.5 | | 19.5 | mV |
| | Time to disable DPWM output based on 0 V to 2.5 V step input on the analog comparator. (8) | | | | 150 | ns |
| | Reference DAC buffered output load (9) | | 0.5 | | 1 | mA |
| | Buffer offset (-0.5 mA) | | 4.6 | | 8.3 | mV |
| | Buffer offset (1.0 mA) | | -0.05 | | 17 | mV |

(8) As designed and characterized. Not 100% tested in production.
(9) Available from reference DACs for comparators D, E, F and G.


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## 3.5 PMBus/SMBus/I²C Timing

The timing characteristics and timing diagram for the communications interface that supports I²C, SMBus, and PMBus in Slave or Master mode are shown in Table 3-1, Figure 3-1, and Figure 3-2. The numbers in Table 3-1 are for 400 kHz operating frequency. However, the device supports all three speeds, standard (100 kHz), fast (400 kHz), and fast mode plus (1 MHz).

**Table 3-1. I²C/SMBus/PMBus Timing Characteristics**

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Typical values at $T_A$ = 25°C and VCC = 3.3 V (unless otherwise noted) | | | | | | |
| $f_{SMB}$ | SMBus/PMBus operating frequency | Slave mode, SMBC 50% duty cycle | | 10 | 400 | kHz |
| $f_{I2C}$ | I²C operating frequency | Slave mode, SCL 50% duty cycle | | 10 | 400 | kHz |
| $t_{(BUF)}$ | Bus free time between start and stop | | | 1.3 | | ms |
| $t_{(HD:STA)}$ | Hold time after (repeated) start | | | 0.6 | | ms |
| $t_{(SU:STA)}$ | Repeated start setup time | | | 0.6 | | ms |
| $t_{(SU:STO)}$ | Stop setup time | | | 0.6 | | ms |
| $t_{(HD:DAT)}$ | Data hold time | Receive mode | | 0 | | ns |
| $t_{(SU:DAT)}$ | Data setup time | | | 100 | | ns |
| $t_{(TIMEOUT)}$ | Error signal/detect (1) | | | | 35 | ms |
| $t_{(LOW)}$ | Clock low period | | | 1.3 | | ms |
| $t_{(HIGH)}$ | Clock high period (2) | | | 0.6 | | ms |
| $t_{(LOW:SEXT)}$ | Cumulative clock low slave extend time (3) | | | | 25 | ms |
| $t_f$ | Clock/data fall time | Rise time $t_r$ = ($V_{ILmax}$ – 0.15) to ($V_{IHmin}$ + 0.15) | 20 + 0.1 Cb (4) | | 300 | ns |
| $t_r$ | Clock/data rise time | Fall time $t_f$ = 0.9 VDD to ($V_{ILmax}$ – 0.15) | 20 + 0.1 Cb (4) | | 300 | ns |
| $C_b$ | Total capacitance of one bus line | | | | 400 | pF |

(1) The device times out when any clock low exceeds $t_{(TIMEOUT)}$.
(2) t(HIGH), Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0] = 0).
(3) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) $C_b$ (pF)

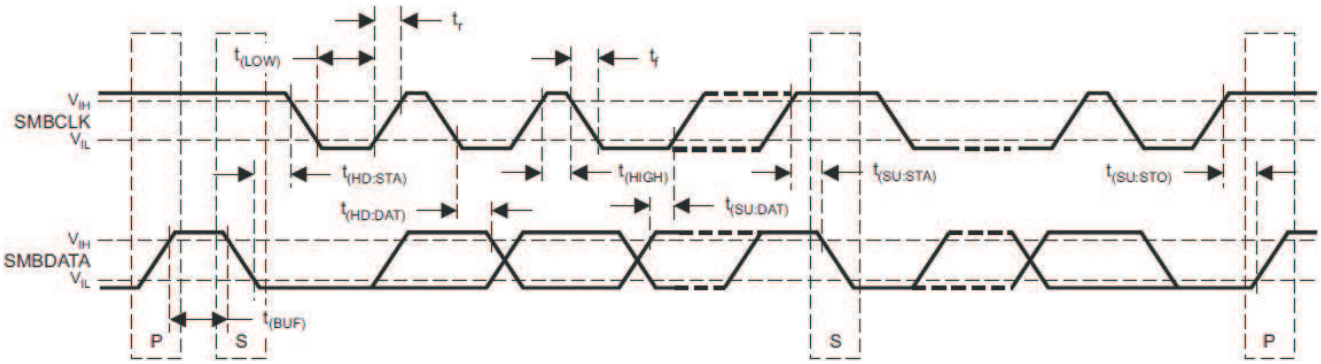


**Figure 3-1. I²C/SMBus/PMBus Timing Diagram**

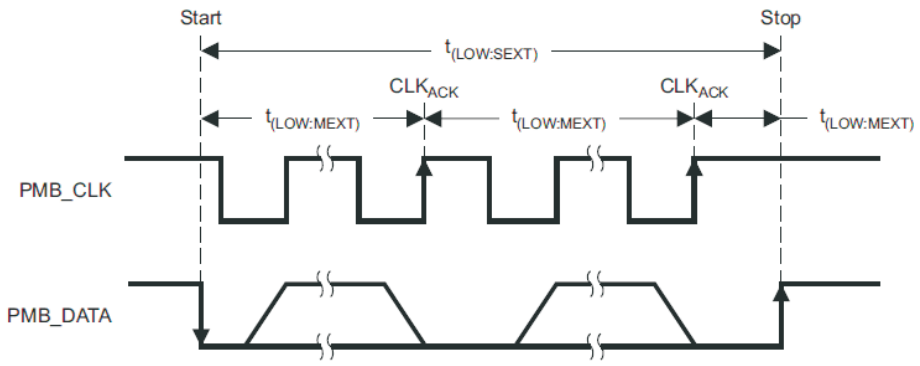


**Figure 3-2. Bus timing in Extended Mode**

## 3.6 Power On Reset (POR) / Brown Out Reset (BOR)

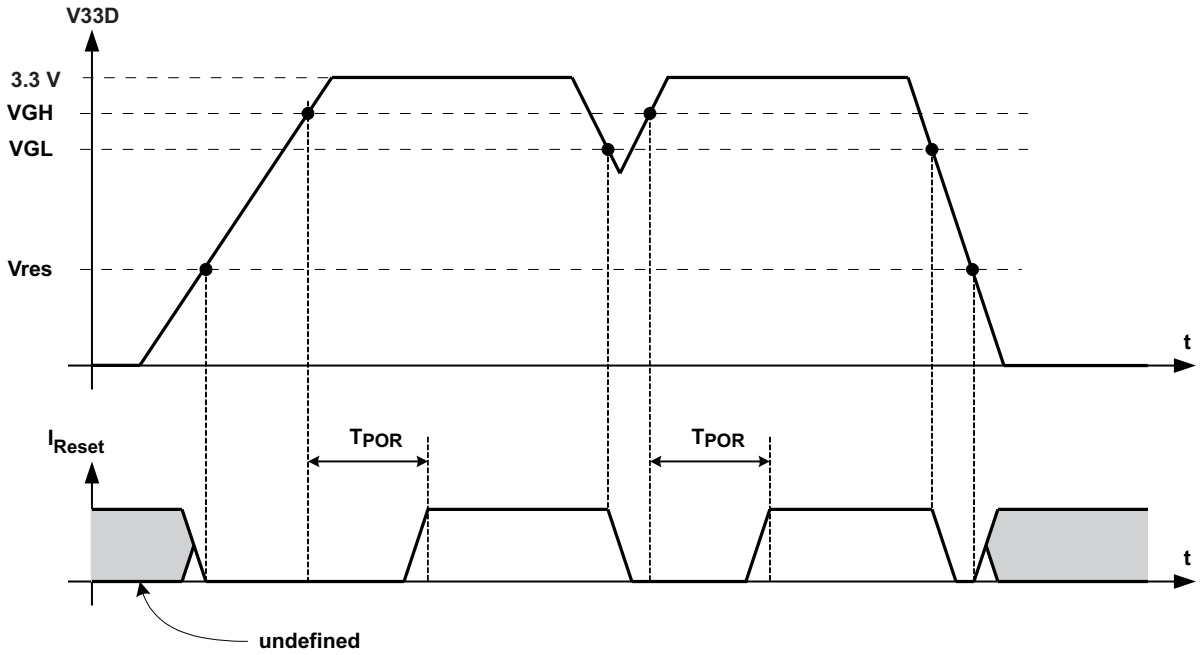


**Figure 3-3. Power On Reset (POR) / Brown Out Reset (BOR)**

VGH – This is the V33D threshold where the internal power is declared good. The UCD3138 comes out of reset when above this threshold.

VGL – This is the V33D threshold where the internal power is declared bad. The device goes into reset when below this threshold.

$V_{res}$ – This is the V33D threshold where the internal reset signal is no longer valid. Below this threshold the device is in an indeterminate state.

$I_{Reset}$ – This is the internal reset signal. When low, the device is held in reset. This is equivalent to holding the reset pin on the IC high.

$T_{POR}$ – The time delay from when VGH is exceeded to when the device comes out of reset.


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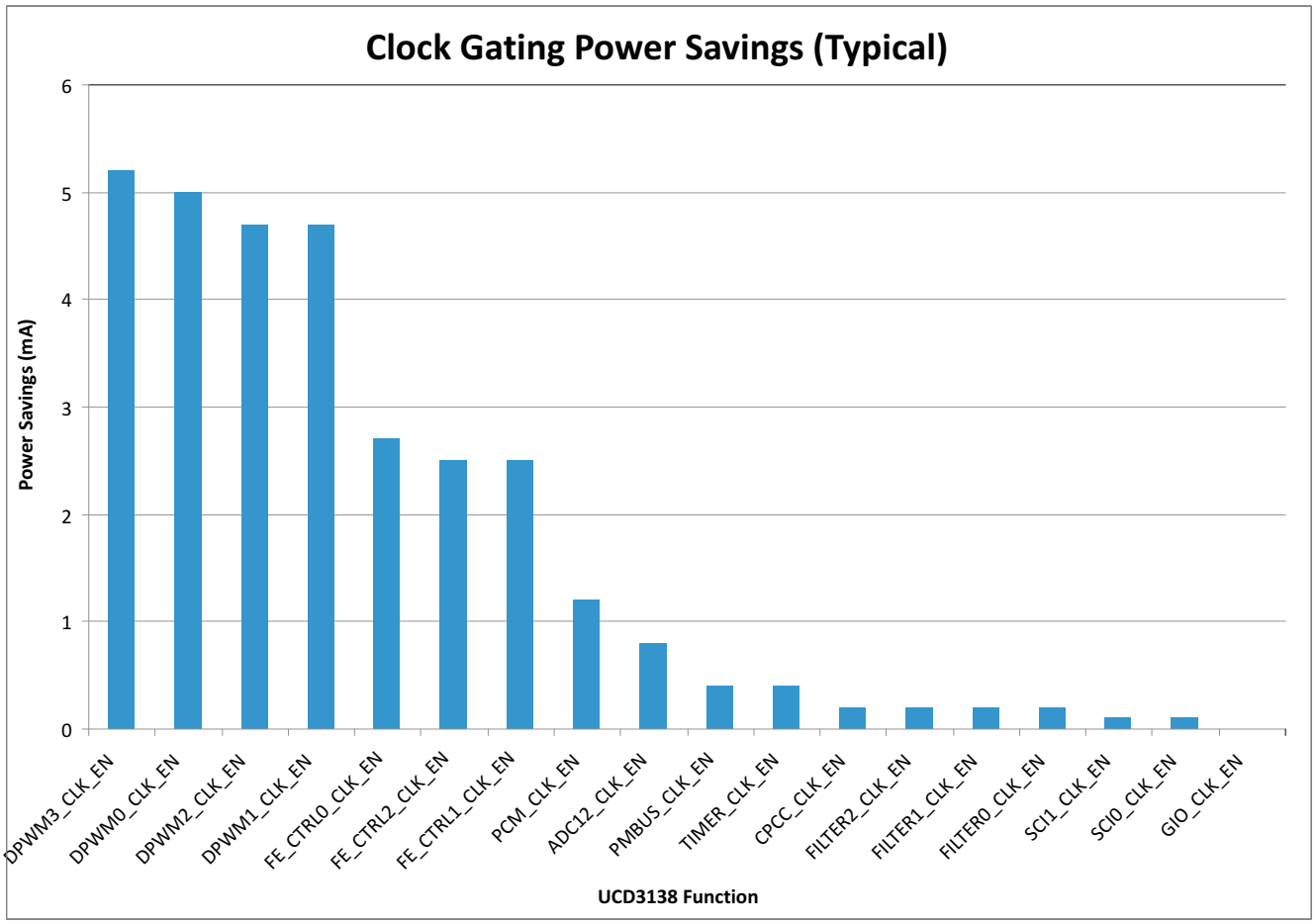
## 3.7 Typical Clock Gating Power Savings



# 4 Functional Overview

## 4.1 ARM Processor

The ARM7TDMI-S processor is a synthesizable member of the ARM family of general purpose 32-bit microprocessors. The ARM architecture is based on RISC (Reduced Instruction Set Computer) principles where two instruction sets are available. The 32-bit ARM instruction set and the 16-bit Thumb instruction set. The Thumb instruction allows for higher code density equivalent to a 16-bit microprocessor, with the performance of the 32-bit microprocessor.

The three-staged pipelined ARM processor has fetch, decode and execute stage architecture. Major blocks in the ARM processor include a 32-bit ALU, 32 x 8 multiplier, and a barrel shifter. A JTAG port is also available for firmware debugging.

## 4.2 Memory

The UCD31xx (ARM7TDMI-S) is a Von-Neumann architecture, where a single bus provides access to all of the memory modules. All of the memory module addresses are sequentially aligned along the same address range. This is applies to program flash, data flash, ROM and all other peripherals.

Within the UCD31xx architecture, there is a 1024x32-bit Boot ROM that contains the initial firmware startup routines for PMBUS communication and non-volatile (FLASH) memory download. This boot ROM is executed after power-up-reset checks if there is a valid FLASH program written. If a valid program is present, the ROM code branches to the main FLASH-program execution.

UCD31xx also supports customization of the boot program by allowing an alternative booting routine to be executed from program FLASH. This feature enables assignment of a unique address to each device; therefore, enabling firmware reprogramming even when several devices are connected on the same communication bus.

Two separate FLASH memory areas are present inside the device. The 32 kB Program FLASH is organized as an 8 k x 32 bit memory block and is intended to be for the firmware program. The block is configured with page erase capability for erasing blocks as small as 1kB per page, or with a mass erase for erasing the entire program FLASH array. The FLASH endurance is specified at 1000 erase/write cycles and the data retention is good for 100 years. The 2 kB data FLASH array is organized as a 512 x 32 bit memory (32 byte page size). The Data FLASH is intended for firmware data value storage and data logging. Thus, the Data FLASH is specified as a high endurance memory of 20 k cycles with embedded error correction code (ECC).

For run time data storage and scratchpad memory, a 4 kB RAM is available. The RAM is organized as a 1 k x 32 bit array.

### *4.2.1 CPU Memory Map and Interrupts*

When the device comes out of power-on-reset, the data memories are mapped to the processor as follows:

#### 4.2.1.1 Memory Map (After Reset Operation)

| Address | Size | Module |
|---|---|---|
| 0x0000_0000 – 0x0000_FFFF<br>In 16 repeated blocks of 4K each | 16 X 4K | Boot ROM |
| 0x0001_0000 – 0x0001_7FFF | 32K | Program Flash |
| 0x0001_8800 – 0x0001_8FFF | 2K | Data Flash |
| 0x0001_9000 – 0x0001_9FFF | 4K | Data RAM |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#### 4.2.1.2 Memory Map (Normal Operation)

Just before the boot ROM program gives control to FLASH program, the ROM configures the memory as follows:

| Address | Size | Module |
|---|---|---|
| 0x0000_0000 – 0x0000_7FFF | 32K | Program Flash |
| 0x0001_0000 – 0x0001_AFFF | 4K | Boot ROM |
| 0x0001_8800 – 0x0001_8FFF | 2K | Data Flash |
| 0x0001_9000 – 0x0001_9FFF | 4K | Data RAM |

#### 4.2.1.3 Memory Map (System and Peripherals Blocks)

| Address | Size | Module |
|---|---|---|
| 0x0002_0000 - 0x0002_00FF | 256 | Loop Mux |
| 0x0003_0000 - 0x0003_00FF | 256 | Fault Mux |
| 0x0004_0000 - 0x0004_00FF | 256 | ADC |
| 0x0005_0000 - 0x0005_00FF | 256 | DPWM 3 |
| 0x0006_0000 - 0x0006_00FF | 256 | Filter 2 |
| 0x0007_0000 - 0x0007_00FF | 256 | DPWM 2 |
| 0x0008_0000 - 0x0008_00FF | 256 | Front End/Ramp I/F 2 |
| 0x0009_0000 - 0x0009_00FF | 256 | Filter 1 |
| 0x000A_0000 - 0x000A_00FF | 256 | DPWM 1 |
| 0x000B_0000 – 0x000B_00FF | 256 | Front End/Ramp I/F 1 |
| 0x000C_0000 - 0x000C_00FF | 256 | Filter 0 |
| 0x000D_0000 - 0x000D_00FF | 256 | DPWM 0 |
| 0x000E_0000 - 0x000E_00FF | 256 | Front End/Ramp I/F 0 |
| 0xFFF7_EC00 - 0xFFF7_ECFF | 256 | UART 0 |
| 0xFFF7_ED00 - 0xFFF7_EDFF | 256 | UART 1 |
| 0xFFF7_F000 - 0xFFF7_F0FF | 256 | Miscellaneous Analog Control |
| 0xFFF7_F600 - 0xFFF7_F6FF | 256 | PMBus Interface |
| 0xFFF7_FA00 - 0xFFF7_FAFF | 256 | GIO |
| 0xFFF7_FD00 - 0xFFF7_FDFF | 256 | Timer |
| 0xFFFF_FD00 - 0xFFFF_FDFF | 256 | MMC |
| 0xFFFF_FE00 - 0xFFFF_FEFF | 256 | DEC |
| 0xFFFF_FF20 - 0xFFFF_FF37 | 23 | CIM |
| 0xFFFF_FF40 - 0xFFFF_FF50 | 16 | PSA |
| 0xFFFF_FFD0 - 0xFFFF_FFEC | 28 | SYS |

The registers and bit definitions inside the System and Peripheral blocks are detailed in the programmer's guide for each peripheral.

### *4.2.2 Boot ROM*

The UCD3138 incorporates a 4k boot ROM. This boot ROM includes support for:

- Program download through the PMBus
- Device initialization
- Examining and modifying registers and memory
- Verifying and executing program FLASH automatically
- Jumping to a customer defined boot program

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The Boot ROM is entered automatically on device reset. It initializes the device and then performs checksums on the Program FLASH. If the first 2 kB of program FLASH has a valid checksum, the program jumps to location 0 in the Program FLASH. This permits the use of a customer boot program. If the first checksum fails, it performs a checksum on the complete 32 kB of program flash. If this is valid, it also jumps to location 0 in the program flash. This permits full automated program memory checking, when there is no need for a custom boot program.

If neither checksum is valid, the Boot ROM stays in control, and accepts commands via the PMBus interface

These functions can be used to read and write to all memory locations in the UCD3138. Typically they are used to download a program to Program Flash, and to command its execution

### *4.2.3 Customer Boot Program*

As described above, it is possible to generate a user boot program using 2 kB or more of the Program Flash. This can support things which the Boot ROM does not support, including:

- Program download via UART – useful especially for applications where the UCD3138 is isolated from the host (e.g., PFC)
- Encrypted download – useful for code security in field updates.

### *4.2.4 Flash Management*

The UCD3138 offers a variety of features providing for easy prototyping and easy flash programming. At the same time, high levels of security are possible for production code, even with field updates. Standard firmware will be provided for storing multiple copies of system parameters in data flash. This is minimizes the risk of losing information if programming is interrupted.

## 4.3 System Module

The System Module contains the interface logic and configuration registers to control and configure all the memory, peripherals and interrupt mechanisms. The blocks inside the system module are the address decoder, memory management controller, system management unit, central interrupt unit, and clock control unit.

### *4.3.1 Address Decoder (DEC)*

The Address Decoder generates the memory selects for the FLASH, ROM and RAM arrays. The memory map addresses are selectable through configurable register settings. These memory selects can be configured from 1 kB to 16 MB. Power on reset uses the default addresses in the memory map for ROM execution, which is then configured by the ROM code to the application setup. During access to the DEC registers, a wait state is asserted to the CPU. DEC registers are only writable in the ARM privilege mode for user mode protection.

### *4.3.2 Memory Management Controller (MMC)*

The MMC manages the interface to the peripherals by controlling the interface bus for extending the read and write accesses to each peripheral. The unit generates eight peripheral select lines with 1 kB of address space decoding.

### *4.3.3 System Management (SYS)*

The SYS unit contains the software access protection by configuring user privilege levels to memory or peripherals modules. It contains the ability to generate fault or reset conditions on decoding of illegal address or access conditions. A clock control setup for processor clock (MCLK) speed, is also available.


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### 4.3.4 Central Interrupt Module (CIM)

The CIM accepts 32 interrupt requests for meeting firmware timing requirements. The ARM processor supports two interrupt levels: FIQ and IRQ. FIQ is the highest priority interrupt. The CIM provides hardware expansion of interrupts by use of FIQ/IRQ vector registers for providing the offset index in a vector table. This numerical index value indicates the highest precedence channel with a pending interrupt and is used to locate the interrupt vector address from the interrupt vector table. Interrupt channel 0 has the lowest precedence and interrupt channel 31 has the highest precedence. To remove the interrupt request, the firmware should clear the request as the first action in the interrupt service routine. The request channels are maskable, allowing individual channels to be selectively disabled or enabled.

**Table 4-1. Interrupt Priority Table**

| NAME | MODULE COMPONENT OR REGISTER | DESCRIPTION | PRIORITY |
|---|---|---|---|
| BRN_OUT_INT | Brownout | Brownout interrupt | 0 (Lowest) |
| EXT_INT | External Interrupts | Interrupt on one external input pins for faults inputs | 1 |
| WDRST_INT | Watchdog Control | Interrupt from watchdog exceeded (reset) | 2 |
| WDWAKE_INT | Watchdog Control | Wakeup interrupt when watchdog equals half of set watch time | 3 |
| SCI_ERR_INT | UART or SCI Control | UART or SCI error Interrupt. Frame, parity or overrun | 4 |
| SCI_RX_0_INT | UART or SCI Control | UART0 RX buffer has a byte | 5 |
| SCI_TX_0_INT | UART or SCI Control | UART0 TX buffer empty | 6 |
| SCI_RX_1_INT | UART or SCI Control | UART1 RX buffer has a byte | 7 |
| SCI_TX_1_INT | UART or SCI Control | UART1 TX buffer empty | 8 |
| PMBUS_INT | | PMBus related interrupt | 9 |
| DIG_COMP_INT | 12-bit ADC Control | Digital comparator interrupt | 10 |
| FE0_INT | Front End 0 | “Prebias complete”, “Ramp Delay Complete”, “Ramp Complete”, “Load Step Detected”, “Over-Voltage Detected”, “EADC saturated” | 11 |
| FE1_INT | Front End 1 | “Prebias complete”, “Ramp Delay Complete”, “Ramp Complete”, “Load Step Detected”, “Over-Voltage Detected”, “EADC saturated” | 12 |
| FE2_INT | Front End 2 | “Prebias complete”, “Ramp Delay Complete”, “Ramp Complete”, “Load Step Detected”, “Over-Voltage Detected”, “EADC saturated” | 13 |
| PWM3_INT | 16-bit Timer PWM 3 | 16-bit Timer PWM3 counter overflow or compare interrupt | 14 |
| PWM2_INT | 16-bit Timer PWM 2 | 16-bit Timer PWM2 counter Overflow or compare interrupt | 15 |
| PWM1_INT | 16-bit Timer PWM 1 | 16-bit Timer PWM1 counter overflow or compare interrupt | 16 |
| PWM0_INT | 16-bit timer PWM 0 | 16-bit Timer PWM1 counter overflow or compare interrupt | 17 |
| OVF24_INT | 24-bit Timer Control | 24-bit Timer counter overflow interrupt | 18 |
| CAPTURE_1_INT | 24-bit Timer Control | 24-bit Timer capture 1 interrupt | 19 |
| COMP_1_INT | 24-bit Timer Control | 24-bit Timer compare 1 interrupt | 20 |
| CAPTURE_0_INT | 24-bit Timer Control | 24-bit Timer capture 0 interrupt | 21 |
| COMP_0_INT | 24-bit Timer Control | 24-bit Timer compare 0 interrupt | 22 |
| CPCC_INT | Constant Power Constant Current | Mode switched in CPCC module Flag needs to be read for details | 23 |
| ADC_CONV_INT | 12-bit ADC Control | ADC end of conversion interrupt | 24 |
| FAULT_INT | Fault Mux Interrupt | Analog comparator interrupts, Over-Voltage detection, Under-Voltage detection, LLM load step detection | 25 |

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**Table 4-1. Interrupt Priority Table (continued)**

| NAME | MODULE COMPONENT OR REGISTER | DESCRIPTION | PRIORITY |
|---|---|---|---|
| DPWM3 | DPWM3 | Same as DPWM1 | 26 |
| DPWM2 | DPWM2 | Same as DPWM1 | 27 |
| DPWM1 | DPWM1 | 1) Every (1-256) switching cycles<br>2) Fault Detection<br>3) Mode switching | 28 |
| DPWM0 | DPWM0 | Same as DPWM1 | 29 |
| EXT_FAULT_INT | External Faults | Fault pin interrupt | 30 |
| SYS_SSI_INT | System Software | System software interrupt | 31 (highest) |

## 4.4 Peripherals

### *4.4.1 Fusion Digital Power Peripherals*

At the core of the UCD31XX controller are 3 Fusion Digital Power Peripherals (FDPP). Each FDPP can be configured to drive from one to eight DPWM outputs. Each FDPP consists of:

- Differential input error ADC (EADC) with sophisticated controls
- Hardware accelerated digital 2-pole/2-zero PID based compensator
- Digital PWM module with support for a variety of topologies

These can be connected in many different combinations, with multiple filters and DPWMs. They are capable of supporting functions like input voltage feed forward, current mode control, and constant current/constant power, etc.. The simplest configuration is shown in the following figure:

#### 4.4.1.1 Front End

The EADC module can be programmed to produce an inverting or non-inverting error relative to the voltage set by the EADC DAC. It also has a successive approximation mode, which can be used to measure absolute voltage. In this case, the SAR module controls the EADC and EADC-DAC to determine the absolute voltage.

The EADC module is shown in Figure 4-1. It contains a differential switch capacitor amplifier. This enables remote sense voltage measurements, using the external EAP and EAN pins. The output of this stage is fed into a second differential amplifier with a reference driven by an internal 10-bit DAC. The gain of this stage is controlled by the AFE register. AFE can have values of 0, 1, 2 or 3 which correspond to an analog gain of 1, 2, 4 or 8 respectively. The EADC has a maximum sense voltage value of 248 mV and a minimum sense value of -256 mV with 8 mV resolution. The analog AFE gain stage effectively makes this resolution programmable to be 8mV, 4 mV, 2 mV or 1 mV. Finally, the EADC output is shifted by 0. 1. 2 or 3 times; this is done to attenuate the digital signal by 1, 2, 4 or 8 times. Both the analog gain value and the digital gain values are determined from the AFE gain setting. Therefore, the total gain of this stage always remains the same and the resolution is always 1 mv/bit.

In addition, the user has the option of enabling an automatic resolution selection algorithm ("gear shifter"). This algorithm will automatically select the finest EADC resolution that can measure the voltage across EAP0 and EAN0. This feature is only available on Front End 0.


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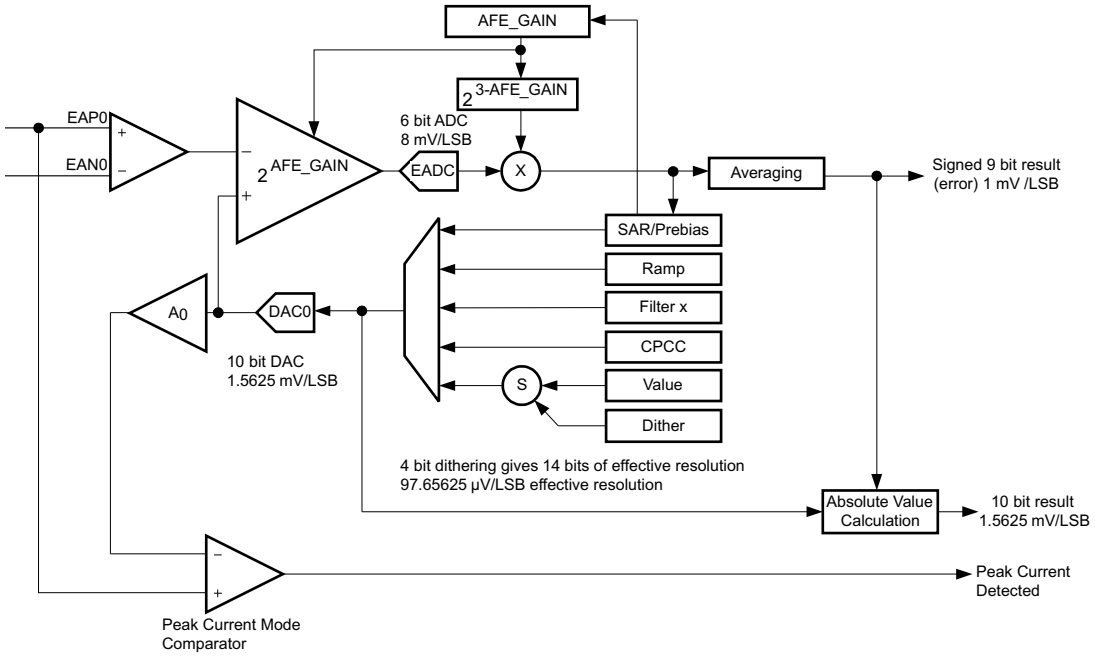


**Figure 4-1. EADC Module**

The EADC control logic receives the sample request from the DPWM module for initiating an EADC conversion. EADC control circuitry captures the EADC-9-bit-code and strobes the digital compensator for processing of the representative error.

#### 4.4.1.2 DPWM Module

The DPWM module represents one complete PWM channel with 2 independent outputs, A and B. Multiple DPWM modules within the UCD3138 system can be configured to support all key power topologies. DPWM modules can be used as independent PWM outputs, each controlling one power supply output voltage rail. It can also be used as a synchronized PWM—with user selectable phase shift between the PWM channels to control power supply outputs with multiphase or interleaved PWM configurations.

The output of the compensator feeds the high resolution DPWM module. The DPWM module produces the pulse width modulated outputs for the power stage switches. The compensator calculates the necessary duty ratio as a 24-bit number in Q23 fixed point format (23 bit integer with 1 sign bit). This represents a value within the range 0.0 to 1.0. This duty ratio value is multiplied by the period of the PWM output to generate the on time of the corresponding PWM output. The resolution of the PWM ON time is 250 psec.

Each DPWM module can be synchronized to another module or to an external sync signal. An input SYNC signal causes a PWM ramp timer to reset. The SYNC signal outputs—from each of the four DPWM modules—occur when the ramp timer crosses a programmed threshold. In this way the phase of the PWM outputs for multiple power stages can be tightly controlled.

The DPWM logic is probably the most complex of the Digital Fusion Peripherals. It takes the output of the compensator and converts it into the correct PWM output for several power supply topologies. It provides for programmable dead times and cycle adjustments for current balancing between phases. It controls the triggering of the EADC. It can synchronize to other DPWMs or to external sources. It can provide synchronization information to other DPWMs or to external recipients. In addition, it interfaces to several fault handling circuits. Some of the control for these fault handling circuits is in the DPWM registers. Fault handling is covered in the Fault Mux section.

Each DPWM module supports the following features:

- Dedicated 14 bit time-base with period and frequency control

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- Shadow period register for end of period updates.
- Quad-event control registers (A and B, rising and falling) (Events 1-4) – Used for on/off PWM duty ratio updates.
- Phase control relative to other DPWM modules
- Sample trigger placement for output voltage sensing at any point during the PWM cycle.
- Support for 2 independent edge placement PWM outputs (same frequency or period setting)
- Dead-time between PWM A and B outputs
- High Resolution capabilities – 250 ps
- Pulse cycle adjustment of up to ±8.192 µs ( 32768 × 250 ps)
- Active high/ active low output polarity selection
- Provides events to trigger both CPU interrupts and start of ADC conversions.

#### 4.4.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*–This register defines where the error voltage is sampled by the EADC in relationship to the PWM period. The programmed value set in the register should be one fourth of the value calculated based on the PWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the PWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the PWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*–count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*–low resolution switching period count. (count of PCLK cycles)
4. *Event 1*–count offset for rising PWM A event. (Count of PCLK cycles)
5. *Event 2*–PWM count for falling PWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*–PWM count for rising PWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*–PWM count for falling PWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*–Constant offset for Event 2 and Event 4 adjustments.

Basic comparisons between the programmed registers and the PWM counter can create the desired edge placements in the DPWM. High resolution edge capability is available on Events 2, 3 and 4.


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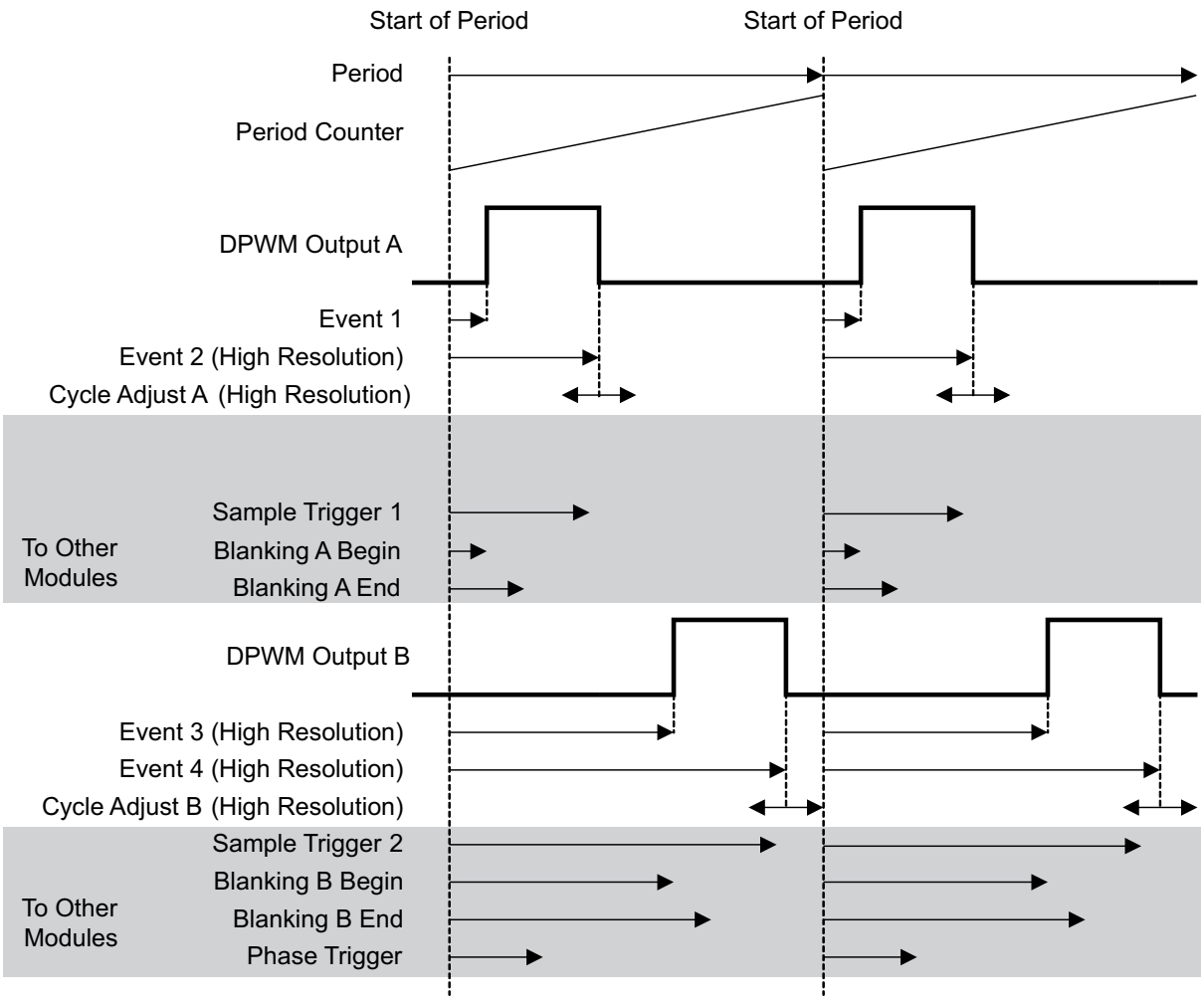
Multi Mode Open Loop




Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
DPWM A Falling Edge = Event 2 + Cycle Adjust A
DPWM B Rising Edge = Event 3
DPWM B Falling Edge = Event 4 + Cycle Adjust B
Phase Trigger = Phase Trigger Register value

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

The drawing above is for multi-mode, open loop. Open loop means that the DPWM is controlled entirely by its own registers, not by the filter output. In other words, the power supply control loop is not closed.

The Sample Trigger signals are used to trigger the Front End to sample input signals. The Blanking signals are used to blank fault measurements during noisy events, such as FET turn on and turn off. Additional DPWM modes are described below.

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#### 4.4.1.4 High Resolution PWM

Unlike conventional PWM controllers where the frequency of the clock dictates the maximum resolution of PWM edges, the UCD3138 DPWM can generate waveforms with resolutions as small as 250 ps. This is 16 times the resolution of the clock driving the DPWM module.

This is achieved by providing the DPWM mechanism with 16 phase shifted clock signals of 250 MHz each. The high resolution section of DPWM can be enabled or disabled, also the resolution can be defined in several steps between 4ns to 250ps. This is done by setting the values of PWM_HR_MULTI_OUT_EN , HIRES_SCALE and ALL_PHASE_CLK_ENA inside the DPWM Control Register 1. See the Fusion Power Peripherals programmer's manual for details.

#### 4.4.1.5 Over Sampling

The DPWM module has the capability to trigger an over sampling event by initiating the EADC to sample the error voltage. The default "00" configuration has the DPWM trigger the EADC once based on the sample trigger register value. The over sampling register has the ability to trigger the sampling 2, 4 or 8 times per PWM period. Thus the time the over sample happens is at the divide by 2, 4, or 8 time set in the sampling register. The "01" setting triggers 2X over sampling, the "10" setting triggers 4X over sampling, and the "11" triggers over sampling at 8X.

#### 4.4.1.6 DPWM Interrupt Generation

The DPWM has the capability to generate a CPU interrupt based on the PWM frequency programmed in the period register. The interrupt can be scaled by a divider ratio of up to 255 for developing a slower interrupt service execution loop. This interrupt can be fed to the ADC circuitry for providing an ADC12 trigger for sequence synchronization. Table 4-2 outlines the divide ratios that can be programmed.

#### 4.4.1.7 DPWM Interrupt Scaling/Range

**Table 4-2. DPWM Interrupt Divide Ratio**

| Interrupt Divide Setting | Interrupt Divide Count | Interrupt Divide Count (hex) | Switching Period Frames (assume 1MHz loop) | Number of 32 MHz Processor Cycles |
|---|---|---|---|---|
| 1 | 0 | 00 | 1 | 32 |
| 2 | 1 | 01 | 2 | 64 |
| 3 | 3 | 03 | 4 | 128 |
| 4 | 7 | 07 | 8 | 256 |
| 5 | 15 | 0F | 16 | 512 |
| 6 | 31 | 1F | 32 | 1024 |
| 7 | 47 | 2F | 48 | 1536 |
| 8 | 63 | 3F | 64 | 2048 |
| 9 | 79 | 4F | 80 | 2560 |
| 10 | 95 | 5F | 96 | 3072 |
| 11 | 127 | 7F | 128 | 4096 |
| 12 | 159 | 9F | 160 | 5120 |
| 13 | 191 | BF | 192 | 6144 |
| 14 | 223 | DF | 224 | 7168 |
| 15 | 255 | FF | 256 | 8192 |


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## 4.5 DPWM Modes of Operation

The DPWM is a complex logic system which is highly configurable to support several different power supply topologies. The discussion below will focus primarily on waveforms, timing and register settings, rather than on logic design.

The DPWM is centered on a period counter, which counts up from 0 to PRD, and then is reset and starts over again.

The DPWM logic causes transitions in many digital signals when the period counter hits the target value for that signal.

### *4.5.1 Normal Mode*

In Normal mode, the Filter output determines the pulse width on DPWM A. DPWM B fits into the rest of the switching period, with a dead time separating it from the DPWM A on-time. It is useful for buck topologies, among others. Here is a drawing of the Normal Mode waveforms:

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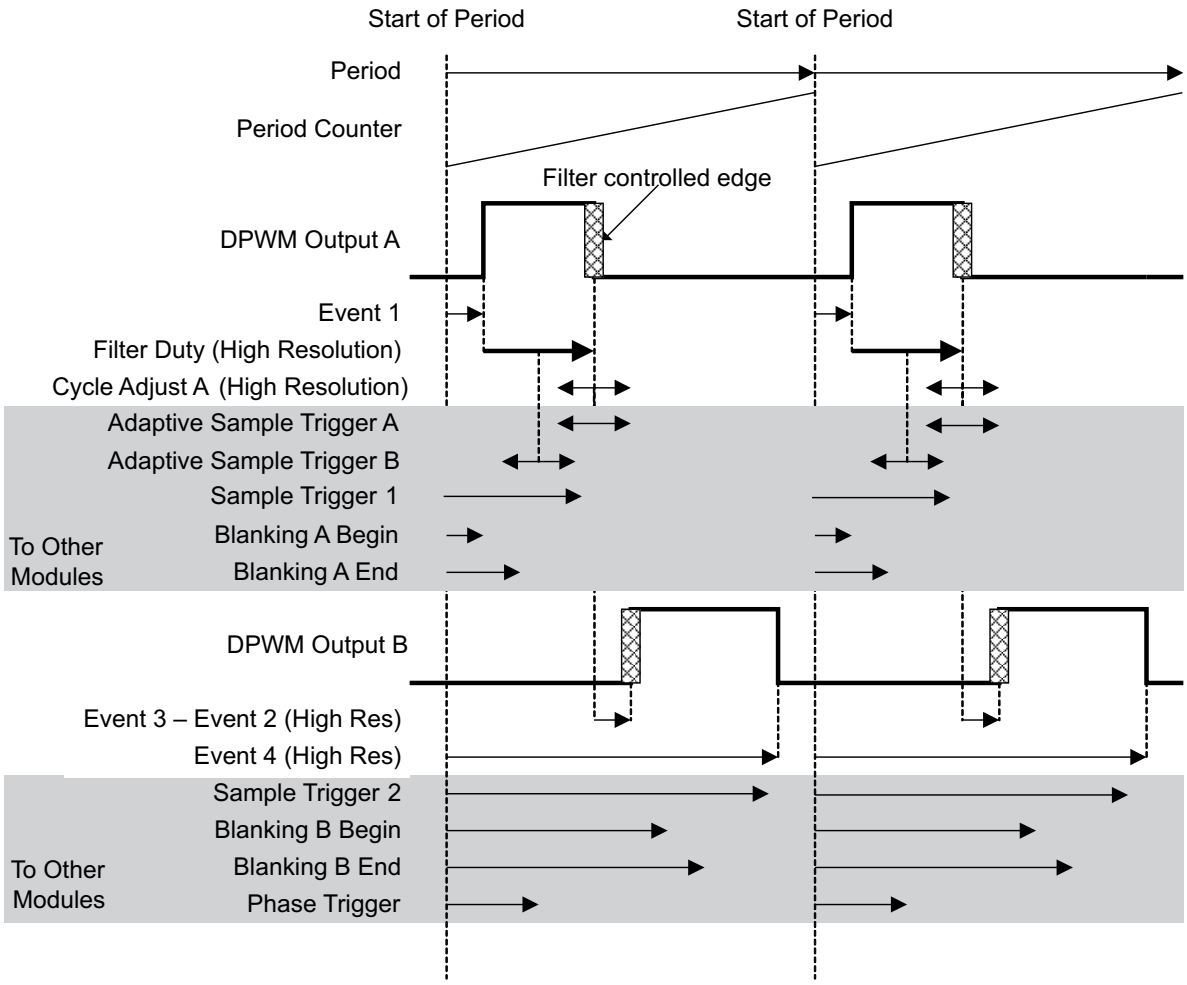
Normal Mode Closed Loop




Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
DPWM A Falling Edge = Event 1 + Filter Duty + Cycle Adjust A
Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register or
Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register
DPWM B Rising Edge = Event 1 + Filter Duty + Cycle Adjust A + (Event 3 – Event 2)
DPWM B Falling Edge = Event 4
Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

Cycle adjust A can be used to adjust pulse widths on individual phases of a multi-phase system. This can be used for functions like current balancing. The Adaptive Sample Triggers can be used to sample in the middle of the on-time (for an average output), or at the end of the on-time (to minimize phase delay) The Adaptive Sample Register provides an offset from the center of the on-time. This can compensate for external delays, such as MOSFET and gate driver turn on times.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Blanking A-Begin and Blanking A-End can be used to blank out noise from the MOSFET turn on at the beginning of the period (PWMA rising edge). Blanking B could be used at the turn off time of PWMB. The other edges are dynamic, so blanking is more difficult.

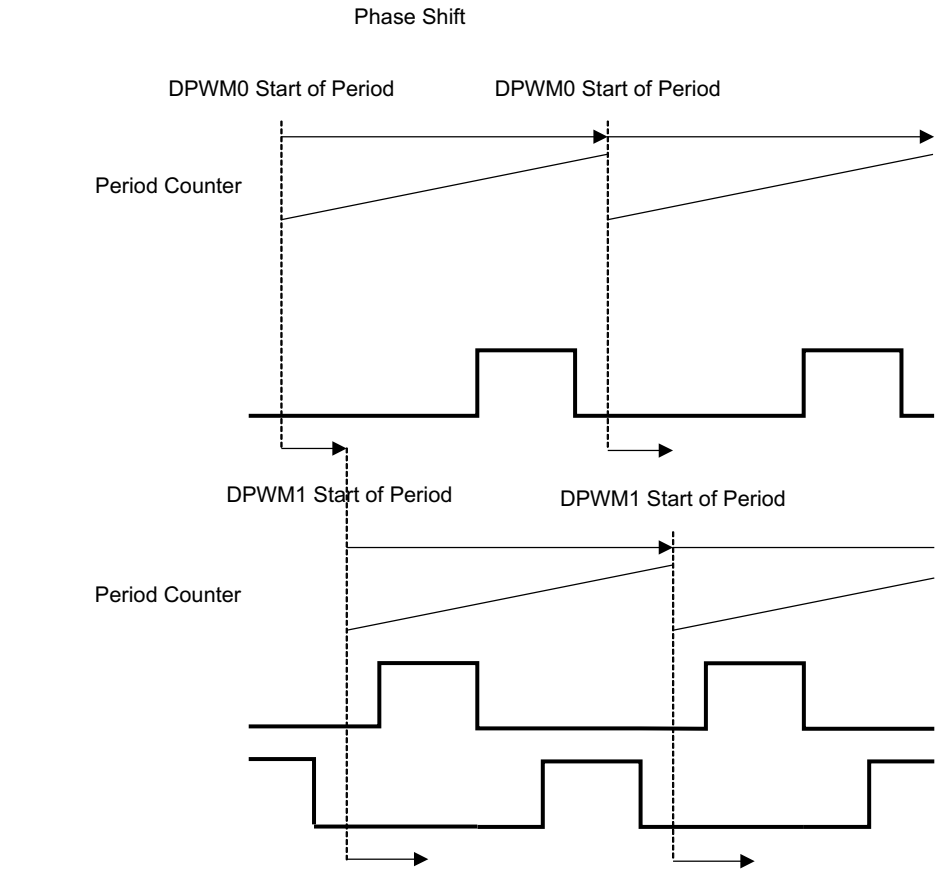
Cycle Adjust B has no effect in Normal Mode.

## 4.6 Phase Shifting

In most modes, it is possible to synchronize multiple DPWM modules using the phase shift signal. The phase shift signal has two possible sources. It can come from the Phase Shift Register. This provides a fixed value, which is useful for an interleaved PFC, for example.

The phase shift value can also come from the filter output. In this case, the changes in the filter output causes changes in the phase relationship of two DPWM modules. This is useful for phase shifted full bridge topologies.

The following figure shows the mechanism of phase shift:



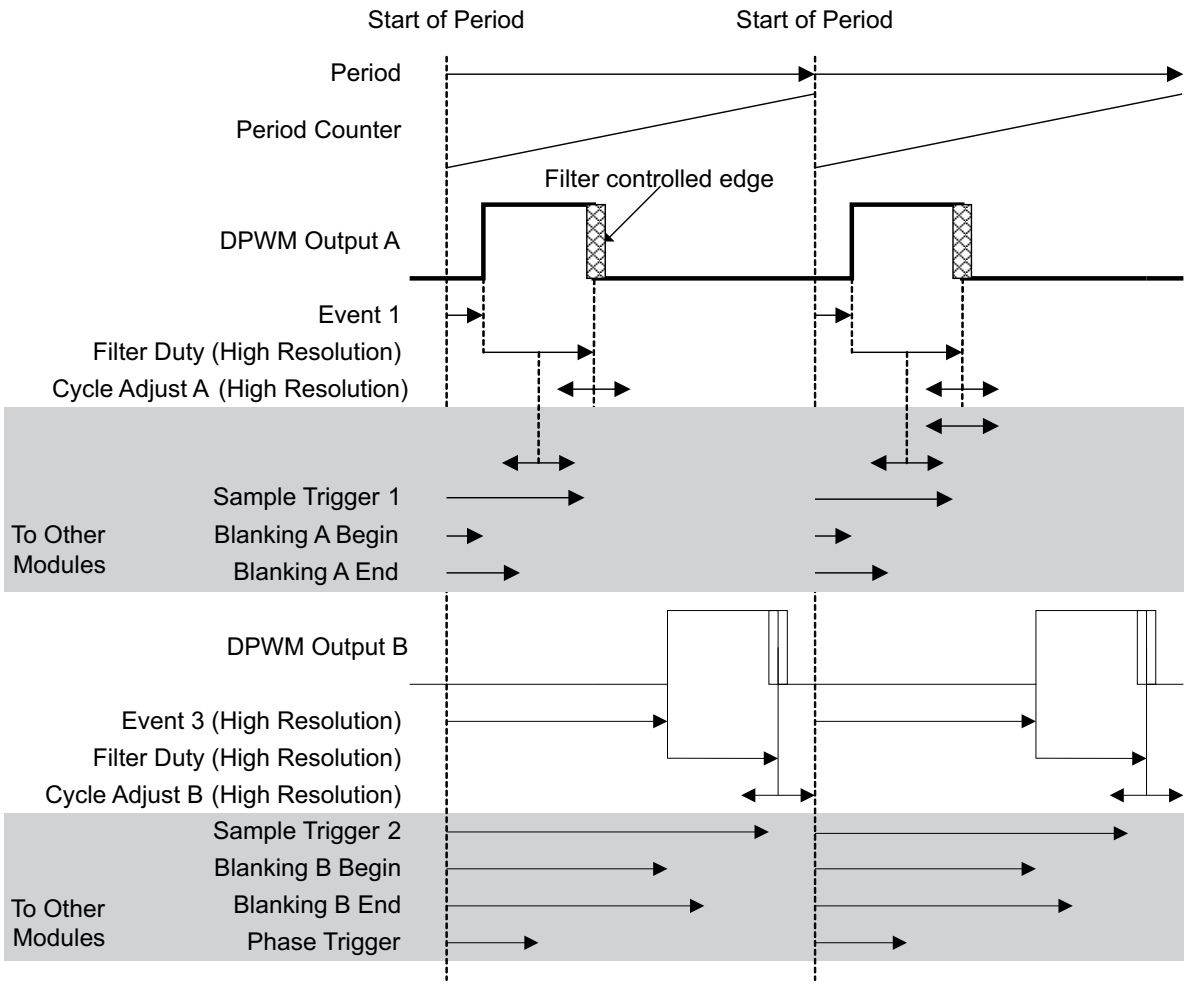

Phase Trigger = Phase Trigger Register value or Filter Duty

## 4.7 DPWM Multiple Output Mode

Multi mode is used for systems where each phase has only one driver signal. It enables each DPWM peripheral to drive two phases with the same pulse width, but with a time offset between the phases, and with different cycle adjusts for each phase.

Here is a diagram for Multi-Mode:

Multi Mode Closed Loop




Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
DPWM A Falling Edge = Event 1 + Filter Duty + Cycle Adjust A
Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register or
Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register
DPWM B Rising Edge = Event 3
DPWM B Falling Edge = Event 3 + Filter Duty + Cycle Adjust B
Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End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Event 2 and Event 4 are not relevant in Multi mode.

DPWMB can cross over the period boundary safely, and still have the proper pulse width, so full 100% pulse width operation is possible. DPWMA cannot cross over the period boundary.

Since the rising edge on DPWM B is also fixed, Blanking B-Begin and Blanking B-End can be used for blanking this rising edge.

And, of course, Cycle Adjust B is usable on DPWM B.

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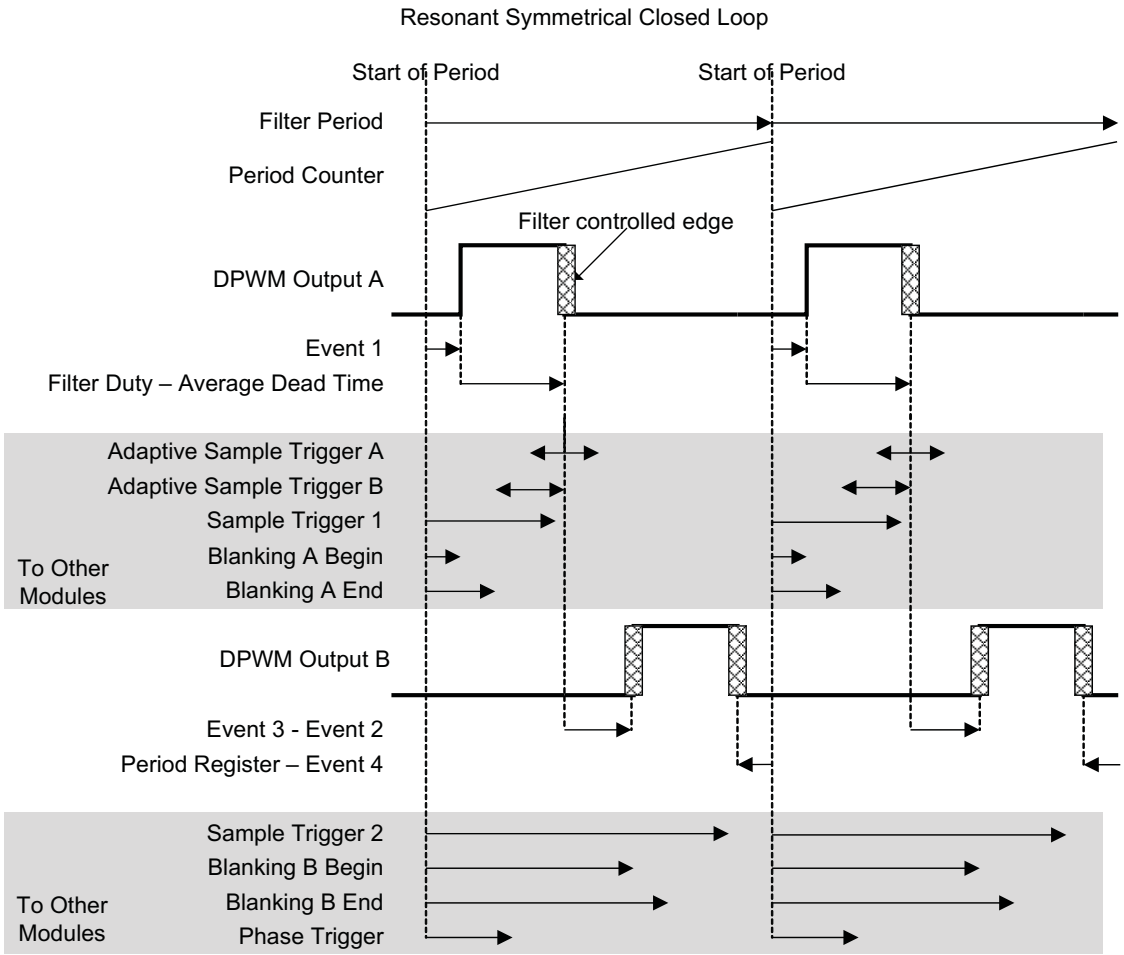
## 4.8 DPWM Resonant Mode

This mode provides a symmetrical waveform where DPWMA and DPWMB have the same pulse width. As the switching frequency changes, the dead times between the pulses remain the same.

The equations for this mode are designed for a smooth transition from PWM mode to resonant mode, as described in the LLC Example section. Here is a diagram of this mode:




Events which change with DPWM mode:

Dead Time 1 = Event 3 – Event 2
Dead Time 2 = Event 1 + Period Register – Event 4)
Average Dead Time = (Dead Time 1 + Dead Time 2)/2

DPWM A Rising Edge = Event 1
DPWM A Falling Edge = Event 1 + Filter Duty – Average Dead Time
Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register
Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register
DPWM B Rising Edge = Event 1 + Filter Duty – Average Dead Time + (Event 3 – Event 2)
DPWM B Falling Edge = Filter Period – (Period Register – Event 4)
Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End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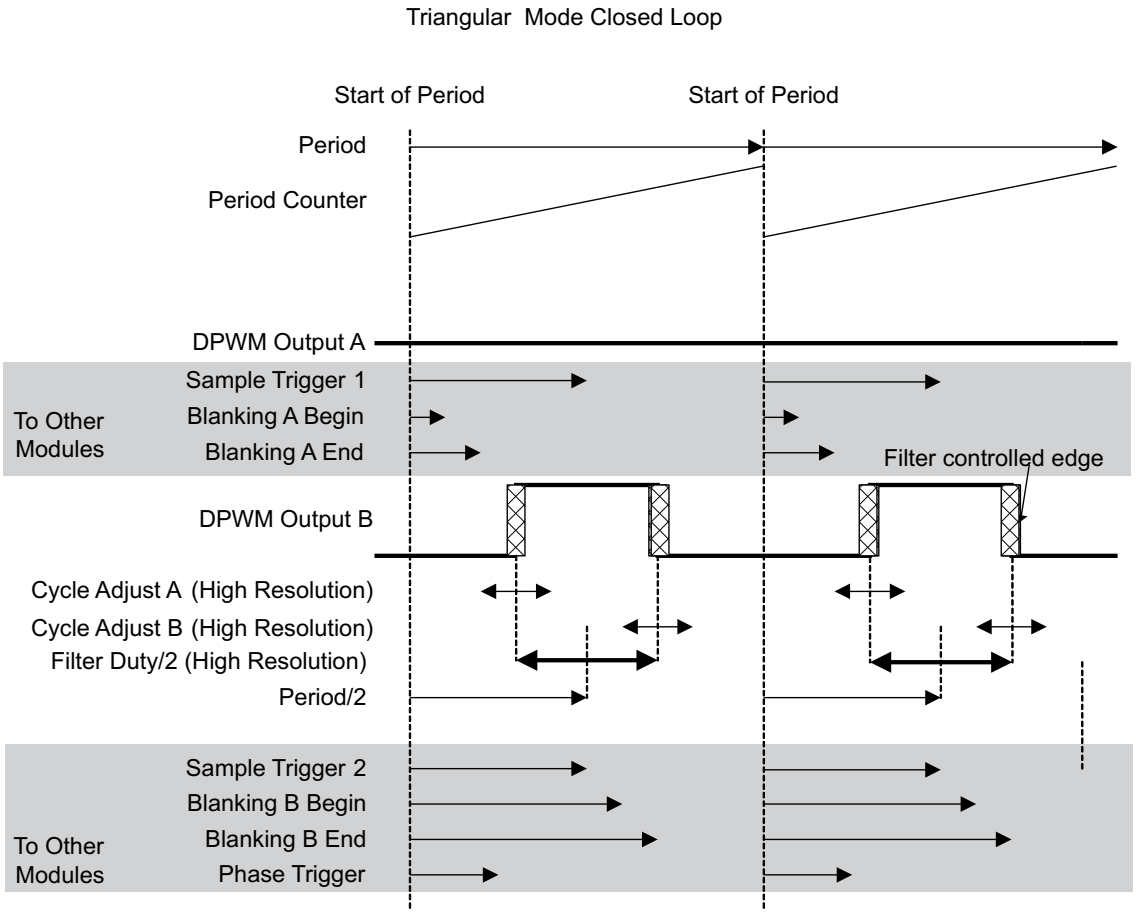
The Filter has two outputs, Filter Duty and Filter Period. In this case, the Filter is configured so that the Filter Period is twice the Filter Duty. So if there were no dead times, each DPWM pin would be on for half of the period. For dead time handling, the average of the two dead times is subtracted from the Filter Duty for both DPWM pins. Therefore, both pins will have the same on-time, and the dead times will be fixed regardless of the period. The only edge which is fixed relative to the start of the period is the rising edge of DPWM A. This is the only edge for which the blanking signals can be used easily.

## 4.9 Triangular Mode

Triangular mode provides a stable phase shift in interleaved PFC and similar topologies. In this case, the PWM pulse is centered in the middle of the period, rather than starting at one end or the other. In Triangular Mode, only DPWM-B is available. Here is a diagram for Triangular Mode:




Events which change with DPWM mode:

DPWM A Rising Edge = None
DPWM A Falling Edge = None
Adaptive Sample Trigger = None
DPWM B Rising Edge = Period/2 - Filter Duty/2 + Cycle Adjust A
DPWM B Falling Edge = Period/2 + Filter Duty/2 + Cycle Adjust B
Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

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All edges are dynamic in triangular mode, so fixed blanking is not that useful. The adaptive sample trigger is not needed. It is very easy to put a fixed sample trigger exactly in the center of the FET on-time, because the center of the on-time does not move in this mode.

## 4.10 Leading Edge Mode

Leading edge mode is very similar to Normal mode, reversed in time. The DPWM A falling edge is fixed, and the rising edge moves to the left, or backwards in time, as the filter output increases. The DPWM B falling edge stays ahead of the DPWMA rising edge by a fixed dead time. Here is a diagram of the Leading Edge Mode:


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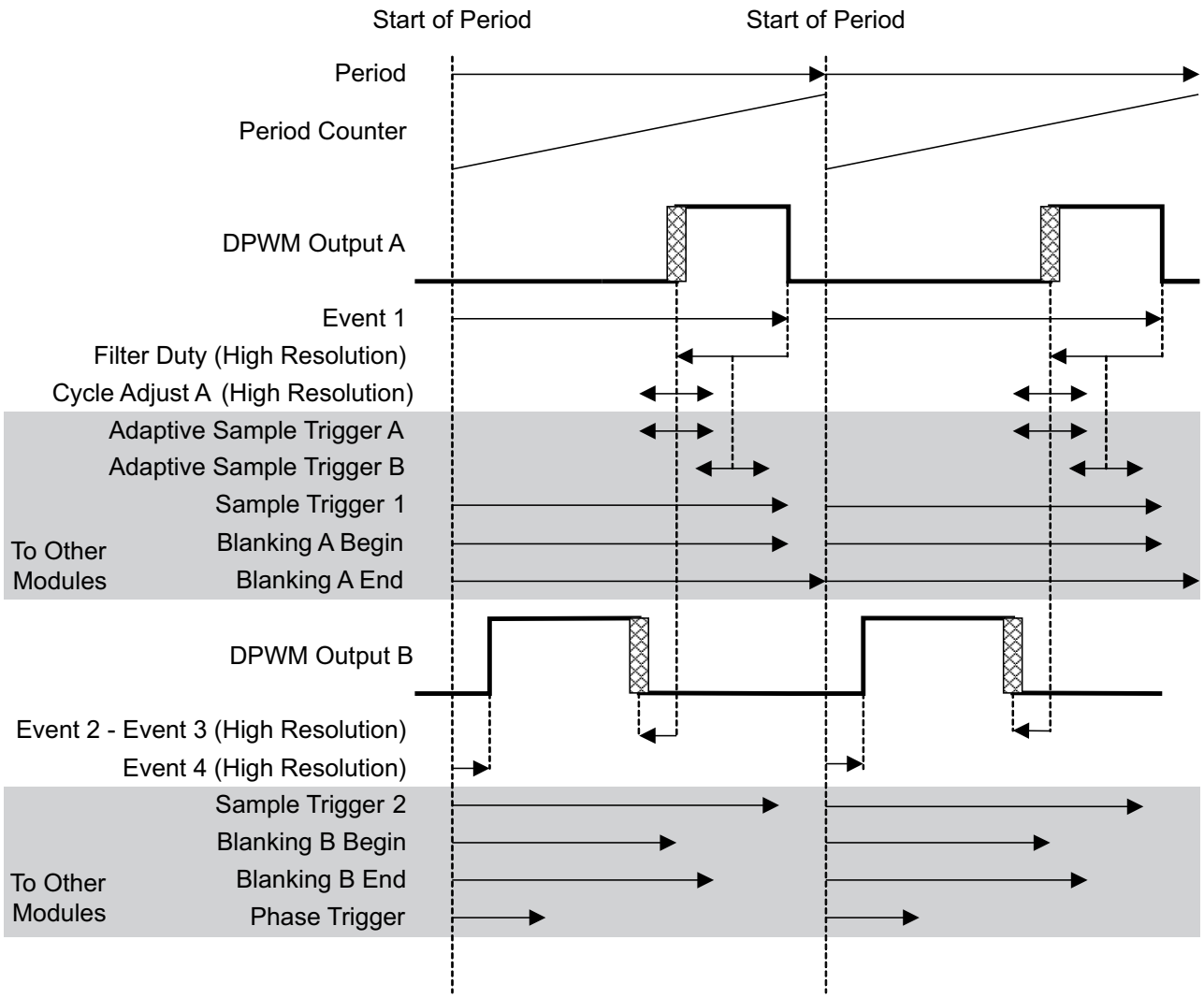
Leading Edge Closed Loop




Events which change with DPWM mode:

DPWM A Falling Edge = Event 1
DPWM A Rising Edge = Event 1 - Filter Duty + Cycle Adjust A
Adaptive Sample Trigger A = Event 1 - Filter Duty + Adaptive Sample Register or
Adaptive Sample Trigger B = Event 1 - Filter Duty/2 + Adaptive Sample Register
DPWM B Rising Edge = Event 4
DPWM B Falling Edge = Event 1 - Filter Duty + Cycle Adjust A -(Event 2 – Event 3)
Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

As in the Normal mode, the two edges in the middle of the period are dynamic, so the fixed blanking intervals are mainly useful for the edges at the beginning and end of the period.

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## 4.11 Sync FET Ramp and IDE Calculation

The UCD3138 has built in logic for controlling MOSFETs for synchronous rectification (Sync FETs). This comes in two forms:

- Sync FET ramp
- Ideal Diode Emulation (IDE) calculation

When starting up a power supply, sometimes there is already a voltage on the output – this is called prebias. It is very difficult to calculate the ideal Sync FET on-time for this case. If it is not calculated correctly, it may pull down the pre-bias voltage, causing the power supply to sink current.

To avoid this, Sync FETs are not turned on until after the power supply has ramped up to the nominal voltage. The Sync FETs are turned on gradually in order to avoid an output voltage glitch. The Sync FET Ramp logic can be used to turn them on at a rate below the bandwidth of the filter.

In discontinuous mode, the ideal on-time for the Sync FETs is a function of Vin, Vout, and the primary side duty cycle (D). The IDE logic in the UCD3138 takes Vin and Vout data from the firmware and combines it with D data from the filter hardware. It uses this information to calculate the ideal on-time for the Sync FETs.

## 4.12 Automatic Mode Switching

Automatic Mode switching enables the DPWM module to switch between modes automatically, with no firmware intervention. This is useful to increase efficiency and power range. The following paragraphs describe phase-shifted full bridge and LLC examples:

### *4.12.1 Phase Shifted Full Bridge Example*

In phase shifted full bridge topologies, efficiency can be increased by using pulse width modulation, rather than phase shift, at light load. This is shown below:


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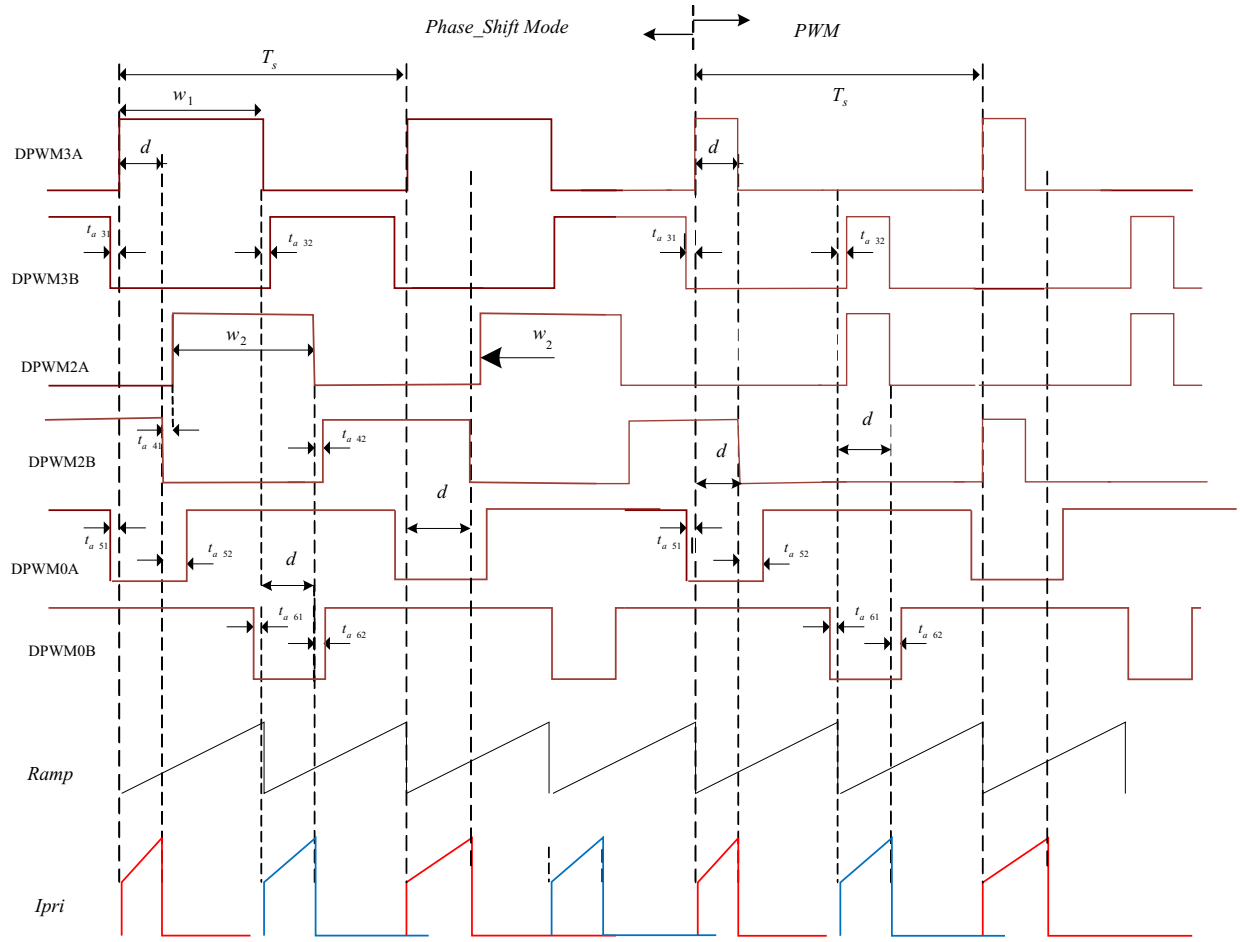
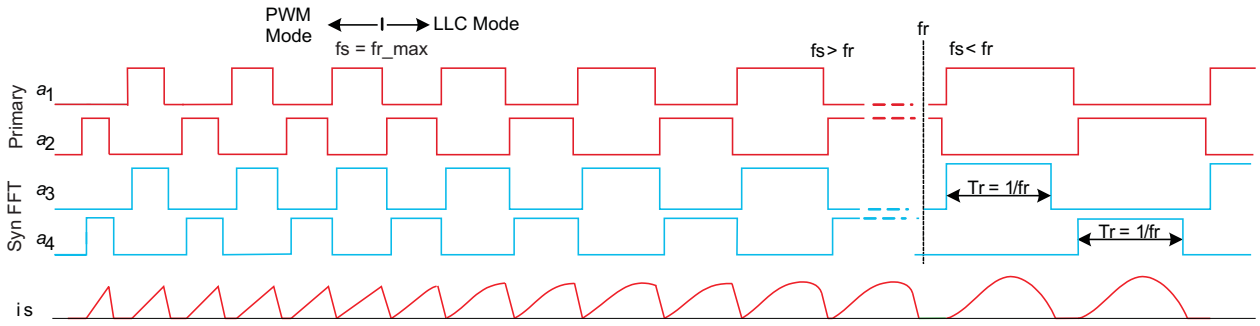



### 4.12.2 LLC Example

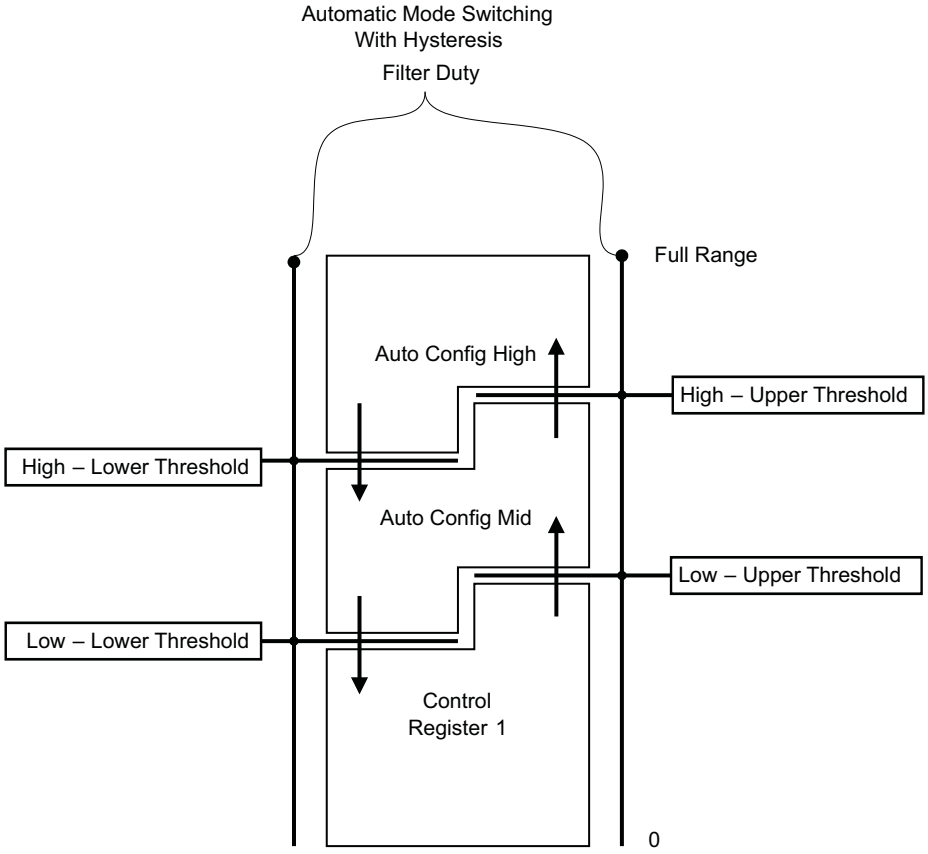
In LLC, three modes are used. At the highest frequency, a pulse width modulated mode (Multi Mode) is used. As the frequency decreases, resonant mode is used. As the frequency gets still lower, the synchronous MOSFET drive changes so that the on-time is fixed and does not increase. Here are the waveforms for the LLC:



### 4.12.3 Mechanism for Automatic Mode Switching

Many of the configuration parameters for the DPWM are in DPWM Control Register 1. For automatic mode switching, some of these parameters are duplicated in the Auto Config Mid and Auto Config High registers.

If automatic mode switching is enabled, the filter duty signal is used to select which of these three registers is used. There are 4 registers which are used to select the points at which the mode switching takes place. They are used as shown below.




As shown, the registers are used in pairs for hysteresis. The transition from Control Register 1 to Auto Config Mid only takes place when the Filter Duty goes above the Low Upper threshold. It does not go back to Auto Config Mid until the Low Lower Threshold is passed. This prevents oscillation between modes if the filter duty is close to a mode switching point.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## 4.13 DPWMC, Edge Generation, IntraMux

The UCD31xx has hardware for generating complex waveforms beyond the simple DPWMA and DPWMB waveforms already discussed – DPWMC, the Edge Generation Module, and the IntraMux.

DPWMC is a signal inside the DPWM logic. It goes high at the Blanking A begin time, and low at the Blanking A end time.

The Edge Gen module takes DPWMA and DPWMB from its own DPWM module, and the next one, and uses them to generate edges for two outputs. For DPWM3, the DPWM0 is considered to be the next DPWM. Each edge (rising and falling for DPWMA and DPWMB) has 8 options which can cause it.

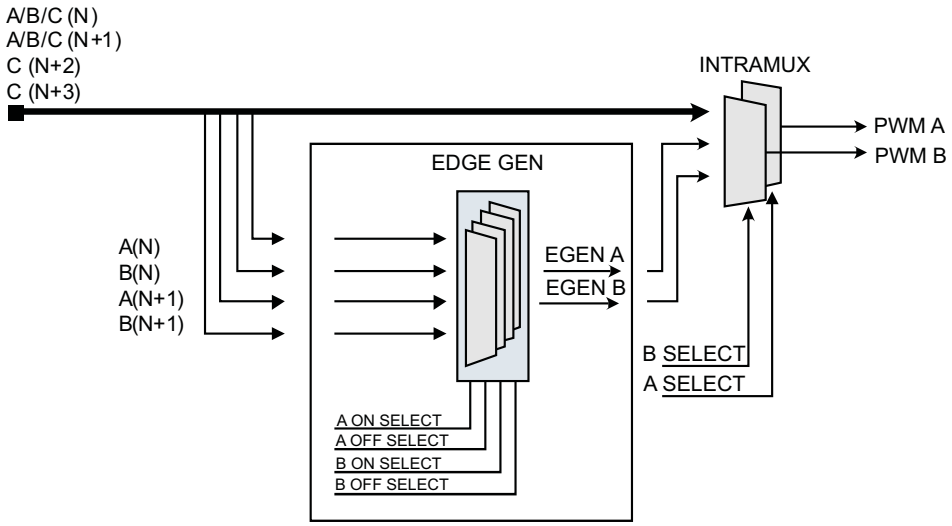
The options are:

0 = DPWM(n) A Rising edge
1 = DPWM(n) A Falling edge
2 = DPWM(n) B Rising edge
3 = DPWM(n) B Falling edge
4 = DPWM(n+1) A Rising edge
5 = DPWM(n+1) A Falling edge
6 = DPWM(n+1) B Rising edge
7 = DPWM(n+1) B Falling edge

The Edge Gen is controlled by the DPWMEDGEGEN register. It also has an enable/disable bit.

The IntraMux is controlled by the Auto Config registers. Intra Mux is short for intra multiplexer. The IntraMux takes signals from multiple DPWMs and from the Edge Gen and combines them logically to generate DPWMA and DPWMB signals This is useful for topologies like phase-shifted full bridge, especially when they are controlled with automatic mode switching. Of course, it can all be disabled, and DPWMA and DPWMB will be driven as described in the sections above. If the Intra Mux is enabled, high resolution must be disabled, and DPWM edge resolution goes down to 4 ns.

Here is a drawing of the Edge Gen/Intra Mux:




Here is a list of the IntraMux modes for DPWMA:

0 = DPWMA(n) pass through (default)
1 = Edge-gen output, DPWMA(n)
2 = DPWNC(n)
3 = DPWMB(n) (Crossover)
4 = DPWMA(n+1)
5 = DPWMB(n+1)

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6 = DPWMC(n+1)
7 = DPWMC(n+2)
8 = DPWMC(n+3)

and for DPWMB:

0 = DPWMB(n) pass through (default)
1 = Edge-gen output, DPWMB(n)
2 = DPWNC(n)
3 = DPWMA(n) (Crossover)
4 = DPWMA(n+1)
5 = DPWMB(n+1)
6 = DPWMC(n+1)
7 = DPWMC(n+2)
8 = DPWMC(n+3)

The DPWM number wraps around just like the Edge Gen unit. For DPWM4 the following definitions apply:

| | |
|---|---|
| DPWM(n) | DPWM4 |
| DPWM(n+1) | DPWM0 |
| DPWM(n+2) | DPWM1 |
| DPWM(n+3) | DPWM2 |

## 4.14 Filter

The UCD31XX filter is a PID filter with many enhancements for power supply control. Some of its features include:

- Traditional PID Architecture
- Programmable non-linear limits for automated modification of filter coefficients based on received EADC error
- Multiple coefficient sets fully configurable by firmware
- Full 24-bit precision throughout filter calculations
- Programmable clamps on integrator branch and filter output
- Ability to load values into internal filter registers while system is running
- Ability to stall calculations on any of the individual filter branches
- Ability to turn off calculations on any of the individual filter branches
- Duty cycle, resonant period, or phase shift generation based on filter output.
- Flux balancing
- Voltage feed forward


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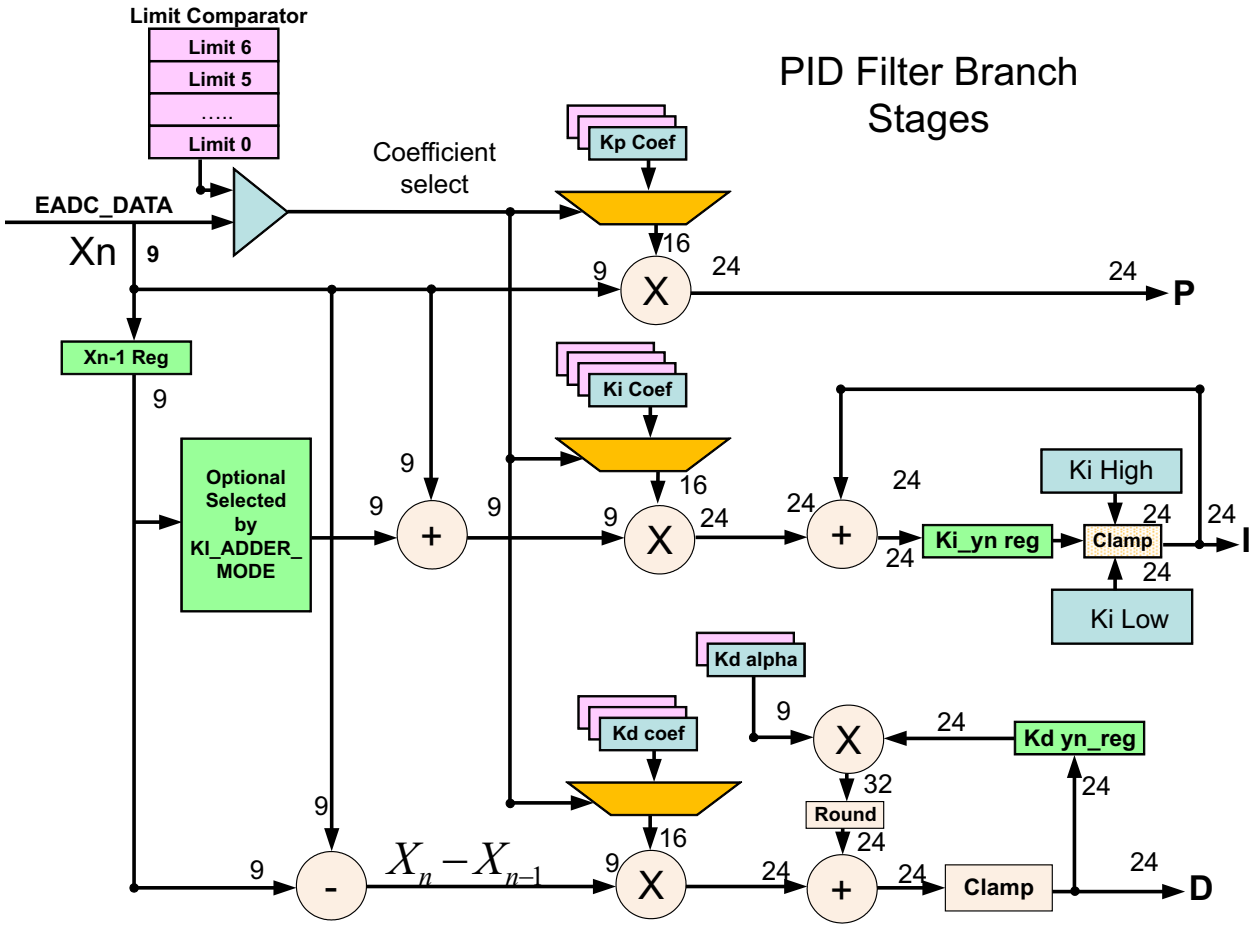
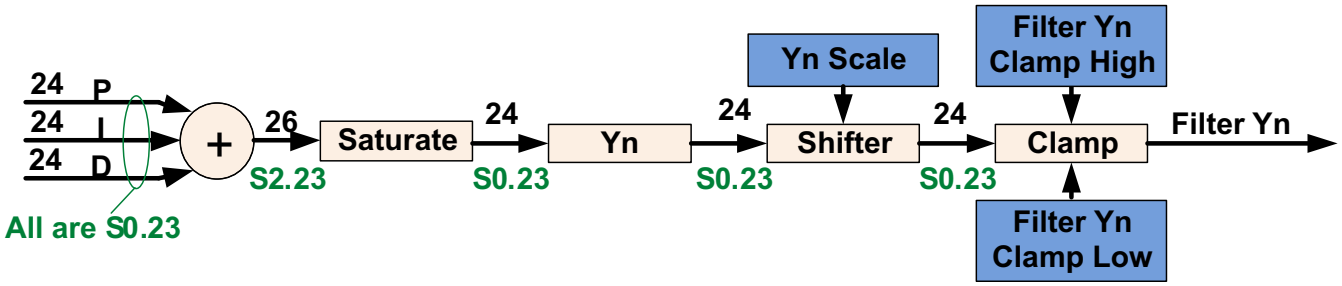
Here is the first section of the Filter:




The filter input, Xn, generally comes from a front end. Then there are three branches, P, I. and D. Note that the D branch also has a pole, Kd Alpha. Clamps are provided both on the I branch and on the D alpha pole.

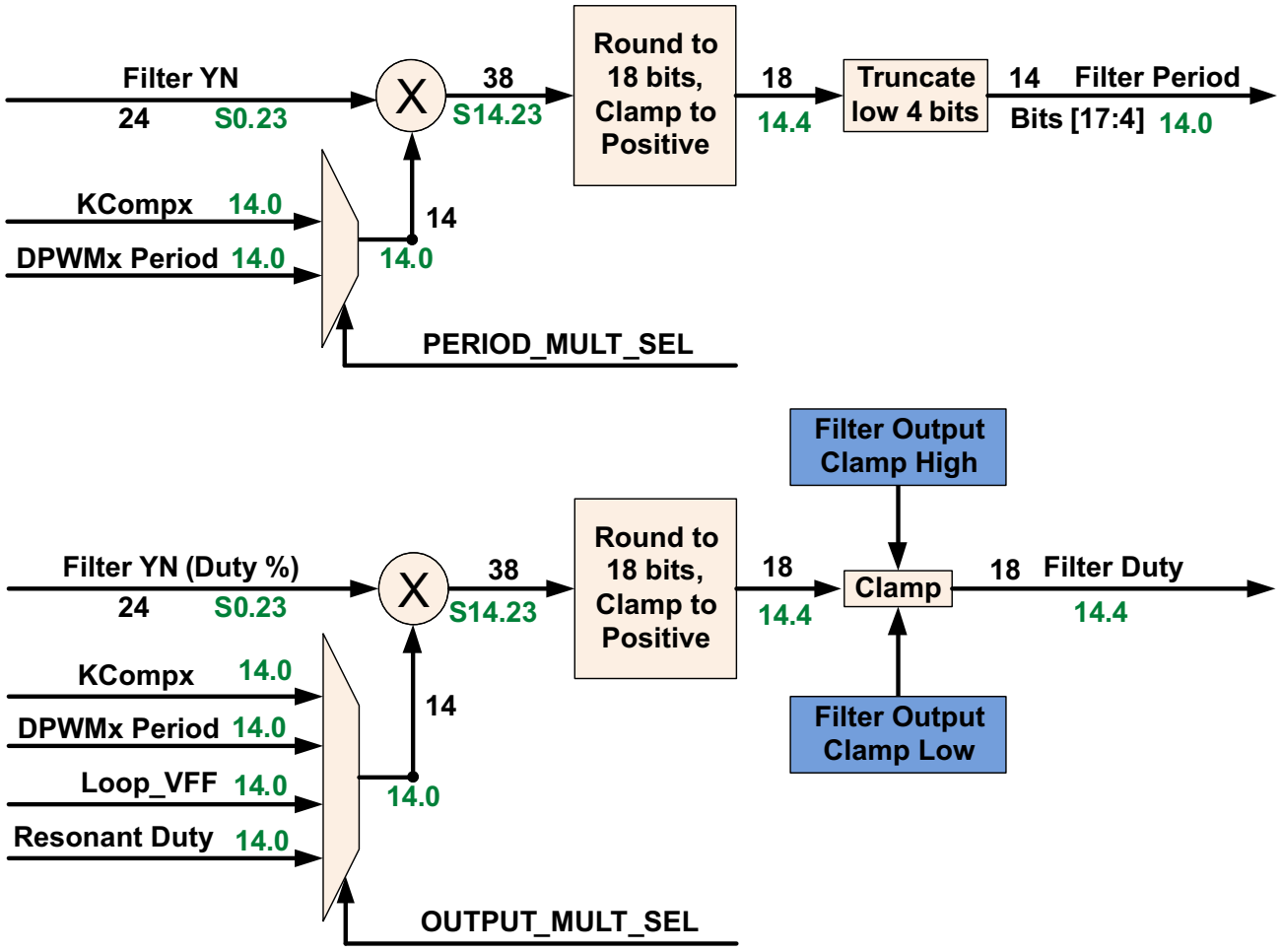
The filter also supports a nonlinear mode, where up to 7 different sets of coefficients can be selected depending on the magnitude of the error input Xn. This can be used to increase the filter gain for higher errors to improve transient response.

Here is the output section of the filter:




This section combines the P, I, and D sections, and provides for saturation, scaling, and clamping.

There is a final section for the filter, which permits its output to be matched to the DPWM:




This permits the filter output to be multiplied by a variety of correction factors to match the DPWM Period, to provide for Voltage Feed Forward, or for other purposes. After this, there is another clamp. For resonant mode, the filter can be used to generate both period and duty cycle.

### 4.14.1 Loop Multiplexer

The Loop Mux controls interconnections between the filters, front ends, and DPWMs. Any filter, front end, and DPWM can be combined with each other in many configurations.

It also controls the following connections:

- DPWM to Front End
- Front End DAC control from Filters or Constant Current/Constant Power Module
- Filter Special Coefficients and Feed Forward
- DPWM synchronization
- Filter to DPWM

The following control modules are configured in the Loop Mux:

- Constant Power/Constant Current
- Cycle Adjustment (Current and flux balancing)
- Global Period
- Light Load (Burst Mode)
- Analog Peak Current Mode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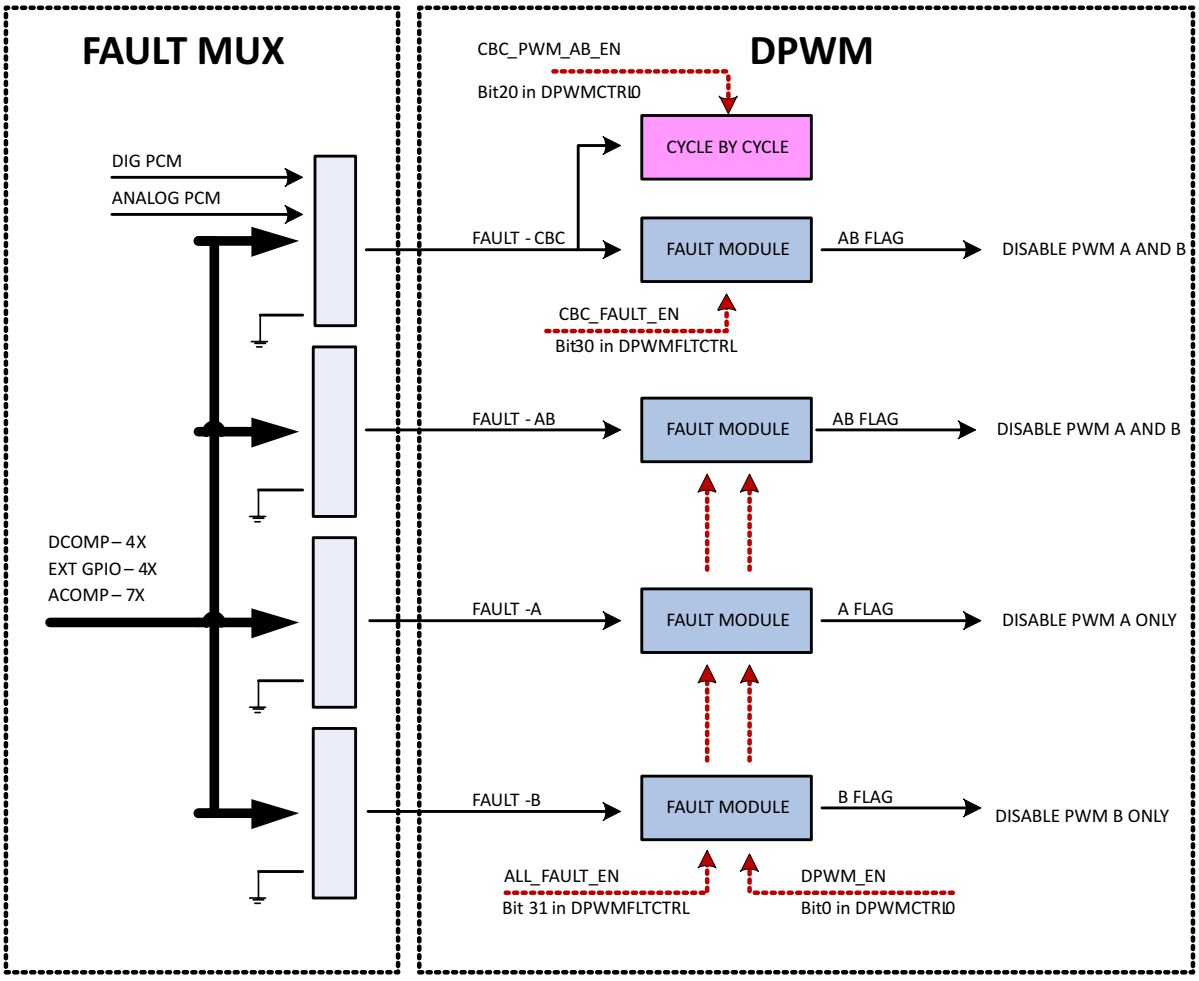
### 4.14.2 Fault Multiplexer

In order to allow a flexible way of mapping several fault triggering sources to all the DPWMs channels, the UCD3138 provides an extensive array of multiplexers that are united under the name Fault Mux module.

The Fault Mux Module supports the following types of mapping between all the sources of fault and all different fault response mechanism inside each DPWM module.

- Many fault sources mapped to a single fault response mechanism. For instance an analog comparator in charge of over voltage protection, a digital comparator in charge of over current protection and an external digital fault pin can be all mapped to a fault-A signal connected to a single FAULT MODULE and shut down DPWM1-A.
- A single fault source can be mapped to many fault response mechanisms inside many DPWM modules. For instance an analog comparator in charge of over current protection can be mapped to DPWM-0 through DPWM-3 by way of several fault modules.
- Many fault sources can be mapped to many fault modules inside many DPWM modules.




The Fault Mux Module provides a multitude of fault protection functions within the UCD3138 high-speed loop (Front End Control, Filter, DPWM and Loop Mux modules). The Fault Mux Module allows highly configurable fault generation based on digital comparators, high-speed analog comparators and external fault pins. Each of the fault inputs to the DPWM modules can be configured to one or any combination of the fault events provided in the Fault Mux Module.

Each one of the DPWM engines has four fault modules. The modules are called CBC fault module, AB fault module, A fault module and B fault module.

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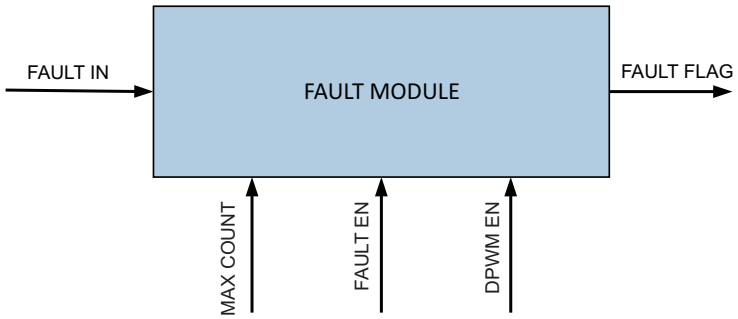
The internal circuitry in all the four fault modules is identical, and the difference between the modules is limited to the way the modules are attached to the DPWMs.




All fault modules provide immediate fault detection but only once per DPWM switching cycle. Each one of the fault modules own a separate max_count and the fault flag will be set only if sequential cycle-by-cycle faults count exceeds max_count.

Once the fault flag is set DPWMs need to be disabled by DPWM_EN going low in order to clear the fault flags. Please note, all four Fault Modules share the same DPWM_EN control, all fault flags (output of Fault Modules) will be cleared simultaneously.

All four Fault Modules share the same global FAULT_EN as well. Therefore a specific Fault Module cannot be enabled/ disabled separately.

Unlike Fault Modules, only one Cycle by Cycle block is available in each DPWM module.

The Cycle by Cycle block works in conjunction with CBC Fault Module and enables DPWM reaction to signals arriving from Analog Peak current mode (PCM) module.

The Fault Mux Module supports the following basic functions:

- 4 digital comparators with programmable thresholds and fault generation
- Configuration for 7 high speed analog comparators with programmable thresholds and fault generation
- External GPIO detection control with programmable fault generation
- Configurable DPWM fault generation for DPWM Current Limit Fault, DPWM Over-Voltage Detection Fault, DPWM A External Fault, DPWM B External Fault and DPWM IDE Flag
- Clock Failure Detection for High and Low Frequency Oscillator blocks
- Discontinuous Conduction Mode Detection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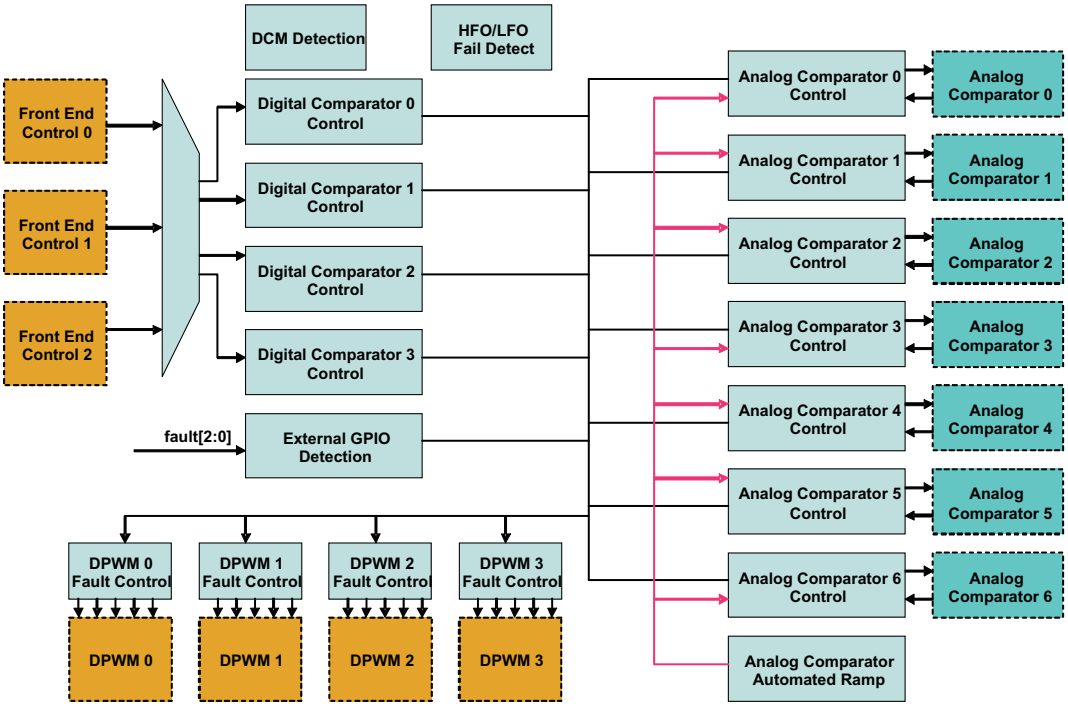


**Figure 4-2. Fault Mux Block Diagram**

## 4.15 Communication Ports

### *4.15.1 SCI (UART) Serial Communication Interface*

A maximum of two independent Serial Communication Interface (SCI) or Universal Asynchronous Receiver/Transmitter (UART) interfaces are included within the device for asynchronous start-stop serial data communication (see the pin out sections for details) Each interface has a 24 bit prescaler for supporting programmable baud rates and has programmable data word and stop bit options. Half or full duplex operation is configurable through register bits. A loop back feature can also be setup for firmware verification. Both SCI-TX and SCI-RX pin sets can be used as GPIO pins when the peripheral is not being used.

### *4.15.2 PMBUS*

The PMBus Interface supports independent master and slave modes controlled directly by firmware through a processor bus interface. Individual control and status registers enable firmware to send or receive I2C, SMBus or PMBus messages in any of the accepted protocols, in accordance with the $I^2C$ Specification, SMBus Specification (Version 2.0) and the PMBUS Power System Management Protocol Specification.

The PMBus interface is controlled through a processor bus interface, utilizing a 32-bit data bus and 6-bit address bus. The PMBus interface is connected to the expansion bus, which features 4 byte write enables, a peripheral select dedicated for the PMBus interface, separated 32-bit data buses for reading and writing of data and active-low write and output enable control signals. In addition, the PMBus Interface connects directly to the $I^2C$/SMBus/PMBus Clock, Data, Alert, and Control signals.

**Example: PMBus Address Decode via ADC12 Reading**

The user can allocate 2 pins of the 12-bit ADC input channels, AD_00 and AD_01, for PMBus address decoding. At power-up the device applies $I_{BIAS}$ to each address detect pin and the voltage on that pin is captured by the internal 12-bit ADC.

Where bin($V_{AD0x}$) is the address bin for one of 12 address as shown in Figure 4-3.

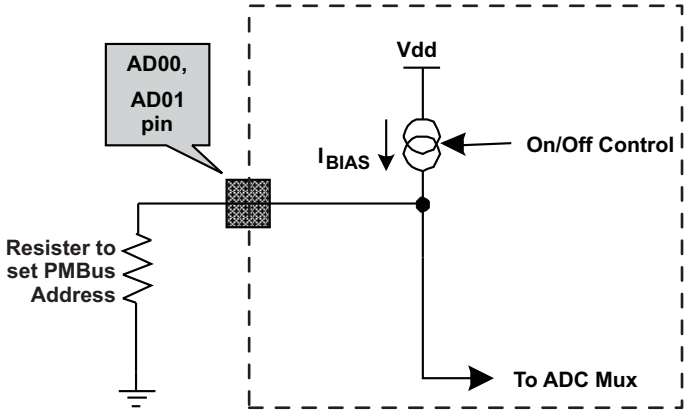


**Figure 4-3. PMBus Address Detection Method**

### *4.15.3 General Purpose ADC12*

The ADC12 is a 12 bit, high speed analog to digital converter, equipped with the following options:

- Typical conversion speed of 268 ksps
- Conversions can consist from 1 to 16 ADC channel conversions in any desired sequence
- Post conversion averaging capability, ranging from 4X, 8X, 16X or 32X samples
- Configurable triggering for ADC conversions from the following sources: firmware, DPWM rising edge, ADC_EXT_TRIG pin or Analog Comparator results
- Interrupt capability to embedded processor at completion of ADC conversion
- Six digital comparators on the first 6 channels of the conversion sequence using either raw ADC data or averaged ADC data
- Two 10 µA current sources for excitation of PMBus addressing resistors
- Dual sample and hold for accurate power measurement
- Internal temperature sensor for temperature protection and monitoring

The control module ( ADC12 Contol Block Diagram) contains the control and conversion logic for auto-sequencing a series of conversions. The sequencing is fully configurable for any combination of 16 possible ADC channels through an analog multiplexer embedded in the ADC12 block. Once converted, the selected channel value is stored in the result register associated with the sequence number. Input channels can be sampled in any desired order or programmed to repeat conversions on the same channel multiple times during a conversion sequence. Selected channel conversions are also stored in the result registers in order of conversion, where the result 0 register is the first conversion of a 16-channel sequence and result 15 register is the last conversion of a 16-channel sequence. The number of channels converted in a sequence can vary from 1 to 16.

Unlike EADC0 through EADC2, which are primarily designed for closing high speed compensation loops, the ADC12 is not usually used for loop compensation purposes. The EADC converters have a substantially faster conversion rate, thus making them more attractive for closed loop control. The ADC12 features make it best suited for monitoring and detection of currents, voltages, temperatures and faults.


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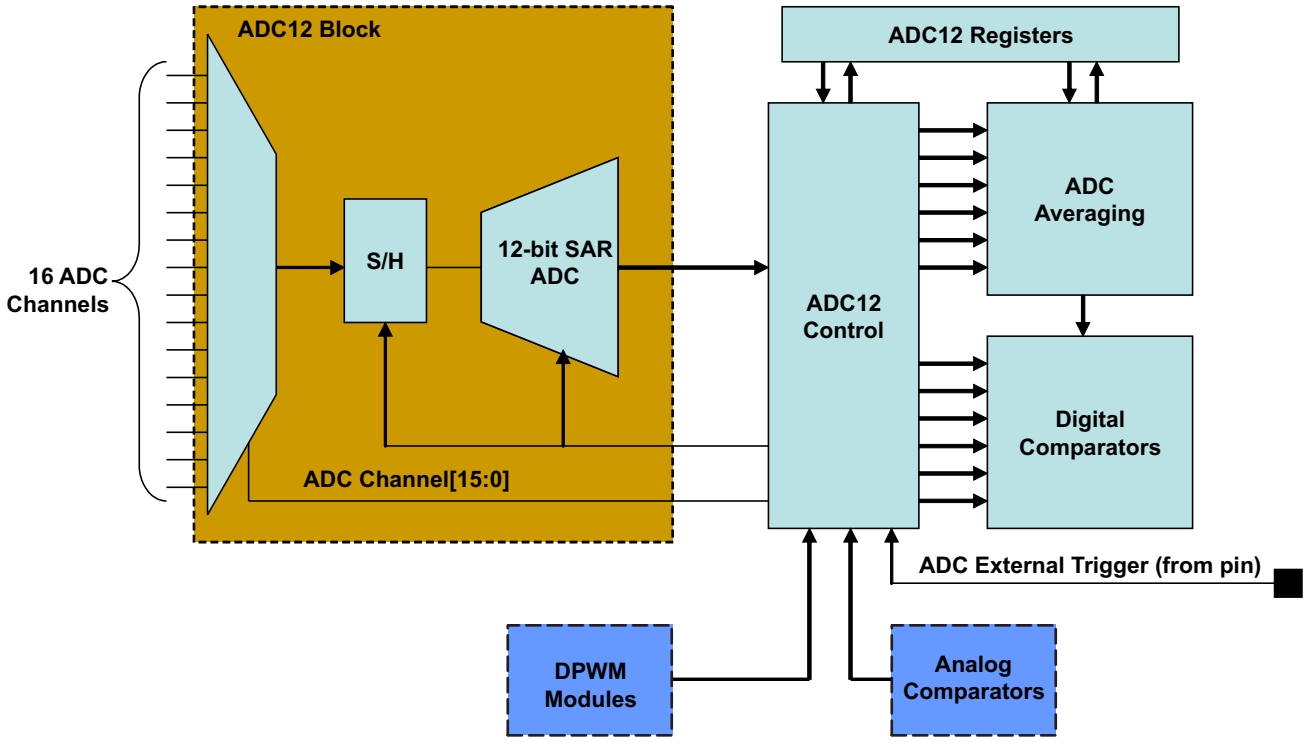


**Figure 4-4. ADC12 Control Block Diagram**

### *4.15.4 Timers*

External to the Fusion Digital Power Peripherals there are 3 different types of timers in UCD3138. They are the 24-bit timer, 16-bit timer and the Watchdog timer

#### 4.15.4.1 24-bit PWM Timer

There is one 24 bit counter PWM timer which runs off the Interface Clock and can further be divided down by an 8-bit pre-scalar to generate a slower PWM time period. The timer has two compare registers (Data Registers) for generating the PWM set/unset events. Additionally, the timer has a shadow register (Data Buffer register) which can be used to store CPU updates of the compare events while still using the timer. The selected shadow register update mode happens after the compare event matches.

The two capture pins TCMP0 and TCMP1 are inputs for recording a capture event. A capture event can be set either to rising, falling, or both edges of the capture pin. Upon this event, the counter value is stored in the corresponding capture data register.

The counter reset can be configured to happen on a counter roll over, a compare equal event, or by software controlled register. Five Interrupts from the PWM timer can be set, which are the counter rollover event (overflow), either capture event 0 or 1, or the two comparison match events. Each interrupt can be disabled or enabled.

Upon an event comparison on only the second event, the TCMP pin can be configured to set, clear, toggle or have no action at the output. The value of PWM pin output can be read for status or simply configured as general purpose I/O for reading the value of the input at the pin. The first compare event can only be used as an interrupt.

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#### 4.15.4.2 16-Bit PWM Timers

There are four 16 bit counter PWM timers which run off the Interface Clock and can further be divided down by a 8-bit pre-scaler to generate slower PWM time periods. Each timer has two compare registers (Data Registers) for generating the PWM set/unset events. Additionally, each timer has a shadow register (Data Buffer register) which can be used to store CPU updates of compare events while still using the timer. The selected shadow register update mode happens after the compare event matches.

The counter reset can be configured to happen on a counter roll over, a compare equal event, or by a software controlled register. Interrupts from the PWM timer can be set due to the counter rollover event (overflow) or by the two comparison match events. Each comparison match and the overflow interrupts can be disabled or enabled.

Upon an event comparison, the PWM pin can be configured to set, clear, toggle or have no action at the output. The value of PWM pin output can be read for status or simply configured as General Purpose I/O for reading the value of the input at the pin.

#### 4.15.4.3 Watchdog Timer

A watchdog timer is provided on the device for ensuring proper firmware loop execution. The timer is clocked off of a separate low speed oscillator source for providing a timeout range between 10 ms and 1.3 s. If the timer is allowed to expire, a reset condition is issued to the ARM processor. The watchdog is reset by a simple CPU write bit to the watchdog key register by the firmware routine. On device power-up the watchdog is disabled. Yet after it is enabled, the watchdog cannot be disabled by firmware. Only a device reset can put this bit back to the default disabled state. A half timer flag is also provided for status monitoring of the watchdog.

### 4.16 Miscellaneous Analog

The Miscellaneous Analog Control (MAC) Registers are a catch-all of registers that control and monitor a wide variety of functions. These functions include device supervisory features such as Brown-Out and power saving configuration, general purpose input/output configuration and interfacing, internal temperature sensor control and current sharing control.

The MAC module also provides trim signals to the oscillator and AFE blocks. These controls are usually used at the time of trimming at manufacturing; therefore this document will not cover these trim controls.

The MAC registers and peripherals are all available in the UCD3138 (64 pin version). Other UCD31xx devices may have reduced resources. See the device pin out description for details.

### 4.17 Package ID Information

Package ID register includes information regarding the package type of the device and can be read by firmware for reporting through PMBus or for other package sensitive decisions.

| BIT NUMBER | 1:0 |
|---|---|
| Bit Name | PKG_ID |
| Access | R/W |
| Default | 00 |

### 4.18 Brownout

Brownout function is used to determine if the device supply voltage is lower than a threshold voltage, a condition that may be considered unsafe for proper operation of the device.

The brownout threshold is higher than the reset threshold voltage; therefore, when the supply voltage is lower than brownout threshold, it still does not necessarily trigger a device reset.

The brownout interrupt flag can be polled or alternatively can trigger an interrupt to service such case by an interrupt service routine. Please see the Power On Reset (POR) / Brown Out Reset (BOR) section.


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## 4.19 Global I/O

Up to 30 pins in UCD31xx can be configured to serve as a general purpose input or output pin (GPIO). This includes all digital input or output pins except for the RESET pin.

The pins that cannot be configured as GPIO pins are the supply pins, ground pins, ADC-12 analog input pins, EADC analog input pins and the RESET pin.

There are two ways to configure and use the digital pins as GPIO pins:

1. Through the centralized Global I/O control registers.
2. Through the distributed control registers in the specific peripheral that shares it pins with the standard GPIO functionality.

The Global I/O registers offer full control of:

1. Configuring each pin as a GPIO.
2. Setting each pin as input or output.
3. Reading the pin's logic state, if it is configured as an input pin.
4. Setting the logic state of the pin, if it is configured as an output pin.
5. Connecting pin/pins to high rail through internal pull up resistors.

The Global I/O registers include Global I/O EN register, Global I/O OE Register, Global I/O Open Drain Control Register, Global I/O Value Register and Global I/O Read Register.

The following is showing the format of Global I/O EN Register (GLBIOEN) as an example:

| **BIT NUMBER** | **29:0** |
|---|---|
| **Bit Name** | GLOBAL_IO_EN |
| **Access** | R/W |
| **Default** | 00_0000_0000_0000_0000_0000_0000_0000 |

**Bits 29-0: GLOBAL_IO_EN –** This register enables the global control of digital I/O pins
0 = Control of IO is done by the functional block assigned to the IO (Default)
1 = Control of IO is done by Global IO registers.

| **BIT** | **PIN_NAME** | **PIN NUMBER** | |
|---|---|---|---|
| | | **UCD3138-64 PIN** | **UCD3138-40 PIN** |
| 29 | FAULT[3] | 43 | NA |
| 28 | ADC_EXT_TRIG | 12, 26 | 8 |
| 27 | TCK | 37 | 21 |
| 26 | TDO | 38 | 20 |
| 25 | TMS | 40 | 24 |
| 24 | TDI | 39 | 23 |
| 23 | SCI_TX[1] | 29 | NA |
| 22 | SCI_TX[0] | 14 | 22 |
| 21 | SCI_RX[1] | 30 | NA |
| 20 | SCI_RX[0] | 13 | 23 |
| 19 | TMR_CAP | 12, 26, 41 | 8, 21 |
| 18 | TMR_PWM[1] | 32 | NA |
| 17 | TMR_PWM[0] | 12, 26, 31, 37 | 21 |
| 16 | PMBUS-CLK | 15 | 9 |
| 15 | PMBUS-DATA | 16 | 10 |
| 14 | CONTROL | 30 | 20 |
| 13 | ALERT | 29 | 19 |
| 12 | EXT_INT | 26, 34 | NA |

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| BIT | PIN_NAME | PIN NUMBER | |
|---|---|---|---|
| | | UCD3138-64 PIN | UCD3138-40 PIN |
| 11 | FAULT[2] | 42 | 25 |
| 10 | FAULT[1] | 36 | 23 |
| 9 | FAULT[0] | 35, 39 | 22 |
| 8 | SYNC | 12, 26,37 | 8, 21 |
| 7 | DPWM3B | 24 | 18 |
| 6 | DPWM3A | 23 | 17 |
| 5 | DPWM2B | 22 | 16 |
| 4 | DPWM2A | 21 | 15 |
| 3 | DPWM1B | 20 | 14 |
| 2 | DPWM1A | 19 | 13 |
| 1 | DPWM0B | 18 | 12 |
| 0 | DPWM0A | 17 | 11 |

## 4.20 Temperature Sensor Control

Temperature sensor control register provides internal temperature sensor enabling and trimming capabilities. The internal temperature sensor is disabled as default.

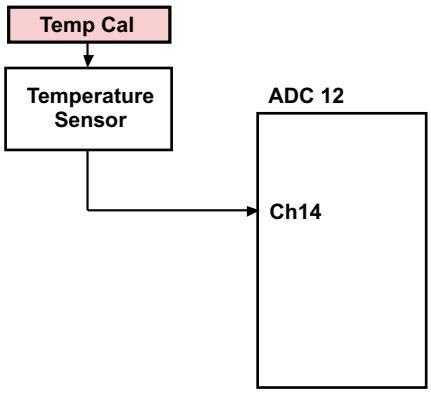


**Figure 4-5. Internal Temp Sensor**

Temperature sensor is calibrated at room temperature (25 °C) via a calibration register value.

The temperature sensor is measured using ADC12 (via Ch14). The temperature is then calculated using a mathematical formula involving the calibration register (this effectively adds a delta to the ADC measurement).

The temperature sensor can be enabled or disabled.

## 4.21 I/O Mux Control

In different packages of UCD3138 several I/O functions are multiplexed and routed toward a single physical pin. I/O Mux Control register may be used in order to choose a single specific functionality that is desired to be assigned to a physical device pin for your application.


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### 4.21.1 JTAG Use for I/O and JTAG Security

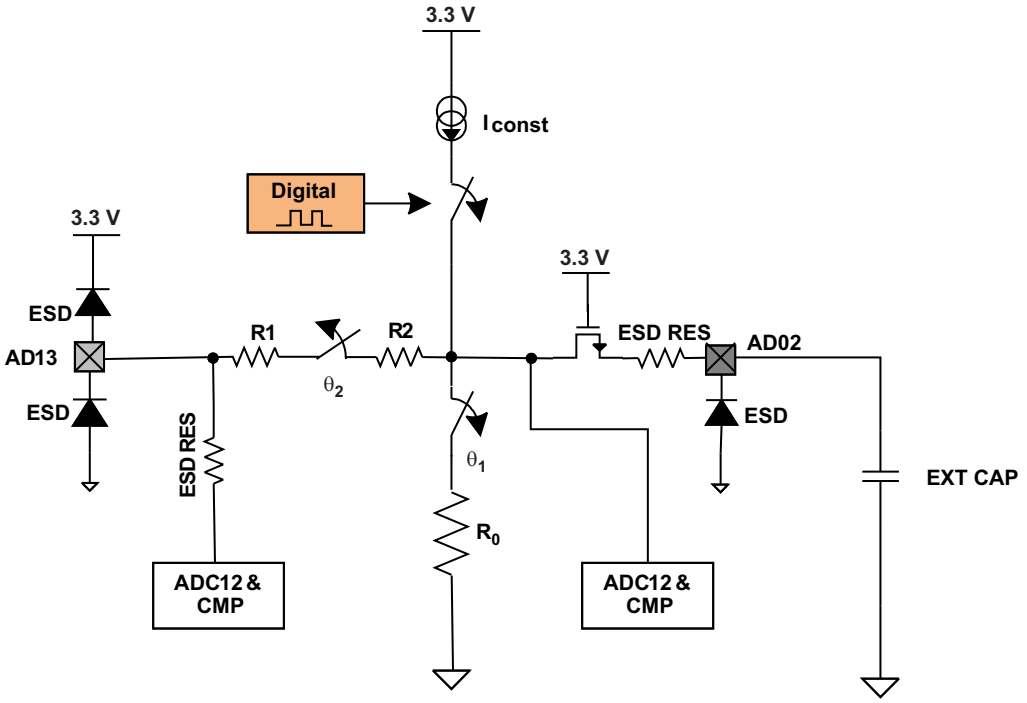
The UCD3138 provides a JTAG interface for debugging and for uploading data and programs. The pins are multiplexed with other pins, and will not be available in certain topologies. For power supplies, other debugging techniques (PMBus, UART, code instrumentation) are often superior to JTAG. Code downloading is much faster via PMBus, or with a user boot program via UART. PMBus support is available from TI. JTAG for debugging has limited support from TI's Code Composer Studio. JTAG parameter download may be supported by third parties.

## 4.22 Current Sharing Control

UCD3138 provides three separate modes of current sharing operation.

- Analog bus current sharing
- PWM bus current sharing
- Master/Slave current sharing

The simplified current sharing circuitry is shown in the drawing below:




| CURRENT SHARING MODE | FOR TEST ONLY, ALWAYS KEEP 00 | CS_MODE | EN_SW1 | EN_SW2 | DPWM |
|---|---|---|---|---|---|
| Off or Slave Mode (3-state) | 00 | 00 (default) | 0 | 0 | 0 |
| PWM Bus | 00 | 01 | 1 | 0 | ACTIVE |
| Off or Slave Mode (3-state) | 00 | 10 | 0 | 0 | 0 |
| Analog Bus or Master | 00 | 11 | 0 | 1 | 0 |

The period and the duty of 8-bit PWM current source and the state of the SW1 and SW2 switches can be controlled through the current sharing control register (CSCTRL).

## 4.23 Temperature Reference

The temperature reference register (TEMPREF) provides the ADC12 count when ADC12 measures the internal temperature sensor (channel 14) during the factory trim and calibration.

This information can be used by different periodic temperature compensation routines implemented in the firmware. But it should not be overwritten by firmware, otherwise this factory written value will be lost.

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## 4.24 Power Disable Control or (Clock Gating Control)

Power disable control register provides control bits that can enable or disable arrival of clock to several peripherals such as, PCM, CPCC, digital filters, front ends, DPWMs, UARTs, ADC-12 and more.

All these controls are enabled as default. If a specific peripheral is not used in a specific application the clock gate can be disabled in order to block the propagation of clock signal to that peripheral and therefore reduce the overall current consumption of the device.


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# 5 IC Grounding and Layout Recommendations

- Two grounds are recommended: AGND (analog) and DGND (digital).
  - AGND plane should be on a different layer than DGND, and right under the UCD3xxx device.
  - UCD3xxx power pad should be tied to AGND plane by at least 4 vias
  - AGND plane should be just large enough to connect to all required components.
  - Power ground (PGND) can be independent or combined with DGND
- Both 3.3VD and 3.3VA should have a local 0.1µF capacitor placed as close as possible to the device pins
- BPCAP decoupling (2.2 µF typically) MUST be connected to DGND
- All analog signal filter capacitors should be tied to AGND
  - If the UCD7201 or UCD7100 driver is used, the filter capacitor for the current sensing pin can be tied to DGND for easy layout
- All digital signals, such as GPIO, PMBus and PWM are referenced to DGND.
- The RESET pin capacitor (0.1µF) should be connected to either DGND or AGND locally. A 10kΩ pull-up resistor to 3.3V is recommended.
- All filter and decoupling capacitors should be placed close to UCD3xxx as possible
  - Resistor placement is less critical and can be moved a little further away
- The DGND and AGND net-short resistor MUST be placed right between one UCD3xxx's DGND pin and one AGND pin. Ground connections to the net short element should be made by a large via (or multiple paralleled vias) for each terminal of the net-short element.
- If a UCD7201 or UCD7100 device is on the control card and there is a PGND connection, a net-short resistor should be tied to the DGND plane and PGND plane by multiple vias. In addition the net-short element should be close to the driver IC.
  - The power pad of the driver IC should be tied to DGND

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# 6 References

1. Programmer's Manual
2. ARM Documentation
3. Fusion Digital Power Designer
4. PMBus Standards
5. SMBus Standards


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# 7 Mechanical Data

Mechanical data is appended to the core document when published.

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## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (March 2012) to Revision A | Page |
|---|---|
| • Added Production Data statement to footnote and removed "Product Preview" banner | 6 |


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| UCD3138RGCR | ACTIVE | VQFN | RGC | 64 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| UCD3138RGCT | ACTIVE | VQFN | RGC | 64 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| UCD3138RHAR | PREVIEW | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| UCD3138RHAT | PREVIEW | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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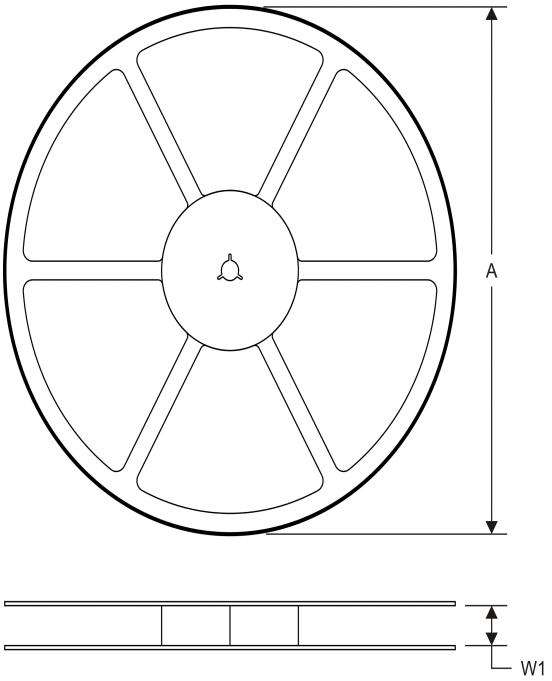
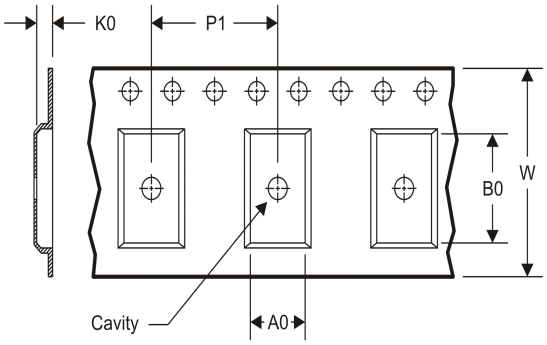
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



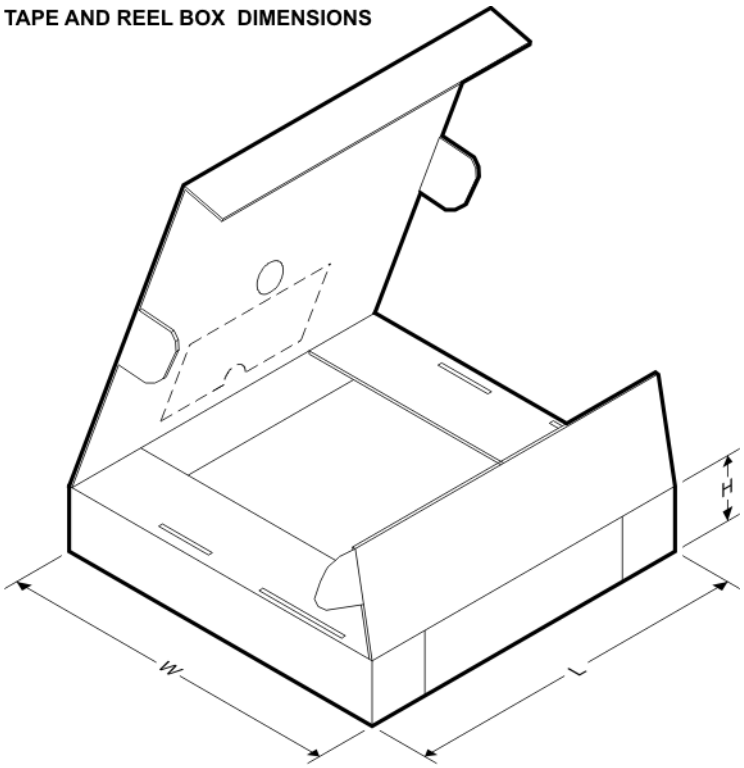

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UCD3138RGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| UCD3138RGCT | VQFN | RGC | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |

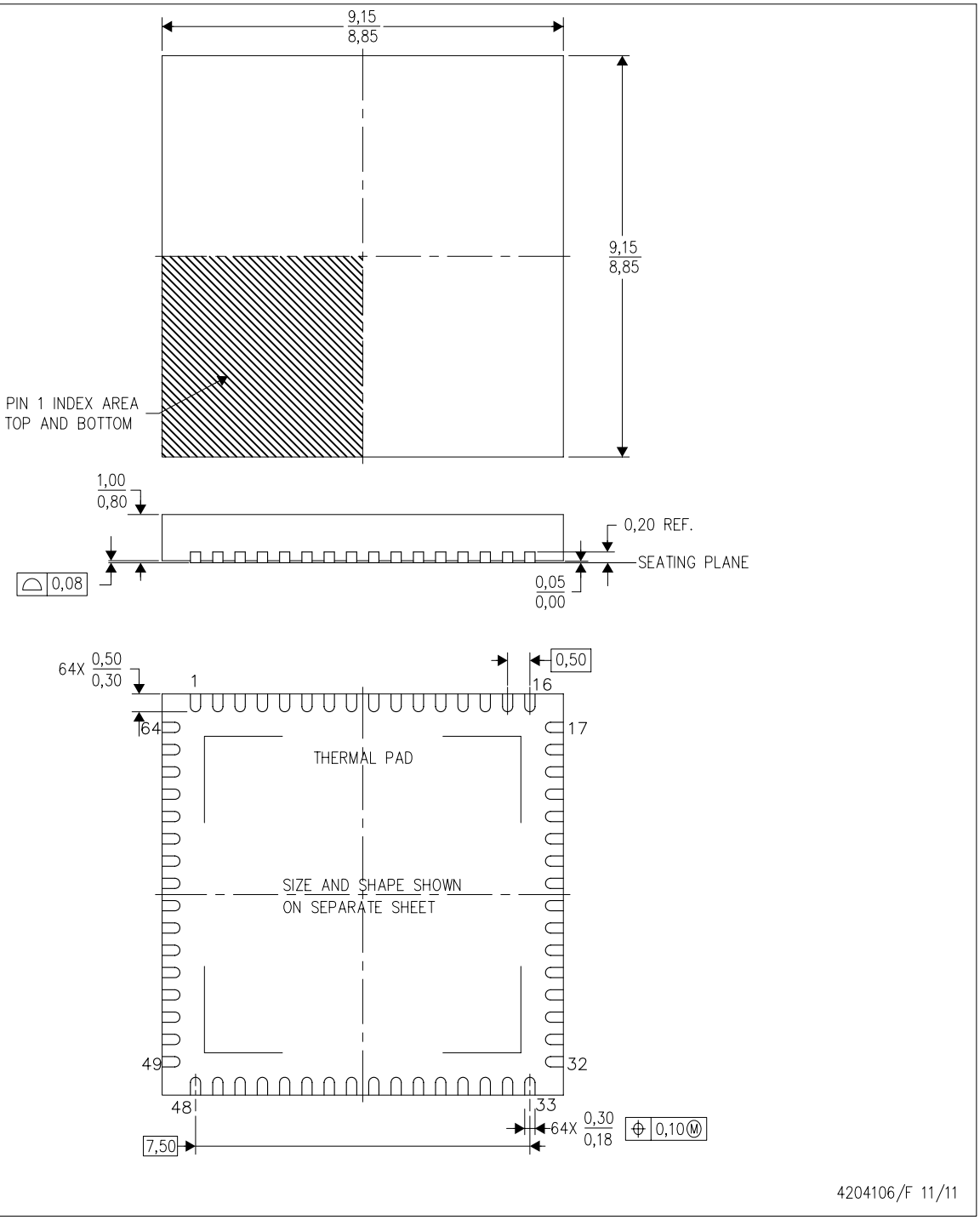
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UCD3138RGCR | VQFN | RGC | 64 | 2000 | 346.0 | 346.0 | 33.0 |
| UCD3138RGCT | VQFN | RGC | 64 | 250 | 210.0 | 185.0 | 35.0 |

RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

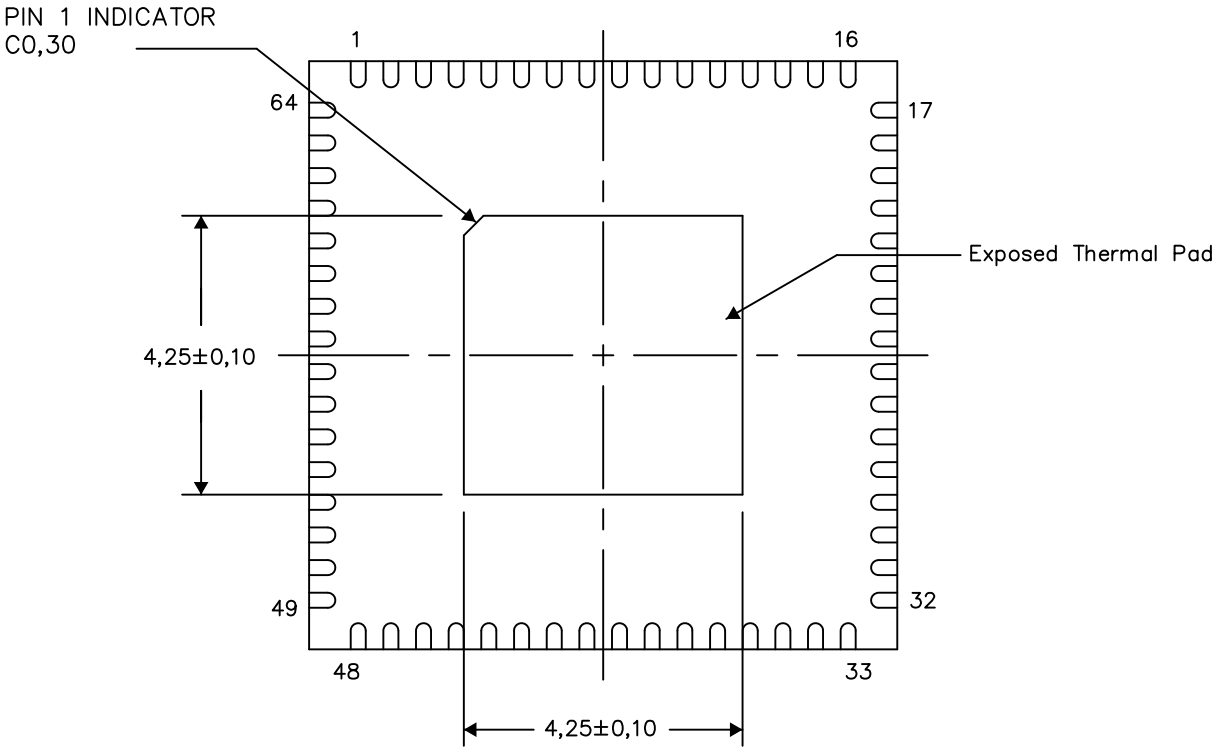
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



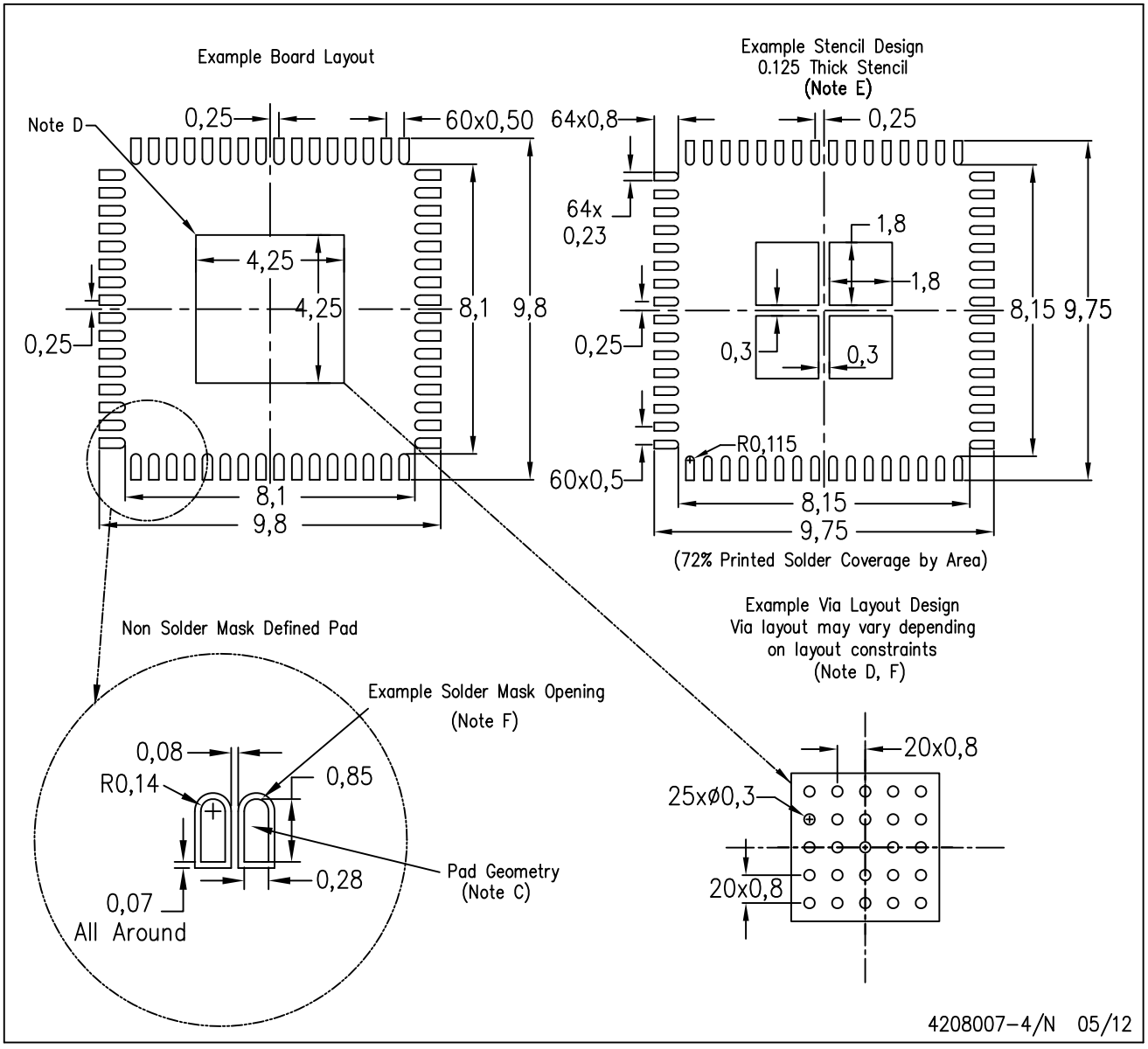

Bottom View

Exposed Thermal Pad Dimensions

4206192–3/R 05/12

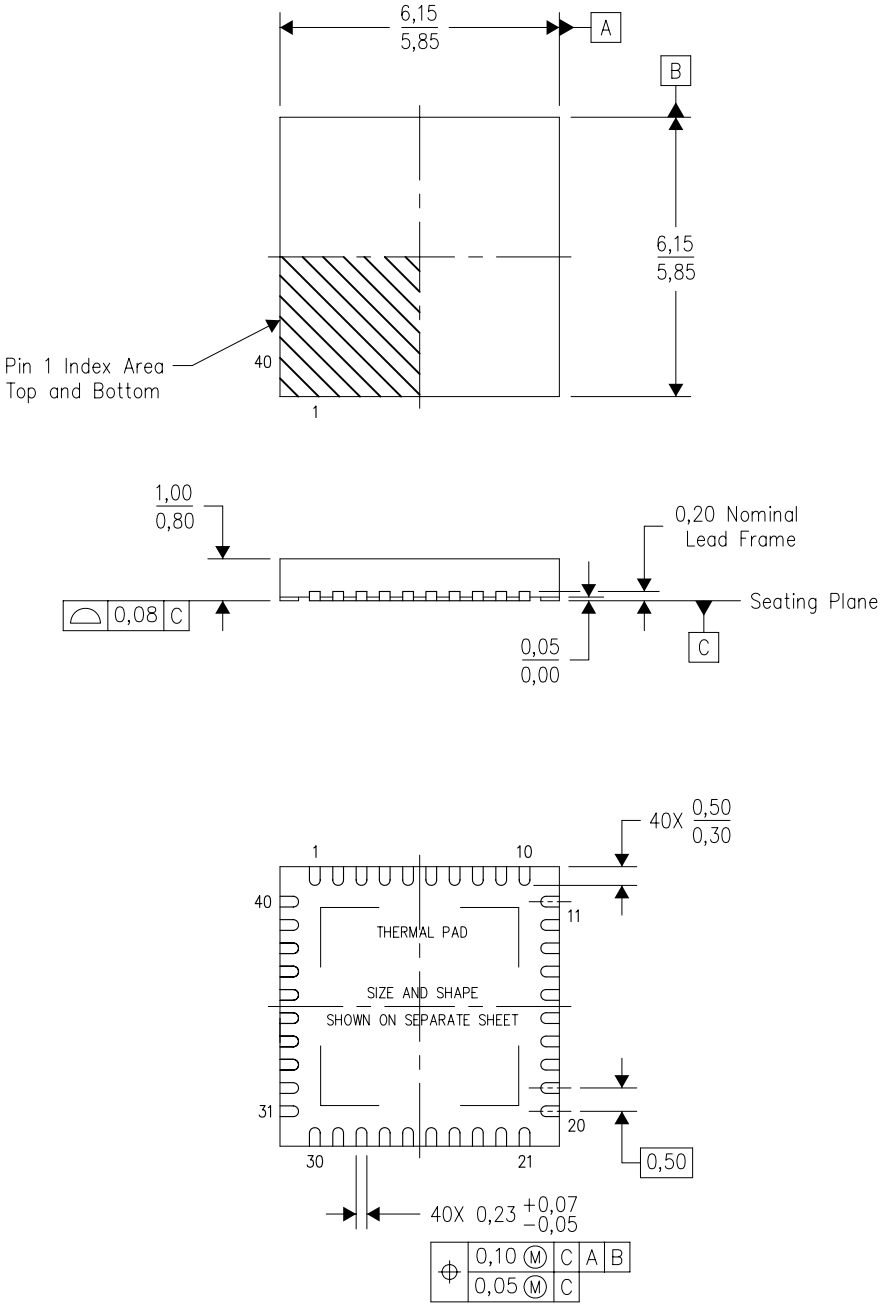
NOTE: A. All linear dimensions are in millimeters

RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD




Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

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