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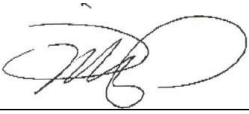
I served as Chief Examiner of the certified court interpreter test for the State of California and as a contract translator and interpreter for various federal agencies through the U.S. Department of State of for more than a decade. I served as an instructor at the University of California at Berkeley and the Middlebury Institute of International Studies at Monterey.

I have more than 30 years of experience translating and/or reviewing thousands of technical, legal, and business submitted to, among others, Korean/Japanese/Chinese judicial authorities, various U.S. federal courts, the U.S. International Trade Commission (ITC), and the USPTO Patent Trial and Appeal Board (PTAB).

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I certify under penalty of perjury that the foregoing is true and correct.

Executed this 12th day of October 2023 in the Contra Costa County of the State of California.

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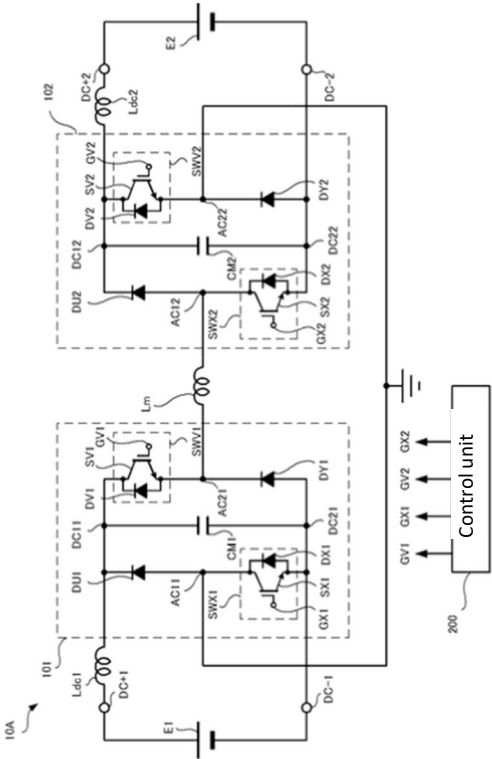
(54) (TITLE) **CURRENT-FED SERIES RESONANT DC/DC CONVERTER AND POWER CONVERSION CONTROL METHOD**

(57) (ABSTRACT)

(PROBLEM) To provide a low-loss current-fed series resonant DC/DC converter that can supply bidirectional DC power and soft switching with simple control regardless of the output voltage of the power supply.

(MEANS TO SOLVE THE PROBLEM) By turning on MERSes 101 and 102, the electrostatic energy stored in capacitors CM1 and CM2 is discharged and stored as magnetic energy in an inductor Lm, and by turning off the MERS on the power receiving side first, the magnetic energy stored in the inductor Lm is stored in the capacitor on the power receiving side, and the electrostatic energy stored in this capacitor charges the battery on the power receiving side.

(SELECTED DRAWING) FIG. 1



(CLAIMS)**(CLAIM 1)**

A current-fed series resonant DC/DC converter characterized in being provided with

first and second magnetic energy recovery switches that are provided with first and second AC terminals, first and second DC terminals, and respective current paths, that turn on and off the respective current path in response to a respectively supplied control signal, and that are configured from first and second switches that conduct substantially in both directions in the respective current path when on and conduct substantially in only one direction from a prescribed end of the respective path to the other end when off, first and second rectifying elements that are each provided with a current path and conduct substantially in only one direction from a prescribed end of the current path to the other end, and a capacitor, the prescribed end of the first rectifying element and the other end of the second switch being connected to the first AC terminal, the prescribed end of the first switch and the other end of the second rectifying element being connected to the second AC terminal, the prescribed end of the capacitor, the other end of the first rectifying element and the other end of the first switch being connected to the first DC terminal, and the other end of the capacitor, the prescribed end of the second switch and the prescribed end of the second rectifying element being connected to the second DC terminal,

a first inductor in a series circuit with an external DC power source, one end of the series circuit being connected to the first DC terminal of the first magnetic energy recovery switch and the other end of the series circuit being connected to the second DC terminal of the first magnetic energy recovery switch,

a second inductor in a series circuit with an external DC load, one end of the series circuit being connected to the first DC terminal of the second magnetic energy recovery switch and the other end of the series circuit being connected to the second DC terminal of the second magnetic energy recovery switch,

a third inductor that stores magnetic energy by means of a current flowing between the second AC terminal of the first magnetic energy recovery switch and the first AC terminal of the second magnetic energy recovery switch and between the second AC terminal of the second magnetic energy recovery switch and the first AC terminal of the first magnetic energy recovery switch, the second AC terminal of the first magnetic energy recovery switch and the first AC terminal of the second magnetic energy recovery switch being electrically connected, and the second AC terminal of the second magnetic energy recovery switch and the first AC terminal of the first magnetic energy recovery switch being connected, and

a control means for providing, to the control terminals of the first and second switches of the first and second magnetic energy recovery switches, a control signal for turning on and a control signal for turning off the current paths of each of the first and second switches of the first and second magnetic energy recovery switches,

the control means repeating a control of turning on the first and second switches of the first and second magnetic energy recovery switches, turning off the first and second switches of the second magnetic energy recovery switch, and then turning off the first and second switches of the first magnetic energy recovery switch.

(CLAIM 2)

The current-fed series resonant DC/DC converter set forth in claim 1 characterized in that when the control means turns on the first and second switches of the first and second magnetic energy recovery switches, no current substantially flows in the third inductor, when the control means turns off the first and second switches of the first magnetic energy recovery switch, no electrostatic energy is substantially stored in the capacitor of the first magnetic energy recovery switch, and when the control means turns off the first and second switches of the second magnetic energy recovery switch, no electrostatic energy is substantially stored in the capacitor of the second magnetic energy recovery switch.

(CLAIM 3)

The current-fed series resonant DC/DC converter set forth in claim 1 or 2 characterized in that

the control means repeats a control of turning on the first and second switches of the first and second magnetic energy recovery switches at substantially the same timing, turning off the first and second switches of the second magnetic energy recovery switch after a first predetermined time elapses, turning off the first and second switches of the first magnetic energy recovery switch after a further second predetermined time elapses, and holding the first and second switches off during a further third predetermined time.

(CLAIM 4)

The current-fed series resonant DC/DC converter set forth in claim 1 or 2 characterized in that

- the first and second rectifying elements of the first and second magnetic energy recovery switches are configured from a third and fourth switch, respectively,
- the third and fourth switches are each equipped with a current path and are switches that turn on and off the respective current paths in response to a control signal supplied to each of them, causing the respective current paths to conduct substantially in both directions when turned on and substantially in only one direction from one predetermined end of the current path to the other when turned off,
- the control means provides control signals to turn on and turn off the current paths of the first to fourth switches of the first and second magnetic energy recovery switches to the control terminals of the first to fourth switches, and repeats alternately
- a control of turning on the first and second switches of the first and second magnetic energy recovery switches, turning off the first and second switches of the second magnetic energy recovery switch, and then turning off the first and second switches of the first magnetic energy recovery switch, and
- a control of turning on the third and fourth switches of the first and second magnetic energy recovery switches, turning off the third and fourth switches of the second magnetic energy recovery switch, and then turning off the third and fourth switches of the first magnetic energy recovery switch.

(CLAIM 5)

The current-fed series resonant DC/DC converter set forth in claim 4 characterized in that

- the control means alternately repeats
- a control of turning on the first and second switches of the first and second magnetic energy recovery switches at substantially the same timing, turning off the first and second switches of the second magnetic energy recovery switch after a first predetermined time elapses, turning off the first and second switches of the first magnetic energy recovery switch after a further second predetermined time elapses, and holding the first to fourth switches off during a further third predetermined time, and
- a control of turning on the third and fourth switches of the first and second magnetic energy recovery switches at substantially the same timing, turning off the third and fourth switches of the second magnetic energy recovery switch after a first predetermined time elapses, turning off the third and fourth switches of the first magnetic energy recovery switch after a further second predetermined time elapses, and holding the first to fourth switches off during a further third predetermined time.

(CLAIM 6)

The current-fed series resonant DC/DC converter set forth in claim 3 or 5 characterized in being further provided with an adjustment means for adjusting the third predetermined time.

(CLAIM 7)

The current-fed series resonant DC/DC converter set forth in any of claims 1 to 6 characterized in that the third inductor is configured from a fourth inductor connected between the second AC terminal of the first magnetic energy recovery switch and the first AC terminal of the second magnetic energy recovery switch and a fifth inductor connected between the second AC terminal of the second magnetic energy recovery switch and the first AC terminal of the first magnetic energy recovery switch.

(CLAIM 8)

The current-fed series resonant DC/DC converter set forth in any of claims 1 to 7 characterized in being further provided with

a transformer configured from a first coil connected to the first and second AC terminals of the first magnetic energy recovery switch and a second coil connected to the first and second AC terminals of the second magnetic energy recovery switch and electromagnetically coupled to the first coil,

the third inductor being a leak third inductance of the transformer.

(CLAIM 9)

The current-fed series resonant DC/DC converter set forth in any of claims 1 to 8 characterized in that

the first inductor is configured from a sixth inductor connected between one end of the DC power supply and the first DC terminal of the first magnetic energy recovery switch and a seventh inductor connected between the other end of the DC power supply and the second DC terminal of the first magnetic energy recovery switch, and

the second inductor is configured from an eighth inductor connected between one end of the DC load and the first DC terminal of the second magnetic energy recovery switch and a ninth inductor connected between the other end of the DC load and the second DC terminal of the second magnetic energy recovery switch.

(CLAIM 10)

The current-fed series resonant DC/DC converter set forth in any of claims 1 to 9 characterized in that

the resonant frequency of the first inductor and the capacitor of the first magnetic energy recovery switch and the resonant frequency between the second inductor and the capacitor of the second magnetic energy recovery switch are both no greater than half of the frequency with which the control means repeats the control.

(CLAIM 11)

The current-fed series resonant DC/DC converter set forth in any of claims 1 to 10 characterized in that

one end of the DC power supply and one end of the DC load or the other end of the DC power supply and the other end of the DC load are connected to a common ground line.

(CLAIM 12)

The current-fed series resonant DC/DC converter set forth in any of claims 1 to 11 characterized in being further provided with

a third rectifying element that interrupts the current flowing in the direction from the first DC terminal of the first magnetic energy recovery switch to one end of the DC power supply, and

a fourth rectifying element that interrupts the current flowing in the direction from one end of the DC load to the first DC terminal of the second magnetic energy recovery switch.

(CLAIM 13)

A current-fed series resonant DC/DC converter characterized in being provided with

a magnetic energy recovery switch that is provided with first and second AC terminals, first and second DC terminals, and respective current paths, that turns on and off the respective current paths in response to a respectively supplied control signal, and that is configured from first and second switches that conduct substantially in both directions in the respective current path when on and conduct substantially in only one direction from a prescribed end of the respective current path to the other end when off, first and second rectifying elements that are each provided with a current path and conduct substantially in only one direction from a prescribed end of the current path to the other end, and a capacitor, the prescribed end of the first rectifying element and the other end of the second switch being connected to the first AC terminal, the prescribed end of the first switch and the other end of the second rectifying element being connected to the second AC terminal, the prescribed end of the capacitor, the other end of the first rectifying element and the other end of the first switch being connected to the first DC terminal, and the other end of the capacitor, the prescribed end of the second switch and the prescribed end of the second rectifying element being connected to the second DC terminal,

a rectifier provided with first and second AC inputs and first and second DC outputs for rectifying power input from between the first and second AC inputs and outputting from between the first and second AC outputs,

a first inductor in a series circuit with an external DC power source, one end of the series circuit being connected to the first DC terminal of the magnetic energy recovery switch and the other end of the series circuit being connected to the second DC terminal of the magnetic energy recovery switch,

a second inductor in a series circuit with an external DC load, one end of the series circuit being connected to the first DC output of the rectifier and the other end of the series circuit being connected to the second DC output of the rectifier,

a third inductor that stores magnetic energy by means of a current flowing between the second AC terminal of the magnetic energy recovery switch and the first AC input of the rectifier and between the second AC input of the rectifier and the first AC terminal of the magnetic energy recovery switch, the second AC terminal of the magnetic energy recovery switch and the first AC input of the rectifier being electrically connected, and the second AC input of the rectifier and the first AC terminal of the magnetic energy recovery switch being connected, and

a control means for providing, to the control terminals of the first and second switches of the magnetic energy recovery switch, a control signal for turning on and a control signal for turning off the current paths of each of the first and second switches of the magnetic energy recovery switch,

the control means repeating a control for simultaneously turning on and off the first and second switches of the magnetic energy recovery switch.

(CLAIM 14)

A power conversion control method that controls a power converter comprising

first and second magnetic energy recovery switches that are provided with first and second AC terminals, first and second DC terminals, and respective current paths, that turn on and off the respective current path in response to a respectively supplied control signal, and that are configured from first and second switches that conduct substantially in both directions in the respective current path when on and conduct substantially in only one direction from a prescribed end of the respective path to the other end when off, first and second rectifying elements that are each provided with a current path and conduct substantially in only one direction from a prescribed end of the current path to the other end, and a capacitor, the prescribed end of the first rectifying element and the other end of the second switch being connected to the first AC terminal, the prescribed end of the first switch and the other end of the second rectifying element being connected to the second AC terminal, the prescribed end of the capacitor, the other end of the first rectifying element and the other end of the first switch being connected to the first DC terminal, and the other end of the capacitor, the prescribed end of the second switch and the prescribed end of the second rectifying element being connected to the second DC terminal,

a first inductor in a series circuit with an external DC power source, one end of the series circuit being connected to the first DC terminal of the first magnetic energy recovery switch and the other end of the series circuit being connected to the second DC terminal of the first magnetic energy recovery switch,

a second inductor in a series circuit with an external DC load, one end of the series circuit being connected to the first DC terminal of the second magnetic energy recovery switch and the other end of the series circuit being connected to the second DC terminal of the second magnetic energy recovery switch, and

a third inductor that stores magnetic energy by means of a current flowing between the second AC terminal of the first magnetic energy recovery switch and the first AC terminal of the second magnetic energy recovery switch and between the second AC terminal of the second magnetic energy recovery switch and the first AC terminal of the first magnetic energy recovery switch, the second AC terminal of the first magnetic energy recovery switch and the first AC terminal of the second magnetic energy recovery switch being electrically connected, and the second AC terminal of the second magnetic energy recovery switch and the first AC terminal of the first magnetic energy recovery switch being connected,

said power conversion control method being characterized by
repeating a control of turning on the first and second switches of the first and second magnetic energy recovery switches, turning off the first and second switches of the second magnetic energy recovery switch, and then turning off the first and second switches of the first magnetic energy recovery switch.

(DETAILED DESCRIPTION OF THE INVENTION)

(TECHNICAL FIELD)

(0001)

The present invention relates to a current-fed series resonant DC/DC converter and a power conversion control method.

(BACKGROUND ART)

(0002)

The magnetic energy recovery switch (MERS) is known as a low-loss switch capable of recovering magnetic energy stored in an inductive load.

Patent Document 1, for example, discloses a low-loss DC/AC power converter uses this MERS to supply AC power from a DC voltage source to a load or DC power from an AC voltage source to a load.

(0003)

This DC/AC power conversion device is equipped with a MERS, an AC inductor connected between the AC terminals of the MERS to form a series circuit with an AC power source or an AC load, and a DC inductor connected between the DC terminals of the MERS to form a series circuit with a DC power source or a DC load.

This DC/AC power converter can charge a secondary battery from an AC power source or supply AC power from a secondary battery to a load by turning on and off a reverse-conducting semiconductor switch in the MERS.

(0004)

(PRIOR ART DOCUMENTS)

(PATENT DOCUMENTS)

(Patent Document 1) Patent Appl. Publication No. JP 2008-193817

(SUMMARY OF THE INVENTION)

(PROBLEM THE INVENTION IS TO SOLVE)

(0005)

However, when converting DC power in order to, for example, charge from one secondary battery to another secondary battery, it is desirable to be able to convert the power reversibly. Nevertheless, it is difficult for the DC/AC power conversion device of Patent Document 1 to convert DC power reversibly with simple control even if the secondary batteries are connected through a rectifier as an AC load and even if the secondary batteries are connected via an inverter as an AC power source. Therefore, there is room for improvement in terms of reversible conversion of DC power for power conversion devices that use MERS for DC/DC conversion, while retaining the advantage of soft-switching capability with simple control of MERS.

(0006)

The present invention was devised after taking these problems into account. It is an object of the present invention to provide a low-loss current-fed series resonant DC/DC converter capable of the bidirectional conversion of power in the mutual coupling of two DC voltage sources, regardless of the output voltage thereof, and of soft switching with simple control, and it is another object of the present invention to provide a power conversion control device and a power conversion control method to achieve such a current-fed series resonant DC/DC converter.

(MEANS TO SOLVE THE PROBLEM)

(0007)

In order to achieve the above objects, the current-fed series resonant DC/DC converter according to the first aspect of the present invention is characterized in being provided with

first and second magnetic energy recovery switches that are provided with first and second AC terminals, first and second DC terminals, and respective current paths, that turn on and off the respective current path in response to a respectively supplied control signal, and that are configured from first and second switches that conduct substantially in both directions in the respective current path when on and conduct substantially in only one direction from a prescribed end of the respective path to the other end when off, first and second rectifying elements that are each provided with a current path and conduct substantially in only one direction from a prescribed end of the current path to the other end, and a capacitor, the prescribed end of the first rectifying element and the other end of the second switch being connected to the first AC terminal, the prescribed end of the first switch and the other end of the second rectifying element being connected to the second AC terminal, the prescribed end of the capacitor, the other end of the first rectifying element and the other end of the first switch being connected to the first DC terminal, and the other end of the capacitor, the prescribed end of the second switch and the prescribed end of the second rectifying element being connected to the second DC terminal,

a first inductor in a series circuit with an external DC power source, one end of said series circuit being connected to the first DC terminal of the first magnetic energy recovery switch and the other end of said series circuit being connected to the second DC terminal of the first magnetic energy recovery switch,

a second inductor in a series circuit with an external DC load, one end of said series circuit being connected to the first DC terminal of the second magnetic energy recovery switch and the other end of said series circuit being connected to the second DC terminal of the second magnetic energy recovery switch,

a third inductor that stores magnetic energy by means of a current flowing between the second AC terminal of the first magnetic energy recovery switch and the first AC terminal of the second magnetic energy recovery switch and between the second AC terminal of the second magnetic energy recovery switch and the first AC terminal of the first magnetic energy recovery switch, the second AC terminal of the first magnetic energy recovery switch and the first AC terminal of the second magnetic energy recovery switch being electrically connected, and the second AC terminal of the second magnetic energy recovery switch and the first AC terminal of the first magnetic energy recovery switch being connected, and

a control means for providing, to the control terminals of the first and second switches of the first and second magnetic energy recovery switches, a control signal for turning on and a control signal for turning off the current paths of each of the first and second switches of the first and second magnetic energy recovery switches,

the control means repeating

a control of turning on the first and second switches of the first and second magnetic energy recovery switches, turning off the first and second switches of the second magnetic energy recovery switch, and then turning off the first and second switches of the first magnetic energy recovery switch.

(0008)

In order to achieve the above objects, the current-fed series resonant DC/DC converter according to the second aspect of the present invention is characterized in being provided with

magnetic energy recovery switches that are provided with first and second AC terminals, first and second DC terminals, and respective current paths, that turn on and off the respective current path in response to a respectively supplied control signal, and that are configured from first and second switches that conduct substantially in both directions in the respective current path when on and conduct substantially in only one direction from a prescribed end of the respective path to the other end when off, first and second rectifying elements that are each provided with a current path and conduct substantially in only one direction from a prescribed end of the current path to the other end, and a capacitor, the prescribed end of the first rectifying element and the other end of the second switch being connected to the first AC terminal, the prescribed end of the first switch and the other end of the second rectifying element being connected to the second AC terminal, the prescribed end of the capacitor, the other end of the first rectifying element and the other end of the first switch being connected to the first DC terminal, and the other end of the capacitor, the prescribed end of the second switch and the prescribed end of the second rectifying element being connected to the second DC terminal,

a rectifier provided with first and second AC inputs and first and second DC outputs for rectifying power input from between the first and second AC inputs and outputting from between the first and second AC outputs,

a first inductor in a series circuit with an external DC power source, one end of the series circuit being connected to the first DC terminal of the magnetic energy recovery switch and the other end of the series circuit being connected to the second DC terminal of the magnetic energy recovery switch,

a second inductor in a series circuit with an external DC load, one end of the series circuit being connected to the first DC output of the rectifier and the other end of the series circuit being connected to the second DC output of the rectifier,

a third inductor that stores magnetic energy by means of a current flowing between the second AC terminal of the magnetic energy recovery switch and the first AC input of the rectifier and between the second AC input of the rectifier and the first AC terminal of the magnetic energy recovery switch, the second AC terminal of the magnetic energy recovery switch and the first AC input of the rectifier being electrically connected, and the second AC input of the rectifier and the first AC terminal of the magnetic energy recovery switch being connected, and

a control means for providing, to the control terminals of the first and second switches of the magnetic energy recovery switches, a control signal for turning on and a control signal for turning off the current paths of each of the first and second switches of the magnetic energy recovery switches,

the control means repeating a control for simultaneously turning on and off the first and second switches of the magnetic energy recovery switches.

(0009)

In order to achieve the above objects, the power conversion control method according to the third aspect of the present invention is characterized in controlling a power converter comprising

first and second magnetic energy recovery switches that are provided with first and second AC terminals, first and second DC terminals, and respective current paths, that turn on and off the respective current path in response to a respectively supplied control signal, and that are configured from first and second switches that conduct substantially in both directions in the respective current path when on and conduct substantially in only one direction from a prescribed end of the respective path to the other end when off, first and second rectifying elements that are each provided with a current path and conduct substantially in only one direction from a prescribed end of the current path to the other end, and a capacitor, the prescribed end of the first rectifying element and the other end of the second switch being connected to the first AC terminal, the prescribed end of the first switch and the other end of the second rectifying element being connected to the second AC terminal, the prescribed end of the capacitor, the other end of the first rectifying element and the other end of the first switch being connected to the first DC terminal, and the other end of the capacitor, the prescribed end of the second switch and the prescribed end of the second rectifying element being connected to the second DC terminal,

a first inductor in a series circuit with an external DC power source, one end of said series circuit being connected to the first DC terminal of the first magnetic energy recovery switch and the other end of said series circuit being connected to the second DC terminal of the first magnetic energy recovery switch,

a second inductor in a series circuit with an external DC load, one end of said series circuit being connected to the first DC terminal of the second magnetic energy recovery switch and the other end of said series circuit being connected to the second DC terminal of the second magnetic energy recovery switch, and

a third inductor that stores magnetic energy by means of a current flowing between the second AC terminal of the first magnetic energy recovery switch and the first AC terminal of the second magnetic energy recovery switch and between the second AC terminal of the second magnetic energy recovery switch and the first AC terminal of the first magnetic energy recovery switch, the second AC terminal of the first magnetic energy recovery switch and the first AC terminal of the second magnetic energy recovery switch being electrically connected, and the second AC terminal of the second magnetic energy recovery switch and the first AC terminal of the first magnetic energy recovery switch being connected, and

repeating a control of turning on the first and second switches of the first and second magnetic energy recovery switches, turning off the first and second switches of the second magnetic energy recovery switch, and then turning off the first and second switches of the first magnetic energy recovery switch.

(EFFECT OF THE INVENTION)

(0010)

According to the present invention, a low-loss current-fed series resonant DC/DC converter capable of the bidirectional conversion of power in the mutual coupling of two DC voltage sources, regardless of the output voltage of those sources, and of soft switching with simple control, is achieved, and a power conversion control method for achieving such a current-fed series resonant DC/DC converter is achieved.

(BRIEF DESCRIPTION OF THE DRAWINGS)

(0011)

(FIG. 1) A circuit diagram showing the configuration of the DC/DC converter of the first embodiment of the present invention.

(FIG. 2A) A circuit diagram using conventional technology for explaining the differences of the conventional DC/DC converter shown in FIG. 1.

(FIG. 2B) A circuit diagram using conventional technology for explaining the differences of the conventional DC/DC converter shown in FIG. 1.

(FIG. 2C) A circuit diagram showing a portion of the conventional DC/DC converter shown in FIG. 1 for explaining the differences of the DC/DC converter.

(FIG. 3) A drawing for explaining the operation when the MERS shown in FIG. 2C is turned off.

(FIG. 4A) A drawing for explaining an operation of turning on the MERS shown in FIG. 2C, discharging the capacitor of the MERS, and storing magnetic energy in the inductor.

(FIG. 4B) A drawing for explaining an operation in which the MERS shown in FIG. 2C is turned off and then discharge of the MERS capacitor completes.

(FIG. 4C) A drawing for explaining an operation of turning off the MERS shown in FIG. 2C and storing the magnetic energy of the inductor as electrostatic energy in the MERS capacitor.

(FIG. 4D) A drawing for explaining an operation in which the MERS shown in FIG. 2C is turned off to recover all of the magnetic energy of the inductor in the MERS.

(FIG. 5) (a) to (d) are drawings for explaining the relationship between the time variation of the current flowing in the inductor connected to the AC terminal of the MERS in FIG. 2C, the time variation of the voltage of the MERS capacitor, the time variation of the power output from the DC source connected to the MERS, and the logic state transition of the gate signals SGGV1 and SGGX1.

(FIG. 6) A drawing for explaining an operation of the DC/DC converter shown in FIG. 1 when both of the DC/DC converter MERSes are kept off.

(FIG. 7A) A drawing for explaining an operation in which both of the two MERSes of the DC/DC converter shown in FIG. 1 are turned on to discharge both of the MERS capacitors and the discharged electrostatic energy is stored as magnetic energy in the inductor.

(FIG. 7B) A drawing for explaining an operation in which both of the two MERSes of the DC/DC converter shown in FIG. 1 are turned on and then the discharge of the capacitor of the MERS on the power receiving side completes.

(FIG. 7C) A drawing for explaining an operation in which, of the two MERSes of the DC/DC converter shown in FIG. 1, only the MERS on the power receiving side is turned off and the magnetic energy of the inductor is recovered in the capacitor of the MERS on the power receiving side.

(FIG. 7D) A drawing for explaining an operation in which, of the two MERSes of the DC/DC converter shown in FIG. 1, only the MERS on the power receiving side is turned off and then the discharge of the capacitor of the MERS on the power transmission side completes.

(FIG. 7E) A drawing for explaining an operation in which both of the two MERSes of the DC/DC converter shown in FIG. 1 are turned off and the magnetic energy of the inductor is recovered in both of the MERS capacitors.

(FIG. 7F) A drawing for explaining an operation in which both of the two MERSes of the DC/DC converter shown in FIG. 1 are turned off and all of the magnetic energy of the inductor connecting the two MERS capacitors is recovered therein.

(FIG. 8A) (a) to (e) are drawings for explaining the relationship between the time variation of the two DC reactances and the current flowing in the inductor when there is a step-up conversion in the DC/DC converter of FIG. 1, the time variation of the voltages in the two MERS capacitors in the DC/DC converter, the time variation of the power supplied from the battery on the power transmission side to the battery on the power receiving side, and the logic state transition of the gate signals SGGV1 and SGGX1 and the gate signals SGGV2 and SGGX2.

(FIG. 8B) (a) to (c) are drawings for explaining the relationship between the time variation of the two DC reactances and the current flowing in the inductor when the power receiving side voltage and the power transmission side voltage are roughly equivalent in the DC/DC converter of FIG. 1, the time variation of the voltages in the two MERS capacitors in the DC/DC converter, and the logic state transition of the gate signals SGGV1 and SGGX1 and the gate signals SGGV2 and SGGX2.

(FIG. 8C) (a) to (c) are drawings for explaining the relationship between the time variation of the two DC reactances and the current flowing in the inductor when there is a step-down conversion in the DC/DC converter of FIG. 1, the time variation of the voltages in the two MERS capacitors in the DC/DC converter, the time variation of the power supplied from the battery on the power transmission side to the battery on the power receiving side, and the logic state transition of the gate signals SGGV1 and SGGX1 and the gate signals SGGV2 and SGGX2.

(FIG. 8D) (a) to c are drawings for explaining that the DC/DC converter of FIG. 1 is capable of reverse conversion.

(FIG. 9) A drawing for showing a variation of the DC/DC converter of FIG. 1.

(FIG. 10) A drawing for showing a variation of the DC/DC converter of FIG. 1.

(FIG. 11) (a) to (c) are drawings for explaining the relationship between the time variation of the two DC reactances and the current flowing in the inductor when the power receiving side voltage and the power transmission side voltage are roughly equivalent in the DC/DC converter of FIG. 10, the time variation of the voltages in the two MERS capacitors in the DC/DC converter, and the logic state transition of the gate signals SGGV1 and SGGX1 and the gate signals SGGV2 and SGGX2.

(FIG. 12) (a) to (c) are drawings for explaining the switching loss of the DC/DC converter of FIG. 1.

(FIG. 13) A circuit diagram for showing the DC/DC converter configuration of the second embodiment of the present invention.

(FIG. 14A) A drawing for explaining an operation in which the electrostatic energy stored in the two MERS capacitors of the DC/DC converter shown in FIG. 13 is discharged and the magnetic energy is stored in the inductor connecting the two MERSes.

(FIG. 14B) A drawing for explaining an operation in which the magnetic energy of the inductor is recovered in the capacitor of the MERS on the power receiving side of the two MERSes of the DC/DC converter shown in FIG. 13.

(FIG. 14C) A drawing for explaining an operation in which the magnetic energy of the inductor is recovered in the capacitors of the two MERSes of the DC/DC converter shown in FIG. 13.

(FIG. 14D) A drawing for explaining an operation in which electrostatic energy stored in the capacitor of the MERS on the power receiving side of the two MERSes of the DC/DC converter shown in FIG. 13 charges the secondary battery on the power receiving side, and the secondary battery on the power transmission side charges the capacitor of the MERS on the power transmission side.

(FIG. 14E) A drawing for explaining an operation in which electrostatic energy stored in the capacitors of the two MERSes of the DC/DC converter shown in FIG. 13 is discharged, and the current flows in the direction opposite of the current flow shown in FIG. 14A so that magnetic energy is stored in the inductor.

(FIG. 14F) A drawing for explaining an operation in which the magnetic energy of the inductor is recovered in the capacitor of the MERS on the power receiving side of the two MERSes of the DC/DC converter shown in FIG. 13.

(FIG. 14G) A drawing for explaining an operation in which the magnetic energy of the inductor is recovered in the capacitors of the two MERSes of the DC/DC converter shown in FIG. 13.

(FIG. 14H) A drawing for explaining an operation in which electrostatic energy stored in the capacitor of the MERS on the power receiving side of the two MERSes of the DC/DC converter shown in FIG. 13 charges the secondary battery on the power receiving side, and the secondary battery on the power transmission side charges the capacitor of the MERS on the power transmission side.

(FIG. 15) A drawing for showing a variation of the DC/DC converter of FIG. 13.

(FIG. 16) A drawing for showing a variation of the DC/DC converter of FIG. 13.

(FIG. 17) A drawing for showing a variation of the DC/DC converter of FIG. 13.

(FIG. 18) (a) to (d) are drawings for explaining the relationship between the time variation of the two DC reactances and the current flowing in the inductor in the DC/DC converter of FIG. 17, the time variation of the voltages in the two MERS capacitors in the DC/DC converter, and the logic state transition of the gate signals SGGV1 and SGGX1 and the gate signals SGGV2 and SGGX2.

(FIG. 19) A drawing for showing an applied example of the DC/DC converter of FIG. 13.

(FIG. 20A) (a) to (c) are drawings for explaining the relationship between the time variations of the voltages in the capacitors of the two MERSes in the DC/DC converter in FIG. 15 when the control is set to a repeat frequency of 10 kHz, the time variation of the current flowing in the inductor, and the on-off transitions of the switches.

(FIG. 20B) (a) to (c) are drawings for explaining the relationship between the time variations of the voltages in the capacitors of the two MERSes in the DC/DC converter in FIG. 15 when the control is set to a repeat frequency of 20 kHz, the time variation of the current flowing in the inductor, and the on-off transitions of the switches.

(FIG. 20C) (a) to (c) are drawings for explaining the relationship between the time variations of the voltages in the capacitors of the two MERSes in the DC/DC converter in FIG. 15 when the control is set to a repeat frequency of 6 kHz, the time variation of the current flowing in the inductor, and the on-off transitions of the switches.

(FIG. 20D) A drawing for explaining variation in the power conversion quantity per unit time in the DC/DC converter of FIG. 15 when the repeat frequency of the control is varied.

(FIG. 21) A drawing for showing a variation of the DC/DC converter of FIG. 1.

(FIG. 22) A drawing for explaining the relationship between the time variation of the two DC reactances and the current flowing in the inductor in the DC/DC converter of FIG. 21, the time variation of the voltages in the MERS capacitors in the DC/DC converter, and the logic state transition of the gate signals SGGV1 and SGGX1.

(FIG. 23) (a) and (b) are block diagrams showing a variation of the control unit.

(EMBODIMENTS)

(0012)

The DC/DC converter of the present invention uses, in series, two MERSes, which perform soft switching operations, to utilize the resonance phenomenon controlled by the gate of the current energy and the electric field energy for DC/DC power conversion.

(0013)

The embodiments of the present invention are described below with reference to the drawings and using an example of a direct current-direct current (DC/DC) converter that mutually charges two secondary batteries. This DC/DC converter is configured with two MERSes connected in series through an inductor.

(0014)

(CONFIGURATION OF FIRST EMBODIMENT)

As shown in FIG. 1, a DC/DC 10A in the first embodiment of the present invention is configured from magnetic energy recovery switches (MERSes) 101 and 102, inductors Ldc1 and Ldc2, an inductor Lm, and a control unit 200. The control unit consists of the following components

(0015)

The MERSEs 101 and 102 are, for example, unidirectional MERSEs, as shown in FIG. 1. The MERS 101 in FIG. 1 is configured from DC terminals DC11 and DC21, AC terminals AC11 and AC21, two reverse-conducting semiconductor switches SWV1 and SWX1, two diode sections DU1 and DY1, and a capacitor CM1. Similarly, the MERS 102 is configured from DC terminals DC12 and DC22, AC terminals AC12 and AC22, two reverse-conducting semiconductor switches SWV2 and SWX2, two diode sections DU2 and DY2, and a capacitor CM2.

(0016)

The reverse-conduction semiconductor switch SWV1 is configured from a diode section DV1 and a switch section SV1. Similarly, the reverse-conducting semiconductor switch SWX1 is configured from a diode section DX1 and a switch section SX1, the reverse-conducting semiconductor switch SWV2 is configured from a diode section DV2 and a switch section SV2, and the reverse-conducting semiconductor switch SWX2 is configured from a diode section DX2 and a switch section SX2.

(0017)

The switch sections SV1, SX1, SV2, and SX2 each comprises a semiconductor switching element such as a metal-oxide-silicon field effect transistor (MOSFET), an insulated gate bipolar transistor (IGBT), or a gate turn-off thyristor (GTO), and each is provided with a current path and a control terminal. When an on signal described below is supplied to each control terminal, the current path conducts, and when an off signal is supplied, the current path is interrupted.

(0018)

The diode sections DU1, DV1, DX1, DY1, DU2, DV2, DX2, and DY2 all comprise a rectifying element such as, for example, a semiconductor diode, and are provided with a current path that conducts current in only one direction. The diode sections DV1, DX1, DV2, and DX2 may be, for example, parasitic diodes of the semiconductor switches configuring the switch sections.

(0019)

Below, each diode part is described as comprising a semiconductor diode, and each switch section is described as comprising an n-channel MOSFET. In this case, the drain-source interval of the MOSFET forms the current path of the switch section, and the gate forms the control terminal.

(0020)

For each reverse-conducting semiconductor switch, the anode of the diode section is connected to the source of the switch section, the cathode of the diode section is connected to the drain of the switch section, and the current paths of the switch section and the diode section together form the current path of the reverse-conducting semiconductor switch.

As a result of this connection relationship, each reverse-conducting semiconductor switch turns the current flowing in the direction from the drain of the switch section to the source (forward direction) on and off according to the value of the signal applied to the gate of the switch section. The current flowing from the source to the drain of the switch section to the drain (reverse direction) is bypassed by the diode section, thus keeping the switch section always on.

(0021)

The anode of the diode section DU1 and the cathode of the diode section DX1 are connected at the AC terminal AC11 of the MERS 101. The anode of the diode section DV1, the cathode of the diode section DY1, and one end of the inductor Lm are connected at the AC terminal AC21.

(0022)

The cathodes of the diode sections DU1 and DV1, one end of the capacitor CM1, and one end of the inductor Ldc1 are connected at the DC terminal DC11 of the MERS101. The other end of the inductor Ldc1 forms a first DC positive terminal DC+1 of a DC/DC converter 10A. The anodes of the diode sections DX1 and DY1 and the other end of the capacitor CM1 are connected at a DC terminal DC21, and a first DC negative terminal DC-1 of the DC/DC converter 10A is formed.

(0023)

The positive electrode of an external secondary battery E1, which is a secondary battery, is connected to the DC positive terminal DC+1, and the negative electrode of a secondary battery E2 is connected to the DC negative terminal DC-1. As a result of these connections, the secondary battery E1 and the inductor Ldc1 form a series circuit. As a result, the inductor Ldc1 stably supplies power output from the secondary battery E1 to the MERS 101.

The inductor Ldc1 may be, for example, a DC reactor.

(0024)

The anode of the diode section DU2, the cathode of the diode section DX2, and the other end of inductor Lm are connected at the AC terminal AC12 of the MERS 102. The anode of the diode section DV2, the cathode of the diode section DY2, and the AC terminal AC11 of the MERS 101 are connected at the AC terminal AC22. In the present embodiment, the AC terminal AC22 is connected to a common ground wire along with the AC terminal AC11 of the MERS 101.

(0025)

The cathodes of the diode sections DU2 and DV2, one end of the capacitor CM2, and one end of the inductor Ldc2 are connected at the DC terminal DC12 of the MERS102. The other end of the inductor Ldc2 is a second DC positive terminal DC+2 of the DC/DC converter 10A. The anodes of the diode sections DX2 and DY2 and the other end of the capacitor CM2 are connected at the DC terminal DC22, and a second DC negative terminal DC-2 is formed in the DC/DC converter 10A.

(0026)

The positive electrode of the external secondary battery E2, which is a secondary battery, is connected to the DC positive terminal DC+2, and the negative electrode of the secondary battery E2 is connected to the DC negative terminal DC-2. As a result of these connections, the secondary battery E2 and the inductor Ldc2 form a series circuit, and the inductor Ldc2 stably supplies the power output from the secondary battery E2 to the MERS 102.

The inductor Ldc2 may be, for example, a DC reactor.

(0027)

The gates (GV1, GX1, GV2, and GX2, in that order) of the switch sections SV1, SX1, SV2, and SX2 are the control terminals of the MERS 101 and the MERS 2 [sic: 102], and are all connected to a control unit 200.

(0028)

The control unit 200 is configured from a computer provided with, for example, a processor such as a central processing unit (CPU) and a memory device such as a random access memory (RAM) or a read only memory (ROM).

The control unit 200 uses the processor to read and execute, for example, a program stored in advance in the memory device, and by repeating the processing described below, e.g., the cycle described below, supplies the gate signals SGGV1, SGGX1, SGGV2, and SGGX2 to the gates GV1, GX1, GV2, and GX2, respectively.

(0029)

Each gate signal indicates on or off for a semiconductor switch provided with a gate to which the gate signal is supplied. For example, a gate signal that indicates on (on signal) has a voltage high enough to turn on the semiconductor switch (high level voltage), and a gate signal that indicates off (off signal) has a voltage low enough to turn off the semiconductor switch (low level voltage).

(0030)

The memory device of the control unit 200 stores in advance a time d1 that the gate signals SGGV1 and SGGX1 should remain on when the control unit 200 causes the MERS 101 to execute the cycle described below, a time d2, shorter than the time d1, that the gate signals SGGV2 and SGGX2 should remain on when the control unit causes the MERS 102 to execute the cycle described below, and a frequency f1 at which the gate signals SGGV1, SGGX1, SGGV2 and SGGX2 repeat the cycle described below.

(0031)

Before the start of operation, the control unit 200 outputs all of the gate signals SGGV1, SGGX1, SGGV2, and SGGX2 as off signals and repeats the next cycle C1 on the basis of the pre-stored times d1 and d2 and the frequency f1 in response to a user instruction, for example.

In the cycle C1, the control unit 200 simultaneously switches all of the gate signals SGGV1, SGGX1, SGGV2, and SGGX2 from the off signal to the on signal. Then, time d2 after switching to the on signals, the gate signals SGGV2 and SGGX2 are switched from on signals to off signals, and then after another time (d1-d2) elapses, the gate signals SGGV1 and SGGX1 are switched from the on signals to the off signals.

The control unit 200 repeats this cycle C1 at the frequency f1.

(0032)

In the present embodiment, the output voltage of the secondary battery E1 is 300 V, the output voltage of the secondary battery E2 is 500 V, the inductance of both of the inductors Ldc1 and Ldc2 is 1 mH, the capacitance of both of the capacitors CM1 and CM2 is 5 μ F, the inductance of the inductor Lm is 0.2 mH, the time d1 is 60 microseconds, the time d2 is 30 microseconds, and the frequency f1 is 7 kHz.

The times d1 and d2 and the frequency f1 are preadjusted so that the switch is turned on when no current is flowing in the inductor Lm, the switch of the MERS 101 is turned off when the voltage of the capacitor CM1 is almost zero, and the switch of the MERS 102 is turned off when the voltage of the capacitor CM2 is almost zero.

The capacitors CM1 and CM2 and the inductors Ldc1 and Ldc2 should be selected so that the resonant frequency between the capacitor CM1 and the inductor Ldc1 and the resonant frequency between the capacitor CM2 and the inductor Ldc2 are no greater than half of the frequency f1.

(0033)

(CONFIGURATION DIFFERENCES COMPARED TO THE PRIOR ART)

Circuits that are transformer-coupled to a flyback boost circuit are conventionally known, as are those that use a snubber lossless switch circuit (circuits sometimes called C-bridges) to soften the switch.

FIG. 2A shows the flyback boost of a conventional hard switch, FIG. 2B shows a hard switch softened with a MERS, and FIG. 2C shows a circuit in which a series circuit of a DC power supply and an inductance are connected between the DC terminals of a MERS and another inductance is connected between the AC terminals (also part of the circuit of the present invention).

(0034)

In the circuit shown in FIG. 2A, the basic principle is that current flows from the secondary battery E1 on the low voltage side to the inductance via a switch, and the switch is turned off to generate high voltage in the inductor, and power is irreversibly supplied to the secondary battery E2 on the high voltage side via a diode.

The switch in the boost circuit in FIG. 2A can be made into a soft switch by substituting a MERS as shown in FIG 2B.

(0035)

For the DC/DC converter according to the present invention, the basic principle is to repeat the following two operations alternately.

In the first operation, the MERS is turned on to discharge the electrostatic energy once stored in the capacitor of the MERS to the inductor. This causes a current to flow in the inductor and magnetic energy to be stored.

In the second operation, the MERS is turned off so that the capacitor of the MERS interrupts the current flowing in the inductor. This allows the magnetic energy of the inductor to be recovered in the capacitor.

(0036)

(DESCRIPTION OF THE BASIC OPERATION OF THE PRESENT INVENTION)

To facilitate understanding of the present invention, a portion thereof, that is, the current unidirectional MERS shown in Figure 2C, is described.

(0037)

The circuit shown in FIG. 2C is the DC/DC converter of FIG. 1, excluding the MERS 102 and the inductor Ldc2. This circuit is substantially identical to that of the DC/DC converter 10A with the AC terminals AC12-AC22 of the MERS102 shorted.

(0038)

(OPERATION OF THE UNIDIRECTIONAL CURRENT MERS)

Operation of the MERS 101 is next described with reference to FIG. 3, FIG. 4A to 4D, and FIG. 5.

(0039)

When the secondary power supply E1 is connected with the MERS 101 off, the secondary battery E1, the inductor Ldc1 and the capacitor CM1 form a series circuit as shown in FIG. 3. As a result, the capacitor CM1 stores power.

The control unit 200 starts operation and switches the MERS101 on and off to repeat the below operation.

(0040)

The following description assumes that the initial state is such that electrostatic energy has stored in the capacitor CM1 and both of the reverse-conducting semiconductor switches SWV1 and SWX1 are on (i.e., the state in FIG. 4D described below).

From this initial state, the control unit 200 supplies gate signals SGGV1 and SGGX1 in the pattern described below, and the MERS 101 repeats the operations described in [1] to [4] below with T1 to T5 described below as one cycle.

(0041)

[1] At a time T1 from the initial state, the control unit 200 switches the gate signals SGV1 and SGX1 from the off signal to the on signal as shown in FIG. 5(d). As a result, the reverse-conducting semiconductor switches SWV1 and SWX1 switch from off to on.

Then, the capacitor CM1 starts discharging, and, as shown in FIG. 4A, a current is generated flowing from the positive pole of the capacitor CM1 to the negative pole of the capacitor CM1 via the on reverse-conducting semiconductor switch SWV1, the inductance Lm and the reverse-conducting semiconductor switch SWX1.

As the capacitor CM1 discharges in this manner, the voltage Vcm1 of the capacitor CM1 decreases as shown in FIG. 5(b). Also, as the electrostatic energy stored in the capacitor CM1 is discharged, the current I_{Lm} flowing in the inductor Lm is amplified as shown in FIG. 5(a), and magnetic energy is stored in the inductor Lm.

(0042)

[2] At a time T2, when the discharge of the capacitor CM1 completes, the current flows in two paths as shown in FIG. 4B.

The first path is the route from the AC terminal AC11 through the current path of the diode section DU1 and the on reverse-conducting semiconductor switch SWV1, in that order.

The second route is through the current path of the on reverse-conducting semiconductor switch SWX1 and the diode section DY1, in that order.

In other words, all the electrostatic energy stored in the capacitor CM1 is stored as magnetic energy in the inductor Lm.

Since no power is consumed in this circuit configuration, the current I_{Lm} remains almost unchanged as shown in Figure 5(a) while the current flows in the paths shown in FIG. 4B, and the voltage Vcm1 also remains almost unchanged as shown in FIG. 5(b).

(0043)

[3] As described above, the control unit 200 switches the gate signals SGGV1 and SGGX1 from the on signal to the off signal at a time T3, which is the time d1 after switching the gate signals SGGV1 and SGGX1 from the off signal to the on signal. As a result, the reverse-conducting semiconductor switches SWV1 and SWX1 switch from on to off.

Then the currents flowing through the reverse-conducting semiconductor switches SWV1 and SWX1 are interrupted, and the magnetic energy stored in the inductor L_m generates a current flowing from the inductor L_m to the positive pole of the capacitor CM1 through the diode section DU1 as shown in FIG. 4C, and a current flows from the negative pole of the capacitor CM1 through the diode section DY1 to the AC terminal AC21. This causes the capacitor CM1 to store, as electrostatic energy in the form of an electric charge, the magnetic energy stored in the inductor L_m , so the voltage V_{cm1} rises as shown in FIG 5(b). Also, the current I_{Lm} decreases as shown in FIG. 5(a) because magnetic energy is recovered in the capacitor CM1 as electrostatic energy in the form of an electric charge.

(0044)

[4] Subsequently at a time T4, when the magnetic energy stored in the inductor L_m is depleted, the current flowing from the AC terminal AC11 to the AC terminal AC21 disappears as shown in FIG. 4D.

During this time, the capacitor CM1 forms a series circuit with the secondary battery E1 and the inductor Ldc1, but in a steady state, the voltage V_{cm1} hardly changes as shown in FIG. 5(b).

(0045)

When a time T5, which corresponds to the time T1 in the next cycle (this time T5 is determined by the frequency f_1), is reached, the operation shown in [1] to [4] above repeats again.

(0046)

As a result of the repeated operation described as [1] to [5] [*sic*: [4]], the inductor L_m and the capacitor CM1 convert between electrostatic energy and magnetic energy as shown in FIG. 5(a) and 5(b). In other words, an effect is achieved in which the control unit 200 switches the reverse-conducting semiconductor switches SWV1 and SWX1 from on to off, causing the magnetic energy stored in the inductor L_m to be recovered as electrostatic energy in the form of an electric charge in the capacitor CM1, and the control unit 200 switches the reverse-conducting semiconductor switches SWV1 and SWX1 from off to on, causing the energy recovered in the capacitor CM1 to be returned to the inductor L_m again.

(0047)

Since the resonance phenomenon of the capacitor CM1 and the inductor L_m is used, the voltage V_{cm1} of the capacitor CM1 can have a peak voltage higher than 300 V, the output voltage of the secondary battery E1.

In this example, the peak of the voltage V_{cm1} exceeds 400 V as shown in FIG. 5(b).

Also, in this example, there is nothing, including the inductor L_m , that consumes power, so in the steady state, the power P output from the secondary battery E1 is roughly 0 W as shown in FIG 5(c). Here, the power P indicates the average power for 1 ms.

(0048)

As shown in FIG. 5(a) and (d), at time T1, when the gate signals SGGV1 and SGGX1 switch from the off signal to the on signal, no current flows in the inductor L_m . Therefore, immediately after the gate signal is switched at time T5, a counter-electromotive force is generated in the inductor L_m in a direction so as to maintain a state of no current flow. Accordingly, at this time, the current path (in the forward direction) from the inductor L_m to the current path of the reverse-conducting semiconductor switch SWX1, the capacitor CM, and the current path (in the forward direction) of the reverse-conducting semiconductor switch SWV1, in that order, are interrupted by the inductor L_m . Therefore, the switching of the reverse-conducting semiconductor switches SWV1 and SWX1 from off to on at the time T5 is carried out in a state where the current flowing in these current paths is roughly zero during the state transition due to the switching of the semiconductor switches SX1 and SV1, and the switching is soft switching.

(0049)

As shown in FIG. 5(b) and 5(d), immediately after the time T3 when the gate signals SGGV1 and SGGX1 switch from the on signal to the off signal, the capacitor CM1 is almost completely discharged. It is therefore possible for the current path of the reverse-conducting semiconductor switch SWV1 to be short-circuited by the capacitor CM1 through the diode section DY1, and the current path of the reverse-conducting semiconductor switch SWX1 to be short-circuited by the capacitor CM1 through the diode section DU1. Moreover, it is possible for the capacitor CM1 to short the current path of the reverse-conducting semiconductor switch SWX1 through the diode section DU1. Therefore, the switching of the reverse-conducting semiconductor switches SWV1 and SWX1 from on to off at the time T3 occurs in a state where the voltage between both ends of these current paths is roughly zero, and there is little switching loss during the state transition of the semiconductor switches due to switching, which is to say the switching is soft switching.

(0050)

(FIRST EMBODIMENT: DC/DC CONVERTER OPERATION)

As described above, the control unit 200 causes the MERS 101 to recover the magnetic energy stored as electrostatic energy in the form of an electric charge in the inductor Lm in the capacitor CM1 by switching the reverse-conducting semiconductor switches SWV1 and SWX1 from on to off, and to return the energy recovered by the capacitor CM1 to the inductor Lm again by switching the reverse-conducting semiconductor switches SWV1 and SWX1 from off to on.

(0051)

In the DC/DC converter 10A, the control unit 200 also causes the MERS 102 to switch the reverse-conducting semiconductor switches SWV2 and SWX2 from on to off. As a result, the magnetic energy stored in the inductor Lm is recovered as electrostatic energy in the form of an electric charge in the capacitor CM2.

The control unit 200 also switches the reverse-conducting semiconductor switches SWV2 and SWX2 from off to on, thereby returning the energy recovered by the capacitor CM2 to the inductor Lm again.

(0052)

In this manner, the control unit 200 controls the MERSes 101 and 102 so that the electrostatic energy stored in the capacitors CM1 and CM2 is discharged and stored as magnetic energy in the inductor Lm and the magnetic energy stored in the inductor Lm is stored as electrostatic energy in the capacitor CM or the capacitor CM2.

(0053)

However, in the DC/DC converter 10A of the present embodiment, the control unit 200 turns off the reverse-conducting semiconductor switches SWV2 and SWX2 of the MERS 102 first of the MERSes 101 and 102. Therefore, all or most of the magnetic energy stored in the inductor Lm charges the capacitor CM2. The power charged in the capacitor CM2 charges the secondary battery E2.

(0054)

The magnetic energy in the inductor Lm used to charge the secondary battery E2 is supplied from the secondary battery E1 via the inductor Ldc1 and from the secondary battery E2 via the inductor Ldc2. However, the power supplied from secondary battery E2 returns to secondary battery E2, so in effect, the secondary battery E1 charges the secondary battery E2.

In this embodiment, the resonant frequency of the capacitor CM1 and the inductor Ldc1 and the resonant frequency of the capacitor CM2 and the inductor Ldc2 are no greater than half of the frequency f1, so power is not supplied from the secondary battery E2 to the DC/DC converter 10A.

(0055)

(FIRST EMBODIMENT: DETAILED OPERATION OF THE DC/DC CONVERTER)

Detailed operation of the DC/DC converter 10A of the present embodiment is described below with reference to FIG. 6, FIG. 7A to 7F, and FIG. 8A to D. In FIG. 8A, the current ILdc1 represents the current flowing from the positive terminal of the secondary battery E1 toward the DC terminal DC11 of the MERS 101, and the current ILdc2 represents the current flowing from the DC terminal DC12 of the MERS 102 toward the positive terminal of the secondary battery E2.

(0056)

When the gate signals SGGV1, SGGX1, SGGV2 and SGGX2 output from the control unit 200 are all off signals, as shown in FIG. 6, the reverse-conducting semiconductor switches SWV1, SWX1, SWV2 and SWX2 are all off, the capacitor CM1 is powered from the secondary battery E1 via the inductor Ldc1, and the capacitor CM2 is powered from the secondary battery E2 via the inductor Ldc2.

(0057)

The following description assumes that the initial state is such that electrostatic energy has stored in the capacitors CM1 and CM2 and the reverse-conducting semiconductor switches SWV1, SWX1, SWV2 and SWX2 are on (i.e., the state in FIG. 7F described below).

From this initial state, the control unit 200 supplies the gate signals SGGV1, SGGX1, SGGV2, and SGGX2 in the pattern described below, so that the MERS 101 periodically carries out the operations described in phases 1 to 6 below at a prescribed frequency f1 in which Ta1 to Ta7 described below are one cycle.

(0058)

(Phase PA1)

At the time Ta1, the control unit 200 switches the gate signals SGGV1, SGGX1, SGGV2 and SGGX2 from the off signal to the on signal. As a result, the reverse-conducting semiconductor switches SWV1, SWX1, SWV2 and SWX2 switch from off to on.

Then, the capacitors CM1 and CM2 start discharging, and as shown in FIG. 7A, currents are generated, one flowing from the positive pole of the capacitor CM1 to the negative pole of the capacitor CM2 via the on reverse-conducting semiconductor switch SWV1, the inductance Lm and the reverse-conducting semiconductor switch SWX2, and one flowing from the positive pole of the capacitor CM2 to the negative pole of the capacitor CM1 via the on reverse-conducting semiconductor switch SWV2 and the reverse-conducting semiconductor switch SWX1.

As the capacitors CM1 and CM2 discharge in this manner, the voltages Vcm1 of the capacitors CM1 and CM2 decrease as shown in FIG. 8A(b). Also, the electrostatic energy stored in the capacitors CM1 and CM2 is discharged, amplifying the current ILm flowing in the inductor Lm as shown in FIG. 8A(a), and magnetic energy is stored in the inductor Lm.

(0059)

(Phase PA2)

In the present embodiment, the discharge of the capacitor CM2 completes before that of the capacitor CM1. When the discharge of the capacitor CM2 completes at the time Ta2, as shown in FIG. 7B, the current flows from the AC terminal AC12 of the MERS 102 to the AC terminal AC22, branching into two routes: one route passing in turn through the current path of the diode section DU2 and the reverse-conducting semiconductor switch SWV2 that is on, and the other route passing in turn through the current path of the reverse-conducting semiconductor switch SWX2 that is on and the diode section DY2.

That is, all of the electrostatic energy stored in the capacitor CM2 is stored as magnetic energy in the inductor Lm. Note that the capacitor CM1 has not completed discharging at this point.

(0060)

(Phase PA3)

As described above, the control unit 200 switches the gate signals SGGV2 and SGGX2 from the on signal to the of signal at the time Ta3, which is time d2 after the time Ta1. As a result, the reverse-conducting semiconductor switches SWV2 and SWX2 are switched from on to off. In the present embodiment, the time Ta3 is reached immediately after the time Ta2.

Then the currents flowing in the reverse-conducting semiconductor switches SWV2 and SW2 are interrupted, and as shown in FIG. 7C, the magnetic energy stored in the inductor Lm generates a current that flows from the inductor Lm to the positive pole of the capacitor CM2 through the diode section DU2, and a current flows from the negative pole of the capacitor CM2 through the diode section DY2 to the AC terminal AC22. As a result, the capacitor CM2 stores the magnetic energy stored in the inductor Lm as electrostatic energy in the form of an electric charge, and so the voltage Vcm2 rises as shown in FIG. 8A(b). Also, the current ILm decreases as shown in FIG. 8A(a) because magnetic energy is stored as electrostatic energy in the form of an electric charge in the capacitor CM2. Further, since the capacitor CM1 continues to discharge, the voltage Vcm1 decreases as shown in FIG. 8A(b).

(0061)

(Phase PA4)

Then, when the discharge of the capacitor CM2 completes at the time Ta4, as shown in FIG. 7D, the current flows from the AC terminal AC11 of the MERS 101 to the AC terminal AC21, branching into two routes: one route passing in turn through the current path of the diode section DU1 and the reverse-conducting semiconductor switch SWV that is on, and the other route passing in turn through the current path of the reverse-conducting semiconductor switch SWX1 that is on and the diode section DY1.

That is, all of the electrostatic energy stored in the capacitor CM1 is stored as magnetic energy in the inductor Lm.

(0062)

(Phase PA5)

The control unit 200 switches the gate signals SGGV1 and SGGX1 from the on signal to the off signal at the time Ta5, which is a time (d1-d2) after the time Ta3 (time d1 after time Ta1). As a result, the reverse-conducting semiconductor switches SWV1 and SWX1 are switched from on to off. In this embodiment, at the time Ta5, the inductor Lm is in a state where current is flowing (magnetic energy remains).

Then, each current flowing through the reverse-conducting semiconductor switches SWV1 and SWX1 is interrupted, and, as shown in Figure 7E, the magnetic energy stored in the inductor Lm generates a current flowing from the inductor Lm to the positive pole of the capacitor CM1 through the diode section DU1, and a current flows from the negative pole of the capacitor CM1 to the AC terminal AC21 through the diode section DY1. Also, a current flows in the MERS 102 in a path shown by phase P5 described above.

Therefore, the capacitors CM1 and CM2 store the magnetic energy stored in the inductor Lm as electrostatic energy in the form of an electric charge, and the voltages Vcm1 and Vcm2 increase as shown in Figure 8A(b). Also, the current ILm decreases as shown in Figure 8A(a) because magnetic energy is stored in the capacitors CM1 and CM2 as electrostatic energy in the form of an electric charge.

(0063)

(Phase PA6)

Then, at the time Ta 6 when the magnetic energy stored in the inductor Lm is depleted, the current flowing through the inductor Lm disappears as shown in FIG. 7F.

(0064)

When the time Ta7 (time 1/f1 after the time Ta1 in the previous cycle), which corresponds to the time Ta1 in the next cycle, is reached, the operations shown in phases PA1 to PA6 above are repeated again.

While these operations are being repeated, as shown in FIG. 8A(a), power is always supplied from the secondary battery E1 to the MERS 101 (the current ILdc1 is positive) and power is always supplied from the MERS 102 to the secondary battery E2 (the current ILdc2 is positive).

(0065)

In this manner, storage as electrostatic energy takes place at the same time in the capacitors CM1 and CM2. As this electrostatic energy is discharged, magnetic energy is stored in the inductor Lm. Since most of this magnetic energy is recovered by the capacitor CM2, the capacitor CM2 is boosted from the voltage of the secondary battery E1, which in this example is higher than the output voltage of the secondary battery E2 as shown in Figure 8A(b). Thus, the capacitor CM2 charges the secondary battery E2. In this example, the power supplied to the secondary battery E2 is always from the secondary battery E1 as shown in Figure 8A(a).

(0066)

In this example, the conversion power from the secondary battery E1 to the secondary battery E2 is 6,300 W. If the switching control frequency f_1 is changed to 5 kHz, the conversion power is 3,600 W, and if the frequency f_1 is changed to 10 kHz, the conversion power is 11,700 W.

(0067)

(OTHER USE CASE 1 OF THE FIRST EMBODIMENT)

The relationship between the time variation of the current I_{Lm} flowing through the inductor L_m , the time variation of the voltages V_{cm1} and V_{cm2} of the capacitors $CM1$ and $CM2$, and the time transitions of the gate signals $SGGV1$ and $SGGX1$ and the gate signals $SGGV2$ and $SGGX2$ is shown in FIG. 8B where the secondary battery E2 is changed from 500 V to 300 V.

In this example, the converted power from the secondary battery E1 to the secondary battery E2 is 5,600W.

(0068)

(OTHER USE CASE 2 OF THE FIRST EMBODIMENT)

The relationship between the time variation of the current I_{Lm} flowing through the inductor L_m , the time variation of the voltages V_{cm1} and V_{cm2} of the capacitors $CM1$ and $CM2$, and the time transition of the gate signals $SGGV1$ and $SGGX1$ and the gate signals $SGGV2$ and $SGGX2$ is shown in FIG. 8C where the 200 V battery is changed from the above secondary battery E2 [sic: where the secondary battery E2 is changed to 200 V].

(0069)

In this example, the conversion power from the secondary battery E1 to the secondary battery E2 is 4,800 W. If the repetition frequency f_1 of the switching control is changed to 5 kHz, the conversion power is 3,200 W, and if the frequency f_1 is changed to 10 kHz, the conversion power is 7,700 W.

In this use case, step-down conversion is used.

(0070)

(CONFIGURATION VARIATION 1 OF THE FIRST EMBODIMENT)

In the embodiment description above, the case in which the time to hold the gate signals $SGGV1$ and $SGGX1$ as on signals is longer than the time to hold the gate signals $SGGV2$ and $SGGX2$ as on signals is described, but it may also be shorter.

For example, the time to hold the gate signals $SGGV1$ and $SGGX1$ as on signals may be set to the time d_2 , and the time to hold the gate signals $SGGV2$ and $SGGX2$ as on signals may be set to the time d_1 . The relationship for this case between the time variation of the current I_{Lm} flowing through the inductor L_m , the time variation of the voltages V_{cm1} and V_{cm2} of the capacitors $CM1$ and $CM2$, and the time transition of the gate signals $SGGV1$ and $SGGX1$ and the gate signals $SGGV2$ and $SGGX2$ is shown in FIG. 8D.

(0071)

In this case, the reverse-conducting semiconductor switches $SWV1$ and $SWX1$ are turned off first, so power is supplied from the secondary battery E2 to the secondary battery E1. In this example, the converted power from the secondary battery E2 to the secondary battery E1 is 12,900 W.

(0072)

Thus, according to the DC/DC converter 10A of the first embodiment of the present invention, by setting the time for holding the gate signals $SGGV1$ and $SGGX1$ as on signals shorter than the time for holding the gate signals $SGGV2$ and $SGGX2$ as on signals, power can be supplied from the secondary battery E2 to the secondary battery E1 (reverse conversion is possible).

In other words, according to the DC/DC converter 10A of the first embodiment of the present invention, by appropriately selecting the time to hold the gate signals $SGGV1$ and $SGGX1$ as on signals and the time to hold the gate signals $SGGV2$ and $SGGX2$ as on signals, it is possible to charge both the secondary battery E1 and the secondary battery E2.

(0073)

(CONFIGURATION VARIATION 2 OF THE FIRST EMBODIMENT)

In the first embodiment, the AC terminal AC11 of the MERS 101 and the AC terminal AC22 of the MERS102 are connected to the ground line. However, it is also possible to connect the negative electrode of the secondary battery E1 and the negative electrode of the secondary battery E2, or the positive electrode of the secondary battery E1 and the positive electrode of the secondary battery E2, to the ground line. However, if the secondary battery E1 and the secondary battery E2 have different output voltages, current may leak through the common ground line.

(0074)

As with the DC/DC converter 10B shown in FIG. 9, the inductor Lm of DC/DC converter 10A is divided into the inductor Lm1 connected between the AC terminal AC21 of the MERS 101 and the AC terminal AC12 of the MERS 102, and the inductor Lm2 connected between the AC terminal AC22 of the MERS 102 and the AC terminal AC11 of the MERS 101. The inductors Lm1 and Lm2 should have the same inductance. This will reduce leakage current even if the secondary batteries E1 and E2 are grounded.

(0075)

The inductors Ldc1 and Ldc2 may be arranged symmetrically around the secondary batteries E1 and E2. The inductor Ldc1 is divided into an inductor Ldc11 connected between one end of the secondary battery E1 and the DC terminal DC11 of the MERS 101 and an inductor Ldc21 connected between the other end of the secondary battery E1 and the DC terminal DC21 of the MERS 101. The inductor Ldc2 is divided into an inductor Ldc12 connected between one end of the secondary battery E2 and the DC terminal DC12 of the MERS 102 and an inductor Ldc22 connected between the other end of the secondary battery E2 and the DC terminal DC22 of the MERS 102. The inductors Ldc11 and Ldc21 should have the same inductance as should the inductors Ldc12 and Ldc22. This also reduces leakage current.

(0076)

For example, if the secondary battery E1 is set to 300 V, the secondary battery E2 to 500 V, the gate signals GGV1 [sic: SGGV1] and SGGX1 to 60 microseconds, the gate signals SGGV2 and SVVX2 to 30 microseconds, and the repetition frequency f1 of switching control to 7 kHz, the conversion power from the secondary battery E1 to the secondary battery E2 is approximately 5,900 W.

(0077)

(CONFIGURATION VARIATION 3 OF THE FIRST EMBODIMENT)

The inductor Lm may use the leakage inductance of a two-winding transformer. That is, for example, the inductor Lm of the DC/DC converter 10B may be replaced with a high-frequency transformer RFT, such as in the DC/DC converter 10C shown in FIG. 10.

The high-frequency transformer RFT is configured from a primary coil L1, a secondary coil, and leakage inductances LM1 and LM2.

(0078)

The primary coil L1 and the secondary coil are electromagnetically connected.

The leakage inductances LM1 and LM2 are the leakage inductances in the coupling between the primary coil L1 and the secondary coil L2. The primary coil L1, the secondary coil L2, and the leakage inductances LM1 and LM2 in the drawing are simple models of the transformer coupling.

(0079)

The leakage inductance LM1 has one end connected to one end of the primary coil L1 and the other end connected to the AC terminal AC21 of the MERS 101. The leakage inductance LM2 has one end connected to one end of the secondary coil L2 and the other end connected to the AC terminal AC21 of the MERS 102.

The other end of the primary coil L1 is connected to the AC terminal AC11 of the MERS 101. The other end of the secondary coil L2 is connected to the AC terminal AC22 of the MERS 102.

However, in reality, there are no leakage inductances LM1 and LM2, and one end of the primary coil L1 is connected to the AC terminal AC21 and one end of the secondary coil L2 is connected to the AC terminal AC12.

(0080)

Thus, it is possible to make an isolated connection between the MERS 101 and the MERS 102 via a transformer.
(0081)

An inductor may be further connected to the leakage inductance LM1 and the leakage inductance LM2.
(0082)

When a high-frequency transformer RFT is selected with a leakage inductance of 0.2 mH and secondary batteries with a 300 V output are selected as the secondary batteries E1 and E2 in the above DC/DC converter 10C, the relationship between the time variation of the current I_{link} flowing through a first coil LM1, the time variation of the voltages V_{cm1} and V_{cm2} of the capacitors CM1 and CM2, and the time transitions of the gate signals SGGV1 and SGGX1 and the gate signals SGGV2 and SGGX2 is shown in FIG 11.

In this case, the waveforms are very similar to those in FIG. 8B above, which is substantially identical in configuration.
(0083)

For example, if the secondary battery E1 is set to 300 V, the secondary battery E2 to 300 V, the gate signals GGV1 [sic: SGGV1] and SGGX1 to 60 microseconds, the gate signals SGGV2 and SVVX2 to 30 microseconds, and the repetition frequency f_1 of switching control to 7 kHz, the conversion power from the secondary battery E1 to the secondary battery E2 is approximately 5,600 W.

(0084)

Note that as the voltage on the power receiving side increases, the energy in the capacitor CM2 increases, and so does the current of the inductance. This is a characteristic of an even larger output.

When the secondary battery E2 is changed to 500 V, the power converted from the secondary battery E1 to the secondary battery E2 is 6,300 W.

(0085)

(SWITCHING LOSS IN THE FIRST EMBODIMENT)

As described above, soft switching is achieved in the first embodiment and its variants. For example, the current and voltage of the semiconductor switch is shown in FIG. 12 when the gate signals SGGV1 and SGGX1 are held on for 60 microseconds, the gate signals SGGV2 and SGGX2 are held on for 30 microseconds, the repetition rate is 7 kHz, and the voltage boost conversion is from 300 V in the secondary battery E1 to 500 V in the secondary battery E2. From the top, the time variation of a current I_{sv1} and a voltage V_{sv1} of the reverse-conducting semiconductor switch SV1, the time variation of a current I_{sv2} and a voltage V_{sv2} of the reverse-conducting semiconductor switch SV2, and the time transitions of the gate signals SGGV1 and SGGX1 and the gate signals SGGV2 and SGGX2 are shown.

(0086)

As described above, when the gate signals SGGV1 and SGGX1 switch from off to on, the current I_{sv1} is almost not flowing, and when the gate signals switch from on to off, the voltage V_{sv1} is almost 0 volts. Similarly, as described above, when the gate signals SGGV2 and SGGX2 switch from off to on, the current I_{sv2} is almost not flowing, and when the gate signals switch from on to off, the voltage V_{sv2} is almost 0 volts.

(0087)

Thus, when the gate signal is switched, i.e., when the reverse-conducting semiconductor switch is switched on or off, a zero current or a zero voltage is present, so soft switching is achieved and there is almost no switching loss.

During the period from the time T_{a1} to the time T_{a2} (during the phase PA1), the capacitors CM1 and CM2 and the inductor L_m are in resonance. Therefore, the higher their resonance frequency is, the shorter the time from the time T_{a1} to the time T_{a2} becomes.

Similarly, in each of the above phases, the capacitor CM1 and/or the capacitor CM2 and the inductor L_m are resonating. Therefore, the higher these resonance frequencies are, the shorter each cycle becomes, and the more power is converted per unit time. Therefore, the times d_1 and d_2 can be set shorter and the control repetition frequency f_1 can be set higher.

(0088)

Although the first embodiment of the present invention has been described above, the configurations of the DC/DC converters 10A to 10C are not limited to those described above. For example, both of the MERSes 101 and 102 do not necessarily have to perform soft switching. Although the loss of power is greater, the secondary battery E2 can be charged from the secondary battery E1 through the DC/DC converter 10A.

(0089)

As described above, according to the DC/DC converters 10A to 10C of the first embodiment of the present invention, DC power can be supplied bidirectionally regardless of the output voltage of the power supply with a simple control of turning on the two MERSes 101 and 102 simultaneously and turning off the power receiving side first.

Soft switching is also possible by turning on when there is essentially no current flowing in inductor Lm, turning off the MERS 102 when there is essentially no voltage in the capacitor CM2, and turning off the MERS 101 when there is essentially no voltage in the capacitor CM1.

(0090)

(SECOND EMBODIMENT)

In the first embodiment described above, the MERS 101 and 102 are unidirectional MERSes. However, the MERSes 101 and 102 may be full-bridge MERSes. In the first embodiment, the power flowing to the inductor Lm was also unidirectional because a MERS for unidirectional current direction was used. However, if a full-bridge MERS is used, it is possible to supply bidirectional current to the inductor Lm. The second embodiment of the present invention with such a configuration is described below.

(0091)

As shown in FIG. 13, the DC/DC converter 10D according to the second embodiment differs from the DC/DC converter 10A of the first embodiment in that the MERS 101 is changed to a full-bridge MERS 103 and the MERS 102 is changed to a full-bridge MERS 104. In addition, the control unit 200 alternately repeats the cycle C1 described above and a C2 described below to switch the gate signals to on and off signals.

The configuration of the DC/DC converter 10D is otherwise essentially identical to the DC/DC converter 10A of the first embodiment.

(0092)

The MERS 103 has a switch section SU1 connected in parallel to the diode section DU1 of the MERS 101 and a switch section SY1 connected in parallel to the diode section DY1. The MERS 103 is otherwise configured substantially identically to the MERS 101.

The MERS 104 has a switch section SU2 connected in parallel to the diode section DU2 of the MERS 102 and a switch section SY2 connected in parallel to the diode section DY2. The MERS 104 is otherwise configured substantially identically to the MERS 102.

(0093)

Switch sections SU1, SY1, SU2, and SY2 each comprises a semiconductor switching device such as, for example, a metal-oxide-silicon field effect transistor (MOSFET) an insulated gate bipolar transistor (IGBT), or a gate turn-off thyristor (GTO), and each is provided with a current path and a control terminal. When an on signal described below is supplied to each control terminal, the current path conducts, and when an off signal is supplied, the current path is interrupted.

(0094)

Diode sections DU1, DY1, DU2 and DY2 may be, for example, parasitic diodes of the semiconductor switches configuring the switch sections.

(0095)

Below, each diode part is described as comprising a semiconductor diode, and each switch section is described as comprising an n-channel MOSFET. In this case, the drain-source interval of the MOSFET forms the current path of the switch section, and the gate forms the control terminal.

(0096)

Before the start of operation, the control unit 200 outputs all of the gate signals SGGU1 to SGGY1 and SGGU2 to SGGY2 as off signals and repeats the cycle C1 and the next cycle C2 alternately at the frequency f1 on the basis of the pre-stored times d1 and d2 and the frequency f1 in response to a user instruction, for example.

In the cycle C2, the control unit 200 simultaneously switches the pair of gate signals SGGU1 and SGGY1 and the pair of gate signals SGGU2 and SGGY2 from the off signal to the on signal. Then, after the time d2 after switching to the on signal, the pair of gate signals SGGU2 and SGGY2 is first switched from the on signal to the off signal, and after another time (d1-d2) elapses (time d1 after switching to the on signal), the pair of gate signals SGGU1 and SGGY1 is switched from the on signal to the off signal.

(0097)

In the present embodiment, the output voltage of the secondary battery E1 is 300 V, the output voltage of the secondary battery E2 is 500 V, the inductances of the inductors Ldc1 and Ldc2 are both 1 mH, the capacitances of the capacitors CM1 and CM2 are both 5 μ F, the inductance of the inductor Lm 1 is 0.2 mH, the time d1 is 60 microseconds, the time d2 is 30 microseconds, and the frequency f is 7 kHz.

(0098)

(SECOND EMBODIMENT: OPERATION OF THE DC/DC CONVERTER)

Operation of the DC/DC converter 10D of the present embodiment is described below with reference to FIG. 13, FIG. 14A to 14H, and FIG. 15.

The initial state is described below as a phase PB8, in which all reverse-conducting semiconductor switches SWU1 to SWY1 and SWU2 to SWY2 are off and electrostatic energy is stored in the capacitors CM1 and CM2.

(0099)

(Phase PB1)

At a time Tb1, the control unit 200 switches the gate signals SGGV1, SGGX1, SGGV2 and SGGX2 from off signals to on signals and holds the gate signals SGGU1, SGGY1, SGGU2 and SGGY2 as off signals. As a result, the reverse-conducting semiconductor switches SWV1, SWX1, SWV2 and SWX2 are switched from off to on. The reverse-conducting semiconductor switches SWU1, SWY1, SWU2 and SWY2 remain unchanged as off signals.

Then, as shown in Figure 14A, the capacitors CM1 and CM2 start discharging and magnetic energy is stored in the inductor Lm.

(0100)

(Phase PB2)

As described above, the control unit 200 switches the gate signals SGGV2 and SGGX2 from the on signal to the off signal at a time Tb2, which is the time d2 after switching the gate signals SGGV1, SGGX1, SGGV2, and SGGX2 from the off signals to the on signals. The other gate signals are held as off signals. As a result, the reverse-conducting semiconductor switches SWV2 and SWX2 are switched from on to off.

Then, as shown in Figure 14B, the current flowing in the inductor Lm is interrupted by the capacitor CM2, which stores the magnetic energy stored in the inductor Lm as electrostatic energy in the form of an electric charge.

(0101)

(Phase PB3)

At a time Tb3, a time (d1-d2) after from time the tb2 [*sic*: Tb2], the control unit 200 switches the gate signals SGGV1 and SGGX1 from on signals to off signals.

Then, as shown in Figure 14C, the current flowing in the inductor Lm is interrupted by the capacitor CM1 and the capacitor CM2, which store the remaining magnetic energy stored in the inductor Lm as electrostatic energy in the form of an electric charge.

(0102)

(Phase PB4)

Then, at a time TB 4 when the magnetic energy stored in the inductor Lm is depleted, the current flowing through the inductor Lm disappears as shown in FIG. 14D.

In the phases PB1 to PB4, the capacitor CM2 recovers most of the power that was once stored in the inductor Lm as magnetic energy by being stored in the capacitors CM1 and CM2 as electrostatic energy and discharged. Therefore, the voltage Vcm2 of the capacitor CM2 is higher than the output voltage of the secondary battery E2. Thus, the capacitor CM2 charges the secondary battery E2. Since most of the power is recovered by the capacitor CM2, the voltage Vcm1 of the capacitor CM1 is lower than the output voltage of the secondary battery E1. Therefore, the capacitor CM1 is charged by the secondary battery E1.

(0103)

(Phase PB5)

At a time Tb5, which is determined by the frequency f1, the control unit 200 switches the gate signals SGGU1, SGGY1, SGGU2 and SGGY2 from off signals to on signals and holds the gate signals SGGV1, SGGX1, SGGV2 and SGGX2 as off signals. As a result, the reverse-conducting semiconductor switches SWU1, SWY1, SWU2 and SWY2 are switched from off to on. The reverse-conducting semiconductor switches SWV1, SWX1, SWV2 and SWX2 remain unchanged as off signals.

Then, as shown in Figure 14E, the capacitors CM1 and CM2 start discharging and magnetic energy is stored in the inductor Lm.

(0104)

(Phase PB6)

As described above, the control unit 200 switches the gate signals SGGU2 and SGGY2 from the on signals to the off signals at the time Tb6, d2 after the gate signals SGGU1, SGGY1, SGGU2 and SGGY2 are switched from the off signals to the on signals. The other gate signals are held as the off signals. As a result, the reverse-conducting semiconductor switches SWU2 and SWY2 are switched from on to off.

Then, as shown in Figure 14F, the current flowing in the inductor Lm is interrupted by the capacitor CM2, which stores, as electrostatic energy in the form of an electric charge, the magnetic energy stored in the inductor Lm.

(0105)

(Phase PB7)

Then, the control unit 200 switches the gate signals SGGU1 and SGGY1 from the on signals to the off signals at the time Tb7, a time (d1-d2) after the time Tb6.

Then, as shown in Figure 14G, the current flowing in the inductor Lm is interrupted by the capacitor CM1 and the capacitor CM2, which store, as electrostatic energy in the form of an electric charge, the magnetic energy stored in the inductor Lm.

(0106)

(Phase PB8)

Then, at a time TB8 when the magnetic energy stored in the inductor Lm is depleted, the current flowing in the inductor Lm disappears as shown in FIG. 14H.

In the phases PB5 to PB8, the capacitor CM2 recovers most of the power that was once stored in the inductor Lm as magnetic energy by being stored in the capacitors CM1 and CM2 as electrostatic energy and discharged. Therefore, the capacitor CM2 the voltage of [sic: the voltage of the capacitor CM2] is boosted, becoming higher than the output voltage of the secondary battery E2. Thus, the capacitor CM2 charges the secondary battery E2. Since most of the power is recovered by the capacitor CM2, the voltage Vcm1 of the capacitor CM1 is lower than the output voltage of the secondary battery E1. Therefore, the capacitor CM1 is charged by the secondary battery E1.

(0107)

As explained above, the DC/DC converter 10D of the second embodiment of the present invention can also charge both the secondary battery E1 on the low-voltage side and the secondary battery E2 on the high-voltage side.

In addition, in the DC/DC converter 10D of the present embodiment, the inductor Lm has the advantage of being less likely to be demagnetized than the DC/DC converter 10A of the first embodiment because an alternating current flows through the inductor Lm.

(0108)

In the case of the DC/DC converter 10D of the present embodiment, when current is flowing in the diode sections, the power loss can be further reduced by turning on the switch section connected in parallel to the diode section.

(0109)

(CONFIGURATION VARIATION 1 OF THE SECOND EMBODIMENT)

(0110)

The inductors Ldc1 and Ldc2 of the DC/DC converter 10D may be arranged symmetrically around the secondary batteries E1 and E2.

As in a DC/DC converter 10E shown in FIG. 15, the inductor Ldc1 is divided into an inductor Ldc11 connected between one end of the secondary battery E1 and the DC terminal DC11 of the MERS 103 and an inductor Ldc21 connected between the other end of the secondary battery E1 and the DC terminal DC21 of the MERS 103. The inductors Ldc11 and Ldc21 should have the same inductance as should the inductors Ldc12 and Ldc22. This also reduces leakage current.

(0111)

(CONFIGURATION VARIATION 2 OF THE SECOND EMBODIMENT)

The inductor Lm may use the inductance of a two-winding transformer structure. That is, for example, the inductor Lm of the DC/DC converter 10E may be replaced with a high-frequency transformer RFT, such as in a DC/DC converter 10F shown in FIG. 16.

(0112)

Thus, it is possible to make an isolated connection between the MERS 101 and the MERS 102 via a transformer. The inductor may be connected in series with the first coil, the second coil, or both.

(0113)

This circuit shown in FIG. 16 is similar to the circuit diagram of a conventional isolated transformer-coupled DC/DC conversion using an inverter, but differ greatly in the matter that the inductances of the inductors Ldc1 (inductors Ldc11 and Ldc12) and Ldc2 (inductors Ldc21 and Ldc22) make the secondary batteries E1 and E2 operate close to the current source and the matter that soft switching is achieved by discharging the capacitors CM1 and CM2 until their voltages are roughly zero.

Another major difference is that the voltages of the capacitors CM1 and CM2 are boosted by the voltage of the connected batteries.

Also, the use of the leakage inductance in the transformer coupling is significantly different from the conventional transformer-coupled DC/DC conversion using an inverter.

(0114)

(CONFIGURATION VARIATION 1 IN EMBODIMENTS 1 AND 2)

As shown in the DC/DC converter 10F in FIG. 17, the DC/DC converter 10E may be further equipped with a diode DR1, which interrupts the current flowing in the direction from the DC terminal DC+1 of the MERS 103 to one end of secondary battery E1, and a diode DR2, which interrupts the current flowing from one end of the secondary battery E1 to the DC terminal DC+2 of the MERS 104.

(0115)

In this case, the power output from the secondary battery E2 does not charge the secondary battery E1. Since the current flowing in the direction to one end of the secondary battery E1 is interrupted, a DC reactor can be used as the inductor Ldc1, and the inductance of the inductor Ldc1 can be made smaller. Doing so makes it possible to make the inductor Ldc1 smaller.

Since the current flowing in the direction from one end of the secondary battery E1 to the DC terminal DC+2 of the MERS 104 is interrupted, the inductor Ldc2 can be made smaller for the same reason that inductor Ldc1 can be made smaller.

Another advantage is that when there is no need to output power from the secondary battery E2, the secondary battery E2 does not discharge unnecessarily.

(0116)

In this example, while all the reverse-conducting semiconductor switches are off, the capacitor CM1 is charged, all the reverse-conducting semiconductor switches are turned on to discharge the electrostatic energy in the capacitor CM1 for storage as magnetic energy in the leakage inductances LM1 and LM2 as the current Ilink, the reverse-conducting semiconductor switches SWV2 and SWX2 are turned off first so the current Ilink is interrupted by the capacitor CM2, recovering the magnetic energy of the leakage inductances LM1 and LM2 in the capacitor CM2, and the secondary battery E2 is charged by the voltage of the capacitor CM2. This operation is repeated to supply power from the secondary battery E1 to the secondary battery E2.

(0117)

FIG. 18 shows the time variations of the current Ilink flowing in the first inductor L1, the current ILdc1 flowing in the inductor Ldc1 and the current ILdc2 flowing in the inductor Ldc2, the time variations of the voltage Vcm1 of the capacitor CM1 and the voltage Vcm2 of the capacitor CM2, the time transitions of the gate signals SGGV1 and SGGX1 and of the gate signals SGGV2 and SGGX2, and the time variations of an output power P1 of the secondary battery E1 and a power P2 supplied to the secondary battery E2.

Note that secondary batteries E1 and E2 have an output of 100 V, the inductors L1 and L2 are 0.2 mH, the capacitors CM1 and CM2 are 0.5 μ F, the leakage inductances LM1 and LM2 are 0.1 mH, the gate signals SGGV1 and SGGX1 have an on-time of 30 μ s, the gate signals SGGV2 and SGGX2 have an on-time of 15 μ s, and the repetition frequency f1 is 6 kHz.

(0118)

When all the reverse-conducting semiconductor switches are turned off, the capacitor CM1 is charged, so the capacitor voltage Vcm1 rises and the voltage is held at the peak of resonance between the inductor L1 and the capacitor CM1.

When all the reverse-conducting semiconductor switches are turned on, the electrostatic energy in the capacitor CM1 is discharged and stored as magnetic energy in the leakage inductances LM1 and LM2 as the current Ilink, so the voltage Vcm1 of the capacitor CM1 decreases and the current Ilink in the leakage inductance Lm1 rises.

In this example, the reverse-conducting semiconductor switches SWV2 and SWX2 are turned off first at the timing when the voltage Vcm1 of the capacitor CM1 becomes almost zero. When the reverse-conducting semiconductor switches SWV2 and SWX2 are turned off first, the current Ilink flowing in the inductance Lm1 is recovered in the capacitor CM2, so the voltage of the capacitor CM2 rises. When the voltage of the capacitor CM2 exceeds the 100 V voltage of the secondary battery E2, discharge from the capacitor CM2 to the secondary battery E2 starts. In this example, the inductor Ldc3 causes the capacitor CM2 to discharge power to the battery E2 until the voltage becomes almost zero.

Then, when the reverse-conducting semiconductor switches SWV1 and SWX1 are turned off, the capacitor CM1 is charged.

This operation is repeated.

(0119)

In the DC/DC converters 10A to 10E, the inductances of the inductors Ldc1 and Ldc2 are described above as 1 mH. In the DC/DC converter 10F of the embodiment variation, the inductances of the inductors Ldc1 and Ldc2 are 0.2 mH.

Since there are no diodes DR1 and DR2 in the DC/DC converters 10A to 10E, the inductances of the inductors Ldc1 and Ldc2 should be sufficiently large to prevent reverse current flow.

(0120)

In the DC/DC converter 10F of the present embodiment variation, the diode DR1 interrupts the current flowing toward one end of the secondary battery E1, and the diode DR2 interrupts the power output of the secondary battery E2.

Therefore, a DC reactor can be used as the inductor Ldc1, and the inductance of the inductor Ldc1 can be reduced. This makes it possible to make the inductor Ldc1 smaller.

(0121)

(CONFIGURATION VARIATION 2 OF THE FIRST AND SECOND EMBODIMENTS)

A separate device may be provided to vary the on-time and off-time of each switch in the MERS.

For example, as in a DC/DC converter 10G shown in FIG. 19, a dial 300 that changes the control repetition frequency f_1 may be connected to the control unit 200 of the DC/DC converter 10D of the second embodiment of the present invention. Turning the dial 300 clockwise lowers the frequency f_1 , and turning the dial 300 counterclockwise increases the frequency f_1 .

(0122)

When the secondary batteries E1 and E2 are 100 V, the inductor Lm is 200 mH, the capacitors CM1 and CM2 are 1 mF, the time d_1 is 25 ms, the time d_2 is 40 ms, and the frequency f_1 is varied, the relationship of the voltages Vcm1 and Vcm2 of the capacitors CM1 and CM2, the current ILm in the inductor Lm and the gate signals SU1 and SY1, SV1 and SX1, SU2 and SY2, and SV2 and SX2 are as shown in FIG. 20A to 20C.

FIG. 20A, 20B, and 20C show the relationships when the frequency f_1 is 10 kHz, 20 kHz, and 6 kHz, respectively.

(0123)

As shown in FIG. 20A, when the frequency f_1 is 10 kHz, the voltages Vcm1 and Vcm2 rise to approximately 200 V and the current ILm rises to approximately 16 A. In each cycle (e.g., one cycle from the gate signals SU1, SY1, SV1, and SX1 turning on to the gate signals SU2, SY2, SV2, and SX2 turning on), the current ILm flows for approximately 100 ms and does not flow for 100 ms.

As shown in FIG. 20B, when a frequency f_2 is 20 kHz, the voltages Vcm1 and Vcm2 rise to approximately 230 V and the current ILm rises to approximately 25 A. In each cycle (e.g., one cycle from the gate signals SU1, SY1, SV1, and SX1 turning on to the gate signals SU2, SY2, SV2, and SX2 turning on), the current ILm flows almost continuously.

As shown in FIG. 20C, when a frequency f_3 is 6 kHz, the voltages Vcm1 and Vcm2 rise to approximately 180 V and the current ILm rises to approximately 10 A. In each cycle (e.g., one cycle from the gate signals SU1, SY1, SV1, and SX1 turning on to the gate signals SU2, SY2, SV2, and SX2 turning on), the current ILm flows for approximately 100 ms and does not flow until the next cycle.

(0124)

As the frequency increases, the peak capacitor voltage increases and the charge per cycle rises. In addition, the number of recharges per unit time increases. Therefore, when the frequency is increased, the amount of power supplied from the secondary battery E1 to the secondary battery E2 increases the more the frequency increases. However, if one cycle is at least as long as the time that the current flows continuously in one direction in the inductor Lm, switching becomes hard switching. Therefore, one cycle determined by the frequency f_1 should be longer than the time that the current flows continuously in one direction in the inductor Lm.

(0125)

As shown in FIG. 20D, the change in the amount of power supplied from the secondary battery E1 to the secondary battery E2 when the frequency f_1 is varied in this example is approximately 50 W when the frequency f_1 is 6 kHz, approximately 230 W when the frequency f_1 is 10 kHz, and approximately 970 W when the frequency f_1 is 20 kHz, the amount of power supplied increasing as the frequency increases.

(0126)

In this way, by adjusting the frequency f_1 , the amount of power charge per time from the secondary battery E1 to the secondary battery E2 can be adjusted.

In other words, when the control unit 200 turns on the switches of the MERS 101 and 102 substantially simultaneously, turns off the switch of one MERS after a first predetermined time, turns off the other MERS after a second predetermined time, and keeps both MERS switches off for a third predetermined time, the amount of power supplied per time from the secondary battery E1 to the secondary battery E2 can be adjusted by adjusting the third predetermined time.

In the DC/DC converter 10F, turning the dial 300 clockwise increases the amount of charge per time and turning counterclockwise decreases the amount of charge per time.

(0127)

As can be seen from FIG. 20A to 20C, when switching the gate signals from the on signal to the off signal, the capacitor voltage of that MERS is almost zero, and when switching the gate signals from the off signal to the on signal, the current flowing in the inductor L_m is almost zero. Therefore, the switching of each switch is at zero voltage or zero current, and soft switching is achieved with both high and low charges per time.

(0128)

As explained above, the DC/DC converter of the present invention can bidirectionally convert power from the secondary battery E1 to the secondary battery E2 regardless of the size of the voltage by repeatedly turning on the switches of the MERSes 101 and 102 and then controlling one MERS switch to be turned off before the other MERS switch.

(0129)

In addition, by changing the MERSes 101 and 102 to the full-bridge MERSes 103 and 104, and by alternately repeating the two controls of turning on the switches of the MERSes 101 and 102 switches and then turning off the switch of one of the MERSes before the switch of the other MERS, and turning on the switches of the MERSes 101 and 102 and then turning off the switch of the latter MERS before the switch of the former MERS, power can be converted bidirectionally from the secondary battery E1 to the secondary battery E2 regardless of the voltage size, and demagnetization of the inductor L_m can be suppressed.

(0130)

By turning on the switches of the MERSes 101 and 102 substantially simultaneously, turning off the switch of one of the MERSes after a first predetermined time, turning the other MERS off after a second predetermined time, and holding the switches of both MERSes off for a third predetermined time, power can be converted bidirectionally from the secondary battery E1 to the secondary battery E2 regardless of the voltage size, and by adjusting this third predetermined time, the power supplied from the power source on the transmitting side to the power source on the receiving side can be adjusted.

(0131)

The present invention is not limited to the above embodiments, and various variations are possible such as, for example, the following. For example, each setting value in the embodiments is an example, and various other settings are possible. It is not necessary to have the entire configuration described in the embodiments, and a combination of some of the configurations may be used if the desired purpose can be achieved.

(0132)

In each of the above embodiments, the secondary battery E1 was used as a DC power source and the secondary battery E2 was used as a DC load, but of course secondary batteries are not necessary.

For example, the secondary battery E1 may be changed to a household power source rectified and smoothed by a smoothing capacitor, and the secondary battery E2 may be changed to an electrical device that operates when supplied with DC power.

For example, if the side that supplies power (secondary battery E1) does not need to be supplied with power (e.g., a primary battery) or the side that is supplied with power (secondary battery E2) does not need to output power (e.g., a secondary battery), then the diodes DR1 and DR2 can be used as shown in FIG. 14. Doing so will interrupt the power supplied to the side supplying power and interrupt the power output from the side supplied with power.

(0133)

Also, instead of the secondary batteries E1 and E2, a DC busbar may be connected.

For example, instead the rechargeable battery E1, a DC busbar connected to various electrical devices in the home may be connected, and the battery E2 may be the internal battery of an electric vehicle.

In this case, during the night, the internal battery of the electric vehicle is on the power receiving side, and the DC busbar is on the power transmitting side. During the daytime, when the user of the electric vehicle is at home, for example, the electric vehicle battery is on the power transmitting side and supplies power to the DC busbar on the power receiving side.

(0134)

It was explained above that in the above DC-DC converter F [*sic*: 10F], the reverse-conducting semiconductor switches SWV2 and SWX2 of the MERS 102 may always be on. Therefore, the switches SV2 and SX2 of the MERS 102 may be absent as in the DC/DC converter H [*sic*: 10H] shown in FIG. 21. In other words, the MERS on the power receiving side may be a rectifier circuit.

In this case, too, as shown in FIG. 22, the MERS 101 stores the power output from the secondary battery E1 as electrostatic energy, and the MERS 101 is turned on to let current flow through the inductance for storage as magnetic energy, which charges the secondary battery E2.

In the example in FIG. 22, the inductor Ldc1 is 0.2 mH, the capacitor CM1 is 0.5 microF, the leakage inductors LM1 and LM2 are 0.1 mH, the output voltage of the secondary battery E1 is 100 V, and the output voltage of the secondary battery E2 is 70 V.

(0135)

The turn ratio of the high-frequency transformer RFT does not have to be 1:1. The boost-buck ratio can be adjusted as desired by changing it accordingly.

(0136)

In the first and second embodiments, the control unit 200 may be configured from a dedicated electronic circuit comprising a comparator, a flip-flop, a timer, and the like.

For example, the circuit of the control unit 200 may be as in FIG. 23 when the repetition frequency f1 is 7 kHz, the on-time of the gate signals SGGV1 and SGGX1 is 60 microseconds, and the on-time of the gate signals SGGV2 and SGGX2 is 30 microseconds.

(0137)

FIG. 23(a) shows a control circuit that outputs the gate signals SGGV1, SGGX1, SGGV2, and SGGX2 of the DC-DC converter using the one-directional MERS described above. This circuit is equipped with an oscillator OSC and one-shot multivibrators MV1 and MV2.

The oscillator OSC outputs clock pulses with the frequency of 7 kHz (frequency f1).

The outputs of the one-shot multivibrator MV1 are output as the gate signals SGGV1 and SGGX1 to the gates GV1 and GX1 of the reverse-conducting semiconductor switches SWV1 and SWX1. The one-shot multivibrator MV1 responds to the rising clock pulse output by the oscillator OSC by switching the off signal to the on signal, holding the on signal for 60 microseconds, and then switching to the off signal.

Similarly, the outputs of the one-shot multivibrator MV2 are output as the gate signals SGGV2 and SGGX2 to the gates GV2 and GX2 of the reverse-conducting semiconductor switches SWV2 and SWX2. The one-shot multivibrator MV2 responds to the rising clock pulse output by the oscillator OSC, switches the off signal to the on signal, holds the on signal for 30 microseconds, and then switches to the off signal.

(0138)

FIG. 23(b) shows a control circuit that outputs the gate signals SGGU1, SGGV1, SGGX1, SGGY1, SGGU2, SGGV2, SGGX2, and SGGY2 of the DC/DC converter using the bidirectional MERS described above. This circuit is equipped with one-shot multivibrators MU1 and MU2 in addition to the control section 200 described in FIG. 23(a).

The outputs of the one-shot multivibrator MV1 are output as the gate signals SGGU1 and SGGY1 to the gates GU1 and GY1 of the reverse-conducting semiconductor switches SWU1 and SWY1. The one-shot multivibrator MU1 responds to the rising clock pulse output by the oscillator OSC by switching the off signal to the on signal, holding the on signal for 60 microseconds, and then switching to the off signal.

Similarly, the outputs of the one-shot multivibrator MU2 are output as the gate signals SGGU2 and SGGY2 to the gates GU2 and GY2 of the reverse-conducting semiconductor switches SWU2 and SWY2. The one-shot multivibrator MU2 responds to the rising clock pulse output by the oscillator OSC, switches the off signal to the on signal, holds the on signal for 30 microseconds, and then switches to the off signal.

(0139)

In the above embodiment, the control unit 200 controls the gate signals on the basis of the preset times d1 and d2 and the frequency f1. However, the gate signal control can be modified in various ways. For example, the on-time of each switch may be controlled with a duty ratio.

The control unit 200 repeats a control so as to turn on the switches of the MERSes 101 and 102 substantially simultaneously, turn off the switch of one of the MERSes after a first predetermined time, turn off the other MERS after a second predetermined time, and keep the switches of both of the MERSes off for a third predetermined time.

(0140)

Also, the configuration of the control unit 200 in the embodiments can also be realized using an ordinary computer system.

For example, a program for executing the above process performed by the control section 200 can be stored and distributed on a compact disk read-only memory (CD-ROM), a digital versatile disk (DVD) or other computer-readable recording medium, and this program can be installed on a computer to configure the control unit 200 described above.

(0141)

The program may also be stored in a disk device or the like of a predetermined server device on a communication network such as the internet, and may be, for example, superimposed on a carrier wave and downloaded to a computer. Furthermore, the above processing can also be accomplished by transferring the program over a communication network during startup and execution.

In cases where the functions described above are handled by an operating system (OS) sharing the workload or by collaboration between the OS and an application, only the non-OS portion may be stored on a medium for distribution or downloaded to a computer.

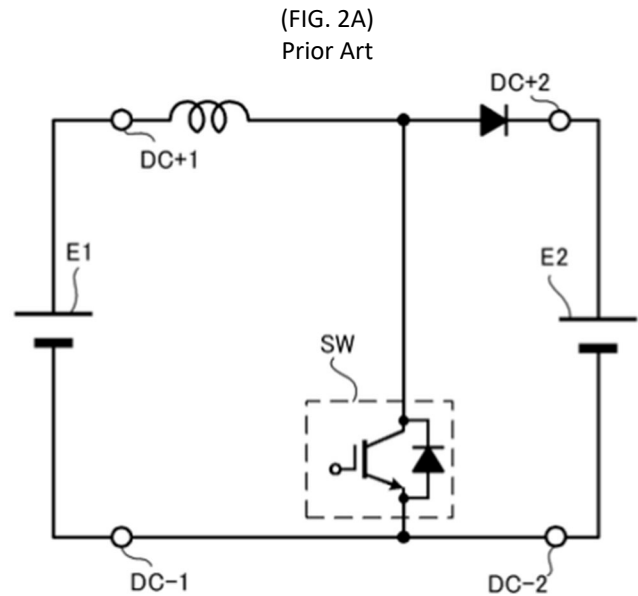
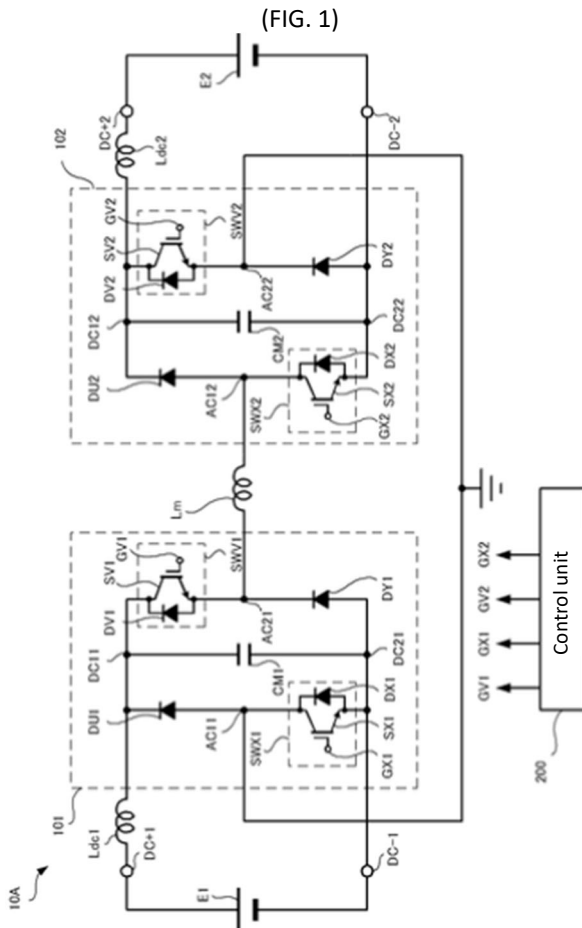
(DESCRIPTION OF THE REFERENTIAL CODES OR SYMBOLS)

(0142)

10A to 10H	DC/DC converters	
DC+1, DC+2	DC input terminals	
DC-1, DC-2	DC output terminals	
Ldc1, Ldc2, Ldc11, Ldc12, Ldc21, Ldc22	inductors	

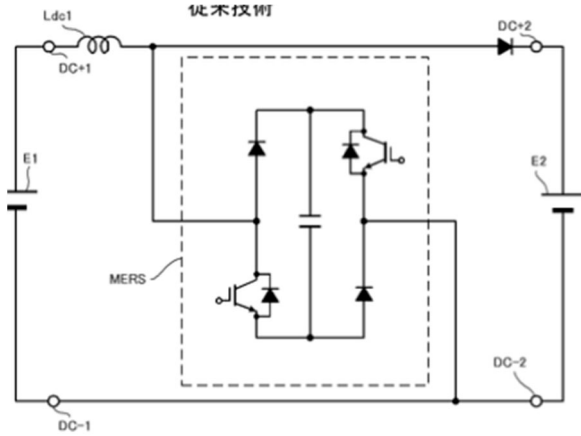
101, 102, 103, 104
 AC11, AC21, AC12, AC22
 DC11, DC21, DC12, DC22
 SWU1, SWV1, SWX1, SWY1, SWU2, SWV2, SWX2, SWY2
 DU1, DV1, DX1, DY1, DU2, DV2, DX2, DY2
 SU1, SV1, SX1, SY1, SU2, SV2, SX2, SY2
 GU1, GV1, GX1, GY1, GU2, GV2, GX2, GY2
 CM1, CM2
 Lm, Lm1, Lm2
 RFT
 L1
 L2
 LM1, LM2
 200
 SGGU1, SGGV1, SGGX1, SGGY1, SGGU2, SGGV2, SGGX2, SGGY2
 E1, E2

MERsEs
 AC terminals
 DC terminals
 reverse-conducting semiconductor switches
 diode sections
 switch sections
 gates
 capacitors
 inductors
 high-frequency transformer
 primary winding
 secondary winding
 leakage inductance
 control unit
 gate signals
 secondary batteries



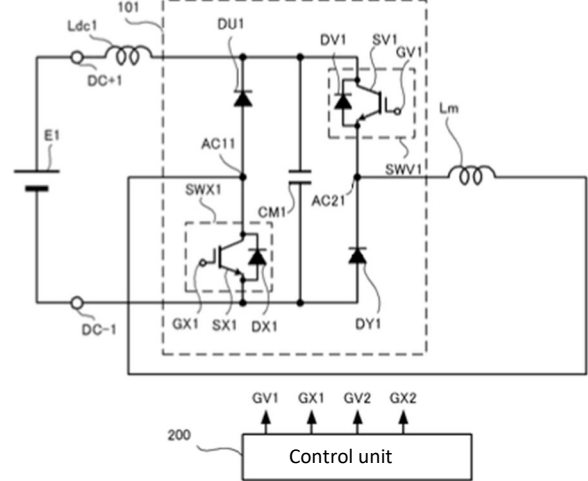
(FIG. 2B)

Prior Art

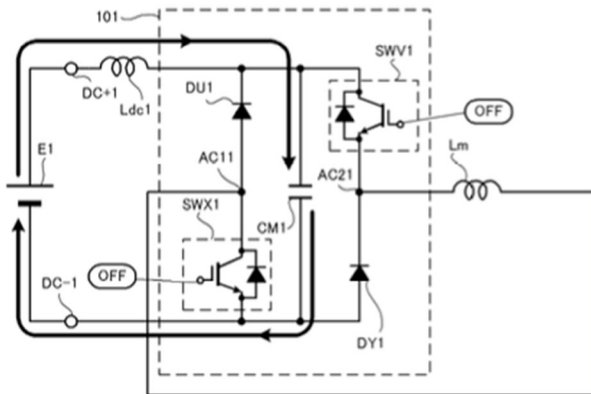


(FIG. 2C)

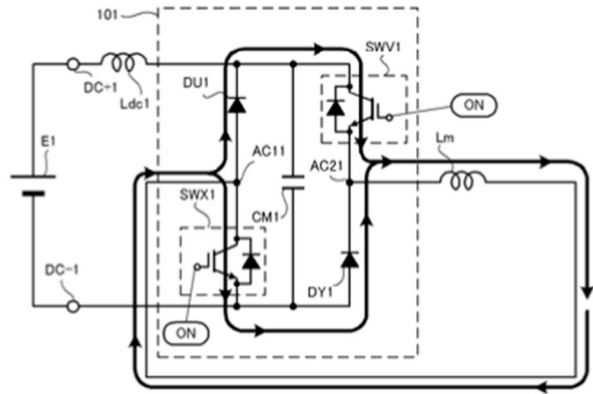
Portion of the Present Invention



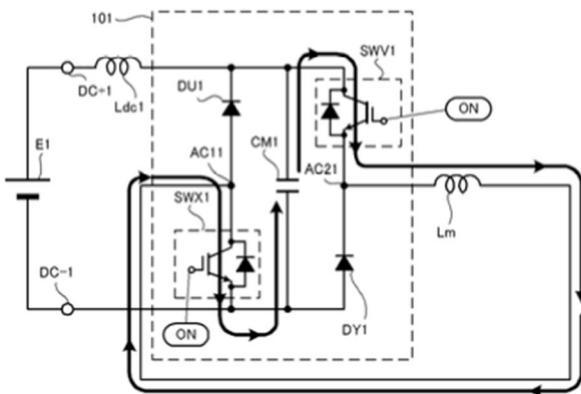
(FIG. 3)



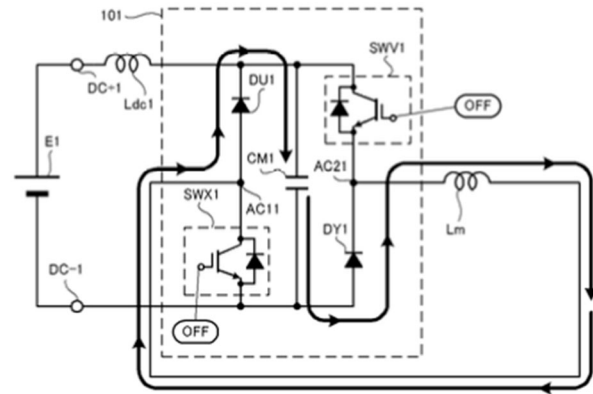
(FIG. 4B)



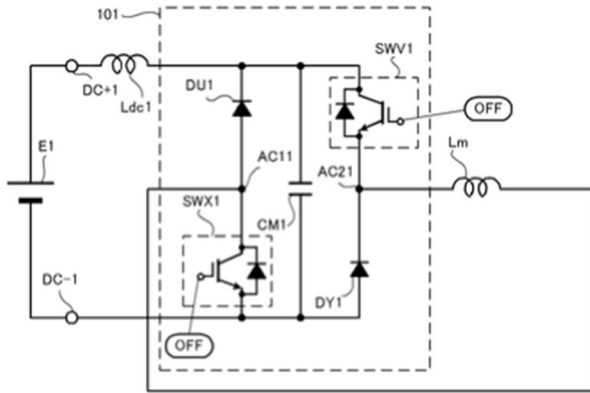
(FIG. 4A)



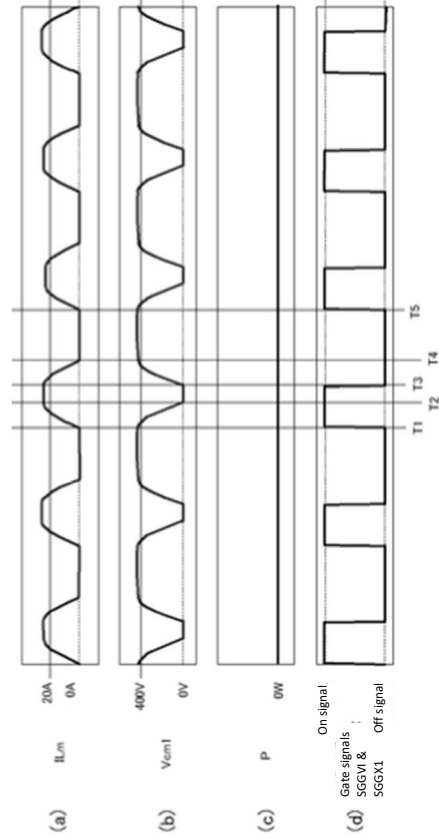
(FIG. 4C)



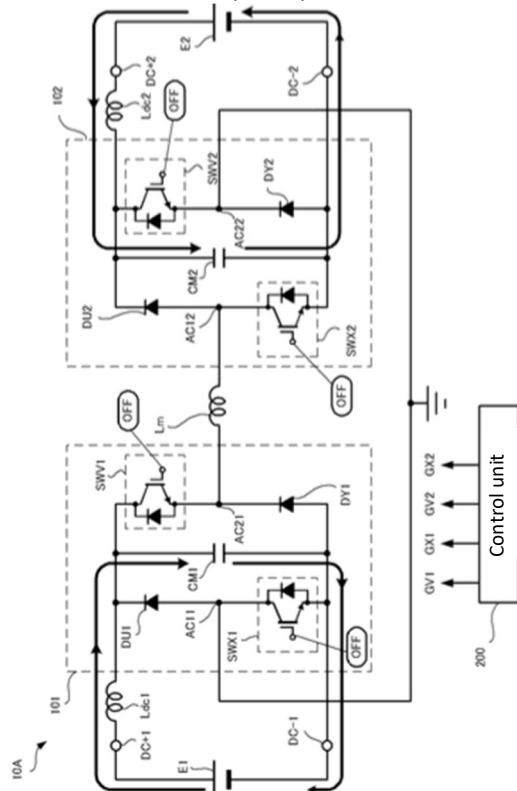
(FIG. 4D)



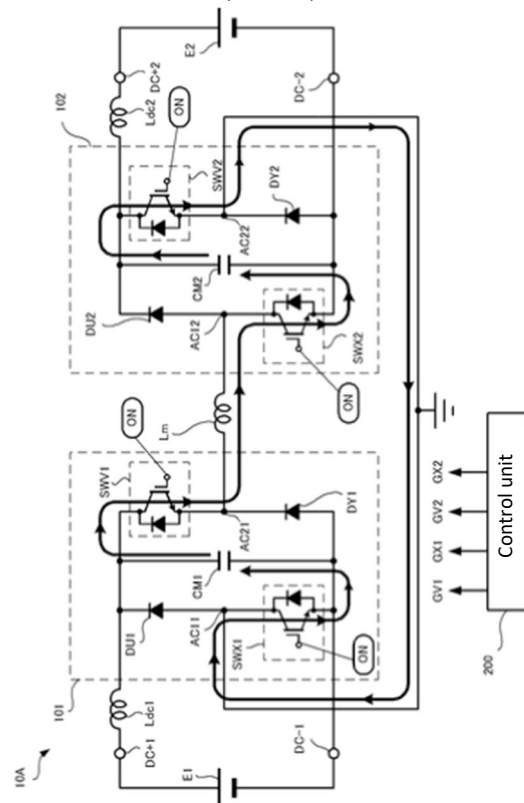
(FIG. 5)

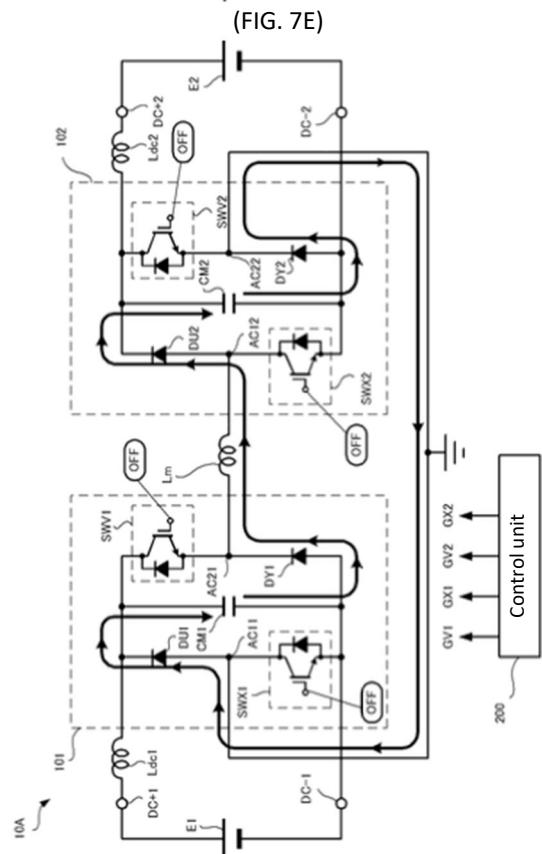
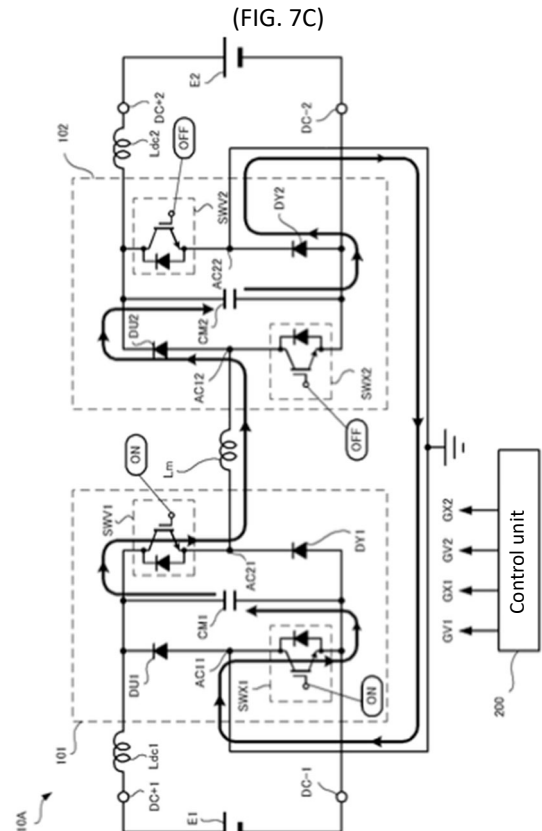
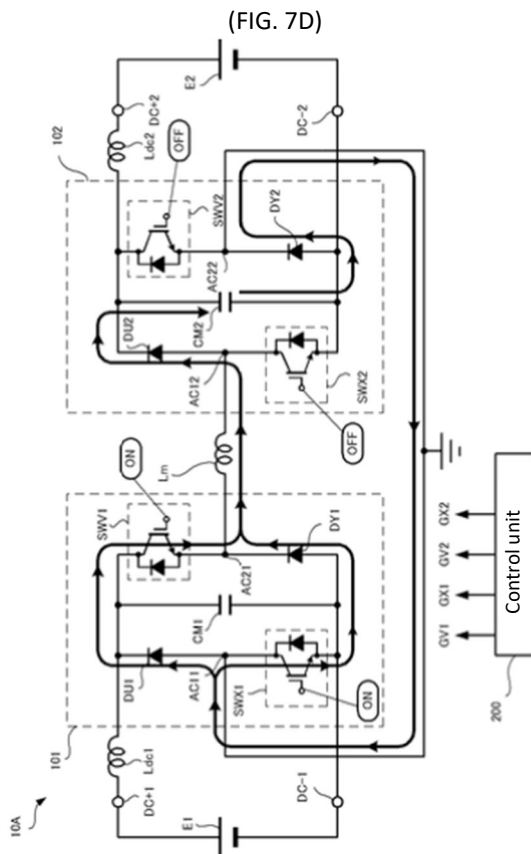
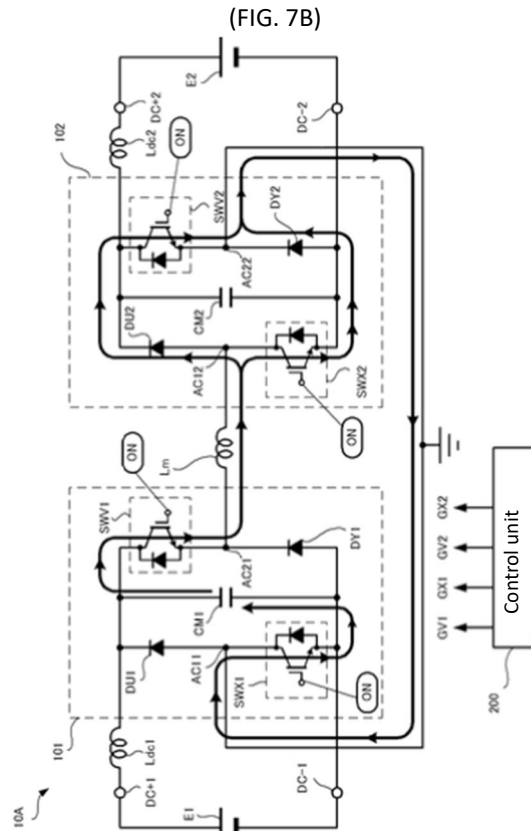


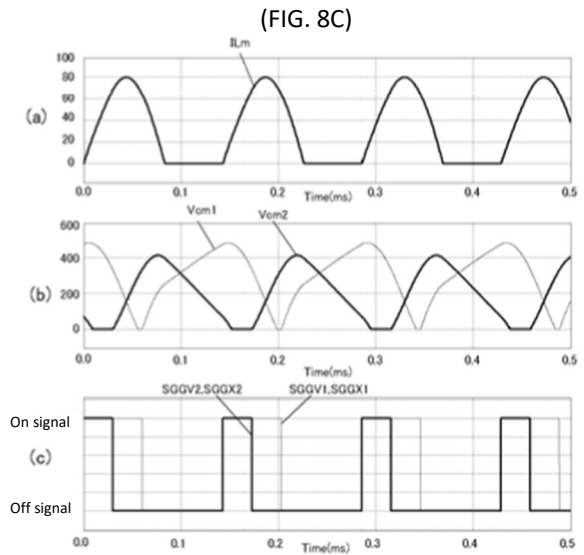
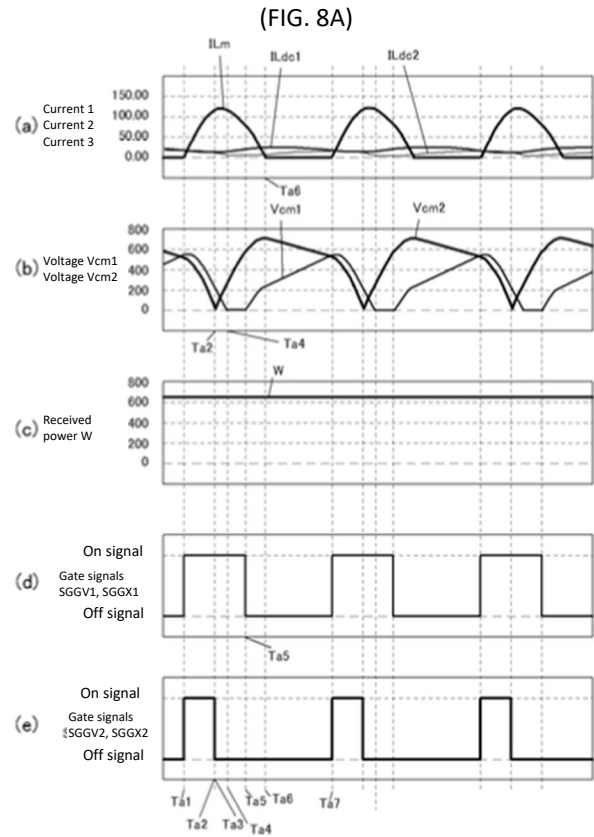
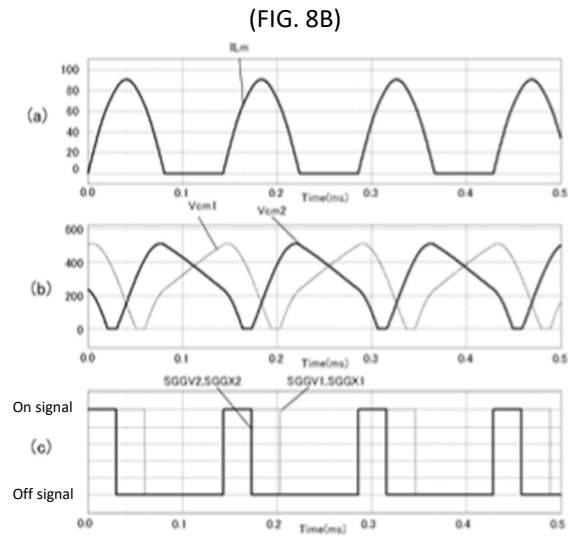
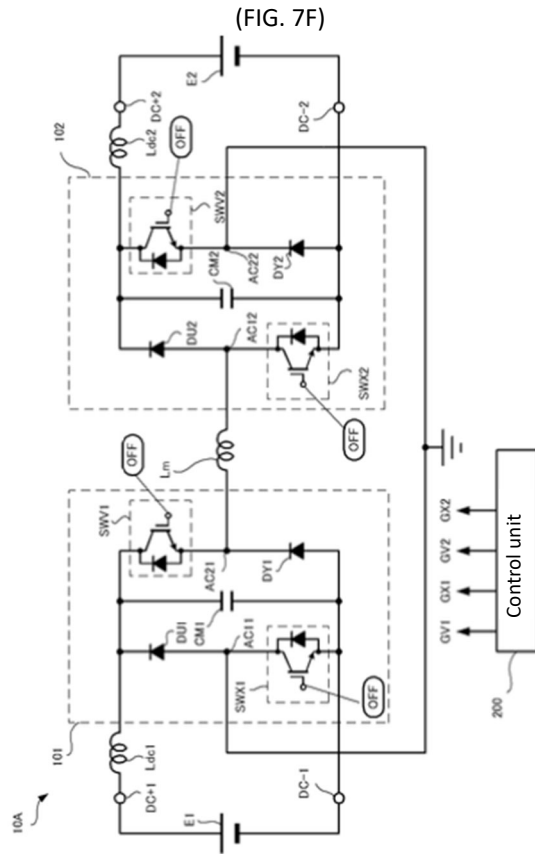
(FIG. 6)



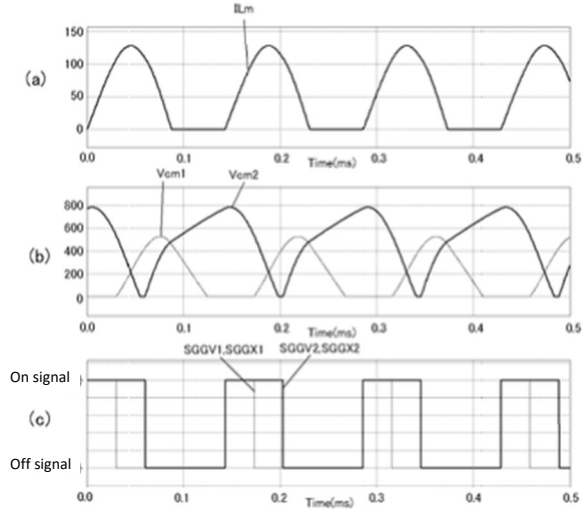
(FIG. 7A)



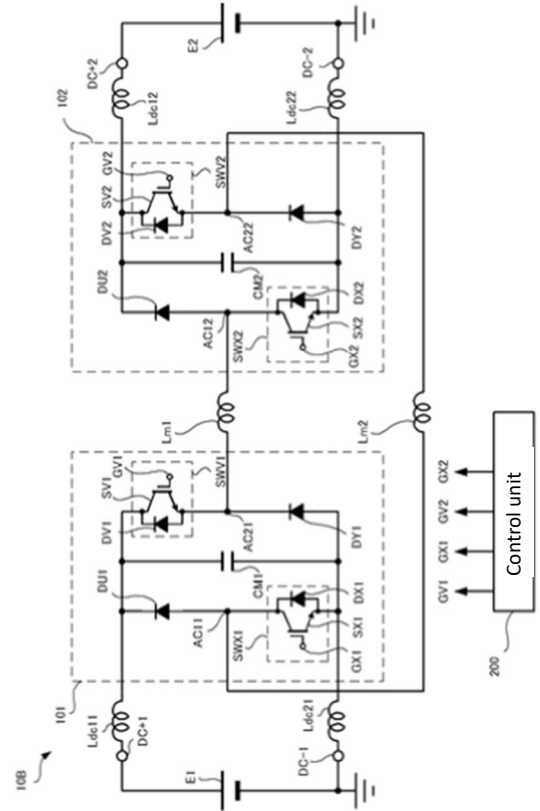




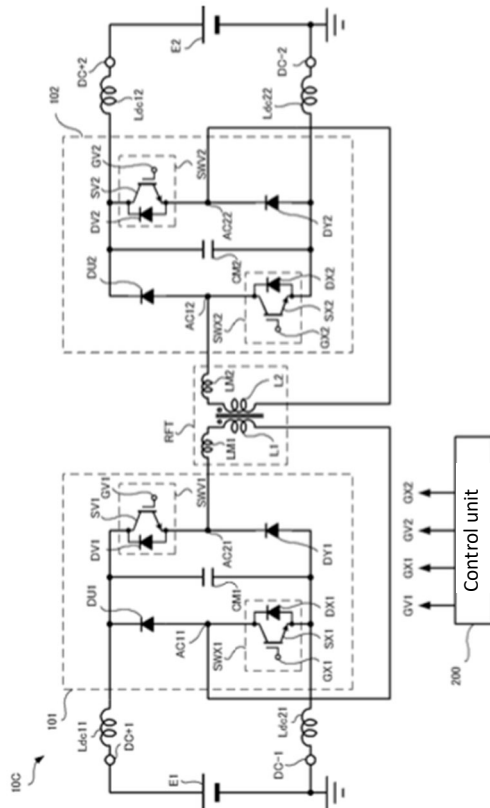
(FIG. 8D)



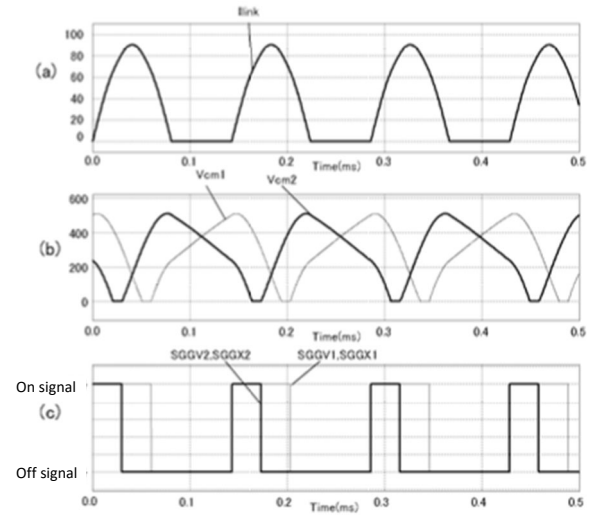
(FIG. 9)



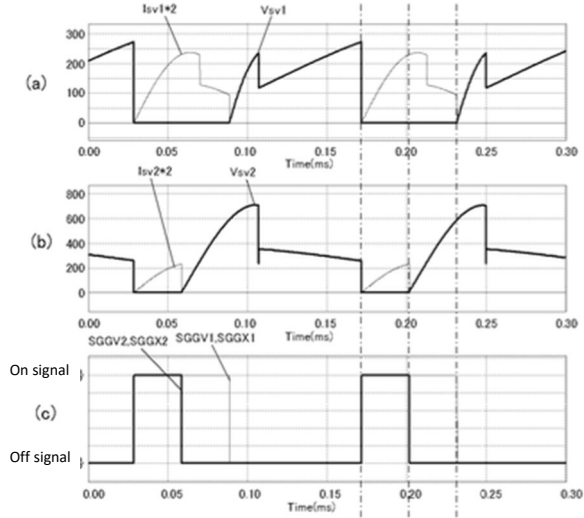
(FIG. 10)



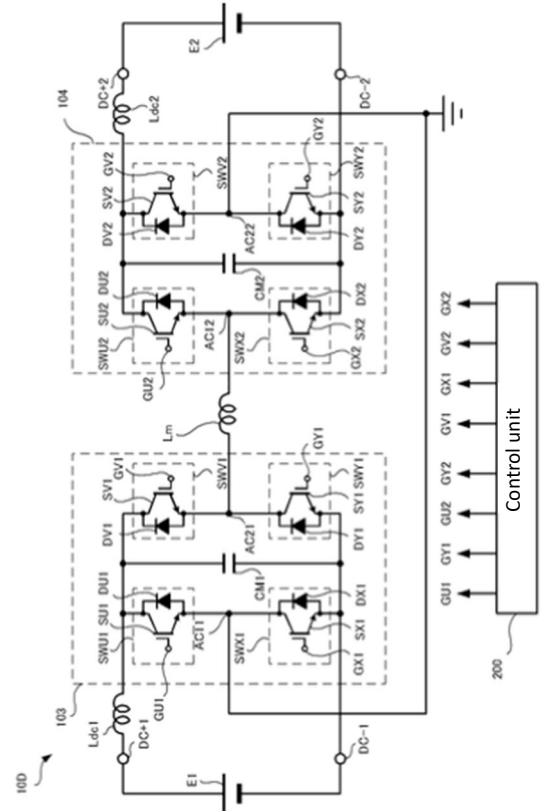
(FIG. 11)



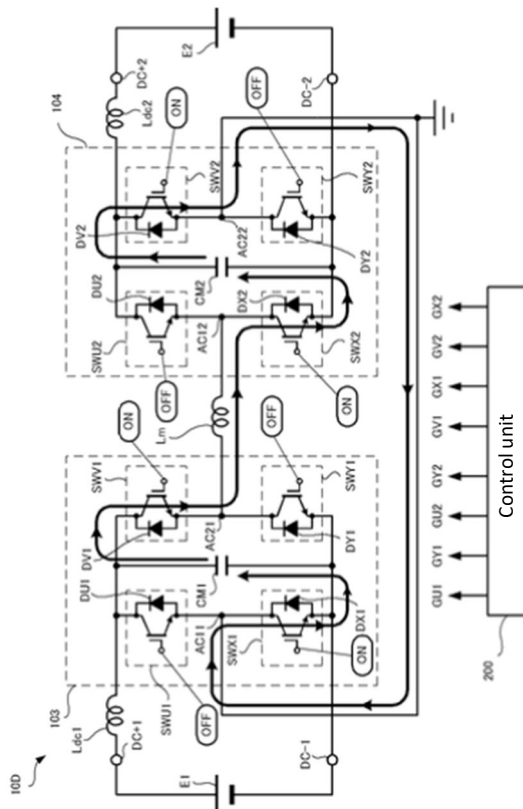
(FIG. 12)



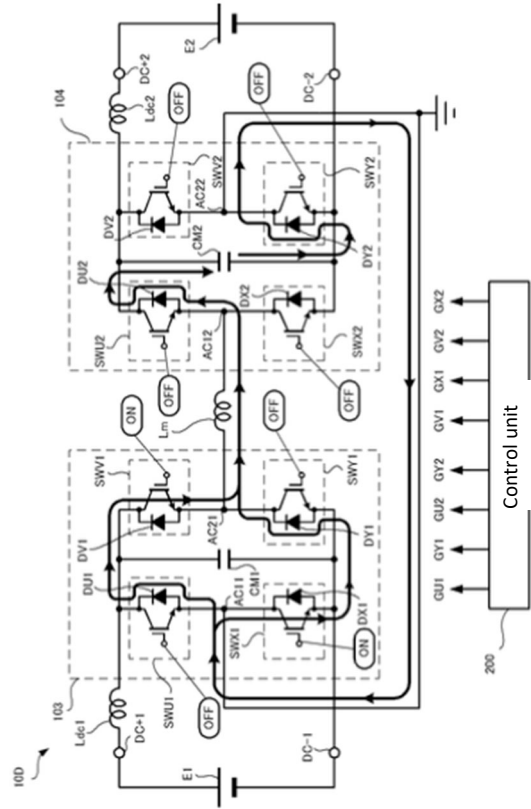
(FIG. 13)

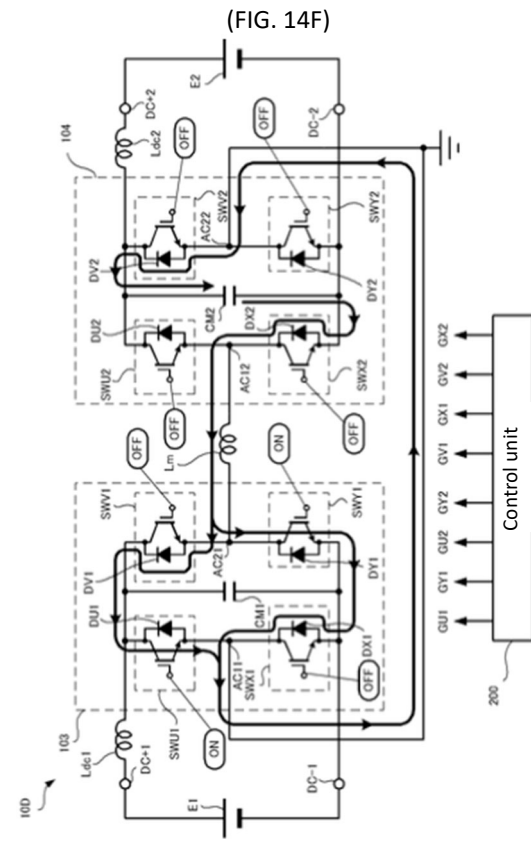
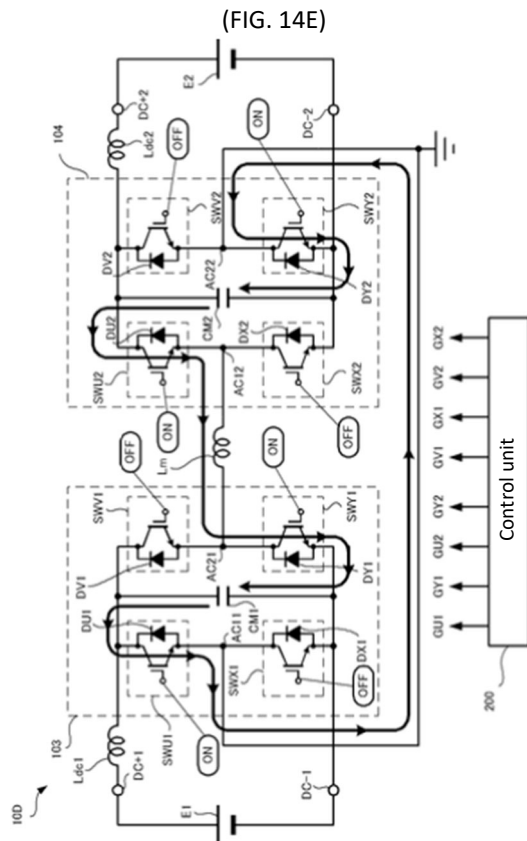
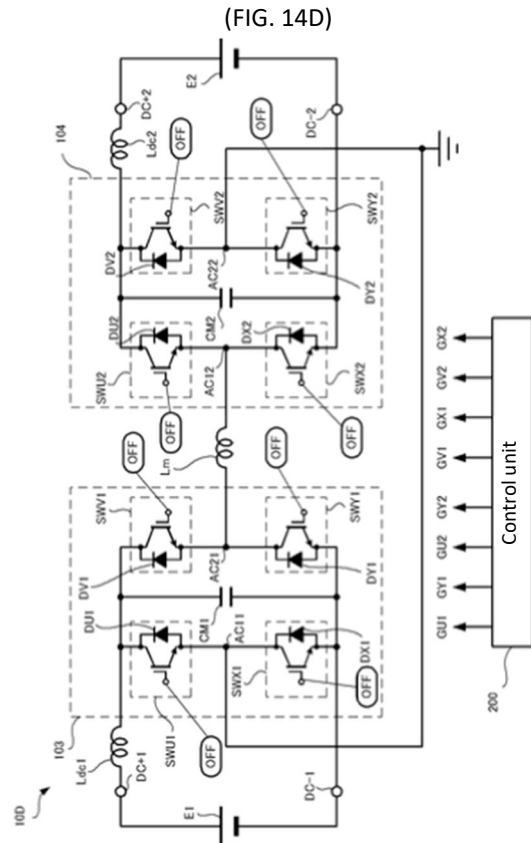
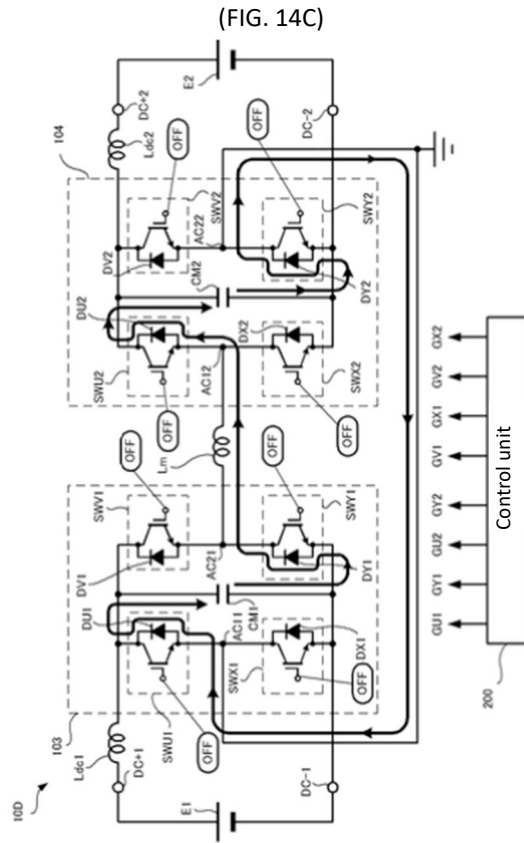


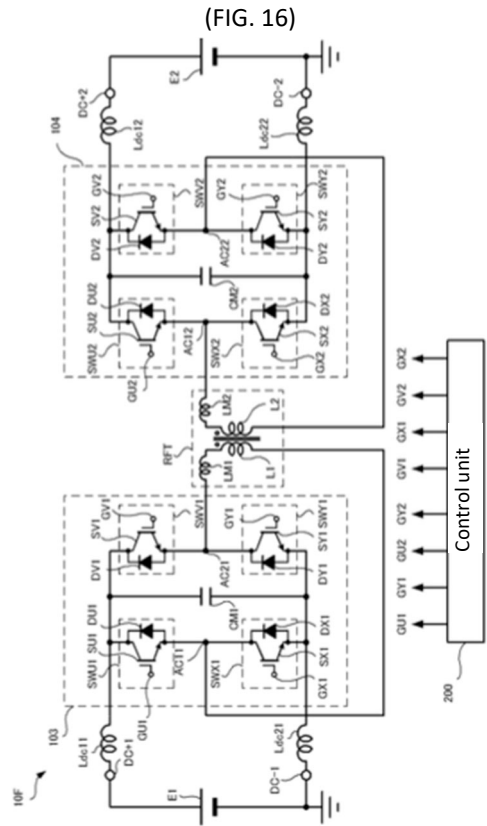
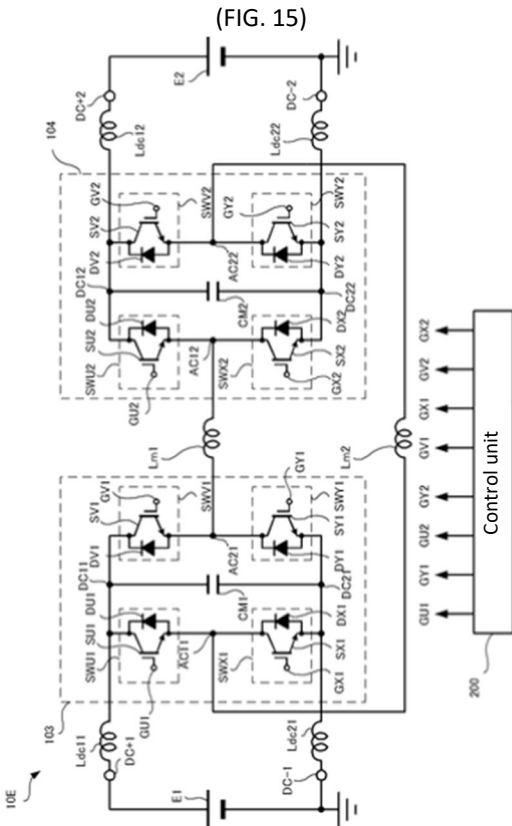
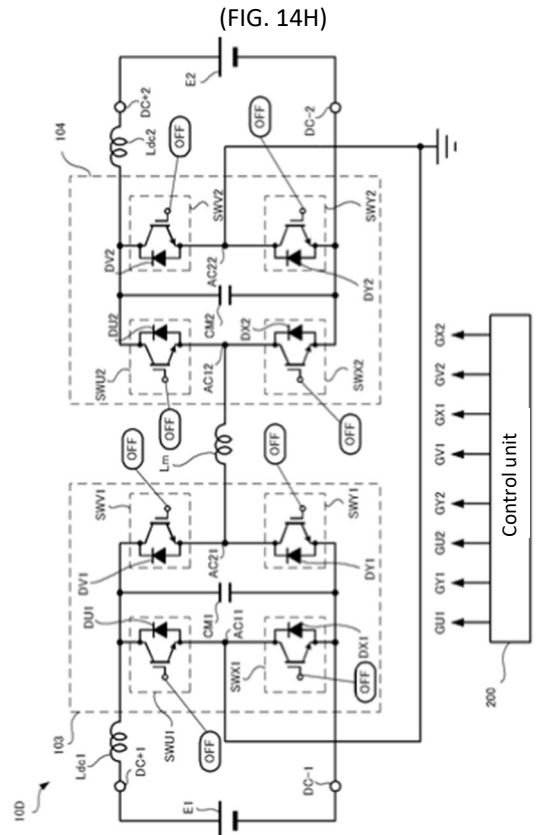
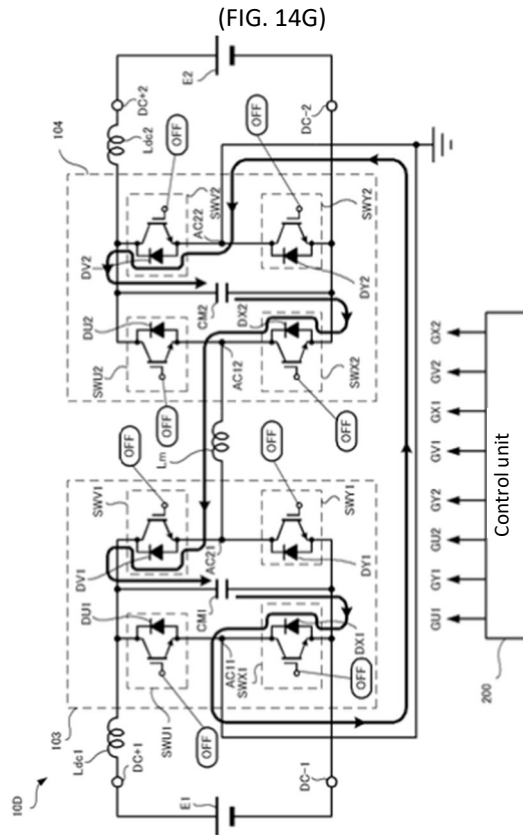
(FIG. 14A)



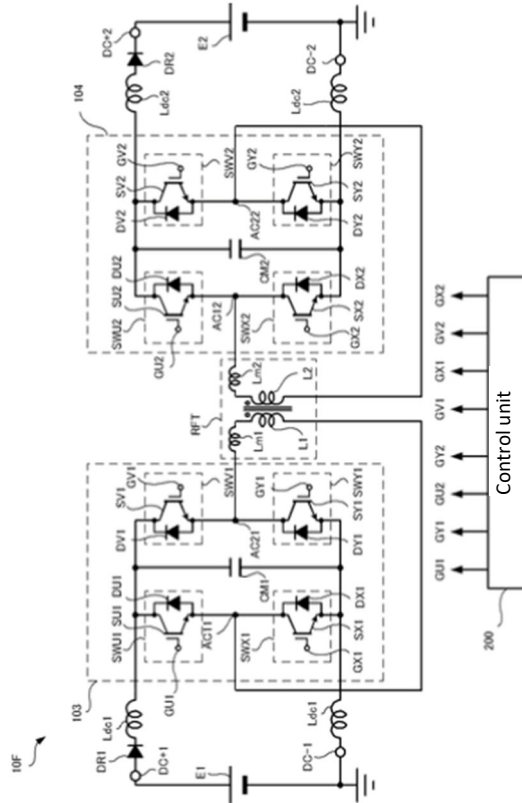
(FIG. 14B)



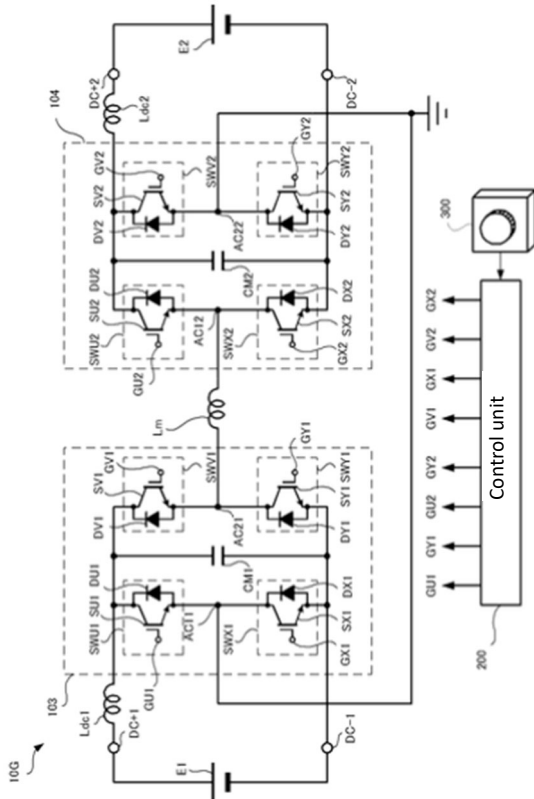




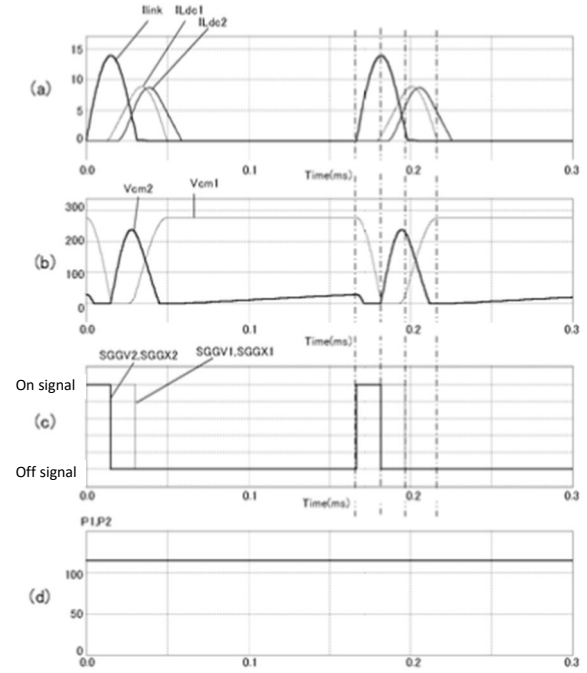
(FIG. 17)



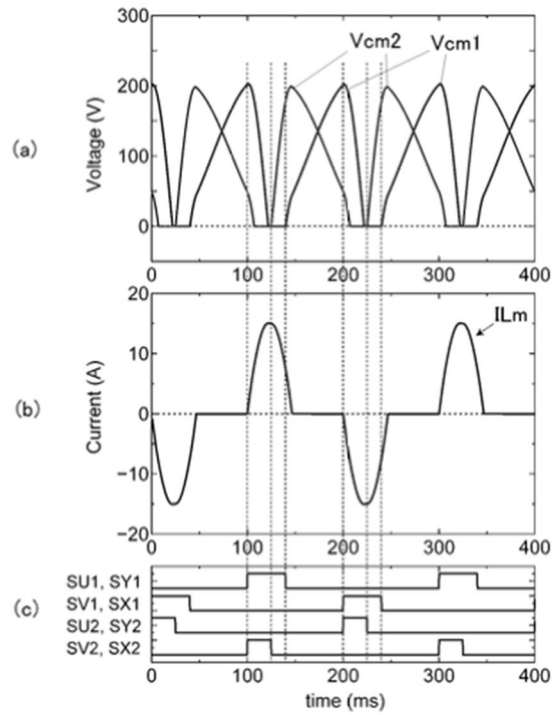
(FIG. 19)

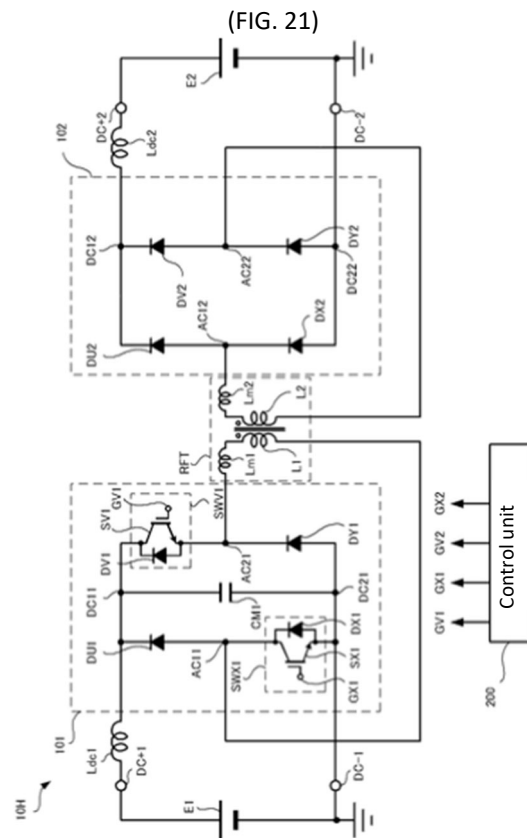
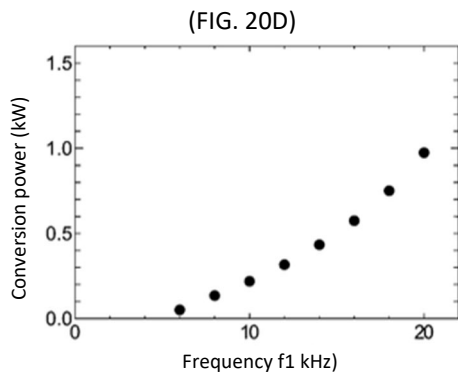
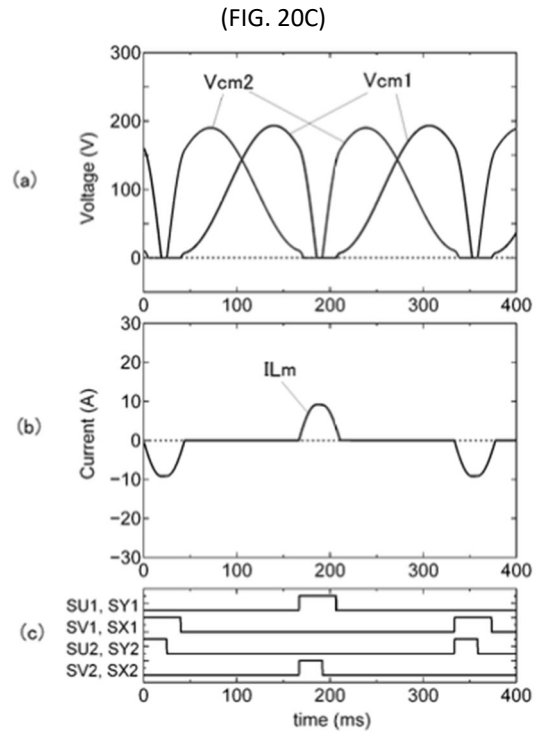
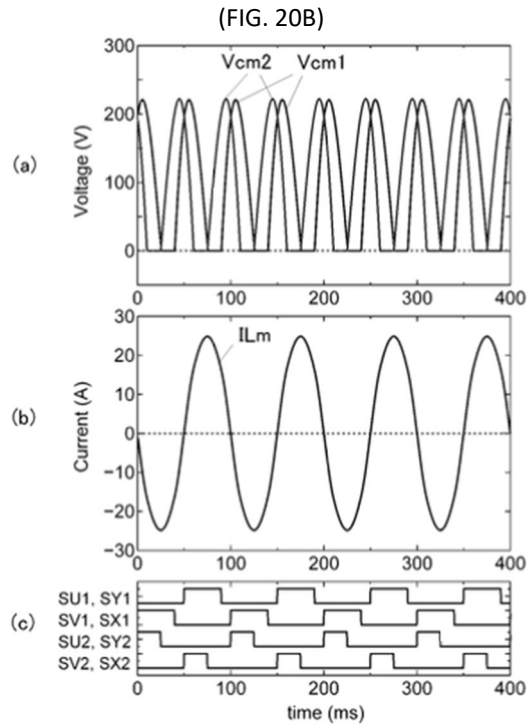


(FIG. 18)

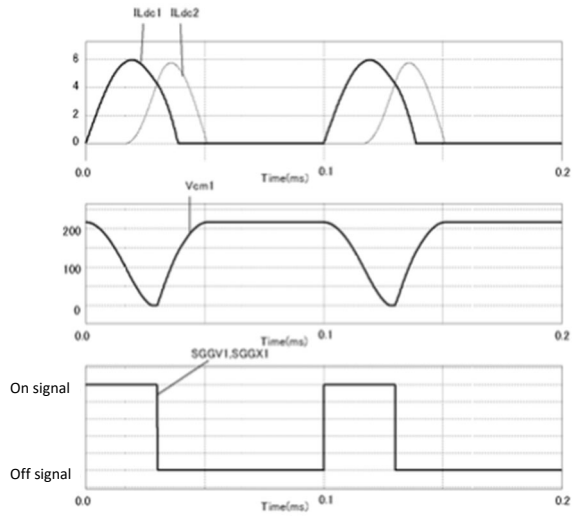


(FIG. 20A)



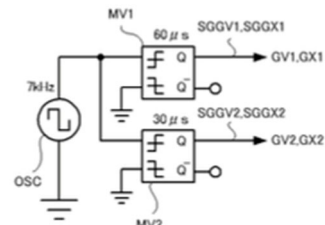


(FIG. 22)



(FIG. 23)

(a)



(b)

