

Secondary-side Adaptive Digital Controlled Series Resonant DC-DC Converters for Low Voltage High Current Applications

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Abstract - It is more difficult for VRMs to supply power to future microprocessors, which need lower supply voltage, large current and large current slew rate. Most of today's VRMs are with inductor-capacitor type output filters. The inductor in the output filter limits the current transient speed. Hence, the secondary-side controlled series resonant converter with capacitor type filter is introduced in this paper to overcome this limitation. The lack of the inductor in its output filter makes it have very quick dynamic response. Also an adaptive control scheme is proposed to control the current-type synchronous MOSFETs, which eliminates the current sensor in the power path. Theoretical analysis and simulation results verify the proposed concept.

I. INTRODUCTION

To decrease power consumption and increase the speed, the next generation of computer microprocessors will operate at significantly lower voltages and higher currents than today's generation. Recently, the supply voltage is reduced to around 1V, which was 5V or 3.3V five or ten years ago. It is expected that in future the supply voltage is going to drop to a level of 0.8V or lower. Future processors will require more than 200A current at the voltage of about 0.8V and needs up to around 120A/ns current transient speed. This makes it much more difficult to maintain an accurate voltage regulation within tight tolerance range for voltage regulator modules (VRM). [1]- [3]

Actually, output filters of most of today's VRM topologies are of inductor input type. Normally a relatively large inductor should be used to limit output current ripple. During the transient period, this large inductor limits the energy transfer speed of the VRM such that the capacitor alone must discharge its stored energy to the load. To improve load transient response, a small inductor is essentially required, which will cause large current ripple. For converters with synchronous rectifiers, the current in synchronous rectifier MOSFET will go to negative value at light load and current swing range is nearly keeping constant from light load to full load. Obviously, it is not efficient operating mode. At the same time, large current ripple will not only cause large conduction losses, but also increase turn-off losses of MOSFET. Moreover, high DC current as well as high AC

ripple current on the output inductor will cause extra conduction losses.

Therefore, when the output filter inductor is eliminated, the current transient speed at the VRM output will be improved for sure. This is the main reason that series resonant DC/DC converter is introduced into low voltage high current applications. Only filter capacitors are employed in the series resonant converter.

Traditionally, the series resonant was regarded as an unsuitable topology for low voltage high current applications [11]. However, for future processors which require lower voltage, higher current, and faster slew rate, the output filter capacitors are working as energy-store components, rather than as ripple current filters. When we turn to capacitor type filter, it may not increase the size of filter capacitor, compared to inductor-capacitor type filter. The use of high-density capacitors with very low parasitics such as 100uF/1.2mΩ ceramic capacitor ensures low ripple voltage and low output voltage spike during load transients.

To further improve current transient speed, the secondary side control (control synchronous rectifiers) is proposed. Thanks to the difference between diode forward voltage (V_d) and synchronous MOSFET on-state voltage, controlling the duty cycle of the rectifier switches will control AC equivalent resistance, then will obtain output voltage regulation. Carefully designing characteristics of the series resonant tank as well as the controlled AC equivalent resistance will achieve good performance while keeping high efficiency over full load range.

A current sensorless adaptive digital control is also proposed to drive the current-type synchronous rectifier MOSFET, which solves the delay effect the current-sensor circuit and gate driver, and also eliminates the current sensor in the power path. It can be extended to generate gate signals for all current-type synchronous rectifier MOSFETs.

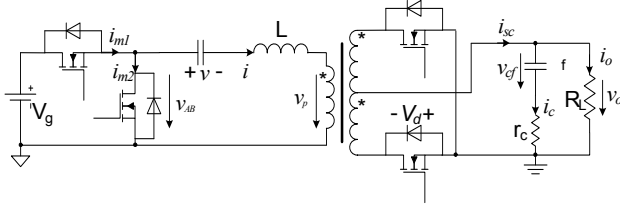


Figure 1. A typical APWM series resonant converter

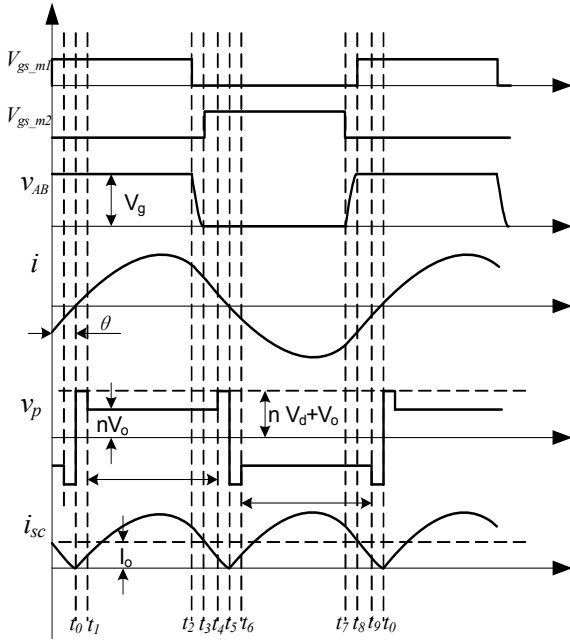


Figure 2. The typical steady state operating waveforms

II. OPERATION PRINCIPLE OF THE PROPOSED CIRCUIT

Series resonant DC/DC converters with constant switching frequency control are utilized. The main stage on the primary side of the transformer could be either half bridge or full bridge with L-C series resonant tank. The secondary side is a central-tapped full-wave rectifier. The control method could be the conventional PWM control, phase-shift control or asymmetrical PWM control [5-10]. Figure 1 shows a typical asymmetric PWM (APWM) series resonant converter, which will be used to illustrate the principle of operation.

The main switches (M_1 & M_2) operate in complementary mode against input voltage variations. The rectifier switches (S_1 & S_2) operate in PWM control mode against load variations. The voltage regulation can be achieved by varying the AC equivalent resistance. Because of the difference between synchronous MOSFET on-state voltage $V_{ds(on)} = i_{sc} \times R_{ds}$ and diode forward voltage (V_d) and, changing duty cycle of the rectifier switches (S_1 & S_2) will change the AC equivalent resistance. The synchronous MOSFETs are fully turned on at full load, while they are partly turned on at reduced load. Such an output regulation mode may cause efficiency impairment somewhat at reduced load. But carefully choosing quality factor (Q_o) and resonant frequency ratio (ω) of the resonant tank will help improve

efficiency at reduced load. But the benefit is that it could achieve faster load transient response. Actually the equivalent regulation frequency is twice the switching frequency and during the transient period, transient-to-response delay is also reduced by half. If the secondary-side control is combined with the primary-side control, the efficiency could be improved further at reduced load.

The typical steady state operating waveforms are shown in Figure 2 and the equivalent circuit of each interval is shown in Figure 3. For each interval, the operation of converter is described as follow.

Interval (t_0 - t_1): At t_0 , the resonant current i is going across zero. During this interval, M_1 is on and M_2 is off. S_1 and S_2 are off. The output voltage v_{AB} of the chopper is V_g . Current i_{sc} goes through the body diode of S_2 . So the voltage on the primary side of transformer is $n(V_d + V_o)$. At t_1 , S_2 is turned on for regulation.

Interval (t_1 - t_2): During this interval, M_1 and S_2 are on, and M_2 and S_1 are off. The output voltage v_{AB} of the chopper is V_g . The voltage on the primary side of transformer is nV_o , if neglecting voltage drop when the MOSFET is on. At t_2 , M_1 is turned off.

Interval (t_2 - t_3): At the beginning of this interval, M_1 is turned off. The positive current flowing through the resonant branch forces the charging of the output capacitance C_{m1} of main switch M_1 and the discharging of the output capacitance C_{m2} of M_2 . Once C_{m1} has fully charged and C_{m2} has fully discharged. The current forces the conduction of body diode D_{m2} of M_2 . At t_3 , M_2 is turned on to achieve zero voltage switching (ZVS).

Interval (t_3 - t_4): During this interval, M_1 is off and M_2 is on. S_1 is off and S_2 is still on. The output voltage v_{AB} of the chopper is zero. The voltage on the primary side of transformer is nV_o . At t_4 , S_2 is turned off for regulation.

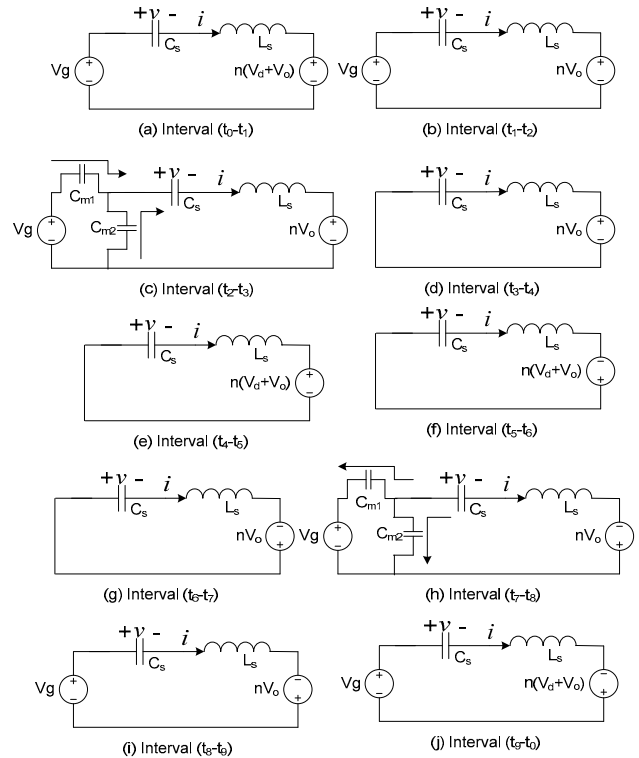


Figure 3. Equivalent circuits of each interval

Interval (t_1 - t_3): During this interval, M_1 is off and M_2 is on. S_1 and S_2 are off. The output voltage v_{AB} of the chopper is zero. Current i_{sc} goes through the body diode of S_2 . The voltage on the primary side of transformer is $n(V_d + V_o)$. At t_5 , the resonant current i is going across zero. Current through the body diode of S_2 is diminished to zero.

Interval (t_3 - t_6): The resonant current changes its direction at t_5 . It forces conduction of the body diode of S_1 . The voltage on the primary side of transformer also changes its direction, $-n(V_d + V_o)$. At t_6 , S_1 is turned on for regulation.

Interval (t_6 - t_7): During this interval, M_2 and S_1 are on, and M_1 and S_2 are off. The output voltage v_{AB} of the chopper is zero. The voltage on the primary side of transformer is $-nV_o$. At t_7 , M_2 is turned off.

Interval (t_7 - t_8): At the beginning of this interval, M_2 is turned off. The negative current flowing through the resonant branch forces the discharging of the output capacitance C_{m1} of main switch M_1 and the charging of the output capacitance C_{m2} of M_2 . Once C_{m1} has fully discharged and C_{m2} has fully charged. The current forces the conduction of body diode D_{m1} of M_1 . At t_8 , M_1 is turned on to achieve zero voltage switching (ZVS).

Interval (t_8 - t_9): During this interval, M_1 is on and M_2 is off. S_2 is off and S_1 is still on. The output voltage v_{AB} of the chopper is V_g . The voltage on the primary side of transformer is $-nV_o$. At t_9 , S_1 is turned off for regulation.

Interval (t_9 - t_{10}): During this interval, M_1 is on and M_2 is off. S_1 and S_2 are off. The output voltage v_{AB} of the chopper is V_g . Current i_{sc} goes through the body diode of S_2 . The voltage on the primary side of transformer is $-n(V_d + V_o)$. At t_{10} , the resonant current i goes across zero. Current through the body diode of S_1 is diminished to zero. Another operating cycle begins.

Description above illustrates the typical operation of this converter. Actually, the turn-off of synchronous MOSFET S_2 could occur before or after the turn-off of main MOSFET M_1 , and the turn-off of synchronous MOSFET S_1 could occur before or after the turn-off of main MOSFET M_2 . There is a little difference in the operation of the converter. But it has no effect on the steady state analysis.

III. STEADY STATE ANALYSIS AND CHARACTERISTICS OF THE CONVERTER

To simply the analysis, the following assumptions are made:

- 1) The main switches and their diodes (M_1 & M_2) are ideal. The duty cycle of switch M_1 is D_m and the duty cycle of switch M_2 is $1-D_m$. The dead time between the two switches is neglected.
- 2) The rectifier switches (S_1 & S_2) are ideal, but their body diode forward voltage is V_d .
- 3) The effect of capacitors across the switches is negligible.
- 4) An ac equivalent resistance at the primary of transformer represents the output rectification stage.

Since the secondary-side control is applied to this converter, the ac equivalent resistance is different from that described in [6-11]. The voltage v_p on the primary side of transformer can be expressed as:

$$v_p(t) = \begin{cases} n \cdot (V_d + V_o) & t_0 \leq t < t_1 = t_0 + \frac{(1-D) \cdot T_s}{4} \\ n \cdot V_o & t_1 \leq t < t_4 = t_0 + \frac{(1+D) \cdot T_s}{4} \\ n \cdot (V_d + V_o) & t_4 \leq t < t_5 = t_0 + \frac{T_s}{2} \\ -n \cdot (V_d + V_o) & t_5 \leq t < t_6 = t_0 + \frac{(3-D) \cdot T_s}{4} \\ -n \cdot V_o & t_6 \leq t < t_9 = t_0 + \frac{(3+D) \cdot T_s}{4} \\ -n \cdot (V_d + V_o) & t_9 \leq t < t_{10} = t_0 + T_s \end{cases}$$

The voltage v_p can be represented in terms of Fourier series in one switching period T_s as follow, if t_0 is assumed to be zero to simply the derivation.

$$v_p(t) = \sum_{k=1,3,5,\dots} \left[\frac{4n \cdot (V_d + V_o) - 4n \cdot V_d \cdot \sin \frac{k\pi}{2} \cdot \sin \frac{kD\pi}{2}}{k\pi} \cdot \sin(k\omega t) \right]$$

Its fundamental component is used in deriving the ac equivalent resistance. That's,

$$V_p(RMS) = \frac{4n \cdot V_o \cdot (1 + \alpha - \alpha \cdot \sin \frac{D\pi}{2})}{\pi\sqrt{2}}$$

The resonant current i is in phase with the fundamental component of v_p , as shown in Figure 2. The series resonant converter uses a capacitive output filter and therefore drives the rectifier with a current source. So the fundamental component of the resonant current can be estimated as [11]:

$$I(RMS) = \frac{\pi}{2\sqrt{2}} \cdot \frac{I_o}{n} = \frac{\pi}{2\sqrt{2}} \cdot \frac{V_o}{n \cdot R_L}$$

Hence, the ac equivalent resistance can be given as:

$$\begin{aligned} R_{ac} &= \frac{V_p(RMS)}{I(RMS)} = \frac{8 \cdot n^2 \cdot R_L}{\pi^2} (1 + \alpha - \alpha \cdot \sin \frac{D\pi}{2}) \\ &= R_{aco} \cdot (1 + \alpha - \alpha \cdot \sin \frac{D\pi}{2}) \end{aligned}$$

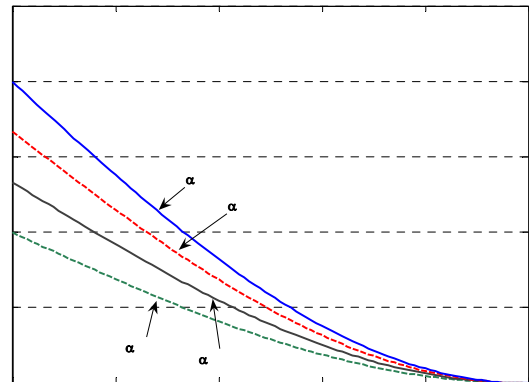


Figure 4. AC equivalent resistance regulation

It can be found that the ac equivalent resistance of the output rectifier stage is regulated by the secondary-side control duty cycle. The ac equivalent resistance also varies with the voltage ratio α . For example, for a low voltage output $V_o = 1$ (V), normally α varies from 0.6 to 1.2, depending on what kind of synchronous MOSFETs are used.

Figure 4 shows the ac equivalent resistance regulation ratio, which is defined by

$$Ratio = 1 + \alpha - \alpha \cdot \sin \frac{D\pi}{2}$$

It can be found that at larger duty cycle α will have less effect on the regulation ratio. Therefore, designing for large duty cycle within whole load ranges are always preferred to reduce the effect of α variations.

The voltage v_{AB} on the input of the resonant tank also can be given using Fourier series as (For simplicity, here in respect of the origin in Figure 2):

$$v_{AB}(t) = D_m \cdot V_g + \sum_{k=1}^{\infty} \left[\frac{2V_g \cdot \sin(k \cdot D_m \cdot \pi)}{k\pi} \cdot \cos(k \cdot \omega_o \cdot t - k \cdot D_m \cdot \pi) \right]$$

where ω_o is the switching frequency.

The following qualities are defined as:

$$\omega_r = \frac{1}{\sqrt{L_s \cdot C_s}}$$

$$\omega = \frac{\omega_o}{\omega_r}$$

$$Q_o = \frac{\omega_r \cdot L_s}{R_{ac}}$$

$$V_{AB(k)}(t) = \frac{2V_g \cdot \sin(k \cdot D_m \cdot \pi)}{k\pi} \cdot \cos(k \cdot \omega_o \cdot t - k \cdot D_m \cdot \pi)$$

Figure 5 shows the k^{th} harmonic equivalent circuit. Obviously, the resonant current i can be expressed as:

$$i(t) = \sum_{k=1}^{\infty} \left[\frac{2V_g \cdot \sin(k \cdot D_m \cdot \pi)}{k\pi \cdot Z_{ink}} \cdot \cos(k \cdot \omega_o \cdot t - k \cdot D_m \cdot \pi - \theta_k) \right]$$

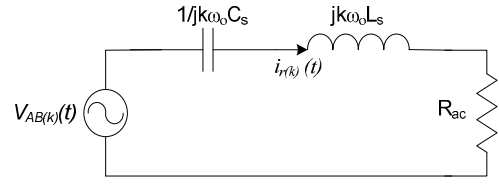
$$Z_{ink} = R_{aco} \cdot \left(1 + \alpha - \alpha \cdot \sin \frac{D\pi}{2} \right) \cdot \left[1 + Q_o^2 \cdot \left(k\omega - \frac{1}{k\omega} \right)^2 \right]^{1/2}$$

$$\theta_k = \arctan \left[Q_o \cdot \left(k\omega - \frac{1}{k\omega} \right) \right]$$

Therefore, the output current and voltage can be expressed as:

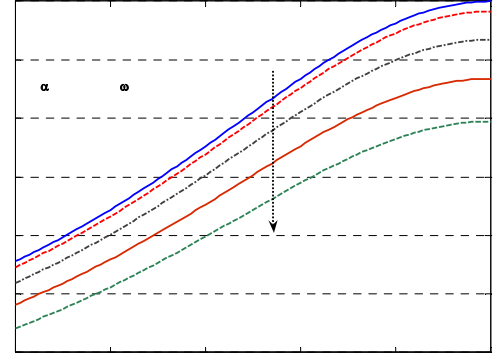
$$I_o = \frac{1}{T_s} \int_0^{T_s} |n \cdot i(t)| \cdot dt = \frac{n}{T_s} \int_0^{T_s} \left| \sum_{k=1}^{\infty} \left[\frac{2V_g \cdot \sin(k \cdot D_m \cdot \pi)}{k\pi \cdot Z_{ink}} \cdot \cos(k \cdot \omega_o \cdot t - k \cdot D_m \cdot \pi - \theta_k) \right] \right| \cdot dt$$

$$V_o = R_L \cdot I_o = \frac{n \cdot R_L}{T_s} \int_0^{T_s} \left| \sum_{k=1}^{\infty} \left[\frac{2V_g \cdot \sin(k \cdot D_m \cdot \pi)}{k\pi \cdot Z_{ink}} \cdot \cos(k \cdot \omega_o \cdot t - k \cdot D_m \cdot \pi - \theta_k) \right] \right| \cdot dt$$

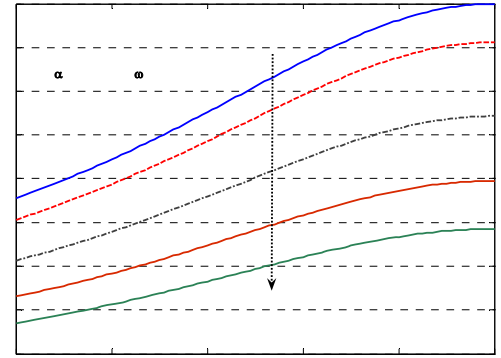


k^{th} harmonic equivalent circuit

Figure 5 k^{th} harmonic equivalent circuit



(a)



(b)

Figure 6 Voltage conversion ratio at different Q_o and ω

Therefore, the voltage conversion ratio (M) is

$$M = \frac{V_o}{V_g} = \frac{n \cdot R_L}{T_s} \int_0^{T_s} \left| \sum_{k=1}^{\infty} \left[\frac{2 \cdot \sin(k \cdot D_m \cdot \pi)}{k\pi \cdot Z_{ink}} \cdot \cos(k \cdot \omega_o \cdot t - k \cdot D_m \cdot \pi - \theta_k) \right] \right| \cdot dt$$

If only the fundamental component is used, the voltage dc conversion ratio (M) will be:

$$M = \frac{4n \cdot R_L \cdot \sin(D_m \cdot \pi)}{\pi^2 \cdot Z_{ink}} = \frac{\sin(D_m \cdot \pi)}{2n \cdot \left(1 + \alpha - \alpha \cdot \sin \frac{D\pi}{2} \right) \cdot \sqrt{1 + Q_o^2 \cdot \left(\omega - \frac{1}{\omega} \right)^2}}$$

If the feed-forward control is supposed to regulate the output voltage of the chopper in order to have:

$$V_g \cdot \sin(D_m \pi) = Const.$$

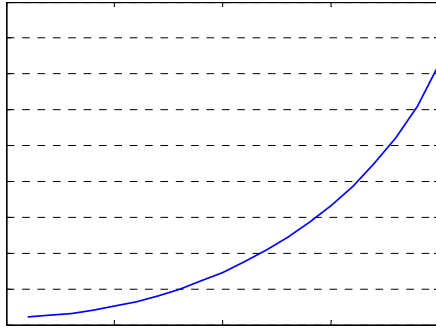


Figure 7. Effective duty cycle range

Then the modified voltage dc conversion ratio (M_s) is defined as:

$$M_s = \frac{V_o}{V_g \cdot \sin(D_m \pi)} = \frac{1}{2n \cdot (1 + \alpha - \alpha \cdot \sin \frac{D\pi}{2}) \cdot \sqrt{1 + Q_o^2 \cdot (\omega - \frac{1}{\omega})^2}}$$

Figure 6 shows the voltage conversion ratio M_s at different Q_o and ω . It is concluded that lower ω ($\omega > 1$) will help achieve good controls over the whole load range and higher ω may cause losing controls at light load. With lower ω , the effective duty cycle range will be narrower, that's, efficiency at reduced load could be improved. Similarly, higher Q_o at the full load will extend the effective duty cycle and may cause losing controls at light load. Therefore, to improve efficiency at reduced loads, reasonable low Q_o and ω is preferred.

For example, a design is assumed as follow: $V_g=12V$, $V_o=1V$, $V_d=0.8V$, $I_o=0\sim 20A$, $f_s=2.5MHz$. If choosing $Q_o=1.5$ and $\omega=1.1$, it can be determined that $n=5.5$, $L_s=130nH$, $C_s=38nF$.

Figure 7 shows the effective duty cycle range versus load current. The effective duty cycle is ranging from 0.79 to 0.92 to regulate the output voltage at the load range from 5% to 100%. That's, the body diodes of the synchronous MOSFETs conduct only 20% the switching period at light load (5%). Moreover, the body diodes always conduct only at the beginning and at the end of each half period when it has low current. Hence, efficiency impairment by this secondary-side regulation mode is minimized.

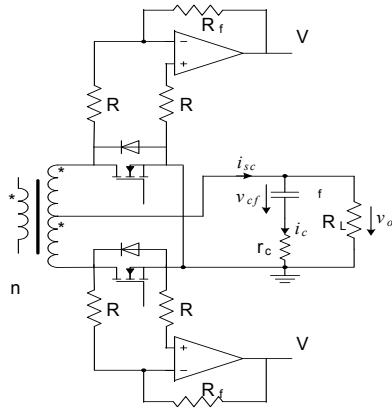


Figure 8. Cross-conduction detection Circuits

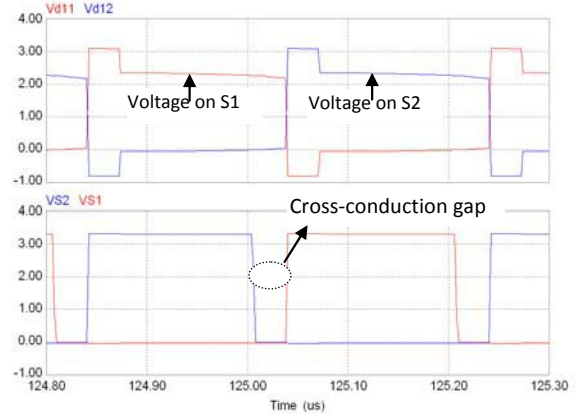


Figure 9. Cross-conduction operation waveforms

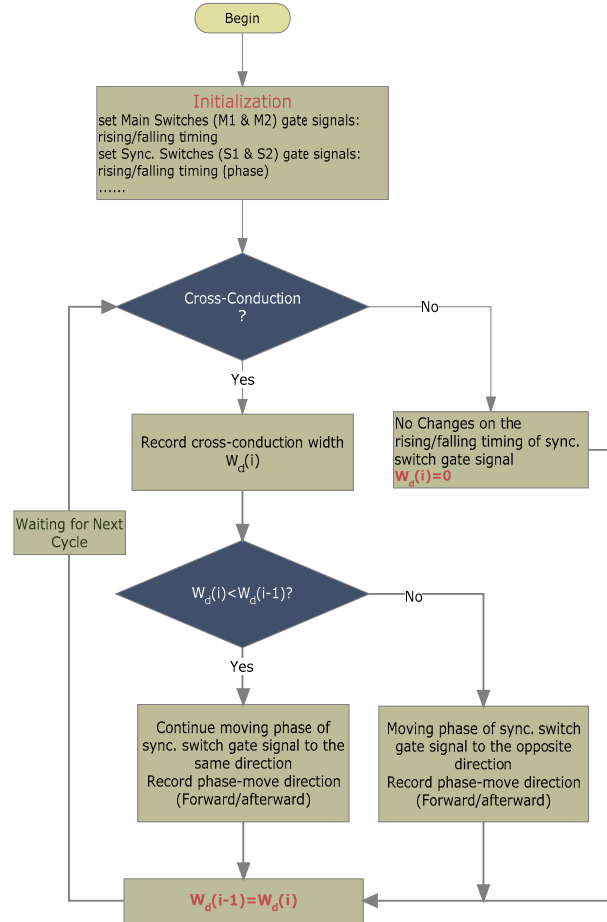


Figure 10. Basic flow chart of the adaptive control

IV. CURRENT SENSORLESS ADAPTIVE DIGITAL CONTROL

Since this power converter has a current drive rectifier and utilizes the secondary side control, the control timing is critical to successful control. Current sensorless adaptive digital control method is proposed. Two windowed comparators, as shown in Figure 8, are used to monitor the polarity of the voltage on the synchronous rectifier MOSFETs, which is related to the current through them. But there are always circuit delay and parasitic inductor in series with MOSFETs, which will shift the voltage phase and may cause cross-conduction.

Therefore, these two comparators together also work as cross-conduction detection circuits, whose typical waveforms are shown in Figure 9. When cross-conduction occurs, the logic 'NOR' of the signals V_{s1} and V_{s2} will have a positive pulse with certain width, which is consistent with the cross-conduction duration. Hence, an adaptive control scheme can be implemented to find the zero-current-crossing point to avoid cross-conduction (no positive pulse on the logic 'NOR' of the signals V_{s1} and V_{s2}). Figure 10 shows the basic flow chart of the adaptive control.

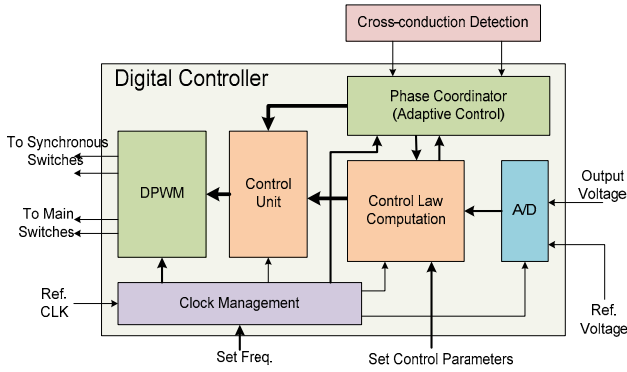
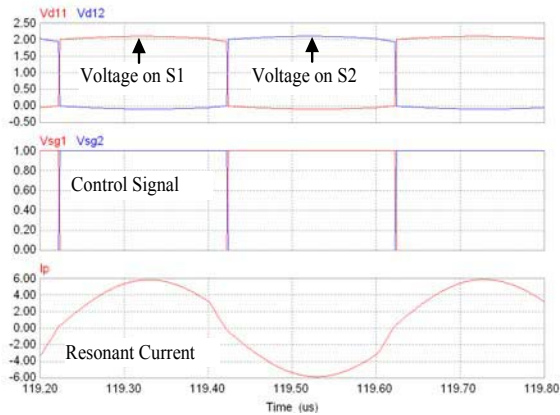
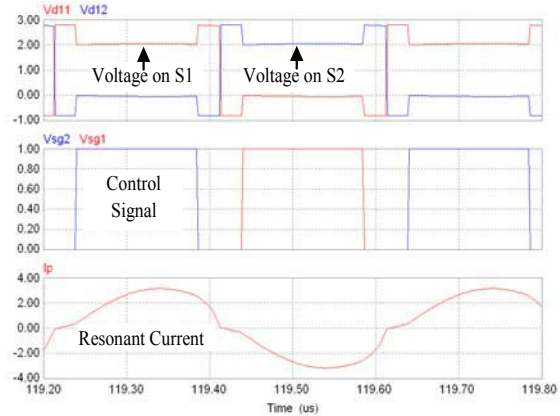


Figure 11. Architecture of digital controller



(a) $I_o=20A$ (Full Load)



(b) $I_o=10A$ (Half Load)

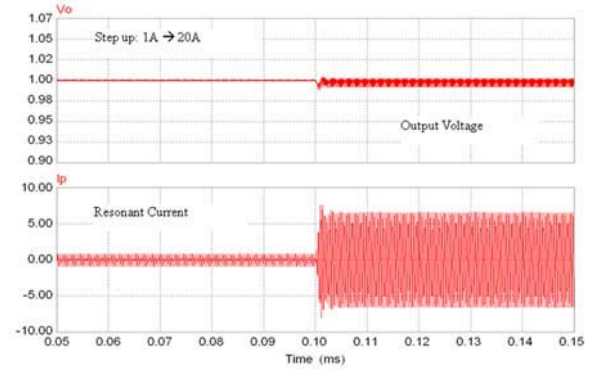
Figure 12. Steady state operation waveforms

V. SIMULATION VERIFICATION

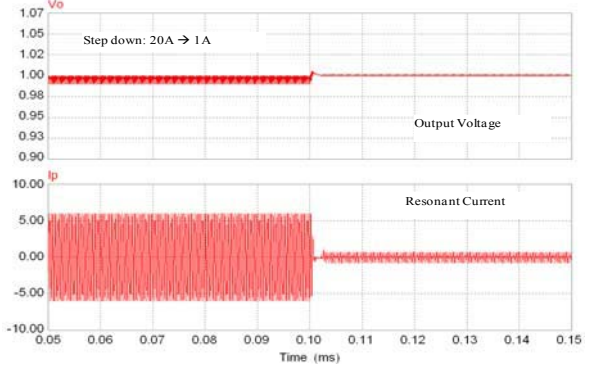
To verify the performance of this proposed converter, simulation is performed in the co-simulation environment involved MATLAB, PSIM and ModelSim. Figure 11 shows the digital controller, which consists of control law computation unit, control unit, phase coordinator (adaptive control unit), digital PWM (DPWM), clock management and analog-to-digital converter (A/D). The digital controller except the A/D converter is implemented by VHDL language in ModelSim. The output voltage was sampled at 20MHz by the A/D converter (5 effective bits). Power stage was constructed in PSIM with following circuit parameters: $V_g=12V$, $V_o=1V$, $V_d=0.8V$, $I_o=0\sim 20A$, $f_s=2.5MHz$, $n=5.5$, $L_s=130nH$, and $C_s=38nF$.

Figure 12 shows the steady state operations of the power converter at full load and at half load, which verifies the theoretical analysis in Section II & III.

Figure 13 shows the load current step up/down response ($5 \times 100\mu F / 1.2m\Omega$ filtering capacitors). The overshoot/undershoot voltage is less than 5mV under 19A load step-down/up. The dynamic performance of the proposed power converter is excellent and very fast transient speed exhibits, which verifies the concept.



(a) Load Step-up



(b) Load Step-down

Figure 13. Load current step-up/down response

VI. CONCLUSION

Future microprocessors need large current with large current slew rate at lower supply voltage. The continuously-decreasing supplied voltage for the processor raises serious challenge for voltage regulation. The allowed voltage regulation window becomes even narrower for effective logic identification and the total voltage tolerance will be much tighter. This makes it

more difficult for VRMs to maintain an accurate voltage regulation.

The inductor in the output filter of today's VRMs limits the current transient speed. Hence, the series resonant converter with capacitor type filter is introduced in this paper to overcome this limitation as a good candidate for VRM topology. The lack of the inductor in its output filter makes it have very quick dynamic response. The secondary-side control is proposed to further improve current transient speed. The AC equivalent resistance then the output voltage can be regulated by the duty cycle of the rectifier switches due to the difference between diode forward voltage (V_d) and synchronous MOSFET on-state voltage. Carefully designing characteristics of the series resonant tank as well as the controlled AC equivalent resistance will achieve good performance while keeping high efficiency over full load range. An adaptive control scheme is proposed to control the current-type synchronous MOSFETs, which eliminates the current sensor in the power path and can be extended to drive all current-type synchronous rectifier MOSFETs. Theoretical analysis and simulation results verify the proposed concept.

REFERENCES

- [1] P.P. Gelsinger, "Microprocessors for the new millennium: Challenges, opportunities, and new frontiers," in Proc. IEEE ISSCC, Pp. 22-25, 2001.
- [2] Ed Stanford, "Power technology roadmap for microprocessor voltage regulators," Presentation at PSMA, Feb. 2003.
- [3] B. Pohlman, "Overcoming the Barriers to 10GHz Processors," Presentation at Microprocessor Forum Keynote, Oct. 16, 2001.
- [4] K. Yao, Y. Meng and F.C. Lee, "Control bandwidth and transient response of buck converters," in Proc. IEEE PESC, Pp. 137-142, 2002.
- [5] P. Jain, "Performance comparison of pulse width modulation resonant mode DC/DC converter for space applications", IEEE IAS conference record, Pp. 1106-1114, 1989.
- [6] P. Jain, A. Martin, et al, "Asymmetrical PWM resonant DC/DC converter topologies, IEEE Transaction on Power Electronics", Vol.11, No.3, Pp. 413-422, 1996.
- [7] S. Mangat, M. Qiu, P. Jain, et al, "A Modified Asymmetric Pulse-Width-Modulated Resonant DC/DC Converter Topology", IEEE Transaction on Power Electronics, Vol. 19, No.1, Jan. 2004
- [8] S. Mangat, Y. Xi, P. Jain, "A modified asymmetrical pulse-width-modulated resonant DC/DC converter topology", IEEE APEC conference, Pp. 662-668, 1998.
- [9] P. Jain, D. Bannard, et al, "A phase-shift modulated double tuned resonant DC/DC converter analysis and experimental results", IEEE conference record, Pp. 90 -97, 1992.
- [10] P. Jain, H. Soin, et al, "Constant frequency resonant DC/DC converters with zero switching losses, IEEE Trans. on Aerospace and Electronic System", Vol. 30, No.2, Pp. 534 -543, April 1994.
- [11] Steigerwald, R.L., "A comparison of half-bridge resonant converter topologies", Power Electronics, IEEE Transactions on Power Electronics, Vol.3, No.2, Pp.174-182, April 1988.