UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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DELTA ELECTRONICS, INC.

Petitioner

v.

VICOR CORPORATION

Patent Owner

IPR2024-00187
Patent No. 9,166,481

PATENT OWNER PRELIMINARY RESPONSE

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Exhibit No.	Description
2001	Declaration of Prof. Juan Rivas-Davila.
2002	Morrison, D., "Distributed Power Moves To Intermediate Voltage Bus", *Electronic Design*, Sept. 16, 2002, pp. 55-61.
2003	Ericsson, Design Note 023, "Selection of Architecture for Systems using Bus Converters and POL Converters", May 2005.
2004	U.S. Pat. No. 10,199,950.
2005	U.S. Pat. No. 8,014,175.
2006	U.S. Pat. No. 6,344,979.
2007	U.S. Pat. No. 7,599,198.
2008	Not submitted.
2009	Not submitted.
2010	Not submitted.
2011	U.S. Pat. No. 7,184,280.
2012	Huang, H, "Designing an LLC Resonant Half-Bridge Power Converter", 2010 Texas Instruments Power Supply Design Seminar.
2013	Not submitted.
2014	Not submitted.
2015	Not submitted.
2016	Not submitted.
2017	Miftakhutdinov, Rais. "Improving system efficiency with a new intermediate-bus architecture." Texas Instruments Inc. Seminar. Vol. 2. 2009.

2018	Not submitted.
2019	Not submitted.
2020	Not submitted.
2021	Intel® Xeon® Processor E5-2400 Product Family Datasheet - Volume One, May 2012
2022	Not submitted.
2023	Salato, “Re-Architecting 48V Power Systems with a Novel Non-Isolated Bus Converter”, Vicor White Paper, 2018.
2024	Vicor Data Sheet for IBC Module IB0xxQ096T70xx-xx
2025	Public Complaint, “In the Matter of Certain Power Converter Modules and Computing Systems Containing the Same”, Investigation No. 337-TA-1370 (USITC July 12, 2023).
2026	Vicor Data Sheet for NBM™ Bus Converter NBM2317S60D1565T0R
2027	Vicor's V-I Chip Bus Converter Module Wins Electronic Products Product of the Year Award, Dec. 15, 2003.
2028	Not submitted.
2029	Not submitted.
2030	Declaration of Dr. Patrizio Vinciarelli
2031	Delta Non-isolated Bus Module Claim Charts
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Patent Owner Vicor Corporation ("Vicor") hereby submits its preliminary response to the Petition for *inter partes* review seeking to challenge claims 1, 22, and 31-35 of U.S. Patent No. 9,166,481 to Vinciarelli, *et al.* ("the '481 patent").

The Petition fails to satisfy the Petitioner's burden[1] for multiple reasons.

First, the art is complex, and *none* of the Petition's seven obviousness Grounds asserts that a Person Having Ordinary Skill in the Art ("PHOSITA") would have had a reasonable expectation of success in modifying the prior art. The failure to even allege—much less substantiate—this basic requirement of an obviousness case warrants denial of Institution.

Second, none of the prior art combinations teaches or renders obvious all of the elements of claim 1 (the only independent claim). Most of the Grounds fail to demonstrate the obviousness of three or four elements, relying on mistaken interpretations of the operation of prior-art converters, dubious inherency arguments, or perfunctory, single-sentence obviousness arguments that do not engage meaningfully with the complexities of the art.

Third, the Petition also fails to engage meaningfully with secondary

[1] *See* 35 U.S.C. § 316(e)("In an inter partes review ..., the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.")

considerations, even though these were known to the Petitioner prior to filing.

The Petition should therefore be denied.

I. BACKGROUND

A. Technology Background

The subject matter of the patent can be a little bit difficult to understand. To aid in understanding the technology background, the attached declaration of Professor Rivas-Davila (Ex. 2001) reviews basic concepts relevant to the '481 patent in ¶¶23-57. It may be useful to review this background explanation before reading the remainder of this Preliminary Response. Dr. Rivas-Davila is a Professor in the Electrical Engineering Department at Stanford University. (Ex. 2001, ¶4). He focuses his research on the design of power converters. (Ex. 2001, ¶4). Near the relevant timeframe, he was the Lead Power Electronics Engineer for General Electric's Global Research Center. (Ex. 2001, ¶7).

B. What is this Dispute About?

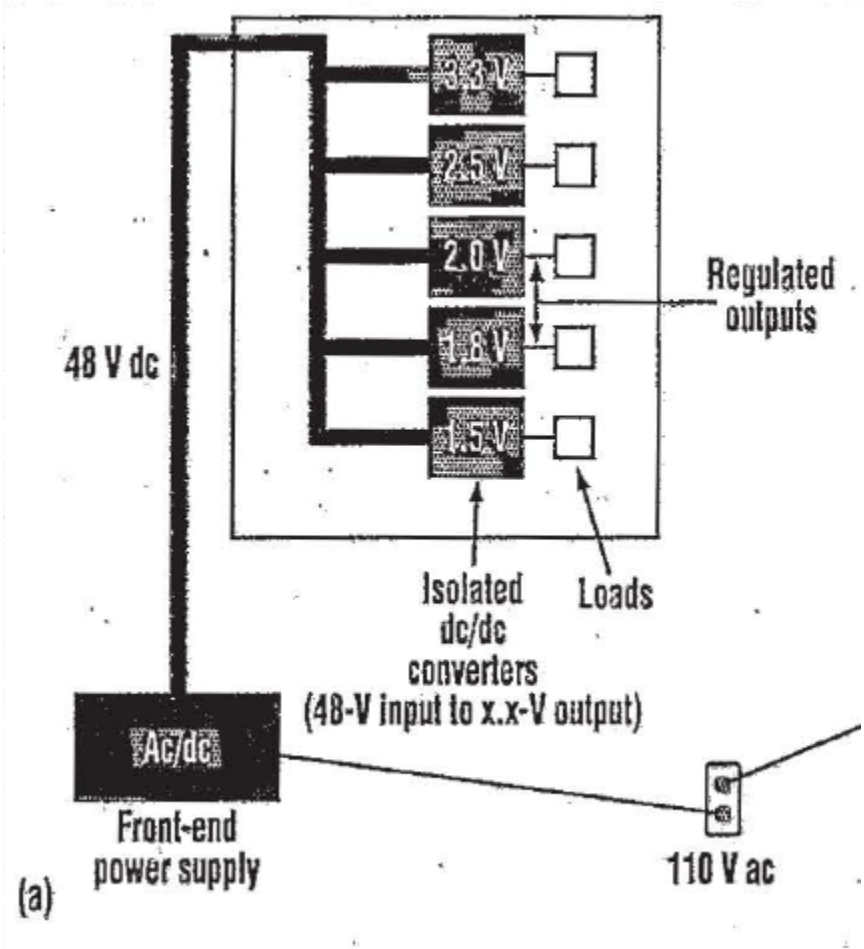
This is a dispute between competitors selling high-efficiency, high-power-density power converters. Vicor, based in Andover, Massachusetts, is a technology leader in the field of power module design and manufacturing. (Ex. 2030, ¶¶4-6). Petitioner Delta is a competitor in that field. Vicor has filed a complaint in the United States International Trade Commission for illegal importation of goods that infringe the '481 patent (at-issue here) along with two other patents. (Ex. 2025). Delta responded with three petitions for *inter partes* review, including this one.

The accused products at the ITC relate to high-efficiency, high-density power converter modules used in data centers. (Ex. 2030, ¶7). As discussed in Professor Rivas-Davila's declaration, data centers can have thousands of servers. (Ex. 2001, ¶58)(Ex. 2030, ¶7). The servers are individual computers in racks that contain a motherboard. (Ex. 2001, ¶58). The motherboard supports the principal components of the server, including one or more processors and power modules, including those of the type at-issue here. (Ex. 2001, ¶58).

Providing power to a processor in a data center (or their technological progenitors: telecom central offices) is a complex task. (Ex. 2001, ¶59). Power needs to be supplied from power lines (providing high-voltage AC power) and ultimately converted to low-voltage (*e.g.* 0.7 V) DC power. (Ex. 2001, ¶59). The power delivered to a processor typically needs to be precisely regulated. (Ex. 2001, ¶59). For example, voltage rails supplied to Intel CPUs in the relevant timeframe needed to be regulated to a specific voltage level, with variations in voltage being limited to +/- 0.015 V. (Ex. 2001, ¶59)(Ex. 2021, p. 152, and chart on pp. 155-156)(Ex. 2010, p. 14).

In a telecom central office, power was converted from utility power lines down to a lower voltage using a transformer, and then turned into DC power ("rectified") using a so-called "front-end converter" or "rectifier". (Ex. 2001, ¶60). Power from the rectifier, in the relevant timeframe, was typically distributed at a

negative 48 V DC to individual telecom boards. (Ex. 2001, ¶60). Power distributed on the negative 48 V bus then needed to be converted to low, positive voltages within the equipment. (Ex. 2001, ¶60). The equipment would typically require a multiplicity of DC voltage levels for different components. (Ex. 2001, ¶60). For example, a fan might operate at 8 V DC, while a processor might operate at 1 V DC, while other components operate with 5 V or 3.3 V DC. (Ex. 2001, ¶60). This is shown in the following diagram (Fig. 1(a) from Morrison 2002), where the boxes showing 3.3 V, 2.5 V, 2.0 V, etc., represent different regulated voltage levels delivered to loads:



(Ex. 2002, Fig. 1)(Ex. 2001, ¶60). The "48 V dc" bus voltage was typically distributed as a negative voltage. (Ex. 2030, ¶10)(Ex. 2003, p. 2, Fig. 1).

Converting the negative 48 V DC power to the various levels needed in a system required DC/DC converters. (Ex. 2001, ¶61). A DC/DC converter was a module that could convert power from one DC voltage level to another. (Ex. 2001, ¶61). A DC/DC converter typically included three functions: isolation, voltage transformation, and regulation. (Ex. 2001, ¶61). "Isolation" meant that the input and the output were "galvanically" isolated from each other, *i.e.*, lacking a direct, wired connection that might compromise system safety and noise immunity. (Ex. 2001, ¶61). Isolation was usually provided by a transformer, which *magnetically* couples its primary and secondary windings to avoid direct electrical contact. (Ex. 2001, ¶61). "Voltage transformation" meant changing the voltage level at the same power level. (Ex. 2001, ¶61). Because power is equal to voltage times current, a change in voltage typically meant an inverse change in current. (Ex. 2001, ¶61). "Regulation" meant controlling the output voltage to a precise level, as the input voltage varied. (Ex. 2001, ¶61). In the 1990s, it was typical to use one DC/DC converter for each different voltage level required by a system on a board, as shown in the Figure from Morrison, above. (Ex. 2001, ¶61).

DC/DC converters were not 100% efficient. (Ex. 2001, ¶62). DC/DC converters in the 1990s achieved 80-90% typical efficiency. (Ex. 2001, ¶62). The

remaining 10-20% was lost in waste heat. (Ex. 2001, ¶62). Waste heat is a problem: it increases input power and the heat itself needs to be removed. (Ex. 2001, ¶62). Currently, the United States uses about 2% of its total electricity in data centers, and nearly 33% of that goes to thermal management. (Ex. 2001, ¶62). Thermal management is required to keep equipment within an acceptable operating temperature range, typically thought to be below 85º C. (Ex. 2001, ¶62). Because of thermal management challenges, data centers tend to be sensitive to the efficiency of their power-supply systems. (Ex. 2001, ¶62). For example, the difference between 98% efficiency and 96% efficiency results in the lower-efficiency converter causing *twice* the waste heat (4% versus 2% inefficiency). (Ex. 2001, ¶62).

The solution of the 1990s—using one DC/DC converter for each DC voltage required in a system—worked for a while, but industry trends soon made it impractical. (Ex. 2001, ¶63). Specifically, system designers kept adding functionalities and components on circuit boards, and the components required different voltage levels. (Ex. 2001, ¶63). Additional components took up more space on the system board, which required more DC/DC converters, which in turn took up more space, cost more, and generated more waste heat. (Ex. 2001, ¶63). System designers could not easily increase the size of system boards, because the equipment had a standard size on which other vendors depended. (Ex. 2001, ¶63).

As a result, in the early 2000s, system designers revived an older power-

supply architecture known as the "Intermediate Bus Architecture" or "IBA". (Ex. 2001, ¶64). IBA relied on the ability to separate the isolation and regulation functions of a DC/DC converter. (Ex. 2001, ¶64). An upstream converter could provide isolation and voltage step-down without regulation, distributing power to a multiplicity of converters providing regulation without additional isolation. (Ex. 2001, ¶64). The isolated, unregulated converter was called a "bus converter", and the downstream regulators were often called "POLs", or Point-of-Load converters. (Ex. 2001, ¶64). In a typical IBA system, the bus converter would convert input power at negative 48 V DC to positive 12 V DC. (Ex. 2001, ¶64). The 12 V power was typically not regulated (or partially regulated), meaning that its output would vary in proportion to its input voltage. (Ex. 2001, ¶64). And the input voltages in typical telecom / data center applications varied considerably. (Ex. 2001, ¶64). For example, a standard input voltage range for bus converters in data centers was from 40 V to 60 V. (Ex. 2001, ¶64)(Ex. 2026, p. 1). This implies that the output of the bus converter might be centered at 12 V, but would vary from 10 V to 15 V. (Ex. 2001, ¶64).

The bus converter output voltage would be carried by an "intermediate bus" to various loads, like processor chips. (Ex. 2001, ¶65). Near these loads, system designers placed POLs that would perform a final down-conversion (say from 12 V DC to 1 V DC), while regulating the output voltage. (Ex. 2001, ¶65). Such an IBA

system is shown here:

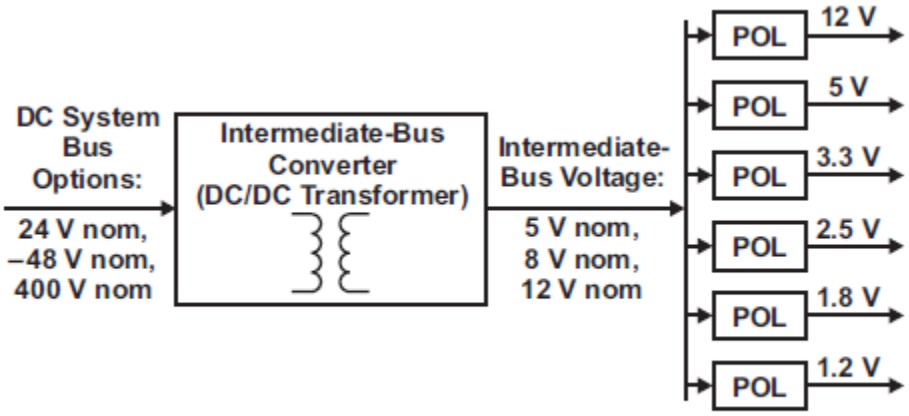


Fig. 4. Example of IBA.

(Ex. 2017, Fig. 4)(Ex. 2001, ¶¶65-66).

Patent Owner Vicor improved upon the Intermediate Bus Architecture in 2003 with its Bus Converter Module (BCM). (Ex. 2030, ¶¶15-17). The Vicor Bus Converter Module used a converter topology called a Sine Amplitude Converter (SAC). (Ex. 2030, ¶15). The Sine Amplitude Converter is the starting point for the '481 patent, and is described in Vicor's prior U.S. Pat. No. 6,984,695, which is incorporated by reference into the '481 patent (Ex. 1001, 1:13-20), and was submitted with the Petition as Ex. 1009.

A Sine Amplitude Converter is a member of a class of fixed-frequency, fixed-ratio, resonant converters. The class of Sine Amplitude Converters is distinct from the class of variable frequency, variable conversion ratio LLC converters. Vicor used its SAC topology to achieve high efficiency, nearly 97%. (Ex. 2027). To achieve high efficiency, Sine Amplitude Converters operate at their resonant

frequency, without variable duty cycle or pulse-width modulation. (Ex. 2030, ¶15)(Ex. 2023, p. 2). This sacrificed the ability to regulate the converter's output voltage, but enabled a SAC to operate with zero-voltage and zero-current switching of its primary and secondary power switches, which led to efficiency gains. (Ex. 2030, ¶15)(Ex. 2023, p. 2). Vicor was thus able to operate its Bus Converter Modules at frequencies well above 1 MHz, nearly 10X higher than competitive converters, enabling a commensurate increase in its power density (power processed divided by volume). (Ex. 2030, ¶15)(Ex. 2023, p. 2). The Vicor BCM won the EDN 2003 Innovation of the Year Award. (Ex. 2030, ¶15)(Ex. 2027).

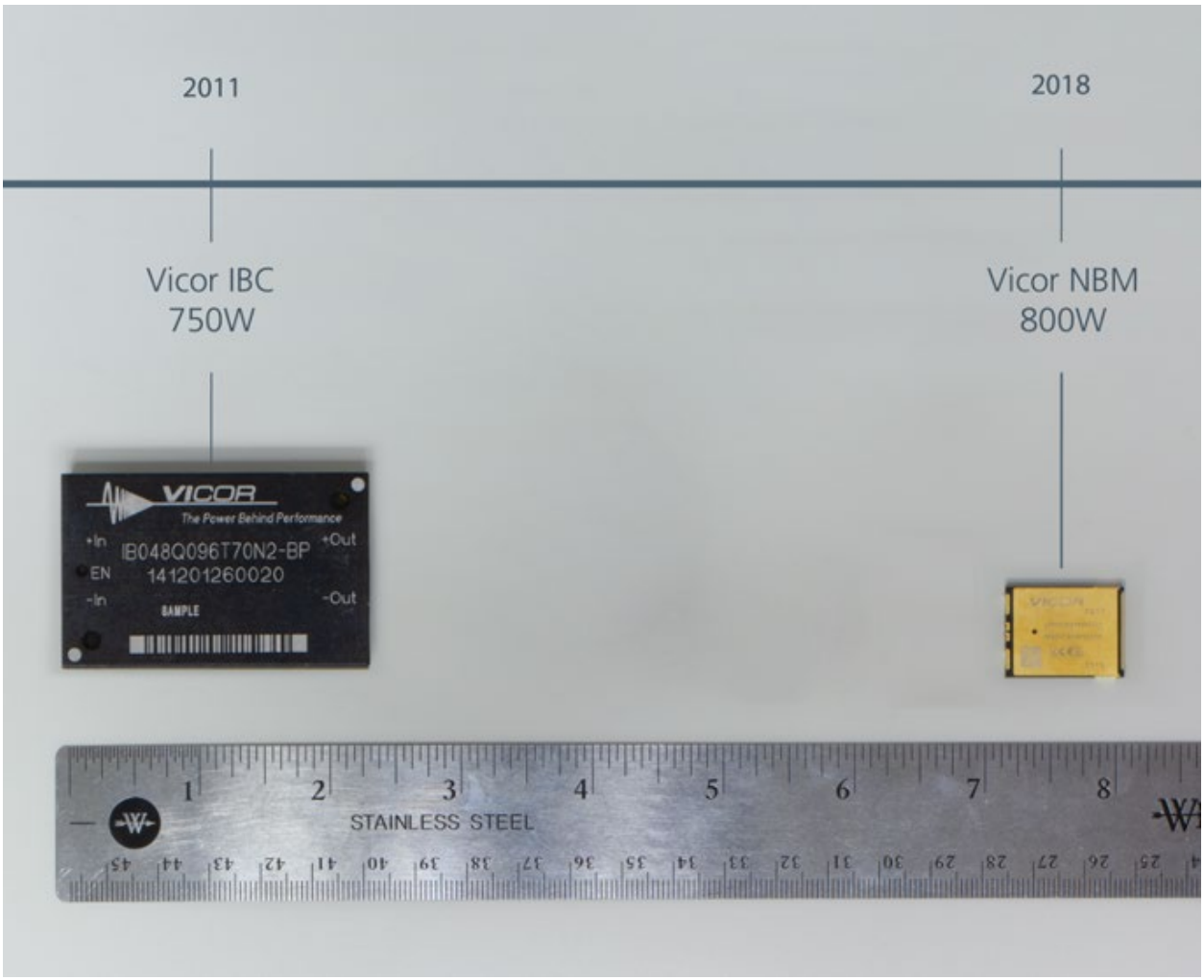
Demand for higher power density did not end there, however. In the past decade, the machine-learning revolution has driven the use of higher-power graphics processing units (GPUs) in data centers. (Ex. 2001, ¶67). Such GPUs demand more current (e.g., one thousand Amperes), at a lower voltage (below 1 V). (Ex. 2001, ¶67). Furthermore, to save power, modern GPUs can shift quickly into low-power modes and back again, creating extreme changes in loads (so-called "fast transients") that the power system must cope with. (Ex. 2001, ¶67). At the same time, there is continued pressure for power supply components to use less board space. (Ex. 2001, ¶67).

Nearly ten years ago, Vicor patented a series of innovations that drove a major step-up in the efficiency and power density of its bus converters, including the

innovations claimed in the ’481 patent at-issue here, as well as U.S. Pats. Nos. 10,199,950 and 9,516,761.[2] (Ex. 2030, ¶¶18, 32). These patented features, applied to the class of Sine Amplitude Converter topologies (Ex. 1001, 4:41-49), increase efficiency to approximately 98%—considerably higher than the efficiency of prior generation Sine Amplitude Converters. (Ex. 2030, ¶32)(Ex. 2023, p. 4). While an increase in efficiency from 97% to 98% may be perceived as small, it represents a one-third reduction in wasted heat. (Ex. 2001, ¶62). Vicor was thus able to decrease the size of the bus converter module and increase its power density accordingly. (Ex. 2030, ¶¶32-35)(Ex. 2023, p. 6).

Using these innovations (including the ’481 patent at-issue here), Vicor developed “NBM” (non-isolated bus module) products. The advance in performance enabled by three patents (the ’481, ’950, and ’761 patents) was considerable, as evidenced in the side-by-side comparison below. The image below shows the footprint of a prior Vicor bus converter used as an isolated bus converter in IBA applications before the invention of the’950, ’481 and ’761 patents (left side), and of a Vicor NBM (NBM2317) using the inventions of the ’950, ’481 and ’761 patents:

[2] These patents are the subject of co-pending IPR2024-00134 and IPR2024-00227, respectively.



(Ex. 2030, ¶34-34). The difference in footprint is apparent. But what is not apparent is that Vicor was also able to reduce bus converter thickness while increasing power capability from 750 W to 800 W. (Ex. 2030, ¶32). In the aggregate, the inventions of the '950, '481, and '761 patents enabled a tenfold increase in power density (power per unit volume). (Ex. 2030, ¶32).

Vicor's NBM products were developed contrary to the conventional wisdom, were initially met with skepticism, but later achieved considerable commercial success. *See* §III.J, below (beginning on page 88). Following the introduction of

Vicor's NBM, Delta introduced a competitive module in the same footprint incorporating all of the inventions of the '950, '481, and '761 patents, and imported these modules into the US. (Ex. 2030, ¶33)(Ex. 2031). Vicor then initiated a complaint at the United States International Trade Commission (Ex. 2025), and Delta filed these petitions in response.

C. The '481 Patent

The '481 patent at-issue in this proceeding contributed to the success of Vicor's NBM products by increasing their efficiency and power density. (Ex. 2030, ¶¶40, 23-28). To accomplish this, the '481 patent disclosed a new SAC controller to drive the gates of primary and secondary switches at the converter's resonant frequency and turn these switches ON and OFF essentially without loss, at zero current and zero voltage. (Ex. 2001, ¶68).

The efficiency increase resulted from an improved method to control the switching of the SAC's primary and secondary switches, MOSFETs. (Ex. 2001, ¶68). Lossless MOSFET switching is enabled by turning these devices ON and OFF at zero current and zero voltage. MOSFETs dissipate power while switching from ON to OFF or *vice versa*. (Ex. 2001, ¶68)(Ex. 2030, ¶¶23, 28). When a MOSFET is ON, its resistance is very low, and current flowing through its channel will produce very little resistive heating. (Ex. 2001, ¶¶48-49). When a MOSFET is fully OFF, its resistance is very high, so that essentially no current can flow through its channel,

and thus resistive losses will also be very low. (Ex. 2001, ¶¶48-49). When a MOSFET is transitioning between ON and OFF, however, its channel resistance is changing from very low to very high or *vice versa*, meaning that current can flow through it *and* the resistance may be substantial. (Ex. 2001, ¶¶48-49). During switching time intervals, MOSFETs may dissipate a considerable amount of power. (Ex. 2001, ¶¶48-49). To minimize these conduction losses, and switching losses caused by discharging the MOSFET's output capacitance, Vicor's Sine Amplitude Converters rely on the combination of Zero Current Switching ("ZCS") and Zero Voltage Switching ("ZVS"): primary and secondary switches are turned ON and OFF at times when MOSFET switches have essentially no voltage across them, and no current (or no resonant current for primary side switches) flowing through them. (Ex. 2001, ¶49).

Vicor's prior generation SAC controller relied, however, on analog control circuitry to effect switching transitions. (Ex. 2030, ¶24). This was thought to be necessary for two reasons. (Ex. 2030, ¶24). First, since the converter's resonant frequency depends upon the value of certain power train components (Ex. 2001, ¶58), component variabilities would cause unintentional variations in resonant frequency from device to device and across different production runs. (Ex. 2030, ¶24). Furthermore, the resonant frequency might vary based on operating conditions, such as temperature. (Ex. 2030, ¶24). If the switching frequency did not

match the resonant frequency within acceptable tolerances, the MOSFET switches would lose ZCS and ZVS, and lose efficiency. (Ex. 2030, ¶24). For this reason, it was thought to be necessary to provide a "closed-loop" feedback mechanism, where circuitry in the converter sensed the phase of resonant current to achieve ZCS and ZVS by automatically varying the switching frequency in response to operating conditions. (Ex. 1009, 21:52-22:8)(Ex. 2030, ¶24). Second, the action of turning MOSFET switches ON and OFF required charging and discharging the gate capacitances of the MOSFETs. (Ex. 2030, ¶25). Analog control circuitry could recycle this gate-charge, to increase efficiency. (Ex. 2030, ¶25).

The '481 patent, however, took a fundamentally different approach. Rather than sensing the phase of resonant current with "closed-loop" control to automatically turn switches ON and OFF by adjusting the SAC's operating period and frequency, the invention of the '481 patent *imposed* a standard SAC operating period and frequency by using a digital controller and clock to set a series of independent switching "events". (Ex. 2030, ¶23). Remarkably, this "open loop" control method provided benefits that more than compensated for the benefits of prior art closed loop control and gate charge recycling. (Ex. 2030, ¶28). Specifically, the inability to compensate for component variabilities and recapture gate charge energy was overcome by the speed with which the digital SAC controller could turn MOSFETs ON and OFF, with ZCS, ZVS, nearly zero dead time and

nearly 100% duty cycle. (Ex. 2030, ¶28). A preset cadence of switching events allowed more consistent and finer timing resolution than with traditional closed-loop control, enabling SACs to operate at a higher frequency, with higher power density while still achieving ZVS and ZCS. (Ex. 2030, ¶28). And the digital SAC controller took up less area than needed by prior generation analog SAC controllers and related sensors. (Ex. 2030, ¶28).

These advantages arise from the entirety of claim 1 of the '481 patent, but in particular from those limitations requiring standard timing for primary and secondary MOSFETs (*e.g.* "generating timing control signals for each of a plurality of events based upon the clock signals in a (A) standard converter operating cycle, having a standard operating period and frequency" and "wherein the oscillator frequency is preset"), the limitations requiring zero-voltage and zero-current switching, and the limitation requiring independent control signals ("the timing of the timing control signals for one or more selected events may be set independently of other timing control signals and events."). (Ex. 2030, ¶28).

II. CLAIM CONSTRUCTION

A. The Preamble of Claim 1 is Limiting

The Board should find that the preamble of claim 1 (limitation 1[a]) is limiting. This limitation reads:

> "A method of synchronously operating a power converter in a series of converter operating cycles the converter having at least one

> primary switch to drive a resonant power train and at least one secondary switch, the resonant power train including a transformer and having a characteristic resonant frequency and period, the method comprising:"

The Petition takes no position on this issue, but qualifies its claim-mapping sections relating to limitation 1[a] with the introductory clause "[t]o the extent the preamble is limiting…."

The preamble *is* limiting. This is at least because the elements recited in the preamble serve as the antecedent basis for later claim terms. *See In re Fought*, 941 F.3d 1175, 1178 (Fed. Cir. 2019)("We have repeatedly held a preamble limiting when it serves as antecedent basis for a term appearing in the body of a claim."). For example, the claim in the preamble recites "at least one primary switch" and "at least one secondary switch". Later, in limitation 1[d], the claim recites "the at least one primary switch", and in limitation 1[e] recites "the at least one secondary switch".

Furthermore, the preamble "recites essential structure or steps" and "is `necessary to give life, meaning, and vitality' to the claim." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002). Specifically, the preamble provides the essential structure within which the method steps are carried out. For example, the preamble recites "the resonant power train including a transformer". The transformer, in turn, defines the boundary between the "primary"

and "secondary" sides referred to in claim limitations 1[d] and 1[e], without which these terms would be meaningless. (Ex. 2001, ¶120). *See Griffin v. Bertina*, 285 F.3d 1029, 1033 (Fed. Cir. 2002)("Consideration of the preamble gives meaning and purpose to the manipulative steps in this case.").

The Board should thus construe the preamble of claim 1 to be limiting.

III. THE BOARD SHOULD DENY THE PETITION

A. The Petition Provides no Evidence that a PHOSITA Would Have Had a Reasonable Expectation of Success for any Ground.

All Grounds in the Petition fail to carry the Petitioner's burden, because the Petition fails even to assert—much less provide evidence for—the existence of a reasonable expectation of success. (Ex. 2001, ¶71). Indeed, the words "reasonable expectation" do not appear in the Petition, and appear in Dr. Hopkins' declaration only in his background discussion of patent law. (Ex. 1003, ¶¶24, 25). The failure of the Petition to even discuss a basic requirement of an obviousness case is sufficient to find that Grounds I-VII do not meet the statutory standard for institution. *See Medtronic, Inc. v. Teleflex Innovations S.A.R.L.*, 70 F.4th 1331, 1345 (Fed. Cir. 2023)("absence of a reasonable expectation of success defeats obviousness")*; Eli Lilly & Co. v. Teva Pharm. Int'l GmbH*, 8 F.4th 1331, 1348 (Fed. Cir. 2021)("it was, at all times, Lilly's [Petitioner's] burden to show that the claims would have been obvious, including that a skilled artisan would have had a reasonable expectation of success in achieving the claimed invention"); *Apotex Inc. v. Wyeth LLC*, IPR2014-

00115, Paper 94, slip op. at 11 (Apr. 20, 2015)("A party that petitions the Board for a determination of obviousness must show that 'a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.'")(*citing Procter & Gamble Co. v. Teva Pharms. USA, Inc.*, 566 F.3d 989, 994 (Fed. Cir. 2009)).

B. Ground I (McDonald in view of TI UCD3138) Does Not Meet the Petitioner's Burden

Ground I (McDonald in view of TI UCD3138) fails to carry the Petitioner's burden because the combination does not meet at least claim limitations 1[c], 1[d], 1[e], and 1[f].

1. Limitation 1[c] — "…standard converter operating cycle, having a standard operating period and frequency…"

The combination does not teach a "standard converter operating cycle, having a standard operating period and frequency" as required by limitation 1[c]. Instead, McDonald's converter design *varies* the frequency to control (or "regulate") the output voltage. (Ex. 1005, p. 3, right column, top)(Ex. 2001, ¶73). Because McDonald's circuit varies its operating frequency, it has neither a standard operating

period nor a standard frequency as required by claim limitation 1[c].[3]

McDonald explains that for its converter "[t]he **output voltage is commonly controlled** by using a fixed duty cycle (e.g., 50 percent) and a **variable frequency**." (Ex. 1005, p. 3, right column, top)(Emphasis added)(Ex. 2001, ¶74). McDonald explains this in more detail, noting that when the input voltage to the converter varies, the converter changes its operating frequency to make sure the output voltage stays the same. (Ex. 1005, p. 5)(*e.g.* "The **input voltage is now reduced** so that **the system control effort changes the frequency** to something below the resonant frequency….")(Emphasis added)(Ex. 1005, p. 5-8 ("You can address this by **constraining the operating frequency to a range where the curves are monotonic**, as shown by the gray box.")(Ex. 2001, ¶74).

This aspect of McDonald is shown in Figure 25 of McDonald, which is relied on by Delta on page 31 of the Petition, and which itself is entitled "Frequency Modulation". (Ex. 1005, Fig. 25)(Ex. 2001, ¶75). This figure is reproduced again here, with highlighting added.

[3] Note that frequency and period are mathematically dependent parameters: period = 1/frequency. (Ex. 2001, ¶73).

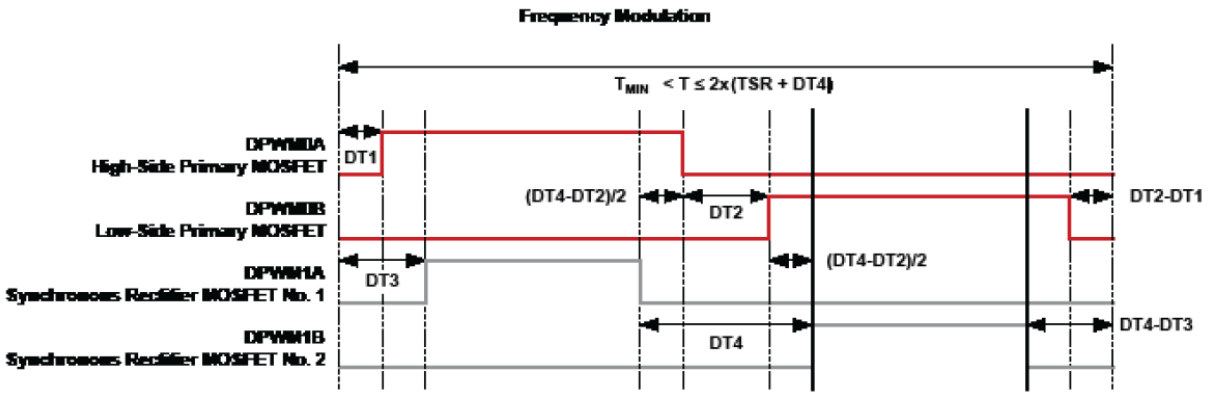


Figure 25 – Frequency modulation.

(Ex. 1005, Fig. 25)(Ex. 2001, ¶75). This figure is not only entitled "Frequency Modulation", but shows at the top how the switching period T can vary within a range. (Ex. 2001, ¶75).

This variation in operating frequency and period is typical for circuits like McDonald's. McDonald's circuit is an example of a class of converters called "LLC series resonant converters". The term "LLC" refers to the fact that two inductors (two "L"s) and one capacitor (one "C") are critical to its operation. (Ex. 2001, ¶76). These components are shown in the added red-dashed box shown in Fig. 1 of McDonald, reproduced here:

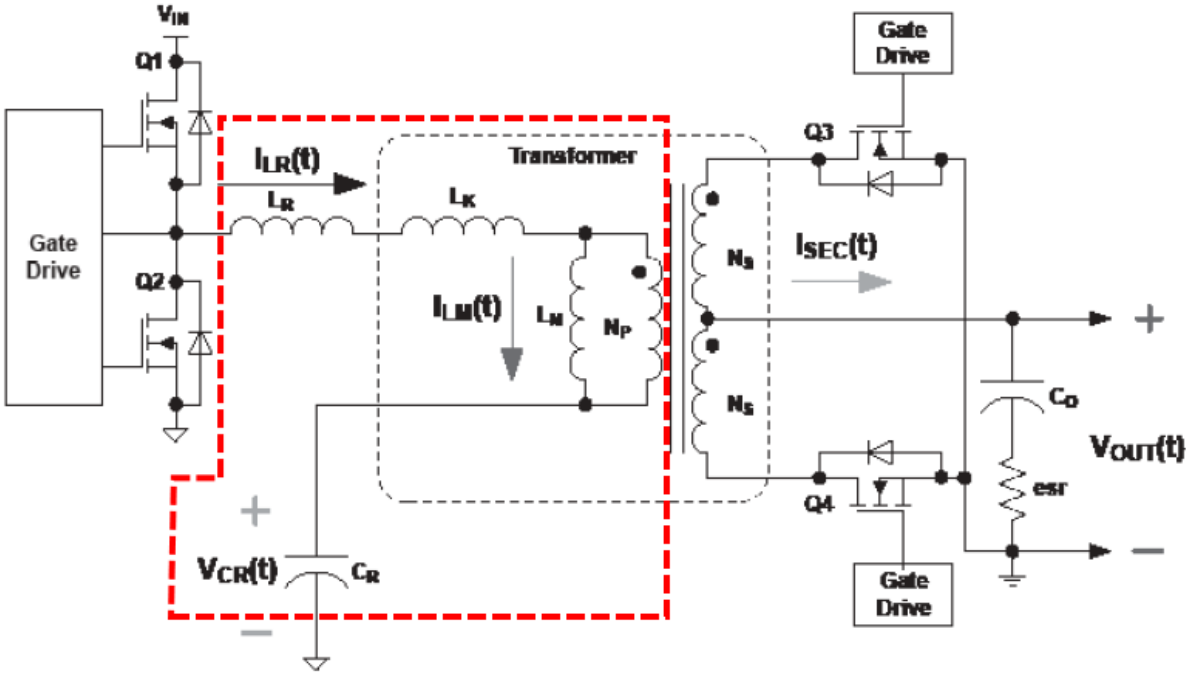


Figure 1 – Basic LLC schematic.

(Ex. 1005, Fig. 1)(Ex. 2001, ¶76). The LLC components consist of the following elements arranged in series: an inductor labeled L_R, the magnetizing inductance of the transformer's primary windings (which have been represented mathematically as the combination of a leakage inductance L_K and a magnetizing inductance L_M), and capacitor C_R. (Ex. 2001, ¶76).

The two inductors and capacitor in the "LLC" circuit are used to provide regulation. (Ex. 2001, ¶77). That is, the operating frequency of the LLC is varied across a range of frequencies, usually above the resonant frequency, to regulate the output voltage of the converter. (Ex. 2001, ¶77). Regulation is provided by frequency-dependent changes in relative impedances of critical LLC components.

(Ex. 2001, ¶77).

At a high level, LLC resonant converters *change their switching frequencies to provide a regulated voltage output*. Petitioner Delta's own U.S. Pat. No. 7,184,280 explains this operation as follows:

> "The power switches S1 and S2 of the **LLC series resonant converter** operate under the condition of equal pulse width, that is, in the condition of 50%. A frequency adjustment controller 140 is therefore demanded because **the adjustment of the output voltage is obtained by changing the operation frequency**."

(Ex. 2011, 1:60-65)(Ex. 2001, ¶78). Note that this discussion refers to the circuit of Fig. 1 of the '280 patent, which has an identical series-resonant topology to that of McDonald. (Ex. 2001, ¶78).

This behavior of LLC resonant converters is explained in a number of other documents. (Ex. 2001, ¶79). For example, a predecessor to McDonald, a 2010 Texas Instruments white paper called "Designing an LLC Resonant Half-Bridge Power Converter" explains:

> "Among resonant converters, two basic types are the **series resonant converter** (SRC), shown in Fig. 1a, **and the parallel resonant converter** (PRC), shown in Fig. 1b. **Both of these converters regulate their output voltage by changing the frequency of the driving voltage** such that the impedance of the resonant circuit changes. The input voltage is split between this impedance and the

load."

(Ex. 2012, p. 1)(Emphasis added)(Ex. 2001, ¶79).

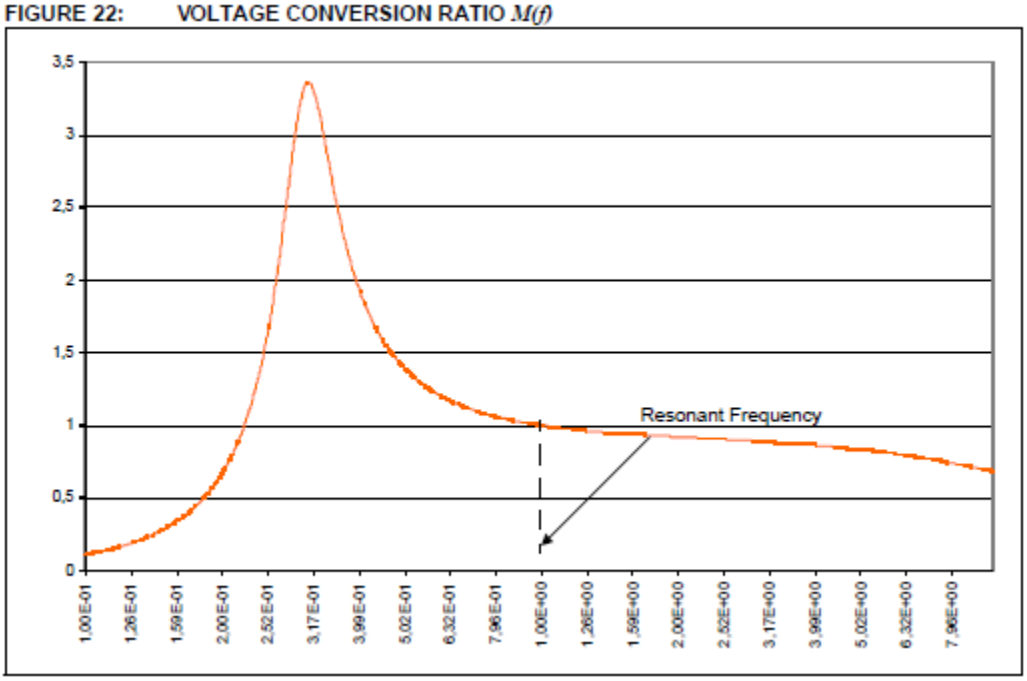
Another prior-art reference put forward by Delta in Ground VII, AN1336, explains:

> "By modifying the switching frequency f_S, the gain of the LLC circuit is changed and therefore the output voltage can be controlled with varying load and input voltage."

(Ex. 1019, p. 1, left column)(Ex. 2001, ¶80).

A plot of the converter voltage conversion ratio (represented by M) versus a normalized operating frequency (the actual operating frequency divided by the resonant frequency, which is a constant) for an LLC resonant converter is shown in Fig. 22 of AN1336, reproduced here:

FIGURE 22: VOLTAGE CONVERSION RATIO *M(f)*



(Ex. 1019, p. 19)(Ex. 2001, ¶81). This curve has a characteristic shape for LLC resonant converters, and similar graphs can be found throughout the literature. (Ex. 2001, ¶81)(Ex. 2012, pp. 10, 12, 15)(Ex. 1005, p. 7).[4] As can be seen from these graphs, the voltage transformation ratio varies substantially with operating frequency. (Ex. 2001, ¶81). The operating frequency, in turn, is varied to counteract changes in input voltage and regulate the output voltage. (Ex. 2001, ¶81).

Delta's quote from page 5-4 of McDonald (Petition, p. 32)("the operating

[4] These graphs sometimes express the voltage transformation ratio as a "gain" function. (Ex. 2012, p. 8)("the relationship between the input voltage and output voltage can be described by their ratio or gain.").

frequency is exactly equal to the dominant frequency of the resonant tank") is taken out of context. (Ex. 2001, ¶82). The quote refers to one part of a "piecewise" (p. 5-4) mathematical analysis of the circuit. (Ex. 2001, ¶82). In this analysis, McDonald breaks down the characteristics of the converter depending on operating frequency. (Ex. 2001, ¶82). The quote from page 5-4 is referring to one portion of the analysis at a boundary *point* between frequency *ranges* above and below the resonant frequency. (Ex. 2001, ¶82). It is clear from the subsequent passages (where McDonald also mathematically analyzes operation *above* and *below* the resonant frequency) that frequency modulation is being used. (Ex. 1005, pp. 5-4 and 5-5)(Ex. 2001, ¶82).

In fact, Delta *relies* on the frequency-modulating aspect of McDonald under limitation 1[d], when it quotes page 5-5 of McDonald (describing how the system will lower the operating frequency to counteract a lower input voltage). (Petition, p. 35)(Ex. 1005, p. 5-5)(Ex. 2001, ¶83).

Because McDonald's converter modulates the operating frequency in order to control the output voltage, McDonald does not have a "standard converter operating cycle, having a standard operating period and frequency", and does not teach limitation 1[c]. (Ex. 2001, ¶84).

2. Limitation 1[d] — "turn the at least one primary switch ON and OFF at times when essentially zero voltage is impressed across the respective at least one primary switch and essentially zero resonant current is flowing in the respective at least one primary switch;"

Limitations 1[d] and 1[e] require (in limitation 1[d]) "turn[ing] the at least one primary switch ON and OFF at times when essentially zero voltage is impressed across the respective at least one primary switch *and* essentially zero resonant current is flowing in the respective at least one primary switch;" and (in limitation 1[e]) "turn[ing] the at least one secondary switch ON and OFF at times when essentially zero current is flowing in the respective at least one secondary switch *and* essentially zero voltage is impressed across the respective at least one secondary switch". This Preliminary Response will refer to these specific requirements of limitations 1[d] and 1[e] with the shorthand of "zero-voltage switching" ("**ZVS**") and "zero-current switching" ("**ZCS**") for primary- and second-side switches.

McDonald does not teach limitation 1[d], because its primary-side switches do not switch with essentially zero resonant current flowing therethrough. (Ex. 2001, ¶85). Specifically, McDonald's LLC resonant converter has two primary-side switches, Q1 and Q2, as shown in Fig. 1, reproduced again here with added red-dashed boxes around the primary-side switches:

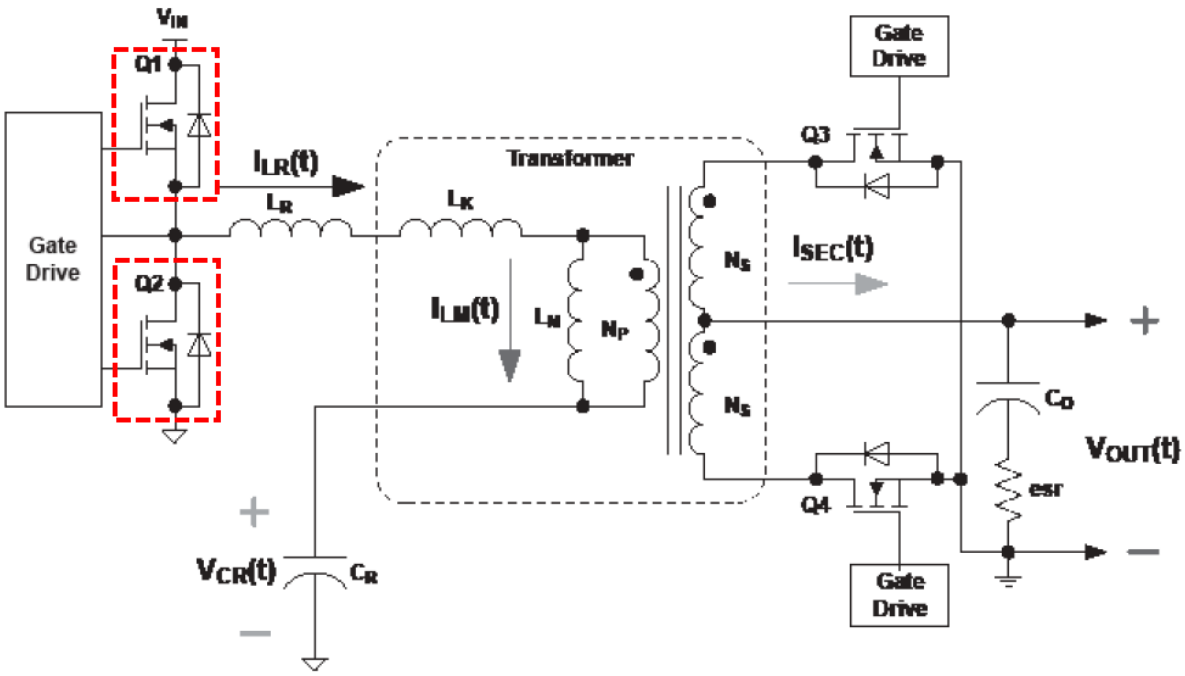


Figure 1 – Basic LLC schematic.

(Ex. 1005, Fig. 1)(Ex. 2001, ¶85).

McDonald states that the converter, while providing ZCS in its secondary switches, Q3 and Q4, does ***not*** provide zero-*current* switching (ZCS) of its primary switches, Q1and Q2. McDonald explains this on page 5-5:

> "In Figures 3 and 4, notice that the current through Q3 and Q4 naturally decays to 0 A, providing zero current switching (ZCS) for these devices. In this case, **switching Q1 and Q2** – prior to Q3 and Q4 reaching zero current – **results in the loss of ZCS for these devices**."

(Ex. 1005, p. 5-5)(Emphasis added)(Ex. 2001, ¶86). Notably, Delta relies on this portion of McDonald for its analysis under limitation 1[e], below.

The ability to achieve only ZVS (**not ZCS**) on the primary-side switches was

a well-known limitation of LLC resonant converters in the relevant timeframe. (Ex. 2001, ¶87). As Delta's own U.S. Pat. No. 6,344,979, issued in 2002, explained for the primary-side switches of a variable frequency resonant converter:

> "Generally, when switching frequency is above the resonant frequency, the switches turn on at Zero Voltage condition, thus eliminating the turn-on switching losses. In order to regulate the output Voltage, the series resonant converter and parallel resonant converter apply a variable switching frequency control method."

(Ex. 2006, 1:42-47)(Emphasis added)(Ex. 2001, ¶87). The primary side of the series-resonant circuit topology to which this discussion pertains (in Fig. 1) is equivalent to the converter in McDonald. (Ex. 2001, ¶87).

Delta's U.S. Pat. No. 7,599,198, issued in 2009, expands this discussion, noting that an LLC resonant converter achieves ZVS (but not ZCS) for primary-side switches, and ZCS (but not ZVS) for secondary-side switches (called "rectification transistors"):

> "In FIG.1, the **LLC series resonance converter** 100 employs the switch circuit 110, the resonance circuit 120, the transformer TX, and the full-wave rectification circuit 130 to convert a DC input Voltage Vin of an input terminal into an output Voltage Vo of an output terminal, wherein **by a suitable parameter design and operating range**, the power **transistors** of the bridge circuit lying to the **primary side** of the transformer TX can be assured to operate under the condition of **zero-voltage switching (ZVS),** and **rectification**

> **transistors** lying to the **secondary side** of the transformer TX can implement **zero-current switching (ZCS)**."

(Ex. 2007, 1:29-41)(Emphasis added)(Ex. 2001, ¶87). The topology of this converter (in Fig. 1) is also equivalent to the topology to McDonald's. (Ex. 2001, ¶87).

Delta's U.S. Pat. No. 7,184,280, issued in 2007, further explains:

> "**LLC series resonant converter** has the characteristics that **proper parametric design and operating ranges** can guarantee the power **switches** of a **primary side** bridge circuit to be operated under a **Zero Voltage Switching (ZVS)** condition, and at the same time causing the rectification **switches** of a **secondary side** to perform as **Zero Current Switching (ZCS)**."

(Ex. 2011, 1:66-2:4)(Emphasis added)(Ex. 2001, ¶87). As each of these patents shows, LLC resonant converters could achieve ZVS, but not ZCS, on their primary-side switches, and ZCS, but not ZVS, on their secondary-side switches. (Ex. 2001, ¶87).

The reason why the primary-side switches can achieve ZVS above the resonant frequency is explained in reference [2] to the McDonald paper, which is an earlier TI paper from the same "Power Supply Design Seminar", entitled "Designing an LLC Resonant Half-Bridge Power Converter". (Ex. 2012)(Ex. 2001, ¶88). This paper explains that to achieve ZVS on the primary-side switches, the input

impedance needs to be inductive. (Ex. 2012, pp. 13-16)("To achieve ZVS, the designer must determine the conditions where the input impedance, Zin (shown in Fig. 9a), can be inductive.")(Ex. 2001, ¶89). By far the largest range of operating conditions under which the input impedance is inductive occurs when the operating frequency is greater than the resonant frequency. (Ex. 2012, pp. 13-16, Fig. 9b)(Ex. 2001, ¶88).

In accord with this known behavior, McDonald only states that the converter achieves ZVS for the primary-side switches and ZCS for the secondary switches, *not* ZCS and ZVS for both, primary and secondary switches. (Ex. 1005, p. 3, right column, p. 5, right column)(Ex. 2001, ¶89). Ignoring the express teachings of McDonald, the Petition attempts to make inferences from graphs and out-of-context statements. The Petition's analysis, however, is incorrect. (Ex. 2001, ¶89).

The Petition argues that Fig. 3 of McDonald shows the primary-side switches Q1 and Q2 turning ON and OFF with zero resonant current. (Petition, pp. 33-34). The Petition again takes McDonald's disclosure out of context. (Ex. 2001, ¶90). Delta takes a "piecewise" analysis of McDonald's operation at a boundary *point* in between two *ranges* of operating frequencies (above or below resonance) and represents it to be characteristic of the operation of the converter. It is not. (Ex. 2001, ¶90). With respect to Fig. 3, upon which the Petition's analysis is based, McDonald states: "Figure 3 shows the operation **at the boundary between two of**

the most common operating modes of the converter." (Ex. 1005, p. 5-4)(Ex. 2001, ¶90). Figure 3 shows the operation at the transition point between two ranges of operating frequencies, below and above the resonant frequency. (Ex. 1005, p. 5-4)(Ex. 2001, ¶90). This is because McDonald's circuit operates (*i.e.*, regulates its output) by changing its frequency either above or below the resonant frequency. (Ex. 1005, p. 5-3)("The output voltage is commonly controlled by using a fixed duty cycle (e.g., 50 percent) and a variable frequency.")(Ex. 1005, p. 5-5)("The input voltage is now reduced so that the system control effort changes the frequency to something below the resonant frequency…")(Ex. 1005, p. 5-5)("The input voltage is now increased so that the system control effort changes the frequency to something above resonance.")(Ex. 2001, ¶90).

The Petition makes no argument that it would have been obvious to change this behavior of McDonald. Thus, the Petition does not show that McDonald teaches claim limitation 1[d].

3. Limitation 1[e] — "turn the at least one secondary switch ON and OFF at times when essentially zero current is flowing in the respective at least one secondary switch and essentially zero voltage is impressed across the respective at least one secondary switch; and"

McDonald likewise does not teach limitation 1[e], because its secondary-side switches do not switch with essentially zero voltage is impressed across them. (Ex. 2001, ¶92).

The discussion above under limitation 1[d] also applies here. As discussed there, McDonald only says that ZCS is achieved for secondary-side switches, not ZVS. (Ex. 2001, ¶93)(*e.g.* Ex. 1005, pp. 5-3 and 5-5)(stating that ZVS is achieved for primary-side switches Q1 and Q2, but not saying that ZVS is achieved for secondary-side switches Q3 and Q4). Achieving ZCS for secondary-side switches, without ZVS, was, in the relevant timeframe, known behavior for LLC Resonant Converters. (Ex. 2001, ¶93)(Ex. 2011, 1:66-2:4)(Ex. 2006, 1:29-41).

In a single sentence, Delta attempts to argue that the secondary-side switches achieve ZVS, stating:

> "McDonald also discloses that secondary switches Q3 and Q4 turn on and off with zero voltage switching. Ex. 1005, 5-21 ('Figures 32, 33 and 34 illustrate this feature in action. . . . Notice that in all cases, the body-diode conduction time across the synchronous rectifiers is very close to minimum.'); Ex. 1003, ¶ 88."

(Petition, p. 36). This argument is not further explained, however, and Dr. Hopkins' declaration at ¶88 copies the Petition verbatim.

In fact, the quoted portion of McDonald does not demonstrate ZVS on the secondary-side switches. (Ex. 2001, ¶95). On page 5-21, McDonald is referring to a synchronous rectifier pulse-width clamp that comes into play when pulse-width modulation is used. (Ex. 1005, p. 5-20)(Ex. 2001, ¶95). Pulse-width modulation is used in McDonald when the switching frequency gets too high. (Ex. 1005, pp. 5-17

– 5-19)(Ex. 2001, ¶95). And as McDonald explains for the synchronous rectifier pulse-width clamp:

> "Figure 31 illustrates the MOSFET control signals for this operating mode. The synchronous rectifiers simply follow the primary MOSFET signal (minus dead times) until the pulse width is longer than the preprogrammed clamp value. Once this happens, **frequency adjustments continue to occur on all channels**; however, only the primary MOSFET control signals maintain their duty-cycle ratio of ~50 percent."

(Ex. 1005, p. 5-20)(Emphasis added)(Ex. 2001, ¶95). Thus Delta's arguments also show that it is relying on a circuit making frequency adjustments (contrary to claim limitation 1[c]) in an attempt to show claim limitation 1[e].

4. Limitation 1[f] — "wherein the oscillator frequency is preset"

Finally, the combination does not teach or render obvious claim limitation 1[f]. For limitation 1[f], the Petition simply refers to "an internal oscillator frequency $f_{(PCLK)}$" of TI UCD 3138, asserting that the frequency is pre-set. (Petition, pp. 36-37). However, TI UCD 3138 itself teaches that the oscillator may vary over the range of 240 to 260 MHz. (Ex. 1006, p. 17)(Ex. 2001, ¶96).

Ground I thus does not satisfy the Petitioner's burden.

C. Grounds II through VII Lack a Reasonable Expectation of Success and Motivation

Grounds II – VII all share a common theme: in each Ground, one or more

lead references (Shimada, Chen, Pan in view of TI UCD3138, Peng in view of TI UCD3138, Leung, and AN1336 in view of dsPIC33FJ06GS101) are combined with alleged admitted prior art ("AAPA") from the '481 patent. The combinations are each based on a standard argument that is essentially the same in each Ground, as shown in the following example passage from Ground II:

> "A POSITA would have been motivated to combine Shimada with the AAPA for purposes of zero current and zero voltage switching because both are related to resonant converters, and Shimada contemplates zero current and zero voltage switching, which the AAPA explicitly teaches. Ex. 1003, ¶ 107. Thus, a POSITA would have understood and expected that the AAPA's teachings, which were generally known in the prior art, would apply to Shimada's resonant converter, and would have looked to the AAPA for additional details related to zero current and zero voltage switching. Id."

(Petition, pp. 50-51). Nearly identical arguments are made in the other Grounds. (Petition, pp. 57-58 (Ground III), 67-68 (Ground IV), 94-95 (Ground V), 106-107 (Ground VI), 115-116 (Ground VII). Dr. Hopkins' declaration copies the Petition verbatim in each case, providing no further explanation. (Ex. 1004, ¶¶107, 127, 151, 194, 233, and 249).

These Grounds are fatally deficient, because they lack *any* explanation of why there would have been a reasonable expectation of success, and lack a sufficient

explanation of the motivation for the combination. (Ex. 2001, ¶99).

1. There would have been no reasonable expectation of success for Grounds II-VII

As discussed above in §III.A, the Petition provides no basis for concluding that there would have been a reasonable expectation of success for any Ground. (Ex. 2001, ¶100). This deficiency plays out similarly for each of Grounds II-VII.

As can be appreciated from the discussion above[5] with respect to McDonald, however, it is not a simple matter to configure a circuit to achieve *either* ZVS or ZCS on *either* the primary or secondary switches, much less both ZVS and ZCS on both a primary- and secondary- switch. (Ex. 2001, ¶101). First, the converter topology and its operating parameters must provide an *opportunity* to implement ZVS or ZCS. (Ex. 2001, ¶101). To achieve ZVS, for example, zero voltage must be present across a MOSFET channel in a time interval long enough for the MOSFET to be turned ON. (Ex. 2001, ¶101). Thus ZVS can *only* be achieved with certain power train topologies, component values, and control methods, which is neither common nor simple. (Ex. 2001, ¶101). As the Peng prior art reference submitted by the Petitioner states:

> "**Switching with zero current** flowing through **or** **zero voltage** across the switching element, which is **known as 'soft switching'**,

[5] *See* §§III.B.2 and III.B.3, beginning on pages 21 and 27.

> alleviates these problems. **Obtaining soft-switching can be difficult**, however, because it requires repeatedly driving the voltage across or forcing the current through the switching element to zero, and then holding the voltage or current at this zero level long enough for the switching element to physically switch."

(Ex. 1012, 1:42-50)(Emphasis added)(Ex. 2001, ¶101).

The precursor publication to McDonald is also illustrative. (Ex. 2012). As explained there, to achieve *only* ZVS on *only* the primary switches of an LLC resonant converter, the designer needed to create dead times during the primary switching drive currents (p. 14), needed to ensure that the input impedance was fundamentally inductive (pp. 14-15)—a requirement the authors met by constraining the operating frequency within a range (points a1 to a4) well above the resonant frequency (p. 15)—and needed to ensure that there was sufficient inductive energy for the converter to operate with ZVS (pp. 15-16). (Ex. 2001, ¶102). And that effort was required to meet only *one* (ZVS on the primary switches) of the four combined ZVS-ZCS requirements of claim limitations 1[d] and 1[e]. The AAPA, in contrast, achieves ZVS-ZCS with a *unique* power train in a class of topologies controlled to do so: Vicor's prior art Sine-Amplitude Converters (SACs). (Ex. 2001, ¶102).

The Petition essentially suggests that a PHOSITA—based on the mere knowledge that Vicor had previously achieved a converter with ZVS and ZCS—would have undertaken some unknown redesign of each of the six different primary

references to achieve claim limitations 1[e] and 1[d]. But given the known difficulties in achieving ZVS and ZCS and the lack of any supporting reasoning in the Petition, there would have been no reasonable expectation that such a redesign would be successful. (Ex. 2001, ¶103).

2. There would have been no motivation for Grounds II-VII.

Beyond the lack of a reasonable expectation of success, the Petition's invitation to perform *ad hoc* circuit surgery on the primary references raises a problem concerning the purported motivation. Even assuming that a hypothetical redesign to achieve *both* ZVS and ZCS for *both* primary- and secondary-side switches was *possible*, the result would be a different circuit, with different principles of operation. (Ex. 2001, ¶104). Vicor's prior Sine-Amplitude Converter, for example, used a power train within a unique class of topologies, component values, and control method to achieve ZVS and ZCS. (Ex. 2001, ¶104). Petitioner has not even attempted to evaluate whether a prior-art circuit, modified in an unknown way to achieve ZVS and ZCS, would not be otherwise impaired to an extent that no one would attempt the modification—even if they knew what it was. *See In re Ratti*, 270 F.2d 810, 813 (C.C.P.A. 1959)(Claim not obvious because the "suggested combination of references would require a substantial reconstruction and redesign of the elements shown in Chinnery et al. as well as a change in the basic principles under which the Chinnery et al. construction was designed to operate.").

Of course, Vicor cannot say whether or how a principle of operation might change without knowing what the changes to the circuits might be, but proposing realistic changes was the Petitioner's burden, especially in a field as complex as this one. *See Medtronic, Inc. v. Teleflex Innovations S.A.R.L.*, 70 F.4th 1331, 1347 (Fed. Cir. 2023)("The Board explained '[t]he extensive need to modify Kontos' device in a way not suggested in the Petition supports [Teleflex's] argument that the proposed modifications are based on a hindsight desire to recreate the claimed invention, as opposed to a known need in the art for such a device.' *Id*. The Board did not err in discounting modifications not presented in Medtronic's petition as indicative of hindsight.").

3. The AAPA teaches away from the combinations in Grounds II-VII.

Finally, with respect to each of Grounds II – VII, the AAPA *teaches away* from switching control in the manner set forth in the claims. The AAPA does this in two ways.

First, as explained above in the Introduction (*see* §I.C, beginning on p. 19), Vicor's prior art SAC used analog circuitry to automatically control ZCS and ZVS of primary and secondary switches. (Ex. 1001, 1:39-43, 2:8-14)(Ex. 1009, 21:52-22:8)(Ex. 2001, ¶106). The analog circuitry controlled the timing of switching events for each primary and secondary MOSFET. (Ex. 2001, ¶106). This was thought to be necessary because the elements that determined the resonant frequency

(transformer leakage inductance and resonant capacitance) could exhibit variabilities. (Ex. 2001, ¶106). The analog control circuitry relied on closed loop control to *automatically* compensate for those variabilities. (Ex. 2001, ¶106). Causing all switch transitions to happen automatically, as taught by the AAPA, was thought to eliminate the need to adjust component values in each module, to achieve zero-voltage and zero-current switching, provide better "spectral purity" (more sinusoidal current waveforms), and improve the performance of converters connected in parallel. This is described in Vicor's prior U.S. Pat. No. 6,984,965 (Ex. 1009), upon which the Petition relies as AAPA under limitation 1[d] in each of Grounds II-VII. (Petition, pp. 55, 62, 75, 100, 112, 120). The '965 patent, discussing a Sine-Amplitude Converter, states:

> "One way of controlling the switches in the SAC is to turn them ON and OFF using signals whose frequency, relative timing and ON and OFF intervals are pre-determined. **This, however, requires that the relative timing of the switch control signals be adjusted** to compensate for variations in the characteristic resonant frequency due, for example, to component value variations in individual units. **A preferred way to control the switches is to provide an 'automatic switch controller'** which automatically turns the switches OFF at times when the sinusoidal component of the currents I, and I (FIGs. 10C, 10D) returns essentially to zero and which provides an energy-recycling interval sufficient for ZVS at each switch transition prior to turning the complementary switch ON. **The**

> **benefits of using an automatic switch controller include** minimization of switching and conduction losses and maximization of converter efficiency; elimination of timing adjustments in individual SAC units due to variations in values of circuit elements resulting from component tolerances, optimization in current sharing accuracy among SACs in a parallel array, as discussed below; optimization of soft switching, *i.e.* primary ZVS and secondary ZCS and ZVS; and maximization of the spectral purity of the sinusoidal waveforms in the converter."

(Ex. 1009, 21:52-22:8)(Emphasis added)(Ex. 2001, ¶106).

The control methodology of the automatic switch controller disclosed in Vicor's prior '965 patent in the paragraph above is in stark contrast to the control methodology of the '481 patent. (Ex. 2001, ¶107). The '481 patent, as described above in the Introduction, uses a digital SAC controller to *impose* a standard operating period and frequency (claim limitation 1[c]), with an oscillator whose frequency is pre-set (claim limitation 1[f]) to set a series of independent switching events. (Ex. 2001, ¶107). This method is rooted in an approach that the '965 patent considered, but rejected, when it states "[o]ne way of controlling the switches in the SAC is to turn them ON and OFF using signals whose frequency, relative **timing and ON and OFF intervals are pre-determined**. **This, however…."** (Ex. 1009, 21:52-22:8)(Emphasis added)(Ex. 2001, ¶107)(Ex 2030, ¶24). Analog circuitry sensing the phase of the resonant current compensated for component variabilities

by not allowing timing events of switch transitions to be set independently (limitation 1[g]). (Ex. 2001, ¶107).

Second, the AAPA in the Background of the '481 patent explains that, for efficient operation at high frequency, it was thought to be necessary to recapture energy used to charge and discharge the gate capacitances of the MOSFET switches. (Ex. 1001, 2:13-22)(Ex. 2001, ¶108). The Background of the '481 patent teaches to use particular analog circuitry to effect the MOSFET switching in order to recapture the energy necessary to charge and discharge MOSFET gate capacitances:

> "One way to efficiently recycle the energy is to use a resonant technique. Apparatus and methods for resonant recycling of capacitive gate energy are described in: High Efficiency Floating Gate Driver Circuit Using Leaking Inductance Transformer, Vinciarelli, U.S. Pat. No. 6,107,860; Lossless Gate Driver Circuit for a High Frequency Converter, Steigerwald, U.S. Pat. No. 5,010,261; High Frequency Control of a Semiconductor Switch, Toile et al., U.S. Pat. No. 7,602.229; and Gate Driving Circuit, Inoshita, U.S. Pat. No. 7,091,753."

(Ex. 1001, 2:13-22)(Ex. 2001, ¶108)(Ex. 2030, ¶¶26-28).

The AAPA thus teaches away from the claims of the '481 patent. *See In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994)("A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction

divergent from the path that was taken by the applicant."). The Petition fails to account in any way for this teaching of the prior art it cites.

D. Ground II (Obviousness over Shimada in view of AAPA) does not meet the Petitioner's burden.

Ground II (obviousness over Shimada in view of AAPA) does not meet the Petitioner's burden because it is fatally unclear, and even so, does not meet several elements of the claims. (Ex. 2001, ¶110).

1. The obviousness case over Shimada is not clear and does not meet the basic requirements of a case for obviousness

The obviousness case over Shimada does not meet the Petitioner's burden to articulate the Petition's theory clearly and with particularity, providing the basic components of a case for obviousness. *See Netflix, Inc. v. DivX, LLC*, No. 2022-1203, at *8-9 (Fed. Cir. Oct. 25, 2023)("Ultimately, it is the petitioner's burden to present a clear argument."); *Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016)("It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify "with particularity" the "evidence that supports the grounds for the challenge to each claim." 35 U.S.C. § 312(a)(3).").

The Petition's argument is insufficiently clear because it relies on different portions of Shimada, relating to different circuits, without explaining how the cited portions of Shimada relate to one another. (Ex. 2001, ¶111). The Petition first seems

as though it will rely on the circuit in Fig. 10, which is reproduced under the Petition's mapping for limitation 1[a]. (Petition, p. 52). However, the remainder of the claim mapping portion does not mention Fig. 10, instead relying on Shimada's teachings at ¶¶0012, 0028-0029, 0031, 0127, and 0137, and the waveforms in Figs. 20A-20C, as well as the circuit in Fig. 23. Paragraphs 0012, 0028-0029, and 0031 relate to the embodiment of **Fig. 1**, while paragraphs 0127 and 0137 (as well as the waveforms of Figs. 20A-20C) relate to the embodiment of **Figs. 15 or 19**. The embodiments of Figs. 1, 15, and 19 are fundamentally different from claim 10, as can be immediately seen from the fact that none of Figs. 1, 15 or 19 has a transformer. (Ex. 2001, ¶111). Figure 10 of Shimada *does* have a transformer, but the Petition provides no explanation of how the teachings relating to transformerless circuits of Figs. 1, 15, and 19 might relate to the embodiment of Fig. 10, instead simply providing citations as if all the circuits operated in the same way. The portion of Shimada that relates to Fig. 10, namely ¶¶0077-0090, is not cited in the Petition. And the Petition provides no argument that it would be obvious to combine different embodiments of Shimada in some way. *See In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017)("Whether a rejection is based on combining disclosures from multiple references, combining multiple embodiments from a single reference, or selecting from large lists of elements in a single reference, there must be a motivation to make the combination and a reasonable expectation that such a

combination would be successful, otherwise a skilled artisan would not arrive at the claimed combination.").

2. Limitation 1[a] — "…the resonant power train including a transformer and having a characteristic resonant frequency and period…"

As noted immediately above, the portions of Shimada on which the Petition relies for each of limitations 1[b] – 1[g] do not have a transformer, nor is there any basis in the Petition to add a transformer to these circuits. (Ex. 2001, ¶112).

3. Limitation 1[c] — "standard converter operating cycle, having a standard operating period and frequency"

Shimada also does not teach or render obvious limitation 1[c], and in particular, the requirement of a "standard converter operating cycle, having a standard operating period and frequency". (Ex. 2001, ¶113).

Under this limitation, the Petition argues that "[t]he converter in Shimada inherently operates at the resonant period and frequency to achieve ZVS and ZCS." (Petition, p. 53). The Petition thus appears to be arguing that because Shimada (allegedly) uses ZVS and ZCS, it is inherently operating at the resonant frequency, and thus inherently at a "standard operating period and frequency". But there are three problems with this:

First, the argument is just factually wrong. Shimada teaches changing the operation frequency in order to change the output power of the converter. (Ex. 1008, ¶0066, 0069, 0121-0126)(Ex. 2001, ¶115). Shimada teaches using a switching

frequency called "f1". (Ex. 1008, ¶0030)("frequency f1 at which the gate signals SGGV1, SGGX1, SGGV2 and SGGX2 repeat the cycle described below.")(*see also* ¶0031)(Ex. 2001, ¶115). Shimada teaches to vary the switching frequency to vary the amount of power transfer:

> "[B]y adjusting the frequency f1, the amount of power charge per time from the secondary battery E1 to the secondary battery E2 can be adjusted."

(Ex. 1008, ¶0126)(Ex. 2001, ¶115). Shimada also directly describes the frequency f1 being different from the resonant frequency, *e.g.*:

> "The capacitors CM1 and CM2 and the inductors Ldc1 and Ldc2 should be selected so that **the resonant frequency** between the capacitor CM1 and the inductor Ldc1 and **the resonant frequency** between the capacitor CM2 and the inductor Ldc2 **are no greater than half of the frequency f1**."

(Ex. 1008, ¶0032)(Emphasis added)(*see also* ¶¶0054, 0087)(Ex. 2001, ¶115).

Second, neither the Petition nor Dr. Hopkins makes a case for inherency. *See Par Pharmaceutical, Inc. v. TWi Pharmaceuticals, Inc.*, 773 F.3d 1186, 1195 (Fed. Cir. 2014)("Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.")(*quoting In re Oelrich*, 666 F.2d 578, 581 (C.C.P.A. 1981)). Showing how operation at the resonant frequency necessarily results from

the ZCS or ZVS teachings of Shimada is especially important, because as discussed above in §III.B.2 (pp. 33-40) with respect to McDonald, it is quite possible for converters to achieve ZVS or ZCS for certain switches, under certain operating conditions, *without* operating at a resonant frequency. (Ex. 2001, ¶116).

Third, the factual premise of the Petition's argument is incorrect: Shimada does not "achieve ZVS and ZCS". (Ex. 2001, ¶117). Shimada states (in the paragraph cited by the Petition at p. 54), that it can, under certain circumstances, achieve *one or the other*:

> "As can be seen from FIG. 20A to 20C, when switching the gate signals from the on signal to the off signal, the capacitor voltage of that MERS is almost zero, and when switching the gate signals from the off signal to the on signal, the current flowing in the inductor Lm is almost zero. Therefore, the switching of each switch is at zero voltage **or** zero current, and soft switching is achieved with both high and low charges per time."

(Ex. 1008, ¶0127)(Emphasis added)(Ex. 2001, ¶117).

Shimada thus does not teach or render obvious the portion of limitation 1[c] requiring a "standard converter operating cycle, having a standard operating period and frequency".

4. Limitations 1[d] and 1[e]—ZVS and ZCS for primary and secondary-side switches

Shimada also does not teach or render obvious the portions of limitations 1[d]

and 1[e] that require ZVS and ZCS for primary- and secondary-side switches. (Ex. 2001, ¶119).

First, in the Petition's discussion relating to limitations 1[d] and 1[e], the Petition relies on ¶0127 of Shimada, which relates to Figs. 15 and 19. (Petition, p. 54)(Ex. 1008, ¶0121)(Ex. 2001, ¶120). The embodiments of these figures do not have a transformer. Because the transformer *defines* the primary and secondary sides (the transformer is the boundary between the two) it makes no sense to talk about "primary" and "secondary" switches in the context of this embodiment of Shimada. (Ex. 2001, ¶120). Second, the very paragraph cited by the Petition (¶0127) states that "switching of each switch is at zero voltage **or** zero current"—not both. (Ex. 1008, ¶0127)(Emphasis added)(Ex. 2001, ¶120).

This problem is not solved by the AAPA for the reasons discussed above in §III.C, beginning on page 40. And in particular, the Petition makes no effort to show how Shimada's transformerless, bidirectional circuit of Fig. 19 has *any* relevance to Vicor's prior work described in the AAPA. (Ex. 2001, ¶121).

Ground II thus does not satisfy the Petitioner's burden.

E. Ground III (Obviousness over Chen in view of AAPA) does not meet the Petitioner's burden

Ground II (obviousness over Chen in view of AAPA) does not meet the Petitioner's burden because it does not meet several elements of the claims. (Ex. 2001, ¶123).

1. Limitation 1[c]—"standard converter operating cycle, having a standard operating period and frequency"

The combination does not teach or render obvious the portion of limitation 1[c] requiring a "standard converter operating cycle, having a standard operating period and frequency". This is because Chen operates with a *variable* operating frequency. (Ex. 1010, 3:38-42)(Ex. 2001, ¶124). The variable operating frequency is controlled by VCO 2. (Ex. 1010, 3:1-5, 3:38-40, 9:63-10:3)(Ex. 2001, ¶124). A "VCO" is a "Voltage-Controlled Oscillator"—an oscillator whose frequency changes depending on its applied voltage. (Ex. 2001, ¶124). Chen uses VCO 2 to change its operating frequency in order to regulate the output voltage of the circuit. As Chen explains:

> "The output voltage V supplied to the load LD is fed back to the driving circuit 3 of the MOSFETs Qa, Qb via the error amplifier 1 and a VCO (voltage controlled oscillator circuit) 2. Here, gate signals Vga, Vgb which are turned on and off in alternation with prescribed timing are generated in the driving circuit 3, and the currents Ia, Ib of the MOSFETs Qa, Qb are controlled so as to flow in the directions of the arrows with prescribed timing. The current Ib flows in the direction opposite the arrow depending on operating conditions. Here, **the output frequency of the VCO 2 is changed to be higher when it is judged from the output of the error amplifier 1 that the output Voltage V is higher than a preset Voltage**, or that the load LD is a light load. Conversely, **when it is judged that the output Voltage V is lower than the preset**

Voltage, or that the load LD is a heavy load, the VCO 2 functions to lower the output frequency."

(Ex. 1010, 9:63-10:3)(Emphasis added)(Ex. 2001, ¶124).

Thus, Chen has no standard operating period and frequency, as required by limitation 1[c]. (Ex. 2001, ¶125).

The Petition asserts that "[t]he converter in Chen inherently operates at the resonant period and frequency to achieve ZCS." (Petition, p. 61). This, however, fails for reasons similar to those described above with respect to Shimada (*see* above, §III.D.3, beginning on p. 51). Specifically, Chen *expressly* teaches that its operating frequency varies (Ex. 1010, 3:1-5) and that it is different from the resonant frequency (Ex. 1010, 3:38-40)("The operating frequency fop changes with the circuit parameters and the load state, but the resonance frequency fr1 is determined by the magnitudes of the resonance capacitor Cr and the resonance inductor Lr.")(Ex. 2001, ¶126). In any case, neither the Petition nor Dr. Hopkins even made a case for inherency. *See Par Pharm.*, 773 F.3d at 1195. And even were *that* not so, Chen does not "achieve ZCS" (a predicate assumption in the Petition's argument), as discussed in the next section. (Ex. 2001, ¶126).

2. Limitations 1[d] and 1[e]—ZVS and ZCS for primary- and secondary-side switches

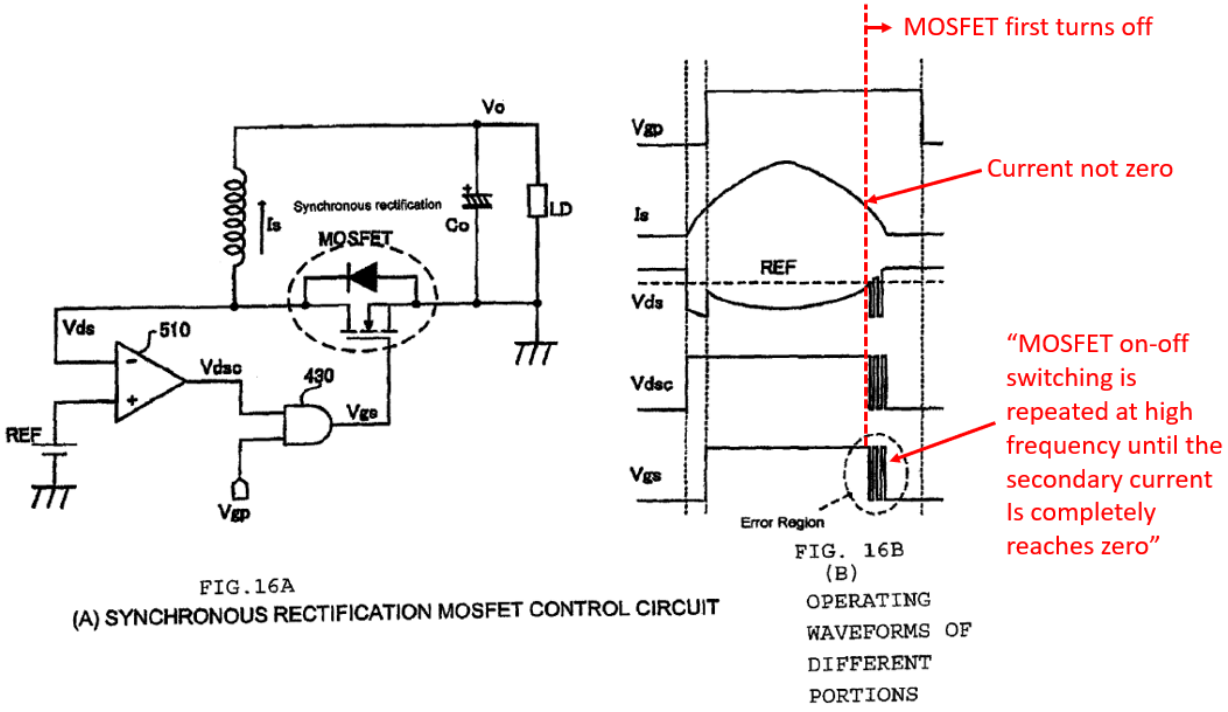
The combination also fails to teach or render obvious claim limitations 1[d] and 1[e], with respect to zero-voltage and zero-current switching on the primary-

and secondary-side switches. (Ex. 2001, ¶127).

The Petition begins under limitation 1[d] by asserting that "Chen discusses zero current switching on the secondary switches", citing Ex. 1010, 5:51-63. But the cited portion of Chen has been deceptively edited in the parenthetical following the citation to 5:51-63. (Ex. 2001, ¶128). Shown side-by-side below are the Petition's parenthetical characterization of Chen 5:51-63 on the left, and the actual text on the right:

"Ex. 1010, 5:51-63 ("When the secondary current Is decreases and becomes zero . . . Then, the comparison signal Vdsc is inverted, the MOSFET is turned off . . . . By this means, the comparison signal Vdsc is again inverted, the MOSFET is again turned on . . . .")."	"However, as shown in FIG. 16B, when the secondary current Is decreases and becomes zero, no matter how low the value of the reference voltage REF, the production of the MOSFET on-state resistance and the flowing current will at some time become smaller. Then, the comparison signal Vdsc is inverted, the MOSFET is turned off, and a state ensues in which current flows in the body diode, so that the drain-source Voltage Vds becomes -V. By this mean the comparison signal Vdsc is again inverted, the MOSFET is again turned on, and as a result the comparison signal Vdsc is inverted yet again. Thereafter, as indicated by the error region in FIG. 16B, MOSFET on-off switching is repeated at high frequency until the secondary current Is completely reaches zero."
(Petition, p. 61)	(Chen, Ex. 1010, 5:51-63).

The Petition's edit to this portion of Chen makes it seem as though a MOSFET is turned off "when the secondary current Is decreases and becomes zero". (Petition, p. 61). In fact, however, the passage indicates that the MOSFET is turned ON and OFF repeatedly *while secondary current is flowing*. (Ex. 1010, 5:51-63)("Thereafter, as indicated by the error region in FIG. 16B, MOSFET on-off switching is repeated at high frequency until the secondary current Is completely reaches zero.")(Ex. 2001, ¶129). This is clearly visible in referenced Fig. 16B of Chen, reproduced below with added red arrows and labels:



(Ex. 1010, Fig. 16B, 5:51-63)(Ex. 2001, ¶129).

The operation of this circuit, where the MOSFET synchronous rectifiers are repeatedly turned ON and OFF while there is current flowing teaches away from the

invention. (Ex. 2001, ¶130). The point of ZCS operation is to avoid current flowing in the MOSFET channel during switch transitions. (Ex. 2001, ¶130). This is because during switch transitions, the channel resistance is low enough that current can flow, but much higher than when the MOSFET is fully ON. (Ex. 2001, ¶130). This leads to high losses. (Ex. 2001, ¶130). Causing the secondary-side MOSFET to turn ON and OFF in rapid succession while secondary-side current is flowing is contrary to ZCS. (Ex. 2001, ¶130).

Even if the passage of Chen on which the Petition relies had not been edited to portray the opposite of what it actually says, it suffers from two other issues. First, the cited portion of Chen is talking about a *secondary*-side switch, not *primary*-side switches as required by limitation 1[d]. (Ex. 2001, ¶131). Second, the cited portion of Chen is in Chen's Background section, referring to *the prior art to Chen* (Ex. 1010, 5:11-16), and the Petition does not explain how the teachings in Chen's Background relate to the circuit on which the Ground otherwise relies, namely that of Fig. 1 of Chen. (Petition, pp. 59-60)(Ex. 2001, ¶131).

The Petition provides no other analysis for limitations 1[d] and 1[e], instead merely relying on its stock language for combination with the AAPA. But as discussed above in §III.C, beginning on page 40, there was no reason to expect success in modifying Chen, nor any particular motivation to do so. (Ex. 2001, ¶132). With specific regard to Chen, Chen's converter performs regulation using frequency

modulation (Ex. 1010, 3:1-5, 3:38-40, 9:63-10:3), contrary to the operation of the AAPA, and the Petition makes no argument for how Chen's circuit would change, what the impact of those changes would be, and why that would be obvious or be expected to be successful.

3. Limitation 1[f] "oscillator frequency is preset"

The combination further does not teach or render obvious that the "oscillator frequency is preset". As discussed above under limitation 1[c], Chen uses a voltage-controlled oscillator, varying the oscillator frequency to regulate the output. (Ex. 1010, 3:1-5, 3:38-40, 9:63-10:3)(Ex. 2001, ¶133).

Ground III thus does not satisfy the Petitioner's burden.

F. Ground IV (Obviousness over Pan in view of TI UCD3138 (or, in the alternative, TI UCD3040) and AAPA) does not meet the Petitioner's burden

Ground IV (obviousness over Pan in view of TI UCD3138 (or, in the alternative, TI UCD3040) and AAPA) does not meet the Petitioner's burden. The lack of a proper motivation and reasonable expectation of success is particularly egregious with respect to this Ground, and—as with the other Grounds—the combination does not meet several elements of the claims. (Ex. 2001, ¶135).

1. There was no motivation or reasonable expectation of success to combine with AAPA

A PHOSITA would not have had a reasonable expectation of success or motivation to combine Pan with the AAPA for the reasons discussed above in §III.C,

beginning on page 40. (Ex. 2001, ¶136).

Furthermore, the modification with the AAPA is particularly inappropriate for Pan. (Ex. 2001, ¶137). While it is difficult to understand in any of these Grounds exactly how the Petition proposes to change the primary reference based on the AAPA, and how any such unknown change would affect the primary reference, with Pan, it *is* possible to determine that *any combination* with AAPA would be contrary to Pan's principle of operation. (Ex. 2001, ¶137). *See Ratti*, 270 F.2d at 813.

The basic reason for this is that Pan *intentionally* sacrifices ZVS / ZCS on the secondary side in order to achieve a faster transient response. (Ex. 1011, p. 1)(Ex. 2001, ¶138). This requires a little bit of background. As Pan states in its introduction:

> "To decrease power consumption and increase the speed, the next generation of computer microprocessors will operate at significantly lower voltages and higher currents than today's generation. Recently, the supply voltage is reduced to around 1V, which was 5V or 3.3V five or ten years ago. It is expected that in future the supply voltage is going to drop to a level of 0.8V or lower. Future processors will require more than 200A current at the voltage of about 0.8V and needs up to around 120A/ns current transient speed. This makes it much more difficult to maintain an accurate voltage regulation within tight tolerance range for voltage regulator modules (VRM). [1]- [3]"

(Ex. 1011, p. 1, left column)(Ex. 2001, ¶138). Here, Pan notes that future microprocessors will require power converters to deliver more power at "up to around 120A/ns current transient speed". (*Id.*). This means that microprocessors are expected to change their power demands quickly, for example, when they go from a "sleep" state to a high-power state. (Ex. 2001, ¶138). The power converter needs to be able to provide the required power quickly (*e.g.* 120 additional Amperes within one nanosecond). (Ex. 1011, p. 1, left column)(Ex. 2001, ¶138).

Pan teaches that certain prior converters were limited in their transient response. (Ex. 1011, p. 1, right column)(Ex. 2001, ¶139). In order to speed up transient response, Pan provides a converter that employs secondary-side regulation. (Ex. 2001, ¶139). As Pan states:

> "To further improve current transient speed, the secondary side control (control synchronous rectifiers) is proposed."

(Ex. 1011, p. 1, right column)(Ex. 2001, ¶139). When Pan says "control" here, it means control (regulation) of the output voltage against variations in input voltage and load current. (Ex. 1011, p. 1)(Ex. 2001, ¶139). When Pan proposes "the secondary side control", Pan means that the circuit will change how the secondary-side MOSFETs (also called "synchronous rectifiers") switch, in order to control the

output voltage.[6] (Ex. 2001, ¶139).

Pan teaches to do this in two different ways, both of which are incompatible with ZVS and ZCS on the secondary side. (Ex. 2001, ¶140). First, Pan states that "[t]he synchronous MOSFETs are fully turned on at full load, while they are **partly turned on at reduced load**. **Such an output regulation mode may cause efficiency impairment** somewhat at reduced load." (Ex. 1011, p. 1, left column, bottom)(Emphasis added)(Ex. 2001, ¶140). This means that Pan is, in part, regulating the output voltage by only partially turning ON the synchronous rectifiers (secondary MOSFETs). When a MOSFET is fully OFF, it has very high resistance, and basically no current flows through its channel. (Ex. 2001, ¶140). When a MOSFET is fully ON, it has very low resistance, and current can flow through it essentially without resistive losses. (Ex. 2001, ¶140). When a MOSFET is "partly turned on", however, its resistance is somewhere between very high and very low, because its gate voltage holds it in what would otherwise be a transitional state. (Ex. 2001, ¶140). This means that current can flow through it, subject to resistive losses, causing a drop in voltage and conversion of power to heat, in a manner that decreases efficiency. (Ex. 2001, ¶140). Pan acknowledges this, stating, "Such an output

[6] Pan also proposes using primary-side control together with secondary-side control. (Ex. 1011, p. 1)(Ex. 2001, ¶139).

regulation mode may cause efficiency impairment." (Ex. 1011, p. 1, left column, bottom)(Ex. 2001, ¶140). This form of regulation is incompatible with ZVS and ZCS, because Pan is intentionally holding the transistor in a switching state between ON and OFF such that current flows through the channel in a resistive state. (Ex. 2001, ¶140).

Second, Pan teaches to use the difference between the MOSFET ON-state resistance and the body diode forward-voltage drop to effect regulation. (Ex. 1011, p. 1, right column)(Ex. 2001, ¶141). Pan explains:

> "To further improve current transient speed, the secondary side control (control synchronous rectifiers) is proposed. Thanks to t**he difference between diode forward voltage (V_d) and synchronous MOSFET on-state voltage**, controlling the duty cycle of the rectifier switches will control AC equivalent resistance, then will obtain output voltage regulation."

(Ex. 1011, p. 1, right column)(Emphasis added)(Ex. 2001, ¶141).

What does this mean? These secondary-side MOSFETs (the "synchronous MOSFETs in the quote above) are in the secondary side return current path. (Ex. 2001, ¶142). For part of the switching cycle, a MOSFET is ON or partly ON, and return current flows through the channel of the MOSFET, which has a certain resistance. (Ex. 2001, ¶142). For another part of the cycle, however, the MOSFET is turned OFF, and return current flows through the body diode of the MOSFET.

(Ex. 2001, ¶142). The body diode has a forward voltage drop when current flows through it. (Ex. 2001, ¶142). Thus, a voltage drop is selectively applied across the MOSFET as it conducts current in its OFF state. (Ex. 2001, ¶142).

Pan uses the difference between the voltage drop of the MOSFET channel (when the MOSFET is ON or partly ON) and the voltage drop of the diode (when the MOSFET is OFF) to regulate the output. (Ex. 1011, p. 1, right column, 3rd full paragraph)(Ex. 2001, ¶143). To do so, Pan varies the time within each cycle that the MOSFET is turned ON (by using PWM or "Pulse-Width Modulation"), thereby increasing or decreasing the average voltage drop across the MOSFET while it is conducting current. (Ex. 2001, ¶143). This changes the output voltage. (Ex. 2001, ¶143). As a consequence of this mode of operation, however, the MOSFET dissipates power when it turns ON (because of the diode voltage drop), and when it turns OFF (while carrying current). (Ex. 2001, ¶143).

This can be seen in the Pan's explanation accompanying Figs. 1-3. (Ex. 1011, pp. 2-3)(Ex. 2001, ¶144). As Pan states, during the interval t0-t1, "M_1 is on and M_2 is off S_1 and S_2 are off." Since M represents a primary-side MOSFET and S represents a secondary-side MOSFET, in the interval t0-t1 both secondary-side MOSFETs are OFF. (Ex. 1011, p. 2, right column)(Ex. 2001, ¶144). Current can still flow in the secondary side, however, because "Current i_{sc} goes through the body diode of S_2." (*Id.*). This means that at the end of a time interval (t0-t1), current

flowing in the S_2 leg of the secondary circuit would switch to the S_2 channel when it turns ON. (Ex. 2001, ¶144). During the following time interval (the interval t1-t2), with S_2 ON, current flows in that circuit leg through the S_2 channel. (Ex. 1011, p. 2, right column)(Ex. 2001, ¶144). Pan describes similar operation for S_1 during the intervals t4-t5 and t5-t6. (Ex. 1011, p. 3, left column, top)(Ex. 2001, ¶144). Thus, Pan is selectively switching its secondary-side transistors, selectively channeling current through their body diodes to speed up transient response time. (Ex. 1011, p. 1, right column)(Ex. 2001, ¶144).

To change the control methodology of the secondary switches of Pan in an attempt to provide ZVS or ZCS would fundamentally conflict with the principle of operation of Pan. (Ex. 2001, ¶145). Pan would no longer be able to operate secondary-side switches in a "partly on" state, nor exploit the difference in voltage drop between the MOSFET channel and the diode to achieve secondary-side regulation and thus a faster transient response. (Ex. 2001, ¶145). *See In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984)(Not obvious to change reference making it "inoperable for its intended purpose"). The Petition provides no reason to modify Pan in this manner to remove its ability to regulate the output.

The Petition also includes two sentences at the end of the introduction to Ground IV, which state:

"TI UCD3138 also relates to resonant converters and contemplates

> zero current and zero voltage switching by referencing 'LLC and phase shifted full bridge mode switching.' Ex. 1006, 7. Similarly, TI UCD3040 discusses resonant LLC converters and contemplates zero current and zero voltage switching. Ex. 1018, 2; Ex. 1003, ¶ 151."

(Petition, p. 67-68). The cited pages of Exs. 1006 and 1018, however, do not discuss zero-voltage or zero-current switching. Each reference merely mentions various types of circuits that could be controlled using TI chips. The proposition that "LLC and phase shifted full bridge mode switching" means that the reference "contemplates zero current and zero voltage switching" is misleading, as the earlier discussion with respect to McDonald (*see* §§III.B.2 and III.B.3, pp. 33-40) illustrates. (Ex. 2001, ¶146).

2. Limitation 1[c]—"standard converter operating cycle, having a standard operating period and frequency"

The Petition does not carry its burden with respect to the portion of limitation 1[c] requiring a "standard converter operating cycle, having a standard operating period and frequency". (Ex. 2001, ¶147). With respect to this limitation, the Petition only states "[t]he converter in Pan inherently operates at the resonant period and frequency to achieve ZVS and ZCS. Ex. 1003, ¶ 160." (Petition, p. 73). In the cited portion of his testimony, Dr. Hopkins states:

> "A POSITA would understand that in Pan the converter operating cycle would have a standard operating period and frequency, which is the resonant period and frequency of the resonant converter,

because Pan discusses achieving ZVS, and this requires a resonant frequency."

(Ex. 1003, ¶160).

The Petition and Dr. Hopkins are wrong. First, the Petition argues that "the converter in Pan inherently operates at the resonant frequency." This is plainly incorrect: Pan defines a ratio, ω, of the operating frequency, which it calls ω_o, to the resonant frequency, which it calls ω_r, such that $\omega = \frac{\omega_o}{\omega_r}$. (Ex. 1011, p. 4, left column, middle)(Ex. 2001, ¶148). Pan then teaches that "lower ω (ω > 1) will help achieve good controls over the whole load range and higher ω may cause losing controls at light load." (Ex. 1011, p. 5, left column, middle)(Ex. 2001, ¶148). In Pan's analysis, he uses an example design with ω=1.1:

> "For example, a design is assumed as follow: Vg=12V, Vo=1V, Vd=0.8V, Io=0~20A, fs=2.5MHz. If choosing Qo=1.5 and **ω =1.1**, it can be determined that n=5.5, Ls=130nH, Cs=38nF."

(Ex. 1011, p. 5, left column, middle)(Emphasis added)(Ex. 2001, ¶148).

When Pan teaches to use ω (the ratio of the operating frequency to the resonant frequency) of greater than 1, it means that the operating frequency is not the resonant frequency, contradicting the Petition's assertion. (Ex. 2001, ¶149).

Dr. Hopkins' testimony does not address this problem. Dr. Hopkins repeats

the Petition's mistake of asserting that the operating frequency is the resonant frequency. He testifies that this is "because Pan discusses achieving ZVS, and this requires a resonant frequency." (Ex. 1003, ¶160). This testimony, however, conflates the operating frequency with the resonant frequency. (Ex. 2001, ¶150). The resonant frequency is set by inductive and capacitive elements in the system. (Ex. 2001, ¶150). The operating frequency, in contrast, is the frequency at which the device operates. (Ex. 2001, ¶150). And as Pan clearly states, the two are not the same. (Ex. 1011, pp. 4-5)(Ex. 2001, ¶150). Thus, the Petition's inherency argument fails.

3. Limitation 1[d]—ZVS and ZCS for primary-side switches

The Petition also does not carry its burden with respect to limitation 1[d]. Pan clearly shows that its primary-side switches do not switch when "essentially zero resonant current is flowing in the respective at least one primary switch". (Ex. 2001, ¶151).

This can be seen directly from the waveforms in Fig. 2 of Pan, reproduced here:

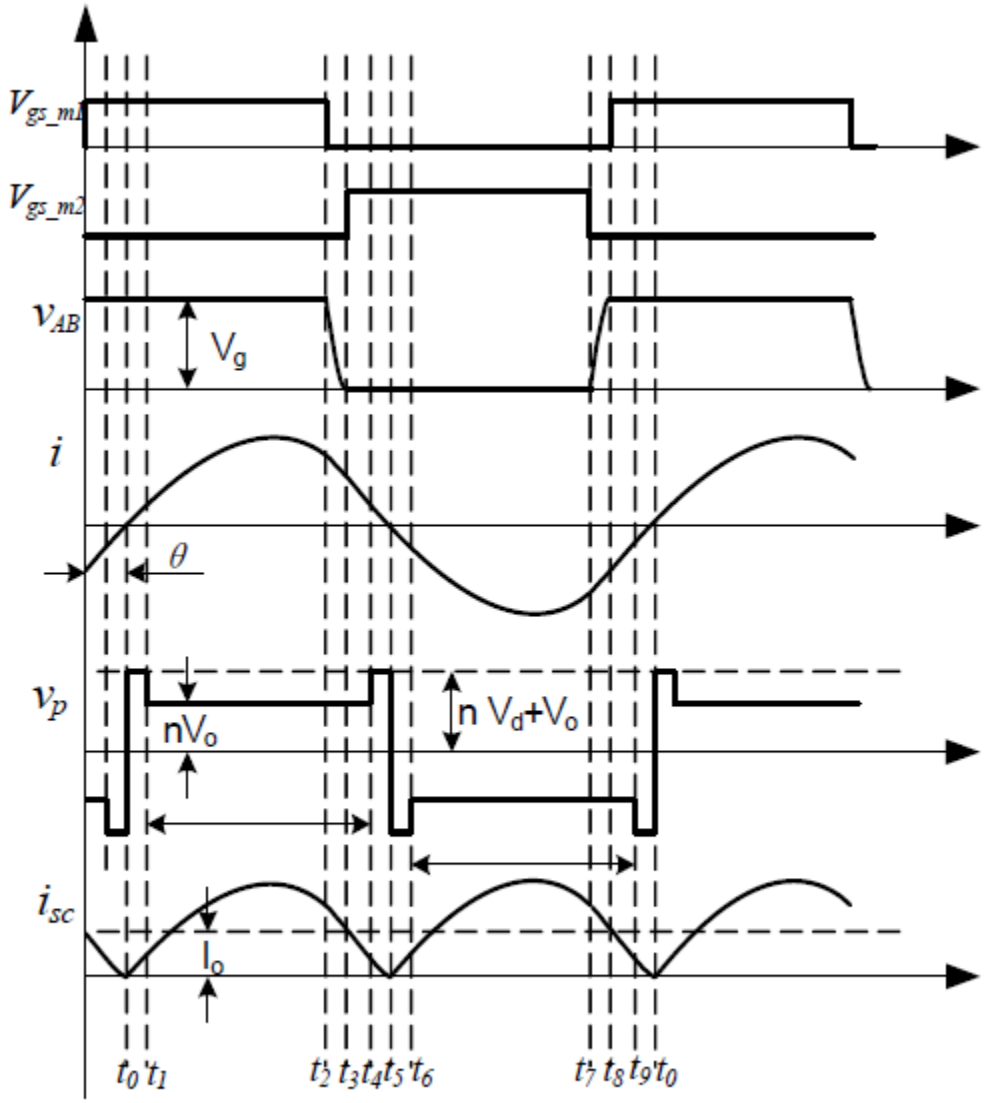


Figure 2. The typical steady state operating waveforms

(Ex. 1011, p. 2). In the figure, the resonant current is the waveform labeled 'i'. (Ex. 1011, p. 2, right column, top)("the resonant current i"). The waveforms V_{gs_m1} and V_{gs_m2} represent the gate-drive waveforms of the primary-side MOSFET switches. (Ex. 2001, ¶152). It can clearly be seen that the times when the resonant current crosses zero (times t0 and t5) are not the switching times (t2', t3, t7', and t8). (Ex.

2001, ¶152). Consistent with this observation, Pan only states that it achieves ZVS (**not ZCS**) for switches M1 and M2. (Ex. 1011, p. 2, right column, middle)(Ex. 2001, ¶152).

The combination with the AAPA, in turn, fails for the reasons provided above in §III.E.1, beginning on page 55.

4. Limitation 1[e]—ZVS and ZCS for secondary-side switches

With respect to limitation 1[e], as discussed above in §III.E.1, beginning on page 55, Pan cannot use, and it would not have been obvious to use, secondary-side ZVS and ZCS. (Ex. 2001, ¶154).

5. Limitation 1[f]—"wherein the oscillator frequency is preset"

The Petition does not carry its burden with respect to limitation 1[f], for the same reasons discussed above with respect to TI UCD3138 (or, in the alternative, TI UCD3040) under §III.B.4, beginning at p. 40). (Ex. 2001, ¶155).

Ground IV thus does not satisfy the Petitioner's burden.

G. Ground V (Obviousness over Peng in view of TI UCD3138 (or, in the alternative, TI UCD3040) and AAPA) does not meet the Petitioner's burden

Ground V (obviousness over Peng in view of TI UCD3138 (or, in the alternative, TI UCD3040) and AAPA) does not meet the Petitioner's burden. The lack of a proper motivation and reasonable expectation of success is again particularly egregious with respect to this Ground, and the combination does not meet several elements of the claims. (Ex. 2001, ¶157).

1. There was no motivation or reasonable expectation of success to combine with AAPA

A PHOSITA would not have had a reasonable expectation of success or motivation to combine Peng with the AAPA for the reasons discussed above in §III.C, beginning on page 40. (Ex. 2001, ¶158).

With regard to Peng in particular, the combination would have been contrary to Peng's principle of operation. Peng is a bi-directional converter that converts power between two different batteries in a hybrid vehicle system. (Ex. 1012, Abstract). To support bi-directional operation, Peng causes switching to occur on only one side of the transformer (either only the primary side or only the secondary side) at a time. (Ex. 1012, 16:64-17:5, Figs. 14-21)(Ex. 2001, ¶159).

To illustrate this, consider the embodiment relied on in the Petition, Fig. 6. This figure shows a converter whose operation is explained with reference to Figs. 14-21. (Ex. 1012, 8:59-9:16, 18:18-24)(Ex. 2001, ¶160). As shown in each of Figs. 14-21, the respective secondary-side switches are simply OFF (held open) during power flow from the primary to the secondary side. (Ex. 1012, 16:64-17:5, Figs. 14-21). Figures 14-21 of Peng show a full cycle, beginning at time t1 through time t9, and then back to time t1. (Ex. 1012, 18:21)(Ex. 2001, ¶160). In every time interval, the secondary-sides switches S3 and S4 are OFF when the power is flowing from left to right, as can be seen in the bottom right of every figure. An example (Fig. 14) is provided below, with the labels for S3 and S4 shown with added highlighting:

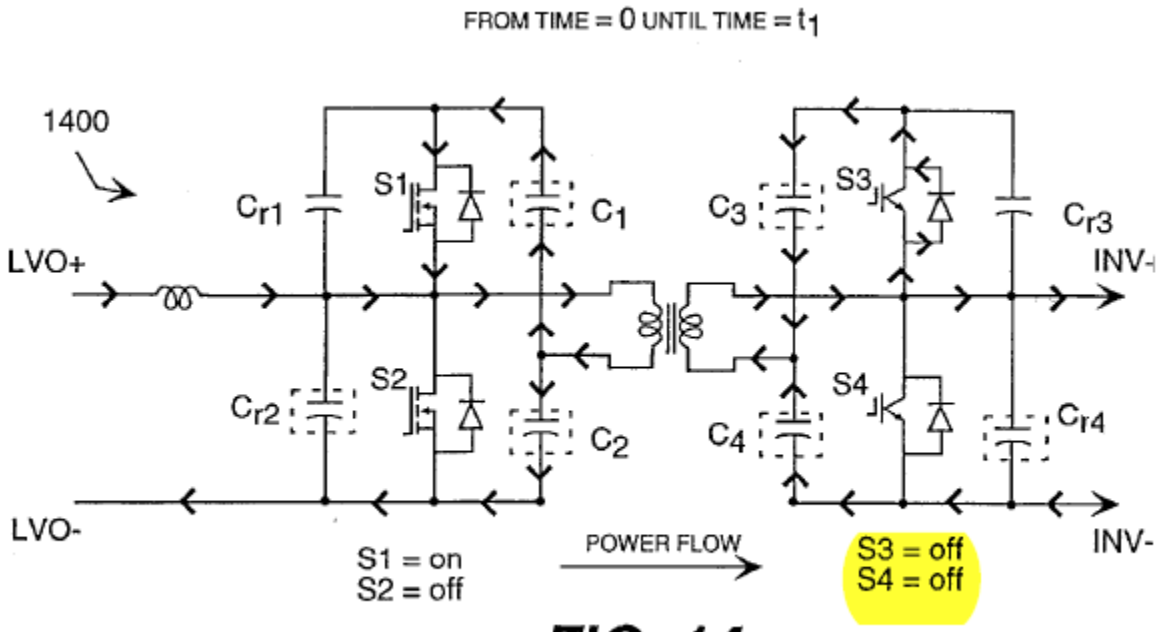


FIG. 14

(Ex. 1012, Fig. 14)(Ex. 2001, ¶160). Because certain switches are being held OFF, those switches are *not* being turned ON and OFF. (Ex. 2001, ¶160). Simply put, Peng holds OFF half of its switches while operating in either forward or reverse mode. (Ex. 2001, ¶160).

Peng explains that the power flow of the Fig. 6 circuit is reversible, and that power flows to the side where the switches are held OFF:

> "**for power flow from the primary to the secondary**, S1 and S2 are gated with **S3 and S4 held open**. The same gating sequence may be used for S3 and S4, with **S1 and S2 held open**, to transmit power **from the secondary to the primary**."

(Ex. 1012, 20:24-27)(Emphasis added)(Ex. 2001, ¶161). When the switches are open (OFF), the diodes perform the rectification function. (Ex. 2001, ¶161).

Given the operation of Peng, it would not have been obvious to modify Peng using the AAPA, because a PHOSITA would have been required to have both the primary- and secondary-side switches turning ON and OFF in a standard operating cycle. (Ex. 2001, ¶162). In contrast, to support bi-directional operation, Peng causes switching to occur on only one side of the transformer (either only the primary side or only the secondary side) in either of its bidirectional modes. (Ex. 2001, ¶162). *See Ratti*, 270 F.2d at 813.

2. Limitation 1[c]—"standard converter operating cycle, having a standard operating period and frequency"

The Petition does not carry its burden for limitation 1[c]. The Petition makes a one-sentence argument, in a manner nearly identical to the argument under Ground IV with Pan, that operation at resonant frequency is "inherent" to perform ZCS and ZVS. (Petition, p. 99). Dr. Hopkins provides an explanation nearly identical to the explanation for under Ground IV with Pan. (*Compare* Ex. 1003, ¶¶160 and 202).

The Petition's reasoning is insufficient. The Petition does not even make an argument to support its bare assertion of inherency, and Dr. Hopkins' reasoning is incorrect for the same reasons provided above under §III.F.2, beginning on p. 68. (Ex. 2001, ¶164).

Furthermore, as will be described below, Peng does not achieve ZVS and ZCS, but rather only ZVS for some switches under some circumstances. (Ex. 2001, ¶165). The Petition's factual predicate to inherency is thus also incorrect. (Ex. 2001,

¶165).

3. Limitations 1[c], 1[d], and 1[e]—"generating timing control signals…in a (A) standard converter operating cycle…to:…(ii) turn the at least one secondary switch ON and OFF"

The Petition does not carry its burden with respect to limitations 1[c], 1[d], and 1[e]. These limitations require the converter to generate timing control signals in a standard converter operating cycle to (limitation 1[c]) turn both the at least one primary switch ON and OFF (limitation 1[d]) and at least one secondary switch ON and OFF (limitation 1[e]). Peng does not teach or render obvious this claimed feature, because (as discussed above under §III.G.1 beginning on page 72) in Peng either the primary or secondary-side switches are held open (OFF). (Ex. 2001, ¶166). Thus, regardless of which direction power is flowing, switches on the primary or secondary side of the transformer are held open (OFF) during a converter's operating cycle, and Peng cannot meet each of limitations 1[c], 1[d], and 1[e]. (Ex. 2001, ¶166).

4. Limitations 1[d] and 1[e]—ZVS and ZCS operation

The Petition also does not carry its burden with respect to the ZVS / ZCS portions of limitations 1[d] and 1[e]. As discussed immediately above, in either forward or reverse mode, either all of the primary or all of the secondary-side switches are held OFF. (Ex. 2001, ¶167).

The Petition relies on Peng's statement that "[t]he switches S1 and S2 are

zero-voltage turn-off and zero-current zero-voltage turn on." (Petition, p. 99)(*citing* Ex. 1012, 16:27-29). This, however, teaches away from turning "the at least one primary switch ON *and* OFF at times when…essentially zero resonant current is flowing in the respective at least one primary switch", because Peng excludes turning the switch OFF at zero current. (Ex. 2001, ¶168).

Peng's operation can be seen clearly in Fig. 13, which is a waveform diagram for the circuit of Fig. 6. (Ex. 1012, 18:14-15)(Ex. 2001, ¶169). Figure 13 is reproduced below, with added red-dashed boxes around the label for the resonant current ("Ir1", 18:20-25) and the times at which S1 and S2 are turned OFF:

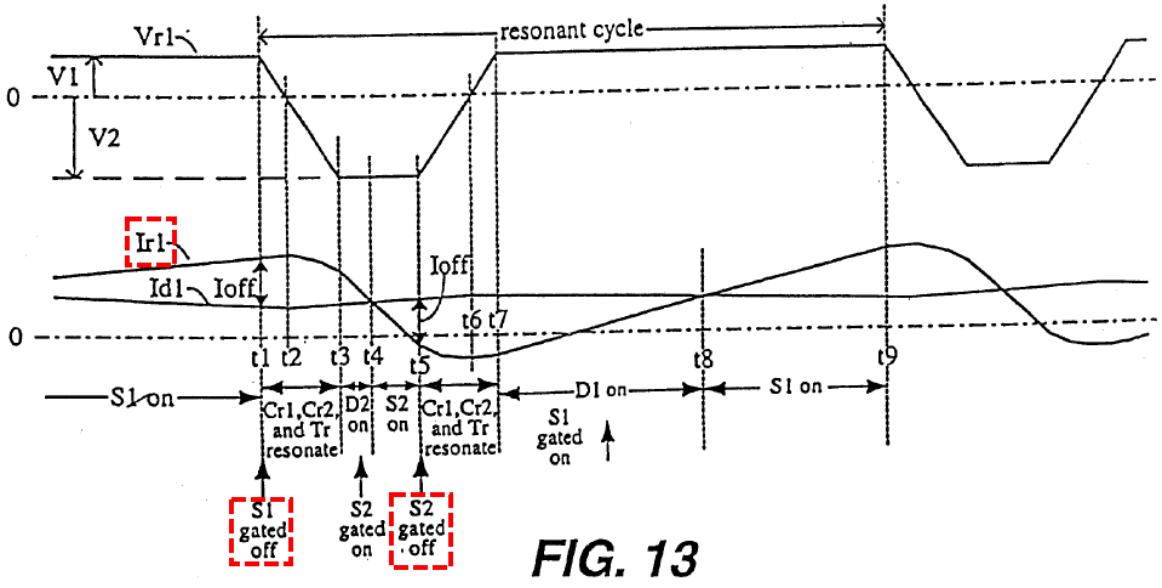


FIG. 13

(Ex. 1012, Fig. 13)(Ex. 2001, ¶169). As can be seen from the figure, resonant current is flowing at the time S1 and S2 are turned OFF (and also when S2 is turned ON). (Ex. 2001, ¶169).

5. Limitation 1[f]—"wherein oscillator frequency is preset"

The Petition does not carry its burden with respect to limitation 1[f], for the same reasons discussed above with respect to TI UCD3138 (or, in the alternative, TI UCD3040) under §III.B.4, beginning at p. 40). (Ex. 2001, ¶170).

Ground V thus does not satisfy the Petitioner's burden.

H. Ground VI (Obviousness over Leung in view of AAPA) does not meet the Petitioner's burden

Ground VI (obviousness over Leung in view of AAPA) does not meet the Petitioner's burden. There would have been no motivation or reasonable expectation of success, and the combination does not meet several elements of the claims. (Ex. 2001, ¶172).

1. There was no motivation or reasonable expectation of success to combine with AAPA

A PHOSITA would not have had a reasonable expectation of success or motivation to combine Leung with the AAPA for the reasons discussed above in §III.C, beginning on page 40. (Ex. 2001, ¶173).

2. Limitation 1[a]—"operating a power converter in a series of converter operating cycles the converter having at least one primary switch to drive a resonant power train and at least one secondary switch, the resonant power train including a transformer and having a characteristic resonant frequency and period"

The Petition does not carry its burden with respect to limitation 1[a] for at least two reasons. First, limitation 1[a] requires a "resonant power train". To address

this limitation, the Petition asserts *only* that:

> "a POSITA would have known that a resonant circuit could be added the Leung's half-bridge converter, which would provide a resonant frequency and period."

(Petition, p. 107).

This argument is pure hindsight. (Ex. 2001, ¶175). Adding a resonant power train, and making it work, is a major redesign effort. (Ex. 2001, ¶175). The Petition does not explain *how* or *why* to add a resonant power train to Leung. (Ex. 2001, ¶175). What would a PHOSITA change about Leung to add a resonant power train? How would any such modifications affect the operation of the circuit? Neither the Petition nor Dr. Hopkins answer any of these questions. The Petition also provides no motivation to "add" a "resonant circuit", does not assert that the change (whatever it is) would have predictable results, and does not assert a reasonable expectation of success. (Ex. 2001, ¶175).

Second, the Petition addresses limitation 1[c] by referring to the "buck converter 402". (Petition, pp. 109-110)(citing Ex. 1012, ¶¶0017-0072, Fig. 4). A Buck converter, however, does not have a transformer, which is required by limitation 1[a]. (Ex. 2001, ¶176). A Buck converter circuit is shown in Fig. 3 of Delta's U.S. Pat. No. 8,014,175. (Ex. 2005, 5:41-45)("the switching power conversion circuit 1 is a buck switching power conversion circuit…."). The buck

converter is shown here:

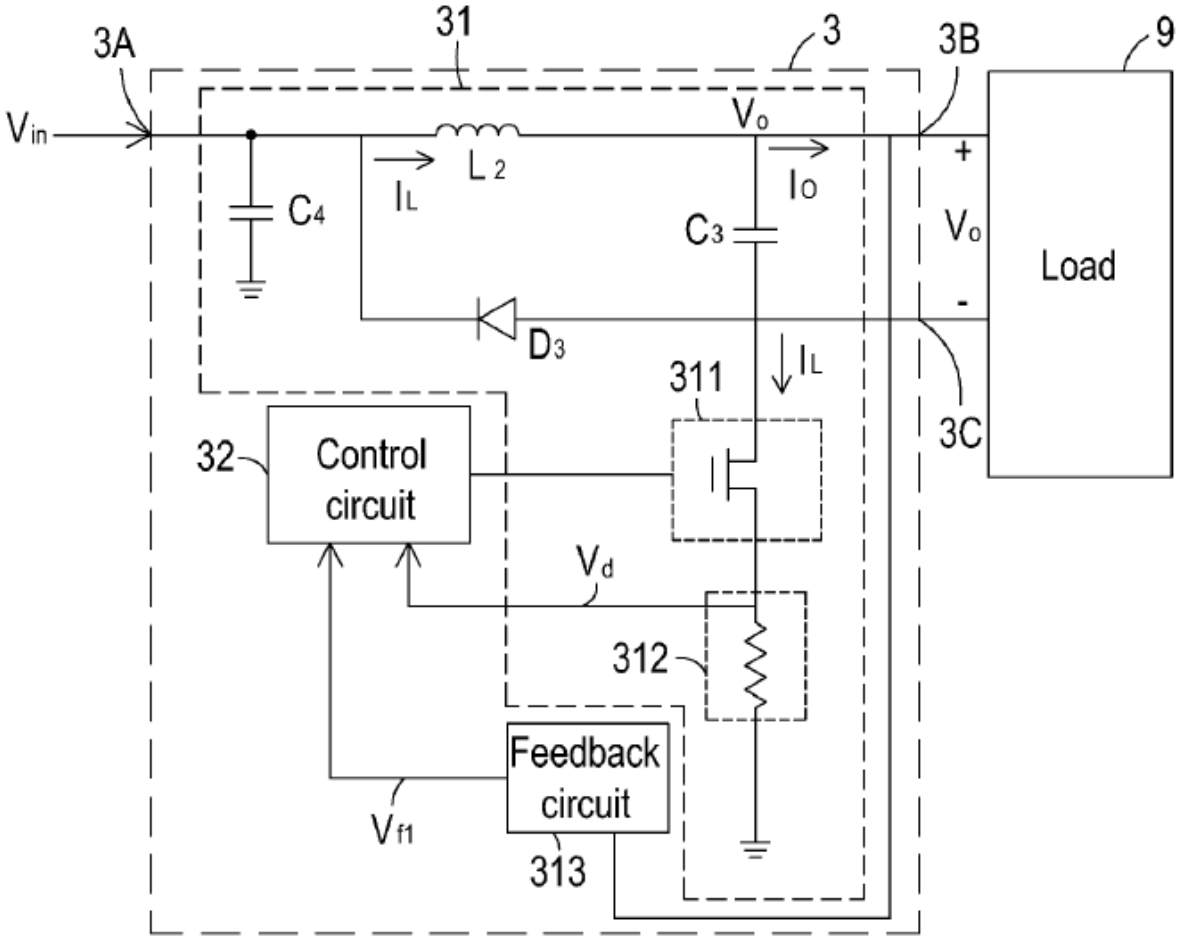


FIG. 3

(Ex. 2005, Fig. 3)(Ex. 2001, ¶176). As can be seen from the Figure, there is an inductor, L2, but there is no transformer. (Ex. 2001, ¶176).

Because a Buck converter has no transformer, and no boundary between primary and secondary sides, the mere disclosure of "buck converter 402" does not teach "at least one primary switch…and at least one secondary switch". (Ex. 2001, ¶177).

3. Limitation 1[c]—"generating timing control signals for each of a plurality of events based upon the clock signals in a (A) standard converter operating cycle, having a standard operating period and frequency, to:"

The Petition does not carry the Petitioner's burden with respect to limitation 1[c] for at least two reasons. First, the Petition relies on Leung at ¶0071-0072, specifically referencing "clock signals which provide the switching phases 404". (Petition, p. 109-110). This misses the mark, because the signals are provided to the Buck converter 402, not the converter of Fig. 2. (Ex. 2001, ¶178). The Petition does not even attempt to argue that it would have been obvious to connect any timing signals mentioned in 0071 and 0072 to the circuit of Fig. 2 in any particular way.

Second, with respect to the claimed "standard converter operating cycle, having a standard operating period and frequency", the Petition states *only* that "[t]he converter in Leung-AAPA inherently operates at the resonant period and frequency to achieve ZVS and ZCS." (Petition, p. 111). Dr. Hopkins provides an explanation nearly identical to the explanation for under Ground IV with Pan and Ground V with Peng (*compare* Ex. 1003, ¶¶160, 202, and 237).

The Petition and Dr. Hopkins are incorrect. (Ex. 2001, ¶180). First, the Petition is making an inherency-in-obviousness argument. That is, the Petition first argued (in a single sentence) that it would have been obvious to modify Leung's converter—in an undisclosed way—to contain a resonant circuit. (Petition, p. 107). From there, the Petition argues that the new, hypothetical circuit would have the

inherent property of operating "at the resonant period and frequency to achieve ZVS and ZCS." (Petition, p. 111). Note that this is not a case where a single reference teaches a claim limitation inherently, and then that reference is used in a combination. This is a case where Delta contends that a hypothetical circuit must first be constructed, and then, *only within that hypothetical circuit*, would an inherent property be found—whether the PHOSITA intended it or not. The Board should thus be cautious in the application of the doctrine of inherency to Leung. *See Par Pharmaceutical, Inc. v. TWi Pharmaceuticals, Inc.*, 773 F.3d 1186, 1195 (Fed. Cir. 2014)("We have, however, also explained that the use of inherency, a doctrine originally rooted in anticipation, must be carefully circumscribed in the context of obviousness.").

Here, the inherency case does not meet the Petitioner's burden. On the one hand, the Petition provides no explanation of why operation at the resonant frequency would be inherent in modified Leung. Indeed, providing such an explanation would have been a difficult task, because the Petition does not provide a proposal for the circuit of modified Leung. On the other hand, there are numerous examples, from the prior art cited in the Petition alone, of circuits that (1) are resonant circuits, but do not operate at the resonant frequency, and (2) achieve either ZVS or ZCS without operating at the resonant frequency. (Ex. 2001, ¶180). *See* discussions of McDonald (§III.B.2, beginning at p. 33, above), Shimada (§III.D.3,

beginning at p. 51), Pan (§III.F.2, beginning at p. 67), and the discussion of AN1336, below. There is simply no requirement that converters with a resonant circuit operate at the resonant frequency, or that achieving ZVS or ZCS under certain operating conditions for certain switches requires operation at the resonant frequency. (Ex. 2001, ¶180).

4. Limitations 1[d] and 1[e]

With respect to the ZVS and ZCS requirements of limitations 1[d] and 1[e], the Petition relies entirely on the AAPA, which cannot be combined with Leung for at least the reasons provided above in §III.C, beginning on page 40. (Ex. 2001, ¶181).

With further respect to Leung, it is not clear how ZVS and ZCS ever could be achieved in Leung's Fig. 2 circuit, because it is a pulse-width-modulated (PWM) circuit. (Ex. 1013, Fig. 3, ¶¶0068-0070)(Ex. 2001, ¶182). In a PWM circuit, the MOSFET switches are turned ON and OFF with varying durations (illustrated in Fig. 3 of Leung). (Ex. 2001, ¶182). By varying the durations of the ON and OFF times, the controller can regulate the output voltage. (Ex. 2001, ¶182). Because of this, however, switch transitions are controlled by feedback from the output voltage level, and are not controlled to provide ZVS and ZCS operation. (Ex. 2001, ¶182). The Petition provides no explanation of how a PHOSITA would have implemented ZVS and ZCS given the varying ON and OFF times of the switches. (Ex. 2001,

¶182).

Ground VI thus does not satisfy the Petitioner's burden.

I. Ground VII (Obviousness over AN1336 in view of dsPIC33FJ06GS101 and AAPA) does not meet the Petitioner's burden

Ground VII (obviousness over AN1336 in view of dsPIC33FJ06GS101 and AAPA) does not satisfy the Petitioner's burden because there was no motivation or reasonable expectation of success, and the combination does not meet several claim elements. (Ex. 2001, ¶184).

1. There was no motivation or reasonable expectation of success to combine with AAPA

A PHOSITA would not have had a reasonable expectation of success or motivation to combine AN1336 with dsPIC33FJ06GS101 and the AAPA for the reasons discussed above in §III.C, beginning on page 40. (Ex. 2001, ¶185).

2. Limitation 1[b]-1[e]—"providing an oscillator for generating clock signals at an oscillator frequency…generating timing control signals for each of a plurality of events based upon the clock signals…to:…turn the at least one primary switch ON and OFF…turn the at least one secondary switch ON and OFF"

The Petition does not carry the Petitioner's burden with respect to limitations 1[b]-1[e]. The Petition relies on two different oscillators ("an oscillator (OSC1 or OSC2") of dsPIC33FJ06GS101. (Petition, p. 116). However, the Petition never connects either of these oscillators to the timing control signals required by the claims. (Ex. 2001, ¶186). Nor is it a given that they would be used to control all

relevant switches: as discussed above in §III.C.3 beginning on p. 45, at the time of the invention certain prior art converters used analog circuitry to control the timing of gate switching. (Ex. 2001, ¶186).

3. Limitation 1[c]—"standard converter operating cycle, having a standard operating period and frequency"

The Petition does not carry the Petitioner's burden with respect to limitation 1[c]. Specifically, the converter in AN1336 does not operate with a "standard converter operating cycle, having a standard operating period and frequency". (Ex. 2001, ¶187).

As discussed above under §III.B.1, beginning at page 30, AN1336 is an LLC resonant converter that *varies* its frequency in order to regulate its output. (Ex. 1019, p. 4). AN1336, explains:

> "By modifying the switching frequency f_S, the gain of the LLC circuit is changed and therefore the output voltage can be controlled with varying load and input voltage."

(Ex. 1019, p. 1, left column)(Emphasis added)(Ex. 2001, ¶188). This is standard operation for LLC resonant converters, which exploit frequency-varying impedances to vary the output voltage. (Ex. 2001, ¶188).

AN1336 lays this out clearly on page 4 for LLC resonant converters:

"These converters are characterized by two operating frequencies:

1. the switching frequency, as imposed by the control electronics

(the frequency at which the MOSFETs are operated)

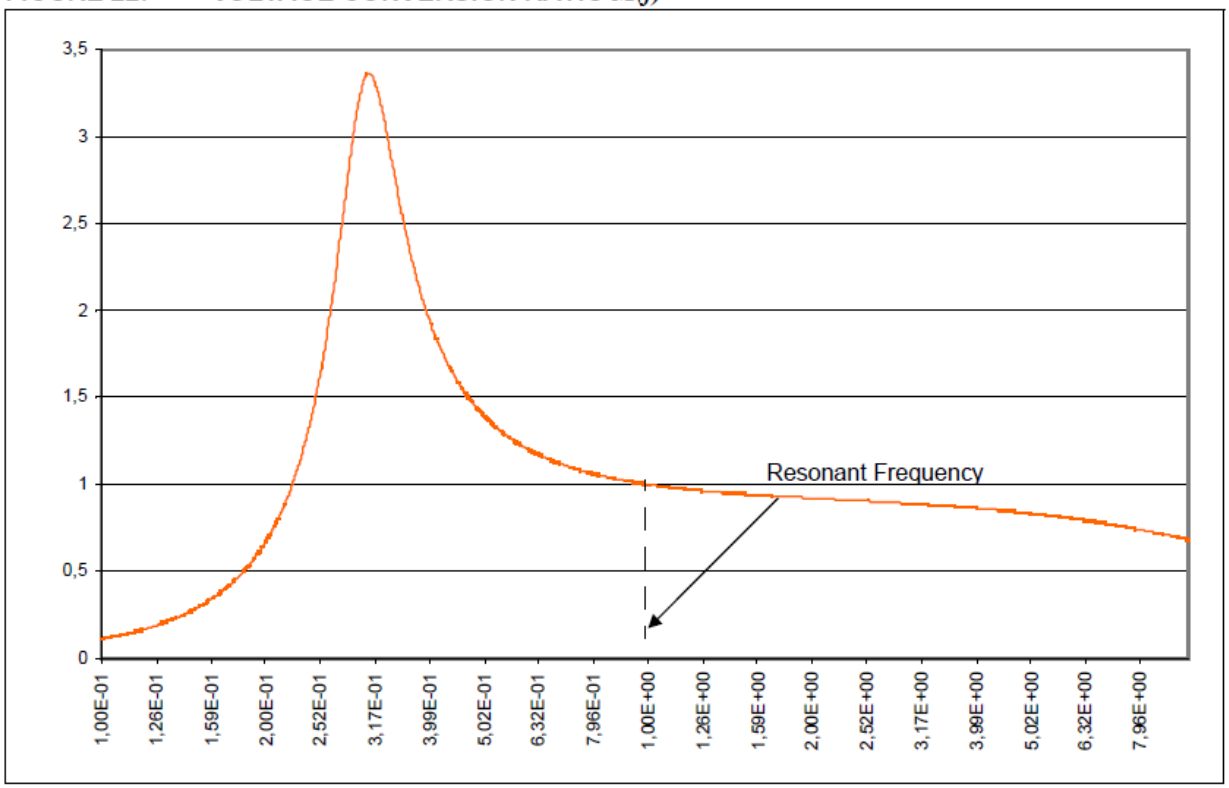
2. the natural resonant frequency of the tank
While the resonant frequency is fixed; as soon as the circuit components (capacitors, inductors and/or transformers) are selected, the switching frequency can be dynamically changed.

This is how the power transfer is managed and the output voltage is controlled, versus load and input voltage changes**. The relationship between the switching and resonant frequency translates into a voltage gain,** which is demonstrated in subsequent sections."

(Ex. 1019, p. 4, left column)(Emphasis added)(Ex. 2001, ¶189).

The voltage gain, also called the voltage conversion ratio, is shown in the graph versus switching frequency in Fig. 22, reproduced here:

FIGURE 22: VOLTAGE CONVERSION RATIO *M(f)*



(Ex. 1019, p. 19)(Ex. 2001, ¶190).

AN1336 states that it operates its circuit in ranges of the conversion ratio where the input appears inductive. (Ex. 1019, p. 25)("Instead, as stated above, **we operate the system in an area of its voltage conversion ratio M(f)** such that it appears to be inductive to the tank input current: that is, the current lags the voltage."). In the reference design, the desired range of operating frequencies is between a minimum of 155kHz and a maximum of 220 kHz:

> "First, the **minimum operating switching frequency** is determined by the intersection of the M(f) plot and the Mmax plot. The resulting value is **155 kHz**. Similarly, the **maximum switching frequency** is determined as the intersection of the M(f) plot and the Mmin plot.

The resulting value is **220 kHz**."

(Ex. 1019, p. 39)(Emphasis added)(Ex. 2001, ¶191).

Because the converter varies its frequency to regulate the output voltage, it does not have a "standard converter operating cycle, having a standard operating period and frequency", as required by limitation 1[c]. (Ex. 2001, ¶192).

The Petition asserts that "[t]he converter in AN1336 operates at a resonant frequency and period", quoting a sentence from page 28 of AN1336. (Petition, p. 118). Dr. Hopkins repeats this assertion verbatim in his declaration, with no further explanation. (Ex. 1003, ¶256).

As with McDonald, however, Delta is quoting the document out of context. On pages 28-34, AN1336 is engaging in another "piecewise" analysis of the mathematical behavior of the converter at a boundary point between its frequency operating ranges, namely frequencies at, below, and above resonance. (Ex. 1019, p. 33, headings)(Ex. 2001, ¶194)(*see also* the preceding section at Ex. 1019, p. 27)("Before going into greater detail regarding the **operation of the converter at, below, and above resonance**, it is useful to consider…."). AN1336 does not state that the converter is operated at the resonant frequency, which would preclude output voltage regulation. (Ex. 1019, p. 4)(Ex. 2001, ¶194).

4. Limitation 1[d] and 1[e]—ZVS/ZCS operation.

The Petition also does not carry the Petitioner's burden with respect to

limitations 1[d] and 1[e]. (Ex. 2001, ¶195).

Like McDonald, AN1336 is a type of LLC series resonant converter. Such converters (as discussed above in §III.B.2 and III.B.3, pp. 33-40) were known to be able—under certain operating conditions—to achieve ZVS (**but not ZCS**) for the primary-side switches and ZCS (**but not ZVS**) for the secondary-side switches. (See above, §III.B.2 and III.B.3, pp. 33-40)(Ex. 2001, ¶196).

For the claimed ZVS/ZCS operation, the Petition cites pages 59-61 of AN1336, as well as Figs. B-9 through B-11. (Petition, pp. 118-120). But these portions of AN1336 only show exactly what was expected, with careful design, from LLC series resonant converters: ZVS *but no ZCS* for primary-side switches, and ZCS *but no ZVS* for secondary-side switches. (Ex. 1019, pp. 59-61)(Ex. 2001, ¶197).

The Petition also provides its generic paragraph regarding obviousness of these limitations in view of the AAPA, which again fails for the reasons discussed above in §III.C, beginning on page 40. (Ex. 2001, ¶198).

Ground VII thus does not satisfy the Petitioner's burden.

J. Objective Evidence of Non-Obviousness

There are also strong objective indicia of non-obviousness, weighing against any finding of obviousness. *See Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1538 (Fed. Cir. 1983)("evidence of secondary considerations may often be the most probative and cogent evidence in the record.").

Delta was on notice of this evidence, but failed to meaningfully address it in the Petition. (Ex. 2025, ¶¶27-33, 56-60, 73-79). The Petition should be denied for that reason alone. *See Robert Bosch Tool Corp. v. SD3 LLC*, IPR2016-01751 (PTAB Mar. 22, 2017)(Paper 15)(denying institution for failure to address objective indicia presented during an ITC proceeding); *Stryker Corp. v. KFX Medical, Inc.*, IPR2019-00817 (PTAB September 16, 2019)(Paper 10)(denying Institution under §314(a) in part for failure to address known secondary considerations from litigation); *Coalition for Affordable Drugs V LLC v. Hoffman–LaRoche, Inc.*, IPR2015–01792 (PTAB Mar. 11, 2016)(Paper 14)(denying institution for failure to address objective indicia considered by Examiner during original prosecution); *Merial Ltd. v. Virbac*, IPR2014–01279 (PTAB Jan. 22, 2015)(Paper 13)(denying institution for failure to address objective indicia considered by Examiner during original prosecution and noting "Merial was aware of the unexpected results showing which the Examiner found persuasive . . . . Merial should have addressed unexpected results in the first instance."); *Omron Oilfield & Marine Inc. v. MD/TOTCO*, IPR2013–00265 (PTAB Oct. 31, 2013)(Paper 11)(denying institution for failure to address objective indicia successfully argued in a reexamination).

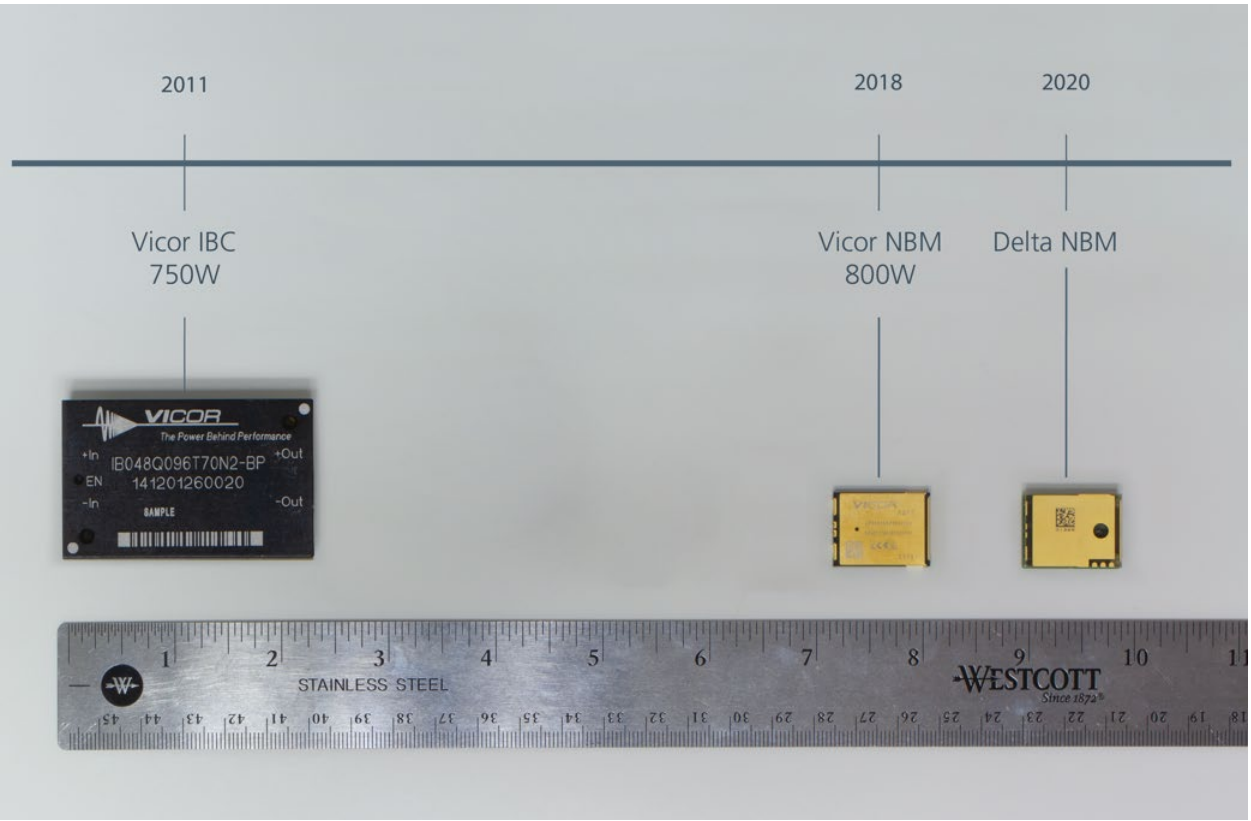
By developing the SAC controller of the '481 patent, the inventors proceeded contrary to the conventional wisdom. (Ex. 2030, ¶¶23-28). This is objective evidence of non-obviousness, and is demonstrated in the '481 patent and Ex. 1009

submitted with the Petition. *See Arkie Lures, Inc. v. Gene Larew Tackle*, 119 F.3d 953, 958 (Fed. Cir. 1997)("[C]onventional wisdom that a combination should not be made is evidence of unobviousness."); *Standard Oil Co. v. American Cyanamid Co.*, 774 F.2d 448, 454 (Fed. Cir. 1985)("A person of ordinary skill in the art is also presumed to be one who thinks along the line of conventional wisdom in the art….");

The claims of the '481 patent went contrary to the conventional wisdom because, as discussed above under §III.C.3, beginning on page 45, it was believed in the relevant timeframe that a Sine Amplitude Converter should use analog circuitry and closed loop control to correct against component variabilities and automatically cause ZCS/ZVS switch transitions, while recapturing and recycling the energy used to charge and discharge MOSFET gate capacitances. (Ex. 2030, ¶¶23-28)(Ex. 1009, 21:52-22:8)(Ex. 1001, 2:13-22). The '481 patent, however, departed from the prior-art by teaching a digital SAC controller using a clock and independently pre-set events to control a SAC to achieve ZCS and ZVS at a standard operating frequency and period. (Ex. 2030, ¶¶23-28).

As the first-named inventor on the '481 patent, Dr. Patrizio Vinciarelli, explains, Vicor released its first Non-isolated Bus Modules (NBMs) incorporating the '481 patent in 2017. (Ex. 2030, ¶¶32-35). The products offered a ten-fold advantage in power density over Vicor's prior generation of products. (Ex. 2030,

¶¶32-35). The improvement in power density can be seen in the following image showing, to scale, the relative dimensions of Vicor's prior bus converter product (2012) on the left, Vicor's NBM 2317 (2018) in the middle, and on the right, a similar product introduced by Delta in 2020, with added annotations at the top:

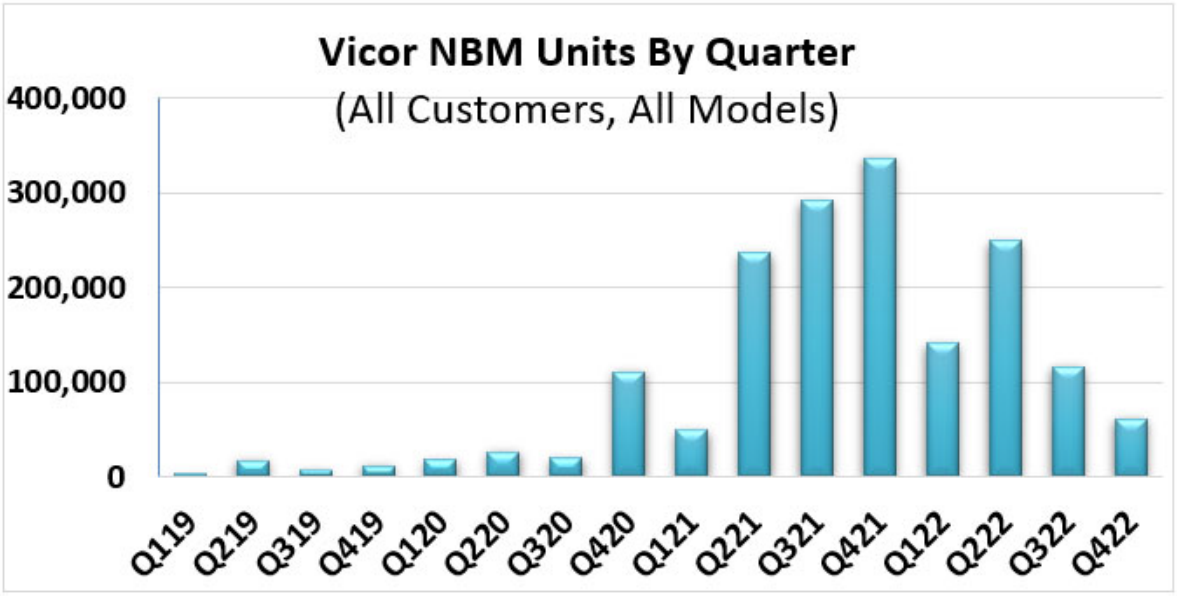


The 2011 converter shown on the left had a maximum power capacity of 750 W in a volume of 1.40 in^3 (2.30 x 1.45 x 0.42in), for a power density of 535 W/in^3. (Ex. 2030, ¶¶16-17). Such a converter would take up an area of 3.3 square inches on a mother board. (Ex. 2030, ¶17). Vicor's 2018 NBM2317, in contrast, processed 800 W within a volume of 0.12 in^3 (0.90 x 0.68 x 0.20in), for a power density of about 6535 W / in^3. (Ex. 2030, ¶¶32-35). The NBM2317 used the inventions of the '481

patent. (Ex. 2030, ¶35). In 2020, Petitioner Delta first released a similar NBM product, which also used the inventions of the '481 patent. (Ex. 2030, ¶33).

Although Vicor initially encountered skepticism (for reasons related to the non-isolated nature of Vicor's NBM products) the dramatic power-density advantage of Vicor's NBM converters won customers over, resulting a surge in sales of Vicor's NBM 2317 product from a few thousand units in the fourth quarter of 2019 to over 300,000 in the third quarter of 2021. (Ex. 2030, ¶¶36-40). In 2021, a leading artificial intelligence ("AI") OEM licensed Vicor's patents and started paying royalties on NBMs sourced from third parties. (Ex. 2030, ¶¶36-40). *See Merck & Co. v. Teva Pharmaceuticals USA, Inc.*, 395 F.3d 1364, 1376 (Fed. Cir. 2005)("Commercial success is relevant because the law presumes an idea would successfully have been brought to market sooner, in response to market forces, had the idea been obvious to persons skilled in the art.").

However, unlicensed sales of infringing products by third parties began in earnest in late 2021, and had a serious impact on sales of Vicor's NBM products, which had otherwise enjoyed an exponential growth curve:



(Ex. 2030, ¶¶36-40).

As Dr. Vinciarelli explains, the advantages of the invention, initial skepticism followed by commercial success of products embodying the invention, are tied to the step up in efficiency and power density gained by the invention—achieved contrary to the conventional wisdom. (Ex. 2030, ¶¶23-40). Higher power density was specifically enabled by a digital SAC controller using a clock and independently pre-set events to control a SAC to achieve ZCS and ZVS at a standard operating frequency and period. (Ex. 2030, ¶¶23-28). Even though the individual contribution of the '481 patent is difficult to quantify, it contributed significantly. (Ex. 2030, ¶40).

In the present case, multiple lines of evidence independently confirm the non-obviousness of the invention. Before the invention, Vicor's industry-leading bus

converters had a power density 10 times lower than following the invention. The inventors improved the control methodology of Sine Amplitude Converters — proceeding contrary to the conventional wisdom that such converters use closed-loop analog circuitry to control switching. This change resulted in notable gains in efficiency and power density. (Ex. 2030, ¶¶23-28). The approach eventually resulted in significant commercial success—until copycat products appeared on the market. This indicates non-obviousness. *See Safety Car Heating Lighting v. General Elec*, 155 F.2d 937, 939 (2d Cir. 1946)("In appraising an inventor's contribution to the art, as we have often said, the most reliable test is to look at the situation before and after it appears.").

IV. CONCLUSION

Petitioner respectfully requests that the Board exercise its discretion to decline institution.

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing patent owner preliminary response, together with all exhibits and other documents filed therewith, was served by electronic mail on February 21, 2024, on the petitioner's counsel of record at the United States Patent & Trademark Office having the following addresses:

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CERTIFICATE OF WORD COUNT

The undersigned hereby certifies that the foregoing patent owner preliminary response contains 17,994 words according to the word processing program used to prepare it, pursuant to the Board's Order of February 7, 2024 (Paper 6), authorizing a word count of 21,000 words for the Preliminary Response.

Date: February 21, 2024 /Matthew A. Smith/ (RN 49,003)