

ANSI INCITS 361-2002

# American National Standard

*for Information Technology –  
AT Attachment with Packet Interface - 6  
(ATA/ATAPI-6)*

**Developed by**



*Where IT all begins*





American National Standard  
for Information Technology –  
**AT Attachment with Packet Interface - 6**  
**(ATA/ATAPI-6)**

Secretariat  
**Information Technology Industry Council (ITI)**

Approved September 20, 2002  
**American National Standards Institute, Inc.**

**Abstract**

This standard specifies the AT Attachment Interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers, and suppliers of intelligent storage devices. It includes the Packet Command feature set implemented by devices commonly known as ATAPI devices.

This standard maintains a high degree of compatibility with the AT Attachment Interface with Packet Interface - 5 (ATA/ATAPI-5), ANSI NCITS 340-2000, and while providing additional functions, is not intended to require changes to presently installed devices or existing software.

## American National Standard

Approval of an American National Standard requires review by ANSI that the requirements for due process, consensus, and other criteria for approval have been met by the standards developer.

Consensus is established when, in the judgement of the ANSI Board of Standards Review, substantial agreement has been reached by directly and materially affected interests. Substantial agreement means much more than a simple majority, but not necessarily unanimity. Consensus requires that all views and objections be considered, and that a concerted effort be made towards their resolution.

The use of American National Standards is completely voluntary; their existence does not in any respect preclude anyone, whether he has approved the standards or not, from manufacturing, marketing, purchasing, or using products, processes, or procedures not conforming to the standards.

The American National Standards Institute does not develop standards and will in no circumstances give an interpretation of any American National Standard. Moreover, no person shall have the right or authority to issue an interpretation of an American National Standard in the name of the American National Standards Institute. Requests for interpretations should be addressed to the secretariat or sponsor whose name appears on the title page of this standard.

**CAUTION NOTICE:** This American National Standard may be revised or withdrawn at any time. The procedures of the American National Standards Institute require that action be taken periodically to reaffirm, revise, or withdraw this standard. Purchasers of American National Standards may receive current information on all standards by calling or writing the American National Standards Institute.

**CAUTION:** The developers of this standard have requested that holders of patents that may be required for the implementation of the standard disclose such patents to the publisher. However, neither the developers nor the publisher have undertaken a patent search in order to identify which, if any, patents may apply to this standard. As of the date of publication of this standard, following calls for the identification of patents that may be required for the implementation of the standard, notice of one or more such claims has been received. By publication of this standard, no position is taken with respect to the validity of this claim or of any rights in connection therewith. The known patent holder(s) has (have), however, filed a statement of willingness to grant a license under these rights on reasonable and nondiscriminatory terms and conditions to applicants desiring to obtain such a license. Details may be obtained from the publisher. No further patent search is conducted by the developer or publisher in respect to any standard it processes. No representation is made or implied that this is the only license that may be required to avoid infringement in the use of this standard.

Published by

**American National Standards Institute, Inc.  
25 West 43rd Street, New York, NY 10036**

Copyright © 2002 by Information Technology Industry Council (ITI)  
All rights reserved.

No part of this publication may be reproduced in any form, in an electronic retrieval system or otherwise, without prior written permission of ITI, 1250 Eye Street NW, Washington, DC 20005.

Printed in the United States of America

Copyright American National Standards Institute  
Provided by IHS Markit under license with ANSI  
No reproduction or networking permitted without license from IHS

Order Number: W2235557  
Sold to: WINSTON & STRAWN LLP [120395100001] - SGEIGER@WINSTON.COM,  
Not for Resale, 2020-08-19 13:40:11 UTC

## Contents

|                                                                                 | Page |
|---------------------------------------------------------------------------------|------|
| Foreword .....                                                                  | viii |
| Introduction .....                                                              | x    |
| 1 Scope .....                                                                   | 1    |
| 2 Normative references .....                                                    | 1    |
| 2.1 Approved references .....                                                   | 1    |
| 2.2 References under development .....                                          | 2    |
| 2.3 Other references.....                                                       | 2    |
| 3 Definitions, abbreviations, and conventions .....                             | 2    |
| 3.1 Definitions and abbreviations .....                                         | 2    |
| 3.2 Conventions.....                                                            | 5    |
| 4 Interface physical and electrical requirements .....                          | 10   |
| 4.1 Cable configuration.....                                                    | 10   |
| 4.2 Electrical characteristics .....                                            | 11   |
| 5 Interface signal assignments and descriptions .....                           | 16   |
| 5.1 Signal summary .....                                                        | 16   |
| 5.2 Signal descriptions .....                                                   | 17   |
| 6 General operational requirements .....                                        | 22   |
| 6.1 Command delivery.....                                                       | 22   |
| 6.2 Register delivered data transfer command sector addressing .....            | 22   |
| 6.3 Interrupts .....                                                            | 23   |
| 6.4 General feature set.....                                                    | 23   |
| 6.5 Multiword DMA .....                                                         | 25   |
| 6.6 Ultra DMA feature set .....                                                 | 26   |
| 6.7 Host determination of cable type by detecting CBLID-.....                   | 28   |
| 6.8 PACKET Command feature set.....                                             | 30   |
| 6.9 Overlapped feature set.....                                                 | 31   |
| 6.10 Queued feature set.....                                                    | 32   |
| 6.11 Power Management feature set .....                                         | 33   |
| 6.12 Advanced Power Management feature set .....                                | 36   |
| 6.13 Security Mode feature set.....                                             | 36   |
| 6.14 Self-monitoring, analysis, and reporting technology feature set.....       | 42   |
| 6.15 Host Protected Area feature set .....                                      | 44   |
| 6.16 CFA feature set .....                                                      | 47   |
| 6.17 Removable Media Status Notification and Removable Media feature sets ..... | 48   |
| 6.18 Power-Up In Standby feature set .....                                      | 50   |
| 6.19 Automatic Acoustic Management feature set.....                             | 50   |
| 6.20 48-bit Address feature set .....                                           | 51   |
| 6.21 Device Configuration Overlay feature set.....                              | 52   |
| 6.22 Media Card Pass Through Command feature set .....                          | 55   |
| 6.23 General Purpose Logging feature set.....                                   | 56   |
| 7 Interface register definitions and descriptions .....                         | 56   |
| 7.1 Device addressing considerations.....                                       | 56   |
| 7.2 I/O register descriptions.....                                              | 63   |

|                                            | Page      |
|--------------------------------------------|-----------|
| 7.3 Alternate Status register .....        | 63        |
| 7.4 Command register .....                 | 64        |
| 7.5 Data port .....                        | 65        |
| 7.6 Data register .....                    | 65        |
| 7.7 Device register .....                  | 66        |
| 7.8 Device Control register .....          | 67        |
| 7.9 Error register .....                   | 68        |
| 7.10 Features register .....               | 68        |
| 7.11 LBA High register .....               | 69        |
| 7.12 LBA Low register .....                | 69        |
| 7.13 LBA Mid register .....                | 70        |
| 7.14 Sector Count register .....           | 70        |
| 7.15 Status register .....                 | 71        |
| <b>8 Command descriptions .....</b>        | <b>74</b> |
| 8.1 CFA ERASE SECTORS .....                | 75        |
| 8.2 CFA REQUEST EXTENDED ERROR CODE .....  | 77        |
| 8.3 CFA TRANSLATE SECTOR .....             | 79        |
| 8.4 CFA WRITE MULTIPLE WITHOUT ERASE ..... | 81        |
| 8.5 CFA WRITE SECTORS WITHOUT ERASE .....  | 82        |
| 8.6 CHECK MEDIA CARD TYPE .....            | 84        |
| 8.7 CHECK POWER MODE .....                 | 86        |
| 8.8 DEVICE CONFIGURATION .....             | 88        |
| 8.9 DEVICE RESET .....                     | 100       |
| 8.10 DOWNLOAD MICROCODE .....              | 101       |
| 8.11 EXECUTE DEVICE DIAGNOSTIC .....       | 103       |
| 8.12 FLUSH CACHE .....                     | 105       |
| 8.13 FLUSH CACHE EXT .....                 | 106       |
| 8.14 GET MEDIA STATUS .....                | 109       |
| 8.15 IDENTIFY DEVICE .....                 | 110       |
| 8.16 IDENTIFY PACKET DEVICE .....          | 132       |
| 8.17 IDLE .....                            | 145       |
| 8.18 IDLE IMMEDIATE .....                  | 147       |
| 8.19 MEDIA EJECT .....                     | 149       |
| 8.20 MEDIA LOCK .....                      | 151       |
| 8.21 MEDIA UNLOCK .....                    | 153       |
| 8.22 NOP .....                             | 155       |
| 8.23 PACKET .....                          | 156       |
| 8.24 READ BUFFER .....                     | 162       |
| 8.25 READ DMA .....                        | 163       |
| 8.26 READ DMA EXT .....                    | 165       |
| 8.27 READ DMA QUEUED .....                 | 168       |
| 8.28 READ DMA QUEUED EXT .....             | 172       |
| 8.29 READ LOG EXT .....                    | 177       |
| 8.30 READ MULTIPLE .....                   | 186       |
| 8.31 READ MULTIPLE EXT .....               | 188       |
| 8.32 READ NATIVE MAX ADDRESS .....         | 191       |
| 8.33 READ NATIVE MAX ADDRESS EXT .....     | 193       |
| 8.34 READ SECTOR(S) .....                  | 195       |
| 8.35 READ SECTOR(S) EXT .....              | 198       |
| 8.36 READ VERIFY SECTOR(S) .....           | 200       |
| 8.37 READ VERIFY SECTOR(S) EXT .....       | 202       |

|                                                       | Page       |
|-------------------------------------------------------|------------|
| 8.38 SECURITY DISABLE PASSWORD .....                  | 205        |
| 8.39 SECURITY ERASE PREPARE .....                     | 207        |
| 8.40 SECURITY ERASE UNIT .....                        | 209        |
| 8.41 SECURITY FREEZE LOCK.....                        | 211        |
| 8.42 SECURITY SET PASSWORD.....                       | 212        |
| 8.43 SECURITY UNLOCK.....                             | 215        |
| 8.44 SEEK .....                                       | 217        |
| 8.45 SERVICE .....                                    | 218        |
| 8.46 SET FEATURES.....                                | 219        |
| 8.47 SET MAX .....                                    | 226        |
| 8.48 SET MAX ADDRESS EXT.....                         | 235        |
| 8.49 SET MULTIPLE MODE .....                          | 238        |
| 8.50 SLEEP .....                                      | 240        |
| 8.51 SMART .....                                      | 242        |
| 8.52 STANDBY.....                                     | 267        |
| 8.53 STANDBY IMMEDIATE .....                          | 269        |
| 8.54 WRITE BUFFER.....                                | 271        |
| 8.55 WRITE DMA .....                                  | 272        |
| 8.56 WRITE DMA EXT .....                              | 274        |
| 8.57 WRITE DMA QUEUED.....                            | 277        |
| 8.58 WRITE DMA QUEUED EXT.....                        | 281        |
| 8.59 WRITE LOG EXT.....                               | 287        |
| 8.60 WRITE MULTIPLE.....                              | 289        |
| 8.61 WRITE MULTIPLE EXT.....                          | 292        |
| 8.62 WRITE SECTOR(S) .....                            | 295        |
| 8.63 WRITE SECTOR(S) EXT .....                        | 297        |
| <b>9 Protocol.....</b>                                | <b>300</b> |
| 9.1 Power-on and hardware reset protocol.....         | 303        |
| 9.2 Software reset protocol .....                     | 307        |
| 9.3 Bus idle protocol .....                           | 311        |
| 9.4 Non-data command protocol .....                   | 322        |
| 9.5 PIO data-in command protocol .....                | 324        |
| 9.6 PIO data-out command protocol.....                | 328        |
| 9.7 DMA command protocol .....                        | 331        |
| 9.8 PACKET command protocol.....                      | 334        |
| 9.9 READ/WRITE DMA QUEUED command protocol .....      | 346        |
| 9.10 EXECUTE DEVICE DIAGNOSTIC command protocol ..... | 350        |
| 9.11 DEVICE RESET command protocol.....               | 355        |
| 9.12 Signature and persistence .....                  | 356        |
| 9.13 Ultra DMA data-in commands.....                  | 357        |
| 9.14 Ultra DMA data-out commands .....                | 359        |
| 9.15 Ultra DMA CRC rules.....                         | 362        |
| 9.16 Single device configurations .....               | 364        |
| <b>10 Timing .....</b>                                | <b>365</b> |
| 10.1 Deskewing .....                                  | 365        |
| 10.2 Transfer timing.....                             | 365        |
| <b>Tables</b>                                         |            |
| <b>1 Byte order .....</b>                             | <b>10</b>  |

|                                                                                              | Page |
|----------------------------------------------------------------------------------------------|------|
| 2 Byte order .....                                                                           | 10   |
| 3 DC characteristics .....                                                                   | 11   |
| 4 AC characteristics .....                                                                   | 12   |
| 5 Driver types and required termination .....                                                | 13   |
| 6 Typical series termination for Ultra DMA .....                                             | 15   |
| 7 Interface signal name assignments .....                                                    | 16   |
| 8 Cable type identification .....                                                            | 19   |
| 9 Host detection of CBLID- .....                                                             | 19   |
| 10 Security mode command actions .....                                                       | 19   |
| 11 48-bit addresses .....                                                                    | 19   |
| 12 28-bit addresses .....                                                                    | 19   |
| 13 Media Card type references .....                                                          | 19   |
| 14 Device response to DOIW-/DOIR- .....                                                      | 19   |
| 15 Device is not selected, DMACK- is not asserted .....                                      | 19   |
| 16 Device is selected, DMACK- is not asserted .....                                          | 19   |
| 17 Device is selected, DMACK- is asserted (for Multiword DMA only) .....                     | 19   |
| 18 Device 1 is selected and Device 0 is responding for Device 1 .....                        | 19   |
| 19 Device is in Sleep mode, DEVICE RESET is not implemented,<br>DMACK- is not asserted ..... | 19   |
| 20 Device is in Sleep mode, DEVICE RESET is implemented,<br>DMACK- is not asserted .....     | 19   |
| 21 Extended error codes .....                                                                | 19   |
| 22 CFA TRANSLATE SECTOR information .....                                                    | 19   |
| 23 Device Configuration Overlay Features register values .....                               | 19   |
| 24 Device Configuration Identify data structure .....                                        | 19   |
| 25 Device Configuration Overlay data structure .....                                         | 19   |
| 26 Diagnostic codes .....                                                                    | 19   |
| 27 IDENTIFY DEVICE information .....                                                         | 19   |
| 28 Minor revision number .....                                                               | 19   |
| 29 IDENTIFY PACKET DEVICE information .....                                                  | 19   |
| 30 Automatic standby timer periods .....                                                     | 19   |
| 31 Log address definition .....                                                              | 19   |
| 32 General Purpose Log directory .....                                                       | 19   |
| 33 Extended Comprehensive SMART error log .....                                              | 19   |
| 34 Extended Error Log data structure .....                                                   | 19   |

|    |                                                                |    |
|----|----------------------------------------------------------------|----|
| 35 | Command data structure .....                                   | 19 |
| 36 | Error data structure .....                                     | 19 |
| 37 | State field values.....                                        | 19 |
| 38 | Extended self-test log data structure .....                    | 19 |
| 39 | Extended self-test log descriptor entry.....                   | 19 |
| 40 | Security password content.....                                 | 19 |
| 41 | SECURITY ERASE UNIT password.....                              | 19 |
| 42 | SECURITY SET PASSWORD data content .....                       | 19 |
| 43 | Identifier and security level bit interaction .....            | 19 |
| 44 | SET FEATURES register definitions.....                         | 19 |
| 45 | Transfer/mode values .....                                     | 19 |
| 46 | Advanced power management levels .....                         | 19 |
| 47 | Automatic acoustic management levels.....                      | 19 |
| 48 | SET MAX Features register values.....                          | 19 |
| 49 | SET MAX SET PASSWORD data content .....                        | 19 |
| 50 | SMART Feature register values.....                             | 19 |
| 51 | SMART EXECUTE OFF-LINE IMMEDIATE Sector Number register values | 19 |
| 52 | Device SMART data structure .....                              | 19 |
| 53 | Off-line data collection status byte values.....               | 19 |
| 54 | Self-test execution status byte values.....                    | 19 |
| 55 | Log address definition.....                                    | 19 |
| 56 | SMART log directory .....                                      | 19 |
| 57 | SMART summary error log sector .....                           | 19 |
| 58 | Error log data structure .....                                 | 19 |
| 59 | Command data structure .....                                   | 19 |
| 60 | Error data structure .....                                     | 19 |
| 61 | State field values.....                                        | 19 |
| 62 | Comprehensive error log .....                                  | 19 |
| 63 | Self-test log data structure .....                             | 19 |
| 64 | Self-test log descriptor entry .....                           | 19 |
| 65 | Equations for parallel generation of a CRC polynomial .....    | 19 |
| 66 | Register transfer to/from device.....                          | 19 |
| 67 | PIO data transfer to/from device .....                         | 19 |
| 68 | Multiword DMA data transfer .....                              | 19 |
| 69 | Ultra DMA data burst timing requirements.....                  | 19 |
| 70 | Ultra DMA data burst timing descriptions.....                  | 19 |

v

|    |                                                            |    |
|----|------------------------------------------------------------|----|
| 71 | Ultra DMA sender and recipient IC timing requirements..... | 19 |
|----|------------------------------------------------------------|----|

## Figures

|    |                                                                                         |    |
|----|-----------------------------------------------------------------------------------------|----|
| 1  | State diagram convention .....                                                          | 8  |
| 2  | Ultra DMA termination with pull-up or pull-down.....                                    | 15 |
| 3  | Cable select example.....                                                               | 19 |
| 4  | Alternate cable select example .....                                                    | 19 |
| 5  | Example configuration of a system with a 40-conductor cable .....                       | 19 |
| 6  | Example configuration of a system where the host detects a<br>40-conductor cable .....  | 19 |
| 7  | Example configuration of a system where the host detects an<br>80-conductor cable ..... | 19 |
| 8  | Power management state diagram .....                                                    | 19 |
| 9  | Security mode state diagram .....                                                       | 19 |
| 10 | SET MAX security state diagram .....                                                    | 19 |
| 11 | Device Configuration Overlay state diagram .....                                        | 19 |
| 12 | Overall host protocol state sequence.....                                               | 19 |
| 13 | Overall device protocol state sequence .....                                            | 19 |
| 14 | Host power-on or hardware reset state diagram.....                                      | 19 |
| 15 | Device power-on or hardware reset state diagram .....                                   | 19 |
| 16 | Host software reset state diagram .....                                                 | 19 |
| 17 | Device 0 software reset state diagram.....                                              | 19 |
| 18 | Device 1 software reset state diagram.....                                              | 19 |
| 19 | Host bus idle state diagram .....                                                       | 19 |
| 20 | Additional host bus idle state diagram with overlap or overlap and queuing              | 19 |
| 21 | Device bus idle state diagram.....                                                      | 19 |
| 22 | Additional device bus idle state diagram with overlap or overlap and queuing            | 19 |
| 23 | Host non-data state diagram.....                                                        | 19 |
| 24 | Device non-data state diagram .....                                                     | 19 |
| 25 | Host PIO data-in state diagram.....                                                     | 19 |
| 26 | Device PIO data-in state diagram .....                                                  | 19 |
| 27 | Host PIO data-out state diagram .....                                                   | 19 |
| 28 | Device PIO data-out state diagram .....                                                 | 19 |
| 29 | Host DMA state diagram.....                                                             | 19 |
| 30 | Device DMA state diagram .....                                                          | 19 |
| 31 | Host PACKET non-data and PIO data command state diagram .....                           | 19 |
| 32 | Device PACKET non-data and PIO data command state diagram.....                          | 19 |
| 33 | Host PACKET DMA command state diagram.....                                              | 19 |

|                |                                                               |    |
|----------------|---------------------------------------------------------------|----|
| 34             | Device PACKET DMA command state diagram .....                 | 19 |
| 35             | Host DMA QUEUED state diagram .....                           | 19 |
| 36             | Device DMA QUEUED command state diagram .....                 | 19 |
| 37             | Host EXECUTE DEVICE DIAGNOSTIC state diagram .....            | 19 |
| 38             | Device 0 EXECUTE DEVICE DIAGNOSTIC state diagram .....        | 19 |
| 39             | Device 1 EXECUTE DEVICE DIAGNOSTIC command state diagram..... | 19 |
| 40             | Host DEVICE RESET command state diagram.....                  | 19 |
| 41             | Device DEVICE RESET command state diagram .....               | 19 |
| 42             | Example parallel CRC generator .....                          | 19 |
| 43             | Register transfer to/from device .....                        | 19 |
| 44             | PIO data transfer to/from device .....                        | 19 |
| 45             | Initiating a Multiword DMA data burst .....                   | 19 |
| 46             | Sustaining a Multiword DMA data burst.....                    | 19 |
| 47             | Device terminating a Multiword DMA data burst.....            | 19 |
| 48             | Host terminating a Multiword DMA data burst .....             | 19 |
| 49             | Initiating an Ultra DMA data-in burst .....                   | 19 |
| 50             | Sustained Ultra DMA data-in burst .....                       | 19 |
| 51             | Host pausing an Ultra DMA data-in burst .....                 | 19 |
| 52             | Device terminating an Ultra DMA data-in burst.....            | 19 |
| 53             | Host terminating an Ultra DMA data-in burst .....             | 19 |
| 54             | Initiating an Ultra DMA data-out burst.....                   | 19 |
| 55             | Sustained Ultra DMA data-out burst .....                      | 19 |
| 56             | Device pausing an Ultra DMA data-out burst.....               | 19 |
| 57             | Host terminating an Ultra DMA data-out burst .....            | 19 |
| 58             | Device terminating an Ultra DMA data-out burst .....          | 19 |
| <b>Annexes</b> |                                                               |    |
| A              | Connectors and cable assemblies .....                         | 19 |
| B              | Device determination of cable type.....                       | 19 |
| C              | Signal integrity and UDMA implementation guide.....           | 19 |
| D              | Bibliography .....                                            | 19 |
| E              | ATA command set summary.....                                  | 19 |

**Foreword** (This foreword is not part of ANSI INCITS 361-2002.)

This AT Attachment with Packet Interface - 6 (ATA/ATAPI-6) standard is designed to maintain a high degree of compatibility with the AT Attachment with Packet Interface - 5 (ATA/ATAPI-5) standard.

This standard was developed by the ATA ad hoc working group of INCITS during 2000 and 2001. The standards approval process started in 2001. This document includes annexes that are informative and are not considered part of the standard.

Requests for interpretation, suggestions for improvement and addenda, or defect reports are welcome. They should be sent to the INCITS Secretariat, Information Technology Industry Council, 1250 Eye Street, NW, Suite 200, Washington, DC 20005-3922.

This standard was processed and approved for submittal to ANSI by InterNational Committee for Information Technology Standards (INCITS). Committee approval of the standard does not necessarily imply that all committee members voted for approval. At the time it approved this standard, INCITS had the following members:

Karen Higginbottom, Chair  
Russ Richards, Vice-Chair  
Jennifer Garner, Secretary

*Organization Represented Name of Representative*

|                                                             |                                                                  |
|-------------------------------------------------------------|------------------------------------------------------------------|
| Apple Computer, Inc.....                                    | David Michael<br>Wanda Cox (Alt.)                                |
| Hewlett-Packard Company.....                                | Karen Higginbottom<br>Scott Jameson (Alt.)<br>Steve Mills (Alt.) |
| Hitachi America, Ltd. ....                                  | John Neumann<br>Harukazu Miyamoto (Alt.)                         |
| IBM Corporation .....                                       | Ronald F. Silletti<br>Chuck Adams (Alt.)                         |
| Institute for Certification of Computer Professionals ..... | Kenneth M. Zemrowski<br>Thomas Kurihara (Alt.)                   |
| Microsoft Corporation .....                                 | Mike Ksar<br>Joseph Zajackowski (Alt.)<br>Mike Deese (Alt.)      |
| National Institute of Standards & Technology .....          | Michael Hogan<br>William LaPlant, Jr. (Alt.)                     |
| Oracle Corporation .....                                    | Donald R. Deutsch<br>Jim Melton (Alt.)                           |
| Panasonic Technologies, Inc. ....                           | Terence Nelson<br>Rudolf Vitti (Alt.)                            |
| Purdue University .....                                     | Stephen Elliott                                                  |
| SHARE Inc. ....                                             | Dave Thewlis                                                     |
| Sony Electronics, Inc.....                                  | Ed Barrett<br>Jean Baronas (Alt.)                                |
| Sun Microsystems, Inc. ....                                 | John Hill<br>Roger Martin (Alt.)<br>Douglas Johnson (Alt.)       |
| Unisys Corporation.....                                     | Arnold F. Winkler<br>Walt Korzeniowski (Alt.)                    |
| US Department of Defense/DISA.....                          | Russ Richards<br>Jerry Smith (Alt.)                              |
| Xerox Corporation .....                                     | Kathleen O'Reilly                                                |

Technical Committee T13 on ATA Interfaces, which reviewed this standard, had the following members:

Pete McLean, Chairman  
Dan Colegrove, Vice-Chairman  
Mark Evans, Secretary

Larry Barras  
Tim Bradshaw  
Darrin Bulik  
Robert Chang  
Phil Gardner  
Tony Goodfellow  
Andre Hedrick  
Skip Jones  
Tasuku Kasebayashi

Mary Morgan  
Marc Noblitt  
Sumit Puri  
Ron Roberts  
Ron Salmon  
Tim Thompson  
Krishnan Varadarajan  
Quong Vuong  
Aaron Wilson

Paul Anderson (Alt.)  
Tom Barrett (Alt.)  
Tom Hanan (Alt.)  
Gary Laatsch (Alt.)  
Wen Lin (Alt.)  
Nita Pan (Alt.)  
Rob Schram (Alt.)  
Randy Sharp (Alt.)  
Curtis Stevens (Alt.)

Technical Committee T13 on ATA Interfaces, which developed this standard, had the following additional participants:

|                   |                     |                   |
|-------------------|---------------------|-------------------|
| Steve Bassett     | Jeroen Heuvelman    | Minoru Ohara      |
| Ken Bovatsek      | Emily Hill          | Hitoshi Ogawa     |
| Randy Buchter     | Akil Houston        | Masataka Ogawa    |
| Ken Bush          | Hiroaki Inoue       | Paul Peissner     |
| Litko Chan        | Joe M. Jackson      | Bruce Perens      |
| Ben Chang         | Mike Jaskowiak      | Nicholas Phillips |
| Fay Chong         | Richard Kalish      | David Platt       |
| Emmanuel Coudray  | Maryann Karinch     | Bob Raicer        |
| David Craft       | Keiji Katata        | Robert Raymond    |
| Lam Dang          | Yoshihide Katsuse   | Charley Riegger   |
| Faheem Dani       | Eric Kvamme         | Juhani Rissanen   |
| David Dickson     | Niek Lambert        | Matt Rooke        |
| Brian Dixon       | Hale Landis         | Bob Rudy          |
| Don Doan          | Andy Lawrence       | Daniel Salmonsens |
| Ricardo Dominguez | Leroy Leach         | Robbie Shergill   |
| Seiichi Domyo     | Raymond Liu         | Kanting Tsai      |
| Michael Eschmann  | Robert Liu          | George Tun        |
| Leroy Fong        | Jeff Lotspiech      | Phil Turner       |
| Henry Gabryjelski | John Marttila       | Tri Van           |
| John Gilmore      | Ron Mathews         | Rudolf Vitti      |
| Gary Glass        | Bill McFerrin       | Jeff Wolford      |
| Eric Gorham       | Lynn McQueen        | Janet Wu          |
| Jonathan Hanmann  | Shigehiro Mishimagi | Han Zou           |
| Richard Harcourt  | Kosuke Nakai        |                   |
| Jim Hatfield      | Terence Nelson      |                   |
| Justin Heindel    | Huy Nguyen          |                   |

X

## Introduction

This standard encompasses the following:

Clause 1 describes the scope.

Clause 2 provides normative references.

Clause 3 provides definitions, abbreviations, and conventions used within this document.

Clause 4 contains the electrical and mechanical characteristics.

Clause 5 contains the signal descriptions of the AT Attachment Interface.

Clause 6 describes the general operating requirements of the AT Attachment Interface.

Clause 7 contains descriptions of the registers of the AT Attachment Interface.

Clause 8 contains descriptions of the commands of the AT Attachment Interface.

Clause 9 contains the protocol of the AT Attachment Interface.

Clause 10 contains the interface timing diagrams.

American National Standard  
for Information Technology –

## AT Attachment with Packet Interface - 6 (ATA/ATAPI-6)

### 1 Scope

This standard specifies the AT Attachment Interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers, and suppliers of intelligent storage devices.

The application environment for the AT Attachment Interface is any host system that has storage devices contained within the processor enclosure.

This standard defines the connectors and cables for physical interconnection between host and storage device, as well as the electrical and logical characteristics of the interconnecting signals. It also defines the operational registers within the storage device, and the commands and protocols for the operation of the storage device.

This standard maintains a high degree of compatibility with the AT Attachment with Packet Interface – 5 standard (ATA/ATAPI-5), NCITS 340-2000, and while providing additional functions, is not intended to require changes to presently installed devices or existing software.

### 2 Normative references

The following standards contain provisions that, through reference in the text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

Copies of the following documents can be obtained from ANSI: Approved ANSI standards, approved and draft international and regional standards (ISO, IEC, CEN/CENELEC, ITUT), and approved and draft foreign standards (including BSI, JIS, and DIN). For further information, contact ANSI Customer Service Department at 212-642-4900 (phone), 212-302-1286 (fax), or via the World Wide Web at <http://www.ansi.org>.

Additional availability contact information is provided below as needed.

#### 2.1 Approved references

The following approved ANSI standards, approved international and regional standards (ISO, IEC, CEN/CENELEC, ITUT), may be obtained from the international and regional organizations who control them.

|                               |                                                              |
|-------------------------------|--------------------------------------------------------------|
| SCSI-3 Primary Commands (SPC) | [ANSI X3.301-1997] (PACKET command feature set device types) |
| Multimedia Commands (MMC)     | [ANSI X3.304-1997] (PACKET command feature set sense codes)  |

Multimedia Commands - 2 (MMC-2) [ANSI NCITS 333-2000] (PACKET command feature set commands)  
Protected Area Run Time Interface Extensions [ANSI NCITS 346-2001]  
SCSI Primary Commands - 2 (SPC-2) [ANSI NCITS 351-2001] (PACKET command feature set commands)

To obtain copies of these documents, contact Global Engineering or NCITS.

## 2.2 References under development

At the time of publication, the following referenced standards were still under development. For information on the current status of the document, or regarding availability, contact the relevant standards body or other organization as indicated.

SCSI Primary Commands - 3 (SPC-3) [T10/1416-D] (PACKET command feature set commands)  
Multimedia Commands - 3 (MMC-3) [T10/1363-D] (PACKET command feature set commands)  
ATAPI for Rewritable Media [SFF8070i]

For more information on the current status of the T10 documents, contact NCITS. To obtain copies of T10 or SFF documents, contact Global Engineering.

## 2.3 Other references

The following standard and specifications are also referenced.

PC Card Standard , February 1995, PCMCIA (68-pin Connector)

For the PC Card Standard published by the Personal Computer Memory Card International Association, contact PCMCIA at 408-433-2273.

CompactFlash™ Association Specification, Revision 1.4

For the CompactFlash™ Association Specification published by the CompactFlash™ Association, contact the CompactFlash™ Association at <http://www.compactflash.org>.

ATA Packet Interface (ATAPI) for Streaming Tape QIC-157 revision D

For QIC specifications published by Quarter-Inch Cartridge Drive Standards, Inc., contact them at 805 963-3853.

## 3 Definitions, abbreviations, and conventions

### 3.1 Definitions and abbreviations

For the purposes of this standard, the following definitions apply:

**3.1.1 ATA (AT Attachment):** ATA defines the physical, electrical, transport, and command protocols for the internal attachment of storage devices to host systems.

**3.1.2 ATA-1 device:** A device that complied with ANSI X3.221-1994, the AT Attachment Interface for Disk Drives. ANSI X3.221-1994 has been withdrawn.

**3.1.3 ATA-2 device:** A device that complied with ANSI X3.279-1996, the AT Attachment Interface with Extensions. ANSI X3.279-1996 has been withdrawn.

**3.1.4 ATA-3 device:** A device that complies with ANSI X3.298-1997, the AT Attachment-3 Interface.

- 3.1.5 ATA/ATAPI-4 device:** A device that complies with ANSI NCITS 317-1998, AT Attachment Interface with Packet Interface Extensions.
- 3.1.6 ATA/ATAPI-5 device:** A device that complies with ANSI NCITS 340-2000, the AT Attachment with Packet Interface -5.
- 3.1.7 ATA/ATAPI-6 device:** A device that complies with this standard.
- 3.1.8 ATAPI (AT Attachment Packet Interface) device:** A device implementing the Packet Command feature set.
- 3.1.9 bus release:** For devices implementing overlap, the term bus release is the act of clearing both DRQ and BSY to zero before the action requested by the command is completed. This allows the host to select the other device or deliver another queued command.
- 3.1.10 byte count:** The value placed in the Byte Count register by the device to indicate the number of bytes to be transferred during this DRQ assertion when executing a PACKET PIO data transfer command.
- 3.1.11 byte count limit:** The value placed in the Byte Count register by the host as input to a PACKET PIO data transfer command to specify the maximum byte count that may be transferred during a single DRQ assertion.
- 3.1.12 CFA:** The CompactFlash™ Association that created the specification for compact flash memory that uses the ATA interface.
- 3.1.13 check condition:** For devices implementing the PACKET Command feature set, this indicates an error or exception condition has occurred.
- 3.1.14 CHS (cylinder-head-sector):** This term defines an obsolete method of addressing the data on the device by cylinder number, head number, and sector number.
- 3.1.15 command aborted:** Command completion with ABRT set to one in the Error register and ERR set to one in the Status register.
- 3.1.16 command acceptance:** A command is considered accepted whenever the currently selected device has the BSY bit cleared to zero in the Status register and the host writes to the Command register. An exception exists for the DEVICE RESET command (see 8.9).
- 3.1.17 Command Block registers:** Interface registers used for delivering commands to the device or posting status from the device.
- 3.1.18 command completion:** Command completion is the completion by the device of the action requested by the command or the termination of the command with an error, the placing of the appropriate error bits in the Error register, the placing of the appropriate status bits in the Status register, the clearing of both BSY and DRQ to zero, and the asserting of INTRQ if nIEN is cleared to zero and the command protocol specifies that INTRQ be asserted.
- 3.1.19 command packet:** A command packet is a data structure transmitted to the device during the execution of a PACKET command that includes the command and command parameters.
- 3.1.20 command released:** When a device supports overlap or queuing, a command is considered released when a bus release occurs before command completion.
- 3.1.21 Control Block registers:** Interface registers used for device control and to post alternate status.
- 3.1.22 CRC:** Cyclical Redundancy Check used to check the validity of certain data transfers.

- 3.1.23 device:** Device is a storage peripheral. Traditionally, a device on the interface has been a hard disk drive, but any form of storage device may be placed on the interface provided the device adheres to this standard.
- 3.1.24 device selection:** A device is selected when the DEV bit of the Device register is equal to the device number assigned to the device by means of a Device 0/Device 1 jumper or switch, or use of the CSEL signal.
- 3.1.25 DMA (direct memory access) data transfer:** A means of data transfer between device and host memory without host processor intervention.
- 3.1.26 don't care:** A term to indicate that a value is irrelevant for the particular function described.
- 3.1.27 driver:** The active circuit inside a device or host that sources or sinks current to assert or negate a signal on the bus.
- 3.1.28 DRQ data block:** This term describes a unit of data words transferred during a single assertion of DRQ when using PIO data transfer. A data block is transferred between the host and the device as a complete unit. For all PIO data transfer commands except READ MULTIPLE, WRITE MULTIPLE, and PACKET, a DRQ data block is one sector, 512 bytes. For READ MULTIPLE and WRITE MULTIPLE commands the DRQ data block is the number of sectors indicated in word 59 of the IDENTIFY DEVICE response. For PACKET command the DRQ data block for transfer of the command packet is the number of bytes indicated in word 0 of the IDENTIFY PACKET DEVICE response.
- 3.1.29 interrupt pending:** Interrupt pending is an internal state of a device that causes the device to notify the host of an event by asserting INTRQ if nIEN is cleared to zero and the device is selected (see 6.3).
- 3.1.30 LBA (logical block address):** This term defines the addressing of data on the device by the linear mapping of sectors.
- 3.1.31 master:** In ATA-1, Device 0 was referred to as the master. Throughout this document the term Device 0 is used.
- 3.1.32 native max address:** The highest address a device accepts in the factory default condition, that is, the highest address that is accepted by the SET MAX ADDRESS command.
- 3.1.33 overlap:** Overlap is a protocol that allows devices that require extended command time to perform a bus release so that commands may be executed by the other device on the bus.
- 3.1.34 packet delivered command:** A command that is delivered to the device using the PACKET command via a command packet that contains the command and the command parameters.
- 3.1.35 PIO (programmed input/output) data transfer:** PIO data transfers are performed by the host processor utilizing accesses to the Data register.
- 3.1.36 queued:** Command queuing allows the host to issue concurrent commands to the same device. Only commands included in the Overlapped feature set may be queued. In this standard, the queue contains all commands for which command acceptance has occurred but command completion has not occurred.
- 3.1.37 read command:** A command that causes the device to read data from the media (e.g., READ SECTOR(S), READ DMA, etc.).
- 3.1.38 register delivered command:** A command that is delivered to the device by placing the command and all of the parameters for the command in the device Command Block registers.

- 3.1.39 register transfers:** Register transfers refer to the host reading and writing any device register except the Data register. Register transfers are 8 bits wide.
- 3.1.40 released:** Indicates that a signal is not being driven. For drivers capable of assuming a high-impedance state, this means that the driver is in the high impedance state. For open-collector drivers, the driver is not asserted.
- 3.1.41 sector:** A uniquely addressable set of 256 words (512 bytes).
- 3.1.42 signature:** A unique set of values placed in the Command Block registers by the device to allow the host to distinguish devices implementing the PACKET Command feature set from those devices not implementing the PACKET Command feature set..
- 3.1.43 slave:** In ATA-1, Device 1 was referred to as the slave. Throughout this document the term Device 1 is used.
- 3.1.44 SMART:** Self-Monitoring, Analysis, and Reporting Technology for prediction of device degradation and/or faults. Throughout this document this is noted as SMART.
- 3.1.45 Ultra DMA burst:** An Ultra DMA burst is defined as the period from an assertion of DMACK- to the subsequent negation of DMACK- when an Ultra DMA transfer mode has been enabled by the host.
- 3.1.46 unit attention condition:** A state that a device implementing the PACKET Command feature set maintains while the device has asynchronous status information to report to the host.
- 3.1.47 unrecoverable error:** An unrecoverable error has occurred when the device sets either the ERR bit or the DF bit to one in the Status register at command completion.
- 3.1.48 VS (vendor specific):** This term is used to describe bits, bytes, fields, and code values that are reserved for vendor specific purposes. These bits, bytes, fields, and code values are not described in this standard, and may vary among vendors. This term is also applied to levels of functionality whose definition is left to the vendor.

NOTE – Industry practice could result in conversion of a Vendor Specific bit, byte, field, or code value into a defined standard value in a future standard.

- 3.1.50 write command:** A command that causes the device to write data to the media (e.g., WRITE SECTOR(S), WRITE DMA, etc.).

## 3.2 Conventions

Lowercase is used for words having the normal English meaning. Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in clause 3 or in the text where they first appear.

The names of abbreviations, commands, fields, and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE). Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field. (see 3.2.6 for the naming convention used for naming bits.)

Names of device registers begin with a capital letter (e.g., LBA Mid register).

The expression "word n" or "bit n" shall be interpreted as indicating the content of word n or bit n.

### 3.2.1 Precedence

If there is a conflict between text, figures, and tables, the precedence shall be tables, figures, then text.

**Transition SM1a:SM1:** When a SET MAX ADDRESS command is received, the command shall be executed and the device shall make a transition to the SM1: Set\_MAX\_Unlocked state.

**Transition SM1b:SM1:** When a SET MAX SET PASSWORD is received, the password stored by the device shall be changed to the new value and the device shall make a transition to the SM1: Set\_MAX\_Unlocked state.

**Transition SM1c:SM1:** When a SET MAX UNLOCK command is received, the command shall not be executed and the device shall make a transition to the SM1: Set\_MAX\_Unlocked state.

**Transition SM1:SM2:** When a SET MAX LOCK command is received, the device shall make a transition to the SM2: Set\_Max\_Locked state.

**Transition SM1:SM3:** When a SET MAX FREEZE LOCK command is received, the device shall make a transition to the SM3: Set\_Max\_Frozen state.

**SM2: Set\_Max\_Locked:** This state is entered when a SET MAX LOCK command is received.

When in this state, a SET MAX security password has been established and the SET MAX security is locked. Bit 8 of word 86 of the identify device data shall be set to one.

**Transition SM2a:SM2:** When a SET MAX ADDRESS or SET MAX SET PASSWORD command is received, the command shall be aborted and the device shall make a transition to the SM2: Set\_Max\_Locked state.

**Transition SM2b:SM2:** When a SET MAX LOCK command is received, the command shall be executed and the device shall make a transition to the SM2: Set\_Max\_Locked state.

**Transition SM2:SM1:** When a SET MAX UNLOCK command is received, the device shall make a transition to the SM1: Set Max Unlocked state.

**Transition SM2:SM3:** When a SET MAX FREEZE LOCK command is received, the device may make a transition to the SM3: Set\_Max\_Frozen state. Hosts should not issue the SET MAX FREEZE LOCK command when in this state.

**SM3: Set\_Max\_Frozen:** This state is entered when a SET MAX FREEZE LOCK command is received.

In this state, the device may not transition to any other state except by a power cycling. When in this mode bit 8 of word 86 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data shall be set to one.

**Transition SM3:SM3:** When a SET MAX ADDRESS, SET MAX SET PASSWORD, SET MAX UNLOCK, SET MAX FREEZE LOCK, or SET MAX LOCK command is received, the command shall be aborted and the device shall make a transition to the SM3: Set\_Max\_Frozen state.

## 6.16 CFA feature set

The optional CompactFlash™ Association (CFA) feature set provides support for solid state memory devices. A device that implements the CFA feature set shall implement the following minimum set of commands:

- CFA REQUEST EXTENDED ERROR CODE
- CFA WRITE SECTORS WITHOUT ERASE
- CFA ERASE SECTORS
- CFA WRITE MULTIPLE WITHOUT ERASE
- CFA TRANSLATE SECTOR
- SET FEATURES Enable/Disable 8-bit transfer

Devices reporting the value 848Ah in IDENTIFY DEVICE data word 0 or devices having bit 2 of IDENTIFY DEVICE data word 83 set to one shall support the CFA feature Set. If the CFA feature set is implemented, all five commands shall be implemented.

Support of DMA commands is optional for devices that support the CFA feature set.

The CFA ERASE SECTORS command preconditions the sector for a subsequent CFA WRITE SECTORS WITHOUT ERASE or CFA WRITE MULTIPLE WITHOUT ERASE command to achieve higher performance during the write operation. The CFA TRANSLATE SECTOR command provides information about a sector such as the number of write cycles performed on that sector and an indication of the sector's erased precondition. The CFA REQUEST EXTENDED ERROR CODE command provides more detailed error information.

Command codes B8h through BFh are reserved for assignment by the CompactFlash™ Association.

## 6.17 Removable Media Status Notification and Removable Media feature sets

This section describes two feature sets that secure the media in removable media storage devices using the ATA/ATAPI interface protocols. The Removable Media Status Notification feature set is intended for use in both devices implementing the PACKET Command feature set and those not implementing the PACKET Command feature set. The Removable Media feature set is intended for use only in devices not implementing the PACKET Command feature set. Only one of these feature sets shall be enabled at any time. If the Removable Media Status Notification feature set is in use then the Removable Media feature set is disabled and vice versa.

The reasons for implementing the Removable Media Status Notification feature Set or the Removable Media feature set are:

- to prevent data loss caused by writing to new media while still referencing the previous media's information.
- to prevent data loss by locking the media until completion of a cached write.
- to prevent removal of the media by unauthorized persons.

### 6.17.1 Removable Media Status Notification feature set

The Removable Media Status Notification feature set is the preferred feature set for securing the media in removable media storage devices. This feature set uses the SET FEATURES command to enable Removable Media Status Notification. Removable Media Status Notification gives the host system maximum control of the media. The host system determines media status by issuing the GET MEDIA STATUS command and controls the device eject mechanism via the MEDIA EJECT command (for devices not implementing the PACKET Command feature set) or the START/STOP UNIT command (for devices implementing the PACKET Command feature set, see clause 2). While Removable Media Status Notification is enabled devices not implementing the PACKET Command feature set execute MEDIA LOCK and MEDIA UNLOCK commands without changing the media lock state (no-operation). While Removable Media Status Notification is enabled the eject button does not eject the media.

Removable Media Status Notification is persistent through medium removal and insertion and is only disabled via the SET FEATURES command, hardware reset, software reset, the DEVICE RESET command, the EXECUTE DEVICE DIAGNOSTIC command, or power-on reset. Removable Media Status Notification shall be re-enabled after any of the previous reset conditions occur. All media status is reset when Removable Media Status Notification is disabled because a reset condition occurred. Any pending media change or media change request is cleared when the Removable Media Status Notification reset condition occurs.

The following commands are defined to implement the Removable Media Status Notification feature set.

- GET MEDIA STATUS
- MEDIA EJECT

- Sector Count register;
- Device register.

The ERR bit shall be cleared to zero by the device:

- 1) when a new command is written to the Command register;
- 2) when the SRST bit is set to one;
- 3) when the RESET- signal is asserted.

When the ERR bit is cleared to zero at the end of a command:

- 1) the content of the Error register shall be ignored by the host.

## 8 Command descriptions

Commands are issued to the device by loading the required registers in the command block with the needed parameters and then writing the command code to the Command register. Required registers are those indicated by a specific content in the Inputs table for the command, i.e., not noted as na or obs.

Each command description in the following clauses contains the following subclauses:

Command code –Specifies the command code for this command.

Feature set –Specifies feature set and if the command is mandatory or optional.

Protocol –Specifies which protocol is used by the command (see clause 9).

Inputs – Describes the Command Block register data that the host shall supply.

| Register                                                                                                                                           | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------------------------------------------------------------------------------------------------------------------------------------|--------------|---|---|---|---|---|---|---|
| Features                                                                                                                                           |              |   |   |   |   |   |   |   |
| Sector Count                                                                                                                                       |              |   |   |   |   |   |   |   |
| LBA Low                                                                                                                                            |              |   |   |   |   |   |   |   |
| LBA Mid                                                                                                                                            |              |   |   |   |   |   |   |   |
| LBA High                                                                                                                                           |              |   |   |   |   |   |   |   |
| Device                                                                                                                                             |              |   |   |   |   |   |   |   |
| Command                                                                                                                                            | Command Code |   |   |   |   |   |   |   |
| NOTE – na specifies the content of a bit or field is not applicable to the particular command. Obs specifies that the use of this bit is obsolete. |              |   |   |   |   |   |   |   |

Normal outputs – Describes the Command Block register data returned by the device at the end of a command.

| Register                                                                                                                                           | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------------------------------------------------------------------------------------------------------------------------------------|---|---|---|---|---|---|---|---|
| Error                                                                                                                                              |   |   |   |   |   |   |   |   |
| Sector Count                                                                                                                                       |   |   |   |   |   |   |   |   |
| LBA Low                                                                                                                                            |   |   |   |   |   |   |   |   |
| LBA Mid                                                                                                                                            |   |   |   |   |   |   |   |   |
| LBA High                                                                                                                                           |   |   |   |   |   |   |   |   |
| Device                                                                                                                                             |   |   |   |   |   |   |   |   |
| Status                                                                                                                                             |   |   |   |   |   |   |   |   |
| NOTE – na indicates the content of a bit or field is not applicable to the particular command. Obs indicates that the use of this bit is obsolete. |   |   |   |   |   |   |   |   |

Error outputs – Describes the Command Block register data that shall be returned by the device at command completion with an unrecoverable error.

| Register                                                                                                                                           | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------------------------------------------------------------------------------------------------------------------------------------|---|---|---|---|---|---|---|---|
| Error                                                                                                                                              |   |   |   |   |   |   |   |   |
| Sector Count                                                                                                                                       |   |   |   |   |   |   |   |   |
| LBA Low                                                                                                                                            |   |   |   |   |   |   |   |   |
| LBA Mid                                                                                                                                            |   |   |   |   |   |   |   |   |
| LBA High                                                                                                                                           |   |   |   |   |   |   |   |   |
| Device                                                                                                                                             |   |   |   |   |   |   |   |   |
| Status                                                                                                                                             |   |   |   |   |   |   |   |   |
| NOTE – na indicates the content of a bit or field is not applicable to the particular command. Obs indicates that the use of this bit is obsolete. |   |   |   |   |   |   |   |   |

Prerequisites – Any prerequisite commands or conditions that shall be met before the command is issued.

Description – The description of the command function(s).

## 8.1 CFA ERASE SECTORS

### 8.1.1 Command code

C0h

### 8.1.2 Feature set

CFA feature set.

- If the CFA feature set is implemented this command shall be implemented.

This command code is Vendor Specific for devices not implementing the CFA feature Set.

### 8.1.3 Protocol

Non-data (see 9.4).

### 8.1.4 Inputs

The LBA High, LBA Mid, LBA Low, and Device registers specify the starting sector address to be erased. The Sector Count register specifies the number of sectors to be erased.

| Register     | 7            | 6   | 5   | 4   | 3           | 2 | 1 | 0 |
|--------------|--------------|-----|-----|-----|-------------|---|---|---|
| Features     | na           |     |     |     |             |   |   |   |
| Sector Count | Sector count |     |     |     |             |   |   |   |
| LBA Low      | LBA (7:0)    |     |     |     |             |   |   |   |
| LBA Mid      | LBA (15:8)   |     |     |     |             |   |   |   |
| LBA High     | LBA (23:16)  |     |     |     |             |   |   |   |
| Device       | obs          | LBA | obs | DEV | LBA (27:24) |   |   |   |
| Command      | C0h          |     |     |     |             |   |   |   |

Sector Count –

number of sectors to be erased. A value of 00h specifies that 256 sectors are to be erased.

LBA Low –

starting LBA bits (7:0).

LBA Mid –

starting LBA bits (15:8).

LBA High –

starting LBA bits (23:16).

Device –

the LBA bit shall be set to one to specify the address is an LBA, starting LBA bits (27:24).

### 8.1.5 Normal outputs

| Register     | 7   | 6    | 5   | 4   | 3  | 2  | 1  | 0   |
|--------------|-----|------|-----|-----|----|----|----|-----|
| Error        | na  |      |     |     |    |    |    |     |
| Sector Count | na  |      |     |     |    |    |    |     |
| LBA Low      | na  |      |     |     |    |    |    |     |
| LBA Mid      | na  |      |     |     |    |    |    |     |
| LBA High     | na  |      |     |     |    |    |    |     |
| Device       | obs | na   | obs | DEV | na | na | na | na  |
| Status       | BSY | DRDY | na  | na  | na | na | na | ERR |

#### Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

ERR shall be cleared to zero.

### 8.1.6 Error outputs

The device shall return command aborted if the command is not supported. An unrecoverable error encountered during execution of this command results in the termination of the command. The command block registers contain the address of the sector where the first unrecovered error occurred.

| Register     | 7           | 6    | 5   | 4    | 3           | 2    | 1  | 0   |
|--------------|-------------|------|-----|------|-------------|------|----|-----|
| Error        | na          | na   | na  | IDNF | na          | ABRT | na | MED |
| Sector Count | na          |      |     |      |             |      |    |     |
| LBA Low      | LBA (7:0)   |      |     |      |             |      |    |     |
| LBA Mid      | LBA (15:8)  |      |     |      |             |      |    |     |
| LBA High     | LBA (23:16) |      |     |      |             |      |    |     |
| Device       | obs         | na   | obs | DEV  | LBA (27:24) |      |    |     |
| Status       | BSY         | DRDY | DF  | na   | na          | na   | na | ERR |

#### Error Register –

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

ABRT shall be set to one if the command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

MED shall be set to one if a media error is detected.

#### LBA Low, LBA Mid, LBA High, Device–

shall be written with the address of first unrecoverable error.

#### Status register –

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

ERR shall be set to one if an Error register bit is set to one.

### 8.1.7 Prerequisites

DRDY set to one.

### 8.1.8 Description

This command pre-erases and conditions from 1 to 256 sectors as specified in the Sector Count register. This command should be issued in advance of a CFA WRITE SECTORS WITHOUT ERASE or a CFA WRITE MULTIPLE WITHOUT ERASE command to increase the execution speed of the write operation.

## 8.2 CFA REQUEST EXTENDED ERROR CODE

### 8.2.1 Command code

03h

### 8.2.2 Feature set

CFA feature set.

- If the CFA feature set is implemented this command shall be implemented.

### 8.2.3 Protocol

Non-data (see 9.4).

### 8.2.4 Inputs

| Register     | 7   | 6  | 5   | 4   | 3  | 2 | 1 | 0 |
|--------------|-----|----|-----|-----|----|---|---|---|
| Features     | na  |    |     |     |    |   |   |   |
| Sector Count | na  |    |     |     |    |   |   |   |
| LBA Low      | na  |    |     |     |    |   |   |   |
| LBA Mid      | na  |    |     |     |    |   |   |   |
| LBA High     | na  |    |     |     |    |   |   |   |
| Device       | obs | na | obs | DEV | na |   |   |   |
| Command      | 03h |    |     |     |    |   |   |   |

### 8.2.5 Normal outputs

The extended error code written into the Error register is an 8-bit code. Table 21 defines these values.

| Register     | 7                   | 6    | 5   | 4   | 3               | 2  | 1  | 0   |
|--------------|---------------------|------|-----|-----|-----------------|----|----|-----|
| Error        | Extended error code |      |     |     |                 |    |    |     |
| Sector Count | Vendor specific     |      |     |     |                 |    |    |     |
| LBA Low      | Vendor specific     |      |     |     |                 |    |    |     |
| LBA Mid      | Vendor specific     |      |     |     |                 |    |    |     |
| LBA High     | Vendor specific     |      |     |     |                 |    |    |     |
| Device       | obs                 | na   | obs | DEV | Vendor specific |    |    |     |
| Status       | BSY                 | DRDY | na  | na  | na              | na | na | ERR |

Error register –

Extended error code.

LBA Low, LBA Mid, LBA High, Device –

May contain additional information.

Status register –

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

ERR shall be cleared to zero.