IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

UNIFICATION TECHNOLOGIES LLC, Plaintiff, v. PHISON ELECTRONICS CORPORATION, Defendant.	§ § § § § § § § § § § §	CIVIL ACTION NO. 2:23-cv-266 **JURY TRIAL DEMANDED**

PLAINTIFF'S COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Unification Technologies LLC files this Complaint against Defendant Phison Electronics Corporation for infringement of U.S. Patent No. 9,575,902 (the "'902 Patent"), U.S. Patent No. 11,061,825, (the "'825 Patent"), U.S. Patent No. 11,573,909 (the "'909 Patent"), and U.S. Patent No. 11,640,359 (the "'359 Patent"), and collectively, the "Asserted Patents."

THE PARTIES

1. Plaintiff Unification Technologies LLC ("UTL") is a Texas Limited Liability Company with its principal place of business at 6136 Frisco Square Boulevard, Suite 400, Frisco, Texas 75034.

2. On information and belief, Phison Electronics Corporation. ("Phison") is a corporation organized and existing under the laws of Taiwan with its principal place of business located at No. 1, Qun Yi Rd., Jhunan, Miaoli, 350 Taiwan. Phison is a market leader in NAND flash controllers and related products sold and distributed in the United States and the world, generally. Phison conducts business in Texas and, particularly, the Eastern District of Texas,

directly or through intermediaries (including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, or others).

3. According to Phison's website, Phison "is now a market leader in NAND Flash controllers and applications including USB, SD, eMMC, PATA, SATA, PCle, and UFS. The company has shipped over 600 million controllers worldwide yearly and topped over US 2.2 billion dollars in sales revenue (2021)." https://www.phison.com/en/company/about-us.

JURISDICTION AND VENUE

4. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq*. This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) and 1367.

5. This Court has specific and personal jurisdiction over Phison consistent with the requirements of the Due Process Clause of the United States Constitution and the Texas Long Arm Statute (*see* Tex. Civ. Prac. & Rem. Code §§17.041 *et seq*.) because, among other things, (i) Phison has done and continues to do business in Texas, and (ii) Phison has committed and continues to commit, directly or through intermediaries (including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others), acts of patent infringement in this State and this District. Such acts of infringement include making, using, offering to sell, and/or selling Accused Products (as more particularly identified and described throughout this Complaint) in this State and this District and/or importing Accused Products into this State and/or inducing others to commit acts of patent infringement in this State. Indeed, Phison has purposefully and voluntarily placed, and is continuing to place, one or more Accused Products into the stream of commerce through established distribution channels (including the Internet) with the expectation and intent that such products will be sold to and purchased by consumers in the United States, this State, and

this District; and with the knowledge and expectation that such products (whether in standalone form or as integrated in downstream products) will be imported into the United States, this State, and this District.

6. Phison has derived substantial revenues from its infringing acts occurring within this State and this District. It has substantial business in this State and this District, including: (i) at least part of its infringing activities alleged herein; and (ii) regularly doing or soliciting business, engaging in other persistent conduct, and/or deriving substantial revenue from infringing goods offered for sale, sold, and imported, and services provided to Texas residents vicariously through and/or in concert with its alter egos, intermediaries, agents, distributors, importers, customers, subsidiaries, and/or consumers.

7. Phison is engaged in making, using, selling, offering for sale, and/or importing products, such as SSD controllers used in PCs and other electronic devices and eMMC/UFS controllers used in smartphones and IoT devices, to and throughout the United States, including this District. Phison also induces its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, and customers in the making, using, selling, offering for sale, and/or importing such products to and throughout the United States, including this District. To this end, Phison and its foreign and U.S.-based subsidiaries—which act together as part of Phison's global network of sales and manufacturing emissaries—have operated as agents of and for one another and have otherwise acted vicariously for Phison as elements of the same business group and/or enterprise. Indeed, they work in concert and in orchestrated fashion, subject to agreements that are far nearer than arm's length, in order to implement a distribution channel of infringing products within this District and the United States.

8. Phison maintains a substantial corporate presence in the United States via at least its U.S.-based affiliate and customers. Phison's website identifies its US counterpart, Phison Technology, Inc. (USA) ("Phison – USA"). https://www.phison.com/en/company/about-us.

9. Upon information and belief, Phison – USA is a corporation organized under the laws of the State of California with a principal place of business at 2526 Qume Drive, Unit 28, San Jose, CA 95131 and is a wholly-owned subsidiary of Phison.

10. Moreover, on information and belief, Phison – USA has registered to conduct business in the State of Texas, including this District, with a registered mailing address of 815 Brazos St., Suite 500, Austin, TX 78701-2509 (Texas Taxpayer ID No. 32086510008).

11. Alone and through at least the activities of its U.S.-based affiliates and subsidiaries (e.g., Phison – USA), Phison conducts business in the United States and this District, including importing, distributing, and selling controllers that are incorporated into devices, systems, and processes that infringe the Asserted Patents. *See Trois v. Apple Tree Auction Center, Inc.*, 882 F.3d 485, 490 (5th Cir. 2018) ("A defendant may be subject to personal jurisdiction because of the activities of its agent within the forum state…."); *see also Cephalon, Inc. v. Watson Pharmaceuticals, Inc.*, 629 F. Supp. 2d 338, 348 (D. Del. 2009) ("The agency theory may be applied not only to parents and subsidiaries, but also to companies that are 'two arms of the same business group,' operate in concert with each other, and enter into agreements with each other that are nearer than arm's length.").

12. Through importation, offers to sell, sales, distributions, and related agreements to transfer ownership of Phison's products (e.g., controllers) with distributors and customers operating in and maintaining significant business presences in the United States, Phison conducts extensive business in the United States, this State, and this District.

13. This Court has personal jurisdiction over Phison, directly or through intermediaries (e.g., subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others), including its U.S.-based affiliates and subsidiaries, *e.g.*, Phison – USA. Through direction and control of such affiliates and subsidiaries, Phison has committed acts of direct and/or indirect patent infringement within this State and elsewhere within the United States giving rise to this action and/or has established minimum contacts with this forum such that the exercise of personal jurisdiction over Phison would not offend traditional notions of fair play and substantial justice. Phison - USA is a wholly-owned affiliate of Phison. On information and belief, the primary business of Phison – USA is the research, development, support, and/or sale of Phison's electronic products in the United States. As such, Phison has a direct financial interest in its U.S.-based subsidiaries and affiliates, and vice versa.

14. On information and belief, Phison controls and otherwise directs and authorizes activities of its U.S.-based subsidiary Phison - USA. Such directed and authorized activities include, the U.S.-based subsidiaries using, offering for sale, selling, and/or importing the Accused Products, their components, and/or products containing the same that incorporate and/or perform the fundamental technologies covered by the Asserted Patents. Phison's U.S.-based subsidiary is expressly authorized to import, distribute, offer to sell, and sell the Accused Products on behalf of Phison. For example, on information and belief, Phison researches, designs, develops, and manufactures controllers, and then directs its U.S.-based subsidiary to import, distribute, offer for sale, and sell the Accused Products in the United States. *See, e.g., United States v. Hui Hsiung*, 778 F.3d 738, 743 (9th Cir. 2015) (finding that the sale of infringing products to third parties rather than for direct import into the U.S. did not "place [defendants'] conduct beyond the reach of United States law [or] escape culpability under the rubric of extraterritoriality"). Phison's U.S.-based

subsidiary also provides, on Phison's behalf, marketing and technical support services for the Accused Products from their facilities in the United States.

15. On information and belief, because Phison's U.S.-based subsidiary is authorized by Phison to import, distribute, offer to sell, and sell Accused Products and/or to perform the fundamental technologies covered by the Asserted Patents, Phison's U.S.-based subsidiary's corporate presence in the United States give Phison substantially the same business advantages it would enjoy if it conducted its business through its own offices and personnel.

16. In addition, on information and belief, Phison has knowingly induced, and continues to knowingly induce, infringement within this District by advertising, marketing, offering for sale and/or selling Accused Products (such as controllers) that incorporate the fundamental technologies covered by the Asserted Patents. Such advertising, marketing, offering for sale and/or selling of Accused Products is directed to manufacturers, integrators, suppliers, distributors, resellers, partners, consumers, customers, and/or end users, and this includes providing instructions, user manuals, advertising, and/or marketing materials facilitating, directing and encouraging use of infringing functionality with Phison's knowledge thereof.

17. Using established channels and chains of distribution, Phison provides Accused Products to be used as components in a variety of end-products that are made, used, sold, and imported into the United States and this District. Phison knew or should have known that by purposefully placing the Accused Products into the stream of commerce, those Accused Products would be sold and used in the United States and this District.

18. On information and belief, Phison provides Accused Products to be used as components in many end-products sold, used, and imported into the United States and this District. For example, Phison states in its 2022 annual report that "our controllers are sold to Tier-1 NAND

vendors such as KIOXIA, Kingston, and Micron, and our system application NAND module products are also sold to major brand customers and system integrators in the U.S., Europe, and Japan . . . ." Phison Elec. Corp. 2002 Annual Report, https://www.phison.com/en/investor-relations/annual-reports?download=1232:2022-en (last accessed May 22, 2023). On information and belief, these Tier-1 NAND vendors and major brand customers sell, use, or import various end-products in the United States and this District that use the Accused Products as components.

19. Upon information and belief, Phison encourages and instructs users of Phison's Accused Products in an infringing manner.

20. Phison has, thus, in the multitude of ways described above, availed itself of the benefits and privileges of conducting business in the United States and this District and willingly subjected itself to the exercise of this Court's personal jurisdiction. Indeed, Phison has sufficient minimum contacts with this forum through its transaction of substantial business in this State and this District and its commission of acts of patent infringement as alleged in this Complaint that are purposefully directed towards this State and District.

21. Alternatively, the Court maintains personal jurisdiction over Phison under Federal Rule of Civil Procedure 4(k)(2).

22. Venue is proper in this District pursuant to 28 U.S.C. § 1391 because, among other things, Phison is not a resident of the United States, and thus may be sued in any judicial district, including this one, pursuant to 28 U.S.C. § 1391(c)(3). *See In re HTC Corp.*, 889 F.3d 1349, 1357 (Fed. Cir. 2018) (holding that "[t]he Court's recent decision in *TC Heartland* does not alter" the alien-venue rule.).

THE PATENTS-IN-SUIT

23. UTL is the sole and exclusive owner of all right, title, and interest in the '902 Patent, the '825 Patent, the '909 Patent, and the '359 Patent, and holds the exclusive right to take all

actions necessary to enforce its rights in, and to, the Asserted Patents, including the filing of this patent infringement lawsuit. UTL also has the right to recover all damages for past, present, and future infringements of the Asserted Patents and to seek injunctive relief as appropriate under the law.

24. The ’902 Patent is titled, “Apparatus, system, and method for managing commands of solid-state storage using bank interleave.” The ’902 Patent lawfully issued on February 21, 2017, and stems from U.S. Patent Application No. 11/952,095, which was filed on December 6, 2007.

25. The ’825 Patent is titled, “Apparatus, system, and method for managing commands of solid-state storage using bank interleave.” The ’825 Patent lawfully issued on July 13, 2021, and stems from U.S. Patent Application No. 15/402,936, which was filed on January 10, 2017.

26. The ’909 Patent is titled, “Apparatus, system, and method for managing commands of solid-state storage using bank interleave.” The ’909 Patent lawfully issued on February 7, 2023, and stems from U.S. Patent Application No. 17/343,116, which was filed on June 9, 2021.

27. The ’359 Patent is titled, “Systems and methods for identifying storage resources that are not in use.” The ’359 Patent lawfully issued on May 2, 2023, and stems from U.S. Patent Application No. 16/543,464, which was filed on August 16, 2019.

28. UTL and its predecessors complied with the requirements of 35 U.S.C. § 287, to the extent necessary, such that UTL may recover pre-suit damages.

29. The claims of the patents-in-suit are directed to patent eligible subject matter under 35 U.S.C. § 101. They are not directed to an abstract idea, and the technologies covered by the claims comprise systems and/or consist of ordered combinations of features and functions that, at the time of invention, were not, alone or in combination, well-understood, routine, or conventional.

DEFENDANT'S PRE-SUIT KNOWLEDGE OF ITS INFRINGEMENT

30. UTL sent a letter to Phison prior to filing this Complaint identifying the Asserted Patents as being infringed by exemplary Phison products, and further included claim charts demonstrating how the identified products infringe the Asserted Patents.

31. The Accused Products addressed in the Counts below include, but are not limited to, the exemplary products identified in UTL's letter to Phison. Phison's past and continuing sales of the Accused Products (i) willfully infringe the Asserted Patents, and (ii) impermissibly usurp the significant benefits of UTL's patented technologies without fairly compensating UTL.

COUNT I

(INFRINGEMENT OF U.S. PATENT NO. 9,575,902)

32. Plaintiff incorporates the preceding paragraphs herein by reference.

33. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

34. UTL is the owner of all substantial rights, title, and interest in and to the '902 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

35. The '902 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on February 21, 2017, after full and fair examination.

36. Phison has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '902 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Phison products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '902 Patent, including, but not limited to, the Phison SSD Controllers, including

but not limited to Phison's Consumer, Embedded and Enterprise SSD Controllers, such as for example Phison's PS5026-E26 PCIe Gen5 SSD Controller or X1 SSD Platform, (collectively, the "'902 Accused Products").

Direct Infringement (35 U.S.C. § 271(a))

37. Phison has directly infringed and continues to directly infringe one or more claims of the'902 Patent in this District and elsewhere in Texas and the United States.

38. Phison has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the '902 Patent[1] as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the '902 Accused Products. Furthermore, Phison makes and sells the '902 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the '902 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '902 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, Phison directly infringes the '902 Patent through its direct involvements in, and control of, the activities of its subsidiaries and/or affiliates, including Phison – USA. Subject to Phison's direction and control, such subsidiaries and affiliates conduct activities that constitute direct infringement of the '902 Patent under 35 U.S.C. § 271(a) by making, offering for sale,

[1] Throughout this Complaint, wherever UTL identifies specific claims of the Asserted Patents infringed by Phison, UTL expressly reserves the right to identify additional claims and products in its infringement contentions in accordance with applicable local rules and the Court's case management order. Specifically identified claims throughout this Complaint are provided for notice pleading only.

selling, and/or importing ’902 Accused Products. Phison receives direct financial benefit from such infringements of its U.S.-based subsidiaries and/or affiliates, including Phison – USA.

39. By way of illustration only, the ’902 Accused Products perform each and every element of claim 1 of the ’902 Patent. As shown below, the ’902 Accused Products perform a method for controlling execution of storage commands on non-volatile solid-state storage in accordance with the requirements of claim 1. Further, Phison directs or controls each step discussed below by including instructions and directives, such as firmware and source code, in the Accused Products that cause this to occur. For example, PS5026-E26 PCIe Gen 5 SSD Controller performs such a method:

“PS5026-E26 PCIe Gen5 SSD Controller,” Product Brochure, Phison Electronics, 2022: https://www.phison.com/images/products_datasheet/ProductBrochure_Consumer_PS5026-E26_12192022.pdf

40. The ’902 Accused Products comprise circuitry implementing a method to receive storage commands at respective command queues, each command queue associated with one of two or more banks of a non-volatile solid-state storage device, wherein the storage commands include storage commands of a first type received in an order at a first command queue associated with a first one of the banks and storage commands of a second, different type, received in an order at a second command queue associated with a second one of the banks. For example, the PS5026-E26 PCIe Gen 5 SSD controller implements the NVM Express (NVMe) 2.0 interface that “allows host software to communicate with a non-volatile memory subsystem.” See “NVM Express Revision 2.0 Base Specification,” May 13, 2021, at 2.

CONTROLLER

PS5026-E26

Features	Specifications
Host Interface	- PCIe 5.0x4 (Bandwidth: 32GT/s x4) - Backward Compatible with Existing PCIe Generation Transfer Rates - Compliance with PCI Express Base Specification Revision 5.0 - Compliance with NVMe 2.0
Processor	- Dual-CPU architecture with built-in Arm Cortex-R5 - TSMC 12nm process technology
Flash Controller	- Up to 8 Channels with 32 Chips Enable (CE) - Flash transfer rate up to 2,400MT/s - Support 3D TLC and QLC NAND flash memory - Compliance with Toggle 5.0 and ONFi 5.0 - Flash I/O operating voltage supply 1.2V
DRAM Controller	- LPDDR4 and DDR4 both supported, transfer rate up to 3200Mbp/s
Data Reliability	- Phison 5th generation LDPC ECC & RAID ECC - SmartECC (RAID ECC) - End-To-End Data Path Protection
Security	- AES 256 - SHA 512 - RSA 4096 - TCG Opal
Performance	- Sequential Read up to 14,000MB/s - Sequential Write up to 11,800MB/s - 4K Random Read up to 1,500K IOPS - 4K Random Write up to 2,000K IOPS
Power Management	- ASPM + APST Supported
Temperature Range	- Operating range: 0~70 °C - Storage range: -40~85 °C - Operating junction temperature: -40~125 °C
Package	- 576-ball FCCSP, 16 mm x 16 mm
Peripheral	- Built-in internal thermal sensor - GPIO pins - Built-in UART function - I3C and SPI for external ROM

"PS5026-E26 PCIe Gen5 SSD Controller," Product Brochure, Phison Electronics, 2022: https://www.phison.com/images/products_datasheet/ProductBrochure_Consumer_PS5026-E26_12192022.pdf

41. Under the NVMe 2.0 interface, "the host software submits commands to the controller through pre-allocated Submission Queues."

When using a memory-based transport implementation (e.g. PCIe), host software submits commands to a controller through pre-allocated Submission Queues. A controller is alerted to newly submitted commands through SQ Tail Doorbell register writes. The difference between the previous doorbell register value and the current register write indicates the number of commands that were submitted.

A controller fetches commands from the Submission Queue(s) and processes them. Except for fused operations, there are no ordering restrictions for processing of commands within or across Submission Queues. Host software should not submit commands to a Submission Queue that may not be re-ordered arbitrarily. Data associated with the processing of a command may or may not be committed to the NVM subsystem non-volatile memory storage medium in the order that commands are submitted.

"NVM Express Revision 2.0 Base Specification," May 13, 2021, at 31.

42. The NVMe 2.0 interface provides that there are Submission Queues in the Controller Memory buffer that allows the host to write the entire submission queue entry (command) to the controller's internal memory space thus avoiding one read from the controller to the host.

> Submission Queues in host memory require the controller to perform a PCI Express read from host memory in order to fetch the submission queue entries. Submission Queues in controller memory enable host software to directly write the entire submission queue entry to the controller's internal memory space, avoiding one read from the controller to the host. This approach reduces latency in command execution and improves efficiency in a PCI Express fabric topology that may include multiple switches. Similarly, PRP Lists or SGLs require separate fetches across the PCI Express fabric, which may be avoided by writing the PRP or SGL to the Controller Memory Buffer. Completion Queues in the Controller Memory Buffer may be used for peer to peer or other applications. For writes of small amounts of data, it may be advantageous to have the host write the data and/or metadata to the Controller Memory Buffer rather than have the controller fetch it from host memory.

"NVM Express Revision 2.0 Base Specification," May 13, 2021, at 350.

43. The submission queues in the Controller Memory Buffer include at least I/O Submission Queue and Admin Submission Queues. See, e.g., id. at 6 (1.51 Admin Queue); id. at 8 (1.5.14 Controller ". . . All controllers implement one Admin Submission Queue and one Admin Completion Queue. Depending on the controller type, a controller may also implement one or more I/O Submission Queues and I/O Completion Queues."); id. at 9 (1.5.33 I/O Submission Queue).

Figure 160: Create I/O Submission Queue – Command Dword 11

Bits	Description
00	**Physically Contiguous (PC):** If set to '1', then the Submission Queue is physically contiguous and PRP Entry 1 (PRP1) is the address of a contiguous physical buffer. If cleared to '0', then the Submission Queue is not physically contiguous and PRP Entry 1 (PRP1) is a PRP List pointer. If this bit is cleared to '0' and CAP.CQR is set to '1', then the controller should return an error of Invalid Field in Command. If the: • queue is located in the Controller Memory Buffer; • PC is cleared to '0'; and • CMBLOC.CQPDS is cleared to '0', then the controller shall abort the command with Invalid Use of Controller Memory Buffer status.

"NVM Express Revision 2.0 Base Specification," May 13, 2021, at 158.

> Support for Sanitize commands in a Controller Memory Buffer (i.e., submitted to an Admin Submission Queue in a Controller Memory Buffer or specifying an Admin Completion Queue in a Controller Memory Buffer) is implementation specific. If an implementation does not support Sanitize commands in a Controller Memory Buffer and a controller's Admin Submission Queue or Admin Completion Queue is in the Controller Memory Buffer, then the controller shall abort all Sanitize commands with a status code of Command Not Supported for Queue in CMB.

"NVM Express Revision 2.0 Base Specification," May 13, 2021, at 283.

44. The NVMe 2.0 interface defines a namespace as a formatted quantity of non-volatile memory accessible by a host. A namespace is also associated with an I/O Command Set that operates on that namespace. The NVMe 2.0 interface provides the common command format of the NVMe 2.0 interface includes a namespace identifier (NSID) which specifies the namespace that the command applies to. The NVMe 2.0 interface additionally defines a command as being processed when "the controller and/or namespace state is being accessed or modified by the command." Id. at 106.

> A namespace is a formatted quantity of non-volatile memory that may be accessed by a host. Associated with each namespace is an I/O Command Set that operates on that namespace. An NVM Express controller may support multiple namespaces that are referenced using a namespace ID. Namespaces may be created and deleted using the Namespace Management and Capacity Management commands. The Identify Namespace data structure, the I/O Command Set specific Identify Namespace data structure, and the I/O Command Set Independent Identify Namespace data structure indicate capabilities and settings that are specific to a particular namespace.

"NVM Express Revision 2.0 Base Specification," May 13, 2021, at 16.

Figure 87: Common Command Format

Bytes	Description
03:00	**Command Dword 0 (CDW0):** This field is common to all commands and is defined in Figure 86.
07:04	**Namespace Identifier (NSID):** This field specifies the namespace that this command applies to. If the namespace identifier is not used for the command, then this field shall be cleared to 0h. The value FFFFFFFFh in this field is a broadcast value (refer to section 3.2.1.2), where the scope (e.g., the NVM subsystem, all attached namespaces, or all namespaces in the NVM subsystem) is dependent on the command. Refer to Figure 138 and Figure 390 for commands that support the use of the value FFFFFFFFh in this field. Specifying an inactive namespace identifier (refer to section 3.2.1.4) in a command that uses the namespace identifier shall cause the controller to abort the command with a status code of Invalid Field in Command, unless otherwise specified. Specifying an invalid namespace identifier (refer to section 3.2.1.2) in a command that uses the namespace identifier shall cause the controller to abort the command with a status code of Invalid Namespace or Format, unless otherwise specified. If the namespace identifier is used for the command (refer to Figure 138), the value FFFFFFFFh is not supported for that command, and the host specifies a value of FFFFFFFFh, then the controller should abort the command with a status code of Invalid Field in Command, unless otherwise specified. If the namespace identifier is not used for the command and the host specifies a value from 1h to FFFFFFFFh, then the controller should abort the command with a status code of Invalid Field in Command, unless otherwise specified.
11:08	**Command Dword 2 (CDW2):** This field is command specific Dword2.
15:12	**Command Dword 3 (CDW3):** This field is command specific Dword3.

"NVM Express Revision 2.0 Base Specification," May 13, 2021, at 92.

45. The NVMe 2.0 interface also supports launching and executing multiple commands from a submission queue in parallel by configuring an Arbitration Burst. "Arbitration burst" is defined as "[t]he maximum number of commands that may be fetched by an arbitration mechanism at one time from a Submission Queue." *Id*. at 7 (1.5.3 arbitration burst).

> In order to make efficient use of the non-volatile memory, it is often advantageous to execute multiple commands from a Submission Queue in parallel. For Submission Queues that are using weighted round robin with urgent priority class or round robin arbitration, host software may configure an Arbitration Burst setting. The Arbitration Burst setting indicates the maximum number of commands that the controller may launch at one time from a particular Submission Queue. It is recommended that host software configure the Arbitration Burst setting as close to the recommended value by the controller as possible (specified in the Recommended Arbitration Burst field of the Identify Controller data structure in Figure 275), taking into consideration any latency requirements. Refer to section 5.27.1.1.

"NVM Express Revision 2.0 Base Specification," May 13, 2021, at 106.

46. As another example of the '902 Accused Products comprising circuitry implementing the method of claim 1, for example, the PS5026-E26 PCIe Gen 5 SSD controller implements the Open NAND Flash Interface (ONFI) 5.0 standardized NAND Flash device interface.

CONTROLLER

PS5026-E26

Features	Specifications
Host Interface	- PCIe 5.0x4 (Bandwidth: 32GT/s x4) - Backward Compatible with Existing PCIe Generation Transfer Rates - Compliance with PCI Express Base Specification Revision 5.0 - Compliance with NVMe 2.0
Processor	- Dual-CPU architecture with built-in Arm Cortex-R5 - TSMC 12nm process technology
Flash Controller	- Up to 8 Channels with 32 Chips Enable (CE) - Flash transfer rate up to 2,400MT/s - Support 3D TLC and QLC NAND flash memory - Compliance with Toggle 5.0 and ONFi 5.0 - Flash I/O operating voltage supply 1.2V
DRAM Controller	- LPDDR4 and DDR4 both supported, transfer rate up to 3200Mbp/s
Data Reliability	- Phison 5th generation LDPC ECC & RAID ECC - SmartECC (RAID ECC) - End-To-End Data Path Protection
Security	- AES 256 - SHA 512 - RSA 4096 - TCG Opal
Performance	- Sequential Read up to 14,000MB/s - Sequential Write up to 11,800MB/s - 4K Random Read up to 1,500K IOPS - 4K Random Write up to 2,000K IOPS
Power Management	- ASPM + APST Supported
Temperature Range	- Operating range: 0~70 °C - Storage range: -40~85 °C - Operating junction temperature: -40~125 °C
Package	- 576-ball FCCSP, 16 mm x 16 mm
Peripheral	- Built-in internal thermal sensor - GPIO pins - Built-in UART function - I3C and SPI for external ROM

"PS5026-E26 PCIe Gen5 SSD Controller," Product Brochure, Phison Electronics, 2022: https://www.phison.com/images/products_datasheet/ProductBrochure_Consumer_PS5026-E26_12192022.pdf

47. ONFI 5.0 NAND flash interface provides that only one Logical Unit (LUN), which is defined as the "minimum unit that can independently execute commands," can be selected for data output at any particular time. "Open NAND Flash Interface (ONFI) Specification, Revision 5.0," May 25, 2021, at 88.

3.1.2. Logical Unit Selection

Logical units that are part of a NAND Target share a single data bus with the host. The host shall ensure that only one LUN is selected for data output to the host at any particular point in time to avoid bus contention.

The host selects a LUN for future data output by issuing a Read Status Enhanced command to that LUN. The Read Status Enhanced command shall deselect the output path for all LUNs that are not addressed by the command. The page register selected for output within the LUN is determined by the previous Read (Cache) commands issued and is not impacted by Read Status Enhanced.

"Open NAND Flash Interface (ONFI) Specification, Revision 5.0," May 25, 2021, at 91.

48. The '902 Accused Products, such as for example the PS5026-E26 PCIe Gen 5 SSD controller, comprise circuitry implementing a method to issue commands from the first and second command queues such that execution of a first command of the first type overlaps in time with execution of a second command of the second type.

49. For example, as noted above the PS5026-E26 PCIe Gen 5 SSD controller implements NVMe 2.0 which supports launching and executing multiple commands from a submission queue in parallel by configuring an Arbitration Burst that sets a maximum number of commands that may be fetched "at one time" from a Submission queue, i.e. before fetching commands from another queue.

In order to make efficient use of the non-volatile memory, it is often advantageous to execute multiple commands from a Submission Queue in parallel. For Submission Queues that are using weighted round robin with urgent priority class or round robin arbitration, host software may configure an Arbitration Burst setting. The Arbitration Burst setting indicates the maximum number of commands that the controller may launch at one time from a particular Submission Queue. It is recommended that host software configure the Arbitration Burst setting as close to the recommended value by the controller as possible (specified in the Recommended Arbitration Burst field of the Identify Controller data structure in Figure 275), taking into consideration any latency requirements. Refer to section 5.27.1.1.

"NVM Express Revision 2.0 Base Specification," May 13, 2021, at 106.

50. As another example, as noted above the PS5026-E26 PCIe Gen 5 SSD controller implements ONFI 5.0 NAND flash interface which provides that separate logical unit (LUNs) "may operate on arbitrary command sequences in parallel."

A logical unit (LUN) is the minimum unit that can independently execute commands and report status. Specifically, separate LUNs may operate on arbitrary command sequences in parallel. For example, it is permissible to start a Page Program operation on LUN 0 and then prior to the operation's completion to start a Read command on LUN 1. See multiple LUN operation restrictions in section 3.1.3. A LUN contains at least one page register and a Flash array. The number of page registers is dependent on the number of multi-plane operations supported for that LUN. The Flash array contains a number of blocks.

"Open NAND Flash Interface (ONFI) Specification, Revision 5.0," May 25, 2021, at 88.

3.1.3. Multiple LUN Operation Restrictions

LUNs are independent entities. A multiple LUN operation is one in which two or more LUNs are simultaneously processing commands. During multiple LUN operations the individual LUNs involved may be in any combination of busy or ready status

When a Page Program command (80h) is issued on any LUN that is not preceded by an 11h command, all idle LUNs may clear their page registers if the program page register clear enhancement is not supported or enabled. Thus, the host should not begin a Page Program command on a LUN while a Read Page operation is either ongoing or has completed but the data has not been read from another LUN, as the contents of the page register for the Read operation are lost. A Read Page can be issued to one LUN while a Page Program is ongoing within a second LUN without any restriction. If the program page register clear enhancement is enabled, this restriction does not apply.

"Open NAND Flash Interface (ONFI) Specification, Revision 5.0," May 25, 2021, at 91.

51. The '902 Accused Products, such as for example the PS5026-E26 PCIe Gen 5 SSD controller, comprise circuitry implementing a method wherein an execution duration of the first command is at least an order of magnitude greater than an execution duration of the second command.

52. On information and belief, the execution duration of at least some of the Admin Commands submitted for example through the Admin Submission Queue (see "NVM Express Revision 2.0 Base Specification," May 13, 2021, at Section 5) is at least an order of magnitude greater than an execution duration of an I/O command submitted for example to an I/O Submission Queue (see *id*. at Section 5). Additionally, the ONFI 5.0 NAND flash interface provides that tADL (used for Program operations) is an order of magnitude greater than tWHR (used for ReadID, Read Status, and Read Status Enhanced commands), and tWC (write cycle time):

Constant Timing Parameter Values			
	Min	Max	Unit
tADL	400	—	ns
tAR	10	—	ns
tCAH	5	—	ns
tCAS	5	—	ns
tCALH	5	—	ns
tCALS	15	—	ns
tCEH	20	—	ns
tCH	5	—	ns
tCS	20	—	ns
tCS1	30	—	ns
tCS2	40	—	ns
tCSD	10	—	ns
tCHZ	—	30	ns
tCLHZ	—	30	ns
tCLR	10	—	ns
tCR	10	—	ns
tCR2	100	—	ns
tCR2 (Read ID)[1]	150	—	ns
tDBS	5	—	ns
tRHW	100	—	ns
tWC	25	—	ns
tWH	11	—	ns
tWP	11	—	ns
tWHR	80	—	ns
tWHRT	400	—	ns
tWTRN	—	200	µs
tWW	100	—	ns
tFEAT	—	1	µs
tITC	—	1	µs
tRST	—	18/30/500	µs
tRR	20	—	ns
tWB	—	100	ns

NOTE:
1. tCR2(min) is 150ns for Read ID sequence only. For all other command sequences tCR2(min) requirement is 100ns.

Table 4-73 NV-DDR2 / NV-DDR3 Timing Parameter Values: Command and Address

"Open NAND Flash Interface (ONFI) Specification, Revision 5.0," May 25, 2021, at 181.

Constant Timing Parameter Values			
	Min	Max	Unit
tADL	400	400	ns
tAR	10	—	ns
tCAH	5	—	ns
tCAS	5	—	ns
tCALH	5	—	ns
tCALS	15	—	ns
tCEH	20	—	ns
tCH	5	—	ns
tCS	20	—	ns
tCS1	30	—	ns
tCS2	40	—	ns
tCSD	10	—	ns
tCHZ	—	30	ns
tCLHZ	—	30	ns
tCLR	10	—	ns
tCR	10	—	ns
tCR2	100	—	ns
tCR2 (Read ID)[1]	150	—	ns
tDBS	5	—	ns
tRHW	100	—	ns
tWC	25	—	ns
tWH	11	—	ns
tWP	11	—	ns
tWHR	80	—	ns
tWHRT	400	—	ns
tWTRN	—	200	µs
tWW	100	—	ns
tFEAT	—	1	µs
tITC	—	1	µs
tRST	—	18/30/500	µs
tRR	20	—	ns
tWB	—	100	ns

NOTE:
1. tCR2(min) is 150ns for Read ID sequence only. For all other command sequences tCR2(min) requirement is 100ns.

Table 4-77 NV-LPDDR4 Timing Parameter Values: Command and Address

"Open NAND Flash Interface (ONFI) Specification, Revision 5.0," May 25, 2021, at 188.

53. The ’902 Accused Products, such as for example the PS5026-E26 PCIe Gen 5 SSD controller, comprise circuitry implementing a method to issue commands from the first command queue in an order different than the order in which the commands were received at the first command queue.

54. For example, under the NVMe 2.0 interface, the controller can fetch commands in order from the Submission Queue but may execute those commands in any order:

> A Submission Queue (SQ) is a circular buffer with a fixed slot size that the host software uses to submit commands for execution by the controller. The host software updates the appropriate SQ Tail doorbell register when there are one to *n* new commands to execute. The previous SQ Tail value is overwritten in the controller when there is a new doorbell register write. The controller fetches SQ entries in order from the Submission Queue and may execute those commands in any order.

“NVM Express Revision 2.0 Base Specification,” May 13, 2021, at 18.

> A candidate command is a submitted command which has been transferred into the controller that the controller deems ready for processing. The controller selects command(s) for processing from the pool of submitted commands for each Submission Queue. The commands that comprise a fused operation shall be processed together and in order by the controller. The controller may select candidate commands for processing in any order. The order in which commands are selected for processing does not imply the order in which commands are completed.

“NVM Express Revision 2.0 Base Specification,” May 13, 2021, at 106.

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

55. In addition and/or in the alternative to its direct infringements, Phison has indirectly infringed and continues to indirectly infringe one or more claims of the ’902 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’902 Accused Products.

56. At a minimum, Phison has knowledge of the ’902 Patent since being served with this Complaint. Phison also has knowledge of the ’902 Patent since receiving detailed correspondence from UTL prior to the filing of the Complaint, alerting Phison to its infringements. Since receiving notice of its infringements, Phison has actively induced the direct infringements

of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the ’902 Patent. Indeed, Phison has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the ’902 Accused Products; creating and/or maintaining established distribution channels for the ’902 Accused Products into and within the United States; manufacturing the ’902 Accused Products in conformity with U.S. laws and regulations; providing technical documentation and tools for the ’902 Accused Products, including product brochures, and descriptions of the features and technologies[2]; promoting the incorporation of the ’902 Accused Products into end-user products.

Damages

57. On information and belief, despite having knowledge of the ’902 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the ’902 Patent, Phison has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Phison’s infringing activities relative to the ’902 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that UTL is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

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[2] *See, e.g.*, https://www.phison.com/en/solutions/consumer/pc-laptop; https://www.phison.com/en/solutions/embedded; https://www.phison.com/en/solutions/enterprise; and the product brochures linked therefrom (last visited May 22, 2023).

58. UTL has been damaged as a result of Phison's infringing conduct described in this Count. Phison is, thus, liable to UTL in an amount that adequately compensates UTL for Phison's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT II

(INFRINGEMENT OF U.S. PATENT NO. 11,061,825)

59. Plaintiff incorporates the preceding paragraphs herein by reference.

60. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

61. UTL is the owner of all substantial rights, title, and interest in and to the '825 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

62. The '825 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on July 13, 2021, after full and fair examination.

63. Phison has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '825 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Phison products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '825 Patent, including, but not limited to, the Phison SSD Controllers, including but not limited to Phison's Consumer, Embedded and Enterprise SSD Controllers, such as for example Phison's PS5018-E18 PCIe Gen4 SSD or X1 SSD Platform, (collectively, the "'825 Accused Products").

Direct Infringement (35 U.S.C. § 271(a))

64. Phison has directly infringed and continues to directly infringe one or more claims of the ’825 Patent in this District and elsewhere in Texas and the United States.

65. Phison has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claims 1 of the ’825 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing, the ’825 Accused Products. Furthermore, Phison makes and sells the ’825 Accused Products outside of the United States and either, delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the ’825 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the ’825 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, Phison directly infringes the ’825 Patent through its direct involvements in, and control of, the activities of its subsidiaries and/or affiliates, including Phison – USA. Subject to Phison’s direction and control, such subsidiaries and/or affiliates conduct activities that constitute direct infringement of the ’825 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing ’825 Accused Products. Phison receives direct financial benefit from such infringements of its U.S.-based subsidiaries and affiliates, including Phison – USA.

66. By way of illustration only, the ’825 Accused Products include each and every element of claim 1 of the ’825 Patent. As shown below, the ’825 Accused Products either comprise a system including a solid state storage device or are configured for inclusion in such a system. For example, Phison’s X1 SSD Platform are a system including a solid state storage device. Additionally, the Accused Phison Motion SSD controllers, including, but not limited to, the Phison

PS5018-E18 PCIe Gen4 SSD controller are configured for inclusion in a system including a solid-state storage device.

PHISON

ENTERPRISE

X1 SSD Platform: Best-in-Class U.3 Enterprise PCIe Gen4x4 eTLC SSD

Customizable Platform

Exceptional Performance at Low Power PCIe Gen4x4 Dual Port.
Our most advanced SSD ever built. The X1 SSD platform has unrivaled performance while also consuming the least amount of power of drives in its class.
This is accomplished utilizing Phison's unique and patented CPU architecture. The X1 SSD solution CPU complex is composed of two performance and power efficient ARM R5 CPUs and dozens of small CPU co-processors that complete computationally heavy, redundant tasks at high speed with a minimum of power consumption.

Joint Development with Seagate
The X1 SSD platform was created in partnership with Seagate, the industry's #1 most trusted brand in Enterprise Storage. Seagate and Phison's engineering teams collaborated in the architecture, features, and development of the X1 SSD solution. Seagate's drive validation lab performed extensive systems and environmental testing to ensure the SSD has world-class reliability.

"X1 SSD Platform," Product Brochure, Phison, 2022; https://www.phison.com/phocadownload/X1-SSD/1285818_ProductBrochure_Enterprise_X1_080122.pdf

Controller **PS5018-E18**

Features	Specifications
Host Interface	• PCIe Gen 4x4 (Bandwidth: 16GT/s x4) • Compatible with PCIe Gen I(2.5Gbps), Gen II(5Gbps), Gen III(8Gbps), Gen IIII(16Gbps) • Compliance with PCI Express Base Specification Revision 4.0 • Compliance with NVMe 1.4
Processor	• Triple-CPU architecture with built-in Arm Cortex-R5 • TSMC 12nm process technology
Flash Controller	• Up to 8 Channels with 32 chips enable (CE) • Flash transfer rate up to 1600MT/s • Capacity up to 8TB • Support 3D TLC and QLC NAND flash memory • Compliance with Toggle 4.0 and ONFi 4.2 • Flash I/O operating voltage supply 1.2V/1.8V
DRAM Controller	• DDR4 (32 bit, 2666Mbps)
Data Reliability	• Phison 4th generation LDPC ECC & RAID ECC • DDR ECC engine • End-To-End Data Path Protection
Security	• Pyrite • AES 256 • SHA 512 • RSA 4096 • TCG Opal
Performance	• Sequential Read up to 7400MB/s • Sequential Write up to 7000MB/s • 4K Random Read up to 1000K IOPS • 4K Random Write up to 1000K IOPS
Power Management	• L1.2 < 5mW

"PS5018-E18 PCIe Gen4 SSD Controller," Product Brochure, Phison Electronics, 2022: https://www.phison.com/images/products_datasheet/Consumer_PS5018-E18_202012.pdf

67. The '825 Accused Products comprise a first controller that directs at least one command to a plurality of queues, wherein the at least one command is separated into the plurality of queues based on a command type of each command of the at least one command, and the plurality of queues comprises a first queue configured to store management commands and a second queue configured to store other commands. For example, the Phison X1 SSD Platform and

PS5018-E18 PCIe Gen4 SSD controller implement the NVM Express (NVMe) 1.4 interface that "allows host software to communicate with a non-volatile memory subsystem." See "NVM Express Revision 1.4c Base Specification," March 9, 2021, at 6.

X1 SSD Platform
Best-in-Class U.3 Enterprise PCIe Gen4x4 eTLC SSD

Capacities	1DWPD: 1.92, 3.84, 7.68, 15.36TB 3DWPD: 1.60, 3.20, 6.40, 12.8TB
Interface	PCIe Gen4x4, NVMe 1.4
Form Factor	U.3, 15mm & 7 mm thickness
NAND Flash	128L 3D eTLC

"X1 SSD Platform," Product Brochure, Phison, 2022; https://www.phison.com/phocadownload/X1-SSD/1285818_ProductBrochure_Enterprise_X1_080122.pdf

Controller **PS5018-E18**

Features	Specifications
Host Interface	• PCIe Gen 4x4 (Bandwidth: 16GT/s x4) • Compatible with PCIe Gen I(2.5Gbps), Gen II(5Gbps), Gen III(8Gbps), Gen IIII(16Gbps) • Compliance with PCI Express Base Specification Revision 4.0 • Compliance with NVMe 1.4
Processor	• Triple-CPU architecture with built-in Arm Cortex-R5 • TSMC 12nm process technology
Flash Controller	• Up to 8 Channels with 32 chips enable (CE) • Flash transfer rate up to 1600MT/s • Capacity up to 8TB • Support 3D TLC and QLC NAND flash memory • Compliance with Toggle 4.0 and ONFi 4.2 • Flash I/O operating voltage supply 1.2V/1.8V

"PS5018-E18 PCIe Gen4 SSD Controller," Product Brochure, Phison Electronics, 2022: https://www.phison.com/images/products_datasheet/Consumer_PS5018-E18_202012.pdf

68. The NVMe 1.4 interface provides that the host software may submit commands to the controller which can be directed to one or more Submission Queues in the Controller Memory Buffer that allows the host to write the entire submission queue entry (command) to the controller's internal memory space thus avoiding one read from the controller to the host.

Host software submits commands to a controller through pre-allocated Submission Queues. A controller is alerted to newly submitted commands through SQ Tail Doorbell register writes. The difference between the previous doorbell register value and the current register write indicates the number of commands that were submitted.

A controller fetches commands from the Submission Queue(s) and processes them. Except for fused operations, there are no ordering restrictions for processing of commands within or across Submission Queues. Host software should not submit commands to a Submission Queue that may not be re-ordered arbitrarily. Data associated with the processing of a command may or may not be committed to the NVM subsystem non-volatile memory storage medium in the order that commands are submitted.

"NVM Express Revision 1.4c Base Specification," March 9, 2021, at 277.

The host enables the CMB's controller memory space via the CMBMSC.CMSE bit. When controller memory space is enabled, if host supplies an address referencing the CMB's controller address range, then the controller directs memory read or write requests for this address to the CMB.

Submission Queues in host memory require the controller to perform a PCI Express read from host memory in order to fetch the queue entries. Submission Queues in controller memory enable host software to directly write the entire Submission Queue Entry to the controller's internal memory space, avoiding one read from the controller to the host. This approach reduces latency in command execution and improves efficiency in a PCI Express fabric topology that may include multiple switches. Similarly, PRP Lists or SGLs require separate fetches across the PCI Express fabric, which may be avoided by writing the PRP or SGL to the Controller Memory Buffer. Completion Queues in the Controller Memory Buffer may be used for peer to peer or other applications. For writes of small amounts of data, it may be advantageous to have the host

"NVM Express Revision 1.4c Base Specification," March 9, 2021, at 85.

69. The Submission Queues in the Controller Memory Buffer include at least I/O Submission Queue (used to submit I/O commands such as Read and Write commands *id*. at 16) and Admin Submission Queues (used to submit administrative commands *id*. at 13); see also *Id*. at 13 (1.6.9 Controller ". . . All controllers implement one Admin Submission Queue and one Admin Completion Queue. Depending on the controller type, a controller may also implement one or more I/O Submission Queues and I/O Completion Queues."); *id*. at 16 (1.6.22 I/O Submission Queue).

Figure 157: Create I/O Submission Queue – Command Dword 11

Bits	Description
00	**Physically Contiguous (PC):** If set to '1', then the Submission Queue is physically contiguous and PRP Entry 1 (PRP1) is the address of a contiguous physical buffer. If cleared to '0', then the Submission Queue is not physically contiguous and PRP Entry 1 (PRP1) is a PRP List pointer. If this bit is cleared to '0' and CAP.CQR is set to '1', then the controller should return an error of Invalid Field in Command. If the: • queue is located in the Controller Memory Buffer; • PC is cleared to '0'; and • CMBLOC.CQPDS is cleared to '0', then the controller shall abort the command with Invalid Use of Controller Memory Buffer status.

"NVM Express Revision 1.4c Base Specification," March 9, 2021, at 104.

Support for Sanitize commands in a Controller Memory Buffer (i.e., submitted to an Admin Submission Queue in a Controller Memory Buffer or specifying an Admin Completion Queue in a Controller Memory Buffer) is implementation specific. If an implementation does not support Sanitize commands in a Controller Memory Buffer and a controller's Admin Submission Queue or Admin Completion Queue is in the Controller Memory Buffer, then the controller shall abort all Sanitize commands with a status of Command Not Supported for Queue in CMB.

"NVM Express Revision 1.4c Base Specification," March 9, 2021, at 239.

70. The '825 Accused Products either comprise a solid-state storage device, such as for example the Phison X1 SSD Platform, or are configured for inclusion in a system including a solid-state storage device, such as for example the Phison PS5018-E18 PCIe Gen4 SSD controller.

"X1 SSD Platform," Product Brochure, Phison, 2022; https://www.phison.com/phocadownload/X1-SSD/1285818_ProductBrochure_Enterprise_X1_080122.pdf

Controller **PS5018-E18**

Features	Specifications
Host Interface	• PCIe Gen 4x4 (Bandwidth: 16GT/s x4) • Compatible with PCIe Gen I(2.5Gbps), Gen II(5Gbps), Gen III(8Gbps), Gen IIII(16Gbps) • Compliance with PCI Express Base Specification Revision 4.0 • Compliance with NVMe 1.4
Processor	• Triple-CPU architecture with built-in Arm Cortex-R5 • TSMC 12nm process technology
Flash Controller	• Up to 8 Channels with 32 chips enable (CE) • Flash transfer rate up to 1600MT/s • Capacity up to 8TB • Support 3D TLC and QLC NAND flash memory • Compliance with Toggle 4.0 and ONFi 4.2 • Flash I/O operating voltage supply 1.2V/1.8V
DRAM Controller	• DDR4 (32 bit, 2666Mbps)
Data Reliability	• Phison 4th generation LDPC ECC & RAID ECC • DDR ECC engine • End-To-End Data Path Protection
Security	• Pyrite • AES 256 • SHA 512 • RSA 4096 • TCG Opal
Performance	• Sequential Read up to 7400MB/s • Sequential Write up to 7000MB/s • 4K Random Read up to 1000K IOPS • 4K Random Write up to 1000K IOPS
Power Management	• L1.2 < 5mW

"PS5018-E18 PCIe Gen4 SSD Controller," Product Brochure, Phison Electronics, 2022: https://www.phison.com/images/products_datasheet/Consumer_PS5018-E18_202012.pdf

71. The '825 Accused Products, such as for example the X1 SSD Platform or PS5018-E18 PCIe Gen4 SSD controller, comprise a second controller configured to receive the at least one command from the plurality of queues, generate subcommands based on the at least one command,

and direct the subcommands to at least one bank of a solid-state storage. For example, as noted above both the X1 SSD Platform or PS5018-E18 PCIe Gen4 SSD controller implement NVMe 1.4 which provides that a controller fetches commands from the Submission Queue(s) and process the commands.

3. The controller transfers the command(s) from in the Submission Queue slot(s) into the controller for future execution. Arbitration is the method used to determine the Submission Queue from which the controller starts processing the next candidate command(s), refer to section 4.13;
4. The controller then proceeds with execution of the next command(s). Commands may complete out of order (the order submitted or started execution);

"NVM Express Revision 1.4c Base Specification," March 9, 2021, at 286.

72. The NVMe 1.4 interface additionally defines a command as being processed when "the controller and/or namespace state is being accessed or modified by the command." *Id.* at 91. A namespace is defined as a formatted quantity of non-volatile memory that may be formatted into logical blocks. NVMe 1.4 interface provides that one or more controllers in an NVM subsystem can access some number of namespaces, (*id*. at 247) and that the various commands of the NVM command set should include a valid namespace ID (NSID) (used by the controller to provide access to a namespace). *id*. at 248. Including an invalid NSID will cause the controller to abort the command. *id*. at 248. Upon information in belief, this processing of commands generates subcommands based on the commands and directs them to at least one bank of the solid-state storage.

Figure 106: Command Format – Admin and NVM Command Set

Bytes	Description
07:04	**Namespace Identifier (NSID):** This field specifies the namespace that this command applies to. If the namespace identifier is not used for the command, then this field shall be cleared to 0h. The value FFFFFFFFh in this field is a broadcast value (refer to section 6.1), where the scope (e.g., the NVM subsystem, all attached namespaces, or all namespaces in the NVM subsystem) is dependent on the command. Refer to Figure 141, Figure 142, and Figure 350 for commands that support the use of the value FFFFFFFFh in this field. Specifying an inactive namespace identifier (refer to section 6.1.4) in a command that uses the namespace identifier shall cause the controller to abort the command with status Invalid Field in Command, unless otherwise specified. Specifying an invalid namespace identifier (refer to section 6.1.2) in a command that uses the namespace identifier shall cause the controller to abort the command with status Invalid Namespace or Format, unless otherwise specified. If the namespace identifier is used for the command (refer to Figure 141 and Figure 142), the value FFFFFFFFh is not supported for that command, and the host specifies a value of FFFFFFFFh, then the controller should abort the command with status Invalid Field in Command, unless otherwise specified. If the namespace identifier is not used for the command and the host specifies a value from 1h to FFFFFFFFh, then the controller should abort the command with status Invalid Field in Command, unless otherwise specified.
15:08	Reserved

"NVM Express Revision 1.4c Base Specification," March 9, 2021, at 67.

73. Additionally, the NVMe 1.4 interface also supports launching and executing multiple commands from a submission que in parallel by configuring an Arbitration Burst. "Arbitration burst" is defined as "[t]he maximum number of commands that may be fetched by an arbitration mechanism at one time from a Submission Queue." *Id.* at 14 (1.6.3 arbitration burst).

> In order to make efficient use of the non-volatile memory, it is often advantageous to execute multiple commands from a Submission Queue in parallel. For Submission Queues that are using weighted round robin with urgent priority class or round robin arbitration, host software may configure an Arbitration Burst setting. The Arbitration Burst setting indicates the maximum number of commands that the controller may launch at one time from a particular Submission Queue. It is recommended that host software configure the Arbitration Burst setting as close to the recommended value by the controller as possible (specified in the Recommended Arbitration Burst field of the Identify Controller data structure in Figure 251), taking into consideration any latency requirements. Refer to section 5.21.1.1.

"NVM Express Revision 1.4c Base Specification," March 9, 2021, at 91.

74. Furthermore, the '825 Accused Products, such as for example the PS5018-E18 PCIe Gen4 SSD Controller, implement the Open NAND Flash Interface (ONFI) 4.2 standardized NAND Flash device interface.

Controller **PS5018-E18**

Features	Specifications
Host Interface	• PCIe Gen 4x4 (Bandwidth: 16GT/s x4) • Compatible with PCIe Gen I(2.5Gbps), Gen II(5Gbps), Gen III(8Gbps), Gen IIII(16Gbps) • Compliance with PCI Express Base Specification Revision 4.0 • Compliance with NVMe 1.4
Processor	• Triple-CPU architecture with built-in Arm Cortex-R5 • TSMC 12nm process technology
Flash Controller	• Up to 8 Channels with 32 chips enable (CE) • Flash transfer rate up to 1600MT/s • Capacity up to 8TB • Support 3D TLC and QLC NAND flash memory • Compliance with Toggle 4.0 and ONFi 4.2 • Flash I/O operating voltage supply 1.2V/1.8V

"PS5018-E18 PCIe Gen4 SSD Controller," Product Brochure, Phison Electronics, 2022: https://www.phison.com/images/products_datasheet/Consumer_PS5018-E18_202012.pdf

75. The ONFI 4.2 NAND flash interface defines Logical Unit (LUN) as "the minimum unit that can independently execute commands." "Open NAND Flash Interface (ONFI) Specification Revision 4.2," February 12, 2020, at 73. The ONFI 4.2 NAND flash interface additionally provides generating subcommands based on a command to be executed. *See id. at* 303. For example, with respect to Read Commands, the ONFI 4.2 NAND flash interface discloses that the target must set tLunSelected to the LUN indicated by the row address received [first subcommand], issue the Read Page with address to the LUN selected [second subcommand], and issue a command requesting all other LUNs not selected to turn off their output buffers [third subcommand]; and after corresponding command cycles are received, the command is passed to the LUN selected for execution.

T_RD_AddrWait	tLastCmd set to 00h. Set tbChgCol to TRUE. Set tbChgColEnh to TRUE. If R/B_n is cleared to zero, then tbStatus78hReq is set to TRUE. Wait for an address cycle.		
1. Address cycle received		→	T_RD_Addr

T_RD_Addr	Store the address cycle received.		
3. More address cycles required		→	T_RD_AddrWait
4. All address cycles received		→	T_RD_LUN_Execute

T_RD_LUN_Execute	The target performs the following actions: 1. tLunSelected is set to the LUN indicated by the row address received. 2. Issues the Read Page with address to LUN tLunSelected. 3. Requests all idle LUNs not selected to turn off their output buffers.[1]		
1. Unconditional		→	T_RD_LUN_Confirm
NOTE: 1. LUNs not selected will only turn off their output buffers if they are in an Idle state. If other LUNs are active, the host shall issue a Read Status Enhanced (78h) command to ensure all LUNs that are not selected turn off their output buffers prior to issuing the Read (00h) command.			

T_RD_LUN_Confirm	Wait for 30h, 31h, 32h, or 35h to be received.		
1. Command cycle of 30h, 31h, 32h, or 35h received		→	T_RD_Cmd_Pass

T_RD_Cmd_Pass	Pass command received to LUN tLunSelected		
1. Command passed was 35h		→	T_RD_Copyback
2. Command passed was 30h, 31h, or 32h		→	T_Idle_Rd

"Open NAND Flash Interface (ONFI) Specification Revision 4.2," February 12, 2020, at 303.

76. The ONFI 4.2 NAND flash interface additionally provides that separate logical units (LUNs) "may operate on arbitrary command sequences in parallel."

> A logical unit (LUN) is the minimum unit that can independently execute commands and report status. Specifically, separate LUNs may operate on arbitrary command sequences in parallel. For example, it is permissible to start a Page Program operation on LUN 0 and then prior to the operation's completion to start a Read command on LUN 1. See multiple LUN operation restrictions in section 3.1.3. A LUN contains at least one page register and a Flash array. The number of page registers is dependent on the number of multi-plane operations supported for that LUN. The Flash array contains a number of blocks.

"Open NAND Flash Interface (ONFI) Specification Revision 4.2," February 12, 2020, at 303.

3.1.3. Multiple LUN Operation Restrictions

LUNs are independent entities. A multiple LUN operation is one in which two or more LUNs are simultaneously processing commands. During multiple LUN operations the individual LUNs involved may be in any combination of busy or ready status

When a Page Program command (80h) is issued on any LUN that is not preceded by an 11h command, all idle LUNs may clear their page registers if the program page register clear enhancement is not supported or enabled. Thus, the host should not begin a Page Program command on a LUN while a Read Page operation is either ongoing or has completed but the data has not been read from another LUN, as the contents of the page register for the Read operation are lost. A Read Page can be issued to one LUN while a Page Program is ongoing within a second LUN without any restriction. If the program page register clear enhancement is enabled, this restriction does not apply.

"Open NAND Flash Interface (ONFI) Specification Revision 4.2," February 12, 2020, at 303.

77. The '825 Accused Products either comprise a solid-state storage, such as for example the X1 SSD Platform, or are configured for inclusion in a system including a solid-state storage, such as for example the PS5018-E18 PCIe Gen4 SSD controller.

X1 SSD Platform
Best-in-Class U.3 Enterprise PCIe Gen4x4 eTLC SSD

Capacities	1DWPD: 1.92, 3.84, 7.68, 15.36TB 3DWPD: 1.60, 3.20, 6.40, 12.8TB
Interface	PCIe Gen4x4, NVMe 1.4
Form Factor	U.3, 15mm & 7 mm thickness
NAND Flash	128L 3D eTLC

"X1 SSD Platform," Product Brochure, Phison, 2022; https://www.phison.com/phocadownload/X1-SSD/1285818_ProductBrochure_Enterprise_X1_080122.pdf

Controller **PS5018-E18**

Features	Specifications
Host Interface	• PCIe Gen 4x4 (Bandwidth: 16GT/s x4) • Compatible with PCIe Gen I(2.5Gbps), Gen II(5Gbps), Gen III(8Gbps), Gen IIII(16Gbps) • Compliance with PCI Express Base Specification Revision 4.0 • Compliance with NVMe 1.4
Processor	• Triple-CPU architecture with built-in Arm Cortex-R5 • TSMC 12nm process technology
Flash Controller	• Up to 8 Channels with 32 chips enable (CE) • Flash transfer rate up to 1600MT/s • Capacity up to 8TB • Support 3D TLC and QLC NAND flash memory • Compliance with Toggle 4.0 and ONFi 4.2 • Flash I/O operating voltage supply 1.2V/1.8V
DRAM Controller	• DDR4 (32 bit, 2666Mbps)
Data Reliability	• Phison 4th generation LDPC ECC & RAID ECC • DDR ECC engine • End-To-End Data Path Protection
Security	• Pyrite • AES 256 • SHA 512 • RSA 4096 • TCG Opal
Performance	• Sequential Read up to 7400MB/s • Sequential Write up to 7000MB/s • 4K Random Read up to 1000K IOPS • 4K Random Write up to 1000K IOPS
Power Management	• L1.2 < 5mW

"PS5018-E18 PCIe Gen4 SSD Controller," Product Brochure, Phison Electronics, 2022: https://www.phison.com/images/products_datasheet/Consumer_PS5018-E18_202012.pdf

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

78. In addition and/or in the alternative to its direct infringements, Phison has indirectly infringed and continues to indirectly infringe one or more claims of the '825 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers,

suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’825 Accused Product.

79. At a minimum, Phison has knowledge of the ’825 Patent since being served with this Complaint. Phison also has knowledge of the ’825 Patent since receiving detailed correspondence from UTL prior to the filing of the Complaint, alerting Phison to its infringements. Since receiving notice of its infringements, Phison has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Indeed, Phison has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the ’825 Accused Products; creating and/or maintaining established distribution channels for the ’825 Accused Products into and within the United States; manufacturing the ’825 Accused Products in conformity with U.S. laws and regulations; distributing or making available videos, training, tools and resources supporting use of the ’825 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the ’825 Accused Products, including product brochures, and descriptions of the features and technologies[3]; promoting the incorporation of the ’825 Accused Products into end-user products.

Damages

80. On information and belief, despite having knowledge of the ’825 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the ’825 Patent,

[3] *See, e.g.*, https://www.phison.com/en/solutions/consumer/pc-laptop; https://www.phison.com/en/solutions/embedded; https://www.phison.com/en/solutions/enterprise; and the product brochures linked therefrom (last visited May 22, 2023).

Phison has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Phison's infringing activities relative to the '825 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that UTL is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

81. UTL has been damaged as a result of Phison's infringing conduct described in this Count. Phison is, thus, liable to UTL in an amount that adequately compensates UTL for Phison's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT III

(INFRINGEMENT OF U.S. PATENT NO. 11,573,909)

82. Plaintiff incorporates the preceding paragraphs herein by reference.

83. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

84. UTL is the owner of all substantial rights, title, and interest in and to the '909 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

85. The '909 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on February 7, 2023, after full and fair examination.

86. Phison has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '909 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Phison products, their components

and processes, and/or products containing the same that incorporate the fundamental technologies covered by the ’909 Patent, including, but not limited to, the Phison SSD Controllers, including but not limited to Phison’s Consumer, Embedded and Enterprise SSD Controllers, such as for example Phison’s PS5018-E18 PCIe Gen4 SSD or X1 SSD Platform, (collectively, the “’909 Accused Products”).

Direct Infringement (35 U.S.C. § 271(a))

87. Phison has directly infringed and continues to directly infringe one or more claims of the’909 Patent in this District and elsewhere in Texas and the United States.

88. Phison has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the ’909 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing, the ’909 Accused Products. Furthermore, Phison makes and sells the ’909 Accused Products outside of the United States and either, delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the ’909 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the ’909 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, Phison directly infringes the ’909 Patent through its direct involvements in, and control of, the activities of its subsidiaries and/or affiliates, including Phison – USA. Subject to Phison’s direction and control, such subsidiaries and/or affiliates conduct activities that constitute direct infringement of the ’909 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing ’909 Accused Products. Phison receives direct financial benefit from such infringements of its U.S.-based subsidiaries and/or affiliates, including Phison – USA.

89. By way of illustration only, the '909 Accused Products include each and every element of claim 1 of the '909 Patent. The '909 Accused Products, such as for example the PS5018-E18 PCIe Gen4 SSD controller or X1 SSD Platform, are a system that includes controllers.

Controller **PS5018-E18**

Features	Specifications
Host Interface	• PCIe Gen 4x4 (Bandwidth: 16GT/s x4) • Compatible with PCIe Gen I(2.5Gbps), Gen II(5Gbps), Gen III(8Gbps), Gen IIII(16Gbps) • Compliance with PCI Express Base Specification Revision 4.0 • Compliance with NVMe 1.4
Processor	• Triple-CPU architecture with built-in Arm Cortex-R5 • TSMC 12nm process technology
Flash Controller	• Up to 8 Channels with 32 chips enable (CE) • Flash transfer rate up to 1600MT/s • Capacity up to 8TB • Support 3D TLC and QLC NAND flash memory • Compliance with Toggle 4.0 and ONFi 4.2 • Flash I/O operating voltage supply 1.2V/1.8V
DRAM Controller	• DDR4 (32 bit, 2666Mbps)
Data Reliability	• Phison 4th generation LDPC ECC & RAID ECC • DDR ECC engine • End-To-End Data Path Protection
Security	• Pyrite • AES 256 • SHA 512 • RSA 4096 • TCG Opal
Performance	• Sequential Read up to 7400MB/s • Sequential Write up to 7000MB/s • 4K Random Read up to 1000K IOPS • 4K Random Write up to 1000K IOPS
Power Management	• L1.2 < 5mW

"PS5018-E18 PCIe Gen4 SSD Controller," Product Brochure, Phison Electronics, 2022: https://www.phison.com/images/products_datasheet/Consumer_PS5018-E18_202012.pdf

PHISON

ENTERPRISE

X1 SSD Platform: Best-in-Class U.3 Enterprise PCIe Gen4x4 eTLC SSD

Customizable Platform

Exceptional Performance at Low Power PCIe Gen4x4 Dual Port.
Our most advanced SSD ever built. The X1 SSD platform has unrivaled performance while also consuming the least amount of power of drives in its class.
This is accomplished utilizing Phison's unique and patented CPU architecture. The X1 SSD solution CPU complex is composed of two performance and power efficient ARM R5 CPUs and dozens of small CPU co-processors that complete computationally heavy, redundant tasks at high speed with a minimum of power consumption.

Joint Development with Seagate
The X1 SSD platform was created in partnership with Seagate, the industry's #1 most trusted brand in Enterprise Storage. Seagate and Phison's engineering teams collaborated in the architecture, features, and development of the X1 SSD solution. Seagate's drive validation lab performed extensive systems and environmental testing to ensure the SSD has world-class reliability.

"X1 SSD Platform," Product Brochure, Phison, 2022; https://www.phison.com/phocadownload/X1-SSD/1285818_ProductBrochure_Enterprise_X1_080122.pdf

90. The '909 Accused Products comprise a first controller that directs at least one command to a plurality of queues, wherein the at least one command is separated into the plurality of queues based on a command type of each command of the at least one command, and the plurality of queues comprises a first queue configured to store management commands and a second queue configured to store other commands, For example, the Phison X1 SSD Platform and PS5018-E18 PCIe Gen4 SSD controller implement the NVM Express (NVMe) 1.4 interface that "allows host software to communicate with a non-volatile memory subsystem." See "NVM Express Revision 1.4c Base Specification," March 9, 2021, at 6.

Controller **PS5018-E18**

Features	Specifications
Host Interface	• PCIe Gen 4x4 (Bandwidth: 16GT/s x4) • Compatible with PCIe Gen I(2.5Gbps), Gen II(5Gbps), Gen III(8Gbps), Gen IIII(16Gbps) • Compliance with PCI Express Base Specification Revision 4.0 • Compliance with NVMe 1.4
Processor	• Triple-CPU architecture with built-in Arm Cortex-R5 • TSMC 12nm process technology
Flash Controller	• Up to 8 Channels with 32 chips enable (CE) • Flash transfer rate up to 1600MT/s • Capacity up to 8TB • Support 3D TLC and QLC NAND flash memory • Compliance with Toggle 4.0 and ONFi 4.2 • Flash I/O operating voltage supply 1.2V/1.8V

"PS5018-E18 PCIe Gen4 SSD Controller," Product Brochure, Phison Electronics, 2022: https://www.phison.com/images/products_datasheet/Consumer_PS5018-E18_202012.pdf

X1 SSD Platform
Best-in-Class U.3 Enterprise PCIe Gen4x4 eTLC SSD

Capacities	1DWPD: 1.92, 3.84, 7.68, 15.36TB 3DWPD: 1.60, 3.20, 6.40, 12.8TB
Interface	PCIe Gen4x4, NVMe 1.4
Form Factor	U.3, 15mm & 7 mm thickness
NAND Flash	128L 3D eTLC

"X1 SSD Platform," Product Brochure, Phison, 2022; https://www.phison.com/phocadownload/X1-SSD/1285818_ProductBrochure_Enterprise_X1_080122.pdf

91. The NVMe 1.4 interface provides that the host software may submit commands to the controller which can be directed to one or more Submission Queues in the Controller Memory Buffer that allows the host to write the entire submission queue entry (command) to the controller's internal memory space thus avoiding one read from the controller to the host.

> Host software submits commands to a controller through pre-allocated Submission Queues. A controller is alerted to newly submitted commands through SQ Tail Doorbell register writes. The difference between the previous doorbell register value and the current register write indicates the number of commands that were submitted.
>
> A controller fetches commands from the Submission Queue(s) and processes them. Except for fused operations, there are no ordering restrictions for processing of commands within or across Submission Queues. Host software should not submit commands to a Submission Queue that may not be re-ordered arbitrarily. Data associated with the processing of a command may or may not be committed to the NVM subsystem non-volatile memory storage medium in the order that commands are submitted.

"NVM Express Revision 1.4c Base Specification," March 9, 2021, at 277.

The host enables the CMB's controller memory space via the CMBMSC.CMSE bit. When controller memory space is enabled, if host supplies an address referencing the CMB's controller address range, then the controller directs memory read or write requests for this address to the CMB.

Submission Queues in host memory require the controller to perform a PCI Express read from host memory in order to fetch the queue entries. Submission Queues in controller memory enable host software to directly write the entire Submission Queue Entry to the controller's internal memory space, avoiding one read from the controller to the host. This approach reduces latency in command execution and improves efficiency in a PCI Express fabric topology that may include multiple switches. Similarly, PRP Lists or SGLs require separate fetches across the PCI Express fabric, which may be avoided by writing the PRP or SGL to the Controller Memory Buffer. Completion Queues in the Controller Memory Buffer may be used for peer to peer or other applications. For writes of small amounts of data, it may be advantageous to have the host

"NVM Express Revision 1.4c Base Specification," March 9, 2021, at 85.

92. The Submission Queues in the Controller Memory Buffer include at least I/O Submission Queue (used to submit I/O commands such as Read and Write commands *id*. at 16) and Admin Submission Queues (used to submit administrative commands *id*. at 13); see also *Id*. at 13 (1.6.9 Controller ". . . All controllers implement one Admin Submission Queue and one Admin Completion Queue. Depending on the controller type, a controller may also implement one or more I/O Submission Queues and I/O Completion Queues."); *id*. at 16 (1.6.22 I/O Submission Queue).

Figure 157: Create I/O Submission Queue – Command Dword 11

Bits	Description
00	**Physically Contiguous (PC):** If set to '1', then the Submission Queue is physically contiguous and PRP Entry 1 (PRP1) is the address of a contiguous physical buffer. If cleared to '0', then the Submission Queue is not physically contiguous and PRP Entry 1 (PRP1) is a PRP List pointer. If this bit is cleared to '0' and CAP.CQR is set to '1', then the controller should return an error of Invalid Field in Command. If the: • queue is located in the Controller Memory Buffer; • PC is cleared to '0'; and • CMBLOC.CQPDS is cleared to '0', then the controller shall abort the command with Invalid Use of Controller Memory Buffer status.

"NVM Express Revision 1.4c Base Specification," March 9, 2021, at 104.

Support for Sanitize commands in a Controller Memory Buffer (i.e., submitted to an Admin Submission Queue in a Controller Memory Buffer or specifying an Admin Completion Queue in a Controller Memory Buffer) is implementation specific. If an implementation does not support Sanitize commands in a Controller Memory Buffer and a controller's Admin Submission Queue or Admin Completion Queue is in the Controller Memory Buffer, then the controller shall abort all Sanitize commands with a status of Command Not Supported for Queue in CMB.

"NVM Express Revision 1.4c Base Specification," March 9, 2021, at 239.

93. The '909 Accused Products, such as for example the X1 SSD Platform PS5018-E18 PCIe Gen4 SSD controller, comprise a second controller configured to receive the at least one command from the plurality of queues, generate subcommands based on the at least one command, and direct the subcommands to at least one bank of a solid-state storage. For example, as noted above both the X1 SSD Platform or PS5018-E18 PCIe Gen4 SSD controller implement NVMe 1.4 which provides that a controller fetches commands from the Submission Queue(s) and process the commands.

3. The controller transfers the command(s) from in the Submission Queue slot(s) into the controller for future execution. Arbitration is the method used to determine the Submission Queue from which the controller starts processing the next candidate command(s), refer to section 4.13;
4. The controller then proceeds with execution of the next command(s). Commands may complete out of order (the order submitted or started execution);

"NVM Express Revision 1.4c Base Specification," March 9, 2021, at 286.

94. The NVMe 1.4 interface additionally defines a command as being processed when "the controller and/or namespace state is being accessed or modified by the command." Id. at 91. A namespace is defined as a formatted quantity of non-volatile memory that may be formatted into logical blocks. NVMe 1.4 interface provides that one or more controllers in an NVM subsystem can access some number of namespaces, (id. at 247) and that the various commands of the NVM command set should include a valid namespace ID (NSID) (used by the controller to provide access to a namespace). id. at 248. Including an invalid NSID will cause the controller to abort the command. id. at 248. Upon information in belief, this processing of commands generates

subcommands based on the commands and directs them to at least one bank of the solid-state storage.

Figure 106: Command Format – Admin and NVM Command Set

Bytes	Description
07:04	**Namespace Identifier (NSID):** This field specifies the namespace that this command applies to. If the namespace identifier is not used for the command, then this field shall be cleared to 0h. The value FFFFFFFFh in this field is a broadcast value (refer to section 6.1), where the scope (e.g., the NVM subsystem, all attached namespaces, or all namespaces in the NVM subsystem) is dependent on the command. Refer to Figure 141, Figure 142, and Figure 350 for commands that support the use of the value FFFFFFFFh in this field. Specifying an inactive namespace identifier (refer to section 6.1.4) in a command that uses the namespace identifier shall cause the controller to abort the command with status Invalid Field in Command, unless otherwise specified. Specifying an invalid namespace identifier (refer to section 6.1.2) in a command that uses the namespace identifier shall cause the controller to abort the command with status Invalid Namespace or Format, unless otherwise specified. If the namespace identifier is used for the command (refer to Figure 141 and Figure 142), the value FFFFFFFFh is not supported for that command, and the host specifies a value of FFFFFFFFh, then the controller should abort the command with status Invalid Field in Command, unless otherwise specified. If the namespace identifier is not used for the command and the host specifies a value from 1h to FFFFFFFFh, then the controller should abort the command with status Invalid Field in Command, unless otherwise specified.
15:08	Reserved

"NVM Express Revision 1.4c Base Specification," March 9, 2021, at 67.

95. Additionally, the NVMe 1.4 interface also supports launching and executing multiple commands from a submission que in parallel by configuring an Arbitration Burst. "Arbitration burst" is defined as "[t]he maximum number of commands that may be fetched by an arbitration mechanism at one time from a Submission Queue." *Id.* at 14 (1.6.3 arbitration burst).

> In order to make efficient use of the non-volatile memory, it is often advantageous to execute multiple commands from a Submission Queue in parallel. For Submission Queues that are using weighted round robin with urgent priority class or round robin arbitration, host software may configure an Arbitration Burst setting. The Arbitration Burst setting indicates the maximum number of commands that the controller may launch at one time from a particular Submission Queue. It is recommended that host software configure the Arbitration Burst setting as close to the recommended value by the controller as possible (specified in the Recommended Arbitration Burst field of the Identify Controller data structure in Figure 251), taking into consideration any latency requirements. Refer to section 5.21.1.1.

"NVM Express Revision 1.4c Base Specification," March 9, 2021, at 91.

96. Furthermore, the '825 Accused Products, such as for example the PS5018-E18 PCIe Gen4 SSD Controller, implement the Open NAND Flash Interface (ONFI) 4.2 standardized NAND Flash device interface.

Controller **PS5018-E18**

Features	Specifications
Host Interface	• PCIe Gen 4x4 (Bandwidth: 16GT/s x4) • Compatible with PCIe Gen I(2.5Gbps), Gen II(5Gbps), Gen III(8Gbps), Gen IIII(16Gbps) • Compliance with PCI Express Base Specification Revision 4.0 • Compliance with NVMe 1.4
Processor	• Triple-CPU architecture with built-in Arm Cortex-R5 • TSMC 12nm process technology
Flash Controller	• Up to 8 Channels with 32 chips enable (CE) • Flash transfer rate up to 1600MT/s • Capacity up to 8TB • Support 3D TLC and QLC NAND flash memory • Compliance with Toggle 4.0 and ONFi 4.2 • Flash I/O operating voltage supply 1.2V/1.8V

"PS5018-E18 PCIe Gen4 SSD Controller," Product Brochure, Phison Electronics, 2022: https://www.phison.com/images/products_datasheet/Consumer_PS5018-E18_202012.pdf

97. The ONFI 4.2 NAND flash interface defines Logical Unit (LUN) as "the minimum unit that can independently execute commands." "Open NAND Flash Interface (ONFI) Specification Revision 4.2," February 12, 2020, at 73. The ONFI 4.2 NAND flash interface additionally provides generating subcommands based on a command to be executed. See id. at 303. For example, with respect to Read Commands, the ONFI 4.2 NAND flash interface discloses that the target must set tLunSelected to the LUN indicated by the row address received [first subcommand], issue the Read Page with address to the LUN selected [second subcommand], and issue a command requesting all other LUNs not selected to turn off their output buffers [third subcommand]; and after corresponding command cycles are received, the command is passed to the LUN selected for execution.

T_RD_AddrWait	tLastCmd set to 00h. Set tbChgCol to TRUE. Set tbChgColEnh to TRUE. If R/B_n is cleared to zero, then tbStatus78hReq is set to TRUE. Wait for an address cycle.		
1. Address cycle received		→	T_RD_Addr

T_RD_Addr	Store the address cycle received.		
3. More address cycles required		→	T_RD_AddrWait
4. All address cycles received		→	T_RD_LUN_Execute

T_RD_LUN_Execute	The target performs the following actions: 1. tLunSelected is set to the LUN indicated by the row address received. 2. Issues the Read Page with address to LUN tLunSelected. 3. Requests all idle LUNs not selected to turn off their output buffers.[1]		
1. Unconditional		→	T_RD_LUN_Confirm
NOTE: 1. LUNs not selected will only turn off their output buffers if they are in an Idle state. If other LUNs are active, the host shall issue a Read Status Enhanced (78h) command to ensure all LUNs that are not selected turn off their output buffers prior to issuing the Read (00h) command.			

T_RD_LUN_Confirm	Wait for 30h, 31h, 32h, or 35h to be received.		
1. Command cycle of 30h, 31h, 32h, or 35h received		→	T_RD_Cmd_Pass

T_RD_Cmd_Pass	Pass command received to LUN tLunSelected		
1. Command passed was 35h		→	T_RD_Copyback
2. Command passed was 30h, 31h, or 32h		→	T_Idle_Rd

"Open NAND Flash Interface (ONFI) Specification Revision 4.2," February 12, 2020, at 303.

98. The ONFI 4.2 NAND flash interface additionally provides that separate logical units (LUNs) "may operate on arbitrary command sequences in parallel."

> A logical unit (LUN) is the minimum unit that can independently execute commands and report status. Specifically, separate LUNs may operate on arbitrary command sequences in parallel. For example, it is permissible to start a Page Program operation on LUN 0 and then prior to the operation's completion to start a Read command on LUN 1. See multiple LUN operation restrictions in section 3.1.3. A LUN contains at least one page register and a Flash array. The number of page registers is dependent on the number of multi-plane operations supported for that LUN. The Flash array contains a number of blocks.

"Open NAND Flash Interface (ONFI) Specification Revision 4.2," February 12, 2020, at 303.

3.1.3. Multiple LUN Operation Restrictions

LUNs are independent entities. A multiple LUN operation is one in which two or more LUNs are simultaneously processing commands. During multiple LUN operations the individual LUNs involved may be in any combination of busy or ready status

When a Page Program command (80h) is issued on any LUN that is not preceded by an 11h command, all idle LUNs may clear their page registers if the program page register clear enhancement is not supported or enabled. Thus, the host should not begin a Page Program command on a LUN while a Read Page operation is either ongoing or has completed but the data has not been read from another LUN, as the contents of the page register for the Read operation are lost. A Read Page can be issued to one LUN while a Page Program is ongoing within a second LUN without any restriction. If the program page register clear enhancement is enabled, this restriction does not apply.

"Open NAND Flash Interface (ONFI) Specification Revision 4.2," February 12, 2020, at 303.

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

99. In addition and/or in the alternative to its direct infringements, Phison has indirectly infringed and continues to indirectly infringe one or more claims of the '909 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the '909 Accused Products.

100. At a minimum, Phison has knowledge of the '909 Patent since being served with this Complaint. Phison also has knowledge of the '909 Patent since receiving detailed correspondence from UTL prior to the filing of the Complaint, alerting Phison to its infringements. Since receiving notice of its infringements, Phison has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Indeed, Phison has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '909 Accused Products; creating and/or

maintaining established distribution channels for the ’909 Accused Products into and within the United States; manufacturing the ’909 Accused Products in conformity with U.S. laws and regulations; distributing or making available videos, training, tools and resources supporting use of the ’909 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the ’909 Accused Products, including product brochures, and descriptions of the features and technologies[4]; promoting the incorporation of the ’909 Accused Products into end-user products.

Damages

101. On information and belief, despite having knowledge of the ’909 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the ’909 Patent, Phison has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Phison’s infringing activities relative to the ’909 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that UTL is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

102. UTL has been damaged as a result of Phison’s infringing conduct described in this Count. Phison is, thus, liable to UTL in an amount that adequately compensates UTL for Phison’s infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

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[4] *See, e.g.*, https://www.phison.com/en/solutions/consumer/pc-laptop; https://www.phison.com/en/solutions/embedded; https://www.phison.com/en/solutions/enterprise; and the product brochures linked therefrom (last visited May 22, 2023).

COUNT IV

(INFRINGEMENT OF U.S. PATENT NO. 11,640,359)

103. Plaintiff incorporates the preceding paragraphs herein by reference.

104. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

105. UTL is the owner of all substantial rights, title, and interest in and to the ’359 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

106. The ’359 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on May 2, 2023, after full and fair examination.

107. Phison has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the ’359 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Phison products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the ’359 Patent, including, but not limited to, the Phison SSD Controllers, including but not limited to Phison’s Consumer, Embedded and Enterprise SSD Controllers, such as for example Phison’s PS5026-E26 PCIe Gen5 SSD Controller or X1 SSD Platform,, (collectively, the “’359 Accused Products”).

Direct Infringement (35 U.S.C. § 271(a))

108. Phison has directly infringed and continues to directly infringe one or more claims of the’359 Patent in this District and elsewhere in Texas and the United States.

109. Phison has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the ’359 Patent as set forth under 35 U.S.C. § 271(a) by making,

offering for sale, selling, and/or importing, the ’359 Accused Products. Furthermore, Phison makes and sells the ’359 Accused Products outside of the United States and either, delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the ’359 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the ’359 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, Phison directly infringes the ’359 Patent through its direct involvements in, and control of, the activities of its subsidiaries and/or affiliates, including Phison – USA. Subject to Phison’s direction and control, such subsidiaries and/or affiliates conduct activities that constitute direct infringement of the ’359 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing ’359 Accused Products. Phison receives direct financial benefit from such infringements of its U.S.-based subsidiaries and/or affiliates, including Phison – USA.

110. By way of illustration only, the ’359 Accused Products include each and every element of claim 1 of the ’359 Patent. As shown below, the ’359 Accused Products perform a method for managing data in a NAND flash storage system in accordance with the requirements of claim 1. Further, SMI directs or controls each step discussed below by including instructions and directives, such as firmware and source code, in the Accused Products that cause this to occur. For example, SMI’s PS5026-E26 PCIe Gen 5 SSD Controller performs such a method:

"PS5026-E26 PCIe Gen5 SSD Controller," Product Brochure, Phison Electronics, 2022: https://www.phison.com/images/products_datasheet/ProductBrochure_Consumer_PS5026-E26_12192022.pdf

111. The '359 Accused Products comprise circuitry implementing a method to receive an empty-block directive from a host at a storage controller in the NAND flash storage system, the empty-block directive including a logical identifier associated with a physical storage location comprising data that does not need to be preserved. For example, the PS5026-E26 PCIe Gen 5 SSD controller implements the NVM Express (NVMe) 2.0 interface that "allows host software to communicate with a non-volatile memory subsystem." *See* "NVM Express Revision 2.0 Base Specification," May 13, 2021, at 2. The NVM Express NVM Command Set Specification "defines a specific NVMe I/O Command Set, the NVM Command Set, which extends the NVM Express Base Specification." "NVM Command Set Specification, Revision 1.0c," October 3, 2022, at 2.

112. The NVM Command Set Specification provides that "[a] logic Block may be marked deallocated as a result of a Dataset Management Command . . . . a Write Zeroes command addressing the logical block; or a sanitize operation." *Id*. at 10-11. The Dataset Management Command can be used by the host to indicate a range of logical blocks are deallocated. *Id*. at 28-29.

Figure 40: Dataset Management – Command Dword 11

Bit	Description
02	**Attribute – Deallocate (AD):** If set to '1', then the NVM subsystem may deallocate all provided ranges. The data returned for logical blocks that were deallocated is specified in section 3.2.3.2.1. The data and metadata for logical blocks that are not deallocated by the NVM subsystem are not changed as the result of a Dataset Management command.
01	**Attribute – Integral Dataset for Write (IDW):** If set to '1', then the dataset should be optimized for write access as an integral unit. The host expects to perform operations on all ranges provided as an integral unit for writes, indicating that if a portion of the dataset is written it is expected that all of the ranges in the dataset are going to be written.
00	**Attribute – Integral Dataset for Read (IDR):** If set to '1', then the dataset should be optimized for read access as an integral unit. The host expects to perform operations on all ranges provided as an integral unit for reads, indicating that if a portion of the dataset is read it is expected that all of the ranges in the dataset are going to be read.

"NVM Command Set Specification, Revision 1.0c," October 3, 2022, at 29.

113. NVMe provides that the Dataset Management command can be used to indicate a range of logical blocks are deallocated using PRP Entries 1 and 2 or SGL Entry 1. *Id*. at 28.

3.2.3 Dataset Management command

The Dataset Management command is used by the host to indicate attributes for ranges of logical blocks. This includes attributes like frequency that data is read or written, access size, and other information that may be used to optimize performance and reliability. This command is advisory; a compliant controller may choose to take no action based on information provided.

The command uses Command Dword 10, and Command Dword 11 fields. If the command uses PRPs for the data transfer, then the PRP Entry 1 and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, then the SGL Entry 1 field is used. All other command specific fields are reserved.

Figure 38: Dataset Management – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the data to use for the command. Refer to the Common Command Format figure in the NVM Express Base Specification for the definition of this field.

"NVM Command Set Specification, Revision 1.0c," October 3, 2022, at 28.

114. NVMe interface provides that the physical memory locations in memory the commands use are specified using Physical Region Page (PRP) entries or Scatter Gather Lists (SGL). "NVM Express Revision 2.0 Base Specification," May 13, 2021, at 30.

39:24	**Data Pointer (DPTR):** This field specifies the data used in the command. If CDW0.PSDT is cleared to 00b, then the definition of this field is:	
	39:32	**PRP Entry 2 (PRP2):** This field: • is reserved if the data transfer does not cross a memory page boundary; • specifies the Page Base Address of the second memory page if the data transfer crosses exactly one memory page boundary. E.g.,: ○ the command data transfer length is equal in size to one memory page and the offset portion of the PBAO field of PRP1 is non-zero; or ○ the Offset portion of the PBAO field of PRP1 is equal to 0h and the command data transfer length is greater than one memory page and less than or equal to two memory pages in size; and • is a PRP List pointer if the data transfer crosses more than one memory page boundary. E.g.,: ○ the command data transfer length is greater than or equal to two memory pages in size but the offset portion of the PBAO field of PRP1 is non-zero; or ○ the command data transfer length is equal in size to more than two memory pages and the Offset portion of the PBAO field of PRP1 is equal to 0h.
	31:24	**PRP Entry 1 (PRP1):** This field contains the first PRP entry for the command or a PRP List pointer depending on the command.
	If CDW0.PSDT is set to 01b or 10b, then the definition of this field is:	
	39:24	**SGL Entry 1 (SGL1):** This field contains the first SGL segment for the command. If the SGL segment is an SGL Data Block or Keyed SGL Data Block or Transport SGL Data Block descriptor, then it describes the entire data transfer. If more than one SGL segment is needed to describe the data transfer, then the first SGL segment is a Segment, or Last Segment descriptor. Refer to section 4.1.2 for the definition of SGL segments and descriptor types. The NVMe Transport may support a subset of SGL Descriptor types and features as defined in the NVMe Transport binding specification.

"NVM Express Revision 2.0 Base Specification," May 13, 2021, at 105

115. The '369 Accused Products comprise circuitry implementing a method to return by the storage controller an indication that the logical identifier is empty, in response to a read command from the host requesting to read the data identified by the logical identifier included in the empty-block directive, wherein the data in the physical storage location remains on the NAND flash storage system.

116. For example, as noted above the PS5026-E26 PCIe Gen 5 SSD controller implements NVMe 2.0 which provides that the completion queue entries indicate a Status Code

Type for the type of completion being reported. "NVM Command Set Specification, Revision 1.0c," October 3, 2022, at 19.

Figure 17: Status Code – Media and Data Integrity Error Values

Value	Description
85h	**Compare Failure:** The command failed due to a miscompare during a Compare command.
87h	**Deallocated or Unwritten Logical Block:** The command failed due to an attempt to copy from, read from, or verify an LBA range containing a deallocated or unwritten logical block.

NVM Command Set Specification, Revision 1.0c," October 3, 2022, at 19.

117. NVMe interface provides that, in response to a command reading deallocated blocks, the controller shall either (1) abort the command and return a status of Deallocated Logical Block using the Error Recovery feature; or (2) return deterministic value of the deallocated block back to the host. Id. at 32.

Using the Error Recovery feature (refer to section 4.1.3.2), host software may select the behavior of the controller when reading deallocated or unwritten blocks. The controller shall abort Copy, Read, Verify, or Compare commands that include deallocated or unwritten blocks with a status of Deallocated or Unwritten Logical Block if that error has been enabled using the DULBE bit in the Error Recovery feature. If the Deallocated or Unwritten Logical error is not enabled, the values read from a deallocated or unwritten block and its metadata (excluding protection information) shall be:

- all bytes cleared to 0h if bits 2:0 in the DLFEAT field are set to 001b;
- all bytes set to FFh if bits 2:0 in the DLFEAT field are set to 010b; or
- either all bytes cleared to 0h or all bytes set to FFh if bits 2:0 in the DLFEAT field are cleared to 000b.

The value read from a deallocated logical block shall be deterministic; specifically, the value returned by subsequent reads of that logical block shall be the same until a write operation occurs to that logical block. A deallocated or unwritten block is no longer deallocated or unwritten when the logical block is written. Read operations and Verify operations do not affect the deallocation status of a logical block.

NVM Command Set Specification, Revision 1.0c," October 3, 2022, at 32.

118. The '369 Accused Products comprise circuitry implementing a method to maintain by the storage controller an index of mappings between the logical identifier and the physical storage location. For example, as noted above the PS5026-E26 PCIe Gen 5 SSD controller implements NVMe 2.0 which provides that "[a] logic Block may be marked deallocated as a result of a Dataset Management Command . . . ." *See, e.g.*, *id.* at 10-11. These Dataset Management commands can be used to indicate a range of logical blocks are deallocated using PRP Entries 1

and 2 or SGL Entry 1, indicating that the controller maintains an index of mappings between the logical identifier and the physical storage location. *Id*. at 28.

119. The ’369 Accused Products comprise circuitry implementing a method to update the index of mappings by the storage controller, in response to the empty-block directive, to indicate that the data in the physical storage location does not need to be preserved. For example, as noted above the PS5026-E26 PCIe Gen 5 SSD controller implements NVMe 2.0 which provides that “[a] logic Block may be marked deallocated as a result of a Dataset Management Command . . . .” *See, e.g.*, *id.* at 10-11. In response to a command to read deallocated blocks, the controller shall either (1) abort the command and return a status of Deallocated Logical Block using the Error Recovery feature; or (2) return deterministic value of the deallocated block back to the host as one example of an indication that the data in the physical storage location does not need to be preserved. *Id*. at 32.

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

120. In addition and/or in the alternative to its direct infringements, Phison has indirectly infringed and continues to indirectly infringe one or more claims of the ’359 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’359 Accused Product.

121. At a minimum, Phison has knowledge of the ’359 Patent since being served with this Complaint. Phison also has knowledge of the ’359 Patent since receiving detailed correspondence from UTL prior to the filing of the Complaint, alerting Phison to its infringements. Since receiving notice of its infringements, Phison has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers,

and/or consumers as set forth under U.S.C. § 271(b). Indeed, Phison has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '359 Accused Products; creating and/or maintaining established distribution channels for the '359 Accused Products into and within the United States; manufacturing the '359 Accused Products in conformity with U.S. laws and regulations; distributing or making available videos, training, tools and resources supporting use of the '359 Accused Products that promote their features, specifications, and applications; providing technical documentation for the '902 Accused Products, including white papers, product briefs, and descriptions of the features and technologies [5]; promoting the incorporation of the '902 Accused Products into end-user products.

Damages

122. On information and belief, despite having knowledge of the '359 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '359 Patent, Phison has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Phison's infringing activities relative to the '359 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that UTL is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

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[5] *See, e.g.*, https://www.siliconmotion.com/products/client/detail; https://www.siliconmotion.com/products/enterprise/detail; https://www.siliconmotion.com/products/Portable/detail; https://www.siliconmotion.com/products/automotive/detail; https://www.siliconmotion.com/product/Ferri-Embedded-Storage.html; and the product briefs and white papers linked therefrom (last visited May 20, 2023).

123. UTL has been damaged as a result of Phison's infringing conduct described in this Count. Phison is, thus, liable to UTL in an amount that adequately compensates UTL for Phison's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

CONCLUSION

124. UTL is entitled to recover from Phison the damages sustained by UTL as a result of Phison's wrongful acts, and willful infringements, in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court.

125. UTL has incurred and will incur attorneys' fees, costs, and expenses in the prosecution of this action. The circumstances of this dispute may give rise to an exceptional case within the meaning of 35 U.S.C. § 285, and UTL is entitled to recover its reasonable and necessary attorneys' fees, costs, and expenses.

JURY DEMAND

126. UTL hereby requests a trial by jury pursuant to Rule 38 of the Federal Rules of Civil Procedure.

PRAYER FOR RELIEF

127. UTL respectfully requests that the Court find in its favor and against Phison, and that the Court grant UTL the following relief:

(i) A judgment that one or more claims of the Asserted Patents have been infringed, either literally and/or under the doctrine of equivalents, by Phison;

(ii) A judgment that one or more claims of the Asserted Patents have been willfully infringed, either literally and/or under the doctrine of equivalents, by Phison;

(iii) A judgment that Phison account for and pay to UTL all damages and costs incurred by Plaintiff because of Phison's infringing activities and other conduct complained of herein, including an accounting for any sales or damages not presented at trial;

(iv) A judgment that Phison account for and pay to UTL a reasonable, ongoing, post judgment royalty because of Phison's infringing activities, including continuing infringing activities, and other conduct complained of herein;

(v) A judgment that UTL be granted pre-judgment and post judgment interest on the damages caused by Phison's infringing activities and other conduct complained of herein;

(vi) A judgment that this case is exceptional under the provisions of 35 U.S.C. § 285 and award enhanced damages; and

(vii) Such other and further relief as the Court deems just and equitable.

Dated: June 2, 2023

Respectfully submitted,

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