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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	FILO00200US27
	Application Number	
Title of Invention	Systems and Methods for Identifying Storage Resources That Are Not In Use	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	David		Flynn	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Sandy	State/Province	UT	Country of Residence	US

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Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jonathan		Thatcher	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

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Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Michael		Zappe	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

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City	Arvada	State/Province	CO	Country of Residence	US

Mailing Address of Inventor:

Address 1	8365 Quay Drive		
Address 2			
City	Arvada	State/Province	CO
Postal Code	80003	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	123084		
Email Address	docketing@gchub.com	Add Email	Remove Email

Application Information:

Title of the Invention	Systems and Methods for Identifying Storage Resources That Are Not In Use		
Attorney Docket Number	FILO00200US27	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	18	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	123084		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove

Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	15460126	2017-03-15

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15460126	Continuation of	15228893	2016-08-04	10387327	2019-08-20

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15228893	Continuation of	14309751	2014-06-19	9632727	2017-04-25

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14309751	Continuation of	13566471	2012-08-03	8762658	2014-06-24

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13566471	Continuation of	11952113	2007-12-06	8261005	2012-09-04

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Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11952113	Claims benefit of provisional	60974470	2007-09-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11952113	Claims benefit of provisional	60873111	2006-12-06
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	FIO Semiconductor Technologies, LLC		
Mailing Address Information For Applicant:			
Address 1	7160 Dallas Parkway		
Address 2	1717 McKinney Avenue, Suite 1050		
City	Dallas	**State/Province**	TX
Country	US	Postal Code	75202
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Spencer C. Patterson/			Date (YYYY-MM-DD)	2019-08-16
First Name	Spencer C.	Last Name	Patterson	Registration Number	43849

Additional Signature may be generated within this form by selecting the Add button. Add

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This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

SYSTEMS AND METHODS FOR IDENTIFYING STORAGE RESOURCES THAT ARE NOT IN USE

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Application No. 15/460,126 filed March 15, 2017, which is a continuation U.S. Application No. 15/228,893 filed August 4, 2016, now U.S. Patent No. 10,387,327, which is a continuation of U.S. Application No. 14/309,751 filed June 19, 2014, now U.S. Patent No. 9,632,727, which is a continuation of U.S. Application No. 13/566,471 filed August 3, 2012, now U.S. Patent No. 8,762,658, which is a continuation of U.S. Application No. 11/952,113 filed December 6, 2007, now U.S. Patent No. 8,261,005, which claims priority to U.S. Provisional Application No. 60/974,470 filed September 22, 2017 and U.S. Provisional Application No. 60/873,111, filed on December 6, 2006. Each of the above-referenced applications are incorporated herein by references in their entirety.

BACKGROUND OF THE INVENTION

[0002] Field of the Invention

[0003] This invention relates to managing data in a data storage device and more particularly relates to managing data in a storage device using an empty data segment directive.

[0004] Description of the Related Art

[0005] Typically, when data is no longer useful it may be erased. In many file systems, an erase command deletes a directory entry in the file system while leaving the data in place in the storage device containing the data. Typically, a data storage device is not involved in this type of erase operation. Another method of erasing data is to write zeros, ones, or some other null data character to the data storage device to actually replace the erased file. However, this is inefficient because valuable bandwidth is used while transmitting the data is being overwritten. In addition, space in the storage device is taken up by the data used to overwrite invalid data.

[0006] In some storage devices, like the solid-state storage device 102 described herein, updating previously stored data does not overwrite existing data. Attempting to overwrite data with a string of ones or a string of zeros on such a device takes up valuable space without fulfilling the desired intent of overwriting the existing data. For these devices, such as solid-state storage devices 102, a client 114 typically does not have an ability to overwrite data to erase it.

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[0007] When receiving a string of repeated characters or character strings, the received data is highly compressible, but typically compression is done by a file system prior to transmission to a storage device. A typical storage device cannot distinguish between compressed data and uncompressed data. The storage device may also receive a command to read the erased file so the storage device may transmit a stream of zeros, ones, or a null character to the requesting device. Again, bandwidth is required to transmit data representing the erased file.

SUMMARY OF THE INVENTION

[0008] From the foregoing discussion, it should be apparent that a need exists for an apparatus, system, and method for a storage device to receive a directive that data is to be erased so that the storage device can store a data segment token that represents an empty data segment or data with repeated characters or character strings. The apparatus, system, and method may also erase the existing data so that the resulting used storage space comprises the small data segment token. An apparatus, system, and method are presented that overcome some or all of the shortcomings of the prior art.

[0009] The present invention has been developed in response to the present state of the art, and in particular, in response to the problems and needs in the art that have not yet been fully solved by currently available data management systems. Accordingly, the present invention has been developed to provide an apparatus, system, and method for managing data that overcome many or all of the above-discussed shortcomings in the art.

[0010] Embodiments of methods for managing a non-volatile storage media are disclosed. The methods may comprise receiving a message comprising a logical identifier corresponding to data that does not need to be preserved on a non-volatile storage medium, and indicating that that contents of a physical storage location on the non-volatile storage medium corresponding to the logical identifier do not need to be preserved on the non-volatile storage medium in response to the message.

[0011] Indicating that the contents of the physical storage location do not need to be preserved may comprise deleting an index entry that associates the logical identifier with the physical storage location, deleting a mapping between the logical identifier and the physical

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storage location, invalidating an association between the logical identifier and an address of the physical storage location, and/or marking the contents of the physical storage location invalid.

[0012] The methods may further comprise maintaining an index of mappings between logical identifiers and physical storage locations, and that the contents of the physical storage location do not need to be preserved may comprise removing a mapping between the logical identifier and the physical storage location from the index.

[0013] Methods for managing a non-volatile storage medium may further comprise receiving a hint or other indication that data of a specified logical identifier does not need to be preserved on a non-volatile storage device, and removing a mapping between the specified logical identifier and a physical address of the data of the specified logical identifier on the non-volatile storage device in response to the hint, wherein removal of the mapping indicates that the data does not need to be preserved on the non-volatile storage device. The methods may further comprise invalidating a data packet in response to the hint.

[0014] In some embodiments, the methods disclosed herein may further comprise erasing the contents of the physical storage location in a storage recovery process, such as garbage collection or the like. The storage recovery process may comprise erasing a storage division comprising the physical storage location (e.g., erase block, logical erase block, or the like).

[0015] In some embodiments, the methods disclosed herein may further comprise receiving the message from a block storage client, such as a file system, operating system, application, client, or the like. The message may be received through a block storage application programming interface, block storage protocol, or the like.

[0016] Disclosed herein are embodiments of apparatuses and/or systems for managing a non-volatile storage medium, comprising a request receiver module configured to receive an indication identifying data that can be erased from a non-volatile storage medium, wherein the indication identifies the data using a logical identifier associated with the data, and a marking module configured to record that data stored at a physical address on the non-volatile storage medium can be erased from the non-volatile storage medium in response to receiving the indication.

[0017] The marking module may be configured to invalidate an association between the logical identifier and the physical address, delete a mapping between the logical identifier and the physical address, and/or mark a data packet at the physical address invalid.

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[0018] The apparatuses and systems disclosed herein may further comprise an index comprising mappings between logical identifiers and physical addresses on the non-volatile storage medium, wherein the marking module is configured to remove a mapping between the logical identifier and the physical addresses of the data from the index. The marking module may be further configured to delete a reference to the physical address from an index entry of the logical identifier. Removal of the mapping may indicate that data stored at the physical address can be erased from the non-volatile storage medium.

[0019] The apparatuses and systems disclosed herein may further comprise a request receiver module configured to receive the hint. The request receiver module may comprise a driver. The request receiver module may be configured to receive the hint from a file system, the file system configured to send the hint in response to deletion of file system data associated with the logical identifier and/or removal of a file associated with the logical identifier.

[0020] In some embodiments, the request receiver module is configured to receive the hint from an application, wherein the application is configured to send the hint in response to determining that data associated with the logical identifier no longer needs to be retained on the non-volatile storage medium.

[0021] The apparatuses and systems disclosed herein may further comprise a storage recovery module configured to recover the physical storage location at the physical address, and a storage module configured to store data associated with another logical identifier on the physical storage location in response to recovering the physical storage location.

[0022] The apparatuses and systems disclosed herein may comprise, an index configured to contain a plurality of entries, wherein each entry associates a logical identifier with a physical storage location of a non-volatile storage medium that comprises valid data of the logical identifier, a request receiver module configured to receive an indication that a specified logical identifier is empty, and an index module configured to remove an entry from the index that associates the specified logical identifier with a physical storage location of the non-volatile storage medium in response to the indication. The request receiver module may be configured to receive the indication through one of a block device interface and via a block storage protocol.

[0023] The apparatuses and systems disclosed herein may further comprise a storage recovery module configured to erase a storage division comprising the physical storage location in response to removing the entry.

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[0024] The apparatuses and systems disclosed herein may further comprise a read request response module configured to return an indication that the logical identifier is empty in response to a request to read data of the logical identifier while the data remains on the non-volatile storage medium.

[0025] Reference throughout this specification to features, advantages, or similar language does not imply that all of the features and advantages that may be realized with the present invention should be or are in any single embodiment of the invention. Rather, language referring to the features and advantages is understood to mean that a specific feature, advantage, or characteristic described in connection with an embodiment is included in at least one embodiment of the present invention. Thus, discussion of the features and advantages, and similar language, throughout this specification may, but do not necessarily, refer to the same embodiment.

[0026] Furthermore, the described features, advantages, and characteristics of the invention may be combined in any suitable manner in one or more embodiments. One skilled in the relevant art will recognize that the invention may be practiced without one or more of the specific features or advantages of a particular embodiment. In other instances, additional features and advantages may be recognized in certain embodiments that may not be present in all embodiments of the invention.

[0027] These features and advantages of the present invention will become more fully apparent from the following description and appended claims, or may be learned by the practice of the invention as set forth hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] In order that the advantages of the invention will be readily understood, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments that are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are not therefore to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings, in which:

[0029] FIG. 1A is a schematic block diagram illustrating one embodiment of a system for data management in a solid-state storage device in accordance with the present invention;

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[0030] FIG. 1B is a schematic block diagram illustrating one embodiment of a system for object management in a storage device in accordance with the present invention;

[0031] FIG. 2A is a schematic block diagram illustrating one embodiment of an apparatus for object management in a storage device in accordance with the present invention;

[0032] FIG. 2B is a schematic block diagram illustrating one embodiment of a solid-state storage device controller in a solid-state storage device in accordance with the present invention;

[0033] FIG. 3 is a schematic block diagram illustrating one embodiment of a solid-state storage controller with a write data pipeline and a read data pipeline in a solid-state storage device in accordance with the present invention;

[0034] FIG. 4A is a schematic block diagram illustrating one embodiment of a bank interleave controller in the solid-state storage controller in accordance with the present invention;

[0035] FIG. 4B is a schematic block diagram illustrating an alternate embodiment of a bank interleave controller in the solid-state storage controller in accordance with the present invention;

[0036] FIG. 5 is a schematic flow chart diagram illustrating one embodiment of a method for managing data in a solid-state storage device using a data pipeline in accordance with the present invention;

[0037] FIG. 6 is a schematic flow chart diagram illustrating another embodiment of a method for managing data in a solid-state storage device using a data pipeline in accordance with the present invention;

[0038] FIG. 7 is a schematic flow chart diagram illustrating an embodiment of a method for managing data in a solid-state storage device using a bank interleave in accordance with the present invention;

[0039] FIG. 8 is a schematic block diagram illustrating one embodiment of an apparatus for garbage collection in a solid-state storage device in accordance with the present invention;

[0040] FIG. 9 is a schematic flow chart diagram illustrating one embodiment of a method for garbage collection in a solid state storage device in accordance with the present invention;

[0041] FIG. 10 is a schematic block diagram illustrating one embodiment of a system with an apparatus for generating a token directive in accordance with the present invention;

[0042] FIG. 11 is a schematic flow chart diagram illustrating an embodiment of a method for generating and transmitting a token directive in accordance with the present invention;

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[0043] FIG. 12 is a schematic flow chart diagram illustrating an embodiment of a method for reading a data segment token in accordance with the present invention;

[0044] FIG. 13 is a schematic block diagram illustrating one embodiment of a system with an apparatus for managing a data segment token in accordance with the present invention;

[0045] FIG. 14 is a schematic flow chart diagram illustrating an embodiment of a method for storing a data segment token in accordance with the present invention; and

[0046] FIG. 15 is a schematic flow chart diagram illustrating an embodiment of a method for reading a data segment token in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0047] Many of the functional units described in this specification have been labeled as modules, in order to more particularly emphasize their implementation independence. For example, a module may be implemented as a hardware circuit comprising custom VLSI circuits or gate arrays, off-the-shelf semiconductors such as logic chips, transistors, or other discrete components. A module may also be implemented in programmable hardware devices such as field programmable gate arrays, programmable array logic, programmable logic devices or the like.

[0048] Modules may also be implemented in software for execution by various types of processors. An identified module of executable code may, for instance, comprise one or more physical or logical blocks of computer instructions which may, for instance, be organized as an object, procedure, or function. Nevertheless, the executables of an identified module need not be physically located together, but may comprise disparate instructions stored in different locations which, when joined logically together, comprise the module and achieve the stated purpose for the module.

[0049] Indeed, a module of executable code may be a single instruction, or many instructions, and may even be distributed over several different code segments, among different programs, and across several memory devices. Similarly, operational data may be identified and illustrated herein within modules, and may be embodied in any suitable form and organized within any suitable type of data structure. The operational data may be collected as a single data set, or may be distributed over different locations including over different storage devices, and may exist, at least partially, merely as electronic signals on a system or network. Where a

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module or portions of a module are implemented in software, the software portions are stored on one or more computer readable media.

[0050] Reference throughout this specification to "one embodiment," "an embodiment," or similar language means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment," "in an embodiment," and similar language throughout this specification may, but do not necessarily, all refer to the same embodiment.

[0051] Reference to a signal bearing medium may take any form capable of generating a signal, causing a signal to be generated, or causing execution of a program of machine-readable instructions on a digital processing apparatus. A signal bearing medium may be embodied by a transmission line, a compact disk, digital-video disk, a magnetic tape, a Bernoulli drive, a magnetic disk, a punch card, flash memory, integrated circuits, or other digital processing apparatus memory device.

[0052] Furthermore, the described features, structures, or characteristics of the invention may be combined in any suitable manner in one or more embodiments. In the following description, numerous specific details are provided, such as examples of programming, software modules, user selections, network transactions, database queries, database structures, hardware modules, hardware circuits, hardware chips, etc., to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art will recognize, however, that the invention may be practiced without one or more of the specific details, or with other methods, components, materials, and so forth. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

[0053] The schematic flow chart diagrams included herein are generally set forth as logical flow chart diagrams. As such, the depicted order and labeled steps are indicative of one embodiment of the presented method. Other steps and methods may be conceived that are equivalent in function, logic, or effect to one or more steps, or portions thereof, of the illustrated method. Additionally, the format and symbols employed are provided to explain the logical steps of the method and are understood not to limit the scope of the method. Although various arrow types and line types may be employed in the flow chart diagrams, they are understood not to limit the scope of the corresponding method. Indeed, some arrows or other connectors may be

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used to indicate only the logical flow of the method. For instance, an arrow may indicate a waiting or monitoring period of unspecified duration between enumerated steps of the depicted method. Additionally, the order in which a particular method occurs may or may not strictly adhere to the order of the corresponding steps shown.

[0054] Solid-State Storage System

[0055] FIG. 1A is a schematic block diagram illustrating one embodiment of a system 100 for data management in a solid-state storage device in accordance with the present invention. The system 100 includes a solid-state storage device 102, a solid-state storage controller 104, a write data pipeline 106, a read data pipeline 108, a solid-state storage 110, a computer 112, a client 114, and a computer network 116, which are described below.

[0056] The system 100 includes at least one solid-state storage device 102. In another embodiment, the system 100 includes two or more solid-state storage devices 102. Each solid-state storage device 102 may include non-volatile, solid-state storage 110, such as flash memory, nano random access memory ("nano RAM or NRAM"), magneto-resistive RAM ("MRAM"), dynamic RAM ("DRAM"), phase change RAM ("PRAM"), etc. The solid-state storage device 102 is described in more detail with respect to FIGS. 2 and 3. The solid-state storage device 102 is depicted in a computer 112 connected to a client 114 through a computer network 116. In one embodiment, the solid-state storage device 102 is internal to the computer 112 and is connected using a system bus, such as a peripheral component interconnect express ("PCI-e") bus, a Serial Advanced Technology Attachment ("serial ATA") bus, or the like. In another embodiment, the solid-state storage device 102 is external to the computer 112 and is connected, a universal serial bus ("USB") connection, an Institute of Electrical and Electronics Engineers ("IEEE") 1394 bus ("FireWire"), or the like. In other embodiments, the solid-state storage device 102 is connected to the computer 112 using a peripheral component interconnect ("PCI") express bus using external electrical or optical bus extension or bus networking solution such as Infiniband or PCI Express Advanced Switching ("PCIe-AS"), or the like.

[0057] In various embodiments, the solid-state storage device 102 may be in the form of a dual-inline memory module ("DIMM"), a daughter card, or a micro-module. In another embodiment, the solid-state storage device 102 is an element within a rack-mounted blade. In another embodiment, the solid state storage device 102 is contained within a package that is integrated directly onto a higher level assembly (e.g. mother board, lap top, graphics processor).

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In another embodiment, individual components comprising the solid-state storage device 102 are integrated directly onto a higher level assembly without intermediate packaging.

[0058] The solid-state storage device 102 includes one or more solid-state storage controllers 104, each may include a write data pipeline 106 and a read data pipeline 108 and each includes a solid-state storage 110, which are described in more detail below with respect to FIGS. 2 and 3.

[0059] The system 100 includes one or more computers 112 connected to the solid-state storage device 102. A computer 112 may be a host, a server, a storage controller of a storage area network ("SAN"), a workstation, a personal computer, a laptop computer, a handheld computer, a supercomputer, a computer cluster, a network switch, router, or appliance, a database or storage appliance, a data acquisition or data capture system, a diagnostic system, a test system, a robot, a portable electronic device, a wireless device, or the like. In another embodiment, a computer 112 may be a client and the solid-state storage device 102 operates autonomously to service data requests sent from the computer 112. In this embodiment, the computer 112 and solid-state storage device 102 may be connected using a computer network, system bus, or other communication means suitable for connection between a computer 112 and an autonomous solid-state storage device 102.

[0060] In one embodiment, the system 100 includes one or more clients 114 connected to one or more computer 112 through one or more computer networks 116. A client 114 may be a host, a server, a storage controller of a SAN, a workstation, a personal computer, a laptop computer, a handheld computer, a supercomputer, a computer cluster, a network switch, router, or appliance, a database or storage appliance, a data acquisition or data capture system, a diagnostic system, a test system, a robot, a portable electronic device, a wireless device, or the like. The computer network 116 may include the Internet, a wide area network ("WAN"), a metropolitan area network ("MAN"), a local area network ("LAN"), a token ring, a wireless network, a fiber channel network, a SAN, network attached storage ("NAS"), ESCON, or the like, or any combination of networks. The computer network 116 may also include a network from the IEEE 802 family of network technologies, such Ethernet, token ring, WiFi, WiMax, and the like.

[0061] The computer network 116 may include servers, switches, routers, cabling, radios, and other equipment used to facilitate networking computers 112 and clients 114. In one

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embodiment, the system 100 includes multiple computers 112 that communicate as peers over a computer network 116. In another embodiment, the system 100 includes multiple solid-state storage devices 102 that communicate as peers over a computer network 116. One of skill in the art will recognize other computer networks 116 comprising one or more computer networks 116 and related equipment with single or redundant connection between one or more clients 114 or other computer with one or more solid-state storage devices 102 or one or more solid-state storage devices 102 connected to one or more computers 112. In one embodiment, the system 100 includes two or more solid-state storage devices 102 connected through the computer network 116 to a client 114 without a computer 112.

[0062] Storage Controller-Managed Objects

[0063] FIG. 1B is a schematic block diagram illustrating one embodiment of a system 101 for object management in a storage device in accordance with the present invention. The system 101 includes one or more storage device 150, each with a storage controller 152 and one or more data storage devices 154, and one or more requesting devices 155. The storage devices 150 are networked together and coupled to one or more requesting devices 155. The requesting device 155 sends object requests to a storage device 150a. An object request may be a request to create an object, a request to write data to an object, a request to read data from an object, a request to delete an object, a request to checkpoint an object, a request to copy an object, and the like. One of skill in the art will recognize other object requests.

[0064] In one embodiment, the storage controller 152 and data storage device 154 are separate devices. In another embodiment, the storage controller 152 and data storage device 154 are integrated into one storage device 150. In another embodiment, a data storage device 154 is a solid-state storage 110 and the storage controller 152 is a solid-state storage device controller 202. In other embodiments, a data storage device 154 may be a hard disk drive, an optical drive, tape storage, or the like. In another embodiment, a storage device 150 may include two or more data storage devices 154 of different types.

[0065] In one embodiment, the data storage device 154 is a solid-state storage 110 and is arranged as an array of solid-state storage elements 216, 218, 220. In another embodiment, the solid-state storage 110 is arranged in two or more banks 214a-n. Solid-state storage 110 is described in more detail below with respect to FIG. 2B.

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[0066] The storage devices 150a-n may be networked together and act as a distributed storage device. The storage device 150a coupled to the requesting device 155 controls object requests to the distributed storage device. In one embodiment, the storage devices 150 and associated storage controllers 152 manage objects and appear to the requesting device(s) 155 as a distributed object file system. In this context, a parallel object file system is an example of a type of distributed object file system. In another embodiment, the storage devices 150 and associated storage controllers 152 manage objects and appear to the requesting device 155(s) as distributed object file servers. In this context, a parallel object file server is an example of a type of distributed object file server. In these and other embodiments the requesting device 155 may exclusively manage objects or participate in managing objects in conjunction with storage devices 150; this typically does not limit the ability of storage devices 150 to fully manage objects for other clients 114. In the degenerate case, each distributed storage device, distributed object file system and distributed object file server can operate independently as a single device. The networked storage devices 150a-n may operate as distributed storage devices, distributed object file systems, distributed object file servers, and any combination thereof having images of one or more of these capabilities configured for one or more requesting devices 155. Fore example, the storage devices 150 may be configured to operate as distributed storage devices for a first requesting device 155a, while operating as distributed storage devices and distributed object file systems for requesting devices 155b. Where the system 101 includes one storage device 150a, the storage controller 152a of the storage device 150a manages objects may appear to the requesting device(s) 155 as an object file system or an object file server.

[0067] In one embodiment where the storage devices 150 are networked together as a distributed storage device, the storage devices 150 serve as a redundant array of independent drives ("RAID") managed by one or more distributed storage controllers 152. For example, a request to write a data segment of an object results in the data segment being stripped across the data storage devices 154a-n with a parity stripe, depending upon the RAID level. One benefit of such an arrangement is that such an object management system may continue to be available when a single storage device 150 has a failure, whether of the storage controller 152, the data storage device 154, or other components of storage device 150.

[0068] When redundant networks are used to interconnect the storage devices 150 and requesting devices 155, the object management system may continue to be available in the

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presence of network failures as long as one of the networks remains operational. A system 101 with a single storage device 150a may also include multiple data storage devices 154a and the storage controller 152a of the storage device 150a may act as a RAID controller and stripe the data segment across the data storage devices 154a of the storage device 150a and may include a parity stripe, depending upon the RAID level.

[0069] In one embodiment, where the one or more storage devices 150a-n are solid-state storage devices 102 with a solid-state storage device controller 202 and solid-state storage 110, the solid-state storage device(s) 102 may be configured in a DIMM configuration, daughter card, micro-module, etc. and reside in a computer 112. The computer 112 may be a server or similar device with the solid-state storage devices 102 networked together and acting as distributed RAID controllers. Beneficially, the storage devices 102 may be connected using PCI-e, PCIe-AS, Infiniband or other high-performance bus, switched bus, networked bus, or network and may provide a very compact, high performance RAID storage system with single or distributed solid-state storage controllers 202 autonomously striping a data segment across solid-state storage 110a-n.

[0070] In one embodiment, the same network used by the requesting device 155 to communicate with storage devices 150 may be used by the peer storage device 150a to communicate with peer storage devices 150b-n to accomplish RAID functionality. In another embodiment, a separate network may be used between the storage devices 150 for the purpose of RAIDing. In another embodiment, the requesting devices 155 may participate in the RAIDing process by sending redundant requests to the storage devices 150. For example, requesting device 155 may send a first object write request to a first storage device 150a and a second object write request with the same data segment to a second storage device 150b to achieve simple mirroring.

[0071] With the ability for object handling within the storage device(s) 102, the storage controller(s) 152 uniquely have the ability to store one data segment or object using one RAID level while another data segment or object is stored using a different RAID level or without RAID striping. These multiple RAID groupings may be associated with multiple partitions within the storage devices 150. RAID 0, RAID 1, RAID5, RAID6 and composite RAID types 10, 50, 60, can be supported simultaneously across a variety of RAID groups comprising data

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storage devices 154a-n. One skilled in the art will recognize other RAID types and configurations that may also be simultaneously supported.

[0072] Also, because the storage controller(s) 152 operate autonomously as RAID controllers, the RAID controllers can perform progressive RAIDing and can transform objects or portions of objects striped across data storage devices 154 with one RAID level to another RAID level without the requesting device 155 being affected, participating or even detecting the change in RAID levels. In the preferred embodiment, progressing the RAID configuration from one level to another level may be accomplished autonomously on an object or even a packet bases and is initiated by a distributed RAID control module operating in one of the storage devices 150 or the storage controllers 152. Typically, RAID progression will be from a higher performance and lower efficiency storage configuration such as RAID1 to a lower performance and higher storage efficiency configuration such as RAID5 where the transformation is dynamically initiated based on the frequency of access. But, one can see that progressing the configuration from RAID5 to RAID1 is also possible. Other processes for initiating RAID progression may be configured or requested from clients or external agents such a storage system management server request. One of skill in the art will recognize other features and benefits of a storage device 102 with a storage controller 152 that autonomously manages objects.

[0073] Apparatus for Storage Controller-Managed Objects

[0074] FIG. 2A is a schematic block diagram illustrating one embodiment of an apparatus 200 for object management in a storage device in accordance with the present invention. The apparatus 200 includes a storage controller 152 with an object request receiver module 260, a parsing module 262, a command execution module 264, an object index module 266, an object request queuing module 268, a packetizer 302 with a messages module 270, and an object index reconstruction module 272, which are described below.

[0075] The storage controller 152 is substantially similar to the storage controller 152 described in relation to the system 101 of FIG. 1B and may be a solid-state storage device controller 202 described in relation to FIG. 2. The apparatus 200 includes an object request receiver module 260 that receives an object request from one or more requesting devices 155. For example, for a store object data request, the storage controller 152 stores the data segment as a data packet in a data storage device 154 coupled to the storage controller 152. The object request is typically directed at a data segment stored or to be stored in one or more object data

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packets for an object managed by the storage controller 152. The object request may request that the storage controller 152 create an object to be later filled with data through later object request which may utilize a local or remote direct memory access ("DMA," "RDMA") transfer.

[0076] In one embodiment, the object request is a write request to write all or part of an object to a previously created object. In one example, the write request is for a data segment of an object. The other data segments of the object may be written to the storage device 150 or to other storage devices. In another example, the write request is for an entire object. In another example, the object request is to read data from a data segment managed by the storage controller 152. In yet another embodiment, the object request is a delete request to delete a data segment or object.

[0077] Advantageously, the storage controller 152 can accept write requests that do more than write a new object or append data to an existing object. For example, a write request received by the object request receiver module 260 may include a request to add data ahead of data stored by the storage controller 152, to insert data into the stored data, or to replace a segment of data. The object index maintained by the storage controller 152 provides the flexibility required for these complex write operations that is not available in other storage controllers, but is currently available only outside of storage controllers in file systems of servers and other computers.

[0078] The apparatus 200 includes a parsing module 262 that parses the object request into one or more commands. Typically, the parsing module 262 parses the object request into one or more buffers. For example, one or more commands in the object request may be parsed into a command buffer. Typically the parsing module 262 prepares an object request so that the information in the object request can be understood and executed by the storage controller 152. One of skill in the art will recognize other functions of a parsing module 262 that parses an object request into one or more commands.

[0079] The apparatus 200 includes a command execution module 264 that executes the command(s) parsed from the object request. In one embodiment, the command execution module 264 executes one command. In another embodiment, the command execution module 264 executes multiple commands. Typically, the command execution module 264 interprets a command parsed from the object request, such as a write command, and then creates, queues, and executes subcommands. For example, a write command parsed from an object request may

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direct the storage controller 152 to store multiple data segments. The object request may also include required attributes such as encryption, compression, etc. The command execution module 264 may direct the storage controller 152 to compress the data segments, encrypt the data segments, create one or more data packets and associated headers for each data packet, encrypt the data packets with a media encryption key, add error correcting code, and store the data packets a specific location. Storing the data packets at a specific location and other subcommands may also be broken down into other lower level subcommands. One of skill in the art will recognize other ways that the command execution module 264 can execute one or more commands parsed from an object request.

[0080] The apparatus 200 includes an object index module 266 that creates an object entry in an object index in response to the storage controller 152 creating an object or storing the data segment of the object. Typically, the storage controller 152 creates a data packet from the data segment and the location of where the data packet is stored is assigned at the time the data segment is stored. Object metadata received with a data segment or as part of an object request may be stored in a similar way.

[0081] The object index module 266 creates an object entry into an object index at the time the data packet is stored and the physical address of the data packet is assigned. The object entry includes a mapping between a logical identifier of the object and one or more physical addresses corresponding to where the storage controller 152 stored one or more data packets and any object metadata packets. In another embodiment, the entry in the object index is created before the data packets of the object are stored. For example, if the storage controller 152 determines a physical address of where the data packets are to be stored earlier, the object index module 266 may create the entry in the object index earlier.

[0082] Typically, when an object request or group of object requests results in an object or data segment being modified, possibly during a read-modify-write operation, the object index module 266 updates an entry in the object index corresponding the modified object. In one embodiment, the object index creates a new object and a new entry in the object index for the modified object. Typically, where only a portion of an object is modified, the object includes modified data packets and some data packets that remain unchanged. In this case, the new entry includes a mapping to the unchanged data packets as where they were originally written and to the modified objects written to a new location.

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[0083] In another embodiment, where the object request receiver module 260 receives an object request that includes a command that erases a data block or other object elements, the storage controller 152 may store at least one packet such as an erase packet that includes information including a reference to the object, relationship to the object, and the size of the data block erased. Additionally, it may further indicate that the erased object elements are filled with zeros. Thus, the erase object request can be used to emulate actual memory or storage that is erased and actually has a portion of the appropriate memory/storage actually stored with zeros in the cells of the memory/storage.

[0084] Beneficially, creating an object index with entries indicating mapping between data segments and metadata of an object allows the storage controller 152 to autonomously handle and manage objects. This capability allows a great amount of flexibility for storing data in the storage device 150. Once the index entry for the object is created, subsequent object requests regarding the object can be serviced efficiently by the storage controller 152.

[0085] In one embodiment, the storage controller 152 includes an object request queuing module 268 that queues one or more object requests received by the object request receiver module 260 prior to parsing by the parsing module 262. The object request queuing module 268 allows flexibility between when an object request is received and when it is executed.

[0086] In another embodiment, the storage controller 152 includes a packetizer 302 that creates one or more data packets from the one or more data segments where the data packets are sized for storage in the data storage device 154. The packetizer 302 is described below in more detail with respect to FIG. 3. The packetizer 302 includes, in one embodiment, a messages module 270 that creates a header for each packet. The header includes a packet identifier and a packet length. The packet identifier relates the packet to the object for which the packet was formed.

[0087] In one embodiment, each packet includes a packet identifier that is self-contained in that the packet identifier contains adequate information to identify the object and relationship within the object of the object elements contained within the packet. However, a more efficient preferred embodiment is to store packets in containers.

[0088] A container is a data construct that facilitates more efficient storage of packets and helps establish relationships between an object and data packets, metadata packets, and other packets related to the object that are stored within the container. Note that the storage controller

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152 typically treats object metadata received as part of an object and data segments in a similar manner. Typically "packet" may refer to a data packet comprising data, a metadata packet comprising metadata, or another packet of another packet type. An object may be stored in one or more containers and a container typically includes packets for no more than one unique object. An object may be distributed between multiple containers. Typically a container is stored within a single logical erase block (storage division) and is typically never split between logical erase blocks.

[0089] A container, in one example, may be split between two or more logical/virtual pages. A container is identified by a container label that associates that container with an object. A container may contain zero to many packets and the packets within a container are typically from one object. A packet may be of many object element types, including object attribute elements, object data elements, object index elements, and the like. Hybrid packets may be created that include more than one object element type. Each packet may contain zero to many elements of the same element type. Each packet within a container typically contains a unique identifier that identifies the relationship to the object.

[0090] Each packet is associated with one container. In a preferred embodiment, containers are limited to an erase block so that at or near the beginning of each erase block a container packet can be found. This helps limit data loss to an erase block with a corrupted packet header. In this embodiment, if the object index is unavailable and a packet header within the erase block is corrupted, the contents from the corrupted packet header to the end of the erase block may be lost because there is possibly no reliable mechanism to determine the location of subsequent packets. In another embodiment, a more reliable approach is to have a container limited to a page boundary. This embodiment requires more header overhead. In another embodiment, containers can flow across page and erase block boundaries. This requires less header overhead but a larger portion of data may be lost if a packet header is corrupted. For these several embodiments it is expected that some type of RAID is used to further ensure data integrity.

[0091] In one embodiment, the apparatus 200 includes an object index reconstruction module 272 that that reconstructs the entries in the object index using information from packet headers stored in the data storage device 154. In one embodiment, the object index reconstruction module 272 reconstructs the entries of the object index by reading headers to

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determine the object to which each packet belongs and sequence information to determine where in the object the data or metadata belongs. The object index reconstruction module 272 uses physical address information for each packet and timestamp or sequence information to create a mapping between the physical locations of the packets and the object identifier and data segment sequence. Timestamp or sequence information is used by the object index reconstruction module 272 to replay the sequence of changes made to the index and thereby typically reestablish the most recent state.

[0092] In another embodiment, the object index reconstruction module 272 locates packets using packet header information along with container packet information to identify physical locations of the packets, object identifier, and sequence number of each packet to reconstruct entries in the object index. In one embodiment, erase blocks are time stamped or given a sequence number as packets are written and the timestamp or sequence information of an erase block is used along with information gathered from container headers and packet headers to reconstruct the object index. In another embodiment, timestamp or sequence information is written to an erase block when the erase block is recovered.

[0093] Where the object index is stored in volatile memory, an error, loss of power, or other problem causing the storage controller 152 to shut down without saving the object index could be a problem if the object index cannot be reconstructed. The object index reconstruction module 272 allows the object index to be stored in volatile memory allowing the advantages of volatile memory, such as fast access. The object index reconstruction module 272 allows quick reconstruction of the object index autonomously without dependence on a device external to the storage device 150.

[0094] In one embodiment, the object index in volatile memory is stored periodically in a data storage device 154. In a particular example, the object index, or "index metadata," is stored periodically in a solid-state storage 110. In another embodiment, the index metadata is stored in a solid-state storage 110n separate from solid-state storage 110a-110n-1 storing packets. The index metadata is managed independently from data and object metadata transmitted from a requesting device 155 and managed by the storage controller 152/solid-state storage device controller 202. Managing and storing index metadata separate from other data and metadata from an object allows efficient data flow without the storage controller 152/solid-state storage device controller 202 unnecessarily processing object metadata.

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[0095] In one embodiment, where an object request received by the object request receiver module 260 includes a write request, the storage controller 152 receives one or more data segments of an object from memory of a requesting device 155 as a local or remote direct memory access ("DMA," "RDMA") operation. In a preferred example, the storage controller 152 pulls data from the memory of the requesting device 155 in one or more DMA or RDMA operations. In another example, the requesting device 155 pushes the data segment(s) to the storage controller 152 in one or more DMA or RDMA operations. In another embodiment, where the object request includes a read request, the storage controller 152 transmits one or more data segments of an object to the memory of the requesting device 155 in one or more DMA or RDMA operations. In a preferred example, the storage controller 152 pushes data to the memory of the requesting device 155 in one or more DMA or RDMA operations. In another example, the requesting device 155 pulls data from the storage controller 152 in one or more DMA or RDMA operations. In another example, the storage controller 152 pulls object command request sets from the memory of the requesting device 155 in one or more DMA or RDMA operations. In another example, the requesting device 155 pushes object command request sets to the storage controller 152 in one or more DMA or RDMA operations.

[0096] In one embodiment, the storage controller 152 emulates block storage and an object communicated between the requesting device 155 and the storage controller 152 comprises one or more data blocks. In one embodiment, the requesting device 155 includes a driver so that the storage device 150 appears as a block storage device. For example, the requesting device 155 may send a block of data of a certain size along with a physical address of where the requesting device 155 wants the data block stored. The storage controller 152 receives the data block and uses the physical block address transmitted with the data block or a transformation of the physical block address as an object identifier. The storage controller 152 then stores the data block as an object or data segment of an object by packetizing the data block and storing the data block at will. The object index module 266 then creates an entry in the object index using the physical block-based object identifier and the actual physical location where the storage controller 152 stored the data packets comprising the data from the data block.

[0097] In another embodiment, the storage controller 152 emulates block storage by accepting block objects. A block object may include one or more data blocks in a block structure. In one embodiment, the storage controller 152 treats the block object as any other object. In

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another embodiment, an object may represent an entire block device, partition of a block device, or some other logical or physical sub-element of a block device including a track, sector, channel, and the like. Of particular note is the ability to remap a block device RAID group to an object supporting a different RAID construction such as progressive RAID. One skilled in the art will recognize other mappings of traditional or future block devices to objects.

[0098] Solid-State Storage Device

[0099] FIG. 2B is a schematic block diagram illustrating one embodiment 201 of a solid-state storage device controller 202 that includes a write data pipeline 106 and a read data pipeline 108 in a solid-state storage device 102 in accordance with the present invention. The solid-state storage device controller 202 may include a number of solid-state storage controllers 0-N 104a-n, each controlling solid-state storage 110. In the depicted embodiment, two solid-state controllers are shown: solid-state controller 0 104a and solid-state storage controller N 104n, and each controls solid-state storage 110a-n. In the depicted embodiment, solid-state storage controller 0 104a controls a data channel so that the attached solid-state storage 110a stores data. Solid-state storage controller N 104n controls an index metadata channel associated with the stored data and the associated solid-state storage 110n stores index metadata. In an alternate embodiment, the solid-state storage device controller 202 includes a single solid-state controller 104a with a single solid-state storage 110a. In another embodiment, there are a plurality of solid-state storage controllers 104a-n and associated solid-state storage 110a-n. In one embodiment, one or more solid state controllers 104a-104n-1, coupled to their associated solid-state storage 110a-110n-1, control data while at least one solid-state storage controller 104n, coupled to its associated solid-state storage 110n, controls index metadata.

[0100] In one embodiment, at least one solid-state controller 104 is field-programmable gate array ("FPGA") and controller functions are programmed into the FPGA. In a particular embodiment, the FPGA is a Xilinx.RTM. FPGA. In another embodiment, the solid-state storage controller 104 comprises components specifically designed as a solid-state storage controller 104, such as an application-specific integrated circuit ("ASIC") or custom logic solution. Each solid-state storage controller 104 typically includes a write data pipeline 106 and a read data pipeline 108, which are describe further in relation to FIG. 3. In another embodiment, at least one solid-state storage controller 104 is made up of a combination FPGA, ASIC, and custom logic components.

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[0101] Solid-State Storage

[0102] The solid state storage 110 is an array of non-volatile solid-state storage elements 216, 218, 220, arranged in banks 214, and accessed in parallel through a bi-directional storage input/output ("I/O") bus 210. The storage I/O bus 210, in one embodiment, is capable of unidirectional communication at any one time. For example, when data is being written to the solid-state storage 110, data cannot be read from the solid-state storage 110. In another embodiment, data can flow both directions simultaneously. However bi-directional, as used herein with respect to a data bus, refers to a data pathway that can have data flowing in only one direction at a time, but when data flowing one direction on the bi-directional data bus is stopped, data can flow in the opposite direction on the bi-directional data bus.

[0103] A solid-state storage element (e.g. SSS 0.0 216a) is typically configured as a chip (a package of one or more dies) or a die on a circuit board. As depicted, a solid-state storage element (e.g. 216a) operates independently or semi-independently of other solid-state storage elements (e.g. 218a) even if these several elements are packaged together in a chip package, a stack of chip packages, or some other package element. As depicted, a column of solid-state storage elements 216, 218, 220 is designated as a bank 214. As depicted, there may be "n" banks 214a-n and "m" solid-state storage elements 216a-m, 218a-m, 220a-m per bank in an array of n.times.m solid-state storage elements 216, 218, 220 in a solid-state storage 110. In one embodiment, a solid-state storage 110a includes twenty solid-state storage elements 216, 218, 220 per bank 214 with eight banks 214 and a solid-state storage 110n includes 2 solid-state storage elements 216, 218 per bank 214 with one bank 214. In one embodiment, each solid-state storage element 216, 218, 220 is comprised of a single-level cell ("SLC") devices. In another embodiment, each solid-state storage element 216, 218, 220 is comprised of multi-level cell ("MLC") devices.

[0104] In one embodiment, solid-state storage elements for multiple banks that share a common storage I/O bus 210a row (e.g. 216b, 218b, 220b) are packaged together. In one embodiment, a solid-state storage element 216, 218, 220 may have one or more dies per chip with one or more chips stacked vertically and each die may be accessed independently. In another embodiment, a solid-state storage element (e.g. SSS 0.0 216a) may have one or more virtual dies per die and one or more dies per chip and one or more chips stacked vertically and each virtual die may be accessed independently. In another embodiment, a solid-state storage

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element SSS 0.0 216a may have one or more virtual dies per die and one or more dies per chip with some or all of the one or more dies stacked vertically and each virtual die may be accessed independently.

[0105] In one embodiment, two dies are stacked vertically with four stacks per group to form eight storage elements (e.g. SSS 0.0-SSS 0.8) 216a-220a, each in a separate bank 214a-n. In another embodiment, 20 storage elements (e.g. SSS 0.0-SSS 20.0) 216 form a virtual bank 214a so that each of the eight virtual banks has 20 storage elements (e.g. SSS0.0-SSS 20.8) 216, 218, 220. Data is sent to the solid-state storage 110 over the storage I/O bus 210 to all storage elements of a particular group of storage elements (SSS 0.0-SSS 0.8) 216a, 218a, 220a. The storage control bus 212a is used to select a particular bank (e.g. Bank-0 214a) so that the data received over the storage I/O bus 210 connected to all banks 214 is written just to the selected bank 214a.

[0106] In a preferred embodiment, the storage I/O bus 210 is comprised of one or more independent I/O buses ("IIOBa-m" comprising 210a.a-m, 210n.a-m) wherein the solid-state storage elements within each row share one of the independent I/O buses accesses each solid-state storage element 216, 218, 220 in parallel so that all banks 214 are accessed simultaneously. For example, one channel of the storage I/O bus 210 may access a first solid-state storage element 216a, 218a, 220a of each bank 214a-n simultaneously. A second channel of the storage I/O bus 210 may access a second solid-state storage element 216b, 218b, 220b of each bank 214a-n simultaneously. Each row of solid-state storage element 216, 218, 220 is accessed simultaneously. In one embodiment, where solid-state storage elements 216, 218, 220 are multi-level (physically stacked), all physical levels of the solid-state storage elements 216, 218, 220 are accessed simultaneously. As used herein, "simultaneously" also includes near simultaneous access where devices are accessed at slightly different intervals to avoid switching noise. Simultaneously is used in this context to be distinguished from a sequential or serial access wherein commands and/or data are sent individually one after the other.

[0107] Typically, banks 214a-n are independently selected using the storage control bus 212. In one embodiment, a bank 214 is selected using a chip enable or chip select. Where both chip select and chip enable are available, the storage control bus 212 may select one level of a multi-level solid-state storage element 216, 218, 220. In other embodiments, other commands are used by the storage control bus 212 to individually select one level of a multi-level solid-state

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storage element 216, 218, 220. Solid-state storage elements 216, 218, 220 may also be selected through a combination of control and of address information transmitted on storage I/O bus 210 and the storage control bus 212.

[0108] In one embodiment, each solid-state storage element 216, 218, 220 is partitioned into erase blocks and each erase block is partitioned into pages. A typical page is 2000 bytes ("2 kB"). In one example, a solid-state storage element (e.g. SSS0.0) includes two registers and can program two pages so that a two-register solid-state storage element 216, 218, 220 has a capacity of 4 kB. A bank 214 of 20 solid-state storage elements 216, 218, 220 would then have an 80 kB capacity of pages accessed with the same address going out the channels of the storage I/O bus 210.

[0109] This group of pages in a bank 214 of solid-state storage elements 216, 218, 220 of 80 kB may be called a virtual page. Similarly, an erase block of each storage element 216a-m of a bank 214a may be grouped to form a virtual erase block. In a preferred embodiment, an erase block of pages within a solid-state storage element 216, 218, 220 is erased when an erase command is received within a solid-state storage element 216, 218, 220. Whereas the size and number of erase blocks, pages, planes, or other logical and physical divisions within a solid-state storage element 216, 218, 220 are expected to change over time with advancements in technology, it is to be expected that many embodiments consistent with new configurations are possible and are consistent with the general description herein.

[0110] Typically, when a packet is written to a particular location within a solid-state storage element 216, 218, 220, wherein the packet is intended to be written to a location within a particular page which is specific to a of a particular erase block of a particular element of a particular bank, a physical address is sent on the storage I/O bus 210 and followed by the packet. The physical address contains enough information for the solid-state storage element 216, 218, 220 to direct the packet to the designated location within the page. Since all storage elements in a row of storage elements (e.g. SSS 0.0-SSS 0.N 216a, 218a, 220a) are accessed simultaneously by the appropriate bus within the storage I/O bus 210a.a, to reach the proper page and to avoid writing the data packet to similarly addressed pages in the row of storage elements (SSS 0.0-SSS 0.N 216a, 218a, 220a), the bank 214a that includes the solid-state storage element SSS 0.0 216a with the correct page where the data packet is to be written is simultaneously selected by the storage control bus 212.

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[0111] Similarly, a read command traveling on the storage I/O bus 210 requires a simultaneous command on the storage control bus 212 to select a single bank 214a and the appropriate page within that bank 214a. In a preferred embodiment, a read command reads an entire page, and because there are multiple solid-state storage elements 216, 218, 220 in parallel in a bank 214, an entire virtual page is read with a read command. However, the read command may be broken into subcommands, as will be explained below with respect to bank interleave. A virtual page may also be accessed in a write operation.

[0112] An erase block erase command may be sent out to erase an erase block over the storage I/O bus 210 with a particular erase block address to erase a particular erase block. Typically, an erase block erase command may be sent over the parallel paths of the storage I/O bus 210 to erase a virtual erase block, each with a particular erase block address to erase a particular erase block. Simultaneously a particular bank (e.g. bank-0 214a) is selected over the storage control bus 212 to prevent erasure of similarly addressed erase blocks in all of the banks (banks 1-N 214b-n). Other commands may also be sent to a particular location using a combination of the storage I/O bus 210 and the storage control bus 212. One of skill in the art will recognize other ways to select a particular storage location using the bi-directional storage I/O bus 210 and the storage control bus 212.

[0113] In one embodiment, packets are written sequentially to the solid-state storage 110. For example, packets are streamed to the storage write buffers of a bank 214a of storage elements 216 and when the buffers are full, the packets are programmed to a designated virtual page. Packets then refill the storage write buffers and, when full, the packets are written to the next virtual page. The next virtual page may be in the same bank 214a or another bank (e.g. 214b). This process continues, virtual page after virtual page, typically until a virtual erase block is filled. In another embodiment, the streaming may continue across virtual erase block boundaries with the process continuing, virtual erase block after virtual erase block.

[0114] In a read, modify, write operation, data packets associated with the object are located and read in a read operation. Data segments of the modified object that have been modified are not written to the location from which they are read. Instead, the modified data segments are again converted to data packets and then written to the next available location in the virtual page currently being written. The object index entries for the respective data packets are modified to point to the packets that contain the modified data segments. The entry or entries

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in the object index for data packets associated with the same object that have not been modified will include pointers to original location of the unmodified data packets. Thus, if the original object is maintained, for example to maintain a previous version of the object, the original object will have pointers in the object index to all data packets as originally written. The new object will have pointers in the object index to some of the original data packets and pointers to the modified data packets in the virtual page that is currently being written.

[0115] In a copy operation, the object index includes an entry for the original object mapped to a number of packets stored in the solid-state storage 110. When a copy is made, a new object is created and a new entry is created in the object index mapping the new object to the original packets. The new object is also written to the solid-state storage 110 with its location mapped to the new entry in the object index. The new object packets may be used to identify the packets within the original object that are referenced in case changes have been made in the original object that have not been propagated to the copy and the object index is lost or corrupted.

[0116] Beneficially, sequentially writing packets facilitates a more even use of the solid-state storage 110 and allows the solid-storage device controller 202 to monitor storage hot spots and level usage of the various virtual pages in the solid-state storage 110. Sequentially writing packets also facilitates a powerful, efficient garbage collection system, which is described in detail below. One of skill in the art will recognize other benefits of sequential storage of data packets.

[0117] Solid-State Storage Device Controller

[0118] In various embodiments, the solid-state storage device controller 202 also includes a data bus 204, a local bus 206, a buffer controller 208, buffers 0-N 222a-n, a master controller 224, a direct memory access ("DMA") controller 226, a memory controller 228, a dynamic memory array 230, a static random memory array 232, a management controller 234, a management bus 236, a bridge 238 to a system bus 240, and miscellaneous logic 242, which are described below. In other embodiments, the system bus 240 is coupled to one or more network interface cards ("NICs") 244, some of which may include remote DMA ("RDMA") controllers 246, one or more central processing unit ("CPU") 248, one or more external memory controllers 250 and associated external memory arrays 252, one or more storage controllers 254, peer controllers 256, and application specific processors 258, which are described below. The

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components 244-258 connected to the system bus 240 may be located in the computer 112 or may be other devices.

[0119] Typically the solid-state storage controller(s) 104 communicate data to the solid-state storage 110 over a storage I/O bus 210. In a typical embodiment where the solid-state storage is arranged in banks 214 and each bank 214 includes multiple storage elements 216, 218, 220 accessed in parallel, the storage I/O bus 210 is an array of busses, one for each row of storage elements 216, 218, 220 spanning the banks 214. As used herein, the term "storage I/O bus" may refer to one storage I/O bus 210 or an array of data independent busses 204. In a preferred embodiment, each storage I/O bus 210 accessing a row of storage elements (e.g. 216a, 218a, 220a) may include a logical-to-physical mapping for storage divisions (e.g. erase blocks) accessed in a row of storage elements 216a, 218a, 220a. This mapping allows a logical address mapped to a physical address of a storage division to be remapped to a different storage division if the first storage division fails, partially fails, is inaccessible, or has some other problem. Remapping is explained further in relation to the remapping module 430 of FIGS. 4A and 4B.

[0120] Data may also be communicated to the solid-state storage controller(s) 104 from a requesting device 155 through the system bus 240, bridge 238, local bus 206, buffer(s) 222, and finally over a data bus 204. The data bus 204 typically is connected to one or more buffers 222a-n controlled with a buffer controller 208. The buffer controller 208 typically controls transfer of data from the local bus 206 to the buffers 222 and through the data bus 204 to the pipeline input buffer 306 and output buffer 330. The buffer controller 208 typically controls how data arriving from a requesting device 155 can be temporarily stored in a buffer 222 and then transferred onto a data bus 204, or vice versa, to account for different clock domains, to prevent data collisions, etc. The buffer controller 208 typically works in conjunction with the master controller 224 to coordinate data flow. As data arrives, the data will arrive on the system bus 240, be transferred to the local bus 206 through a bridge 238.

[0121] Typically the data is transferred from the local bus 206 to one or more data buffers 222 as directed by the master controller 224 and the buffer controller 208. The data then flows out of the buffer(s) 222 to the data bus 204, through a solid-state controller 104, and on to the solid-state storage 110 such as NAND flash or other storage media. In a preferred embodiment, data and associated out-of-band metadata ("object metadata") arriving with the data is communicated using one or more data channels comprising one or more solid-state storage

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controllers 104a-104n-1 and associated solid-state storage 110a-110n-1 while at least one channel (solid-state storage controller 104n, solid-state storage 110n) is dedicated to in-band metadata, such as index information and other metadata generated internally to the solid-state storage device 102.

[0122] The local bus 206 is typically a bidirectional bus or set of busses that allows for communication of data and commands between devices internal to the solid-state storage device controller 202 and between devices internal to the solid-state storage device 102 and devices 244-258 connected to the system bus 240. The bridge 238 facilitates communication between the local bus 206 and system bus 240. One of skill in the art will recognize other embodiments such as ring structures or switched star configurations and functions of buses 240, 206, 204, 210 and bridges 238.

[0123] The system bus 240 is typically a bus of a computer 112 or other device in which the solid-state storage device 102 is installed or connected. In one embodiment, the system bus 240 may be a PCI-e bus, a Serial Advanced Technology Attachment ("serial ATA") bus, parallel ATA, or the like. In another embodiment, the system bus 240 is an external bus such as small computer system interface ("SCSI"), FireWire, Fiber Channel, USB, PCIe-AS, or the like. The solid-state storage device 102 may be packaged to fit internally to a device or as an externally connected device.

[0124] The solid-state storage device controller 202 includes a master controller 224 that controls higher-level functions within the solid-state storage device 102. The master controller 224, in various embodiments, controls data flow by interpreting object requests and other requests, directs creation of indexes to map object identifiers associated with data to physical locations of associated data, coordinating DMA requests, etc. Many of the functions described herein are controlled wholly or in part by the master controller 224.

[0125] In one embodiment, the master controller 224 uses embedded controller(s). In another embodiment, the master controller 224 uses local memory such as a dynamic memory array 230 (dynamic random access memory "DRAM"), a static memory array 232 (static random access memory "SRAM"), etc. In one embodiment, the local memory is controlled using the master controller 224. In another embodiment, the master controller 224 accesses the local memory via a memory controller 228. In another embodiment, the master controller 224 runs a Linux server and may support various common server interfaces, such as the World Wide Web,

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hyper-text markup language ("HTML"), etc. In another embodiment, the master controller 224 uses a nano-processor. The master controller 224 may be constructed using programmable or standard logic, or any combination of controller types listed above. One skilled in the art will recognize many embodiments for the master controller 224.

[0126] In one embodiment, where the storage controller 152/solid-state storage device controller 202 manages multiple data storage devices/solid-state storage 110a-n, the master controller 224 divides the work load among internal controllers, such as the solid-state storage controllers 104a-n. For example, the master controller 224 may divide an object to be written to the data storage devices (e.g. solid-state storage 110a-n) so that a portion of the object is stored on each of the attached data storage devices. This feature is a performance enhancement allowing quicker storage and access to an object. In one embodiment, the master controller 224 is implemented using an FPGA. In another embodiment, the firmware within the master controller 224 may be updated through the management bus 236, the system bus 240 over a network connected to a NIC 244 or other device connected to the system bus 240.

[0127] In one embodiment, the master controller 224, which manages objects, emulates block storage such that a computer 112 or other device connected to the storage device/solid-state storage device 102 views the storage device/solid-state storage device 102 as a block storage device and sends data to specific physical addresses in the storage device/solid-state storage device 102. The master controller 224 then divides up the blocks and stores the data blocks as it would objects. The master controller 224 then maps the blocks and physical address sent with the block to the actual locations determined by the master controller 224. The mapping is stored in the object index. Typically, for block emulation, a block device application program interface ("API") is provided in a driver in the computer 112, client 114, or other device wishing to use the storage device/solid-state storage device 102 as a block storage device.

[0128] In another embodiment, the master controller 224 coordinates with NIC controllers 244 and embedded RDMA controllers 246 to deliver just-in-time RDMA transfers of data and command sets. NIC controller 244 may be hidden behind a non-transparent port to enable the use of custom drivers. Also, a driver on a client 114 may have access to the computer network 116 through an I/O memory driver using a standard stack API and operating in conjunction with NICs 244.

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[0129] In one embodiment, the master controller 224 is also a redundant array of independent drive ("RAID") controller. Where the data storage device/solid-state storage device 102 is networked with one or more other data storage devices/solid-state storage devices 102, the master controller 224 may be a RAID controller for single tier RAID, multi-tier RAID, progressive RAID, etc. The master controller 224 also allows some objects to be stored in a RAID array and other objects to be stored without RAID. In another embodiment, the master controller 224 may be a distributed RAID controller element. In another embodiment, the master controller 224 may comprise many RAID, distributed RAID, and other functions as described elsewhere.

[0130] In one embodiment, the master controller 224 coordinates with single or redundant network managers (e.g. switches) to establish routing, to balance bandwidth utilization, failover, etc. In another embodiment, the master controller 224 coordinates with integrated application specific logic (via local bus 206) and associated driver software. In another embodiment, the master controller 224 coordinates with attached application specific processors 258 or logic (via the external system bus 240) and associated driver software. In another embodiment, the master controller 224 coordinates with remote application specific logic (via the computer network 116) and associated driver software. In another embodiment, the master controller 224 coordinates with the local bus 206 or external bus attached hard disk drive ("HDD") storage controller.

[0131] In one embodiment, the master controller 224 communicates with one or more storage controllers 254 where the storage device/solid-state storage device 102 may appear as a storage device connected through a SCSI bus, Internet SCSI ("iSCSI"), fiber channel, etc. Meanwhile the storage device/solid-state storage device 102 may autonomously manage objects and may appear as an object file system or distributed object file system. The master controller 224 may also be accessed by peer controllers 256 and/or application specific processors 258.

[0132] In another embodiment, the master controller 224 coordinates with an autonomous integrated management controller to periodically validate FPGA code and/or controller software, validate FPGA code while running (reset) and/or validate controller software during power on (reset), support external reset requests, support reset requests due to watchdog timeouts, and support voltage, current, power, temperature, and other environmental measurements and setting of threshold interrupts. In another embodiment, the master controller

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224 manages garbage collection to free erase blocks for reuse. In another embodiment, the master controller 224 manages wear leveling. In another embodiment, the master controller 224 allows the data storage device/solid-state storage device 102 to be partitioned into multiple virtual devices and allows partition-based media encryption. In yet another embodiment, the master controller 224 supports a solid-state storage controller 104 with advanced, multi-bit ECC correction. One of skill in the art will recognize other features and functions of a master controller 224 in a storage controller 152, or more specifically in a solid-state storage device 102.

[0133] In one embodiment, the solid-state storage device controller 202 includes a memory controller 228 which controls a dynamic random memory array 230 and/or a static random memory array 232. As stated above, the memory controller 228 may be independent or integrated with the master controller 224. The memory controller 228 typically controls volatile memory of some type, such as DRAM (dynamic random memory array 230) and SRAM (static random memory array 232). In other examples, the memory controller 228 also controls other memory types such as electrically erasable programmable read only memory ("EEPROM"), etc. In other embodiments, the memory controller 228 controls two or more memory types and the memory controller 228 may include more than one controller. Typically, the memory controller 228 controls as much SRAM 232 as is feasible and by DRAM 230 to supplement the SRAM 232.

[0134] In one embodiment, the object index is stored in memory 230, 232 and then periodically off-loaded to a channel of the solid-state storage 110n or other non-volatile memory. One of skill in the art will recognize other uses and configurations of the memory controller 228, dynamic memory array 230, and static memory array 232.

[0135] In one embodiment, the solid-state storage device controller 202 includes a DMA controller 226 that controls DMA operations between the storage device/solid-state storage device 102 and one or more external memory controllers 250 and associated external memory arrays 252 and CPUs 248. Note that the external memory controllers 250 and external memory arrays 252 are called external because they are external to the storage device/solid-state storage device 102. In addition the DMA controller 226 may also control RDMA operations with requesting devices through a NIC 244 and associated RDMA controller 246. DMA and RDMA are explained in more detail below.

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[0136] In one embodiment, the solid-state storage device controller 202 includes a management controller 234 connected to a management bus 236. Typically the management controller 234 manages environmental metrics and status of the storage device/solid-state storage device 102. The management controller 234 may monitor device temperature, fan speed, power supply settings, etc. over the management bus 236. The management controller 234 may support the reading and programming of erasable programmable read only memory ("EEPROM") for storage of FPGA code and controller software. Typically the management bus 236 is connected to the various components within the storage device/solid-state storage device 102. The management controller 234 may communicate alerts, interrupts, etc. over the local bus 206 or may include a separate connection to a system bus 240 or other bus. In one embodiment the management bus 236 is an Inter-Integrated Circuit ("I.sup.2C") bus. One of skill in the art will recognize other related functions and uses of a management controller 234 connected to components of the storage device/solid-state storage device 102 by a management bus 236.

[0137] In one embodiment, the solid-state storage device controller 202 includes miscellaneous logic 242 that may be customized for a specific application. Typically where the solid-state device controller 202 or master controller 224 is/are configured using a FPGA or other configurable controller, custom logic may be included based on a particular application, customer requirement, storage requirement, etc.

[0138] Data Pipeline

[0139] FIG. 3 is a schematic block diagram illustrating one embodiment 300 of a solid-state storage controller 104 with a write data pipeline 106 and a read data pipeline 108 in a solid-state storage device 102 in accordance with the present invention. The embodiment 300 includes a data bus 204, a local bus 206, and buffer control 208, which are substantially similar to those described in relation to the solid-state storage device controller 202 of FIG. 2. The write data pipeline 106 includes a packetizer 302 and an error-correcting code ("ECC") generator 304. In other embodiments, the write data pipeline 106 includes an input buffer 306, a write synchronization buffer 308, a write program module 310, a compression module 312, an encryption module 314, a garbage collector bypass 316 (with a portion within the read data pipeline 108), a media encryption module 318, and a write buffer 320. The read data pipeline 108 includes a read synchronization buffer 328, an ECC correction module 322, a depacketizer 324, an alignment module 326, and an output buffer 330. In other embodiments, the read data

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pipeline 108 may include a media decryption module 332, a portion of the garbage collector bypass 316, a decryption module 334, a decompression module 336, and a read program module 338. The solid-state storage controller 104 may also include control and status registers 340 and control queues 342, a bank interleave controller 344, a synchronization buffer 346, a storage bus controller 348, and a multiplexer ("MUX") 350. The components of the solid-state controller 104 and associated write data pipeline 106 and read data pipeline 108 are described below. In other embodiments, synchronous solid-state storage 110 may be used and synchronization buffers 308 328 may be eliminated.

[0140] Write Data Pipeline

[0141] The write data pipeline 106 includes a packetizer 302 that receives a data or metadata segment to be written to the solid-state storage, either directly or indirectly through another write data pipeline 106 stage, and creates one or more packets sized for the solid-state storage 110. The data or metadata segment is typically part of an object, but may also include an entire object. In another embodiment, the data segment is part of a block of data, but may also include an entire block of data. Typically, an object is received from a computer 112, client 114, or other computer or device and is transmitted to the solid-state storage device 102 in data segments streamed to the solid-state storage device 102 or computer 112. A data segment may also be known by another name, such as data parcel, but as referenced herein includes all or a portion of an object or data block.

[0142] Each object is stored as one or more packets. Each object may have one or more container packets. Each packet contains a header. The header may include a header type field. Type fields may include data, object attribute, metadata, data segment delimiters (multi-packet), object structures, object linkages, and the like. The header may also include information regarding the size of the packet, such as the number of bytes of data included in the packet. The length of the packet may be established by the packet type. The header may include information that establishes the relationship of the packet to the object. An example might be the use of an offset in a data packet header to identify the location of the data segment within the object. One of skill in the art will recognize other information that may be included in a header added to data by a packetizer 302 and other information that may be added to a data packet.

[0143] Each packet includes a header and possibly data from the data or metadata segment. The header of each packet includes pertinent information to relate the packet to the

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object to which the packet belongs. For example, the header may include an object identifier and offset that indicates the data segment, object, or data block from which the data packet was formed. The header may also include a logical address used by the storage bus controller 348 to store the packet. The header may also include information regarding the size of the packet, such as the number of bytes included in the packet. The header may also include a sequence number that identifies where the data segment belongs with respect to other packets within the object when reconstructing the data segment or object. The header may include a header type field. Type fields may include data, object attributes, metadata, data segment delimiters (multi-packet), object structures, object linkages, and the like. One of skill in the art will recognize other information that may be included in a header added to data or metadata by a packetizer 302 and other information that may be added to a packet.

[0144] The write data pipeline 106 includes an ECC generator 304 that generates one or more error-correcting codes ("ECC") for the one or more packets received from the packetizer 302. The ECC generator 304 typically uses an error correcting algorithm to generate ECC which is stored with the packet. The ECC stored with the packet is typically used to detect and correct errors introduced into the data through transmission and storage. In one embodiment, packets are streamed into the ECC generator 304 as un-encoded blocks of length N. A syndrome of length S is calculated, appended and output as an encoded block of length N+S. The value of N and S are dependent upon the characteristics of the algorithm which is selected to achieve specific performance, efficiency, and robustness metrics. In the preferred embodiment, there is no fixed relationship between the ECC blocks and the packets; the packet may comprise more than one ECC block; the ECC block may comprise more than one packet; and a first packet may end anywhere within the ECC block and a second packet may begin after the end of the first packet within the same ECC block. In the preferred embodiment, ECC algorithms are not dynamically modified. In a preferred embodiment, the ECC stored with the data packets is robust enough to correct errors in more than two bits.

[0145] Beneficially, using a robust ECC algorithm allowing more than single bit correction or even double bit correction allows the life of the solid-state storage 110 to be extended. For example, if flash memory is used as the storage medium in the solid-state storage 110, the flash memory may be written approximately 100,000 times without error per erase cycle. This usage limit may be extended using a robust ECC algorithm. Having the ECC

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generator 304 and corresponding ECC correction module 322 onboard the solid-state storage device 102, the solid-state storage device 102 can internally correct errors and has a longer useful life than if a less robust ECC algorithm is used, such as single bit correction. However, in other embodiments the ECC generator 304 may use a less robust algorithm and may correct single-bit or double-bit errors. In another embodiment, the solid-state storage device 110 may comprise less reliable storage such as multi-level cell ("MLC") flash in order to increase capacity, which storage may not be sufficiently reliable without more robust ECC algorithms.

[0146] In one embodiment, the write pipeline 106 includes an input buffer 306 that receives a data segment to be written to the solid-state storage 110 and stores the incoming data segments until the next stage of the write data pipeline 106, such as the packetizer 302 (or other stage for a more complex write data pipeline 106) is ready to process the next data segment. The input buffer 306 typically allows for discrepancies between the rate data segments are received and processed by the write data pipeline 106 using an appropriately sized data buffer. The input buffer 306 also allows the data bus 204 to transfer data to the write data pipeline 106 at rates greater than can be sustained by the write data pipeline 106 in order to improve efficiency of operation of the data bus 204. Typically when the write data pipeline 106 does not include an input buffer 306, a buffering function is performed elsewhere, such as in the solid-state storage device 102 but outside the write data pipeline 106, in the computer 112, such as within a network interface card ("NIC"), or at another device, for example when using remote direct memory access ("RDMA").

[0147] In another embodiment, the write data pipeline 106 also includes a write synchronization buffer 308 that buffers packets received from the ECC generator 304 prior to writing the packets to the solid-state storage 110. The write synch buffer 308 is located at a boundary between a local clock domain and a solid-state storage clock domain and provides buffering to account for the clock domain differences. In other embodiments, synchronous solid-state storage 110 may be used and synchronization buffers 308 328 may be eliminated.

[0148] In one embodiment, the write data pipeline 106 also includes a media encryption module 318 that receives the one or more packets from the packetizer 302, either directly or indirectly, and encrypts the one or more packets using an encryption key unique to the solid-state storage device 102 prior to sending the packets to the ECC generator 304. Typically, the entire packet is encrypted, including the headers. In another embodiment, headers are not encrypted. In

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this document, encryption key is understood to mean a secret encryption key that is managed externally from an embodiment that integrates the solid-state storage 110 and where the embodiment requires encryption protection. The media encryption module 318 and corresponding media decryption module 332 provide a level of security for data stored in the solid-state storage 110. For example, where data is encrypted with the media encryption module 318, if the solid-state storage 110 is connected to a different solid-state storage controller 104, solid-state storage device 102, or computer 112, the contents of the solid-state storage 110 typically could not be read without use of the same encryption key used during the write of the data to the solid-state storage 110 without significant effort.

[0149] In a typical embodiment, the solid-state storage device 102 does not store the encryption key in non-volatile storage and allows no external access to the encryption key. The encryption key is provided to the solid-state storage controller 104 during initialization. The solid-sate storage device 102 may use and store a non-secret cryptographic nonce that is used in conjunction with an encryption key. A different nonce may be stored with every packet. Data segments may be split between multiple packets with unique nonces for the purpose of improving protection by the encryption algorithm. The encryption key may be received from a client 114, a computer 112, key manager, or other device that manages the encryption key to be used by the solid-state storage controller 104. In another embodiment, the solid-state storage 110 may have two or more partitions and the solid-state storage controller 104 behaves as though it were two or more solid-state storage controllers 104, each operating on a single partition within the solid-state storage 110. In this embodiment, a unique media encryption key may be used with each partition.

[0150] In another embodiment, the write data pipeline 106 also includes an encryption module 314 that encrypts a data or metadata segment received from the input buffer 306, either directly or indirectly, prior sending the data segment to the packetizer 302, the data segment encrypted using an encryption key received in conjunction with the data segment. The encryption module 314 differs from the media encryption module 318 in that the encryption keys used by the encryption module 314 to encrypt data may not be common to all data stored within the solid-state storage device 102 but may vary on an object basis and received in conjunction with receiving data segments as described below. For example, an encryption key for a data segment to be encrypted by the encryption module 314 may be received with the data segment or may be

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received as part of a command to write an object to which the data segment belongs. The solid-sate storage device 102 may use and store a non-secret cryptographic nonce in each object packet that is used in conjunction with the encryption key. A different nonce may be stored with every packet. Data segments may be split between multiple packets with unique nonces for the purpose of improving protection by the encryption algorithm. In one embodiment, the nonce used by the media encryption module 318 is the same as that used by the encryption module 314.

[0151] The encryption key may be received from a client 114, a computer 112, key manager, or other device that holds the encryption key to be used to encrypt the data segment. In one embodiment, encryption keys are transferred to the solid-state storage controller 104 from one of a solid-state storage device 102, computer 112, client 114, or other external agent which has the ability to execute industry standard methods to securely transfer and protect private and public keys.

[0152] In one embodiment, the encryption module 314 encrypts a first packet with a first encryption key received in conjunction with the packet and encrypts a second packet with a second encryption key received in conjunction with the second packet. In another embodiment, the encryption module 314 encrypts a first packet with a first encryption key received in conjunction with the packet and passes a second data packet on to the next stage without encryption. Beneficially, the encryption module 314 included in the write data pipeline 106 of the solid-state storage device 102 allows object-by-object or segment-by-segment data encryption without a single file system or other external system to keep track of the different encryption keys used to store corresponding objects or data segments. Each requesting device 155 or related key manager independently manages encryption keys used to encrypt only the objects or data segments sent by the requesting device 155.

[0153] In another embodiment, the write data pipeline 106 includes a compression module 312 that compresses the data for metadata segment prior to sending the data segment to the packetizer 302. The compression module 312 typically compresses a data or metadata segment using a compression routine known to those of skill in the art to reduce the storage size of the segment. For example, if a data segment includes a string of 512 zeros, the compression module 312 may replace the 512 zeros with code or token indicating the 512 zeros where the code is much more compact than the space taken by the 512 zeros.

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[0154] In one embodiment, the compression module 312 compresses a first segment with a first compression routine and passes along a second segment without compression. In another embodiment, the compression module 312 compresses a first segment with a first compression routine and compresses the second segment with a second compression routine. Having this flexibility within the solid-state storage device 102 is beneficial so that clients 114 or other devices writing data to the solid-state storage device 102 may each specify a compression routine or so that one can specify a compression routine while another specifies no compression. Selection of compression routines may also be selected according to default settings on a per object type or object class basis. For example, a first object of a specific object may be able to override default compression routine settings and a second object of the same object class and object type may use the default compression routine and a third object of the same object class and object type may use no compression.

[0155] In one embodiment, the write data pipeline 106 includes a garbage collector bypass 316 that receives data segments from the read data pipeline 108 as part of a data bypass in a garbage collection system. A garbage collection system typically marks packets that are no longer valid, typically because the packet is marked for deletion or has been modified and the modified data is stored in a different location. At some point, the garbage collection system determines that a particular section of storage may be recovered. This determination may be due to a lack of available storage capacity, the percentage of data marked as invalid reaching a threshold, a consolidation of valid data, an error detection rate for that section of storage reaching a threshold, or improving performance based on data distribution, etc. Numerous factors may be considered by a garbage collection algorithm to determine when a section of storage is to be recovered.

[0156] Once a section of storage has been marked for recovery, valid packets in the section typically must be relocated. The garbage collector bypass 316 allows packets to be read into the read data pipeline 108 and then transferred directly to the write data pipeline 106 without being routed out of the solid-state storage controller 104. In a preferred embodiment, the garbage collector bypass 316 is part of an autonomous garbage collector system that operates within the solid-state storage device 102. This allows the solid-state storage device 102 to manage data so that data is systematically spread throughout the solid-state storage 110 to improve performance,

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data reliability and to avoid overuse and underuse of any one location or area of the solid-state storage 110 and to lengthen the useful life of the solid-state storage 110.

[0157] The garbage collector bypass 316 coordinates insertion of segments into the write data pipeline 106 with other segments being written by clients 114 or other devices. In the depicted embodiment, the garbage collector bypass 316 is before the packetizer 302 in the write data pipeline 106 and after the depacketizer 324 in the read data pipeline 108, but may also be located elsewhere in the read and write data pipelines 106, 108. The garbage collector bypass 316 may be used during a flush of the write pipeline 106 to fill the remainder of the virtual page in order to improve the efficiency of storage within the Solid-State Storage 110 and thereby reduce the frequency of garbage collection.

[0158] In one embodiment, the write data pipeline 106 includes a write buffer 320 that buffers data for efficient write operations. Typically, the write buffer 320 includes enough capacity for packets to fill at least one virtual page in the solid-state storage 110. This allows a write operation to send an entire page of data to the solid-state storage 110 without interruption. By sizing the write buffer 320 of the write data pipeline 106 and buffers within the read data pipeline 108 to be the same capacity or larger than a storage write buffer within the solid-state storage 110, writing and reading data is more efficient since a single write command may be crafted to send a full virtual page of data to the solid-state storage 110 instead of multiple commands.

[0159] While the write buffer 320 is being filled, the solid-state storage 110 may be used for other read operations. This is advantageous because other solid-state devices with a smaller write buffer or no write buffer may tie up the solid-state storage when data is written to a storage write buffer and data flowing into the storage write buffer stalls. Read operations will be blocked until the entire storage write buffer is filled and programmed. Another approach for systems without a write buffer or a small write buffer is to flush the storage write buffer that is not full in order to enable reads. Again this is inefficient because multiple write/program cycles are required to fill a page.

[0160] For depicted embodiment with a write buffer 320 sized larger than a virtual page, a single write command, which includes numerous subcommands, can then be followed by a single program command to transfer the page of data from the storage write buffer in each solid-state storage element 216, 218, 220 to the designated page within each solid-state storage

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element 216, 218, 220. This technique has the benefits of eliminating partial page programming, which is known to reduce data reliability and durability and freeing up the destination bank for reads and other commands while the buffer fills.

[0161] In one embodiment, the write buffer 320 is a ping-pong buffer where one side of the buffer is filled and then designated for transfer at an appropriate time while the other side of the ping-pong buffer is being filled. In another embodiment, the write buffer 320 includes a first-in first-out ("FIFO") register with a capacity of more than a virtual page of data segments. One of skill in the art will recognize other write buffer 320 configurations that allow a virtual page of data to be stored prior to writing the data to the solid-state storage 110.

[0162] In another embodiment, the write buffer 320 is sized smaller than a virtual page so that less than a page of information could be written to a storage write buffer in the solid-state storage 110. In the embodiment, to prevent a stall in the write data pipeline 106 from holding up read operations, data is queued using the garbage collection system that needs to be moved from one location to another as part of the garbage collection process. In case of a data stall in the write data pipeline 106, the data can be fed through the garbage collector bypass 316 to the write buffer 320 and then on to the storage write buffer in the solid-state storage 110 to fill the pages of a virtual page prior to programming the data. In this way a data stall in the write data pipeline 106 would not stall reading from the solid-state storage device 102.

[0163] In another embodiment, the write data pipeline 106 includes a write program module 310 with one or more user-definable functions within the write data pipeline 106. The write program module 310 allows a user to customize the write data pipeline 106. A user may customize the write data pipeline 106 based on a particular data requirement or application. Where the solid-state storage controller 104 is an FPGA, the user may program the write data pipeline 106 with custom commands and functions relatively easily. A user may also use the write program module 310 to include custom functions with an ASIC, however, customizing an ASIC may be more difficult than with an FPGA. The write program module 310 may include buffers and bypass mechanisms to allow a first data segment to execute in the write program module 310 while a second data segment may continue through the write data pipeline 106. In another embodiment, the write program module 310 may include a processor core that can be programmed through software.

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[0164] Note that the write program module 310 is shown between the input buffer 306 and the compression module 312, however, the write program module 310 could be anywhere in the write data pipeline 106 and may be distributed among the various stages 302-320. In addition, there may be multiple write program modules 310 distributed among the various states 302-320 that are programmed and operate independently. In addition, the order of the stages 302-320 may be altered. One of skill in the art will recognize workable alterations to the order of the stages 302-320 based on particular user requirements.

[0165] Read Data Pipeline

[0166] The read data pipeline 108 includes an ECC correction module 322 that determines if a data error exists in ECC blocks a requested packet received from the solid-state storage 110 by using ECC stored with each ECC block of the requested packet. The ECC correction module 322 then corrects any errors in the requested packet if any error exists and the errors are correctable using the ECC. For example, if the ECC can detect an error in six bits but can only correct three bit errors, the ECC correction module 322 corrects ECC blocks of the requested packet with up to three bits in error. The ECC correction module 322 corrects the bits in error by changing the bits in error to the correct one or zero state so that the requested data packet is identical to when it was written to the solid-state storage 110 and the ECC was generated for the packet.

[0167] If the ECC correction module 322 determines that the requested packets contains more bits in error than the ECC can correct, the ECC correction module 322 cannot correct the errors in the corrupted ECC blocks of the requested packet and sends an interrupt. In one embodiment, the ECC correction module 322 sends an interrupt with a message indicating that the requested packet is in error. The message may include information that the ECC correction module 322 cannot correct the errors or the inability of the ECC correction module 322 to correct the errors may be implied. In another embodiment, the ECC correction module 322 sends the corrupted ECC blocks of the requested packet with the interrupt and/or the message.

[0168] In the preferred embodiment, a corrupted ECC block or portion of a corrupted ECC block of the requested packet that cannot be corrected by the ECC correction module 322 is read by the master controller 224, corrected, and returned to the ECC correction module 322 for further processing by the read data pipeline 108. In one embodiment, a corrupted ECC block or portion of a corrupted ECC block of the requested packet is sent to the device requesting the

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data. The requesting device 155 may correct the ECC block or replace the data using another copy, such as a backup or mirror copy, and then may use the replacement data of the requested data packet or return it to the read data pipeline 108. The requesting device 155 may use header information in the requested packet in error to identify data required to replace the corrupted requested packet or to replace the object to which the packet belongs. In another preferred embodiment, the solid-state storage controller 104 stores data using some type of RAID and is able to recover the corrupted data. In another embodiment, the ECC correction module 322 sends and interrupt and/or message and the receiving device fails the read operation associated with the requested data packet. One of skill in the art will recognize other options and actions to be taken as a result of the ECC correction module 322 determining that one or more ECC blocks of the requested packet are corrupted and that the ECC correction module 322 cannot correct the errors.

[0169] The read data pipeline 108 includes a depacketizer 324 that receives ECC blocks of the requested packet from the ECC correction module 322, directly or indirectly, and checks and removes one or more packet headers. The depacketizer 324 may validate the packet headers by checking packet identifiers, data length, data location, etc. within the headers. In one embodiment, the header includes a hash code that can be used to validate that the packet delivered to the read data pipeline 108 is the requested packet. The depacketizer 324 also removes the headers from the requested packet added by the packetizer 302. The depacketizer 324 may directed to not operate on certain packets but pass these forward without modification. An example might be a container label that is requested during the course of a rebuild process where the header information is required by the object index reconstruction module 272. Further examples include the transfer of packets of various types destined for use within the solid-state storage device 102. In another embodiment, the depacketizer 324 operation may be packet type dependent.

[0170] The read data pipeline 108 includes an alignment module 326 that receives data from the depacketizer 324 and removes unwanted data. In one embodiment, a read command sent to the solid-state storage 110 retrieves a packet of data. A device requesting the data may not require all data within the retrieved packet and the alignment module 326 removes the unwanted data. If all data within a retrieved page is requested data, the alignment module 326 does not remove any data.

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[0171] The alignment module 326 re-formats the data as data segments of an object in a form compatible with a device requesting the data segment prior to forwarding the data segment to the next stage. Typically, as data is processed by the read data pipeline 108, the size of data segments or packets changes at various stages. The alignment module 326 uses received data to format the data into data segments suitable to be sent to the requesting device 155 and joined to form a response. For example, data from a portion of a first data packet may be combined with data from a portion of a second data packet. If a data segment is larger than a data requested by the requesting device 155, the alignment module 326 may discard the unwanted data.

[0172] In one embodiment, the read data pipeline 108 includes a read synchronization buffer 328 that buffers one or more requested packets read from the solid-state storage 110 prior to processing by the read data pipeline 108. The read synchronization buffer 328 is at the boundary between the solid-state storage clock domain and the local bus clock domain and provides buffering to account for the clock domain differences.

[0173] In another embodiment, the read data pipeline 108 includes an output buffer 330 that receives requested packets from the alignment module 326 and stores the packets prior to transmission to the requesting device 155. The output buffer 330 accounts for differences between when data segments are received from stages of the read data pipeline 108 and when the data segments are transmitted to other parts of the solid-state storage controller 104 or to the requesting device. The output buffer 330 also allows the data bus 204 to receive data from the read data pipeline 108 at rates greater than can be sustained by the read data pipeline 108 in order to improve efficiency of operation of the data bus 204.

[0174] In one embodiment, the read data pipeline 108 includes a media decryption module 332 that receives one or more encrypted requested packets from the ECC correction module 322 and decrypts the one or more requested packets using the encryption key unique to the solid-state storage device 102 prior to sending the one or more requested packets to the depacketizer 324. Typically the encryption key used to decrypt data by the media decryption module 332 is identical to the encryption key used by the media encryption module 318. In another embodiment, the solid-state storage 110 may have two or more partitions and the solid-state storage controller 104 behaves as though it were two or more solid-state storage controllers 104 each operating on a single partition within the solid-state storage 110. In this embodiment, a unique media encryption key may be used with each partition.

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[0175] In another embodiment, the read data pipeline 108 includes a decryption module 334 that decrypts a data segment formatted by the depacketizer 324 prior to sending the data segment to the output buffer 330. The data segment decrypted using an encryption key received in conjunction with the read request that initiates retrieval of the requested packet received by the read synchronization buffer 328. The decryption module 334 may decrypt a first packet with an encryption key received in conjunction with the read request for the first packet and then may decrypt a second packet with a different encryption key or may pass the second packet on to the next stage of the read data pipeline 108 without decryption. Typically, the decryption module 334 uses a different encryption key to decrypt a data segment than the media decryption module 332 uses to decrypt requested packets. When the packet was stored with a non-secret cryptographic nonce, the nonce is used in conjunction with an encryption key to decrypt the data packet. The encryption key may be received from a client 114, a computer 112, key manager, or other device that manages the encryption key to be used by the solid-state storage controller 104.

[0176] In another embodiment, the read data pipeline 108 includes a decompression module 336 that decompresses a data segment formatted by the depacketizer 324. In the preferred embodiment, the decompression module 336 uses compression information stored in one or both of the packet header and the container label to select a complementary routine to that used to compress the data by the compression module 312. In another embodiment, the decompression routine used by the decompression module 336 is dictated by the device requesting the data segment being decompressed. In another embodiment, the decompression module 336 selects a decompression routine according to default settings on a per object type or object class basis. A first packet of a first object may be able to override a default decompression routine and a second packet of a second object of the same object class and object type may use the default decompression routine and a third packet of a third object of the same object class and object type may use no decompression.

[0177] In another embodiment, the read data pipeline 108 includes a read program module 338 that includes one or more user-definable functions within the read data pipeline 108. The read program module 338 has similar characteristics to the write program module 310 and allows a user to provide custom functions to the read data pipeline 108. The read program module 338 may be located as shown in FIG. 3, may be located in another position within the read data pipeline 108, or may include multiple parts in multiple locations within the read data

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pipeline 108. Additionally, there may be multiple read program modules 338 within multiple locations within the read data pipeline 108 that operate independently. One of skill in the art will recognize other forms of a read program module 338 within a read data pipeline 108. As with the write data pipeline 106, the stages of the read data pipeline 108 may be rearranged and one of skill in the art will recognize other orders of stages within the read data pipeline 108.

[0178] The solid-state storage controller 104 includes control and status registers 340 and corresponding control queues 342. The control and status registers 340 and control queues 342 facilitate control and sequencing commands and subcommands associated with data processed in the write and read data pipelines 106, 108. For example, a data segment in the packetizer 302 may have one or more corresponding control commands or instructions in a control queue 342 associated with the ECC generator 304. As the data segment is packetized, some of the instructions or commands may be executed within the packetizer 302. Other commands or instructions may be passed to the next control queue 342 through the control and status registers 340 as the newly formed data packet created from the data segment is passed to the next stage.

[0179] Commands or instructions may be simultaneously loaded into the control queues 342 for a packet being forwarded to the write data pipeline 106 with each pipeline stage pulling the appropriate command or instruction as the respective packet is executed by that stage. Similarly, commands or instructions may be simultaneously loaded into the control queues 342 for a packet being requested from the read data pipeline 108 with each pipeline stage pulling the appropriate command or instruction as the respective packet is executed by that stage. One of skill in the art will recognize other features and functions of control and status registers 340 and control queues 342.

[0180] The solid-state storage controller 104 and or solid-state storage device 102 may also include a bank interleave controller 344, a synchronization buffer 346, a storage bus controller 348, and a multiplexer ("MUX") 350, which are described in relation to FIGS. 4A and 4B.

[0181] Bank Interleave

[0182] FIG. 4A is a schematic block diagram illustrating one embodiment 400 of a bank interleave controller 344 in the solid-state storage controller 104 in accordance with the present invention. The bank interleave controller 344 is connected to the control and status registers 340 and to the storage I/O bus 210 and storage control bus 212 through the MUX 350, storage bus

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controller 348, and synchronization buffer 346, which are described below. The bank interleave controller 344 includes a read agent 402, a write agent 404, an erase agent 406, a management agent 408, read queues 410a-n, write queues 412a-n, erase queues 414a-n, and management queues 416a-n for the banks 214 in the solid-state storage 110, bank controllers 418a-n, a bus arbiter 420, and a status MUX 422, which are described below. The storage bus controller 348 includes a mapping module 424 with a remapping module 430, a status capture module 426, and a NAND bus controller 428, which are described below.

[0183] The bank interleave controller 344 directs one or more commands to two or more queues in the bank interleave controller 344 and coordinates among the banks 214 of the solid-state storage 110 execution of the commands stored in the queues, such that a command of a first type executes on one bank 214a while a command of a second type executes on a second bank 214b. The one or more commands are separated by command type into the queues. Each bank 214 of the solid-state storage 110 has a corresponding set of queues within the bank interleave controller 344 and each set of queues includes a queue for each command type.

[0184] The bank interleave controller 344 coordinates among the banks 214 of the solid-state storage 110 execution of the commands stored in the queues. For example, a command of a first type executes on one bank 214a while a command of a second type executes on a second bank 214b. Typically the command types and queue types include read and write commands and queues 410, 412, but may also include other commands and queues that are storage media specific. For example, in the embodiment depicted in FIG. 4A, erase and management queues 414, 416 are included and would be appropriate for flash memory, NRAM, MRAM, DRAM, PRAM, etc.

[0185] For other types of solid-state storage 110, other types of commands and corresponding queues may be included without straying from the scope of the invention. The flexible nature of an FPGA solid-state storage controller 104 allows flexibility in storage media. If flash memory were changed to another solid-state storage type, the bank interleave controller 344, storage bus controller 348, and MUX 350 could be altered to accommodate the media type without significantly affecting the data pipelines 106, 108 and other solid-state storage controller 104 functions.

[0186] In the embodiment depicted in FIG. 4A, the bank interleave controller 344 includes, for each bank 214, a read queue 410 for reading data from the solid-state storage 110, a

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write queue 412 for write commands to the solid-state storage 110, an erase queue 414 for erasing an erase block in the solid-state storage, an a management queue 416 for management commands. The bank interleave controller 344 also includes corresponding read, write, erase, and management agents 402, 404, 406, 408. In another embodiment, the control and status registers 340 and control queues 342 or similar components queue commands for data sent to the banks 214 of the solid-state storage 110 without a bank interleave controller 344.

[0187] The agents 402, 404, 406, 408, in one embodiment, direct commands of the appropriate type destined for a particular bank 214a to the correct queue for the bank 214a. For example, the read agent 402 may receive a read command for bank-1 214b and directs the read command to the bank-1 read queue 410b. The write agent 404 may receive a write command to write data to a location in bank-0 214a of the solid-state storage 110 and will then send the write command to the bank-0 write queue 412a. Similarly, the erase agent 406 may receive an erase command to erase an erase block in bank-1 214b and will then pass the erase command to the bank-1 erase queue 414b. The management agent 408 typically receives management commands, status requests, and the like, such as a reset command or a request to read a configuration register of a bank 214, such as bank-0 214a. The management agent 408 sends the management command to the bank-0 management queue 416a.

[0188] The agents 402, 404, 406, 408 typically also monitor status of the queues 410, 412, 414, 416 and send status, interrupt, or other messages when the queues 410, 412, 414, 416 are full, nearly full, non-functional, etc. In one embodiment, the agents 402, 404, 406, 408 receive commands and generate corresponding sub-commands. In one embodiment, the agents 402, 404, 406, 408 receive commands through the control & status registers 340 and generate corresponding sub-commands which are forwarded to the queues 410, 412, 414, 416. One of skill in the art will recognize other functions of the agents 402, 404, 406, 408.

[0189] The queues 410, 412, 414, 416 typically receive commands and store the commands until required to be sent to the solid-state storage banks 214. In a typical embodiment, the queues 410, 412, 414, 416 are first-in, first-out ("FIFO") registers or a similar component that operates as a FIFO. In another embodiment, the queues 410, 412, 414, 416 store commands in an order that matches data, order of importance, or other criteria.

[0190] The bank controllers 418 typically receive commands from the queues 410, 412, 414, 416 and generate appropriate subcommands. For example, the bank-0 write queue 412a may

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receive a command to write a page of data packets to bank-0 214a. The bank-0 controller 418a may receive the write command at an appropriate time and may generate one or more write subcommands for each data packet stored in the write buffer 320 to be written to the page in bank-0 214a. For example, bank-0 controller 418a may generate commands to validate the status of bank 0 214a and the solid-state storage array 216, select the appropriate location for writing one or more data packets, clear the input buffers within the solid-state storage memory array 216, transfer the one or more data packets to the input buffers, program the input buffers into the selected location, verify that the data was correctly programmed, and if program failures occur do one or more of interrupting the master controller 224, retrying the write to the same physical location, and retrying the write to a different physical location. Additionally, in conjunction with example write command, the storage bus controller 348 will cause the one or more commands to multiplied to each of the each of the storage I/O buses 210a-n with the logical address of the command mapped to a first physical addresses for storage I/O bus 210a, and mapped to a second physical address for storage I/O bus 210b, and so forth as further described below.

[0191] Typically, bus arbiter 420 selects from among the bank controllers 418 and pulls subcommands from output queues within the bank controllers 418 and forwards these to the Storage Bus Controller 348 in a sequence that optimizes the performance of the banks 214. In another embodiment, the bus arbiter 420 may respond to a high level interrupt and modify the normal selection criteria. In another embodiment, the master controller 224 can control the bus arbiter 420 through the control and status registers 340. One of skill in the art will recognize other means by which the bus arbiter 420 may control and interleave the sequence of commands from the bank controllers 418 to the solid-state storage 110.

[0192] The bus arbiter 420 typically coordinates selection of appropriate commands, and corresponding data when required for the command type, from the bank controllers 418 and sends the commands and data to the storage bus controller 348. The bus arbiter 420 typically also sends commands to the storage control bus 212 to select the appropriate bank 214. For the case of flash memory or other solid-state storage 110 with an asynchronous, bi-directional serial storage I/O bus 210, only one command (control information) or set of data can be transmitted at a time. For example, when write commands or data are being transmitted to the solid-state storage 110 on the storage I/O bus 210, read commands, data being read, erase commands, management commands, or other status commands cannot be transmitted on the storage I/O bus

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210. For example, when data is being read from the storage I/O bus 210, data cannot be written to the solid-state storage 110.

[0193] For example, during a write operation on bank-0 the bus arbiter 420 selects the bank-0 controller 418a which may have a write command or a series of write sub-commands on the top of its queue which cause the storage bus controller 348 to execute the following sequence. The bus arbiter 420 forwards the write command to the storage bus controller 348, which sets up a write command by selecting bank-0 214a through the storage control bus 212, sending a command to clear the input buffers of the solid-state storage elements 110 associated with the bank-0 214a, and sending a command to validate the status of the solid-state storage elements 216, 218, 220 associated with the bank-0 214a. The storage bus controller 348 then transmits a write subcommand on the storage I/O bus 210, which contains the physical addresses including the address of the logical erase block for each individual physical erase solid-stage storage element 216a-m as mapped from the logical erase block address. The storage bus controller 348 then muxes the write buffer 320 through the write sync buffer 308 to the storage I/O bus 210 through the MUX 350 and streams write data to the appropriate page. When the page is full, then storage bus controller 348 causes the solid-state storage elements 216a-m associated with the bank-0 214a to program the input buffer to the memory cells within the solid-state storage elements 216a-m. Finally, the storage bus controller 348 validates the status to ensure that page was correctly programmed.

[0194] A read operation is similar to the write example above. During a read operation, typically the bus arbiter 420, or other component of the bank interleave controller 344, receives data and corresponding status information and sends the data to the read data pipeline 108 while sending the status information on to the control and status registers 340. Typically, a read data command forwarded from bus arbiter 420 to the storage bus controller 348 will cause the MUX 350 to gate the read data on storage I/O bus 210 to the read data pipeline 108 and send status information to the appropriate control and status registers 340 through the status MUX 422.

[0195] The bus arbiter 420 coordinates the various command types and data access modes so that only an appropriate command type or corresponding data is on the bus at any given time. If the bus arbiter 420 has selected a write command, and write subcommands and corresponding data are being written to the solid-state storage 110, the bus arbiter 420 will not allow other command types on the storage I/O bus 210. Beneficially, the bus arbiter 420 uses

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timing information, such as predicted command execution times, along with status information received concerning bank 214 status to coordinate execution of the various commands on the bus with the goal of minimizing or eliminating idle time of the busses.

[0196] The master controller 224 through the bus arbiter 420 typically uses expected completion times of the commands stored in the queues 410, 412, 414, 416, along with status information, so that when the subcommands associated with a command are executing on one bank 214a, other subcommands of other commands are executing on other banks 214b-n. When one command is fully executed on a bank 214a, the bus arbiter 420 directs another command to the bank 214a. The bus arbiter 420 may also coordinate commands stored in the queues 410, 412, 414, 416 with other commands that are not stored in the queues 410, 412, 414, 416.

[0197] For example, an erase command may be sent out to erase a group of erase blocks within the solid-state storage 110. An erase command may take 10 to 1000 times more time to execute than a write or a read command or 10 to 100 times more time to execute than a program command. For N banks 214, the bank interleave controller 344 may split the erase command into N commands, each to erase a virtual erase block of a bank 214a. While bank-0 214a is executing an erase command, the bus arbiter 420 may select other commands for execution on the other banks 214b-n. The bus arbiter 420 may also work with other components, such as the storage bus controller 348, the master controller 224, etc., to coordinate command execution among the buses. Coordinating execution of commands using the bus arbiter 420, bank controllers 418, queues 410, 412, 414, 416, and agents 402, 404, 406, 408 of the bank interleave controller 344 can dramatically increase performance over other solid-state storage systems without a bank interleave function.

[0198] In one embodiment, the solid-state controller 104 includes one bank interleave controller 344 that serves all of the storage elements 216, 218, 220 of the solid-state storage 110. In another embodiment, the solid-state controller 104 includes a bank interleave controller 344 for each row of storage elements 216a-m, 218a-m, 220a-m. For example, one bank interleave controller 344 serves one row of storage elements SSS 0.0-SSS 0.N 216a, 218a, 220a, a second bank interleave controller 344 serves a second row of storage elements SSS 1.0-SSS 1.N 216b, 218b, 220b, etc.

[0199] FIG. 4B is a schematic block diagram illustrating an alternate embodiment 401 of a bank interleave controller 344 in the solid-state storage controller 104 in accordance with the

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present invention. The components 210, 212, 340, 346, 348, 350, 402-430 depicted in the embodiment shown in FIG. 4B are substantially similar to the bank interleave apparatus 400 described in relation to FIG. 4A except that each bank 214 includes a single queue 432a-n and the read commands, write commands, erase commands, management commands, etc. for a bank (e.g. Bank-0 214a) are directed to a single queue 432a for the bank 214a. The queues 432, in one embodiment, are FIFO. In another embodiment, the queues 432 can have commands pulled from the queues 432 in an order other than the order they were stored. In another alternate embodiment (not shown), the read agent 402, write agent 404, erase agent 406, and management agent 408 may be combined into a single agent assigning commands to the appropriate queues 432a-n.

[0200] In another alternate embodiment (not shown), commands are stored in a single queue where the commands may be pulled from the queue in an order other than how they are stored so that the bank interleave controller 344 can execute a command on one bank 214a while other commands are executing on the remaining banks 214b-n. One of skill in the art will easily recognize other queue configurations and types to enable execution of a command on one bank 214a while other commands are executing on other banks 214b-n.

[0201] Storage-Specific Components

[0202] The solid-state storage controller 104 includes a synchronization buffer 346 that buffers commands and status messages sent and received from the solid-state storage 110. The synchronization buffer 346 is located at the boundary between the solid-state storage clock domain and the local bus clock domain and provides buffering to account for the clock domain differences. The synchronization buffer 346, write synchronization buffer 308, and read synchronization buffer 328 may be independent or may act together to buffer data, commands, status messages, etc. In the preferred embodiment, the synchronization buffer 346 is located where there are the fewest number of signals crossing the clock domains. One skilled in the art will recognize that synchronization between clock domains may be arbitrarily moved to other locations within the solid-state storage device 102 in order to optimize some aspect of design implementation.

[0203] The solid-state storage controller 104 includes a storage bus controller 348 that interprets and translates commands for data sent to and read from the solid-state storage 110 and status messages received from the solid-state storage 110 based on the type of solid-state storage

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110. For example, the storage bus controller 348 may have different timing requirements for different types of storage, storage with different performance characteristics, storage from different manufacturers, etc. The storage bus controller 348 also sends control commands to the storage control bus 212.

[0204] In the preferred embodiment, the solid-state storage controller 104 includes a MUX 350 that comprises an array of multiplexers 350a-n where each multiplexer is dedicated to a row in the solid-state storage array 110. For example, multiplexer 350a is associated with solid-state storage elements 216a, 218a, 220a. MUX 350 routes the data from the write data pipeline 106 and commands from the storage bus controller 348 to the solid-state storage 110 via the storage I/O bus 210 and routes data and status messages from the solid-state storage 110 via the storage I/O bus 210 to the read data pipeline 108 and the control and status registers 340 through the storage bus controller 348, synchronization buffer 346, and bank interleave controller 344.

[0205] In the preferred embodiment, the solid-state storage controller 104 includes a MUX 350 for each row of solid-state storage elements (e.g. SSS 0.1 216a, SSS 0.2 218a, SSS 0.N 220a). A MUX 350 combines data from the write data pipeline 106 and commands sent to the solid-state storage 110 via the storage I/O bus 210 and separates data to be processed by the read data pipeline 108 from commands. Packets stored in the write buffer 320 are directed on busses out of the write buffer 320 through a write synchronization buffer 308 for each row of solid-state storage elements (SSS x.0 to SSS x.N 216, 218, 220) to the MUX 350 for each row of solid-state storage elements (SSS x.0 to SSS x.N 216, 218, 220). The commands and read data are received by the MUXes 350 from the storage I/O bus 210. The MUXes 350 also direct status messages to the storage bus controller 348.

[0206] The storage bus controller 348 includes a mapping module 424. The mapping module 424 maps a logical address of an erase block to one or more physical addresses of an erase block. For example, a solid-state storage 110 with an array of twenty storage elements (e.g. SSS 0.0 to SSS M.0 216) per block 214a may have a logical address for a particular erase block mapped to twenty physical addresses of the erase block, one physical address per storage element. Because the storage elements are accessed in parallel, erase blocks at the same position in each storage element in a row of storage elements 216a, 218a, 220a will share a physical address. To select one erase block (e.g. in storage element SSS 0.0 216a) instead of all erase

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blocks in the row (e.g. in storage elements SSS 0.0, 0.1, . . . 0.N 216a, 218a, 220a), one bank (in this case bank-0 214a) is selected.

[0207] This logical-to-physical mapping for erase blocks is beneficial because if one erase block becomes damaged or inaccessible, the mapping can be changed to map to another erase block. This mitigates the loss of losing an entire virtual erase block when one element's erase block is faulty. The remapping module 430 changes a mapping of a logical address of an erase block to one or more physical addresses of a virtual erase block (spread over the array of storage elements). For example, virtual erase block 1 may be mapped to erase block 1 of storage element SSS 0.0 216a, to erase block 1 of storage element SSS 1.0 216b, . . . , and to storage element M.0 216m, virtual erase block 2 may be mapped to erase block 2 of storage element SSS 0.1 218a, to erase block 2 of storage element SSS 1.1 218b, . . . , and to storage element M.1 218m, etc.

[0208] If erase block 1 of a storage element SSS0.0 216a is damaged, experiencing errors due to wear, etc., or cannot be used for some reason, the remapping module 430 could change the logical-to-physical mapping for the logical address that pointed to erase block 1 of virtual erase block 1. If a spare erase block (call it erase block 221) of storage element SSS 0.0 216a is available and currently not mapped, the remapping module 430 could change the mapping of virtual erase block 1 to point to erase block 221 of storage element SSS 0.0 216a, while continuing to point to erase block 1 of storage element SSS 1.0 216b, erase block 1 of storage element SSS 2.0 (not shown) . . . , and to storage element M.0 216m. The mapping module 424 or remapping module 430 could map erase blocks in a prescribed order (virtual erase block 1 to erase block 1 of the storage elements, virtual erase block 2 to erase block 2 of the storage elements, etc.) or may map erase blocks of the storage elements 216, 218, 220 in another order based on some other criteria.

[0209] In one embodiment, the erase blocks could be grouped by access time. Grouping by access time, meaning time to execute a command, such as programming (writing) data into pages of specific erase blocks, can level command completion so that a command executed across the erase blocks of a virtual erase block is not limited by the slowest erase block. In other embodiments, the erase blocks may be grouped by wear level, health, etc. One of skill in the art will recognize other factors to consider when mapping or remapping erase blocks.

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[0200] In one embodiment, the storage bus controller 348 includes a status capture module 426 that receives status messages from the solid-state storage 110 and sends the status messages to the status MUX 422. In another embodiment, when the solid-state storage 110 is flash memory, the storage bus controller 348 includes a NAND bus controller 428. The NAND bus controller 428 directs commands from the read and write data pipelines 106, 108 to the correct location in the solid-state storage 110, coordinates timing of command execution based on characteristics of the flash memory, etc. If the solid-state storage 110 is another solid-state storage type, the NAND bus controller 428 would be replaced by a bus controller specific to the storage type. One of skill in the art will recognize other functions of a NAND bus controller 428.

[0210] Flow Charts

[0211] FIG. 5 is a schematic flow chart diagram illustrating one embodiment of a method 500 for managing data in a solid-state storage device 102 using a data pipeline in accordance with the present invention. The method 500 begins 502 and the input buffer 306 receives 504 one or more data segments to be written to the solid-state storage 110. The one or more data segments typically include at least a portion of an object but may be an entire object. The packetizer 302 may create one or more object specific packets in conjunction with an object. The packetizer 302 adds a header to each packet which typically includes the length of the packet and a sequence number for the packet within the object. The packetizer 302 receives 504 the one or more data or metadata segments that were stored in the input buffer 306 and packetizes 506 the one or more data or metadata segments by creating one or more packets sized for the solid-state storage 110 where each packet includes one header and data from the one or more segments.

[0212] Typically, a first packet includes an object identifier that identifies the object for which the packet was created. A second packet may include a header with information used by the solid-state storage device 102 to associate the second packet to the object identified in the first packet and offset information locating the second packet within the object, and data. The solid-state storage device controller 202 manages the bank 214 and physical area to which the packets are streamed.

[0213] The ECC generator 304 receives a packet from the packetizer 302 and generates 508 ECC for the data packets. Typically, there is no fixed relationship between packets and ECC blocks. An ECC block may comprise one or more packets. A packet may comprise one or more

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ECC blocks. A packet may start and end anywhere within an ECC block. A packet may start anywhere in a first ECC block and end anywhere in a subsequent ECC block.

[0214] The write synchronization buffer 308 buffers 510 the packets as distributed within the corresponding ECC blocks prior to writing ECC blocks to the solid-state storage 110 and then the solid-state storage controller 104 writes 512 the data at an appropriate time considering clock domain differences, and the method 500 ends 514. The write synch buffer 308 is located at the boundary between a local clock domain and a solid-state storage 110 clock domain. Note that the method 500 describes receiving one or more data segments and writing one or more data packets for convenience, but typically a stream of data segments is received and a group. Typically a number of ECC blocks comprising a complete virtual page of solid-state storage 110 are written to the solid-state storage 110. Typically the packetizer 302 receives data segments of one size and generates packets of another size. This necessarily requires data or metadata segments or parts of data or metadata segments to be combined to form data packets to capture all of the data of the segments into packets.

[0215] FIG. 6 is a schematic flow chart diagram illustrating another embodiment of a method 600 for managing data in a solid-state storage device 102 using a data pipeline in accordance with the present invention. The method 600 begins 602 and the input buffer 306 receives 604 one or more data or metadata segments to be written to the solid-state storage 110. The packetizer 302 adds a header to each packet which typically includes the length of the packet within the object. The packetizer 302 receives 604 the one or more segments that were stored in the input buffer 306 and packetizes 606 the one or more segments by creating one or more packets sized for the solid-state storage 110 where each packet includes a header and data from the one or more segments.

[0216] The ECC generator 304 receives a packet from the packetizer 302 and generates 608 one or more ECC blocks for the packets. The write synchronization buffer 308 buffers 610 the packets as distributed within the corresponding ECC blocks prior to writing ECC blocks to the solid-state storage 110 and then the solid-state storage controller 104 writes 612 the data at an appropriate time considering clock domain differences. When data is requested from the solid-state storage 110, ECC blocks comprising one or more data packets are read into the read synchronization buffer 328 and buffered 614. The ECC blocks of the packet are received over

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the storage I/O bus 210. Since the storage I/O bus 210 is bi-directional, when data is read, write operations, command operations, etc. are halted.

[0217] The ECC correction module 322 receives the ECC blocks of the requested packets held in the read synchronization buffer 328 and corrects 616 errors within each ECC block as necessary. If the ECC correction module 322 determines that one or more errors exist in an ECC block and the errors are correctable using the ECC syndrom, the ECC correction module 322 corrects 616 the error in the ECC block. If the ECC correction module 322 determines that a detected error is not correctable using the ECC, the ECC correction module 322 sends an interrupt.

[0218] The depacketizer 324 receives 618 the requested packet after the ECC correction module 322 corrects any errors and depacketizes 618 the packets by checking and removing the packet header of each packet. The alignment module 326 receives packets after depacketizing, removes unwanted data, and re-formats 620 the data packets as data or metadata segments of an object in a form compatible with the device requesting the segment or object. The output buffer 330 receives requested packets after depacketizing and buffers 622 the packets prior to transmission to the requesting device 155, and the method 600 ends 624.

[0219] FIG. 7 is a schematic flow chart diagram illustrating an embodiment of a method 700 for managing data in a solid-state storage device 102 using a bank interleave in accordance with the present invention. The method 700 begins 702 and the bank interleave controller 344 directs 604 one or more commands to two or more queues 410, 412, 414, 416. Typically the agents 402, 404, 406, 408 direct 704 the commands to the queues 410, 412, 414, 416 by command type. Each set of queues 410, 412, 414, 416 includes a queue for each command type. The bank interleave controller 344 coordinates 706 among the banks 214 execution of the commands stored in the queues 410, 412, 414, 416 so that a command of a first type executes on one bank 214a while a command of a second type executes on a second bank 214b, and the method 700 ends 708.

[0220] Storage Space Recovery

[0221] FIG. 8 is a schematic block diagram illustrating one embodiment of an apparatus 800 for garbage collection in a solid-state storage device 102 in accordance with the present invention. The apparatus 800 includes a sequential storage module 802, a storage division selection module 804, a data recovery module 806, and a storage division recovery module 808,

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which are described below. In other embodiments, the apparatus 800 includes a garbage marking module 812 and an erase module 810.

[0222] The apparatus 800 includes a sequential storage module 802 that sequentially writes data packets in a page within a storage division. The packets are sequentially stored whether they are new packets or modified packets. Modified packets are in this embodiment are typically not written back to a location where they were previously stored. In one embodiment, the sequential storage module 802 writes a packet to a first location in a page of a storage division, then to the next location in the page, and to the next, and the next, until the page is filled. The sequential storage module 802 then starts to fill the next page in the storage division. This continues until the storage division is filled.

[0223] In a preferred embodiment, the sequential storage module 802 starts writing packets to storage write buffers in the storage elements (e.g. SSS 0.0 to SSS M.0 216) of a bank (bank-0 214a). When the storage write buffers are full, the solid-state storage controller 104 causes the data in the storage write buffers to be programmed into designated pages within the storage elements 216 of the bank 214a. Then another bank (e.g. bank-1 214b) is selected and the sequential storage module 802 starts writing packets to storage write buffers of the storage elements 218 of the bank 214b while the first bank-0 214a is programming the designated pages. When the storage write buffers of this bank 214b are full, the contents of the storage write buffers are programmed into another designated page in each storage element 218. This process is efficient because while one bank 214a is programming a page, storage write buffers of another bank 214b can be filling.

[0224] The storage division includes a portion of a solid-state storage 110 in a solid-state storage device 102. Typically the storage division is an erase block. For flash memory, an erase operation on an erase block writes ones to every bit in the erase block by charging each cell. This is a lengthy process compared to a program operation which starts with a location being all ones, and as data is written, some bits are changed to zero by discharging the cells written with a zero. However, where the solid-state storage 110 is not flash memory or has flash memory where an erase cycle takes a similar amount of time as other operations, such as a read or a program, the storage division may not be required to be erased.

[0225] As used herein, a storage division is equivalent in area to an erase block but may or may not be erased. Where erase block is used herein, an erase block may refer to a particular

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area of a designated size within a storage element (e.g. SSS 0.0 216a) and typically includes a certain quantity of pages. Where "erase block" is used in conjunction with flash memory, it is typically a storage division that is erased prior to being written. Where "erase block" is used with "solid-state storage," it may or may not be erased. As used herein, an erase block may include one erase block or a group of erase blocks with one erase block in each of a row of storage elements (e.g. SSS 0.0 to SSS M.0 216a-n), which may also be referred to herein as a virtual erase block. When referring to the logical construct associated with the virtual erase block, the erase blocks may be referred to herein as a logical erase block ("LEB").

[0226] Typically, the packets are sequentially stored by order of processing. In one embodiment, where a write data pipeline 106 is used, the sequential storage module 802 stores packets in the order that they come out of the write data pipeline 106. This order may be a result of data segments arriving from a requesting device 155 mixed with packets of valid data that are being read from another storage division as valid data is being recovered from a storage division during a recovery operation as explained below. Re-routing recovered, valid data packets to the write data pipeline 106 may include the garbage collector bypass 316 as described above in relation to the solid-state storage controller 104 of FIG. 3.

[0227] The apparatus 800 includes a storage division selection module 804 that selects a storage division for recovery. Selecting a storage division for recovery may be to reuse the storage division by the sequential storage module 802 for writing data, thus adding the recovered storage division to the storage pool, or to recover valid data from the storage division after determining that the storage division is failing, unreliable, should be refreshed, or other reason to take the storage division temporarily or permanently out of the storage pool. In another embodiment, the storage division selection module 804 selects a storage division for recovery by identifying a storage division or erase block with a high amount of invalid data.

[0228] In another embodiment, the storage division selection module 804 selects a storage division for recovery by identifying a storage division or erase block with a low amount of wear. For example, identifying a storage division or erase block with a low amount of wear may include identifying a storage division with a low amount of invalid data, a low number of erase cycles, low bit error rate, or low program count (low number of times a page of data in a buffer is written to a page in the storage division; program count may be measured from when the device was manufactured, from when the storage division was last erased, from other

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arbitrary events, and from combinations of these). The storage division selection module 804 may also use any combination of the above or other parameters to determine a storage division with a low amount of wear. Selecting a storage division for recovery by determining a storage division with a low amount of wear may be desirable to find storage divisions that are under used, may be recovered for wear leveling, etc.

[0229] In another embodiment, the storage division selection module 804 selects a storage division for recovery by identifying a storage division or erase block with a high amount of wear. For example, identifying a storage division or erase block with a high amount of wear may include identifying a storage division with a high number of erase cycles, high bit error rate, a storage division with a non-recoverable ECC block, or high program count. The storage division selection module 804 may also use any combination of the above or other parameters to determine a storage division with a high amount of wear. Selecting a storage division for recovery by determining a storage division with a high amount of wear may be desirable to find storage divisions that are over used, may be recovered by refreshing the storage division using an erase cycle, etc. or to retire the storage division from service as being unusable.

[0230] The apparatus 800 includes a data recovery module 806 that reads valid data packets from the storage division selected for recovery, queues the valid data packets with other data packets to be written sequentially by the sequential storage module 802, and updates an index with a new physical address of the valid data written by the sequential storage module 802. Typically, the index is the object index mapping data object identifiers of objects to physical addresses of where packets derived from the data object are stored in the solid-state storage 110.

[0231] In one embodiment the apparatus 800 includes a storage division recovery module 808 that prepares the storage division for use or reuse and marks the storage division as available to the sequential storage module 802 for sequentially writing data packets after the data recovery module 806 has completed copying valid data from the storage division. In another embodiment, the apparatus 800 includes a storage division recovery module 808 that marks the storage division selected for recovery as unavailable for storing data. Typically this is due to the storage division selection module 804 identifying a storage division or erase block with a high amount of wear such that the storage division or erase block is not in condition to be used for reliable data storage.

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[0232] In one embodiment, the apparatus 800 is in a solid-state storage device controller 202 of a solid-state storage device 102. In another embodiment, the apparatus 800 controls a solid-state storage device controller 202. In another embodiment, a portion of the apparatus 800 is in a solid-state storage device controller 202. In another embodiment, the object index updated by the data recovery module 806 is also located in the solid-state storage device controller 202.

[0233] In one embodiment, the storage division is an erase block and the apparatus 800 includes an erase module 810 that erases an erase block selected for recovery after the data recovery module 806 has copied valid data packets from the selected erase block and before the storage division recovery module 808 marks the erase block as available. For flash memory and other solid-state storage with an erase operation taking much longer than read or write operations, erasing a data block prior to making it available for writing new data is desirable for efficient operation. Where the solid-state storage 110 is arranged in banks 214, the erase operation by the erase module 810 may be executed on one bank while other banks are executing reads, writes, or other operations.

[0234] In one embodiment, the apparatus 800 includes a garbage marking module 812 that identifies a data packet in a storage division as invalid in response to an operation indicating that the data packet is no longer valid. For example, if a data packet is deleted, the garbage marking module 812 may identify the data packet as invalid. A read-modify-write operation is another way for a data packet to be identified as invalid. In one embodiment, the garbage marking module 812 may identify the data packet as invalid by updating an index. In another embodiment, the garbage marking module 812 may identify the data packet as invalid by storing another data packet that indicates that the invalid data packet has been deleted. This is advantageous because storing, in the solid-state storage 110, information that the data packet has been deleted allows the object index reconstruction module 272 or similar module to reconstruct the object index with an entry indicating that the invalid data packet has been deleted.

[0235] In one embodiment, the apparatus 800 may be utilized to fill the remainder of a virtual page of data following a flush command in order to improve overall performance, where the flush command halts data flowing into the write pipeline 106 until the write pipeline 106 empties and all packets have been permanently written into non-volatile solid-state storage 110. This has the benefit of reducing the amount of garbage collection required, the amount of time used to erase storage divisions, and the amount of time required to program virtual pages. For

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example, a flush command may be received when only one small packet is prepared for writing into the virtual page of the solid-state storage 110. Programming this nearly empty virtual page might result in a need to immediately recover the wasted space, causing the valid data within the storage division to be unnecessarily garbage collected and the storage division erased, recovered and returned to the pool of available space for writing by the sequential storage module 802. Marking the data packet as invalid rather than actually erasing an invalid data packet is efficient because, as mentioned above, for flash memory and other similar storage an erase operation takes a significant amount of time. Allowing a garbage collection system, as described in the apparatus 800, to operate autonomously within the solid-state storage 110 provides a way to separate erase operations from reads, writes, and other faster operations so that the solid-state storage device 102 can operate much faster than many other solid-state storage systems or data storage devices.

[0236] FIG. 9 is a schematic flow chart diagram illustrating an embodiment of a method 900 for storage recovery in accordance with the present invention. The method 900 begins 902 and the sequential storage module 802 sequentially writes 904 data packets in a storage division. The storage division is a portion of a solid-state storage 110 in a solid-state storage device 102. Typically a storage division is an erase block. The data packets are derived from an object and the data packets are sequentially stored by order of processing.

[0237] The storage division selection module 804 selects 906 a storage division for recovery and the data recovery module 806 reads 908 valid data packets from the storage division selected for recovery. Typically valid data packets are data packets that have not been marked for erasure or deletion or some other invalid data marking and are considered valid or "good" data. The data recovery module 806 queues 910 the valid data packets with other data packets scheduled to be written sequentially by the sequential storage module 802. The data recovery module 806 updates 912 an index with a new physical address of the valid data written by the sequential storage module 802. The index includes a mapping of physical addresses of data packets to object identifiers. The data packets are those stored in stored in the solid-state storage 110 and the object identifiers correspond to the data packets.

[0238] After the data recovery module 806 completes copying valid data from the storage division, the storage division recovery module 808 marks 914 the storage division selected for

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recovery as available to the sequential storage module 802 for sequentially writing data packets and the method 900 ends 916.

[0239] Empty Data Segment Directive

[0240] Typically, when data is no longer useful it may be erased. In many file systems, an erase command deletes a directory entry in the file system while leaving the data in place in the storage device containing the data. Typically, a data storage device is not involved in this type of erase operation. Another method of erasing data is to write zeros, ones, or some other null data character to the data storage device to actually replace the erased file. However, this is inefficient because valuable bandwidth is used while transmitting the data is being overwritten. In addition, space in the storage device is taken up by the data used to overwrite invalid data.

[0241] In some storage devices, like the solid-state storage device 102 described herein, updating previously stored data does not overwrite existing data. Attempting to overwrite data with a string of ones or a string of zeros on such a device takes up valuable space without fulfilling the desired intent of overwriting the existing data. For these devices, such as solid-state storage devices 102, a client 114 typically does not have an ability to overwrite data to erase it.

[0242] When receiving a string of repeated characters or character strings, the received data is highly compressible, but typically compression is done by a file system prior to transmission to a storage device. A typical storage device cannot distinguish between compressed data and uncompressed data. The storage device may also receive a command to read the erased file so the storage device may transmit a stream of zeros, ones, or a null character to the requesting device. Again, bandwidth is required to transmit data representing the erased file.

[0243] From the foregoing discussion, it should be apparent that a need exists for an apparatus, system, and method for a storage device to receive a directive that data is to be erased so that the storage device can store a data segment token that represents an empty data segment or data with repeated characters or character strings. The apparatus, system, and method may also erase the existing data so that the resulting used storage space comprises the small data segment token. An apparatus, system, and method are presented that overcome some or all of the shortcomings of the prior art.

[0244] FIG. 10 is a schematic block diagram illustrating one embodiment of a system 1000 with an apparatus for generating a token directive in accordance with the present invention.

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The apparatus includes a token directive generation module 1002, a token directive transmission module 1004, a read receiver module 1006, a read request transmission module 1008, a read token directive receiver module 1010, a requesting client response module 1012, and data segment regeneration module 1014, which are described below. In one embodiment, the apparatus is in a server 112 connected to a storage device 150 with a storage controller 152 and a data storage device 154, which are substantially similar to those described above.

[0245] In one embodiment, the apparatus includes a token directive generation module 1002 that generates a storage request with a token directive. The token directive includes a request to store a data segment token on the storage device 150. The token directive is intended to be substituted for a series of repeated, identical characters or a series of repeated, identical character strings that would be sent to the storage device 150 and stored as a data segment if the data segment token was not sent in its place. In one embodiment, the series of repeated, identical characters indicate that the data segment is empty. For example, the series of repeated, identical characters may be zeros or ones and a data segment filled with zeros or ones may be interpreted as empty.

[0246] The token directive includes at least a data segment identifier and a data segment length. The data segment identifier is typically an object ID, file name, or other identifier known to a file system, application, server 112, etc. seeking to store the repeated, identical characters or character string on the storage device. The data segment length is typically the storage space required by the series of repeated, identical characters or character strings. The data segment token and the token directive typically do not include data of the data segment, such as the series of repeated, identical characters.

[0247] The token directive may, however, include other pertinent information for forming the data segment token, such as at least one instance of the repeated, identical character or character string. The token directive may also include metadata, such as a data segment location, an address from a file system, location on a data storage device corresponding to the data segment, etc. One of skill in the art will recognize other information that may be included with a token directive. In one embodiment, the token directive generation module 1002 generates a data segment token along with the token directive.

[0248] In one embodiment, the token directive generation module 1002 generates both a token directive and a secure erase command in response to a request to overwrite existing data on

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the storage device 150. The existing data includes data identified on the storage device 150 with the same data segment identifier as the data segment identifier in the token directive. Typically, a request to overwrite data is sent where it is not sufficient to merely mark data as invalid or garbage, delete a pointer to the data, or other typical delete operation, but where the data is required to be overwritten in such a way that that the data is not recoverable. For example, the request to overwrite the data may be required where data is considered sensitive information and must be destroyed for security reasons.

[0249] The secure erase command directs the storage device 150 to overwrite existing data so that the existing data is non-recoverable. The storage device 150 then creates the data segment token as well as overwrites, recovers, erases, etc. the existing data. As a result, the existing data is non-recoverable and the data segment token is stored on the storage device 150, which typically takes much less storage space than the existing data.

[0250] In a further embodiment, the apparatus includes an erase confirmation module 1016 that receives a confirmation that the existing data on the storage device 150 has been overwritten with characters so that the existing data is non-recoverable. The confirmation may be forwarded to a requesting device or client 114 and may be used to verify that the existing data has been put in a condition where it is non-recoverable. In other embodiments, the secure erase command may direct the storage device 150 to overwrite the existing data with a specific character or character string or the execute command may be executed multiple times. One of skill in the art will recognize other ways to configure one or more secure erase commands to ensure the existing data is non-recoverable.

[0251] Data may be encrypted and then stored on a storage device 150 where encryption is accomplished using an encryption key received by the storage device 150 in conjunction with storing the data. Where the existing data is encrypted with this received encryption key before being stored, in another embodiment the token directive generation module 1002 generates an encryption erase command along with generating a token directive in response to receiving a request to overwrite the existing data. The encryption erase command erases the encryption key used to store the existing data so that the encryption key is non-recoverable.

[0252] In one embodiment, erasing the encryption key includes erasing the encryption key from the requesting device. In another embodiment, erasing the encryption key includes erasing the encryption key from a server, key vault, or other location where the encryption key is

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stored. Erasing the encryption key may include replacing the encryption key with other data or with a series of characters so that the encryption key cannot be recovered in any way. Erasing the encryption key typically makes the existing data on the storage device 150 non-recoverable where an encryption routine was used to encrypt the existing data that is robust enough to thwart attempts to decrypt the existing data. The request to overwrite the existing data could be a secure erase directive where the data is overwritten for security reasons, a request to overwrite data to erase the data, a request that seeks to replace the existing data with the repeated, identical characters or character strings, or the like. In one embodiment, a secure erase directive causes devices to both securely erase the encryption key and securely erase the existing data. In one embodiment, erasure of the encryption key may allow secure erasure of the data on the storage device 150 to be postponed until a garbage collection process erases the data as part of a storage space recovery process. One of skill in the art will recognize other ways to erase an encryption key and other ways to receive a request to overwrite existing data.

[0253] In one embodiment, a token directive includes the data segment token and the token directive transmission module 1004 transmits the data segment token with the token directive. In another embodiment, a token directive does not include the data segment token and includes a command for the storage device 150 to generate the data segment token. In this embodiment, the token directive transmission module 1004 transmits the token directive with the command to generate a data segment token, but does not transmit a data segment token.

[0254] The apparatus includes a token directive transmission module 1004 that transmits the token directive to the storage device 150. Typically, the token directive transmission module 1004 transmits the token directive as part of a storage request. The storage request may be in the form of an object request, a data request, or other form known to those of skill in the art. Where the token directive generation module 1002 generates a secure erase directive, the token directive transmission module 1004 transmits the secure erase directive to the storage device 150. Where the token directive generation module 1002 generates an erase encryption key command, the erase encryption key command is transmitted, where necessary, to another device to execute the command.

[0255] In one embodiment, the token directive transmission module 1004 transmits a token directive without a data segment token. In this embodiment, the token directive includes instructions and information for the storage device 150 to create a data segment token. In another

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embodiment, the token directive transmission module 1004 transmits a token directive that includes a data segment token. In this embodiment, the storage device 150 is capable of recognizing that the data segment token received with the token directive represents a data segment and takes appropriate action to store the data segment token such that the data segment token represents the data segment rather than merely storing the data segment token as ordinary data.

[0256] The apparatus, in a particular embodiment, includes a read receiver module 1006 that receives a storage request to read the data segment from the storage device 150 and a read request transmission module 1008 that transmits the storage request to the storage device 150. Typically, the storage request is received from a requesting client 114, such as an external client 114, a client 114 internal to the server 112, such as an application or file server running on the server 112, etc. One of skill in the art will recognize other devices and software functioning as a requesting client 114 from which the read receiver module 1006 can receive a storage request.

[0257] The storage request includes a request to read the data segment corresponding to the data segment token requested to be stored in the token directive transmitted to the storage device 150 by the token directive transmission module 1004. The requesting client 114, in one embodiment, is unaware that the data segment has been stored in the form of a data segment token. In another embodiment, the requesting device is aware that the data segment has been stored as a data segment token but is unaware of the information stored in the data segment token.

[0258] The apparatus, in the particular embodiment, also includes a read token directive receiver module 1010 that receives a message corresponding to the requested data segment token from the storage device 150, where the message includes at least the data segment identifier and the data segment length. The message typically does not include data of the data segment. The message may also include other information stored in the data segment token, such as a data segment location or the repeated, identical character or character string. In the particular embodiment, the apparatus includes a requesting client response module 1012 that transmits a response to the requesting client 113 formulated from the message received from the storage device 150.

[0259] In one embodiment, read token directive receiver module 1010 also receives in the message a confirmation that existing data has been overwritten with characters such that the

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existing data is non-recoverable, where the existing data has been previously stored on the storage device 150 and referenced with the same data segment identifier from the data segment token received in the message. The confirmation may also be received from the storage device 150 independently from any storage request to read the data segment.

[0260] In another embodiment, where the requesting client 114 requires the data segment, the apparatus includes a data segment regeneration module 1014 that reconstitutes data of the data segment using information contained in the message. In this case, the response sent to the requesting client includes the reconstituted data segment. In another embodiment, the response sent to the requesting client includes information contained in the message received from the storage device 150. The requesting client 114 may then reconstitute the data segment or use the information in some other way. In another embodiment, the message includes the data segment token. The data segment token may be used by the data segment regeneration module 1014 to reconstitute the data segment before forwarding to the requesting client 114 or the requesting client response module 1012 may simply forward the data segment token.

[0261] In one embodiment, the storage request with the token directive also includes a request to reserve storage space on the storage device 150, where the requested reserved storage space is an amount of storage space that is about the same to the data segment length. In another embodiment, the request to reserve storage space is for an amount of storage space different than the data segment length. For example, if the storage device 150 is a solid-state storage device 102, the solid-state storage device 102 may be connected to a hard drive or other long-term, inexpensive storage while the solid-state storage 110 is configured as cache for the long-term storage. The request to reserve storage may cause the solid-state storage device 102 to flush a portion of the cache to the long-term storage in preparation for writing data to the solid-state storage device 102. One of skill in the art will recognize other situations were a request to reserve storage space is desired.

[0262] In one embodiment, an apparatus may be provided with a read receiver module 1006, a read request transmission module 1008, a read token directive receiver module 1010, and a requesting client response module 1012, which are substantially similar to those described above. In the embodiment, the modules 1006-1012 may be independent from an apparatus including a token directive generation module 1002 or a token directive transmission module

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1004. In one embodiment, the apparatus includes a data segment regeneration module 1014, which is substantially similar to the data segment regeneration module 1014 described above.

[0263] FIG. 11 is a schematic flow chart diagram illustrating an embodiment of a method 1100 for generating and transmitting a token directive in accordance with the present invention. The method 1100 begins 1102 and the token directive generation module 1002 generates 1104 a storage request with a token directive, where the token directive includes a request to store a data segment token on the storage device 150. The token directive transmission module 1004 transmits 1106 the token directive to the storage device 150 and the method 1100 ends 1108. In one embodiment, the storage request includes a token directive to store the data segment token where the storage request is essentially free from data of the data segment. In another embodiment, storage request includes data from the data segment. In a preferred embodiment, a software application creates a storage request using the token directive so as to avoid the creation of the data segment. In another embodiment, a software application requests the creation of the token directive.

[0264] FIG. 12 is a schematic flow chart diagram illustrating an embodiment of a method 1200 for reading a data segment token in accordance with the present invention. The method 1200 begins 1202 and the read receiver module 1006 receives 1204 a storage request to read a data segment from a storage device 150 from a requesting client 114. The read request transmission module 1008 transmits 1206 the storage request to the storage device 150.

[0265] The read token directive receiver module 1010 receives 1208 a message corresponding to the requested data segment token from the storage device 150, where the message includes at least the data segment identifier and the data segment length. The message is substantially free from data of the data segment. The requesting client response module 1012 transmits 1210 a response to the requesting client formulated from the message received from the storage device 150 and the method 1200 ends 1212.

[0266] FIG. 13 is a schematic block diagram illustrating one embodiment of a system 1300 with an apparatus for managing a data segment token in accordance with the present invention. The system 1300 includes an apparatus with a write request receiver module 1302 and a data segment token storage module 1304, and in various embodiments a token generation module 1306, a read request receiver module 1308, a read data segment token module 1310, a read request response module 1312 with a transmit data segment token module 1314 and a

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transmit data segment module 1316, a reconstitute data segment module 1318, a secure erase module 1320 with an erase confirmation module 1322, and a storage space reservation module 1324, which are described below. The system 1300 includes a storage device 150 with a storage controller 152 and a data storage device 154, which are substantially similar to those described above. The system 1300 includes a requesting device 1326, which is described below, in communication with the storage device 150.

[0267] In the depicted embodiment, the modules 1302-1324 are included in the storage device 150 or storage controller 152. In another embodiment, at least a portion of one or more of the modules 1302-1324 is located outside the storage device 150. In a further embodiment, the requesting device 1326 includes a portion of the modules 1302-1324 in the form of drivers, software, or other function of one or more of the modules 1302-1324. For example, a token generation module 1306 and a reconstitute data segment module 1318 are shown in the requesting device 1326. One of skill in the art will recognize other ways to distribute and implement the functionality of the modules 1302-1324.

[0268] The apparatus includes a write request receiver module 1302 that receives a storage request from the requesting device 1326, where the storage request includes a request to store a data segment in the storage device 150. The data segment includes a series of repeated, identical characters or character strings. Typically, the series of repeated, identical characters signify that the data segment is empty. This is especially true when the series of repeated, identical characters are ones or zeros. The apparatus includes a data segment token storage module 1304 that stores a data segment token in the storage device 150. The data segment token includes at least a data segment identifier and a data segment length. The data segment token is substantially free of the actual data from the data segment.

[0269] The data segment token may be stored in many forms. In one embodiment, includes an entry in an index, where the index corresponds to information and data stored on the storage device 150. For example, the index may be an object index as described above in relation to the apparatus 200 depicted in FIG. 2. The index may also be file system index, a block storage index, or other index known to those of skill in the art. In another embodiment, the data segment token includes or is in the form of metadata stored on the storage device 150. In another embodiment, the data segment token is stored as metadata on the storage device 150 and includes

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an entry in an index. One of skill in the art will recognize other ways to storage a data segment token.

[0270] In one embodiment, the storage request includes a token directive to store the data segment token where the storage request is essentially free from data of the data segment. The token directive may include the data segment token or a command to generate a data segment token. Where the token directive does not include the data segment token, the data segment token storage module 1304 generates the data segment token from information in the token directive. If the token directive includes the data segment token, the data segment token storage module 1304 recognizes the data segment token as a data structure representing the data segment identified by the data segment identifier in the token directive and stores the data segment token appropriately.

[0271] Typically, where the data segment token storage module 1304 recognizes a data segment token, the data segment token is differentiated in some way from other data stored on the storage device 150. For example, a requesting device 1326 may merely compress data and send a compressed object, file, or data segment so that the storage device 150 does not distinguish the compressed data segment from other data received by way of other storage requests.

[0272] Where the data segment token storage module 1304 recognizes that a received data segment token is a data segment token, the data segment token storage module 1304 may store the data segment token in such a way that when read, it may appear as a data segment rather than the data segment token. One of skill in the art will recognize other ways that the data segment token storage module 1304 may store a data segment token after recognizing that a received data segment token is a data segment token rather than a data segment.

[0273] In another embodiment, storage request includes data from the data segment. In this embodiment, the apparatus includes a token generation module 1306 that generates a data segment token from the data segment, where the data segment token is created in response to the storage request to store the data segment. In a further embodiment, the token generation module 1306 resides in the requesting device 1326, possibly in the form of a driver.

[0274] In one embodiment, the apparatus includes a secure erase module 1320 that overwrites existing data with characters such that the existing data is non-recoverable, where the existing data includes data of a data segment previously stored on the storage device 150

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identified with the same data segment identifier as the data segment identified in the storage request. In this embodiment, a data segment token is stored with the data segment identifier and data segment length and existing data identified by the same data segment identifier stored in the data segment token is erased by overwriting the existing data. Typically the existing characters are overwritten by zeros, ones, or some other character string so that the existing data is destroyed and is non-recoverable.

[0275] In a further embodiment, the secure erase module 1320 also includes an erase confirmation module 1322 that transmits a message indicating that the existing data has been overwritten. Typically the message is sent to the requesting device 1326. The erase confirmation message is transmitted after the secure erase module 1320 has overwritten the existing data. The message may be transmitted in the same transaction as the storage request or in a different transaction.

[0276] In another embodiment, the secure erase module 1320 overwrites the existing data during a storage space recovery operation. For example, if the storage device 150 is a solid-state storage device 102, as described above, the storage space recovery operation may be related to the garbage collection describe in relation to the apparatus 800 depicted in FIG. 8. However, a storage space recovery operation involving a request to overwrite the existing data would typically be expedited so that the storage location where the existing data is stored is necessarily recovered prior to any confirmation message is sent by the erase confirmation module 1322. In one embodiment, the existing data is marked or otherwise identified to indicate that a secure erase has been requested. The confirmation message would typically not be sent until the existing data marked for erasure has been overwritten and made non-recoverable. In another embodiment, the secure erase module 1320 merely marks the existing data as invalid for later storage space recovery. In another embodiment, the secure erase updates an index to indicate that the existing data is invalid and prevents access to this data until the data is overwritten during later storage space recovery.

[0277] In one embodiment, the secure erase module 1320 overwrites the existing data each time a data segment token is stored. In another embodiment, the storage request specifically includes a request to overwrite the existing data and the secure erase module 1320 overwrites the existing data in response to the request to overwrite the existing data. In another embodiment, the

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secure erase module 1320 stores metadata information regarding confirmation that the existing data has been erased so that subsequent reads can indicate the erasure.

[0278] In other embodiments where a secure erase is not received, the existing data is deleted. In one embodiment, deleting the data includes deleting an index entry, address, etc. In a preferred embodiment, the when a data segment token is stored, the corresponding existing data is marked as invalid or otherwise ready for storage recovery. The data may be later recovered in a storage recovery operation, garbage collection operation, etc.

[0279] In a particular embodiment, the apparatus includes a read request receiver module 1308 that receives a storage request to read the data segment, a read data segment token module 1310 that reads the data segment token corresponding to the data segment requested by the storage request, and a read request response module 1312 that transmits a response to the requesting device 1326. The response is generated using the data segment token corresponding to the requested data segment.

[0280] The storage request to read the data segment, in one embodiment, is associated with the storage request and serves to confirm that the storage request has been successful. In another embodiment, the request to read the data segment is independent from the storage request and may be initiated by the requesting device 1326 that made the storage request or another separate requesting device 1326.

[0281] In one embodiment, where the requesting device 1326 is capable of receiving information from the data segment token in place of actual data, the read request response module 1312 includes a transmit data segment token module 1314 that transmits in the response a message to the requesting device 1326. The message includes at least the data segment identifier and the data segment length, but may also include a data segment location, at least one instance of the repeated, identical character or character string, or other pertinent information. Typically, the message does not include the actual data of the data segment, other than what is included in the data segment token.

[0282] In another embodiment, where the requesting device 1326 is expecting to receive a data segment, the apparatus includes a reconstitute data segment module 1318 that reconstitutes data of the data segment using the data segment token. The read request response module 1312 also includes a transmit data segment module 1316 that transmits the reconstituted requested data segment to the requesting device 1326. In another embodiment, the reconstitute data segment

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module 1318 resides at the requesting device 1326, possibly as in the form of a driver, and the transmit data segment token module 1314 transmits the message with the data segment token information to the requesting device 1326. The reconstitute data segment module 1318 at the requesting device 1326 reconstitutes the requested data segment from the message.

[0283] In one embodiment, the system 1300 includes a separate apparatus that includes a read request receiver module 1308, a read data segment token module 1310, a read request response module 1312, which are substantially similar to those described above. The apparatus may be independent from the apparatus including the write request receiver module 1302 and the data segment token storage module 1304. In one embodiment, the read request response module 1312 includes a transmit data segment token module 1314 and/or a transmit data segment module 1316, and the apparatus may include a reconstitute data segment module 1318, where the modules 1314, 1316, 1318 are substantially similar to those described above.

[0284] FIG. 14 is a schematic flow chart diagram illustrating an embodiment of a method 1400 for storing a data segment token in accordance with the present invention. The method 1400 begins 1402 and the write request receiver module 1302 receives 1404 a storage request from the requesting device 1326, where the storage request includes a request to store a data segment in the storage device 150. The data segment includes a series of repeated, identical characters or character strings. The data segment token storage module 1304 stores 1406 a data segment token in the storage device 150 and the method 1400 ends 1408. The data segment token includes at least a data segment identifier and a data segment length and the data segment token does not include data from the data segment for the most part.

[0285] FIG. 15 is a schematic flow chart diagram illustrating an embodiment of a method 1500 for reading a data segment token in accordance with the present invention. The method 1500 begins 1502 and the read request receiver module 1308 receives 1504 a storage request to read a data segment from the storage device 150. The data segment is represented on the storage device 150 by a data segment token and the data segment includes a series of repeated, identical characters or character strings. The data segment token includes at least a data segment identifier and a data segment length and the data segment token does not include data from the data segment. The read data segment token module 1310 reads 1506 the data segment token corresponding to the data segment requested in the storage request, the read request response module 1312 transmits 1508 a response to the requesting storage device 150 and the method

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Page 82 of 382

1500 ends 1510. The response is generated using the data segment token corresponds to the requested data segment.

[0286] The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

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Silicon Motion v. UTL - IPR2024-00199
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WHAT IS CLAIMED IS:

1. A method for managing data in a block-based NAND flash storage system, the method comprising:

a host processor,

deleting a file, and

issuing an empty-block directive including a block identifier; and a NAND controller,

receiving the empty-block directive, and

updating a table mapping logical identifiers to physical NAND flash storage locations, wherein the table is updated to indicate that data stored in one or more physical NAND flash storage locations associated with the block identifier do not need to be preserved.

2. The method of claim 1, wherein responsive to receiving a read command including the block identifier from the host processor, the NAND controller returns a data string comprising data bits with a predetermined logic level.

3. The method of claim 2, wherein the predetermined logic level is zero.

4. The method of claim 1, wherein at least a part of the table is maintained in volatile memory.

5. The method of claim 1, wherein the empty-block directive issued by the host processor further comprises an indication that data stored in the one or more physical NAND flash storage locations associated with the block identifier should be overwritten.

6. The method of claim 1, wherein the empty-block directive is part of a block storage protocol.

7. The method of claim 1, wherein the empty-block directive is issued at an application programming interface of the host processor.

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Silicon Motion v. UTL - IPR2024-00199
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8. The method of claim 1, wherein the empty-block directive is issued by a file system of the host processor.

9. The method of claim 1, wherein the empty-block directive is issued by a storage client of the host processor.

10. The method of claim 1, further comprising the NAND controller performing garbage collection in the NAND flash storage system.

11. The method of claim 9, wherein performing garbage collection comprises the NAND controller:

copying a block containing data that should be preserved from an erase block comprising blocks containing data that does not need to be preserved; and

erasing the erase block.

12. The method of claim 10, further comprising the NAND controller writing data to the erased erase block.

13. The method of claim 1, wherein the NAND flash storage system is an append-only storage system.

14. The method of claim 1, wherein each of the one or more physical NAND flash storage locations are smaller than a NAND flash erase block.

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15. A method for managing data in a NAND flash storage system, the method comprising:

receiving an empty-block directive at a storage controller, the empty block directive including a logical identifier associated with a physical storage location comprising data deleted by a host; and

returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty block directive.

16. The method of claim 14, wherein the predetermined logic level is zero.

17. The method of claim 14, further comprising:

determining that the empty-block directive further includes an indication that data associated with the logical identifier should be overwritten; and

overwriting the data associated with the logical identifier.

18. The method of claim 14, wherein the empty-block directive is part of a block storage protocol.

19. The method of claim 14, wherein the empty-block directive is received through an application programming interface.

20. The method of claim 14, wherein the empty-block directive is received from a file system.

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Silicon Motion v. UTL - IPR2024-00199
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ABSTRACT

An apparatus, system, and method are disclosed for managing a non-volatile storage medium. A storage controller receives a message that identifies data that no longer needs to be retained on the non-volatile storage medium. The data may be identified using a logical identifier. The message may comprise a hint, directive, or other indication that the data has been erased and/or deleted. In response to the message, the storage controller records an indication that the contents of a physical storage location and/or physical address associated with the logical identifier do not need to be preserved on the non-volatile storage medium.

Silicon Motion - Exhibit 1014
Silicon Motion v. UTL - IPR2024-00199
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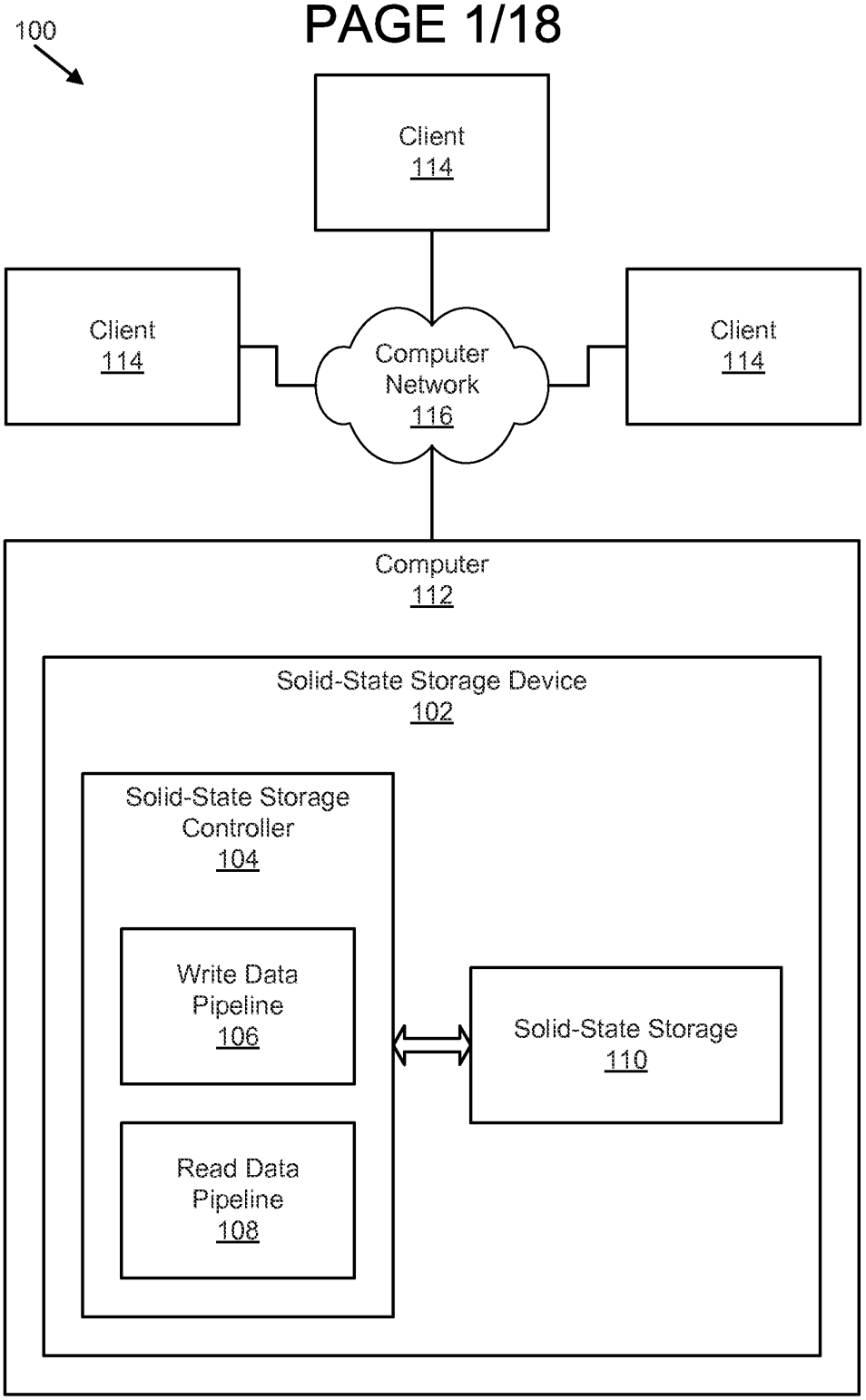


FIG. 1A

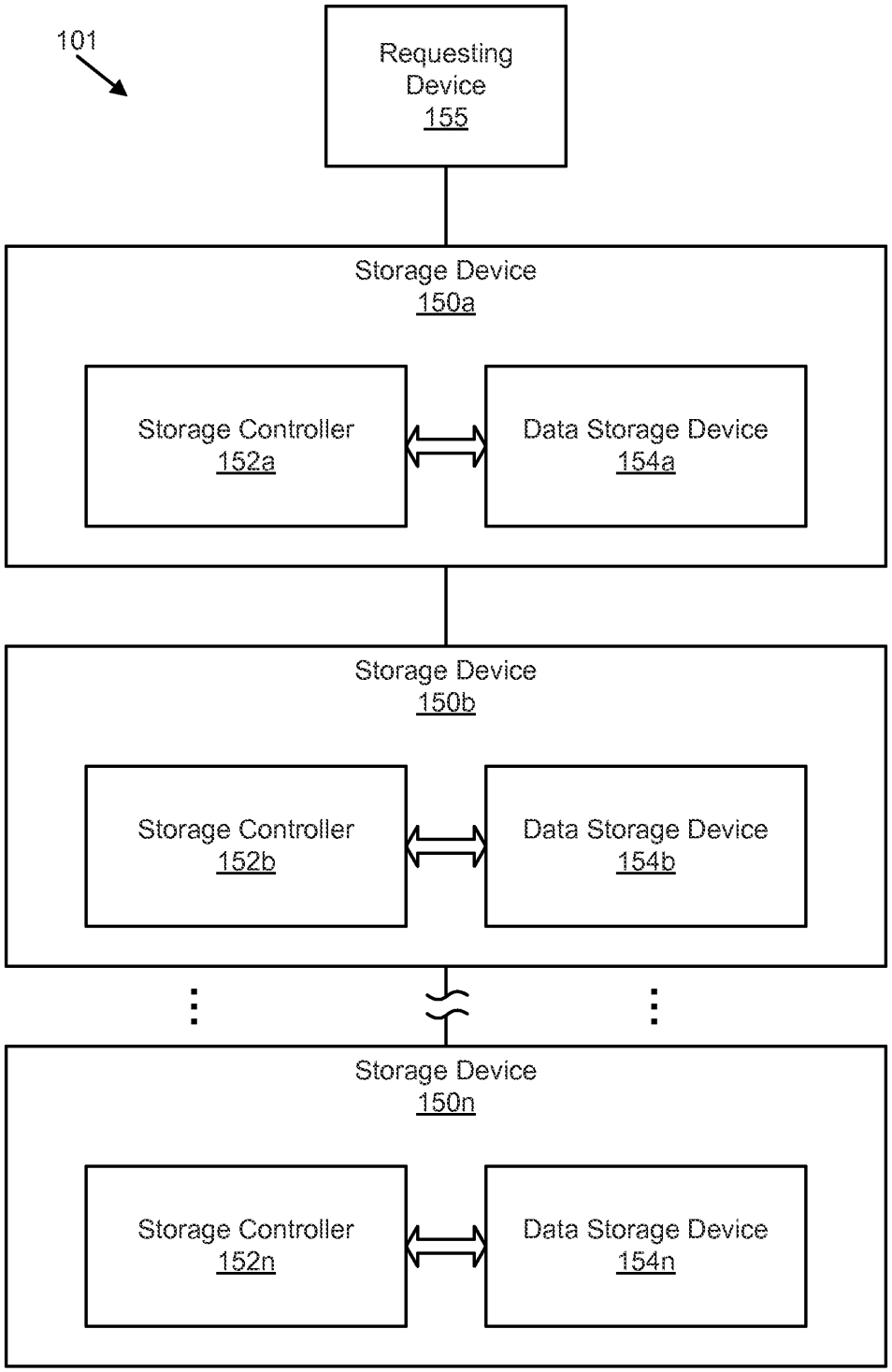

101
Requesting Device 155
Storage Device 150a
Storage Controller 152a
Data Storage Device 154a
Storage Device 150b
Storage Controller 152b
Data Storage Device 154b
Storage Device 150n
Storage Controller 152n
Data Storage Device 154n

FIG. 1B

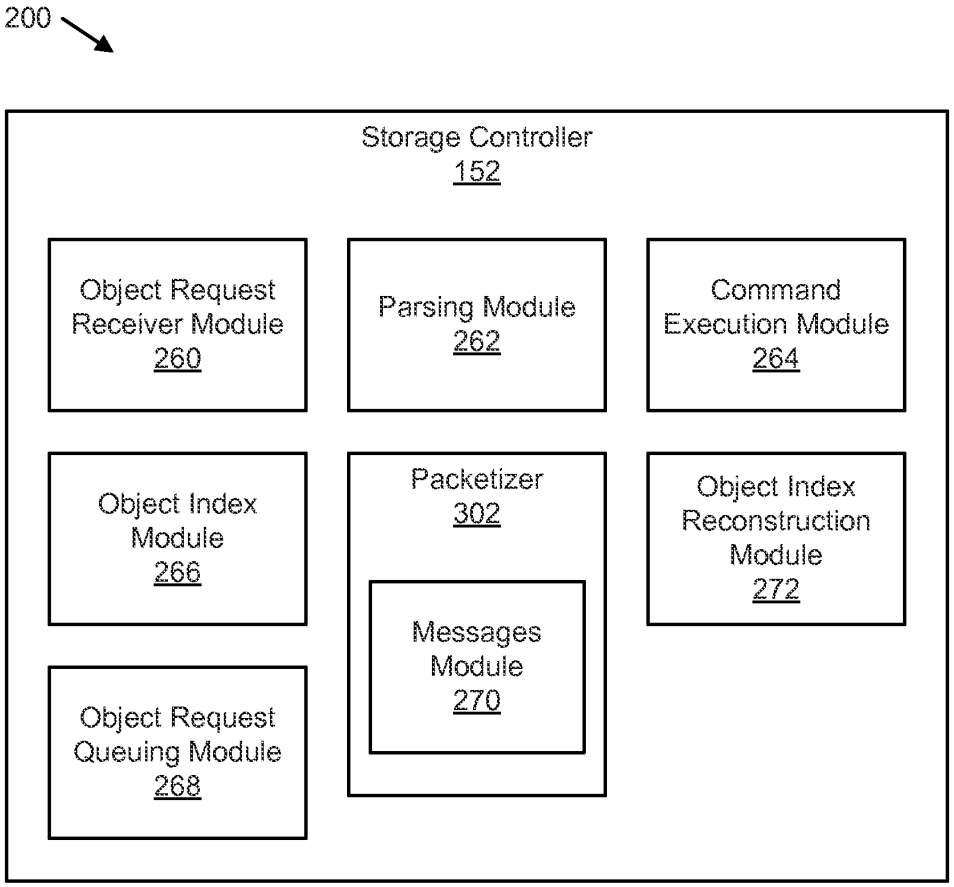

200
Storage Controller
152
Object Request Receiver Module
260
Parsing Module
262
Command Execution Module
264
Object Index Module
266
Packetizer
302
Messages Module
270
Object Index Reconstruction Module
272
Object Request Queuing Module
268

FIG. 2A

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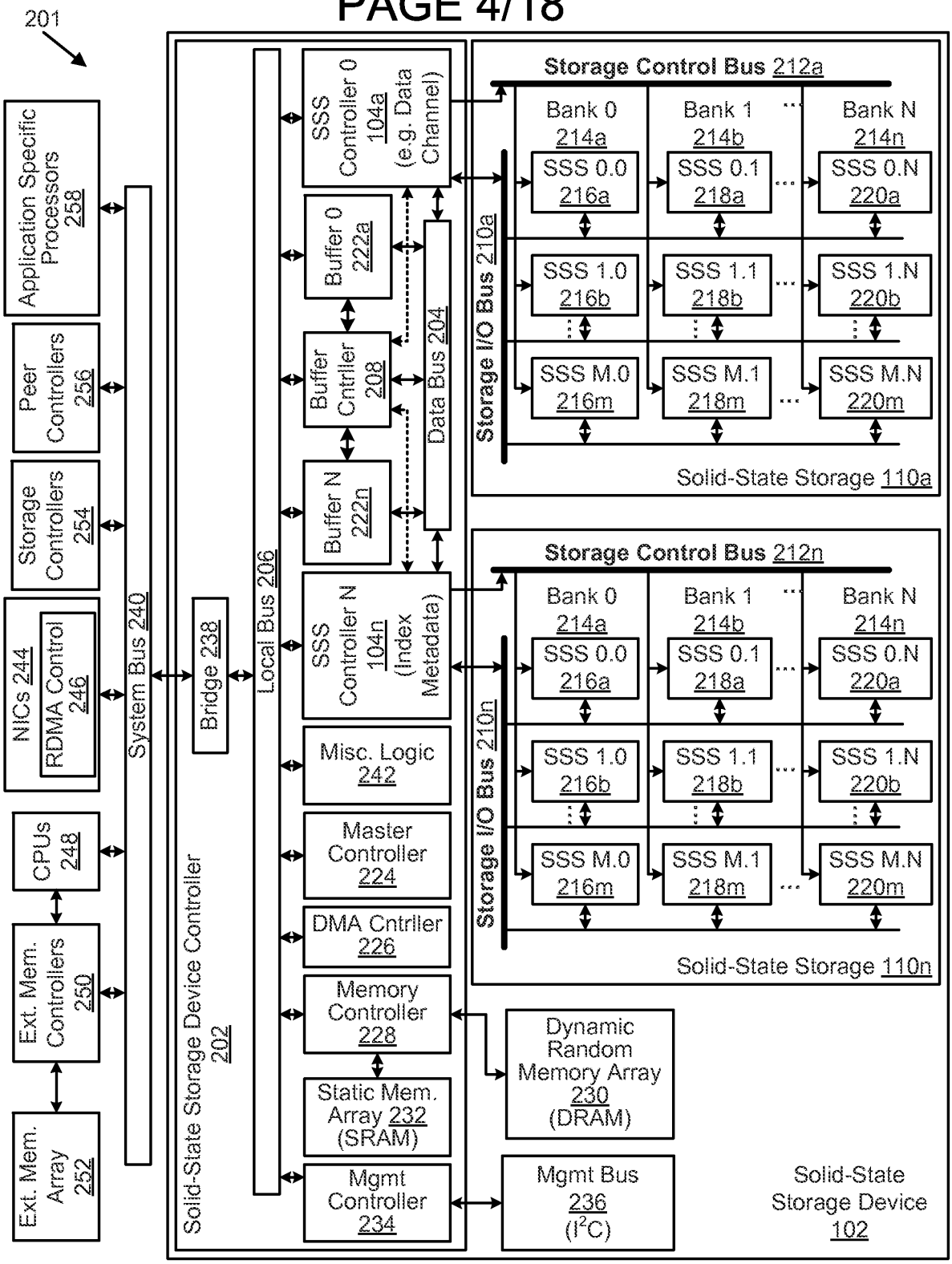


FIG. 2B

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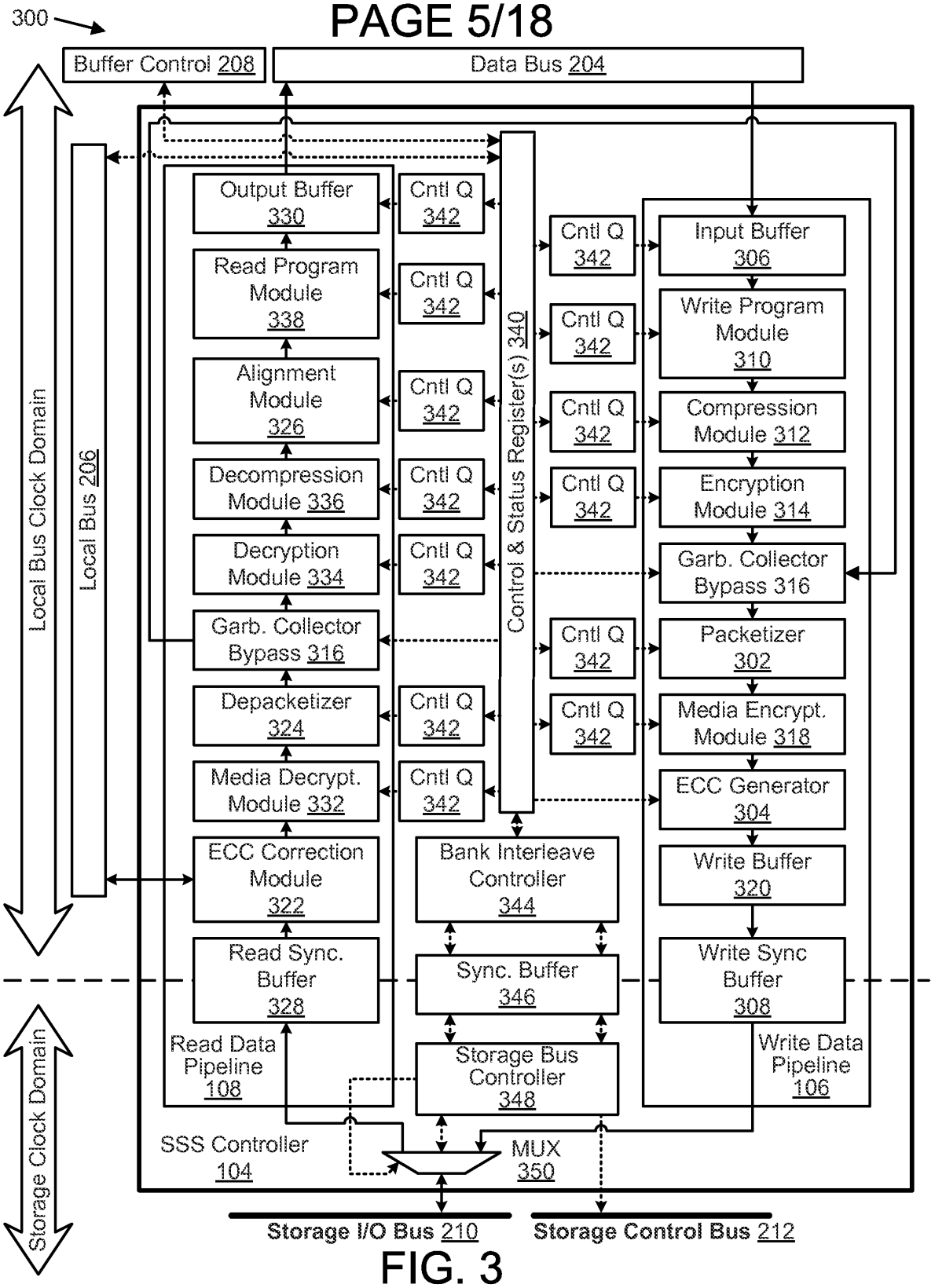


FIG. 3

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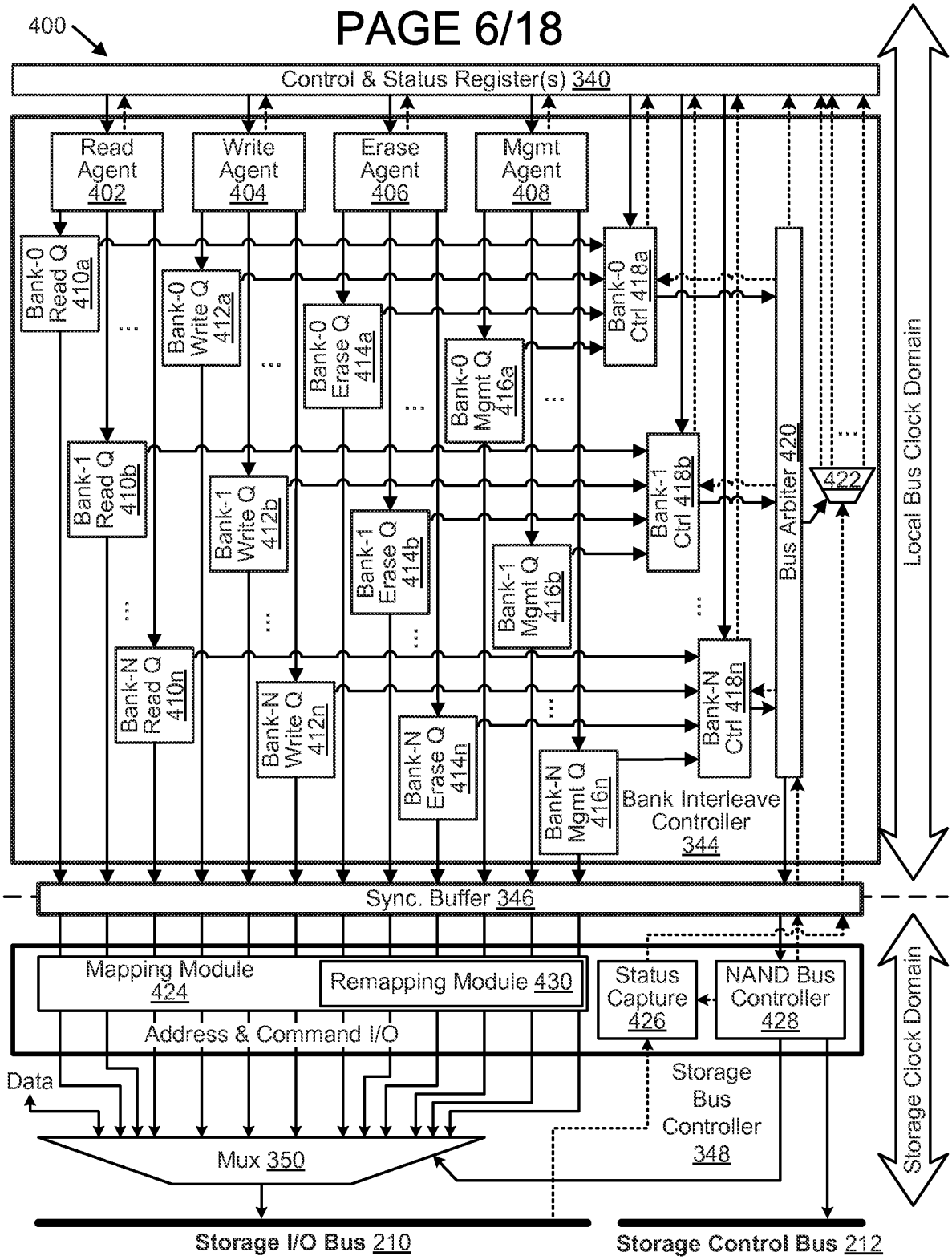


FIG. 4A

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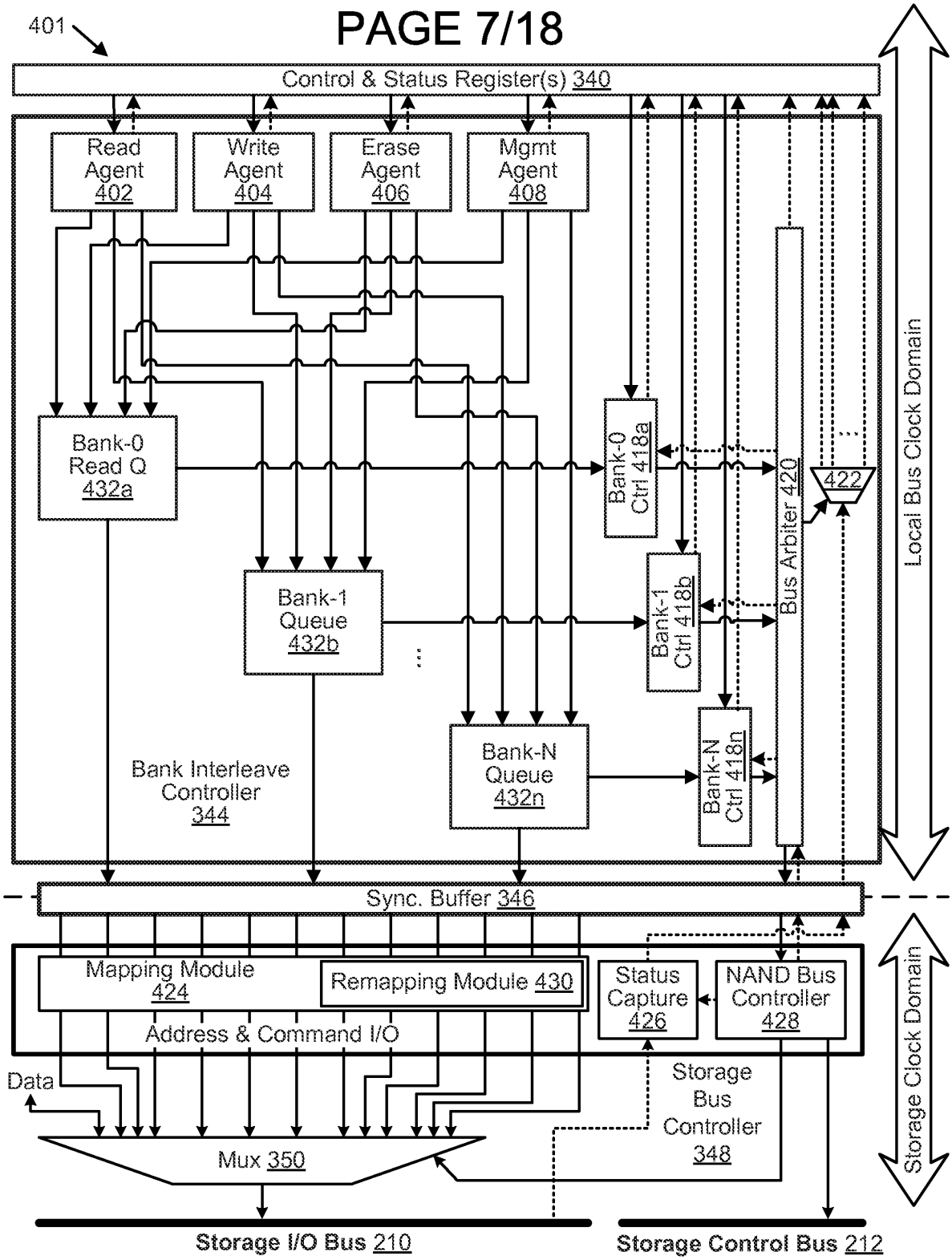


FIG. 4B

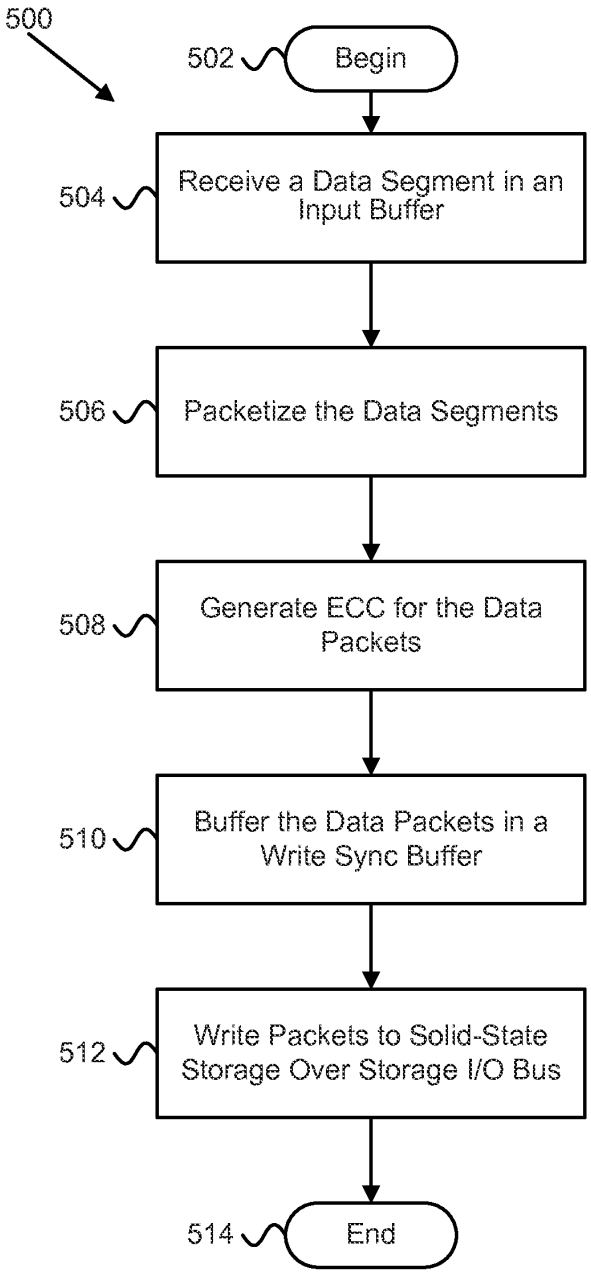

500
502
Begin
504
Receive a Data Segment in an Input Buffer
506
Packetize the Data Segments
508
Generate ECC for the Data Packets
510
Buffer the Data Packets in a Write Sync Buffer
512
Write Packets to Solid-State Storage Over Storage I/O Bus
514
End

FIG. 5

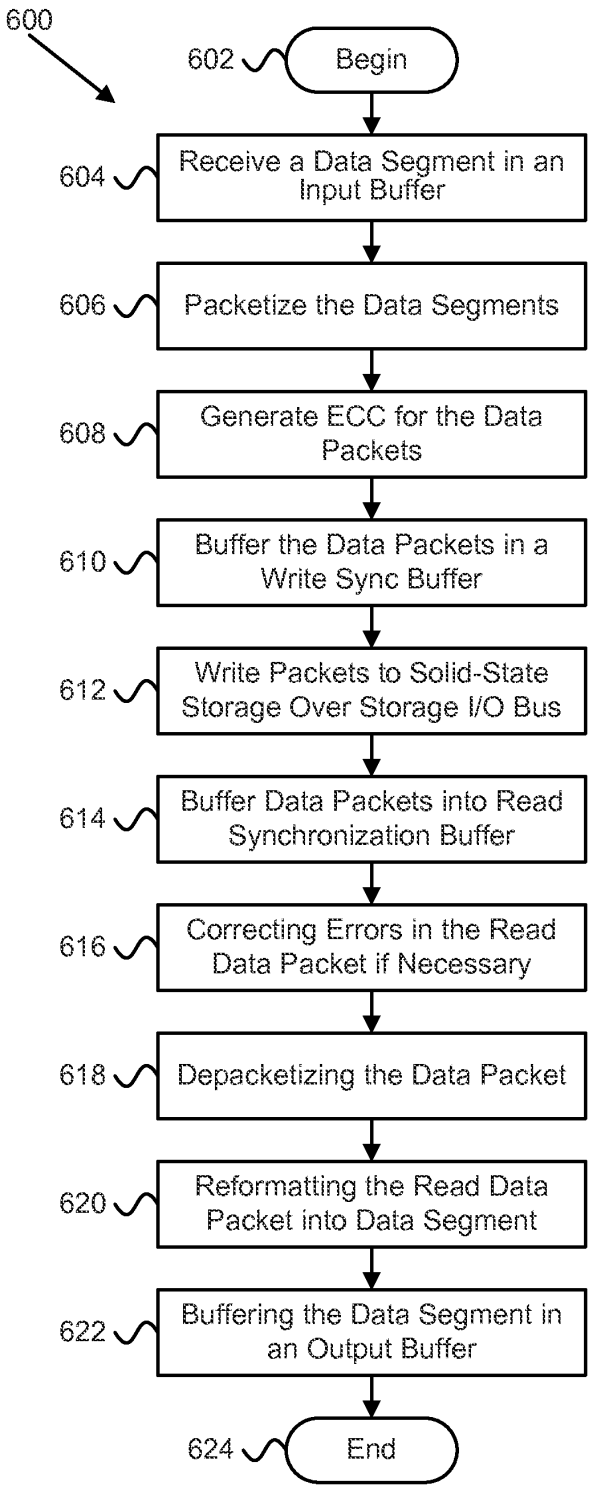

600
602
Begin
604
Receive a Data Segment in an Input Buffer
606
Packetize the Data Segments
608
Generate ECC for the Data Packets
610
Buffer the Data Packets in a Write Sync Buffer
612
Write Packets to Solid-State Storage Over Storage I/O Bus
614
Buffer Data Packets into Read Synchronization Buffer
616
Correcting Errors in the Read Data Packet if Necessary
618
Depacketizing the Data Packet
620
Reformatting the Read Data Packet into Data Segment
622
Buffering the Data Segment in an Output Buffer
624
End

FIG. 6

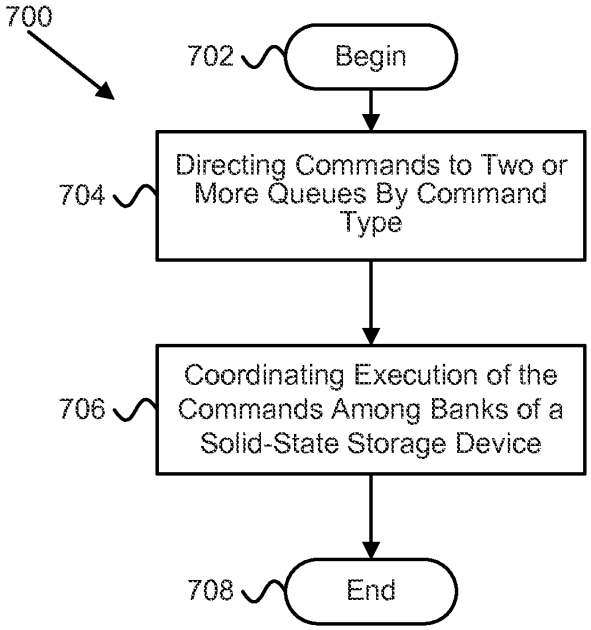

700
702
Begin
704
Directing Commands to Two or More Queues By Command Type
706
Coordinating Execution of the Commands Among Banks of a Solid-State Storage Device
708
End

FIG. 7

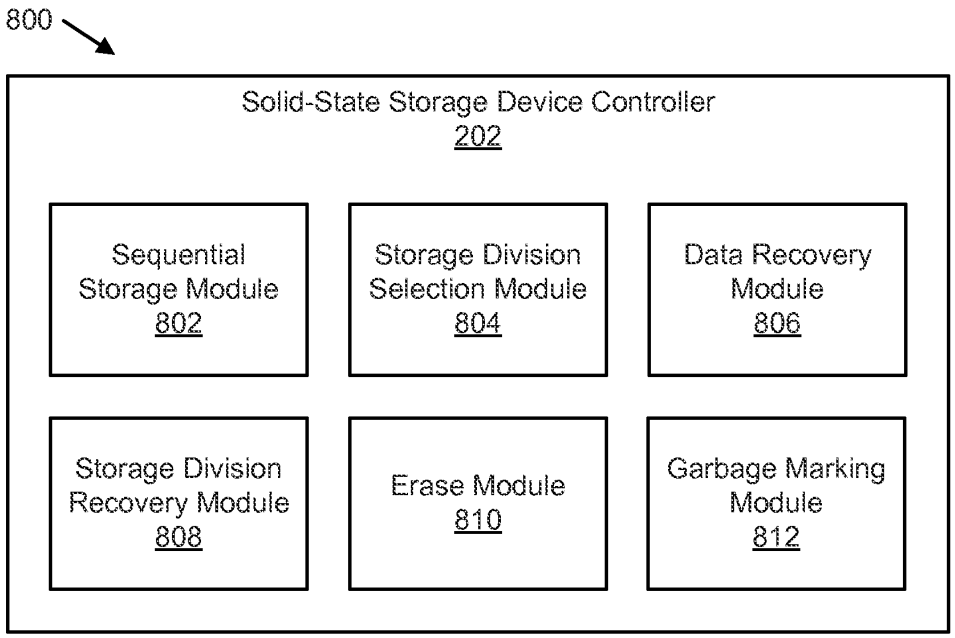

800
Solid-State Storage Device Controller
202
Sequential Storage Module
802
Storage Division Selection Module
804
Data Recovery Module
806
Storage Division Recovery Module
808
Erase Module
810
Garbage Marking Module
812

FIG. 8

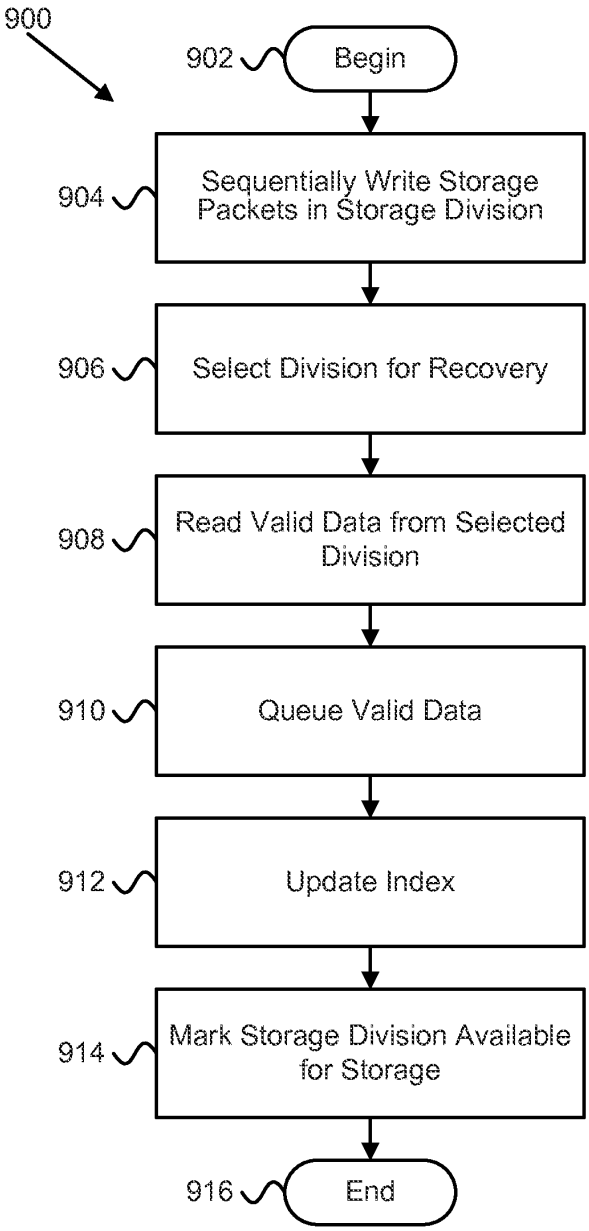

900
902
Begin
904
Sequentially Write Storage Packets in Storage Division
906
Select Division for Recovery
908
Read Valid Data from Selected Division
910
Queue Valid Data
912
Update Index
914
Mark Storage Division Available for Storage
916
End

FIG. 9

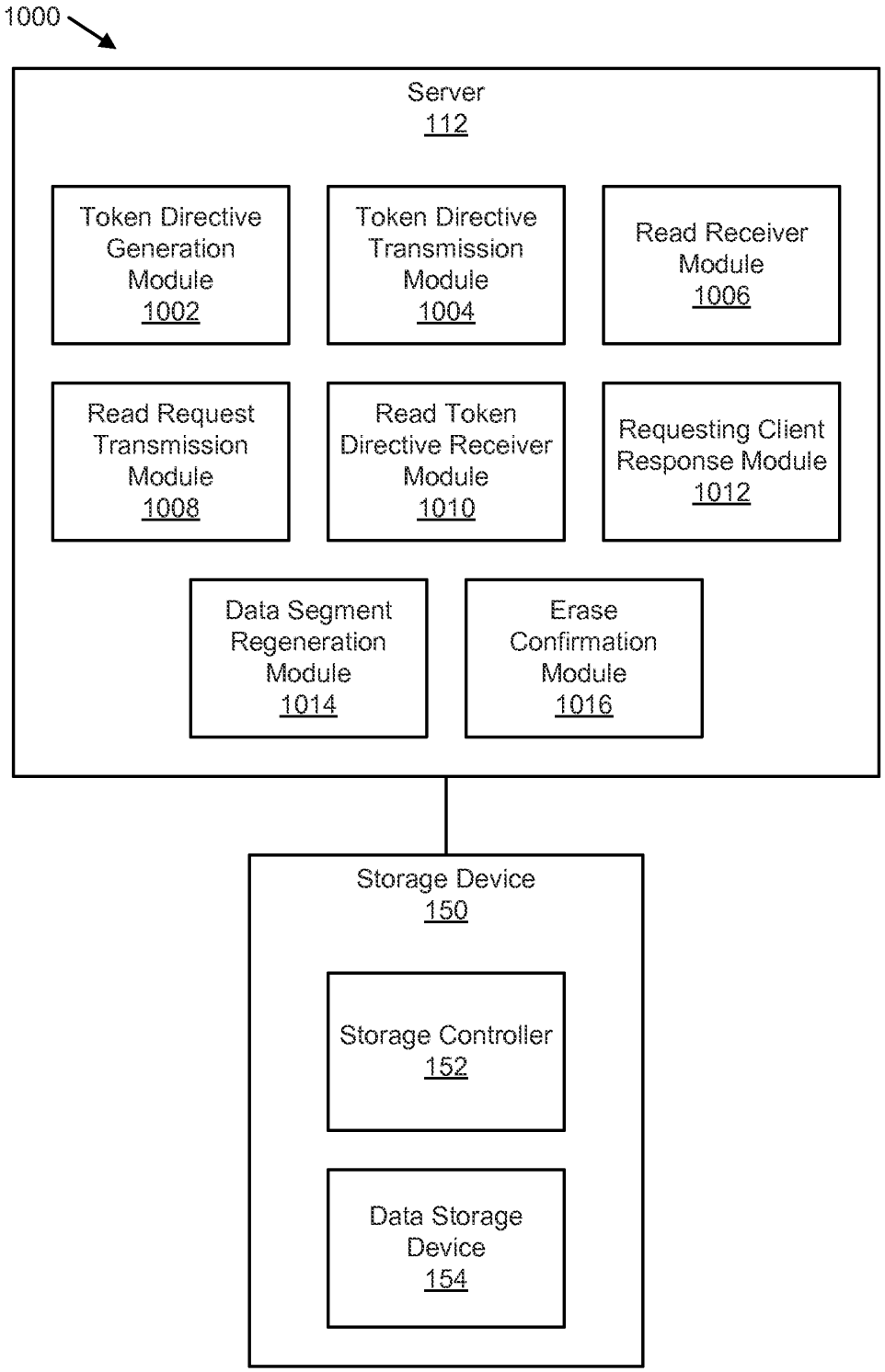

1000
Server
112
Token Directive Generation Module
1002
Token Directive Transmission Module
1004
Read Receiver Module
1006
Read Request Transmission Module
1008
Read Token Directive Receiver Module
1010
Requesting Client Response Module
1012
Data Segment Regeneration Module
1014
Erase Confirmation Module
1016
Storage Device
150
Storage Controller
152
Data Storage Device
154

FIG. 10

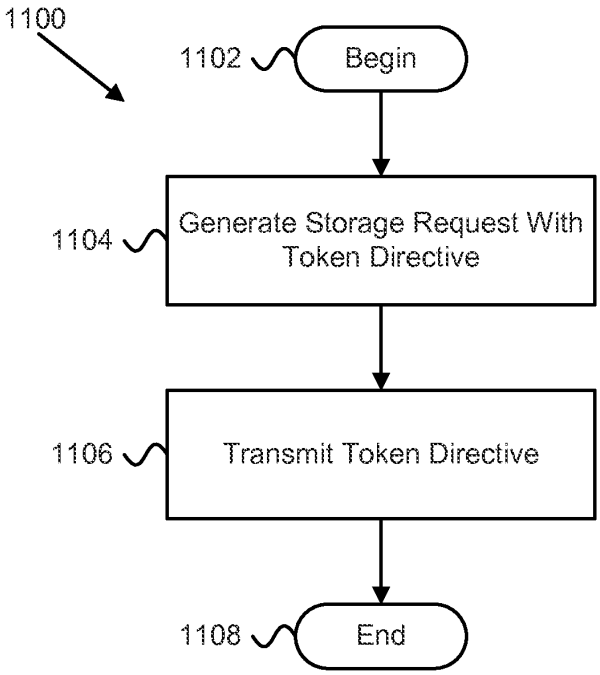

1100
1102
Begin
1104
Generate Storage Request With Token Directive
1106
Transmit Token Directive
1108
End

FIG. 11

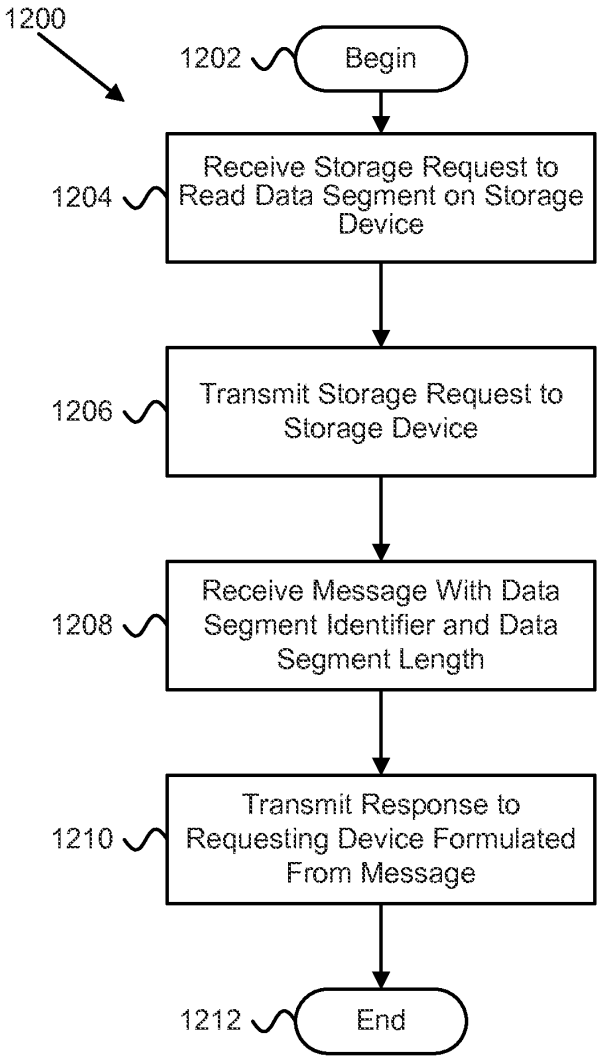

1200
1202
Begin
1204
Receive Storage Request to Read Data Segment on Storage Device
1206
Transmit Storage Request to Storage Device
1208
Receive Message With Data Segment Identifier and Data Segment Length
1210
Transmit Response to Requesting Device Formulated From Message
1212
End

FIG. 12

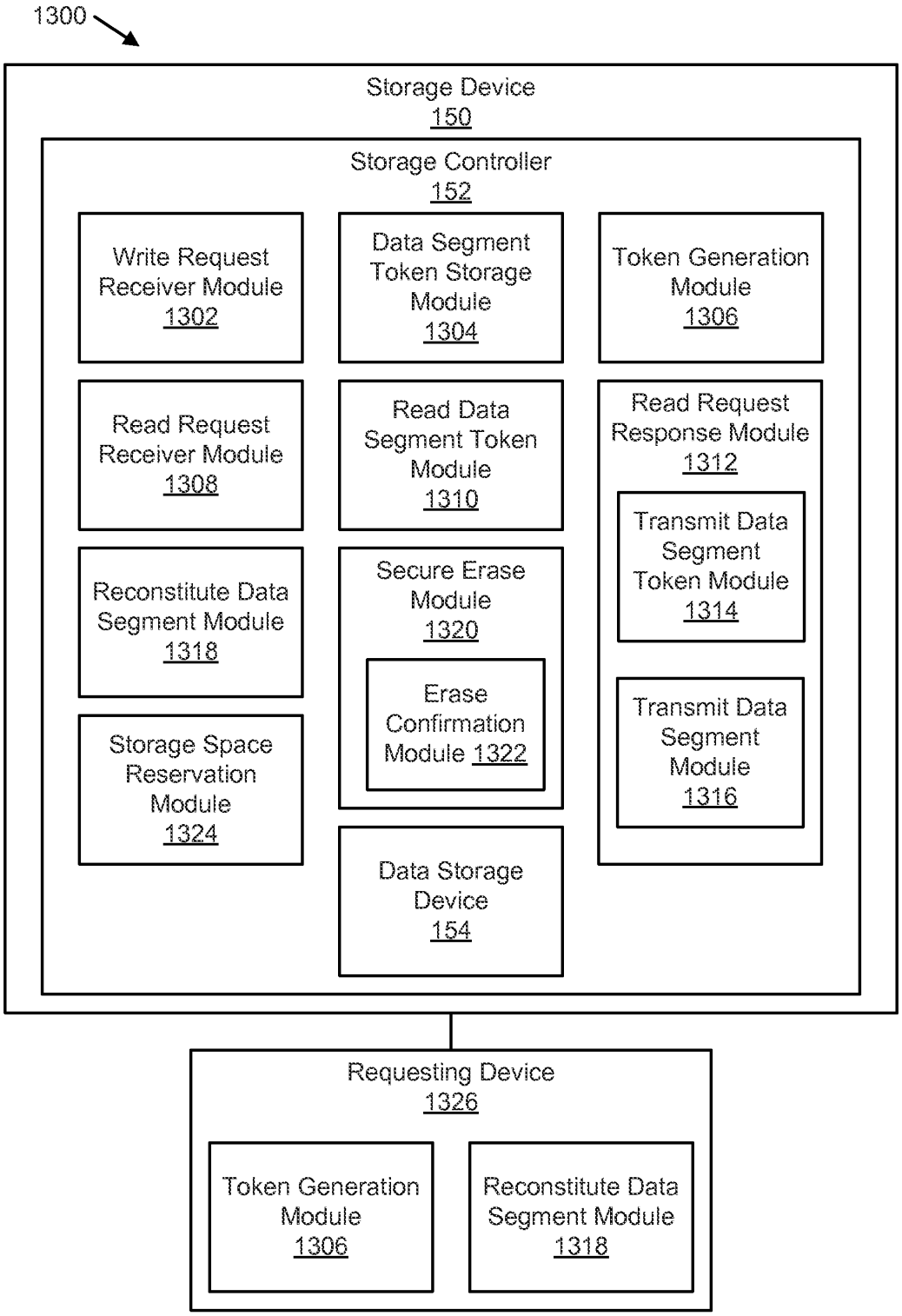

1300
Storage Device
150
Storage Controller
152
Write Request Receiver Module
1302
Data Segment Token Storage Module
1304
Token Generation Module
1306
Read Request Receiver Module
1308
Read Data Segment Token Module
1310
Read Request Response Module
1312
Transmit Data Segment Token Module
1314
Reconstitute Data Segment Module
1318
Secure Erase Module
1320
Erase Confirmation Module 1322
Transmit Data Segment Module
1316
Storage Space Reservation Module
1324
Data Storage Device
154
Requesting Device
1326
Token Generation Module
1306
Reconstitute Data Segment Module
1318

FIG. 13

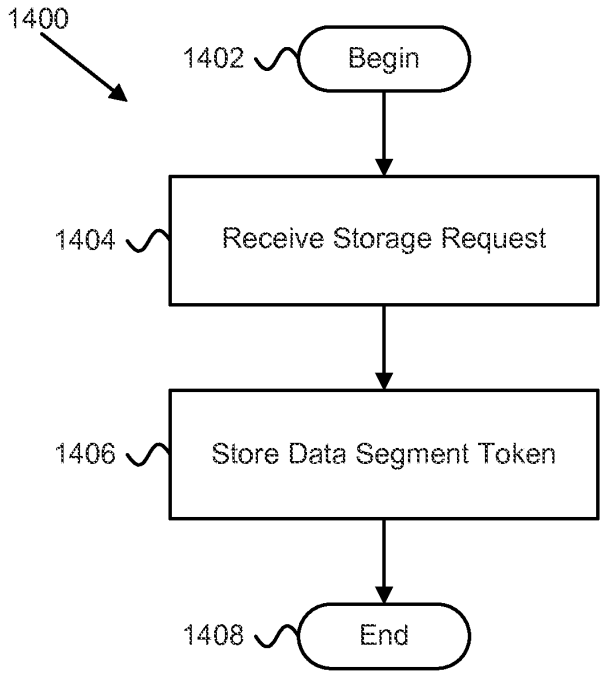

1400
1402
Begin
1404
Receive Storage Request
1406
Store Data Segment Token
1408
End

FIG. 14

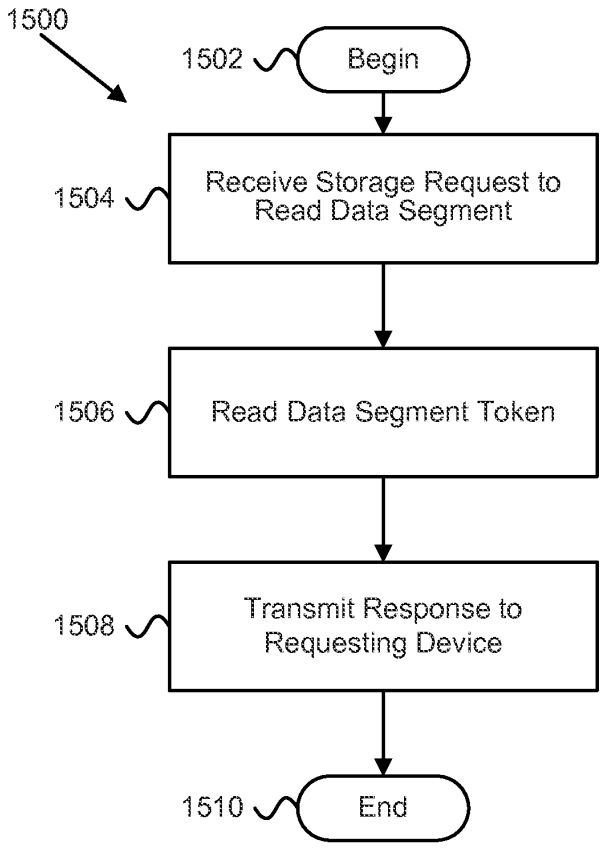

1500
1502
Begin
1504
Receive Storage Request to Read Data Segment
1506
Read Data Segment Token
1508
Transmit Response to Requesting Device
1510
End

FIG. 15

Electronic Acknowledgement Receipt	
EFS ID:	36904793
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems And Methods For Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	123084
Filer:	Spencer Chase Patterson/Denise Wilson
Filer Authorized By:	Spencer Chase Patterson
Attorney Docket Number:	FILO00200US27
Receipt Date:	16-AUG-2019
Filing Date:	
Time Stamp:	20:45:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1720
RAM confirmation Number	E20198FK46264556
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	FILO00200US27-ADS.pdf	1256742 074ca88759c91464701bb149f0551ff3c7480b48	no	9
Warnings:					
Information:					
2		FILO00200US27-App.pdf	364907 4e70a0044f7dee7f1067ea0fa12da4dbe604c153	yes	78

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	74
	Claims	75	77
	Abstract	78	78

Warnings:					
Information:					
3	Drawings-only black and white line drawings	FILO00200US27-Dwgs.pdf	588370 0479ec0dd3c7753597e734c4b2eaa6f9ec5a584a	no	18
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4	Oath or Declaration filed	FILO00200US27-Decl.pdf	238554 419ec2dbabc62f58209e43e3406a3e88a45dc8b9	no	6
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	34902 4a83ce059afecaed30fd83f2952cfd8a3ccb5237	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	2483475

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	David Flynn	§	Docket No.:	FILO00200US27
		§		
Serial No.:	16/543,464	§	Examiner:	TBD
		§		
Filed:	August 16, 2019	§	Art Unit:	TBD
		§		
Title:	Systems and Methods for Identifying Storage Resources That Are Not In Use	§	Conf. No.:	4625

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Dear Sir:

Pursuant to MPEP 609.02, Applicant(s) expect the Examiner to consider all the references submitted, cited, or otherwise considered during the prosecution of all the ancestor applications listed on the application data sheet of the present application. The Applicant(s) do not plan to resubmit a listing of those references unless the Examiner explicitly requests.

Respectfully submitted,

/Spencer C. Patterson/

Spencer C. Patterson
Reg. No.: 43,849
Attorney for Applicant

Date: August 16, 2019

Grable Martin Fulton PLLC
1914 Skillman Street, Ste. 110-144
Dallas, Texas 75206

Electronic Acknowledgement Receipt

EFS ID:	36905000
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	123084
Filer:	Spencer Chase Patterson/Denise Wilson
Filer Authorized By:	Spencer Chase Patterson
Attorney Docket Number:	FILO00200US27
Receipt Date:	16-AUG-2019
Filing Date:	
Time Stamp:	21:56:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	IDS-Transmittal.pdf	18336 220d13796558d41b1a1c207bc218b53a5dad1489	no	1

Warnings:

Information:	
Total Files Size (in bytes):	18336

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	36905002
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	123084
Filer:	Spencer Chase Patterson/Denise Wilson
Filer Authorized By:	Spencer Chase Patterson
Attorney Docket Number:	FILO00200US27
Receipt Date:	16-AUG-2019
Filing Date:	
Time Stamp:	21:57:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA.pdf	308911 52ebe80dc7bbe082d8a64915def8ace8d90a3584	no	2
Warnings:					

Information:	
Total Files Size (in bytes):	308911

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	36918677
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	123084
Filer:	Spencer Chase Patterson/Denise Wilson
Filer Authorized By:	Spencer Chase Patterson
Attorney Docket Number:	FILO00200US27
Receipt Date:	19-AUG-2019
Filing Date:	
Time Stamp:	22:42:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA.pdf	1195449 9aaea4e5df441b10a470c72406584fc44072318a	no	2
Warnings:					

Information:	
Total Files Size (in bytes):	1195449

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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New International Application Filed with the USPTO as a Receiving Office

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Electronic Acknowledgement Receipt	
EFS ID:	37599589
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	123084
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Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	FILO-notice.pdf	98060 e59bc24a71b934027620eef37979bbddfffd d4bf	no	2
Warnings:					
Information:					
2	Applicant Response to Pre-Exam Formalities Notice	FILO-response.pdf	17401 135006cfce198ae1486e6822db6b5c901b5 2bd13	no	1
Warnings:					
Information:					
3	Oath or Declaration filed	FILO-dec.pdf	114542 217d78f63f30cd9d806490f98089952c4c15 d23c	no	2
Warnings:					
Information:					
4	Power of Attorney	FIO-POA.pdf	295859 a4616ebccb6dd9eb778fc31bc129c46f68b 4638d	no	2
Warnings:					
Information:					
5	Assignee showing of ownership per 37 CFR 3.73	FIO-statement.pdf	126332 d674e25e82d4d547f2b50b08f0c3d7334e8 7210e	no	3
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	30487 1b6716e9b89dd964ec0418c6e656394562 71dada	no	2
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/543,464	08/16/2019	2136	1880	FILO00200US39	20	2

CONFIRMATION NO. 4625

UPDATED FILING RECEIPT

123084
Grable Martin Fulton (Marconi)
1914 Skillman Street, Suite 110-144
Dallas, TX 75206



Date Mailed: 11/01/2019

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

David Flynn, Sandy, UT;
Jonathan Thatcher, Liberty Lake, WA;
Michael Zappe, Arvada, CO;

Applicant(s)

FIO Semiconductor Technologies, LLC, Dallas, TX;

Power of Attorney: The patent practitioners associated with Customer Number 123084

Domestic Priority data as claimed by applicant

This application is a CON of 15/460,126 03/15/2017 PAT 10387328
which is a CON of 15/228,893 08/04/2016 PAT 10387327
which is a CON of 14/309,751 06/19/2014 PAT 9632727
which is a CON of 13/566,471 08/03/2012 PAT 8762658
which is a CON of 11/952,113 12/06/2007 PAT 8261005
which claims benefit of 60/974,470 09/22/2007
and claims benefit of 60/873,111 12/06/2006

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 08/27/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/543,464**

Projected Publication Date: 12/05/2019

Non-Publication Request: No

Early Publication Request: No

Title

Systems and Methods for Identifying Storage Resources That Are Not In Use

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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Silicon Motion - Exhibit 1014
Silicon Motion v. UTL - IPR2024-00199
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/543,464	08/16/2019	David Flynn	FILO00200US39

CONFIRMATION NO. 4625

123084
Grable Martin Fulton (Marconi)
1914 Skillman Street, Suite 110-144
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PUBLICATION NOTICE

OC000000113122519

Title: Systems and Methods for Identifying Storage Resources That Are Not In Use

Publication No.US-2019-0370185-A1
Publication Date:12/05/2019

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

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Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/543,464	08/16/2019	David Flynn	FILO00200US39	4625

123084 7590 09/10/2020

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1914 Skillman Street, Suite 110-144
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EXAMINER	
DUDEK JR, EDWARD J	

ART UNIT	PAPER NUMBER
2136	

NOTIFICATION DATE	DELIVERY MODE
09/10/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

prosecution@marconi.com
spatterson@GCHub.com

Office Action Summary	Application No. 16/543,464	Applicant(s) Flynn et al.	
	Examiner EDWARD J DUDEK JR	Art Unit 2136	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 16 January 2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-20 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 16 January 2019 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

This Office Action is responsive to the application filed 16 August 2019.

Claims 1-20 are pending and have been presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11, 12 and 16 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claim 11 recites the limitation "wherein performing garbage collection comprises" in 1. Claim 9 does not set forth a step of performing garbage collection, while claim 10 does introduce this step. There is insufficient antecedent basis for this limitation in the claim. For purposes of examination, the Examiner will interpret claim 11 as being dependent on claim 10, as that resolves the 112 issue.

Claim 12 recites the limitation "the erased erase block" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim. For purposes of examination, the Examiner will interpret claim 12 as being dependent on claim 11, as that resolves the 112 issue.

Claim 16 recites the limitation "the predetermined logic level" in line 1. There is insufficient antecedent basis for this limitation in the claim. For purposes of examination, the Examiner will interpret claim 16 as being dependent on claim 15, as that resolves the 112 issue.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-12 and 14 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (**U.S. Patent Application Publication #2006/0020744**) in view of Rajan (**U.S. Patent Application Publication #2009/0248763**).

1. Sinclair discloses A method for managing data in a block-based NAND flash storage system **(see [0030], flash memory system)**, the method comprising: a host processor **(see [0038], an application is executing on the host, implying that a processor is present to allow for execution of an application)**, deleting a file **(see [0036], file is deleted)**, *and issuing an empty-block directive including a block identifier (see Rajan below)*; and a NAND controller **(see [0038], flash memory controller)**, *receiving the empty-block directive (see Rajan below)*, and updating a table mapping logical identifiers to physical NAND flash storage locations, wherein the table is updated to indicate that data stored in one or more physical NAND flash storage locations associated with the block identifier do not need to be preserved **(see [0038], storage controller performs logical to physical mapping, [0047], new data is written to a different location which would involve updating mapping data, [0048], data that is deleted is marked as deallocated)**.

Sinclair fails to disclose issuing an empty-block directive including a block identifier and receiving the empty-block directive. Sinclair does disclose that FAT information is stored on the flash memory **(see [0042])**. When the application deletes a file, the FAT information is updated to indicate that the entry is deleted **(see [0036])**. It could be fair to interpret this change to the FAT as the empty-block directive, since the command would need to be sent to the flash memory controller as the FAT is on the flash memory. However, this is not an explicit command to delete data, and therefore a secondary reference is being introduced to fully teach the empty-block directives.

Rajan discloses issuing an empty-block directive including a block identifier and receiving the empty-block directive **(see [0053])**. Notifying the storage system of data that is no longer in use prevents excess storage allocation **(see [0012])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the teachings of Sinclair to allow the application to send an empty-block directive to prevent excess storage allocation, as taught by Rajan.

4. The method of claim 1, *wherein at least a part of the table is maintained in volatile memory (see below)*.

Sinclair and Rajan do not explicitly disclose that tat least part of the table is maintained in volatile memory. Sinclair does utilize flash, and the translations are stored on the flash memory **(see [0042])**. It is well-known in the art that repeated write and erase operations will increase the wear of a flash memory leasing to a shorter life span. Volatile memory, such as DRAM, also provides faster access. Having translation tables stored in volatile memory allows for faster access while also limiting the wear of the flash memory, and Official Notice is hereby taken.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the teachings of Sinclair and Rajan to store at least part of the table in volatile memory to provide faster access and reduce wear on the flash memory.

5. The method of claim 1, wherein the empty-block directive issued by the host processor further comprises an indication that data stored in the one or more physical NAND flash storage locations associated with the block identifier should be overwritten

(see Sinclair [0052], unallocated data is not copied, and would be overwritten after the block is erase and returned as a free block).

6. The method of claim 1, wherein the empty-block directive is part of a block storage protocol **(see Sinclair [0030], the system is communicating with a block based memory, so it can be interpreted as having a block storage protocol)**.

7. The method of claim 1, wherein the empty-block directive is issued at an application programming interface of the host processor **(see Sinclair [0038], host interfaces with the memory controller through an application)**.

8. The method of claim 1, wherein the empty-block directive is issued by a file system of the host processor **(see Sinclair [0036], file system indicates data that is deleted)**.

9. The method of claim 1, wherein the empty-block directive is issued by a storage client of the host processor **(see Sinclair [0038], host application)**.

10. The method of claim 1, further comprising the NAND controller performing garbage collection in the NAND flash storage system **(see Sinclair [0052])**.

11. The method of claim 9, wherein performing garbage collection comprises the NAND controller: copying a block containing data that should be preserved from an erase block comprising blocks containing data that does not need to be preserved; and erasing the erase block **(see Sinclair [0052])**.

12. The method of claim 10, further comprising the NAND controller writing data to the erased erase block **(see Sinclair [0004], the purpose of erasing a block is to allow new data to be written to the block)**.

14. The method of claim 1, wherein each of the one or more physical NAND flash storage locations are smaller than a NAND flash erase block **(see Sinclair [0004])**.

Claims 2-3 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (**U.S. Patent Application Publication #2006/0020744**) and Rajan (**U.S. Patent Application Publication #2009/0248763**) as applied to claims 1, 4-12 and 14 above, and further in view of Adelmann (**U.S. Patent Application Publication #2004/0003002**).

2. The method of claim 1 **(see Sinclair and Rajan above)**, *wherein responsive to receiving a read command including the block identifier from the host processor, the NAND controller returns a data string comprising data bits with a predetermined logic level (see Adelmann below).*

Sinclair and Rajan fail to disclose responsive to receiving a read command including the block identifier from the host processor, the NAND controller returns a data string comprising data bits with a predetermined logic level.

Adelmann discloses responsive to receiving a read command including the block identifier from the host processor, the NAND controller returns a data string comprising data bits with a predetermined logic level **(see [0039] and [0043], the user can access the file and be provided with additional details about the file, such as when the file was deleted)**. This allows the user to more intelligently manage large numbers of files by being able to accurately track when files are created, modified and deleted **(see [0003])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have to modify the teachings of Sinclair and Rajan to return predetermined data when reading a deleted file so that a user can accurately determine the status of a file, as taught by Adelmann.

3. The method of claim 2, wherein the predetermined logic level is zero **(see Rajan [0031], all data that is transferred over a bus is comprised of bits with logic level zero or logic level one. Therefore, depending on the data that is sent, the string could comprise all zero's, all one's or a mix of one's and zero's. The ability to send all zero's is within the operating parameters of the system)**.

Claim 13 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (**U.S. Patent Application Publication #2006/0020744**) and Rajan (**U.S. Patent Application Publication #2009/0248763**) as applied to claims 1, 4-12 and 14 above, and further in view of "A New Flash Memory Management for Flash Storage System", hereinafter referred to as NPL1.

13. The method of claim 1 **(see Sinclair and Rajan above)**, *wherein the NAND flash storage system is an append-only storage system (see NPL1 below)*.

Sinclair and Rajan fail to disclose wherein the NAND flash storage system is an append-only storage system.

NPL1 discloses wherein the NAND flash storage system is an append-only storage system **(see section 2 "Flash Memory Management)**. Append only writing provides a positive of effect of cycle-leveling **(see section 2 "Flash Memory Management)**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the teachings of Sinclair and Rajan to use an append only system to provide even wear leveling of the flash memory, as taught by NPL1.

Claims 15-20 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (**U.S. Patent Application Publication #2006/0020744**) in view of Rajan (**U.S. Patent Application Publication #2009/0248763**) and Adelmann (**U.S. Patent Application Publication #2004/0003002**).

15. Sinclair discloses A method for managing data in a NAND flash storage system **(see [0030], flash memory)**, the method comprising: *receiving an empty-block directive at a storage controller, the empty block directive including a logical identifier associated with a physical storage location (see Rajan below)* comprising data deleted by a host **(see [0036], file is deleted)**; *and returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty block directive (see Adelmann below).*

Sinclair fails to disclose receiving an empty-block directive at a storage controller, the empty block directive including a logical identifier associated with a physical storage location comprising data deleted by a host. Sinclair does disclose that FAT information is stored on the flash memory **(see [0042])**. When the application deletes a file, the FAT information is updated to indicate that the entry is deleted **(see [0036])**. It could be fair to interpret this change to the FAT as the empty-block directive, since the command

would need to be sent to the flash memory controller as the FAT is on the flash memory. However, this is not an explicit command to delete data, and therefore a secondary reference is being introduced to fully teach the empty-block directives.

Rajan discloses receiving an empty-block directive at a storage controller, the empty block directive including a logical identifier associated with a physical storage location comprising data deleted by a host **(see [0053])**. Notifying the storage system of data that is no longer in use prevents excess storage allocation **(see [0012])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the teachings of Sinclair to allow the application to send an empty-block directive to prevent excess storage allocation, as taught by Rajan.

Sinclair fails to disclose returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty block directive.

Adelmann discloses returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty block directive **(see [0039] and [0043], the user can access the file and be provided with additional details about the file, such as when the file was deleted)**. This allows the user to more intelligently manage large numbers of files by being able to accurately track when files are created, modified and deleted **(see [0003])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have to modify the teachings of Sinclair and Rajan to

return predetermined data when reading a deleted file so that a user can accurately determine the status of a file, as taught by Adelmann.

16. The method of claim 14, wherein the predetermined logic level is zero **(see Rajan [0031], all data that is transferred over a bus is comprised of bits with logic level zero or logic level one. Therefore, depending on the data that is sent, the string could comprise all zero's, all one's or a mix of one's and zero's. The ability to send all zero's is within the operating parameters of the system)**.

17. The method of claim 14, further comprising: determining that the empty-block directive further includes an indication that data associated with the logical identifier should be overwritten; and overwriting the data associated with the logical identifier **(see Sinclair [0052], unallocated data is not copied, and would be overwritten after the block is erase and returned as a free block)**.

18. The method of claim 14, wherein the empty-block directive is part of a block storage protocol **(see Sinclair [0030], the system is communicating with a block based memory, so it can be interpreted as having a block storage protocol)**.

19. The method of claim 14, wherein the empty-block directive is received through an application programming interface **(see Sinclair [0038], host interfaces with the memory controller through an application)**.

20. The method of claim 14, wherein the empty-block directive is received from a file system **(see Sinclair [0036], file system indicates data that is deleted)**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWARD J DUDEK JR whose telephone number is (571)270-1030. The examiner can normally be reached on Monday - Friday, 8:00A-4:00P.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Rones can be reached on 571-272-4085. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EDWARD J DUDEK JR/
Primary Examiner, Art Unit 2136

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~FILO00200US27~~ 10788.0721
	Application Number	
Title of Invention	Systems and Methods for Identifying Storage Resources That Are Not In Use	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	David		Flynn	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Sandy	State/Province	UT	Country of Residence	US

Mailing Address of Inventor:

Address 1	11222 Eagle View Drive		
Address 2			
City	Sandy	State/Province	UT
Postal Code	84092	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jonathan		Thatcher	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	Liberty Lake	State/Province	WA	Country of Residence	US

Mailing Address of Inventor:

Address 1	619 S. Neyland Avenue		
Address 2			
City	Liberty Lake	State/Province	WA
Postal Code	99019	Country	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Michael		Zappe	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~FILO00200US27~~ 10788.0721
	Application Number	
Title of Invention	Systems and Methods for Identifying Storage Resources That Are Not In Use	

City	Arvada	State/Province	CO	Country of Residence	US

Mailing Address of Inventor:

Address 1	8365 Quay Drive		
Address 2			
City	Arvada	State/Province	CO
Postal Code	80003	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	~~123084~~ 39602		
Email Address	~~docketing@gchub.com~~ docketing@ngtechlaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	Systems and Methods for Identifying Storage Resources That Are Not In Use		
Attorney Docket Number	~~FILO00200US27~~ 10788.0721	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	18	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~FILO00200US27~~ 10788.0721
	Application Number	
Title of Invention	Systems and Methods for Identifying Storage Resources That Are Not In Use	

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	~~123084~~ 39602		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	15460126	2017-03-15

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15460126	Continuation of	15228893	2016-08-04	10387327	2019-08-20

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15228893	Continuation of	14309751	2014-06-19	9632727	2017-04-25

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14309751	Continuation of	13566471	2012-08-03	8762658	2014-06-24

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13566471	Continuation of	11952113	2007-12-06	8261005	2012-09-04

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~FILE00200US27~~ 10788.0721
	Application Number	
Title of Invention	Systems and Methods for Identifying Storage Resources That Are Not In Use	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11952113	Claims benefit of provisional	60974470	2007-09-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11952113	Claims benefit of provisional	60873111	2006-12-06
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~FILO00200US27~~ 10788.0721
	Application Number	
Title of Invention	Systems and Methods for Identifying Storage Resources That Are Not In Use	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~FILO00200US27~~ 10788.0721
	Application Number	
Title of Invention	Systems and Methods for Identifying Storage Resources That Are Not In Use	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	~~FIO Semiconductor Technologies, LLC~~ Unification Technologies LLC		
Mailing Address Information For Applicant:			
Address 1	~~7160 Dallas Parkway~~ 6136 Frisco Square Blvd.		
Address 2	~~1717 McKinney Avenue, Suite 1050~~ Suite 400		
City	~~Dallas~~ Frisco	**State/Province**	TX
Country	US	Postal Code	~~75202~~ 75034
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~FILG00200US27-~~ 10788.0721
	Application Number	
Title of Invention	Systems and Methods for Identifying Storage Resources That Are Not In Use	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	~~/Spencer C. Patterson/~~ /David Wade Schnell/	Date (YYYY-MM-DD)	~~2019-08-16~~ 2020-11-17
First Name	~~Spencer C.~~ David Wade	Last Name	~~Patterson~~ Schnell
Registration Number	~~43849~~ 53563		

Additional Signature may be generated within this form by selecting the Add button. Add

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~FILQ00200US27~~ 10788.0721
	Application Number	
Title of Invention	Systems and Methods for Identifying Storage Resources That Are Not In Use	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	41142996
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	123084
Filer:	David Wade Schnell/Sally Hartway
Filer Authorized By:	David Wade Schnell
Attorney Docket Number:	FILO00200US39
Receipt Date:	17-NOV-2020
Filing Date:	16-AUG-2019
Time Stamp:	12:23:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	107880721_2020-11-17_transmittal_POA.pdf	132049 592e8966d9515862f2042696f7c9e5a763f3cb16	no	1

Warnings:

Information:					
2	Power of Attorney	107880721_2020-11-17_poa_signed_final.pdf	280519 c2bb6306f4ad1cc6b62edb7bf6364f9abba963e4	no	1
Warnings:					
Information:					
3	Assignee showing of ownership per 37 CFR 3.73	107880721_2020-11-17_373_Statement.pdf	117139 225850a1d6b958a59b7663c88336cccdc667e095	no	3
Warnings:					
Information:					
4	Miscellaneous Incoming Letter	107880721_2020-11-17_373_additional_page.pdf	36093 bfacc9d1b397d41684f6bace67a832c464185464	no	1
Warnings:					
Information:					
5	Application Data Sheet	107880721_2020-11-17_revised_ADS.pdf	360543 c35cfd4e5590d5a1df4ca7ff99d670f5876879a3	no	9
Warnings:					
Information:					
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			Total Files Size (in bytes):	926343	

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/543,464	08/16/2019	2136	1880	10788.0721	20	2

CONFIRMATION NO. 4625

CORRECTED FILING RECEIPT

39602
THE NOBLITT GROUP, PLLC
Daniel J. Noblitt
8777 NORTH GAINEY CENTER DRIVE
SUITE 175
SCOTTSDALE, AZ 85258



Date Mailed: 11/23/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

David Flynn, Sandy, UT;
Jonathan Thatcher, Liberty Lake, WA;
Michael Zappe, Arvada, CO;

Applicant(s)

Unification Technologies LLC, Frisco, TX;

Power of Attorney: The patent practitioners associated with Customer Number 39602

Domestic Priority data as claimed by applicant

This application is a CON of 15/460,126 03/15/2017 PAT 10387328
which is a CON of 15/228,893 08/04/2016 PAT 10387327
which is a CON of 14/309,751 06/19/2014 PAT 9632727
which is a CON of 13/566,471 08/03/2012 PAT 8762658
which is a CON of 11/952,113 12/06/2007 PAT 8261005
which claims benefit of 60/974,470 09/22/2007
and claims benefit of 60/873,111 12/06/2006

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 08/27/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/543,464**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

Systems and Methods for Identifying Storage Resources That Are Not In Use

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT

Inventor:	David Flynn	Docket No.:	10788.0721
Serial No.:	16/543,464	Examiner:	Edward J. Dudek Jr.
Filing Date:	August 16, 2019	Art Unit:	2136
Title:	Systems and Methods for Identifying Storage Resources That Are Not In Use	Conf. No. :	4625

AMENDMENT AND RESPONSE TO OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Commissioner:

The following submission is made in response to the office action mailed September 10, 2020.

Amendments to the Claims begin on page 2 of this paper; and

Remarks/Arguments begin on page 5 of this paper.

Electronic Acknowledgement Receipt

EFS ID:	41196089
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	39602
Filer:	David Wade Schnell/Sally Hartway
Filer Authorized By:	David Wade Schnell
Attorney Docket Number:	10788.0721
Receipt Date:	23-NOV-2020
Filing Date:	16-AUG-2019
Time Stamp:	12:05:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		107880721_2020-11-23_response_NFOA_Sept10_2020_FINAL.pdf	186861 d67e97a2d9af63ba9e060eea700d70d177de1314	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Arguments/Remarks Made in an Amendment	5	11
	Claims	2	4
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Warnings:			
Information:			
	Total Files Size (in bytes):	186861	

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

1. 35 U.S.C. § 112 Rejections

Claims 11, 12, and 16 are rejected under 35 U.S.C. 112(b), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor regards as the invention. In particular, and regarding claim 11, the office action asserts that there is insufficient antecedent basis for "wherein performing garbage collection comprises." In response, the applicant has amended claim 11 to depend from claim 10, which recites "performing garbage collection." Regarding claim 12, the office action asserts that there is insufficient antecedent basis for "the erased erase block." In response, the applicant has amended claim 12 to depend from claim 11, which recites "erasing the erase block." Regarding claim 16, the office action asserts that there is insufficient antecedent basis for "the predetermined logic level." In response, the applicant has amended claim 16 to depend from claim 15, which recites "a predetermined logic level." Accordingly, the applicant submits that the claims provide proper antecedent basis for the limitations and requests that the rejections be withdrawn.

2. 35 U.S.C. § 103 Rejections

Claims 1, 4-12 and 14 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent Pub. No. 2006/0020744 to Sinclair (the "Sinclair reference") in view of U.S. Patent Pub. No. 2009/0248763 to Rajan (the "Rajan reference").

Claims 2 and 3 stand rejected under 35 U.S.C. § 103 as being unpatentable over the Sinclair reference in view of the Rajan reference and in further view of U.S. Patent Pub. No. 2001/0003002 to Adelmlann (the "Adelmann reference").

Claim 13 stands rejected under 35 U.S.C. § 103 as being unpatentable over the Sinclair reference in view of the Rajan reference and in further view of "A New Flash Memory Management for Flash Storage System."

Claims 15-20 stand rejected under 35 U.S.C. § 103 as being unpatentable over the Sinclair reference in view of the Rajan reference and in further view of the Adelmlann reference.

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Under the rationale used to reject the claims, the prior art references when modified must still teach or suggest all the claim limitations of the rejected claims. The applicant submits that claimed elements and limitations are not disclosed by the references nor can they be modified to arrive at the claimed invention and the rejections should be withdrawn.

The Sinclair reference fails to disclose a table that is updated to indicate that data stored in a flash storage location associated with the block identifier do not need to be preserved.

Claim 1 expressly requires "updating a table mapping logical identifiers to physical NAND flash storage locations, wherein the table is updated to indicate that data stored in one or more physical NAND flash storage locations associated with the block identifier do not need to be preserved." In support of the rejection, the office action asserts that paragraphs 0038, 0047, and 0048 of the Sinclair reference teach that a "storage controller performs logical to physical mapping," "new data is written to a different location which would involve updating mapping data," and "data that is deleted is marked as deallocated." The applicant asserts that the office action has ignored the express language of the claims, and as a result, the office action incorrectly asserts that the Sinclair reference teaches the claim limitations. In particular, the applicant submits that the Sinclair reference does not teach a "table that is updated to indicate that data…associated with the block identifier does not need to be preserved." Rather, the Sinclair reference teaches that "if it is determined (616) that one or more clusters have been deallocated, the status of the one or more clusters in a Data Allocation Table (DAT) is changed to indicate a "deallocated" status." (paragraph 0048). In other words, the Sinclair reference teaches that the table is updated to indicate data that has already been deallocated (i.e., that a deallocation happened *in the past*). There is nothing in the Sinclair reference that teaches that the table indicates data that does not need to be preserved (i.e., referring to a preservation of the data *in the future*).

The applicant asserts that the references, either alone or combination, fail to teach a table that indicates data that does not need to be preserved, as claimed. Therefore, the applicant submits that the 35 U.S.C. § 103 rejection should be withdrawn. Inasmuch as claims 2-14

depend from and include the limitations of independent claim 1 the rejections should also be withdrawn.

The Sinclair reference fails to disclose the empty-block directive

Claims 5-9 further define the claimed empty-block directive, which is first recited in claim 1. As it relates to claim 1, the office action admitted that the Sinclair reference did not teach the empty-block directive and instead relied on the Rajan reference to teach this limitation. However, in claims 5-9, which depend from claim 1, the office action relied on the Sinclair reference to teach limitations relating to the empty-block directive. The applicant asserts that if the Sinclair reference does not teach the empty-block directive of claim 1, it is not possible for the Sinclair reference to now teach the empty-block directive of claims 5-9. Accordingly, the rejections are inappropriate and should be withdrawn.

The Sinclair reference fails to disclose that a physical NAND flash storage location is smaller than a NAND flash erase block

Claim 14 expressly requires "wherein each of the one or more physical NAND flash storage locations are smaller than a NAND flash erase block." In support of the rejection, the office action submits that paragraph 0004 of the Sinclair reference teaches the limitations. The applicant disagrees. Paragraph 0004 of the Sinclair reference describes that physical memory cells are divided into "blocks" of cells that are erased together, which means that the "blocks" are smaller than physical memory cell. This is exactly the opposite of the plain language of the claim.

Accordingly, the applicant asserts that the references, either alone or combination, fail to teach a physical NAND flash storage location is smaller than a NAND flash erase block, as claimed. Therefore, applicant submits that the 35 U.S.C. § 103 rejection should be withdrawn.

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The Adelmann reference fails to disclose a data string comprising data bits with a predetermined logic level

Claim 2 expressly requires "the NAND controller returns a data string comprising data bits with a predetermined logic level" in response to receiving a read command including the block identifier from the host processor. Similarly, independent claim 15 expressly requires "returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty block directive."

In support of the rejections, the office action refers generally to paragraphs 0039 and 0043 of the Adelmann reference and states that "the user can access the file and be provided with additional details about the file, such as when the file was deleted." The applicant disagrees. Paragraph 0039 describes the process in which a user can access a file stored in the memory 120 by way of the file-management system 100. Paragraph 0043 describes the how the system operates to determine when a file is modified/deleted and that the system stores information related to the modification/deletion, such as the day the file was created, edited, moved and deleted. This information related to modification/deletions of a file can be accessed by the user. There is nothing in the foregoing paragraphs or anywhere in the Adelmann reference that teaches a data string comprising data bits with a *predetermined logic level*. In the Adelmann reference, the information stored relating to modifications/deletions of a particular file do not have a "predetermined logic level." Instead, the information provided to the user about a file will be specific to that file, and are therefore are not "predetermined."

Accordingly, the applicant asserts that the references, either alone or combination, fail to teach a data string comprising data bits with a predetermined logic level, as claimed. Therefore, applicant submits that the 35 U.S.C. § 103 rejection should be withdrawn. Inasmuch as claims 16-20 depend from and include the limitations of independent claim 15 the rejections should also be withdrawn.

The office action relies on improper Official Notice

Claim 4 stands rejected under 35 U.S.C. § 103 as purportedly being unpatentable over the Sinclair and Rajan references in view of Official Notice.

Official notice unsupported by documentary evidence should only be taken where the facts asserted to be well-known, or to be common knowledge in the art, are capable of instant and unquestionable demonstration as being well-known. MPEP § 2144.03(A). "For example, assertions of technical facts in the areas of esoteric technology or specific knowledge of the prior art must **always** be supported by citation to some reference work recognized as standard in the pertinent art. *In re Ahlert*, 424 F.2d at 1091, 165 USPQ at 420-21" (*Id.*, emphasis added). The applicant notes that no such support has been provided in this case.

Reviewing courts must rely on the record, and the Federal Circuit has always required that absent the case where Official Notice is "instant and unquestionable", the office action must provide support and reasoning for Official Notice to be proper. Any facts so noticed should be of notorious character and serve only to "fill in the gaps" in an insubstantial manner which might exist in the evidentiary showing made by the examiner to support a particular ground for rejection. MPEP § 2144.03(A). It is never appropriate to rely solely on common knowledge in the art without evidentiary support in the record as the principal evidence upon which a rejection was based. *Id.* Furthermore, "[i]f the examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding." MPEP § 2144.03(C) (citing 37 CFR § 1.104(d)(2)).

In the present case, the office action takes Official Notice that "repeated write and erase operations increase the wear of the flash memory," that "volatile memory, such as DRAM, provides faster access," and that "having translation tables stored in volatile memory allows for faster access while also limiting the wear of the flash memory."

The applicant respectfully traverses this attempted use of Official Notice. Per the above, the facts asserted as well-known must be capable of instant and unquestionable demonstration as being well-known, and the applicant does not believe that such is the case here. **In particular,**

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the applicant asserts that the noticed facts are not considered to be common knowledge or well-known in the art because they are in areas of esoteric technology and relate to specific knowledge of the prior art, and must be supported.

If the examiner continues to believe that the above-recited features are well known in the art, the applicant respectfully requests that the examiner provide a reference or references in the next office action allegedly offering evidence that this is the case.

If the applicant adequately traverses the examiner's assertion of official notice, the examiner must provide documentary evidence in the next Office action if the rejection is to be maintained. See 37 CFR 1.104(c)(2). See also *Zurko*, 258 F.3d at 1386, 59 USPQ2d at 1697 ("[T]he Board [or examiner] must point to some concrete evidence in the record in support of these findings" to satisfy the substantial evidence test). If the examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding. See 37 CFR 1.104(d)(2). (MPEP § 2144.03(C)). The legal standard for applying Official Notice under MPEP § 2144.03 is rigorous, and the applicant respectfully submits that the present application of Official Notice falls short of meeting this high standard.

To the extent the office action relies on "common knowledge" in the rejections of the claims, the applicant traverses these findings and request adequate evidence to support them in accordance with 37 CFR § 1.104 and MPEP § 2144.03.

Per the above, the cited reference fails to teach or suggest all of the features of claim 4. Accordingly, it is respectfully submitted that the rejection is overcome and respectfully requested that the rejection be withdrawn.

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CONCLUSION

In view of the foregoing, it is believed that all of the pending claims are in condition for allowance. The applicant therefore requests that the examiner withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding office action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is requested. If the examiner believes that a telephone conference would be useful in moving the application toward allowance, the examiner is encouraged to contact the attorney of record.

Respectfully submitted,

Date: November 23, 2020

/David Wade Schnell/
David Wade Schnell
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Amendments to the Claims

1. (Original) A method for managing data in a block-based NAND flash storage system, the method comprising:

a host processor,

deleting a file, and

issuing an empty-block directive including a block identifier; and

a NAND controller,

receiving the empty-block directive, and

updating a table mapping logical identifiers to physical NAND flash storage locations, wherein the table is updated to indicate that data stored in one or more physical NAND flash storage locations associated with the block identifier do not need to be preserved.

2. (Original) The method of claim 1, wherein responsive to receiving a read command including the block identifier from the host processor, the NAND controller returns a data string comprising data bits with a predetermined logic level.

3. (Original) The method of claim 2, wherein the predetermined logic level is zero.

4. (Original) The method of claim 1, wherein at least a part of the table is maintained in volatile memory.

5. (Original) The method of claim 1, wherein the empty-block directive issued by the host processor further comprises an indication that data stored in the one or more physical NAND flash storage locations associated with the block identifier should be overwritten.

6. (Original) The method of claim 1, wherein the empty-block directive is part of a block storage protocol.

7. (Original) The method of claim 1, wherein the empty-block directive is issued at an application programming interface of the host processor.

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8. (Original) The method of claim 1, wherein the empty-block directive is issued by a file system of the host processor.

9. (Original) The method of claim 1, wherein the empty-block directive is issued by a storage client of the host processor.

10. (Original) The method of claim 1, further comprising the NAND controller performing garbage collection in the NAND flash storage system.

11. (Currently amended) The method of claim [[9]] 10, wherein performing garbage collection comprises the NAND controller:

copying a block containing data that should be preserved from an erase block comprising blocks containing data that does not need to be preserved; and

erasing the erase block.

12. (Currently amended) The method of claim [[10]] 11, further comprising the NAND controller writing data to the erased erase block.

13. (Original) The method of claim 1, wherein the NAND flash storage system is an append-only storage system.

14. (Original) The method of claim 1, wherein each of the one or more physical NAND flash storage locations are smaller than a NAND flash erase block.

15. (Original) A method for managing data in a NAND flash storage system, the method comprising:

receiving an empty-block directive at a storage controller, the empty block directive including a logical identifier associated with a physical storage location comprising data deleted by a host; and

returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty block directive.

16. (Currently amended) The method of claim [[14]] 15, wherein the predetermined logic level is zero.

17. (Currently amended) The method of claim [[14]] 15, further comprising:

determining that the empty-block directive further includes an indication that data associated with the logical identifier should be overwritten; and

overwriting the data associated with the logical identifier.

18. (Currently amended) The method of claim [[14]] 15, wherein the empty-block directive is part of a block storage protocol.

19. (Currently amended) The method of claim [[14]] 15, wherein the empty-block directive is received through an application programming interface.

20. (Currently amended) The method of claim [[14]] 15, wherein the empty-block directive is received from a file system.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/543,464	08/16/2019	David Flynn	10788.0721	4625

175872 7590 01/27/2021

Acacia Research Group, LLC
4 Park Plaza, Suite 550
Irvine, AZ 92614

EXAMINER	
DUDEK JR, EDWARD J	

ART UNIT	PAPER NUMBER
2136	

NOTIFICATION DATE	DELIVERY MODE
01/27/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@ngtechlaw.com
dwschnell@ngtechlaw.com

Office Action Summary	Application No. 16/543,464	Applicant(s) Flynn et al.	
	Examiner EDWARD J DUDEK JR	Art Unit 2136	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 23 November 2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-20 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

This Office Action is responsive to the reply filed 23 November 2020.

Claims 1-20 are pending and have been presented for examination.

Response to Arguments

Applicant's arguments, see page 5, filed 23 November 2020, with respect to claims 11, 12 and 16 have been fully considered and are persuasive. The rejection of claims 11, 12 and 16 under 35 U.S.C. § 112 has been withdrawn.

Applicant's arguments filed 23 November 2020 have been fully considered but they are not persuasive.

Applicant argues (see page 6):

> Claim 1 expressly requires "updating a table mapping logical identifiers to physical NAND flash storage locations, wherein the table is updated to indicate that data stored in one or more physical NAND flash storage locations associated with the block identifier do not need to be preserved." In support of the rejection, the office action asserts that paragraphs 0038, 0047, and 0048 of the Sinclair reference teach that a "storage controller performs logical to physical mapping," "new data is written to a different location which would involve updating mapping data," and "data that is deleted is marked as deallocated." The applicant asserts that the office action has ignored the express language of the claims, and as a result, the office action incorrectly asserts that the Sinclair reference teaches the claim limitations. In particular, the applicant submits

> that the Sinclair reference does not teach a "table that is updated to indicate that data...associated with the block identifier does not need to be preserved." Rather, the Sinclair reference teaches that "if it is determined (616) that one or more clusters have been deallocated, the status of the one or more clusters in a Data Allocation Table (DAT) is changed to indicate a "deallocated" status." (paragraph 0048). In other words, the Sinclair reference teaches that the table is updated to indicate data that has already been deallocated (i.e., that a deallocation happened in the past). There is nothing in the Sinclair reference that teaches that the table indicates data that does not need to be preserved (i.e., referring to a preservation of the data in the future).

The Examiner respectfully disagrees. It is well known that flash memory cannot be overwritten and in order to write new data to a flash cell the cell must first be erased (see [0004]). Sinclair implements a Data Attribute Store that involves the use of a Data Attribute Table (see [0031]-[0032]). When a file, or a portion of a file, is deallocated by the host (i.e. deleted), the status of the cluster will be recorded in the DAT to indicate it has been deallocated (see [0033], [0048]-[0049]). This deallocated data is data that is no longer required to be maintained. In the future, when garbage collection operations are performed, this status information is used to determine which clusters are copied from the old location to the new locations (see [0035]). The garbage collection operation copies clusters that are allocated and does not copy (i.e. does not preserve) clusters that have been deallocated. Therefore, the DAT does indicate which data does not need to preserved.

Applicant argues (see page 7):

> Claims 5-9 further define the claimed empty-block directive, which is first recited in claim 1. As it relates to claim 1, the office action admitted that the Sinclair reference did

> not teach the empty-block directive and instead relied on the Rajan reference to teach this limitation. However, in claims 5-9, which depend from claim 1, the office action relied on the Sinclair reference to teach limitations relating to the empty-block directive. The applicant asserts that if the Sinclair reference does not teach the empty-block directive of claim 1, it is not possible for the Sinclair reference to now teach the empty-block directive of claims 5-9. Accordingly, the rejections are inappropriate and should be withdrawn.

The Examiner respectfully disagrees. The rejection of clam 1, from which claims 5-9 depend from, provide a foundation for combining Sinclair and Rajan. Rajan is relied upon solely for an explicit empty-block directive. Sinclair already discloses a communication path and protocol for communication between a host and a storage device. There is no suggestion that this communication is modified by the inclusion of the empty-block directive disclosed by Rajan. Sinclair is cited for claims 5-9, as Sinclair provides the communication structure. Knowing the combination of Sinclair and Rajan, from claim 1, would result in the addition of an empty-block directive to the system disclosed by Sinclair, it is clear that this empty-block directive would be sent over the existing communication structure disclosed by Sinclair.

Applicant argues (see page 7):

> Claim 14 expressly requires "wherein each of the one or more physical NAND flash storage locations are smaller than a NAND flash erase block." In support of the rejection, the office action submits that paragraph 0004 of the Sinclair reference teaches the limitations. The applicant disagrees. Paragraph 0004 of the Sinclair reference describes that physical memory cells are divided into "blocks" of cells that are erased together, which means that the "blocks" are smaller than physical memory cell. This is exactly the opposite of the plain language of the claim.

The Examiner respectfully disagrees. This section of Sinclair is not disclosing splitting flash cells, but rather grouping multiple flash cells into blocks. Sinclair states that a block contains multiple pages, with each page storing a minimum of 512 bytes of user data. A memory cell holds three of fewer bits of data (see [0003]). So it is not possible for a page to hold 512 bytes of data but yet be smaller than a cell that holds at most three bits of data.

Applicant argues (see page 8):

> Claim 2 expressly requires "the NAND controller returns a data string comprising data bits with a predetermined logic level" in response to receiving a read command including the block identifier from the host processor. Similarly, independent claim 15 expressly requires "returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty block directive."
>
> In support of the rejections, the office action refers generally to paragraphs 0039 and 0043 of the Adelmann reference and states that "the user can access the file and be provided with additional details about the file, such as when the file was deleted." The applicant disagrees. Paragraph 0039 describes the process in which a user can access a file stored in the memory 120 by way of the file-management system 100. Paragraph 0043 describes the how the system operates to determine when a file is modified/deleted and that the system stores information related to the modification/deletion, such as the day the file was created, edited, moved and deleted. This information related to modification/deletions of a file can be accessed by the user. There is nothing in the foregoing paragraphs or anywhere in the Adelmann reference that teaches a data string comprising data bits with a predetermined logic level. In the Adelmann reference, the information stored relating to modifications/deletions of a particular file do not have

> a "predetermined logic level." Instead, the information provided to the user about a file will be specific to that file, and are therefore are not "predetermined."

The Examiner respectfully disagrees. Predetermined is being interpreted as being known prior to asking for the information. Adelmann stores information indicating data has been deleted. In the future, when a host attempts to access the file, the information about the deletion of the file can be returned to the user. All information is stored as a series of bits. As the deletion has already taken place, and the data about the deletion has been stored, the bits that represent this information have been predetermined prior to the user asking for this information.

Applicant argues (see pages 9-10):

> In the present case, the office action takes Official Notice that "repeated write and erase operations increase the wear of the flash memory," that "volatile memory, such as DRAM, provides faster access," and that "having translation tables stored in volatile memory allows for faster access while also limiting the wear of the flash memory."
>
> The applicant respectfully traverses this attempted use of Official Notice. Per the above, the facts asserted as well-known must be capable of instant and unquestionable demonstration as being well-known, and the applicant does not believe that such is the case here. In particular, the applicant asserts that the noticed facts are not considered to be common knowledge or well-known in the art because they are in areas of esoteric technology and relate to specific knowledge of the prior art, and must be supported.
>
> If the examiner continues to believe that the above-recited features are well known in the art, the applicant respectfully requests that the examiner provide a reference or references in the next office action allegedly offering evidence that this is the case.

In response the Examiner would refer applicant to:

2004/0177216: paragraph [0015]: storing the reference table in RAM reduces access latency.

6,725,312: column 7, lines 30-45: storing address translation entries in a temporary memory such as an SRAM improves address translation speed.

2006/0020747: paragraphs [0018] and [0022]: storing address translation data in a RAM avoids the overhead associated with updating the translation data on flash, thereby reducing the amount of wear incurred by the flash memory.

Therefore, it is clear that the practice of caching the translation data on a RAM is well-known in the art and is advantageous based on the known operating properties of flash and RAM memories.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject

matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-12 and 14 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (**U.S. Patent Application Publication #2006/0020744**) in view of Rajan (**U.S. Patent Application Publication #2009/0248763**).

1. Sinclair discloses A method for managing data in a block-based NAND flash storage system **(see [0030], flash memory system)**, the method comprising: a host processor **(see [0038], an application is executing on the host, implying that a processor is present to allow for execution of an application)**, deleting a file **(see [0036], file is deleted)**, *and issuing an empty-block directive including a block identifier (see Rajan below)*; and a NAND controller **(see [0038], flash memory controller)**, *receiving the empty-block directive (see Rajan below)*, and updating a table mapping logical identifiers to physical NAND flash storage locations, wherein the table is updated to indicate that data stored in one or more physical NAND flash storage locations associated with the block identifier do not need to be preserved **(see [0038], storage controller performs logical to physical mapping, [0047], new data is written to a different location which would involve updating mapping data, [0048], data that is deleted is marked as deallocated)**.

Sinclair fails to disclose issuing an empty-block directive including a block identifier and receiving the empty-block directive. Sinclair does disclose that FAT information is stored on the flash memory **(see [0042])**. When the application deletes a file, the FAT information is updated to indicate that the entry is deleted **(see [0036])**. It could be fair to interpret this change to the FAT as the empty-block directive, since the command would need to be sent to the flash memory controller as the FAT is on the

flash memory. However, this is not an explicit command to delete data, and therefore a secondary reference is being introduced to fully teach the empty-block directives.

Rajan discloses issuing an empty-block directive including a block identifier and receiving the empty-block directive **(see [0053])**. Notifying the storage system of data that is no longer in use prevents excess storage allocation **(see [0012])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the teachings of Sinclair to allow the application to send an empty-block directive to prevent excess storage allocation, as taught by Rajan.

4. The method of claim 1, *wherein at least a part of the table is maintained in volatile memory (see below)*.

Sinclair and Rajan do not explicitly disclose that tat least part of the table is maintained in volatile memory. Sinclair does utilize flash, and the translations are stored on the flash memory **(see [0042])**. It is well-known in the art that repeated write and erase operations will increase the wear of a flash memory leasing to a shorter life span. Volatile memory, such as DRAM, also provides faster access. Having translation tables stored in volatile memory allows for faster access while also limiting the wear of the flash memory, and Official Notice is hereby taken.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the teachings of Sinclair and Rajan to store at least part of the table in volatile memory to provide faster access and reduce wear on the flash memory.

5. The method of claim 1, wherein the empty-block directive issued by the host processor further comprises an indication that data stored in the one or more physical NAND flash storage locations associated with the block identifier should be overwritten **(see Sinclair [0052], unallocated data is not copied, and would be overwritten after the block is erase and returned as a free block; Sinclair already discloses providing an indication that clusters are deallocated, and therefore can be overwritten; based on the above combination with Rajan, this information would be part of an empty block directive as a result of the combination of Sinclair and Rajan)**.

6. The method of claim 1, wherein the empty-block directive is part of a block storage protocol **(see Sinclair [0030], the system is communicating with a block based memory, so it can be interpreted as having a block storage protocol; Rajan discloses the empty block directive as explained above; a combination of Sinclair and Rajan would result in the empty block directive being sent via the existing infrastructure disclosed by Sinclair)**.

7. The method of claim 1, wherein the empty-block directive is issued at an application programming interface of the host processor **(see Sinclair [0038], host interfaces with the memory controller through an application; Rajan discloses the empty block directive as explained above; a combination of Sinclair and Rajan would result in the empty block directive being sent via the existing infrastructure disclosed by Sinclair)**.

8. The method of claim 1, wherein the empty-block directive is issued by a file system of the host processor **(see Sinclair [0036], file system indicates data that is**

deleted; Rajan discloses the empty block directive as explained above; a combination of Sinclair and Rajan would result in the empty block directive being sent via the existing infrastructure disclosed by Sinclair).

9. The method of claim 1, wherein the empty-block directive is issued by a storage client of the host processor **(see Sinclair [0038], host application; Rajan discloses the empty block directive as explained above; a combination of Sinclair and Rajan would result in the empty block directive being sent via the existing infrastructure disclosed by Sinclair)**.

10. The method of claim 1, further comprising the NAND controller performing garbage collection in the NAND flash storage system **(see Sinclair [0052])**.

11. The method of claim 10, wherein performing garbage collection comprises the NAND controller: copying a block containing data that should be preserved from an erase block comprising blocks containing data that does not need to be preserved; and erasing the erase block **(see Sinclair [0052])**.

12. The method of claim 11, further comprising the NAND controller writing data to the erased erase block **(see Sinclair [0004], the purpose of erasing a block is to allow new data to be written to the block)**.

14. The method of claim 1, wherein each of the one or more physical NAND flash storage locations are smaller than a NAND flash erase block **(see Sinclair [0004])**.

Claims 2-3 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (**U.S. Patent Application Publication #2006/0020744**) and Rajan (**U.S. Patent Application Publication #2009/0248763**) as applied to claims 1, 4-12 and 14

above, and further in view of Adelmann (**U.S. Patent Application Publication #2004/0003002**).

2. The method of claim 1 **(see Sinclair and Rajan above)**, *wherein responsive to receiving a read command including the block identifier from the host processor, the NAND controller returns a data string comprising data bits with a predetermined logic level (see Adelmann below).*

Sinclair and Rajan fail to disclose responsive to receiving a read command including the block identifier from the host processor, the NAND controller returns a data string comprising data bits with a predetermined logic level.

Adelmann discloses responsive to receiving a read command including the block identifier from the host processor, the NAND controller returns a data string comprising data bits with a predetermined logic level **(see [0039] and [0043], the user can access the file and be provided with additional details about the file, such as when the file was deleted)**. This allows the user to more intelligently manage large numbers of files by being able to accurately track when files are created, modified and deleted **(see [0003])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have to modify the teachings of Sinclair and Rajan to return predetermined data when reading a deleted file so that a user can accurately determine the status of a file, as taught by Adelmann.

3. The method of claim 2, wherein the predetermined logic level is zero **(see Rajan [0031], all data that is transferred over a bus is comprised of bits with logic level zero or logic level one. Therefore, depending on the data that is sent, the**

string could comprise all zero's, all one's or a mix of one's and zero's. The ability to send all zero's is within the operating parameters of the system).

Claim 13 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (**U.S. Patent Application Publication #2006/0020744**) and Rajan (**U.S. Patent Application Publication #2009/0248763**) as applied to claims 1, 4-12 and 14 above, and further in view of "A New Flash Memory Management for Flash Storage System", hereinafter referred to as NPL1.

13. The method of claim 1 **(see Sinclair and Rajan above)**, *wherein the NAND flash storage system is an append-only storage system (see NPL1 below)*.

Sinclair and Rajan fail to disclose wherein the NAND flash storage system is an append-only storage system.

NPL1 discloses wherein the NAND flash storage system is an append-only storage system **(see section 2 "Flash Memory Management)**. Append only writing provides a positive of effect of cycle-leveling **(see section 2 "Flash Memory Management)**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the teachings of Sinclair and Rajan to use an append only system to provide even wear leveling of the flash memory, as taught by NPL1.

Claims 15-20 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (**U.S. Patent Application Publication #2006/0020744**) in

view of Rajan (**U.S. Patent Application Publication #2009/0248763**) and Adelmann (**U.S. Patent Application Publication #2004/0003002**).

15. Sinclair discloses A method for managing data in a NAND flash storage system **(see [0030], flash memory)**, the method comprising: *receiving an empty-block directive at a storage controller, the empty block directive including a logical identifier associated with a physical storage location (see Rajan below)* comprising data deleted by a host **(see [0036], file is deleted)**; *and returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty block directive (see Adelmann below).*

Sinclair fails to disclose receiving an empty-block directive at a storage controller, the empty block directive including a logical identifier associated with a physical storage location comprising data deleted by a host. Sinclair does disclose that FAT information is stored on the flash memory **(see [0042])**. When the application deletes a file, the FAT information is updated to indicate that the entry is deleted **(see [0036])**. It could be fair to interpret this change to the FAT as the empty-block directive, since the command would need to be sent to the flash memory controller as the FAT is on the flash memory. However, this is not an explicit command to delete data, and therefore a secondary reference is being introduced to fully teach the empty-block directives.

Rajan discloses receiving an empty-block directive at a storage controller, the empty block directive including a logical identifier associated with a physical storage location comprising data deleted by a host **(see [0053])**. Notifying the storage system of data that is no longer in use prevents excess storage allocation **(see [0012])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the teachings of Sinclair to allow the application to send an empty-block directive to prevent excess storage allocation, as taught by Rajan.

Sinclair fails to disclose returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty block directive.

Adelmann discloses returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty block directive **(see [0039] and [0043], the user can access the file and be provided with additional details about the file, such as when the file was deleted)**. This allows the user to more intelligently manage large numbers of files by being able to accurately track when files are created, modified and deleted **(see [0003])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have to modify the teachings of Sinclair and Rajan to return predetermined data when reading a deleted file so that a user can accurately determine the status of a file, as taught by Adelmann.

16. The method of claim 15, wherein the predetermined logic level is zero **(see Rajan [0031], all data that is transferred over a bus is comprised of bits with logic level zero or logic level one. Therefore, depending on the data that is sent, the string could comprise all zero's, all one's or a mix of one's and zero's. The ability to send all zero's is within the operating parameters of the system)**.

17. The method of claim 15, further comprising: determining that the empty-block directive further includes an indication that data associated with the logical identifier should be overwritten; and overwriting the data associated with the logical identifier **(see Sinclair [0052], unallocated data is not copied, and would be overwritten after the block is erase and returned as a free block)**.

18. The method of claim 15, wherein the empty-block directive is part of a block storage protocol **(see Sinclair [0030], the system is communicating with a block based memory, so it can be interpreted as having a block storage protocol)**.

19. The method of claim 15, wherein the empty-block directive is received through an application programming interface **(see Sinclair [0038], host interfaces with the memory controller through an application)**.

20. The method of claim 15, wherein the empty-block directive is received from a file system **(see Sinclair [0036], file system indicates data that is deleted)**.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWARD J DUDEK JR whose telephone number is (571)270-1030. The examiner can normally be reached on Monday - Friday, 8:00A-4:00P.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Rones can be reached on 571-272-4085. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access

to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EDWARD J DUDEK JR/
Primary Examiner, Art Unit 2136

REMARKS/ARGUMENTS

Claims 1-20 are currently pending in the application. Claims 1-20 have been rejected. Claims 1-14 have been cancelled. Claims 21-34 have been added. Claim 15 has been amended. The following remarks are believed to be fully responsive to the outstanding office action. The examiner is respectfully requested to withdraw the rejections in view of the present amendments and remarks.

1. 35 U.S.C. § 103 Rejections

Claims 1, 4-12 and 14 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent Pub. No. 2006/0020744 to Sinclair (the "Sinclair reference") in view of U.S. Patent Pub. No. 2009/0248763 to Rajan (the "Rajan reference").

Claims 2 and 3 stand rejected under 35 U.S.C. § 103 as being unpatentable over the Sinclair reference in view of the Rajan reference and in further view of U.S. Patent Pub. No. 2001/0003002 to Adelmann (the "Adelmann reference").

Claim 13 stands rejected under 35 U.S.C. § 103 as being unpatentable over the Sinclair reference in view of the Rajan reference and in further view of "A New Flash Memory Management for Flash Storage System."

Claims 15-20 stand rejected under 35 U.S.C. § 103 as being unpatentable over the Sinclair reference in view of the Rajan reference and in further view of the Adelmann reference.

Under the rationale used to reject the claims, the prior art references when modified must still teach or suggest all the claim limitations of the rejected claims. The applicant submits that, in light of the current amendments, the claimed elements and limitations are not disclosed by the references nor can they be modified to arrive at the claimed invention and the rejections should be withdrawn.

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The references fail to disclose a table that indicates that data stored in a storage location is currently preserved but does not need to be preserved.

Claim 15, as amended, expressly requires "maintaining a table mapping the logical identifier to the physical storage location, wherein the table indicates that the contents of the physical storage location *are currently preserved* but do not need to be preserved." Similarly, new claim 21 expressly requires "wherein the table is updated to indicate that data stored in one or more physical NAND flash storage locations associated with the empty-block identifier *is currently preserved* but do not need to be preserved." The applicant asserts the Sinclair reference teaches that "if it is determined (616) that one or more clusters have been deallocated, the status of the one or more clusters in a Data Allocation Table (DAT) is changed to indicate a "deallocated" status." (paragraph 0048). In other words, the Sinclair reference teaches that the table is updated to indicate data that has already been deallocated (i.e., that a deallocation has already happened *in the past*). There is nothing in the Sinclair reference that teaches that the table indicates data that is currently preserved does not need to be preserved (i.e., referring to a preservation of the data *in the future*). The office action dated January 27, 2021 further confirmed this fact and admits that "the status of the cluster will be recorded in the DAT to indicate it has been deallocated." (page 3 of the office action).

The applicant asserts the references, either alone or combination, fail to teach a table that indicates data in a storage location is currently preserved but does not need to be preserved, as claimed. Therefore, the applicant submits the 35 U.S.C. § 103 rejection should be withdrawn. Inasmuch as claims 16-20 and 22-34 depend from and include the limitations of independent claims 15 and 21, the rejections should also be withdrawn.

CONCLUSION

In view of the foregoing, it is believed that all of the pending claims are in condition for allowance. The applicant therefore requests that the examiner withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding office action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is requested. If the examiner believes that a telephone conference would be useful in moving the application toward allowance, the examiner is encouraged to contact the attorney of record.

Respectfully submitted,

Date: April 27, 2021

/David Wade Schnell/
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Amendments to the Claims

1. – 14. (Canceled)

15. (Currently amended) A method for managing data in a NAND flash storage system, the method comprising:

receiving an empty-block directive at a storage controller, the ~~empty block~~ empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host; ~~and~~

returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the ~~empty block~~ empty-block directive; and

maintaining a table mapping the logical identifier to the physical storage location, wherein the table indicates that the contents of the physical storage location are currently preserved but do not need to be preserved.

16. (Previously presented) The method of claim 15, wherein the predetermined logic level is zero.

17. (Previously presented) The method of claim 15, further comprising:

determining that the empty-block directive further includes an indication that data associated with the logical identifier should be overwritten; and

overwriting the data associated with the logical identifier.

18. (Previously presented) The method of claim 15, wherein the empty-block directive is part of a block storage protocol.

19. (Previously presented) The method of claim 15, wherein the empty-block directive is received through an application programming interface.

20. (Previously presented) The method of claim 15, wherein the empty-block directive is received from a file system.

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21. (New) A method for managing data in a system having a processor and a block-based NAND flash storage system, the NAND flash storage system having physical NAND flash storage locations controlled by a NAND controller, the method comprising:

receiving, via the processor, an indication of deletion of a file in a first location;

creating, via the processor, an empty-block identifier in response to the indication of deletion;

receiving, via the NAND controller, the empty-block identifier; and

updating, via the NAND controller, a table mapping logical identifiers to physical NAND flash storage locations, wherein the table is updated to indicate that data stored in one or more physical NAND flash storage locations associated with the empty-block identifier is currently preserved but do not need to be preserved.

22. (New) The method of claim 21, further comprising:

receiving a read command including the block identifier from the host processor; and returning, via the NAND controller, a data string comprising data bits with a predetermined logic level in response to receiving the read command.

23. (New) The method of claim 22, wherein the predetermined logic level is zero.

24. (New) The method of claim 21, wherein at least a part of the table is maintained in volatile memory.

25. (New) The method of claim 21, wherein the empty-block identifier issued by the host processor indicates that data stored in the one or more physical NAND flash storage locations associated with the empty-block identifier should be overwritten.

26. (New) The method of claim 21, further comprising transmitting a message indicating that the data stored in one or more physical NAND flash storage locations has been overwritten.

27. (New) The method of claim 21, further comprising overwriting data stored in the one or more physical NAND flash storage locations with a series of characters such that the overwritten data is non-recoverable.

28. (New) The method of claim 21, further comprising performing garbage collection, via the NAND controller, in the NAND flash storage system.

29. (New) The method of claim 28, wherein performing garbage collection comprises:
copying a block containing data that should be preserved from an erase block comprising blocks containing data that does not need to be preserved; and
erasing the erase block.

30. (New) The method of claim 29, further comprising writing data, via the NAND controller, to the erased erase block.

31. (New) The method of claim 21, wherein the NAND flash storage system is an append-only storage system.

32. (New) The method of claim 21, wherein each of the one or more physical NAND flash storage locations are smaller than a NAND flash erase block.

33. (New) The method of claim 15, further comprising transmitting a message indicating that the data in the physical storage location has been deleted in response to a delete command.

34. (New) The method of claim 15, further comprising overwriting data stored in the physical storage location with a series of characters such that the overwritten data is non-recoverable.

Silicon Motion - Exhibit 1014
Silicon Motion v. UTL - IPR2024-00199
Page 190 of 382

PTO/SB/06 (09-11)
Approved for use through 1/31/2014, OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/543,464	Filing Date 08/16/2019	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	04/27/2021	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/JESSICA T GAYNOR/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/543,464	08/16/2019	David Flynn	10788.0722	4625

175872 7590 05/19/2021

The Noblitt Group, PLLC
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8777 NORTH GAINEY CENTER DRIVE, STE.175
Scottsdale, AZ 85258

EXAMINER	
DUDEK JR, EDWARD J	

ART UNIT	PAPER NUMBER
2136	

NOTIFICATION DATE	DELIVERY MODE
05/19/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@ngtechlaw.com
dwschnell@ngtechlaw.com

Office Action Summary	Application No. 16/543,464	Applicant(s) Flynn et al.	
	Examiner EDWARD J DUDEK JR	Art Unit 2136	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 27 April 2021.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 15-34 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 15-34 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

This Office Action is responsive to the request for continued examination filed 27 April 2021.

Claims 15-34 are pending and have been presented for examination.

Claims 1-14 have been cancelled.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 27 April 2021 has been entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 15-34 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-AIA 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 15 contains the limitation "… wherein the table indicates that the contents of the physical storage location are currently preserved but do not need to be preserved." The specification does not provide support for this limitation. Paragraphs [0012]-[0020] discuss receiving a hint or identifier to specific that data associated with a logical identifier does not need to be preserved. The section also states that the message could mark a data packet as invalid. The Examiner does not find support in the specification for an indication that the contents are currently preserved but do not need to be preserved. Marking a location as containing data that does not need to be preserved doesn't imply that the data is currently preserved. Prior to any garbage the data may still exist on the storage device, however, there is nothing in the specification that disclosed any indication that the data is still being preserved.

Claim 21 contains similar limitations to claim 15 and is rejected for the same reasons set forth for claim 15.

Claims 16-20 and 22-34 are rejected as they depend from either claims 15 or 21 and fail to resolve the issued identified above for claims 15 and 21.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWARD J DUDEK JR whose telephone number is (571)270-1030. The examiner can normally be reached on Monday - Friday, 8:00A-4:00P.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Rones can be reached on 571-272-4085. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EDWARD J DUDEK JR/
Primary Examiner, Art Unit 2136

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT

Inventor:	David Flynn	Docket No.:	10788.0722
Serial No.:	16/543,464	Examiner:	Edward J. Dudek Jr.
Filing Date:	August 16, 2019	Art Unit:	2136
Title:	Systems and Methods for Identifying Storage Resources That Are Not In Use	Conf. No. :	4625

RESPONSE TO OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Commissioner:

The following submission is made in response to the office action mailed May 19, 2021.

Remarks/Arguments begin on page 2 of this paper.

REMARKS/ARGUMENTS

Claims 15-34 are currently pending in the application. Claims 15-34 have been rejected. The following remarks are believed to be fully responsive to the outstanding office action. The examiner is respectfully requested to withdraw the rejections in view of the present amendments and remarks.

1. 35 U.S.C. § 112 Rejections

Claims 17-20 are rejected under 35 U.S.C. 112(a) first paragraph for failing to comply with the written description requirement. In particular, the office action asserts that the claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor had possession of the claimed invention. The office action submits that the limitation "wherein the table indicates that the contents of the physical storage location are currently preserved but do not need to be preserved" is not supported by the specification. The applicant respectfully disagrees and asserts that at least paragraphs [0016]-[0022], [0078]-[0082], [0204]-[0206], and [0236] of the applicant's specification, when considered together and in light of the entire specification, support the limitation.

The office action further submits that "[m]arking a location as containing data that does not need to be preserved doesn't imply that the data is currently preserved." The applicant does not concede this statement, and the applicant submits that the claim language is directed to *a table* that indicates contents of a physical storage location. The claim does not use the term "mark" or "marking." As such, the applicant submits that the statement by the office action is irrelevant.

The office action further submits that "[p]rior to any garbage the data may still exist on the storage device, however, there is nothing in the specification that disclosed any indication

that the data is still being preserved." Again, the applicant does not concede this statement, and the applicant submits that the claim language is directed to *a table* that indicates contents of a physical storage location. As such, the applicant submits that the statement by the office action is irrelevant.

CONCLUSION

In view of the foregoing, it is believed that all of the pending claims are in condition for allowance. The applicant therefore requests that the examiner withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding office action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is requested. If the examiner believes that a telephone conference would be useful in moving the application toward allowance, the examiner is encouraged to contact the attorney of record.

Respectfully submitted,

Date: June 15, 2021

/David Wade Schnell/
David Wade Schnell
Reg. No. 53,563

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Facsimile: 480.994.9025

Electronic Acknowledgement Receipt

EFS ID:	42994547
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	175872
Filer:	David Wade Schnell/Sally Hartway
Filer Authorized By:	David Wade Schnell
Attorney Docket Number:	10788.0722
Receipt Date:	15-JUN-2021
Filing Date:	16-AUG-2019
Time Stamp:	17:08:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		107880722_2021-06-15_RNFOA_2021-05-19.pdf	133919 d411c05dae40bc608acfa3bc77e7e06af36dfe5e	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Applicant Arguments/Remarks Made in an Amendment	2	3
Warnings:			
Information:			
	Total Files Size (in bytes):	133919	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/543,464	08/16/2019	David Flynn	10788.0722	4625

175872 7590 08/27/2021

NOBLITT & NEWSON, PLLC (Acacia)
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Scottsdale, AZ 85258

EXAMINER	
DUDEK JR, EDWARD J	

ART UNIT	PAPER NUMBER
2136	

NOTIFICATION DATE	DELIVERY MODE
08/27/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@ngtechlaw.com
dwschnell@ngtechlaw.com

Office Action Summary	Application No. 16/543,464	Applicant(s) Flynn et al.	
	Examiner EDWARD J DUDEK JR	Art Unit 2136	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 15 June 2021.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 15-34 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 15-34 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

This Office Action is responsive to the reply filed 15 June 2021.

Claims 15-34 are pending and have been presented for examination.

Claims 1-14 have been cancelled.

Response to Arguments

Applicant's arguments filed 15 June 2021 have been fully considered but they are not persuasive.

Applicant argues (see pages 2-3):

> The office action further submits that "[m]arking a location as containing data that does not need to be preserved doesn't imply that the data is currently preserved." The applicant does not concede this statement, and the applicant submits that the claim language is directed to a table that indicates contents of a physical storage location. The claim does not use the term "mark" or "marking." As such, the applicant submits that the statement by the office action is irrelevant.
>
> The office action further submits that "[p]rior to any garbage the data may still exist on the storage device, however, there is nothing in the specification that disclosed any indication that the data is still being preserved." Again, the applicant does not concede this statement, and the applicant submits that the claim language is directed to a table that indicates contents of a physical storage location. As such, the applicant submits that the statement by the office action is irrelevant.

The Examiner respectfully disagrees. A dictionary definition of the term mark shows that a mark is something that can be used to provide an indication. In context it is clear the Examiner was using the term mark as a way to show an indication. While the claim does not use the term mark, it should be clear that the Examiner was conveying that the specification does not provide support for a table that provides an indication that data is currently preserved, but does not need to be preserved. Also, applicant's specification uses the term marking module when referring to the table for tracking locations of data on the storage device. The Applicant has provided multiple citations to the specification as support for the claimed limitation of "… table indicates that the contents of the physical storage location are currently preserved but do not need to be preserved." The Examiner does not believe these citations support this limitation of the claim. Looking at [0016]-[0022]: this section seems to be the most relevant. Here, the specification discusses a marking module to record that data can be erased, invalidating a mapping between a logical identifier and physical address, mark a data packet at the physical address as invalid, etc. This clearly supports an identification that contents as a physical location do not need to be preserved. However, there does not appear to be any indications that would convey that the contents are currently preserved as well. The claim states a table that indicates the contents of the physical location are currently preserved but do not need to be preserved. Per the discussion in paragraphs [0016]-[0022], there are plenty of details that show an indication that data does not need to be preserved. For example, invalidating a mapping. However, there are no details to show what indication in a table

conveys that the data is currently preserved as well. For example, when the mapping is invalidated it is clear this data does not need to be preserved. But it is not clear if this data is still being maintained. Looking at [0078]-[0082]: this section discusses parsing an object request and adding an object entry into an index. This does not appear relevant to the claimed limitation "… table indicates that the contents of the physical storage location are currently preserved but do not need to be preserved." Looking at [0204]-[0206]: this section discusses routing data to the memory and the mapping of erase blocks. This does not appear relevant to the claimed limitation "… table indicates that the contents of the physical storage location are currently preserved but do not need to be preserved." Looking at [0236]: this section discusses sequential writing of a data packet. This does not appear relevant to the claimed limitation "… table indicates that the contents of the physical storage location are currently preserved but do not need to be preserved."

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 15-34 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-AIA 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 15 contains the limitation "… wherein the table indicates that the contents of the physical storage location are currently preserved but do not need to be preserved." The specification does not provide support for this limitation. Paragraphs [0012]-[0020] discuss receiving a hint or identifier to specific that data associated with a logical identifier does not need to be preserved. The section also states that the message could mark a data packet as invalid. The Examiner does not find support in the specification for an indication that the contents are currently preserved but do not need to be preserved. Marking a location as containing data that does not need to be preserved doesn't imply that the data is currently preserved. Prior to any garbage the data may still exist on the storage device, however, there is nothing in the specification that disclosed any indication that the data is still being preserved.

Claim 21 contains similar limitations to claim 15 and is rejected for the same reasons set forth for claim 15.

Claims 16-20 and 22-34 are rejected as they depend from either claims 15 or 21 and fail to resolve the issued identified above for claims 15 and 21.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWARD J DUDEK JR whose telephone number is (571)270-1030. The examiner can normally be reached on Monday - Friday, 8:00A-4:00P.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Rones can be reached on 571-272-4085. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EDWARD J DUDEK JR/
Primary Examiner, Art Unit 2136

Electronic Acknowledgement Receipt

EFS ID:	44141184
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	175872
Filer:	David Wade Schnell/Sally Hartway
Filer Authorized By:	David Wade Schnell
Attorney Docket Number:	10788.0722
Receipt Date:	27-OCT-2021
Filing Date:	16-AUG-2019
Time Stamp:	17:55:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	107880722_2021-10-27_Sub_Stmt_Thatcher_signed.pdf	2297707 28f2da665a9b6197d2393aef1d4de7e0699 31924	no	3
Warnings:					

Information:					
2	Miscellaneous Incoming Letter	107880722_2021-10-27_Notice_Regarding_Declaration.pdf	51958 c7217594a4bd9ff4b6493e6e5b5a9524eb922463	no	1
Warnings:					
Information:					
			Total Files Size (in bytes):	2349665	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	16/543,464
Filing Date:	August 16, 2019
Applicant:	Unification Technologies LLC
Inventors:	David Flynn
Confirmation No.:	4625
Group Art Unit:	2136
Examiner:	Edward J. Dudek Jr.
Title:	Systems and Methods for Identifying Storage Resources That Are Not In Use
Attorney Docket:	10788.0722

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

RESPONSE TO FINAL OFFICE ACTION

In response to the Final Office Action mailed August 27, 2021, please enter the following the Amendments and Remarks set forth below.

Amendment to the Claims begin on page 2 of this paper

Remarks begin on page 7 of this paper.

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS

1– 14. (Canceled)

15. (Currently amended) A method for managing data in a NAND flash storage system, the method comprising:

receiving an empty-block directive at a storage controller, the empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host;

returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive; ~~and~~

maintaining ~~a table~~ an index of mapping between the logical identifier ~~to~~ and the physical storage location[[,]]; and

updating ~~wherein~~ the index to ~~table~~ indicate[[s]] that the contents of the physical storage location ~~are currently preserved but~~ do not need to be preserved.

16. (Previously presented) The method of claim 15, wherein the predetermined logic level is zero.

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17. (Previously presented) The method of claim 15, further comprising:

determining that the empty-block directive further includes an indication that data associated with the logical identifier should be overwritten; and

overwriting the data associated with the logical identifier.

18. (Previously presented) The method of claim 15, wherein the empty-block directive is part of a block storage protocol.

19. (Previously presented) The method of claim 15, wherein the empty-block directive is received through an application programming interface.

20. (Previously presented) The method of claim 15, wherein the empty-block directive is received from a file system.

21. (Currently amended) A method for managing data in a system having a processor and a block-based NAND flash storage system, the NAND flash storage system having physical NAND flash storage locations controlled by a NAND controller, the method comprising:

receiving, via the processor, an indication of deletion of a file in a first location;

creating, via the processor, an empty-block identifier in response to the indication of deletion;

receiving, via the NAND controller, the empty-block identifier; ~~and~~

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maintaining ~~updating~~, via the NAND controller, ~~a table~~ an index of mapping between logical identifiers ~~to~~ and physical NAND flash storage locations[[,]]; and

~~wherein~~ updating the index ~~table is updated~~ to indicate that data stored in one or more of the physical NAND flash storage locations associated with the empty-block identifier ~~is currently preserved but~~ does not need to be preserved.

22. (Currently amended) The method of claim 21, further comprising:

receiving a read command including the empty-block identifier from the host processor; and

returning, via the NAND controller, a data string comprising data bits with a predetermined logic level in response to receiving the read command.

23. (Previously presented) The method of claim 22, wherein the predetermined logic level is zero.

24. Canceled.

25. (Currently amended) The method of claim 21, wherein the empty-block identifier issued by the ~~host~~ processor indicates that data stored in the one or more physical NAND flash storage locations associated with the empty-block identifier should be overwritten.

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26. (Previously presented) The method of claim 21, further comprising transmitting a message indicating that the data stored in one or more physical NAND flash storage locations has been overwritten.

27. (Previously presented) The method of claim 21, further comprising overwriting data stored in the one or more physical NAND flash storage locations with a series of characters such that the overwritten data is non-recoverable.

28. (Previously presented) The method of claim 21, further comprising performing garbage collection, via the NAND controller, in the NAND flash storage system.

29. (Previously presented) The method of claim 28, wherein performing garbage collection comprises:

copying a block containing data that should be preserved from an erase block comprising blocks containing data that does not need to be preserved; and

erasing the erase block.

30. (Previously presented) The method of claim 29, further comprising writing data, via the NAND controller, to the erased erase block.

31. (Previously presented) The method of claim 21, wherein the NAND flash storage system is an append-only storage system.

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32. (Previously presented) The method of claim 21, wherein each of the one or more physical NAND flash storage locations are smaller than a NAND flash erase block.

33. (Previously presented) The method of claim 15, further comprising transmitting a message indicating that the data in the physical storage location has been deleted in response to a delete command.

34. (Previously presented) The method of claim 15, further comprising overwriting data stored in the physical storage location with a series of characters such that the overwritten data is non-recoverable.

35. (New) The method of claim 15, further comprising removing a mapping between the logical identifier and the physical storage location from the index.

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REMARKS

Claims 15-34 are currently pending. All claims were rejected in this Office Action. In response, Applicant has amended claims 15, 21-22, and 25. In addition, Applicant has canceled dependent claim 24, without prejudice or disclaimer. Finally, Applicant has added new claim 35, which is dependent on independent claim 15. The above Amendments and the following Remarks are believed to be fully responsive to the pending Office Action.

Rejections under 35 USC 112

Claims 15-34 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. According to the Office Action, the claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. This rejection is traversed.

In response, Applicant has amended independent claim 1 to state:

"maintaining ~~a table~~ an index of mapping between the logical identifier ~~to~~ and the physical storage location[[,]]; and updating ~~wherein~~ the index to ~~table~~ indicate[[s]] that the contents of the physical storage location ~~are currently preserved but~~ do not need to be preserved".

Support for these amendments can found throughout the pending application and especially in paragraph [0012]. For example, paragraph [0012] includes the following disclosure: "The methods may further comprise maintaining an index of mappings between

logical identifiers and physical storage locations, and that the contents of the physical storage location do not need to be preserved".

Applicant submits that independent claim 15, as amended, complies with the written description requirement, under 35 U.S.C. 112, first paragraph. Accordingly, pending claims 16-20, which are dependent on claim 15, comply with the written description requirement, under 35 U.S.C. 112, first paragraph.

Moving to independent claim 21, Applicant has amended this claim to state

"maintaining ~~updating~~, via the NAND controller, ~~a table~~ an index of mapping between logical identifiers ~~to~~ and physical NAND flash storage locations[[,]]; and ~~wherein~~ updating the index ~~table is updated~~ to indicate that data stored in one or more of the physical NAND flash storage locations associated with the empty-block identifier ~~is currently preserved but~~ does not need to be preserved". Support for these amendments can found throughout the pending application and especially in paragraphs [0010]-[0020].

Applicant submits that independent claim 21, as amended, complies with the written description requirement, under 35 U.S.C. 112, first paragraph. Accordingly, pending claims 22-23 and 25-34, which are dependent on claim 21, comply with the written description requirement, under 35 U.S.C. 112, first paragraph.

No new matter has been added by these claim amendments. Since all pending claims, as amended, comply with 35 U.S.C. 112, first paragraph, Applicant requests withdrawal of all 112 rejections and an allowance of the pending claims 15-13 and 25-34.

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Other Claim Amendments

Applicant has amended claims 22 and 25 to correct antecedent basis.

New Claim

Applicant has added new claim 35, which is dependent on independent claim 15. New claim 35 states: "The method of claim 15, further comprising removing a mapping between the logical identifier and the physical storage location from the index." Support for this new claim is found throughout the pending application and especially in paragraph [0012], which includes the following disclosure: "The methods may further comprise maintaining an index of mappings between logical identifiers and physical storage locations, and that the contents of the physical storage location do not need to be preserved may comprise removing a mapping between the logical identifier and the physical storage location from the index". New claim 35 adds no new matter. New claim 35 is within the scope of the presently claimed invention.

Applicant respectfully requests examination and allowance of new claim 35.

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CONCLUSION

In view of the foregoing, it is believed that all of the pending claims are in condition for allowance. The Applicant therefore requests that the Examiner withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Final Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this Response is requested. If the Examiner believes that a telephone conference would be useful in moving the application toward allowance, the Examiner is encouraged to contact the attorney of record.

Respectfully submitted,

Dated: October 27, 2021

By: /David Wade Schnell/___
David Wade Schnell
Reg. No. 53,563

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Electronic Acknowledgement Receipt

EFS ID:	44140618
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	175872
Filer:	David Wade Schnell/Sally Hartway
Filer Authorized By:	David Wade Schnell
Attorney Docket Number:	10788.0722
Receipt Date:	27-OCT-2021
Filing Date:	16-AUG-2019
Time Stamp:	17:13:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		107880722_2021-10-27_Response_to_Final_Office_Action.pdf	103792 2d86889853bb7beef07f91e79fe038701ba137ff	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Response After Final Action	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	10
Warnings:			
Information:			
	Total Files Size (in bytes):	103792	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	16/543,464
Filing Date:	August 16, 2019
Applicant:	Unification Technologies LLC
Inventors:	David Flynn
Confirmation No.:	4625
Group Art Unit:	2136
Examiner:	Edward J. Dudek Jr.
Title:	Systems and Methods for Identifying Storage Resources That Are Not In Use
Attorney Docket:	10788.0722

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

RESPONSE TO FINAL OFFICE ACTION

In response to the Final Office Action mailed August 27, 2021, please enter the following the Amendments and Remarks set forth below.

Amendment to the Claims begin on page 2 of this paper

Remarks begin on page 7 of this paper.

DO NOT ENTER: /E.J.D/

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	16543464	Filing Date	2019-08-16	Docket Number (if applicable)	10788.0722	Art Unit	2136
First Named Inventor	David Flynn			Examiner Name	Edward J. Dudek, Jr.		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☒ Consider the arguments in the Appeal Brief or Reply Brief previously filed on 2021-10-27
- ☐ Other _____

☐ Enclosed

- ☐ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☒ Other 2 month Extension of Time

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 502993

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/David Wade Schnell/	Date (YYYY-MM-DD)	2022-01-10
Name	David Wade Schnell	Registration Number	53563

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	16543464
Filing Date:	16-Aug-2019
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Filer:	David Wade Schnell/Sally Hartway
Attorney Docket Number:	10788.0722

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 2 months with $0 paid	1252	1	640	640
Miscellaneous:				
RCE- 2ND AND SUBSEQUENT REQUEST	1820	1	2000	2000
		Total in USD ($)		**2640**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/543,464	08/16/2019	David Flynn	10788.0722	4625

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EXAMINER	
DUDEK JR, EDWARD J	

ART UNIT	PAPER NUMBER
2136	

NOTIFICATION DATE	DELIVERY MODE
02/07/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@ngtechlaw.com
dwschnell@ngtechlaw.com

Office Action Summary	Application No. 16/543,464	Applicant(s) Flynn et al.	
	Examiner EDWARD J DUDEK JR	Art Unit 2136	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 10 January 2022.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 15-23 and 25-35 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 15-23 and 25-35 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

This Office Action is responsive to the request for continued examination filed 10 January 2022.

Claims 15-23 and 25-35 are pending and have been presented for examination.

Claims 1-14 and 24 have been cancelled.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 27 October 2021 has been entered.

Response to Arguments

Applicant's arguments, see pages 7-8, filed 27 October 2021, with respect to claims 15-34 have been fully considered and are persuasive. The rejection of claims 15-34 under 35 U.S.C. 112, first paragraph, has been withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 15-20 and 33 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over SINCLAIR (**U.S. Patent Application Publication #2006/0020744**) in view of RAJAN (**U.S. Patent Application Publication #2009/0248763**) and ADELMANN (**U.S. Patent Application Publication #2004/0003002**).

15. SINCLAIR discloses A method for managing data in a NAND flash storage system **(see [0030], flash memory system)**, the method comprising: *receiving an empty-block directive at a storage controller, the empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host (see RAJAN below); returning a data string comprising data of a predetermined*

logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive (see ADELMANN below); and maintaining an index of mapping between the logical identifier and the physical storage location **(see [0038]: flash controller maps the host logical address space into a physical address space on the flash memory)**; and updating the index to indicate that the contents of the physical storage location do not need to be preserved **(see [0038], storage controller performs logical to physical mapping, [0047], new data is written to a different location which would involve updating mapping data, [0048], data that is deleted is marked as deallocated, [0045]: data attribute store provides information about the portion of the data that is to be maintained, by identifying data to be maintained, the data that doesn't need to be maintained {preserved} is also identified)**.

SINCLAIR discloses an index for mapping logical identifiers from the host to physical memory locations, and also discloses a DAS (which is another index) for tracking various attributes of the host logical cluster allocations **(see [0038]-[0041])**. Clearly, SINCLAIR discloses the mapping and the indication that contents do not need to be preserved. However, this information is maintained in two tables rather than one. While the claim does not specifically claim a single index, the claim simply refers to "the index" and the Examiner will interpret this as one index. This is a matter of design choice. SINCLAIR already discloses all the elements of the claimed index. Implementing this index as a single structure, or multiple structures is up to the person implementing the system. "When there is a design need for market pressure to solve a problem and there are a finite number if identified, predictable solutions, a person of

ordinary skill has good reason to pursue the known options within his or her technical grasp." *KSR*, 82 USPQ2d at 1397.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have implemented the mapping and the DAS disclosed in SINCLAIR as a single table, as that is one solution, from a limited number of solutions, for storing all the attributes that are already being tracked by SINCLAIR.

SINCLAIR fails to disclose receiving an empty-block directive at a storage controller, the empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host.

RAJAN discloses receiving an empty-block directive at a storage controller, the empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host **(see [0053]: punch hole command that include a logical block address field)**. Notifying the storage system of data that is no longer in use prevents excess storage allocation **(see [0012])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by SINCLAIR to receive an empty block directive, as disclosed by RAJAN. One of ordinary skill in the art would have been motivated to make such a modification in order to prevent excess storage allocation for data that is no longer needed by the host, as taught by RAJAN. SINCLAIR and RAJAN are in the same field of endeavor as they are both directed to recovering storage space when data is deleted by a host.

SINCLAIR fails to disclose returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive.

ADELMANN discloses returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive **(see [0039] and [0043], the user can access the file and be provided with additional details about the file, such as when the file was deleted)**. This allows the user to more intelligently manage large numbers of files by being able to accurately track when files are created, modified and deleted **(see [0003])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by SINCLAIR to return data of a predetermined logic level, as disclosed by ADELMANN. One of ordinary skill in the art would have been motivated to make such a modification in order to allow the user to more intelligently manage large numbers of files, as taught by ADELMANN. SINCLAIR and ADELMANN are in the same field of endeavor as they are both directed to managing data deleted by a host.

16. The method of claim 15, wherein the predetermined logic level is zero **(see RAJAN [0031], all data that is transferred over a bus is comprised of bits with logic level zero or logic level one. Therefore, depending on the data that is sent, the string could comprise all zero's, all one's or a mix of one's and zero's. The ability to send all zero's is within the operating parameters of the system)**.

17. The method of claim 15, further comprising: determining that the empty-block directive further includes an indication that data associated with the logical identifier should be overwritten; and overwriting the data associated with the logical identifier **(see SINCLAIR [0052], unallocated data is not copied, and would be overwritten after the block is erase and returned as a free block)**.

18. The method of claim 15, wherein the empty-block directive is part of a block storage protocol **(see SINCLAIR [0030], the system is communicating with a block based memory, so it can be interpreted as having a block storage protocol)**.

19. The method of claim 15, wherein the empty-block directive is received through an application programming interface **(see SINCLAIR [0038], host interfaces with the memory controller through an application)**.

20. The method of claim 15, wherein the empty-block directive is received from a file system **(see SINCLAIR [0036], file system indicates data that is deleted)**.

33. The method of claim 15, further comprising transmitting a message indicating that the data in the physical storage location has been deleted in response to a delete command **(see RAJAN [0056]: response from storage system that the punch hole command was successful)**.

Claims 21, 25, 28-30 and 32 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over SINCLAIR (**U.S. Patent Application Publication #2006/0020744**) in view of RAJAN (**U.S. Patent Application Publication #2009/0248763**).

21. SINCLAIR discloses A method for managing data in a system having a processor **(see [0030]: a host accesses the flash memory, the host would have a processor; [0059]: computer code designed to be executed by a computer, a processor would be necessary to execute the code)** and a block-based NAND flash storage system **(see [0030]: flash memory is a block based storage)**, the NAND flash storage system having physical NAND flash storage locations controlled by a NAND controller **(see [0002]-[0003]: controller that manages the physical memory arrays)**, the method comprising: *receiving, via the processor, an indication of deletion of a file in a first location; creating, via the processor, an empty-block identifier in response to the indication of deletion; receiving, via the NAND controller, the empty-block identifier (see RAJAN below)*; and maintaining, via the NAND controller, an index of mapping between logical identifiers and physical NAND flash storage locations **(see [0038]: flash controller maps the host logical address space into a physical address space on the flash memory)**; and updating the index to indicate that data stored in one or more of the physical NAND flash storage locations associated with the empty-block identifier does not need to be preserved **(see [0038], storage controller performs logical to physical mapping, [0047], new data is written to a different location which would involve updating mapping data, [0048], data that is deleted**

is marked as deallocated, [0045]: data attribute store provides information about the portion of the data that is to be maintained, by identifying data to be maintained, the data that doesn't need to be maintained {preserved} is also identified).

SINCLAIR fails to disclose receiving, via the processor, an indication of deletion of a file in a first location; creating, via the processor, an empty-block identifier in response to the indication of deletion; receiving, via the NAND controller, the empty-block identifier.

RAJAN discloses receiving, via the processor, an indication of deletion of a file in a first location **(see [0052]: generation of a punch hold command by agent for data that is no longer needed {which includes deletion of data})**; creating, via the processor, an empty-block identifier in response to the indication of deletion; receiving, via the NAND controller, the empty-block identifier **(see [0053]: punch hole command that include a logical block address field)**. Notifying the storage system of data that is no longer in use prevents excess storage allocation **(see [0012])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by SINCLAIR to receive an empty block directive, as disclosed by RAJAN. One of ordinary skill in the art would have been motivated to make such a modification in order to prevent excess storage allocation for data that is no longer needed by the host, as taught by RAJAN. SINCLAIR and RAJAN are in the same field of endeavor as they are both directed to recovering storage space when data is deleted by a host.

25. The method of claim 21, wherein the empty-block identifier issued by the processor indicates that data stored in the one or more physical NAND flash storage locations associated with the empty-block identifier should be overwritten **(see SINCLAIR [0052], unallocated data is not copied, and would be overwritten after the block is erase and returned as a free block)**.

28. The method of claim 21, further comprising performing garbage collection, via the NAND controller, in the NAND flash storage system **(see SINCLAIR [0033]: DAS is used during garbage collection)**.

29. The method of claim 28, wherein performing garbage collection comprises: copying a block containing data that should be preserved from an erase block comprising blocks containing data that does not need to be preserved; and erasing the erase block **(see SINCLAIR [0035]: clusters that are being used are copied, clusters that are not being used are not copied)**.

30. The method of claim 29, further comprising writing data, via the NAND controller, to the erased erase block **(see SINCLAIR [0011]: when blocks are erased they are returned to a pool to available memory blocks so that data can be written to the block, in the future the block will be written to again)**.

32. The method of claim 21, wherein each of the one or more physical NAND flash storage locations are smaller than a NAND flash erase block **(see SINCLAIR [0041]: portions of a cluster can be tracked)**.

Claims 22-23 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over SINCLAIR (**U.S. Patent Application Publication #2006/0020744**) and RAJAN (**U.S. Patent Application Publication #2009/0248763**) as applied to claims 21, 25, 28-30 and 32 above, and further in view of ADELMANN (**U.S. Patent Application Publication #2004/0003002**).

22. The method of claim 21 **(see SINCLAIR above)**, further comprising: *receiving a read command including the empty-block identifier from the host processor; and returning, via the NAND controller, a data string comprising data bits with a predetermined logic level in response to receiving the read command (see ADELMANN below).*

SINCLAIR fails to disclose receiving a read command including the empty-block identifier from the host processor; and returning, via the NAND controller, a data string comprising data bits with a predetermined logic level in response to receiving the read command.

ADELMANN discloses receiving a read command including the empty-block identifier from the host processor; and returning, via the NAND controller, a data string comprising data bits with a predetermined logic level in response to receiving the read command **(see [0039] and [0043], the user can access the file and be provided with**

additional details about the file, such as when the file was deleted). This allows the user to more intelligently manage large numbers of files by being able to accurately track when files are created, modified and deleted **(see [0003])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by SINCLAIR to return data of a predetermined logic level, as disclosed by ADELMANN. One of ordinary skill in the art would have been motivated to make such a modification in order to allow the user to more intelligently manage large numbers of files, as taught by ADELMANN. SINCLAIR and ADELMANN are in the same field of endeavor as they are both directed to managing data deleted by a host.

23. The method of claim 22, wherein the predetermined logic level is zero **(see RAJAN [0031], all data that is transferred over a bus is comprised of bits with logic level zero or logic level one. Therefore, depending on the data that is sent, the string could comprise all zero's, all one's or a mix of one's and zero's. The ability to send all zero's is within the operating parameters of the system)**.

Claims 26-27 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over SINCLAIR (**U.S. Patent Application Publication #2006/0020744**) and RAJAN (**U.S. Patent Application Publication #2009/0248763**) as applied to claims 21, 25, 28-30 and 32 above, and further in view of JENSEN (**U.S. Patent Application Publication #2006/0120235**).

26. The method of claim 21 **(see SINCLAIR above)**, *further comprising transmitting a message indicating that the data stored in one or more physical NAND flash storage locations has been overwritten (see JENSEN below).*

SINCLAIR fails to disclose transmitting a message indicating that the data stored in one or more physical NAND flash storage locations has been overwritten.

JENSEN discloses transmitting a message indicating that the data stored in one or more physical NAND flash storage locations has been overwritten **(see [0046]-[0050]: data locations that are subject to an erase command are overwritten, once the overwrite is complete a status signal is returned to the host)**. Overwriting data that was subject to an erase command is useful to protect personal or confidential data **(see [0004]-[0006])**.

27. The method of claim 21 **(see SINCLAIR above)**, *further comprising overwriting data stored in the one or more physical NAND flash storage locations with a series of characters such that the overwritten data is non-recoverable (see JENSEN below).*

SINCLAIR fails to disclose overwriting data stored in the one or more physical NAND flash storage locations with a series of characters such that the overwritten data is non-recoverable.

JENSEN discloses overwriting data stored in the one or more physical NAND flash storage locations with a series of characters such that the overwritten data is non-recoverable **(see [0046]-[0050]: data locations that are subject to an erase**

command are overwritten, once the overwrite is complete a status signal is returned to the host). Overwriting data that was subject to an erase command is useful to protect personal or confidential data **(see [0004]-[0006])**.

Claim 31 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over SINCLAIR (**U.S. Patent Application Publication #2006/0020744**) and RAJAN (**U.S. Patent Application Publication #2009/0248763**) as applied to claims 21, 25, 28-30 and 32 above, and further in view of "A New Flash Memory Management for Flash Storage System", hereinafter referred to as NPL1.

31. The method of claim 21 **(see SINCLAIR above)**, *wherein the NAND flash storage system is an append-only storage system (see NPL1 below)*.

SINCLAIR fails to disclose wherein the NAND flash storage system is an append-only storage system.

NPL1 discloses wherein the NAND flash storage system is an append-only storage system **(see section 2 "Flash Memory Management)**. Append only writing provides a positive of effect of cycle-leveling **(see section 2 "Flash Memory Management)**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by SINCLAIR to use an append only system, as disclosed by NPL1. One of ordinary skill in the art would have been motivated to make such a modification in order to provide even wear leveling

of the flash memory, as taught by NPL1. SINCLAIR and NPL1 are in the same field of endeavor as they are both directed to managing data on a storage system.

Claims 34 and 35 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over SINCLAIR (**U.S. Patent Application Publication #2006/0020744**), RAJAN (**U.S. Patent Application Publication #2009/0248763**) and ADELMANN (**U.S. Patent Application Publication #2004/0003002**) as applied to claims 15-20 and 33 above, and further in view of JENSEN (**U.S. Patent Application Publication #2006/0120235**).

34. The method of claim 15 **(see SINCLAIR above)**, *further comprising overwriting data stored in the physical storage location with a series of characters such that the overwritten data is non-recoverable (see JENSEN below).*

SINCLAIR fails to disclose overwriting data stored in the physical storage location with a series of characters such that the overwritten data is non-recoverable.

JENSEN discloses overwriting data stored in the physical storage location with a series of characters such that the overwritten data is non-recoverable **(see [0046]-[0050]: data locations that are subject to an erase command are overwritten, once the overwrite is complete a status signal is returned to the host)**. Overwriting data that was subject to an erase command is useful to protect personal or confidential data **(see [0004]-[0006])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by SINCLAIR to overwrite data stored in a physical location, as disclosed by JENSEN. One of ordinary skill in the art would have been motivated to make such a modification in order to protect personal or confidential data, as taught by JENSEN. SINCLAIR and JENSEN are in the same field of endeavor as they are both directed to managing data deleted by a host.

35. The method of claim 15 **(see SINCLAIR above)**, *further comprising removing a mapping between the logical identifier and the physical storage location from the index (see JENSEN below)*.

SINCLAIR fails to disclose removing a mapping between the logical identifier and the physical storage location from the index.

JENSEN discloses removing a mapping between the logical identifier and the physical storage location from the index **(see [0005]: one method for erasing data involves deleting a pointer that points to the data, this pointer would be the mapping between the logical and physical storage location)**. Removing this mapping would accomplish the goal of erasing the data and making the data inaccessible. Although it is not the most secure way of erasing data, it is one known method for doing so. “When there is a design need for market pressure to solve a problem and there are a finite number if identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *KSR*, 82 USPQ2d at 1397.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by SINCLAIR to remove the mapping, as disclosed by JENSEN. One of ordinary skill in the art would have been motivated to make such a modification in order to prevent data that was erased from being easily accessible, as taught by JENSEN. SINCLAIR and JENSEN are in the same field of endeavor as they are both directed to managing data that was deleted by a host.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWARD J DUDEK JR whose telephone number is (571)270-1030. The examiner can normally be reached Monday - Friday, 8:00A-4:00P.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Rones can be reached on 571-272-4085. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-

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Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EDWARD J DUDEK JR/
Primary Examiner, Art Unit 2136

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/543,464	Filing Date 08/16/2019	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	05/03/2022	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/BRENDA L TURNER/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	16/543,464
Filing Date:	August 16, 2019
Applicant:	Unification Technologies LLC
Inventors:	David Flynn
Confirmation No.:	4625
Group Art Unit:	2136
Examiner:	Edward J. Dudek Jr.
Title:	Systems and Methods for Identifying Storage Resources That Are Not In Use
Attorney Docket:	10788.0722

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

RESPONSE TO OFFICE ACTION

In response to the Office Action mailed February 7, 2022, please enter the following the Remarks set forth below.

Claims begin on page 2 of this paper

Remarks begin on page 6 of this paper.

CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

1– 14. (Canceled)

15. (Previously presented) A method for managing data in a NAND flash storage system, the method comprising:

receiving an empty-block directive at a storage controller, the empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host;

returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive;

maintaining an index of mapping between the logical identifier and the physical storage location; and

updating the index to indicate that the contents of the physical storage location do not need to be preserved.

16. (Previously presented) The method of claim 15, wherein the predetermined logic level is zero.

17. (Previously presented) The method of claim 15, further comprising:

determining that the empty-block directive further includes an indication that data associated with the logical identifier should be overwritten; and

overwriting the data associated with the logical identifier.

18. (Previously presented) The method of claim 15, wherein the empty-block directive is part of a block storage protocol.

19. (Previously presented) The method of claim 15, wherein the empty-block directive is received through an application programming interface.

20. (Previously presented) The method of claim 15, wherein the empty-block directive is received from a file system.

21. (Previously presented) A method for managing data in a system having a processor and a block-based NAND flash storage system, the NAND flash storage system having physical NAND flash storage locations controlled by a NAND controller, the method comprising:

receiving, via the processor, an indication of deletion of a file in a first location;

creating, via the processor, an empty-block identifier in response to the indication of deletion;

receiving, via the NAND controller, the empty-block identifier;

maintaining, via the NAND controller, an index of mapping between logical identifiers and physical NAND flash storage locations; and

updating the index to indicate that data stored in one or more of the physical NAND flash storage locations associated with the empty-block identifier does not need to be preserved.

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22. (Previously presented) The method of claim 21, further comprising:

receiving a read command including the empty-block identifier from the host processor; and

returning, via the NAND controller, a data string comprising data bits with a predetermined logic level in response to receiving the read command.

23. (Previously presented) The method of claim 22, wherein the predetermined logic level is zero.

24. Canceled.

25. (Previously presented) The method of claim 21, wherein the empty-block identifier issued by the processor indicates that data stored in the one or more physical NAND flash storage locations associated with the empty-block identifier should be overwritten.

26. (Previously presented) The method of claim 21, further comprising transmitting a message indicating that the data stored in one or more physical NAND flash storage locations has been overwritten.

27. (Previously presented) The method of claim 21, further comprising overwriting data stored in the one or more physical NAND flash storage locations with a series of characters such that the overwritten data is non-recoverable.

28. (Previously presented) The method of claim 21, further comprising performing garbage collection, via the NAND controller, in the NAND flash storage system.

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29. (Previously presented) The method of claim 28, wherein performing garbage collection comprises:

copying a block containing data that should be preserved from an erase block comprising blocks containing data that does not need to be preserved; and

erasing the erase block.

30. (Previously presented) The method of claim 29, further comprising writing data, via the NAND controller, to the erased erase block.

31. (Previously presented) The method of claim 21, wherein the NAND flash storage system is an append-only storage system.

32. (Previously presented) The method of claim 21, wherein each of the one or more physical NAND flash storage locations are smaller than a NAND flash erase block.

33. (Previously presented) The method of claim 15, further comprising transmitting a message indicating that the data in the physical storage location has been deleted in response to a delete command.

34. (Previously presented) The method of claim 15, further comprising overwriting data stored in the physical storage location with a series of characters such that the overwritten data is non-recoverable.

35. (Previously presented) The method of claim 15, further comprising removing a mapping between the logical identifier and the physical storage location from the index.

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REMARKS

Claims 15-23 and 25-35 are currently pending. All claims were rejected in this Office Action. The following Remarks are believed to be fully responsive to the pending Office Action.

Rejections under 35 USC 103

Claims 15-20 and 33 stand rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (US2006/0020744) in view of Rajan (US2009/0248763) and Adelmann (US2004/0003002).

These rejections are traversed. The cited references, individually or in combination, fail to teach, suggest, anticipate, or render obvious the combination of claim elements in dependent claim 15 and claims 16-20 and 33, dependent thereon. The examiner has failed to establish a *prima facie* basis for obviousness under 35 U.S.C. §103(a).

The Supreme Court decision *KSR v. Teleflex* held that any obviousness determination must be consistent with the traditional *Graham* factors. *KSR Intern. Co. v. Teleflex*, 550 U.S. 398, 416-17 (2007). Thus, obviousness is determined according to (1) the scope and content of the prior art, (2) the level of ordinary skill in the art, (3) the differences between the prior art and the claimed invention, and (4) the extent of any objective indicia of nonobviousness. *Graham v. John Deere Co. of Kansas City,* 383 U.S. 1, 148 USPQ 459 (1966).

In review of the rejections presented herein, the examiner is using impermissible hindsight reasoning to piece together an obviousness rejection using selected sentences

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from the cited references. According to MPEP 2142, "impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art".

Moreover, the examiner's rejections fail to meet the requirements of *KSR* and *Graham*. "In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences *themselves* would have been obvious, but whether the claimed invention *as a whole* would have been obvious." *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1537, 218 USPQ 871 (Fed. Cir. 1983) (emphasis added). As stated in *KSR*, the mere fact that references *can* be combined or modified does not render the resultant combination. *KSR*, 550 U.S. at 416-17.

It has also long been established that:

> It is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. *Eli Lilly and Co. v. Zenith Goldmine Pharm.*, 364 F.Supp.2d 820, 902 (S.D. Ind. 2005)(citing *In re Wesslau*, 353 F.2d 238, 241 (1965)).

Furthermore, "a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418.

In the rejections presented in this Office Action, the examiner picks and chooses elements from the references to build a case of obviousness and ignores teachings in these references that are contrary to the examiner's position. The examiner fails to fully appreciate what such reference fairly suggests to one of ordinary skill in the art. The

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applicant submits that the examiner has failed to establish a *prima facie* case of obviousness because the combination of the cited references fails to provide the claimed invention.

Although the cited reference of Sinclair maybe directed to flash memory, and the reference of Adelmann merely mentions a flash memory card in a list of memory types, the reference of Rajan has nothing to do with flash memory storage, but rather, teaches virtual memory systems.

In contrast to the other references, Rajan fails to even mention flash memory, but rather teaches: "a method for reclaiming unused storage space from a thinly provisioned data container, such as a logical unit number (LUN) of a storage system. A host-side agent executes on a client (host) of the storage system. The host-side agent detects which blocks have been freed from a host-side file system and sends a novel Punch Hole command to the storage system, which causes the storage system to deallocate certain ranges of blocks within the data container, thereby permitting the data container to shrink in size."

In fact, this thinly provisioned storage is a virtual storage system, which is not compatible with the thick (FAT) provisioned flash storage disclosed by Sinclair. With thick provisioning, a large amount of storage space is provided in advance in anticipation of future storage needs, which may cause underutilization of storage capacity. Thin provisioning, in contrast to thick provisioning, eliminates storage underutilization problems by allocating storage space in a flexible on-demand manner. In contrast to thick provisioned storage, when data is deleted from a thin-provisioned virtual disk, the operating system deletes only the indexes from the file table that refer to the file body in the file system and marks the blocks that belonged to "deleted" files as free and accessible for new data. Since the thin-provisioned virtual disk does not perform a full deletion, a data

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string, such as zeroes, are not written over the "deleted" blocks, which is in contrast to deletion of data on thick provisioned storage.

The cited references, individually or in combination, fail to teach, suggest, anticipate, or render obvious an "empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host", as required by independent claim 15. As known to those of skill in the art and according to NIST, a logical identifier is defined as a device identifier that is expressed logically by the device's software.

The examiner admits, on page 5 of the Office Action, that "Sinclair fails to disclose receiving an empty-block directive at a storage controller, the empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host". The applicant agrees with this statement.

However, the examiner mischaracterizes the reference of Rajan, incorrectly stating the "punch hole command that include a logical block address field" at paragraph [0053] discloses "an empty-block directive at a storage controller, the empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host". The applicant strongly disagrees with this statement and the examiner's reasoning.

Specifically, the examiner completely ignores paragraph [0052], which states "[t]he present invention is directed to a system and method for reclaiming unused storage space from a thinly provisioned data container". Since the thin-provisioned storage does not write over the "deleted" blocks with a data string, the hole punch command converts the "deleted blocks" into free space. As stated by Rajan in paragraph [0057], "as result of the

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Punch Hole command being processed by the storage system, the underlying blocks of the data container of the storage system are also freed and may be reutilized by the storage system".

As taught by Rajan, a hole punch command is not an empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host as required by claim 15.

According to the Office Action on page 5, the examiner alleges: "It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by Sinclair to receive an empty block directive, as disclosed by Rajan. One of ordinary skill in the art would have been motivated to make such a modification in order to prevent excess storage allocation for data that is no longer needed by the host, as taught by Rajan. Sinclair and Rajan are in the same field of endeavor as they are both directed to recovering storage space when data is deleted by a host." The applicant respectfully disagrees.

In contrast to the examiner's allegation of obvious, one of ordinary skill in the art would know that Rajan's thinly provisioned storage virtual storage system is not compatible with the Sinclair's thick (FAT) provisioned flash storage, as discussed above. Accordingly, one of ordinary skill in the art would not be motivated to combine the references.

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Assoc., Inc. v. Garlock, Inc.,* 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983).

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The examiner makes assumptions about and adds to the actual disclosure of Sinclair in cited paragraphs [0038], [0047], [0048], and [0045]. The examiner has impermissibly picked and chosen from Sinclair only so much of it as will support a given position. For example, Sinclair fails to teach or suggest "maintaining an index of mapping" in paragraph [0038] and "updating the index to indicate that the contents of the physical storage location do not need to be preserved" in cited paragraphs [0038], [0047], [0048], and [0045].

The examiner admits, on page 6 of the Office Action, that "Sinclair fails to disclose returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive". The applicant agrees with this statement.

However, the examiner alleges that "Adelmann discloses returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive (see [0039] and [0043], the user can access the file and be provided with additional details about the file, such as when the file was deleted). This allows the user to more intelligently manage large numbers of files by being able to accurately track when files are created, modified and deleted (see [0003])". The applicant strongly disagrees with this statement and the examiner's reasoning.

In review of Adelmann, paragraph [0039], at best, states "the storage device 112 does include some information pertinent to the initial modification made to a file"; and paragraph [0043] states "when the further modification to the file is to delete the file using the appliance 114, the information is updated when the processor 221 of the storage device 112 recognizes that the file was not stored on the storage device 112 after making the

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further modification." However, Adelmann fails to teach, suggest, disclose, or anticipate: "returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive", as required by claim 15. The applicant requests the examiner to clarify the interpretation of Adelmann.

The examiner concludes "[i]t would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by Sinclair to return data of a predetermined logic level, as disclosed by Adelmann. One of ordinary skill in the art would have been motivated to make such a modification in order to allow the user to more intelligently manage large numbers of files, as taught by Adelmann." The applicant respectfully disagrees.

In contrast to the examiner's allegation of obvious, one of ordinary skill in the art would understand that Adelmann does not teach the concepts, as alleged by the examiner. Accordingly, one of ordinary skill in the art would not be motivated to combine the references.

The examiner provides no valid motivation or suggestion based on the cited references that would lead one skilled in the art to arrive at the claimed invention. To support a finding of obviousness, the cited references must expressly or impliedly suggest the claimed invention, or the examiner must provide a convincing line of reasoning why the claimed invention would have been obvious to one skilled in the art. "A patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 401.

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Moreover, the combination of the cited references fails to provide the claimed invention. Under the rationale used to reject the claims, the prior art references when modified must still teach or suggest all the claim limitations of the rejected claims. In this case, the 35 U.S.C. § 103 obviousness rejections are inappropriate because the claimed elements and limitations are *not* disclosed in Sinclair in view of Rajan and Adelmann.

In reference to dependent claims 16-10 and 33, the applicant disagrees with examiner's logic and conclusions. The applicant makes no admissions by not responding to each dependent claim and reserves the right to argue against these rejections in the future. Since claim 15 is non-obvious and allowable, claims 16-20 and 33 are also nonobvious and allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Accordingly, the applicant submits the examiner has failed to establish a *prima facie* case of obviousness for the claimed invention and respectfully requests allowance of claims 15-20 and 33.

Claims 21, 25, 28-30 and 32 stand rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (US2006/0020744) in view of Rajan (US2009/0248763).

These rejections are traversed. The cited references, individually or in combination, fail to teach, suggest, anticipate, or render obvious the combination of claim elements in independent claim 21 and claims 25, 28-30 and 32, dependent thereon. The examiner has failed to establish a *prima facie* basis for obviousness under 35 U.S.C. §103(a).

As discussed above, the applicant disagrees with the examiner's characterization of Sinclair. On page 9 of the Office Action, the examiner admits "Sinclair fails to disclose

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receiving, via the processor, an indication of deletion of a file in a first location; creating, via the processor, an empty-block identifier in response to the indication of deletion; receiving, via the NAND controller, the empty block identifier." The applicant agrees with this statement.

However, the examiner mischaracterizes the reference of Rajan, incorrectly stating "Rajan discloses receiving, via the processor, an indication of deletion of a file in a first location (see [0052]: generation of a punch hold command by agent for data that is no longer needed {which includes deletion of data}); creating, via the processor, an empty-block identifier in response to the indication of deletion; receiving, via the NAND controller, the empty-block identifier (see [0053]: punch hole command that include a logical block address field). Notifying the storage system of data that is no longer in use prevents excess storage allocation (see [0012])." The applicant strongly disagrees with this statement and the Examiner's reasoning.

As stated above, Rajan fails to teach or suggest flash memory, but rather teaches thinly provisioned storage devices. Rajan certainly does not teach a NAND controller. Discussion of the failure of paragraphs [0052] and [0053] to teach the alleged elements is documented above in detail.

The examiner alleges "[i]t would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by Sinclair to receive an empty block directive, as disclosed by Rajan. One of ordinary skill in the art would have been motivated to make such a modification in order to prevent excess storage allocation for data that is no longer needed by the host, as taught by Rajan." The applicant respectfully disagrees.

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In contrast to the examiner's allegation of obvious, one of ordinary skill in the art would know that Rajan's thinly provisioned storage virtual storage system is not compatible with the Sinclair's thick (FAT) provisioned flash storage, as discussed above. Accordingly, one of ordinary skill in the art would not be motivated to combine the references.

In reference to dependent claims 25, 28-30 and 32, the applicant disagrees with examiner's logic and conclusions. The applicant makes no admissions by not responding to each dependent claim and reserves the right to argue against these rejections in the future. Since claim 21 is non-obvious and allowable, claims 25, 28-30 and 32 are also nonobvious and allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Accordingly, the applicant submits the examiner has failed to establish a *prima facie* case of obviousness for the claimed invention and respectfully requests allowance of claims 21, 25, 28-30 and 32.

Claims 22-23 stand rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (US2006/0020744) in view of Rajan (US2009/0248763), as applied to claims 21, 25, 28-30 and 32, and further in view of Adelmann (US2004/0003002).

These rejections are traversed. In reference to dependent claims 22 and 23, the applicant disagrees with the examiner's logic and conclusions. The applicant makes no admissions by not responding to each dependent claim and reserves the right to argue against these rejections in the future. Since claim 21 is non-obvious and allowable, claims 22 and 23 are also nonobvious and allowable. If an independent claim is nonobvious under

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35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Accordingly, the applicant submits the examiner has failed to establish a *prima facie* case of obviousness for the claimed invention and respectfully requests allowance of claims 22 and 23.

Claims 26-27 stand rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (US2006/0020744) and Rajan (US2009/0248763) as applied to claims 21, 25, 28-30 and 32 above, and further in view of Jensen (US2006/0120235).

These rejections are traversed. In reference to dependent claims 26 and 27, the applicant disagrees with the examiner's logic and conclusions. The applicant makes no admissions by not responding to each dependent claim and reserves the right to argue against these rejections in the future. Since claim 21 is non-obvious and allowable, claims 26 and 27 are also nonobvious and allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Accordingly, the applicant submits the examiner has failed to establish a *prima facie* case of obviousness for the claimed invention and respectfully requests allowance of claims 26 and 27.

Claim 31 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (US2006/0020744) and Rajan (US2009/0248763) as applied to claims 21, 25, 28-30 and 32 above, and further in view, of "A New Flash Memory Management for Flash Storage System", hereinafter referred to as NPL 1.

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This rejection is traversed. In reference to dependent claim 31, the applicant disagrees with the examiner's logic and conclusions. The applicant makes no admissions by not responding to each dependent claim and reserves the right to argue against these rejections in the future. Since claim 21 is non-obvious and allowable, claim 31 is also nonobvious and allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Accordingly, the applicant submits the examiner has failed to establish a *prima facie* case of obviousness for the claimed invention and respectfully requests allowance of claim 31.

Claims 34 and 35 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (US2006/0020744) in view of Rajan (US2009/0248763) and Adelmann (US2004/0003002) and as applied to claims 15-20 and 33 above, and further in view of Jensen (US2006/0120235).

These rejections are traversed. In reference to dependent claims 34 and 35, the applicant disagrees with the examiner's logic and conclusions. The applicant makes no admissions by not responding to each dependent claim and reserves the right to argue against these rejections in the future. Since claim 15 is non-obvious and allowable, claims 34 and 35 are also nonobvious and allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

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Accordingly, the applicant submits the examiner has failed to establish a *prima facie* case of obviousness for the claimed invention and respectfully requests allowance of claims 34 and 35.

CONCLUSION

In view of the foregoing, it is believed that all of the pending claims are in condition for allowance. The applicant therefore requests that the examiner withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this response is requested. If the examiner believes that a telephone conference would be useful in moving the application toward allowance, the examiner is encouraged to contact the attorney of record.

Respectfully submitted,

Dated: May 3, 2022

By: /David Wade Schnell/___
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Electronic Acknowledgement Receipt

EFS ID:	45624904
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	175872
Filer:	David Wade Schnell/Sally Hartway
Filer Authorized By:	David Wade Schnell
Attorney Docket Number:	10788.0722
Receipt Date:	03-MAY-2022
Filing Date:	16-AUG-2019
Time Stamp:	16:23:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		107880722_2022-05-03_Response_to_Office_Action_DWS_FINAL_AS_FILED.pdf	161907 897e7cb2119f60bbe6c1072f4a76a9a2e6b3f56a	yes	18

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Request for Reconsideration-After Non-Final Rejection	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	18
Warnings:			
Information:			
	Total Files Size (in bytes):	161907	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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16/543,464	08/16/2019	David Flynn	10788.0722	4625

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EXAMINER	
DUDEK JR, EDWARD J	

ART UNIT	PAPER NUMBER
2136	

NOTIFICATION DATE	DELIVERY MODE
06/23/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@ngtechlaw.com
dwschnell@ngtechlaw.com

Office Action Summary	**Application No.** 16/543,464	**Applicant(s)** Flynn et al.	
	Examiner EDWARD J DUDEK JR	**Art Unit** 2136	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 03 May 2022.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 15-23 and 25-35 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 15-23 and 25-35 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

This Office Action is responsive to the reply filed 03 May 2022.

Claims 15-23 and 25-35 are pending and have been presented for examination.

Claims 1-14 and 24 have been cancelled.

Response to Arguments

Applicant's arguments filed 03 May 2022 have been fully considered but they are not persuasive.

Applicant argues (see pages 8-9):

> In contrast to the other references, Rajan fails to even mention flash memory, but rather teaches: "a method for reclaiming unused storage space from a thinly provisioned data container, such as a logical unit number (LUN) of a storage system. A host-side agent executes on a client (host) of the storage system. The host-side agent detects which blocks have been freed from a host-side file system and sends a novel Punch Hole command to the storage system, which causes the storage system to deallocate certain ranges of blocks within the data container, thereby permitting the data container to shrink in size."
>
> In fact, this thinly provisioned storage is a virtual storage system, which is not compatible with the thick (FAT) provisioned flash storage disclosed by Sinclair. With thick provisioning, a large amount of storage space is provided in advance in anticipation of future storage needs, which may cause underutilization of storage capacity. Thin provisioning, in contrast to thick provisioning, eliminates storage underutilization

> problems by allocating storage space in a flexible on-demand manner. In contrast to thick provisioned storage, when data is deleted from a thin-provisioned virtual disk, the operating system deletes only the indexes from the file table that refer to the file body in the file system and marks the blocks that belonged to "deleted" files as free and accessible for new data. Since the thin-provisioned virtual disk does not perform a full deletion, a dataPage 8 of string, such as zeroes, are not written over the "deleted" blocks, which is in contrast to deletion of data on thick provisioned storage.

The Examiner respectfully disagrees. SINCLAIR discloses a storage system that a host accesses using logical addresses that are then translated into physical locations in the storage system (See [0038]). RAJAN discloses a storage system that presents a vdisk to a client (see [0029]), access requests from the client use a logical address that is then translated to a physical location in the storage (see [0049]). These are very similar, and common concepts, in the field of storage systems. The Examiner is relying upon the similar addressing techniques used by both references for the combination. The storage system in both references receive a logical address and translate that logical address into a physical address. Therefore, the punch hold command utilized by RAJAN would be compatible in the system of SINCLAIR. The Applicant also describes various procedures that are used during data deletion. The Examiner would note that the claims do not specify how the data is deleted. The claimed punch hole command is only used to notify the storage system that data does not need to be maintained.

Applicant argues (See pages 9-10):

> The examiner admits, on page 5 of the Office Action, that "Sinclair fails to disclose receiving an empty-block directive at a storage controller, the empty-block

directive including a logical identifier associated with a physical storage location comprising data deleted by a host". The applicant agrees with this statement.

However, the examiner mischaracterizes the reference of Rajan, incorrectly stating the "punch hole command that include a logical block address field" at paragraph [0053] discloses "an empty-block directive at a storage controller, the empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host". The applicant strongly disagrees with this statement and the examiner's reasoning.

Specifically, the examiner completely ignores paragraph [0052], which states "[t]he present invention is directed to a system and method for reclaiming unused storage space from a thinly provisioned data container". Since the thin-provisioned storage does not write over the "deleted" blocks with a data string, the hole punch command converts the "deleted blocks" into free space. As stated by Rajan in paragraph [0057], "as result of the Punch Hole command being processed by the storage system, the underlying blocks of the data container of the storage system are also freed and may be reutilized by the storage system".

As taught by Rajan, a hole punch command is not an empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host as required by claim 15.

According to the Office Action on page 5, the examiner alleges: "It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by Sinclair to receive an empty block directive, as disclosed by Rajan. One of ordinary skill in the art would have been motivated to make such a modification in order to prevent excess storage allocation for data that is no longer needed by the host, as taught by Rajan. Sinclair and Rajan are in the same field of endeavor as they are both directed to recovering storage space when data is deleted by a host." The applicant respectfully disagrees.

> In contrast to the examiner's allegation of obvious, one of ordinary skill in the art would know that Rajan's thinly provisioned storage virtual storage system is not compatible with the Sinclair's thick (FAT) provisioned flash storage, as discussed above. Accordingly, one of ordinary skill in the art would not be motivated to combine the references.

The Examiner respectfully disagrees. The Examiner is relying upon the similar addressing techniques used by both references for the combination. The storage system in both references receive a logical address and translate that logical address into a physical address. Therefore, the punch hold command utilized by RAJAN would be compatible in the system of SINCLAIR. Applicants discussion regarding data blocks being overwritten are not relevant to the current claims. The claimed empty block directive does not specify how the data is deleted, only that it is a notification of data that does not need to be maintained.

Applicant argues (see pages 11-12):

> The examiner admits, on page 6 of the Office Action, that "Sinclair fails to disclose returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive". The applicant agrees with this statement.
>
> However, the examiner alleges that "Adelmann discloses returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive (see [0039] and [0043], the user can access the file and be provided with additional details about the file, such as when the file was deleted). This allows the user to more intelligently manage large numbers of files by being able to accurately track

when files are created, modified and deleted (see [0003])". The applicant strongly disagrees with this statement and the examiner's reasoning.

In review of Adelmann, paragraph [0039], at best, states "the storage device 112 does include some information pertinent to the initial modification made to a file"; and paragraph [0043] states "when the further modification to the file is to delete the file using the appliance 114, the information is updated when the processor 221 of the storage device 112 recognizes that the file was not stored on the storage device 112 after making the further modification." However, Adelmann fails to teach, suggest, disclose, or anticipate: "returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive", as required by claim 15. The applicant requests the examiner to clarify the interpretation of Adelmann.

The examiner concludes "[i]t would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by Sinclair to return data of a predetermined logic level, as disclosed by Adelmann. One of ordinary skill in the art would have been motivated to make such a modification in order to allow the user to more intelligently manage large numbers of files, as taught by Adelmann." The applicant respectfully disagrees.

In contrast to the examiner's allegation of obvious, one of ordinary skill in the art would understand that Adelmann does not teach the concepts, as alleged by the examiner. Accordingly, one of ordinary skill in the art would not be motivated to combine the references.

The examiner provides no valid motivation or suggestion based on the cited references that would lead one skilled in the art to arrive at the claimed invention. To support a finding of obviousness, the cited references must expressly or impliedly suggest the claimed invention, or the examiner must provide a convincing line of reasoning why the claimed invention would have been obvious to one skilled in the art. "A

> patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." KSR, 550 U.S. at 401.
>
> Moreover, the combination of the cited references fails to provide the claimed invention. Under the rationale used to reject the claims, the prior art references when modified must still teach or suggest all the claim limitations of the rejected claims. In this case, the 35 U.S.C. § 103 obviousness rejections are inappropriate because the claimed elements and limitations are not disclosed in Sinclair in view of Rajan and Adelmann.

The Examiner respectfully disagrees. In the combination of SINCLAIR and RAJAN, the punch hole command is used to notify the storage system that data has been deleted As a result, the data that was associated with the logical address in the punch hole command is now considered deleted by the storage system. ADELAMAN discloses that a user can receive information from the storage system concerning data that has been deleted. Since the data associated with the logical address in the punch hole command is deleted data, access to this data by the user would provide them with information about the deletion of the data. This information that is provided to the user would be the data of a predetermined logic level. Predetermined simply means that it is known already. The claims do not provide any limitations about the predetermined logic level. The claims also do not provide any limitations that link the empty block directive and the read command. These are interpreted as two separate commands that are not dependent on each other.

In summary, the Examiner will also address the numerous references by Applicant to data deletion on thick and thin provisioned storage. Data deletion by removing translation data and/or by overwriting the data with all zeros are techniques

that are used in storage system generally for the deletion of data. However, none of these techniques are performed exclusively by thin or thick provisioned storage. Applicant seems to imply in the arguments that the use of thick or thin provisioned storage alone would imply that a particular erase technique is used. The Examiner strongly disagrees with this. The only material difference between thick and thin provisioned storage is manner in which physical resources are dynamically allocated and deallocated in thin provisioned storage. Both storage systems (thin and thick) are compatible with data deletion by removing translation references and/or overwriting storage data.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 15-20 and 33 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over SINCLAIR (**U.S. Patent Application Publication #2006/0020744**) in view of RAJAN (**U.S. Patent Application Publication #2009/0248763**) and ADELMANN (**U.S. Patent Application Publication #2004/0003002**).

15. SINCLAIR discloses A method for managing data in a NAND flash storage system **(see [0030], flash memory system)**, the method comprising: *receiving an empty-block directive at a storage controller, the empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host (see RAJAN below); returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive (see ADELMANN below)*; and maintaining an index of mapping between the logical identifier and the physical storage location **(see [0038]: flash controller maps the host logical address space into a physical address space on the flash memory)**; and updating the index to indicate that the contents of the physical storage location do not need to be preserved **(see [0038], storage controller performs logical to physical mapping, [0047], new data is written to a different location which would involve updating mapping data, [0048], data that is deleted is marked as deallocated, [0045]: data attribute store provides information about the portion of the data that is to be maintained, by**

identifying data to be maintained, the data that doesn't need to be maintained {preserved} is also identified).

SINCLAIR discloses an index for mapping logical identifiers from the host to physical memory locations, and also discloses a DAS (which is another index) for tracking various attributes of the host logical cluster allocations **(see [0038]-[0041])**. Clearly, SINCLAIR discloses the mapping and the indication that contents do not need to be preserved. However, this information is maintained in two tables rather than one. While the claim does not specifically claim a single index, the claim simply refers to "the index" and the Examiner will interpret this as one index. This is a matter of design choice. SINCLAIR already discloses all the elements of the claimed index. Implementing this index as a single structure, or multiple structures is up to the person implementing the system. "When there is a design need for market pressure to solve a problem and there are a finite number if identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *KSR*, 82 USPQ2d at 1397.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have implemented the mapping and the DAS disclosed in SINCLAIR as a single table, as that is one solution, from a limited number of solutions, for storing all the attributes that are already being tracked by SINCLAIR.

SINCLAIR fails to disclose receiving an empty-block directive at a storage controller, the empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host.

RAJAN discloses receiving an empty-block directive at a storage controller, the empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host **(see [0053]: punch hole command that include a logical block address field)**. Notifying the storage system of data that is no longer in use prevents excess storage allocation **(see [0012])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by SINCLAIR to receive an empty block directive, as disclosed by RAJAN. One of ordinary skill in the art would have been motivated to make such a modification in order to prevent excess storage allocation for data that is no longer needed by the host, as taught by RAJAN. SINCLAIR and RAJAN are in the same field of endeavor as they are both directed to recovering storage space when data is deleted by a host.

SINCLAIR fails to disclose returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive.

ADELMANN discloses returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive **(see [0039] and [0043], the user can access the file and be provided with additional details about the file, such as when the file was deleted)**. This allows the user to more intelligently manage large numbers of files by being able to accurately track when files are created, modified and deleted **(see [0003])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by SINCLAIR to return data of a predetermined logic level, as disclosed by ADELMANN. One of ordinary skill in the art would have been motivated to make such a modification in order to allow the user to more intelligently manage large numbers of files, as taught by ADELMANN. SINCLAIR and ADELMANN are in the same field of endeavor as they are both directed to managing data deleted by a host.

16. The method of claim 15, wherein the predetermined logic level is zero **(see RAJAN [0031], all data that is transferred over a bus is comprised of bits with logic level zero or logic level one. Therefore, depending on the data that is sent, the string could comprise all zero's, all one's or a mix of one's and zero's. The ability to send all zero's is within the operating parameters of the system)**.

17. The method of claim 15, further comprising: determining that the empty-block directive further includes an indication that data associated with the logical identifier should be overwritten; and overwriting the data associated with the logical identifier **(see SINCLAIR [0052], unallocated data is not copied, and would be overwritten after the block is erase and returned as a free block)**.

18. The method of claim 15, wherein the empty-block directive is part of a block storage protocol **(see SINCLAIR [0030], the system is communicating with a block based memory, so it can be interpreted as having a block storage protocol)**.

19. The method of claim 15, wherein the empty-block directive is received through an application programming interface **(see SINCLAIR [0038], host interfaces with the memory controller through an application)**.

20. The method of claim 15, wherein the empty-block directive is received from a file system **(see SINCLAIR [0036], file system indicates data that is deleted)**.

33. The method of claim 15, further comprising transmitting a message indicating that the data in the physical storage location has been deleted in response to a delete command **(see RAJAN [0056]: response from storage system that the punch hole command was successful)**.

Claims 21, 25, 28-30 and 32 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over SINCLAIR (**U.S. Patent Application Publication #2006/0020744**) in view of RAJAN (**U.S. Patent Application Publication #2009/0248763**).

21. SINCLAIR discloses A method for managing data in a system having a processor **(see [0030]: a host accesses the flash memory, the host would have a processor; [0059]: computer code designed to be executed by a computer, a processor would be necessary to execute the code)** and a block-based NAND flash storage system **(see [0030]: flash memory is a block based storage)**, the NAND

flash storage system having physical NAND flash storage locations controlled by a NAND controller **(see [0002]-[0003]: controller that manages the physical memory arrays)**, the method comprising: *receiving, via the processor, an indication of deletion of a file in a first location; creating, via the processor, an empty-block identifier in response to the indication of deletion; receiving, via the NAND controller, the empty-block identifier (see RAJAN below)*; and maintaining, via the NAND controller, an index of mapping between logical identifiers and physical NAND flash storage locations **(see [0038]: flash controller maps the host logical address space into a physical address space on the flash memory)**; and updating the index to indicate that data stored in one or more of the physical NAND flash storage locations associated with the empty-block identifier does not need to be preserved **(see [0038], storage controller performs logical to physical mapping, [0047], new data is written to a different location which would involve updating mapping data, [0048], data that is deleted is marked as deallocated, [0045]: data attribute store provides information about the portion of the data that is to be maintained, by identifying data to be maintained, the data that doesn't need to be maintained {preserved} is also identified)**.

SINCLAIR fails to disclose receiving, via the processor, an indication of deletion of a file in a first location; creating, via the processor, an empty-block identifier in response to the indication of deletion; receiving, via the NAND controller, the empty-block identifier.

RAJAN discloses receiving, via the processor, an indication of deletion of a file in a first location **(see [0052]: generation of a punch hold command by agent for data**

that is no longer needed {which includes deletion of data}); creating, via the processor, an empty-block identifier in response to the indication of deletion; receiving, via the NAND controller, the empty-block identifier **(see [0053]: punch hole command that include a logical block address field)**. Notifying the storage system of data that is no longer in use prevents excess storage allocation **(see [0012])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by SINCLAIR to receive an empty block directive, as disclosed by RAJAN. One of ordinary skill in the art would have been motivated to make such a modification in order to prevent excess storage allocation for data that is no longer needed by the host, as taught by RAJAN. SINCLAIR and RAJAN are in the same field of endeavor as they are both directed to recovering storage space when data is deleted by a host.

25. The method of claim 21, wherein the empty-block identifier issued by the processor indicates that data stored in the one or more physical NAND flash storage locations associated with the empty-block identifier should be overwritten **(see SINCLAIR [0052], unallocated data is not copied, and would be overwritten after the block is erase and returned as a free block)**.

28. The method of claim 21, further comprising performing garbage collection, via the NAND controller, in the NAND flash storage system **(see SINCLAIR [0033]: DAS is used during garbage collection)**.

29. The method of claim 28, wherein performing garbage collection comprises: copying a block containing data that should be preserved from an erase block comprising blocks containing data that does not need to be preserved; and erasing the erase block **(see SINCLAIR [0035]: clusters that are being used are copied, clusters that are not being used are not copied)**.

30. The method of claim 29, further comprising writing data, via the NAND controller, to the erased erase block **(see SINCLAIR [0011]: when blocks are erased they are returned to a pool to available memory blocks so that data can be written to the block, in the future the block will be written to again)**.

32. The method of claim 21, wherein each of the one or more physical NAND flash storage locations are smaller than a NAND flash erase block **(see SINCLAIR [0041]: portions of a cluster can be tracked)**.

Claims 22-23 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over SINCLAIR (**U.S. Patent Application Publication #2006/0020744**) and RAJAN (**U.S. Patent Application Publication #2009/0248763**) as applied to claims 21, 25, 28-30 and 32 above, and further in view of ADELMANN (**U.S. Patent Application Publication #2004/0003002**).

22. The method of claim 21 **(see SINCLAIR above)**, further comprising:

receiving a read command including the empty-block identifier from the host processor;

and returning, via the NAND controller, a data string comprising data bits with a predetermined logic level in response to receiving the read command (see ADELMANN below).

SINCLAIR fails to disclose receiving a read command including the empty-block identifier from the host processor; and returning, via the NAND controller, a data string comprising data bits with a predetermined logic level in response to receiving the read command.

ADELMANN discloses receiving a read command including the empty-block identifier from the host processor; and returning, via the NAND controller, a data string comprising data bits with a predetermined logic level in response to receiving the read command **(see [0039] and [0043], the user can access the file and be provided with additional details about the file, such as when the file was deleted)**. This allows the user to more intelligently manage large numbers of files by being able to accurately track when files are created, modified and deleted **(see [0003])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by SINCLAIR to return data of a predetermined logic level, as disclosed by ADELMANN. One of ordinary skill in the art would have been motivated to make such a modification in order to allow the user to more intelligently manage large numbers of files, as taught by ADELMANN. SINCLAIR and ADELMANN are in the same field of endeavor as they are both directed to managing data deleted by a host.

23. The method of claim 22, wherein the predetermined logic level is zero **(see RAJAN [0031], all data that is transferred over a bus is comprised of bits with logic level zero or logic level one. Therefore, depending on the data that is sent, the string could comprise all zero's, all one's or a mix of one's and zero's. The ability to send all zero's is within the operating parameters of the system)**.

Claims 26-27 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over SINCLAIR (**U.S. Patent Application Publication #2006/0020744**) and RAJAN (**U.S. Patent Application Publication #2009/0248763**) as applied to claims 21, 25, 28-30 and 32 above, and further in view of JENSEN (**U.S. Patent Application Publication #2006/0120235**).

26. The method of claim 21 **(see SINCLAIR above)**, *further comprising transmitting a message indicating that the data stored in one or more physical NAND flash storage locations has been overwritten (see JENSEN below).*

SINCLAIR fails to disclose transmitting a message indicating that the data stored in one or more physical NAND flash storage locations has been overwritten.

JENSEN discloses transmitting a message indicating that the data stored in one or more physical NAND flash storage locations has been overwritten **(see [0046]-[0050]: data locations that are subject to an erase command are overwritten, once the overwrite is complete a status signal is returned to the host)**. Overwriting data

that was subject to an erase command is useful to protect personal or confidential data **(see [0004]-[0006])**.

27. The method of claim 21 **(see SINCLAIR above)**, *further comprising overwriting data stored in the one or more physical NAND flash storage locations with a series of characters such that the overwritten data is non-recoverable (see JENSEN below).*

SINCLAIR fails to disclose overwriting data stored in the one or more physical NAND flash storage locations with a series of characters such that the overwritten data is non-recoverable.

JENSEN discloses overwriting data stored in the one or more physical NAND flash storage locations with a series of characters such that the overwritten data is non-recoverable **(see [0046]-[0050]: data locations that are subject to an erase command are overwritten, once the overwrite is complete a status signal is returned to the host)**. Overwriting data that was subject to an erase command is useful to protect personal or confidential data **(see [0004]-[0006])**.

Claim 31 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over SINCLAIR (**U.S. Patent Application Publication #2006/0020744**) and RAJAN (**U.S. Patent Application Publication #2009/0248763**) as applied to claims 21, 25, 28-30 and 32 above, and further in view of "A New Flash Memory Management for Flash Storage System", hereinafter referred to as NPL1.

31. The method of claim 21 **(see SINCLAIR above)**, *wherein the NAND flash storage system is an append-only storage system (see NPL1 below).*

SINCLAIR fails to disclose wherein the NAND flash storage system is an append-only storage system.

NPL1 discloses wherein the NAND flash storage system is an append-only storage system **(see section 2 "Flash Memory Management)**. Append only writing provides a positive of effect of cycle-leveling **(see section 2 "Flash Memory Management)**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by SINCLAIR to use an append only system, as disclosed by NPL1. One of ordinary skill in the art would have been motivated to make such a modification in order to provide even wear leveling of the flash memory, as taught by NPL1. SINCLAIR and NPL1 are in the same field of endeavor as they are both directed to managing data on a storage system.

Claims 34 and 35 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over SINCLAIR (**U.S. Patent Application Publication #2006/0020744**), RAJAN (**U.S. Patent Application Publication #2009/0248763**) and ADELMANN (**U.S. Patent Application Publication #2004/0003002**) as applied to claims 15-20 and 33 above, and further in view of JENSEN (**U.S. Patent Application Publication #2006/0120235**).

34. The method of claim 15 **(see SINCLAIR above)**, *further comprising overwriting data stored in the physical storage location with a series of characters such that the overwritten data is non-recoverable (see JENSEN below).*

SINCLAIR fails to disclose overwriting data stored in the physical storage location with a series of characters such that the overwritten data is non-recoverable.

JENSEN discloses overwriting data stored in the physical storage location with a series of characters such that the overwritten data is non-recoverable **(see [0046]-[0050]: data locations that are subject to an erase command are overwritten, once the overwrite is complete a status signal is returned to the host)**. Overwriting data that was subject to an erase command is useful to protect personal or confidential data **(see [0004]-[0006])**.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by SINCLAIR to overwrite data stored in a physical location, as disclosed by JENSEN. One of ordinary skill in the art would have been motivated to make such a modification in order to protect personal or confidential data, as taught by JENSEN. SINCLAIR and JENSEN are in the same field of endeavor as they are both directed to managing data deleted by a host.

35. The method of claim 15 **(see SINCLAIR above)**, *further comprising removing a mapping between the logical identifier and the physical storage location from the index (see JENSEN below).*

SINCLAIR fails to disclose removing a mapping between the logical identifier and the physical storage location from the index.

JENSEN discloses removing a mapping between the logical identifier and the physical storage location from the index **(see [0005]: one method for erasing data involves deleting a pointer that points to the data, this pointer would be the mapping between the logical and physical storage location)**. Removing this mapping would accomplish the goal of erasing the data and making the data inaccessible. Although it is not the most secure way of erasing data, it is one known method for doing so. "When there is a design need for market pressure to solve a problem and there are a finite number if identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *KSR*, 82 USPQ2d at 1397.

It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by SINCLAIR to remove the mapping, as disclosed by JENSEN. One of ordinary skill in the art would have been motivated to make such a modification in order to prevent data that was erased from being easily accessible, as taught by JENSEN. SINCLAIR and JENSEN are in the same field of endeavor as they are both directed to managing data that was deleted by a host.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWARD J DUDEK JR whose telephone number is (571)270-1030. The examiner can normally be reached Monday - Friday, 8:00A-4:00P.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Rones can be reached on 571-272-4085. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-

center for more information about Patent Center and

https://www.uspto.gov/patents/docx for information about filing in DOCX format. For

additional questions, contact the Electronic Business Center (EBC) at 866-217-9197

(toll-free). If you would like assistance from a USPTO Customer Service

Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EDWARD J DUDEK JR/
Primary Examiner, Art Unit 2136

Electronic Acknowledgement Receipt	
EFS ID:	46555740
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	175872
Filer:	David Wade Schnell/Sally Hartway
Filer Authorized By:	David Wade Schnell
Attorney Docket Number:	10788.0722
Receipt Date:	06-SEP-2022
Filing Date:	16-AUG-2019
Time Stamp:	14:03:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$2000
RAM confirmation Number	E202296E06242461
Deposit Account	502993
Authorized User	Sally Hartway
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		107880722_2022-09-06_Response_Final_Office_Action_FINAL_AS_FILED.pdf	169826 7be8691cb5f033d6a712f963bb0f862314e0ae54	yes	21

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Response After Final Action	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	21

Warnings:					
Information:					
2	Request for Continued Examination (RCE)	107880722_2022-09-06_RCE.pdf	1667148 efb4a381eae9018b67495600d33ef846b9c0c82b	no	3
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	38126 5d5daefe802855ce6b3dabba0639667f485db9c6	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1875100		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	16/543,464
Filing Date:	August 16, 2019
Applicant:	Unification Technologies LLC
Inventors:	David Flynn
Confirmation No.:	4625
Group Art Unit:	2136
Examiner:	Edward J. Dudek Jr.
Title:	Systems and Methods for Identifying Storage Resources That Are Not In Use
Attorney Docket:	10788.0722

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

RESPONSE TO OFFICE ACTION

In response to the Office Action mailed June 23, 2022, please enter the following the Remarks set forth below.

Amendments to the Claims begin on page 2 of this paper

Remarks begin on page 7 of this paper.

Filed September 6, 2022

CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

1– 14. (Canceled)

15. (Currently amended) A method for managing data in a NAND flash storage system, the method comprising:

receiving an empty-block directive from a host at a storage controller in the NAND flash storage system, the empty-block directive including a logical identifier associated with a physical storage location comprising data that does not need to be preserved ~~deleted by a host~~;

returning by the storage controller an indication that the logical identifier is empty, ~~a data string comprising data of a predetermined logic level~~ in response to a read command from the host requesting to read the data ~~associated with~~ identified by the logical identifier included in the empty-block directive, wherein the data in the physical storage location remains on the NAND flash storage system;

maintaining by the storage controller an index of mappings between the logical identifier and the physical storage location; and

updating the index of mappings by the storage controller, in response to the empty-block directive, to indicate that the data in ~~contents of~~ the physical storage location does not need to be preserved.

16. (Currently amended) The method of claim 15, wherein the indication is at least one zero.

17. (Currently amended) The method of claim 15, further comprising:

determining that the empty-block directive further includes an indication that the data ~~associated with~~ identified by the logical identifier should be overwritten; and

overwriting the data ~~associated with~~ identified by the logical identifier.

18. (Previously presented) The method of claim 15, wherein the empty-block directive is part of a block storage protocol.

19. (Previously presented) The method of claim 15, wherein the empty-block directive is received through an application programming interface.

20. (Previously presented) The method of claim 15, wherein the empty-block directive is received from a file system.

21. (Currently amended) A method for managing data in a system having a host processor and a block-based NAND flash storage system, the NAND flash storage system having physical NAND flash storage locations controlled by a NAND controller, the method comprising:

receiving, via the host processor, an indication of deletion of a file at the host processor ~~in a first location~~;

creating, via the host processor, an empty-block identifier in response to the indication of deletion;

receiving, via the NAND controller, the empty-block identifier;

maintaining, via the NAND controller, an index of mappings between logical identifiers and physical NAND flash storage locations; and

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updating the index of mappings, in response to the receiving the empty-block identifier, to indicate that data ~~stored in~~ associated with the file on one or more of the physical NAND flash storage locations ~~associated with~~ identified by the empty-block identifier does not need to be preserved.

22. (Currently amended) The method of claim 21, further comprising:

receiving, via the NAND controller, a read command including a logical identifier that was associated with the empty-block ~~identifier from the host processor~~; and

returning, via the NAND controller, a data string indicating that the logical identifier is empty ~~comprising data bits with a predetermined logic level~~ in response to the receiving the read command.

23. (Currently amended) The method of claim 22, wherein the data string comprises ~~predetermined logic level is~~ at least one zero.

24. Canceled.

25. (Currently amended) The method of claim 21, wherein the empty-block identifier ~~issued by the processor~~ indicates that the data ~~stored in~~ associated with the file on the one or more physical NAND flash storage locations ~~associated with~~ identified by the empty-block identifier should be overwritten.

26. (Currently amended) The method of claim 21, further comprising transmitting a message indicating that the data ~~stored in~~ associated with the file on one or more physical NAND flash storage locations identified by the empty-block identifier has been overwritten.

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27. (Currently amended) The method of claim 21, further comprising overwriting the data ~~stored in~~ associated with the file on the one or more physical NAND flash storage locations identified by the empty-block identifier with a series of characters such that the overwritten data is non-recoverable.

28. (Previously presented) The method of claim 21, further comprising performing garbage collection, via the NAND controller, in the NAND flash storage system.

29. (Previously presented) The method of claim 28, wherein performing garbage collection comprises:

copying a block containing data that should be preserved from an erase block comprising blocks containing data that does not need to be preserved; and

erasing the erase block.

30. (Currently amended) The method of claim 29, further comprising writing the copied data, via the NAND controller, to the erased erase block.

31. (Previously presented) The method of claim 21, wherein the NAND flash storage system is an append-only storage system.

32. (Currently amended) The method of claim 29 [[21]], wherein each of the one or more physical NAND flash storage locations are smaller than ~~a NAND flash~~ the erase block.

33. (Previously presented) The method of claim 15, further comprising transmitting a message indicating that the data in the physical storage location has been deleted in response to a delete command.

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34. (Currently amended) The method of claim 15, further comprising overwriting the data ~~stored~~ in the physical storage location with a series of characters such that the overwritten data is non-recoverable.

35. (Currently amended) The method of claim 15, further comprising removing a mapping between the logical identifier and the physical storage location from the index of mappings; and erasing the data stored in the physical storage location

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REMARKS

Claims 15-23 and 25-35 are currently pending. All claims were rejected in this Office Action. In response, Applicant has amended claims 15-17, 21-23, 25-27, 30, 32, and 34-35. The Amendments to the Claims, as listed above, and the following Remarks are believed to be fully responsive to all rejections presented in the pending Office Action.

Regarding the Response to Argument

Applicant appreciates the examiner's time and consideration in the drafting of the response to argument. However, applicant still disagrees with various points made in the response to argument. Applicant stands by the remarks made in the previous response to the office action and makes no admissions to the examiner's response to argument or to the characterization of any of the references, individually or in combination, that were cited in the response to argument. Applicant has addressed some of the examiner's points in the remarks below, however, applicant preserves all rights to respond, oppose, and/or rectify any position presented in the response to argument in the future, without prejudice.

In the response to argument, the examiner continues to use impermissible hindsight reasoning to piece together an obviousness rejection using selected sentences from the cited references. According to MPEP 2142, "impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art".

Moreover, the examiner's response to argument and the rejections below fail to meet the requirements of *KSR* and *Graham*. "In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences *themselves* would have been obvious, but whether the claimed invention *as a whole* would have been obvious." *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1537, 218 USPQ

871 (Fed. Cir. 1983) (emphasis added). As stated in *KSR*, the mere fact that references *can* be combined or modified does not render the resultant combination. *KSR*, 550 U.S. at 416-17.

It has also long been established that:

> It is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. *Eli Lilly and Co. v. Zenith Goldmine Pharm.*, 364 F.Supp.2d 820, 902 (S.D. Ind. 2005)(citing *In re Wesslau*, 353 F.2d 238, 241 (1965)).

In the response to argument and the rejections presented below, the examiner picks and chooses elements from the references to build a case of obviousness and ignores teachings in these references that are contrary to the examiner's position. The examiner fails to fully appreciate what such reference fairly suggests to one of ordinary skill in the art. Moreover, "a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418.

Rejections under 35 USC 103

Claims 15-20 and 33 stand rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (US2006/0020744) in view of Rajan (US2009/0248763) and Adelmann (US2004/0003002).

These rejections are traversed. The cited references, either individually or in combination, fail to teach, suggest, anticipate, or render obvious the combination of claim elements in independent claim 15 and claims 16-20 and 33, dependent thereon. The

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examiner has failed to establish a *prima facie* basis for obviousness under 35 U.S.C. §103(a).

Sinclair at [0038] appears to teach "The flash-memory controller maps the host's logical address space into a controller logical address space, which is in turn, mapped to a physical address space on the flash-memory."

However, Sinclair at [0045], [0047], and [0048] fails to teach, suggest, anticipate, or render obvious "updating the index of mappings by the storage controller, in response to the empty-block directive, to indicate that the data in the physical storage location does not need to be preserved", as required by claim 15, as amended.

Furthermore, Sinclair at [0045], [0047], and [0048] teaches a write command, as illustrated in FIG 6. On page 9, the examiner actually acknowledges this fact by stating: "[0047], new data is written to a different location which would involve updating mapping data". In contrast to the examiner's position, Sinclair at [0047] teaches a "compare old data to new data" (610), without preforming a read (606), after the "perform write operation" (608). Accordingly, Sinclair at [0047] fails to teach "updating mapping data". Sinclair at [0048] states: "if it is determined (612) that a change to data has been detected, the change is interpreted (614) to determine (616) whether one or more clusters have been deallocated...if it is determined (616) that one or more clusters have been deallocated, the status of the one or more clusters in a Data Allocation Table (DAT) is changed to indicate a "deallocated" status."

Sinclair appears to teach writing new data to a designated address that has old data stored; comparing the new data and the old data; determining if the old data changed; if the old data changed, determine if one or more clustered has been deallocated; if one or more

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clustered has been deallocated, change the status of the one or more clusters in a DAT to deallocated, as described in FIG 6 and [0046]-[0048].

In contrast to claim 15, as amended, Sinclair fails to teach or suggest, updating the index of mappings by the storage controller, in response to the empty-block directive to indicate that the data in the physical storage location does not need to be preserved. In support, the examiner on page 10 states: "SINCLAIR fails to disclose receiving an empty-block directive at a storage controller, the empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host."

To move this application towards allowance, applicant has amended independent claim 15 to state: "maintaining by the storage controller an index of mappings between the logical identifier and the physical storage location; and updating the index of mappings by the storage controller, in response to the empty-block directive, to indicate that the data in the physical storage location does not need to be preserved."

These amendments are supported throughout the pending application, especially, for example at [0014] and [0020]. These amendments add clarity to independent claim 15, which overcome the examiner's interpretation of Sinclair.

The cited references, either individually or in combination, fail to teach, suggest, anticipate, or render obvious the elements of independent claim 15, as amended. For example, the cited references, either individually or in combination, fail to teach, suggest, anticipate, or render obvious "updating the index of mappings by the storage controller, in response to the empty-block directive, to indicate that the data in contents of the physical storage location does not need to be preserved," as required by independent claim 15.

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On page 11, the examiner alleges: "RAJAN discloses receiving an empty-block directive at a storage controller, the empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host (see [0053]: punch hole command that include a logical block address field). Notifying the storage system of data that is no longer in use prevents excess storage allocation (see [0012])."

The cited references, either individually or in combination, fail to teach, suggest, anticipate, or render obvious "receiving an empty-block directive at a storage controller, the empty-block directive including a logical identifier associated with a physical storage location comprising data deleted by a host", as required by independent claim 15.

In contrast to the examiner's statement, Rajan at [0012] states: "Although the file system typically records appropriate meta data entries when a file is deleted, no status message is passed to the storage system that notifies the system that certain blocks of the LUN are no longer in use."

Furthermore, Rajan fails to teach "receiving an empty-block directive at a storage controller". Rather, Rajan teaches "the term 'storage operating system' generally refers to the computer-executable code operable on, a computer that manages data access and may, in the case of a multi-protocol storage appliance, implement data access semantics." It appears that Rajan teaches the storage controller is on the computer or host side, which supported by FIGS 8-9.

To add clarity to the claim, applicant has amended independent claim 15 to state: "receiving an empty-block directive from a host at a storage controller in the NAND flash storage system, the empty-block directive including a logical identifier associated with a physical storage location comprising data that does not need to be preserved". The cited

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references, either individually or in combination, fail to teach, suggest, anticipate, or render obvious receiving an empty-block directive from a host at a storage controller in the NAND flash storage system, the empty-block directive including a logical identifier associated with a physical storage location comprising data that does not need to be preserved, as required by independent claim 15, as amended.

The examiner admits, on page 11 of the Office Action, that "Sinclair fails to disclose returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive". Applicant agrees with this statement.

However, the examiner alleges that "Adelmann discloses returning a data string comprising data of a predetermined logic level in response to a read command requesting to read data associated with the logical identifier included in the empty-block directive (see [0039] and [0043], the user can access the file and be provided with additional details about the file, such as when the file was deleted). This allows the user to more intelligently manage large numbers of files by being able to accurately track when files are created, modified and deleted (see [0003])".

In review of Adelmann, paragraph [0039], at best, states "the storage device 112 does include some information pertinent to the initial modification made to a file"; and paragraph [0043] states "when the further modification to the file is to delete the file using the appliance 114, the information is updated when the processor 221 of the storage device 112 recognizes that the file was not stored on the storage device 112 after making the further modification." However, Adelmann fails to teach, suggest, disclose, or anticipate: "returning a data string comprising data of a predetermined logic level in response to a read

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command requesting to read data associated with the logical identifier included in the empty-block directive", as required by claim 15.

To further move this application towards allowance, applicant has amended independent claim 15 to state: "returning by the storage controller an indication that the logical identifier is empty, in response to a read command from the host requesting to read the data identified by the logical identifier included in the empty-block directive, wherein the data in the physical storage location remains on the NAND flash storage system." This amendment is supported throughout the pending application, especially, for example at [0022].

The cited references, either individually or in combination, fail to teach, suggest, anticipate, or render obvious returning by the storage controller an indication that the logical identifier is empty, in response to a read command from the host requesting to read the data identified by the logical identifier included in the empty-block directive, wherein the data in the physical storage location remains on the NAND flash storage system., as required by independent claim 15, as amended.

In reference to dependent claims 16-10 and 33, applicant disagrees with examiner's logic and conclusions. Applicant makes no admissions by not responding to each dependent claim and reserves the right to respond against these rejections in the future. Since claim 15, as amended, is non-obvious and allowable, claims 16-20 and 33 are also nonobvious and allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

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Accordingly, applicant submits the examiner has failed to establish a *prima facie* case of obviousness for the claimed invention and respectfully requests allowance of claims 15-20 and 33, as amended.

Claims 21, 25, 28-30 and 32 stand rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (US2006/0020744) in view of Rajan (US2009/0248763).

These rejections are traversed. The cited references, either individually or in combination, fail to teach, suggest, anticipate, or render obvious the combination of claim elements in independent claim 21 and claims 25, 28-30 and 32, dependent thereon. The examiner has failed to establish a *prima facie* basis for obviousness under 35 U.S.C. §103(a).

Sinclair at [0038] appears to teach "The flash-memory controller maps the host's logical address space into a controller logical address space, which is in turn, mapped to a physical address space on the flash-memory"

In contrast to the examiner's conclusion, Sinclair at [0045], [0047], and [0048] teaches a write command, as illustrated in FIG 6. On page 14, the examiner actually acknowledges this fact by stating: "[0047], new data is written to a different location which would involve updating mapping data". Further, Sinclair at [0047] teaches a "compare old data to new data" (610), without preforming a read (606), after the "perform write operation" (608). Sinclair appears to teach writing new data to a designated address that has old data stored; comparing the new data and the old data; determining if the old data changed; if the old data changed, determine if one or more clustered has been deallocated; if one or more clustered has been deallocated, change the status of the one or more clusters in a DAT to deallocated, as described in FIG 6 and [0046]-[0048].

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However, Sinclair fails to teach or suggest updating the index of mappings, in response to the receiving the empty-block identifier, to indicate that data associated with the file on one or more of the physical NAND flash storage locations identified by the empty-block identifier does not need to be preserved. In support, the examiner at page 14 states: "SINCLAIR fails to disclose receiving, via the processor, an indication of deletion of a file in a first location; creating, via the processor, an empty-block identifier in response to the indication of deletion; receiving, via the NAND controller, the empty block identifier."

Moreover, Sinclair at fails to teach "updating the to indicate that data stored in one or more of the physical NAND flash storage locations associated with the empty-block identifier does not need to be preserved", as required by independent pending claim 21.

However, to move this application to allowance, applicant has amended claim 21 to state: "updating the index of mappings, in response to the receiving the empty-block identifier, to indicate that data associated with the file on one or more of the physical NAND flash storage locations identified by the empty-block identifier does not need to be preserved".

The cited references, either individually or in combination, fail to teach, suggest, anticipate, or render obvious "receiving, via the NAND controller, the empty-block identifier; maintaining, via the NAND controller, an index of mappings between logical identifiers and physical NAND flash storage locations; and updating the index of mappings, in response to the receiving the empty-block identifier, to indicate that data associated with the file on one or more of the physical NAND flash storage locations

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identified by the empty-block identifier does not need to be preserved," as required by independent claim 21, as amended.

On page 14 of the Office Action, the examiner admits "Sinclair fails to disclose receiving, via the processor, an indication of deletion of a file in a first location; creating, via the processor, an empty-block identifier in response to the indication of deletion; receiving, via the NAND controller, the empty block identifier." Applicant agrees with this statement.

However, the examiner mischaracterizes the reference of Rajan, incorrectly stating "Rajan discloses receiving, via the processor, an indication of deletion of a file in a first location (see [0052]: generation of a punch hold command by agent for data that is no longer needed {which includes deletion of data}); creating, via the processor, an empty-block identifier in response to the indication of deletion; receiving, via the NAND controller, the empty-block identifier (see [0053]: punch hole command that include a logical block address field). Notifying the storage system of data that is no longer in use prevents excess storage allocation (see [0012])." Applicant strongly disagrees with this statement and the Examiner's reasoning.

In contrast to the examiner's statement, Rajan at [0012] states: "Although the file system typically records appropriate meta data entries when a file is deleted, no status message is passed to the storage system that notifies the system that certain blocks of the LUN are no longer in use."

Furthermore, Rajan fails to teach "receiving, via the NAND controller, the empty-block identifier (see [0053]: punch hole command that include a logical block address

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field)." As discussed above, it appears that Rajan teaches the storage controller is on the computer or host side, which is supported by FIGS 8-9.

The cited references, either individually or in combination, fail to teach, suggest, anticipate, or render obvious receiving, via the NAND controller, the empty-block identifier, as required by independent claim 21. Furthermore, The cited references, either individually or in combination, fail to teach, suggest, anticipate, or render obvious receiving, via the host processor, an indication of deletion of a file at the host processor; creating, via the host processor, an empty-block identifier in response to the indication of deletion; receiving, via the NAND controller, the empty-block identifier, as required by independent claim 21.

In reference to dependent claims 25, 28-30 and 32, applicant disagrees with examiner's logic and conclusions. Applicant makes no admissions by not responding to each dependent claim and reserves the right to respond against these rejections in the future. Since claim 21 is non-obvious and allowable, claims 25, 28-30 and 32 are also nonobvious and allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Accordingly, applicant submits the examiner has failed to establish a *prima facie* case of obviousness for the claimed invention and respectfully requests allowance of claims 21, 25, 28-30 and 32, as amended.

Claims 22-23 stand rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (US2006/0020744) in view of Rajan (US2009/0248763), as applied to claims 21, 25, 28-30 and 32, and further in view of Adelmann (US2004/0003002).

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These rejections are traversed. In reference to dependent claims 22 and 23, applicant disagrees with the examiner's logic and conclusions. Applicant makes no admissions by not responding to each dependent claim and reserves the right to respond against these rejections in the future. Since claim 21 is non-obvious and allowable, claims 22 and 23 are also nonobvious and allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Accordingly, applicant submits the examiner has failed to establish a *prima facie* case of obviousness for the claimed invention and respectfully requests allowance of claims 22 and 23.

Claims 26-27 stand rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (US2006/0020744) and Rajan (US2009/0248763) as applied to claims 21, 25, 28-30 and 32 above, and further in view of Jensen (US2006/0120235).

These rejections are traversed. In reference to dependent claims 26 and 27, applicant disagrees with the examiner's logic and conclusions. Applicant makes no admissions by not responding to each dependent claim and reserves the right to respond against these rejections in the future. Since claim 21 is non-obvious and allowable, claims 26 and 27 are also nonobvious and allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Accordingly, applicant submits the examiner has failed to establish a *prima facie* case of obviousness for the claimed invention and respectfully requests allowance of claims 26 and 27.

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Claim 31 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (US2006/0020744) and Rajan (US2009/0248763) as applied to claims 21, 25, 28-30 and 32 above, and further in view, of "A New Flash Memory Management for Flash Storage System", hereinafter referred to as NPL 1.

This rejection is traversed. In reference to dependent claim 31, applicant disagrees with the examiner's logic and conclusions. Applicant makes no admissions by not responding to each dependent claim and reserves the right to respond against these rejections in the future. Since claim 21 is non-obvious and allowable, claim 31 is also nonobvious and allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Accordingly, applicant submits the examiner has failed to establish a *prima facie* case of obviousness for the claimed invention and respectfully requests allowance of claim 31.

Claims 34 and 35 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sinclair (US2006/0020744) in view of Rajan (US2009/0248763) and Adelmann (US2004/0003002) and as applied to claims 15-20 and 33 above, and further in view of Jensen (US2006/0120235).

These rejections are traversed. In reference to dependent claims 34 and 35, applicant disagrees with the examiner's logic and conclusions. Applicant makes no admissions by not responding to each dependent claim and reserves the right to respond against these rejections in the future. Since claim 15 is non-obvious and allowable, claims 34 and 35 are also nonobvious and allowable. If an independent claim is nonobvious under

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35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Accordingly, applicant submits the examiner has failed to establish a *prima facie* case of obviousness for the claimed invention and respectfully requests allowance of claims 34 and 35.

Other Claim Amendments

Applicant has amended dependent claims 16-17 and 34-35 to follow the antecedent basis of the claim elements in independent claim 15, as amended. Applicant has amended claims 22-23, 25-27, and 30 to follow the antecedent basis of the claim elements in independent claim 21, as amended. Applicant has amended claim 32 to properly depend on claim 29. The amendments to dependent claims 16-17, 22-23, 25-27, 30, 32 and 34-35 are not to overcome the cited art, individually or in combination. Accordingly, dependent claims 16-17, 22-23, 25-27, 30, 32 and 34-35 entitled to their full range of equivalents.

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CONCLUSION

In view of the foregoing, it is believed that all of the pending claims are in condition for allowance. Applicant therefore requests that the examiner withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Final Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this response is requested. If the examiner believes that a telephone conference would be useful in moving the application toward allowance, the examiner is encouraged to contact the attorney of record.

Respectfully submitted,

Dated: September 06, 2022

By: /David Wade Schnell/___
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PATENT AND TRADEMARK OFFICE

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Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/543,464	**09/09/2022 11:41:11 AM ET**	**10788.0722**

Title of Invention

Systems and Methods for Identifying Storage Resources That Are Not In Use

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4625	FILED BY	Thomas Lavan
PATENT CENTER #	60952857	FILING DATE	08/16/2019
CUSTOMER #	175872	FIRST NAMED INVENTOR	David Flynn
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
POA_16543464_090922.pdf	4	Power of Attorney	318 KB
373C_16543464_090922.pdf	4	Assignee showing of ownership per 37 CFR 3.73	401 KB

Digest

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373C_16543464_090922.pdf 34710B23031F5A1D4531A4FA8A5ABC61F3CCEC45B4B4B6936C966B83B96A4DECB0FF0AD4399FB8E68860CF87FC5B5DEB0C350204465A307FD9D2828E80EBCEF3

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/543,464	**09/19/2022 11:04:02 AM ET**	**10788.0722**

Title of Invention

Systems and Methods for Identifying Storage Resources That Are Not In Use

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4625	FILED BY	Thomas Lavan
PATENT CENTER #	60978943	FILING DATE	08/16/2019
CUSTOMER #	175872	FIRST NAMED INVENTOR	David Flynn
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
POA_16543464_091922.pdf	4	Power of Attorney	211 KB
373C_16543464_090922.pdf	4	Assignee showing of ownership per 37 CFR 3.73	401 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
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373C_16543464_090922.pdf	34710B23031F5A1D4531A4FA8A5ABC61F3CCEC45B4B4B6936 C966B83B96A4DECB0FF0AD4399FB8E68860CF87FC5B5DEB0 C350204465A307FD9D2828E80EBCEF3

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Number	16/543,464	**Docket Number**	
Filed	8/16/2019	**Group Art Unit**	2136
Examiner	Edward J. Dudek Jr.	**Customer No.**	
Application Title	Systems and Methods for Identifying Storage Resources That are Not in Use		
First Named Inventor	David Flynn		

Mail Stop **Assignment**
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This sheet adds one item to the chain of title for Statement under 3.73(c) filed for the above named application.

7. From Starboard Value Intermediate Fund LP, as Collateral Agent To Unification Technologies LLC

The document was recorded in the United States Patent and Trademark Office at Reel 058134, Frame 0001, or for which a copy thereof is attached.

Respectfully submitted,

/ **THOMAS J. LAVAN** /
By:_____

THOMAS J. LAVAN
Registration No. 58,487
Tel: (303) 301-4431

9/9/2022
Date: _____

Silicon Motion - Exhibit 1014
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Page 324 of 382

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/543,464	**10/10/2022 01:13:40 PM ET**	**UTP0001 US**

Title of Invention

Systems and Methods for Identifying Storage Resources That Are Not In Use

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4625	FILED BY	Thomas Lavan
PATENT CENTER #	61049131	FILING DATE	08/16/2019
CUSTOMER #	189660	FIRST NAMED INVENTOR	David Flynn
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
Maintenance_Fee_Address_Change_UTP0001-004_US_101022.pdf	2	Maintenance Fee Address Change	231 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	46789033
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	189660
Filer:	Thomas John Lavan/NGTECHLAW MaxVal
Filer Authorized By:	Thomas John Lavan
Attorney Docket Number:	UTP0001 US
Receipt Date:	11-OCT-2022
Filing Date:	16-AUG-2019
Time Stamp:	06:31:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	Public_File_History_9632727_Part1_EFS.pdf	24867775 e3ed511129d6052493a32762bbe835a5ab1bab7c	no	140

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Information:					
2	Non Patent Literature	Public_File_History_9632727_Part2_EFS.pdf	24541079 708b8488d4c47c524b217ee14cb2b8f700f54e20	no	137
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4	Non Patent Literature	SD_Specifications_PHYSICAL_LAYER_2005_134pgs_EFS.pdf	14411853 7857b56d741ca6c7f93c59781d5331f7eecd34df	no	134
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7	Non Patent Literature	Serial_ATA_Rev_2_5_27Oct2005_587pgs_Part3_EFS.pdf	15251920 bf6131578c9d75d0abcef17d440a0168430d9959	no	302
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Information:					

9	Non Patent Literature	Serial_ATA_High_Speed_Rev1_0_29Aug2001_307pgs_Part2_EFS.pdf	24120917 e56a57d41e25d26ab0bbcf4b6f7af208ee9413d1	no	142
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Information:					
10	Non Patent Literature	US60974470_Apparatus_System_2007_121pgs_EFS.pdf	20259746 523b13d5c4c6b4502cf91864938ad21ba1ce4edf	no	121
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11	Non Patent Literature	US60912728_REMOVE_DELETE_TECHNOLOGIES_2007_30pgs_EFS.pdf	3732279 b87c2dd6515f11c97935477ae9b07ce01e9d1da0	no	30
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12	Non Patent Literature	US60873111_Elemental_Blade_System_2006_104pgs_EFS.pdf	19670976 7a7a7e54628fd4fb4d68794c1772c9c666591243	no	104
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15	Non Patent Literature	BROWN_BREWER_NONVOLATILE_SEMICONDUCTOR_1998_618pgs_Part2_EFS.pdf	22023726 72ff14212e41158258ebadd9c225bef2546d2ecf	no	89
Warnings:					
Information:					

16	Non Patent Literature	BROWN_BREWER_NONVOLATILE_SEMICONDUCTOR_1998_618pgs_Part3_EFS.pdf	20743549 a6cfe5b6a6a822cc68ae79224cd8fbcdf45db52f	no	89
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Information:					
17	Non Patent Literature	BROWN_BREWER_NONVOLATILE_SEMICONDUCTOR_1998_618pgs_Part4_EFS.pdf	22361497 3a28c6d356f7b1f1e9c4682965f2c346c2abb607	no	89
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Information:					
18	Non Patent Literature	BROWN_BREWER_NONVOLATILE_SEMICONDUCTOR_1998_618pgs_Part5_EFS.pdf	22282526 fe110229952ed42c6a0b9078604df69e9202481d	no	89
Warnings:					
Information:					
19	Non Patent Literature	BROWN_BREWER_NONVOLATILE_SEMICONDUCTOR_1998_618pgs_Part6_EFS.pdf	24337051 c1c6fda064df8f65c0157ce58c9abcacdb599b62	no	89
Warnings:					
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20	Non Patent Literature	BROWN_BREWER_NONVOLATILE_SEMICONDUCTOR_1998_618pgs_Part7_EFS.pdf	21366163 194d0b53cb1748487e082e038b034ddb15394ff1	no	84
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21	Information Disclosure Statement (IDS) Form (SB08)	UTP0001_US_IDS_SB08_20221011054840.pdf	2044988 2be002c7699a41593680d12593079e84c43d1810	no	7
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
			Total Files Size (in bytes):	384173740	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	46789095
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	189660
Filer:	Thomas John Lavan/NGTECHLAW MaxVal
Filer Authorized By:	Thomas John Lavan
Attorney Docket Number:	UTP0001 US
Receipt Date:	11-OCT-2022
Filing Date:	16-AUG-2019
Time Stamp:	10:31:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	OA_EP097312433_25May2012_EFS.pdf	103116 7009a13c10bd8ca10d61f851f3791692572f1120	no	4

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2	Non Patent Literature	OA_EP108161084_30Sep2015_EFS.pdf	495613 97ca5639d48cf795f048c25aa5e10fad0988feb4	no	10
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3	Non Patent Literature	EESR_EP10816108_4Feb2014_7pgs_EFS.pdf	1156260 cf8ce341f087c53ed7d6f5fa0089efee1229c02f	no	7
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5	Non Patent Literature	OA_EP118481746_30Jun2015_EFS.pdf	215551 8a5e3904e6a40441d7322bc20f1ba49fa8918e3e	no	6
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6	Non Patent Literature	OA_EP118481746_02Apr2014_EFS.pdf	219022 855555b6118ea3763ab61140a284cb73caae3e12	no	7
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7	Non Patent Literature	OA_US12877971_18Apr2013_EFS.pdf	773739 42aef35239aca7d9edd4cf9d50923161b7dc13c4	no	22
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8	Non Patent Literature	OA_EP121768261_10Dec2012_EFS.pdf	149843 2613458e2f0ff6ea20a45a7824630fecc5d78f49	no	5
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9	Non Patent Literature	NOA_US13088211_29May2015_EFS.pdf	173480 84f26abb35a85a36af1e38222297a20943fdcdd1	no	5
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13	Non Patent Literature	IPRP_PCTUS2007086683_05Nov2009_10pgs_EFS.pdf	352501 9b12b928c1a31f84c72c4b160a3e5ffa113b2cf9	no	10
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33	Non Patent Literature	ISR_WO_PCTUS2009039673_6Jul2009_15pgs_EFS.pdf	625423 3fecd612feb9f2ec206d5b6b167336f523d631be	no	15
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34	Non Patent Literature	ISR_WO_PCTUS2010048321_28Apr2011_10pgs_EFS.pdf	410998 1452c3e275fc97a220fb147f54e31ac701df586a	no	10
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41	Non Patent Literature	IPRP_PCTUS2011053792_02Apr2013_EFS.pdf	171113 fda8fb0186418e661a82fa2546fa32fc473a34c1	no	4
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42	Non Patent Literature	ISR_PCTUS2011053792_04May2012_EFS.pdf	127281 d3f8665e0703b7c88940b31436f60b62f0f5c75b	no	3
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43	Non Patent Literature	WO_PCTUS2011053792_04May2012_EFS.pdf	134215 719d2013f5e89f5ede0097afe3519c0895607670	no	3
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44	Non Patent Literature	ISR_WO_PCTUS2011053795_04May2012_EFS.pdf	288171 2641eda5ba0adb8162fbe20ec3cacc717a51c202	no	7
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45	Non Patent Literature	IPRP_PCTUS2011065927_18Jun2013_4pgs_EFS.pdf	177665 303aec41803d4dd2c4f7965a53f732be0e9e66a0	no	4
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47	Non Patent Literature	IPRP_PCTUS2012024927_13Aug2013_9pgs_EFS.pdf	384318 2fc5bbefd8d5fc2171434162b0f729edf374102d	no	9
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55	Non Patent Literature	Dusseau_Removing_the_Cost_2010_5pgs_EFS.pdf	2529103 e69d07950f0124858465e064e2a4acffc3f2aeab	no	5
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58	Non Patent Literature	Bandulet_Evolution_File_Systems_2009_24pgs_EFS.pdf	9881181 a703786b3ab95a6952431a900290fae0850dc11a	no	24
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59	Non Patent Literature	OA_US60625495_05Nov2004_EFS.pdf	1110968 cf2b2696fd358ef23938d7084c1d33046efa5b7b	no	26
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	46789175
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	189660
Filer:	Thomas John Lavan/NGTECHLAW MaxVal
Filer Authorized By:	Thomas John Lavan
Attorney Docket Number:	UTP0001 US
Receipt Date:	11-OCT-2022
Filing Date:	16-AUG-2019
Time Stamp:	10:36:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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40	Non Patent Literature	OA_US13372430_06Aug2014_EFS.pdf	216122 707e835e68b2b3344cc54cc169470b8aba9a21a5	no	4
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41	Non Patent Literature	OA_US13372430_21Apr2014_EFS.pdf	756913 83748f5bd600c2464562c68578fad0e8d58be942	no	20
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42	Non Patent Literature	OA_US13372430_07Nov2013_EFS.pdf	520985 7e5ee6cf242b85d1bd2a31c61d12b92eb9fcf632	no	14
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43	Non Patent Literature	OA_US13406287_02Jun2014_EFS.pdf	163951 b931316de93629b1b67793239b397d6f8be059c6	no	4
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44	Non Patent Literature	OA_US13406287_16Dec2013_EFS.pdf	159992 21dd347ddf77522fd659373f49b63dd4ceeced3a	no	4
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45	Non Patent Literature	NOA_US13600077_30Apr2013_EFS.pdf	420633 9448285763979065c4a998d1bf605e438e1db36f	no	9
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46	Non Patent Literature	OA_US13600077_07Jan2013_EFS.pdf	300728 179f38d362738ba2d296ab4f9815ae0bdd5a6734	no	8
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47	Non Patent Literature	NOA_US13607486_11Jul2013_EFS.pdf	495948 100cb1328069b3b5487cbd75b2ec93cb20298fd5	no	11
Warnings:					
Information:					
48	Non Patent Literature	OA_US13607486_10Jan2013_EFS.pdf	383120 efbe56e692b148784857019cbf94f08588b3c66	no	11
Warnings:					
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49	Non Patent Literature	OA_US13652427_20Nov2014_EFS.pdf	199614 cbce4c57433d0f712a72a248f542310079f6ee8c	no	6
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50	Non Patent Literature	OA_US13730602_15Jan2015_EFS.pdf	699582 28af88f5a9e1af92e8ca61fa2fc5496c9819b81f	no	26
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51	Non Patent Literature	OA_US13776389_20Jun2014_EFS.pdf	2803978 b08b80a229092dce17acd7f8014a53e0ce94c0dd	no	71
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52	Non Patent Literature	OA_US13776389_16Dec2013_EFS.pdf	1571320 9f34053ffa55bda0f9c0a843e1f20c0e4c6a4dac	no	44
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53	Non Patent Literature	NOA_US13776406_13May2014_EFS.pdf	644051 01c4f3e70a1cef3a578467d7c3d45285dda9c384	no	15
Warnings:					
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54	Non Patent Literature	OA_US13776406_06Nov2013_EFS.pdf	1649585 bd6862d3d6e323bdea0e9249450ff5f731e29e99	no	43
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55	Non Patent Literature	OA_US13800628_05Dec2014_EFS.pdf	416824 d18b2a7f84594a784acf8bc61db3b82e87b1b6bb	no	11
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Information:					
56	Non Patent Literature	OA_US13830652_12Aug2014_EFS.pdf	334782 9b271a2b2ed3535e1d2c300538e33ed22f91b7dc	no	10
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Information:					
57	Non Patent Literature	OA_US13834955_08Sep2014_EFS.pdf	956899 e692918c1a332e00def7a311b55145cc8cc40cb1	no	23
Warnings:					
Information:					

58	Non Patent Literature	OA_US13834955_04Apr2014_EFS.pdf	772978 601535faa5c6db710df375e371f9922db137d51b	no	19
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59	Non Patent Literature	NOA_US13836826_30Jul2015_EFS.pdf	446658 ef1375099825b207a3a64d0cd75b787e96fa2f47	no	8
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Information:					
60	Non Patent Literature	OA_US13836826_24Feb2015_EFS.pdf	749948 74382cf36cdcdb7e6ceed102f12992d84054152b	no	18
Warnings:					
Information:					
		Total Files Size (in bytes):	29518902		

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
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Electronic Acknowledgement Receipt

EFS ID:	46789156
Application Number:	16543464
International Application Number:	
Confirmation Number:	4625
Title of Invention:	Systems and Methods for Identifying Storage Resources That Are Not In Use
First Named Inventor/Applicant Name:	David Flynn
Customer Number:	189660
Filer:	Thomas John Lavan/NGTECHLAW MaxVal
Filer Authorized By:	Thomas John Lavan
Attorney Docket Number:	UTP0001 US
Receipt Date:	11-OCT-2022
Filing Date:	16-AUG-2019
Time Stamp:	10:34:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	Ranaweera_SAT_Write_Same_2005_2pgs_EFS.pdf	534874 25d6b0578de861d615ddc47a2093d78ad58acdb3	no	2
Warnings:					

Information:					
2	Non Patent Literature	Randal_Understanding_Logging_2009_12pgs_EFS.pdf	4228592 67629edbf1f9a063ea6302ddcb6ed1c678bff5c9	no	12
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Information:					
3	Non Patent Literature	Renata_Tutorial_RDMA_Model_15Sep2006_16pgs_EFS.pdf	7604504 d34a85355380f83ad2399d3aecdf8b87d0d87cef	no	16
Warnings:					
Information:					
4	Non Patent Literature	Rose_FPGA_PCIe_Bandwidth_2010_7pgs_EFS.pdf	2933810 d3535275c7d648ea2ac986b20cf59ca26331050a	no	7
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5	Non Patent Literature	Rosenblum_The_Design_and_Implementatio_1992_15pgs_EFS.pdf	6040260 2bddce2f25e8b43c69e5b277f64b36e0c7820005	no	15
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6	Non Patent Literature	Russinovich_Windows_Internals_2009_Part1_209pgs_EFS.pdf	22984806 995593df22a1d29f39e2ffafece90e7874af37b9	no	105
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Information:					
7	Non Patent Literature	Russinovich_Windows_Internals_2009_Part2_209pgs_EFS.pdf	15059923 207d98aed1cb3aad904a6ce13c705f0f9fb9bd57	no	104
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8	Non Patent Literature	Salcic_PROTOS_microcontroller_1997_8pgs_EFS.pdf	2530298 9997cd022a35b9991a7c87bf46f77ad80edb4d9d	no	8
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9	Non Patent Literature	SANDISK_Extreme_FFS_2009_2pgs_EFS.pdf	707102 5765a731085f7a04ef68b411f937d325708e420e	no	2
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10	Non Patent Literature	SanDisk_Extreme_FFS3_2009_3pgs_EFS.pdf	1108116 5cc0b5e9f495958c00abe1fbdfc8e7c1723e2532	no	3
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11	Non Patent Literature	Sandisk_SanDisk_Introduces_Extreme_2009_3pgs_EFS.pdf	1120748 d4b5ff982c2819ea26c18545fb9a1472b8b66c71	no	3
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12	Non Patent Literature	Savov_Viking_Modular_27Aug2010_11pgs_EFS.pdf	2552515 78266c3398d076d6ada346b3d84c4a600c2f42c6	no	11
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13	Non Patent Literature	Sears_Stasis_Flexible_Transactional_2010_176pgs_Part1_EFS.pdf	20465126 aa78e4efae4ce6ffcffbf57d9207f5bd8d73d1a4	no	58
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14	Non Patent Literature	Sears_Stasis_Flexible_Transactional_2010_176pgs_Part2_EFS.pdf	24064470 a875bcbd4a0e17391fac139e3704fe838e6adfe3	no	58
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15	Non Patent Literature	Sears_Stasis_Flexible_Transactional_2010_176pgs_Part3_EFS-.pdf	24110488 e890cdb25df7d7c3022e44ecc5e019881c540592	no	60
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16	Non Patent Literature	Sears_Stasis_Flexible_2006_PP_29_44_EFS.pdf	5725914 018ebdf4956b5599fde196e53e94a8f371705121	no	16
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17	Non Patent Literature	Seltzer_Transaction_Support_1993_8pgs_EFS.pdf	6072572 5738d071e32d20bcf7ddb4af199b1d0a31651036	no	8
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18	Non Patent Literature	Seltzer_File_System_Performance_1992_133pgs_Part3_EFS.pdf	11535720 88cdfd5c593df7c1c8076cf4002c0631e3e8b61e	no	30
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19	Non Patent Literature	Seltzer_File_System_Performance_1992_133pgs_Part2_EFS.pdf	12775569 c14f75e9898198d493cfc6fa35803ae2dde58ece	no	35
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20	Non Patent Literature	Seltzer_File_System_Performance_1992_133pgs_Part1_EFS.pdf	12104760 2aa0651cbf23a123fb4c69ab408659558b611b37	no	35
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21	Non Patent Literature	Seltzer_File_System_Performance_1992_133pgs_Part4_EFS.pdf	13151570 719e5b8b0daca89f34d71c3dd171e51252a41aa3	no	33
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23	Non Patent Literature	Seltzer_Transaction_Support_1990_12pgs_EFS.pdf	2683770 174e07d58dee6da30f4da64175380b01eb6fc7ca	no	12
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24	Non Patent Literature	Shimpi_SSD_Anthology_18Mar2009_5pgs_EFS.pdf	1537816 993ce146ac059c03d3337e5fd30d26e5bc85d087	no	5
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25	Non Patent Literature	Shrout_Gigabyte_iRAM_Solid_5Apr2006_8pgs_EFS.pdf	1491217 ca2de0a2225dff3198b57cc7fd403e5676d2605b	no	8
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26	Non Patent Literature	Shu_Data_Set_Management_2007_9pgs_EFS.pdf	1838823 8ec5050d4ed56ea93e7f32211640d4467baa311c	no	9
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27	Non Patent Literature	Small_PCI_Bus_Master_1995_5pgs_EFS.pdf	976491 5fde2ab9373a4d8813bf2d74205cbb449063fbdb	no	5
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28	Non Patent Literature	Spillane_Enabling_Transactional_2009_14pgs_EFS.pdf	7854017 3f074efa5372bf37722f857e4ebfc0d8ccc4e5a8	no	14
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29	Non Patent Literature	Staf_Adaptation_of_OSEck_2007_93pgs_EFS.pdf	23948873 ded225ad5950c068fefbc1066ee459d87281d109	no	93
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30	Non Patent Literature	Stodolsky_Parity_Logging_Overcoming_1993_12pgs_EFS.pdf	2934382 a4be7fe10839f9942b97cffdf61254d40af3f559	no	12
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31	Non Patent Literature	Stokes_Intels_New_Flash_2009_2pgs_EFS.pdf	867026 95e69aca6e0e4e2f6ea1ec6e56f7d3d3e44895ae	no	2
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32	Non Patent Literature	Suh_A33_V32Mb_NAND_Flash_1995_3pgs_EFS.pdf	1134896 6ce1cf7ebb6b9c59fc2441249d5a1fc2ed8f20dd	no	3
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33	Non Patent Literature	Jain_Point_to_Point_Connectivity_2007_17pgs_EFS.pdf	4949589 b79cec6fefbfc54fc911c471e133152f456ae409	no	17
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34	Non Patent Literature	Tal_NAND_vs_NOR_2002_5pgs_EFS.pdf	1772072 faefc9a63e025ba820d3691e97a646b2366d4ca0	no	5
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36	Non Patent Literature	OA_US60797127_03May2006_EFS.pdf	5002335 c39522c51d4638914f14f930add33b13342d7177	no	133
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37	Non Patent Literature	NOA_US11952091_28Jun2012_EFS.pdf	335333 e6c4779e06b65e5635774225913962 9e26ed928f	no	5
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38	Non Patent Literature	OA_US11952095_14Feb2012_EFS.pdf	449929 e951e4bd8e09223c4db7552276edf99aa8f8bdf7	no	13
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39	Non Patent Literature	OA_US11952095_08Jun2011_EFS.pdf	448859 d47c8e181dd226319722113eb1befd6186fb84de	no	12
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42	Non Patent Literature	OA_US11952098_18Sep2012_EFS.pdf	395996 cf2bc214ff34fe7a65fb205a099d1615294e18d8	no	11
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44	Non Patent Literature	OA_US11952098_07Jan2011_EFS.pdf	374600 0d25c662d7f605a648b41e697212d25a5e6e41f4	no	11
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46	Non Patent Literature	OA_US11952101_22Dec2011_EFS.pdf	446910 ef4f258d8381ee6ddd4b7fdfdd3e3796de53fe91	no	13
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47	Non Patent Literature	OA_US11952101_06Jan2011_EFS.pdf	458406 7bdbd215f7ee530f9e88a07973bb78630b21346d	no	13
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48	Non Patent Literature	OA_US11952109_01Jul2011_EFS.pdf	306309 318adc044b5a2eb3b390522343628559418509 0f	no	10
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49	Non Patent Literature	OA_US11952109_17Mar2011_EFS.pdf	246108 6b6fc020d9231db688f73d1efabf87756ca630f2	no	8
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50	Non Patent Literature	OA_US11952115_26Apr2011_EFS.pdf	334250 861029d5bb5a4248236b9e9d68edd8d5627350e9	no	5
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51	Non Patent Literature	OA_US11952115_10Mar2010_EFS.pdf	408680 15d22832303ec4fa38fff16df45596052de77a02	no	12
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52	Non Patent Literature	OA_US11952120_20Dec2010_EFS.pdf	257272 7bbeee89a9a1ddaccdd3e1506b55422c75b0b99f	no	4
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53	Non Patent Literature	OA_US11952120_20Apr2010_EFS.pdf	504290 48ef14f86d7057455c9d3e6caa9d7124645e3351	no	14
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54	Non Patent Literature	OA_US11952120_13Aug2010_EFS.pdf	488392 66f2949b11b2521993aa8cec6cab557031c64158	no	15
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55	Non Patent Literature	OA_US11952121_19Dec2016_EFS.pdf	1138318 00a4815c54422edf3196d3950488b9ee038244fa	no	33
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56	Non Patent Literature	OA_US11952123_05Oct2010_EFS.pdf	485995 8a0dea6139444460d602a03ebb32228eeec832aac	no	15
Warnings:					
Information:					
57	Non Patent Literature	NOA_US11952123_08Apr2011_EFS.pdf	335708 86a8cd9a2875d7471bbcd4092b50dbe12da7c5b5	no	5
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58	Non Patent Literature	NOA_US11952123_19Jan2011_EFS.pdf	357699 56f2d5ae0f5f2024a1b3b8c27e9868827060e220	no	8
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59	Non Patent Literature	OA_US11952123_05May2010_EFS.pdf	464954 5289c25432758b49428c6a6b3f9162133c101672	no	14
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Information:					
60	Non Patent Literature	OA_US12098427_19Jun2012_EFS.pdf	258385 0e824c64f87920f78876a35e9e8a8eed5b99215d	no	7
Warnings:					
Information:					
		Total Files Size (in bytes):	270162156		

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<u>New International Application Filed with the USPTO as a Receiving Office</u>
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189660 7590 10/26/2022

Unification Technologies LLC
6136 Frisco Square Boulevard
Suite 400
Frisco, TX 75034

EXAMINER
DUDEK JR, EDWARD J

ART UNIT	PAPER NUMBER
2136	

DATE MAILED: 10/26/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/543,464	08/16/2019	David Flynn	UTP0001 US	4625

TITLE OF INVENTION: Systems and Methods for Identifying Storage Resources That Are Not In Use

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	01/26/2023

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THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

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III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

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PTOL-85 (Rev. 02/11)

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Frisco, TX 75034

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(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/543,464	08/16/2019	David Flynn	UTP0001 US	4625

TITLE OF INVENTION: Systems and Methods for Identifying Storage Resources That Are Not In Use

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	01/26/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
DUDEK JR, EDWARD J	2136	711-103000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Silicon Motion - Exhibit 1014
Silicon Motion v. UTL - IPR2024-00199
Page 364 of 382

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/543,464	08/16/2019	David Flynn	UTP0001 US	4625

189660 7590 10/26/2022

Unification Technologies LLC
6136 Frisco Square Boulevard
Suite 400
Frisco, TX 75034

EXAMINER	
DUDEK JR, EDWARD J	
ART UNIT	PAPER NUMBER
2136	

DATE MAILED: 10/26/2022

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/543,464	Applicant(s) Flynn et al.	
	Examiner EDWARD J DUDEK JR	Art Unit 2136	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to the RCE filed 06 September 2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 15-23 and 25-35 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/EDWARD J DUDEK JR/
Primary Examiner, Art Unit 2136

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

This Office Action is responsive to the reply filed 06 September 2022.

Claims 15-23 and 25-35 are pending and have been presented for examination.

Claims 1-14 and 24 have been cancelled.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06 September 2022 has been entered.

Allowable Subject Matter

Claims 15-23 and 25-35 are allowed.

The following is an examiner's statement of reasons for allowance: the amendments to the claims, along with applicants' arguments, are persuasive and have overcome the cited references.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWARD J DUDEK JR whose telephone number is (571)270-1030. The examiner can normally be reached Monday - Friday, 8:00A-4:00P.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Rones can be reached on 571-272-4085. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EDWARD J DUDEK JR/
Primary Examiner, Art Unit 2136

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/543,464	11/08/2022 09:26:06 AM ET	UTP0001 US

Title of Invention

Systems and Methods for Identifying Storage Resources That Are Not In Use

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4625	FILED BY	Thomas Lavan
PATENT CENTER #	61154042	AUTHORIZED BY	-
CUSTOMER #	189660	FILING DATE	08/16/2019
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	David Flynn

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 0845	E2022A8026424362	Thomas Lavan

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1501	UTILITY ISSUE FEE	1200.00	1	1200.00
			TOTAL AMOUNT:	$1,200.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage

submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/543,464	**11/08/2022 09:26:06 AM ET**	**UTP0001 US**

Title of Invention

Systems and Methods for Identifying Storage Resources That Are Not In Use

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4625	FILED BY	Thomas Lavan
PATENT CENTER #	61154042	FILING DATE	08/16/2019
CUSTOMER #	189660	FIRST NAMED INVENTOR	David Flynn
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
Issue_Fee_Payment_UTP0001_US_110822.pdf	2	Issue Fee Payment (PTO-85B)	276 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
Issue_Fee_Payment_UTP0001_US_110822.pdf	22916E8D275032868EB9BBF4025DCE570E0D023713CE849642 1391346C384A8A6E10889761EA5E3CF5EE1C049990E76A2B45 825CD802271368235C47320733BA

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized

by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/543,464	08/16/2019	David Flynn	UTP0001 US	4625

189660 7590 03/23/2023

Unification Technologies LLC
6136 Frisco Square Boulevard
Suite 400
Frisco, TX 75034

EXAMINER	
DUDEK JR, EDWARD J	

ART UNIT	PAPER NUMBER
2136	

NOTIFICATION DATE	DELIVERY MODE
03/23/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

T_Lavan@msn.com
myuspto@appcoll.com

Corrected ***Notice of Allowability***	**Application No.** 16/543,464	**Applicant(s)** Flynn et al.	
	Examiner EDWARD J DUDEK JR	**Art Unit** 2136	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to the RCE filed 06 September 2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 15-23 and 25-35 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☑ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/EDWARD J DUDEK JR/
Primary Examiner, Art Unit 2136

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

35. (Currently amended) The method of claim 15, further comprising removing a mapping between the logical identifier and the physical storage location from the index of mappings; and erasing the data stored in the physical storage location.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWARD J DUDEK JR whose telephone number is (571)270-1030. The examiner can normally be reached Monday - Friday, 8:00A-4:00P.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Rones can be reached on 571-272-4085. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EDWARD J DUDEK JR/
Primary Examiner, Art Unit 2136

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/543,464	**04/01/2023 03:18:47 PM ET**	**UTP0001 US**

Title of Invention

Systems and Methods for Identifying Storage Resources That Are Not In Use

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4625	FILED BY	Thomas Lavan
PATENT CENTER #	61853624	FILING DATE	08/16/2019
CUSTOMER #	189660	FIRST NAMED INVENTOR	David Flynn
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 3

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
Notice_to_File_Corrected_Application_Papers_UTP0001_US_033023.PDF	3	Miscellaneous Incoming Letter	121 KB
Replacement_Drawings_UTP0001_US_040123.pdf	4	Drawings-only black and white line drawings	66 KB
Response_to_Notice_to_File_Corrected_Application_Papers_UTP0001_US_040123.pdf	1	Post Allowance Communication - Incoming	349 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
Notice_to_File_Corrected_Application_Papers_UTP0001_US_033023.PDF	43BAE2DE81037D89DF50666AFF415B315EC687A2F9761926996E52E99DA4098E6A816CB10BFCE2D4E724AF03499B5BD1D13F59BDE0E3E6E034E97D4296098AAB
Replacement_Drawings_UTP0001_US_040123.pdf	C56CAF612640FE6164E482DADAA47EFD2FA05D5F9531C2B75C7786B42D610C501AE2E112AE3D5CFE47A5F4497377EE83272D84F6AD966EC8190804FBE0E25506
Response_to_Notice_to_File_Corrected_Application_Papers_UTP0001_US_040123.pdf	881844533C1F30F89F8F9D1366904CD4AC39795AEF2AD1873D06F6E5B4A42984D5E22EDF75231DC789A73A1F480FDC34F06403BA462E680F9177A7B14CD8E239

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/543,464	05/02/2023	11640359	UTP0001 US	4625

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ISSUE NOTIFICATION

The projected patent number and issue date are specified above. The patent will issue electronically. The electronically issued patent is the official patent grant pursuant to 35 U.S.C. § 153. The patent may be accessed on or after the issue date through Patent Center at https://patentcenter.uspto.gov/. The patent will be available in both the public and the private sides of Patent Center. Further assistance in electronically accessing the patent, or about Patent Center, is available by calling the Patent Electronic Business Center at 1-888-217-9197.

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Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

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