

# American National Standard

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(Vol.1)

*for Information Technology –  
AT Attachment with Packet Interface - 7  
Volume 1 - Register Delivered Command Set,  
Logical Register Set  
(ATA/ATAPI-7 V1)*

**Developed by**



*Where IT all begins*





American National Standard  
for Information Technology –

AT Attachment with Packet Interface - 7  
Volume 1 - Register Delivered Command Set,  
Logical Register Set  
(ATA/ATAPI-7 V1)

Secretariat

**Information Technology Industry Council**

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**Abstract**

This standard specifies the AT Attachment Interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers, and suppliers of intelligent storage devices. It includes the Packet Command feature set implemented by devices commonly known as ATAPI devices. It also includes the Serial Transport Protocols and Physical Interconnect for AT Attachment devices commonly known as Serial ATA.

This standard maintains a high degree of compatibility with the AT Attachment Interface with Packet Interface - 6 (ATA/ATAPI-6), ANSI INCITS 361-2002, and while providing additional functions, is not intended to require changes to presently installed devices or existing software.

## American National Standard

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**Foreword** (This foreword is not part of American National Standard  
ANSI INCITS 397-2005 (Vol.1).)

This standard defines the AT Attachment with Packet Interface (ATAPI). The standard includes the command set and two transport protocols to support parallel and serial physical interconnects. The document is partitioned into three volumes:

Volume 1 - Register Delivered Command Set, Logical Register Set  
(ATA/ATAPI-7 V1)

Volume 2 - Parallel Transport Protocols and Physical Interconnect  
(ATA/ATAPI-7 V2)

Volume 3 - Serial Transport Protocols and Physical Interconnect  
(ATA/ATAPI-7 V3)

The document is partitioned in this way to separate the command set (Volume 1) for ease of reference and maintenance. The command set is the same for both the parallel transport (Volume 2) and the serial transport (Volume 3).

Volumes 1 and Volume 2 were substantially derived from the prior version of this specification (ATA/ATAPI-6, ANSI INCITS 361-2002). Volume 3 is new material defining the serial transport of the ATA/ATAPI interface.

All three volumes have a section that includes introductory material, a common glossary, and an index to the major clauses of the other two volumes. After Clause 3 in each of the volumes, the material is volume specific. Within each volume, references are made to other volumes, typically by volume and major clause number.

In order to implement the standard for a parallel transport, it is necessary to comply with both Volume 1 and Volume 2. In order to implement the serial transport, it is necessary to comply with both Volume 1 and Volume 3. It should be recognized, however, that the serial transport as described in Volume 3 relies heavily on logical interconnect and protocol concepts and requirements described in Volume 2. These concepts are called "parallel emulation" in Volume 3. In some cases references are made to the parallel implementation of ATA, which refers to the parallel transport (Volume 2). The reader is strongly advised to consult all three volumes when implementing the serial transport.

This volume (ATA/ATAPI-7 V1) contains the command feature sets for ATA. This volume defines structures used by the parallel implementation of ATA and the serial implementation of ATA. The command descriptions are in alphabetical order, with a cross reference by command codes in Annex B.

Requests for interpretation, suggestions for improvement and addenda, or defect reports are welcome. They should be sent to the INCITS Secretariat, ITI, 1250 Eye Street, NW, Suite 200, Washington, DC 20005-3922.

This standard was processed and approved for submittal to ANSI by the International Committee for Information Technology Standards (INCITS). Committee approval of this standard does not necessarily imply that all committee members voted for approval. At the time it approved this standard, INCITS had the following members:

Karen Higginbottom, Chair  
Jennifer Garner, Secretary

| <i>Organization Represented</i>                            | <i>Name of Representative</i> |
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Jim Hatfield, Vice-Chairman  
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| Tom Barrett      | Phil Gardner       | Marc Noblitt      |
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| Stephen Finch    | John Masiewicz     | Kanting Tsai      |
| Lance Flake      | Conrad Maxwell     | Karen Zelenko     |
|                  | Pete McLean        |                   |

## **Introduction**

This standard encompasses the following:

### **Volume 1**

Clause 1 describes the scope.

Clause 2 provides normative references for the entire standard.

Clause 3 provides definitions, abbreviations, and conventions used within the entire standard.

Clause 4 describes the general operating requirements of the command layer.

Clause 5 describes the I/O registers.

Clause 6 contains descriptions of the commands.

Clauses 7 through 12 point to the material in Volume 2.

Clauses 13 through 19 point to material in Volume 3.

### **Volume 2**

Clause 1 describes the scope.

Clause 2 provides normative references for the entire standard.

Clause 3 provides definitions, abbreviations, and conventions used within the entire standard.

Clauses 4, 5, and 6 point to the material in Volume 1.

Clause 7 contains the electrical and mechanical characteristics.

Clause 8 contains the signal descriptions.

Clause 9 describes the general operating requirements of the physical, data link, and transport layers.

Clause 10 contains describes register addressing.

Clause 11 contains the transport protocols.

Clause 12 contains the interface timing diagrams.

Clauses 13 through 19 point to material in Volume 3.

### **Volume 3**

Clause 1 describes the scope.

Clause 2 provides normative references for the entire standard.

Clause 3 provides definitions, abbreviations, and conventions used within the entire standard.

Clauses 4, 5, and 6 point to the material in Volume 1.

Clauses 7 through 12 point to the material in Volume 2.

Clause 13 contains a general overview of the serial interface.

Clause 14 describes the serial physical layer.

Clause 15 describes the serial link layer.

Clause 16 describes the serial transport layer.

Clause 17 describes the device command layer protocol for the serial interface.

Clause 18 describes the host command layer protocol for the serial interface.

Clause 19 describes the serial interface host adapter register interface.

Clause 20 describes the serial interface error handling.

American National Standard  
for Information Technology –

## AT Attachment with Packet Interface – 7

### Volume 1 – Register Delivered Command Set, Logical Register Set (ATA/ATAPI-7 V1)

#### 1 Scope

This standard specifies the AT Attachment Interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers, and suppliers of intelligent storage devices.

Volume 1 defines the register delivered commands used by devices implementing the standard. Volume 2 defines the connectors and cables for physical interconnection between host and storage device, the electrical and logical characteristics of the interconnecting signals, and the protocols for the transporting of commands, data, and status over the interface for the parallel interface. Volume 3 defines the connectors and cables for physical interconnection between host and storage device, the electrical and logical characteristics of the interconnecting signals, and the protocols for the transporting of commands, data, and status over the interface for the serial interface. Figure 1 shows the relationship of these documents. For devices implementing the PACKET command feature set, additional command layer standards are listed in Table 1 and described in Clause 2.

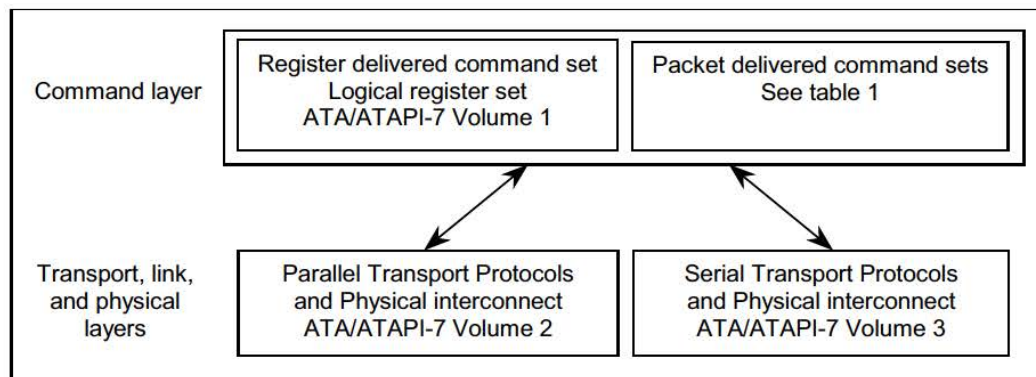


Figure 1 - ATA document relationships

**Table 1 - PACKET delivered command sets**

|                                                                    |
|--------------------------------------------------------------------|
| Standard                                                           |
| SCSI Primary Commands (SPC)                                        |
| SCSI Primary Commands - 2 (SPC-2)                                  |
| SCSI Primary Commands - 3 (SPC-3)                                  |
| SCSI Block Commands (SBC-2)                                        |
| SCSI Stream Commands (SSC)                                         |
| Multimedia Commands (MMC)                                          |
| Multimedia Commands - 2 (MMC-2)                                    |
| Multimedia Commands - 3 (MMC-3)                                    |
| Multimedia Commands - 4 (MMC-4)                                    |
| ATAPI for Removable Media (SFF8070I)                               |
| ATA Packet Interface (ATAPI) for Streaming Tape QIC-157 revision D |

This standard maintains compatibility with the AT Attachment with Packet Interface - 6 standard (ATA/ATAPI-6), ANSI INCITS 361-2002, and while providing additional functions, is not intended to require changes to presently installed devices or existing software.

## 2 Normative references

The following standards contain provisions that, through reference in the text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

Copies of the following documents can be obtained from ANSI: Approved ANSI standards, approved and draft international and regional standards (ISO, IEC, CEN/CENELEC, ITUT), and approved and draft foreign standards (including BSI, JIS, and DIN). For further information, contact ANSI Customer Service Department at 212-642-4900 (phone), 212-302-1286 (fax), or via the World Wide Web at <http://www.ansi.org>.

Additional availability contact information is provided below as needed.

### 2.1 Approved references

The following approved ANSI standards, approved international and regional standards (ISO, IEC, CEN/CENELEC, ITUT), may be obtained from the international and regional organizations who control them.

#### 2.1.1 ANSI References

|                                                              |                                |
|--------------------------------------------------------------|--------------------------------|
| SCSI-3 Block Commands (SBC)                                  | [ANSI INCITS 306-1998 (R2003)] |
| SCSI-3 Primary Commands (SPC)                                | [ANSI INCITS 301-1997 (R2002)] |
| SCSI-3 Streaming Commands (SSC)                              | [ANSI INCITS 335-2000]         |
| Multimedia Commands (MMC)                                    | [ANSI INCITS 304-1997 (R2002)] |
| Multimedia Commands - 2 (MMC-2)                              | [ANSI INCITS 333-2000]         |
| Multimedia Commands - 3 (MMC-3)                              | [ANSI INCITS 360-2002]         |
| Protected Area Run Time Interface Extensions (PARTIES)       | [ANSI INCITS 346-2001]         |
| SCSI Primary Commands - 2 (SPC-2)                            | [ANSI INCITS 351-2001]         |
| ATA Attachment with Packet Interface Extension (ATA/ATAPI-4) | [ANSI INCITS 317-1998] (R2003) |

#### 2.1.2 ISO References

|                                                                                                              |                      |
|--------------------------------------------------------------------------------------------------------------|----------------------|
| Control and Status Register (CSR) Architecture for microprocessor buses                                      | [ISO/IEC 13213:1994] |
| Acoustics - Measurement of airborne noise emitted by information technology and telecommunications equipment | [ISO 7779: 1999]     |

### 2.2 References under development

At the time of publication, the following referenced standards were still under development. For information on the current status of the document, or regarding availability, contact the relevant standards body or other organization as indicated.

|                                   |              |
|-----------------------------------|--------------|
| SCSI Block Commands - 2 (SBC-2)   | [T10/1417-D] |
| SCSI Primary Commands - 3 (SPC-3) | [T10/1416-D] |
| ATAPI for Rewritable Media        | [SFF8070i]   |
| Multimedia Commands - 4 (MMC-4)   | [T10/1545D]  |

For more information on the current status of the T10 documents, contact INCITS. To obtain copies of T10 or SFF documents, contact Global Engineering. To obtain copies of these documents, contact Global Engineering or INCITS. Additional information may be available at <http://www.t10.org> and <http://www.t13.org>.

### 2.3 Other references

The following standards and specifications are also referenced.

PC Card Standard, February 1995, PCMCIA (68-pin Connector)

For the PC Card Standard published by the Personal Computer Memory Card International Association, contact PCMCIA at 408-433-2273 or <http://www.pc-card.org>.

CompactFlash™ Association Specification, Revision 1.4

For the CompactFlash™ Association Specification published by the CompactFlash™ Association, contact the CompactFlash™ Association at <http://www.compactflash.org>.

ATA Packet Interface (ATAPI) for Streaming Tape QIC-157 revision D

For QIC specifications published by Quarter-Inch Cartridge Drive Standards, Inc., contact them at 805 963-3853 or <http://www.qic.org>.

EIA-364-09 TP-09C - Durability test procedure for electrical connectors and contacts

EIA-364-13 Mating and unmating forces test procedures for electrical connectors

EIA-364-17 TP-17B - Temperature life with or without electrical load test procedure for electrical connectors and sockets

EIA-364-18 Visual and dimensional inspection for electrical connectors

EIA-364-20 TP-20B - Withstanding voltage test procedure for electrical connectors, sockets, and coaxial contacts

EIA-364-21 Insulation resistance test procedure for electrical connectors, sockets, and coaxial contacts

EIA-364-23 Low level contact resistance test procedure for electrical connectors and sockets

EIA-364-27 Mechanical pulse (specified pulse) for electrical connectors

EIA-364-28 TP-28D Vibration test procedure for electrical connectors and sockets

EIA-364-31 Humidity test procedure for electrical connectors and sockets

EIA-364-32 Thermal shock (temperature cycling) test procedure for electrical connectors and sockets

EIA-364-38 TP-38B - Cable pull-out test procedure for electrical connectors

EIA-364-41 TP-41C - Cable flexing test procedure for electrical connectors

EIA-364-65 TP-65A Mixed flowing gas

For EIA specifications, contact them at <http://www.eia.org>.

### 3 Definitions, abbreviations, and conventions

#### 3.1 Definitions and abbreviations

For the purposes of this standard, the following definitions apply:

- 3.1.1 ASCII Character:** Designates 8-bit value that is encoded using the ASCII Character set.
- 3.1.2 acoustics:** Measurement of airborne noise emitted by information technology and telecommunications equipment [ISO 7779:1999(E)]
- 3.1.3 ATA (AT Attachment):** ATA defines the physical, electrical, transport, and command protocols for the internal attachment of storage devices to host systems.
- 3.1.4 ATA-1 device:** A device that complied with ANSI X3.221-1994, the AT Attachment Interface for Disk Drives. ANSI X3.221-1994 has been withdrawn.
- 3.1.5 ATA-2 device:** A device that complied with ANSI X3.279-1996, the AT Attachment Interface with Extensions. ANSI X3.279-1996 has been withdrawn.
- 3.1.6 ATA-3 device:** A device that complies with ANSI INCITS 298-1997, the AT Attachment-3 Interface. ANSI INCITS 298-1997 has been withdrawn.
- 3.1.7 ATA/ATAPI-4 device:** A device that complies with ANSI INCITS 317-1998, AT Attachment Interface with Packet Interface Extensions-4.
- 3.1.8 ATA/ATAPI-5 device:** A device that complies with ANSI INCITS 340-2000, the AT Attachment with Packet Interface-5.
- 3.1.9 ATA/ATAPI-6 device:** A device that complies with ANSI INCITS 361-2002, the AT Attachment with Packet Interface-6.
- 3.1.10 ATA/ATAPI-7 device:** A device that complies with this standard.
- 3.1.11 ATAPI (AT Attachment Packet Interface) device:** A device implementing the Packet Command feature set.
- 3.1.12 AU (Allocation Unit):** The minimum number of logically contiguous sectors on the media as used in the Streaming feature set. An Allocation Unit may be accessed with one or more requests.
- 3.1.13 AV (Audio-Video):** Audio-Video applications use data that is related to video images and/or audio. The distinguishing characteristic of this type of data is that accuracy is of lower priority than timely transfer of the data.
- 3.1.14 backchannel:** When transmitting a FIS, the backchannel is the receive channel.
- 3.1.15 BER (bit error rate):** The statistical probability of a transmitted encoded bit being erroneously received in a communication system.
- 3.1.16 bus release:** For devices implementing overlap, the term bus release is the act of clearing both DRQ and BSY to zero before the action requested by the command is completed. This allows the host to select the other device or deliver another queued command.
- 3.1.17 byte count:** The value placed in the Byte Count register by the device to indicate the number of bytes to be transferred during this DRQ assertion when executing a PACKET PIO data transfer command.
- 3.1.18 byte count limit:** The value placed in the Byte Count register by the host as input to a PACKET PIO data transfer command to specify the maximum byte count that may be transferred during a single DRQ assertion.
- 3.1.19 CFA (CompactFlash™ Association):** The CompactFlash™ Association which created the specification for compact flash memory that uses the ATA interface.
- 3.1.20 check condition:** For devices implementing the PACKET Command feature set, this indicates an error or exception condition has occurred.
- 3.1.21 CHS (cylinder-head-sector):** An obsolete method of addressing the data on the device by cylinder number, head number, and sector number.

- 3.1.22 code violation:** In a serial interface implementation, a code violation is an error that occurs in the decoding of an encoded character. (See Volume 3, Clause 15)
- 3.1.23 command aborted:** Command completion with ABRT set to one in the Error register and ERR set to one in the Status register.
- 3.1.24 command acceptance:** A command is considered accepted whenever the currently selected device has the BSY bit cleared to zero in the Status register and the host writes to the Command register. An exception exists for the DEVICE RESET command (See Volume 1, Clause 6) In a serial implementation, command acceptance is a positive acknowledgment of a host to device register FIS.
- 3.1.25 Command Block registers:** Interface registers used for delivering commands to the device or posting status from the device. In a serial implementation, the command block registers are FIS payload fields.
- 3.1.26 command completion:** Command completion is the completion by the device of the action requested by the command or the termination of the command with an error, the placing of the appropriate error bits in the Error register, the placing of the appropriate status bits in the Status register, the clearing of both BSY and DRQ to zero, and Interrupt Pending.
- 3.1.27 command packet:** A data structure transmitted to the device during the execution of a PACKET command that includes the command and command parameters.
- 3.1.28 command released:** When a device supports overlap or queuing, a command is considered released when a bus release occurs before command completion.
- 3.1.29 Control Block registers:** In a parallel implementation, interface registers used for device control and to post alternate status. In a serial interface implementation, the logical field of a FIS corresponding to the Device Register bits of a parallel implementation.
- 3.1.30 control character:** In a serial interface implementation, an encoded character that represents a non-data byte (See Volume 3, Clause 15)
- 3.1.31 CRC (Cyclical Redundancy Check):** A means used to check the validity of certain data transfers.
- 3.1.32 Cylinder High register:** The name used for the LBA High register in previous ATA/ATAPI standards.
- 3.1.33 Cylinder Low register:** The name used for the LBA Mid register in previous ATA/ATAPI standards.
- 3.1.34 data character:** In a serial interface implementation, an encoded character that represents a data byte. (See Volume 3 Clause 15)
- 3.1.35 data-in:** The protocol that moves data from the device to the host. Such transfers are initiated by READ commands.
- 3.1.36 data-out:** The protocol that moves data from the host to the device. Such transfers are initiated by WRITE commands.
- 3.1.37 Delayed LBA:** Any sector for which the performance specified by the Streaming Performance Parameters log is not valid.
- 3.1.38 device:** A storage peripheral. Traditionally, a device on the interface has been a hard disk drive, but any form of storage device may be placed on the interface provided the device adheres to this standard.
- 3.1.39 device selection:** In a parallel implementation, a device is selected when the DEV bit of the Device register is equal to the device number assigned to the device by means of a Device 0/Device 1 jumper or switch, or use of the CSEL signal. In a serial implementation the device ignores the DEV bit, the host adapter may use this bit to emulate device selection.
- 3.1.40 disparity:** The difference between the number of ones and the number of zeros in an encoded character. (See Volume 3, Clause 15)
- 3.1.41 DMA (direct memory access) data transfer:** A means of data transfer between device and host memory without host processor intervention.
- 3.1.42 don't care:** A term to indicate that a value is irrelevant for the particular function described.
- 3.1.43 driver:** The active circuit inside a device or host that sources or sinks current to assert or negate a signal on the bus.

- 3.1.44 DRQ data block:** A unit of data words transferred during a single assertion of DRQ when using PIO data transfer.
- 3.1.45 elasticity buffer:** In a serial interface implementation, a portion of the receiver where character slipping and/or character alignment is performed.
- 3.1.46 encoded character:** In a serial interface implementation, the output of the 8b/10b encoder. (See Volume 3, Clause 15)
- 3.1.47 First party DMA access:** A method by which a device accesses host memory. First party DMA differs from DMA in that the device sends a DMA Setup FIS to select host memory regions; whereas for DMA the host configures the DMA controller.
- 3.1.48 FIS (Frame Information Structure):** A data structure and is the payload of a frame and does not include the SOF primitive, CRC, and EOF primitive.
- 3.1.49 frame:** A unit of information exchanged between the host adapter and a device. A frame consists of an SOF primitive, a Frame Information Structure, a CRC calculated over the contents of the FIS, and an EOF primitive.
- 3.1.50 FUA (Forced Unit Access):** Forced Unit Access requires that user data be transferred to or from the device media before command completion even if caching is enabled.
- 3.1.51 Gen1 DWORD Time:** The time it takes to transmit a 40 bit encoded value at 1.5 Gb/Sec.
- 3.1.52 host:** The computer system executing the software BIOS and/or operating system device driver controlling the device and the adapter hardware for the ATA interface to the device.
- 3.1.53 host adapter:** The implementation of the host transport, link, and physical layers.
- 3.1.54 Interrupt Pending:** In a parallel implementation, an internal state of a device. In this state, the device asserts INTRQ if nIEN is cleared to zero and the device is selected (See Clause 9). In a serial implementation, the Interrupt Pending state is an internal state of the host adapter. This state is entered by reception of a FIS with the I field set to one (See Volume 3, Clause 16)
- 3.1.55 LBA (logical block address):** The addressing of data on the device by the linear mapping of sectors.
- 3.1.56 LFSR (Linear Feedback Shift Register):** (See Volume 3, Clause 15)
- 3.1.57 link:** The link layer manages the phy layer to achieve the delivery and reception of frames. (See Volume 3, Clause 15)
- 3.1.58 logical sector:** A uniquely addressable set of 256 words (512 bytes).
- 3.1.59 native max address:** The highest address a device accepts in the factory default condition, that is, the highest address that is accepted by the SET MAX ADDRESS command.
- 3.1.60 overlap:** A protocol that allows devices that require extended command time to perform a bus release so that commands may be executed by the other device (if present) on the bus.
- 3.1.61 packet delivered command:** A command that is delivered to the device using the PACKET command via a command packet that contains the command and the command parameters. See also register delivered command.
- 3.1.62 phy:** Physical layer electronics, see Volume 3, Clause 14
- 3.1.63 physical sector:** A group of contiguous logical sectors that are read from or written to the device media in a single operation.
- 3.1.64 PIO (programmed input/output) data transfer:** PIO data transfers are performed by the host processor utilizing accesses to the Data register.
- 3.1.65 primitive:** In a serial interface implementation, a single DWORD of information that consists of a control character in byte 0 followed by three additional data characters in byte 1 through 3.
- 3.1.66 queued:** Command queuing allows the host to issue concurrent commands to the same device. Only commands included in the Overlapped feature set may be queued. In this standard, the queue contains all commands for which command acceptance has occurred but command completion has not occurred.
- 3.1.67 read command:** A command that causes the device to transfer data from the device to the host (e.g., READ SECTOR(S), READ DMA, etc.).
- 3.1.68 register:** A register may be a physical hardware register or a logical field.

- 3.1.69 register delivered command:** A command that is delivered to the device by placing the command and all of the parameters for the command in the device Command Block registers. See also packet delivered command.
- 3.1.70 register transfers:** The host reading and writing any device register except the Data register. Register transfers are 8 bits wide.
- 3.1.71 released:** In a parallel interface implementation, indicates that a signal is not being driven. For drivers capable of assuming a high-impedance state, this means that the driver is in the high impedance state. For open-collector drivers, the driver is not asserted.
- 3.1.72 sector:** A uniquely addressable set of 256 words (512 bytes).
- 3.1.73 Sector Number register:** The LBA Low register in previous ATA/ATAPI standards.
- 3.1.74 Shadow Command Block:** In a serial interface implementation, a set of virtual fields in the host adapter that map the Command Block registers defined at the command layer to the fields within the FIS content.
- 3.1.75 Shadow Control Block:** In a serial interface implementation, a set of virtual fields in the host adapter that map the Control Block registers defined at the command layer to the fields within the FIS content.
- 3.1.76 signature:** A unique set of values placed in the Command Block registers by the device to allow the host to distinguish devices implementing the PACKET Command feature set from those devices not implementing the PACKET Command feature set.
- 3.1.77 SMART (Self-Monitoring, Analysis, and Reporting Technology):** for prediction of device degradation and/or faults.
- 3.1.78 transport:** The transport layer manages the lower layers (link and phy) as well as constructing and parsing FIS's. See Volume 3, Clause 13
- 3.1.78 Ultra DMA burst:** An Ultra DMA burst is defined as the period from an assertion of DMACK- to the subsequent negation of DMACK- when an Ultra DMA transfer mode has been enabled by the host.
- 3.1.79 unaligned write:** A write command that does not start at the first logical sector of a physical sector or does not end at the last logical sector of a physical sector.
- 3.1.80 unit attention condition:** A state that a device implementing the PACKET Command feature set maintains while the device has asynchronous status information to report to the host.
- 3.1.81 unrecoverable error:** When the device sets either the ERR bit or the DF bit to one in the Status register at command completion.
- 3.1.82 VS (vendor specific):** Bits, bytes, fields, and code values that are reserved for vendor specific purposes. These bits, bytes, fields, and code values are not described in this standard, and may vary among vendors. This term is also applied to levels of functionality whose definition is left to the vendor.  
NOTE – Industry practice could result in conversion of a Vendor Specific bit, byte, field, or code value into a defined standard value in a future standard.
- 3.1.83 write command:** A command that causes the device to transfer data from the host to the device (e.g., WRITE SECTOR(S), WRITE DMA, etc.).
- 3.1.84 WWN (world wide name):** A 64-bit worldwide unique name based upon a company's IEEE identifier. (See IDENTIFY DEVICE Words (111:108) in Volume 1, Clause 6.)

## 3.2 Conventions

Lowercase is used for words having the normal English meaning. Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in Clause 3 or in the text where they first appear.

The names of abbreviations, commands, fields, and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE). Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field. (See 3.2.6 for the naming convention used for naming bits.)

**Transition SM1b:SM1:** When a SET MAX SET PASSWORD is received, the password stored by the device shall be changed to the new value and the device shall make a transition to the SM1: Set\_MAX\_Unlocked state.

**Transition SM1c:SM1:** When a SET MAX UNLOCK command is received, the command shall not be executed and the device shall make a transition to the SM1: Set\_MAX\_Unlocked state.

**Transition SM1:SM2:** When a SET MAX LOCK command is received, the device shall make a transition to the SM2: Set\_Max\_Locked state.

**Transition SM1:SM3:** When a SET MAX FREEZE LOCK command is received, the device shall make a transition to the SM3: Set\_Max\_Frozen state.

**SM2: Set\_Max\_Locked:** This state is entered when a SET MAX LOCK command is received.

When in this state, a SET MAX security password has been established and the SET MAX security is locked. Bit 8 of word 86 of the IDENTIFY DEVICE data shall be set to one.

**Transition SM2a:SM2:** When a SET MAX ADDRESS or SET MAX SET PASSWORD command is received, the command shall be aborted and the device shall make a transition to the SM2: Set\_Max\_Locked state.

**Transition SM2b:SM2:** When a SET MAX LOCK command is received, the command shall be executed and the device shall make a transition to the SM2: Set\_Max\_Locked state.

**Transition SM2:SM1:** When a SET MAX UNLOCK command is received, the device shall make a transition to the SM1: Set Max Unlocked state.

**Transition SM2:SM3:** When a SET MAX FREEZE LOCK command is received, the device may make a transition to the SM3: Set\_Max\_Frozen state. Hosts should not issue the SET MAX FREEZE LOCK command when in this state.

**SM3: Set\_Max\_Frozen:** This state is entered when a SET MAX FREEZE LOCK command is received.

In this state, the device may not transition to any other state except by a power cycling. When in this mode bit 8 of word 86 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data shall be set to one.

**Transition SM3:SM3:** When a SET MAX ADDRESS, SET MAX SET PASSWORD, SET MAX UNLOCK, SET MAX FREEZE LOCK, or SET MAX LOCK command is received, the command shall be aborted and the device shall make a transition to the SM3: Set\_Max\_Frozen state.

#### 4.10 CompactFlash™ Association (CFA) feature set

The optional CompactFlash™ Association (CFA) feature set provides support for solid state memory devices. A device that implements the CFA feature set shall implement the following minimum set of commands:

- CFA REQUEST EXTENDED ERROR CODE
- CFA WRITE SECTORS WITHOUT ERASE
- CFA ERASE SECTORS
- CFA WRITE MULTIPLE WITHOUT ERASE
- CFA TRANSLATE SECTOR
- SET FEATURES Enable/Disable 8-bit transfer

Devices reporting the value 848Ah in IDENTIFY DEVICE data word 0 or devices having bit 2 of IDENTIFY DEVICE data word 83 set to one shall support the CFA feature Set. If the CFA feature set is implemented, all five commands shall be implemented.

Support of DMA commands is optional for devices that support the CFA feature set.

The CFA ERASE SECTORS command preconditions the sector for a subsequent CFA WRITE SECTORS WITHOUT ERASE or CFA WRITE MULTIPLE WITHOUT ERASE command to achieve higher performance during the write operation. The CFA TRANSLATE SECTOR command provides information about a sector such as the number of write cycles performed on that sector and an indication of the sector's erased precondition. The CFA REQUEST EXTENDED ERROR CODE command provides more detailed error information.

Command codes B8h through BFh are reserved for assignment by the CompactFlash™ Association.

#### **4.11 Removable Media Status Notification and Removable Media feature sets**

This subclause describes two feature sets that secure the media in removable media storage devices using the ATA/ATAPI interface protocols. The Removable Media Status Notification feature set is intended for use in both devices implementing the PACKET Command feature set and those not implementing the PACKET Command feature set. The Removable Media feature set is intended for use only in devices not implementing the PACKET Command feature set. Only one of these feature sets shall be enabled at any time. If the Removable Media Status Notification feature set is in use then the Removable Media feature set is disabled and vice versa.

The reasons for implementing the Removable Media Status Notification feature Set or the Removable Media feature set are:

- to prevent data loss caused by writing to new media while still referencing the previous media's information.
- to prevent data loss by locking the media until completion of a cached write.
- to prevent removal of the media by unauthorized persons.

##### **4.11.1 Removable Media Status Notification feature set**

The Removable Media Status Notification feature set is the preferred feature set for securing the media in removable media storage devices. This feature set uses the SET FEATURES command to enable Removable Media Status Notification. Removable Media Status Notification gives the host system maximum control of the media. The host system determines media status by issuing the GET MEDIA STATUS command and controls the device eject mechanism via the MEDIA EJECT command (for devices not implementing the PACKET Command feature set) or the START/STOP UNIT command (for devices implementing the PACKET Command feature set, See Clause 1). While Removable Media Status Notification is enabled devices not implementing the PACKET Command feature set execute MEDIA LOCK and MEDIA UNLOCK commands without changing the media lock state (no-operation). While Removable Media Status Notification is enabled the eject button does not eject the media.

Removable Media Status Notification is persistent through medium removal and insertion and is only disabled via the SET FEATURES command, hardware reset, software reset, the DEVICE RESET command, the EXECUTE DEVICE DIAGNOSTIC command, or power-on reset. Removable Media Status Notification shall be re-enabled after any of the previous reset conditions occur. All media status is reset when Removable Media Status Notification is disabled because a reset condition occurred. Any pending media change or media change request is cleared when the Removable Media Status Notification reset condition occurs.

The following commands are defined to implement the Removable Media Status Notification feature set.

- GET MEDIA STATUS
- MEDIA EJECT
- SET FEATURES (Enable media status notification)
- SET FEATURES (Disable media status notification)

## 6 Command Descriptions

### 6.1 Overview

Commands are issued to the device by loading the required registers in the command block with the needed parameters and then writing the command code to the Command register. Required registers are those indicated by a specific content in the Inputs table for the command, i.e., not noted as na or obs.

References to parallel implementation bus signals (e.g. DMACK, DMARQ, etc) apply only to parallel implementations. See Volume 3 for additional information on serial protocol. Some register bits (e.g. nLEN, SRST, etc.) have different requirements in the serial implementation (See Volume 3).

Each command description in the following clauses contains the following subclauses:

Command code -Specifies the command code for this command.

Feature set -Specifies feature set and if the command is mandatory or optional.

Protocol -Specifies which protocol is used by the command (See Clause 11).

Inputs - Describes the Command Block register data that the host shall supply.

| Register                                                                                                                                           | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------------------------------------------------------------------------------------------------------------------------------------|--------------|---|---|---|---|---|---|---|
| Features                                                                                                                                           |              |   |   |   |   |   |   |   |
| Sector Count                                                                                                                                       |              |   |   |   |   |   |   |   |
| LBA Low                                                                                                                                            |              |   |   |   |   |   |   |   |
| LBA Mid                                                                                                                                            |              |   |   |   |   |   |   |   |
| LBA High                                                                                                                                           |              |   |   |   |   |   |   |   |
| Device                                                                                                                                             |              |   |   |   |   |   |   |   |
| Command                                                                                                                                            | Command Code |   |   |   |   |   |   |   |
| NOTE – na specifies the content of a bit or field is not applicable to the particular command. Obs specifies that the use of this bit is obsolete. |              |   |   |   |   |   |   |   |

Normal outputs - Describes the Command Block register data returned by the device at the end of a command.

| Register                                                                                                                                           | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------------------------------------------------------------------------------------------------------------------------------------|---|---|---|---|---|---|---|---|
| Error                                                                                                                                              |   |   |   |   |   |   |   |   |
| Sector Count                                                                                                                                       |   |   |   |   |   |   |   |   |
| LBA Low                                                                                                                                            |   |   |   |   |   |   |   |   |
| LBA Mid                                                                                                                                            |   |   |   |   |   |   |   |   |
| LBA High                                                                                                                                           |   |   |   |   |   |   |   |   |
| Device                                                                                                                                             |   |   |   |   |   |   |   |   |
| Status                                                                                                                                             |   |   |   |   |   |   |   |   |
| NOTE – na indicates the content of a bit or field is not applicable to the particular command. Obs indicates that the use of this bit is obsolete. |   |   |   |   |   |   |   |   |

Error outputs - Describes the Command Block register data that shall be returned by the device at command completion with an unrecoverable error.

| Register                                                                                                                                           | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------------------------------------------------------------------------------------------------------------------------------------|---|---|---|---|---|---|---|---|
| Error                                                                                                                                              |   |   |   |   |   |   |   |   |
| Sector Count                                                                                                                                       |   |   |   |   |   |   |   |   |
| LBA Low                                                                                                                                            |   |   |   |   |   |   |   |   |
| LBA Mid                                                                                                                                            |   |   |   |   |   |   |   |   |
| LBA High                                                                                                                                           |   |   |   |   |   |   |   |   |
| Device                                                                                                                                             |   |   |   |   |   |   |   |   |
| Status                                                                                                                                             |   |   |   |   |   |   |   |   |
| NOTE – na indicates the content of a bit or field is not applicable to the particular command. Obs indicates that the use of this bit is obsolete. |   |   |   |   |   |   |   |   |

Prerequisites - Any prerequisite commands or conditions that shall be met before the command is issued.

Description - The description of the command function(s).

## 6.2 CFA ERASE SECTORS

### 6.2.1 Command code

C0h

### 6.2.2 Feature set

CFA feature set.

- If the CFA feature set is implemented this command shall be implemented.

This command code is Vendor Specific for devices not implementing the CFA feature Set.

### 6.2.3 Protocol

Non-data (See Clause 11).

### 6.2.4 Inputs

The LBA High, LBA Mid, LBA Low, and Device registers specify the starting sector address to be erased. The Sector Count register specifies the number of sectors to be erased.

| Register     | 7            | 6   | 5   | 4   | 3           | 2 | 1 | 0 |
|--------------|--------------|-----|-----|-----|-------------|---|---|---|
| Features     | na           |     |     |     |             |   |   |   |
| Sector Count | Sector count |     |     |     |             |   |   |   |
| LBA Low      | LBA (7:0)    |     |     |     |             |   |   |   |
| LBA Mid      | LBA (15:8)   |     |     |     |             |   |   |   |
| LBA High     | LBA (23:16)  |     |     |     |             |   |   |   |
| Device       | obs          | LBA | obs | DEV | LBA (27:24) |   |   |   |
| Command      | C0h          |     |     |     |             |   |   |   |

Sector Count -

number of sectors to be erased. A value of 00h specifies that 256 sectors are to be erased.

LBA Low -

starting LBA bits (7:0).

LBA Mid -

starting LBA bits (15:8).

LBA High -

starting LBA bits (23:16).

Device -

the LBA bit shall be set to one to specify the address is an LBA, starting LBA bits (27:24).

### 6.2.5 Normal outputs

| Register     | 7   | 6    | 5   | 4   | 3  | 2  | 1  | 0   |
|--------------|-----|------|-----|-----|----|----|----|-----|
| Error        | na  |      |     |     |    |    |    |     |
| Sector Count | na  |      |     |     |    |    |    |     |
| LBA Low      | na  |      |     |     |    |    |    |     |
| LBA Mid      | na  |      |     |     |    |    |    |     |
| LBA High     | na  |      |     |     |    |    |    |     |
| Device       | obs | na   | obs | DEV | na | na | na | na  |
| Status       | BSY | DRDY | na  | na  | na | na | na | ERR |

**Status register**

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

ERR shall be cleared to zero.

**6.2.6 Error outputs**

The device shall return command aborted if the command is not supported. An unrecoverable error encountered during execution of this command results in the termination of the command. The command block registers contain the address of the sector where the first unrecovered error occurred.

| Register     | 7           | 6    | 5   | 4    | 3           | 2    | 1  | 0   |
|--------------|-------------|------|-----|------|-------------|------|----|-----|
| Error        | na          | na   | na  | IDNF | na          | ABRT | na | MED |
| Sector Count | na          |      |     |      |             |      |    |     |
| LBA Low      | LBA (7:0)   |      |     |      |             |      |    |     |
| LBA Mid      | LBA (15:8)  |      |     |      |             |      |    |     |
| LBA High     | LBA (23:16) |      |     |      |             |      |    |     |
| Device       | obs         | na   | obs | DEV  | LBA (27:24) |      |    |     |
| Status       | BSY         | DRDY | DF  | na   | na          | na   | na | ERR |

**Error Register -**

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

ABRT shall be set to one if the command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

MED shall be set to one if a media error is detected.

**LBA Low, LBA Mid, LBA High, Device-**

shall be written with the address of first unrecoverable error.

**Status register -**

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

ERR shall be set to one if an Error register bit is set to one.

**6.2.7 Prerequisites**

DRDY set to one.

**6.2.8 Description**

This command pre-erases and conditions from 1 to 256 sectors as specified in the Sector Count register. This command should be issued in advance of a CFA WRITE SECTORS WITHOUT ERASE or a CFA WRITE MULTIPLE WITHOUT ERASE command to increase the execution speed of the write operation.