



Serial ATA International Organization:

Serial ATA Revision 2.5

27-October-2005

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TABLE OF CONTENTS

1	Revision history	18
1.1	Revision 2.5 (Ratification Date October 27, 2005)	18
2	Scope	19
3	Normative references	20
3.1	Approved references	20
3.2	References under development	22
3.3	Other references	22
4	Definitions, abbreviations, and conventions	23
4.1	Definitions and abbreviations	23
4.1.1	active port	23
4.1.2	ATA (AT Attachment)	23
4.1.3	ATAPI (AT Attachment Packet Interface) device	23
4.1.4	BER (bit error rate)	23
4.1.5	bitrate	23
4.1.6	bit synchronization	23
4.1.7	burst	23
4.1.8	byte	23
4.1.9	character	23
4.1.10	character alignment	23
4.1.11	character slipping	23
4.1.12	code violation	24
4.1.13	comma character	24
4.1.14	comma sequence	24
4.1.15	command aborted	24
4.1.16	command completion	24
4.1.17	command packet	24
4.1.18	concentrator	24
4.1.19	Control Block registers	25
4.1.20	control character	25
4.1.21	control port	25
4.1.22	control variable	25
4.1.23	CRC (Cyclic Redundancy Check)	25
4.1.24	data character	25
4.1.25	data signal source	25
4.1.26	device	25
4.1.27	device port	25
4.1.28	DCB (DC block)	25
4.1.29	differential signal	25
4.1.30	DJ (deterministic jitter – peak to peak)	25
4.1.31	DMA (direct memory access)	26
4.1.32	Dword	26
4.1.33	Dword synchronization	26
4.1.34	EMI (Electromagnetic Interference)	26
4.1.35	encoded character	26
4.1.36	endpoint device	26
4.1.37	elasticity buffer	26
4.1.38	Fbaud	26
4.1.39	FER (frame error rate)	26
4.1.40	First-party DMA Data Phase	27
4.1.41	First-party DMA access	27
4.1.42	FIS (Frame Information Structure)	27
4.1.43	frame	27
4.1.44	Gen1	27

4.1.45	Gen1i	27
4.1.46	Gen1m	27
4.1.47	Gen1x	27
4.1.48	Gen2	27
4.1.49	Gen2i	27
4.1.50	Gen2m	27
4.1.51	Gen2x	27
4.1.52	HBA (Host Bus Adapter).....	27
4.1.53	HBWS (High Bandwidth Scope)	28
4.1.54	HFTP (High Frequency Test Pattern).....	28
4.1.55	host port.....	28
4.1.56	inactive port	28
4.1.57	interrupt pending.....	28
4.1.58	ISI (inter-symbol interference)	28
4.1.59	JMD (jitter measuring device).....	28
4.1.60	junk	28
4.1.61	LBA (Logical Block Address)	28
4.1.62	LBP (lone bit pattern).....	28
4.1.63	LED (Light Emitting Diode)	29
4.1.64	legacy mode	29
4.1.65	legal character	29
4.1.66	LFSR (Linear Feedback Shift Register).....	29
4.1.67	LFTP (low frequency test pattern)	29
4.1.68	LL (laboratory load).....	29
4.1.69	LSS (laboratory sourced signal or lab-sourced signal).....	29
4.1.70	MFTP (mid frequency test pattern).....	29
4.1.71	OOB (Out-of-Band signaling)	29
4.1.72	OS-aware hot plug.....	29
4.1.73	OS-aware hot removal.....	30
4.1.74	Phy offline	30
4.1.75	PIO (programmed input/output).....	30
4.1.76	port address.....	30
4.1.77	PRD (Physical Region Descriptor)	30
4.1.78	primitive.....	30
4.1.79	protocol-based port selection	30
4.1.80	quiescent power condition	30
4.1.81	RJ (random jitter)	30
4.1.82	sector	30
4.1.83	SEMB (Serial ATA Enclosure Management Bridge)	30
4.1.84	SEP (Storage Enclosure Processor)	31
4.1.85	Shadow Register Block registers.....	31
4.1.86	side-band port selection.....	31
4.1.87	SMART	31
4.1.88	SSC (spread spectrum clocking)	31
4.1.89	surprise hot plug	31
4.1.90	surprise hot removal	31
4.1.91	SYNC Escape	31
4.1.92	TDR (time domain reflectometer)	31
4.1.93	TIA (timing interval analyzer).....	31
4.1.94	TJ (total jitter).....	32
4.1.95	UI (unit interval)	32
4.1.96	unrecoverable error	32
4.1.97	UUT (unit under test)	32
4.1.98	VNA (vector network analyzer).....	32
4.1.99	word	32
4.1.100	zero crossing	32

4.2	Conventions.....	32
4.2.1	Precedence.....	32
4.2.2	Keywords.....	33
4.2.3	Numbering.....	34
4.2.4	Dimensions.....	34
4.2.5	Signal conventions.....	34
4.2.6	Bit conventions.....	34
4.2.7	State machine conventions.....	35
4.2.8	Timing conventions.....	36
4.2.9	Byte, word and Dword Relationships.....	37
5	General overview.....	38
5.1	Architecture.....	39
5.2	Usage Models.....	40
5.2.1	Internal 1 meter Cabled Host to Device.....	41
5.2.2	Short Backplane to Device.....	41
5.2.3	Long Backplane to Device.....	42
5.2.4	Internal 4-lane Cabled Disk Arrays.....	43
5.2.5	System to System Interconnects – Data Center Applications.....	44
5.2.6	System to System Interconnects – External Desktop Applications.....	46
5.2.7	Proprietary Serial ATA Disk Arrays.....	47
5.2.8	Serial ATA and SAS.....	47
5.2.9	Potential External SATA Incompatibility Issues.....	47
5.2.10	Mobile Applications.....	48
5.2.11	Port Multiplier Example Applications.....	48
6	Cables and connectors.....	52
6.1	Internal cables and connectors.....	52
6.1.1	Internal Single Lane Description.....	52
6.1.2	Connector locations.....	55
6.1.3	Mating interfaces.....	64
6.1.4	Signal cable receptacle connector.....	68
6.1.5	Signal host plug connector.....	70
6.1.6	Backplane connector.....	73
6.1.7	Power cable receptacle connector.....	76
6.1.8	Internal single lane cable.....	78
6.1.9	Connector labeling.....	79
6.1.10	Connector and cable assembly requirements and test procedures.....	79
6.1.11	Internal Multi Lane cables.....	83
6.2	External cables and connectors.....	89
6.2.1	External Single Lane.....	89
6.2.2	External Multi Lane.....	99
6.3	Cable and Connector Electrical Specifications.....	103
6.3.1	Serial ATA Cable.....	103
6.3.2	Cable/Connector Test Methodology.....	104
6.4	Power Segment Pin P11 Definition (Optional).....	112
6.4.1	Device Activity Signal.....	113
6.4.2	Staggered Spin-up Disable Control.....	115
6.5	Precharge and Device Presence Detection.....	116
6.5.1	Device Requirements.....	116
6.5.2	Receptacle Precharge (Informative).....	116
6.5.3	Presence Detection (Informative).....	118
7	Physical layer.....	120
7.1	Descriptions of Phy Electrical Specifications.....	120
7.1.1	List of services.....	121
7.1.2	Low Level Electronics Block Diagrams (Informative).....	122
7.1.3	Compliance Testing.....	128
7.1.4	Link Performance.....	129

7.2	Electrical specifications	129
7.2.1	Physical Layer Requirements Tables	131
7.2.2	Physical Layer Requirements Details	141
7.2.3	Loopback	157
7.2.4	Test Pattern Requirements	160
7.2.5	Hot Plug Considerations	177
7.2.6	Mated Pair Definition	179
7.2.7	Compliance Interconnect Channels (Gen1x, Gen2x)	181
7.2.8	Impedance Calibration (Optional)	184
7.3	Jitter	185
7.3.1	Definition	186
7.3.2	Reference Clock Definition	186
7.3.3	Spread Spectrum Clocking	187
7.3.4	Jitter Budget	188
7.3.5	Jitter Formulas without SSC (Informative)	189
7.4	Measurements	191
7.4.1	Frame error rate testing	192
7.4.2	Measurement of Differential Voltage Amplitudes	195
7.4.3	Rise and Fall Times	206
7.4.4	Transmitter Amplitude	207
7.4.5	Receive Amplitude	209
7.4.6	Long Term Frequency Accuracy	213
7.4.7	Jitter Measurements	214
7.4.8	Transmit Jitter	217
7.4.9	Receiver Tolerance	218
7.4.10	Return Loss and Impedance Balance	220
7.4.11	SSC Profile	223
7.4.12	Intra-pair Skew	224
7.4.13	Sequencing Transient Voltage	226
7.4.14	AC Coupling Capacitor	227
7.4.15	TX Amplitude Imbalance	228
7.4.16	TX Rise/Fall Imbalance	228
7.4.17	TX AC Common Mode Voltage	228
7.4.18	OOB Common Mode Delta	229
7.4.19	OOB Differential Delta	229
7.4.20	Squelch Detector Tests	230
7.4.21	OOB signaling tests	231
7.4.22	TDR Differential Impedance (Gen1i / Gen1m)	232
7.4.23	TDR Single Ended-Impedance (Gen1i / Gen1m)	233
7.4.24	DC Coupled Common Mode Voltage (Gen1i / Gen1m)	234
7.4.25	AC Coupled Common Mode Voltage (Gen1i / Gen1m)	235
7.5	Interface States	236
7.5.1	Out Of Band signaling	236
7.5.2	Idle bus condition	247
7.6	Elasticity buffer management	247
8	OOB and Phy Power States	248
8.1	Interface power states	248
8.2	Asynchronous Signal Recovery (Optional)	248
8.2.1	Unsolicited COMINIT Usage (Informative)	248
8.3	Power-on sequence state machine	249
8.3.1	Host Phy Initialization state machine	249
8.3.2	Device Phy Initialization state machine	254
8.3.3	Speed Negotiation	257
9	Link layer	264
9.1	Overview	264
9.1.1	Frame transmission	264

9.1.2	Frame reception.....	264
9.2	Encoding method.....	264
9.2.1	Notation and conventions	265
9.2.2	Character code	266
9.2.3	Transmission summary.....	275
9.2.4	Reception summary.....	277
9.3	Transmission overview	278
9.4	Primitives	280
9.4.1	Overview	280
9.4.2	Primitive descriptions.....	280
9.4.3	Primitive encoding	282
9.4.4	DMAT _P primitive.....	282
9.4.5	CONT _P primitive.....	283
9.4.6	ALIGN _P primitive	286
9.4.7	Flow control signaling latency.....	286
9.4.8	Examples of primitive usage (Informative)	287
9.5	CRC and scrambling.....	291
9.5.1	Relationship between scrambling of FIS data and repeated primitives	291
9.5.2	Relationship between scrambling and CRC	292
9.5.3	Scrambling Disable (Informative)	292
9.6	Link layer state machine	293
9.6.1	Terms used in Link layer transition tables	293
9.6.2	Link idle state diagram.....	294
9.6.3	Link transmit state diagram.....	298
9.6.4	Link receive state diagram.....	305
9.6.5	Link power mode state diagram	312
10	Transport layer.....	317
10.1	Overview	317
10.1.1	FIS construction	317
10.1.2	FIS decomposition	317
10.2	Frame Information Structure (FIS).....	317
10.2.1	Overview	317
10.2.2	Payload content	318
10.3	FIS Types	318
10.3.1	FIS Type values	318
10.3.2	CRC Errors on Data FISes	319
10.3.3	All FIS types.....	319
10.3.4	Register - Host to Device.....	320
10.3.5	Register - Device to Host.....	322
10.3.6	Set Device Bits - Device to Host.....	324
10.3.7	DMA Activate - Device to Host	326
10.3.8	DMA Setup – Device to Host or Host to Device (Bidirectional)	327
10.3.9	BIST Activate - Bidirectional	330
10.3.10	PIO Setup – Device to Host.....	333
10.3.11	Data - Host to Device or Device to Host (Bidirectional).....	336
10.4	Host transport states.....	338
10.4.1	Host transport idle state diagram.....	338
10.4.2	Host Transport transmit command FIS diagram	341
10.4.3	Host Transport transmit control FIS diagram.....	342
10.4.4	Host Transport transmit DMA Setup – Device to Host or Host to Device FIS state diagram	343
10.4.5	Host Transport transmit BIST Activate FIS.....	345
10.4.6	Host Transport decompose Register FIS diagram	346
10.4.7	Host Transport decompose a Set Device Bits FIS state diagram	347
10.4.8	Host Transport decompose a DMA Activate FIS diagram.....	348
10.4.9	Host Transport decompose a PIO Setup FIS state diagram.....	351

10.4.10	Host Transport decompose a DMA Setup FIS state diagram	355
10.4.11	Host transport decompose a BIST Activate FIS state diagram	356
10.5	Device transport states	357
10.5.1	Device transport idle state diagram	357
10.5.2	Device Transport send Register – Device to Host state diagram	359
10.5.3	Device Transport send Set Device Bits FIS state diagram	360
10.5.4	Device Transport transmit PIO Setup – Device to Host FIS state diagram	361
10.5.5	Device Transport transmit DMA Activate FIS state diagram	362
10.5.6	Device Transport transmit DMA Setup – Device to Host FIS state diagram	363
10.5.7	Device Transport transmit Data – Device to Host FIS diagram	364
10.5.8	Device Transport transmit BIST Activate FIS diagram	366
10.5.9	Device Transport decompose Register – Host to Device state diagram	367
10.5.10	Device Transport decompose Data (Host to Device) FIS state diagram	368
10.5.11	Device Transport decompose DMA Setup – Host to Device state diagram	370
10.5.12	Device Transport decompose a BIST Activate FIS state diagram	371
11	Device command layer protocol	372
11.1	Power-on and COMRESET protocol	372
11.2	Device Idle protocol	375
11.3	Software reset protocol	380
11.4	EXECUTE DEVICE DIAGNOSTIC command protocol	383
11.5	DEVICE RESET command protocol	384
11.6	Non-data command protocol	385
11.7	PIO data-in command protocol	387
11.8	PIO data-out command protocol	389
11.9	DMA data in command protocol	390
11.10	DMA data out command protocol	391
11.11	PACKET protocol	393
11.12	READ DMA QUEUED command protocol	398
11.13	WRITE DMA QUEUED command protocol	400
11.14	FPDMA QUEUED command protocol	402
12	Host command layer protocol	409
12.1	FPDMA QUEUED command protocol	409
13	Application layer	413
13.1	Parallel ATA Emulation	413
13.1.1	Software Reset	413
13.1.2	Master-only emulation	414
13.1.3	Master/Slave emulation (optional)	415
13.2	IDENTIFY (PACKET) DEVICE and SET FEATURES	421
13.2.1	IDENTIFY DEVICE	422
13.2.2	IDENTIFY PACKET DEVICE	428
13.2.3	Determining Support for Serial ATA Features	432
13.2.4	SET FEATURES	433
13.2.5	READ LOG EXT Log Directory	435
13.3	Device Configuration Overlay	435
13.4	Software Settings Preservation (Optional)	436
13.5	Native Command Queuing (Optional)	438
13.5.1	Overview	438
13.5.2	Definition	438
13.5.3	Intermixing Non-Native Queued Commands and Native Queued Commands ...	444
13.5.4	Command Definitions	445
13.5.5	First-party DMA HBA Support (Informative)	452
13.6	Asynchronous Notification (Optional)	454
13.6.1	Set Device Bits FIS Notification bit	454
13.6.2	Notification Mechanism	454
13.6.3	State Diagram for Asynchronous Notification	454
13.6.4	ATAPI Notification	455

13.7	Phy Event Counters (Optional).....	455
13.7.1	Counter Reset Mechanisms	456
13.7.2	Counter Identifiers	456
13.7.3	READ LOG EXT Log Page 11h.....	459
13.8	Staggered Spin-up (Optional).....	460
13.8.1	ATA Power States	460
13.9	Non-512 Byte Sector Size (Informative).....	460
13.10	Defect Management (Informative).....	461
13.10.1	Overview (Informative).....	461
13.10.2	Typical Serial ATA Reliability Metrics (Informative).....	461
13.10.3	An Overview of Serial ATA Defect Management (Informative)	461
13.10.4	Continuous Background Defect Scanning (Informative)	462
13.10.5	Self-Monitoring, Analysis and Reporting Technology (Informative)	462
13.11	Enclosure Services/Management (Optional).....	463
13.11.1	Overview	463
13.11.2	Topology	463
13.11.3	Limitations.....	465
13.11.4	Definition.....	465
13.11.5	SES and SAF-TE Extensions	471
13.11.6	Enclosure Services Hardware Interface	477
13.12	HDD Activity Indication (Optional)	478
13.12.1	HDD Activity Emulation of Desktop Behavior	478
13.12.2	Activity/Status Indication Reference (Informative).....	479
13.13	Port Multiplier Discovery and Enumeration	482
13.13.1	Power-up	482
13.13.2	Resets.....	483
13.13.3	Software Initialization Sequences (Informative)	484
13.13.4	Port Multiplier Discovery and Device Enumeration (Informative).....	484
14	Host adapter register interface	486
14.1	Status and Control Registers.....	487
14.1.1	SStatus register	488
14.1.2	SError register	489
14.1.3	SControl register.....	491
14.1.4	SActive register.....	492
14.1.5	SNotification register (Optional).....	492
15	Error handling	494
15.1	Architecture.....	494
15.2	Phy error handling overview	495
15.2.1	Error detection	495
15.2.2	Error control actions.....	496
15.2.3	Error reporting.....	497
15.3	Link layer error handling overview.....	497
15.3.1	Error detection	497
15.3.2	Error control actions.....	497
15.3.3	Error reporting.....	498
15.4	Transport layer error handling overview	498
15.4.1	Error detection	499
15.4.2	Error control actions.....	499
15.4.3	Error reporting.....	501
15.5	Application layer error handling overview.....	501
15.5.1	Error detection	501
15.5.2	Error control actions.....	502
16	Port Multiplier	503
16.1	Introduction	503
16.2	Overview.....	503
16.3	Definition.....	504

16.3.1	Addressing Mechanism	504
16.3.2	Device Port Requirements.....	504
16.3.3	Policies.....	506
16.4	Port Multiplier Registers	516
16.4.1	General Status and Control Registers.....	516
16.4.2	Port Status and Control Registers	525
16.5	Port Multiplier Command Definitions	526
16.5.1	READ PORT MULTIPLIER.....	526
16.5.2	WRITE PORT MULTIPLIER.....	528
16.5.3	Interrupts.....	530
16.6	Controlling PM Port value and Interface Power Management	530
16.7	Switching Types (Informative)	530
16.7.1	Command-based switching	530
16.7.2	FIS-based switching	530
17	Port Selector	532
17.1	Example Applications	532
17.2	Overview.....	533
17.3	Active Port Selection.....	534
17.3.1	Protocol-based Port Selection	534
17.3.2	Side-band Port Selection.....	537
17.3.3	Behavior during a change of active port.....	537
17.4	Behavior and Policies	538
17.4.1	Control State Machine	538
17.4.2	BIST support.....	542
17.4.3	Flow control signaling latency.....	542
17.4.4	Power Management.....	542
17.4.5	OOB Phy signals	543
17.4.6	Hot Plug.....	543
17.4.7	Speed Negotiation	543
17.4.8	Spread spectrum clocking	544
17.5	Power-up and Resets	544
17.5.1	Power-up	544
17.5.2	Resets.....	544
17.6	Host Implementation (Informative)	544
17.6.1	Software Method for Protocol-based Selection (Informative).....	544
Appendix A.	Sample Code for CRC and Scrambling (Informative)	547
A.1	CRC calculation	547
A.1.1	Overview	547
A.1.2	Maximum frame size.....	547
A.1.3	Example code for CRC algorithm	547
A.1.4	Example code for CRC algorithm	547
A.1.5	Example CRC implementation output	549
A.2	Scrambling calculation.....	550
A.2.1	Overview	550
A.2.2	Example code for scrambling algorithm	550
A.2.3	Example scrambler implementation	550
A.2.4	Example scrambler implementation output	553
A.3	Example frame.....	554
Appendix B.	Command processing overview (Informative)	555
B.1	Non-data commands	555
B.2	DMA read by host from device	555
B.3	DMA write by host to device	555
B.4	PIO data read from the device.....	556
B.5	PIO data write to the device	556
B.6	ATA Tagged Command Queuing DMA read from device	557
B.7	ATA Tagged Command Queuing DMA write to device	558

B.8	ATAPI Packet commands with PIO data in	558
B.9	ATAPI Packet commands with PIO data out	559
B.10	ATAPI Packet commands with DMA data in	560
B.11	ATAPI Packet commands with DMA data out	561
B.12	Odd word count considerations	562
B.12.1	DMA read from target for odd word count	563
B.12.2	DMA write by host to target for odd word count	563
B.13	PIO data read from the device	563
B.14	PIO data write to the device	564
B.15	Native Command Queuing Examples (Informative)	564
B.15.1	Queued Commands with Out of Order Completion	564
B.15.2	Interrupt Aggregation	566
Appendix C.	Device Emulation of nIEN with Interrupt Pending (Informative)	569
Appendix D.	I/O Controller Module (Informative)	570
D.1	Supported Configurations	570
D.1.1	Single I/O Controller Signals	571
D.1.2	Dual I/O Controller Signals	572
D.1.3	Further optional features	572
D.2	Optional High Speed Channel configurations	573
D.3	Optional Low Speed Channel configurations	575
D.4	I/O Controller Module Connectors	576
D.4.1	I/O Controller Module Connector	576
D.5	I/O Controller Module Connector Locations	579
D.5.1	Purpose	579
D.6	Pinout Listing	582
D.7	Signal Descriptions	583

TABLE OF FIGURES

Figure 1 – Byte, word and Dword relationships.....	37
Figure 2 – Parallel ATA device connectivity	38
Figure 3 – Serial ATA connectivity	39
Figure 4 – Communication layers.....	40
Figure 5 – Internal 1 meter Cabled Host to Device Application	41
Figure 6 – Short Backplane to Device Application	42
Figure 7 – Long Backplane to Device Application.....	43
Figure 8 – Internal 4-lane Cabled Disk Array	44
Figure 9 – System to System Interconnects.....	45
Figure 10 – External Desktop Application	46
Figure 11 – SATA Disk Arrays.....	47
Figure 12 – Enclosure example using Port Multipliers with Serial ATA as the connection within the rack.....	49
Figure 13 – Enclosure example using Port Multipliers with a different connection within the rack.....	50
Figure 14 – Mobile docking station example using a Port Multiplier	51
Figure 15 – Serial ATA connector examples.....	53
Figure 16 – SATA Cable / Connector Connection Diagram.....	54
Figure 17 – SATA Host / Device Connection Diagram.....	55
Figure 18 – Optical Device Plug Connector Location on 5.25" form factor.....	56
Figure 19 – Non-Optical Alternate Device Plug Connector Location on 5.25" form factor	57
Figure 20 – Device Plug Connector Location on 3.5" Side Mounted Device	58
Figure 21 – Device Plug Connector Location on 3.5" Bottom Mounted Device.....	59
Figure 22 – Device Plug Connector Location on 2.5" Side Mounted Device	60
Figure 23 – Device Plug Connector Location on 2.5" Bottom Mounted Device.....	61
Figure 24 – Device Plug Connector Location on 1.8" Side Mounted Device	62
Figure 25 – Device Plug Connector Location on 1.8" Bottom Mounted Device.....	63
Figure 26 – Device Plug Connector Keep Out Zones	64
Figure 27 – Device Plug Connector.....	65
Figure 28 – Device Plug Connector (additional views).....	66
Figure 29 – Connector Pin and Feature Locations.....	68
Figure 30 – Cable receptacle connector interface dimensions	69
Figure 31 – Latching signal cable receptacle	70
Figure 32 – Host signal plug connector interface dimensions.....	71
Figure 33 – Non-Latching Connector Stack Spacing and Orientation	72
Figure 34 – Latching Connector Stack Spacing and Orientation	72
Figure 35 – Backplane connector interface dimensions.....	74
Figure 36 – Connector pair blind-mate misalignment tolerance.....	75
Figure 37 – Device-backplane mating configuration	76
Figure 38 – Power receptacle connector interface dimensions	77
Figure 39 – Latching power cable receptacle.....	78
Figure 40 – Detailed cross-section of an example internal single lane cable	79
Figure 41 – Isometric drawings of the internal 2 Lane cable and connector.....	84
Figure 42 – Isometric drawings of the internal 4 Lane cable and connector.....	85
Figure 43 – 4 Lane Pin Assignments.....	86
Figure 44 – 4 Lane to 4 x 1 Lanes, Fanout Implementation.....	87
Figure 45 – 4 Lane Fanout Pin Assignments	88
Figure 46 – 2 Lane Fanout Pin Assignments	89
Figure 47 – Usage Model for HBA with external cable and single device enclosure.....	90
Figure 48 – Usage Model for on-Board Serial ATA Connector with extension cable to external cable to disk.....	91
Figure 49 – Renderings of External Serial ATA cable receptacle and right angle plug	92
Figure 50 – Mechanical dimensions of External Serial ATA cable receptacle assembly.....	93
Figure 51 – Mechanical dimensions of External Serial ATA RA SMT plug.....	94

Figure 52 – Mechanical dimensions of External SATA RA SMT plug – Reversed Pin Out	95
Figure 53 – Mechanical dimensions of External Serial ATA RA Through-hole	96
Figure 54 – Mechanical dimensions of External Serial ATA Vertical SMT plug	97
Figure 55 – Mechanical dimensions of External Serial ATA Vertical Through-hole plug	98
Figure 56 – External Multi Lane cable and connector	100
Figure 57 – Multi Lane Cable Connector Blocking Key Locations	101
Figure 58 – Plug/Receptacle Keying	102
Figure 59 – Example activity signal electrical block diagram	113
Figure 60 – Example host LED driver circuits	114
Figure 61 – Example host circuit for signaling staggered spin-up disable	116
Figure 62 – Typical precharge configuration	117
Figure 63 – Example presence detection implementation	118
Figure 64 – Physical plant overall block diagram (Informative)	122
Figure 65 – Analog front end (AFE) block diagram	125
Figure 66 – Analog front end (AFE) cabling	127
Figure 67 – The Simplex Link	128
Figure 68 – Common mode biasing examples for Gen1i (Informative)	142
Figure 69 – Common mode biasing for Gen1x, Gen2i, and Gen2x	143
Figure 70 – Differential Return Loss Limits	145
Figure 71 – Common Mode Return Loss Limits	146
Figure 72 – Impedance Balance Limits	147
Figure 73 – Signal rise and fall times	148
Figure 74 – TX Intra-pair Skew	149
Figure 75 – OOB Differential Delta (at Compliance Point with AC coupling)	150
Figure 76 – LL Laboratory Load	152
Figure 77 – LSS Lab-Sourced Signal	153
Figure 78 – RX Differential Input Voltage Conditions	153
Figure 79 – RX Intra-pair Skew	155
Figure 80 – Far-End Retimed Loopback	158
Figure 81 – Far-End Analog Loopback	158
Figure 82 – Near-End Analog Loopback	159
Figure 83 – Compliant test patterns	161
Figure 84 – Low Transition Density Pattern (LTDP) starting with RD-	163
Figure 85 – Low Transition Density Pattern (LTDP) starting with RD+	164
Figure 86 – High Transition Density Pattern (HTDP) starting with RD-	165
Figure 87 – High Transition Density Pattern (HTDP) starting with RD+	166
Figure 88 – Low Frequency Spectral Content Pattern (LFSCP) starting with RD-	167
Figure 89 – Low Frequency Spectral Content Pattern (LFSCP) starting with RD+	168
Figure 90 – Simultaneous Switching Outputs Pattern (SSOP) starting with RD-	169
Figure 91 – Simultaneous Switching Outputs Pattern (SSOP) starting with RD+	169
Figure 92 – Lone-Bit Pattern (LBP) starting with RD-	170
Figure 93 – Lone-Bit Pattern (LBP) starting with RD+	170
Figure 94 – Composite-Bit Pattern (COMP) starting with RD-	173
Figure 95 – Composite-Bit Pattern (COMP) starting with RD+	176
Figure 96 – Example Circuit for Common Mode Transients	178
Figure 97 – Mated Connector Pair	179
Figure 98 – Mated Connector Pair, Pin Tail Detail	180
Figure 99 – Compliance Channel Loss for Gen2x	182
Figure 100 – Compliance Channel Loss for Gen1x	183
Figure 101 – SSC Profile Example: Triangular	187
Figure 102 – Spectral fundamental frequency comparison	188
Figure 103 – Jitter Deviations	189
Figure 104 – Edge to Edge Timing	190
Figure 105 – Differential Voltage Amplitude Measurement	195
Figure 106 – Differential Voltage Amplitude Measurement Pattern Example	195
Figure 107 – LFTP Pattern on High BW Scope (HBWS)	203

Figure 108 – Single Ended Rise and Fall Time	206
Figure 109 – Transmit Amplitude Test with Laboratory Load	207
Figure 110 – Transmit Amplitude Test with Compliance Interconnect Channel	207
Figure 111 – Receiver Amplitude Test--Setting Levels	209
Figure 112 – Receiver Amplitude Test	209
Figure 113 - Voltage at Receiver Input.....	210
Figure 114 – TX Long Term Frequency Measurement	213
Figure 115 – Receiver Model for Jitter	214
Figure 116 – Jitter at Receiver	215
Figure 117 – Jitter at Receiver, High Pass Function	215
Figure 118 – Transmitter Jitter Test (Gen1i, Gen2i).....	217
Figure 119 – Transmit Jitter Test with Compliance Interconnect Channel (Gen1x, Gen2x).....	217
Figure 120 – Receiver Jitter and CM Tolerance Test--Setting Levels	218
Figure 121 – Receiver Jitter and CM Tolerance Test.....	219
Figure 122 – Return Loss Test--Calibration	221
Figure 123 – Return Loss Test.....	222
Figure 124 – Intra-pair Skew test for a transmitter	224
Figure 125 – Receiver Intra-pair Skew Test-Setting Levels	224
Figure 126 – Receiver Intra-pair Skew Test.....	225
Figure 127 – Example Intra-pair Skew test for Transmitter (10.8 pS).....	225
Figure 128 – TX/RX Sequencing Transient Voltage Measurement	226
Figure 129 – AC Coupled Capacitance Measurement.....	227
Figure 130 – Squelch Detector Threshold Test--Setting Levels	230
Figure 131 – Squelch Detector Threshold Test.....	230
Figure 132 – TDR Impedance Test--Setting Risetime	232
Figure 133 – TDR Impedance Test	232
Figure 134 – TDR Impedance Test--Setting Risetime	233
Figure 135 – DC Coupled Common Mode Voltage Measurement.....	234
Figure 136 – AC Coupled Common Mode Voltage Measurement.....	235
Figure 137 – TDR Impedance Test	235
Figure 138 – OOB signals	237
Figure 139 – Transmitter examples.....	238
Figure 140 – Transmitter examples (concluded).....	239
Figure 141 – COMRESET sequence	240
Figure 142 – COMINIT sequence.....	242
Figure 143 – OOB signal detector	245
Figure 144 – Squelch detector	246
Figure 145 – Power-on Sequence.....	258
Figure 146 – PHYRDY to Partial/Slumber - Host initiated	261
Figure 147 – PHYRDY to Partial/Slumber - device initiated	262
Figure 148 – Bit designations	265
Figure 149 – Nomenclature reference.....	266
Figure 150 – Conversion examples.....	266
Figure 151 – Encoding examples.....	270
Figure 152 – Bit ordering and significance	276
Figure 153 – Single bit error with two character delay	278
Figure 154 – Single bit error with one character delay.....	278
Figure 155 – Transmission structures	279
Figure 156 – CONT _P usage example	285
Figure 157 – FIS type value assignments	319
Figure 158 – Register - Host to Device FIS layout.....	320
Figure 159 – Register - Device to Host FIS layout.....	322
Figure 160 – Set Device Bit - Device to Host FIS layout.....	324
Figure 161 – DMA Activate - Device to Host FIS layout.....	326
Figure 162 – DMA Setup – Device to Host or Host to Device FIS layout	327
Figure 163 – BIST Activate - Bidirectional.....	330

Figure 164 – PIO Setup - Device to Host FIS layout	333
Figure 165 – Data – Host to Device or Device to Host FIS layout	336
Figure 166 – Features enable/disable values	433
Figure 167 – Feature identification values	433
Figure 168 – Device Configuration Overlay data structure	435
Figure 169 – DMA Setup FIS definition for memory buffer selection	440
Figure 170 – Register values for successful result.....	441
Figure 171 – Set Device Bits FIS and SActive field	442
Figure 172 – Register values for error result.....	444
Figure 173 – READ FPDMA QUEUED command definition.....	445
Figure 174 – READ FPDMA QUEUED success status result values	446
Figure 175 – READ FPDMA QUEUED error status result values.....	447
Figure 176 – WRITE FPDMA QUEUED command definition	448
Figure 177 – WRITE FPDMA QUEUED success status result values.....	449
Figure 178 – WRITE FPDMA QUEUED error status result values	450
Figure 179 – READ LOG EXT Log Page 10h data structure definition.....	451
Figure 180 – Example DMA engine indirection for First-party DMA support	453
Figure 181 – Phy Event Counter Identifiers	457
Figure 182 – READ LOG EXT Log Page 11h data structure definition.....	459
Figure 183 – Generic enclosure services topology	464
Figure 184 – Simplified view of generic topology	464
Figure 185 – Enclosure services definition configuration.....	465
Figure 186 – Register Signature Indicating Presence of Enclosure Services Device.....	466
Figure 187 – Register Signature for Absent Enclosure Processor.....	466
Figure 188 – Command Block Register Fields Used in Enclosure Processor Communications	467
Figure 189 – I ² C Frame for Conveying an Enclosure Services Command	468
Figure 190 – WRITE SEP Command Block Registers.....	469
Figure 191 – I ² C Transactions Corresponding to a WRITE SEP Command	470
Figure 192 – READ SEP Command Block Registers	471
Figure 193 – I ² C Transactions Corresponding to READ SEP Command	471
Figure 194 – IDENTIFY SEP data structure definition	472
Figure 195 – SAF-TE Write Device Slot Status data structure	474
Figure 196 – SES Device Element data structure.....	475
Figure 197 – Example Subsystem.....	476
Figure 198 – SAF-TE Device ID field convention.....	476
Figure 199 – SES Slot Address field convention.....	477
Figure 200 – Activity LED definition for desktop behavior emulation	479
Figure 201 – Device Activity LEDs with Separate Wires.....	480
Figure 202 – Device Activity LEDs with Ribbon Cable.....	481
Figure 203 – Device Activity LEDs in a Storage Subsystem.....	482
Figure 204 – Software reset to control port result values.....	483
Figure 205 – Port Multiplier Signature.....	485
Figure 206 – SActive register definition.....	492
Figure 207 – SNotification register definition.....	492
Figure 208 – Error handling architecture.....	494
Figure 209 – Port Multiplier Overview	503
Figure 210 – Register values for an unsupported command	513
Figure 211 – Static Information Registers	516
Figure 212 – Status Information and Control Registers	518
Figure 213 – Features Supported Registers	522
Figure 214 – Features Enabled Registers.....	523
Figure 215 – Vendor Unique Registers	524
Figure 216 – PSCR definition	525
Figure 217 – READ PORT MULTIPLIER command definition.....	526
Figure 218 – READ PORT MULTIPLIER success status result values	527
Figure 219 – READ PORT MULTIPLIER error status result values	527

Figure 220 – WRITE PORT MULTIPLIER command definition	528
Figure 221 – WRITE PORT MULTIPLIER success status result values	529
Figure 222 – WRITE PORT MULTIPLIER error status result values	529
Figure 223 – Port Selector Overview.....	532
Figure 224 – Example Failover Application with Two Hosts	533
Figure 225 – Port selection signal based on assertion of COMRESET to assertion of following COMRESET	535
Figure 226 – Complete port selection signal consisting of two sequences with requisite inter-reset spacings.....	536
Figure 227 – Control State Machine.....	538
Figure 228 – Phy Block Diagram.....	539
Figure 229 – Concept summary interconnect structure	570
Figure 230 – An example of signal connections with one I/O Controller.....	571
Figure 231 – Example of signal connections with two I/O Modules	573
Figure 232 – High Speed Channels – Configuration 0.....	574
Figure 233 – High-Speed Channels – Configuration 1	574
Figure 234 – Low Speed Channels	575
Figure 235 – Interconnect Channels	575
Figure 236 – I/O Controller Module Connector Rendering.....	576
Figure 237 – Connector Pin Layout and Pin Lengths.....	577
Figure 238 – I/O Controller Module Connector Receptacle Engineering Drawing.....	578
Figure 239 – Side View of Connector.....	578
Figure 240 – I/O Controller Module Connector Locations on 1xWide I/O module	580
Figure 241 – I/O Controller Module Connector Locations on 2xWide I/O Module	581

TABLE OF TABLES

Table 1 – State Table Cell Description	35
Table 2 – Signal and Power SATA Plug and Nominal Mate Sequence	67
Table 3 – Allowed values for dimension A and B for device-to-backplane mating	76
Table 4 – Housing and contact electrical parameters, test procedures, and requirements	79
Table 5 – Mechanical test procedures and requirements	81
Table 6 – Environmental parameters, test procedures, and requirements	82
Table 7 – Additional requirement	82
Table 8 – Connector test sequences	83
Table 9 – Multi Lane Pin Assignments	103
Table 10 – Internal Cable / Connector Measurement Parameter and Requirements	103
Table 11 – External Single Lane Cable / Connector Measurement Parameter and Requirements	104
Table 12 – External Multi Lane Cable / Connector Measurement Parameter and Requirements	104
Table 13 – Common Interconnect Measurement Procedure Methodologies	107
Table 14 – Interconnect Test Methodologies / Procedures	108
Table 15 – Power segment pin P11 activity signal electrical parameters	113
Table 16 – Host activity signal electrical parameters	114
Table 17 – Activity signal functional states	115
Table 18 – Host staggered spin-up control electrical requirements	115
Table 19 – Comparator voltages for alternate example presence detection circuit	119
Table 20 – General Specifications	131
Table 21 – Transmitter Specifications	133
Table 22 – Transmitted Signal Requirements	135
Table 23 – Receiver Specifications	137
Table 24 – Lab-Sourced Signal (for Receiver Tolerance Testing)	138
Table 25 – OOB Specifications	140
Table 26 – Frame Error Rate Confidence Levels versus Sample Size	193
Table 27 – Bit Error Rate Confidence Levels versus Sample Size	194
Table 28 – OOB Signal Times	237
Table 29 – Interface Power States	248
Table 30 – 5B/6B coding	269
Table 31 – 3B/4B coding	269
Table 32 – Valid data characters	271
Table 33 – Valid control characters	275
Table 34 – Description of primitives	281
Table 35 – Primitive encoding	282
Table 36 – SRST write from host to device transmission breaking through a device to host Data FIS	288
Table 37 – Command Shadow Register Block register transmission example	289
Table 38 – Data from host to device transmission example	290
Table 39 – Simplified Shadow Register Block register numbering	318
Table 40 – IDENTIFY DEVICE information	422
Table 41 – IDENTIFY PACKET DEVICE information	428
Table 42 – SCR definition	486
Table 43 – SCR Definition	487
Table 44 – Port selection signal inter-reset timing requirements	535
Table 45 – CRC and scrambler calculation example - PIO Write Command	554
Table 46 – J1, J2, J3 Pin Assignments	582
Table 47 – J4, J5, J6 Pin Assignments	582

1 Revision history

1.1 Revision 2.5 (Ratification Date October 27, 2005)

Release that integrates and consolidates the following previously published specifications including all erratum against those specifications:

- ☐ Serial ATA revision 1.0a
- ☐ Serial ATA II: Extensions to Serial ATA 1.0a revision 1.2
- ☐ Serial ATA II: Electrical Specification revision 1.0
- ☐ Serial ATA II: Cable and Connectors Volume 1 revision 1.0
- ☐ Serial ATA II: Cable and Connectors Volume 2 revision 1.0
- ☐ Serial ATA II: Port Multiplier revision 1.2
- ☐ Serial ATA II: Port Selector revision 1.0

2 Scope

This specification defines a high-speed serialized ATA data link interface (specifying Phy, Link, Transport, and Application layers). The serialized interface uses the command set from the ATA/ATAPI-6 standard, augmented with Native Command Queuing commands optimized for the serialized interface. The serialized ATA interface is defined in a register-compatible manner with parallel ATA to enable backward compatibility with parallel ATA drivers. The physical interface is defined to ease integration (low pin count, low voltages) and enable scalable performance (with currently defined data rates of 1.5 Gbps and 3.0 Gbps).

Complementary components are also specified including interconnect solutions for various applications, port expansion devices, and failover devices.

Normative information is provided to allow interoperability of components designed to this specification. Informative information, when provided, may illustrate possible design implementation.

3 Normative references

The following standards contain provisions that, through reference in the text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

Copies of the following documents can be obtained from ANSI: Approved ANSI standards, approved and draft international and regional standards (ISO, IEC, CEN/CENELEC, ITUT), and approved and draft foreign standards (including BSI, JIS, and DIN). For further information, contact ANSI Customer Service Department at 212-642-4900 (phone), 212-302-1286 (fax) or via the World Wide Web at <http://www.ansi.org>.

Additional availability contact information is provided below as needed.

3.1 Approved references

The following approved ANSI standards, approved international and regional standards (ISO, IEC, CEN/CENELEC, ITUT), may be obtained from the international and regional organizations who control them.

AT Attachment with Packet Interface – 5 (ATA/ATAPI-5) [ANSI INCITS 340-2000]

AT Attachment with Packet Interface – 6 (ATA/ATAPI-6) [ANSI INCITS 361-2002]

Serial Attached SCSI (SAS) [ANSI INCITS 376-2003]

SCSI-3 Enclosure Services (SES) Command Set [ANSI INCITS 305-1998]

SCSI-3 Enclosure Services (SES) Amendment 1 [ANSI INCITS 305-1998/AM1-2000]

SCSI Block Commands 2 (SBC-2) [ANSI INCITS 405-2005]

SCSI Primary Commands 3 (SPC-3) [ANSI INCITS 408-2005]

ATA/ATAPI Host Adapters Standard [ANSI INCITS 370-2004]

To obtain copies of these documents, contact Global Engineering or INCITS.

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Additional material and draft versions available from <http://www.T10.org> and <http://www.T13.org>.

SAF-TE – SCSI Accessed Fault-Tolerant Enclosure version 1.00 [revision R041497, April 14, 1997]. Available for download at <http://www.intel.com/design/servers/ipmi/pdf/sr041497.pdf>.

I²C-Bus Specification version 2.1. Available from Philips Semiconductors at <http://www.semiconductor.philips.com/buses/i2c>.

IPMB - Intelligent Platform Management Bus Communications Protocol Specification version 1.0. Available for download at <http://www.intel.com/design/servers/ipmi/spec.htm>.

IPMI - Intelligent Platform Management Interface Specification version 1.5. Available for download at <http://www.intel.com/design/servers/ipmi/spec.htm>.

JEDEC Standards (Located on <http://www.jedec.com>).

- ☐ JESD22-A114-B, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- ☐ JESD22-C101-A, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components"

The following standards published by the SFF Committee are referenced. These standards are available for download through <http://www.sffcommittee.org>.

- ☐ SFF-8111, 1.8" drive form factor (60x70mm)
- ☐ SFF-8201, 2.5" drive form factor
- ☐ SFF-8301, 3.5" drive form factor
- ☐ SFF-8470, Shielded High Speed Serial Multilane Copper Connector
- ☐ SFF-8484, Multi Lane Internal Serial Attachment Connector

The following EIA-364-xx standards published by EIA are referenced. To obtain copies of these documents, contact Global Engineering.

- ☐ EIA-364-09, Durability Test Procedure for Electrical Connectors and Contacts
- ☐ EIA-364-13, Mating and Unmating Forces Test Procedure for Electrical Connectors
- ☐ EIA-364-17, Temperature Life with or without Electrical Load Test Procedure for Electrical Connectors and Sockets
- ☐ EIA-364-18, Visual and Dimensional Inspection for Electrical Connector
- ☐ EIA-364-20, Withstanding Voltage Test Procedure for Electrical Connectors, Sockets and Coaxial Contacts
- ☐ EIA-364-21, Insulation Resistance Test Procedure for Electrical Connectors, Sockets, and Coaxial Contacts
- ☐ EIA-364-23, Low Level Contact Resistance Test Procedure for Electrical Connectors and Sockets
- ☐ EIA-364-27, Mechanical Shock (Specified Pulse) Test Procedure for Electrical Connectors
- ☐ EIA-364-28, Vibration Test Procedure for Electrical Connectors and Sockets
- ☐ EIA-364-31, Humidity Test Procedure for Electrical Connectors and Sockets
- ☐ EIA-364-32, Thermal Shock (Temperature Cycling) Test Procedure for Electrical Connectors and Sockets
- ☐ EIA-364-38, Cable Pull-Out Test Procedure for Electrical Connectors
- ☐ EIA-364-41, Cable Flexing Test Procedure for Electrical Connectors
- ☐ EIA-364-65, Mixed Flowing Gas

Many of the EIA-364-xx specifications are available for download from:
<http://www.ecaus.org/engineering/Downloads/eia364.htm>

The following form factor standards published by EIA are referenced. These standards can be obtained from Global Engineering.

- ☐ EIA-740, specification for small form factor 3.5" disk drives
- ☐ EIA-720, specification for small form factor 2.5" disk drives

3.2 References under development

The following ANSI standards under development are referenced. Draft versions of these standards are available from <http://www.T10.org> or <http://www.T13.org>.

SCSI Enclosure Services - 2 (SES-2) [ANSI INCITS T10/1559-D]

Serial Attached SCSI – 1.1 (SAS-1.1) [ANSI INCITS T10/1601-D]

ATA/ATAPI-8 Command Set [ANSI INCITS T13/1699-D]

3.3 Other references

The 8b/10b code used in Serial ATA is based on the following published references:

- [1] A.X. Widmer and P.A. Franaszek, "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code." *IBM Journal of Research and Development*, 27, no. 5: 440-451 (September, 1983)
- [2] U.S. Patent 4,486,739. Peter A. Franaszek and Albert X. Widmer. *Byte Oriented DC Balanced (0,4) 8B/10B Partitioned Block Transmission Code*. (Dec. 4, 1984)

4 Definitions, abbreviations, and conventions

4.1 Definitions and abbreviations

4.1.1 active port

The active port is the currently selected host port on a Port Selector.

4.1.2 ATA (AT Attachment)

ATA defines the physical, electrical, transport, and command protocols for the attachment of storage devices.

4.1.3 ATAPI (AT Attachment Packet Interface) device

A device implementing the Packet Command feature set.

4.1.4 BER (bit error rate)

4.1.5 bitrate

Reciprocal of the unit interval. $\text{Bitrate} = 1 / \text{UI}$.

4.1.6 bit synchronization

The state in which a receiver has synchronized the internal receiver clock to the external transmitter and is delivering retimed serial data.

4.1.7 burst

A short pulse of data starting from and ending with the idle condition on the interface. These are used for OOB signaling.

4.1.8 byte

A byte is 8 bits of data. The least significant bit is bit 0 and the most significant bit is bit 7. The most significant bit is shown on the left. In the encoding process the bits in a byte are referred to as HGFEDCBA, or "A,B,C,D,E,F,G,H" where A corresponds to bit 0 and H corresponds to bit 7. Case is significant.

4.1.9 character

A character is a representation of a data byte or control code. There are two types of characters: data characters and control characters.

4.1.10 character alignment

Character alignment is a receiver action that resets the character boundary to that of the comma sequence found in the K28.5 control character of the ALIGN_P primitive, and establishes Dword synchronization of the incoming serial data stream.

4.1.11 character slipping

Character slipping is the receiver action that realigns the receiver's clock to the received bit stream by adding or removing bit times within the characters of the ALIGN_P primitive.

4.1.12 code violation

A code violation is an error that occurs in the reception process as a result of (1) a running disparity violation or (2) an encoded character that does not translate to a valid data or control character or (3) an encoded character that translates to a control character other than K28.5 or K28.3 in byte 0 of a Dword or (4) an encoded character that translates to any control character (valid or invalid) in bytes 1-3 of a Dword.

4.1.13 comma character

A comma character is a control character, that when encoded, contains the comma sequence. In Serial ATA the only comma character used is K28.5, and only the ALIGN_P primitive contains the comma character. The comma sequence is the first seven bits of the encoded character.

4.1.14 comma sequence

The comma sequence is a seven-bit sequence of 0011111 or 1100000 in an encoded stream. The comma sequence is unique in that it appears only in a single encoded character, and furthermore, cannot appear in any subset of bits in adjacent encoded characters. This unique property allows the comma sequence to be used for determining alignment of the received data stream.

4.1.15 command aborted

Command aborted is command completion with ABRT set to one in the Error register, and ERR set to one in the Status register.

4.1.16 command completion

Command completion describes the completion of an action requested by command, applicable to the device. Command completion also applies to the case where the command has terminated with an error, and the following actions occurred:

- a) the appropriate bits of the Status Register have been updated
- b) BSY & DRQ have been cleared to zero
- c) assertion of INTRQ (if nIEN is active-low), assuming that the command protocol specifies INTRQ to be asserted

In Serial ATA, the register contents are transferred to the host using a Register - Device-to-Host FIS.

4.1.17 command packet

A data structure transmitted to the device during the execution of a PACKET command that includes the command and command parameters.

4.1.18 concentrator

A concentrator is a generic term used to describe a logical block that has multiple Serial ATA ports to connect to Serial ATA devices plus some small number of ports to connect to a host. In the simplest case a concentrator may be a host bus adapter (HBA) that is plugged into the host that connects to some number of Serial ATA devices (like a PCI Serial ATA controller card). A concentrator may also be an internal or external RAID controller such as a fibre-channel to Serial ATA RAID controller, or may be some element that expands the number of ports through a fan-out scheme, like a Port Multiplier.

4.1.19 Control Block registers

Control Block registers are interface registers used for device control and to post alternate status.

4.1.20 control character

A control character is a combination of a byte value with the control variable equal to K.

4.1.21 control port

The Port Multiplier has one port address reserved for control and status communication with the Port Multiplier itself. The control port has port address Fh.

4.1.22 control variable

The control variable, Z, is a flag that determines the code set to be used to interpret a data byte. The control variable has the value D (for data characters) or K (for control characters).

4.1.23 CRC (Cyclic Redundancy Check)

An error checking mechanism that checks data integrity by computing a polynomial algorithm based checksum. In Serial ATA a 32-bit CRC is calculated over the contents of a Frame Information Structure. The Serial ATA CRC is the Dword in a frame that immediately precedes the EOF_P primitive.

4.1.24 data character

A data character is a combination of a byte value with the control variable equal to D.

4.1.25 data signal source

An instrument which provides a Serial ATA data signal.

4.1.26 device

Device is a storage peripheral. Traditionally, a device on the interface has been a hard disk drive, but any form of storage device may be placed on the interface provided the device adheres to this specification and to an ATA standard.

4.1.27 device port

The device port is a port on a Port Multiplier or a Port Selector that is connected to the device. Port Multipliers may have up to 15 device ports. Port Selectors have one device port.

4.1.28 DCB (DC block)

The DC block is defined as a device that passes frequencies from 10 MHz to at least 12 GHz with minimal effect on the amplitude or phase of the signal.

4.1.29 differential signal

The differential signal is the voltage on the positive conductor minus the voltage on the negative conductor (i.e. TX+ – TX-).

4.1.30 DJ (deterministic jitter – peak to peak)

All jitter sources that have bounded probability distribution functions (i.e. values outside the bounds have probability zero). Four kinds of deterministic jitter are identified: duty cycle distortion,

data dependent (ISI), sinusoidal, and uncorrelated (to the data) bounded. DJ is characterized by its bounded, peak-to-peak value.

4.1.31 DMA (direct memory access)

DMA is a means of data transfer between device and host memory without host processor intervention.

4.1.32 Dword

A Dword is thirty-two (32) bits of data. A Dword may be represented as 32 bits, as two adjacent words, or as four adjacent bytes. When shown as bits the least significant bit is bit 0 and most significant bit is bit 31. The most significant bit is shown on the left. When shown as words the least significant word (lower) is word 0 and the most significant (upper) word is word 1. When shown as bytes the least significant byte is byte 0 and the most significant byte is byte 3. See Figure 1 for a description of the relationship between bytes, words, and Dwords. Dwords are aligned on four byte boundaries to a zero reference defined by a comma character.

4.1.33 Dword synchronization

The state in which a receiver has recognized the comma sequence and is producing an aligned data stream of Dwords (four contiguous bytes) from the zero-reference of the comma character.

4.1.34 EMI (Electromagnetic Interference)

4.1.35 encoded character

An encoded character is the output of the 8b/10b encoder – the result of encoding a character. An encoded character consists of 10 bits, where bit 0 is the most significant bit and bit 9 is the least significant. The bits in an encoded character are symbolically referred to as “abcdeifghj” where “a” corresponds to bit 0 and “j” corresponds to bit 9. Case is significant. Note the out-of-order representation. See Figure 149 for a description of the relationship between bytes, characters and encoded characters.

4.1.36 endpoint device

An endpoint device is an ATA or ATAPI device, as reported by the device signature after power-on or reset. This may include hard disk drives, optical disk drives, and tape drives.

4.1.37 elasticity buffer

The elasticity buffer is a portion of the receiver where character slipping and/or character alignment is performed.

4.1.38 Fbaud

The nominal rate of data through the channel.

4.1.39 FER (frame error rate)

Refer to section 7.2.2.1.2.

4.1.40 First-party DMA Data Phase

The First-party DMA Data Phase is the period from the reception of a DMA Setup FIS until either the exhaustion of the associated data transfer count or the assertion of the ERR bit in the shadow Status register.

4.1.41 First-party DMA access

First-party DMA access is a method by which a device accesses host memory.

4.1.42 FIS (Frame Information Structure)

The user payload of a frame, does not include the SOF_P, CRC, and EOF_P delimiters.

4.1.43 frame

A frame is an indivisible unit of information exchanged between a host and device. A frame consists of an SOF_P primitive, a Frame Information Structure, a CRC calculated over the contents of the FIS, and an EOF_P primitive.

4.1.44 Gen1

Refers to first generation signaling characterized by a speed of 1.5 Gbps. Refer to section 7.

4.1.45 Gen1i

The internal electrical specifications at 1.5 Gbps with cable lengths up to 1 m.

4.1.46 Gen1m

The electrical specifications used in the Short Backplane Application and the External Desktop Application defined at 1.5 Gbps.

4.1.47 Gen1x

The external cabled applications or Long Backplane Applications defined at 1.5 Gbps.

4.1.48 Gen2

Refers to second generation signaling characterized by a speed of 3.0 Gbps. Refer to section 7.

4.1.49 Gen2i

The internal electrical specifications at 3.0 Gbps with cable lengths up to 1 m.

4.1.50 Gen2m

The electrical specifications used in the Short Backplane Application and the External Desktop Application defined at 3.0 Gbps.

4.1.51 Gen2x

The external cabled applications or Long Backplane Applications defined at 3.0 Gbps.

4.1.52 HBA (Host Bus Adapter)

HBA is a component that connects to the host system's expansion bus to provide connectivity for devices. HBAs are also often referred to as controller cards or merely controllers.

4.1.53 HBWS (High Bandwidth Scope)

An oscilloscope with an analog bandwidth of 10 GHz or greater in the measurement path.

4.1.54 HFTP (High Frequency Test Pattern)

This pattern provides the maximum frequency allowed within the Serial ATA encoding rules. Pattern: 1010101010 1010101010b = encoded D10.2. The pattern is repetitive.

4.1.55 host port

The host port is the port that is used to connect the Port Multiplier or Port Selector to a host. Port Multipliers have one host port. Port Selectors have two host ports.

4.1.56 inactive port

The inactive port is the host port that is not currently selected on the Port Selector.

4.1.57 interrupt pending

Interrupt pending is an internal state of the device that exists when the device protocol requires the device to notify the host of an event by asserting INTRQ, given the condition where nIEN is asserted active-low to zero.

4.1.58 ISI (inter-symbol interference)

Data-dependent deterministic jitter caused by the time differences required for the signal to arrive at the receiver threshold when starting from different places in bit sequences (symbols). For example media attenuates the peak amplitude of the bit sequence [0,1,0,1...], more than it attenuates the peak amplitude of the bit sequence [0,0,0,0,1,1,1,1...], thus the time required to reach the receiver threshold with the [0,1,0,1...] sequence is less than required from the [0,0,0,0,1,1,1,1...] sequence. The run length of 4 produces a higher amplitude which takes more time to overcome when changing bit values and therefore produces a time difference compared to the run length of 1 bit sequence. When different run lengths are mixed in the same transmission the different bit sequences (symbols) therefore interfere with each other. ISI is expected whenever any bit sequence has frequency components that are propagated at different rates by the transmission media. This translates into a high level of high-frequency, data-dependent, jitter.

4.1.59 JMD (jitter measuring device)

A device used to measure jitter. Examples are a bit error rate tester (BERT), a timing interval analyzer (TIA), a single shot capture oscilloscope and processing software, or a HBWS.

4.1.60 junk

An 8b/10b encoded data Dword sent between a CONT_P primitive and another primitive transmitted on the link. All junk Dwords shall be ignored by the receiver.

4.1.61 LBA (Logical Block Address)

As defined in the ATA/ATAPI-6 standard.

4.1.62 LBP (lone bit pattern)

This pattern is defined in section 7.2.4.3.5. The pattern is repetitive.

4.1.63 LED (Light Emitting Diode)

4.1.64 legacy mode

Legacy mode is the mode of operation which provides software-transparent communication of commands and status between a host and device using the ATA Command Block and Control Block registers.

4.1.65 legal character

A legal character is one for which there exists a valid decoding, either into the data character or control character fields. Due to running disparity constraints not all 10-bit combinations result in a legal character. Additional usage restrictions in Serial ATA result in a further reduction in the SATA defined control character space.

4.1.66 LFSR (Linear Feedback Shift Register)

Refer to section 9.4.5 for details on using a LFSR in scrambling.

4.1.67 LFTP (low frequency test pattern)

This pattern provides a low frequency, which is allowed within the Serial ATA encoding rules. Pattern: 0111100011 1000011100b = encoded D30.3. The pattern is repetitive.

4.1.68 LL (laboratory load)

An electrical test system connected to the unit under test. The LL receives a signal from the UUT at the defined impedance level of 100 Ohms differential and 25 Ohms common mode.

4.1.69 LSS (laboratory sourced signal or lab-sourced signal)

An instrument and electrical test system connected to the unit under test. The LSS provides a signal to the UUT at the defined impedance level of 100 Ohms differential and 25 Ohms common mode.

4.1.70 MFTP (mid frequency test pattern)

This pattern provides a middle frequency which is allowed within the Serial ATA encoding rules. Pattern: 1100110011 0011001100b = encoded D24.3. The pattern is repetitive.

4.1.71 OOB (Out-of-Band signaling)

OOB signaling is a pattern of ALIGN_P primitives or Dwords composed of D24.3 characters and idle time and is used to initialize the Serial ATA interface. OOB signaling is also used to recover from low power states and to signal specific actions during test modes. Refer to section 8.

4.1.72 OS-aware hot plug

The insertion of a SATA device into a backplane that has power shutdown. The backplane is later powered, and both the device and the host power up, and the host-initiated OOB sequence determines the time that SATA operations begin.

4.1.73 OS-aware hot removal

The removal of a SATA device from a powered backplane, that has been first placed in a quiescent state.

4.1.74 Phy offline

In this mode the host Phy is forced off and the host Phy does not recognize nor respond to COMINIT or COMWAKE. This mode is entered by setting the DET field of the SControl register to 0100b. This is a mechanism for the host to turn off its Phy.

4.1.75 PIO (programmed input/output)

PIO is a means of accessing device registers. PIO is also used to describe one form of data transfers. PIO data transfers are performed by the host processor utilizing PIO register accesses to the Data register.

4.1.76 port address

The control port and each device port present on a Port Multiplier have a port address. The port address is used to route FISes between the host and a specific device or the control port.

4.1.77 PRD (Physical Region Descriptor)

A PRD table is a data structure used by DMA engines that comply with the ATA/ATAPI Host Adapters standard. The PRD describes memory regions to be used as the source or destination of data during DMA transfers. A PRD table is often referred to as a scatter/gather list.

4.1.78 primitive

A primitive is a single Dword of information that consists of a control character in byte 0 followed by three additional data characters in bytes 1-3.

4.1.79 protocol-based port selection

Protocol-based port selection is a method that may be used by a host to select the host port that is active on a Port Selector. Protocol-based port selection uses a sequence of Serial ATA OOB Phy signals to select the active host port.

4.1.80 quiescent power condition

Entering a quiescent power condition for a particular Phy is defined as the Phy entering the idle bus condition as defined in section 7.5.2.

4.1.81 RJ (random jitter)

Random jitter is Gaussian. Random jitter is equal to the peak to peak value of 14 times the 1σ standard deviation value given the 10^{-12} BER requirement.

4.1.82 sector

A set of data bytes accessed and referenced as a unit.

4.1.83 SEMB (Serial ATA Enclosure Management Bridge)

A SEMB is a logical block that translates Serial ATA transactions into I²C transactions to communicate enclosure services commands to a Storage Enclosure Processor.

4.1.84 SEP (Storage Enclosure Processor)

A SEP is a logical block that interfaces with the various enclosure sensors and actuators in an enclosure and is controlled through an I²C interface to the Serial ATA Enclosure Management Bridge.

4.1.85 Shadow Register Block registers

Shadow Register Block registers are interface registers used for delivering commands to the device or posting status from the device.

4.1.86 side-band port selection

Side-band port selection is a method that may be used by a host to select the host port that is active on a Port Selector. Side-band port selection uses a mechanism that is outside of the Serial ATA protocol for determining which host port is active. The port selection mechanism used in implementations that support side-band port selection is outside the scope of this specification.

4.1.87 SMART

Self-Monitoring, Analysis, and Reporting Technology for prediction of device degradation and/or faults.

4.1.88 SSC (spread spectrum clocking)

The technique of modulating the operating frequency of a signal slightly to spread its radiated emissions over a range of frequencies. This reduction in the maximum emission for a given frequency helps meet radiated emission requirements.

4.1.89 surprise hot plug

The insertion of a SATA device into a backplane that has power present. The device powers up and initiates an OOB sequence.

4.1.90 surprise hot removal

The removal of a SATA device from a powered backplane, without first being placed in a quiescent state.

4.1.91 SYNC Escape

The condition when a SYNC_P primitive is used to escape from the present FIS transmission on the interface and resynchronize the link back to an IDLE state. The most common use of the SYNC Escape mechanism is to bring the link to an IDLE condition in order to send a Control Register FIS with a software reset to the device, but can be used at other times to recover link communication from erroneous conditions. A SYNC Escape is requested by the Transport layer to the Link layer.

4.1.92 TDR (time domain reflectometer)

An instrument used to test the impedance of the unit under test.

4.1.93 TIA (timing interval analyzer)

Timing interval analyzer with Duty Cycle Distortion and ISI noise floor performance of better than 5% of a UI for K28.5 with less than 67 ps rise and fall times.

4.1.94 TJ (total jitter)

Peak to peak value of $(14 * RJ_G) + DJ$.

4.1.95 UI (unit interval)

Equal to the time required to transmit one bit (e.g. 666.667 ps for Gen1).

4.1.96 unrecoverable error

An unrecoverable error is defined as having occurred at any point when the device sets either the ERR bit or the DF bit to one in the Status register at command completion.

4.1.97 UUT (unit under test)

The product under test and the other half of the “mated” connector (which is physically on the laboratory load but considered part of the UUT).

4.1.98 VNA (vector network analyzer)

An instrument used to test the impedance of the unit under test.

4.1.99 word

A word is sixteen (16) bits of data. A word may be represented as 16 bits or as two adjacent bytes. When shown as bits the least significant bit is bit 0 and most significant bit is bit 15. The most significant bit is shown on the left. When shown as bytes the least significant byte (lower) byte is byte 0 and the most significant byte (upper) byte is byte 1. See Figure 1 for a description of the relationship between bytes, words and Dwords.

4.1.100 zero crossing

To locate the zero crossing of a Data Eye, turn on the horizontal histogram function to horizontally enclose all waveforms associated with the “edge” and vertically limit to +/-5% of the waveform voltage. The “zero crossing” is the location of the mean of the waveforms.

4.2 Conventions

Lowercase is used for words having the normal English meaning. Certain words and terms used in this document have a specific meaning beyond the normal English meaning. These words and terms are defined either in section 4.1 or in the text where they first appear.

The names of abbreviations, commands, fields, and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE). Fields containing only one bit are usually referred to as the “name” bit instead of the “name” field.

Names of device registers begin with a capital letter (e.g., LBA Mid register).

Primitive names are followed by a ‘P’ subscript (e.g., R_OK_P).

4.2.1 Precedence

If there is a conflict between text, figures, and tables, the precedence shall be tables, figures, and then text.

4.2.2 Keywords

Several keywords are used to differentiate between different levels of requirements and optionality.

4.2.2.1 expected

A keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

4.2.2.2 mandatory

A keyword indicating items to be implemented as defined by this standard.

4.2.2.3 may

A keyword that indicates flexibility of choice with no implied preference.

4.2.2.4 obsolete

A keyword used to describe bits, bytes, fields, and code values that no longer have consistent meaning or functionality from one implementation to another. However, some degree of functionality may be required for items designated as “obsolete” to provide for backward compatibility. An obsolete bit, byte, field, or command shall never be reclaimed for any other use in any future standard. Bits, bytes, fields, and code values that had been designated as “obsolete” in previous standards may have been reclassified as “retired” in this standard based on the definitions herein for “obsolete” and “retired”.

4.2.2.5 optional

A keyword that describes features that are not required by this standard. However, if any optional feature defined by the standard is implemented, the feature shall be implemented in the way defined by the standard.

4.2.2.6 retired

A keyword indicating that the designated bits, bytes, fields, and code values that had been defined in previous standards are not defined in this standard and may be reclaimed for other uses in future standards. If retired bits, bytes, fields, or code values are utilized before they are reclaimed, they shall have the meaning or functionality as described in previous standards.

4.2.2.7 reserved

A keyword indicating reserved bits, bytes, words, fields, and code values that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this or other standards. A reserved bit, byte, word, or field shall be cleared to zero, or in accordance with a future extension to this standard. The recipient shall not check reserved bits, bytes, words, or fields. Receipt of reserved code values in defined fields shall be treated as a command parameter error and reported by returning command aborted.

4.2.2.8 shall

A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other standard conformant products.

4.2.2.9 should

A keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase "it is recommended".

4.2.3 Numbering

Numbers that are not immediately followed by a lowercase "b" or "h" are decimal values. Numbers that are immediately followed by a lowercase "b" (e.g., 01b) are binary values. Numbers that are immediately followed by a lowercase "h" (e.g., 3Ah) are hexadecimal values.

4.2.4 Dimensions

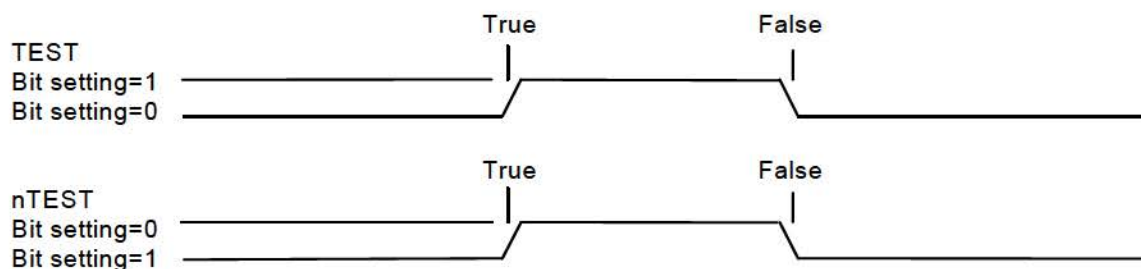
All dimensions are shown in millimeters unless otherwise noted.

4.2.5 Signal conventions

Signal names are shown in all uppercase letters.

4.2.6 Bit conventions

Bit names are shown in all uppercase letters except where a lowercase n precedes a bit name. If there is no preceding n, then when BIT is set to one the meaning of the bit is true, and when BIT is cleared to zero the meaning of the bit is false. If there is a preceding n, then when nBIT is cleared to zero the meaning of the bit is true and when nBIT is set to one the meaning of the bit is false.



4.2.7 State machine conventions

For each function to be completed a state machine approach is used to describe the sequence requirements. Each function is composed of several states to accomplish a set goal. Each state of the set is described by an individual state table. Table 1 below shows the general layout for each of the state tables that comprise the set of states for the function.

Table 1 – State Table Cell Description

State Designator: State name		Action list _[P W]	
	Transition condition 0	→	Next state 0
	Transition condition 1	→	Next state 1

Each state is identified by a state designator and a state name. The state designator is unique among all states in all state diagrams in this document. The state designator consists of a set of letters that are capitalized followed by a unique number. The state name is a brief description of the primary action taken during the state, and the same state name may appear in other state diagrams. If the same primary function occurs in other states in the same state diagram, they are designated with a unique letter at the end of the name. Additional actions may be taken while in a state and these actions are described in the state description text.

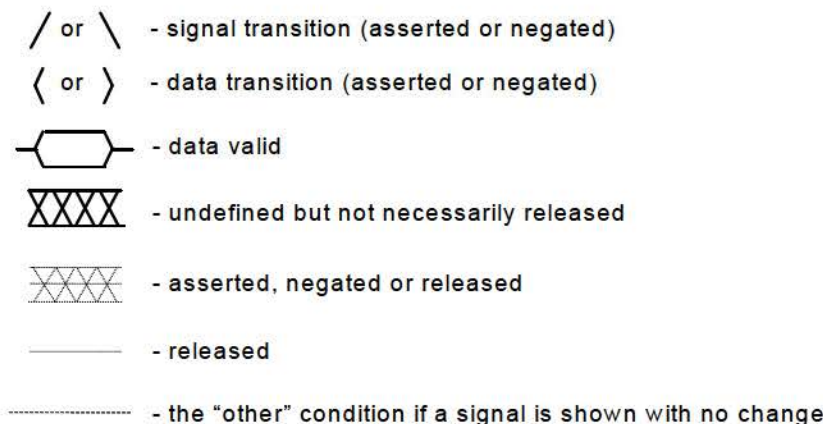
Each transition is identified by a transition label and a transition condition. The transition label consists of the state designator of the state from which the transition is being made followed by the state designator of the state to which the transition is being made. The transition condition is a brief description of the event or condition that causes the transition to occur and may include a transition action that is taken when the transition occurs. This action is described fully in the transition description text.

Upon entry to a state, all actions to be executed in that state are executed. If a state is re-entered from itself, all actions to be executed in the state are executed again.

It is assumed that all actions are executed within a state and that transitions from state to state are instantaneous.

4.2.8 Timing conventions

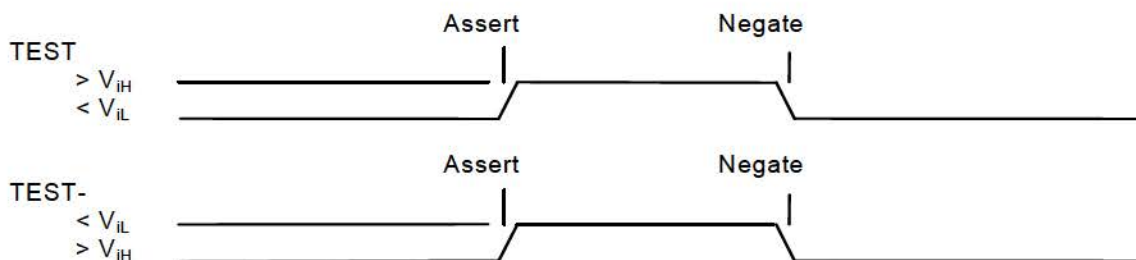
Certain symbols are used in the timing diagrams. These symbols and their respective definitions are listed below.



All signals are shown with the asserted condition facing to the top of the page. The negated condition is shown towards the bottom of the page relative to the asserted condition.

The interface uses a mixture of negative and positive signals for control and data. The terms asserted and negated are used for consistency and are independent of electrical characteristics.

In all timing diagrams, the lower line indicates negated, and the upper line indicates asserted. The following illustrates the representation of a signal named TEST going from negated to asserted and back to negated, based on the polarity of the signal.



In the case of the Serial ATA interface itself, all signals are differential. Each signal is actually transmitted or received on two lines and the state of the signal is determined by the relationship of these lines to each other rather than to a reference ground. These two lines are named the same except the names end in either "+" or "-". The above symbols are used when representing these signals however, assertion of a differential signal is assumed to mean that the "+" signal line is positive in relation to the "-" line. In other words, if the signal is "TX", assertion means that the voltage on TX+ minus the voltage on TX- results in a positive number. Conversely, negation means that the result is a negative number.

4.2.9 Byte, word and Dword Relationships

Figure 1 illustrates the relationship between bytes, words and Dwords.

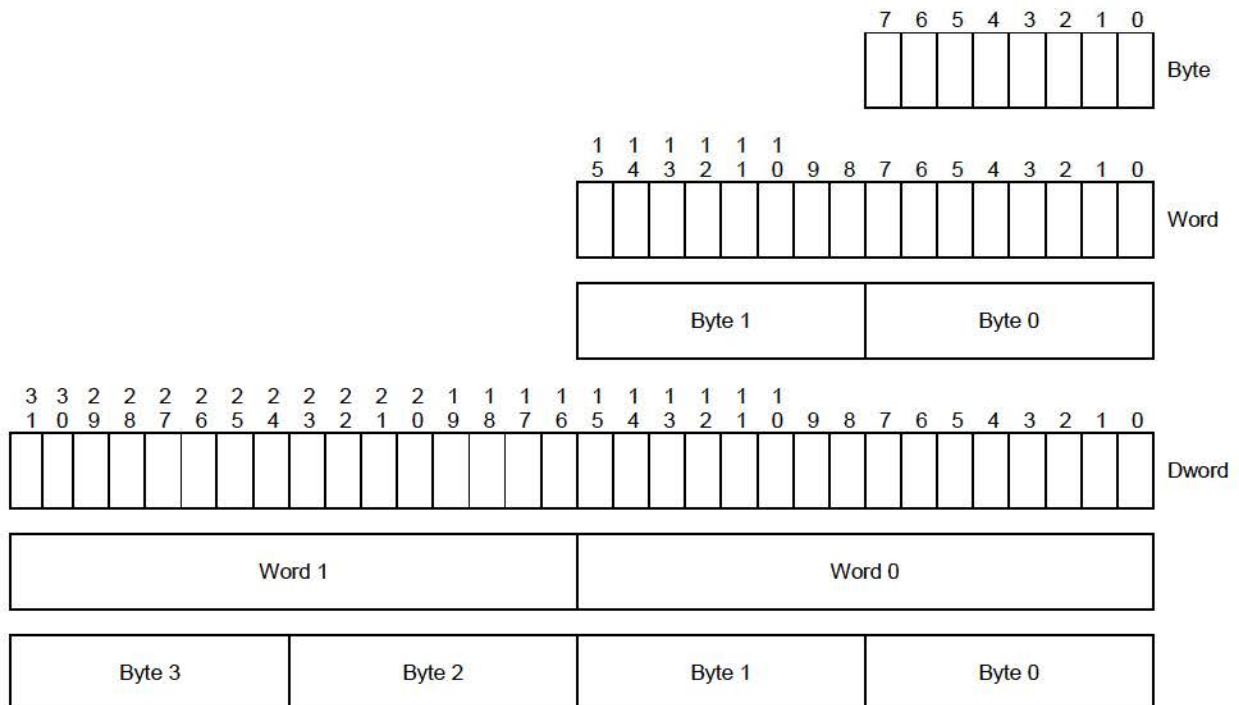


Figure 1 – Byte, word and Dword relationships

5 General overview

Serial ATA is a high-speed serial link replacement for the parallel ATA attachment of mass storage devices. The serial link employed is a high-speed differential layer that utilizes Gigabit technology and 8b/10b encoding.

Figure 2 illustrates how two devices are connected to a parallel ATA host adapter. This method allows up to two devices to be connected to a parallel ATA bus using a Master/Slave communication technique. Each device is connected via a ribbon cable that “daisy chains” the devices.

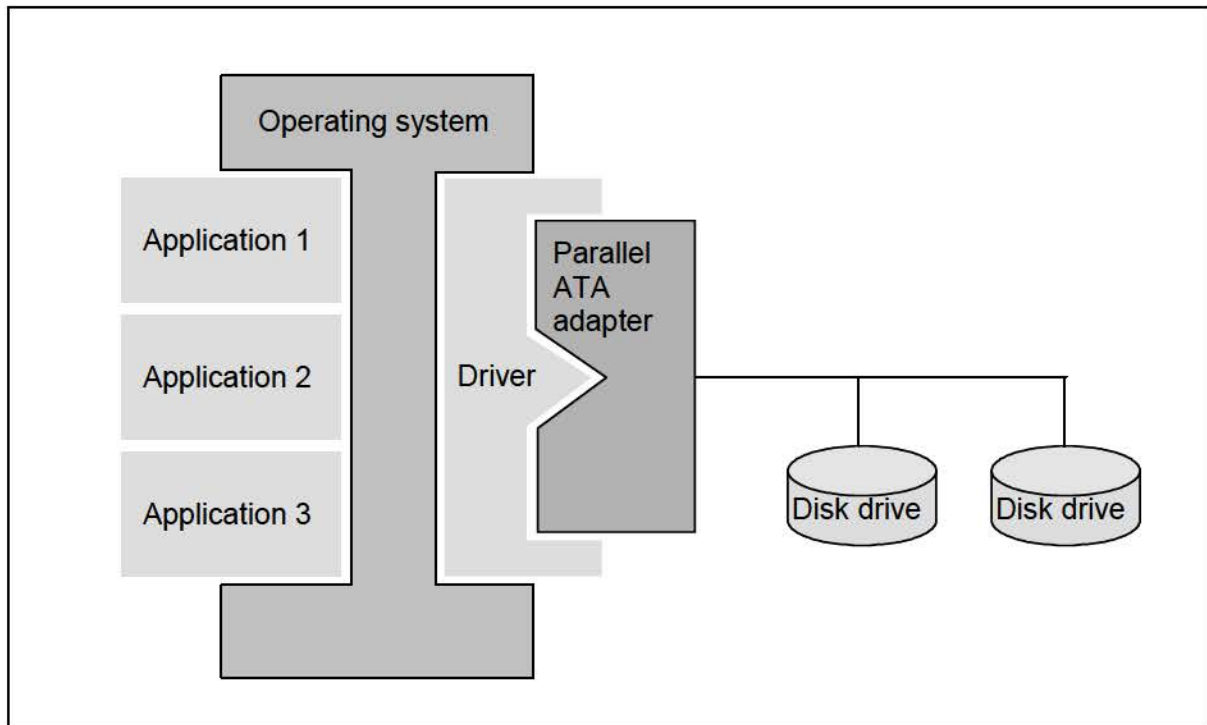


Figure 2 – Parallel ATA device connectivity

Figure 3 shows an example of how the same two devices are connected using a Serial ATA HBA. In this figure the dark grey portion is functionally identical to the dark grey portion of Figure 2. Host software that is only parallel ATA aware accesses the Serial ATA subsystem in exactly the same manner and functions correctly. In this case, however, the software views the two devices as if they were “masters” on two separate ports. The right hand portion of the HBA is of a new design that converts the normal operations of the software into a serial data/control stream. The Serial ATA structure connects each of the two drives with their own respective cables in a point-to-point fashion.

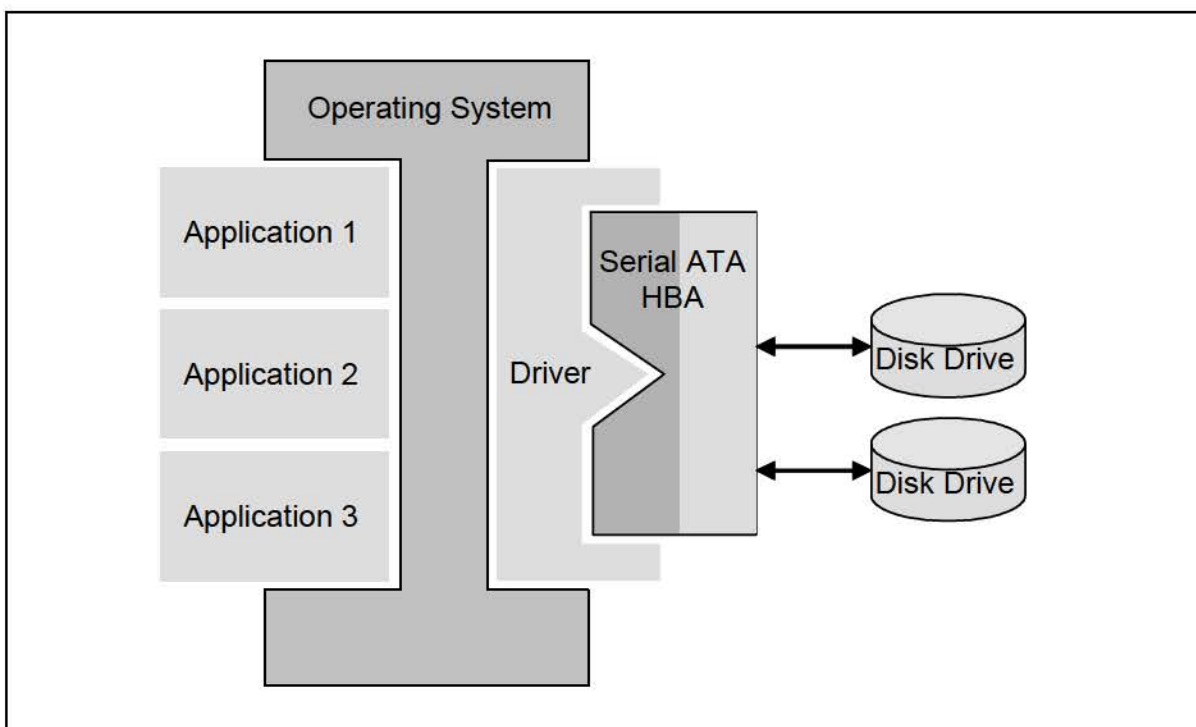


Figure 3 – Serial ATA connectivity

5.1 Architecture

There are four layers in the Serial ATA architecture: Application, Transport, Link, and Phy. The Application layer is responsible for overall ATA command execution, including controlling Command Block Register accesses. The Transport layer is responsible for placing control information and data to be transferred between the host and device in a packet/frame, known as a Frame Information Structure (FIS). The Link layer is responsible for taking data from the constructed frames, encoding or decoding each byte using 8b/10b, and inserting control characters such that the 10-bit stream of data may be decoded correctly. The Phy layer is responsible for transmitting and receiving the encoded information as a serial data stream on the wire.

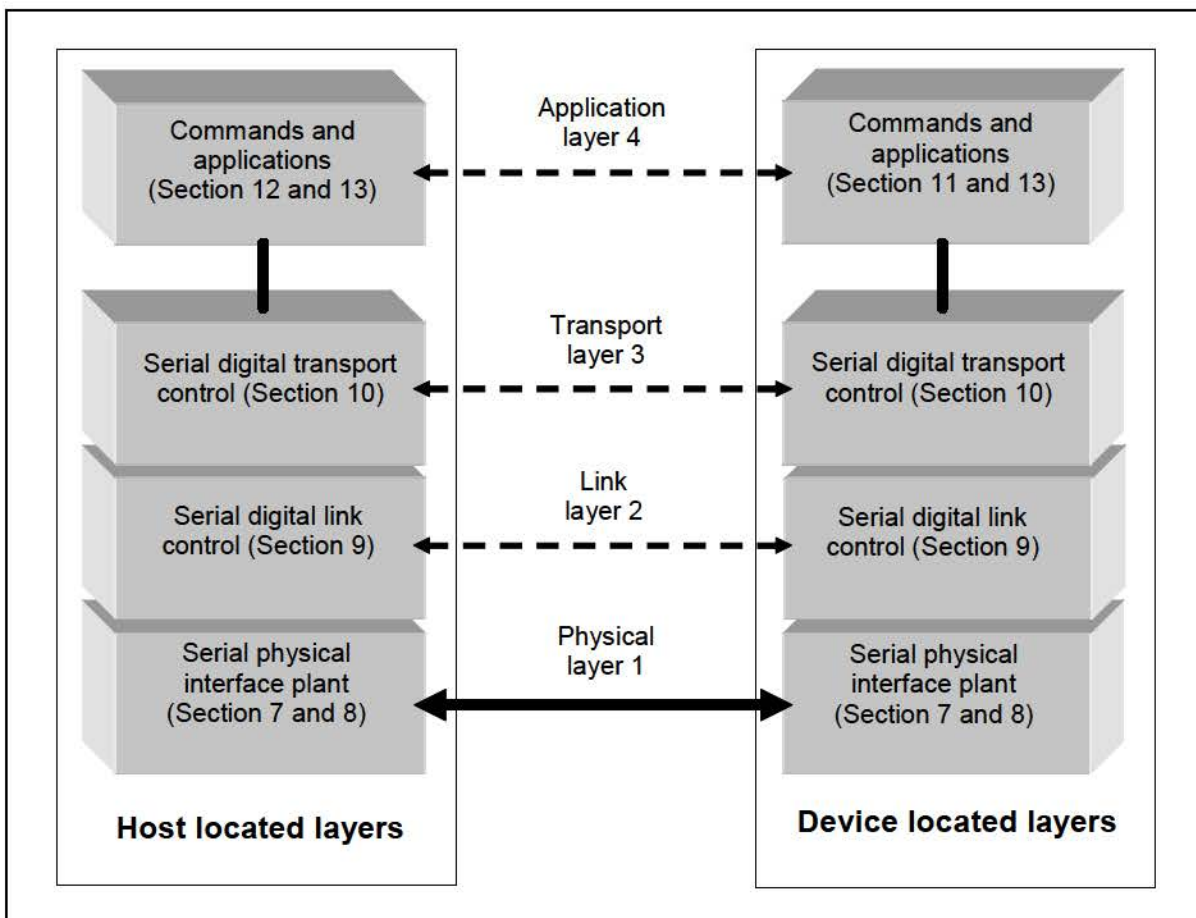


Figure 4 – Communication layers

The host may interact with the Application layer through a register interface that is equivalent to that presented by a traditional parallel ATA host adapter. When using parallel ATA emulation, the host software follows existing ATA/ATAPI-6 standards and conventions when accessing the register interface and follows standard command protocol conventions.

5.2 Usage Models

This section describes some of the potential applications of Serial ATA, including usage models that take advantage of features such as Native Command Queuing, enclosure management, Port Multipliers, and Port Selectors.

5.2.1 Internal 1 meter Cabled Host to Device

In this application, Gen1i or Gen2i electrical specifications compliant points are located at the Serial ATA mated connectors on both the host controller and device. The cable, specified in section 6, operates at both 1.5 Gbps and 3.0 Gbps. The application may comply with the electrical hot plug specification described in section 7.2.5.

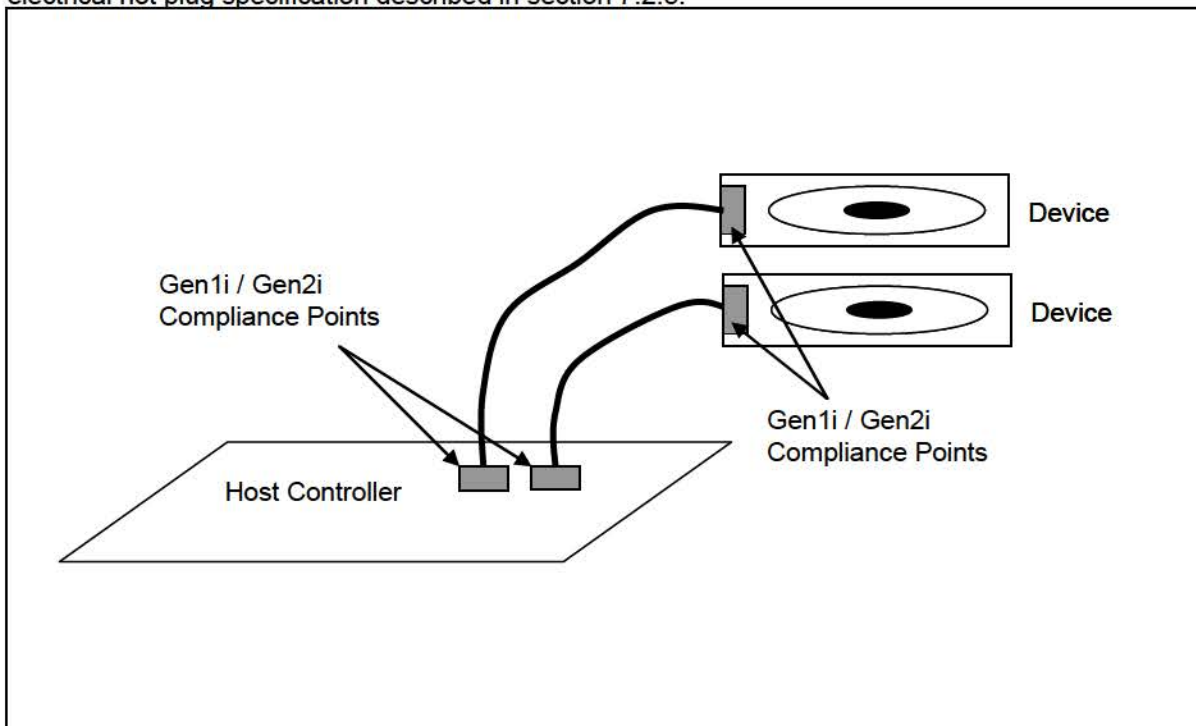


Figure 5 – Internal 1 meter Cabled Host to Device Application

5.2.2 Short Backplane to Device

In this application, Gen1i/2i disk drives within a small disk array are installed into drive canisters which are plugged into a “short” backplane. The host controller connecting to the Backplane shall contain a Host component which exceeds Gen1i/2i transmitter and receiver Differential Swings specifications so that the signals at the host controller connector complies with or exceeds the Gen1m/2m electrical specifications. All other electrical specifications at this compliance point shall meet Gen1i/2i specifications. Compliance points are located at the Serial ATA mated connectors on both the device (Gen1i/2i) and the host controller (Gen1m/2m). The signaling at the host controller connector may exceed the Gen1m/Gen2m transmit maximum providing the Gen1i/Gen2i receiver maximum is not exceeded at the device connector. The application does not contain a cable but routes Serial ATA signals on printed circuit board at 1.5 Gbps and 3.0 Gbps where it is anticipated that the backplanes attenuate signals more than the compliant copper cable described in section 6. The burden falls on the host controller to increase transmit signal swing and accommodate smaller receive swings at the host controller connector. The Gen1i/2i drives are not required to comply with the electrical hot plug specification described in section 7.2.5. However, there are practical application benefits from complying with the hot plug electrical specifications.

NOTE: At Gen2 speeds the designer faces significant challenges regarding signal integrity issues. Validation/feasibility data at Gen2 speeds has not been provided. Making this work is up to the system designer. Using a laboratory load to measured the host controller amplitude or jitter

at the device connector and comparing with Table 24 is not appropriate. Additional margin is required due to the non-ideal impedance match of transmitter and receiver. The receiver is tested to work at these amplitudes and jitter levels when the signal is applied from a lab-sourced signal.

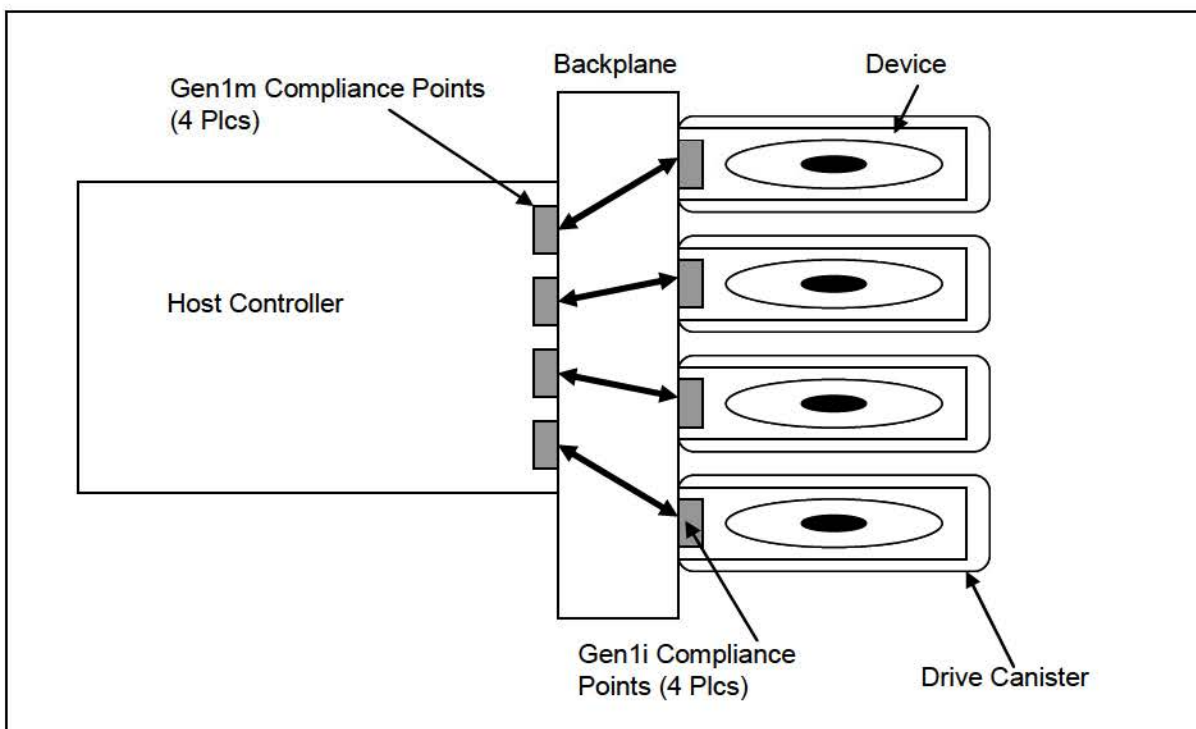


Figure 6 – Short Backplane to Device Application

5.2.3 Long Backplane to Device

In this 1.5 Gbps or 3.0 Gbps application, the length of the backplane is longer than in the previous example so attenuation of signals reduce their amplitude beyond usable levels. Therefore an IC may be placed between the device and the canister's connector to the backplane to convert the disk's Gen1i/Gen2i levels to Gen1x/Gen2x levels. A typical circuit might be a Serial ATA Port Selector. Likewise, the host controller complies with Gen1x/Gen2x levels at the backplane connector to the host controller. This allows reliable transmission of Serial ATA data over backplanes longer than in the Short Backplane Application described above. The burden of determining whether a Backplane Application is Short or Long falls upon the system designer based on the system's attenuation. Compliance points are located at the Serial ATA mated connectors on both the canister (Gen1x/Gen2x) and the host controller (Gen1x/Gen2x). The Gen1x/Gen2x Electrical Specifications require Hot Plug capability so that the disk/canister can be plugged and unplugged without damage.

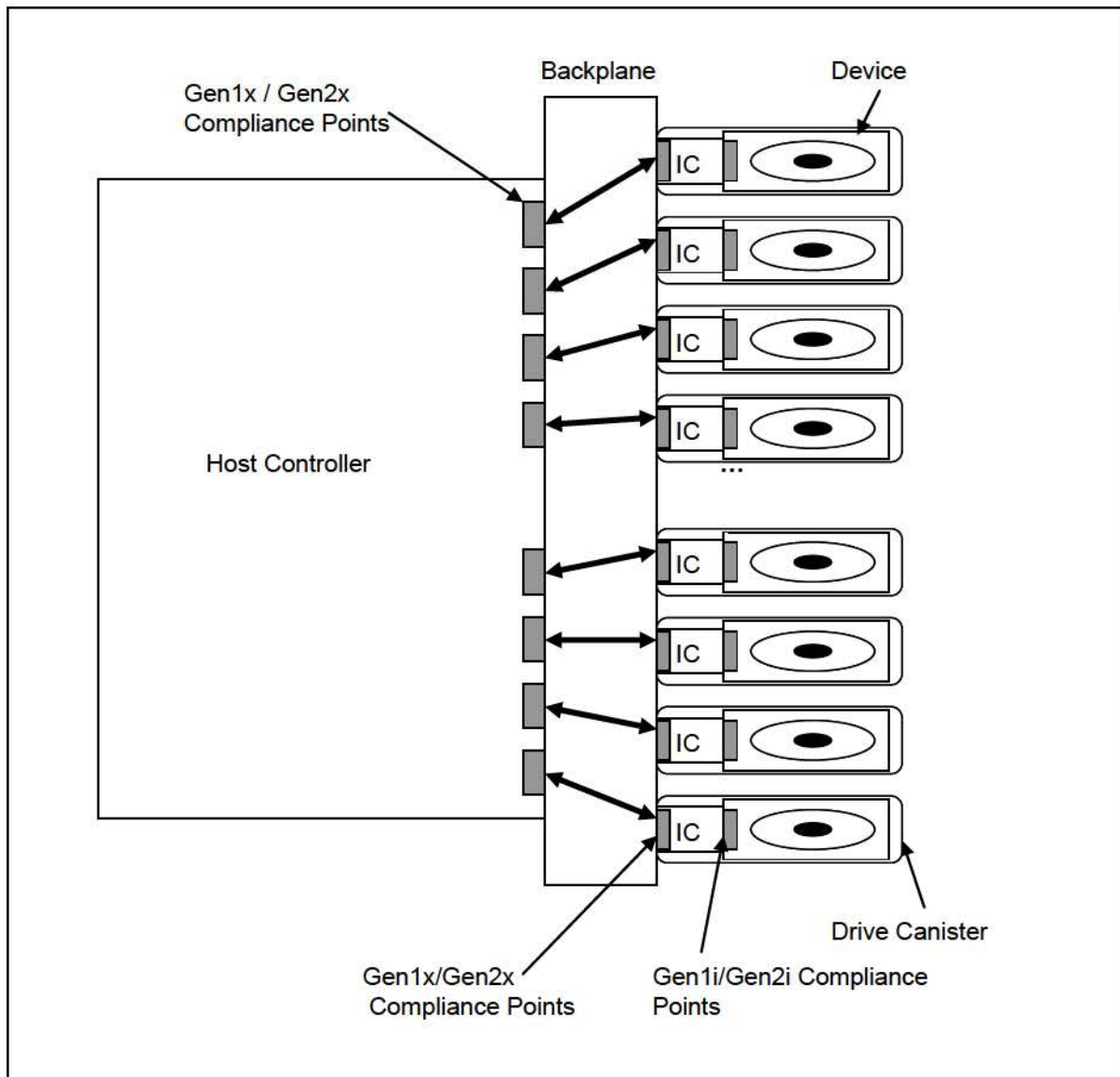


Figure 7 – Long Backplane to Device Application

5.2.4 Internal 4-lane Cabled Disk Arrays

In this application, Gen1i and Gen2i Serial ATA drives are connected to the host controller via the internal 4-lane cable solution. Gen1i and Gen2i specifications shall be met at each end of the 4-lane cable mated interface. The internal 4-lane cable shall connect to the device by one of the following two approaches.

- The host end of the internal 4-lane solution shall mate directly to the host controller board. The device end shall consist of four individual single lane Serial ATA cables for direct mate with up to four individual Serial ATA devices.
- The host end of the internal 4-lane solution shall mate directly to the host controller board. The device end of the internal 4-lane cable shall consist of a single internal 4-lane connector mated to a backplane which provides individual connection points to up to four Serial ATA devices. The backplane design is proprietary.

In the second solution, attenuation of the backplane reduces signal amplitude below specification limits at the compliance points. An IC, such as a Port Selector, shall be placed between the device and the internal 4-lane cable mated interface. Gen1i and Gen2i specifications shall be met at each end of the 4-lane cable mated interface and the device mated connector interface.

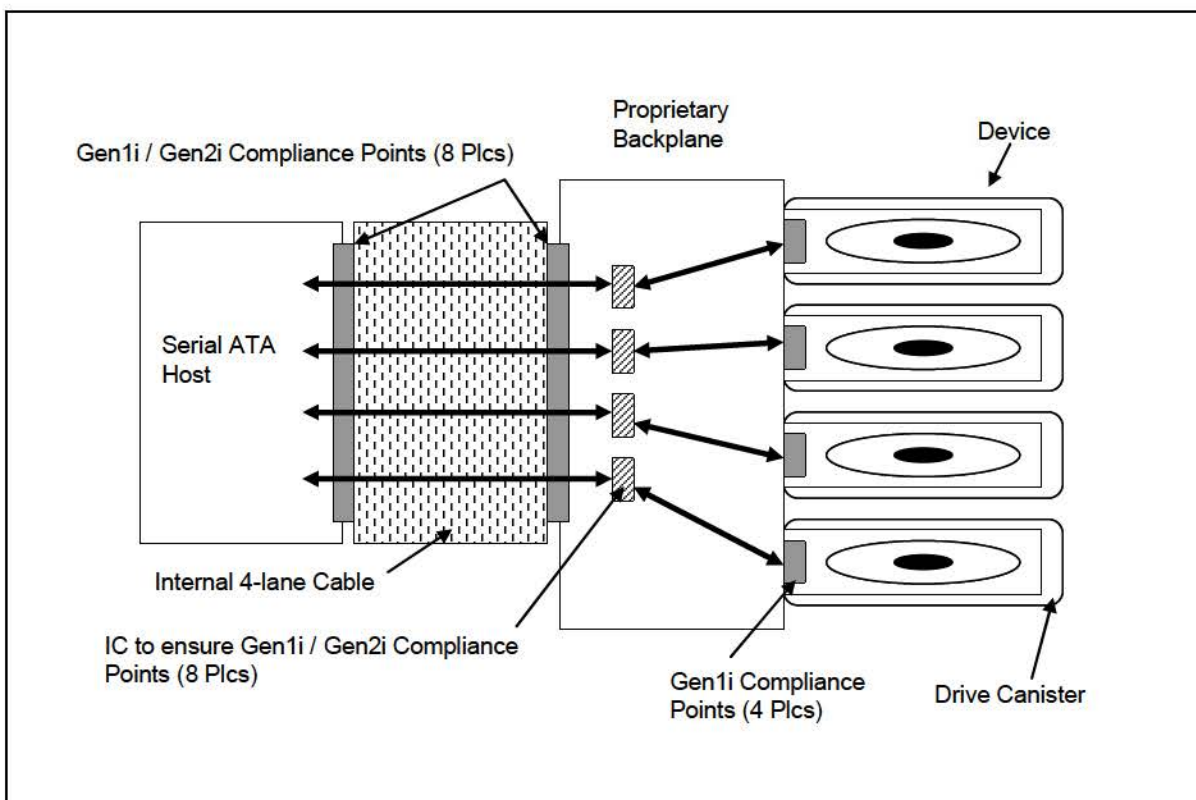


Figure 8 – Internal 4-lane Cabled Disk Array

NOTE: For Gen2i drives the link from the host to the drive (through the IC on the backplane) does not have an electrical specification for the “delivered signal” to the drive. Consider the compliance point for the backplane-drive connector (through the mated pair). If the signal at the compliance point, into a lab load meets all the requirements of Table 20 and Table 22, and the backplane meets all the requirements of Table 21, then interoperability is confirmed.

However, it is anticipated that the additional trace length on the backplane between the IC and the backplane-drive connector makes compliance to these specifications difficult. The burden for ensuring interoperability with all Gen1i/Gen2i drives falls upon the implementer of the system. Essentially the implementer would use simulations and empirical results to confirm that the compliance point at the backplane-drive connector is equivalent to or better than a compliant host and cable combination.

5.2.5 System to System Interconnects – Data Center Applications

This application uses the external Multi Lane cable defined in section 6.2.2.

In this application, Gen1x or Gen2x Electrical Specifications are used to connect two systems together using an external cable. This differs from the application described in section 5.2.6, External Desktop Application, because this application requires higher quality cables/connectors that meet the longer distance requirements of data center storage applications. All external Serial ATA cables function at both 1.5 Gbps and 3.0 Gbps. Use of a cable that operates at 1.5 Gbps

but not at 3.0 Gbps is allowed but this cable assembly shall not be interchangeable with standard Serial ATA cables. For example, if this 1.5 Gbps cable uses Serial ATA specified connectors, the cable shall be keyed to insure that it cannot plug into standard Serial ATA connections. Hot pluggability is a requirement in this application. Compliance points are located at the mated bulkhead connectors of each system.

NOTE: Gen1i, Gen2i and Gen1m specifications are not allowed for these external interfaces.

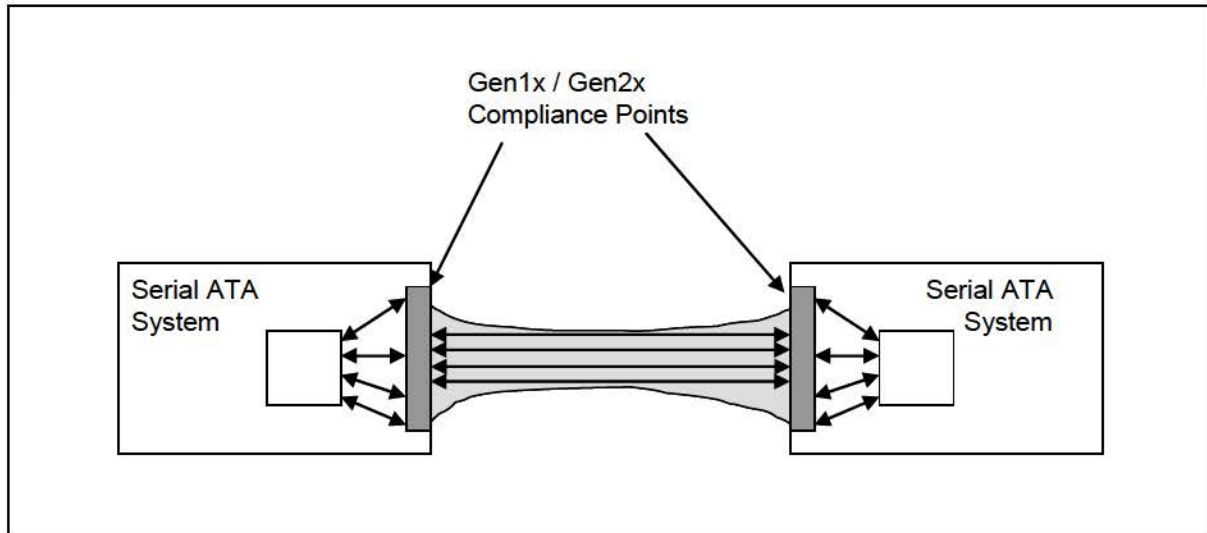


Figure 9 – System to System Interconnects

5.2.6 System to System Interconnects – External Desktop Applications

This application is aimed at external storage applications that require a single lane with approximately two meters or less of cable length. This application uses the external single lane connector system defined in section 6.2.1.

In the example shown below, a device enclosure contains a Gen1i / Gen2i device and an interposer card which contains an integrated circuit unless the device is specifically designed for external connection. Regardless of the implementation, the outside of the device enclosure shall meet Gen1m specifications when operating at Gen1 speeds and Gen2m specifications when operating at Gen2 speeds. A cable/connector has been defined for this application which operates at both Gen1 and Gen2. The host system has an external connector which meets Gen1m specifications when operating at Gen1 speeds and Gen2m specifications when operating at Gen2 speeds.

The entire system shall meet the following requirements:

- The cable/connector shall operate at Gen1 and Gen2 speeds. Systems shall not deploy any cable which cannot operate at Gen2 speeds when the host system and device enclosure both comply with Gen2m electrical specifications.
- The host system and device enclosure shall comply with Gen1m specifications when operating at Gen1 speeds.
- The host system and device enclosure may operate at Gen2 speeds. However, if they operate at Gen2 speeds the host system and device enclosure shall comply with Gen2m specifications when operating at Gen2 speeds and shall also be able to operate at Gen1 speeds using Gen1m electrical specifications.
- The host system and the device enclosure shall comply with the Hot Plug Specifications in this document.
- NOTE: AC Coupling on the transmitters and receivers of the host system and device enclosure is strongly recommended for Gen1m and required for Gen2m.

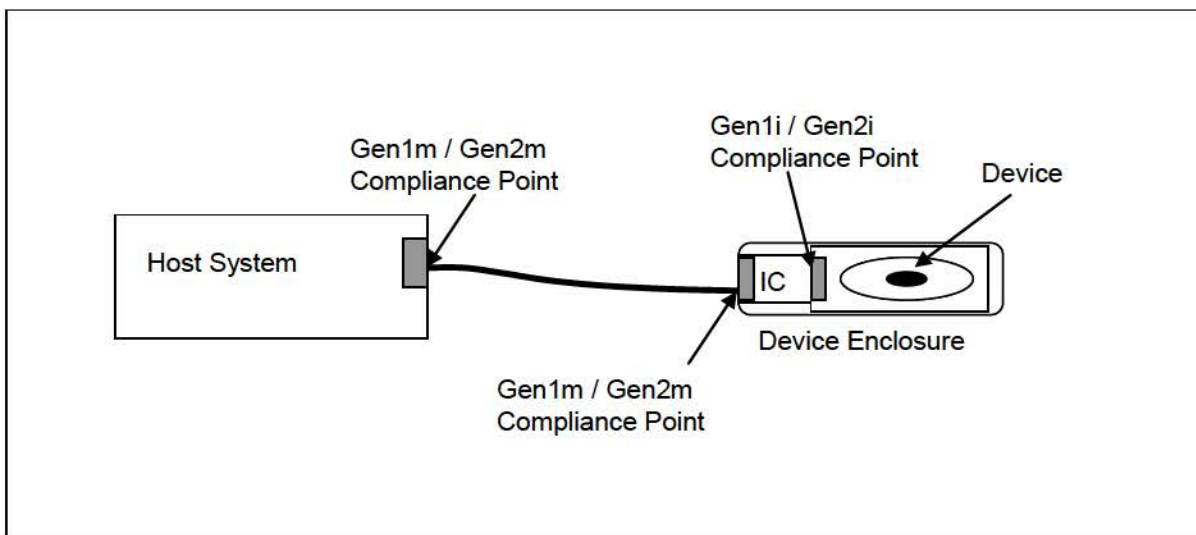


Figure 10 – External Desktop Application

5.2.7 Proprietary Serial ATA Disk Arrays

In this application, Serial ATA drives are connected to a backplane and the links are routed over a combination of internal backplanes or cables as well as an external cable to a Serial ATA system. There are not semiconductors between the drives and the system so the intermediate connectors are not compliance points. Although this application is allowed, the external connectors on the disk array shall not be standard Serial ATA connectors. This is to prevent users from connecting standard external cables between the system and the disk array since they may not function reliably.

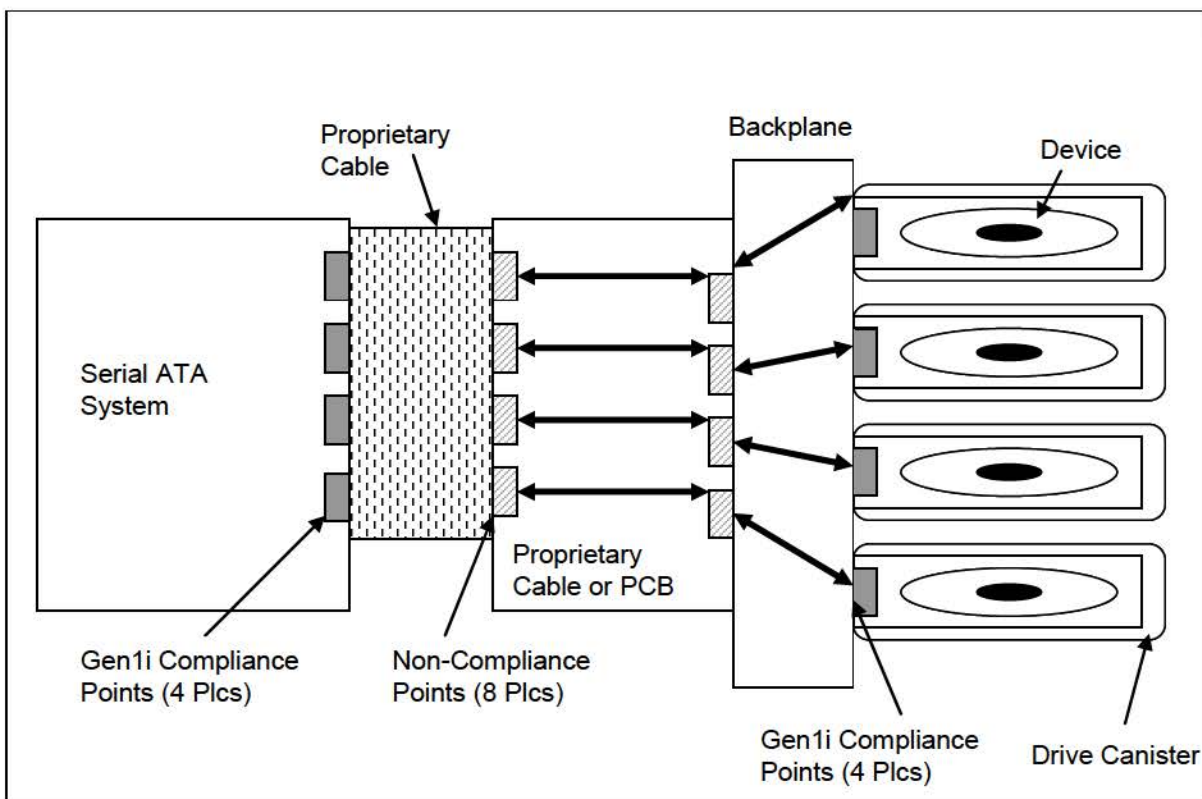


Figure 11 – SATA Disk Arrays

5.2.8 Serial ATA and SAS

The SAS reference is a standard that specifies a SCSI transport protocol over a serial link. The SAS standard borrows heavily from the SATA Phy, Link, and Transport layers. A SAS domain may support attachment to and control of unmodified SATA devices connected directly into the SAS domain using the Serial ATA Tunneled Protocol (STP).

5.2.9 Potential External SATA Incompatibility Issues

WARNING: The functionality of External Desktop and External Data Center cabled applications is not defined by this specification. Consequently, two systems could be connected which may not interoperate even though all the components comply with the electrical specifications defined in this document. External applications are not required to support Port Multipliers or Port Selectors. As a result, a host with an External Data Center connector could be connected to a disk array containing a Port Multiplier and the resulting system may not operate correctly.

5.2.10 Mobile Applications

Applications and compliance points for Serial ATA devices within or connected to mobile computers are not defined in this document. If any proprietary cables/connectors or electrical specifications are developed for this application, the system shall be designed so as to prevent connection with standard SATA components. If standard cables/connectors/electrical interfaces are used within the mobile computer, within the docking bay or to external storage components, these shall comply with the applicable requirements in this specification and interoperate properly with Serial ATA components.

Internal Applications:

It is expected that all internal interfaces comply with the Gen1i and Gen2i specifications. Any mobile computer designer modifying electrical specifications of hosts and devices within the mobile computer is free to do so, however, all proprietary interfaces shall be designed so as to prevent connection with standard SATA components.

Docking Bay Applications:

Proprietary docking bay interfaces shall be designed so as to prevent connection with standard SATA components.

External Applications:

Applications for external Serial ATA interfaces on mobile computers may use either the External Desktop cable/connector (Gen1m at 1.5 Gbps, Gen2m at 3.0 Gbps) or the System-to-System Data Center cable/connector (Gen1x at 1.5 Gbps or Gen2x at 3.0 Gbps). Proprietary solutions shall be designed so as to prevent connection with standard SATA components.

5.2.11 Port Multiplier Example Applications

One possible application of the Port Multiplier is to increase the number of Serial ATA connections in an enclosure that does not have a sufficient number of Serial ATA connections for all of the drives in the enclosure. An example is shown in Figure 12. A Multi Lane cable with two Serial ATA connections is delivered to the enclosure. The enclosure contains eight Serial ATA drives. To create the appropriate number of Serial ATA connections, two 1-to-4 Port Multipliers are used to create eight Serial ATA connections.

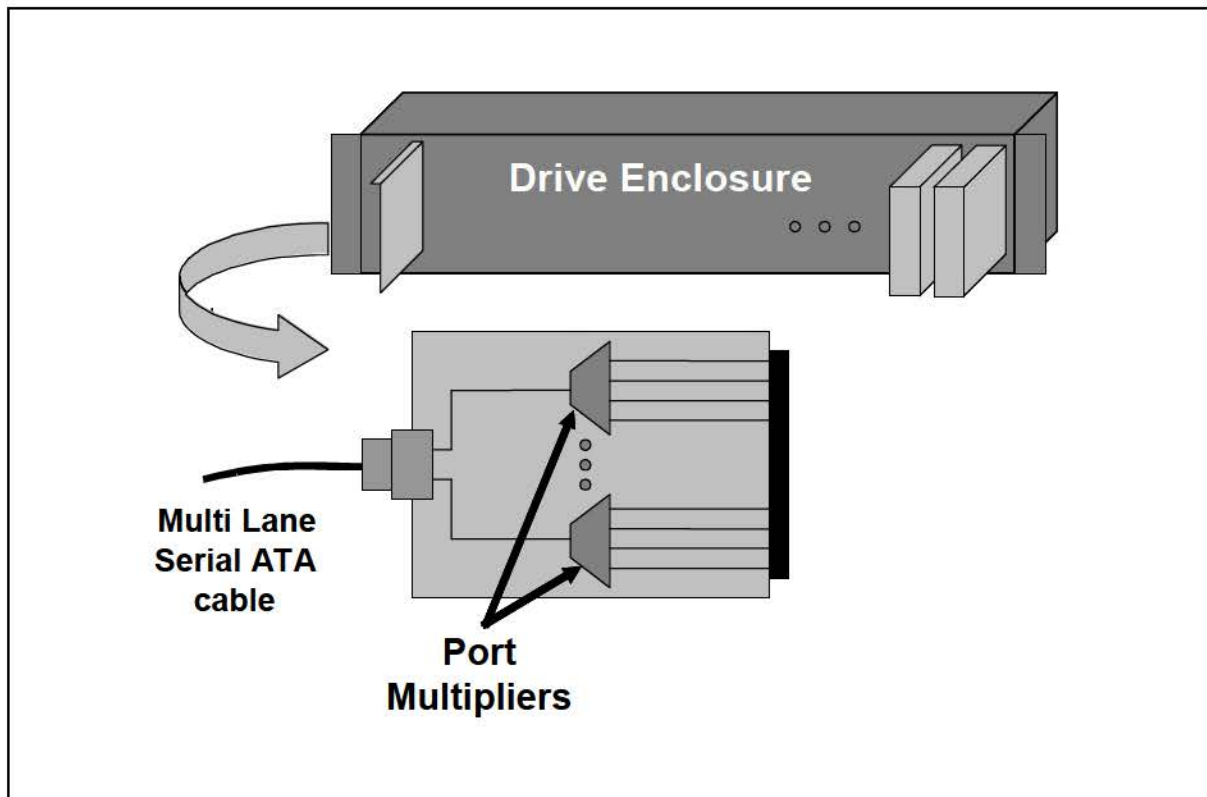


Figure 12 – Enclosure example using Port Multipliers with Serial ATA as the connection within the rack

Another example is shown in Figure 13. Fibre Channel, Infiniband, or Gigabit Ethernet is used as the connection within the rack to the enclosure. Inside the enclosure, a host controller creates two Serial ATA connections from the connection delivered. The enclosure contains eight Serial ATA drives. To create the appropriate number of Serial ATA connections, two 1-to-4 Port Multipliers are used to create eight Serial ATA connections.

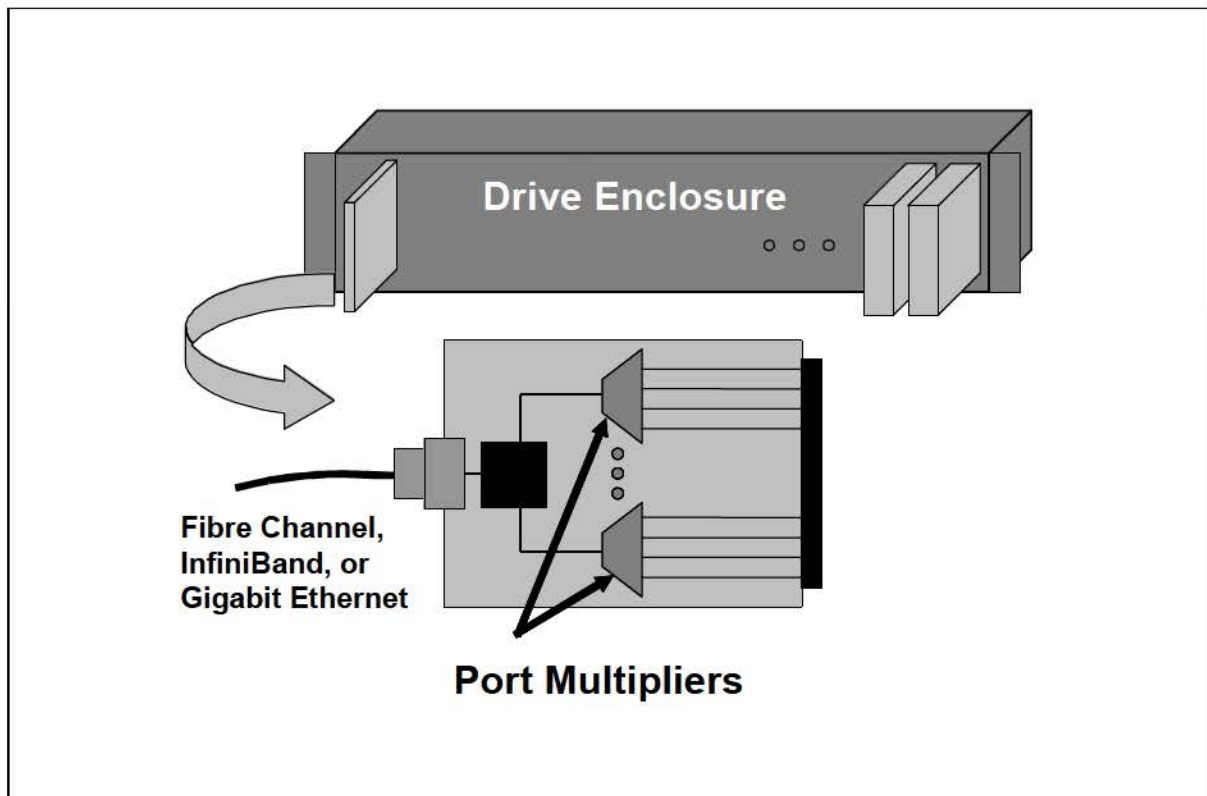


Figure 13 – Enclosure example using Port Multipliers with a different connection within the rack

The Port Multiplier allows host controllers with a modest number of connections to be used in these enclosures and then the connectivity is increased as product requirements dictate.

Another example application is using a Port Multiplier to increase the number of Serial ATA connections in a mobile docking station. The example shown in Figure 14 has a proprietary interface between the laptop and the docking station. The proprietary interface may route a Serial ATA connection from the laptop to the docking station or the docking station may create a Serial ATA connection itself. The docking station routes the Serial ATA connection to a Port Multiplier to create an appropriate number of Serial ATA connections for the number of devices to be attached.

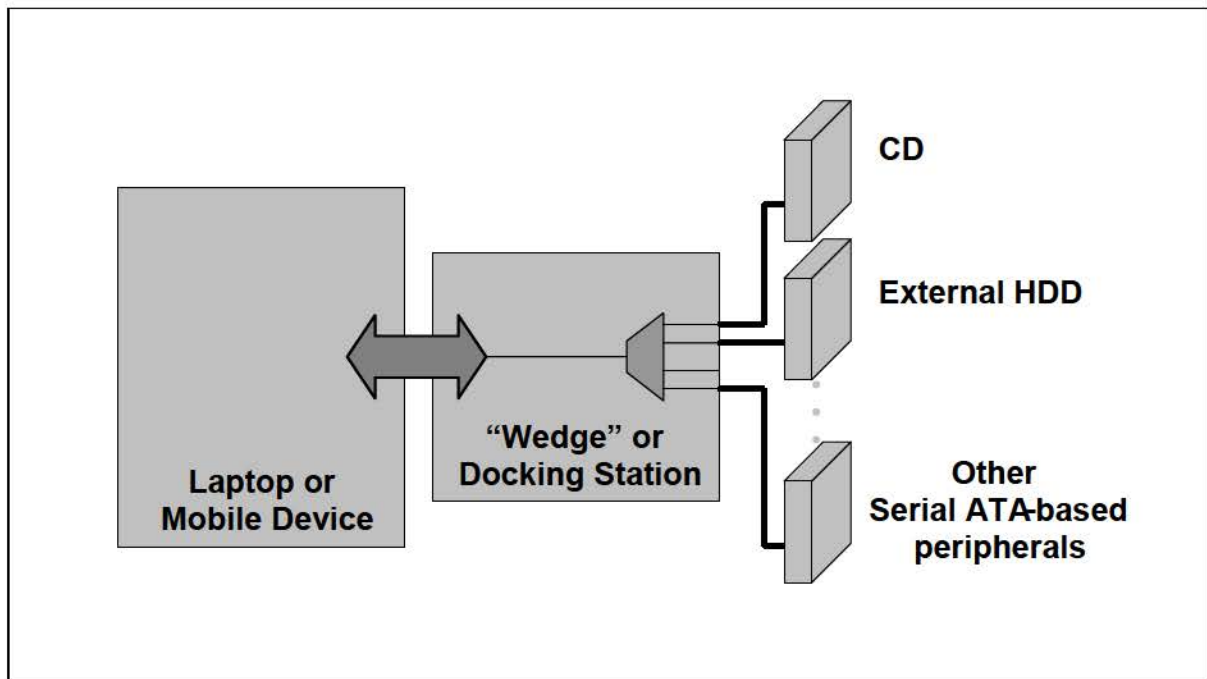


Figure 14 – Mobile docking station example using a Port Multiplier

These are a few examples of possible applications of the Port Multiplier and are not meant to be all encompassing.

6 Cables and connectors

This section defines the connectors and cable assemblies for Serial ATA. It specifies:

- The mating interfaces between the connectors
- The connector location on the Serial ATA device
- The electrical, mechanical and reliability requirements of the connectors and cable assemblies

The mating interfaces of Serial ATA connectors are defined in terms of their front end (i.e. separable) characteristics only. All SATA internal and external connector contact mating areas shall have a gold or gold-compatible finish. Unless otherwise specified, connector back end characteristics including finish, PCB mounting features, and cable termination features are not defined.

6.1 Internal cables and connectors

6.1.1 Internal Single Lane Description

A Serial ATA device may be either directly connected to a host or connected to a host through a cable.

For direct connection, the device plug connector, shown as (a) and (b) in Figure 15, is inserted directly into a backplane connector, illustrated as (g) in Figure 15. The device plug connector and the backplane connector incorporate features that enable the direct connection to be hot pluggable and blind mateable.

For connection via cable, the device signal plug connector, shown as (a) in Figure 15, mates with the signal cable receptacle connector on one end of the cable, illustrated as (c) in Figure 15. The signal cable receptacle connector on the other end of the cable is inserted into a host signal plug connector, shown as (f) in Figure 15. The signal cable wire consists of two twinax sections in a common outer sheath.

Besides the signal cable, there is also a separate power cable for the cabled connection. A Serial ATA power cable includes a power cable receptacle connector, shown as (d) in Figure 15, on one end and may be directly connected to the host power supply on the other end or may include a power cable receptacle on the other end. The power cable receptacle connector on one end of the power cable mates with the device power plug connector, shown as (b) in Figure 15. The other end of the power cable is attached to the host as necessary.

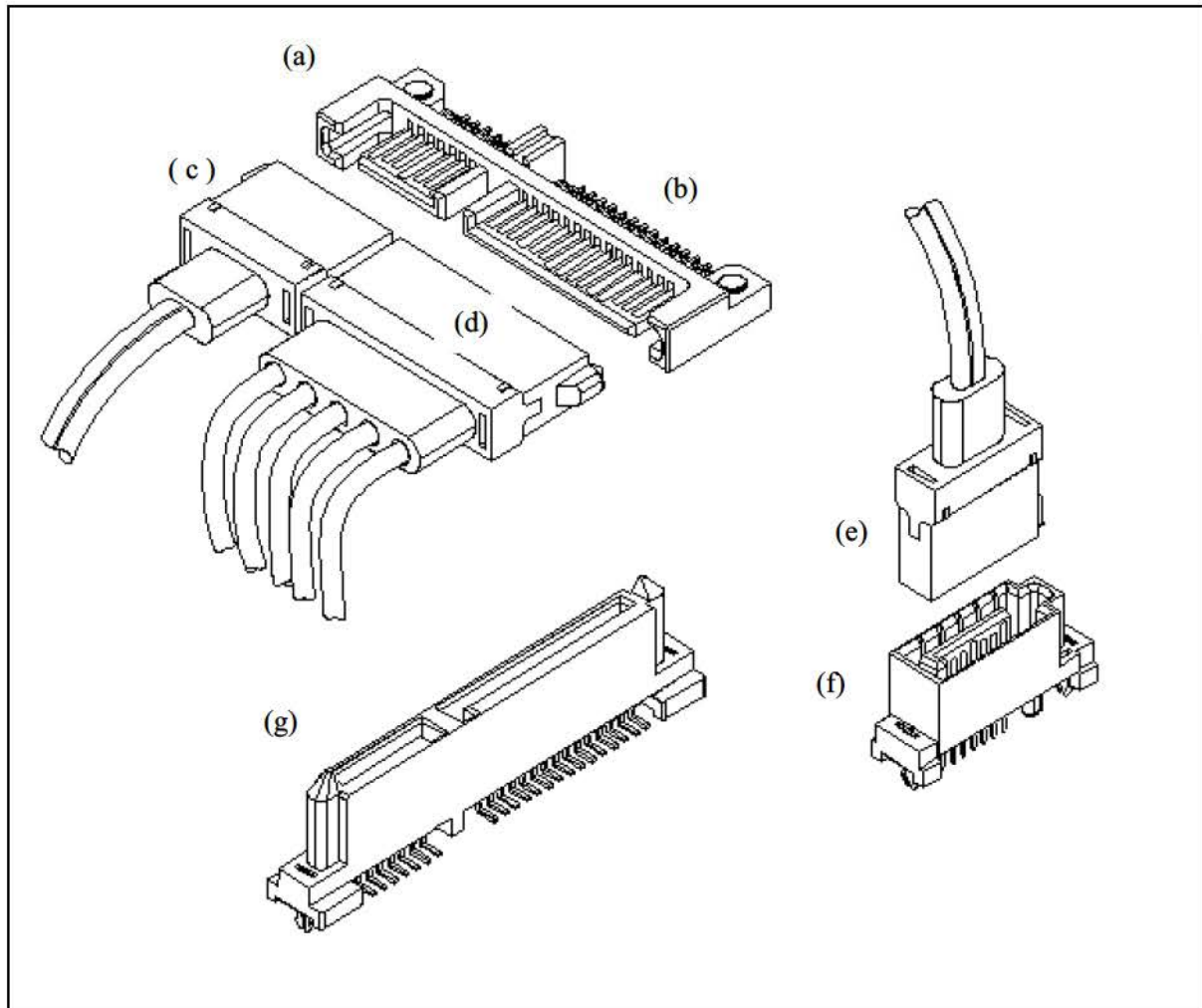


Figure 15 – Serial ATA connector examples

Illustrated above: (a) device signal plug segment or connector; (b) device power plug segment or connector; (c) signal cable receptacle connector, to be mated with (a); (d) power cable receptacle connector, to be mated with (b); (e) signal cable receptacle connector, to be mated with (f), the host signal plug connector; (g) backplane connector mating directly with device plug connector (a) & (b).

Figure 16 shows a direct cable / connector connection and highlights the signal path of the differential TX and RX pairs.

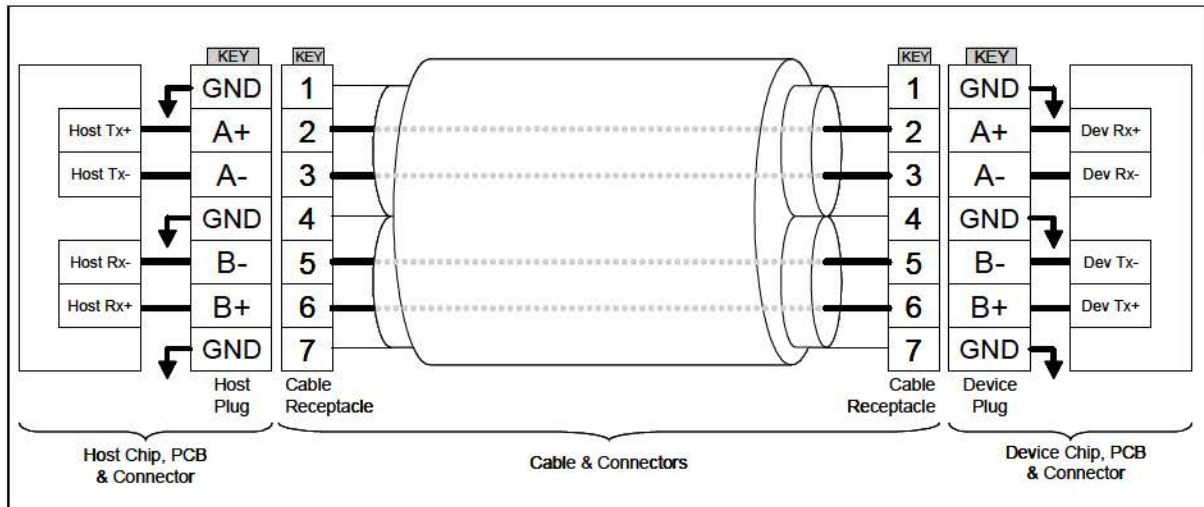


Figure 16 – SATA Cable / Connector Connection Diagram

The connector on the left represents the Host with TX/RX differential pairs connected to a cable. The connector on the right shows the Device with TX/RX differential pairs also connected to the cable. Notice also the ground path connecting the shielding of the cable to the Cable Receptacle.

Figure 17 shows the connection between host and device as a direct connection. It is similar to the cable/connector connection with the exception of the cable.

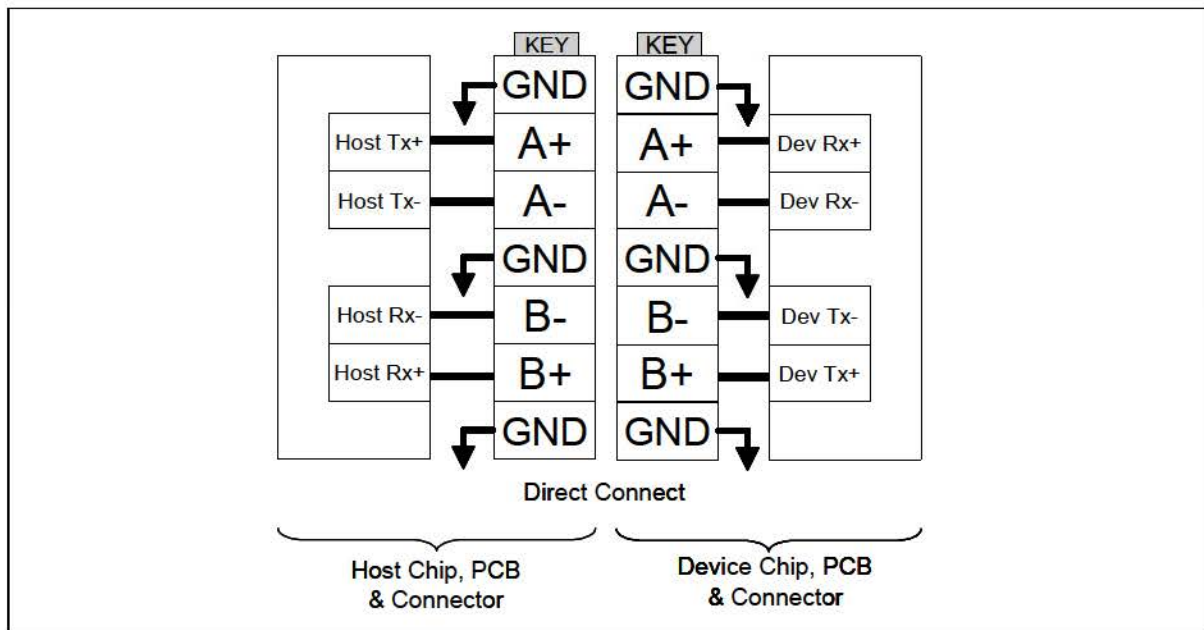


Figure 17 – SATA Host / Device Connection Diagram

In both cases the connection of the TX differential signal pair on the host side to the RX differential signal pair on the device side. A similar connection of the host RX pair to the device TX pair is also shown.

6.1.2 Connector locations

The device connector location is defined to facilitate blind mating.

Figure 18 and Figure 19 define the connector location on 5.25" devices. Optical devices shall locate the connector as indicated in the optical device connector location. Non-optical devices should locate the connector as indicated in the optical device connector location but may locate the connector as indicated in the non-optical device alternate connector location. The Serial ATA connector is nominally flush to the end of the device factor.

Figure 20 defines the connector location on side mounted 3.5" devices. Figure 21 defines the connector location on bottom mounted 3.5" devices. Refer to EIA-740 and SFF-8301 for 3.5" device form factor specifications. The Serial ATA connector is nominally flush to the end of the device factor.

Figure 22 defines the connector location on side mounted 2.5" devices. Figure 23 defines the connector location on bottom mounted 2.5" devices. Refer to EIA-720 and SFF-8201 for 2.5" device form factor specifications. The Serial ATA connector nominally protrudes 0.3 mm from the end of the device factor.

Figure 24 defines the Serial ATA connector location on side mounted 1.8" devices. Figure 25 defines the Serial ATA connector location on bottom mounted 1.8" devices. Refer to SFF-8111 for 1.8" device form factor specifications. The Serial ATA connector nominally protrudes 0.3 mm from the end of the device factor.

To ensure mating of devices to backplanes with proper mechanical and electrical interface and without physical conflict, Figure 37 illustrates the fully mated condition of the device to a nominally

flush backplane receptacle and Figure 26 defines the keep out zones for devices of all form factors. The application shall ensure that these areas do not contain any materials or construction that prevents the fully mated condition.

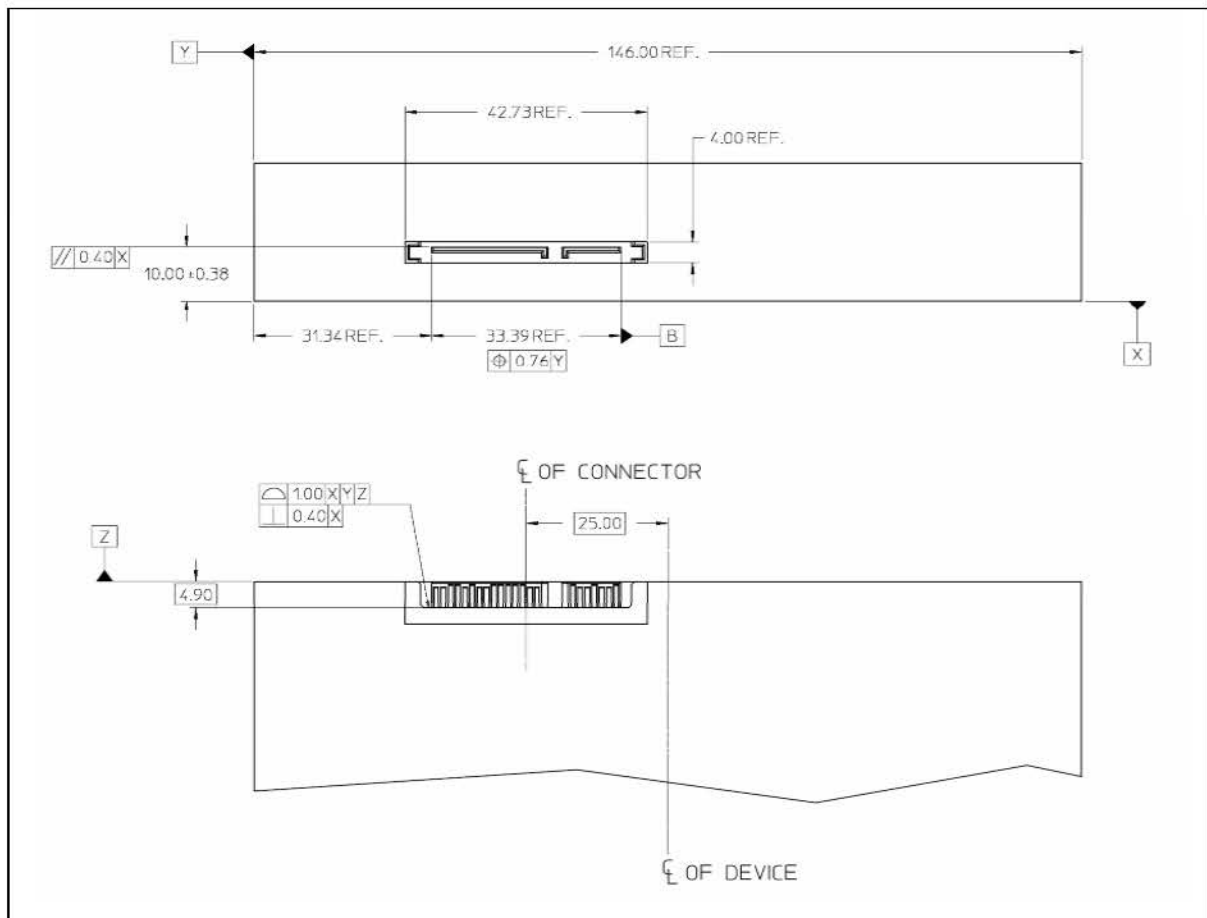


Figure 18 – Optical Device Plug Connector Location on 5.25" form factor

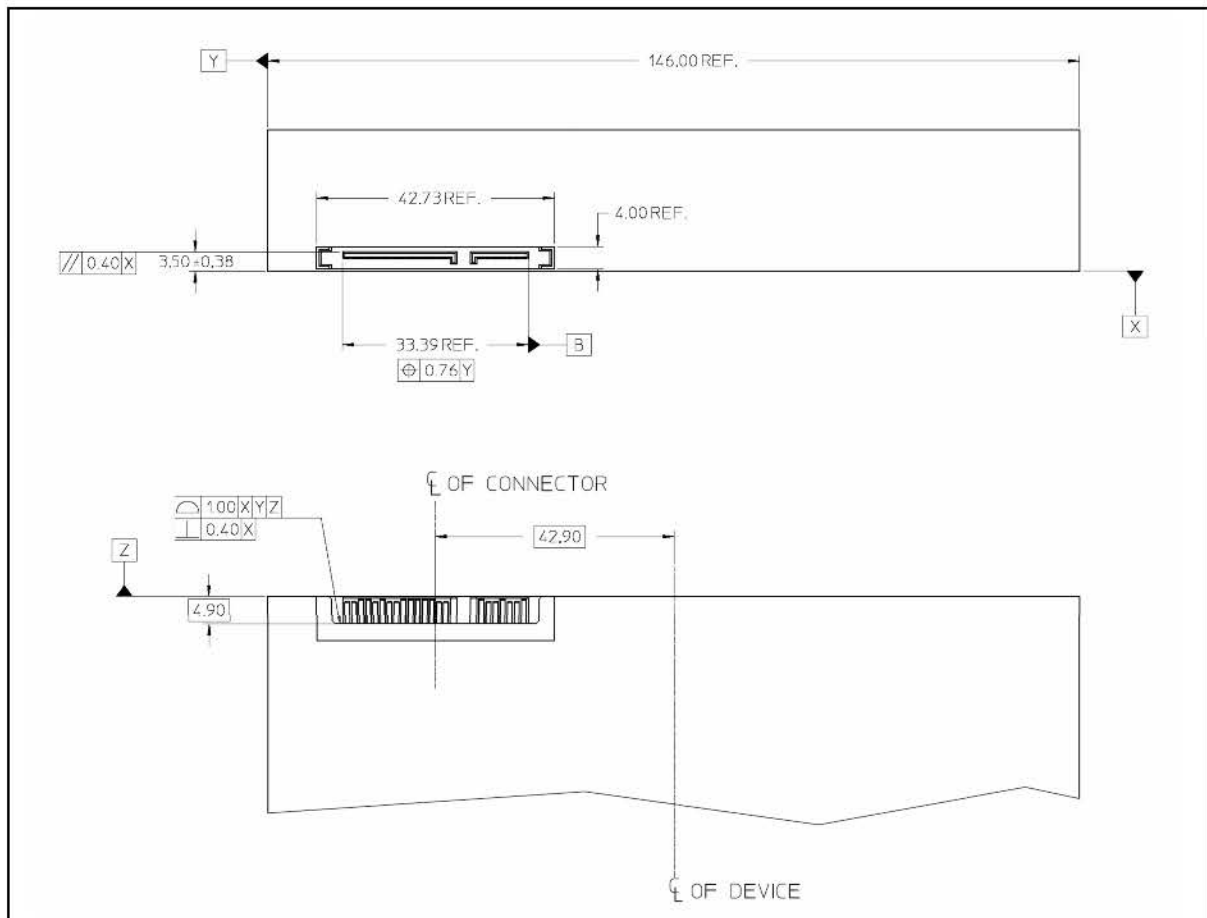


Figure 19 – Non-Optical Alternate Device Plug Connector Location on 5.25" form factor

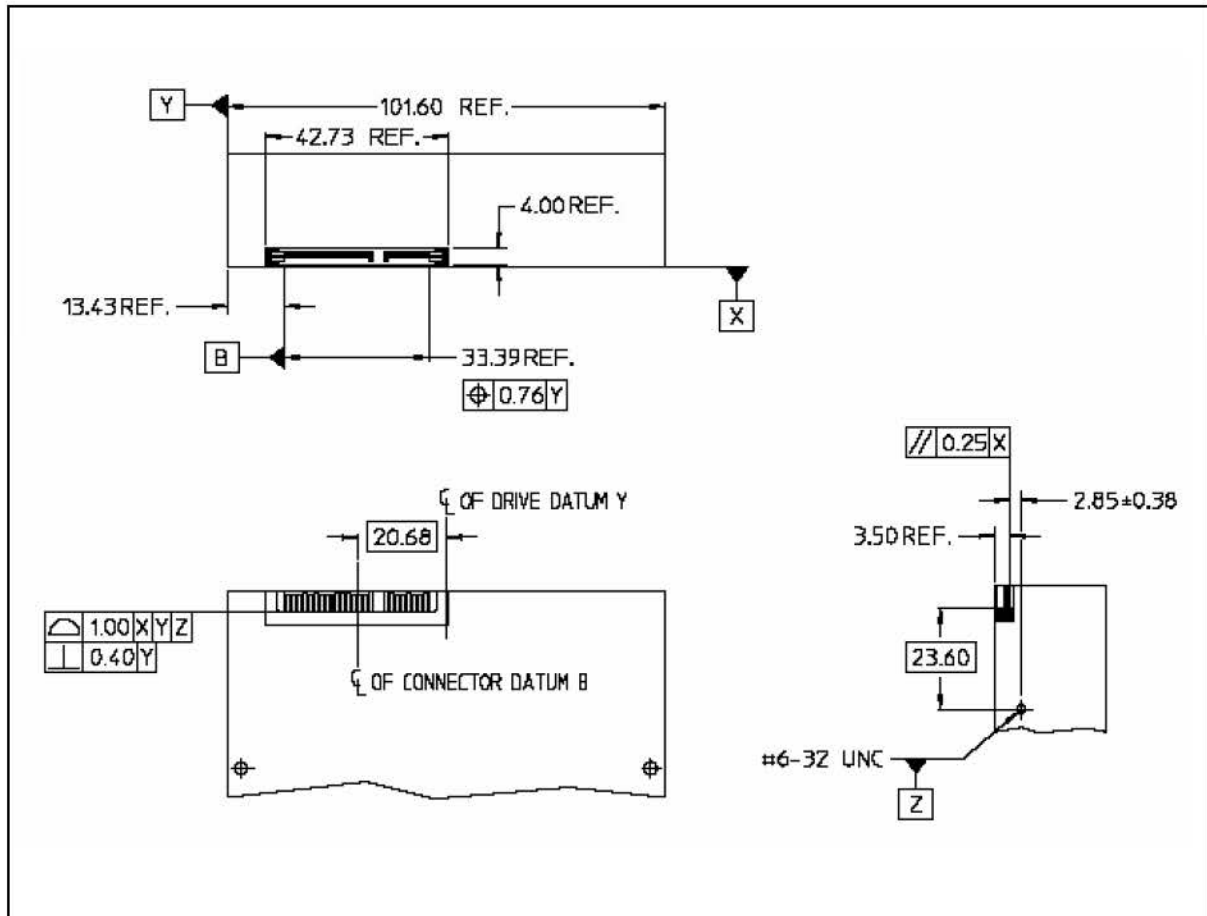


Figure 20 – Device Plug Connector Location on 3.5" Side Mounted Device

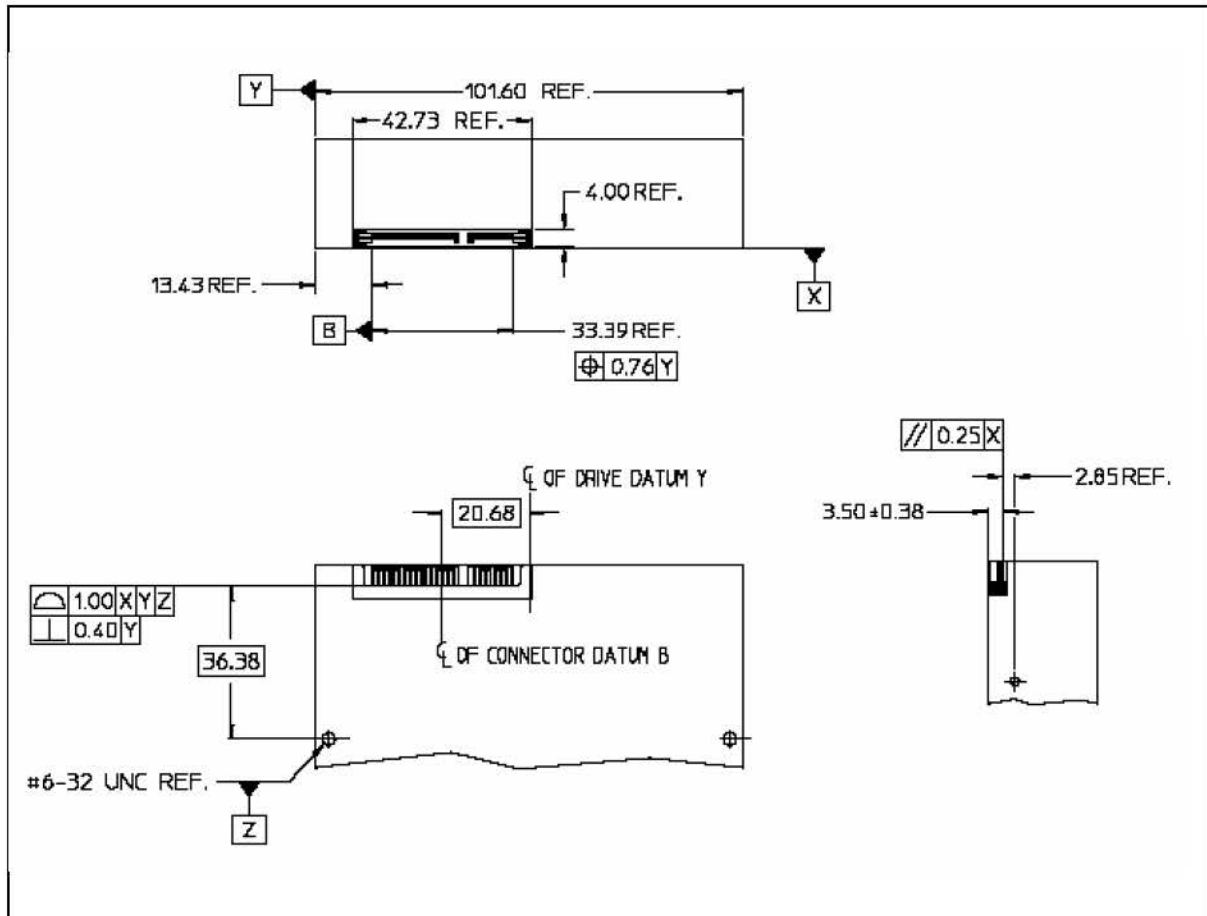


Figure 21 – Device Plug Connector Location on 3.5" Bottom Mounted Device

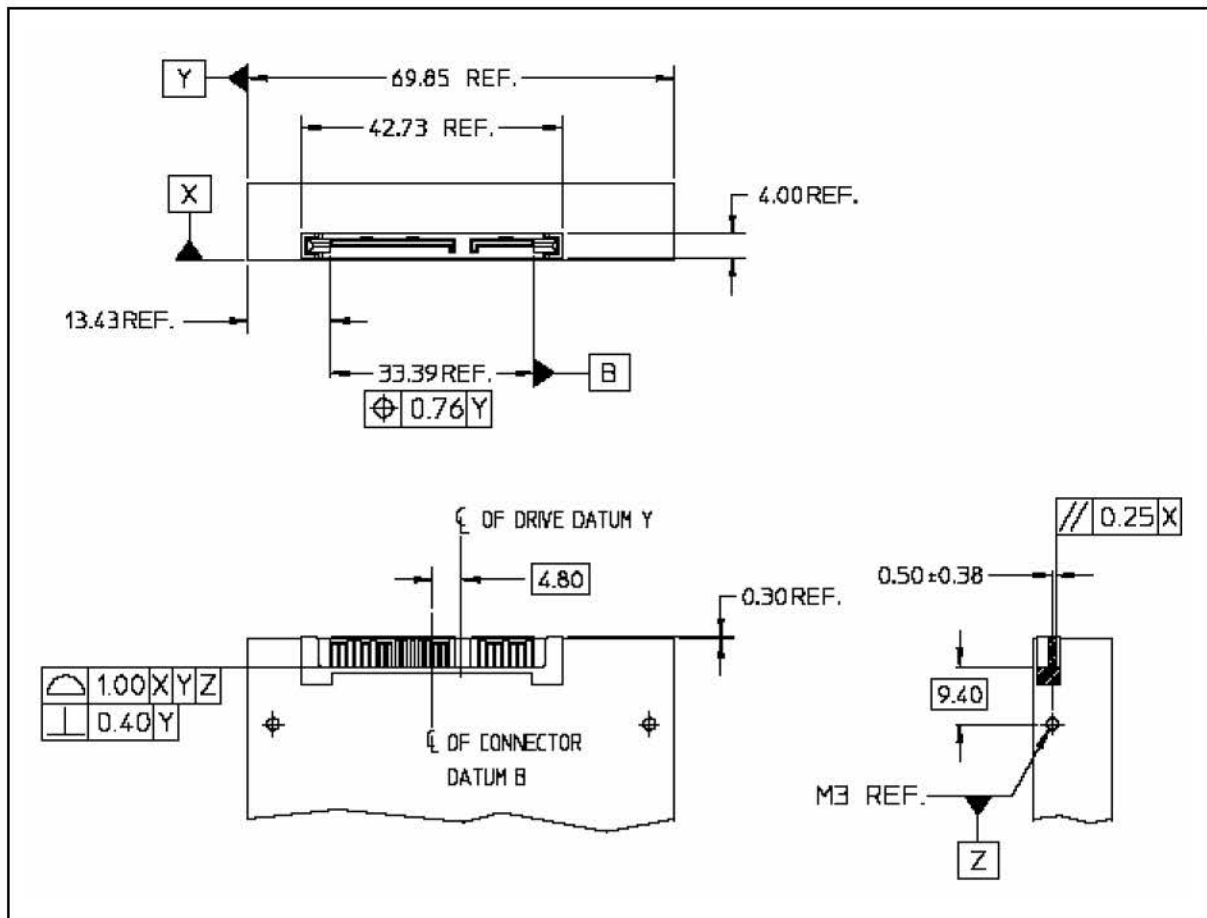


Figure 22 – Device Plug Connector Location on 2.5" Side Mounted Device

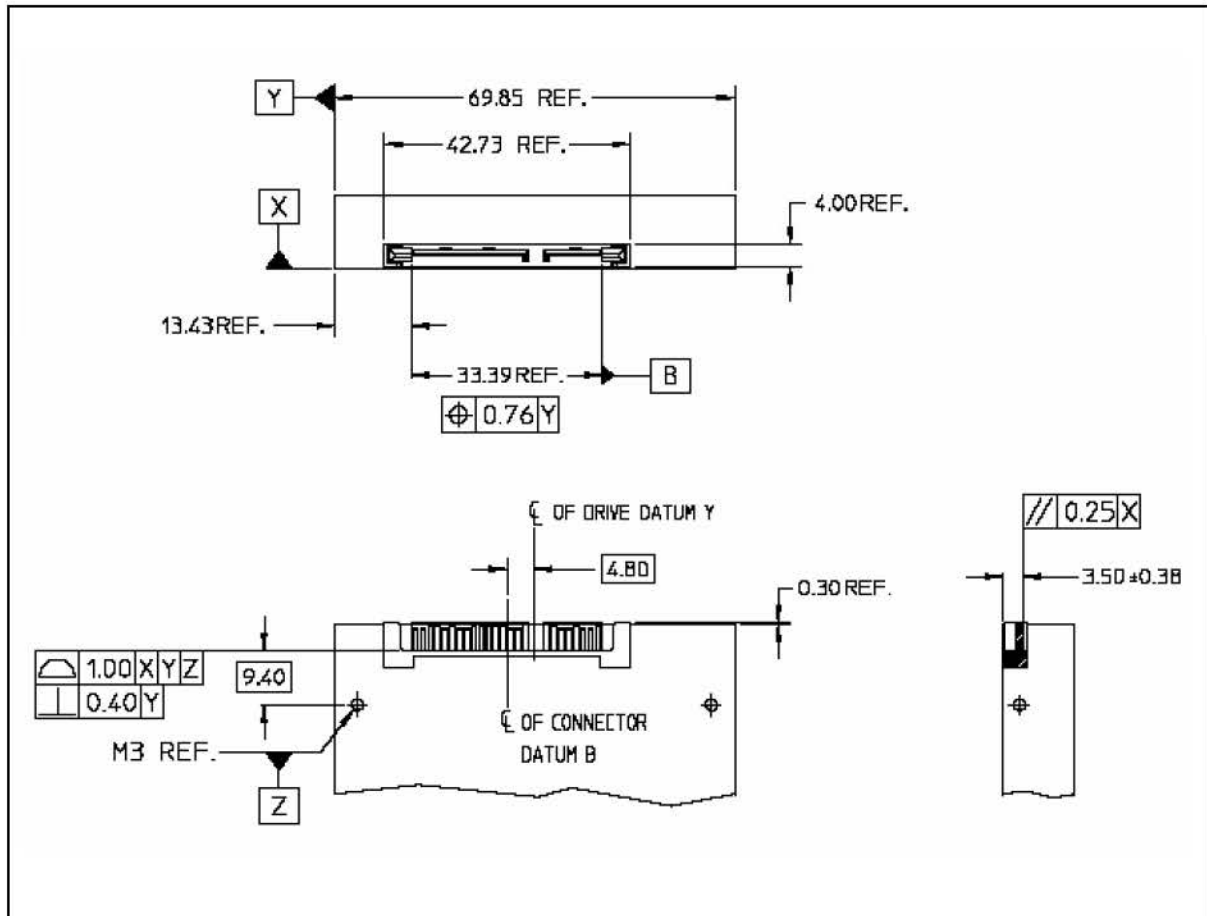


Figure 23 – Device Plug Connector Location on 2.5" Bottom Mounted Device

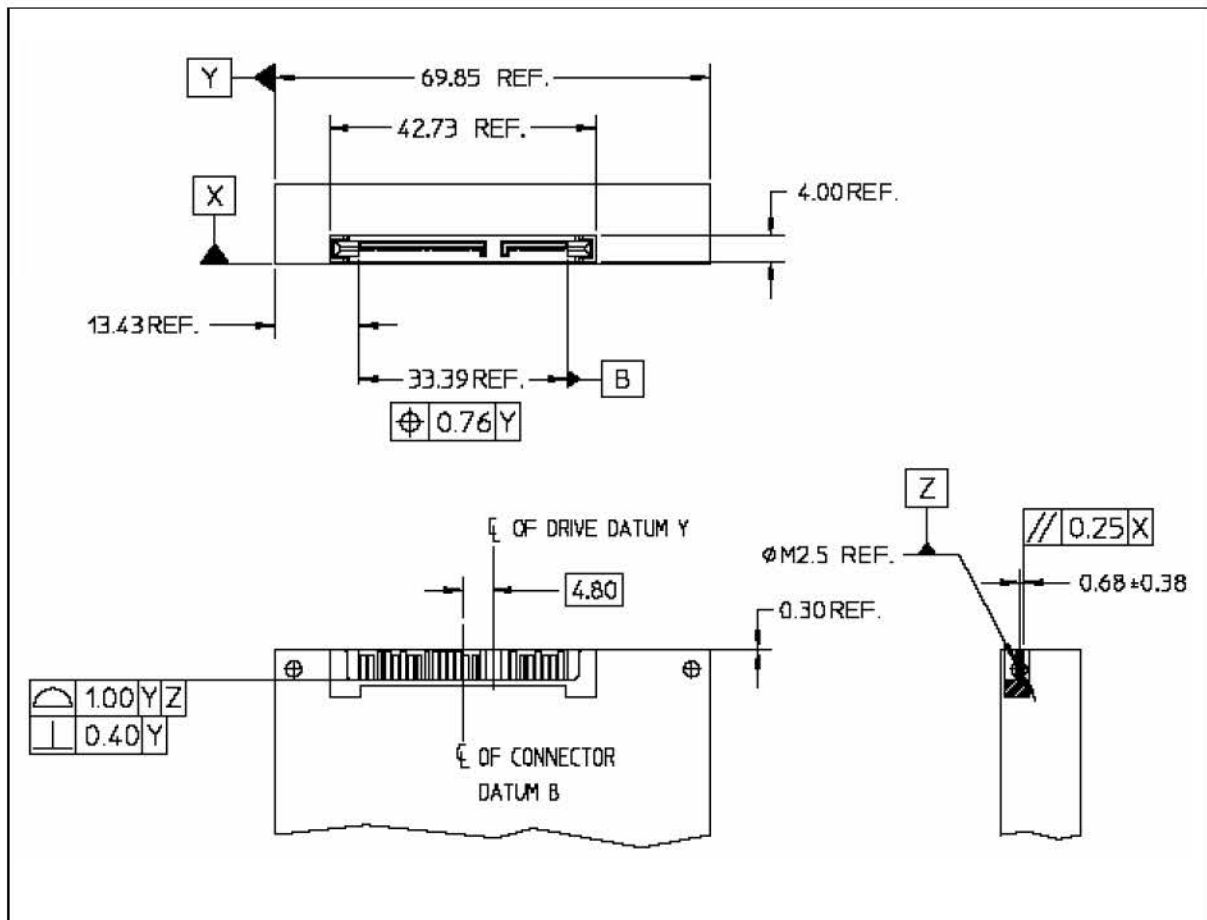


Figure 24 – Device Plug Connector Location on 1.8" Side Mounted Device

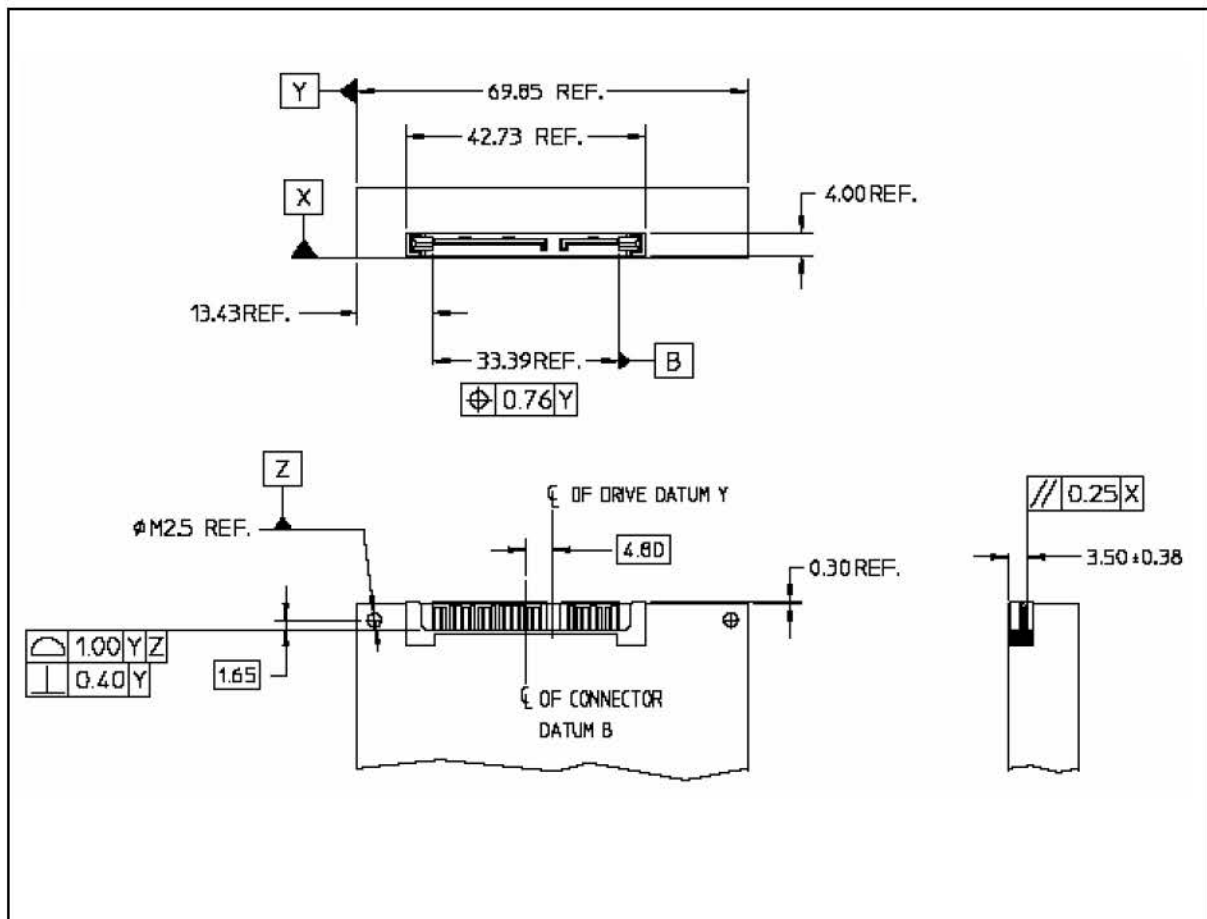


Figure 25 – Device Plug Connector Location on 1.8" Bottom Mounted Device

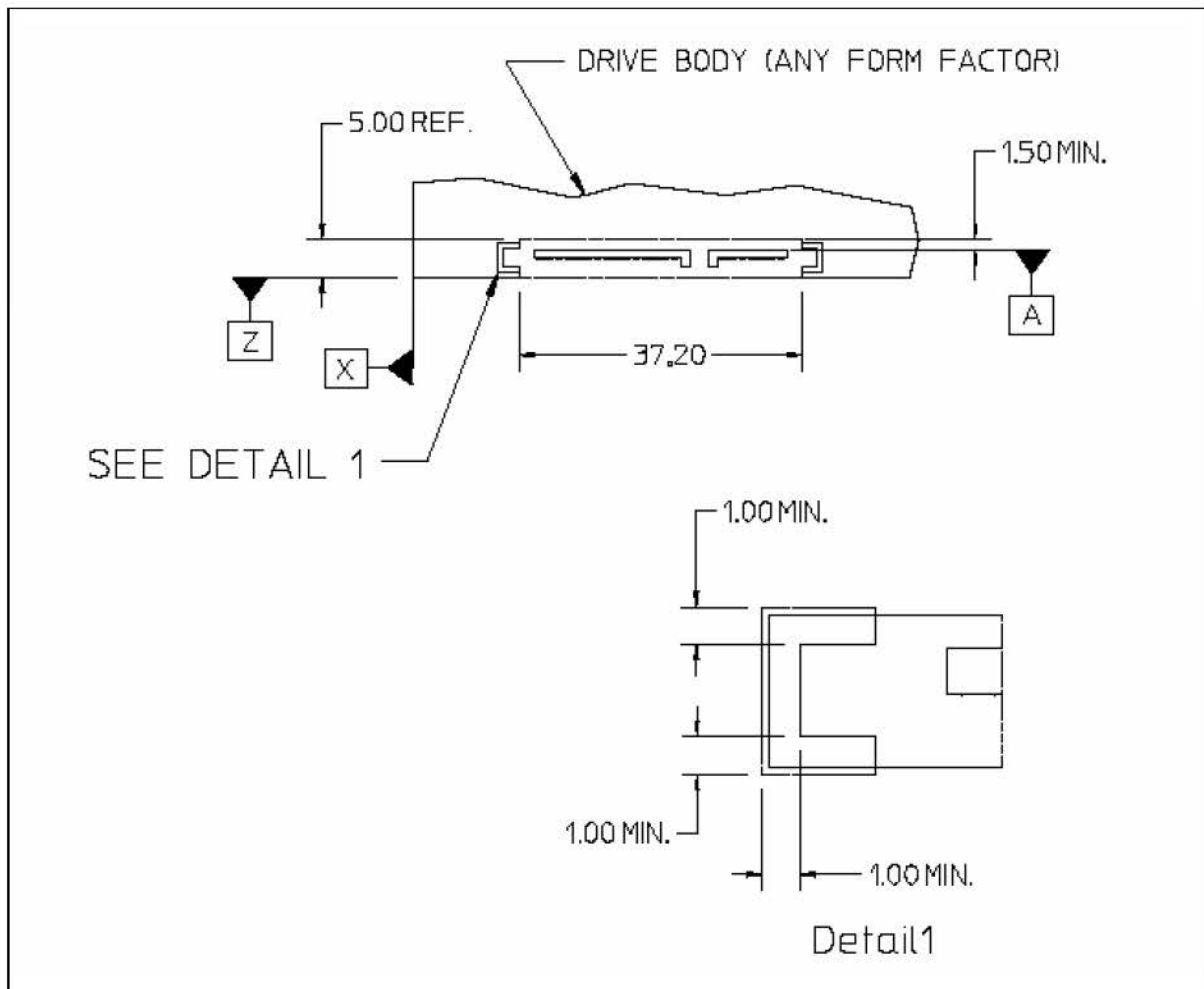


Figure 26 – Device Plug Connector Keep Out Zones

Notes:

1. The 1.50 keepout area above Datum A extends into the form factor to the connector Datum C in Figure 27.
2. The 1.00 keepout area shown in Detail 1 applies to both ends of the connector and extends from the connector housing outward to the outermost point of the form factor.

6.1.3 Mating interfaces

6.1.3.1 Device plug connector

Figure 27 and Figure 28 show the interface dimensions for the device plug connector with both signal and power segments. The device plug includes optional features to allow use of latching cables, fillets, and additional material to improve connector robustness. Table 2 defines the pin definitions and contact mating sequence for hot plug. These optional features should be included in all plug designs.

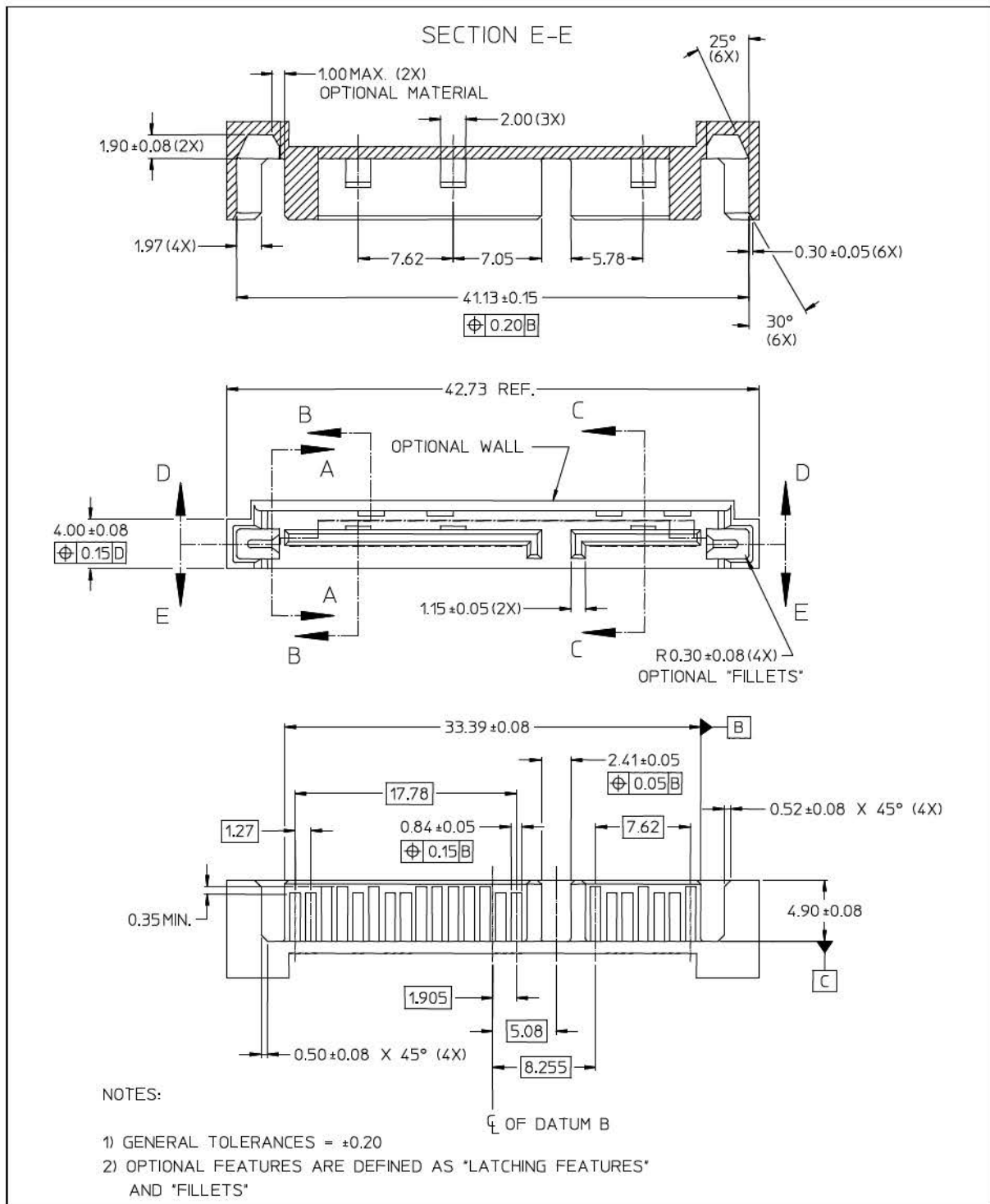


Figure 27 – Device Plug Connector

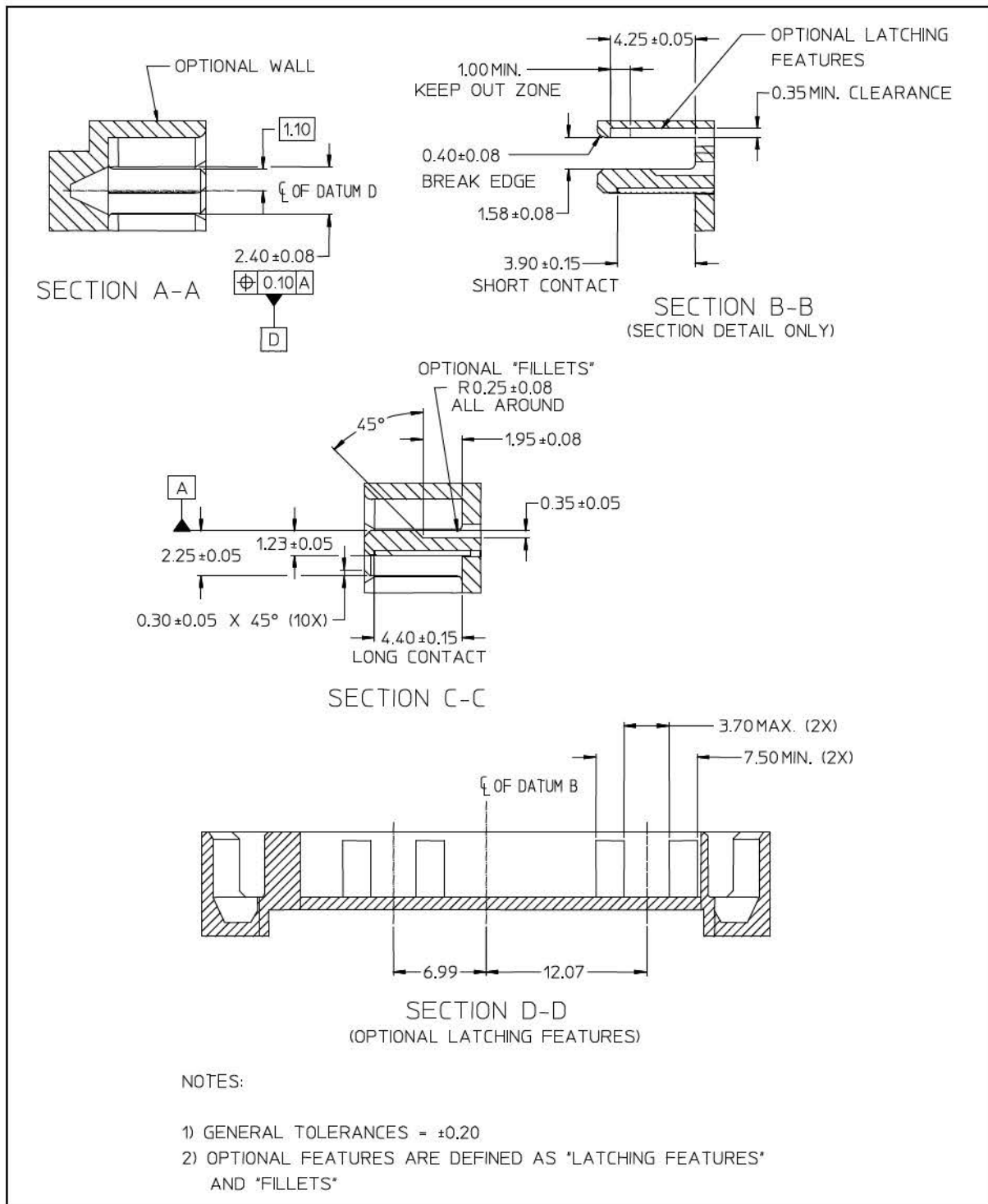


Figure 28 – Device Plug Connector (additional views)

6.1.3.2 Pin Signal Definition and Contact Mating Sequence

Table 2 details the pin names, types, and contact order of the two SATA plug options. A brief description is also included for signal, ground and power pins. There are total of 7 pins in the signal segment and 15 pins in the power segment.

Table 2 – Signal and Power SATA Plug and Nominal Mate Sequence

	Name	Type	Description	Cable Usage ^{2, 3}	Backplane Usage ³
Signal Segment	S1	GND		1 st Mate	2 nd Mate
	S2	A+	Differential Signal Pair A	2 nd Mate	3 rd Mate
	S3	A-		2 nd Mate	3 rd Mate
	S4	GND		1 st Mate	2 nd Mate
	S5	B-	Differential Signal Pair B	2 nd Mate	3 rd Mate
	S6	B+		2 nd Mate	3 rd Mate
	S7	GND		1 st Mate	2 nd Mate
Key and Spacing separate signal and power segments ⁴					
Power Segment	P1	V ₃₃	3.3V Power	2 nd Mate	3 rd Mate
	P2	V ₃₃	3.3V Power	2 nd Mate	3 rd Mate
	P3	V ₃₃	3.3V Power, Pre-charge	1 st Mate	2 nd Mate
	P4	GND		1 st Mate	1 st Mate
	P5	GND		1 st Mate	2 nd Mate
	P6	GND		1 st Mate	2 nd Mate
	P7	V ₅	5V Power, Pre-charge	1 st Mate	2 nd Mate
	P8	V ₅	5V Power	2 nd Mate	3 rd Mate
	P9	V ₅	5V Power	2 nd Mate	3 rd Mate
	P10	GND		1 st Mate	2 nd Mate
	P11	DAS/DSS	Device Activity Signal / Disable Staggered Spinup ¹	2 nd Mate	3 rd Mate
	P12	GND		1 st Mate	1 st Mate
	P13	V ₁₂	12V Power, Pre-charge	1 st Mate	2 nd Mate
	P14	V ₁₂	12V Power	2 nd Mate	3 rd Mate
	P15	V ₁₂	12V Power	2 nd Mate	3 rd Mate
NOTE:					
1. The corresponding pin to be mated with P11 in the power cable receptacle connector shall always be grounded. For specific optional usage of pin P11 see section 6.4.					
2. Although the mate order is shown, hot plugging is not supported when using the cable connector receptacle.					
3. All mate sequences assume zero angular offset between connectors.					
4. The signal segment and power segment may be separate.					

Mating Configuration Notes

- All pins are in a single row with 1.27mm (.050") pitch
- All ground pins in the Serial ATA device plug power segment (connector (pins P4, P5, P6, P10, and P12) shall be bussed together on the Serial ATA device.
- The connection between the Serial ATA device signal ground and power ground is vendor specific.
- The following sets of voltage pins in the Serial ATA device plug power segment shall be bussed together on the Serial ATA device:
 - P1, P2, and P3 3.3V power delivery and precharge
 - P7, P8, and P9 5V power delivery and precharge
 - P13, P14, and P15 12V power delivery and precharge

- The use of power delivery schemes that do not deliver all the specified voltages should only be used in scenarios where there is sufficient configuration control to ensure that the attached device does not require a supply voltage that is not provided.

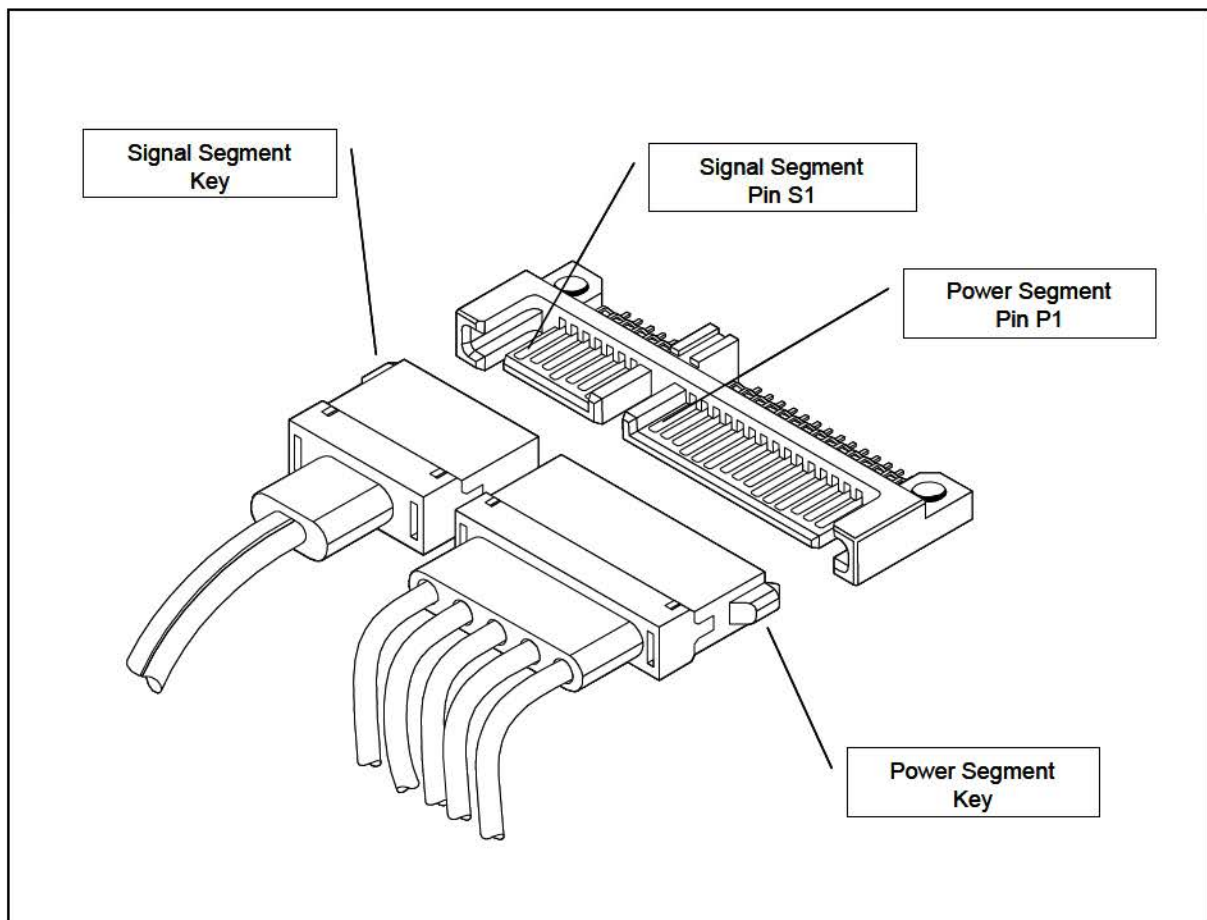


Figure 29 – Connector Pin and Feature Locations

6.1.4 Signal cable receptacle connector

Figure 30 shows the interface dimensions for the signal cable receptacle connector. There are two identical receptacles at the two ends of the Serial ATA cable assembly. The cable receptacle mates with either the signal segment of the device plug connector on the device, or the host plug connector on the host.

Figure 31 defines an optional positive latch solution for internal cabled system applications. The latch requires the user to press and hold a release mechanism when disconnecting the cable. The latching feature option for device and host plug connectors are required in order to provide a latching surface. Without a latching surface, there is no retention feature to hold a latching cable assembly in place.

It is optional to implement the latch on cable receptacles.



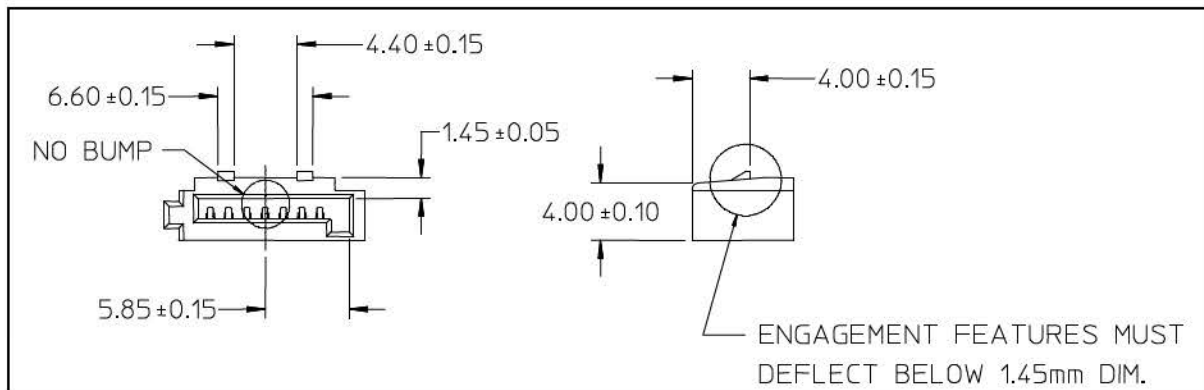


Figure 31 – Latching signal cable receptacle

The pin out of the cable receptacle connector is the mirror image of the signal segment of the device plug connector. Notice that

- ☐ The two differential pin pairs are terminated with the corresponding differential cable pairs
- ☐ The ground pins are terminated with the cable drain wires, if it applies
- ☐ The choice of cable termination methods, such as crimping or soldering is up to each connector vendor

6.1.5 Signal host plug connector

The signal host plug connector is to be mated with one end of the Serial ATA cable assembly. The pinout of the host plug connector is the mirror image of the signal cable receptacle. Figure 32 shows the host plug connector interface definition. The host plug includes optional features to allow use of latching cables, fillets, and additional material to improve connector robustness.

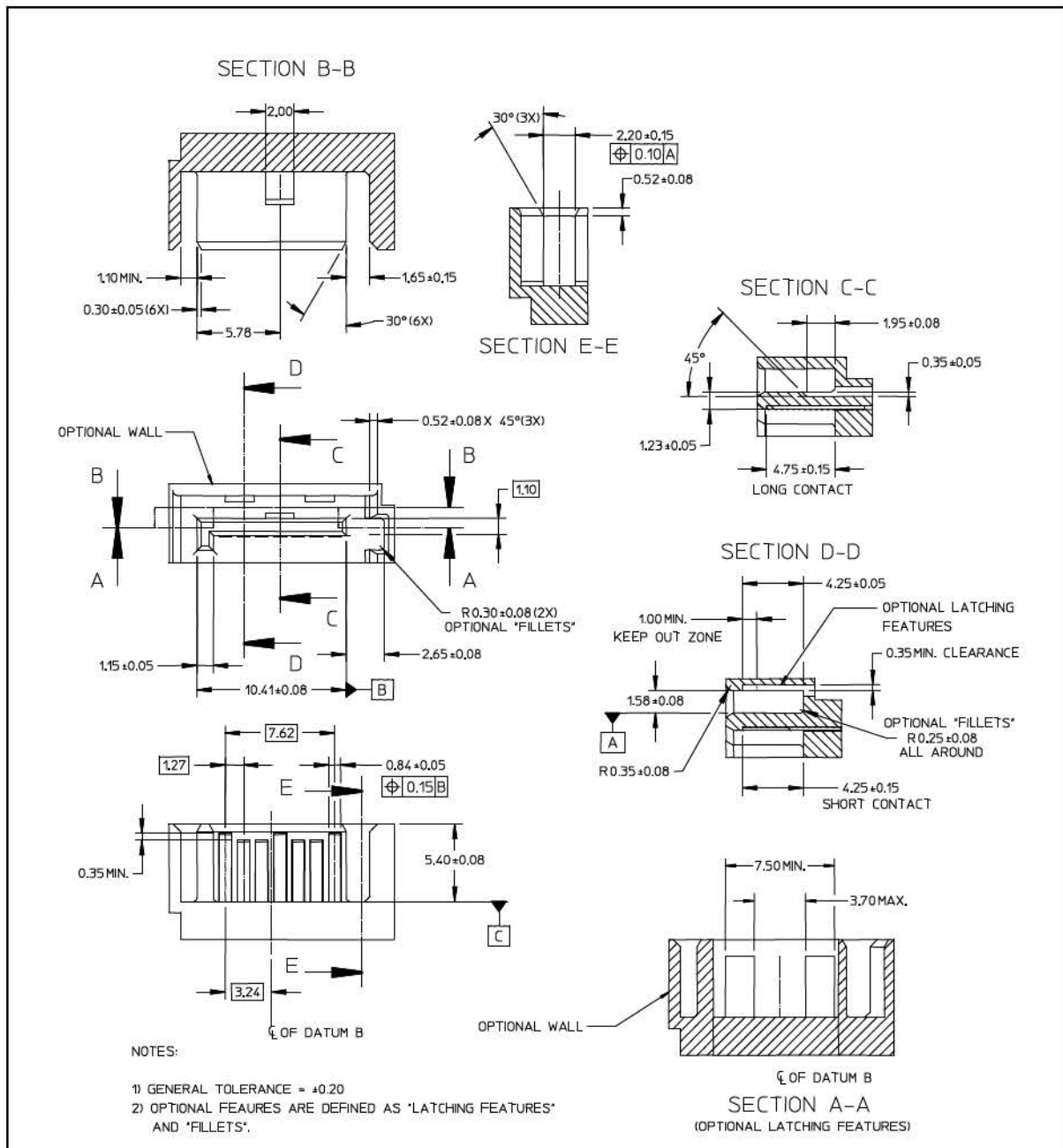


Figure 32 – Host signal plug connector interface dimensions

6.1.5.1 Internal plug stacking

The purpose of this recommended layout is to conserve motherboard, HBA and I/O controller printed circuit board space to support system density and size goals for such products.

For applications where multiple Serial ATA ports or connectors are stacked together on the host, there is a clearance or spacing requirement to prevent the cable assemblies from interfering with

each other. Figure 33 shows the recommended clearance or spacing. Figure 34 shows the recommended clearance and orientation to allow access for latching cables.

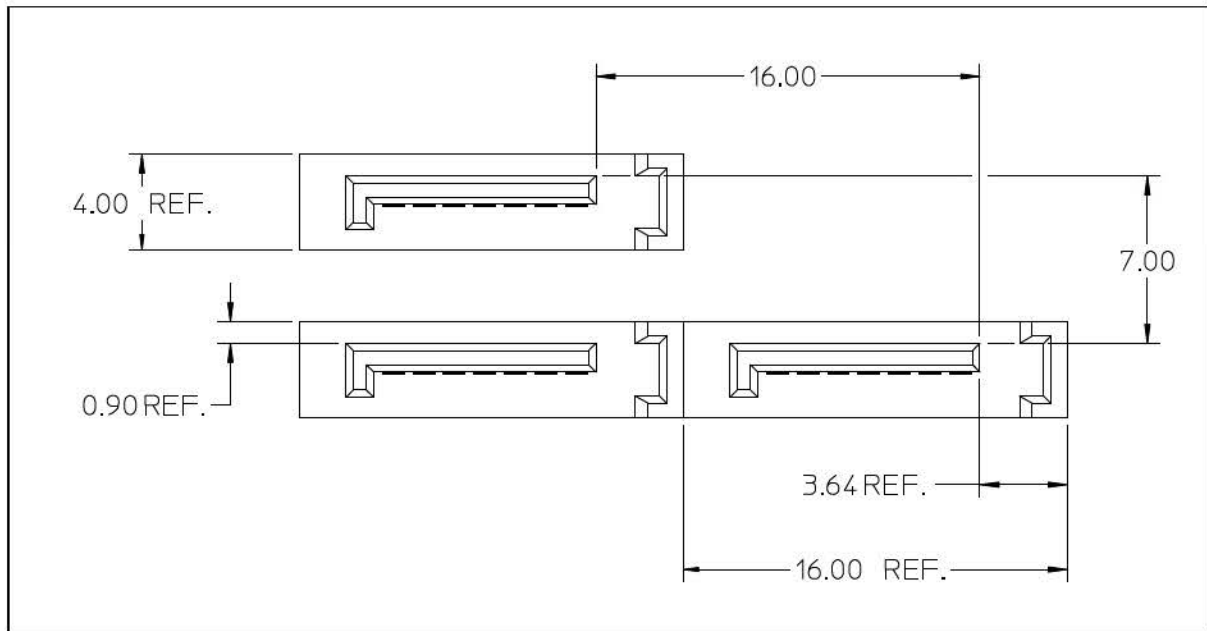


Figure 33 – Non-Latching Connector Stack Spacing and Orientation

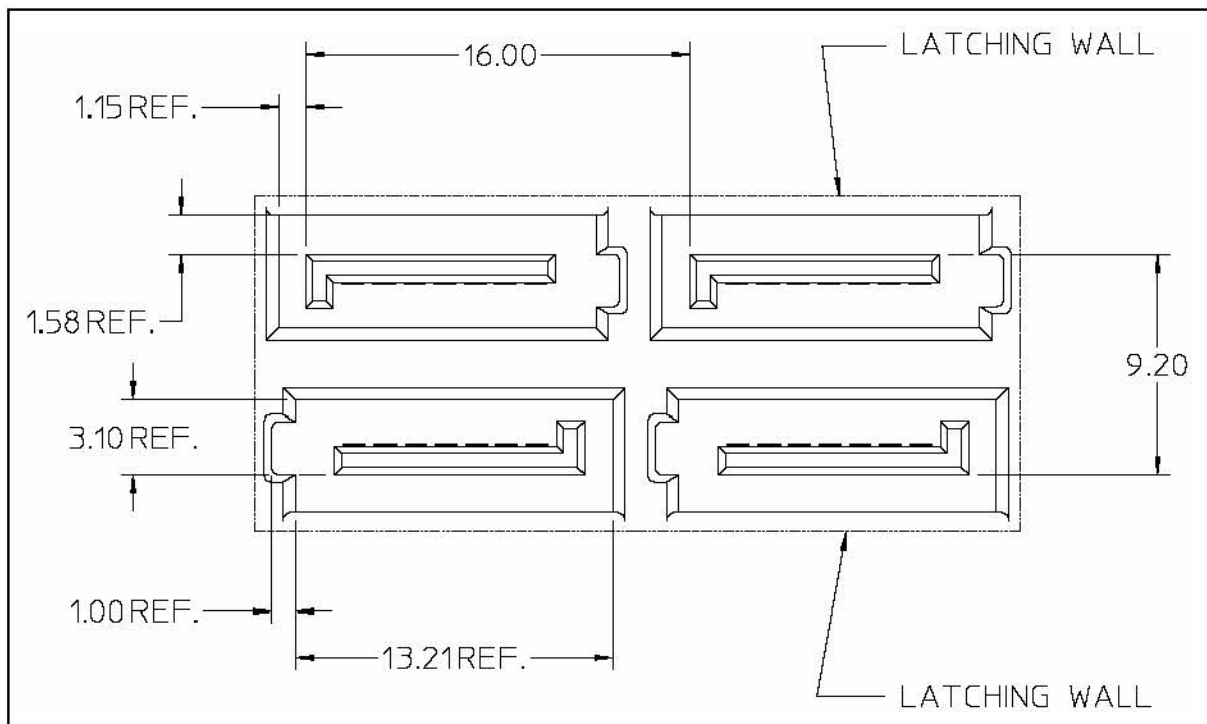


Figure 34 – Latching Connector Stack Spacing and Orientation

6.1.6 Backplane connector

The backplane connector is to be blind-mated directly with the device plug connector. The interface dimensions for the backplane connector are shown in Figure 35. Note that dimension B allows two values: 8.15mm and 14.15mm. There are two levels of contacts in the backplane connector. The advancing ground contacts P4 and P12 mate first with the corresponding ground pins on the device plug connector, followed by the engaging of the pre-charged power pins. An appropriate external retention mechanism independent of the connector is required to keep the host PCB and the device in place. The backplane connector is not designed with any retention mechanism.

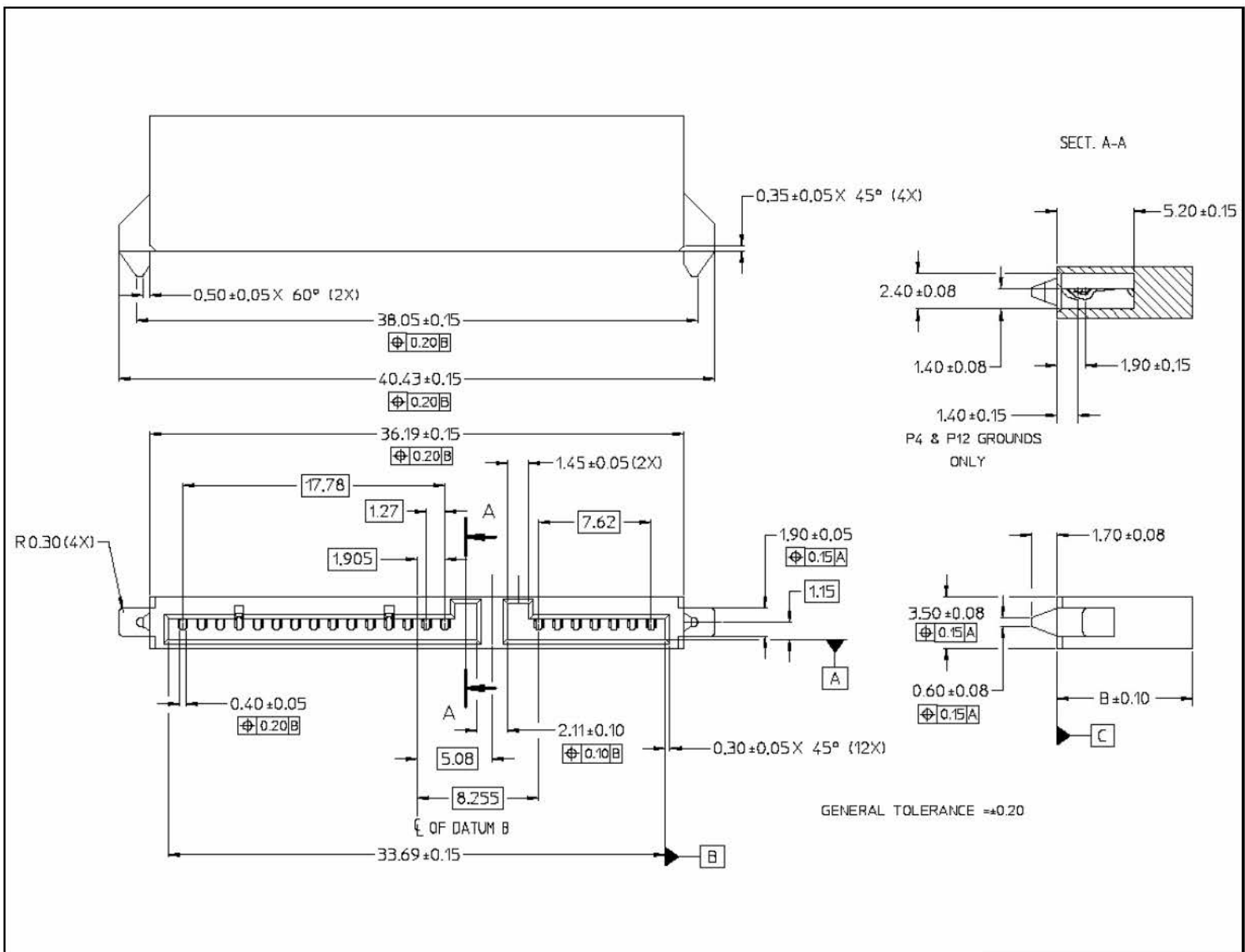


Figure 35 – Backplane connector interface dimensions

6.1.6.1 Backplane connector configuration and blind-mating tolerance

The maximum blind-mate misalignment tolerances are ± 1.50 mm and ± 1.00 mm, respectively, for two perpendicular axes illustrated in Figure 36. Any skew angle of the plug, with respect to the receptacle, reduces the blind-mate tolerances.

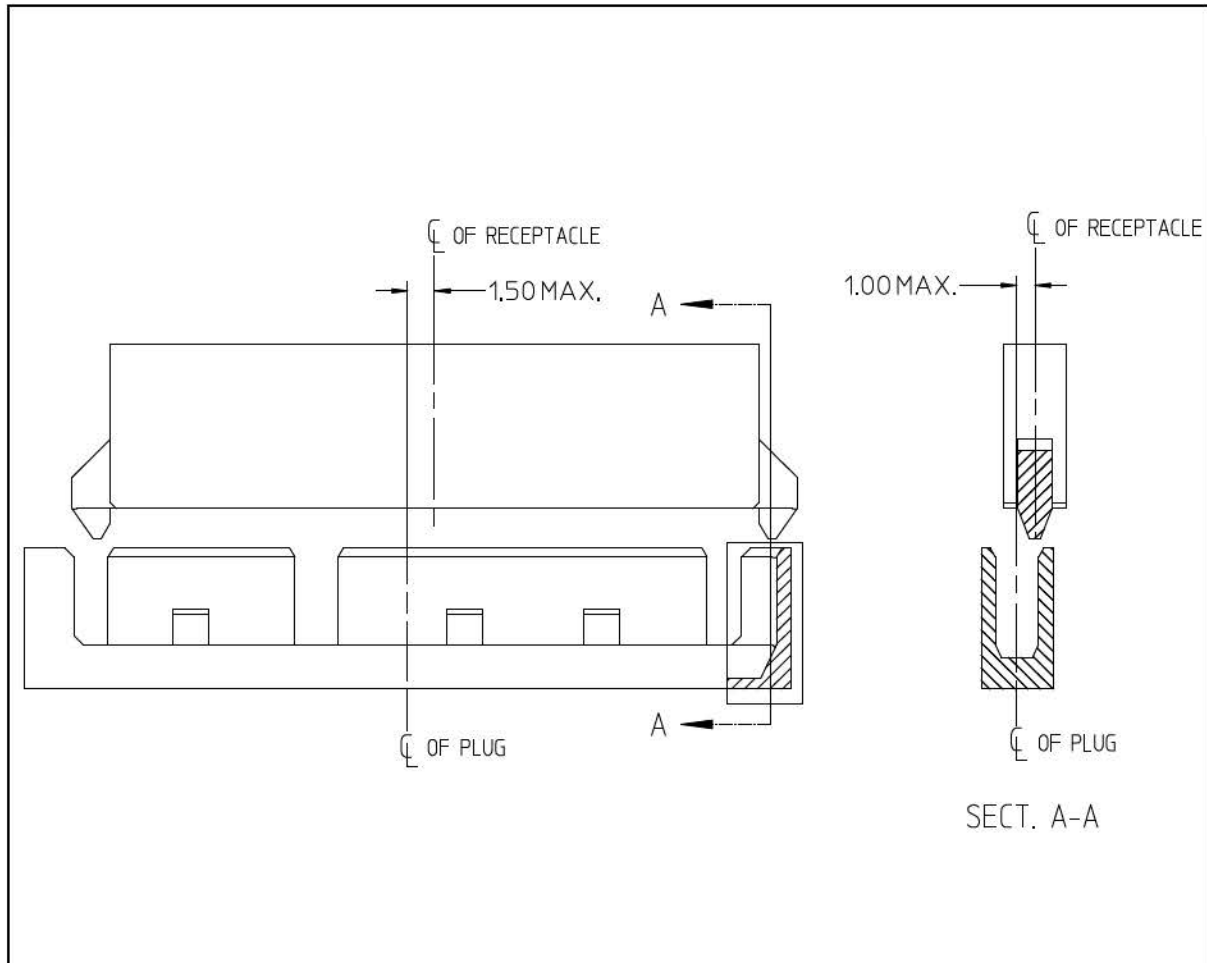


Figure 36 – Connector pair blind-mate misalignment tolerance

The device-to-backplane mating configuration is shown in Figure 37. The allowed values for dimension A and dimension B are shown in Table 3.

Table 3 – Allowed values for dimension A and B for device-to-backplane mating

Description	Standard	Extended
Device mated height (A)	8.45 mm	14.45 mm
Component clearance (B)	3.55 mm	9.55 mm

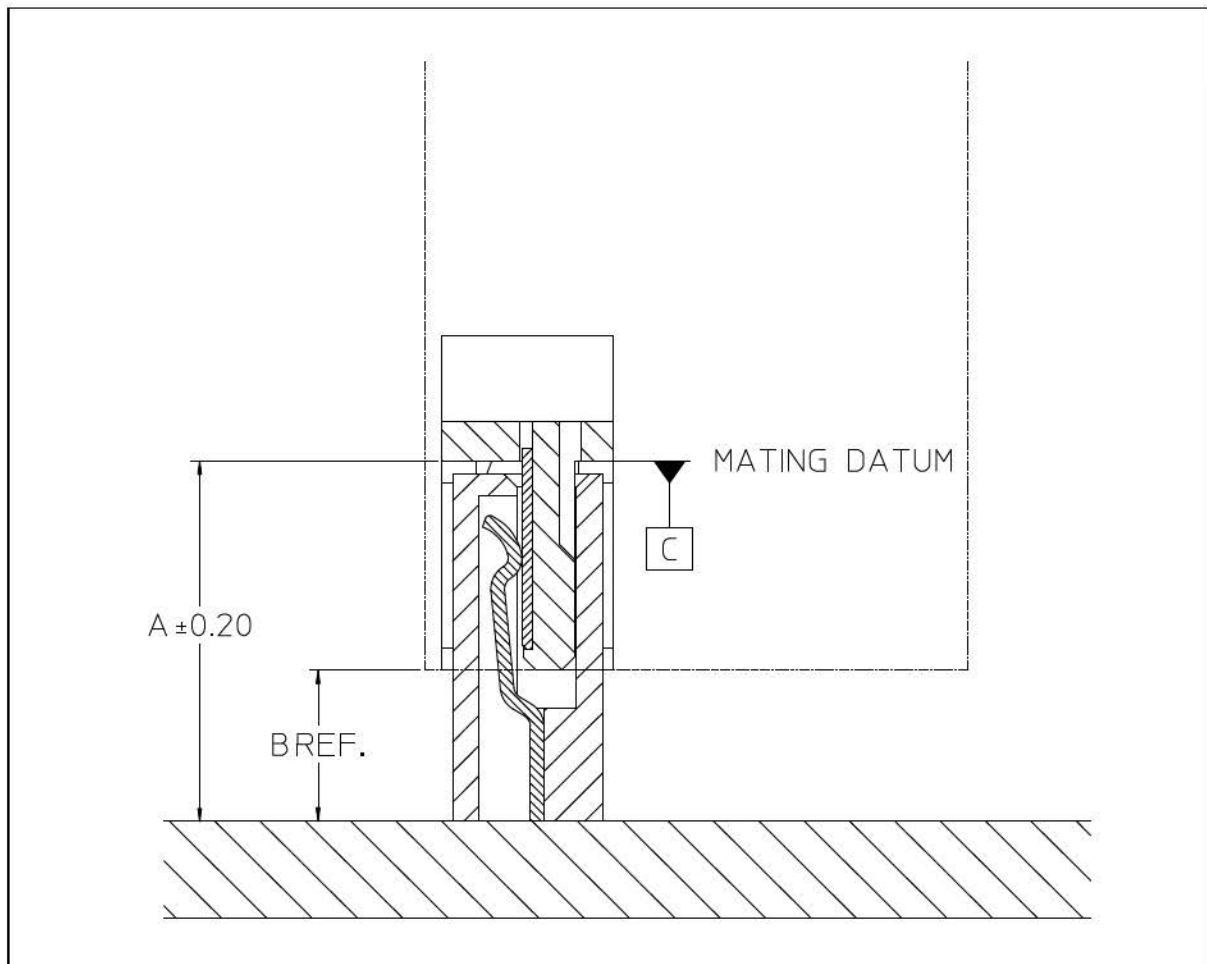


Figure 37 – Device-backplane mating configuration

6.1.7 Power cable receptacle connector

The power cable receptacle connector mates with the power segment of the device plug, bringing power to the device. Figure 38 shows the interface dimensions of the power receptacle connector. The pinout of the connector is the mirror image of the power segment of the device plug shown in Table 2. Figure 39 defines an optional positive latch solution for internal cabled system applications. The latch requires the user to press and hold a release mechanism when disconnecting the cable. The latching feature option for device plug connectors is required in order to provide a latching surface. Without a latching surface, there is no retention feature to hold a latching cable assembly in place.

It is optional to implement the latch on cable receptacles.

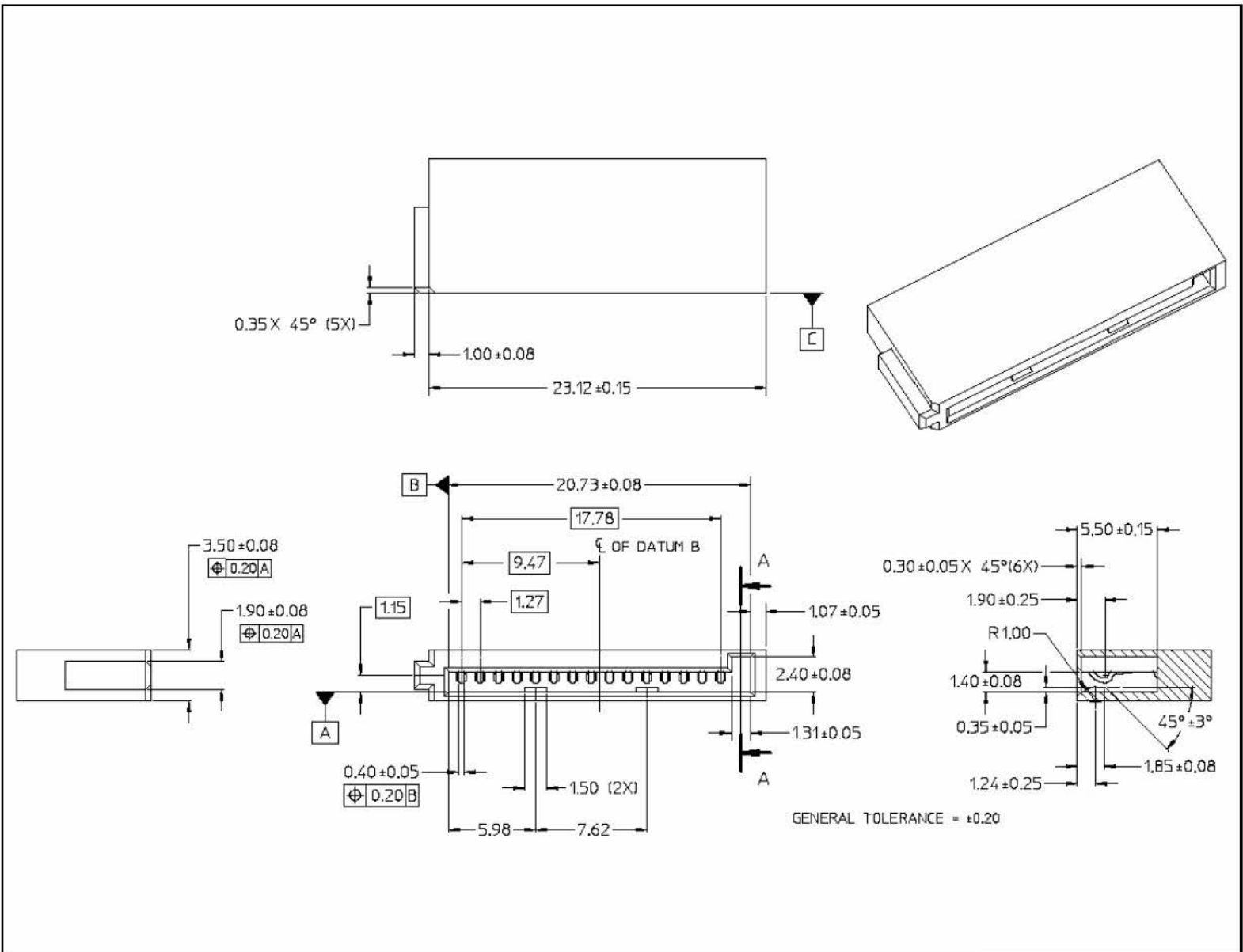


Figure 38 – Power receptacle connector interface dimensions

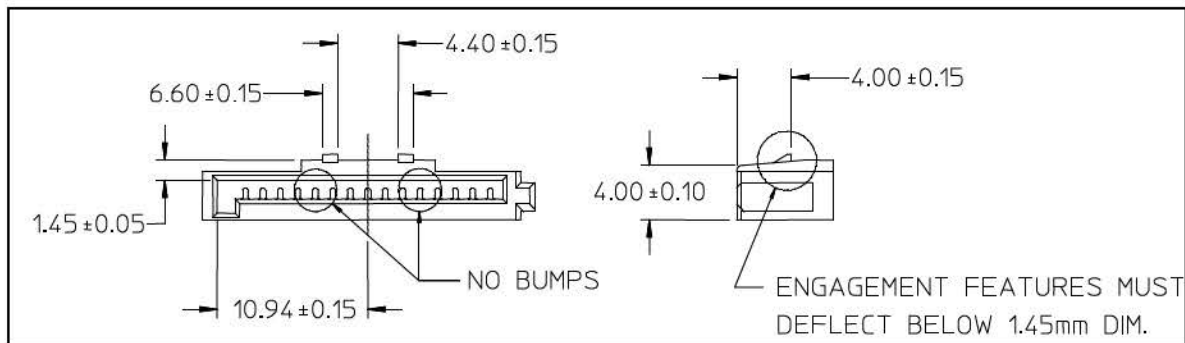


Figure 39 – Latching power cable receptacle

The power receptacle connector is terminated onto 18 AWG wires that are connected to the system power supply or other power sources. Five 18 AWG wires may be used, with three wires terminated to the nine power pins for the three voltages, while the remaining two wires to the six ground pins.

6.1.8 Internal single lane cable

The internal single lane cable consists of four conductors in two differential pairs. If necessary, the cable may also include drain wires to be terminated to the ground pins in the Serial ATA cable receptacle connectors. The conductor size may be 30 to 26 AWG. The cable maximum length is one meter.

This specification does not specify a standard internal single lane cable. Any cable that meets the electrical requirements in section 6.2 is considered an acceptable internal single lane cable. The connector and cable vendors have the flexibility to choose cable constructions and termination methods based on performance and cost considerations. An example cable construction is given in Figure 40 for an informational purpose only.

Although construction methodologies are not specified, there are a few essential elements of the Serial ATA cable that should be considered. Physical characteristics of the Serial ATA cable may include the following items. See Figure 40 for details.

- ☐ Shielded Pairs (2)
- ☐ Solid Tinned Copper (26 AWG)
- ☐ White Foam Polyolefin (43.5 mil Diameter)
- ☐ Parallel Drain Pairs (2 pr., 28 AWG – Solid Tinned Copper)
- ☐ Aluminized Polyester Foil (1 mil thick w/35mil overlap)
- ☐ Foil may be the blue longitudinal wrap that is sealed with heat
- ☐ Jacket (20 mil PVC wall)

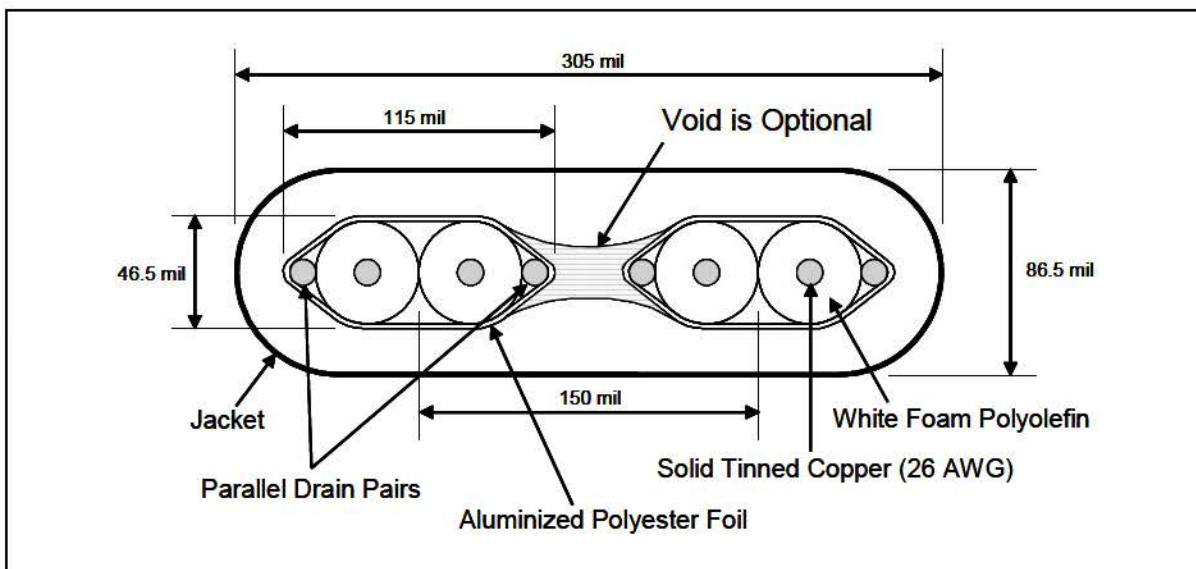


Figure 40 – Detailed cross-section of an example internal single lane cable

6.1.9 Connector labeling

Labeling on a connector with the connector manufacturer identifier or Serial ATA icon is optional.

6.1.10 Connector and cable assembly requirements and test procedures

Unless otherwise specified, all measurements shall be performed within the following lab conditions:

- ☐ Mated
- ☐ Temperature: 15° to 35° C
- ☐ Relative Humidity: 20% to 80%
- ☐ Atmospheric Pressure: 650 mm to 800 mm of Hg

If an EIA (Electronic Industry Association) test is specified without a letter suffix in the test procedures, the latest approved version of that test shall be used.

6.1.10.1 Housing and contact electrical requirements

Table 4 is the connector housing and contact electrical requirements.

Table 4 – Housing and contact electrical parameters, test procedures, and requirements

Parameter	Procedure	Requirement
Insulation resistance	EIA 364-21 After 500 VDC for 1 minute, measure the insulation resistance between the adjacent contacts of mated and unmated connector assemblies.	1000 MΩ minimum

Parameter	Procedure	Requirement
Dielectric withstanding voltage	EIA 364-20 Method B Test between adjacent contacts of mated and unmated connector assemblies.	The dielectric shall withstand 500 VAC for 1 minute at sea level.
Low level contact resistance (LLCR)	EIA 364-23 Subject mated contacts assembled in housing to 20mV maximum open circuit at 100mA maximum	☐ Initially 30 mΩ maximum. ☐ Resistance increase 15 mΩ maximum after stress
Contact current rating (Power segment)	☐ Mount the connector to a test PCB ☐ Wire power pins P1, P2, P8, and P9 in parallel for power ☐ Wire ground pins P4, P5, P6, P10, and P12 in parallel for return ☐ Supply 6 A total DC current to the power pins in parallel, returning from the parallel ground pins (P4, P5, P6, P10, and P12) ☐ Record temperature rise when thermal equilibrium is reached	1.5 A per pin minimum. The temperature rise above ambient shall not exceed 30° C at any point in the connector when contact positions are powered. The ambient condition is still air at 25° C.

6.1.10.2 Mechanical and environmental requirements

Table 5 lists the mechanical parameters and requirements, while Table 6 the environmental and reliability tests and requirements:

Table 5 – Mechanical test procedures and requirements

Visual and dimensional inspections	EIA-364-18 Visual, dimensional and functional per applicable quality inspection plan.	Meets product drawing requirements
Cable pull-out	EIA-364-38 Condition A Subject a Serial ATA cable assembly to a 40 N axial load for a min of one minute while clamping one end of the cable plug.	No physical damage
Cable flexing	For round cable: EIA-364-41 Condition I Dimension $x=3.7 \times$ cable diameter, 100 cycles in each of two planes. For flat cable: EIA-364-41 Condition II 250 cycles using either method 1 or 2.	No physical damage. No discontinuity over 1 us during flexing.
Insertion force Cabled signal connector	EIA-364-13 Measure the force necessary to mate the connector assemblies at a max. rate of 12.5 mm per minute.	45 N Max.
Removal force Cabled signal connector (Non-latching)	EIA-364-13 Measure the force necessary to unmate the connector assemblies at a max. rate of 12.5 mm per minute.	10 N Min. through 50 cycles
Insertion force Cabled power connector	EIA-364-13 Measure the force necessary to mate the connector assemblies at a max. rate of 12.5 mm per minute.	45 N Max.
Removal force Cabled power connector (Non-latching)	EIA-364-13 Measure the force necessary to unmate the connector assemblies at a max. rate of 12.5 mm per minute.	15 N Min. for cycles 1 through 5 10 N Min. through 50 cycles
Insertion force Backplane connector	EIA-364-13 Measure the force necessary to mate the connector assemblies at a max. rate of 12.5 mm per minute.	20 N Max.
Removal force Backplane connector	EIA-364-13 Measure the force necessary to unmate the connector assemblies at a max. rate of 12.5 mm per minute.	4 N Min. after 500 cycles
Removal force Cabled Latching connector Includes power and signal connectors	EIA-364-13 Apply a static 25 N unmating test load	No damage and no disconnect through 50 mating cycles
Durability	EIA-364-09 50 cycles for internal cabled application; 500 cycles for backplane/blindmate application. Test done at a maximum rate of 200 cycles per hour.	No physical damage. Meet requirements of additional tests as specified in the test sequence in section 6.3.9.5

Table 6 – Environmental parameters, test procedures, and requirements

Parameter	Procedure	Requirement
Physical shock	EIA 364-27 Condition H Subject mated connectors to 30 g's half-sine shock pulses of 11 ms duration. Three shocks in each direction applied along three mutually perpendicular planes for a total of 18 shocks. See NOTE 2.	No discontinuities of 1 us or longer duration. No physical damage.
Random vibration	EIA 364-28 Condition V Test letter A Subject mated connectors to 5.35 g's RMS. 30 minutes in each of three mutually perpendicular planes. See NOTE 2.	No discontinuities of 1 us longer duration.
Humidity	EIA 364-31 Method II Test Condition A. Subject mated connectors to 96 hours at 40° C with 90% to 95% RH.	See NOTE 1
Temperature life	EIA 364-17 Test Condition III Method A. Subject mated connectors to temperature life at +85°C for 500 hours.	See NOTE 1.
Thermal shock	EIA 364-32 Test Condition I. Subject mated connectors to 10 cycles between –55° C and +85° C.	See NOTE 1.
Mixed Flowing Gas	EIA 364-65, Class 2A Half of the samples are exposed unmated for seven days, then mated for remaining seven days. Other half of the samples are mated during entire testing.	See NOTE 1.
<p>NOTE:</p> <ol style="list-style-type: none"> 1. Shall meet EIA 364-18 Visual Examination requirements, show no physical damage, and shall meet requirements of additional tests as specified in the test sequence in section 6.3.9.5. 2. Shock and vibration test fixture is to be determined by each user with connector vendors. 		

An additional requirement is listed in Table 7.

Table 7 – Additional requirement

Parameter	Procedure	Requirement
Flammability	UL 94V-0	Material certification or certificate of compliance required with each lot to satisfy the Underwriters Laboratories follow-up service requirements.

It should be pointed out that this specification does not attempt to define the connector and cable assembly reliability requirements that are considered application-specific. It is up to users and their connector suppliers to determine if additional requirements shall be added to satisfy the application needs. For example, a user who requires a SMT connector may want to include additional requirements for SMT connector reliability.

6.1.10.3 Sample selection

Samples shall be prepared in accordance with applicable manufacturers' instructions and shall be selected at random from current production. Each test group shall provide 100 data points for a good statistical representation of the test result. For a connector with greater than 20 pins, a test group shall consist of a minimum of five connector pairs. From these connector pairs, a minimum of 20 contact pairs per mated connector shall be selected and identified. For connectors with less than 20 pins, choose the number of connectors sufficient to provide 100 data points.

6.1.10.4 Test sequence

Table 8 shows the connector test sequences for five groups of tests.

Table 8 – Connector test sequences

Test or examination	Test group				
	A	B	C	D	E
Examination of the connector(s)	1, 5	1, 9	1, 8	1, 8	1, 7
Low-Level Contact Resistance (LLCR)	2, 4	3, 7	2, 4, 6		4, 6
Insulation resistance				2, 6	
Dielectric withstanding voltage				3, 7	
Current rating			7		
Insertion force		2			
Removal force		8			
Durability	3	4 ⁽¹⁾			2 ⁽¹⁾
Physical shock		6			
Vibration		5			
Humidity				5	
Temperature life			3		
Reseating (manually unplug/plug three times)			5		5
Mixed Flowing Gas					3
Thermal shock				4	
NOTE –					
1. Preconditioning, 20 cycles for the 50-durability cycle requirement, 50 cycles for the 500-durability cycle requirement. The insertion and removal cycle is at the maximum rate of 200 cycles per hour.					

For example, in Test Group A, one would perform the following tests:

1. Examination of the connector(s)
2. LLCR
3. Durability
4. LLCR
5. Examination of the connector(s)

6.1.11 Internal Multi Lane cables

This section defines standard cable assemblies and headers for connecting multiple Serial ATA links from a RAID host bus adapter to a backplane within the same enclosure or server, or for connecting multiple Serial ATA links from a host bus adapter to individual devices.

This cable/connector is based on the SFF-8484 specification. The SFF-8484 specification is also used by Serial Attached SCSI (SAS).

6.1.11.1 Requirements

- ☐ 2 or 4 lanes, SAS/Serial ATA signals.
- ☐ Either point to point with a high density connector on both ends of the cable or fanout with a high density connector on one end of the cable assembly and individual single lane connectors on the other end of the cable assembly.
- ☐ Additional pins/conductors for sideband signals.
- ☐ Specifications for PCB footprint for SMT, thru hole and press fit.
- ☐ RX, TX, RX, TX pin sequencing to minimize crosstalk.
- ☐ Ground reference between each pair.
- ☐ Flexible cable for routing and airflow.
- ☐ Performance for 3.0 Gbps.
- ☐ Compliance points are at the ends of a mated cable interface. If additional interconnect media between host and device exists, that portion of the design is proprietary and shall ensure the mated cable interface compliance points are met.
- ☐ The Internal Multi Lane cable assembly shall meet the electrical characteristics defined in section 6.3.

6.1.11.2 Multi Lane Component Descriptions

Three components are defined in this section for Multi Lane applications. Each component has a 2 Lane and a 4 Lane version. Pin assignments are provided at the end of this section.

- ☐ Cable Receptacles and Backshells
- ☐ Vertical Headers
- ☐ Right Angle Headers

6.1.11.2.1 Multi Lane Cable Receptacles and Backshells

Figure 41 and Figure 42 show isometric drawings of the internal Multi Lane cables and connectors. Refer to SFF-8484 for dimensions and mechanical details.

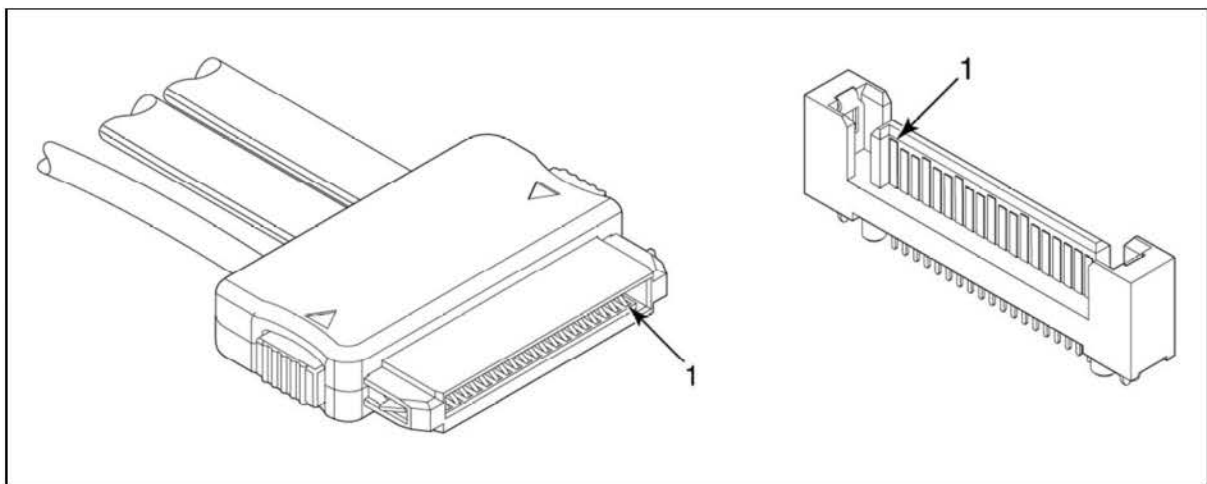


Figure 41 – Isometric drawings of the internal 2 Lane cable and connector

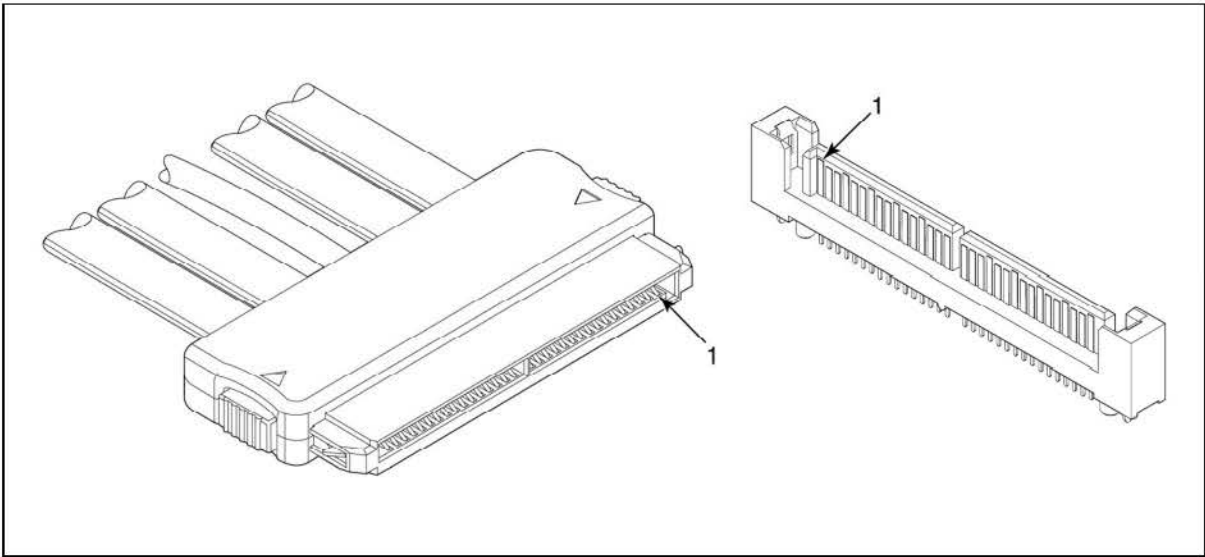
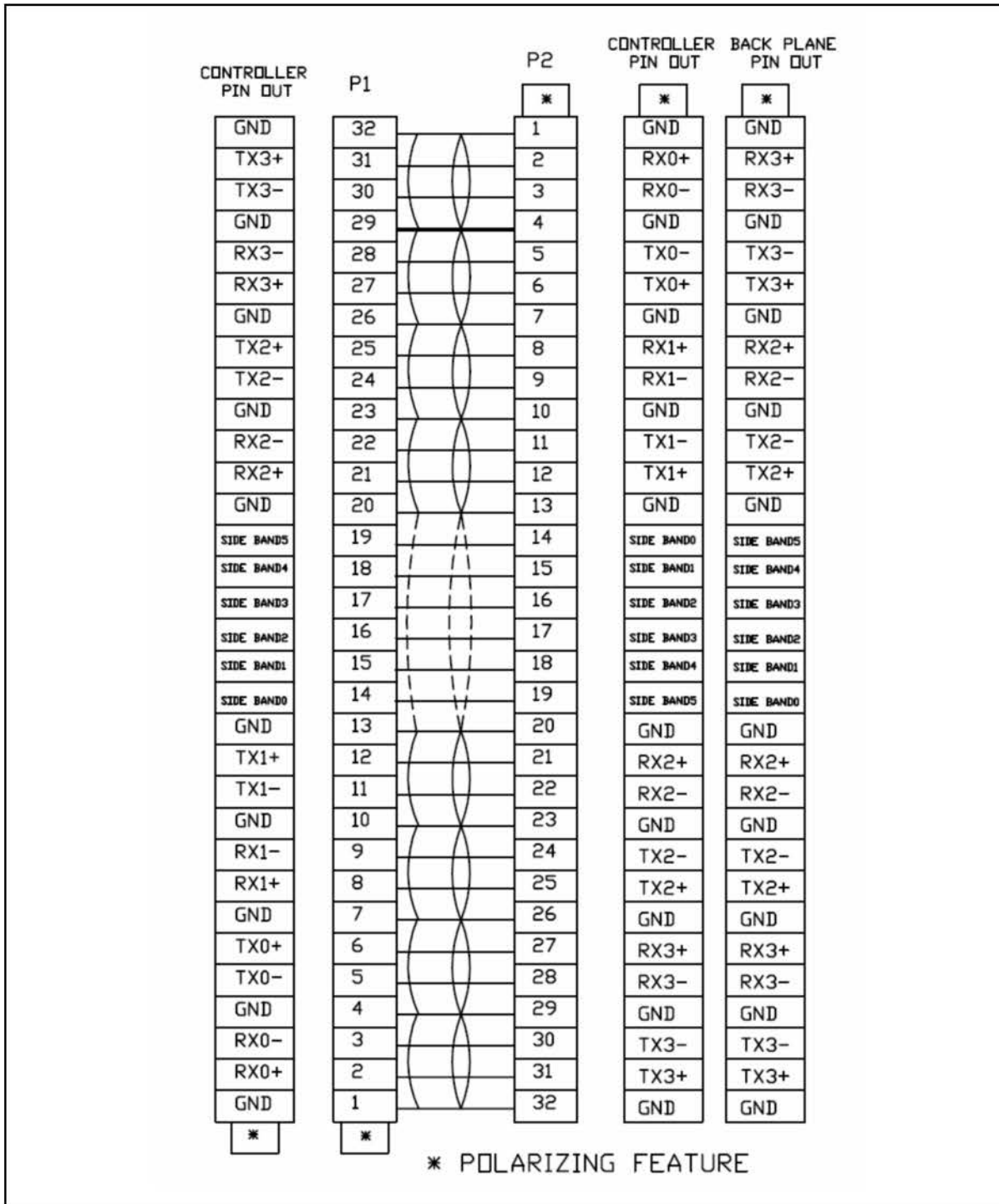


Figure 42 – Isometric drawings of the internal 4 Lane cable and connector

6.1.11.2.24 Lane Pin Assignments



Note: Dashed line around Side Band lines 14 – 19 indicates shielding optional based on application and may be connected to the adjacent signal grounds.

Figure 43 – 4 Lane Pin Assignments

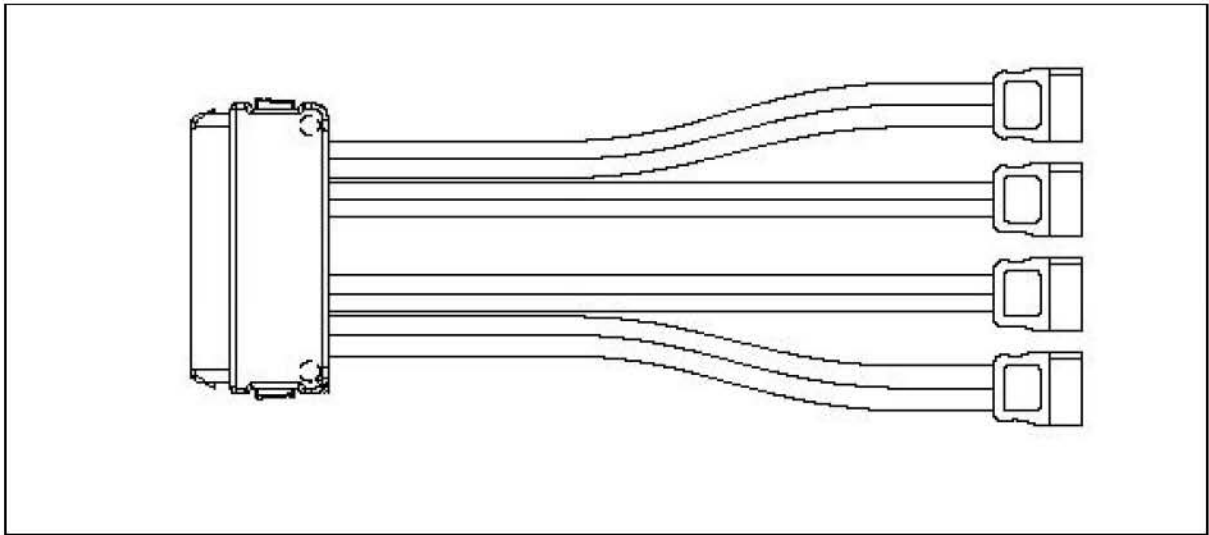
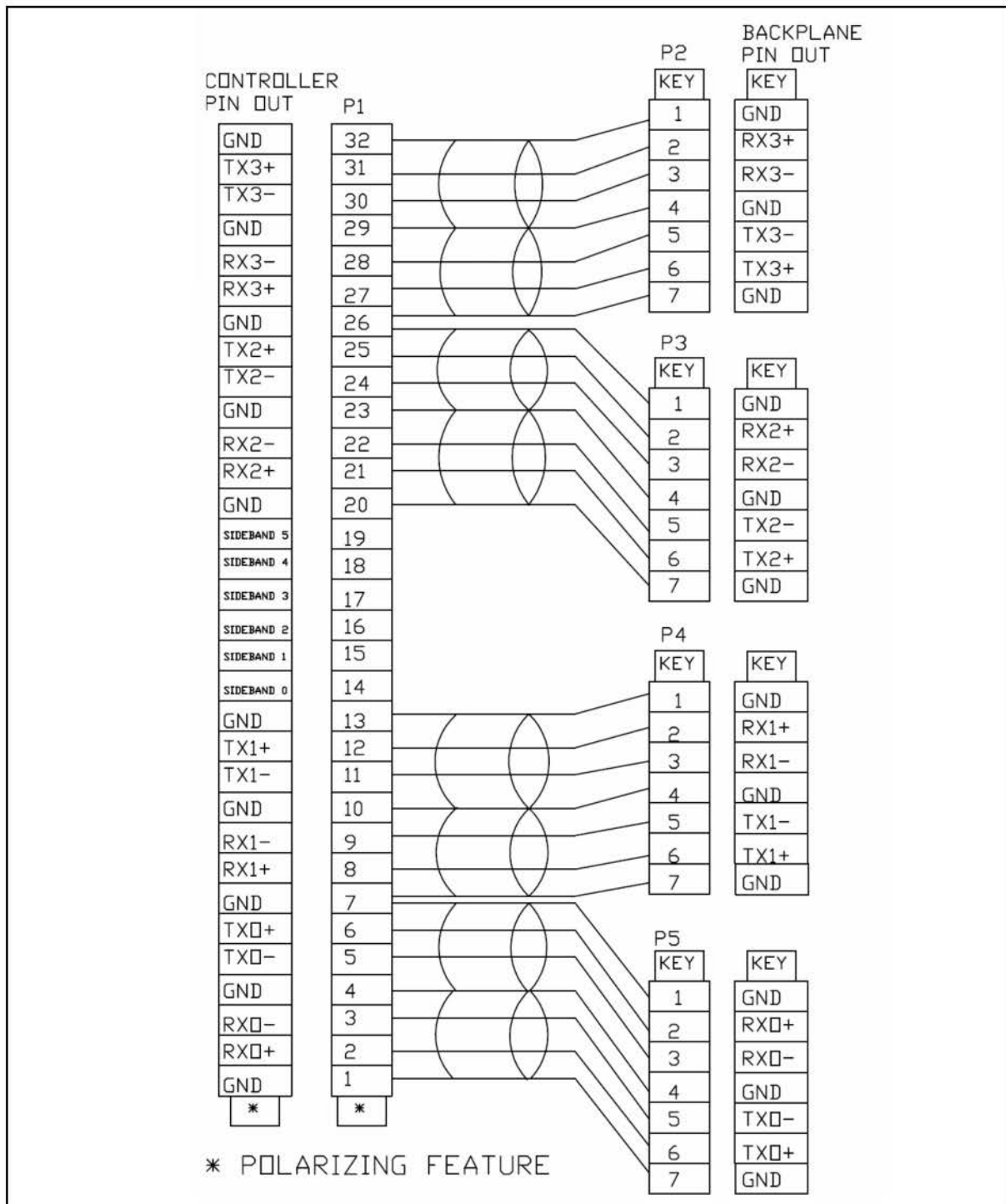


Figure 44 – 4 Lane to 4 x 1 Lanes, Fanout Implementation



Note: Sideband signals not shown

Figure 45 – 4 Lane Fanout Pin Assignments

6.1.11.3 2 Lane Pin Assignments

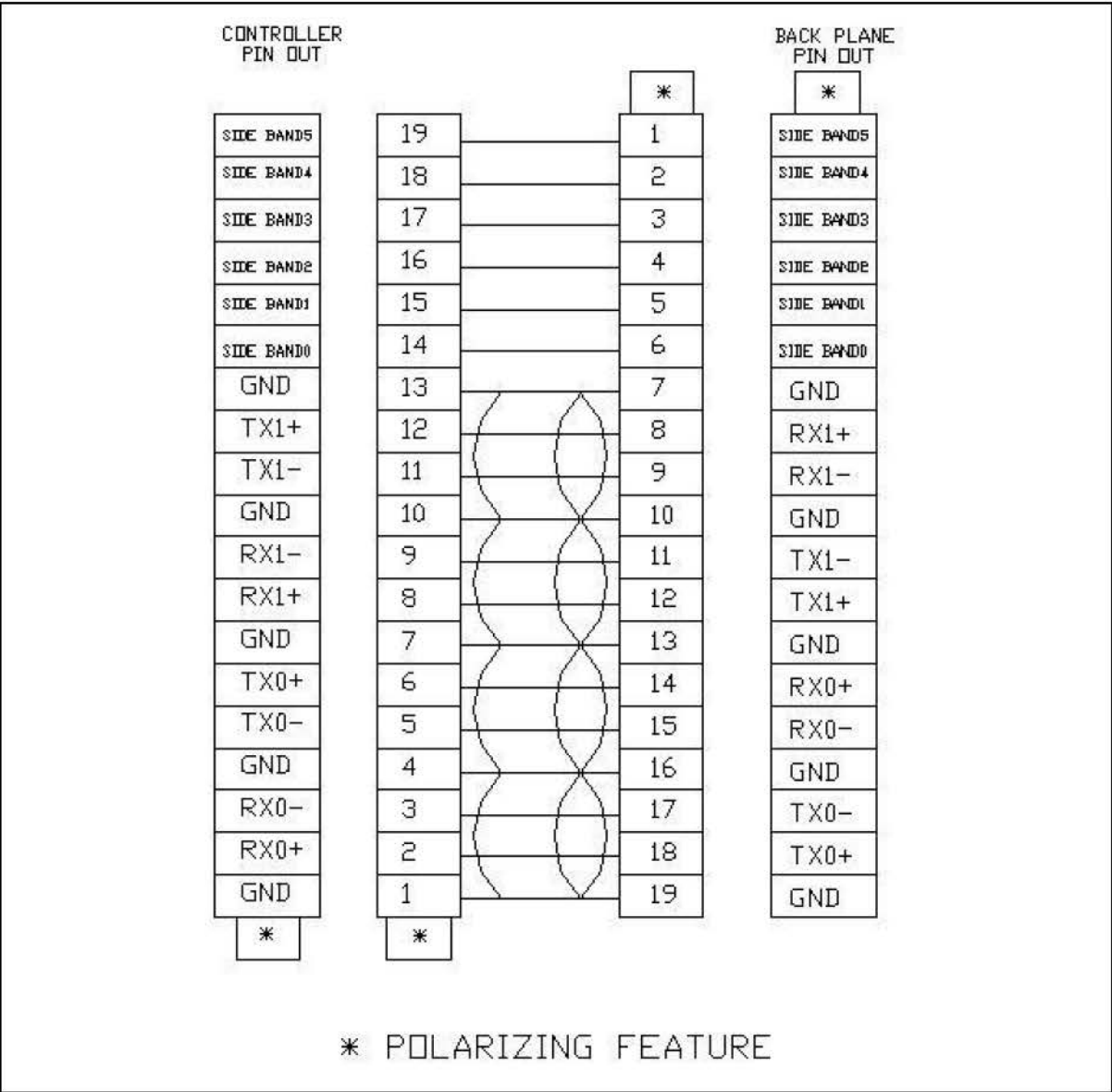


Figure 46 – 2 Lane Fanout Pin Assignments

6.2 External cables and connectors

6.2.1 External Single Lane

The External Single Lane system provides a single lane connection between a PC/Laptop and a commodity storage device using Gen1i/Gen2i Serial ATA devices. This interface is for the use of an external drive that resides outside the PC chassis, similar to USB or 1394 hard drives and optical drives. While this does not exclude other usages, the requirements are derived based on this usage model.

Power is supplied to the external storage device via a separate means, which is outside the scope of this specification. This separate means is expected to be similar to power delivery for USB or 1394 external drives.

This section defines the external interconnect, compliance points, and associated electrical requirements/parameters for device interoperability.

The primary implementation is:

- ☐ An HBA connected to a shielded external connector. A buffer IC is required to interface to a Gen1i/Gen2i Serial ATA host unless the Serial ATA host is Gen1m/Gen2m compliant and designed for direct external connection.
- ☐ A shielded Serial ATA cable designed for external usage.
- ☐ A Serial ATA device enclosure with a corresponding external connector. A buffer IC is required to interface to a Gen1i/Gen2i Serial ATA device unless the Serial ATA device is Gen1m/Gen2m compliant and designed for direct external connection.

This implementation is shown in Figure 47.

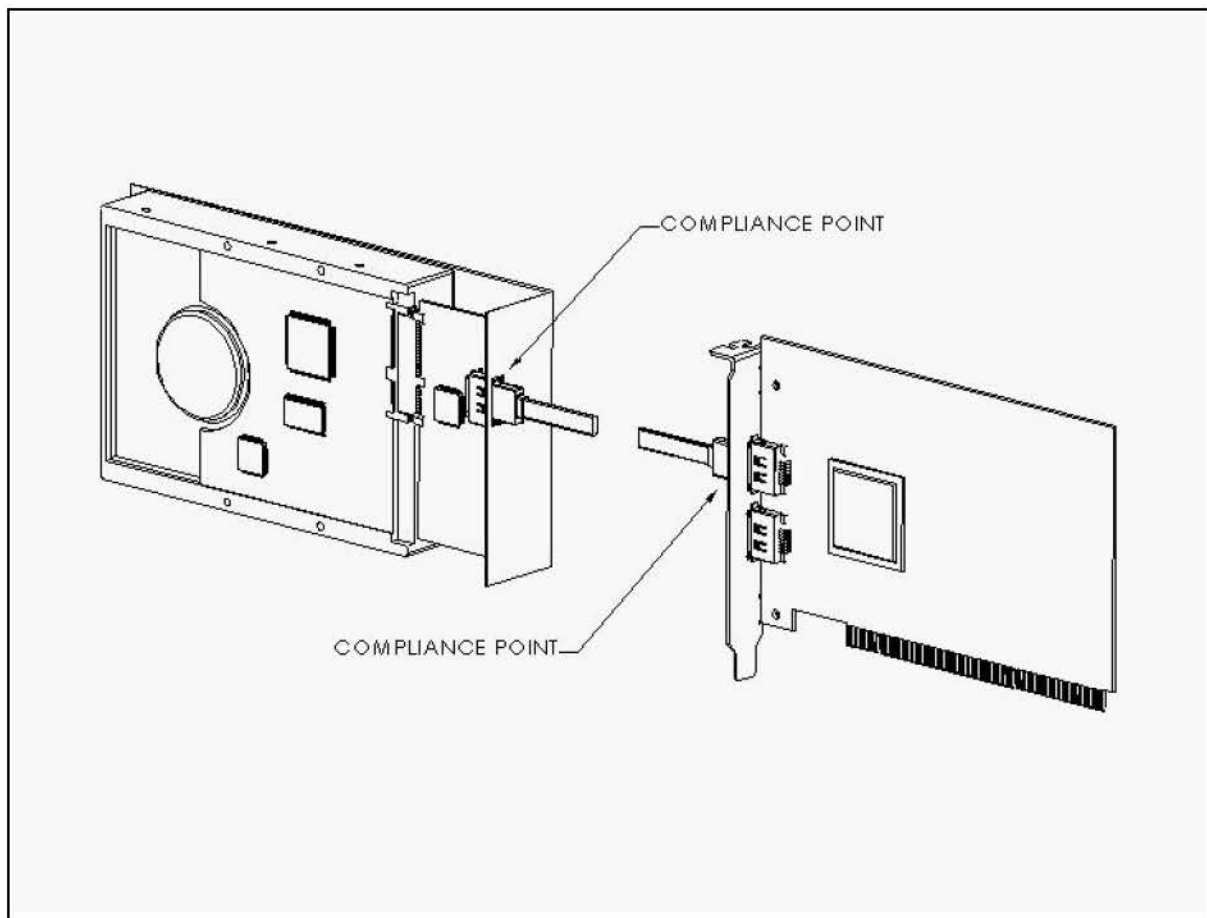


Figure 47 – Usage Model for HBA with external cable and single device enclosure

A second potential implementation is a Serial ATA host directly assembled on the motherboard connected to a shielded external connector via a pigtail to the motherboard connection. In this implementation, the external Serial ATA cable and the drive assembly are similar to Figure 83,

but another cable and connector pair between the motherboard and the external cable is introduced, placing an additional discontinuity point between host and drive.

There are two compliance points for the External Single Lane system, one at each shielded external connector. As with other cable and connector system descriptions, interconnect between the IC/Phy and the connectors at the mating interface are outside the scope of the definition and are considered part of the delivered Phy solution. Implementations that have additional connections between the Phy/IC and the shielded external connector shall provide such interconnects as part of the engineered solution. For an implementation such as shown in Figure 48, the compliance points remain at the shielded external connectors.

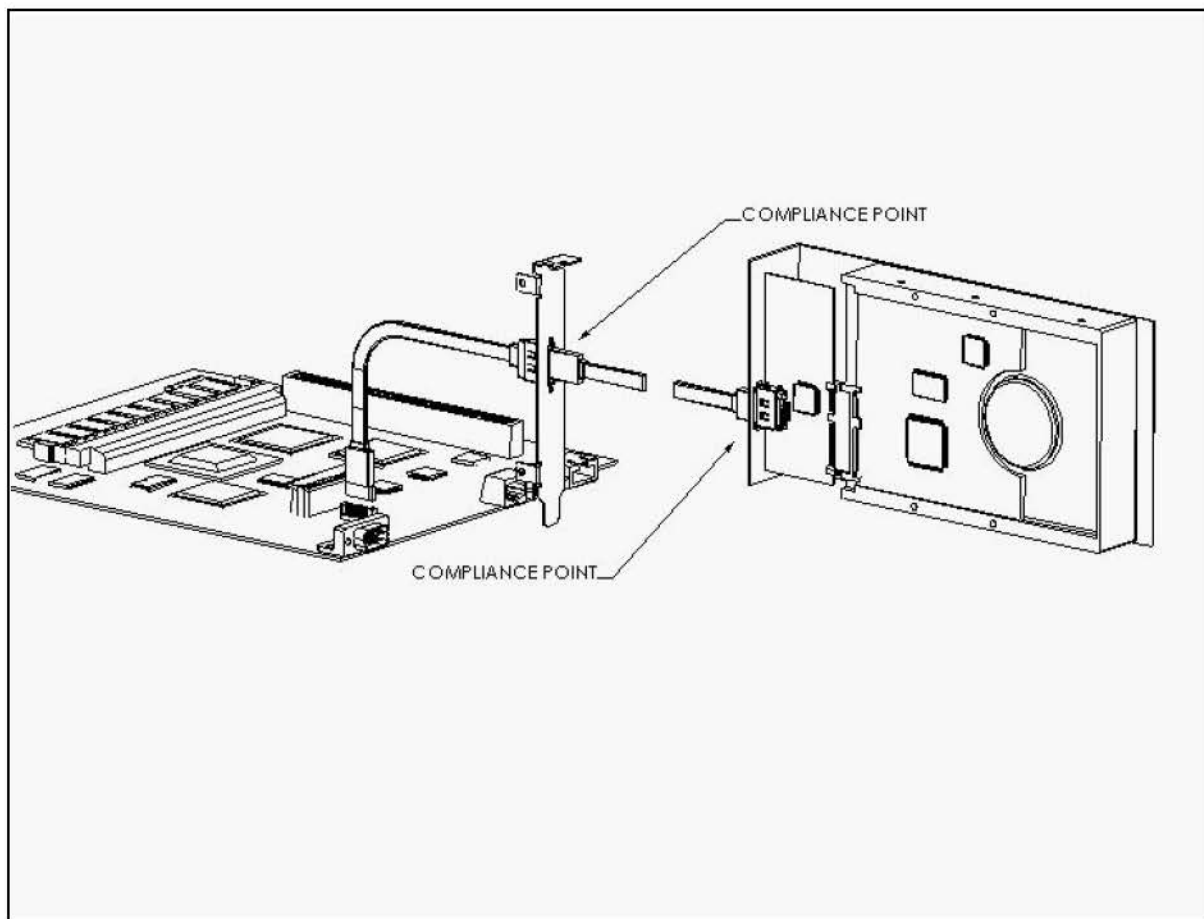


Figure 48 – Usage Model for on-Board Serial ATA Connector with extension cable to external cable to disk

The typical cable length is two meters (six feet); long enough to reach from a floor mounted PC to a drive placed on the desktop. The compliance points for both ends of the external cable shall meet the Gen2m electrical specification.

The use of a standard internal Serial ATA host or device not specifically designed for direct external connection requires a buffer IC as part of the implementation. Note that since Single Lane External Serial ATA cables are a straight through design, (pin to pin), the host and device external connections, using the same external connector, have the same pin one locations but opposite signal definitions. Refer to Table 2 for both host and device connection signal assignments.

6.2.1.1 External Serial ATA Component General Descriptions

Five components are defined in this section to support external Serial ATA.

- ☐ A shielded external cable receptacle for use with shielded (external Serial ATA) cabling.
- ☐ A fully shielded RA PCB mounted SMT plug, (and reversed pin-out version).
- ☐ A fully shielded RA PCB mounted through-hole plug.
- ☐ A fully shielded vertical PCB mounted SMT plug.
- ☐ A fully shielded vertical PCB mounted through-hole plug.

Footprints and recommended panel cutouts are included to encourage greater interoperability from multiple vendors.

The external cable connector is a shielded version of the internal single lane connector defined in section 6, with these basic differences:

- ☐ The External connector has no “L” shaped key, and the guide features are vertically offset and reduced in size. This prevents the use of unshielded internal cables in external applications.
- ☐ To prevent ESD damage, the insertion depth is increased from 5mm to 6.6mm and the contacts are mounted further back in both the receptacle and plug.
- ☐ The retention features are springs built into the shield on both the top and bottom surfaces.

External Serial ATA Connector renderings:

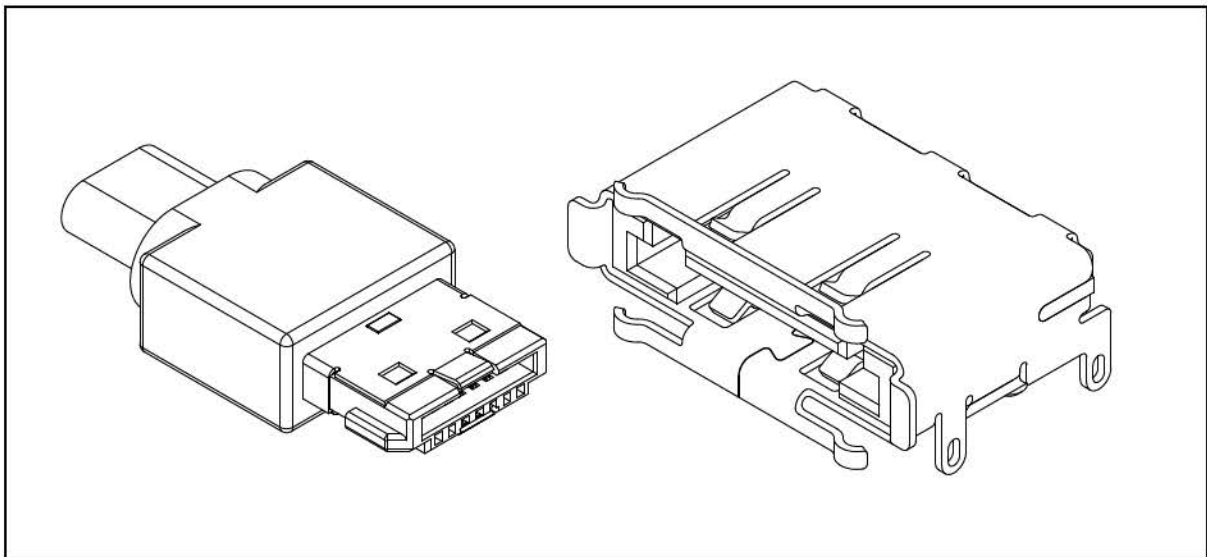


Figure 49 – Renderings of External Serial ATA cable receptacle and right angle plug

6.2.1.1.1 External Serial ATA Connector Mechanical drawings

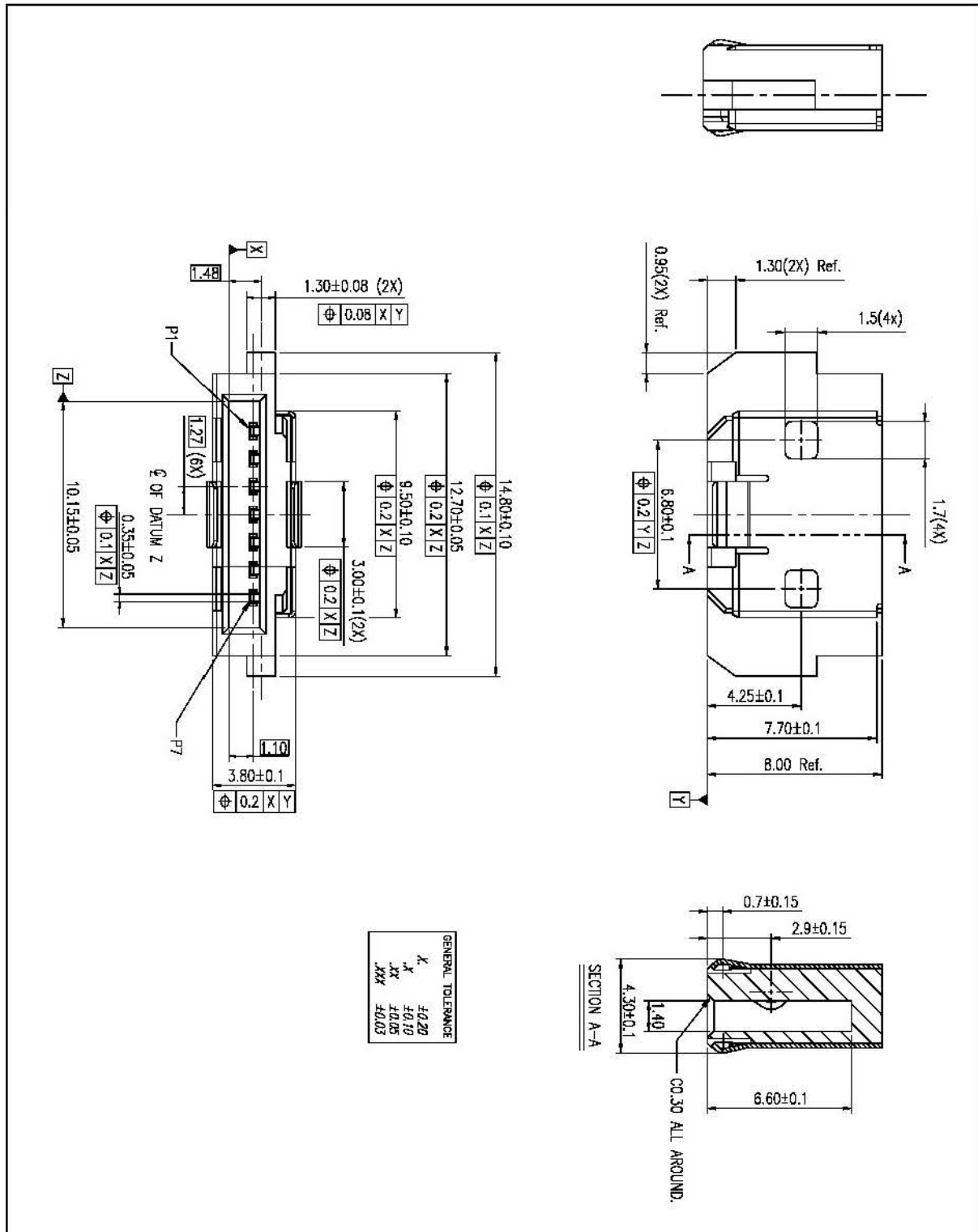


Figure 50 – Mechanical dimensions of External Serial ATA cable receptacle assembly

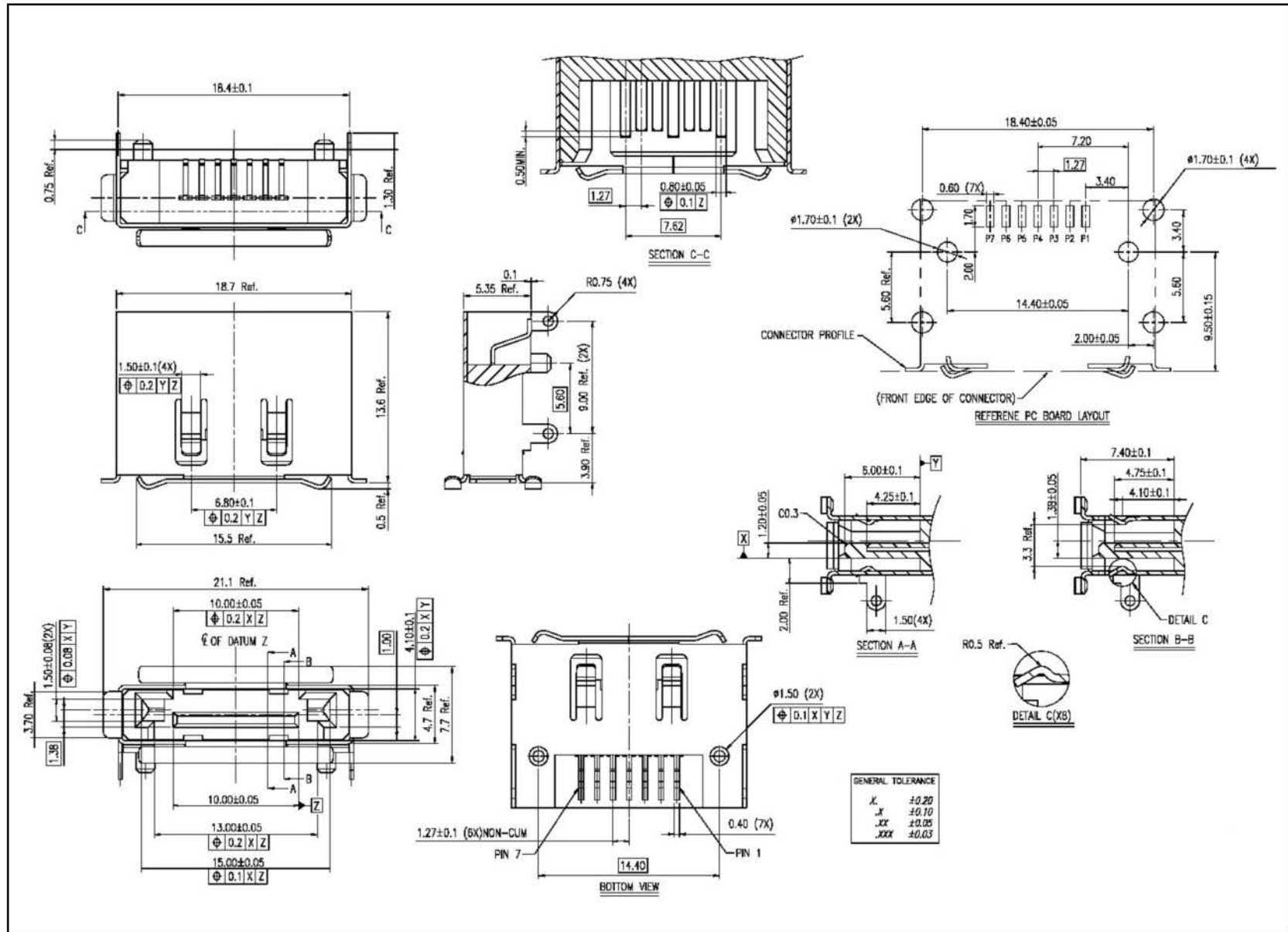


Figure 51 – Mechanical dimensions of External Serial ATA RA SMT plug

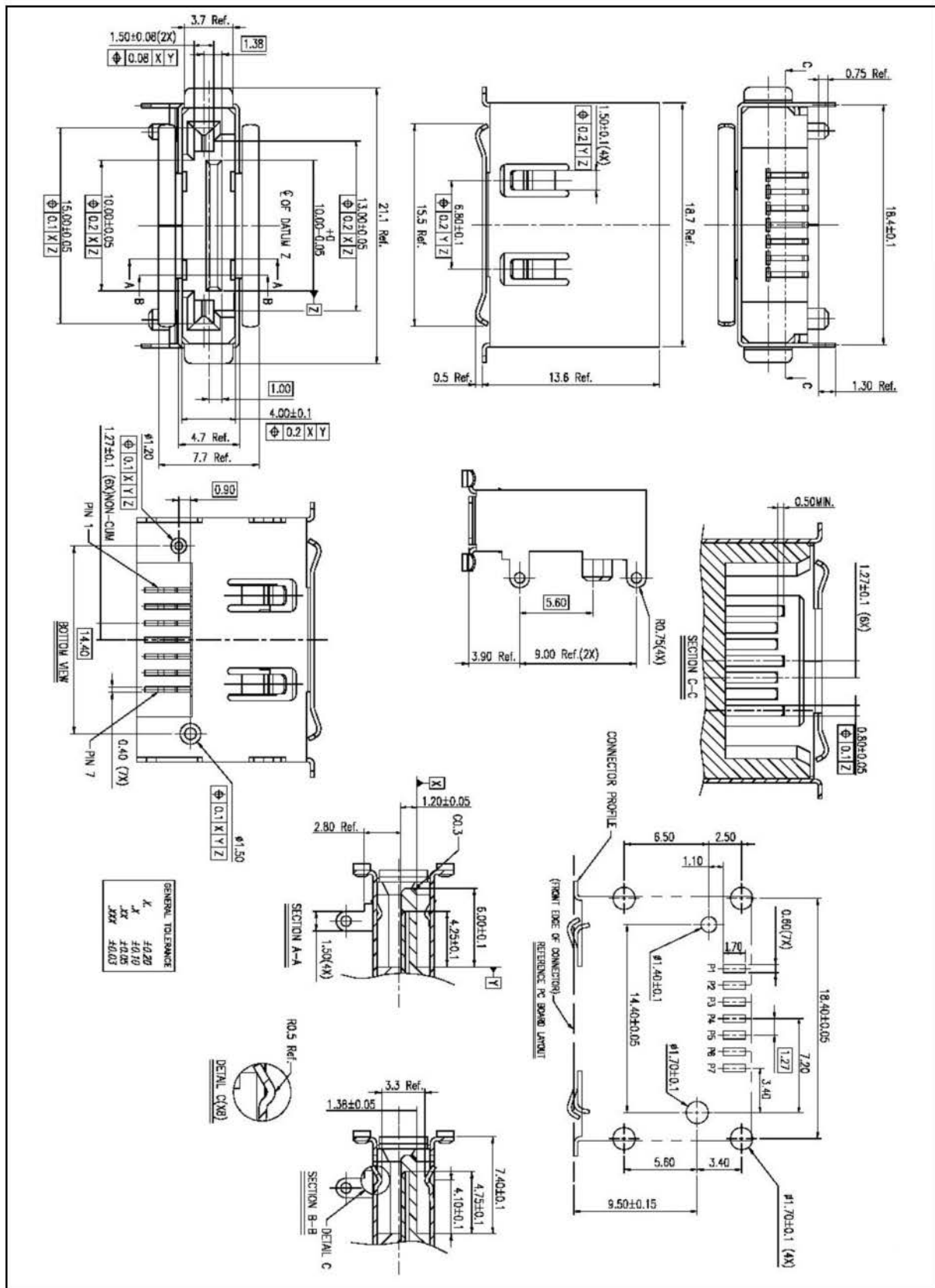


Figure 52 – Mechanical dimensions of External SATA RA SMT plug – Reversed Pin Out



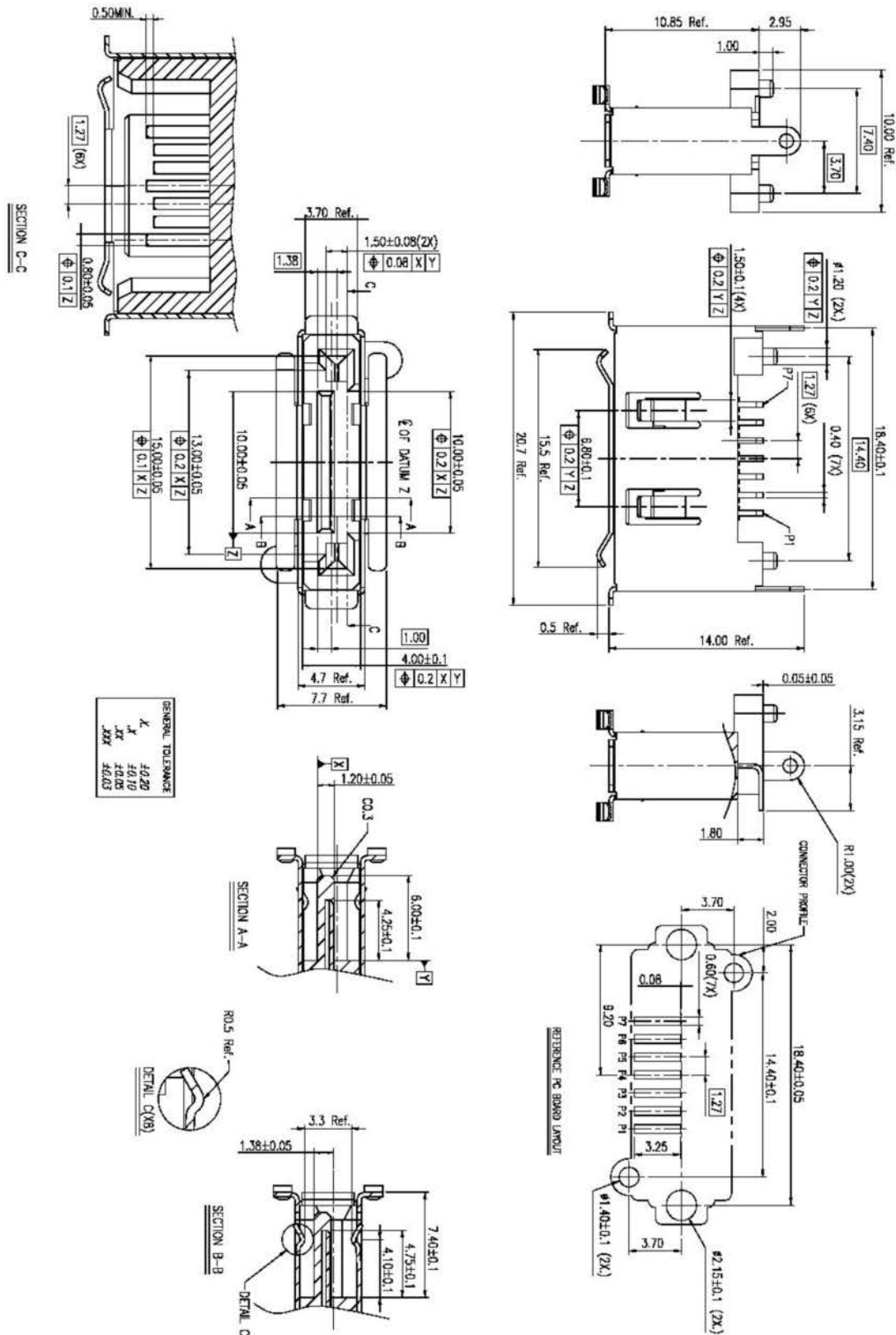


Figure 54 – Mechanical dimensions of External Serial ATA Vertical SMT plug

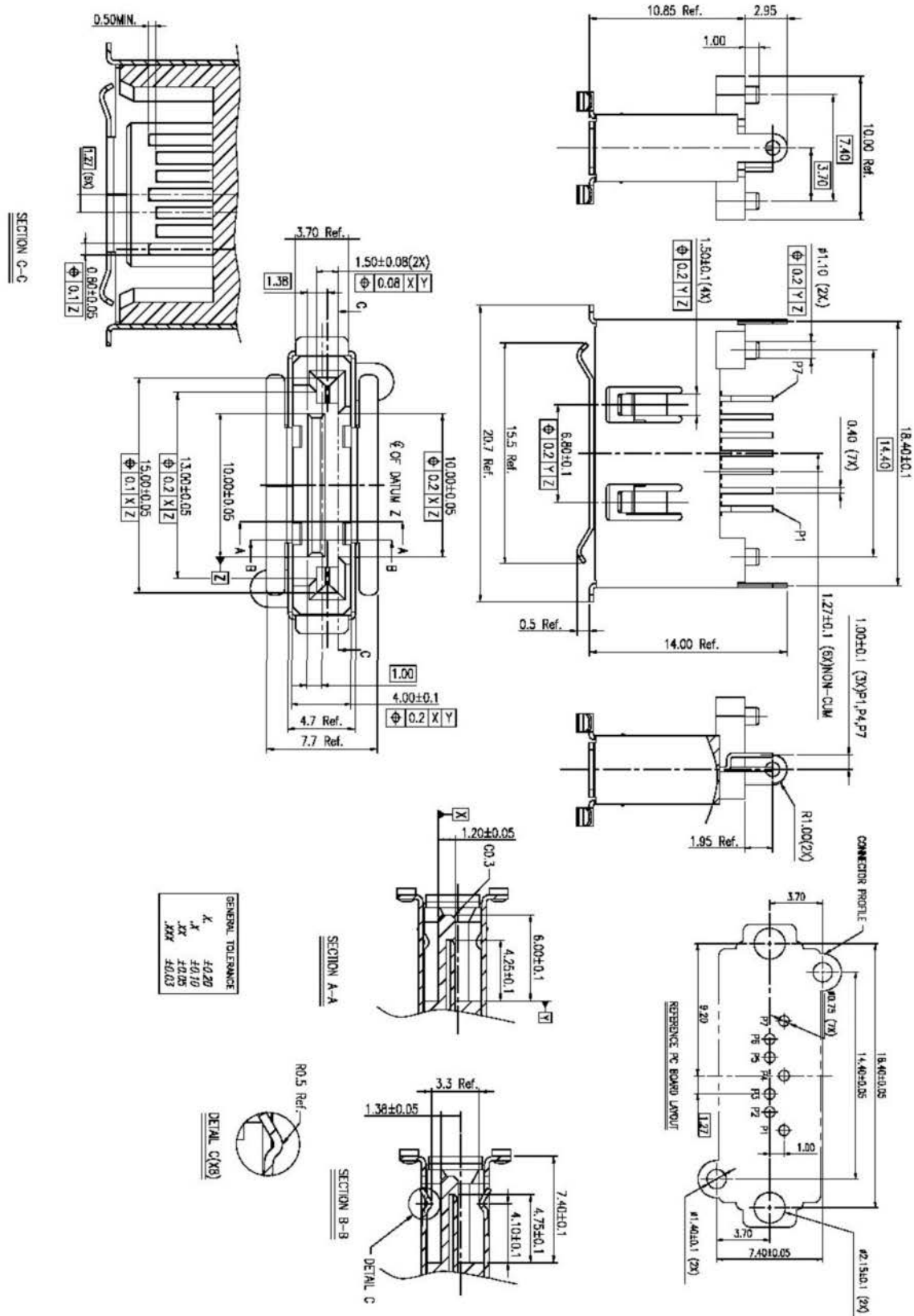


Figure 55 – Mechanical dimensions of External Serial ATA Vertical Through-hole plug

6.2.1.2 External Serial ATA Electrical Requirements

The external cable assembly shall meet the electrical characteristics defined in section 6.3.

The Single Lane External Serial ATA Data Interface Phy electrical performance shall comply with the following:

- ☐ Electrical characteristics defined in section 6.3, Gen1m and/or Gen2m at the shielded external connector compliance points.
- ☐ Support hot plugging and non-powered device attachment.
- ☐ AC coupling is required at the device interface and recommended at the host interface.

6.2.1.3 External Serial ATA Mechanical Requirements

The external connector mechanical performance specifications shall be consistent with the internal single lane connector specifications in section 6, with the following exceptions:

- ☐ Durability shall be 2500 cycles with no exposure of the base metal of the signal contacts.
- ☐ Insertion force shall be a maximum of 40 N.
- ☐ Removal force shall be a minimum of 10 N at the conclusion of the durability test.

6.2.1.4 External Serial ATA Device Direct Connection Requirements

Serial ATA devices may have data interfaces specifically designed for direct connection in the Single Lane External Serial ATA environment without requiring a buffer IC. The data interface of the Single Lane External Serial ATA device shall comply with all external Serial ATA mechanical requirements of section 6.2.1.3. The Phy electrical performance shall comply with the following:

- ☐ Electrical characteristics defined in section 6.3, Gen1m and/or Gen2m at the shielded external connector compliance points.
- ☐ Support hot plugging and non-powered device attachment.
- ☐ AC coupling is required at the device interface and recommended at the host interface.

6.2.2 External Multi Lane

This section defines standard cable assemblies and headers for connecting multiple Serial ATA channels from a RAID host bus adapter to an intelligent backplane in an adjacent JBOD (just a bunch of disks) unit. The RAID HBA and the JBOD units are envisioned as using different power supplies.

This cable/connector set is based on the SFF-8470 specification. The SFF-8470 specification also describes the cable/connector set used by Serial Attached SCSI (SAS).

6.2.2.1 Multi Lane Cable Conformance Criteria

The External Multi Lane cable/connector shall be used with Gen1x and Gen2x signal levels only.

6.2.2.1.1 Electrical Parameters

The External Multi Lane cable assembly shall meet the electrical characteristics defined in section 6.3.

6.2.2.1.2 Mechanical Parameters

Detailed mechanical requirements are specified in SFF-8470, reference type 4X with thumbscrews. The PCI add-in card form factor supports two 4X interfaces.

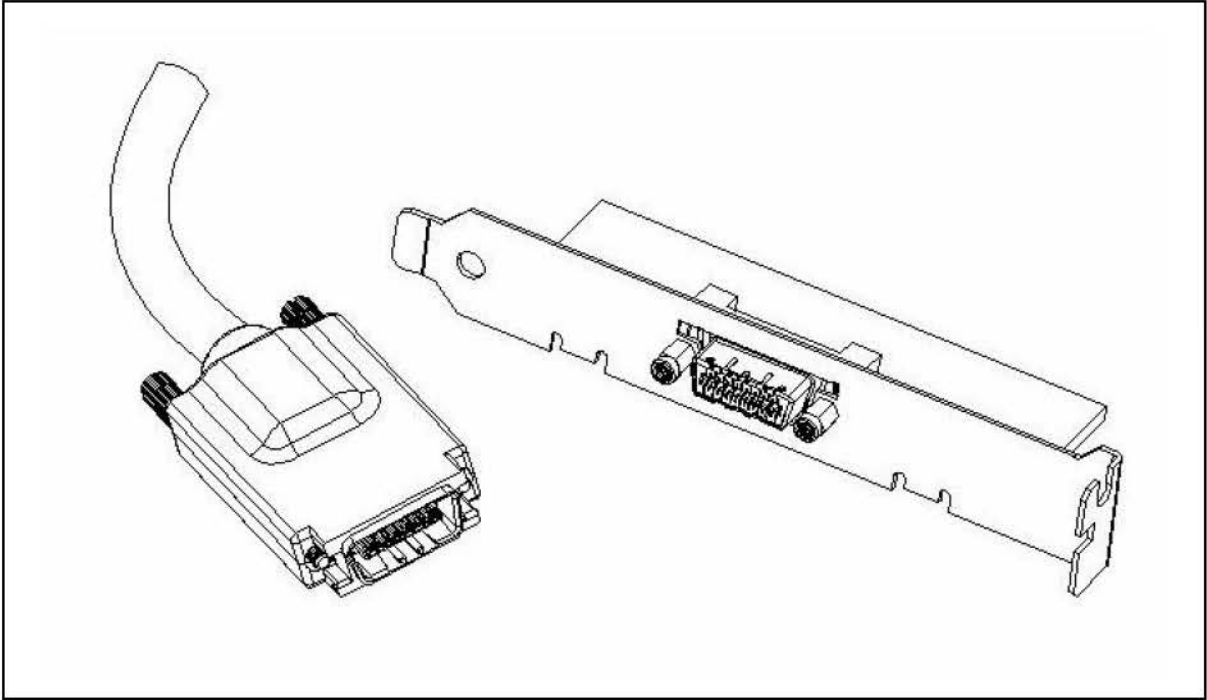


Figure 56 –External Multi Lane cable and connector

6.2.2.2 Keying Requirements

The Serial ATA External Multi Lane cable/connector may include keying features, a variant from the SFF-8470. The Serial ATA key locations are shown in Figure 57.

Optional keying allows connection between Serial ATA HBAs and JBODs but disallows connection to SAS HBAs or JBODs if the SAS units do not have connectors with key slots. If present, the External Multi Lane cable connector blocking key locations shall be 3, 4 and 5 and the corresponding mating connector blocking key locations shall be 1, 2, and 6.

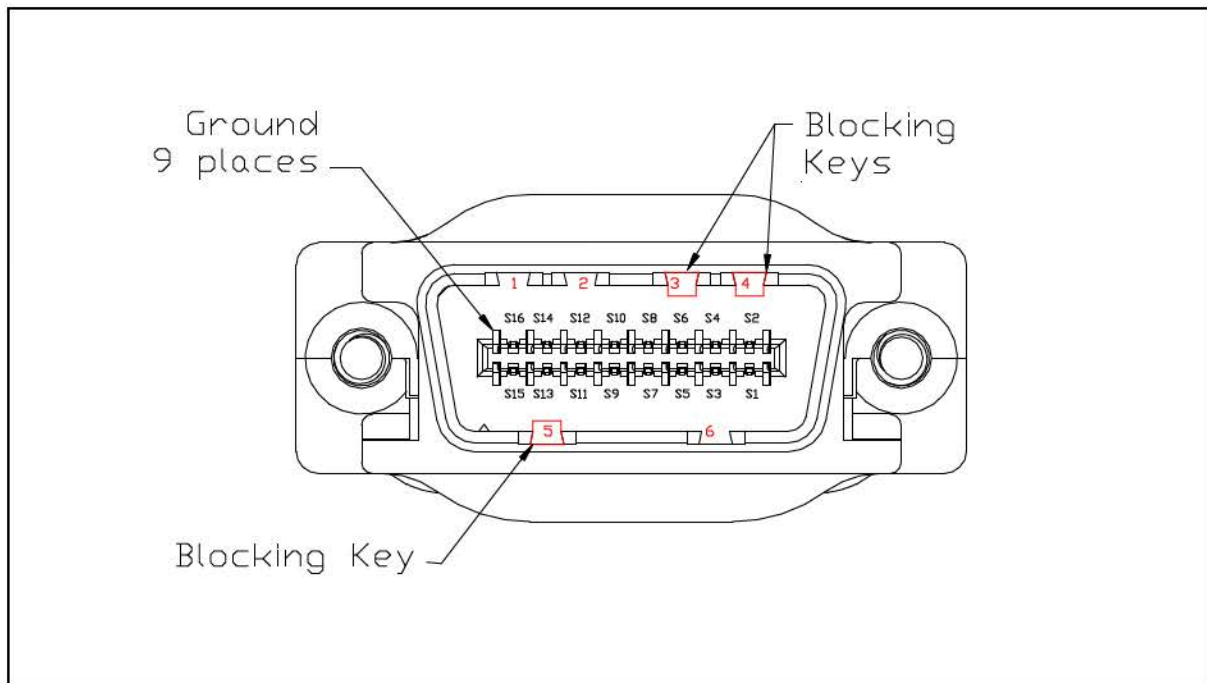


Figure 57 – Multi Lane Cable Connector Blocking Key Locations

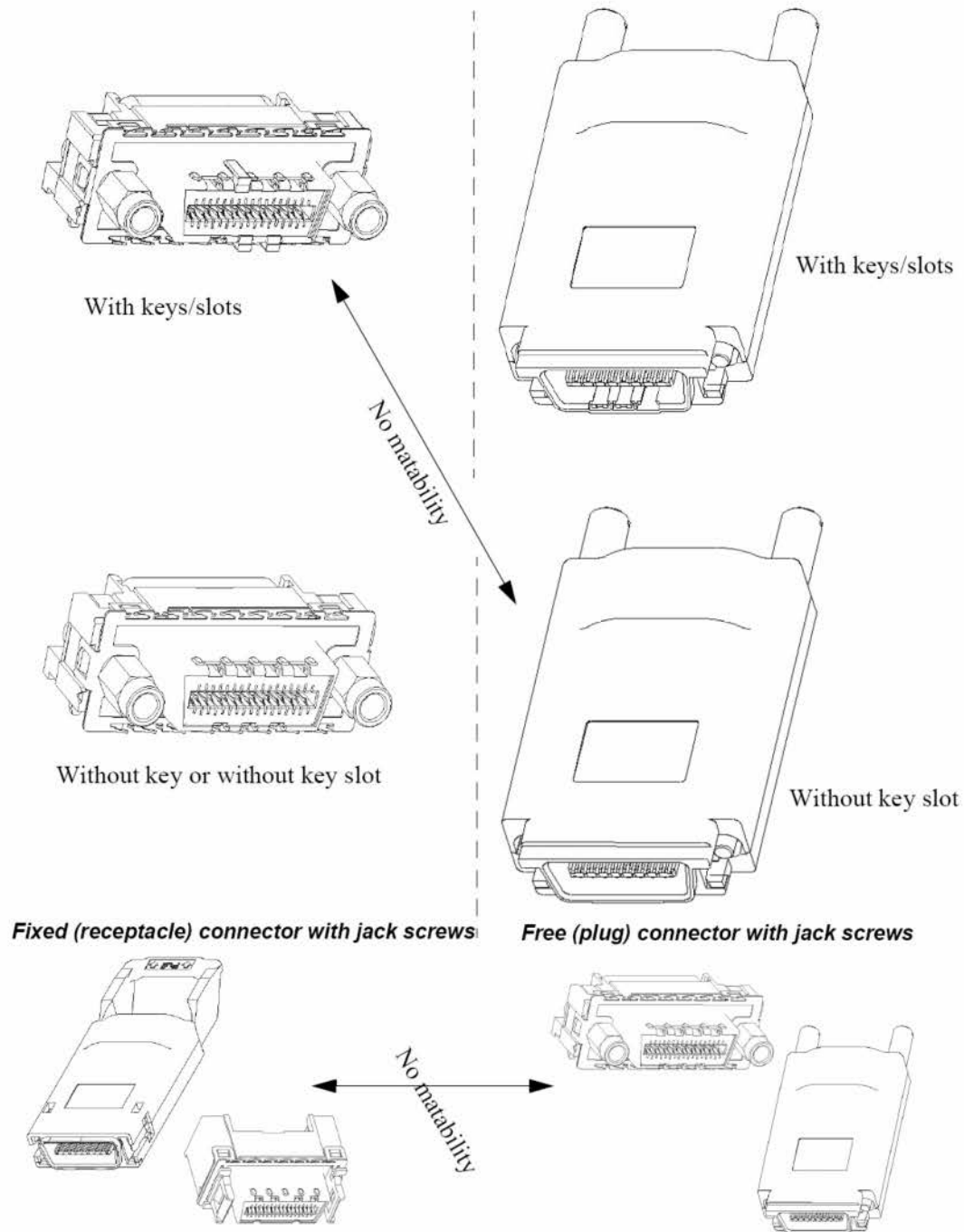


Figure 58 – Plug/Receptacle Keying

6.2.2.3 4 Lane Pin Assignments

Table 9 – Multi Lane Pin Assignments

Signal	Signal pin to use based on number of physical links supported by the cable			
	One	Two	Three	Four
Rx 0+	S1	S1	S1	S1
Rx 0-	S2	S2	S2	S2
Rx 1+	N/C	S3	S3	S3
Rx 1-	N/C	S4	S4	S4
Rx 2+	N/C	N/C	S5	S5
Rx 2-	N/C	N/C	S6	S6
Rx 3+	N/C	N/C	N/C	S7
Rx 3-	N/C	N/C	N/C	S8
Tx 3-	N/C	N/C	N/C	S9
Tx 3+	N/C	N/C	N/C	S10
Tx 2-	N/C	N/C	S11	S11
Tx 2+	N/C	N/C	S12	S12
Tx 1-	N/C	S13	S13	S13
Tx 1+	N/C	S14	S14	S14
Tx 0-	S15	S15	S15	S15
Tx 0+	S16	S16	S16	S16
SIGNAL GROUND	G1-G9			
CHASSIS GROUND	Housing			
Note: N/C: Not connected				

6.3 Cable and Connector Electrical Specifications

The purpose of this section is to specify the electrical characteristics of the cable and connector for Gen1i/Gen2i. The electrical characteristics defined herein describe relevant electrical characteristics required for high-speed signal transmission. Additionally, a test methodology is presented as a tool for characterizing cables, connectors, and PCB signal paths, i.e. microstrip and stripline traces.

6.3.1 Serial ATA Cable

6.3.1.1 Electrical Requirements

The electrical requirements for the internal single lane and Multi Lane Serial ATA cables and connectors (for Gen1i/2i applications) are listed in Table 10. Additionally, the table identifies the procedure number that defines the methodology used to measure the cable and connector for the given parameter. All measurement procedures are located in Table 13.

Table 10 – Internal Cable / Connector Measurement Parameter and Requirements

Parameter	Requirement	Procedure
-----------	-------------	-----------

Mated Connector Differential Impedance	100 Ohms $\pm 15\%$	P1
Cable Absolute Differential Impedance	100 Ohms $\pm 10\%$	P2
Cable Pair Matching Impedance	± 5 Ohms	P3
Common Mode Impedance	25 - 40 Ohms	P4
Maximum Insertion Loss of Cable (10-4500 MHz)	6 dB	P5
Maximum Crosstalk: NEXT (10-4500 MHz)	26 dB loss	P6
Maximum Rise Time (35 ps input)	85 ps	P8
Maximum Inter-Symbol Interference	50 ps	P9
Maximum Intra-Pair Skew	10 ps	P10

The electrical requirements for the External Single Lane cable and connector are defined in Table 11.

Table 11 – External Single Lane Cable / Connector Measurement Parameter and Requirements

Parameter	Requirement	Procedure
Mated Connector Differential Impedance	100 Ohms $\pm 15\%$	P1
Cable Absolute Differential Impedance	100 Ohms $\pm 10\%$	P2
Cable Pair Matching Impedance	± 5 Ohms	P3
Common Mode Impedance	25 - 40 Ohms	P4
Maximum Insertion Loss of Cable (10-4500 MHz)	8 dB	P5
Maximum Crosstalk: NEXT (10-4500 MHz)	26 dB loss	P6
Maximum Rise Time (35 ps input)	150 ps	P8
Maximum Inter-Symbol Interference	50 ps	P9
Maximum Intra-Pair Skew	20 ps	P10

The electrical requirements for the External Multi Lane cable and connector are defined in Table 12.

Table 12 – External Multi Lane Cable / Connector Measurement Parameter and Requirements

Parameter	Requirement	Procedure
Mated Connector Differential Impedance	100 Ohms $\pm 10\%$	P1
Cable Absolute Differential Impedance	100 Ohms $\pm 5\%$	P2
Cable Pair Matching Impedance	± 5 Ohms	P3
Common Mode Impedance	25 Ohms - 40 Ohms	P4
Maximum Insertion Loss of Cable (10-4500 MHz)	16 dB	P5
Maximum Crosstalk: CXT (10-4500 MHz)	30 dB CXT	P7
Maximum Rise Time (35 ps input)	150 ps	P8
Maximum Inter-Symbol Interference	60 ps	P9
Maximum Intra-Pair Skew	20 ps	P10

Note: All External Multi Lane signaling is at Gen1x or Gen2x levels.

6.3.2 Cable/Connector Test Methodology

6.3.2.1 Test Equipment

The following list identifies the type and performance of suggested equipment to perform the characterization procedures outlined in Table 13 and Table 14.

- ☐ High Bandwidth Sampling Oscilloscope
- ☐ TDR Module – < 35 ps Edge Rate Step Response
- ☐ Vector Network Analyzer – 5 GHz BW
 - Suggested 4-Port or equivalent capability
- ☐ High Performance Coaxial Cables – ≥ 20 GHz BW

6.3.2.2 Test and Measurement Conditions

Unless otherwise specified, all tests and measurements shall be performed under the following conditions:

- ☐ Cable/Connector Mated
- ☐ Temperature: 15° to 35° C
- ☐ Relative Humidity: 20% to 80%
- ☐ Atmospheric Pressure: 650 mm to 800 mm of Hg

6.3.2.3 Test Fixture Considerations

Characterization of the cable/connector configuration requires an interface between the unit under test (UUT) and the test equipment and is commonly referred to as the test fixture. A primary objective in using a test fixture is to eliminate, as much as possible, the adverse signal integrity effects of the PCB. The following guidelines should be followed when defining the test fixture. Consider the following:

- ☐ The test fixture should use differential microstrip traces (100 ± 5 Ohms) over a ground plane (single ended 50 ± 2.5 Ohms).
- ☐ Open or shorted traces with the same length as the input signal traces shall be provided to enable the following:
 - Establish system input rise time
 - Synchronize pulses
 - Establish reference plane
- ☐ Traces for crosstalk measurements should diverge from each other.
- ☐ Provisions for attenuation reference measurement should also be provided.

6.3.2.4 Test Definition / Methodology

There are a number of steps within the test procedures used in preparation of making a measurement and are referred to as common procedures. They consist of calibration, de-skewing, establishing a reference plane, and establishing a rise time reference trace.

Prior to performing any procedures or gathering data, ensure that the test equipment has been properly calibrated.

The methodology to complete each of the common procedures is outlined in Table 13.

Table 13 – Common Interconnect Measurement Procedure Methodologies

C1	Minimizing Skew between V+ and V-, Diff Signals
	<ol style="list-style-type: none"> 1. Define Differential Channel Stimulus <ol style="list-style-type: none"> a. Channel 1/3 positive edge step response (V^+) b. Channel 2/4 negative edge step response (V^-) 2. Differential Response – Identify the differential signal (V_{diff}) as a scope response, e.g. Use math function to obtain $V_{diff} = V^+ - V^-$ (CH1-CH2 or CH3-CH4) 3. Minimize skew between the V+ (positive) and V- (negative) edges by adjusting either the V+ (CH1/3) or V- (CH2/4) edge forward or backward in time until both edges align to within 1ps.
C2	Establishing a reference plane at the connector
	<ol style="list-style-type: none"> 1. Follow calibration procedures outlined in the firmware of the oscilloscope. 2. Select the define reference plane option within the scope firmware to establish a reference plane at the input of the test fixture. 3. When establishing a new reference plane, use precision 50 Ohm loads or precision air lines that are terminated with 50 Ohm loads for the test fixture.
C3	Establishing the rise time reference trace
	<ol style="list-style-type: none"> 1. Configure the TDR modules to generate a differential step impulse response and identify the differential rising edge of the trace. 2. Identify the high and low voltage values of the impulse response. 3. Identify the 20% and 80% voltage levels and verify that the rise time of the step impulse is between 25 ps and 35 ps. There are two methods for adjusting the step impulse response to be within the desired range: <ol style="list-style-type: none"> a. The system rise time is to be set via equipment filtering techniques. The filter programmed equals $\sqrt{t_{r(observable)}^2 - t_{r(stimulus)}^2}$ b. Capture the measurement data and perform a post processing step to filter the captured data to the desired rise time within a waveform viewer or TDR SW application. 4. Once the correct rise time has been established, verify the rise time using the reference traces on the PCB fixture.

The test methodologies and procedures outlined in Table 14 refer to the common procedures described in Table 13. The actual specification requirement values for each of these methodologies are listed in section 6.3.1.1.

Table 14 – Interconnect Test Methodologies / Procedures

P1	Mated Connector Differential Impedance
	<ol style="list-style-type: none"> 1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3. 2. Measure and record the maximum and minimum values of the near end connector differential impedance.
P2	Cable Absolute Differential Impedance
	<ol style="list-style-type: none"> 1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3. 2. Measure and record maximum and minimum cable differential impedance values in the first 500 ps of cable response following any vestige of the connector response.
P3	Cable Pair Matching
	<ol style="list-style-type: none"> 1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3. 2. Measure and record the single-ended cable impedance of each cable within a pair, e.g. Z_{L1}, Z_{L2}. 3. Measure and record the maximum and minimum cable impedance values in the first 500ps of cable response following any vestige of the connector response, e.g. Z_{L1-max}, Z_{L1-min} and Z_{L2-max}, Z_{L2-min}. 4. The desired parameter equals $Z_{max} = Z_{L1-max} - Z_{L2-max}$ and $Z_{min} = Z_{L1-min} - Z_{L2-min}$.

P4	Common Mode Impedance
	<ol style="list-style-type: none"> 1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3. 2. Select the negative edge step response channel to be a positive edge step response such that both channels generate a positive edge step response. 3. Measure the even mode impedance of the first step generator. 4. Perform a math function on the waveform to divide the even mode impedance response by 2. The result is the Common Mode Impedance. 5. Make the same measurement and math calculation of the second step generator. 6. The Common Mode Impedance for each step generator shall meet the requirement.
P5	Insertion Loss
	<ol style="list-style-type: none"> 1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1 and C2. 2. Measure and store the insertion loss (IL) of the fixturing using the IL reference traces provided on the board over a frequency range of 10 to 4500 MHz, e.g. IL_{fixture}. 3. Measure and record the IL of the sample, which includes fixturing IL, over a frequency range of 10 to 4500 MHz, e.g. IL_{system}. 4. The insertion loss of the sample is calculated by $IL_{\text{sample}} = IL_{\text{system}} - IL_{\text{fixture}}$.

P6	Differential to Differential Crosstalk: NEXT
	<ol style="list-style-type: none">1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3.2. Terminate the far ends of the reference trace with characteristic impedance loads of 50 Ohms.3. Measure and record the system and fixturing crosstalk. It is defined as the noise floor, e.g. V_{noise}.4. Terminate the far ends of the drive and listen lines with characteristic impedance loads of 50 Ohms.5. Connect the source to the drive pair and the receiver to the near-end of the listen pair.6. Measure the NEXT over a frequency range of 10 to 4500 MHz, e.g. V_{NEXT}.7. Verify that the sample crosstalk is out of the noise floor, e.g. $V_{NEXT} > V_{noise}$.

P7	Multi Lane (Multi Disturber) Differential Crosstalk: ML-CXT
	<ol style="list-style-type: none"> 1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3. 2. Terminate the far ends of the reference trace with characteristic impedance loads of 50 Ohms. 3. Measure and record the system and fixturing crosstalk. It is defined as the noise floor, e.g. V_{noise}. 4. Terminate the far ends of the drive and listen lines with characteristic impedance loads of 50 Ohms. 5. Connect the source to the drive pair and the receiver to the near-end of the listen pair. 6. Measure the CXT over a frequency range of 10 to 4500 MHz, e.g. V_{CXT}. 7. Verify that the sample crosstalk is out of the noise floor, e.g. $V_{CXT} > V_{noise}$. 8. $MLCXT(f) = -20 \cdot \log \left(\sum_{A=1}^{71} 10^{-V_{CXT}(f)_I/20} \right)$ <p>where:</p> <p>$MLCXT(f)$ is the Multi Lane Cable assembly Crosstalk at frequency f observed on any given receive lane.</p> <p>$V_{CXT}(f)_A$ is the relative crosstalk at frequency f between the receiver/victim and any combination of aggressor A^1, which exhibits less than 40 dB of isolation.</p> <p>f is the frequency ranging from 10 MHz to 4.5 GHz</p> <p>A is the 1,2 – 7 (receiver/victim to aggressor¹ pair combinations)</p> <p>1. Aggressor: Any lane identified as a Tx (input) shall be considered as a potential aggressor. This includes near end and far end Tx lane</p> <p>Note:</p> <p>MLCXT summation calculations accounts for any aggressor¹ relative to a receiver/victim pair which exhibit less than 40 dB of isolation.</p>

P8	Differential Rise Time
	<ol style="list-style-type: none"> 1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3. 2. Connect the TDR step impulse response generators to the near end of the signal path under test. 3. Record the output rise time at the far end of the signal path under test.
P9	Inter-Symbol Interference
	<ol style="list-style-type: none"> 1. Observe and record the cable fixtures intrinsic RJ and DJ for this setup through a 2X cal/reference trace which should be present on all SMA to cable break-out boards. 2. Connect a differential pattern source at the input of the test fixture. Generate a lone bit pattern at 3.0 Gbps through the fixture. The lone bit pattern more accurately emphasizes ISI. 3. Using a JMD, evaluate the Deterministic Jitter (DJ) introduced at the end of the cable. Bear in mind the deterministic contribution from test fixtures and stimulus systems. As incident (test system induced) DJ cannot be de-convolved from the end results, it's critical one use a high quality (low jitter) fixture and stimulus system when performing this measurement.
P10	Intra-Pair Skew
	<ol style="list-style-type: none"> 1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3. 2. Measure the propagation delay of each single ended signal within a pair at the mid point of the voltage swing, e.g. $t_{\text{delay}} = V_{\text{mid}+} - V_{\text{mid}-}$ where $V_{\text{mid}} = \frac{V_{\text{high}} - V_{\text{low}}}{2}$.

6.4 Power Segment Pin P11 Definition (Optional)

Pin P11 of the power segment of the device connector may be used by the device to provide the host with an activity indication and it may be used by the host to indicate whether staggered spin-up should be used. To accomplish both of these goals, pin P11 acts as an input from the host to the device prior to PHYRDY for staggered spin-up control and then acts as an output from the device to the host after PHYRDY for activity indication. The activity indication provided by pin P11 is primarily for use in backplane applications. Reference section 13.12 for information on activity LED generation for desktop applications.

A device may optionally support activity indication via pin P11, staggered spin-up control via pin P11, or both features. If neither feature is supported, then pin P11 is a no-connect at the device as specified in Table 2.

A host may only support one pin P11 feature, either receiving activity indication or staggered spin-up disable control. If a host supports receiving activity indication via pin P11, then the host

shall not use pin P11 to disable staggered spin-up. If a host does not support receiving activity indication via pin P11, then the host may use pin P11 to disable staggered spin-up.

6.4.1 Device Activity Signal

6.4.1.1 Electrical Definition

The signal the device provides for activity indication is a low-voltage low-current driver intended for efficient integration into current and future IC manufacturing processes. The signal is not suitable for directly driving an LED and shall first be buffered using a circuit external to the device before driving an LED.

The activity signal is based on an open-collector or open-drain active-low driver. The device shall tolerate the activity signal being shorted to ground. The device shall tolerate a no-connect floating activity signal.

Table 15 and Table 16 define the electrical parameters and requirements for the activity signal for both the device and the host. Figure 59 is an example of an activity signal implementation for illustrative purposes. Note that the host cannot rely on a particular resistor pull-up value on the device side, nor can the device rely on particular host resistor values. No direct support for wired OR signals from multiple devices is accommodated. Host implementations that produce a single activity signal by combining multiple device inputs should buffer the signals prior to combining them.

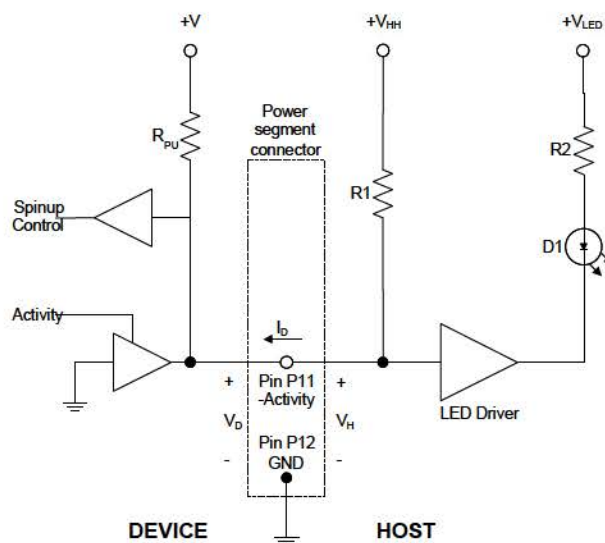


Figure 59 – Example activity signal electrical block diagram

All voltage references in Table 15 and Table 16 are to ground pin P12 on the device connector. All voltages and currents in Table 15 and Table 16 are measured at pin P11 on the device connector.

Table 15 – Power segment pin P11 activity signal electrical parameters

Parameter	Min Value	Max Value	Description & Conditions
V_{DIn}	-0.5 V	2.1 V	Tolerated input voltage

V_{DAct}	0 mV	225 mV	Device output voltage when driving low under the condition I_D less than or equal to 300 μ A
V_{DInact}	-0.1 V	3.3 V	Device output voltage when not driving low
I_{DInact}	-10 μ A	100 μ A	Device leakage current when not driven

Table 16 – Host activity signal electrical parameters

Parameter	Min Value	Max Value	Description & Conditions
V_{HIIn}	-0.5 V	3.3 V	Tolerated input voltage
V_{HH}		2.1 V	Host voltage presented to device when device not driving signal low. (Also see section 6.4.2 for staggered spin-up control).
V_{HL}	-0.1 V		Minimum allowable host voltage that may be presented to the device.
I_{HAct}		300 μ A	Host current delivered to device when device driving signal low. Value specified at V_{DAct} voltage of 0 V.

6.4.1.2 LED Driver Circuit (Informative)

The LED driver circuit provided by the host to drive an activity LED is vendor specific. Figure 60 illustrates two conceptual driver circuits that satisfy the electrical requirements and provide a signal suitable for driving an activity LED. Variations in the driver circuits can be employed to drive the LED when active or to drive the LED when the device is inactive through the use of an inverting or non-inverting buffering arrangement.

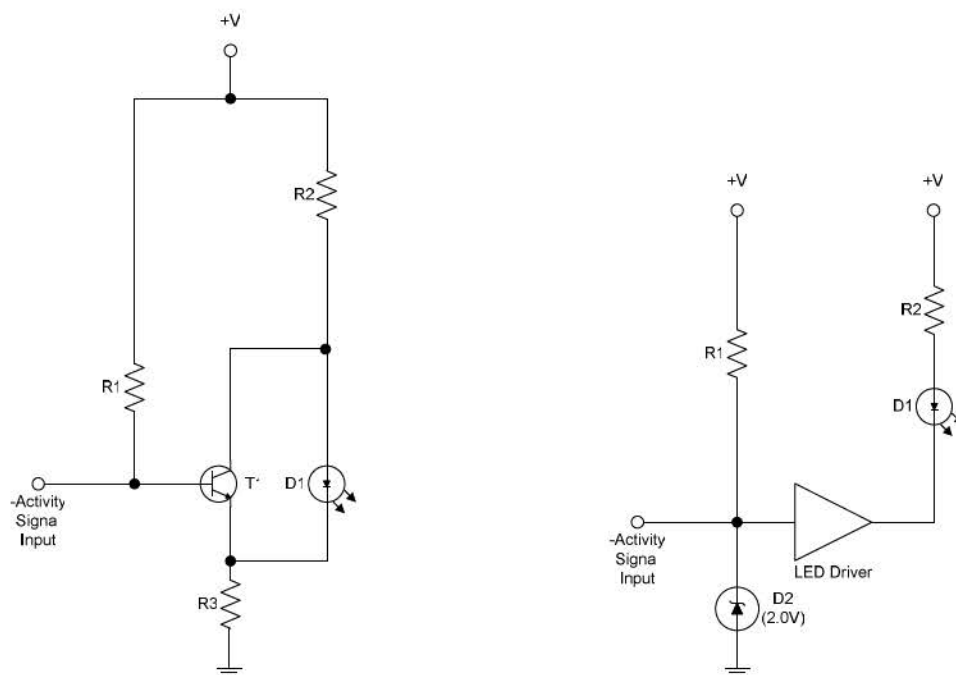


Figure 60 – Example host LED driver circuits

6.4.1.3 Functional Definition

Table 17 defines the two activity signal states and the corresponding conditions.

Table 17 – Activity signal functional states

State	Condition
Signal asserted (driven low)	Command(s) outstanding ¹
Signal de-asserted (high impedance)	All other conditions
Notes: 1. Devices may omit asserting the activity signal for commands that do not access the media and have an expected service time too short to allow visual perception of the signal. Command(s) outstanding does not include the software reset, power-on reset, or COMRESET command protocols. As a consequence, pin P11 shall not be driven low by the device prior to return of the reset signature for the reset command protocols. This is behaviorally different than the parallel ATA DASP- signal.	

6.4.2 Staggered Spin-up Disable Control

6.4.2.1 Electrical and Functional Definition

The staggered spin-up feature is defined in section 13.8. Devices may optionally provide support to disable staggered spin-up through pin P11 of the power segment connector. The staggered spin-up disable control is an active asserted low host signal.

Before the device spins up its media, devices that support staggered spin-up disable control shall detect whether pin P11 is asserted low by the host. If pin P11 is asserted low the device shall disable staggered spin-up and immediately initiate media spin-up. If pin P11 is not connected in the host (floating), devices that support staggered spin-up disable through pin P11 shall enable staggered spin-up. Table 18 defines the electrical signal requirements for the device detection of staggered spin-up disable.

Table 18 – Host staggered spin-up control electrical requirements

Parameter	Min Value	Max Value	Description & Conditions
V _{HEnb}	1.8 V	V _{HHmax}	Host voltage presented to device to not disable staggered spin-up in devices that support staggered spin-up control. Value specified for all allowable I _{DInact} leakage currents.
V _{HDis}	-0.1 V	225 mV	Host voltage presented to device to disable staggered spin-up in devices that support staggered spin-up control. Value specified for all allowable I _{DInact} leakage currents.

The staggered spin-up control indication provided by a host or storage subsystem shall be static and shall not be changed while power is applied. If the signal is pulled low by the host during the staggered spin-up disable detection period, the signal shall remain low. Devices shall disable the activity signal if the host signals staggered spin-up disable.

If supported, the device shall sample the staggered spin-up disable condition after the time DC power is applied and before PHYRDY is asserted.

6.4.2.2 Staggered Spin-up Disable Circuit (Informative)

The host circuit for signaling staggered spin-up disable by pulling pin P11 low is vendor specific. Figure 61 illustrates a conceptual host circuit that would satisfy the electrical requirements for signaling staggered spin-up disable. It is permissible for the host to statically short pin P11 to ground or for the host to actively drive the signal low.

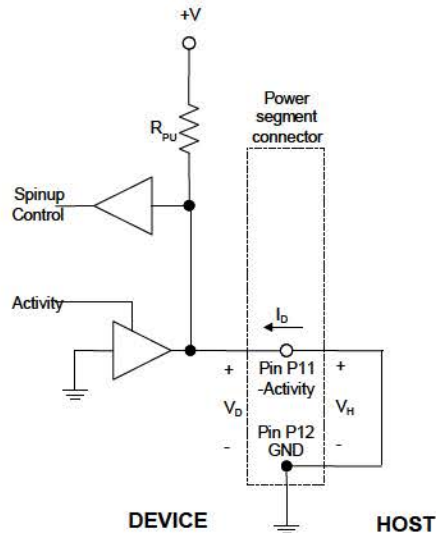


Figure 61 – Example host circuit for signaling staggered spin-up disable

6.5 Precharge and Device Presence Detection

For a storage subsystem, hot-plug capability is required as well as the ability to seamlessly handle presence detection in those cases where the storage subsystem can remove power to individual receptacles.

6.5.1 Device Requirements

In order to accommodate hot-insertion with the use of the precharge feature as well as a means for presence detection, Serial ATA devices shall bus together all power delivery pins for each supply voltage.

6.5.2 Receptacle Precharge (Informative)

The Serial ATA device connector has been specifically designed to accommodate a robust hot-plug capability. One feature of the device connector is the ability for receptacles to limit the instantaneous inrush current through the use of a precharge scheme. This scheme relies on one power delivery contact for each voltage being longer than the remaining contacts in order to allow power to be delivered through this longer contact through a current limiting device. Figure 62 illustrates one hot-plug power delivery scheme that utilizes the precharge connector feature.

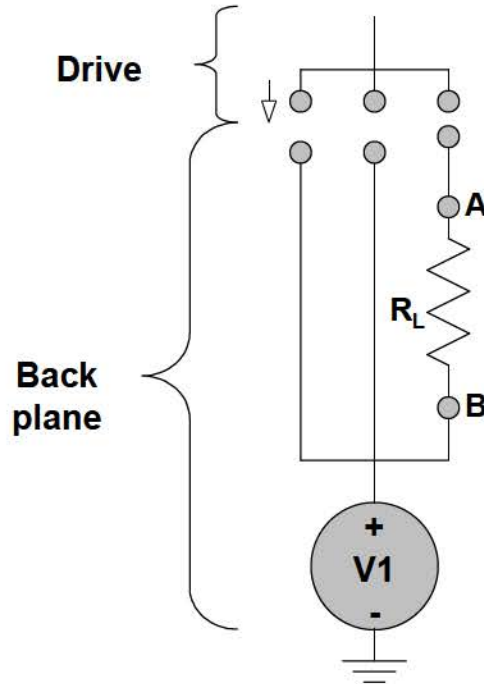


Figure 62 – Typical precharge configuration

All burden for limiting the inrush current for a newly inserted device is borne by the receptacle/backplane. The exact current limiting resistor size appropriate for a particular backplane solution depends on the details of the implementation. A few of the variables to be considered in sizing the current limiting resistor include:

- Device insertion velocity
- Effective capacitance of the inserted device
- Contact current carrying capacity

A survey of these variables by the group indicated that for one particular application, the maximum insertion velocity yielded a contact precharge time of approximately 3 ms. A poll of several disk drive vendors indicated a typical effective capacitance for disk drive devices of approximately 20 uF. For illustrative purposes, these values are presumed in an example scenario for estimating the precharge resistor value. The amount of time required to charge the effective capacitance to 90% of full charge is roughly $2.2 \cdot R \cdot C$. Thus:

$$T = 2.2 \cdot R \cdot C_{EQ}$$

$$R = \frac{T}{2.2 \cdot C_{EQ}}$$

For the example charging time of 3 ms and an effective capacitance of 20 uF, the resultant precharge resistor value is approximately:

$$R = \frac{3ms}{2.2 \cdot 20uF} = 68\Omega$$

Because the Serial ATA power conductors can support currents up to 1.5 A, the computed resistor size can be substantially reduced without adverse consequence in order to reduce the sensitivity to the device's actual effective capacitance. For the 12 V supply rail, the resistor may be as small as 8 Ohms and still not exceed the current carrying capacity of the precharge contact.

Depending on the details of the actual enclosure subsystem design, typical precharge resistor values for the illustrative example scenario may therefore be in the range of 10-20 Ohms.

6.5.3 Presence Detection (Informative)

Presence detection relies on the device signaling the host using the OOB sequence to indicate its presence after a hot insertion. This approach presumes the device is inserted into a hot receptacle and also presumes the device inserted is not malfunctioning. In a storage subsystem, these assumptions may not be appropriate since such storage solutions may have the ability to unpower individual device receptacles in order to make device insertion/removal safer. Thus, a means for determining device presence in a receptacle that does not have power applied and without the device having to function is desired.

One possible device presence detection mechanism utilizes the precharge circuit outlined in section 6.5.2. The basic approach is to determine presence of a device by measuring the impedance between points A and B in the diagram. Because devices bus together their respective power delivery contacts, the impedance between points A and B in the diagram is R_L with no device present and is effectively zero with a device inserted in the receptacle.

Figure 63 illustrates one possible circuit for handling device presence detect with the receptacle either powered or unpowered. The example circuit is subject to tolerance buildup of the selected components and the supply voltages, and are only presented as conceptual examples.

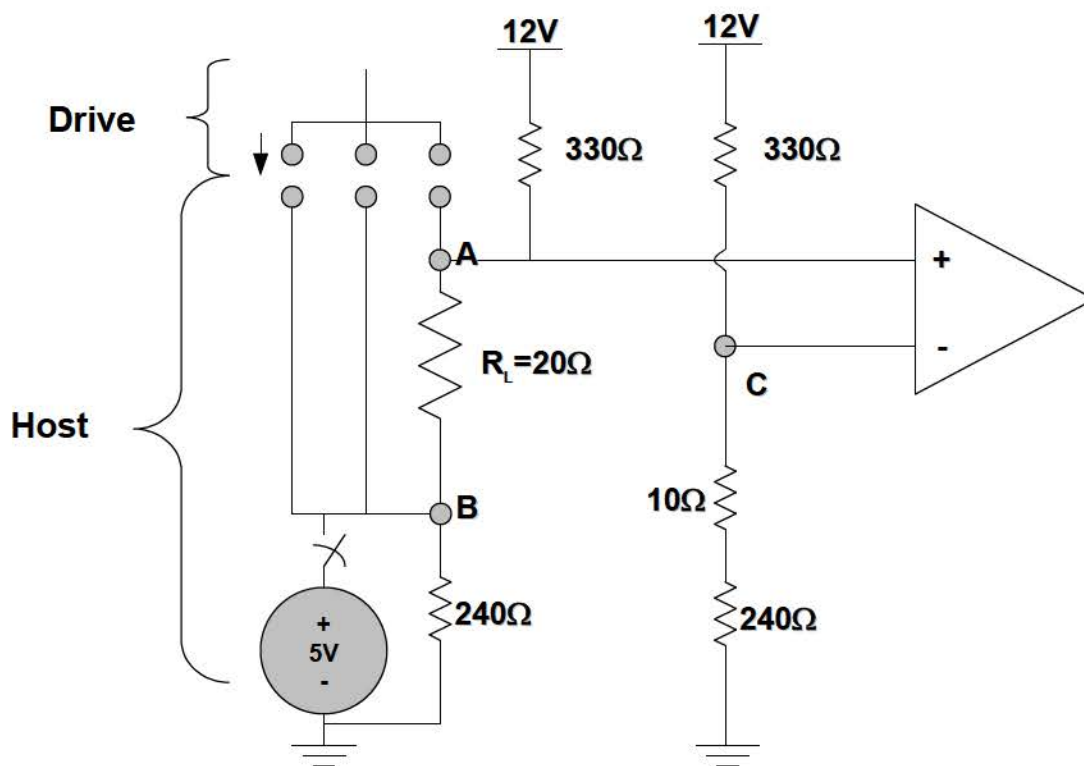


Figure 63 – Example presence detection implementation

Table 19 – Comparator voltages for alternate example presence detection circuit

	Receptacle Powered		Receptacle unpowered	
Device not present	$V_A = 5.40\text{ V}$	$V_C = 5.17\text{ V}$	$V_A = 5.29\text{ V}$	$V_C = 5.17\text{ V}$
Device present	$V_A = 5.0\text{ V}$	$V_C = 5.17\text{ V}$	$*V_A = 5.05\text{ V}$	$V_C = 5.17\text{ V}$

*If the inserted device provides a finite impedance to ground, then V_A should be lower than this value increasing the voltage differential further and increasing the margins.

7 Physical layer

This section describes the physical layer of Serial ATA. The information that is provided is comprised of two types – informative and normative. Unless otherwise described, the information should be considered normative in nature and is included in this document as a necessary requirement in order to properly allow a piece of equipment to attach to another piece of equipment. The normative information is deliberately structured to constrain and define areas only to the degree that is required for compatibility. The information that is provided and marked informative is provided only to help the reader better understand the normative sections and should be taken as examples only. Exact implementations may vary.

7.1 Descriptions of Phy Electrical Specifications

The following terms have been developed for the various Electrical Specifications:

- **Gen1i:** Generation 1 Electrical Specifications: These are the 1.5 Gbps electrical specifications for internal host to device applications.
- **Gen1m:** Generation 1 Electrical Specifications for Short Backplane and External Desktop Applications: These are the 1.5 Gbps electrical specifications aimed at short 1.5 Gbps internal backplane applications and the External Desktop Application. These include only modified receiver Differential input specifications. All other electrical specifications relating to Gen1m compliance points are identical to Gen1i specifications. This specification is for these limited applications only and is not intended for any other system topology.
- **Gen2i:** Generation 2 Electrical Specifications: These are 3.0 Gbps electrical specifications for internal host to device applications.
- **Gen2m:** Generation 2 Electrical Specifications for Short Backplane and External Desktop Applications: These are 3.0 Gbps electrical specifications aimed only at these applications. These include only modified receiver differential input specifications. All other electrical specifications relating to Gen2m compliance points are identical to Gen2i specifications. This specification is for this limited application only and is not intended for any other system topology.
- **Gen1x:** Extended Length 1.5 Gbps Electrical Specifications: These are electrical specifications aimed at 1.5 Gbps links in Long Backplane and System-to-System Applications. These specifications are based upon the SAS references.
- **Gen2x:** Extended Length 3.0 Gbps Electrical Specifications: These are electrical specifications aimed at 3.0 Gbps links in Long Backplane and System-to-System Applications. These specifications are based upon the SAS references.

7.1.1 List of services

- ☐ Transmit a 1.5 Gbps or 3.0 Gbps differential NRZ serial stream at specified voltage levels
- ☐ Provide a 100 Ohm matched termination (differential) at the transmitter
- ☐ Serialize a 10, 20, 40, or other width parallel input from the Link for transmission
- ☐ Receive a 1.5 Gbps or 3.0 Gbps differential NRZ serial stream with data rates of ± 350 ppm with $\pm 0/-5000$ ppm (due to SSC profile) from the nominal data rate
- ☐ Provide a 100 Ohms matched termination (differential) at the receiver
- ☐ Extract data (and, optionally, clock) from the serial stream
- ☐ De-serialize the serial stream
- ☐ Detect the K28.5 comma character and provide a bit and word aligned 10, 20, 40, or other width parallel output
- ☐ Provide specified OOB signaling detection and transmission
- ☐ Use OOB signaling protocol for initializing the Serial ATA interface, and use this OOB sequence to execute a pre-defined speed negotiation function
- ☐ Perform proper power-on sequencing and speed negotiation
- ☐ Provide device status to Link layer
 - ☐ Device present
 - ☐ Device absent
 - ☐ Device present but failed to negotiate communications
- ☐ Optionally support power management modes
- ☐ Optionally perform transmitter and receiver impedance calibration
- ☐ Handle the input data rate frequency variation due to a spread spectrum transmitter clock
- ☐ Accommodate request to go into Far-End retimed loopback, and other BIST Activate FIS test modes of operation when commanded

7.1.2 Low Level Electronics Block Diagrams (Informative)

The following block diagrams are provided as a reference for the following sections of this document. Although informative in nature, the functions of the blocks described herein provide the basis upon which the normative specifications apply. The individual blocks provided are provided as an example of one possible implementation.

7.1.2.1 Physical Plant Block Diagram

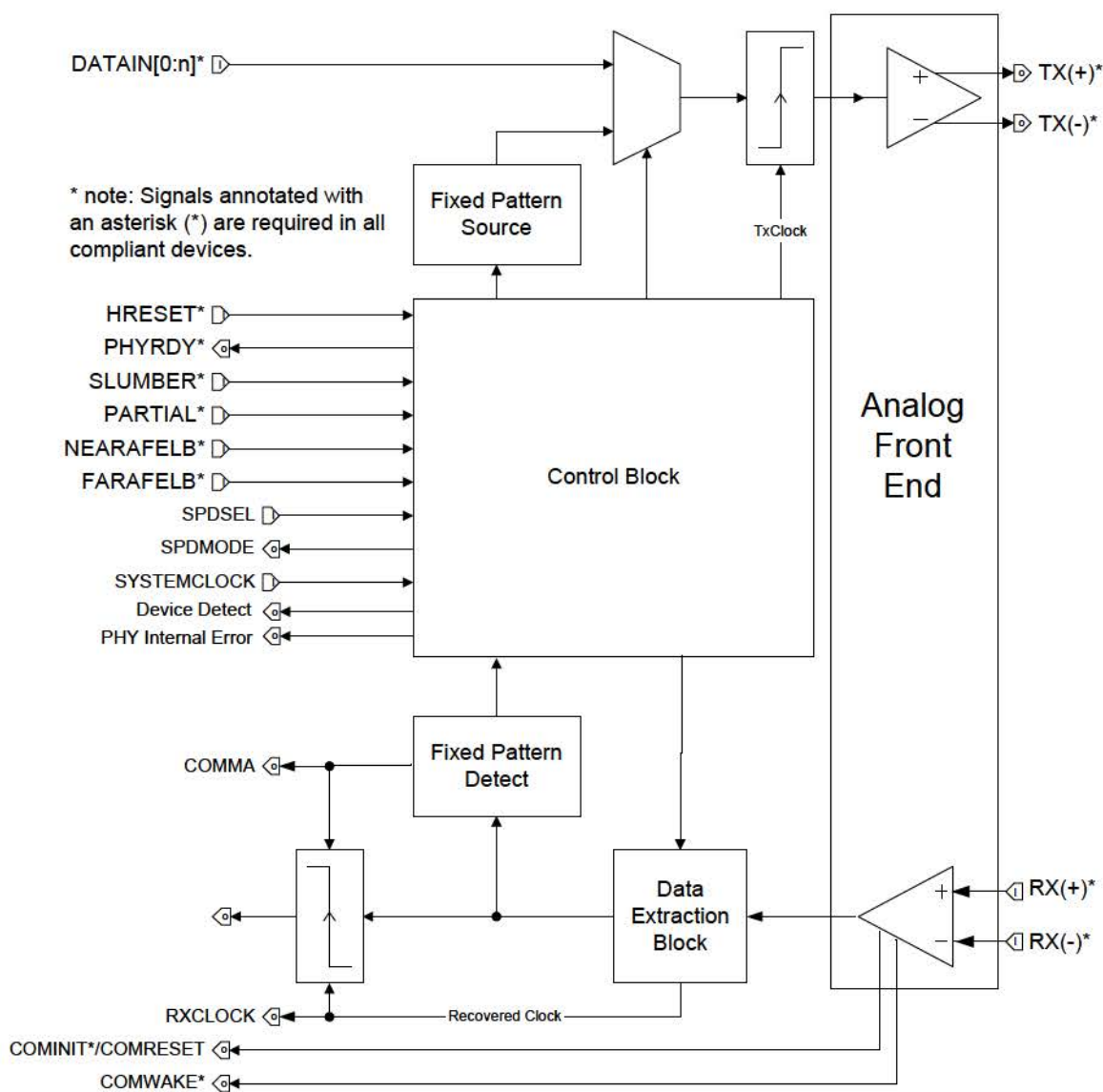


Figure 64 – Physical plant overall block diagram (Informative)

7.1.2.2 Physical plant overall block diagram description

Analog front end	This block is the basic interface to the transmission line. This block consists of the high speed differential drivers and receivers as well as the OOB signaling circuitry.
Control block	This block is a collection of logic circuitry that controls the overall functionality of the Physical plant circuitry.
Fixed pattern source	This block provides the support circuitry that generates the patterns as needed to implement the ALIGN _P primitive activity.
Fixed pattern detect	This block provides the support circuitry to allow proper processing of the ALIGN _P primitives.
Data extraction block	This block provides the support circuitry to separate the clock and data from the high speed input stream.
TX clock	This signal is internal to the Physical plant and is a reference signal that regulates the frequency at which the serial stream is sent via the high speed signal path
TX + / TX -	These signals are the outbound high speed differential signals that are connected to the serial ATA cable.
RX + / RX -	These signals are the inbound high speed differential signals that are connected to the serial ATA cable.
DATAIN	Data sent from the Link layer to the Phy layer for serialization and transmission.
PHYRESET	This input signal causes the Phy to initialize to a known state and start generating the COMRESET OOB signal across the interface.
PHYRDY	Signal indicating Phy has successfully established communications. The Phy is maintaining synchronization with the incoming signal to its receiver and is transmitting a valid signal on its transmitter.
SLUMBER	Causes the Phy layer to transition to the Slumber power management state.
PARTIAL	Causes the Phy layer to transition to the Partial power management state
NEARAFELB	Causes the Phy to loop back the serial data stream from its transmitter to its receiver
FARAFELB	Causes the Phy to loop back the serial data stream from its receiver to its transmitter
SPDSEL	Causes the control logic to automatically negotiate for a usable interface speed or sets a particular interface speed. The actual functionality of this input is vendor specific and varies from manufacturer to manufacturer.

SPDMODE	Output signal that reflects the current interface speed setting. The actual functionality of this signal is vendor specific and varies from manufacturer to manufacturer.
SYSTEMCLOCK	This input is the clock source for much of the control circuit and is the basis from which the transmitting interface speed is established.
COMMA	This signal indicates that a K28.5 character was detected in the inbound high speed data stream.
DATAOUT	Data received and de-serialized by the Phy and passed to the Link layer
RX CLOCK / Recovered clock	This signal is derived from the high speed input data signal and determines when parallel data has been properly formed at the DATAOUT pins and is available for transfer to outside circuitry.
COMRESET / COMINIT	Host: Signal from the OOB detector that indicates the COMINIT OOB signal is being detected. Device: Signal from the OOB detector that indicates the COMRESET OOB signal is being detected.
COMWAKE	Signal from the OOB detector that indicates the COMWAKE OOB signal is being detected.

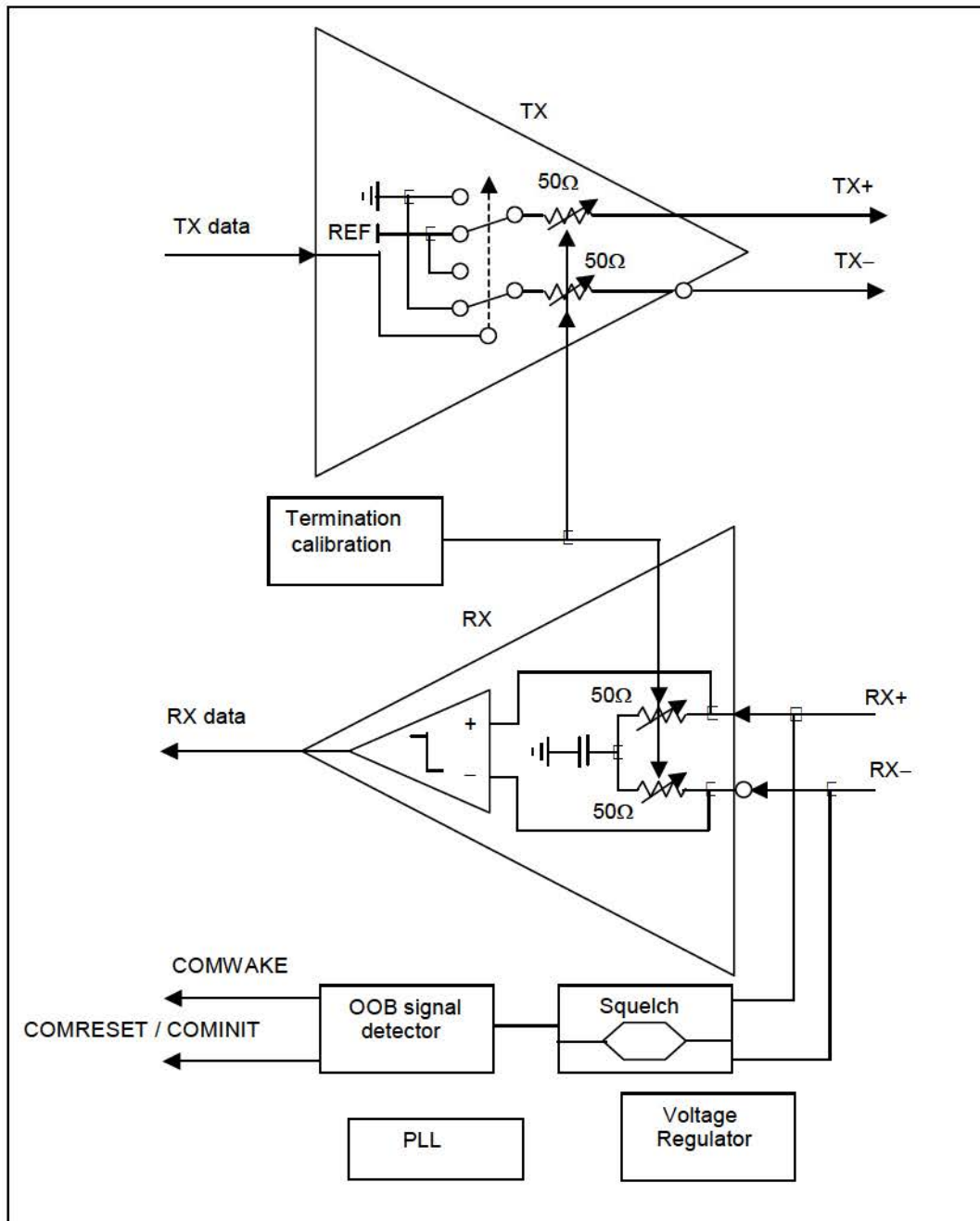


Figure 65 – Analog front end (AFE) block diagram
[External AC caps not shown]

7.1.2.3 Analog front end (AFE) block diagram description

TX	This block contains the basic high speed driver electronics
RX	This block contains the basic high speed receiver electronics
Termination calibration	This block is used to establish the impedance of the RX block in order to properly terminate the high speed serial cable.
Squelch	This block establishes a limit so that detection of a common mode signal can be properly accomplished.
OOB signal detector	This block decodes OOB signal from the high speed input signal path.
PLL	This block is used to synchronize an internal clocking reference so that the input high speed data stream may be properly decoded.
Voltage Regulator	This block stabilizes the internal voltages used in the other blocks so that reliable operation may be achieved. This block may or may not be required for proper operation of the balance of the circuitry. The need for this block is implementation specific.
TX+ / TX-	This is the same signal as described in the previous section: Physical plant overall block diagram description
RX+ / RX-	This is the same signal as described in the previous section: Physical plant overall block diagram description
TxData	Serially encoded 10b data attached to the high speed serial differential line driver.
RxData	Serially encoded 10b data attached to the high speed serial differential line receiver.
COMWAKE	This is the same signal as described in the previous section: Physical plant overall block diagram description
COMRESET / COMINIT	This is the same signal as described in the previous section: Physical plant overall block diagram description

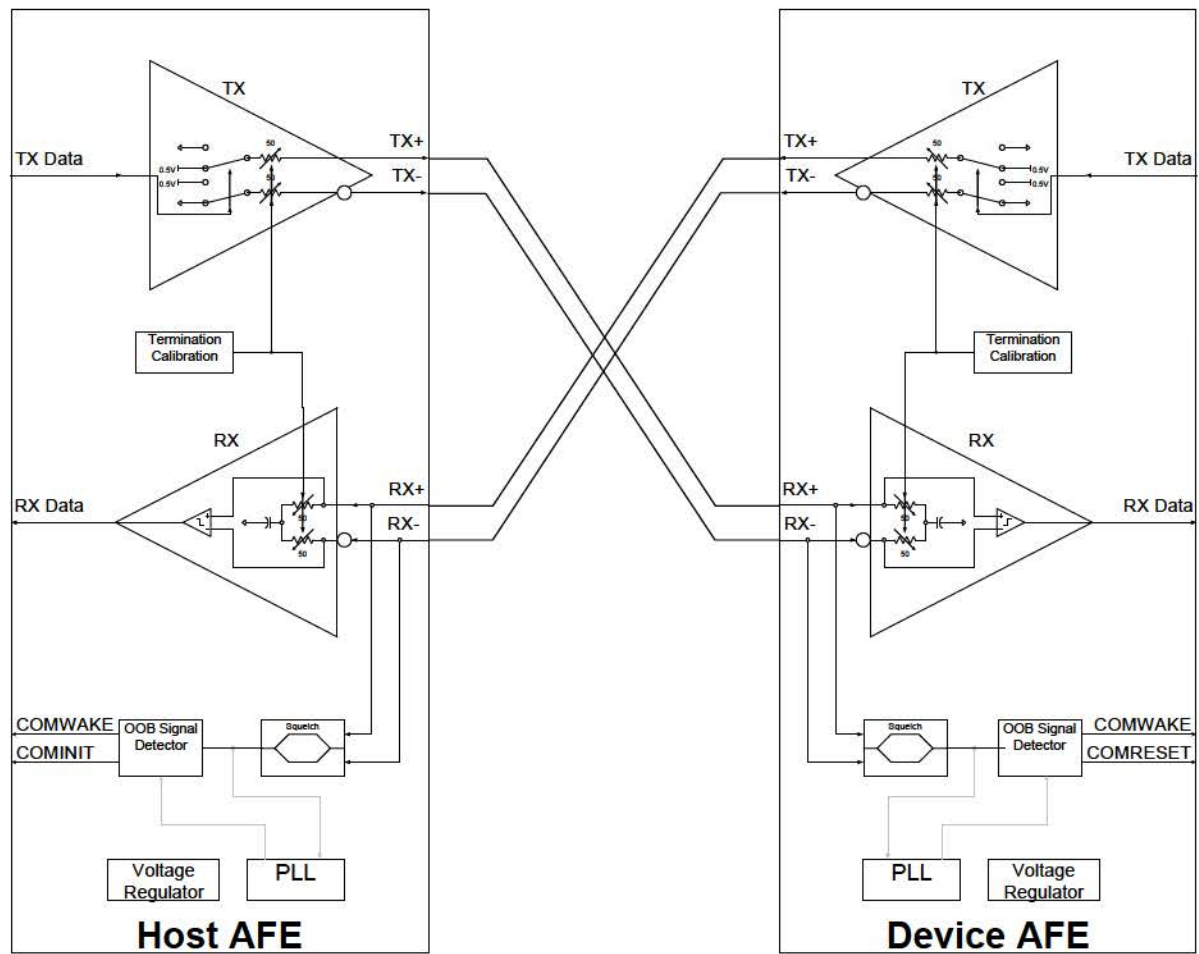


Figure 66 – Analog front end (AFE) cabling
[External AC Coupling Capacitors not shown]

7.1.3 Compliance Testing

This document provides electrical specifications that when met by hosts, devices, and interconnects, satisfy the link performance specifications when combined into a system. This section of the document provides an overview of how to determine whether a Host, Device, or Interconnect is compliant to the specifications of this document.

Each electrical specification requires a specific measurement, test setup and data patterns. This section ties all of these requirements together to aid the reader in understanding what is needed for compliance testing.

Table 20, Table 21, Table 22, Table 23, Table 24, and Table 25 detail the electrical requirements for SATA compliance. Each requirement is defined in section 7.2.2. Jitter is described in section 7.3. Measurement methods for each specification are detailed in section 7.4. Section 7.5 discusses Interface States relating to OOB and power management. Section 6.3 describes the Interconnect requirements.

The Phy layer is divided into a transmitter, interconnect, and a receiver.

The SATA link is a full duplex point to point link as continuous data activity exists on each direction. For purposes of compliance testing of Hosts and Devices, the full duplex link is broken into two simplex links, one for the Host transmitting to the Device and the other for the Device transmitting to the Host. Each link is tested for compliance separately. Each transmitter to receiver Link contains the following elements:

Transmitter (IC/PCB/SATA Connector) – to –
Interconnect (Connector/Cable or PCB/Connector) – to –
Receiver (SATA Connector / PCB / IC)

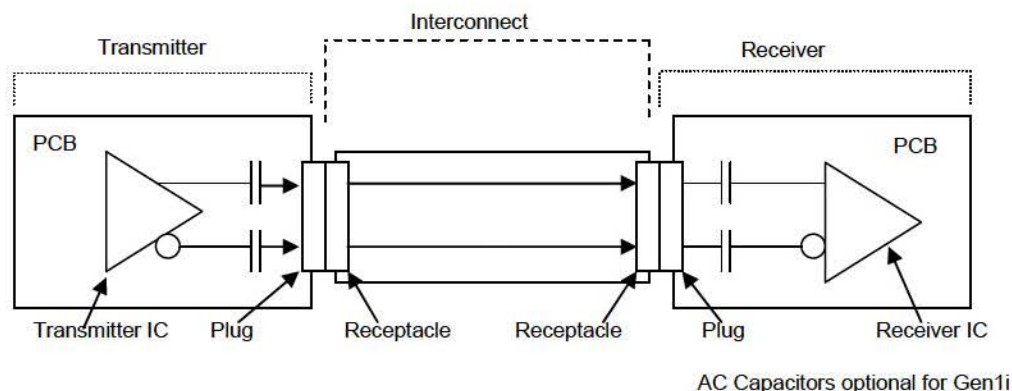


Figure 67 – The Simplex Link

In testing the compliance of SATA components that make up a system there are five Compliance Areas to be measured:

1. "Transmitted Signal"—Examine the transmitted signal quality at the compliance point for the Host/Device into a Laboratory Load. Electrical specifications include amplitude, rise/fall time, frequency, jitter, etc. The Electrical specifications apply to the signal output from the Transmitter-Under-Test at the mated connector when driving a Laboratory Load. No attempt has been made to specify the signal when attached to a cable, backplane or directly into another Device. Actual signals "In-System" may vary.
2. "Transmitter" — Examine all specified characteristics of the Transmitter from the compliance point. This includes specifications such as differential and common-mode impedance. The "Transmitter" includes the IC which incorporates the transmitter, the PCB, the SATA connector as well as any additional components between the IC and the SATA connector.
3. "Receiver" — Examine all specified characteristics of the Receiver from the compliance point. This includes specifications such as differential and common-mode impedance. The "Receiver" includes the SATA connector, the PCB and the IC which incorporates the receiver as well as any additional components between the IC and the SATA connector.
4. "Receiver Tolerance" — When the Receiver is presented with a worst-case "Lab-Sourced Signal", and operating with its active transmitter, shall meet the specified Frame Error Rates. This requires carefully controlled signal sources in order to generate a worst-case signal.
5. "Interconnect" -- Examine all specified characteristics of the interconnect using test equipment. The interconnect includes SATA connector pairs at each end. The testing requirements and procedures are described in section 6.3.

In order to determine compliance to the specifications of this document, measurements shall be performed separately with Host, Device, or Interconnect being tested when connected to test equipment. Compliance tests are not done with a Host, Device, or Interconnect connected together. Unless otherwise specified, all compliance measurements shall be taken through the mated connector pair.

NOTE: The electrical specifications in the Receiver Tolerance Table do not describe the characteristics of the received signal; these describe the Lab-Sourced Signal calibrated into a Laboratory Load and subsequently applied to the Receiver. The Receiver Tolerance Table does not describe the characteristics of a signal from a Transmitter through an Interconnect into a Laboratory Load. Received signals in a system are potentially worse due to the non-ideal impedance match of the transmitter and the receiver.

7.1.4 Link Performance

The performance of a SATA system with Host and Device linked together with an Interconnect is measured by the frame error rate, using a set of reference frames, defined by a specific set of ordered test patterns within the frame. An operating Host-Device duplex link that meets the Frame Error Rate (FER) specifications of Table 20 for both of its simplex links is deemed to fulfill Serial ATA performance levels. A Host or Device is commanded to generate the various test patterns through the use of the BIST Activate FIS or other vendor unique commands to the device under test.

7.2 Electrical specifications

The goal of this specification is to provide a description of characteristics to ensure interoperability of SATA components; devices, hosts, and interconnects. Any combination of compliant components should provide the stated link performance. Secondly a means of

validation to the requirements is described in section 7.4. Validation consists of performing tests on individual SATA components.

Serial ATA devices and hosts shall comply with the electrical specifications shown in Table 20, Table 21, Table 22, Table 23, Table 24, and Table 25. The transmitter consists of the driver, printed circuit board, and mated connector pair. The receiver consists of the receiver IC, printed circuit board, and mated connector pair.

Unless otherwise stated, all specifications include the mated connector pair.

7.2.1 Physical Layer Requirements Tables

Table 20 – General Specifications

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
Channel Speed	Gbps	Nom	1.5			3.0			7.2.2.1.1	-
Fbaud	GHz	Nom	1.5			3.0			-	-
FER, Frame Error Rate		Max	8.2e-8 at 95% confidence level			8.2e-8 at 95% confidence level			7.2.2.1.2	7.4.1
T _{UI} , Unit Interval	ps	Min	666.4333			333.2167			7.2.2.1.3	7.4.11
		Nom	666.6667			333.3333				
		Max	670.2333			335.1167				
f _{tol} , TX Frequency Long Term Stability	ppm	Min	-350			-350			7.2.2.1.4	7.4.6
		Max	+350			+350				
f _{SSC} , Spread- Spectrum Modulation Frequency	kHz	Min	30			30			7.2.2.1.5 7.3.3	7.4.11
		Max	33			33				
SSC _{tol} , Spread-Spectrum Modulation Deviation	ppm	Min	-5000			-5000			7.2.2.1.6 7.3.3	7.4.11
		Max	+0			+0				
V _{cm,dc} , DC Coupled Common Mode Voltage	mV	Min	200	-	-			7.2.2.1.7	7.4.4	
		Nom	250	-	-					
		Max	450	-						
V _{cm,ac coupled} , AC Coupled Common Mode Voltage	mV	Min	0	-	-			7.2.2.1.8	7.4.25	
		Max	2000	-	-					
Z _{diff} , Nominal Differential Impedance	Ohm	Nom	100	-	-			7.2.2.1.9	7.4.22	

C_{ac coupling} AC Coupling Capacitance	nF	Max	12		12	7.2.2.1.10	7.4.14
t_{settle,cm} Common Mode Transient Settle Time	ns	Max	10	-	-	7.2.2.3.6	-
V_{trans} Sequencing Transient Voltage	V	Min	-2.0		-2.0	7.2.2.1.11	7.4.13
		Max	2.0		2.0		

Table 21 – Transmitter Specifications

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
Z_{diffTX} , TX Pair Differential Impedance	Ohm	Min	85	85	-	-	-	85	7.2.2.2.1	7.4.22
		Max	115	115	-	-	-	115		
Z_{s-eTX} , TX Single-Ended Impedance	Ohm	Min	40	-	-	-	-	-	7.2.2.2.2	7.4.23
$RL_{DD11,TX}$, TX Differential Mode Return Loss (all values Min)	dB	150 MHz- 300 MHz	-	-	-	14	14	-	7.2.2.2.3	7.4.10
		300 MHz- 600 MHz	-	-	-	8	8	-		
		600 MHz- 1.2 GHz	-	-	-	6	6	-		
		1.2 GHz- 2.4 GHz	-	-	-	6	6	-		
		2.4 GHz- 3.0 GHz	-	-	-	3	3	-		
		3.0 GHz- 5.0 GHz	-	-	-	1	-	-		
$RL_{CC11,TX}$, TX Common Mode Return Loss (all values Min)	dB	150 MHz- 300 MHz	-	-	-	8	5	-	7.2.2.2.4	7.4.10
		300 MHz- 600 MHz	-	-	-	5	5	-		
		600 MHz- 1.2 GHz	-	-	-	2	2	-		
		1.2 GHz- 2.4 GHz	-	-	-	2	2	-		
		2.4 GHz- 3.0 GHz	-	-	-	2	1	-		
		3.0 GHz- 5.0 GHz	-	-	-	1	-	-		

RL_{DC11,TX}, TX Impedance Balance (all values Min)	dB	150 MHz- 300 MHz	-	30	30	-	7.2.2.2.5	7.4.10
		300 MHz- 600 MHz	-	20	20	-		
		600 MHz- 1.2 GHz	-	10	10	-		
		1.2 GHz- 2.4 GHz	-	10	10	-		
		2.4 GHz- 3.0 GHz	-	4	4	-		
		3.0 GHz- 5.0 GHz	-	4	-	-		

Table 22 – Transmitted Signal Requirements

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
V_{diffTX}, TX Differential Output Voltage	mVppd	Min	400	400	400	400	400	400	7.2.2.3.1	7.4.4
		Nom	500		-	-				
		Max	600		1600	700		1600		
UI_{VminTX}, TX Minimum Voltage Measurement Interval	UI		-		0.5	0.45-0.55		0.5	7.2.2.3.2	7.4.4
t_{20-80TX}, TX Rise/Fall Time	ps (UI)	Min 20-80%	100 (.15)		67 (.10)	67 (.20)			7.2.2.3.3	7.4.3
		Max 20-80%	273 (.41)		273 (.41)	136 (.41)				
t_{skewTX}, TX Differential Skew	ps	Max	20			20		15	7.2.2.3.4	7.4.12
V_{cm,acTX}, TX AC Common Mode Voltage	mVp-p	Max	-			50		-	7.2.2.3.5	7.4.17
D_{VdiffOOB}, OOB Differential Delta	mV	Max	-		25	25			7.2.2.3.7	7.4.19
D_{VcmOOB}, OOB Common Mode Delta	mV	Max	-		50	50			7.2.2.3.8	7.4.18
R/F_{bal}, TX Rise/Fall Imbalance	%	Max	-			20		-	7.2.2.3.9	7.4.16
Amp_{bal}, TX Amplitude Imbalance	%	Max	-		10	10			7.2.2.3.10	7.4.15

TJ at Connector, Data-Data, 5UI	UI	Max	0.355	-	-	7.2.2.3.11 7.3	-
DJ at Connector, Data-Data, 5UI	UI	Max	0.175	-	-		
TJ at Connector, Data-Data, 250UI	UI	Max	0.47	-	-		
DJ at Connector, Data-Data, 250UI	UI	Max	0.22	-	-		
TJ at Connector, Clk-Data, $f_{BAUD}/10$	UI	Max	-	-	0.30	7.2.2.3.12 7.3	7.4.7 0
DJ at Connector, Clk-Data, $f_{BAUD}/10$	UI	Max	-	-	0.17		
TJ at Connector, Clk-Data, $f_{BAUD}/500$	UI	Max	-	-	0.37		
DJ at Connector, Clk-Data, $f_{BAUD}/500$	UI	Max	-	-	0.19		
TJ after CIC, Clk-Data, $f_{BAUD}/1667$	UI	Max	-	0.55	-		
DJ after CIC, Clk-Data, $f_{BAUD}/1667$	UI	Max	-	0.35	-		

Table 23 – Receiver Specifications

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
Z_{diffRX} , RX Pair Differential Impedance	Ohm	Min	85			-		85	7.2.2.4.1	7.4.22
		Max	115			-		115		
Z_{s-eRX} , RX Single-Ended Impedance	Ohm	Min	40		-	-			7.2.2.4.2	7.4.23
$RL_{DD11,RX}$, RX Differential Mode Return Loss (all values are Min)	dB	150 MHz-300 MHz	-			18	18	-	7.2.2.4.3	7.4.10
		300 MHz-600 MHz	-			14	14	-		
		600 MHz-1.2 GHz	-			10	10	-		
		1.2 GHz-2.4 GHz	-			8	8	-		
		2.4 GHz-3.0 GHz	-			3	3	-		
		3.0 GHz-5.0 GHz	-			1	-	-		
$RL_{CC11,RX}$, RX Common Mode Return Loss (all values are Min)	dB	150 MHz-300 MHz	-			5	5	-	7.2.2.4.4	7.4.10
		300 MHz-600 MHz	-			5	5	-		
		600 MHz-1.2 GHz	-			2	2	-		
		1.2 GHz-2.4 GHz	-			2	2	-		
		2.4 GHz-3.0 GHz	-			2	1	-		
		3.0 GHz-5.0 GHz	-			1	-	-		
$RL_{DC11,RX}$, RX Impedance Balance (all values are Min)	dB	150 MHz-300 MHz	-			30	30	-	7.2.2.4.5	7.4.10
		300 MHz-600 MHz	-			30	30	-		
		600 MHz-1.2 GHz	-			20	20	-		
		1.2 GHz-2.4 GHz	-			10	10	-		
		2.4 GHz-3.0 GHz	-			4	4	-		
		3.0 GHz-5.0 GHz	-			4	-	-		

Table 24 – Lab-Sourced Signal (for Receiver Tolerance Testing)

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
V_{diffRX} , RX Differential Input Voltage	mVppd	Min	325	240	275	275	240	275	7.2.2.6.1	7.4.5
		Nom	400		-					
		Max	600		1600	750	750	1600		
t_{20-80RX} , RX Rise/Fall Time	ps (UI)	Min 20-80%	100 (.15)		67 (.10)	67 (.20)			7.2.2.6.2	7.4.3
		Max 20-80%	273 (.41)			136 (.41)				
UI_{VminRX} , RX Minimum Voltage Measurement Interval	UI		-		0.5	0.5			7.2.2.6.3	7.4.5
t_{skewRX} , RX Differential Skew	ps	Max	-		80	50		75	7.2.2.6.4	7.4.12
V_{cm,acRX} , RX AC Common Mode Voltage	mVp-p	Max	100		150	100		150	7.2.2.6.5	7.4.9
f_{cm,acRX} , AC Common Mode Frequency	MHz	Min	2			2			7.2.2.6.6	7.4.9
		Max	200			200				
TJ at Connector, Data-Data, 5UI	UI	Max	0.43		-				7.2.2.6.7 7.3	-
DJ at Connector, Data-Data, 5UI	UI	Max	0.25		-					
TJ at Connector, Data-Data, 250UI	UI	Max	0.6		-					
DJ at Connector, Data-Data, 250UI	UI	Max	0.35		-	-				

TJ at Connector, Clk-Data, $f_{BAUD}/10$	UI	Max	-	0.46	-	7.2.2.6.8 7.3	7.4.7 7.4.9
DJ at Connector, Clk-Data, $f_{BAUD}/10$	UI	Max	-	0.35	-		
TJ at Connector, Clk-Data, $f_{BAUD}/500$	UI	Max	-	0.60	-		
DJ at Connector, Clk-Data, $f_{BAUD}/500$	UI	Max	-	0.42	-		
TJ at Connector, Clk-Data, $f_{BAUD}/1667$	UI	Max	-	0.65	-		
DJ at Connector, Clk-Data, $f_{BAUD}/1667$	UI	Max	-	0.35	-		

Table 25 – OOB Specifications

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
V_{thresh}, OOB Signal Detection Threshold	mVppd	Min	50	120	75	120	7.2.2.7.1	7.4.20		
		Nom	100	-	125	-				
		Max	200	240	200	240				
U_{IOOB}, UI During OOB Signaling	ps	Min	646.67		646.67		7.2.2.7.2	-		
		Nom	666.67		666.67					
		Max	686.67		686.67					
COMINIT/ COMRESET and COMWAKE Transmit Burst Length	U _{IOOB}		160		160		7.2.2.7.3	7.4.21		
COMINIT/ COMRESET Transmit Gap Length	U _{IOOB}		480		480		7.2.2.7.4	7.4.21		
COMWAKE Transmit Gap Length	U _{IOOB}		160		160		7.2.2.7.5	7.4.21		
COMWAKE Gap Detection Windows	ns	May detect	55 ≤ T < 175		55 ≤ T < 175		7.2.2.7.6	7.4.21		
		Shall detect	101.3 ≤ T ≤ 112		101.3 ≤ T ≤ 112					
		Shall not detect	T < 55 or T ≥ 175		T < 55 or T ≥ 175					
COMINIT/ COMRESET Gap Detection Windows	ns	May detect	175 ≤ T < 525		175 ≤ T < 525		7.2.2.7.7	7.4.21		
		Shall detect	304 ≤ T ≤ 336		304 ≤ T ≤ 336					
		Shall not detect	T < 175 or T ≥ 525		T < 175 or T ≥ 525					

7.2.2 Physical Layer Requirements Details

7.2.2.1 General Specifications Details

This section contains the details on Table 20 entries.

7.2.2.1.1 Channel Speed

A reference value showing the nominal rate of data through the channel.

7.2.2.1.2 Frame Error Rate

Frame error rate is the measure of link performance using all the intermediate circuit blocks in the chain from low-level Phy Layer, Link Layer, through Transport Layer. Frame error rate is a system level test, not a compliance test. Error detection is at the frame level using the CRC (Cyclic Redundancy Check) error detection mechanism, and respective reporting to the higher layer levels.

7.2.2.1.3 Unit Interval

This is the operating data period (nominal value architecture specific). This value includes the long term frequency accuracy and the Spread Spectrum Clock FM frequency deviation (rounded to 4 places).

This is the time interval value of each cycle of the Reference Clock.

7.2.2.1.4 TX Frequency Long Term Stability

This specifies the allowed frequency variation from nominal; this does not include frequency variation due to jitter, Spread Spectrum Clocking, or phase noise of the clock source.

7.2.2.1.5 Spread Spectrum Modulation Frequency

The modulation frequency of the Spread Spectrum frequency modulation. See further details of Spread Spectrum in section 7.3.3.

7.2.2.1.6 Spread Spectrum Modulation Deviation

This is the allowed frequency variation from nominal due to the SSC AC modulation expressed in terms of the unit interval deviation from the unit interval value of the long term frequency value. See further details of Spread Spectrum in section 7.3.3.

7.2.2.1.7 DC Coupled Common Mode Voltage (Gen1i)

The Common mode DC level is defined as $[(TX+) + (TX-)]/2$ and $[(RX+) + (RX-)]/2$ measured at the mated connector.

This requirement only applies to Gen1i DC-coupled designs (no blocking capacitors) that hold the common-mode DC level at the connector. The four possible common mode biasing configurations shown in Figure 68 below demonstrate that only DC-coupled designs need sustain the specified common-mode level to ensure interoperability. AC coupled designs may allow the DC level at the connector to float. The SATA interfaces defined as Gen1x, Gen2i, Gen2x shall be AC-coupled and this requirement does not apply to these.

A DC-coupled receiver shall weakly hold the common-mode level of its inputs to the $V_{cm,dc}$ value specified in Table 20. A DC-coupled transmitter shall transmit with the $V_{cm,dc}$ value specified in Table 20 while driving into a 100 Ohm differential impedance.

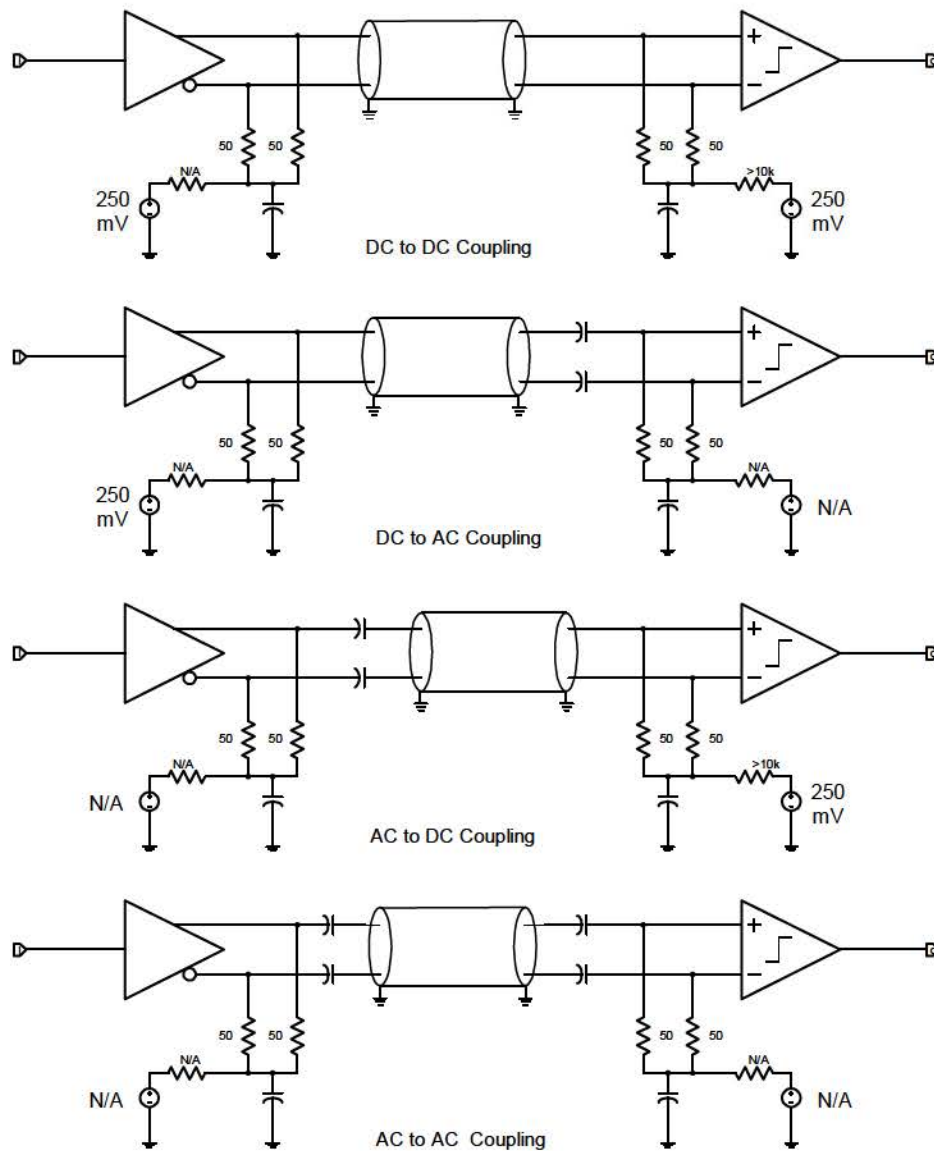


Figure 68 – Common mode biasing examples for Gen1i (Informative)

7.2.2.1.8 AC Coupled Common Mode Voltage

The SATA interface defined as Gen1i may be AC or DC coupled as shown in Figure 68. The SATA interfaces defined as Gen1x, Gen2i, Gen2x shall be AC-coupled. Figure 69 shows an example of a fully AC-coupled system.

Compliance points for SATA are defined at the connector. The AC coupled common mode voltage in Table 20 defines the open circuit DC voltage level of each single-ended signal at the IC side of the coupling capacitor in an AC coupled Phy and it shall be met during all possible power and electrical conditions of the Phy including power off and power ramping. Since the Gen1x, Gen2i, Gen2x specification defines only the signal characteristics as observable at the connector, this value is not applicable to those specifications. The common mode transient requirements defined in Table 20 were determined sufficient to limit stresses on the attached components under transient conditions which was the sole intent of the AC coupled common mode voltage requirement. Due to this, the following is true even for Gen1i where $V_{cm,ac}$ coupled applies: AC coupled common mode voltage levels outside the specified range may be used provided that the transient voltage requirements of Table 20 are met.

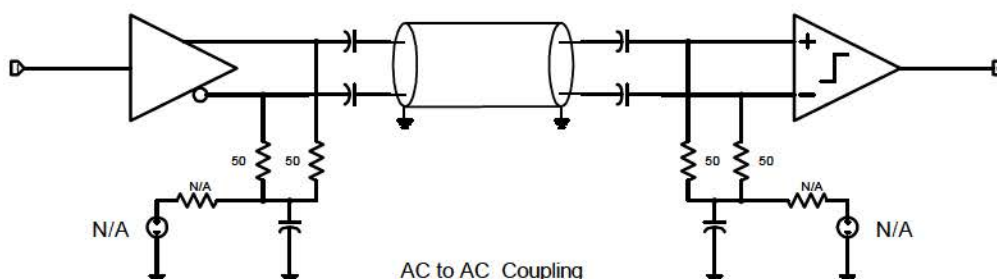


Figure 69 – Common mode biasing for Gen1x, Gen2i, and Gen2x

7.2.2.1.9 Nominal Differential Impedance (Gen1i)

The nominal impedance of all components in a SATA system.

7.2.2.1.10 AC Coupling Capacitance

The value of the coupling capacitor used in AC coupled implementations. AC coupling is optional for Gen1i and mandatory of Gen1x, Gen2i, and Gen2x.

7.2.2.1.10.1 Coupling Capacitor Characteristics (Informative)

The physical size of the capacitor should be as small as practical to reduce the capacitance to ground. Body sizes larger than 0603 (or values less than 300 pF) should be avoided since they are likely to result in a failure of the return loss requirements in Table 21 and Table 23 in section 7.2.1.

7.2.2.1.11 Sequencing Transient Voltage

This parameter addresses the transient voltages on the serial data bus during power sequencing and power mode changes. Since either the receiver or the transmitter may be affected by power sequencing transients, the term "aggressor" is used to indicate the sequencing interface circuit and the term "victim" is used for the interface circuit receiving the transient.

In order to limit the voltage and energy seen by the victim receiver or transmitter circuitry during power sequencing, several parameters of the aggressor and victim are involved. Although parameters of the victim, such as common mode voltage and single ended impedance, affect the observed transient, this measurement addresses limiting the aggressor contribution.

The aggressor common mode voltage, single ended impedance, and AC coupling capacitor value determine the level of the sequencing transient. This measurement addressed the common mode voltage of the aggressor. The rate of change of the power on or power off ramp also affects this level. The limits provided allow for power up or power down ramps at rates faster than the time constants of the signal lines, although practical systems may not achieve this rate. This measurement shall include the test conditions of power on and power off ramping at the fastest possible rate expected in systems using the Phy, as well as any power mode transitions.

7.2.2.2 Transmitter Specification Details

This section contains the details on Table 21 entries.

7.2.2.2.1 TX Pair Differential Impedance (Gen1i)

As seen by a differential TDR with 100 ps (max) edge looking into connector (20%-80%). Measured with TDR in differential mode.

7.2.2.2.2 TX Single-Ended Impedance (Gen1i)

As seen by TDR with 100 ps (max) edge looking into connector (20%-80%). The TDR is set to produce simultaneous positive pulses on both signals of the TX pair. Single-ended impedance is the resulting (even mode) impedance of each signal. Both signals shall meet the single ended impedance requirement.

This requirement shall be met during all possible power and electrical conditions of the Phy including power off and power ramping.

7.2.2.2.3 TX Differential Mode Return Loss (Gen2i, Gen2m)

The differential mode return loss is defined as the ratio (expressed in dB) of differential mode incident power to differential mode reflected power both at a 100 Ohm impedance level. In the system environment the purpose of controlling the return loss of devices and hosts is to limit signal reflections that cause data dependent jitter. These signal reflections in question are over and above those that exist in compliance testing when connected to a matched source or load.

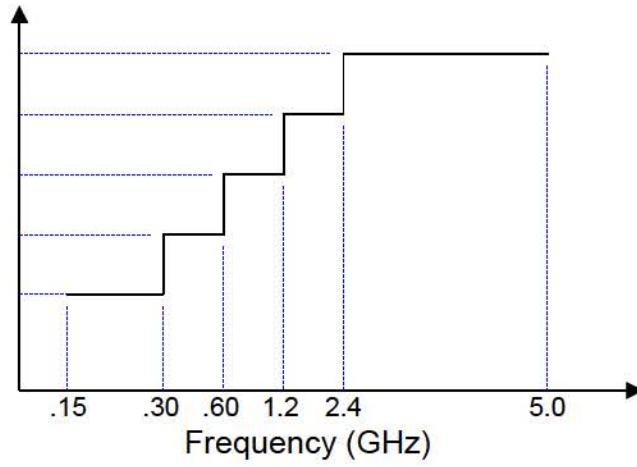


Figure 70 – Differential Return Loss Limits

7.2.2.2.4 TX Common Mode Return Loss (Gen2i, Gen2m)

The common mode return loss is defined as the ratio (expressed in dB) of common mode incident power to common mode reflected power both at a 25 Ohm impedance level. The intended signal propagation mode in SATA is the differential mode. However, imperfections in the system create some coupling between the common and differential modes. This has three consequences: radiated emissions, noise susceptibility, and signal degradation. Common mode reflections exacerbate these impairments. The common mode return loss is a bound on the magnitude of common mode reflections in the system.

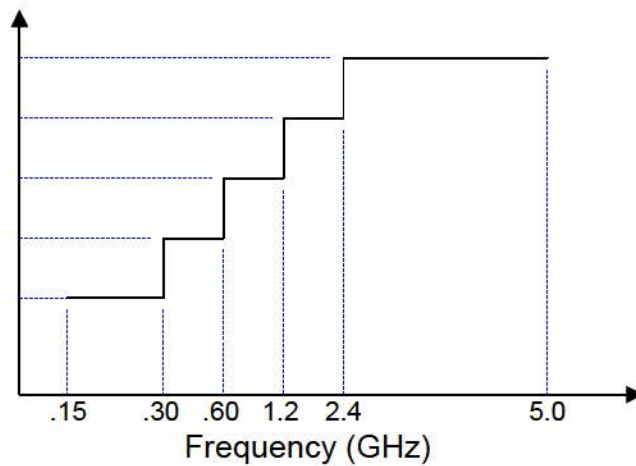


Figure 71 – Common Mode Return Loss Limits

7.2.2.2.5 TX Impedance Balance (Gen2i, Gen2m)

Impedance balance is defined as the ratio (expressed in dB) of common mode incident power at a 100 Ohm impedance level to differential mode reflected power at a 25 Ohm impedance level. The impedance balance is a bound on the coupling between common and differential modes.

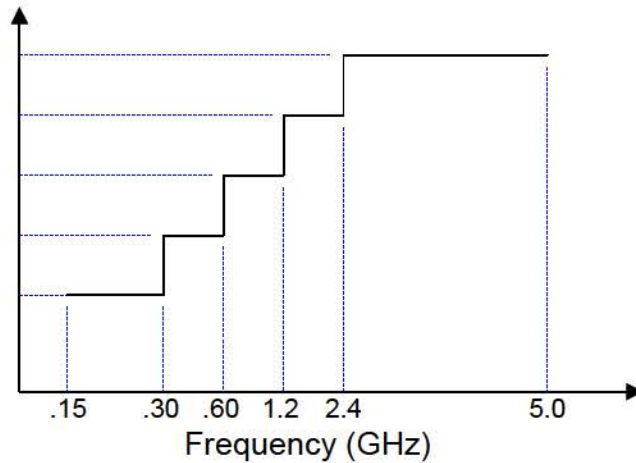


Figure 72 – Impedance Balance Limits

7.2.2.3 Transmitted Signal Requirements Details

This section contains the details on Table 22 entries.

7.2.2.3.1 TX Differential Output Voltage

The differential voltage $[(TX+) - (TX-)]$ measured at the Transmitter shall comply to the respective electrical specifications of section 7.2.

This is measured at mated Serial ATA connector on transmit side including any pre-emphasis.

7.2.2.3.2 TX Minimum Voltage Measurement Interval

The point within a UI where the signal shall meet minimum levels.

7.2.2.3.3 TX Rise/Fall Time

Rise times and fall times are measured between 20% and 80% of the signal, see Figure 73. The rise and fall time requirement $t_{r/f}$ applies to differential transitions (TX+ – TX-), for both normal and OOB signaling.

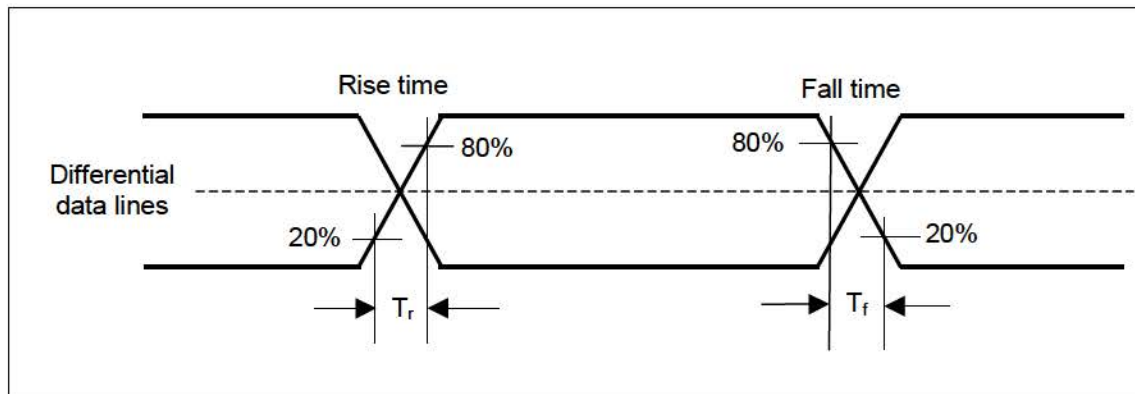


Figure 73 – Signal rise and fall times

7.2.2.3.4 TX Differential Skew (Gen2i, Gen1x, Gen2x)

TX Differential Skew is the time difference between the single-ended mid-point of the TX+ signal rising/falling edge, and the single-ended mid-point of the TX- signal falling/rising edge. It is an important parameter to control as excessive skew can result in increased high frequency jitter and common mode noise levels seen at the far end of the interconnect. The effects on the receiver are addressed in more detail in section 7.2.2.6.4. Excessive TX Differential Skew also increases EMI emissions.

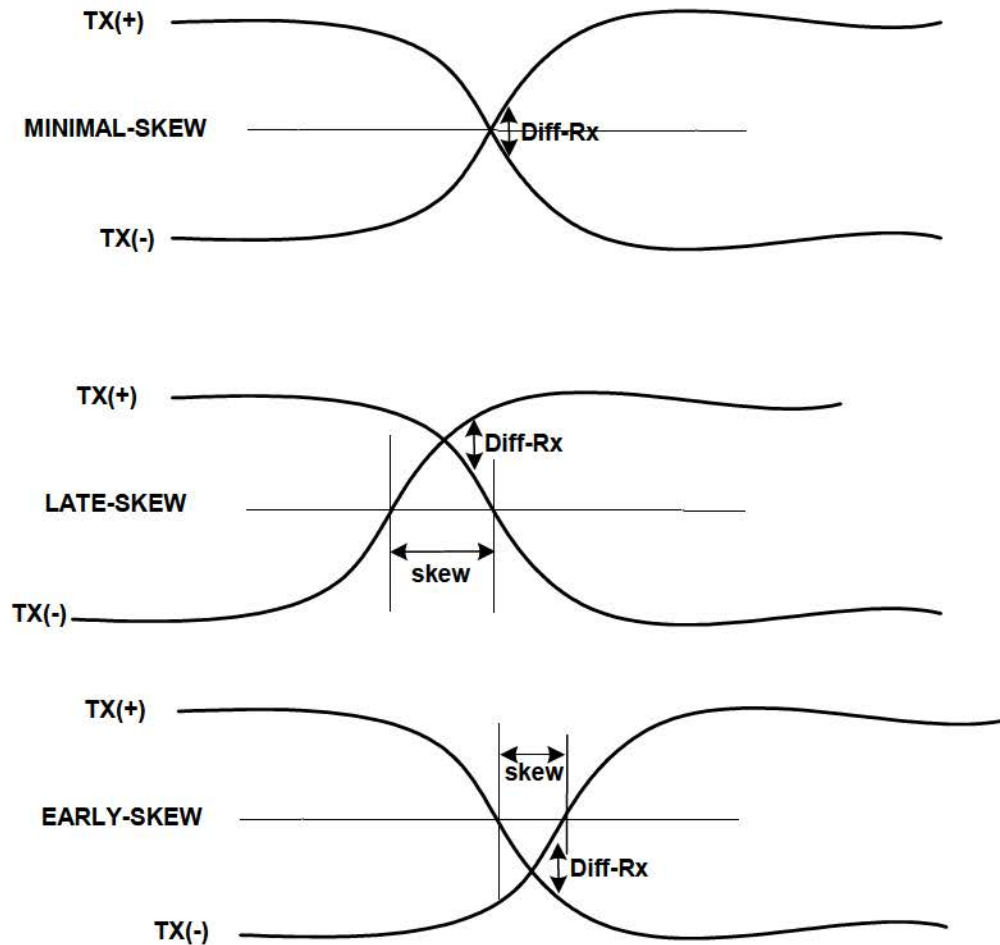


Figure 74 – TX Intra-pair Skew