Transmitter	Receiver
XXXX	XXXX
XXXX	XXXX
X_RDY_P	XXXX
X_RDY_P	XXXX
$CONT_P$	XXXX
XXXX	XXXX
XXXX	R_RDY_P
XXXX	R_RDY_P
XXXX	$CONT_P$
SOF_P	XXXX
DATA (FIS Type)	XXXX
DATA	XXXX
DATA	R_IP_P
DATA	R_IP_P
DATA	$CONT_P$
$HOLD_P$	XXXX
$HOLD_P$	XXXX
$CONT_P$	XXXX
XXXX	XXXX
XXXX	$HOLDA_P$
XXXX	$HOLDA_P$
$HOLD_P$	$CONT_P$
DATA	XXXX
DATA	XXXX
DATA	XXXX
CRC	XXXX
EOF_P	R_IP_P
$WTRM_P$	R_IP_P
$WTRM_P$	$CONT_P$
$WTRM_P$	XXXX
$CONT_P$	XXXX
XXXX	R_OK_P
XXXX	R_OK_P
XXXX	$CONT_P$
XXXX	XXXX
$SYNC_P$	XXXX
$SYNC_P$	XXXX
$CONT_P$	XXXX
XXXX	XXXX
XXXX	$SYNC_P$
XXXX	$SYNC_P$
XXXX	$CONT_P$
XXXX	XXXX
XXXX	XXXX

NOTE –
XXXX Scrambled data values (non-primitives)
DATA FIS payload data

Figure 156 – $CONT_P$ usage example

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9.4.5.1 Scrambling of data following the $CONT_P$ primitive

The data following the $CONT_P$ shall be the output of an LFSR which implements the same polynomial as is used to scramble FIS contents. That polynomial is defined in section 9.5.

The resulting LFSR value shall be encoded using the 8b/10b rules for encoding data characters before transmission by the Link layer.

The LFSR used to supply data after the $CONT_P$ primitive shall be reset to the initial value upon detection of a COMINIT or COMRESET event.

Since the data following a $CONT_P$ primitive is discarded by the Link layer, the value of the LFSR is undefined between $CONT_P$ primitives. That is, the LFSR result used for $CONT_P$ sequence N is not required to be continuous from the last LFSR result of $CONT_P$ sequence N-1.

The sequence of LFSR values used to scramble the payload contents of a FIS shall not be affected by the scrambling of data used during repeated primitive suppression. That is, the data payload LFSR shall not be advanced during repeated primitive suppression and shall only be advanced for each data payload character that is scrambled using the data payload LFSR. See section 7.5 for additional information on scrambling and repeated primitive suppression.

9.4.5.2 Periodic Retransmission of Sustained Primitives (Informative)

In order to be able to determine the state that a bus is in, it is recommended that a sustained primitive periodically be retransmitted. The only requirement is that the interval at which the retransmit occurs is large enough that EMI is not substantially affected. Since the ALIGN sequence is required to be sent at an interval of at most 256 Dwords, one solution to providing visibility to a suppressed primitive stream is to retransmit the suppressed primitive sequence immediately after the $ALIGN_P$ primitives are inserted. For example, if the original sequence was PRIM / PRIM / $CONT_P$ / junk. . . $ALIGN_P$ / $ALIGN_P$ / junk. . . the new sequence could look like: PRIM / PRIM / $CONT_P$ / junk . . . $ALIGN_P$ / $ALIGN_P$ / PRIM / PRIM / $CONT_P$ / junk.

The actual interval chosen by an implementation could be longer. The goal is to make visible the primitive stream being sustained within the normal depth of a logic analyzer.

9.4.6 $ALIGN_P$ primitive

The Link layer shall ignore reception of $ALIGN_P$ primitives. The Phy layer is free to consume received $ALIGN_P$ primitives. Implementations where the Phy does not consume received $ALIGN_P$ primitives shall effectively drop received $ALIGN_P$ primitives at the input to the Link layer or shall include Link layer processing that yields behavior equivalent to the behavior produced if all received $ALIGN_P$ primitives are consumed by the Phy and not presented to the Link.

9.4.7 Flow control signaling latency

There is a finite pipeline latency in a round-trip handshake across the Serial ATA interface. In order to avoid buffer overflow in flow control situations, the maximum tolerable latency from when a receiver issues a $HOLD_P$ signal until it receives the $HOLDA_P$ signal from the transmitter is specified. This allows the high-water mark to be set in the receive FIFO so as to avoid buffer overflow while avoiding excessive buffering/FIFO space.

In the case where the receiver wants to flow control the incoming data, it transmits $HOLD_P$ characters on the back channel. Some number of received Dwords later, valid data ceases, and $HOLDA_P$ characters are received. The larger the latency between transmitting $HOLD_P$ until receiving $HOLDA_P$, the larger the receive FIFO needs to be. The maximum allowed latency from the time the MSB of the $HOLD_P$ primitive is on the wire, until the MSB of the $HOLDA_P$ is on the wire shall be no more than 20 Dword times. The LSB is transmitted first. A receiver shall be able

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to accommodate reception of 20 Dwords of additional data after the time it transmits the $HOLD_P$ flow control character to the transmitter, and the transmitter shall respond with a $HOLDA_P$ in response to receiving a $HOLD_P$ within 20 Dword times.

There is no reference design in this specification. The specified maximum latency figure is based on the layers and states described throughout this document. It is recognized that the Link Layer may have two separate clock domains -- transmit clock domain, and the receive clock domain. It is also recognized that a Link state machine could run at the Dword clock rate, implying synchronizers between three potential clock domains. In practice more efficient implementations would be pursued and the actual latencies may be less than indicated here. The figures represent an almost literal interpretation of the spec into logic design. A synchronizer is assumed to be a worst case of 2.99 clocks of any clock domain and is rounded to three whole clocks. The Serial ATA cable contains less than half of a Dword in at Gen1 and Gen2 speeds, and is therefore rounded to 0. Two Dwords of pipeline delay are assumed for the Phy, and the FIFO is assumed to run at the Link state machine rate. No synchronization is needed between the two.

The following figure outlines the origin of the 20 Dword latency specification. The example illustrates the components of a round trip delay when the receiver transmits $HOLD_P$ on the link until reception of the $HOLDA_P$ from the transmitter. This corresponds to the number of Dwords that the receiver shall be able to accept after transmitting a $HOLD_P$.

Receiver sends $HOLD_P$:

1 Dword	Convert to 40 bit data.
1 Dword	10b/8b conversion.
1 Dword	De scrambling.
3 Dwords	Synchronization between receive clock, and Link state machine clock.
1 Dword	Link state machine is notified that primitive has been received.
1 Dword	Link state machine takes action.
1 Dword	FIFO is notified of primitive reception.
1 Dword	FIFO stops sending data to Link layer.
1 Dword	Link is notified to insert $HOLDA_P$.
1 Dword	Link acts on notification and inserts $HOLDA_P$ into data stream.
1 Dword	Scrambling.
1 Dword	8b/10b conversion.
1 Dword	Synchronize to transmit clock (3 transmit clocks, which are four times the Link state machine rate).
1 Dword	Convert to 10 bit data.
2 Dwords	Phy, transmit side.

$HOLDA_P$ on the cable.

9.4.8 Examples of primitive usage (Informative)

The following examples illustrate basic primitive usage. They do not show detailed lengthy sequences which invoke the use of the $CONT_P$ primitive.

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Table 36 – SRST write from host to device transmission breaking through a device to host Data FIS

Host	Device	Description
…	…	Previous activity abbreviated for clarity
R_IP$_P$	DATA n	Device transmitting data
R_IP$_P$	DATA n+1	
R_IP$_P$	HOLD$_P$	Device transmit FIFO empty, and flow control applied
R_IP$_P$	HOLD$_P$	Host receives and decodes HOLD$_P$ flow control
HOLDA$_P$	HOLD$_P$	Host acknowledges flow control. Device internally deadlocked and no more data forthcoming (drive hung)
HOLDA$_P$	HOLD$_P$	
…	…	System in this state until host decides to reset drive
HOLDA$_P$	HOLD$_P$	Host detects SRST write to Device Control register, needs to break deadlock
SYNC$_P$	HOLD$_P$	Host transmits SYNC$_P$ primitive to abort current transmission
SYNC$_P$	HOLD$_P$	Device receives and decodes SYNC$_P$, abandons transmission in progress
SYNC$_P$	SYNC$_P$	Host sends SYNC$_P$ / Device sends SYNC$_P$ (both returned to idle state)
SYNC$_P$	SYNC$_P$	Host receives and decodes SYNC$_P$, can now initiate new FIS transmission
X_RDY$_P$	SYNC$_P$	Host ready to send Shadow register block registers for SRST write
X_RDY$_P$	SYNC$_P$	Device decodes X_RDY$_P$
X_RDY$_P$	R_RDY$_P$	Device indicates ready to receive
X_RDY$_P$	R_RDY$_P$	Host decodes R_RDY$_P$
SOF$_P$	R_RDY$_P$	Host starts a frame
etc	etc	etc

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Table 37 – Command Shadow Register Block register transmission example

Host	Device	Description
$SYNC_P$	$SYNC_P$	Idle condition
$SYNC_P$	$SYNC_P$	Idle condition
X_RDY_P	$SYNC_P$	Host ready to send Shadow register block registers
X_RDY_P	$SYNC_P$	Device decodes X_RDY_P
X_RDY_P	R_RDY_P	Device indicates ready to receive
X_RDY_P	R_RDY_P	Host decodes R_RDY_P
SOF_P	R_RDY_P	Host starts a frame
DATA 0	R_RDY_P	Host sends Register FIS Dword 0 / device decodes SOF_P
DATA 1	R_IP_P	Host sends Register FIS Dword 1 / device stores DATA Dword 0
…	…	…
DATA n	R_IP_P	Host sends Register FIS Dword n / device stores DATA Dword n-1
CRC	R_IP_P	Host sends CRC / device stores DATA Dword n
EOF_P	R_IP_P	Host sends EOF_P / device stores CRC
$WTRM_P$	R_IP_P	Device decodes EOF_P
$WTRM_P$	R_IP_P	Device computes good CRC and releases TF contents
$WTRM_P$	R_OK_P	Device sends good end
$WTRM_P$	R_OK_P	Host decodes R_OK_P as good results
$SYNC_P$	R_OK_P	Host releases interface
$SYNC_P$	R_OK_P	Device decodes release by host - is allowed to release
$SYNC_P$	$SYNC_P$	Idle condition

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Table 38 – Data from host to device transmission example

Host	Device	Description
$SYNC_P$	$SYNC_P$	Idle condition
$SYNC_P$	$SYNC_P$	Idle condition
X_RDY_P	$SYNC_P$	Host ready to send Shadow register block registers
X_RDY_P	$SYNC_P$	Device decodes X_RDY_P
X_RDY_P	R_RDY_P	Device indicates ready to receive
X_RDY_P	R_RDY_P	Host decodes R_RDY_P
SOF_P	R_RDY_P	Host starts a frame
DATA 0	R_RDY_P	Host sends DATA Dword 0 / device decodes SOF_P
DATA 1	R_IP_P	Host sends DATA Dword 1 / device stores DATA Dword 0
...	..	...
DATA x	R_IP_P	Host sends DATA Dword x / device stores DATA Dword (x-1)
$HOLD_P$	R_IP_P	Host sends HOLD / device stores DATA Dword (x) and decodes $HOLD_P$
$HOLD_P$	$HOLDA_P$	Device acknowledges $HOLD_P$
$HOLD_P$	$HOLDA_P$	Host decodes $HOLDA_P$ – host may release $HOLD_P$ at any time
DATA(n-2)	$HOLDA_P$	Host sends (n-2)th DATA Dword / device decodes DATA Dword
DATA(n-1)	R_IP_P	Host sends (n-1)th data Dword / device stores (n-2)th DATA Dword
DATA(n)	R_IP_P	Host sends nth data Dword / device stores (n-1)th DATA Dword
CRC	R_IP_P	Host sends CRC / device stores nth DATA Dword
EOF_P	R_IP_P	Host sends EOF_P / device stores CRC
$WTRM_P$	R_IP_P	Device decodes EOF_P
$WTRM_P$	R_IP_P	Device computes good CRC and releases data contents
$WTRM_P$	R_OK_P	Device sends good end
$WTRM_P$	R_OK_P	Host decodes R_OK_P as good results
$SYNC_P$	R_OK_P	Host releases interface
$SYNC_P$	R_OK_P	Device decodes release by host - is allowed to release
$SYNC_P$	$SYNC_P$	Idle condition

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9.5 CRC and scrambling

The CRC (Cyclic Redundancy Check) of a frame is a Dword (32-bit) field that shall follow the last Dword of the contents of a FIS and precede the EOF_P primitive. The CRC calculation covers all of the FIS transport data between the SOF_P and EOF_P primitives, and excludes any intervening primitives and $CONT_P$ stream contents. The CRC value shall be computed on the contents of the FIS before encoding for transmission (scrambling) and after decoding upon reception.

The CRC shall be calculated on Dword quantities. If a FIS contains an odd number of words the last word of the FIS shall be padded with zeros to a full Dword before the Dword is used in the calculation of the CRC.

The CRC shall be aligned on a Dword boundary.

The CRC shall be calculated using the following 32-bit generator polynomial:

$$G(X) = X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$$

The CRC value shall be initialized with a value of 52325032h before the calculation begins.

The maximum number of Dwords between the SOF_P primitive to the EOF_P primitive shall not exceed 2064 Dwords including the FIS type and CRC..

The contents of a frame shall be scrambled before transmission by the physical layer.

Scrambling shall be performed on Dword quantities by XORing the data to be transmitted with the output of a linear feedback shift register (LFSR). The shift register shall implement the following polynomial:

$$G(X) = X^{16} + X^{15} + X^{13} + X^4 + 1$$

The serial shift register shall be initialized with the seed value of FFFFh before the first shift of the LFSR. The shift register shall be initialized to the seed value before the SOF_P primitive is transmitted. All data words between the SOF_P and EOF_P shall be scrambled, including the CRC.

9.5.1 Relationship between scrambling of FIS data and repeated primitives

There are two separate scramblers used in Serial ATA. One scrambler is used for the data payload encoding and a separate scrambler is used for repeated primitive suppression. The scrambler used for data payload encoding shall maintain consistent and contiguous context over the scrambled payload characters of a frame (between SOF_P and EOF_P), and shall not have its context affected by the scrambling of data used for repeated primitive suppression.

Scrambling is applied to all data (non-primitive) Dwords. Primitives, including $ALIGN_P$, do not get scrambled and shall not advance the data payload LFSR register. Similarly, the data payload LFSR shall not be advanced during transmission of Dwords during repeated primitive suppression (i.e. after a $CONT_P$ primitive). Since it is possible for a repeated primitive stream to occur in the middle of a data frame – multiple $HOLD_P$/$HOLDA_P$ primitives are likely – care should be taken to insure that the data payload LFSR is only advanced for each data payload character that it scrambles and that it is not advanced for primitives or for data characters transmitted as part of repeated primitive suppression which uses a separate scrambler.

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9.5.2 Relationship between scrambling and CRC

The order of application of scrambling shall be as follows. For a Dword of data following the SOF_P primitive the Dword shall be used in the calculation of the CRC. The same Dword value shall be XORed with the scrambler output, and the resulting Dword submitted to the 8b/10b encoder for transmission. Similarly, on reception, the Dword shall be decoded using a 10b/8b decoder, the scrambler output shall be XORed with the resulting Dword, and the resulting Dword presented to the Link layer and subsequently used in calculating the CRC. The CRC Dword shall be scrambled according to the same rules.

9.5.3 Scrambling Disable (Informative)

Hosts and devices should provide a vendor-specific means of disabling the transmission/reception of scrambled data. Three independent controls are recommended – one to disable the scrambling of transmitted FIS payload data, the second to disable the $CONT_P$/junk method of repeated primitive suppression, and the third to disable the unscrambling of received FIS payload data.

Using the scrambling disable capabilities is intended for testability and design debug, and not recommended as an end-user feature. It is the responsibility of the engineer/operator to ensure that both ends of the cable are configured in such a way that the host and device can communicate (i.e. if scrambled transmission is disabled on the device then scrambled reception shall be disabled on the host). Devices that disable payload scrambling may not interoperate with other devices that do not implement this recommendation. Systems that disable scrambling may not meet EMI regulatory requirements.

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9.6 Link layer state machine

9.6.1 Terms used in Link layer transition tables

1. LRESET: Link layer COMRESET or COMINIT signal
2. PHYRDYn: The negation of the PHYRDY signal.
3. PHYRDY: Phy status as defined in section 7.1.2.
4. DecErr: Bad decode of a 32 bit Dword transferred from Phy to Link
   - Invalid 10b pattern
   - Disparity error
   - Primitive with a control character in the first byte but not an allowed control character
   - Any control character in other than the first byte of the Dword
5. DatDword: A 32 bit pattern that is formed correctly, but does not have the primitive leading 10b pattern (K28.5 or K28.3).
6. COMWAKE: Signal from the OOB detector in the Phy indicating that the COMWAKE OOB signal is being detected.
7. AnyDword: A 32 bit pattern of any type - even one with DecErr received from Phy

9.6.2 Link idle state diagram

L1: L_IDLE[4]	Transmit $SYNC_P$	
1. Transport layer requests frame transmission and PHYRDY[2]	→	HL_SendChkRdy or DL_SendChkRdy[1]
2. Transport layer requests transition to Partial and PHYRDY[2]	→	L_TPMPartial
3. Transport layer requests transition to Slumber and PHYRDY[2]	→	L_TPMSlumber
4. X_RDY_P received from Phy	→	L_RcvWaitFifo
5. Phy layer forwards ($PMREQ\_P_P$ or $PMREQ\_S_P$) and power modes are enabled and acceptable	→	L_PMOff
6. Phy layer forwards ($PMREQ\_P_P$ or $PMREQ\_S_P$) and power modes are disabled or are unacceptable	→	L_PMDeny
7. Phy layer forwards AnyDword other than (X_RDY_P or $PMREQ\_P_P$ or $PMREQ\_S_P$) and no transmit request from Transport layer[2,3]	→	L_IDLE
8. PHYRDYn	→	L_NoCommErr

NOTE:
1. The host Link layer makes a transition to the HL_SendChkRdy state; the device Link layer makes a transition to the DL_SendChkRdy state.
2. This transition is taken even if errors such as 10b decoding errors are detected.
3. This statement also ignores any unrecognized sequences or commands not defined in this specification.
4. Upon entry to this state from the LS3:L_SendAlign state or the LPM8:L_WakeUp2 state, use of the $CONT_P$ primitive is not allowed until either a minimum of 10 non-$ALIGN_P$ primitives have been transmitted or until receipt of a primitive other than $SYNC_P$ or $ALIGN_P$ has been detected.

L2: L_SyncEscape[1]	Transmit $SYNC_P$	
1. AnyDword other than X_RDY_P or $SYNC_P$ received from Phy	→	L_SyncEscape
2. X_RDY_P or $SYNC_P$ received from Phy	→	L_IDLE
3. PHYRDYn	→	L_NoCommErr[2]

NOTE:
1. This state is entered asynchronously from any other Link layer state where the Link layer has transmitted a $SYNC_P$ primitive to escape a FIS transfer, also known as a SYNC Escape.
2. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer.

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LS1: L_NoCommErr	Post Phy not ready error to Transport layer		
	1. Unconditional	→	L_NoComm

LS2: L_NoComm	Transmit $ALIGN_P$[1]		
	1. PHYRDYn	→	L_NoComm
	2. PHYRDY	→	L_SendAlign
	NOTE: 1. Also deactivate any signal for Phy layer to abort operation.		

LS3: L_SendAlign	Transmit $ALIGN_P$		
	1. PHYRDYn	→	L_NoCommErr
	2. PHYRDY	→	L_IDLE

LS4: L_RESET[1]	Reset Link state to initial conditions		
	1. LRESET Link reset signal asserted	→	L_RESET
	2. LRESET Link reset signal deasserted	→	L_NoComm
	NOTE: 1. This state is entered asynchronously when the link reset control is active.		

L1: L_IDLE state: This state is entered when a frame transmission has been completed by the Link layer.

When in this state, the Link layer transmits the $SYNC_P$ primitive and waits for an X_RDY_P primitive from the Phy layer or a frame transmission request from the Transport layer.

Transition L1:1a: When the host Link layer receives a request to transmit a frame from the Transport layer and the Phy layer is ready, the Link layer shall make a transition to the LT1: HL_SendChkRdy state.

Transition L1:1b: When the device Link layer receives a request to transmit a frame from the Transport layer and the Phy layer is ready, the Link layer shall make a transition to the LT2: DL_SendChkRdy state.

Transition L1:2: When the Link layer receives a request to enter the Partial power mode from the Transport layer and the Phy layer is ready, the Link layer shall make a transition to the L_TPMPartial state.

Transition L1:3: When the Link layer receives a request to enter the Slumber power mode from the Transport layer and the Phy layer is ready, the Link layer shall make a transition to the L_TPMSlumber state.

Transition L1:4: When the Link layer receives an X_RDY_P from the Phy layer, the Link layer shall make a transition to the LR2: L_RcvWaitFifo state.

Transition L1:5: When the Link layer receives a $PMREQ\_P_P$ or $PMREQ\_S_P$ from the Phy layer,is enabled to perform power management modes, and in a state to accept power mode requests, the Link layer shall make a transition to the LPM3: L_PMOff state.

Transition L1:6: When the Link layer receives a $PMREQ\_P_P$ or a $PMREQ\_S_P$ from the Phy layer and is not enabled to perform power management modes or is not in a state to accept power

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mode requests, the Link layer shall make a transition to the LR0: L_PMDeny state. This transition is still valid if interface power states are supported and enabled as verified by Word 76 bit 9 set to one in IDENTIFY (PACKET) DEVICE data.

Transition L1:7: When the Link layer does not receive a request to transmit a frame from the Transport layer, does not receive a request to go to a power mode from the Transport layer, does not receive an X_RDY_P from the Phy layer or does not receive a PMREQ_x from the Phy layer the Link layer shall make a transition to the L1: L_IDLE state.

Transition L1:8: If the Phy layer becomes not ready even if the Transport layer is requesting an operation, the Link layer transitions to the L_NoCommErr state.

L2: L_SyncEscape state: This state is entered when the Link layer transmits a $SYNC_P$ primitive to escape a FIS transmission. The Link layer may choose to escape a FIS transmission due to a request from the Transport layer or due to an invalid state transition. This state is only entered by the initiator of the SYNC Escape.

When in this state, the Link layer transmits the $SYNC_P$ primitive and waits for a $SYNC_P$ primitive from the Phy layer before proceeding to L_IDLE. The Link layer also transitions to L_IDLE if an X_RDY_P primitive is received in order to avoid a deadlock condition.

Transition L2:1: When the Link layer receives any Dword from the Phy that is not an X_RDY_P or a $SYNC_P$ primitive, the Link layer shall make a transition to the L2: L_SyncEscape state.

Transition L2:2: When the Link layer receives an X_RDY_P or a $SYNC_P$ primitive from the Phy, the Link layer shall make a transition to the L1: L_IDLE state.

Transition L2:3: When the host Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

LS1: L_NoCommErr state: This state is entered upon detection of a non ready condition of the Phy layer while attempting to process another state. The entry into this state heralds a relatively serious error condition in the Link layer. This state is executed only once so as to pass on the error condition up to the Transport layer.

Transition LS1:1: The transition is made to LS1:L_NoComm unconditionally.

LS2: L_NoComm state: This state is entered directly from the LS1:L_NoCommErr state or the LS4:L_RESET State. The Link Layer remains in this state until the Phy signals that it has established communications and is ready.

Transition LS2:1: For as long as the Phy layer stays not ready, the transition is made to LS2: L_NoComm.

Transition LS2:2: When the Phy layer signals it is ready, a transition is made to LS3: L_SendAlign.

LS3: L_SendAlign state: This state is entered whenever an $ALIGN_P$ needs to be sent to the Phy layer.

Transition LS3:1: If the Phy layer becomes not ready, then a transition is made to LS1: L_NoCommErr.

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Transition LS3:2: If the Phy indicates that it is ready, a transition is made to the L1: L_IDLE state.

LS4: L_RESET state: This state is entered whenever the Link LRESET control is active. All Link layer hardware is initialized to and held at a known state/value. While in this state all requests or triggers from other layers are ignored. While in this state, the Phy reset signal is also asserted.

Transition LS4:1: While the RESET control is active a transition is made back to the LS4: L_RESET state.

Transition LS4:2: When the RESET control goes inactive a transition is made to the LS2: L_NoComm state.

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9.6.3 Link transmit state diagram

LT1: HL_SendChkRdy	Transmit X_RDY_P	
1. R_RDY_P received from Phy	→	L_SendSOF
2. X_RDY_P received from Phy	→	L_RcvWaitFifo
3. AnyDword other than (R_RDY_P or X_RDY_P)[1] received from Phy layer	→	HL_SendChkRdy
4. PHYRDYn	→	L_NoCommErr[2]
NOTE: 1. Any received errors such as 10b decoding errors and invalid primitives are ignored 2. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer		

LT2: DL_SendChkRdy	Transmit X_RDY_P	
1. R_RDY_P received from Phy	→	L_SendSOF
2. AnyDword other than R_RDY_P received from Phy	→	DL_SendChkRdy
3. PHYRDYn	→	L_NoCommErr

LT3: L_SendSOF	Transmit SOF_P	
1. PHYRDY[1]	→	L_SendData
2. PHYRDYn	→	L_NoCommErr[2]
3. $SYNC_P$ received from Phy	→	L_IDLE[2]
NOTE: 1. Any received errors such as 10b decoding errors and invalid primitives are ignored 2. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer		

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LT4: L_SendData	Transmit data Dword		
1.	More data to transmit and AnyDword other than ($HOLD_P$ or $DMAT_P$ or $SYNC_P$) received from Phy[1,2]	→	L_SendData
2.	More data to transmit and $HOLD_P$ received from Phy	→	L_RcvrHold
3.	Data transmit not complete and data not ready to transmit and AnyDword other than $SYNC_P$ received from Phy	→	L_SendHold
4.	$DMAT_P$ received from Phy or data transmit complete and AnyDword other than $SYNC_P$ received from Phy	→	L_SendCRC[5]
5.	$SYNC_P$ received from Phy	→	L_IDLE[3]
6.	PHYRDYn	→	L_NoCommErr[3]
7.	Transport Layer indicates request to escape current frame[4]	→	L_SyncEscape

NOTE:
1. Any received errors such as 10b decoding errors and invalid primitives are ignored
2. This makes possible a back channel during this time
3. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer.
4. When this condition is true, the associated transition has priority over all other transitions exiting this state.
5. The $DMAT_P$ signal is advisory and data transmission should be halted at the earliest opportunity but is not required to cease immediately. It is allowable to stay in the LT4: L_SendData state when there is more data to transmit and $DMAT_P$ is received.

LT5: L_RcvrHold	Transmit $HOLDA_P$		
1.	More data to transmit and AnyDword other than ($HOLD_P$ or $SYNC_P$ or $DMAT_P$) received from Phy with no DecErr	→	L_SendData
2.	More data to transmit and $HOLD_P$ received from Phy or DecErr	→	L_RcvrHold
3.	More data to transmit and $SYNC_P$ received from Phy	→	L_IDLE[1]
4.	More data to transmit and $DMAT_P$ received from Phy	→	L_SendCRC[3]
5.	PHYRDYn	→	L_NoCommErr[1]
6.	Transport Layer indicates request to escape current frame[2]	→	L_SyncEscape
7.	$SYNC_P$ received from Phy	→	L_IDLE[1]

NOTE:
1. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer
2. When this condition is true, the associated transition has priority over all other transitions exiting this state.
3. The $DMAT_P$ signal is advisory and data transmission should be halted at the earliest opportunity but is not required to cease immediately. It is allowable to stay in the LT5: L_RcvrHold state when there is more data to transmit and $DMAT_P$ is received.

LT6: L_SendHold	Transmit $HOLD_P$	
1. More data ready to transmit and AnyDword other than ($HOLD_P$ or $SYNC_P$) received from Phy	→	L_SendData
2. More data ready to transmit and $HOLD_P$ received from Phy	→	L_RcvrHold
3. Data transmit not complete and data not ready to transmit and AnyDword other than ($SYNC_P$ or $DMAT_P$) received from Phy	→	L_SendHold
4. $DMAT_P$ received from Phy	→	L_SendCRC[3]
5. $SYNC_P$ received from Phy	→	L_IDLE[1]
6. PHYRDYn	→	L_NoCommErr[1]
7. Transport Layer indicates request to escape current frame[2]	→	L_SyncEscape

NOTE:
1. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer.
2. When this condition is true, the associated transition has priority over all other transitions exiting this state.
3. The $DMAT_P$ signal is advisory and data transmission should be halted at the earliest opportunity but is not required to cease immediately. It is allowable to stay in the LT6: L_SendHold state when there is more data to transmit and $DMAT_P$ is received.

LT7: L_SendCRC	Transmit CRC	
1. PHYRDY and $SYNC_P$ not received from Phy	→	L_SendEOF
2. PHYRDYn	→	L_NoCommErr[1]
3. PHYRDY and $SYNC_P$ received from Phy	→	L_IDLE[1]

NOTE:
1. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer.

LT8: L_SendEOF	Transmit EOF_P	
1. PHYRDY and $SYNC_P$ not received from Phy	→	L_Wait
2. PHYRDYn	→	L_NoCommErr[1]
3. PHYRDY and $SYNC_P$ received from Phy	→	L_IDLE[1]

NOTE:
1. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer.

LT9: L_Wait	Transmit $WTRM_P$	
1. R_OK_P received from Phy	→	L_IDLE (good status)
2. R_ERR_P received from Phy	→	L_IDLE (bad status)
3. $SYNC_P$ received from Phy	→	L_IDLE[1]
4. AnyDword other than (R_OK_P or R_ERR_P or $SYNC_P$) received from Phy	→	L_Wait
5. PHYRDYn	→	L_NoCommErr[1]
NOTE: 1. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer.		

LT1: HL_SendChkRdy state: This state is entered when a frame transmission has been requested by the host Transport layer.

When in this state, the Link layer transmits an X_RDY_P primitive and waits for an X_RDY_P primitive or R_RDY_P primitive from the Phy layer.

NOTE – It is possible that both the host and the device simultaneously request frame transmission by transmitting X_RDY_P. If the host receives X_RDY_P while transmitting X_RDY_P, the host shall back off and enter the L_RcvChkRdy state, postponing its desired frame transmission until the device has completed its frame transmission and the bus is idle.

Transition LT1:1: When the host Link layer receives an R_RDY_P primitive from the Phy layer, the Link layer shall make a transition to the LT3: L_SendSOF state.

Transition LT1:2: When the host Link layer receives an X_RDY_P primitive from the Phy layer, the Link layer shall make a transition to the LR2: L_RcvWaitFifo state.

Transition LT1:3: When the host Link layer receives any Dword other than an R_RDY_P or an X_RDY_P primitive from the Phy layer, the Link layer shall make a transition to the LT1: HL_SendChkRdy state.

Transition LT1:4: When the host Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

LT2: DL_SendChkRdy state: This state is entered when a frame transmission has been requested by the device Transport layer.

When in this state, the Link layer transmits an X_RDY_P primitive and waits for an R_RDY_P primitive from the Phy layer.

Transition LT2:1: When the device Link layer receives an R_RDY_P primitive from the Phy layer, the Link layer shall make a transition to the LT3: L_SendSOF state.

Transition LT2:2: When the device Link layer does not receive an R_RDY_P primitive from the Phy layer, the Link layer shall make a transition to the LT2: DL_SendChkRdy state.

Transition LT2:3: When the device Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

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LT3: L_SendSOF state: This state is entered an R_RDY_P primitive has been received from the Phy layer.

When in this state, the Link layer transmits an SOF_P primitive.

Transition LT3:1: When the device Link layer has transmitted an SOF_P primitive, the Link layer shall make a transition to the LT4: L_SendDATA state.

Transition LT3:2: When the Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

Transition LT3:3: When the Link layer receives a $SYNC_P$ primitive from the Phy layer, the Link layer shall notify the Transport layer of the illegal transition error condition and shall make a transition to the L1:L_IDLE state.

LT4: L_SendData state: This state is entered when an SOF_P primitive has been transmitted.

When in this state, the Link layer takes a data Dword from the Transport layer, encodes the Dword, and transmits it. The Dword is also entered into the CRC calculation before encoding.

Transition LT4:1: When the Link layer receives any Dword other than a $HOLD_P$, $DMAT_P$, or $SYNC_P$ primitive from the Phy layer and the Transport layer indicates a Dword is available for transfer, the Link layer shall make a transition to the LT4: L_SendData state. The $DMAT_P$ signal is advisory and data transmission should be halted at the earliest opportunity but is not required to cease immediately. It is therefore allowable to stay in the LT4: L_SendData state when there is more data to transmit and $DMAT_P$ is received.

Transition LT4:2: When the device Link layer receives a $HOLD_P$ primitive from the Phy layer, the Link layer shall make a transition to the LT5: L_RcvrHold state.

Transition LT4:3: When the Transport layer indicates that the next Dword is not available to transfer and any Dword other than a $SYNC_P$ primitive has been received from the Phy layer, the Link layer shall make a transition to the LT6: L_SendHold state.

Transition LT4:4: When the Transport layer indicates that all data for the frame has been transferred and any Dword other than a $SYNC_P$ primitive has been received from the Phy layer, the Link layer shall make a transition to the LT7: L_SendCRC state. When the Link layer receives a $DMAT_P$ primitive from the Phy layer, it shall notify the Transport layer and terminate the transmission in progress as described in section 7.4.4 and shall transition to the LT7: L_SendCRC state.

Transition LT4:5: When the Link layer receives a $SYNC_P$ primitive from the Phy layer, the Link layer shall notify the Transport layer of the illegal transition error condition and shall make a transition to the L1:L_IDLE state
Transition LT4:6: When the Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

Transition LT4:7: When the Link layer receives notification from the Transport layer that the current frame transfer should be escaped, a transition to the L_SyncEscape state shall be made.

LT5: L_RcvrHold state: This state is entered when a $HOLD_P$ primitive has been received from the Phy layer.

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When in this state, the Link layer shall transmit the $HOLDA_P$ primitive.

Transition LT5:1: When the Link layer receives any Dword other than a $HOLD_P$, $SYNC_P$, or a $DMAT_P$ primitive from the Phy layer with no decoding error detected, and the Transport layer indicates that a Dword is available for transfer, the Link layer shall make a transition to the LT4: L_SendData state.

Transition LT5:2: When the device Link layer receives a $HOLD_P$ primitive from the Phy layer or a decoding error was detected, the Link layer shall make a transition to the LT5: L_RcvrHold state.

Transition LT5:3: When the Link layer receives a $SYNC_P$ primitive from the Phy layer, the Link layer shall make a transition to the L1: L_IDLE state. The Transport layer shall be notified of the illegal transition error condition.

Transition LT5:4: When the Link layer receives a $DMAT_P$ primitive from the Phy layer, it shall notify the Transport layer and terminate the transmission in progress as described in section 9.4.4 and shall transition to the LT7: L_SendCRC state.

Transition LT5:5: When the Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

Transition LT5:6: When the Link layer receives notification from the Transport layer that the current frame should be escaped, a transition to the L_SyncEscape state shall be made.

Transition LT5:7: When the Link layer receives a $SYNC_P$ primitive from the Phy layer, the Link layer shall notify the Transport layer of the illegal transition error condition and shall make a transition to the L1:L_IDLE state.

LT6: L_SendHold state: This state is entered when the Transport layer indicates a Dword is not available for transfer and a $HOLD_P$ primitive has not been received from the Phy layer.

When in this state, the Link layer shall transmit the $HOLD_P$ primitive.

Transition LT6:1: When the Link layer receives any Dword other than a $HOLD_P$ or $SYNC_P$ primitive from the Phy layer and the Transport layer indicates that a Dword is available for transfer, the Link layer shall make a transition to the LT4: L_SendData state.

Transition LT6:2: When the Link layer receives a $HOLD_P$ primitive from the Phy layer and the Transport layer indicates a Dword is available for transfer, the Link layer shall make a transition to the LT5: L_RcvrHold state.

Transition LT6:3: When the Transport layer indicates that a Dword is not available for transfer and any Dword other than a $SYNC_P$ primitive is received from the Phy layer, the Link layer shall make a transition to the LT6: L_SendHold state.

Transition LT6:4: When the Link layer receives a $DMAT_P$ primitive from the Phy layer, it shall notify the Transport layer and terminate the transmission in progress as described in section 9.4.4 and shall transition to the LT7:L_SendCRC state.

Transition LT6:5: When the Link layer receives a $SYNC_P$ primitive from the Phy layer, the Link layer shall make a transition to the L1: L_IDLE state. The Transport layer shall be notified of the illegal transition error condition.

Transition LT6:6: When the Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

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Transition LT6:7: When the Link layer receives notification from the Transport layer that the current frame should be escaped, a transition to the L_SyncEscape state shall be made.

LT7: L_SendCRC state: This state is entered when the Transport layer indicates that all data Dwords have been transferred for this frame.

When in this state, the Link layer shall transmit the calculated CRC for the frame.

Transition LT7:1: When the CRC has been transmitted, the Link layer shall make a transition to the LT8: L_SendEOF state.

Transition LT7:2: When the Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

Transition LT7:3: When the Link layer receives a $SYNC_P$ primitive from the Phy layer, the Link layer shall notify the Transport layer of the illegal transition error condition and shall make a transition to the L1:L_IDLE state.

LT8: L_SendEOF state: This state is entered when the CRC for the frame has been transmitted.

When in this state, the Link layer shall transmit the EOF_P primitive.

Transition LT8:1: When the EOF_P primitive has been transmitted, the Link layer shall make a transition to the LT9: L_Wait state.

Transition LT8:2: When the Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

Transition LT8:3: When the Link layer receives a $SYNC_P$ primitive from the Phy layer, the Link layer shall notify the Transport layer of the illegal transition error condition and shall make a transition to the L1:L_IDLE state.

LT9: L_Wait state: This state is entered when the EOF_P primitive has been transmitted.

When in this state, the Link layer shall transmit the $WTRM_P$ primitive.

Transition LT9:1: When the Link layer receives an R_OK_P primitive from the Phy layer, the Link layer shall notify the Transport layer and make a transition to the L1: L_IDLE state.

Transition LT9:2: When the Link layer receives an R_ERR_P primitive from the Phy layer, the Link layer shall notify the Transport layer and make a transition to the L1: L_IDLE state.

Transition LT9:3: When the Link layer receives a $SYNC_P$ primitive from the Phy layer, the Link layer shall notify the Transport layer and make a transition to the L1: L_IDLE state.

Transition LT9:4: When the Link layer receives any Dword other than an R_OK_P, R_ERR_P, or $SYNC_P$ primitive from the Phy layer, the Link layer shall make a transition to the LT9: L_Wait state.

Transition LT9:5: When the Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

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9.6.4 Link receive state diagram

LR1: L_RcvChkRdy	Transmit R_RDY_P	
1. X_RDY_P received from Phy	→	L_RcvChkRdy
2. SOF_P received from Phy	→	L_RcvData
3. Any Dword other than (X_RDY_P or SOF_P) received from Phy	→	L_IDLE
4. PHYRDYn	→	L_NoCommErr[1]
NOTE: 1. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer.		

LR2: L_ RcvWaitFifo	Transmit $SYNC_P$	
1. X_RDY_P received from Phy and FIFO space available	→	L_RcvChkRdy
2. X_RDY_P received from Phy and FIFO space not available	→	L_RcvWaitFifo
3. Any Dword other than X_RDY_P received from Phy	→	L_IDLE
4. PHYRDYn	→	L_NoCommErr[1]
NOTE: 1. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer.		

LR3: L_RcvData	Transmit R_IP_P or $DMAT_P$[1]	
1. (DatDword received from Phy and FIFO space) or $HOLDA_P$ received from Phy	→	L_RcvData
2. DatDword received from Phy and insufficient FIFO space	→	L_Hold
3. $HOLD_P$ received from Phy	→	L_SendHold
4. EOF_P received from Phy	→	L_RcvEOF
5. $WTRM_P$ received from Phy	→	L_BadEnd
6. $SYNC_P$ received from Phy	→	L_IDLE
7. AnyDword other than ($HOLD_P$ or EOF_P or $HOLDA_P$ or $SYNC_P$ or $WTRM_P$) received from Phy	→	L_RcvData
8. PHYRDYn	→	L_NoCommErr[2]
9. Transport Layer indicates request to escape current frame	→	L_SyncEscape
NOTE: 1. If the Transport layer signals that it wishes to terminate the transfer, $DMAT_P$ is transmitted in place of R_IP_P. 2. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer.		

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LR4: L_Hold	Transmit $HOLD_P$	
1. FIFO space available and AnyDword other than $HOLD_P$ or EOF_P received from Phy	→	L_RcvData
2. FIFO space available and $HOLD_P$ received from Phy	→	L_SendHold
3. EOF_P received from Phy	→	L_RcvEOF
4. No FIFO space available and EOF_P not received from Phy and $SYNC_P$ not received from Phy and PHYRDY	→	L_Hold
5. PHYRDYn	→	L_NoCommErr[1]
6. $SYNC_P$ received from Phy	→	L_IDLE
7. Transport Layer indicates request to escape current frame	→	L_SyncEscape
NOTE: 1. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer.		

LR5: L_SendHold	Transmit $HOLDA_P$ or $DMAT_P$[1]	
1. AnyDword other than ($HOLD_P$ or EOF_P or $SYNC_P$) received from Phy	→	L_RcvData
2. $HOLD_P$ received from Phy	→	L_SendHold
3. EOF_P received from Phy	→	L_RcvEOF
4. $SYNC_P$ received from Phy	→	L_IDLE
5. PHYRDYn	→	L_NoCommErr[2]
6. Transport Layer indicates request to escape current frame	→	L_SyncEscape
NOTE: 1. If the Transport layer signals that it wishes to terminate the transfer, $DMAT_P$ is transmitted in place of $HOLDA_P$. 2. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer.		

LR6: L_RcvEOF	Transmit R_IP_P	
1. CRC check not complete	→	L_RcvEOF
2. CRC good	→	L_GoodCRC
3. CRC bad	→	L_BadEnd
4. PHYRDYn	→	L_NoCommErr

LR7: L_GoodCRC	Transmit R_IP_P	
1. Transport Layer indicated good result	→	L_GoodEnd
2. Transport Layer indicates unrecognized FIS	→	L_BadEnd
3. Transport Layer has yet to respond	→	L_GoodCRC
4. PHYRDYn	→	L_NoCommErr
5. Transport or Link Layer indicated error detected during reception of recognized FIS	→	L_BadEnd
6. $SYNC_P$ received from Phy	→	L_IDLE
NOTE: 1. Upon entering this state for the first time, the Link Layer shall notify the Transport Layer that the CRC for this frame is valid.		

LR8: L_GoodEnd	Transmit R_OK_P	
1. $SYNC_P$ received from Phy	→	L_IDLE
2. AnyDword other than $SYNC_P$ received from Phy	→	L_GoodEnd
3. PHYRDYn	→	L_NoCommErr

LR9: L_BadEnd	Transmit R_ERR_P	
1. $SYNC_P$ received from Phy	→	L_IDLE
2. AnyDword other than $SYNC_P$ received from Phy	→	L_BadEnd
3. PHYRDYn	→	L_NoCommErr

LR1: L_RcvChkRdy state: This state is entered when an X_RDY_P primitive has been received from the Phy layer.

When in this state, the Link layer shall transmit an R_RDY_P primitive and wait for an SOF_P primitive from the Phy layer.

Transition LR1:1: When the Link layer receives an X_RDY_P primitive from the Phy layer, the Link layer shall make a transition to the LR1: L_RcvChkRdy state.

Transition LR1:2: When the Link layer receives an SOF_P primitive from the Phy layer, the Link layer shall make a transition to the LR2: L_RcvData state.

Transition LR1:3: When the Link layer receives any Dword other than an X_RDY_P or SOF_P primitive from the Phy layer, the Link layer shall notify the Transport layer of the condition and make a transition to the L1: L_IDLE state.

Transition LR1:4: When the Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

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LR2: L_RcvWaitFifo state: This state is entered when an X_RDY_P has been received, and the FIFO is not ready to receive a FIS.

When in this state, the Link layer shall transmit the $SYNC_P$ primitive.

Transition LR2:1: When the Link layer receives a X_RDY_P primitive from the Phy layer and the FIFO is ready to accept data, the Link layer shall make a transition to the LR1: L_RcvChkRdy state.

Transition LR2:2: When the Link layer receives a X_RDY_P primitive from the Phy layer and the FIFO is not ready to accept data, the Link layer shall make a transition to the LR2: L_RcvWaitFifo state.

Transition LR2:3: When the Link layer receives any Dword other than an X_RDY_P primitive from the Phy layer, the Link layer shall notify the Transport layer of the condition and make a transition to the L1: L_IDLE state.

Transition LR2:4: When the Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

LR3: L_RcvData state: This state is entered when an SOF_P primitive has been received from the Phy layer.

When in this state, the Link layer receives an encoded character sequence from the Phy layer, decodes it into a Dword, and passes the Dword to the Transport layer. The Dword is also entered into the CRC calculation. When in this state the Link layer either transmits a R_IP_P primitive to signal transmission to continue or transmits a $DMAT_P$ primitive to signal the transmitter to terminate the transmission.

Transition LR3:1: When the Transport layer indicates that space is available in its FIFO, the Link layer shall make a transition to the LR3: L_RcvData state.

Transition LR3:2: When the Transport layer indicates that sufficient space is not available in its FIFO, the Link layer shall make a transition to the LR4: L_Hold state.

Transition LR3:3: When the Link layer receives a $HOLD_P$ primitive from the Phy layer, the Link layer shall make a transition to the LR5: L_SendHold state.

Transition LR3:4: When the Link layer receives an EOF_P primitive from the Phy layer, the Link layer shall make a transition to the LR6: L_RcvEOF state.

Transition LR3:5: When the Link layer receives a $WTRM_P$ primitive from the Phy layer, the Link layer shall make a transition to the LR8: L_BadEnd state.

Transition LR3:6: When the Link layer receives a $SYNC_P$ primitive from the Phy layer, the Link layer shall notify the Transport layer that reception was aborted and shall make a transition to the L1: L_IDLE state.

Transition LR3:7: When the Link layer receives any Dword other than a $HOLD_P$, $HOLDA_P$, EOF_P, or $SYNC_P$ primitive from the Phy layer, the Link layer shall make a transition to the LR3: L_RcvData state.

Transition LR3:8: When the Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

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Transition LR3:9: When the Link layer receives notification from the Transport layer that the current frame should be escaped, a transition to the L_SyncEscape state shall be made.

LR4: L_Hold state: This state is entered when the Transport layer indicates that sufficient space is not available in its receive FIFO.

When in this state, the Link layer shall transmit the $HOLD_P$ primitive and may receive an encoded character from the Phy layer.

Transition LR4:1: When the Link layer receives any Dword other than a $HOLD_P$ primitive from the Phy layer and the Transport layer indicates that sufficient space is now available in its receive FIFO, the Link layer shall make a transition to the LR3: L_RcvData state.

Transition LR4:2: When the Link layer receives a $HOLD_P$ primitive from the Phy layer and the Transport layer indicates that space is now available in its FIFO, the Link layer shall make a transition to the LR5: L_SendHold state.

Transition LR4:3: When the Link layer receives an EOF_P primitive from the Phy layer, the Link layer shall make a transition to the LR6: L_RcvEOF state. Note that due to pipeline latency, an EOF_P may be received when in the L_Hold state in which case the receiving Link shall use its FIFO headroom to receive the EOF_P and close the frame reception.

Transition LR4:4: When the Transport layer indicates that there is not sufficient space available in its FIFO and the Phy layer is ready, the Link layer shall make a transition to the LR4: L_Hold state.

Transition LR4:5: When the Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

Transition LR4:6: When the Link layer receives a $SYNC_P$ primitive from the Phy layer, the Link layer shall notify the Transport layer of the illegal transition error condition and shall make a transition to the L1: L_IDLE state.

Transition LR4:7: When the Link layer receives notification from the Transport layer that the current frame should be escaped, a transition to the L_SyncEscape state shall be made.

LR5: L_SendHold state: This state is entered when a $HOLD_P$ primitive has been received from the Phy layer.

When in this state, the Link layer shall either transmit the $HOLDA_P$ primitive to signal transmission to proceed when the transmitter becomes ready or transmit a $DMAT_P$ primitive to signal the transmitter to terminate the transmission.

Transition LR5:1: When the Link layer receives any Dword other than a $HOLD_P$ or $SYNC_P$ primitive from the Phy layer, the Link layer shall make a transition to the LR3: L_RcvData state.

Transition LR5:2: When the Link layer receives a $HOLD_P$ primitive from the Phy layer, the Link layer shall make a transition to the LR5: L_SendHold state.

Transition LR5:3: When the Link layer receives an EOF_P primitive from the Phy layer, the Link layer shall make a transition to the LR6: L_RcvEOF state.

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Transition LR5:4: When the Link layer receives a $SYNC_P$ primitive from the Phy layer, the Link layer shall make a transition to the L1: L_IDLE state. The Transport layer shall be notified of the illegal transition error condition.

Transition LR5:5: When the Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

Transition LR5:6: When the Link layer receives notification from the Transport layer that the current frame should be escaped, a transition to the L_SyncEscape state shall be made.

LR6: L_RcvEOF state: This state is entered when the Link layer has received an EOF_P primitive from the Phy layer.

When in this state, the Link layer shall check the calculated CRC for the frame and transmit one or more R_IP_P primitives.

Transition LR6:1: If the CRC calculation and check is not yet completed, the Link layer shall make a transition to the LR6: L_RcvEOF state.

Transition LR6:2: When the CRC indicates no error, the Link layer shall notify the Transport layer and make a transition to the LR7: L_GoodCRC state.

Transition LR6:3: When the CRC indicates an error has occurred, the Link layer shall notify the Transport layer and make a transition to the LR8: L_BadEnd state.

Transition LR6:4: When the Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

LR7: L_GoodCRC state: This state is entered when the CRC for the frame has been checked and determined to be good.

When in this state, the Link layer shall wait for the Transport Layer to check the frame and transmit one or more R_IP_P primitives.

Transition LR7:1: When the Transport Layer indicates a good result, the Link Layer shall transition to the LR8: L_GoodEnd state.

Transition LR7:2: When the Transport Layer indicates an unrecognized FIS, the Link Layer shall transition to the LR9: L_BadEnd state.

Transition LR7:3: If the Transport Layer has not supplied status, then the Link Layer shall transition to the LR7: L_GoodCRC state.

Transition LR7:4: When the Link layer detects that the Phy layer is not ready, the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

Transition LR7:5: When the Transport layer or Link layer indicates an error was encountered during the reception of the recognized FIS, the Link layer shall transition to the LR9: L_BadEnd state.

Transition LR7:6: When the Link layer receives a $SYNC_P$ primitive from the Phy layer, the Link layer shall notify the Transport layer of the illegal transition error condition and shall make a transition to the L1: L_IDLE state.

LR8: L_GoodEnd state: This state is entered when the CRC for the frame has been checked and determined to be good.

When in this state, the Link layer shall transmit the R_OK_P primitive.

Transition LR8:1: When the Link layer receives a $SYNC_P$ primitive from the Phy layer, the Link layer shall make a transition to the L1: L_IDLE state.

Transition LR8:2: When the Link layer receives any Dword other than a $SYNC_P$ primitive from the Phy layer, the Link layer shall make a transition to the LR7: L_GoodEnd state.

Transition LR8:3: When the Link layer detects that the Phy layer is not ready, the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

LR9: L_BadEnd state: This state is entered when the CRC for the frame has been checked and determined to be bad or when the Transport layer has notified the Link layer that the received FIS is invalid.

When in this state, the Link layer shall transmit the R_ERR_P primitive.

Transition LR9:1: When the Link layer receives a $SYNC_P$ primitive from the Phy layer, the Link layer shall make a transition to the L1: L_IDLE state.

Transition LR9:2: When the Link layer receives any Dword other than a $SYNC_P$ primitive from the Phy layer, the Link layer shall make a transition to the LR8:BadEnd state.

Transition LR9:3: When the Link layer detects that the Phy layer is not ready the Link layer shall notify the Transport layer of the condition and make a transition to the LS1: L_NoCommErr state.

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9.6.5 Link power mode state diagram

LPM1: L_TPMPartial	Transmit $PMREQ\_P_P$		
	1. $PMACK_P$ received from Phy	→	L_ChkPhyRdy
	2. X_RDY_P received from Phy	→	L_RcvWaitFifo[1]
	3. $SYNC_P$ or R_OK_P received from Phy	→	L_TPMPartial
	4. AnyDword other than ($PMACK_P$ or $PMNAK_P$ or X_RDY_P or $SYNC_P$ or R_OK_P or $PMREQ\_P_P$[3] or $PMREQ\_S_P$[3])[1] received from Phy layer	→	L_IDLE
	5. $PMREQ\_P_P$ or $PMREQ\_S_P$ received from Phy	→	L_TPMPartial[3]
	6. PHYRDYn	→	L_NoCommErr[2]
	7. $PMNAK_P$ received from Phy	→	L_NoPmnak
	NOTE: 1. This transition aborts the request from the Transport layer to enter a power mode. A status indication to the Transport layer of this event is required 2. This is an unexpected transition and constitutes an error condition. An error condition needs to be sent to the Transport layer as a result. 3. If $PMREQ\_P_P$ or $PMREQ\_S_P$ is received, the host shall make a transition to the L_IDLE state, but the device shall make a transition to the L_TPMPartial state.		

LPM2: L_TPMSlumber	Transmit $PMREQ\_S_P$		
	1. $PMACK_P$ received from Phy	→	L_ChkPhyRdy
	2. X_RDY_P received from Phy	→	L_RcvWaitFifo[1]
	3. $SYNC_P$ or R_OK_P received from Phy	→	L_TPMSlumber
	4. AnyDword other than ($PMACK_P$ or $PMNAK_P$ or X_RDY_P or $SYNC_P$ or R_OK_P or $PMREQ\_P_P$[3] or $PMREQ\_S_P$[3])[1] received from Phy layer	→	L_IDLE
	5. $PMREQ\_P_P$ or $PMREQ\_S_P$ received from Phy	→	L_TPMSlumber[3]
	6. PHYRDYn	→	L_NoCommErr[2]
	7. $PMNAK_P$ received from Phy	→	L_NoPmnak
	NOTE: 1. This transition aborts the request from the Transport layer to enter a power mode. A status indication to the Transport layer of this event is required 2. This is an unexpected transition and constitutes an error condition. An error condition needs to be sent to the Transport layer as a result. 3. If $PMREQ\_P_P$ or $PMREQ\_S_P$ is received, the host shall make a transition to the L_IDLE state, but the device shall make a transition to the L_TPMSlumber state.		

LPM3: L_PMOff	Transmit $PMACK_P$[1]		
	1. A total of 4<=n<=16 $PMACK_P$ primitives sent	→	L_ChkPhyRdy
	2. Less than n $PMACK_P$ primitives sent	→	L_PMOff
	NOTE: 1. A flag is set according to whether a $PMREQ\_P_P$ or $PMREQ\_S_P$ was received from the Phy layer		

LPM4: L_PMDeny	Transmit $PMNAK_P$	
1. $PMREQ\_P_P$ or $PMREQ\_S_P$ received from Phy	→	L_PMDeny
2. AnyDword other than ($PMREQ\_P_P$ or $PMREQ\_S_P$) received from Phy layer	→	L_IDLE
3. PHYRDYn	→	L_NoCommErr

LPM5: L_ChkPhyRdy	Assert Partial/Slumber to Phy (as appropriate)	
1. PHYRDY	→	L_ChkPhyRdy
2. PHYRDYn	→	L_NoCommPower

LPM6: L_NoCommPower	Maintain Partial/Slumber assertion (as appropriate)	
1. Transport layer requests a wakeup or COMWAKE detected	→	L_WakeUp1
2. Transport layer not requesting wakeup and COMWAKE not detected	→	L_NoCommPower

LPM7: L_WakeUp1	Deassert both Partial and Slumber	
1. PHYRDY	→	L_WakeUp2
2. PHYRDYn	→	L_WakeUp1

LPM8: L_WakeUp2	Transmit $ALIGN_P$	
1. PHYRDY	→	L_IDLE
2. PHYRDYn	→	L_NoCommErr

LPM9: L_NoPmnak	Transmit $SYNC_P$	
1. $PMNAK_P$ received from Phy	→	L_NoPmnak
2. AnyDword other than ($PMNAK_P$) received from Phy	→	L_IDLE

LPM1: L_TPMPartial state: This state is entered when the Transport layer has indicated that a transition to the Partial power state is desired.

Transition LPM1:1: When in this state a $PMREQ\_P_P$ primitive shall be transmitted. When the Link layer receives a $PMACK_P$ primitive a transition to the LPM5: L_ChkPhyRdy state shall be made.

Transition LPM1:2: If the Link layer receives an X_RDY_P primitive a transition shall be made to the LR2: L_RcvWaitFifo state, effectively aborting the request to a power mode state.

Transition LPM1:3: If the Link layer receives a $SYNC_P$ or R_OK_P primitive, then it is assumed that the opposite side has not yet processed the $PMREQ\_P_P$ primitive yet and time is needed. A transition to the LPM1: L_TPMPartial state shall be made.

Transition LPM1:4: If the host Link layer receives any Dword from the Phy layer other than a $PMACK_P$, $PMNAK_P$, X_RDY_P, $SYNC_P$ or R_OK_P primitive, then the request to enter the Partial state is aborted and a transition to L1: L_IDLE shall be made. If the device Link layer receives any Dword from the Phy layer other than a $PMACK_P$, $PMNAK_P$, X_RDY_P, $SYNC_P$, $PMREQ\_P_P$, $PMREQ\_S_P$, or R_OK_P primitive, then the request to enter the Partial state is aborted and a transition to L1: L_IDLE shall be made.

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Transition LPM1:5: The host Link layer shall not make this transition as it applies only to the device Link layer. If the device Link layer receives a $PMREQ\_P_P$ or $PMREQ\_S_P$ primitive from the host, it shall remain in this state by transitioning back to LPM1: L_TPMPartial.

Transition LPM1:6: If the Link layer detects that the Phy layer has become not ready, this is interpreted as an error condition. The Transport layer shall be notified of the condition and a transition shall be made to the LS1: L_NoCommErr state.

Transition LPM1:7: If the Link layer receives a $PMNAK_P$, then the request to enter the Partial state is aborted and a transition to LPM9: L_NoPmnak shall be made.

LPM2: L_TPMSlumber state: This state is entered when the Transport layer has indicated that a transition to the Slumber power state is desired.

Transition LPM2:1: When in this state a $PMREQ\_S_P$ primitive shall be transmitted. When the Link layer receives a $PMACK_P$ primitive, a transition to the LPM5: L_ChkPhyRdy state shall be made.

Transition LPM2:2: If the Link layer receives an X_RDY_P primitive, a transition to the LR2: L_RcvWaitFifo state shall be made, effectively aborting the request to a power mode state.

Transition LPM2:3: If the Link layer receives a $SYNC_P$ or R_OK_P primitive, then it is assumed that the opposite side has not yet processed the $PMREQ\_S_P$ primitive yet and time is needed. The transition to the LPM2: L_TPMSlumber state shall be made.

Transition LPM2:4: If the host Link layer receives any Dword from the Phy layer other than a $PMACK_P$, $PMNAK_P$, X_RDY_P, $SYNC_P$, or R_OK_P primitive, then the request to enter the Slumber state is aborted and a transition to L1: L_IDLE shall be made. If the device Link layer receives any Dword from the Phy layer other than a $PMACK_P$, $PMNAK_P$, X_RDY_P, $SYNC_P$, $PMREQ\_P_P$, $PMREQ\_S_P$, or R_OK_P primitive, then the request to enter the Slumber state is aborted and a transition to L1: L_IDLE shall be made.

Transition LPM2:5: The host Link layer shall not make this transition as it applies only to the device Link layer. If the device Link layer receives a $PMREQ\_P_P$ or $PMREQ\_S_P$ primitive from the host, it shall remain in this state by transitioning back to LPM2: L_TPMSlumber.

Transition LPM2:6: If the Link layer detects that the Phy layer has become not ready, this is interpreted as an error condition. The Transport layer shall be notified of the condition and a transition shall be made to the L_NoCommErr state.

Transition LPM2:7: If the Link layer receives a $PMNAK_P$, then the request to enter the Slumber state is aborted and a transition to LPM9: L_NoPmnak shall be made.

LPM3: L_PMOff state: This state is entered when either a $PMREQ\_S_P$ or $PMREQ\_P_P$ primitive was received by the Link layer. The Link layer transmits a $PMACK_P$ primitive for each execution of this state.

Transition LPM3:1: If $4<=n<=16$ $PMACK_P$ primitives have been transmitted, a transition shall be made to the L_ChkPhyRdy state.

Transition LPM3:2: If less than n $PMACK_P$ primitives have been transmitted, a transition shall be made to L_PMOff state.

LPM4: L_PMDeny state: This state is entered when any primitive is received by the Link layer to enter a power mode and power modes are currently disabled. The Link layer shall transmit a $PMNAK_P$ primitive to inform the opposite end that a power mode is not allowed.

Transition LPM4:1: If the Link layer continues to receive a request to enter any power mode than a transition back to the same LPM4: L_PMDeny state shall be made.

Transition LPM4:2: If the Link layer receives any Dword other than a power mode request primitive, then the Link layer assumes that the power mode request has been removed and shall make a transition to the L1: L_IDLE state.

Transition LPM4:3: If the Link layer detects that the Phy layer has become not ready, this is interpreted as an error condition. The Transport layer shall be notified of the condition and a transition shall be made to the LS1: L_NoCommErr state.

LPM5: L_ChkPhyRdy state: This state is entered whenever it is desired for the Phy layer to enter a low power condition. For each execution in this state a request is made to the Phy layer to enter the state and deactivate the PHYRDY signal. Partial or Slumber is asserted to the Phy as appropriate.

Transition LPM6:1: If the Phy layer has not yet processed the request to enter the power saving state and not deactivated the PHYRDY signal, then the Link layer shall remain in the LPM5: L_ChkPhyRdy state and continue to request the Phy layer to enter the power mode state.

Transition LPM6:2: When the Phy layer has processed the power mode request and has deactivated the PHYRDY signal, then a transition shall be made to the LPM6: L_NoCommPower state.

LPM6: L_NoCommPower state: This state is entered when the Phy has deasserted its PHYRDY signal indicating that it is in either Partial or Slumber state. In this state, the Link layer waits for the OOB detector to signal reception of the COMWAKE signal (for a wakeup initiated by the other device), or for the Transport layer to request a wakeup.

Transition LPM6:1: If the Transport layer requests a wakeup or the OOB signal detector indicates reception of the COMWAKE signal, then a transition shall be made to LPM7: L_WakeUp1

Transition LPM6:2: If the Transport layer does not request a wakeup and the OOB detector does not indicate reception of the COMWAKE signal, then a transition shall be made to LPM6: L_NoCommPower.

LPM7: L_WakeUp1 state: This state is entered when the Transport layer has initiated a wakeup. In this state, the Link layer shall deassert both Partial and Slumber to the Phy, and wait for the PHYRDY signal from the Phy to be asserted. While in this state the Phy is performing the wakeup sequence.

Transition LPM7:1 When the Phy asserts its PHYRDY signal, a transition shall be made to LPM8: L_WakeUp2.

Transition LPM7:2: When the Phy remains not ready, a transition shall be made to LPM7: L_WakeUp1.

LPM8: L_WakeUp2 state: This state is entered when the Phy has acknowledged an initiated wakeup request by asserting its PHYRDY signal. In this state, the Link layer shall transmit the ALIGN sequence, and transition to the L1: L_IDLE state.

Transition LPM8:1 If the Phy keeps PHYRDY asserted, a transition shall be made to the L1: L_IDLE state.

Transition LPM8:2 If the Phy deasserts PHYRDY, this is an error condition. The Transport layer shall be notified of the condition and a transition shall be made to the LS1: L_NoCommErr state.

LPM9: L_NoPmnak state: This state is entered when the Link layer has indicated that a request to enter the Slumber or Partial state has been denied. The Link layer transmits a $SYNC_P$ primitive for each execution of this state. In this state, the Link layer waits for receipt of any Dword that is not $PMNAK_P$ from the Phy layer.

Transition LPM9:1: If the Link layer receives a $PMNAK_P$, then the Link layer shall remain in the LPM9: L_NoPmnak state and continue to wait for receipt of a primitive that is not $PMNAK_P$ from the Phy layer.

Transition LPM9:2: If the Link layer receives any Dword from the Phy layer other than $PMNAK_P$, then the request to enter the power management state is aborted and a transition to L1: L_IDLE shall be made.

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10 Transport layer

10.1 Overview

The Transport layer need not be cognizant of how frames are transmitted and received. The Transport layer simply constructs Frame Information Structures (FISes) for transmission and decomposes received Frame Information Structures. Host and device Transport layer state differ in that the source of the FIS content differs. The Transport layer maintains no context in terms of ATA commands or previous FIS content.

10.1.1 FIS construction

When requested to construct a FIS by a higher layer, the Transport layer provides the following services:

- Gathers FIS content based on the type of FIS requested.
- Places FIS content in the proper order.
- Notifies the Link layer of required frame transmission and passes FIS content to Link.
- Manages Buffer/FIFO flow, notifies Link of required flow control.
- Receives frame receipt acknowledge from Link layer.
- Reports good transmission or errors to requesting higher layer.

10.1.2 FIS decomposition

When a FIS is received from the Link layer, the Transport layer provides the following services:

- Receives the FIS from the Link layer.
- Determines FIS type.
- Distributes the FIS content to the locations indicated by the FIS type.
- For the host Transport layer, receipt of a FIS may also cause the construction of a FIS to be returned to the device.
- Reports good reception or errors to higher layer

10.2 Frame Information Structure (FIS)

10.2.1 Overview

A FIS is a group of Dwords that convey information between host and device as described previously. Primitives are used to define the boundaries of the FIS and may be inserted to control the rate of the information flow. This section describes the information content of the FIS - referred to as payload - and assumes the reader is aware of the primitives that are needed to support the information content.

The contents of the info field is divided into three categories: (1) register type, (2) setup type, and (3) data type. For each category the organization of each frame is defined in the following section.

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10.2.2 Payload content

The type and layout of the payload is indicated by the Frame Information Type field located in byte 0 of the first Dword of the payload. See Figure 158 as an example. This example type is used primarily to transfer the contents of the Shadow Register Block Registers from the host to the device. Table 39 can be referenced to refresh the reader's memory of a simplified version of the Shadow Register Block organization of an ATA adapter.

Table 39 – Simplified Shadow Register Block register numbering

				Register access operation	
	A2	**A1**	**A0**	**Read**	**Write**
CS 0 Active	0	0	0	Data Port	
	0	0	1	Error	Features
	0	1	0	Sector Count [15:8], [7:0]	
	0	1	1	LBA Low [31:24], [7:0]	
	1	0	0	LBA Mid [39:32], [15:8]	
	1	0	1	LBA High [47:40], [23:16]	
	1	1	0	Device / Head	
	1	1	1	Status	Command
CS 1 active	1	1	0	Alternate Status	Device Control

The following sections detail the types of payloads that are possible. The SOF_P, EOF_P and $HOLD_P$ primitives have been removed for clarity.

10.3 FIS Types

The following sections define the structure of each individual FIS.

10.3.1 FIS Type values

The value for the FIS Type fields of all FISes has been selected to provide additional robustness. In minimally buffered implementations that may not buffer a complete FIS, the state machines may begin acting on the received FIS Type value prior to the ending CRC having been checked. Because the FIS Type value may be acted upon prior to the integrity of the complete FIS being checked against its ending CRC, the FIS Type field values have been selected to maximize the Hamming distance between them.

Figure 157 enumerates the FIS Type values and their assignments.

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Type field value	Description
27h	Register FIS – Host to Device
34h	Register FIS – Device to Host
39h	DMA Activate FIS – Device to Host
41h	DMA Setup FIS – Bi-directional
46h	Data FIS – Bi-directional
58h	BIST Activate FIS – Bi-directional
5Fh	PIO Setup FIS – Device to Host
A1h	Set Device Bits FIS – Device to Host
A6h	Reserved for future Serial ATA definition
B8h	Reserved for future Serial ATA definition
BFh	Reserved for future Serial ATA definition
C7h	Vendor specific
D4h	Vendor specific
D9h	Reserved for future Serial ATA definition

Figure 157 – FIS type value assignments

10.3.1.1 Unrecognized FIS Types

A device or host may receive a FIS type that is not defined or vendor specific in Figure 157. The receiver of a FIS determines whether to handle a FIS type that is not defined or reserved as "unrecognized". There may be cases where a receiver accepts undefined or vendor specific FISes. The host and device should negotiate any undefined or vendor specific FIS types that may be transmitted prior to their use.

If the receiver decides to treat a FIS type as unrecognized, it shall follow the link layer state machine definitions in section 9.6 upon receipt of that FIS type.

10.3.2 CRC Errors on Data FISes

Following a Serial ATA CRC error on a Data FIS, if the device transmits a Device-to-Host FIS it shall set the ERR bit to one and both the BSY bit and DRQ bit cleared to zero in the Status field, and the ABRT bit set to one in the Error field. It is recommended for the device to also set the bit 7 (i.e. ICRC bit) to one in the Error field. See the ATA/ATAPI-8 Command Set reference.

There is no Device-to-Host FIS transmitted after a Serial ATA CRC error on the last Data FIS of a PIO-in command nor following a Serial ATA CRC error on the ATAPI command packet transfer. Thus, there is no mechanism for the device to indicate a Serial ATA CRC error to the host in either of these cases. The host should check the SError register to determine if a Link layer error has occurred in both of these cases.

10.3.3 All FIS types

In all of the following FIS structures the following rules shall apply:

1. All reserved fields shall be written or transmitted as all zeroes
2. All reserved fields shall be ignored during the reading or reception process.

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10.3.4 Register - Host to Device

0	Features	Command	C	R	R	R	PM Port	FIS Type (27h)
1	Device	LBA High	LBA Mid					LBA Low
2	Features (exp)	LBA High (exp)	LBA Mid (exp)					LBA Low (exp)
3	Control	Reserved (0)	Sector Count (exp)					Sector Count
4	Reserved (0)	Reserved (0)	Reserved (0)					Reserved (0)

Figure 158 – Register - Host to Device FIS layout

Field Definitions

FIS Type - Set to a value of 27h. Defines the rest of the FIS fields. Defines the length of the FIS as five Dwords.

C - This bit is set to one when the register transfer is due to an update of the Command register. The bit is cleared to zero when the register transfer is due to an update of the Device Control register. Setting C=1 and SRST=1 in the Device Control Field is invalid and results in indeterminate behavior.

Command - Contains the contents of the Command register of the Shadow Register Block.

LBA Low - Contains the contents of the LBA Low register of the Shadow Register Block.

Control - Contains the contents of the Device Control register of the Shadow Register Block.

LBA Mid - Contains the contents of the LBA Mid register of the Shadow Register Block.

LBA Mid (exp) – Contains the contents of the expanded address field of the Shadow Register Block

LBA High - Contains the contents of the LBA High register of the Shadow Register Block.

LBA High (exp) – Contains the contents of the expanded address field of the Shadow Register Block

Device - Contains the contents of the Device register of the Shadow Register Block.

Features - Contains the contents of the Features register of the Shadow Register Block.

Features (exp) – Contains the contents of the expanded address field of the Shadow Register Block

PM Port – When an endpoint device is attached via a Port Multiplier, specifies the device port address that the FIS should be delivered to. This field is set by the host.

R – Reserved – shall be cleared to zero.

Sector Count - Contains the contents of the Sector Count register of the Shadow Register Block.

Sector Count (exp) – Contains the contents of the expanded address field of the Shadow Register Block

LBA Low - Contains the contents of the LBA Low register of the Shadow Register Block.

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LBA Low (exp) – Contains the contents of the expanded address field of the Shadow Register Block

10.3.4.1 Description

The Register – Host to Device FIS is used to transfer the contents of the Shadow Register Block from the host to the device. This is the mechanism for issuing ATA commands to the device.

10.3.4.2 Transmission

Transmission of a Register – Host to Device FIS is initiated by a write operation to either the command register, or a write to the Device Control register with a value different than is currently in the Device Control register in the host adapter's Shadow Register Block. Upon initiating transmission, the current contents of the Shadow Register Block are transmitted and the C bit in the FIS is set according to whether the transmission was a result of the Command register being written or the Device Control register being written. The host adapter shall set the BSY bit in the shadow Status register to one within 400 ns of the write operation to the Command register that initiated the transmission. The host adapter shall set the BSY bit in the shadow Status register to one within 400 ns of a write operation to the Device Control register if the write to the Device Control register changes the state of the SRST bit from zero to one. The host adapter shall not set the BSY bit in the shadow Status register for writes to the Device Control register that do not change the state of the SRST bit from zero to one.

It is important to note that Serial ATA host adapters enforce the same access control to the Shadow Register Block as legacy (parallel) ATA devices enforce to the Command Block Registers. Specifically, the host is prohibited from writing the Features, Sector Count, LBA Low, LBA Mid, LBA High, or Device registers when either BSY or DRQ is set in the Status Register. Any write to the Command Register when BSY or DRQ is set is ignored unless the write is to issue a Device Reset command.

10.3.4.3 Reception

Upon reception of a valid Register - Host to Device FIS the device updates its local copy of the Command and Control Block Register contents. Then the device either initiates execution of the command indicated in the command register or initiates execution of the control request indicated in the Device Control register, depending on the state of the C bit in the FIS.

There are legacy BIOS and drivers that write the Device Control register to enable the interrupt just prior to issuing a command. To avoid unnecessary overhead, this FIS is transmitted to the device only upon a change of state from the previous value.

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10.3.5 Register - Device to Host

0	Error							Status							R	I	R	R	PM Port				FIS Type (34h)							
1	Device							LBA High							LBA Mid								LBA Low							
2	Reserved (0)							LBA High (exp)							LBA Mid (exp)								LBA Low (exp) (0)							
3	Reserved (0)							Reserved (0)							Sector Count (exp)								Sector Count							
4	Reserved (0)							Reserved (0)							Reserved (0)								Reserved (0)							

Figure 159 – Register - Device to Host FIS layout

Field Definitions

FIS Type - Set to a value of 34h. Defines the rest of the FIS fields. Defines the length of the FIS as five Dwords.

LBA Mid - Contains the new value of the LBA Mid register of the Shadow Register Block.

LBA Mid (exp) – Contains the contents of the expanded address field of the Shadow Register Block

LBA High - Contains the new value of the LBA High register of the Shadow Register Block.

LBA High (exp) – Contains the contents of the expanded address field of the Shadow Register Block

Device - Contains the new value of the Device register of the Shadow Register Block.

Error - Contains the new value of the Error register of the Shadow Register Block.

I - Interrupt bit. This bit reflects the interrupt bit line of the device. Devices shall not modify the behavior of this bit based on the state of the nIEN bit received in Register Host to Device FISes.

PM Port – When an endpoint device is attached via a Port Multiplier, specifies the device port address that the FIS is received from. This field is set by the Port Multiplier. Endpoint devices shall set this field to 0h.

R - Reserved, – shall be cleared to zero.

Sector Count - Contains the new value of the sector count register of the Shadow Register Block.

Sector Count (exp) – Contains the contents of the expanded address field of the Shadow Register Block

LBA Low - Contains the new value of the LBA Low register of the Shadow Register Block.

LBA Low (exp) – Contains the contents of the expanded address field of the Shadow Register Block

Status - Contains the new value of the Status (and Alternate status) register of the Shadow Register Block.

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10.3.5.1 Description

The Register – Device to Host FIS is used to by the device to update the contents of the host adapter's Shadow Register Block. This is the mechanism by which devices indicate command completion status or otherwise change the contents of the host adapter's Shadow Register Block.

10.3.5.2 Transmission

Transmission of a Register - Device to Host FIS is initiated by the device in order to update the contents of the host adapter's Shadow Register Block. Transmission of the Register - Device to Host FIS is typically as a result of command completion by the device.

The Register - Device to Host FIS shall only be used to set the SERV bit in the Status Register to request service for a bus released command if the BSY bit or the DRQ bit is currently set in the Status Register; the Set Device Bits FIS shall be used to set the SERV bit when the BSY bit and DRQ bit are both cleared to zero in the Status Register. The SERV bit transmitted with the Register - Device to Host FIS is written to the shadow Status Register and so the bit should accurately reflect the state of pending service requests when the FIS is transmitted as a result of a command completion by the device.

10.3.5.3 Reception

Upon reception of a valid Register - Device to Host FIS the received register contents are transferred to the host adapter's Shadow Register Block.

If the BSY bit and DRQ bit in the shadow Status Register are both cleared when a Register - Device to Host FIS is received by the host adapter, then the host adapter shall discard the contents of the received FIS and not update the contents of any shadow register.

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10.3.6 Set Device Bits - Device to Host

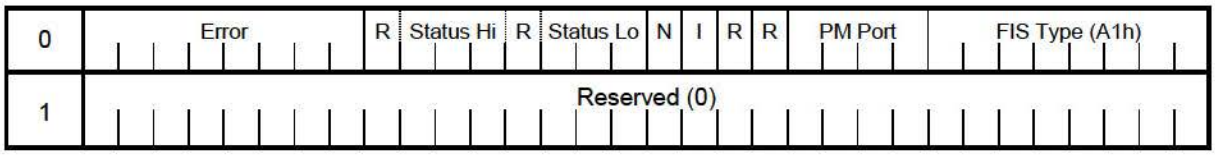


Figure 160 – Set Device Bit - Device to Host FIS layout

Field Definitions

FIS Type – Set to a value of A1h. Defines the rest of the FIS fields. Defines the length of the FIS as two Dwords.

I – Interrupt Bit. This bit signals the host adapter to enter an interrupt pending state. If the host is executing legacy queued commands (READ DMA QUEUED or WRITE DMA QUEUED) with the device, the host should only enter the interrupt pending state if both the BSY bit and the DRQ bit in the shadow Status register are zero when the frame is received. If the host is executing native queued commands (READ FPDMA QUEUED or WRITE FPDMA QUEUED) with the device, the interrupt pending state is entered regardless of the current state of the BSY bit or the DRQ bit in the shadow Status register. Devices shall not modify the behavior of this bit based on the state of the nIEN bit received in Register Host to Device FISes.

N – Notification Bit. This bit signals the host that the device needs attention. If the bit is set to one, the host should interrogate the device and determine what type of action is needed. If the bit is cleared to zero, the device is not requesting attention from the host. Refer to section 13.6.

Error – Contains the new value of the Error register of the Shadow Register Block.

PM Port – When an endpoint device is attached via a Port Multiplier, specifies the device port address that the FIS is received from. This field is set by the Port Multiplier. Endpoint devices shall set this field to 0h.

Status-Hi – Contains the new value of bits 6, 5, and 4 of the Status register of the Shadow Register Block.

Status-Lo– Contains the new value of bits 2,1, and 0 of the Status register of the Shadow Register Block.

R – Reserved – shall be cleared to zero.

10.3.6.1 Description

The Set Device Bits FIS is used by the device to load Shadow Register Block bits for which the device has exclusive write access. These bits are the eight bits of the Error register and six of the eight bits of the Status register. This FIS does not alter bit 7, BSY, or bit 3, DRQ, of the Status register.

The FIS includes a bit to signal the host adapter to generate an interrupt if the BSY bit and the DRQ bit in the shadow Status Register are both cleared to zero when this FIS is received.

Some Serial ATA to parallel ATA bridge solutions may elect to not support this FIS based on the requirements of their target markets.

10.3.6.2 Transmission

The device transmits a Set Device Bits FIS to alter one or more bits in the Error register or in the Status register in the Shadow Register Block. This FIS should be used by the device to set the

SERV bit in the Status register to request service for a bus released command. When used for this purpose the device shall set the Interrupt bit to one.

10.3.6.3 Reception

Upon receiving a Set Device Bits FIS, the host adapter shall load the data from the Error field into the shadow Error register, the data from the Status-Hi field into bits 6, 5, and 4, of the shadow Status register, and the data from the Status-Lo field into bits 2, 1, and 0 of the shadow Status register. Bit 7, BSY, and bit 3, DRQ, of the shadow Status register shall not be changed. If the I bit in the FIS is set to a one, and if both the BSY bit and the DRQ bit in the Shadow status register are cleared to zero when this FIS is received, then the host adapter shall enter an interrupt pending state.

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10.3.7 DMA Activate - Device to Host

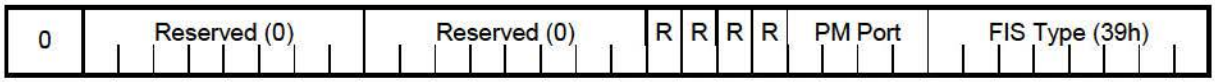


Figure 161 – DMA Activate - Device to Host FIS layout

Field Definitions

FIS Type - Set to a value of 39h. Defines the rest of the FIS fields. Defines the length of the FIS as one Dword.

PM Port – When an endpoint device is attached via a Port Multiplier, specifies the device port address that the FIS is received from. This field is set by the Port Multiplier. Endpoint devices shall set this field to 0h.

R - Reserved – shall be cleared to zero.

10.3.7.1 Description

The DMA Activate FIS is used by the device to signal the host to proceed with a DMA data transfer of data from the host to the device. This is the mechanism by which a legacy device signals its readiness to receive DMA data from the host.

A situation may arise where the host needs to send multiple Data FISes in order to complete the overall data transfer request. The host shall wait for a successful reception of a DMA Activate FIS before sending each of the Data FISes that are needed.

10.3.7.2 Transmission

The device transmits a DMA Activate to the host in order to initiate the flow of DMA data from the host to the device as part of the data transfer portion of a corresponding DMA write command. When transmitting this FIS, the device shall be prepared to subsequently receive a Data - Host to Device FIS from the host with the DMA data for the corresponding command.

10.3.7.3 Reception

Upon receiving a DMA Activate, if the host adapter's DMA controller has been programmed and armed, the host adapter shall initiate the transmission of a Data FIS and shall transmit in this FIS the data corresponding to the host memory regions indicated by the DMA controller's context. If the host adapter's DMA controller has not yet been programmed and armed, the host adapter shall set an internal state indicating that the DMA controller has been activated by the device, and as soon as the DMA controller has been programmed and armed, a Data FIS shall be transmitted to the device with the data corresponding to the host memory regions indicated by the DMA controller context.

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10.3.8 DMA Setup – Device to Host or Host to Device (Bidirectional)

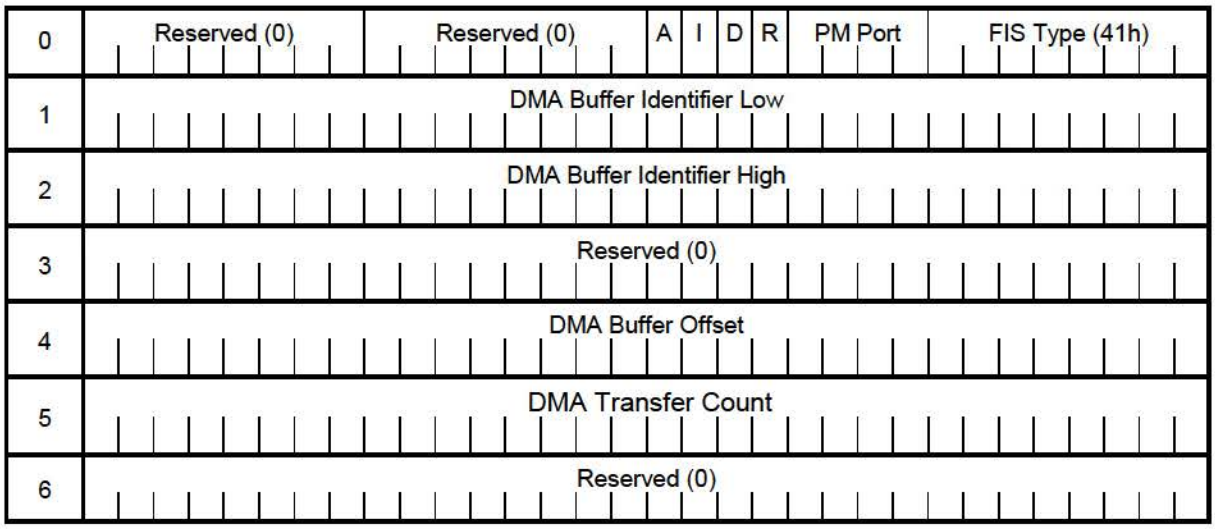


Figure 162 – DMA Setup – Device to Host or Host to Device FIS layout

Field Definitions

FIS Type - Set to a value of 41h. Defines the rest of the FIS fields. Defines the total length of the FIS as seven Dwords.

D Direction - Indicates whether subsequent data transferred after this FIS is from transmitter to receiver or from receiver to transmitter 1 = transmitter to receiver, 0 = receiver to transmitter.

A Auto-Activate - If set to one, in response to a DMA Setup FIS with data transfer direction of Host-to-Device, causes the host to initiate transfer of the first Data FIS to the device after the DMA context for the transfer has been established. The device shall not transmit a DMA Activate FIS to trigger the transmission of the first Data FIS from the host. If cleared to zero, a DMA Activate FIS is required to trigger the transmission of the first Data FIS from the host when the data transfer direction is Host-to-Device.

DMA Buffer Identifier Low/High - This field is used to identify a DMA buffer region in host memory. The contents are not described in this specification and are host dependent. The buffer identifier is supplied by the host to the device and the device echoes it back to the host. This allows the implementation to pass a physical address or or, in more complex implementations, the buffer identifier could be a scatter gather list or other information that can identify a DMA "channel".

DMA Buffer Offset - This is the byte offset into the buffer. Bits [1:0] shall be zero.

DMA Transfer Count - This is the number of bytes to be read or written. Bit zero shall be zero.

I Interrupt - If the Interrupt bit is set to one an interrupt pending shall be generated when the DMA transfer count is exhausted. Devices shall not modify the behavior of this bit based on the state of the nIEN bit received in Register Host to Device FISes.

PM Port – When an endpoint device is attached via a Port Multiplier, specifies the device port address that the FIS should be delivered to or is received from. This field is set by the host for Host to Device transmission and this field is set by the Port Multiplier for Device to Host transmission. Endpoint devices shall set this field to 0h for Device to Host transmissions.

R - Reserved – shall be cleared to zero.

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10.3.8.1 Description

The DMA Setup – Device to Host or Host to Device FIS is the mechanism by which first-party DMA access to host memory is initiated. This FIS is used to request the host or device to program its DMA controller before transferring data. The FIS allows the actual host memory regions to be abstracted (depending on implementation) by having memory regions referenced via a base memory descriptor representing a memory region that the host has granted the device access to. The specific implementation for the memory descriptor abstraction is not defined.

The device or host is informed of the 64-bit DMA buffer identifier/descriptor at some previous time by an implementation specific mechanism such as a command issued to or as defined in a specification. Random access within a buffer is accomplished by using the buffer offset.

First party DMA is a superset capability not necessarily supported by legacy devices or legacy device drivers but essential for accommodating future capabilities.

10.3.8.2 Transmission

A device or host transmits a DMA Setup – Device to Host or Host to Device FIS as the first step in performing a DMA access. The purpose of the DMA Setup – Device to Host or Host to Device is to establish DMA hardware context for one or more data transfers.

A DMA Setup – Device to Host or Host to Device is required only when the DMA context is to be changed. Multiple Data – Host to Device or Device to Host FISes can follow in either direction, for example, if the transfer count exceeds the maximum Data – Host to Device or Device to Host transfer length or when a data transfer is interrupted. When multiple Data – Host to Device or Device to Host FISes follow a DMA Setup – Device to Host or Host to Device FIS, the device or host shall place the data contained in the FIS in sequential addresses; that is, if the last Dword of a FIS is placed in (or obtained from) address N, the first Dword of a subsequent Data – Host to Device or Device to Host shall be placed in (or obtained from) address N+4 unless an intervening DMA Setup – Device to Host or Host to Device FIS is used to alter the DMA context. This mechanism allows for the efficient streaming of data into a buffer.

10.3.8.3 Reception

Upon receiving a DMA Setup – Device to Host or Host to Device FIS, the receiver of the FIS shall validate the received DMA Setup request, and provided that the buffer identifier and the specified offset/count are valid, program and arm the adapter's DMA controller using the information in the FIS. The specific implementation of the buffer identifier and buffer/address validation is not specified. After a valid DMA Setup – Device to Host or Host to Device FIS with the D bit cleared to zero, the receiver of the DMA Setup – Device to Host or Host to Device FIS responds with one or more Data – Host to Device or Device to Host FISes until the DMA count is exhausted. After a valid DMA Setup – Device to Host or Host to Device FIS with the D bit set to one, the receiver of the FIS shall be prepared to accept one or more Data – Host to Device or Device to Host FISes until the DMA count is exhausted.

An interrupt pending condition shall be generated upon the completion of the DMA transfer if the I bit is set to one. The definition DMA transfer completion is system dependent but typically includes the exhaustion of the transfer count or the detection of an error by the DMA controller.

NOTE – First-party DMA accesses are categorized in two groups: command/status transfers and user-data transfers. Interrupts would not typically be generated on user-data transfers. The optimal interrupt scheme for command/status transfers is not defined in this specification.

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10.3.8.3.1 Auto-Activate

First Party DMA transfers from the host to the device require transmission of both the DMA Setup FIS and a subsequent DMA Activate FIS in order to trigger the host transfer of data to the device. Because the device can elect to submit the DMA Setup FIS only when it is already prepared to receive the subsequent Data FIS from the host, the extra transaction for the DMA Activate FIS can be eliminated by merely having the DMA Setup FIS automatically activate the DMA controller by setting the Auto-Activate 'A' bit to one in the DMA Setup FIS.

Devices shall not attempt to utilize this capability prior to the optimization having been explicitly enabled by the host as defined in section 13.2.4.2. The host response to a DMA Setup FIS with the Auto-Activate bit set to one when the host has not enabled Auto-Activate is not defined.

10.3.8.4 HBA Enforcement of First-party DMA Data Phase Atomicity

The host bus adapter shall ensure the First-party DMA Data Phase is uninterrupted. Unless the ERR bit in the shadow Status register is set, the host shall ensure no FIS other than requested data payload or a FIS for a software reset is transmitted from the host to device between the reception of a DMA Setup FIS and the exhaustion of the associated transfer count.

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10.3.9 BIST Activate - Bidirectional

0	Reserved (0)								Pattern Definition								R	R	R	R	PM Port				FIS Type (58h)							
									T	A	S	L	F	P	R	V															
1	Data [31:24]								Data [23:16]								Data [15:8]								Data [7:0]							
2	Data [31:24]								Data [23:16]								Data [15:8]								Data [7:0]							

Figure 163 – BIST Activate - Bidirectional

Field Definitions

FIS Type - Set to a value of 58h. Defines the rest of the FIS fields.
F – Far End Analog (AFE) Loopback (Optional)
L - Far End Retimed Loopback* Transmitter shall insert additional $ALIGN_P$ primitives
R - Reserved – shall be cleared to zero.
T - Far end transmit only mode
A - $ALIGN_P$ Bypass (Do not Transmit $ALIGN_P$ primitives) (valid only in combination with T Bit) (optional behavior)
S - Bypass Scrambling (valid only in combination with T Bit) (optional behavior)
P - Primitive bit. (valid only in combination with the T Bit) (optional behavior)
PM Port – When an endpoint device is attached via a Port Multiplier, specifies the device port address that the FIS should be delivered to or is received from. This field is set by the host for Host to Device transmission and this field is set by the Port Multiplier for Device to Host transmission. Endpoint devices shall set this field to 0h for Device to Host transmissions.
V - Vendor Specific Test Mode. Causes all other bits to be ignored

10.3.9.1 Description

The BIST Activate FIS shall be used to place the receiver in one of several loopback modes.

The BIST Activate FIS is a bi-directional FISthat can be sent by either the host or the device. The sender and receiver have distinct responsibilities in order to insure proper cooperation between the two parties. The state machines for transmission and reception of the FIS are symmetrical. The method of causing a BIST Activate FIS transmission is not defined in this specification.

The state machines for the transmission of the FIS do not attempt to specify the actions the sender takes once successful transmission of the request has been performed. After the Application layer is notified of the successful transmission of the FIS the sender's Application layer prepares its own Application, Transport and Physical layers into the appropriate states that support the transmission of a stream of data. The FIS shall not be considered successfully transmitted until the receiver has acknowledged reception of the FIS as per normal FIS transfers documented in various sections of this specification. The transmitter of the BIST Activate FIS should transmit continuous $SYNC_P$ primitives after reception of the R_OK_P primitive until such a time that it is ready to interact with the receiver in the BIST exchange.

Similarly, the state machines for the reception of the FIS do not specify the actions of the receiver's Application layer. Once the FIS has been received, the receiver's Application layer places its own Application, Transport and Physical layers into states that perform the appropriate retransmission of the sender's data. The receiver shall not enter the BIST state until after it has properly received a good BIST Activate FIS (good CRC), indicated a successful transfer of the FIS to the transmitting side via the R_OK_P primitive and has received at least one good $SYNC_P$ primitive. Once in the self-test mode, a receiver shall continue to allow processing of the COMINIT or COMRESET signals in order to exit from the self-test mode.

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Note, that BIST mode is intended for Inspection/Observation Testing, as well as support for conventional laboratory equipment, rather than for in-system automated testing.

F: The Far End Analog (Analog Front End - AFE) Loopback, shall be defined as a vendor optional mode where the raw data is received, and retransmitted, without any retiming or re-synchronization, etc. The implementation of Far End AFE Loopback is optional due to the round-trip characteristics of the test as well as the lack of retiming. This mode is intended to give a quick indication of connectivity, and test failure is not an indication of system failure.

L: The Far End Retimed Loopback, shall be defined as a mode where the receiver retimes the data, and retransmits the retimed data. The initiator of the retimed loopback mode shall account for the loopback device consuming up to two $ALIGN_P$ primitives (one ALIGN sequence) every 256 Dwords transmitted and, if it requires any $ALIGN_P$ primitives to be present in the returned data stream, it should insert additional $ALIGN_P$ primitives in the transmitted stream. The initiator shall transmit additional ALIGN sequences in a single burst at the normal interval of every 256 Dwords transmitted (as opposed to inserting ALIGN sequences at half the interval).

The loopback device may remove zero, one, or two $ALIGN_P$ primitives from the received data. It may insert one or more $ALIGN_P$ primitives if they are directly preceded or followed by the initiator inserted $ALIGN_P$ primitives (resulting in ALIGN sequences consisting of at least two $ALIGN_P$ primitives) or it may insert two or more $ALIGN_P$ primitives if not preceded or followed by the initiator's $ALIGN_P$ primitives. One side effect of the loopback retiming is that the returned data stream may have instances of an odd number of $ALIGN_P$ primitives, however, returned $ALIGN_P$ primitives are always in bursts and if the initiator transmitted dual ALIGN sequences (four consecutive $ALIGN_P$ primitives), then the returned data stream shall include $ALIGN_P$ bursts that are no shorter than two $ALIGN_P$ primitives long (although the length of the $ALIGN_P$ burst may be odd). The initiator of the retimed loopback mode shall not assume any relationship between the relative position of the $ALIGN_P$ primitives returned by the loopback device and the relative position of the $ALIGN_P$ primitives sent by the initiator.

In retimed loopback mode, the initiator shall transmit only valid 8b/10b characters so the loopback device may 10b/8b decode it and re-encode it before retransmission. If the loopback device descrambles incoming data it is responsible for rescrambling it with the same sequence of scrambling syndromes in order to ensure the returned data is unchanged from the received data. The loopback device's running disparity for its transmitter and receiver are not guaranteed to be the same and thus the loopback initiator shall 10b/8b decode the returned data rather than use the raw 10b returned stream for the purpose of data comparison. The loopback device shall return all received data unaltered and shall disregard protocol processing of primitives. Only the OOB signals and $ALIGN_P$ processing is acted on by the loopback device, while all other data is retransmitted without interpretation.

T: The Far-End Transmit Mode shall be defined as a mode that can be used to invoke the Far-End Interface to send data patterns, upon receipt of the BIST Activate FIS, as defined by Pattern Dwords #1, and #2. Note that Pattern Dwords #1, and #2 shall be applicable only when the T bit is active, indicating "Far-End Transmit Mode".

This data is modified by the following bits.

P: The transmit primitives bit. When this bit is set in far end transmit mode, the lowest order byte of the two following Dwords are treated as K Characters. It is the responsibility of the sender of the BIST FIS to ensure that the data in byte 0 of the Dwords are valid D character versions of the K character (i.e. BCh for K28.5). Applicable only when the T bit is set.

A: The $ALIGN_P$ primitive sequence bypass mode. When set to one, no $ALIGN_P$ primitives are sent. When the A-bit is not asserted, $ALIGN_P$ primitives are sent normally as defined in this document. Applicable only when the T bit is set.

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S: The Bypass Scrambling shall be defined as a mode that can be used to send data or patterns, during BIST activation, that are not scrambled, however are encoded and decoded to normal and legal 8b/10b values. Applicable only when the T bit is set.

V: The vendor unique mode is implementation specific and shall be reserved for individual vendor use. All other bits are ignored in this mode.

10.3.9.2 Transmission

The initiator transmits a BIST Activate to the recipient in order to initiate the BIST mode of operation.

10.3.9.3 Reception

Upon receiving a BIST Activate, the recipient shall begin operations as per the BIST Activate FIS, described in this document above.

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10.3.10 PIO Setup – Device to Host

0	Error							Status				R	I	D	R	PM Port	FIS Type (5Fh)											
1	Device							LBA High				LBA Mid								LBA Low								
2	Reserved (0)							LBA High (exp)				LBA Mid (exp)								LBA Low (exp) (0)								
3	E_Status							Reserved (0)				Sector Count (exp)								Sector Count								
4	Reserved (0)																			Transfer Count								

Figure 164 – PIO Setup - Device to Host FIS layout

Field Definitions

FIS Type - Set to a value of 5Fh. Defines the rest of the FIS fields. Defines the length of the FIS as five Dwords.

LBA Mid - Holds the contents of the LBA Mid register of the Commanf Block.

LBA Mid (exp) – Contains the contents of the expanded address field of the Shadow Register Block

LBA High - Holds the contents of the LBA High register of the Command Block.

LBA High (exp) – Contains the contents of the expanded address field of the Shadow Register Block

D - Indicates the data transfer direction. When set to one the transfer is from device to host, when cleared to zero the transfer is from host to device.

Device - Holds the contents of the Device register of the Command Block.

Status - Contains the new value of the Status register of the Command Block for initiation of host data transfer.

Error - Contains the new value of the Error register of the Command Block at the conclusion of all subsequent Data to Device frames.

I - Interrupt bit. This bit reflects the interrupt bit line of the device. Devices shall not modify the behavior of this bit based on the state of the nIEN bit received in Register – Host to Device FISes.

PM Port – When an endpoint device is attached via a Port Multiplier, specifies the device port address that the FIS is received from. This field is set by the Port Multiplier. Endpoint devices shall set this field to 0h.

R – Reserved – shall be cleared to zero.

Sector Count - Holds the contents of the sector count register of the Command Block.

Sector Count (exp) – Contains the contents of the expanded address field of the Shadow Register Block

LBA Low - Holds the contents of the LBA Low register of the Command Block.

LBA Low (exp) – Contains the contents of the expanded address field of the Shadow Register Block

E_Status - Contains the new value of the Status register of the Command Block at the conclusion of the subsequent Data FIS.

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Transfer Count – Holds the number of bytes to be transferred in the subsequent Data FIS. The Transfer Count value shall be nonzero and the low order bit shall be zero (even number of bytes transferred).

10.3.10.1 Description

The PIO Setup – Device to Host FIS is used by the device to provide the host adapter with sufficient information regarding a PIO data phase to allow the host adapter to efficiently handle PIO data transfers. For PIO data transfers, the device shall send to the host a PIO Setup – Device to Host FIS just before each and every data transfer FIS that is required to complete the data transfer. Data transfers from Host to Device as well as data transfers from Device to Host shall follow this algorithm. Because of the stringent timing constraints in the ATA standard, the PIO Setup FIS includes both the starting and ending status values. These are used by the host adapter to first signal to host software readiness for PIO write data (BSY deasserted and DRQ asserted), and following the PIO write burst to properly signal host software by deasserting DRQ and possibly raising BSY.

10.3.10.2 Transmission of PIO Setup by Device Prior to a Data Transfer from Host to Device

The device transmits a PIO Setup – Device to Host FIS to the host in preparation for a PIO data payload transfer just before each and every PIO data payload transfer required to complete the total data transfer for a command. The device includes in the FIS the values to be placed in the Status shadow register at the beginning of the PIO data payload transfer and the value to be placed in the Status shadow register at the end of the data payload transfer. The device shall be prepared to receive a Data FIS in response to transmitting a PIO Setup FIS.

10.3.10.3 Reception of PIO Setup by Host Prior to a Data Transfer from Host to Device

Upon receiving a PIO Setup – Device to Host FIS, the host shall transfer the Status and Error values into the Status and Error Shadow registers and shall hold the E_Status value in a temporary register. The Transfer Length value shall be loaded into a countdown register. Upon detecting the change in the Status shadow register, host software proceeds to perform a series of write operations to the Data shadow register, which the host adapter shall collect to produce a Data FIS to the device. Each write of the Data shadow register results in another word of data being concatenated into the Data FIS, and the countdown register being decremented accordingly. The E_Status value shall be transferred to the Status shadow register within 400 ns of the countdown register reaching terminal count. In the case that the transfer length represents an odd number of words, the last word shall be placed in the low order (word 0) of the final Dword and the high order word (word 1) of the final Dword shall be padded with zeros before transmission. This process is repeated for each and every data FIS needed to complete the overall data transfer of a command.

10.3.10.4 Transmission of PIO Setup by Device Prior to a Data Transfer from Device to Host

The device transmits a PIO Setup – Device to Host FIS to the host in preparation for a PIO data payload transfer just before each and every PIO data payload transfer required to complete the total data transfer for a command. The device includes in the FIS the values to be placed in the Status shadow register at the beginning of the PIO data payload transfer and the value to be placed in the Status shadow register at the end of the data payload transfer. The device shall be prepared to transmit a Data FIS following the transmittal of a PIO Setup FIS.

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10.3.10.5 Reception of PIO Setup by Host Prior to a Data Transfer from Device to Host

Upon receiving a PIO Setup – Device to Host FIS for a device to host transfer, the host shall hold the Status, Error, and E_Status values in temporary registers. The Transfer Length value shall be loaded into a countdown register. Upon reception of a Data FIS from the device, the Status and Error values are loaded into the Status and Error Shadow registers and host software proceeds to perform a series of read operations from the Data shadow register. Each read of the Data shadow register results in a countdown register being decremented accordingly. The E_Status value shall be transferred to the Status shadow register within 400 ns of the countdown register reaching terminal count. This process is repeated for each and every data FIS needed to complete the overall data transfer of a command.

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10.3.11 Data - Host to Device or Device to Host (Bidirectional)

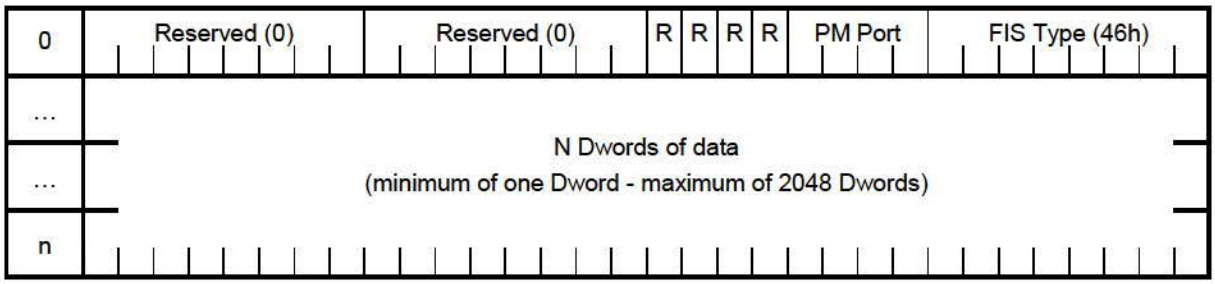


Figure 165 – Data – Host to Device or Device to Host FIS layout

Field Definitions

FIS Type - Set to a value of 46h. Defines the rest of the FIS fields. Defines the length of the FIS as n+1 Dwords.

Dwords of data - Contain the actual data to transfer. Only 32 bit fields are transferred. The last Dword is padded with zeros when only a partial Dword is to be transmitted.

NOTE –The maximum amount of user data that can be sent in a single Data – Host to Device or Data – Device to Host FIS is limited. See description.

PM Port – When an endpoint device is attached via a Port Multiplier, specifies the device port address that the FIS should be delivered to or is received from. This field is set by the host for Host to Device transmission and this field is set by the Port Multiplier for Device to Host transmission. Endpoint devices shall set this field to 0h for Device to Host transmissions.

R – Reserved – shall be cleared to zero.

10.3.11.1 Description

The Data – Host to Device and the Data – Device to Host FISes are used for transporting payload data, such as the data read from or written to a number of sectors on a hard drive. The FIS may either be generated by the device to transmit data to the host or may be generated by the host to transmit data to the device. This FIS is generally only one element of a sequence of transactions leading up to a data transmission and the transactions leading up to and following the Data FIS establish the proper context for both the host and device.

The byte count of the payload is not an explicit parameter, rather it is inferred by counting the number of Dwords between the SOF_P and EOF_P primitives, and discounting the FIS type and CRC Dwords. The payload size shall be no more than 2048 Dwords (8192 bytes). Non-packet devices, with or without bridges, should report a SET MULTIPLE limit of 16 sectors or less in word 47 of their IDENTIFY DEVICE information.

In the case that the transfer length represents an odd number of words, the last word shall be placed in the low order (word 0) of the final Dword and the high order word (word 1) of the final Dword shall be padded with zeros before transmission.

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10.3.11.2 Transmission

The device transmits a Data – Device to Host FIS to the host during the data transfer phase of legacy mode PIO reads, DMA reads, and First-party DMA writes to host memory. The device shall precede a Data FIS with any necessary context-setting transactions as appropriate for the particular command sequence. For example, a First-party DMA host memory write shall be preceded by a DMA Setup – Device to Host FIS to establish proper context for the Data FIS that follows.

The host transmits a Data – Host to Device FIS to the device during the data transfer phase of PIO writes, DMA writes, and First-party DMA reads of host memory. The FIS shall be preceded with any necessary context-setting transactions as appropriate for the particular command sequence. For example, a legacy mode DMA write to the device is preceded by a DMA Activate – Device to Host FIS with the DMA context having been pre-established by the host.

When used for transferring data for DMA operations multiple Data – Host to Device or Device to Host FISes can follow in either direction. Segmentation can occur when the transfer count exceeds the maximum Data – Host to Device or Device to Host transfer length or if a data transfer is interrupted.

When used for transferring data in response to a PIO Setup, the Data FIS shall contain the number of bytes indicated in the Transfer Count field of the preceding PIO Setup FIS.

In the event that a transfer is broken into multiple FISes, all intermediate FISes shall contain an integral number of full Dwords. If the total data transfer is for an odd number of words, then the high order word (word 1) of the last Dword of the last FIS shall be padded with zeros before transmission and discarded on reception.

The Serial ATA protocol does not permit for the transfer of an odd number of bytes.

10.3.11.3 Reception

Neither the host nor device is expected to buffer an entire Data FIS in order to check the CRC of the FIS before processing the data. Incorrect data reception for a Data FIS should be reflected in the overall command completion status.

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10.4 Host transport states

FIS reception is asynchronous in nature. In the case of a non-Data FIS transmission, the host may be pre-empted by a non-Data FIS reception from the device. The host shall hold off on the pending transmission and process the incoming FIS from the device before attempting to retransmit the pending FIS.

10.4.1 Host transport idle state diagram

HTI1: HT_HostIdle	Host adapter waits for frame or frame request.	
1. Command Register FIS transmission pending	→	HT_CmdFIS
2. Control Register FIS transmission pending	→	HT_CntrlFIS [1]
3. Frame receipt indicated by Link layer	→	HT_ChkTyp [3]
4. DMA Setup FIS transmission pending	→	HT_DMASTUPFIS
5. BIST Activate FIS transmission pending	→	HT_XmitBIST
6. Previous FIS was PIO Setup and Application layer indicates data direction is host to device	→	HT_PIOOTrans2 [2]

NOTE:
1. Transmission of a Control Register FIS is mandatory if the state of the SRST bit in the Device Control Shadow Register is changed, and is optional if the state of the SRST bit is not changed. If a Control Register FIS transmission with a modified value for the SRST bit is triggered while another non-Control Register FIS transmission is already pending, all pending non-Control Register FIS transmissions shall be aborted. If the state of the SRST bit is not modified from its previous value in a Control Register FIS transmission, then pending non-Control Register FIS transmissions shall not be aborted.
2. The PIO Setup FIS shall set an indication that PIO Setup was the last FIS received. Indication from the Application layer that it is transmitting data to the device can be determined from the Application layer performing write operations to the Data register in the Shadow Register Block.
3. FIS reception shall have priority over all other transitions in this state.

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HTI2: HT_ChkTyp	Received FIS type checked.	
1. Register FIS type detected	→	HT_RegFIS
2. Set Device Bits FIS type detected	→	HT_DB_FIS
3. DMA Activate FIS type detected	→	HT_DMA_FIS
4. PIO Setup FIS type detected	→	HT_PS_FIS
5. DMA Setup FIS type detected	→	HT_DS_FIS
6. BIST FIS type detected	→	HT RcvBIST
7. Data FIS type detected and previous FIS was not PIO Setup	→	HT_DMAITrans [1]
8. Data FIS type detected and previous FIS was PIO Setup	→	HT_PIOITrans1 [1]
9. Unrecognized FIS received	→	HT_HostIdle
10. Notification of illegal transition error received from Link layer	→	HT_HostIdle
NOTE: 1. The PIO Setup FIS shall set an indication that PIO Setup was the last FIS sent, so that this state can determine whether to transition to DMA data transfer, or PIO data transfer.		

HTI1: HT_HostIdle state: This state is entered when a Frame Information Structure (FIS) transaction has been completed by the Transport layer.

When in this state, the Transport layer waits for the shadow Command register to be written, the shadow Device Control register to be written, or the Link layer to indicate that a FIS is being received.

TransitionHTI1:1: When a Command Register FIS transmission is pending, the Transport layer shall make a transition to the HTCM1: HT_CmdFIS state. A Command Register FIS becomes pending upon a write operation to the Command shadow register, and ceases pending at successful transmission of the FIS as indicated by the link layer.

Transition HTI1:2: When a Control Register FIS transmission is pending, the Transport layer shall make a transition to the HTCR1: HT_CntrlFIS state. A Control Register FIS becomes pending upon a write operation to the Device Control shadow register that changes the state of the SRST bit from the previous value, or optionally upon a write operation to the Device Control shadow register that does not change the state of the SRST bit. A Control Register FIS ceases pending at successful transmission of the FIS as indicated by the link layer.

Transition HTI1:3: When the Link layer indicates that a FIS is being received, the Transport layer shall make a transition to the HTI2: HT_ChkTyp state.

Transition HTI1:4: When the Application layer indicates that a DMA Setup FIS is to be sent, the Transport layer shall make a transition to the HT_DMASTUP0:HT_DMASTUPFIS state.

Transition HTI1:5: When the Application layer requests the transmission of a BIST request to the device the Transport layer shall make a transition to the HTXBIST1:HT state.

Transition HTI1:6: When the Application layer requests the transmission of data to the device and the previous FIS was a PIOSetup type, the Transport layer shall make a transition to the HTPS3:HT_PIOOTrans2 state. The Application layer signals transmission of PIO data to the device by performing writes to the Data register in the Shadow Register Block.

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HTI2: HT_ChkTyp state: This state is entered when the Link layer indicates that a FIS is being received.

When in this state, the Transport layer checks the FIS type of the incoming FIS.

Transition HTI2:1: When the incoming FIS is a register type, the Transport layer shall notify the Link Layer that it has received a valid FIS, and make a transition to the HTR1: HT_RegFIS state.

Transition HTI2:2: When the incoming FIS is a Set Device Bits type, the transport layer shall notify the Link Layer that it has received a valid FIS and make a transition to the HTDB0:HT_DB_FIS state.

Transition HTI2:3: When the incoming FIS is a DMA Activate type, the Transport layer shall notify the Link Layer that it has received a valid FIS, and make a transition to the HTDA1: HT_DMA_FIS state.

Transition HTI2:4: When the incoming FIS is a PIO Setup type, the Transport layer shall notify the Link Layer that it has received a valid FIS, and make a transition to the HTPS1: HT_PS_FIS state.

Transition HTI2:5: When the incoming FIS is a DMA Setup type, the Transport layer shall notify the Link Layer that it has received a valid FIS, and make a transition to the HTDS1: HT_DS_FIS state.

Transition HTI2:6: When the incoming FIS is a BIST Activate type, the Transport layer shall notify the Link Layer that it has received a valid FIS, and make a transition to the HTRBIST1:HT_RcvBIST state.

Transition HTI2:7: When the incoming FIS is a Data type, and the previous FIS was not a PIO Setup type, the Transport layer shall notify the Link Layer that it has received a valid FIS, and make a transition to the HTDA6:HT_DMAITrans state.

Transition HTI2:8: When the incoming FIS is a Data type, and the previous FIS was a PIO Setup type, the Transport layer shall notify the Link Layer that it has received a valid FIS, and make a transition to the HTPS6:HT_PIOITrans state.

Transition HTI2:9: When the received FIS is of an unrecognized, or unsupported type, the Transport layer shall notify the Link Layer that it has received an unrecognized FIS, and make a transition to the HTI1: HT_HostIdle state.

Transition HTI2:10: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1: HT_HostIdle state.

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10.4.2 Host Transport transmit command FIS diagram

This protocol builds a FIS that contains the host adapter shadow register content and sends it to the device when the software driver or BIOS writes the host adapter shadow Command register.

HTCM1: HT_CmdFIS	Construct Register – Host to Device FIS with C=1 from the content of the shadow registers and notify Link to transfer.		
	1. FIS transfer complete	→	HT_CmdTransStatus
	2. Notification of illegal transition error received from Link layer	→	HT_HostIdle
	3. Frame receipt indicated by Link layer	→	HT_HostIdle

HTCM2: HT_CmdTransStatus	Check Link and Phy transmission results and if an error occurred take appropriate action.		
	1. Status checked and no error detected	→	HT_HostIdle
	2. Status checked and error detected[1]	→	HT_HostIdle
	NOTE: 1. Upon return to the HT_HostIdle state in response to a detected error, the associated FIS remains pending for transmission		

HTCM1: HT_CmdFIS state: This state is entered when the shadow Command register is written.

When in this state, the Transport layer shall construct a Register – Host to Device FIS with C=1, notify the Link layer that the FIS is to be transmitted, and pass the FIS to the Link layer.

Transition HTCM1:1: When the entire FIS has been passed to the Link layer, the Transport layer shall indicate to the Link layer that the FIS transmit is complete and make a transition to the HTCM2: HT_CmdTransStatus state.

Transition HTCM1:2: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1: HT_HostIdle state.

Transition HTCM1:3: When the Link layer indicates that a FIS is being received, the Transport Layer shall make a transition to the HTI1:HT_HostIdle state.

HTCM2: HT_CmdTransStatus state: This state is when the entire FIS has been passed to the Link layer.

When in this state, the Transport layer shall wait for the Link and Phy ending status for the FIS and take appropriate error handling action if required.

Transition HTCM2:1: When the FIS status has been handled and no errors detected, the Transport layer shall transition to the HTI1: HT_HostIdle state.

Transition HTCM2:2: When the FIS status has been handled and an error has been detected, the Transport layer shall transition to the HTI1: HT_HostIdle state. The associated FIS remains pending for transmission.

10.4.3 Host Transport transmit control FIS diagram

This protocol builds a FIS that contains the host adapter shadow register content and sends it to the device when the software driver or BIOS writes the host adapter shadow Device Control register.

HTCR1: HT_CntrlFIS	Construct Register – Host to Device FIS with C=0 from the content of the shadow registers and notify Link to transfer.	
1. FIS transfer complete	→	HT_CtrlTransStatus
2. Notification of illegal transition error received from Link layer	→	HT_HostIdle
3. Frame receipt indicated by Link layer	→	HT_HostIdle

HTCR2: HT_CtrlTransStatus	Check Link and Phy transmission results and if an error occurred take appropriate action.	
1. Status checked and no errors detected	→	HT_HostIdle
2. Status checked and error detected[1]	→	HT_HostIdle
NOTE: 1. Upon return to the HT_HostIdle state in response to a detected error, the associated FIS remains pending for transmission		

HTCR1: HT_Cntrl_FIS state: This state is entered when the shadow Device Control register is written.

When in this state, the Transport layer shall construct a Register – Host to Device FIS with C=0, notify the Link layer that the FIS is to be transmitted, and pass the FIS to the Link layer.

Transition HTCR1:1: When the entire FIS has been passed to the Link layer, the Transport layer shall indicate to the Link layer that the FIS transmit is complete and make a transition to the HTCR2: HT_CtrlTransStatus state.

Transition HTCR1:2: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1: HT_HostIdle state.

Transition HTCR1:3: When the Link layer indicates that a FIS is being received, the Transport Layer shall make a transition to the HTI1:HT_HostIdle state.

HTCR2: HT_CtrlTransStatus state: This state is when the entire FIS has been passed to the Link layer.

When in this state, the Transport layer shall wait for the Link and Phy ending status for the FIS and take appropriate error handling action if required.

Transition HTCR2:1: When the FIS status has been handled and no errors have been detected, the Transport layer shall transition to the HTI1: HT_HostIdle state.

Transition HTCR2:2: When the FIS status has been handled and an error has been detected, the Transport layer shall transition to the HTI1: HT_HostIdle state. The associated FIS remains pending for transmission.

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10.4.4 Host Transport transmit DMA Setup – Device to Host or Host to Device FIS state diagram

This protocol transmits a DMA Setup – Device to Host or Host to Device FIS to a receiver. This FIS is a request by a transmitter for the receiver to program its DMA controller for a First-party DMA transfer and is followed by one or more Data FISes that transfer data. The DMA Setup – Device to Host or Host to Device FIS request includes the transfer direction indicator, the host buffer identifier, the host buffer offset, the byte count, and the interrupt flag.

HTDMASTUP0: HT_DMASTUPFIS	Construct the DMA Setup – Host to Device or Device to Host FIS from the content provided by the Application layer and notifies Link to transfer.	
1. FIS transfer complete	→	HT_DMASTUPTransStatus
2. Notification of illegal transition error received from Link layer	→	HT_HostIdle
3. Frame receipt indicated by Link layer	→	HT_HostIdle

HTPDMASTUP1: HT_DMASTUPTransStatus	Check Link and Phy transmission results and if an error occurred take appropriate action.	
1. Status checked and no error detected	→	HT_HostIdle
2. Status checked and error detected[1]	→	HT_HostIdle
NOTE: 1. Upon return to the HT_HostIdle state in response to a detected error, the associated FIS remains pending for transmission		

HTDMASTUP0: HT_DMASTUPFIS state: This state is entered when the Application requests the transmission of a DMA Setup – Host to Device or Device to Host FIS.

When in this state, the Transport layer shall construct a DMA Setup – Host to Device or Device to Host FIS, notify the Link layer that the FIS is to be transmitted, and pass the FIS to the Link layer.

Transition HTDMASTUP0:1: When the entire FIS has been passed to the Link layer, the Transport layer shall indicate to the Link layer that the FIS transmission is complete and make a transition to the HTDMASTUP1: HT_DMASTUPTransStatus state.

Transition HTDMASTUP0:2: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1: HT_HostIdle state.

Transition HTDMASTUP0:3: When the Link layer indicates that a FIS is being received, the Transport Layer shall make a transition to the HTI1:HT_HostIdle state.

HTPDMASTUP1: HT_DMASTUPTransStatus state: This state is entered when the entire FIS has been passed to the Link layer.

When in this state, the Transport layer shall wait for the Link and Phy ending status for the FIS and take appropriate error handling action if required.

Transition HTDMASTUP1:1: When the FIS status has been handled, and no error detected, the Transport layer shall transition to the HTI1: HT_HostIdle state.

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Transition HTDMASTUP1:2: When the FIS status has been handled, and an error detected, the Transport layer shall transition to the HTI1: HT_HostIdle state. The associated FIS remains pending for transmission.

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10.4.5 Host Transport transmit BIST Activate FIS

This protocol builds a BIST Activate FIS that tells the device to prepare to enter the appropriate Built-in Self-test mode. After successful transmission, the host Transport layer enters the idle state. The Application layer, upon detecting successful transmission to the device shall then cause the host's Transport layer, Link layer and Physical layer to enter the appropriate mode for the transmission of the Built-in Test data defined by the FIS. The means by which the Transport, Link and Physical layers are placed into self-test mode are not defined by this specification.

HTXBIST1: HT_XmitBIST	Construct the BIST Activate FIS from the content provided by the Application layer and notify Link to transfer.	
1. FIS transfer complete	→	HT_TransBISTStatus
2. Notification of illegal transition error received from Link layer	→	HT_HostIdle
3. Frame receipt indicated by Link layer	→	HT_HostIdle

HTXBIST2: HT_TransBISTStatus	Check Link and Phy transmission results and if an error occurred take appropriate action.	
1. Status check completed	→	HT_HostIdle
2. Status check and at least one error detected	→	HT_HostIdle[1]
NOTE: 1. Re-transmission of the BIST Activate FIS due to errors is not required but allowed.		

HTXBIST1: HT_XmitBIST state: This state is entered to send a BIST FIS to the device.

Transition HTXBIST1:1: When the entire FIS has been passed to the Link layer, the Transport layer shall indicate to the Link layer that the FIS transmission is complete and make a transition to the HTXBIST2:HT_TransBISTStatus state.

Transition HTXBIST1:2: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1: HT_HostIdle state.

Transition HTXBIST1:3: When the Link layer indicates that a FIS is being received, the Transport Layer shall make a transition to the HTI1:HT_HostIdle state.

HTXBIST2: HT_TransBISTStatus state: This state is entered when the entire FIS has been passed to the Link layer.

Transition HTXBIST2:1: When the FIS transmission is completed the Transport layer shall transition to the HTI1:HT_HostIdle state.

Transition HTXBIST2:2: When the FIS transmission is completed and at least one error is detected the Transport layer shall transition to the HTI1:HT_HostIdle state. The associated FIS may remain pending for transmission.

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10.4.6 Host Transport decompose Register FIS diagram

This protocol receives a Register – Device to Host FIS from the device containing new shadow register content and places that content into the shadow registers.

HTR1: HT_RegFIS	Place FIS contents from device into appropriate holding registers.		
	1. FIS transfer complete	→	HT_RegTransStatus
	2. Notification of illegal transition error received from Link layer	→	HT_HostIdle

HTR2: HT_RegTransStatus	Check Link and Phy transmission results and if an error occurred take appropriate action.		
	1. Status checked	→	HT_HostIdle

HTR1: HT_RegFIS state: This state is entered the Link layer has indicated that a FIS is being received and that the FIS is of the register type.

When in this state, the Transport layer shall decompose the Register FIS and place the contents into the appropriate holding registers.

Transition HTR1:1: When the entire Register – Device to Host FIS has been placed into the holding registers, the Transport layer shall make a transition to the HTR2: HT_RegTransStatus state.

Transition HTR1:2: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1: HT_HostIdle state.

HTR2: HT_RegTransStatus state: This state is when the entire FIS has been placed into the holding registers.

When in this state, the Transport layer shall wait for the Link and Phy ending status for the FIS and take appropriate error handling action if required.

Transition HTR2:1: When the FIS status has been handled and no errors detected, the contents of the holding registers shall be placed in the shadow registers and if the interrupt bit is set, the Transport layer shall set the interrupt pending flag. The Transport layer shall transition to the HTI1: HT_HostIdle state. When the FIS status has been handled and at least one error detected, the contents of the holding registers shall not be transferred to the shadow registers, error status shall be returned to the device, and the Transport layer shall transition to the HTI1: HT_HostIdle state.

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10.4.7 Host Transport decompose a Set Device Bits FIS state diagram

This protocol receives a Set Device Bits FIS from the device containing new Error and Status shadow register content and places that content into the Error and Status Shadow registers. The Set Device Bits FIS may also contain SActive register content and asynchronous notification content.

HTDB0:HT_DB_FIS	Receive Set Device Bits FIS	
1. FIS status checked and no error detected	→	HT_Dev_Bits
2. FIS status checked and error detected.	→	HT_HostIdle

HTDB1:HT_Dev_Bits	Load Error register and bits of the Status register	
1. Register bits loaded	→	HT_HostIdle

HTDB0:HT_DB_FIS state: This state is entered when the Link layer has indicated that a FIS being received and that the FIS is a Set Device Bits type.

When in this state, the Transport layer shall wait for the FIS reception to complete and for Link and Phy ending status to be posted.

Transition HTDB0:1: When the FIS reception is complete with no errors detected, the Transport layer shall transition to the HTDB1:HT_Dev_Bits state.

Transition HTDB0:2: When the FIS reception is complete with errors detected, the Transport layer shall return error status to the device and transition to the HTI1:HT_HostIdle state.

HTDB1:HT_Dev_Bits state: This state is entered when a Set Device Bits FIS has been received with no errors.

When in this state, the data in the Error field of the received FIS shall be loaded into the host adapter's shadow Error register. The data in the Status-Hi field of the received FIS shall be loaded into bits 6, 5, and 4 of the shadow Status register. The data in the Status-Lo field of the received FIS shall be loaded into bits 2, 1, and 0 of the shadow Status register. Bit 7, BSY, and bit 3, DRQ, in the shadow Status register shall not be changed. If the I bit in the FIS is set to one and if both the BSY bit and the DRQ bit in the shadow Status register are cleared to zero, then the host adapter shall enter an interrupt pending state.

Transition HTDB1:1: The Transport layer shall transition to the HTI1:HT_HostIdle state.

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10.4.8 Host Transport decompose a DMA Activate FIS diagram

This protocol receives a DMA Activate FIS that requests a DMA data out transfer. The data transfer is from the host to the device and the DMA Activate FIS causes the host adapter to transmit the data in a subsequent Data FIS.

HTDA1: HT_DMA_FIS		
1. Status checked and no error detected.	→	HT_DMAOTrans1
2. Status checked and error detected	→	HT_HostIdle
3. Notification of illegal transition error received from Link layer	→	HT_HostIdle

HTDA2: HT_DMAOTrans1	DMA controller initialized?	
1. DMA controller not initialized.	→	HT_DMAOTrans1
2. DMA controller initialized.	→	HT_DMAOTrans2
3. Notification of software reset or device reset command from the host application	→	HT_HostIdle

HTDA3: HT_DMAOTrans2	Activate DMA controller	
1. Transfer not complete and < 2048 Dwords transmitted	→	HT_DMAOTrans2
2. Transfer not complete and 2048 Dwords transmitted	→	HT_DMAEnd
3. Abort notification from Link layer	→	HT_DMAEnd
4. Transfer complete	→	HT_DMAEnd
5. Notification of illegal transition error received from Link layer	→	HT_HostIdle
6. Notification of software reset or device reset command from the host application	→	HT_HostIdle

HTDA4: HT_DMAEnd	Check DMA Controller completion	
1. DMA controller actions completed, no error detected	→	HT_HostIdle
2. DMA controller actions completed, and error detected.	→	HT_HostIdle
3. Abort notification from Link layer, no error detected	→	HT_HostIdle
4. Abort notification from Link layer, error detected.	→	HT_HostIdle

HTDA5: HT_DMAITrans	Activate DMA controller if initialized, receive Data FIS.	
1. Transfer not complete	→	HT_DMAITrans
2. SRST asserted, or device reset command issued	→	HT_HostIdle
3. Transfer complete	→	HT_DMAEnd
4. Notification of illegal transition error received from Link layer	→	HT_HostIdle

HTDA1: HT_DMA_FIS state: This state is entered when the Link layer has indicated that a FIS is being received and the Transport layer has determined that a DMA Activate FIS is being received.

When in this state, the Transport layer shall determine the direction of the DMA transfer being activated.

Transition HTDA1:1: The Transport layer shall make a transition to the HTDA2: HT_DMAOTrans1 state. This transition occurs if no error is detected.

Transition HTDA1:2: When an error is detected, status is conveyed to the Link layer and to the Application layer. The Transport layer shall make a transition to the HTI1:HT_HostIdle state.

Transition HTDA1:3: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1: HT_HostIdle state.

HTDA2: HT_DMAOTrans1 state: This state is entered when it is determined that the DMA transfer that is being activated is a transfer from host to device..

When in this state, the Transport layer shall determine if the DMA controller has been initialized.

Transition HTDA2:1: When the DMA controller has not yet been initialized, the Transport layer shall transition to the HTDA2: HT_DMAOTrans1 state.

Transition HTDA2:2: When the DMA controller has been initialized, the Transport layer shall transition to the HTDA3: HT_DMAOTrans2 state.

Transition HTDA2:3: When the host has asserted the SRST bit by writing to the Device Control register, or the ATAPI Device Reset command is written to the Command register, the Transport layer shall inform the Link layer to send a SYNC Escape, and the Transport layer shall transition to the HTI1:HT_HostIdle state.

HTDA3: HT_DMAOTrans2 state: This state is entered when the DMA controller has been initialized.

When in this state, the Transport layer shall activate the DMA controller and pass data to the Link layer.

Transition HTDA3:1: When the transfer is not complete and less than 2048 Dwords of payload data has been transmitted, the Transport layer shall transition to the HTDA3: HT_DMAOTrans2 state.

Transition HTDA3:2: When the transfer is not complete but 2048 Dwords of payload data has been transmitted, the Link layer shall be notified to close the current frame and the Transport layer shall deactivate the DMA engine and transition to the HTDA4: HT_DMAEnd state.

Transition HTDA3:3: When notified by the Link layer that the DMA Abort primitive was received, the Transport layer shall transition to the HTDA4: HT_DMAEnd state.

Transition HTDA3:4: When the requested DMA transfer is complete, the Transport layer shall transition to the HTDA4: HT_DMAEnd state.

Transition HTDA3:5: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1: HT_HostIdle state.

Transition HTDA3:6: When the host has asserted the SRST bit by writing to the Device Control register, or the ATAPI Device Reset command is written to the Command register, the Transport layer shall inform the Link layer to send a SYNC Escape, and the Transport layer shall transition to the HTI1:HT_HostIdle state.

HTDA4: HT_DMAEnd state: This state is entered when the DMA data transfer is complete.

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When in this state, the Transport layer shall ensure that the activities of the DMA controller have completed.

Transition HTDA4:1: When the DMA controller has completed its activities, whether it has exhausted its transfer count or has been deactivated as a result of reaching the 2048 Dword data payload limit, the Transport layer shall transition to the HTI1: HT_HostIdle state. This transition occurs if no error is detected.

Transition HTDA4:2: When an error is detected, status shall be reported to the Link and Application layers. The Transport layer shall transition to the HTI1:HT_HostIdle state.

Transition HTDA4:3: When notified by the Link layer that a DMA Abort primitive was received, the transfer shall be truncated, and the Link layer notified to append CRC and end the frame. When it is determined that the transfer is completed with no error, the Transport layer shall make a transition to the HTI1:HT_HostIdle state.

Transition HTDA4:4: When notified by the Link layer that a DMA Abort primitive was received, the transfer shall be truncated, and the Link layer notified to append CRC and end the frame. When it is determined that the transfer is completed with an error, the Transport layer shall report status to the host and make a transition to the HTI1:HT_HostIdle state.

HTDA5: HT_DMAITrans state: This state is entered when the Transport layer has determined that the DMA transfer being activated is from device to host.

When in this state, the Transport layer shall activate the DMA controller if the DMA controller is initialized. A data frame is received from the device and a received data Dword shall be placed in the data FIFO.

When in this state, the Transport layer shall wait until the Link layer has begun to receive the DMA data frame and data is available to be read by the host.

Transition HTDA5:1: When the transfer is not complete, the Transport layer shall transition to the HTDA5: HT_DMAITrans state. This includes the condition where the host DMA engine has not yet been programmed and the transfer is therefore held up until the DMA engine is prepared to transfer the received data to the destination memory locations.

Transition HTDA5:2: When the SRST bit is asserted by the host writing the Device Control register, or a device reset command has been written to an ATAPI device, the Link layer shall be informed to send a $SYNC_P$ primitive, and the Transport layer shall transition to the HTI1:HT_Idle state.

Transition HTDA5:3: When the requested DMA transfer is complete, the Transport layer shall transition to the HTDA4: HT_DMAEnd state.

Transition HTDA5:4: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1: HT_HostIdle state.

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10.4.9 Host Transport decompose a PIO Setup FIS state diagram

This protocol receives a PIO Setup FIS that requests a PIO data transfer. If the direction is from host to device, the Transport layer transmits a Data FIS to the device containing the PIO data. If the direction of transfer is from device to host, the Transport layer receives a Data FIS from the device. The PIO data shall be sent in a single Data FIS.

HTPS1: HT_PS_FIS	Determine the direction of the requested PIO transfer.		
	1. Transfer host to device, no error detected. D bit = 0.	→	HT_PIOOTrans1
	2. Transfer device to host, no error detected. D bit = 1.	→	HT_HostIdle
	3. Error detected.	→	HT_HostIdle
	4. Notification of illegal transition error received from Link layer	→	HT_HostIdle

HTPS2: HT_PIOOTrans1	Place initial register content received from FIS into shadow registers.		
	1. Unconditional	→	HT_ HostIdle

HTPS3: HT_PIOOTrans2	Wait for Link layer to indicate data transfer complete		
	1. Transfer not complete	→	HT_PIOOTrans2
	2. Transfer complete	→	HT_PIOEnd
	3. Abort notification from Link layer	→	HT_PIOEnd
	4. Notification of illegal transition error received from Link layer	→	HT_HostIdle
	5. Notification of software reset or device reset command from the host application	→	HT_HostIdle

HTPS4: HT_PIOEnd	Place ending register content from PIO REQ FIS into shadow registers.		
	1. No error detected.	→	HT_HostIdle
	2. Error detected	→	HT_HostIdle

HTPS5: HT_PIOITrans1	Wait until initial PIO data received in data frame.		
	1. Received PIO data available.	→	HT_PIOITrans2[1]
	2. SRST asserted, or device reset command issued	→	HT_HostIdle
	3. Notification of illegal transition error received from Link layer	→	HT_HostIdle
	NOTE: 1. When transitioning to the HT_PIOITrans2 state, the starting status and I bit value from the PIO Setup FIS shall be transferred to the status shadow register and interrupt signal shall then reflect the value of the I bit.		

HTPS6: HT_PIOITrans2	Wait for Link layer to indicate data transfer complete.		
	1. Transfer not complete	→	HT_PIOITrans2
	2. Transfer complete	→	HT_PIOEnd
	3. Abort notification from Link layer	→	HT_PIOEnd
	4. Notification of illegal transition error received from Link layer	→	HT_HostIdle

HTPS1: HT_PS_FIS state: This state is entered when the Link layer has indicated that a FIS is being received and that the Transport layer has determined a PIO Setup FIS is being received.

When in this state, the Transport layer shall determine the direction of the requested PIO transfer and indicate that the last FIS sent was a PIO Setup.

Transition HTPS1:1: When the direction of transfer requested is from host to device (D=0), the Transport layer shall make a transition to the HTPS2: HT_PIOOTrans1 state. This transition occurs if no error is detected.

Transition HTPS1:2: When the direction of transfer requested is from device to host (D=1), the Transport layer shall make a transition to the HTI1:HT_HostIdle state. This transition occurs if no error is detected.

Transition HTPS1:3: When an error is detected, status shall be reported to the Link layer. The Transport layer shall make a transition to the HTI1:HT_HostIdle state.

Transition HTPS1:4: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1:HT_HostIdle state.

HTPS2: HT_PIOOTrans1 state: This state is entered when the direction of the requested PIO data transfer is from host to device.

When in this state, the Transport layer shall place the FIS initial register content into the shadow registers, the FIS byte count, and set the interrupt pending flag if the FIS indicates to do so.

Transition HTPS2:1: When the FIS initial register content has been placed into the shadow registers, interrupt pending set if requested, and the Transport layer is ready to begin transmitting the requested PIO data FIS, the Transport layer shall make a transition to the HTI1:HT_HostIdle state.

HTPS3: HT_PIOOTrans2 state: This state is entered when PIO data is available in the PIO FIFO to be passed the Link layer.

When in this state, the Transport layer shall wait for the Link layer to indicate that all data has been transferred.

> NOTE – Since the software driver or BIOS sees DRQ set and BSY cleared, it continues writing the Data register filling the PIO FIFO.

Transition HTPS3:1: When the transfer is not complete, the Transport layer shall transition to the HTPS3: HT_PIOOTrans2 state.

Transition HTPS3:2: When the byte count for this DRQ data block is reached, the Transport layer shall transition to the HTPS4: HT_PIOEnd state.

Transition HTPS3:3: When notified by the Link layer that the DMA Abort primitive was received, the Transport layer shall transition to the HTPS4: HT_PIOEnd state.

Transition HTPS3:4: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1:HT_HostIdle state.

Transition HTPS3:5: When the host has asserted the SRST bit by writing to the Device Control register, or the ATAPI Device Reset command is written to the Command register, the Transport

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layer shall inform the Link layer to send a SYNC Escape, and the Transport layer shall transition to the HTI1:HT_HostIdle state.

HTPS4: HT_PIOEnd state: This state is entered when the PIO data transfer is complete.

When in this state, the Transport layer shall place the ending register content from the received PIO request FIS into the shadow registers.

Transition HTPS4:1: When the ending register content for the PIO request FIS has been placed into the shadow registers and there were no errors detected with the transfer, the Transport layer shall transition to the HTI1: HT_HostIdle state.

Transition HTPS4:2: When the ending register content from the previous PIO Setup FIS has been placed into the shadow registers, the Transport layer shall transition to the HTI1:HT_HostIdle state. For data in transfers, the Transport layer shall notify the Link layer of any error encountered during the transfer, and the error shall be reflected in the end of frame handshake. If the transfer was not the final transfer for the PIO data in command, the device shall reflect the error status by transmitting an appropriate Register FIS to the host. If the transfer was the final transfer for the associated PIO data in command, the error condition is not detectable. For data out transfers, errors detected by the device shall be reflected in the end of frame handshake. The device shall reflect the error status by transmitting an appropriate Register FIS to the host.

HTPS5: HT_PIOITrans1 state: This state is entered when the direction of the PIO data transfer is device to host.

When in this state, the Transport layer shall wait until the Link layer has begun to receive the PIO data frame and data is available to be read by the host.

Transition HTPS5:1: When data is available for the host to read in the shadow Data register, the Transport layer shall place the initial register content received in the PIO Setup frame into the shadow registers and transition to the HTPS6: HT_PIOITrans2 state.

Transition HTPS5:2: When the host has asserted the SRST bit by writing to the Device Control register, or the ATAPI Device Reset command is issued, the Transport layer shall inform the Link layer to send a SYNC Escape, and the Transport layer shall transition to the HTI1: HT_HostIdle state.

Transition HTPS5:3: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1:HT_HostIdle state.

HTPS6: HT_PIOITrans2 state: This state is entered when PIO data is available in the PIO FIFO to be read by the host and the initial shadow register content has been set.

When in this state, the Transport layer shall wait for the Link layer to indicate that the data transfer is complete

Transition HTPS6:1: When the transfer is not complete, the Transport layer shall transition to the HTPS6: HT_PIOITrans2 state.

Transition HTPS6:2: When the byte count for this DRQ data block is reached, the Transport layer shall transition to the HTPS5: HT_PIOEnd state.

Transition HTPS6:3: When notified by the Link layer that the DMA Abort primitive was received, the Transport layer shall transition to the HTPS5: HT_PIOEnd state.

Transition HTPS6:4: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1:HT_HostIdle state.

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10.4.10 Host Transport decompose a DMA Setup FIS state diagram

This protocol receives a FIS that sets up the host adapter DMA controller to allow the transfer of subsequent Data FISes according to the First-party DMA protocol. For a a First-party DMA write request when Auto-Activate is not used, a separate DMA Activate FIS is issued by the device to trigger the start of the data transfer from the host.

HTDS1: HT_DS_FIS	Initialize the DMA controller for a First-party DMA transfer with the content of the DMA Setup FIS.	
1. No error detected and (Direction=1 in DMA Setup FIS) or (Direction=0 and Auto-Activate = 0 in DMA Setup FIS).	→	HT_HostIdle
2. Error detected.	→	HT_HostIdle
3. Notification of illegal transition error received from Link layer	→	HT_HostIdle
4. No error detected and (Direction=0 and Auto-Activate=1 in DMA Setup FIS).	→	HT_DMAOTrans2

HTDS1: HT_DS_FIS state: This state is entered when the Link layer has indicated that a FIS is being received and that the Transport layer has determined the FIS is of the DMA Setup type.

When in this state, the Transport layer shall initialize the DMA controller with content from the FIS.

Transition HTDS1:1: When the DMA controller has been initialized and the request is a read (Direction is set to one) or the request is a write (Direction is cleared to zero) and Auto-Activate is zero in the DMA Setup FIS, the Transport layer shall transition to the HTI1: HT_HostIdle state. This transition is made if no error is detected.

Transition HTDS1:2: When an error is detected, status shall be reported to the Link layer. The Transport layer shall transition to the HTI1:HI_HostIdle state.

Transition HTDS1:3: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1:HT_HostIdle state.

Transition HTDS1:4: When the DMA controller has been initialized and the request is a write (Direction is cleared to zero) and Auto-Activate is one in the DMA Setup FIS, the Transport layer shall transition to the HT_DMAOTrans2 state. This transition is made if no error is detected.

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10.4.11 Host transport decompose a BIST Activate FIS state diagram

This protocol receives a BIST Activate FIS that instructs the host to enter one of several Built-in Self-test modes that cause the host to retransmit the data it receives. If the mode is supported the host's Application layer places both the transmit and receive portions of the Transport, Link and/or Physical layers into appropriate state to perform the loopback operation.

HTRBIST1: HT_RcvBIST	Determine validity of loopback mode requested.	
1. Status checked, no error detected and Loopback mode valid	→	HT_BISTTrans1
2. Status checked, no error detected and Loopback mode is invalid or not supported.	→	HT_HostIdle
3. Status checked and error detected	→	HT_HostIdle
4. Notification of illegal transition error received from Link layer	→	HT_HostIdle

HTRBIST2: HT_BISTTrans1	Notify Application layer of desired BIST modes	
1. Unconditional	→	HT_HostIdle

HTRBIST1: HT_RcvBIST state: This state is entered when the link layer has indicated that a FIS is being received and the Transport layer has determined that a BIST Activate FIS is being received.

When in this state, the Transport layer shall determine the validity of the loopback request.

Transition HTRBIST1:1: If no reception error is detected and the FIS contents indicate a form of loopback request that is supported by the host the Transport layer shall make a transition to the HTRBIST2: HT_BISTTrans1 state.

Transition HTRBIST1:2: If no reception error is detected and the FIS contents indicate a form of loopback request that is not supported by the host the Transport layer shall make a transition to the HTI1:HT_HostIdle state.

Transition HTRBIST1:3: If a reception error is indicated the Transport layer shall make a transition to the HTI1:HT_HostIdle state.

Transition HTRBIST1:4: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1:HT_HostIdle state.

HTRBIST2: HT_BISTTrans1 state: This state is entered when the Transport layer has determined that a valid BIST Activate FIS has been received.

Having received a valid FIS, the Transport layer informs the Application layer that it should place the Transport, Link and Physical layers into the appropriate modes to loop the received data back to the transmitter. The method by which this is performed is not defined by this specification.

Transition HTRBIST2:1: When the Application layer has been notified the Transport layer shall transition to the HTI1:HostIdle state.

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10.5 Device transport states

10.5.1 Device transport idle state diagram

DTI0: DT_DeviceIdle	Device waits for FIS or FIS request.		
	1. Transmission of Register – Device to Host FIS requested by Application layer	→	DT_RegDHFIS
	2. Transmission of Set Device Bits FIS requested by Application layer	→	DT_DB_FIS
	3. Transmission of PIO Setup FIS requested by Application layer	→	DT_PIOSTUPFIS
	4. Transmission of DMA Activate FIS requested by Application layer	→	DT_DMAACTFIS
	5. Transmission of DMA Setup FIS requested by Application layer	→	DT_DMASTUPDHFIS
	6. Transmission of Data FIS requested by Application layer	→	DT_DATAIFIS
	7. Transmission of BIST Activate FIS requested by Application layer	→	DT_XmitBIST
	8. Frame receipt indicated by Link layer	→	DT_ChkTyp

DTI1: DT_ChkTyp	Received FIS type checked.		
	1. Register – Host to Device FIS type detected	→	DT_RegHDFIS
	2. Data FIS type detected	→	DT_DATAOFIS
	3. DMA Setup FIS type detected	→	DT_DMASTUPHDFIS
	4. BIST Activate FIS type detected	→	DT_RcvBIST
	5. Notification of illegal transition error received from Link layer or unrecognized FIS type	→	DT_DeviceIdle

DTI0: DT_DeviceIdle state: This state is entered when a Frame Information Structure (FIS) transaction has been completed by the Transport layer.

When in this state, the Transport layer waits for the Application layer to indicate that a FIS is to be transmitted or the Link layer to indicate that a FIS is being received.

Transition DTI0:1: When the Application layer indicates that a Register – Device to Host FIS is to be transmitted, the Transport layer shall make a transition to the DTR0: DT_RegDHFIS state.

Transition DTI0:2: When the Application layer indicates that a Set Device Bits FIS is to be transmitted, the Transport layer shall make a transition to the DTDB0:DT_DB_FIS state.

Transition DTI0:3: When the Application layer indicates that a PIO Setup FIS is to be transmitted, the Transport layer shall make a transition to the DTPIOSTUP0: DT_PIOSTUPFIS state.

Transition DTI0:4: When the Application layer indicates that a DMA Activate FIS is to be transmitted, the Transport layer shall make a transition to the DTDMAACT0: DT_DMAACTFIS state.

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Transition DTI0:5: When the Application layer indicates that a DMA Setup FIS is to be transmitted, the Transport layer shall make a transition to the DTDMASTUP0: DT_DMASTUPDHFIS state.

Transition DTI0:6: When the Application layer indicates that a Data FIS is to be transmitted, the Transport layer shall make a transition to the DTDATAI0: DT_DATAIFIS state.

Transition DTI0:7: When the Application layer indicates that a BIST Activate FIS is to be transmitted, the Transport layer shall make a transition to the DTXBIST1:DT XmitBIST state.

Transition DTI0:8: When the Link layer indicates that a FIS is being received, the Transport layer shall make a transition to the DTI1: DT_ChkTyp state.

DTI1: DT_ChkTyp state: This state is entered when the Transport layer is idle and Link layer indicates that a FIS is being received.

When in this state, the Transport layer checks the FIS type of the incoming FIS.

Transition DTI1:1: When the incoming FIS is a Register – Host to Device FIS type, the Transport layer shall make a transition to the DTCMD0: DT_RegHDFIS state.

Transition DTI1:2: When the incoming FIS is a Data - Host to Device FIS type, the Transport layer shall make a transition to the DTDATAO0: DT_DATAOFIS state.

Transition DTI1:3: When the incoming FIS is a DMA Setup FIS type, the Transport layer shall make a transition to the DTSTP0: DT_ DMASTUPHDFIS state.

Transition DTI1:4: When the incoming FIS is a BIST Activate FIS type, the Transport layer shall make a transition to the DTRBIST1:DT_RcvBIST state.

Transition DTI1:5: When the Transport layer receives notification from the Link layer of an illegal state transition or the FIS type is not recognized, the Transport layer shall make a transition to the DTI0: DT_DeviceIdle state.

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10.5.2 Device Transport send Register – Device to Host state diagram

This protocol builds a Register – Device to Host FIS that contains the register content and sends it to the host when the Application layer requests the transmission.

DTR0: DT_RegDHFIS	Construct Register – Device to Host FIS from the content of the registers and notify Link to transfer.		
	1. FIS transfer complete	→	DT_RegTransStatus
	2. Notification of illegal transition error received from Link layer	→	DT_DeviceIdle

DTR1: DT_RegTransStatus	Check Link and Phy transmission results and if an error occurred take appropriate action.		
	1. Status checked, and no error detected.	→	DT_DeviceIdle
	2. Status checked, and error detected.	→	DT_RegDHFIS

DTR0: DT_RegDHFIS state: This state is entered the Application requests the transmission of a Register – Device to Host FIS.

When in this state, the Transport layer shall construct a Register – Device to Host FIS, notify the Link layer that the FIS is to be transmitted, and pass the FIS to the Link layer.

Transition DTR0:1: When the entire FIS has been passed to the Link layer, the Transport layer shall indicate to the Link layer that the FIS transmission is complete and make a transition to the DTR1: DT_RegTransStatus state.

Transition DTR0:2: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the DTI0: DT_DeviceIdle state.

DTR1: DT_RegTransStatus state: This state is when the entire FIS has been passed to the Link layer.

When in this state, the Transport layer shall wait for the Link and Phy ending status for the FIS and take appropriate error handling action if required.

Transition DTR1:1: When the FIS status has been handled, and no error detected, the Transport layer shall transition to the DTI0: DT_DeviceIdle state.

Transition DTR1:2: When the FIS status has been handled, and an error detected, the Transport layer shall report status to the Link layer, and retry this transfer by transitioning to the DT_RegDHFISstate.

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10.5.3 Device Transport send Set Device Bits FIS state diagram

This protocol sends a Set Device Bits FIS to the host adapter when the Application layer requests the transmission.

DTDB0: DT_DB_FIS	Inform Link to transmit Set Device Bits FIS	
1. FIS transfer complete	→	DT_SDBTransStatus

DTDB1: DT_SDBTransStatus	Check Link and Phy transmission results and if an error occurred take appropriate action.	
1. Status checked and no error detected	→	DT_DeviceIdle
2. Status checked and error detected.	→	DT_DB_FIS

DTDB0:DT_DB_FIS state: This state is entered when the Application layer requests the transmission of a Set Device Bits FIS.

When in this state, the Transport layer shall construct a Set Device Bits FIS, notify the Link layer that the FIS is to be transmitted, and pass the FIS to the Link layer.

Transition DTDB0:1: When the entire FIS has been passed to the Link layer, the Transport layer shall indicate to the Link layer that the FIS transmission is complete and make a transition to the DTDB1:DT_SDBTransStatus state.

DTDB1:DT_SDBTransStatus state: This state is entered when the entire FIS has been passed to the Link layer.

When in this state, the Transport layer shall wait for the Link and Phy ending status for the FIS and take appropriate error handling action if required.

Transition DTDB1:1: When the FIS status has been handled and no error detected, the Transport layer shall transition to the DTI0:DT_DeviceIdle state.

Transition DTDB1:2: When the FIS status has been handled and an error detected, the Transport layer shall report status to the Link layer and retry this transfer by transitioning to the DTDB0:DT_DB_FIS state.

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10.5.4 Device Transport transmit PIO Setup – Device to Host FIS state diagram

This protocol transmits a PIO Setup – Device to Host FIS to the host. Following this PIO Setup frame, a single data frame containing PIO data shall be transmitted or received depending on the state of the D bit in the PIO Setup frame.

DTPIOSTUP0: DT_PIOSTUPFIS	Construct PIO Setup – Device to Host FIS from the content provided by the Application layer and notify Link to transfer. This FIS shall include the beginning and ending register content, the byte count, and the interrupt flag.		
1. FIS transfer complete		→	DT_PIOSTUPTransStatus
2. Notification of illegal transition error received from Link layer		→	DT_DeviceIdle

DTPIOSTUP1: DT_PIOSTUPTransStatus	Check Link and Phy transmission results and if an error occurred take appropriate action.		
1. Status checked, and no error detected.		→	DT_Device Idle
2. Status checked, and error detected.		→	DT_PIOSTUPFIS

DTPIOSTUP0: DT_PIOSTUPFIS state: This state is entered the Application layer requests the transmission of a PIO Setup – Device to Host FIS.

When in this state, the Transport layer shall construct a PIO Setup – Device to Host FIS, notify the Link layer that the FIS is to be transmitted, and pass the FIS to the Link layer.

Transition DTPIOSTUP0:1: When the entire FIS has been passed to the Link layer, the Transport layer shall indicate to the Link layer that the FIS transmission is complete and make a transition to the DTPIOSTUP1: DT_PIOSTUPTransStatus state.

Transition DTPIOSTUP0:2: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the DTI0: DT_DeviceIdle state.

DTPIOSTUP1: DT_PIOSTUPTransStatus state: This state is when the entire FIS has been passed to the Link layer.

When in this state, the Transport layer shall wait for the Link and Phy ending status for the FIS and take appropriate error handling action if required.

Transition DTPIOSTUP1:1: When the FIS status has been handled and no error detected, the Transport layer shall transition to the DTI0: DT_DeviceIdle state.

Transition DTPIOSTUP1:2: When the FIS status has been handled and an error detected, the Transport layer shall report status to the Link layer and retry this transfer by transitioning to the DT_PIOSTUPFIS state.

10.5.5 Device Transport transmit DMA Activate FIS state diagram

This protocol transmits a DMA Activate FIS to the host adapter. Following the DMA Activate FIS, a Data FIS shall be sent from the host to the device.

DTDMAACT0: DT_DMAACTFIS	Construct DMA Activate FIS from the content provided by the Application layer and notify Link to transfer.		
	1. FIS transfer complete	→	DT_DMAACTTransStatus
	2. Notification of illegal transition error received from Link layer	→	DT_DeviceIdle

DTDMAACT1: DT_DMAACTTransStatus	Check Link and Phy transmission results and if an error occurred take appropriate action.		
	1. Status checked, and no error detected.	→	DT_DeviceIdle
	2. Status checked, and error detected.	→	DT_DMAACTFIS

DTDMAACT0: DT_DMAACTFIS state: This state is entered when the Application layer requests the transmission of a DMA Activate FIS.

When in this state, the Transport layer shall construct a DMA Activate FIS, notify the Link layer that the FIS is to be transmitted, and pass the FIS to the Link layer.

Transition DTDMAACT0:1: When the entire FIS has been passed to the Link layer, the Transport layer shall indicate to the Link layer that the FIS transmission is complete and make a transition to the DTDMAACT1: DT_DMAACTTransStatus state.

Transition DTDMAACT0:2: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the DTI0: DT_DeviceIdle state.

DTDMAACT1: DT_DMAACTTransStatus state: This state entered is when the entire FIS has been passed to the Link layer.

When in this state, the Transport layer shall wait for the Link and Phy ending status for the FIS and take appropriate error handling action if required.

Transition DTDMAACT1:1: When the FIS status has been handled and no error detected, the Transport layer shall transition to the DTI0: DT_DeviceIdle state.

Transition DTDMAACT1:2: When the FIS status has been handled and an error detected, the Transport layer shall report status to the Link layer and retry this transfer by transitioning to the DT_DMAACTFIS state.

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10.5.6 Device Transport transmit DMA Setup – Device to Host FIS state diagram

This protocol transmits a DMA Setup – Device to Host FIS to the host adapter. This FIS is a request by the device for the host adapter to program the DMA controller for a First-party DMA transfer and is followed by one or more Data FISes that transfer the data to or from the host adapter depending on the direction of the transfer. The DMA Setup – Device to Host request includes the transfer direction indicator, the host buffer identifier, the host buffer offset, the byte count, and the interrupt flag.

DTDMASTUP0: DT_DMASTUPDHFIS	Construct the DMA Setup – Device to Host FIS from the content provided by the Application layer and notify Link to transfer.	
1. FIS transfer complete	→	DT_DMASTUPTransStatus
2. Notification of illegal transition error received from Link layer	→	DT_DeviceIdle

DTDMASTUP1: DT_DMASTUPTransStatus	Check Link and Phy transmission results and if an error occurred take appropriate action.	
1. Status checked, and no error detected.	→	DT_DeviceIdle
2. Status checked, and error detected.	→	DT_DMASTUPFIS

DTDMASTUP0: DT_DMASTUPDHFIS state: This state is entered when the Application layer requests the transmission of a DMA Setup – Device to Host FIS.

When in this state, the Transport layer shall construct a DMA Setup – Device to Host FIS, notify the Link layer that the FIS is to be transmitted, and pass the FIS to the Link layer.

Transition DTDMASTUP0:1: When the entire FIS has been passed to the Link layer, the Transport layer shall indicate to the Link layer that the FIS transmission is complete and make a transition to the DTDMASTUP1: DT_DMASTUPTransStatus state.

Transition DTIDMASTUP0:2: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the DTI0: DT_DeviceIdle state.

DTPDMASTUP1: DT_DMASTUPTransStatus state: This state is entered when the entire FIS has been passed to the Link layer.

When in this state, the Transport layer shall wait for the Link and Phy ending status for the FIS and take appropriate error handling action if required.

Transition DTDMASTUP1:1: When the FIS status has been handled and no error detected, the Transport layer shall transition to the DTI0: DT_DeviceIdle state.

Transition DTDMASTUP1:2: When the FIS status has been handled and an error detected, the Transport layer shall report status to the Link layer and retry this transfer by transitioning to the DT_DMASTUPFIS state.

10.5.7 Device Transport transmit Data – Device to Host FIS diagram

This protocol builds a Data – Device to Host FIS.

DTDATAI0: DT_DATAIFIS	Construct Data – Device to Host FIS content from the content provided by the Application layer and notify Link to transfer.	
1. Unconditional	→	DT_DATAITrans

DTDATAI1: DT_DATAITrans	Pass data Dwords from data FIFO to Link layer	
1. Transfer not complete	→	DT_DATAITrans
2. Transfer complete	→	DT_DATAIEnd
3. Application layer requests termination of DMA in transfer.	→	DT_DATAIEnd
4. Notification of illegal transition error received from Link layer	→	DT_DeviceIdle

DTDATAI2: DT_DATAIEnd	Check Link and Phy transmission results and if an error occurred take appropriate action.	
1. Status checked, and no error detected.	→	DT_DeviceIdle
2. Status checked, and error detected.	→	DT_DeviceIdle
3. Application layer requests termination of DMA in transfer, no error detected.	→	DT_DeviceIdle
4. Application layer requests termination of DMA in transfer, error detected.	→	DT_DeviceIdle
5. Notification of illegal transition error received from Link layer	→	DT_DeviceIdle

DTDATAI0: DT_DATAFIS state: This state is entered when the Application layer has requested the transmission of a Data – Device to Host FIS.

When in this state the Transport layer shall pass a portion of the DMA data to the Link layer.

Transition DTDATAI0:1: When ready and there is data in the FIFO to be passed to the Link layer, the Transport layer shall transition to the DTDATAI1: DT_DATAITrans state.

DTDATAI1: DT_DATAITrans state: This state is entered when data is available in the FIFO to be passed the Link layer.

When in this state, the Transport layer shall pass a Dword of data from the FIFO to the Link layer.

Transition DTDATAI1:1: When the transfer is not complete, the Transport layer shall transition to the DTDATAI1: DT_DATAITrans state.

Transition DTDATAI1:2: When the transfer is complete, the Transport layer shall transition to the DTDATAI2: DT_DATAIEnd state.

Transition DTDATAI1:3: When the Application layer requests that a DMA operation is to be aborted, the Transport Layer shall transition to the DTDATAI2:DT_DATAIEnd state.

Transition DTDATAI1:4: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the DTI0: DT_DeviceIdle state.

DTDATAI2: DT_DATAIEnd state: This state is entered when the data transfer is complete or an abort has been requested by the Application layer.

When in this state, the Transport layer shall wait for the Link layer and Phy layer ending status for the FIS and take appropriate error handling action if required.

Transition DTDATAI2:1: When the FIS status has been handled and no error detected, the Transport layer shall transition to the DTI0: DT_DeviceIdle state.

Transition DTDATAI2:2: When the FIS status has been handled and an error detected, status shall be reported to the Link layer. The Transport layer shall transition to the DTI0: DT_DeviceIdle state.

Transition DTDATAI2:3: When the Application layer requests the termination of a DMA data in transaction, it reports the abort condition to the Link layer, waits for an EOF_P and, if no error is detected, shall transition to the DTI0:DT_DeviceIdle state.

Transition DTDATAI2:4: When the Application layer requests the termination of a DMA data in transaction, it reports the abort condition to the Link layer, waits for an EOF_P, and if an error is detected, reports the error to the Link layer, and shall transition to the DTI0:DT_DeviceIdle state.

Transition DTDATAI2:5: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall transition to the DTI0: DT_DeviceIdle state.

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10.5.8 Device Transport transmit BIST Activate FIS diagram

This protocol builds a BIST Activate FIS that tells the host to prepare to enter the appropriate Built-in Self Test mode. After successful transmission, the device Transport layer enters the idle state. The Application layer, upon detecting successful transmission to the host shall then cause the device's Transport layer, Link layer and Physical layer to enter the appropriate mode for the transmission of the Built-in Test data defined by the FIS. The means by which the Transport, Link and Physical layers are placed into self-test mode are not defined by this specification.

DTXBIST1: DT_XmitBIST	Construct the BIST Activate FIS from the content provided by the Application layer and notifies Link to transfer.		
	1. FIS transfer complete	→	DT_TransBISTStatus
	2. Notification of illegal transition error received from Link layer	→	DT_DeviceIdle

DTXBIST2: DT_TransBISTStatus	Check Link and Phy transmission results and if an error occurred take appropriate action.		
	1. Status check completed	→	DT_DeviceIdle
	2. Status check and at least one error detected	→	DT_XmitBIST[1]
	NOTE: 1. Re-transmission of the BIST Activate FIS due to errors is not required but allowed.		

DTXBIST1: DT_XmitBIST state: This state is entered to send a BIST FIS to the host.

Transition DTXBIST1:1: When the entire FIS has been passed to the Link layer, the Transport layer shall indicate to the Link layer that the FIS transmission is complete and make a transition to the DTXBIST2:DT_TransBISTSTatus state.

Transition DTXBIST1:2: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the DTI0: DT_DeviceIdle state.

DTXBIST2: DT_TransBISTStatus state: This state is entered when the entire FIS has been passed to the Link layer.

Transition DTXBIST2:1: When the FIS transmission is completed the Transport layer shall transition to the DTI0: DT_DeviceIdle state.

Transition DTXBIST2:2: When the FIS transmission is completed and at least one error is detected, the Transport layer may transition to the DTXBIST1: DT_XmitBIST state.

10.5.9 Device Transport decompose Register – Host to Device state diagram

This protocol receives a Register – Host to Device FIS, places received register content into the device registers, and notifies the Application layer of the FIS receipt.

DTCMD0: DT_RegHDFIS	Receive a Register – Host to Device FIS		
	1. FIS transfer complete, and no error detected.	→	DT_DeviceIdle
	2. FIS transfer complete, and error detected	→	DT_DeviceIdle
	3. Notification of illegal transition error received from Link layer	→	DT_DeviceIdle

DTCMD0: DT_RegHDFIS state: This state is entered when the receipt of a DT_RegHDFISFIS is recognized.

When in this state, the Transport layer shall receive the FIS and place the contents of the FIS into the device registers when it is determined that the FIS was received without error.

Transition DTCMD0:1: When the entire FIS has been received from the Link layer without error, the Transport layer shall indicate to the Application layer that a command FIS was received and make a transition to the DTI0: DT_DeviceIdle state.

Transition DTCMD0:2: When the entire FIS has been received from the Link layer and an error has been detected, status shall be sent to the Link layer. The Transport layer shall make a transition to the DTI0:DT_DeviceIdle state.

Transition DTCMD0:3: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the DTI0: DT_DeviceIdle state.

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10.5.10 Device Transport decompose Data (Host to Device) FIS state diagram

This protocol receives a Data - Host to Device FIS.

DTDATAO0: DT_DATAOFIS	Prepare to receive data		
	Unconditional	→	DT_DATAOREC

DTDATAO1: DT_DATAOREC	Place received data Dword into data FIFO and signal Link to continue transfer.		
	1. Transfer not complete	→	DT_DATAOREC
	2. Transfer complete	→	DT_DeviceIdle
	3. Abort Transfer from Application layer	→	DT_DeviceAbort
	4. Notification of illegal transition error received from Link layer	→	DT_DeviceIdle

DTDATAO2: DT_DeviceAbort	Signal Link to abort transfer.		
	1. Transfer not complete	→	DT_DATAOREC
	2. Transfer complete	→	DT_ DeviceIdle

DTDATAO0: DT_DATAOFIS state: This state is entered when the Link layer has indicated that a FIS is being received and that the Transport layer has determined the FIS is of Data - Host to Device type.

When in this state, the Transport layer shall prepare to receive the data.

Transition DTDATAO0:1: When ready to receive the data, the Transport layer shall make a transition to the DTDATAO1: DT_DATAOREC state.

DTDATAO1: DT_DATAOREC state: This state is entered when the Transport layer is ready to receive the data.

When in this state, the Transport layer shall wait for the Link layer to indicate the transfer is complete.

Transition DTDATAO1:1: When Link layer has not indicated that the end of the FIS has been reached, the Transport layer shall transition to the DTDATAO1: DT_DATAOREC state.

Transition DTDATAO1:2: When the Link layer indicates that the end of the FIS has been reached, the Transport layer shall transition to the DTI0: DT_DeviceIdle state.

Transition DTDATAO1:3: When the Application layer indicates that the FIS is to be aborted, the Transport layer shall transition to the DTDATAO2: DT_DeviceAbort state.

Transition DTDATAO1:4: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the DTI0: DT_DeviceIdle state.

DTDATAO2: DT_DeviceAbort state: This state is entered when the Application layer indicates that the current transfer is to be aborted.

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When in this state, the Transport layer shall signal the Link layer to Abort the incoming transmission and return to either DT_DATAOREC or DT_DATAOhold, depending upon the current state of the FIFO. If the abort occurs coincident with an end of transfer indication from the Link, then the transition to DTI0: DT_DeviceIdle is also accommodated. After issuing an Abort, the Transport returns to normal data transfer, and awaits the end of transfer indication from the Link.

Transition DTDATAO2:1: Inform Link layer to issue an abort. When Transfer is not complete, the Transport layer shall transition to the DTDATAO1: DT_DATAOREC state.

Transition DTDATAO2:2: Inform Link layer to issue an abort. When the Link layer indicates that the end of the FIS has been reached, the Transport layer shall transition to the DTI0: DT_DeviceIdle state.

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10.5.11 Device Transport decompose DMA Setup – Host to Device state diagram

This protocol receives a DMA Setup – Host to Device FIS, passes received DMA Setup content, and notification of FIS receipt to the Application layer.

DTSTP0: DT_DMASTUPHDFIS	Receive a DMA Setup – Host to Device FIS	
1. FIS transfer complete, and no error detected.	→	DT_DeviceIdle
2. FIS transfer complete, and error detected	→	DT_DeviceIdle
3. Notification of illegal transition error received from Link layer	→	DT_DeviceIdle

DTSTP0: DT_DMASTUPHDFIS state: This state is entered when the receipt of a DT_DMASTUP FIS is recognized.

Transition DTSTP0:1: When the entire FIS has been received from the Link layer without error, the Transport layer shall indicate to the Application layer that a DMA Setup – Host to Device FIS was received and make a transition to the DTI0: DT_DeviceIdle state.

Transition DTSTP0:2: When the entire FIS has been received from the Link layer and an error has been detected, status shall be sent to the link layer. The Transport layer shall make a transition to the DTI0: DT_DeviceIdle state.

Transition DTSTP0:3: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the DTI0: DT_DeviceIdle state.

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10.5.12 Device Transport decompose a BIST Activate FIS state diagram

This protocol receives a FIS that instructs the device to enter one of several Built-in Self-test modes that cause the device to retransmit the data it receives. If the mode is supported the Device's Application layer places both the transmit and receive portions of the Transport, Link and/or Physical layers into appropriate state to perform the loopback operation.

DTRBIST1: DT_RcvBIST	Determine validity of loopback mode requested.	
1. Status checked, no error detected and Loopback mode valid	→	DT_BISTTrans1
2. Status checked, no error detected and Loopback mode is invalid or not supported.	→	DT_DeviceIdle
3. Status checked and error detected	→	DT_DeviceIdle
4. Notification of illegal transition error received from Link layer	→	DT_DeviceIdle

DTRBIST2: DT_BISTTrans1	Notify Application layer of desired BIST modes	
1. Unconditional	→	DT_DeviceIdle

DTRBIST1: DT_RcvBIST state: This state is entered when the Link layer has indicated that a FIS is being received and the Transport layer has determined that a BIST Activate FIS is being received.

When in this state, the Transport layer shall determine the validity of the loopback request.

Transition DTRBIST1:1: If no reception error is detected and the FIS contents indicate a form of loopback request that is supported by the host the Transport layer shall make a transition to the DTRBIST2: DT_BISTTrans1 state.

Transition DTRBIST1:2: If no reception error is detected and the FIS contents indicate a form of loopback request that is not supported by the host the Transport layer shall make a transition to the DTI0:DT_DeviceIdle state.

Transition DTRBIST1:3: If a reception error is indicated the Transport layer shall make a transition to the DTI0:DT_DeviceIdle state.

Transition DTRBIST1:4: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the DTI0: DT_DeviceIdle state.

DTRBIST2: DT_BISTTrans1 state: This state is entered when the Transport layer has determined that a valid BIST Activate FIS has been received.

Having received a valid FIS, the Transport layer informs the Application layer that it should place the Transport, Link and Physical layers into the appropriate modes to loop the received data back to the transmitter. The method by which this is performed is not defined by this specification.

Transition DTRBIST2:1: When the Application layer has been notified the Transport layer shall transition to the DTI0:DT_DeviceIdle state.

11 Device command layer protocol

In the following Device command layer protocols, if the host sends COMRESET before the device has completed executing a command layer protocol, then the device shall start executing the COMRESET protocol from the beginning. If the device receives a Register – Host to Device FIS with C=0 and the SRST bit set to one before the device has completed executing a command layer protocol, then the device shall start executing its software reset protocol from the beginning.

SYNC Escape is used by a host or device to bring the link back to a known state, and may be used for vendor specific recovery of error or hang conditions. After a SYNC Escape is performed, a software reset may be necessary prior to issuing the next command to the device.

11.1 Power-on and COMRESET protocol

If the host asserts Hard Reset regardless of the power management mode or the current device command layer state, the device shall execute the hardware reset protocol.

DHR0: Hardware_reset_asserted	Wait.	
1. COMRESET negated.	→	DHR1: Execute_diagnostics

DHR1: Execute_diagnostics	Initialize hardware and execute diagnostics.	
1. Initialization and diagnostics completed successfully.	→	DHR2: Send_good_status
2. Initialization completed and diagnostics failed.	→	DHR3: Send_bad_status

DHR2: Send_good_status	Request transmission of Register FIS with good status.	
1. Register FIS transmitted.	→	DI0: Device_idle

DHR3: Send_bad_status	Request transmission of Register FIS with bad status.	
1. Register FIS transmitted.	→	DI0: Device_idle

DHR0: Hardware_reset_asserted: This state is entered when the Transport layer indicates that the COMRESET signal is asserted.

When in this state, the device awaits the negation of the COMRESET signal.

Transition DHR0:1: When the Transport layer indicates that the COMRESET signal has been negated, the device shall transition to the DHR1: Execute_diagnostics state.

DHR1: Execute_diagnostics: This state is entered when the Transport layer indicates that the COMRESET signal has been negated.

When in this state, the device initializes the device hardware and executes its power-up diagnostics.

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Transition DHR1:1: When the device hardware has been initialized and the power-up diagnostics successfully completed, the device shall transition to the DHR2: Send_good_status state.

Transition DHR1:2: When the device hardware has been initialized and the power-up diagnostics failed, the device shall transition to the DHR3: Send_bad_status state.

DHR2: Send_good_status: This state is entered when the device hardware has been initialized and the power-up diagnostics successfully completed.

When in this state, the device requests that the Transport layer transmit a Register FIS to the host. If the device does not implement the PACKET command feature set the register content shall be:

Sector Count	01h
LBA Low	01h
LBA Mid	00h
LBA High	00h
Device	00h
Error	01h
Status	00h-70h (see note)
NOTE – Setting of bits [6:4] in the Status register are device specific.	

If the device implements the PACKET command feature set, the register content shall be:

Sector Count	01h
LBA Low	01h
LBA Mid	14h
LBA High	EBh
Device	00h
Error	01h
Status	00h

Transition DHR2:1: When the Transport layer indicates that the Register FIS has been transmitted, the device shall transition to the DI0: Device_Idle state.

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DHR3: Send_bad_status: This state is entered when the device hardware has been initialized and the power-up diagnostics failed.

When in this state, the device requests that the Transport layer transmit a Register FIS to the host. If the device does not implement the PACKET command feature set the register content shall be:

Sector Count	01h
LBA Low	01h
LBA Mid	00h
LBA High	00h
Device	00h
Error	00h, 02h-7Fh
Status	00h-70h (see note)
NOTE – Setting of bits [6:4] in the Status register are device specific.	

If the device implements the PACKET command feature set, the register content shall be:

Sector Count	01h
LBA Low	01h
LBA Mid	14h
LBA High	EBh
Device	00h
Error	00h, 02h-7Fh
Status	00h

Transition DHR3:1: When the Transport layer indicates that the Register FIS has been transmitted, the device shall transition to the DI0: Device_Idle state.

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11.2 Device Idle protocol

The state diagram below describes the idle protocol for a device. States and transitions preceded by an * are utilized when Native Command Queuing or ATA Tagged Command Queuing commands are implemented.

DI0: Device_idle	Wait.	
1. FIS receipt	→	DI1: Check_FIS
2. * Ready to complete released command.	→	DI4: Set_service
3. * Ready to receive data for WRITE FPDMA QUEUED command and FIS receipt not indicated and no error encountered	→	DFPDMAQ4: DataPhase_ PreWriteSetup
4. * Ready to transmit data for READ FPDMA QUEUED command and FIS receipt not indicated and no error encountered	→	DFPDMAQ3: DataPhase_ ReadSetup
5. * One or more FPDMA QUEUED commands completed successfully and FIS receipt not indicated and no error encountered	→	DFPDMAQ10: SendStatus[1]
6. * FPDMA QUEUED command terminated with failure and FIS receipt not indicated	→	DFPDMAQ11: ERROR
7. Asynchronous Notification is enabled and event has occurred that requires notification and NotifyPending = 0 and FIS receipt not indicated.	→	AN0: Notify_host
NOTE: 1. This condition may be true simultaneously with condition 3 or 4. Devices implementing status aggregation may select any of the transitions 3, 4, or 5 if their conditions evaluate to true. Devices not implementing status aggregation shall prioritize transition 5 over transitions 3 and 4.		

DI1: Check_FIS	Check_FIS type and C bit.	
1. Register type, C bit cleared, and SRST set.	→	DSR0: Software_reset_ asserted
2. Register type, C bit cleared, and SRST cleared	→	DI0: Device_idle[1]
3. Register type and C bit set.	→	DI2: Check_command
4. DMA Setup FIS Received	→	DI0 : Device_idle
5. Unexpected FIS type.	→	DI0: Device_idle
NOTE: 1. A Device to Host Register FIS shall not be sent in response to the received Register FIS.		

DI2: Check_command[1]	Check the command to determine required command protocol. If asynchronous notification is supported then NotifyPending is cleared to zero.	
1. Non-data command protocol and no native queued command outstanding.	→	DND0: Non-data
2. PIO data-in command protocol and no native queued command outstanding.	→	DPIOI0: PIO_in
3. PIO data-out command protocol and no native queued command outstanding.	→	DPIOO0: PIO_out
4. READ DMA command protocol (legacy) and no native queued command outstanding.	→	DDMAI0: DMA_in
5. WRITE DMA command protocol (legacy) and no native queued command outstanding.	→	DDMAO0: DMA_out
6. PACKET command protocol and no native queued command outstanding.	→	DP0: PACKET
7. * READ DMA QUEUED command protocol (legacy) and no native queued command outstanding.	→	DDMAQI0: DMA_queued_in
8. * WRITE DMA QUEUED command protocol (legacy) and no native queued command outstanding.	→	DDMAQIO: DMA_queued_out
9. EXECUTE DEVICE DIAGNOSTIC command protocol and no native queued command outstanding.	→	DEDD0: Execute_device_diag
10. DEVICE RESET command protocol.	→	DDR0: Device_reset
11. Command not implemented and no native queued command outstanding.	→	DI3: No_command
12. * SERVICE command protocol and no native queued command outstanding.	→	DI5: Service
13. * READ FPDMA QUEUED command protocol.	→	DFPDMAQ1: AddCommand_ ToQueue
14. * WRITE FPDMA QUEUED command protocol.	→	DFPDMAQ1: AddCommand_ ToQueue
15. * Not READ FPDMA QUEUED and not WRITE FPDMA QUEUED and not DEVICE RESET and native queued command(s) outstanding	→	DFPDMAQ12: BrokenHost_ ClearBusy
NOTE: 1. This state shows transitions for all commands. If a device does not implement any particular command, then that transition should not be processed.		

DI3: No_command	Request transmission of Register FIS with ABRT error.	
1. FIS transmission complete.	→	DI0: Device_idle

* DI4: Set_service	Request transmission of Set Device Bits FIS with SERV set.	
1. FIS transmission complete.	→	DI0: Device_idle

* DI5: Service_test	Test command to see if Register FIS is needed to set DRQ and set Tag.	
1. PACKET PIO data-in or PACKET PIO data-out.	→	DI7: Service_decode
2. Other	→	DI6: Service_send_tag

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* DI6: Service_send_tag	Request transmission of Register FIS with BSY=0, DRQ=1, and SC=Tag		
	1. FIS transmission complete	→	DI7: Service_decode

* DI7: Service_decode	Check command type to be serviced.		
	1. PACKET PIO data-in.	→	DP4: PACKET_PIO_in
	2. PACKET PIO data-out.	→	DP6: PACKET_PIO_out
	3. PACKET DMA data-in.	→	DP9: PACKET_DMA_in
	4. PACKET DMA data-out.	→	DP11: PACKET_DMA_out
	5. READ DMA QUEUED.	→	DDMAQI1: Send_data
	6. WRITE DMA QUEUED.	→	DDMAQO1: Send_DMA_activate

DI0: Device_Idle: This state is entered when the device has completed the execution of a command protocol, a COMRESET protocol, a software reset protocol, or a queued command has been released.

When in this state, the device is awaiting a command. If queuing is supported, the device may be waiting to acquire data or establish buffer space to complete a queued command

Transition DI0:1: When the device receives a FIS from the Transport layer, the device shall transition to the DI1: Check_FIS state.

*** Transition DI0:2:** When the device is ready to complete the data transfer for a queued command, the device shall transition to the DI4: Set_service state.

*** Transition DI0:3:** When the device is ready to receive the data for a WRITE FPDMA QUEUED command, the device shall transition to the DFPDMAQ4: DataPhasePreWriteSetup state. This condition also applies for the case where non-zero buffer offsets are used to complete a previous partial data transfer.

*** Transition DI0:4:** When the device is ready to transmit the data for a READ FPDMA QUEUED command, the device shall transition to the DFPDMAQ3: DataPhaseReadSetup state. This condition also applies for the case where non-zero buffer offsets are used to complete a previous partial data transfer.

*** Transition DI0:5:** When the device has successfully completed a FPDMA QUEUED command, the device shall transition to the DFPDMAQ10: SendStatus state.

*** Transition DI0:6:** When the device has encountered an error in a FPDMA QUEUED command, the device shall transition to the DFPDMAQ11: ERROR state.

Transition DI0:7: If Asynchronous Notification is enabled and an event requiring notification of the host has occurred and the NotifyPending variable is cleared to zero and FIS receipt not indicated, the device shall transition to the AN0: AN_Notify state.

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DI1: Check_FIS state: This state is entered when the device receives a FIS from the Transport layer.

When in this state, the device shall check the FIS type.

Transition DI1:1: If the FIS type is a Register FIS, the C bit in the FIS is cleared, and the SRST bit in the FIS is set, the device shall transition to the DSR0: Software_reset_asserted state.

Transition DI1:2: If the FIS type is a Register FIS, the C bit in the FIS is cleared, and the SRST bit in the FIS is cleared, the device shall transition to the DI0: Device_idle state.

Transition DI1:3: If the FIS type is a Register FIS and the C bit in the FIS is set, the device shall transition to the DI2: Check_command state.

Transition DI1:4: If the FIS type is a First Party DMA Setup FIS, the device shall inform the Transport layer of the reception of the First Party DMA Setup FIS, and transition to the DI0: Device_idle state.

Transition DI1:5: For any other FIS, the device shall transition to the DI0: Device_idle state.

DI2: Check_command state: This state is entered when the device recognizes that the received Register FIS contains a new command. NOTE: This state shows transitions for all commands. If a device does not implement any particular command, then transition DI2:11 to state DI3:No_command shall be made.

When in this state, the device shall check the command protocol required by the received command and clears NotifyPending to zero if asynchronous notification is supported. Clearing NotifyPending to zero allows future asynchronous notification messages to be sent to the host.

Transition DI2:1: When the received command is a non-data transfer command, the device shall transition to the DND0: Non-data state.

Transition DI2:2: When the received command is a PIO data-in command, the device shall transition to the DPIOI0: PIO_in state.

Transition DI2:3: When the received command is a PIO data-out command, the device shall transition to the DPIOO0: PIO_out state.

Transition DI2:4: When the received command is a READ DMA command, the device shall transition to the DDMAI0: DMA_in state.

Transition DI2:5: When the received command is a WRITE DMA command, the device shall transition to the DDMAO0: DMA_out state.

Transition DI2:6: When the received command is a PACKET command, the device shall transition to the DP0: PACKET state.

* **Transition DI2:7:** When the received command is a READ DMA QUEUED command, the device shall transition to the DDMAQI0: DMA_queued_in state.

* **Transition DI2:8:** When the received command is a WRITE DMA QUEUED command, the device shall transition to the DDMAQO0: DMA_queued_out state.

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Transition DI2:9: When the received command is an EXECUTE DEVICE DIAGNOSTICS command, the device shall transition to the DEDD0: Execute_device_diag state.

Transition DI2:10: When the received command is an RESET DEVICE command, the device shall transition to the DDR0: Device_reset state.

Transition DI2:11: When the received command is not implemented by the device, the device shall transition to the DI3: No_command state.

* **Transition DI2:12:** When the received command is a SERVICE command, the device shall transition to the DI5: Service state.

* **Transition DI2:13:** When the received command is a READ FPDMA QUEUED command protocol, the device shall transition to the DFPDMAQ1: AddCommandToQueue state.

* **Transition DI2:14:** When the received command is a WRITE FPDMA QUEUED command protocol, the device shall transition to the DFPDMAQ1: AddCommandToQueue state.

* **Transition DI2:15:** When the received command is a not a READ FPDMA QUEUED; and not a WRITE FPDMA QUEUED; and not a DEVICE RESET; and there are native queued command(s) outstanding, an error has occurred and the device shall transition to the DFPDMAQ12: BrokenHost_ClearBusy state.

DI3: No_command state: This state is entered when the device recognizes that the received command is not implemented by the device.

When in this state, the device shall request that the Transport layer transmit a Register FIS with register content as described in the command description in the ATA/ATAPI-6 standard and the I bit set to one.

Transition DI2:1: When the Transport layer has transmitted the Register FIS, the device shall transition to the DI0: Device_idle state.

* **DI4: Set_service state:** This state is entered when the ready to complete the data transfer for a queued command.

When in this state, the device shall request that the Transport layer transmit a Set Device Bits FIS with the SERV bit set in the Status register and with all other bits in the Error and Status fields the same as the current contents of the respective registers, and the I bit set to one.

Transition DI4:1: When the Transport layer has transmitted the Set Device Bits FIS, the device shall transition to the DI0: Device_idle state.

* **DI5: Service_test state:** This state is entered when the SERVICE command has been received.

When in this state, the device shall determine the type of command that the device has requested service to complete. The PACKET command using the PIO protocol provides its own register update to set DRQ and send the command tag, but other queued commands require a Register FIS.

Transition DI5:1: When the command to be serviced is a PIO data-in or PIO data-out command, the device shall transition to the DI7: Service_decode state.

Transition DI5:2: When the command to be serviced is neither a PIO data-in nor a PIO data-out command, the device shall transition to the DI6: Service_send_tag state.

*** DI6: Service_send_tag state:** This state is entered when the SERVICE command has been received and sending a Register Device to Host FIS is necessary for the command being serviced.

When in this state, the device shall request that the Transport layer transmit a Register FIS with register contents, including the desired command tag, as described in the command description of the ATA/ATAPI-6 standard for the command being serviced.

Transition DI6:1: When the Transport layer has transmitted the Register FIS, the device shall transition to theDI7: Service_decode state.

*** DI7: Service_decode state:** This state is entered when a Register FIS has been transmitted, if necessary to send the register contents, including the desired command tag, in response to a SERVICE command.

When in this state, the device shall again determine the type of command that the device has requested service to complete, and branch to that command's data transfer and completion.

Transition DI7:1: When the command to be serviced is a PIO data-in command, the device shall transition to the DP4: PACKET_PIO_in state.

Transition DI7:2: When the command to be serviced is a PIO data-out command, the device shall transition to the DP6: PACKET_PIO_out state.

Transition DI7:3: When the command to be serviced is a DMA data-in command, the device shall transition to the DP9: PACKET_DMA_in state.

Transition DI7:4: When the command to be serviced is a DMA data-out command, the device shall transition to the DP11: PACKET_DMA_out state.

Transition DI7:5: When the command to be serviced is a READ DMA QUEUED command, the device shall transition to the DDMAQI1: Send_data state.

Transition DI7:6: When the command to be serviced is a WRITE DMA QUEUED command, the device shall transition to the DDMAQO1: Send_DMA_activate state.

11.3 Software reset protocol

When the host sends a Register FIS with a one in the SRST bit position of the Device Control register byte, regardless of the power management mode, the device shall execute the software reset protocol.

DSR0: Software_reset_asserted	Begin initialization and diagnostic execution.	
1. Software reset negated.	→	DSR1: Execute_diagnostics
2. Software reset asserted.	→	DSR0: Software_reset_ asserted

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DSR1: Execute_diagnostics	Complete Initialization and diagnostics execution.		
	1. Initialization and diagnostics completed successfully.	→	DSR2: Send_good_status
	2. Initialization completed and diagnostics failed.	→	DSR3: Send_bad_status

DSR2: Send_good_status	Request transmission of Register FIS with good status.		
	1. Register FIS transmitted.	→	DI0: Device_idle

DSR3: Send_bad_status	Request transmission of Register FIS with bad status.		
	1. Register FIS transmitted.	→	DI0: Device_idle

DSR0: Software_reset_asserted: This state is entered when a Register FIS is received with the C bit in the FIS cleared to zero and the SRST bit set to one in the Device Control register.

When in this state, the device begins its initialization and diagnostics execution and awaits the clearing of the SRST bit.

Transition DSR0:1: When a Register FIS is received with the C bit in the FIS cleared to zero and the SRST bit cleared to zero in the Device Control register, the device shall transition to the DSR1: Execute_diagnostics state.

Transition DSR0:2: If a Register FIS is received with the C bit in the FIS set to one, or the SRST bit set to one in the Device Control register, the device shall transition to the DSR0: Software_reset_asserted state.

DSR1: Execute_diagnostics: This state is entered when a Register FIS is received with the C bit in the FIS cleared to zero and the SRST bit cleared to zero in the Device Control register.

When in this state, the device completes initialization and execution of its diagnostics.

Transition DSR1:1: When the device has been initialized and the diagnostics successfully completed, the device shall transition to the DSR2: Send_good_status state.

Transition DSR1:2: When the device has been initialized and the diagnostics failed, the device shall transition to the DSR3: Send_bad_status state.

DSR2: Send_good_status: This state is entered when the device has been initialized and the diagnostics successfully completed.

When in this state, the device requests that the Transport layer transmit a Register FIS to the host. If the device does not implement the PACKET command feature set the register content shall be:

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Sector Count	01h
LBA Low	01h
LBA Mid	00h
LBA High	00h
Device	00h
Error	01h
Status	00h-70h (see note)
NOTE – Setting of bits [6:4] in the Status register are device specific.	

If the device implements the PACKET command feature set, the register content shall be:

Sector Count	01h
LBA Low	01h
LBA Mid	14h
LBA High	EBh
Device	00h
Error	01h
Status	00h

Transition DSR2:1: When the Transport layer indicates that the Register FIS has been transmitted, the device shall transition to the DI0: Device_Idle state.

DSR3: Send_bad_status: This state is entered when the device has been initialized and the diagnostics failed.

When in this state, the device requests that the Transport layer transmit a Register FIS to the host. If the device does not implement the PACKET command feature set the register content shall be:

Sector Count	01h
LBA Low	01h
LBA Mid	00h
LBA High	00h
Device	00h
Error	00h, 02h-7Fh
Status	00h-70h (see note)
NOTE – Setting of bits [6:4] in the Status register are device specific.	

If the device implements the PACKET command feature set, the register content shall be:

Sector Count	01h
LBA Low	01h
LBA Mid	14h
LBA High	EBh
Device	00h
Error	00h, 02h-7Fh
Status	00h

Transition DSR3:1: When the Transport layer indicates that the Register FIS has been transmitted, the device shall transition to the DI0: Device_Idle state.

11.4 EXECUTE DEVICE DIAGNOSTIC command protocol

This class includes:

– EXECUTE DEVICE DIAGNOSTIC

If the host sends COMRESET before the device has completed executing the EXECUTE DEVICE DIAGNOSTIC protocol, then the device shall immediately start executing the COMRESET protocol form the beginning. If the host asserts SRST in the Device Control register before the device has completed executing the EXECUTE DEVICE DIAGNOSTIC protocol, then the device shall immediately start executing its software reset protocol from the beginning.

DEDD0: Execute_device_diag	Execute diagnostics.	
1. Diagnostics completed successfully.	→	DEDD1: Send_good_status
2. Diagnostics failed.	→	DEDD2: Send_bad_status

DEDD1: Send_good_status	Request transmission of Register FIS with good status.	
1. Register FIS transmitted.	→	DI0: Device_idle

DEDD2: Send_bad_status	Request transmission of Register FIS with bad status.	
1. Register FIS transmitted.	→	DI0: Device_idle

DEDD0: Execute_device_diag: This state is entered when an EXECUTE DEVICE DIAGNOSTIC command is received.

When in this state, the device executes its diagnostics.

Transition DEDD0:1: When the device successfully completed the diagnostics, the device shall transition to the DEDD1: Send_good_status state.

Transition DEDD1:2: When the device has failed the diagnostics, the device shall transition to the DEDD2: Send_bad_status state.

DEDD1: Send_good_status: This state is entered when the device has successfully completed the diagnostics.

When in this state, the device shall request that the Transport layer transmit a Register FIS to the host, with the I bit set to one. If the device does not implement the PACKET command feature set the register content shall be:

Sector Count	01h
LBA Low	01h
LBA Mid	00h
LBA High	00h
Device	00h
Error	01h
Status	00h-70h (see note)
NOTE – Setting of bits [6:4] in the Status register are device specific.	

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If the device implements the PACKET command feature set, the register content shall be:

Sector Count	01h
LBA Low	01h
LBA Mid	14h
LBA High	EBh
Device	00h
Error	01h
Status	00h

Transition DEDD1:1: When the Transport layer indicates that the Register FIS has been transmitted, the device shall transition to the DI0: Device_Idle state.

DEDD2: Send_bad_status: This state is entered when the device has been initialized and the diagnostics failed.

When in this state, the device shall request that the Transport layer transmit a Register FIS to the host, with the I bit set to one. If the device does not implement the PACKET command feature set the register content shall be:

Sector Count	01h
LBA Low	01h
LBA Mid	00h
LBA High	00h
Device	00h
Error	00h, 02h-7Fh
Status	00h-70h (see note)
NOTE – Setting of bits [6:4] in the Status register are device specific.	

If the device implements the PACKET command feature set, the register content shall be:

Sector Count	01h
LBA Low	01h
LBA Mid	14h
LBA High	EBh
Device	00h
Error	00h, 02h-7Fh
Status	00h

Transition DEDD2:1: When the Transport layer indicates that the Register FIS has been transmitted, the device shall transition to the DI0: Device_Idle state.

11.5 DEVICE RESET command protocol

This class includes:

– DEVICE RESET

If the host sends COMRESET before the device has completed executing the DEVICE RESET protocol, then the device shall immediately start executing the COMRESET protocol from the beginning. If the host asserts SRST in the Device Control register before the device has

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completed executing the DEVICE RESET protocol, then the device shall immediately start executing its software reset protocol from the beginning.

DDR0: Device_reset	Stop execution and background activity.	
1. Activity ceased.	→	DDR1: Send_good_status

DDR1: Send_good_status	Request transmission of Register – Device to Host FIS with good status.	
1. Register FIS transmitted.	→	DI0: Device_idle

DDR0: Device_reset: This state is entered when an DEVICE RESET command is received.

When in this state, the device stops any execution or activity in progress.

Transition DDR0:1: When the device has ceased any execution or activity and has completed its internal diagnostics, the device shall transition to the DDR1: Send_good_status state.

DDR1: Send_good_status: This state is entered when the device has been initialized and the diagnostics successfully completed.

When in this state, the device requests that the Transport layer transmit a Register – Device to Host FIS to the host.

The register content shall be:

Sector Count	01h
LBA Low	01h
LBA Mid	14h
LBA High	EBh
Device	00h
Error	01h
Status	00h

Transition DDR1:1: When the Transport layer indicates that the Register – Device to Host FIS has been transmitted, the device shall transition to the DI0: Device_Idle state.

11.6 Non-data command protocol

This class includes:

- CFA ERASE SECTORS
- CFA REQUEST EXTENDED ERROR CODE
- CHECK POWER MODE
- FLUSH CACHE
- FLUSH CACHE EXT
- GET MEDIA STATUS
- IDLE
- IDLE IMMEDIATE

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- INITIALIZE DEVICE PARAMETERS
- MEDIA EJECT
- MEDIA LOCK
- MEDIA UNLOCK
- NOP
- READ NATIVE MAX ADDRESS
- READ NATIVE MAX ADDRESS EXT
- READ VERIFY SECTOR(S)
- SECURITY ERASE PREPARE
- SECURITY FREEZE LOCK
- SEEK
- SET FEATURES
- SET MAX ADDRESS
- SET MAX ADDRESS EXT
- SET MULTIPLE MODE
- SLEEP
- SMART DISABLE OPERATION
- SMART ENABLE/DISABLE AUTOSAVE
- SMART ENABLE OPERATION
- SMART EXECUTE OFFLINE IMMEDIATE
- SMART RETURN STATUS
- STANDBY
- STANDBY IMMEDIATE

Execution of these commands involves no data transfer. See the NOP command description and the SLEEP command description for additional protocol requirements.

DND0: Non-data	Execute Non-data command.		
1. Command execution complete.		→	DND1: Send_status

DND1: Send_status	Request transmission of a Register FIS.		
1. FIS transmission complete.		→	DI0: Device_idle

DND0: Non-data State: This state is entered when a received command is a non-data command.

When in this state, the device shall execute the requested command if supported.

Transition DND0: 1: When command execution completes, the device shall transition to the DND1: Send_status state.

DND1: Send_status State: This state is entered when the execution of the non-data command has been completed.

When in this state, the device shall request that the Transport layer transmit a Register FIS with register content as described in the command description in the ATA/ATAPI-6 standard and the I bit set to one.

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Transition DND1:1: When the FIS has been transmitted, then the device shall transition to the DI0: Device_idle state.

11.7 PIO data-in command protocol

This class includes:

- IDENTIFY DEVICE
- IDENTIFY PACKET DEVICE
- READ BUFFER
- READ LOG EXT
- READ MULTIPLE
- READ MULTIPLE EXT
- READ SECTOR(S)
- READ SECTOR(S) EXT
- SMART READ DATA
- SMART READ LOG SECTOR

Execution of this class of command includes the PIO transfer of one or more blocks of data from the device to the host.

DPIOI0: PIO_in	Prepare a DRQ data block for transfer to the host.	
1. DRQ data block ready to transfer and no error encountered.	→	DPIOI1: Send_PIO_setup
2. Error encountered during command execution.	→	DPIOI3: Error_status

DPIOI1: Send_PIO_setup	Request transmission of a PIO Setup FIS to host.	
1. PIO Setup FIS transmitted.	→	DPIOI2: Transmit_data

DPIOI2: Transmit_data	Request transmission of a Data FIS to host.	
1. Data FIS transmitted, no more data transfer required for this command.	→	DI0: Device_idle
2. Data FIS transmitted, more data transfer required for this command, or 2048 Dwords transmitted.	→	DPIOI0: PIO_in

DPIOI3: Error_status	Request transmission of a Register - Device to Host FIS.	
1. FIS transmission complete.	→	DI0: Device_idle

DPIOI0: PIO_in State: This state is entered when the device receives a PIO data-in command or the transmission of one or more additional DRQ data blocks is required to complete the command.

When in this state, device shall prepare a DRQ data block for transfer to the host.

Transition DPIOI0:1: When the device has a DRQ data block ready to transfer and no error was encountered, the device shall transition to the DPIOI1: Send_PIO_setup state.

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Transition DPIOI0:2: When the device has encountered an error during command execution, the device shall transition to the DPIOI3: Error_status state.

DPIOI1: Send_PIO_setup: This state is entered when the device is ready to transmit a DRQ data block from the host.

When in this state, the device shall request that the Transport layer transmit a PIO Setup FIS. The initial status shall have BSY cleared to zero and DRQ set to one and with register content as described in the command description in the ATA/ATAPI-6 standard. The I bit shall be set. If this is the last DRQ data block requested by the command, the ending status shall have BSY cleared to zero and DRQ cleared to zero. If this is not the last data block requested by the command, the ending status shall have BSY set to one and DRQ cleared to zero.

Transition DPIOI1:1: When the PIO Setup FIS has been transferred, the device shall transition to the DPIOI2: Transmit_data state.

DPIOI2: Transmit_data: This state is entered when the device has transmitted a PIO Setup FIS to the host.

When in this state, the device shall request that the Transport layer transmit a Data FIS containing the DRQ data block.

Transition DPIOI2:1: When the Data FIS has been transferred and all data requested by this command have been transferred, the device shall transition to the DI0: Device_idle.

Transition DPIOI2:2: When the Data FIS has been transferred but all data requested by this command has not been transferred, or the 2048 Dword (8KB) transfer limit has been reached, then the device shall transition to the DPIOI0: PIO_in state.

DPIOI3: Error_status: This state is entered when the device has encountered an error that causes the command to abort before completing the transfer of the requested data.

When in this state, the device shall request that the Transport layer transmit a Register FIS with register content as described in the command description in the ATA/ATAPI-6 standard and the I bit set to one.

Transition DPIOI3:1: When the FIS has been transmitted, the device shall transition to the DI0: Device_idle state.

11.8 PIO data-out command protocol

This class includes:

- CFA WRITE MULTIPLE WITHOUT ERASE
- CFA WRITE SECTORS WITHOUT ERASE
- DOWNLOAD MICROCODE
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT
- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SMART WRITE LOG SECTOR
- WRITE BUFFER
- WRITE LOG EXT
- WRITE MULTIPLE
- WRITE MULTIPLE EXT
- WRITE SECTOR(S)
- WRITE SECTOR(S) EXT

Execution of this class of command includes the PIO transfer of one or more blocks of data from the host to the device.

DPIOO0: PIO_out	Prepare to receive DRQ data block transfer from the host.	
1. Ready to receive DRQ data block transfer.	→	DPIOO1: Send_PIO_setup
2. All DRQ data blocks received or command aborted due to error.	→	DPIOO3: Send_status

DPIOO1: Send_PIO_setup	Request transmission of a PIO Setup FIS to host.	
1. PIO Setup FIS transmitted.	→	DPIOO2: Receive_data

DPIOO2: Receive_data	Receive Data FIS from the Transport layer.	
1. Data FIS received.	→	DPIOO0: PIO_out

DPIOO3: Send_status	Request transmission of a Register - Device to Host FIS.	
1. FIS transmission complete.	→	DI0: Device_idle

DPIOI0: PIO_out State: This state is entered when the device receives a PIO data-out command or the receipt of one or more DRQ data blocks is required to complete this command.

When in this state, device shall prepare to receive a DRQ data block transfer from the host.

Transition DPIOO0:1: When the device is ready to receive a DRQ data block, the device shall transition to the DPIOO1: Send_PIO_setup state.

Transition DPIOO0:2: When the device has received all DRQ data blocks requested by this command or the device has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DPIOO3: Send_status state.

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DPIOO1: Send_PIO_setup: This state is entered when the device is ready to receive a DRQ data block from the host.

When in this state, the device shall request that the Transport layer transmit a PIO Setup FIS. The initial status shall have BSY cleared to zero and DRQ set to one. If this is the first DRQ data block for this command, the I bit shall be cleared to zero. If this is not the first DRQ data block for this command, the I bit shall be set to one. The ending status shall have BSY set to one and DRQ cleared to zero. The byte count for the DRQ data block shall be indicated.

Transition DPIOO1:1: When the PIO Setup FIS has been transferred, the device shall transition to the DPIOO2: Receive_data state.

DPIOO2:Receive_data: This state is entered when the device has transmitted a PIO Setup FIS to the host.

When in this state, the device shall receive the requested Data FIS from the Transport layer.

Transition DPIOO2:1: When the Data FIS has been received, the device shall transition to the DPIOO0: PIO_out state.

DPIOO3: Send_status: This state is entered when the device has received all DRQ data blocks requested by this command or the device has encountered an error that causes the command to abort before completing the transfer of the requested data.

When in this state, the device shall request that the Transport layer transmit a Register FIS with register content as described in the command description in the ATA/ATAPI-6 standard and the I bit set to one.

Transition DPIOO3:1: When the FIS has been transmitted, the device shall transition to the DI0: Device_idle state.

11.9 DMA data in command protocol

This class includes:

- READ DMA
- READ DMA EXT

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host using DMA transfer.

DDMAI0: DMA_in	Prepare data for the transfer of a Data FIS.		
	1. Data for Data FIS ready to transfer.	→	DDMAI1: Send_data
	2. Command completed or aborted due to error.	→	DDMAI2: Send_status

DDMAI1: Send_data	Request transmission of a Data FIS to host.		
	1. Data FIS transmitted. No more data transfer required for this command, or 2048 Dwords (8KB) transmitted.	→	DDMAI0: DMA_in

DDMAI2: Send_status	Request transmission of a Register FIS to host.	
1. Register FIS transmitted.	→	DI0: Device_idle

DDMAI0: DMA_in State: This state is entered when the device receives a DMA data-in command or the transmission of one or more data FIS is required to complete the command.

When in this state, device shall prepare the data for transfer of a data FIS to the host.

Transition DDMAI0:1: When the device has the data ready to transfer a data FIS, the device shall transition to the DDMAI1: Send_data state.

Transition DDMAI0:2: When the device has transferred all of the data requested by this command or has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DDMAI2: Send_status state.

DDMAI1: Send_data: This state is entered when the device has the data ready to transfer a data FIS to the host.

When in this state, the device shall request that the Transport layer transmit a data FIS containing the data. The device command layer shall request a Data FIS size of no more than 2048 Dwords (8KB).

Transition DDMAI1:1: When the data FIS has been transferred, the device shall transition to the DMAOI0: DMA_in state.

DDMAI2: Send_status: This state is entered when the device has transferred all of the data requested by the command or has encountered an error that causes the command to abort before completing the transfer of the requested data.

When in this state, the device shall request that the Transport layer transmit a Register FIS with register content as described in the command description in the ATA/ATAPI-6 standard and the I bit set to one.

Transition DDMAI2:1: When the FIS has been transmitted, the device shall transition to the DI0: Device_idle state.

11.10 DMA data out command protocol

This class includes:

- WRITE DMA
- WRITE DMA EXT

Execution of this class of command includes the transfer of one or more blocks of data from the host to the device using DMA transfer. A single interrupt is issued at the completion of the successful transfer of all data required by the command.

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DDMAO0: DMA_out	Prepare to receive a Data FIS from the host.	
1. Ready to receive Data FIS.	→	DDMAO1: Send_DMA_activate
2. All data requested for this command received or command aborted due to error.	→	DDMAO3: Send_status

DDMAO1: Send_DMA_activate	Request transmission of a DMA Activate FIS to host.	
1. DMA Activate FIS transmitted.	→	DDMAO2: Receive_data

DDMAO2: Receive_data	Receive Data FIS from the Transport layer.	
1. Data FIS received.	→	DDMAO0: DMA_out

DDMAO3: Send_status	Request transmission of a Register FIS to host.	
1. Register FIS transmitted.	→	DI0: Device_idle

DDMAO0: DMA_out State: This state is entered when the device receives a DMA data-out command or the receipt of one or more Data FIS is required to complete this command.

When in this state, device shall prepare to receive a Data FIS from the host.

Transition DDMAO0:1: When the device is ready to receive a Data FIS, the device shall transition to the DDMAO1: Send_DMA_activate state.

Transition DDMAO0:2: When the device has received all the data requested by this command or the device has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DDMAO3: Send_status state.

DDMAO1: Send_DMA_activate: This state is entered when the device is ready to receive a Data FIS from the host.

When in this state, the device shall request that the Transport layer transmit a DMA Activate FIS.

Transition DDMAO1:1: When the DMA Activate FIS has been transferred, the device shall transition to the DDMAO2: Receive_data state.

DDMAO2: Receive_data: This state is entered when the device transmitted a DMA Activate FIS to the host.

When in this state, the device shall receive the requested Data FIS from the Transport layer.

Transition DDMAO2:1: When the Data FIS has been received, the device shall transition to the DDMAO0: DMA_out state.

DDMAO3: Send_status: This state is entered when the device has received all the data requested by this command or the device has encountered an error that causes the command to abort before completing the transfer of the requested data.

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When in this state, the device shall request that the Transport layer transmit a Register FIS with register content as described in the command description in the ATA/ATAPI-6 standard and the I bit set to one.

Transition DDMAO3:1: When the FIS has been transmitted, the device shall transition to the DI0: Device_idle state.

11.11 PACKET protocol

This class includes:

- PACKET

States marked with an * are only utilized when queuing is implemented

DP0: PACKET	Request transmission of a PIO Setup FIS.	
1. FIS transmission complete.	→	DP1: Receive_command

DP1: Receive_command	Receive Data FIS containing command packet.	
1. FIS receiption complete.	→	DP2: Check_command

DP2: Check_command	Determine the protocol required for the received command.	
1. Non-data command.	→	DP3: PACKET_non-data
2. PIO data-in command.	→	DP4: PACKET_PIO_in
3. PIO data-out command.	→	DP6: PACKET_PIO_out
4. DMA data-in command	→	DP9: PACKET_DMA_in
5. DMA data-out command	→	DP11: PACKET_DMA_out

DP3: PACKET_non-data	Execute Non-data command.	
1. Command execution complete.	→	DP14: Send_status

DP4: PACKET_PIO_in	Prepare a DRQ data block for transfer to the host.	
1. DRQ data block ready to transfer.	→	DP4a: PIO_in_setup
2. Transfer complete or command aborted due to error.	→	DP14: Send_status
3. * DRQ block is not ready for immediate transfer	→	DP15: Release

DP4a: PIO_in_setup	Request transmission of a PIO Setup FIS to host.	
1. PIO Setup FIS transmitted.	→	DP5: Send_PIO_data

DP5: Send_PIO_data	Request transmission of a Data FIS to host.	
1. Data FIS transmitted.	→	DP4: PACKET_PIO_in

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DP6: PACKET_PIO_out	Prepare to receive DRQ data block from the host.		
	1. Ready to receive DRQ data block transfer.	→	DP7: PIO_out_setup
	2. All DRQ data blocks received or command aborted due to error.	→	DP14: Send_status
	3. * Not ready to accept DRQ block immediately.	→	DP15: Release

DP7: PIO_out_setup	Request transmission of a PIO Setup FIS to host.		
	1. PIO Setup FIS transmitted.	→	DP8: Receive_PIO_data

DP8: Receive_PIO_data	Receive Data FIS from the Transport layer.		
	1. Data FIS received.	→	DP6: PACKET_PIO_out

DP9: PACKET_DMA_in	Prepare data for the transfer of a Data FIS.		
	1. Data for Data FIS ready to transfer.	→	DP10: Send_DMA_data
	2. Command completed or aborted due to error.	→	DP14: Send_status
	3. * Data is not ready for immediate transfer.	→	DP15: Release

DP10: Send_DMA_data	Request transmission of a Data FIS to host.		
	1. Data FIS transmitted. No more data transfer required for this command, or 2048 Dwords (8KB) transmitted.	→	DP9: PACKET_DMA_IN

DP11: PACKET_DMA_out	Prepare to receive a Data FIS from the host.		
	1. Ready to receive Data FIS.	→	DP12: Send_DMA_activate
	2. All data requested for this command received or command aborted due to error.	→	DP14: Send_status
	3. * Not ready for immediate transfer.	→	DP15: Release

DP12: Send_DMA_activate	Request transmission of a DMA Activate FIS to host.		
	1. DMA Activate FIS transmitted.	→	DP13: Receive_DMA_data

DP13: Receive_DMA_data	Receive Data FIS from the Transport layer.		
	1. Data FIS received.	→	DP11: PACKET_DMA_out

DP14: Send_status	Request transmission of a Register FIS.		
	1. FIS transmission complete.	→	DI0: Device_idle

* DP15: Release	Request transmission of a Register FIS.		
	1. FIS transmission complete.	→	DI0: Device_idle

DP0: PACKET: This state is entered when the device receives a PACKET command.

When in this state, the device shall request that the Transport layer transmit a PIO Setup FIS to acquire the command packet associated with this command. The initial status shall have BSY

cleared to zero and DRQ set to one. The I bit shall be cleared to zero. The ending status shall have BSY set to one and DRQ cleared to zero. The byte count for the DRQ data block shall be indicated.

Transition DP0:1: When the PIO Setup FIS has been transferred, the device shall transition to the DP1: Receive_command state.

DP1: Receive_command: This state is entered when the device transmitted a PIO Setup FIS to the host to get the command packet.

When in this state, the device shall receive the requested Data FIS from the Transport layer.

Transition DP1:1: When the Data FIS has been received, the device shall transition to the DP2: Check_command state.

DP2: Check_command: This state is entered when the Data FIS containing the command packet has been received.

When in this state, the device shall determine the protocol for the command contained in the command packet.

Transition DP2:1: When the command is a non-data transfer command, the device shall transition to the DP3: PACKET_non-data state.

Transition DP2:2: When the command is a PIO data-in transfer command, the device shall transition to the DP4: PACKET_PIO_in state.

Transition DP2:3: When the command is a PIO data-out transfer command, the device shall transition to the DP6: PACKET_PIO_out state.

Transition DP2:4: When the command is a DMA data-in transfer command, the device shall transition to the DP9: PACKET_DMA_in state.

Transition DP2:5: When the command is a DMA data-out transfer command, the device shall transition to the DP11: PACKET_DMA_out state.

DP3: PACKET_non-data State: This state is entered when a received command is a non-data command.

When in this state, the device shall execute the requested command.

Transition DP3:1: When command execution completes, the device shall transition to the DP14: Send_status state.

DP4: PACKET_PIO_in State: This state is entered when the device receives a PIO data-in command or the transmission of one or more DRQ data blocks is required to complete the command.

When in this state, device shall prepare a DRQ data block for transfer to the host.

Transition DP4:1: When the device has a DRQ data block ready to transfer, the device shall transition to the DP4a: PIO_in_setup.

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Transition DP4:2: When all of the data requested by this command has been transferred or the device has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DP14: Send_status state.

*** Transition DP4:3:** When the device supports overlap and queuing and does not have a DRQ data block ready to transfer immediately, the device shall transition to the DP15: Release state.

DP4a: PIO_in_setup: This state is entered when the device is ready to transfer a DRQ block to the host.

When in this state, the device shall request that the Transport layer transmit a PIO Setup FIS. The initial status shall have BSY cleared to zero and DRQ set to one. The I bit shall be set to one. The ending status shall have BSY set to one and DRQ cleared to zero. The byte count for the DRQ data block shall be indicated.

Transition DP4a:1: When the PIO Setup FIS has been transferred, the device shall transition to the DP5:SendPIO_data state.

DP5:Send_PIO_data: This state is entered when the device is ready to transfer a DRQ data block to the host.

When in this state, the device shall request that the Transport layer transmit a Data FIS containing the DRQ data block.

Transition DP5:1: When the Data FIS has been transferred, the device shall transition to the DP4: PACKET_PIO_in state.

DP6: PACKET_PIO_out State: This state is entered when the device receives a PIO data-out command or the receipt of one or more DRQ data blocks is required to complete the command.

When in this state, device shall prepare to receive a DRQ data block transfer from the host.

Transition DP6:1: When the device is ready to receive a DRQ data block transfer, the device shall transition to the DP7: PIO_out_setup state.

Transition DP6:2: When the device has received all DRQ data blocks requested by this command or the device has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DP14: Send_status state.

*** Transition DP6:3:** When the device supports overlap and queuing and can not accept a DRQ data block immediately, the device shall transition to the DP15: Release state.

DP7: PIO_out_setup: This state is entered when the device is ready to receive a DRQ data block from the host.

When in this state, the device shall request that the Transport layer transmit a PIO Setup FIS. The initial status shall have BSY cleared to zero and DRQ set to one. The I bit shall be set to one. The ending status shall have BSY set to one and DRQ cleared to zero. The byte count for the DRQ data block shall be indicated.

Transition DP7:1: When the PIO Setup FIS has been transferred, the device shall transition to the DP8: Receive_PIO_data state.

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DP8: Receive_PIO_data: This state is entered when the device transmitted a PIO Setup FIS to the host.

When in this state, the device shall receive the requested Data FIS from the Transport layer.

Transition DP8:1: When the Data FIS has been received, the device shall transition to the DP6: PACKET_PIO_out state.

DP9: PACKET_DMA_in State: This state is entered when the device receives a DMA data-in command or the transmission of one or more Data FIS is required to complete the command.

When in this state, device shall prepare the data for transfer of a Data FIS to the host.

Transition DP9:1: When the device has the data ready to transfer a Data FIS, the device shall transition to the DP10: Send_DMA_data state.

Transition DP9:2: When the device has transferred all of the data requested by this command or has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DP14: Send_status state.

*** Transition DP9:3:** When the device supports overlap and queuing and does not have data ready to transfer immediately, the device shall transition to the DP15: Release state.

DP10: Send_DMA_data: This state is entered when the device has the data ready to transfer a Data FIS to the host.

When in this state, the device shall request that the Transport layer transmit a Data FIS containing the data.

Transition DP10:1: When the Data FIS has been transferred, the device shall transition to the DP9: PACKET_DMA_in state. The device command layer shall request a data FIS size of no more than 2048 Dwords (8KB).

DP11: PACKET_DMA_out State: This state is entered when the device receives a DMA data-out command or the receipt of one or more Data FIS is required to complete the command.

When in this state, device shall prepare to receive a Data FIS from the host.

Transition DP11:1: When the device is ready to receive a Data FIS, the device shall transition to the DP12: Send_DMA_activate state.

Transition DP11:2: When the device has received all the data requested by this command or the device has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DP14: Send_status state.

*** Transition DP11:3:** When the device supports overlap and queuing and can not accept a Data FIS immediately, the device shall transition to the DP15: Release state.

DP12: Send_DMA_activate: This state is entered when the device is ready to receive a Data FIS from the host.

When in this state, the device shall request that the Transport layer transmit a DMA Activate FIS.

Transition DP12:1: When the DMA Activate FIS has been transferred, the device shall transition to the DP13: Receive_DMA_data state.

DP13: Receive_DMA_data: This state is entered when the device transmitted a DMA Activate FIS to the host.

When in this state, the device shall receive the requested Data FIS from the Transport layer.

Transition DP13:1: When the Data FIS has been received, the device shall transition to the DP11: PACKET_DMA_out state.

DP14: Send_status: This state is entered when the device has received all the data requested by this command or the device has encountered an error that causes the command to abort before completing the transfer of the requested data.

When in this state, the device shall request that the Transport layer transmit a Register FIS with register content as described in the command description in the ATA/ATAPI-6 standard and the I bit set to one.

Transition DP14:1: When the FIS has been transmitted, then the device shall transition to the DI0: Device_idle state.

*** DP15: Release:** This state is entered when the device is not able to do a data transfer immediately.

When in this state, the device shall request that the Transport layer transmit a Register FIS with register content as described in the command description in the ATA/ATAPI-6 standard, with the REL bit set to one, and, if the bus release interrupt has been enabled by a previous Set Features Command, with the I bit set to one.

Transition DP15:1: When the FIS has been transmitted, then the device shall transition to the DI0: Device_idle state.

11.12 READ DMA QUEUED command protocol

This class includes:

- READ DMA QUEUED
- READ DMA QUEUED EXT

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host using DMA transfer. All data for the command may be transferred without a bus release between the command receipt and the data transfer. This command may bus release before transferring data. The host shall initialize the DMA controller prior to transferring data. When data transfer is begun, all data for the request shall be transferred without a bus release.

DDMAQI0: DMA_queued_in	Determine whether to transfer or release.	
1. Data for Data FIS ready to transfer.	→	DDMAQI1: Send_data
2. Command aborted due to error.	→	DDMAQI3: Send_status
3. Bus release	→	DDMAQI4: Release

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DDMAQI1: Send_data	Request transmission of a Data FIS to host.	
1. Data FIS transmitted. No more data transfer required for this command, or 2048 Dwords (8KB) transmitted.	→	DDMAQI2: Prepare_data

DDMAQI2: Prepare_data	Prepare data for the next Data FIS.	
1. Data ready.	→	DDMAQI1: Send _data
2. Command complete or aborted due to error.	→	DDMAQI3: Send_status

DDMAQI3: Send_status	Request transmission of a Register FIS to host.	
1. Register FIS transmitted.	→	DI0: Device_idle

DDMAQI4: Release	Request transmission of a Register FIS to host.	
1. Register FIS transmitted.	→	DI0: Device_idle

DDMAQI0: DMA_queued_in State: This state is entered when the device receives a READ DMA QUEUED command.

When in this state, device shall determine if the requested data is ready to transfer to the host.

Transition DDMAQI0:1: When the device has the requested data ready to transfer a Data FIS immediately, the device shall transition to the DDMAQI1: Send_data state.

Transition DDMAQI0:2: When the device has encountered an error that causes the command to abort before completing the transfer of the requested data, the device shall transition to the DDMAQI3: Send_status state.

Transition DDMAQI0:3: When the device does not have the requested data ready to transfer a Data FIS immediately, the device shall transition to the DDMAQI4: Release state.

DDMAQI1: Send_data: This state is entered when the device has the data ready to transfer a Data FIS to the host.

When in this state, the device shall request that the Transport layer transmit a Data FIS containing the data.

Transition DDMAQI1:1: When the Data FIS has been transferred, the device shall transition to the DDMAQI2: Prepare_data state. The device command layer shall request a Data FIS size of no more than 2048 Dwords (8KB).

DDMAQI2: Prepare_data: This state is entered when the device has completed the transfer a Data FIS to the host.

When in this state, the device shall prepare the data for the next Data FIS.

Transition DDMAQI2:1: When data is ready for the Data FIS, the device shall transition to the DDMAQI1: Send_data state.

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