

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DELTA ELECTRONICS, INC.,
Petitioner,

v.

VICOR CORPORATION,
Patent Owner.

Case No. IPR2024-00227

U.S. PATENT NO. 9,516,761

PETITION FOR *INTER PARTES* REVIEW

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Exhibit No.	Description
1001	United States Patent No. 9,516,761 (“’761 Patent”)
1002	Declaration of Dr. Steven B. Leeb
1003	<i>Curriculum Vitae</i> of Dr. Steven B. Leeb
1004	File History of U.S. Patent No. 9,516,761
1005	U.S. No. 8,966,747
1006	Declaration of Dr. Sylvia Hall-Ellis
1007	Ericsson BMR 453 series DC/DC converters Technical Specification (July 2010), <i>available at</i> https://web.archive.org/web/20101108165728/http://archive.ericsson.net/service/internet/picov/get?DocNo=28701-EN/LZT146395&Lang=EN&HighestFree=Y . (“Ericsson-BMR”)
1008	Robert W. Erickson and Dragan Maksimovic, <i>Fundamentals of Power Electronics</i> (2d ed. 2001). (“ <i>Fundamentals</i> ”)
1009	U.S. Patent 6,965,517 (“Wanes”)
1010	U.S. Patent 6,970,367 (“Takeshima”)
1011	G. Spiazzi, L. Rossetto, P. Mattavelli, P. Cova, and N. Delmonte, <i>Layout Considerations and Thermal Analysis of a 1.8 MHz Resonant VRM</i> , 2007 IEEE Industry Applications Annual Meeting, 1993 (2007). (“Spiazzi”)
1012	Laszlo Huber, Kevin Hsu, Milan M. Jovanovi, Dennis Solley, Gennady Gurov and Robert J. Porter, <i>1.8-MHz, 48-V Resonant VRM: Analysis, Design, and Performance Evaluation</i> , 21 IEEE Transactions on Power Electronics 79 (2006)
1013	Excerpts of Complainant Vicor Corporation’s Second Supplemental Objections And Responses To Respondents’ First Set Of Joint Interrogatories (Nos. 1-20)

1014	Picture of Ericsson BMR 453 series DC/DC converter, https://web.archive.org/web/20120131104718/http://www.ericsson.com/solutions/news/powermodules/2009/hires_BMR453_jan09.jpg .
1015	U.S. Patent No. 7,403,397
1016	Laszlo Balogh, Design Review: 140W, Multiple Output High Density DC/DC Converter, (1997), <i>available at</i> https://web.archive.org/web/20050129014555/http://focus.ti.com:80/lit/ml/slup117/slup117.pdf .
1017	J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, <i>Principles of Power Electronics</i> (1st ed. 1991) (<i>physical copy available upon request, select excerpts filed electronically</i>)
1018	<u>Power Modules: Digital DC/DC converter family integrates PMBus connectivity</u> (2009), <i>available at</i> https://web.archive.org/web/20090902060840/http://www.ericsson.com:80/technology/docs/article_PowerModules_digital_dc-dc.pdf
1019	U.S. Patent 6,466,454
1020	U.S. Patent 8,749,990
1021	Declaration of Nathaniel E. Frank-White authenticating Exhibits 1007, 1014, and 1018
1022	Declaration of Nathaniel E. Frank-White authenticating Exhibit 1016
1023	U.S. Patent Application No. 2011/0057713
1024	U.S. Patent 6,724,631
1025	Claim Chart for the Infringement of Independent Claim 1 and Dependent Claims 2, 3, 4, 5, 6, 7 of Complainant Vicor Corporation's United States Patent 9,516,761 by Delta U50SU4P162 High Power Density 48V / 12V Bi-Directional DC-DC Converter Power Module and Computing Systems Containing the Same (<i>filed under seal</i>)
1026	Ericsson BMR 453 series DC/DC converters Technical Specification (September 2008) ("BMR-2008")

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1027	Vishay Siliconix N-Channel 75 V (D-S) MOSFET SiE818DF Technical Specification (July 13, 2009), <i>available at</i> https://www.digikey.com/en/products/detail/vishay-siliconix/SIE818DF-T1-E3/1656715
1028	March 25, 2014 Claim Amendment in prosecution of U.S. Patent No. 8,966,747 (divisional of '761 patent)
1029	TDK Data Sheet: FReta iQD Series – Single Output Quarter Brick Bus Converter, <i>available at</i> https://www.datasheetarchive.com/datasheet?id=0c23ebb9024bd4c7b5c5d7b96a5c82316b8b34&type=M&term=iqd48025a120v007
1030	Vishay Siliconix N-Channel 40-V (D-S) MOSFET Si7884DP (Sept. 8, 2008), <i>available at</i> https://www.vishay.com/docs/68395/si7884bd.pdf .
1031	Declaration of Henrik Borgengren

I. INTRODUCTION

The '761 Patent relates to power converters, but the '761 Patent does not purport to invent a new type of power converter or component thereof, nor does it purport to invent a new type of circuit to convert power. Instead, the purported innovation of the '761 Patent is the purely functional result that the power dissipated on the top and bottom sides of the power converter's printed circuit board (PCB) are roughly the same (specifically, within 150% of each other).

This functional result was the natural outcome, however, of a conventional layout of power converter electrical components on a PCB, in particular a layout that was symmetrical on top and bottom. Prior art power converters were routinely made with symmetric layouts on the top and bottom of their PCBs. *See, e.g.*, EX1007 at 1, 24; EX1009 at Fig. 9A-B; EX1010 at Fig. 2; EX1011 at Fig. 5; EX1019 at Fig. 14; EX1024 at Fig. 4 (various prior art references each depicting symmetrical layouts). This symmetrical layout was known to be useful (and, as a result, routinely used) for a number of reasons, including enhanced durability. *See, e.g.*, EX1023 ¶¶51-52. As makes intuitive sense and as a person of ordinary skill in the art ("POSITA") would have recognized, if the same electrical components are used in the same way and symmetrically laid out on the top and bottom of a PCB, then the results are going to be the same (or at least very close to the same) on the top and bottom.

The '761 Patent applicant did not, however, disclose any of these symmetry-teaching references during prosecution. *See generally* EX1004. As explained in detail below, these prior art references would all have naturally and obviously achieved the purportedly innovative result of the '761 Patent during their normal operation. Accordingly, Petitioner respectfully requests that *inter partes* review of the '761 Patent be instituted and that all of its claims be cancelled.

II. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

A. 37 C.F.R. §42.104(b)(1): Claims for Which IPR Is Requested

Petitioner challenges the patentability of claims 1-7 (the “Challenged Claims”) of U.S. patent no. 9,516,761 (EX1001, “the '761 Patent”).

B. 37 C.F.R. §42.104(b)(2): Grounds for Challenge

The '761 Patent purports to be subject to pre-AIA law. The challenge presented herein is based on the following references, none of which were before the Examiner during prosecution:

- **Ericsson-BMR (EX1007):** Ericsson-BMR is a technical specification from Ericsson for the BMR 453 series DC/DC converter, published in July 2010. *See* EX1021. Accordingly, Ericsson-BMR qualifies as prior art under at least 35 U.S.C. § 102(a).
- **BMR-2008 (EX1026):** BMR-2008 is a technical specification from Ericsson for the BMR 453 series DC/DC converter, published in September 2008. *See* EX1026. Accordingly, Ericsson-BMR qualifies as prior art under at least 35 U.S.C. § 102(b).
- **Wanes (EX1009):** Wanes is a U.S. patent issued on November 15, 2005. Accordingly, Wanes qualifies as prior art under at least 35 U.S.C. § 102(b).

- **Takeshima (EX1010):** Takeshima is a U.S. patent issued on November 29, 2005. Accordingly, Takeshima qualifies as prior art under at least 35 U.S.C. § 102(b).
- **Spiazzi (EX1011):** Spiazzi is a conference paper from the 2007 IEEE Industry Applications Annual Meeting that was published by at least 2007. EX1011, 1993; EX1006 ¶¶64-68. Accordingly, Spiazzi qualifies as prior art under at least 35 U.S.C. § 102(b).

Petitioner requests cancellation of the Challenged Claims on the following grounds:

Ground	Statutory Basis	Claims	Prior Art
I	§ 103	1-5, 7	Obvious by Ericsson-BMR or, alternatively, BMR-2008
II	§ 103	1-5, 7	Obvious by Ericsson-BMR in view of Spiazzi, or, alternatively, by BMR-2008 in view of Spiazzi
III	§ 103	1-7	Obvious by Ericsson-BMR in view of Wanes, or, alternatively, by BMR-2008 in view of Wanes
IV	§ 103	1-7	Obvious by Takeshima
V	§ 103	1-7	Obvious by Takeshima in view of Spiazzi
VI	§ 103	1-7	Obvious by Takeshima in view of Wanes
VII	§ 103	1-7	Obvious by Ericsson-BMR in view of Takeshima, or, alternatively, by BMR-2008 in view of Takeshima
VIII	§ 103	1-7	Obvious by Spiazzi in view of Wanes

C. 37 C.F.R. § 42.104(b)(3): Claim Construction

Only for purposes of this Petition, Petitioner applies Patent Owner's apparent understanding of the terms as reflected in its infringement contentions, to the extent

that Petitioner can understand Patent Owner's deficient and opaque contentions. *See* EX1025.¹

D. 37 C.F.R. § 42.104(b)(4): How the Claims Are Unpatentable

A detailed explanation of how the Challenged Claims are unpatentable is provided below.

E. 37 C.F.R. § 42.104(b)(5): Evidence Supporting Challenge

A list of exhibits is provided at the beginning of this Petition.

III. OVERVIEW OF THE '761 PATENT

A. Priority Date

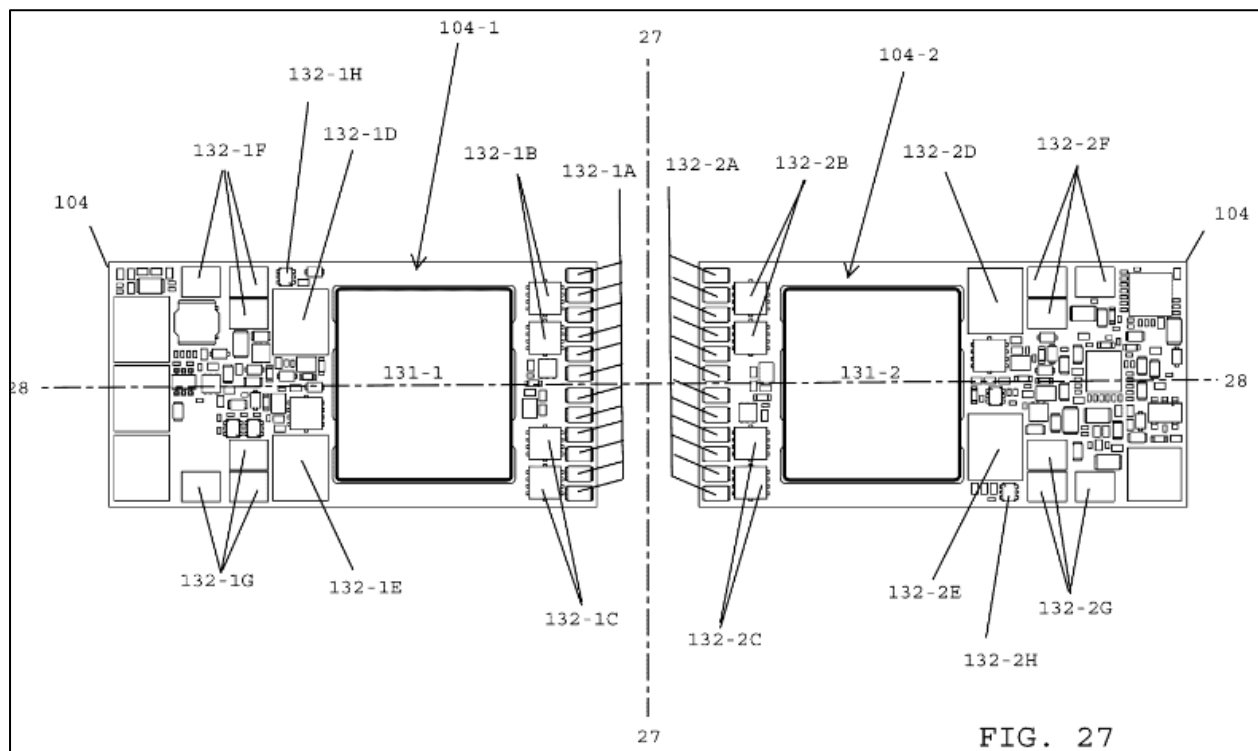
The '761 Patent claims priority on its face to May 11, 2011, but Patent Owner has contended the '761 Patent was conceived in April 2010. The obviousness analysis presented herein would not change regardless of which priority date applies, although Petitioner contends that the '761 Patent is not entitled to a priority date any earlier than May 11, 2011.

B. Purported Invention

The '761 Patent relates to the layout, packaging, and manufacture of power converters and power modules. *See* EX1001 at 1:16-20; EX1013 at 79. Power

¹ Petitioner does not admit that Patent Owner's apparent constructions are correct or that the claims are not indefinite.

converters are a type of electronic assembly that can be used to convert power from one level to another, for example converting higher-voltage power available from the outlet of a home into lower-voltage power used by a laptop inside the home. The essence of the purported invention of the '761 Patent is captured by the following quote from the specification of the '761 Patent, presented below alongside Figure 27 for ease of reference:



Symmetrical Power Dissipation Between PCB Surfaces

The components may be arranged between the PCB surfaces according to heat dissipated during operation. For example, the heat dissipative components may be arranged in a manner that distributes the heat evenly between the two PCB surfaces allowing heat produced by power

dissipating devices to be extracted from both surfaces of the PCB improving the thermal performance. This type of heat dissipation symmetry is also factored into the component layout shown in the power converter of FIG. 27. For example, two input cells each using the same basic circuit topology are shown, one above and another below axis 28. ... To ensure heat dissipation symmetry between the two surfaces, the cells may be arranged in mirror image layouts as shown. ... In some examples, the FETs are arranged such that during operation, the power FETs on the top surface dissipate power at a level that is comparable to the level of power dissipated by the power FETs on the bottom surface. Also, the level of power dissipated by the power FETs in the upper input cell is comparable to the level of power dissipated by the power FETs in the lower input cell. For example, the level of power dissipated by the power FETs on one surface is less than 150% of the level of power dissipated by the power FETs on the other surface. The level of power dissipated by the power FETs in the upper cell is less than 150% of the level of power dissipated by the power FETs in the lower cell, and vice versa.

See EX1001 at 24:45-25:24.

C. Prosecution History

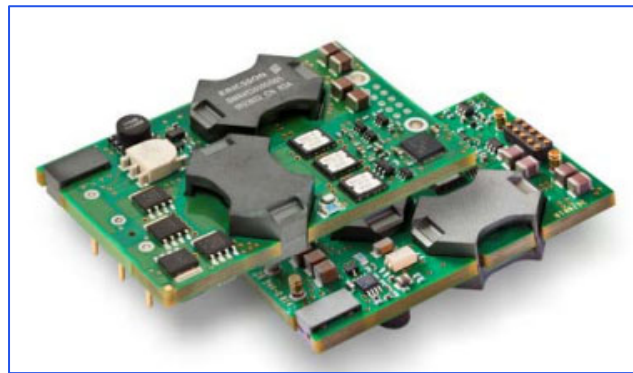
During prosecution, there was no substantive discussion by the applicant or Examiner of any prior art, the meaning of any claim terms, or reasons for allowance.

See generally EX1004. The prosecution of the '761 Patent did not address any of the prior art relied upon in this Petition.

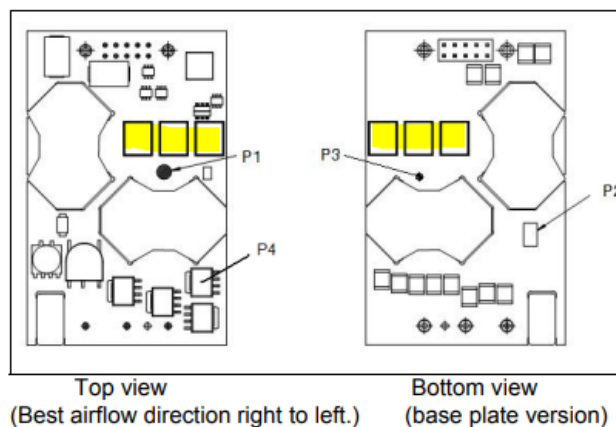
IV. SUMMARY OF THE PRIOR ART

A. Ericsson-BMR (EX1007) And BMR-2008 (EX1026)

Ericsson-BMR is a technical specification related to a product previously sold by Ericsson for its BMR 453 series DC/DC power converter, pictured here (top and bottom sides):



See EX1007 at 1. Ericsson-BMR taught that certain of its power semiconductor devices are symmetrically disposed overlapping each other on top and bottom, as highlighted here:

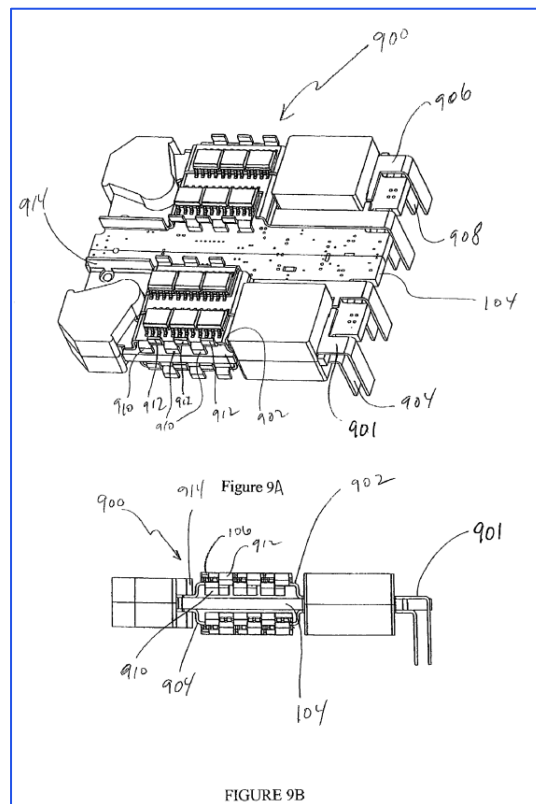


See EX1007 at 24 (annotated). Ericsson-BMR is analogous art to the '761 Patent, including because the Ericsson-BMR module is a power converter and is thus in the same field of endeavor. See EX1002 ¶¶32-33.

BMR-2008 is a technical specification that is substantially similar in relevant respect to Ericsson-BMR, and is therefore relevant and analogous art for the same reasons as Ericsson-BMR. Compare EX1026, with EX1007; EX1002 ¶34.

B. Wanes (EX1009)

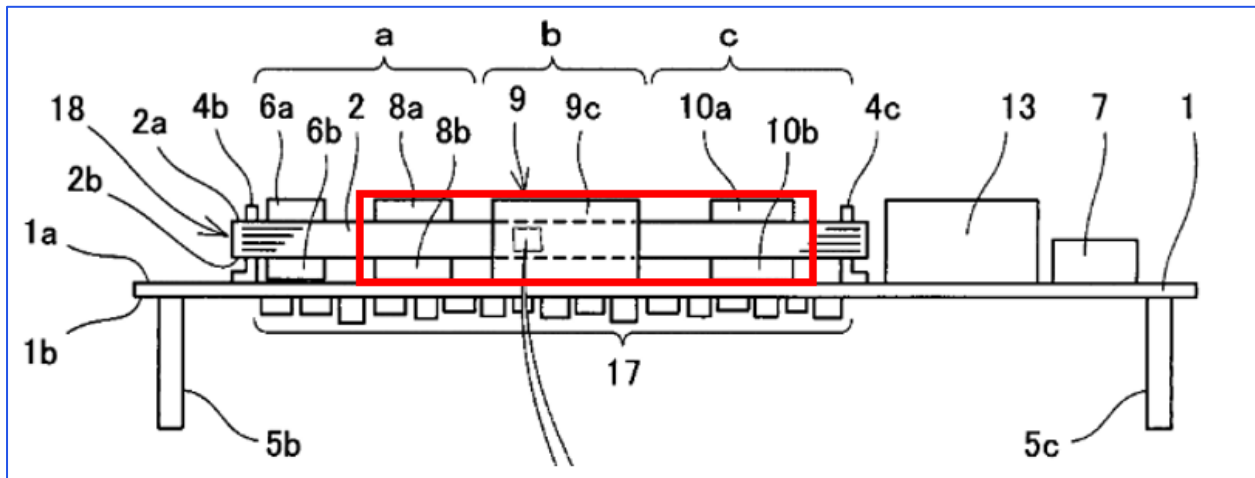
Wanes is a U.S. patent claiming eight years of priority over the '761 Patent. See EX1009 at Cover Page. As shown in Wanes, it was well-known to a POSITA to symmetrically dispose and mirror cells of electrical components:



See EX1009 at Figs. 9A-B. Wanes is analogous art to the '761 Patent, including because the Wanes module is a power converter and is thus in the same field of endeavor. See EX1002 ¶¶35-36.

C. Takeshima (EX1010)

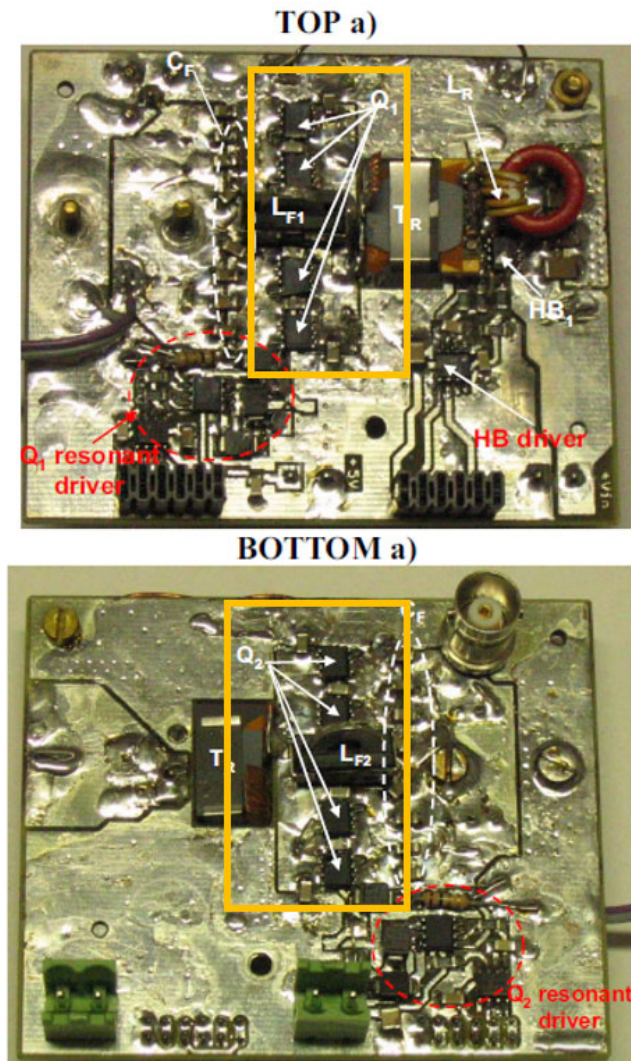
Takeshima is a U.S. patent claiming seven years of priority over the '761 Patent. See EX1010 at Cover Page. Like Wanes and Ericsson-BMR, Takeshima also demonstrates that it was well known in the art to symmetrically dispose overlapping power semiconductor devices on the top and bottom of PCBs, as outlined in red below in this cropped version of Takeshima's Figure 2:



EX1010, Fig. 2 (cropped and annotated). Takeshima is analogous art to the '761 Patent, including because the Takeshima module is a power converter and is thus in the same field of endeavor. See EX1002 ¶¶37-38.

D. Spiazzi (EX1011)

Spiazzi is a 2007 conference paper. *See* EX1011 at 1993. Like Ericsson-BMR, Wanes, and Takeshima, Spiazzi also demonstrates that it was well known to a POSITA to symmetrically lay out overlapping MOSFETs (power semiconductor devices) on the top and bottom of a PCB, as shown (for example) by the layout of top-side MOSFETS Q1 relative to the bottom-side MOSFETs Q2, highlighted here within the orange box:



See EX1011 at Fig. 5 (cropped, annotated with orange box, other annotations in original). Spiazzi is analogous art to the '761 Patent, including because the Spiazzi module is a power converter and is thus in the same field of endeavor. See EX1002 ¶¶39-40.

Spiazzi and the other references discussed above are also analogous art because they are relevant to the particular problem faced by the alleged inventors of the '761 Patent, including addressing power dissipation. See EX1002 ¶¶41-42.

V. LEVEL OF ORDINARY SKILL

A POSITA at the time of the '761 Patent (whether that date is May 11, 2011 or April 2010) would have at least a Master's degree in electrical engineering and two or more years of work experience relating to power electronics and the manufacture of power converters or printed circuit board design for power converters. Additional education might compensate for less work experience, and vice-versa. See EX1013 at 79.

VI. GROUNDS

A. Ground I: Claims 1-5 And 7 Are Rendered Obvious By Ericsson-BMR Or, Alternatively, By BMR-2008

1. Claim 1

Ericsson-BMR renders obvious Claim 1. See EX1002 ¶46.

a. 1/[preamble]²

Ericsson-BMR teaches the preamble. *See* EX1002 ¶¶47-48. The Ericsson-BMR apparatus can be seen, for example, on the first page of the document (showing the top and bottom sides of the apparatus):



See EX1007 at 1.

b. 1/[a]

Ericsson teaches this element. *See* EX1007 at, *e.g.*, 1 (“DC/DC *converters*”)³; EX1002 ¶¶49-50. For example, as shown in this cropped and highlighted portion of page 2, the Ericsson-BMR module has an input of 36-75 volts, and in various embodiments has an output of 3.3, 5, 9, or 12 volts:

² *See* the Claim Listing at the end of this Petition for corresponding claim language of each claim element.

³ All emphasis in the Petition is added unless indicated otherwise.

BMR 453 series DC/DC converters, Input 36-75 V, Output up to 60 A / 396 W	
Ordering Information Product Program	General Information Reliability The Mean Time full output power (T _A) of +40°C, w and Communica methods could b and failure rate v Ericsson Power Predicted MTBF
Product program	Output
BMR4530002/003	3.3 V / 60 A, 198 W
BMR4530002/004	5 V / 60 A, 300 W
BMR4530000/002	9 V / 33 A, 297 W
BMR4530000/001	12 V / 33 A, 396 W

See EX1007 at 2 (highlighted).

c. 1/b/

Ericsson-BMR teaches and renders obvious this element. See EX1002 ¶¶51-54.

Ericsson-BMR teaches a PCB that has a top surface and a bottom surface. See EX1002 ¶52. Ericsson-BMR states that it is implemented using a PCB. See EX1007 at 21 (“The sense traces should be located close to the **PCB** ground layer . . .”). Ericsson-BMR’s PCB is depicted, for example, as the green printed circuit board shown below, which is green on both the top surface and bottom surfaces seen here:

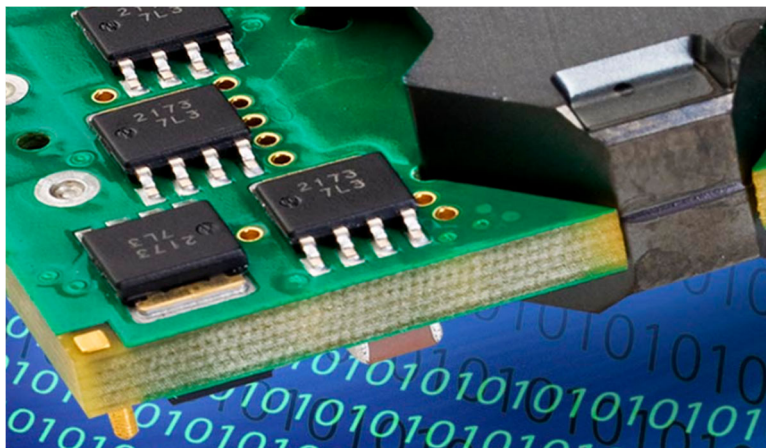


See EX1007 at 1.

As a POSITA would have recognized, Ericsson-BMR's PCB is comprised of a plurality of conductive layers. See EX1002 ¶¶53-54. The top and bottom layers are a plurality of conductive layers, and the picture above shows a series of gold striations between those top and bottom layers which a POSITA would have expected, or at least have obviously expected, correspond to an additional plurality of conductive layers:



See EX1007 at 1 (zoomed). A clearer view of this additional plurality of layers can be seen in additional documentation regarding the Ericsson-BMR module:



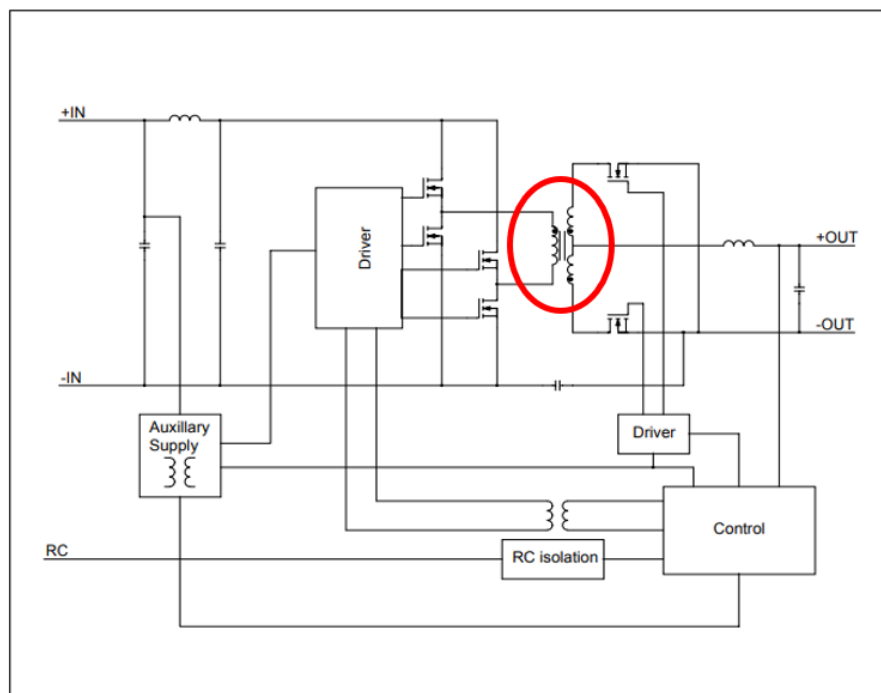
See EX1014.

Ericsson-BMR also teaches that the “sense traces should be located close to the **PCB ground layer**,” because there are a plurality of conductive “layer[s]” in the PCB and certain components (such as the sense traces) should be located on the specific “layer” corresponding to the “ground layer” as opposed to another conductive “layer” in the PCB. See EX1007 at 21.

d. I/c

Ericsson-BMR teaches and renders obvious this element. See EX1002 ¶¶55-59.

As background, Ericsson-BMR teaches that its module employs the following fundamental circuit topology, where the transformer of the circuit has been circled in red:

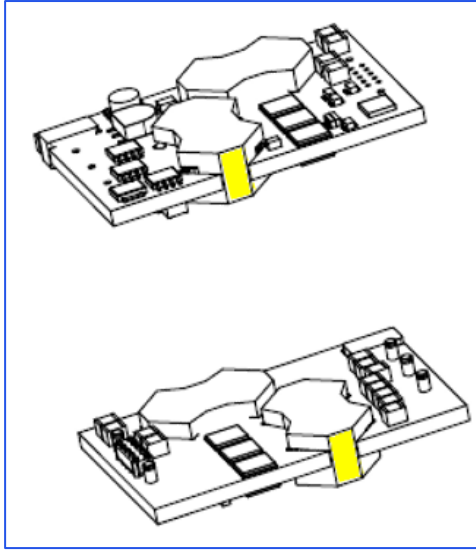


See EX1007 at 5. As a POSITA would have recognized, the transformer symbol indicates the use of magnetic material with windings that transform (or convert) the input power to an output power. See EX1002 ¶56; EX1008 at Fig. 1.5. Thus, a POSITA would have expected that Ericsson-BMR's apparatus includes a magnetic core structure, and those are indeed found in the apparatus as the larger, dark grey components, one of which is circled here in red:



A POSITA would recognize these black structures as magnetic cores because they are a common shape for these types of magnetic core components. See EX1002 ¶56; *see also, e.g.*, EX1020 at Fig. 1A, 3:12-21 (planar magnetic of same shape).

A POSITA would have further recognized, or at least would have found obvious, that the transformer's magnetically coupled windings are formed by traces in one or more of the conductive layers in the PCB, including because, as shown here where highlighted, the magnetic cores extend through the PCB such that there is no other place for the windings to be other than as traces in one or more of the PCB layers:



See EX1007 at 31 (annotated); EX1002 ¶57. This understanding of a POSITA is confirmed by higher resolution photos of the Ericsson-BMR unit from the time, which also show the magnetic core extending all the way to the surface of the PCB and through it, such that there is no other place for the magnetically coupled windings to be located other than as traces in the PCB layers:



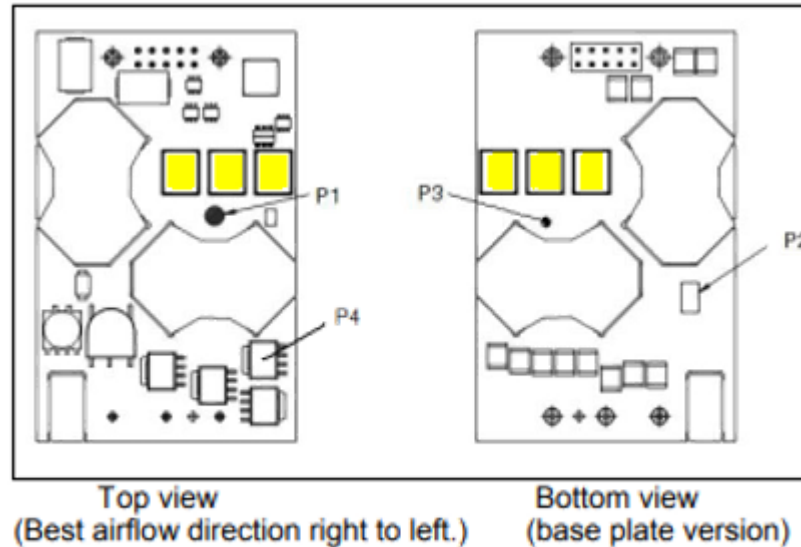
See EX1014 (annotated); *see also* EX1018 at 6 (same disclosure). As a POSITA would have been aware, this was the standard way to apply planar magnetics such as those shown above in the Ericsson-BMR module. *See, e.g.*, EX1020 at 3:13-16 (“In general, to apply the planar magnetics technology (called ‘*ferrite core on board*’) requires many layers of thick (‘heavy’ in the circuit board industry) copper clad to construct the powertrain, *including the transformer windings*.”); EX1002 ¶58.

At a minimum, it would have been obvious to a POSITA for the windings to have been formed by traces in one or more of the conductive layers in the PCB, including because (as discussed above) there is no other place in the Ericsson-BMR module for the windings to be, and because placing traces in the conductive layers in the PCB for the windings was well-known in the art as a useful way to economize on space. *See, e.g.*, EX1019 at 1:54-60 (patent from 1999, more than a decade before the ’761 Patent: “The windings of the magnetic elements ... are incorporated in the multilayer PCB.... In this way the footprint of the magnetic elements is reduced to the footprint of the transformer core.”); EX1020 at 3:13-16; EX1002 ¶59.

e. 1/d]

Ericsson-BMR teaches and renders obvious this element. *See* EX1002 ¶¶60-74. As Dr. Leeb explains, through analysis of the power converter circuit and layout, visual inspection, and additional documentary evidence, a POSITA would have

known or at least found obvious the squares highlighted here in yellow correspond to power semiconductor devices mounted on the top surface and bottom surface:

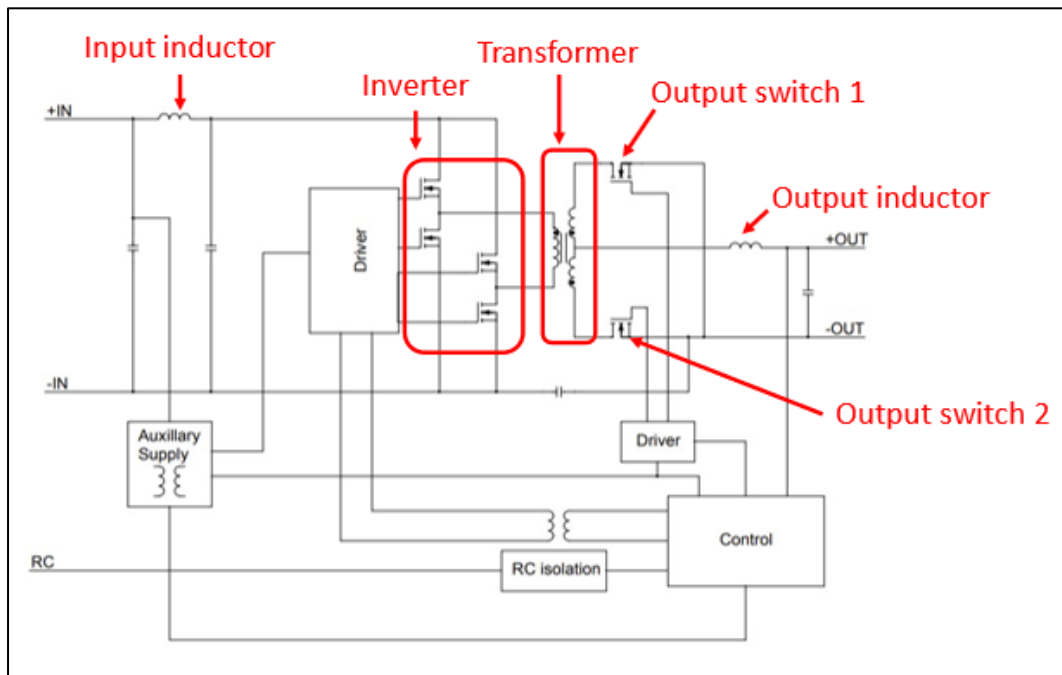


which correspond (on the top surface) to the power semiconductor devices circled here in red:

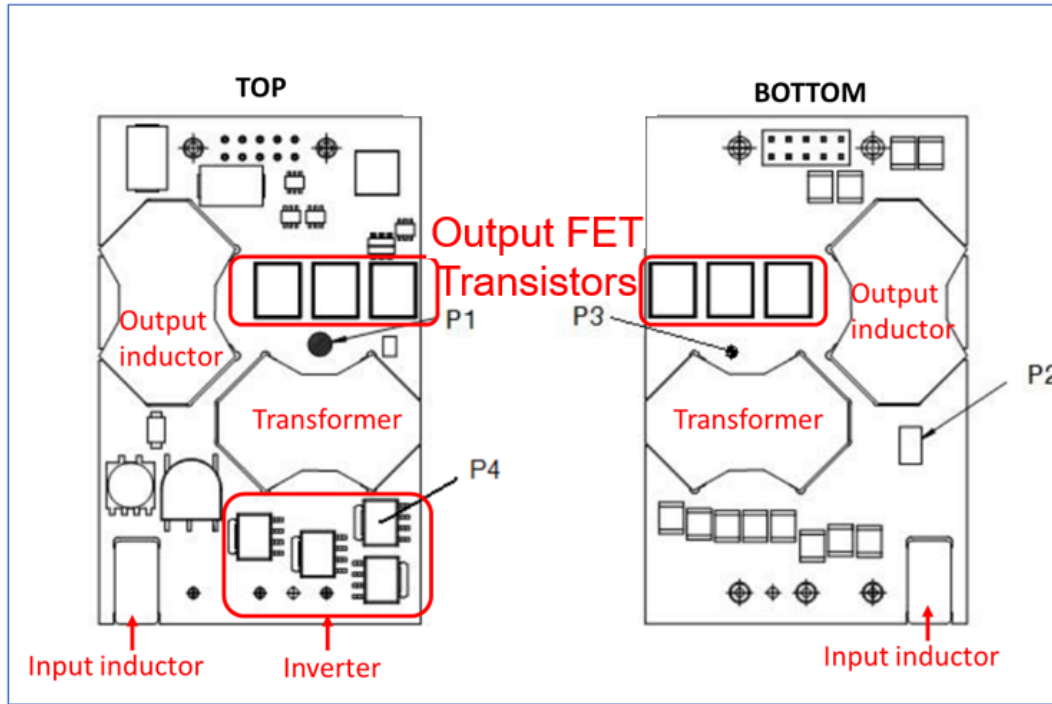


See EX1007 at 1, 24 (annotated); EX1002 ¶¶60-74.

A POSITA would have found known and found obvious that these were power semiconductor devices for at least the following reasons. As background, Ericsson-BMR teaches the use of two output switches, as shown here in red in an annotated version of Ericsson-BMR’s “fundamental circuit diagram” that is a functional representation of the components on the PCB:



See EX1007 at 5 (annotated); EX1002 ¶62. As Dr. Leeb explains, an analysis of the teachings of the Ericsson-BMR document and a POSITA’s visual recognition of certain components (such as the hallmark shape of the output inductor planar magnetics) would allow a POSITA to map the components in the fundamental circuit diagram to the real-world components on the Ericsson-BMR module as follows:



See EX1007 at 24 (annotated); EX1002 ¶¶63-65. As Dr. Leeb explains, three of the six output FET transistors correspond to one of the output switches, while the other three correspond to the second of the output switches. See EX1002 ¶¶63, 74.

These output FETs are power semiconductor devices, are comprised of transistors (the T in FET is “transistor”), use semiconductors, and are used in this power converter module. See EX1002 ¶65. And as shown in the fundamental circuit diagram above, these power semiconductor devices are electrically connected. They would also dissipate some amount of power at a particular level (P_t in the parlance of the '761 Patent for the top three power semiconductor devices, P_b for the bottom three power semiconductor devices) during operation of the power converter. See EX1002 ¶¶63, 74; EX1008 at 2-3.

f. 1[e]

Ericsson-BMR teaches and renders obvious this element. *See* EX1002 ¶¶75-82.

As discussed in the previous element, there are three relevant power semiconductor devices on both the top and bottom of the PCB, which would dissipate power during operation of the power converter. A POSITA would have known, or at least found obvious, that the current and voltage (and thus, power) through the top three power semiconductor devices would be equal (or at least approximately equal) over time to the bottom three power semiconductor devices, for the following reason. *See* EX1002 ¶76.

As background, the circuit employed by Ericsson-BMR (pictured above on page 5 of Ericsson-BMR) is a type of “full-bridge” circuit, as a POSITA would have known. *See* EX1002 ¶77; EX1008 at Fig. 6.18. As Dr. Leeb explains in his accompanying declaration, a POSITA would have known, and found it obvious, to power such a full-bridge circuit with equal (or at least approximately equal) power for the two sets of power semiconductor devices comprising the output switches, because otherwise the transformer would become saturated and stop working properly. *See* EX1002 ¶¶77-79. This basic POSITA knowledge regarding the proper, balanced way to drive a full-bridge circuit is reflected throughout the prior art. *See, e.g.,* EX1008 at 148 (“So the magnetizing current is determined by the integral [over

time] of the applied winding voltage. The principle of inductor volt-second balance also applies: when the converter operates in steady-state, the dc component of voltage applied to the magnetizing inductance must be zero.... Otherwise, during each switching period there will be a net increase in magnetizing current, eventually leading to excessively large currents and transformer saturation.”), 150 (“[T]he transformer causes $i_{D5}(t)$ [the current through the top power semiconductor device in their example] and $i_{D6}(t)$ [the current through bottom power semiconductor device] to be *equal* in magnitude”), Fig. 6.19 (showing symmetric wave forms for a full-bridge converter).

As a POSITA would have recognized, because the voltage, current, and power through the three power semiconductor devices is equal (or at least approximately equal) to the voltage, current, and power through the other three power semiconductor devices over time, their power dissipation levels (P_t and P_b , respectively) are equal (or at least approximately equal) and therefore well within the mutual 150% threshold required by this claim element. *See* EX1002 ¶81. This is the logical result of two sets of identical electrical structures being driven by the same power over time; a POSITA would have expected that they have the same performance characteristics, as the prior art taught they would. *See, e.g.*, EX1015 at 9:19-23 (“[T]he amount of current flowing through the switching power-supply

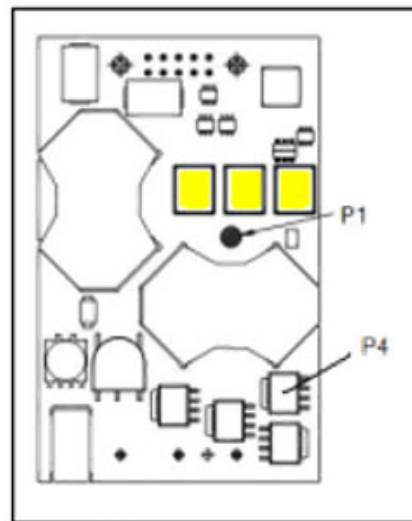
circuits P_A and P_B is substantially equal, such that the heat generation of components of the switching power-supply circuits P_A and P_B are also substantially equal.”).

2. **Claim 2**

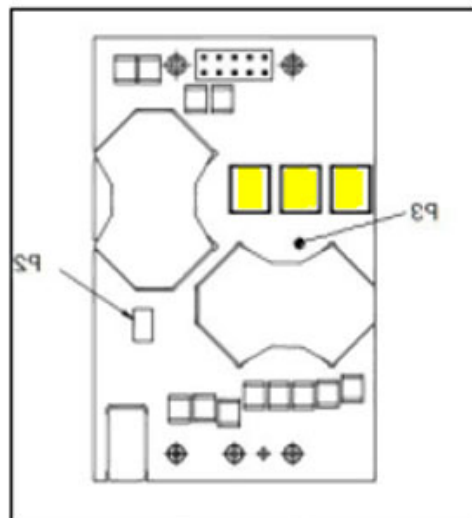
Ericsson-BMR renders obvious Claim 2.⁴ See EX1002 ¶¶83-85.

By reference to the the “Top view” and “Bottom view” of the Ericsson-BMR apparatus on page 24, turning over the “Bottom view” demonstrates that the three bottom power semiconductor devices (highlighted in yellow) are indeed directly under, and thus overlap, the three top power semiconductor devices:

⁴ In each dependent claim discussed in this Petition, the corresponding analysis of the underlying claim(s) on which the dependent claim depends is incorporated by reference from the same Ground (including any cross-references to other Grounds). For example, the analysis of how Claim 1 is rendered obvious in view of Ericsson-BMR is incorporated by reference into this analysis of dependent Claim 2, and the discussion presented in this Claim 2 section then focuses on the additional requirements found specifically in Claim 2.

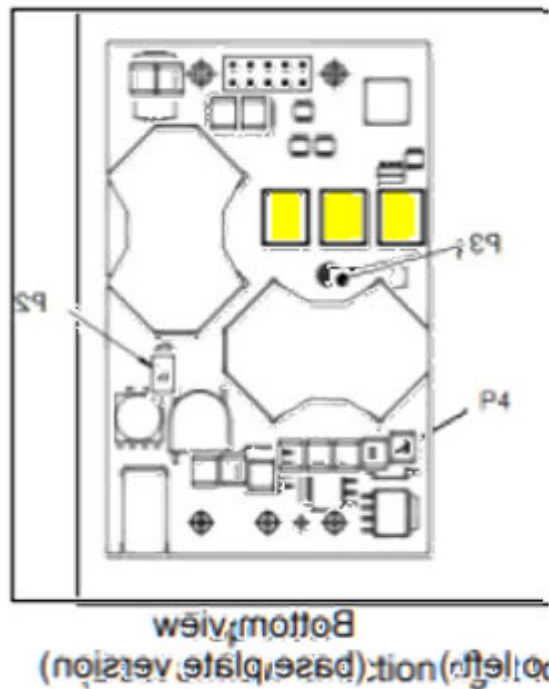


Top view
(Best airflow direction right to left)



Bottom view
(base plate version) (left to right)

See EX1007 at 24 (cropped, rotated, highlighted). This is further confirmed by overlaying the images of the top and bottom views of the Ericsson-BMR, further confirming that the top three power semiconductor devices and the bottom three power semiconductor devices are directly overlapping each other (as are the planar magnet bowtie shapes as well, as expected):



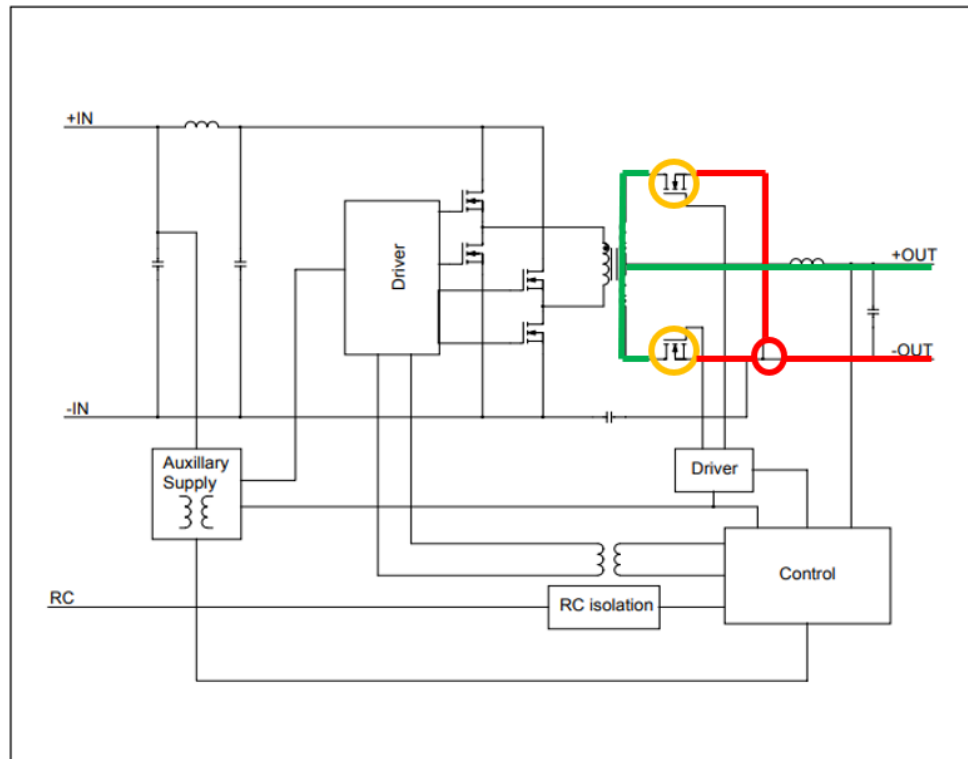
See EX1007 at 24 (modified as described above). Thus, in Ericsson-BMR's module, a plurality of the power semiconductor devices in the first set (*i.e.*, the top three power semiconductor devices highlighted in yellow) are each positioned in a location on the top surface directly overlapping a location on the bottom surface occupied by a power semiconductor device in the second set (*i.e.*, the bottom three power semiconductor devices also highlighted in yellow).

3. **Claim 3**

Ericsson-BMR renders obvious Claim 3. See EX1002 ¶¶87-90.

By reference to Ericsson-BMR's circuit diagram, the output switch on the top (circled in orange at the top of the diagram below) shares a common output connection (circled and outlined in red, for example, and also shown in green) with

the output switch on the bottom (circled in orange at the bottom of the diagram below):



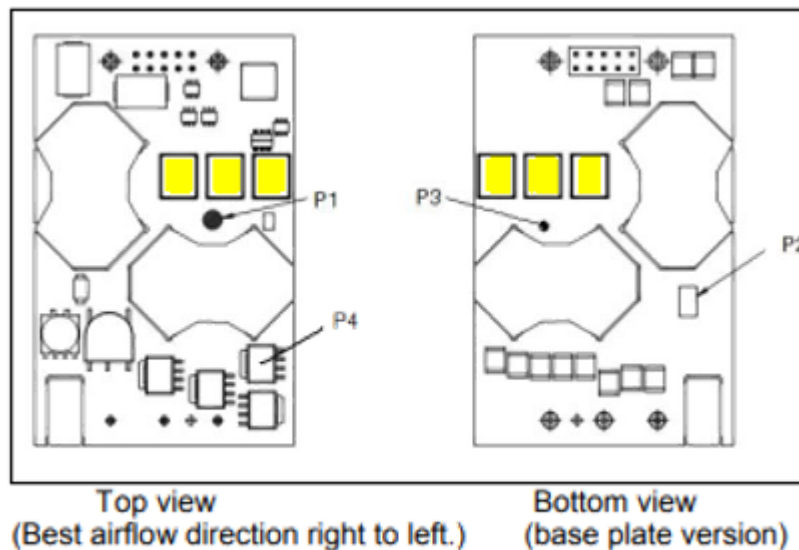
See EX1007 at 5 (annotated). Since these output switches are comprised of power semiconductor devices on the top and bottom of the PCB, a POSITA would therefore have recognized, or at least found obvious, that the top output switch thus shares conductive vias with the bottom output switch, because vias (which function as electrical connections through the PCB) are how the components on the top of the PCB would be electrically connected to the same output as the components associated on the bottom of the PCB. See EX1002 ¶¶89-90. And as discussed above in analyzing Claim 1[e], the output switches are comprised of the three power semiconductor devices pictured on each of the top and bottom views of Ericsson-

BMR (*see* EX1007 at 24), so it would be a plurality of three power semiconductor devices in the top and bottom sets sharing their respective conductive vias. *See id.*

4. **Claim 4**

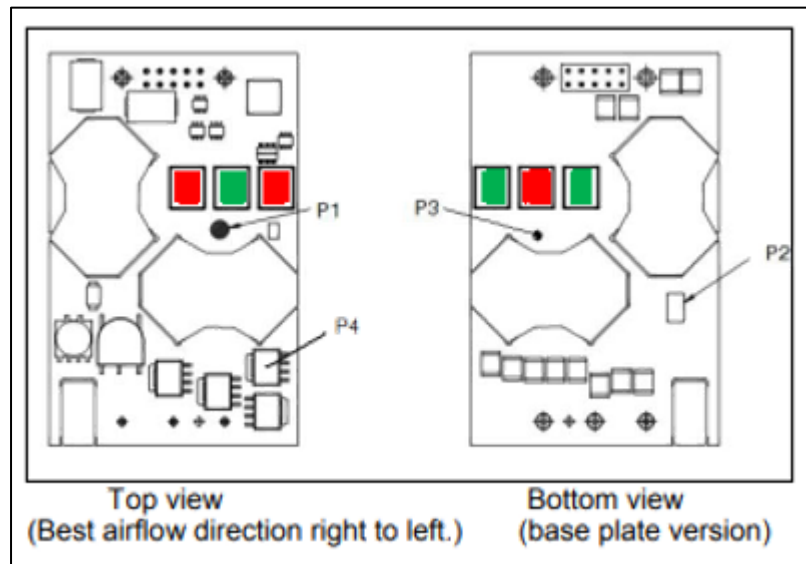
Ericsson-BMR renders obvious Claim 4. *See* EX1002 ¶¶91-95.

As discussed above in Claim 1[d], a POSITA would have recognized the six identical components highlighted below as two sets of three MOSFETs comprising the two output switches:



See EX1007 at 24 (annotated). However, Ericsson-BMR is not explicit as to which of the three MOSFETs on each side correspond to the two output switches. As Dr. Leeb explains, there are only 20 possible combinations that might apply. *See* EX1002 ¶93. Many of those combinations would result in a mirrored layout, and there is no material distinction between any of the combinations. As a result, it would have been obvious for a POSITA to try assigning FETs to output switches as follows

(which is just one of several of the 20 combinations that would reflect a mirrored layout), where the green-highlighted FETs correspond to one output switch and the red-highlighted FETs correspond to the other output switch:



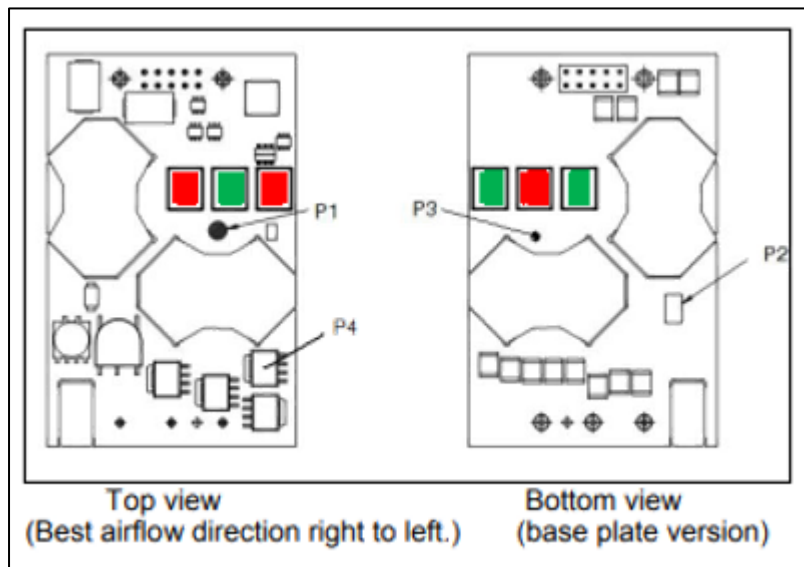
See EX1007 at 24 (annotated); EX1002 ¶¶93-94 (discussing similar examples of FET allocations such as this known in the art, evidencing both motivation as obvious to try and a reasonable expectation of success in this arrangement).

In this arrangement, each of these output switches is a cell having the same circuit topology and each including FET power semiconductor devices from the top and bottom surfaces (*i.e.*, from the first and second sets), and each cell has its respective components arranged in a pattern wherein the pattern of components of one cell is a mirror image, over an axis co-planar with the PCB, of the pattern of components in the other cell. See EX1002 ¶94.

5. **Claim 5**

Ericsson-BMR renders obvious Claim 5. *See* EX1002 ¶¶96-98.

As discussed above in Claim 4, the (for example) middle MOSFET of the first output switch is on the opposite surface of the middle MOSFET of the second output switch, as indicated by the red/green distinction:

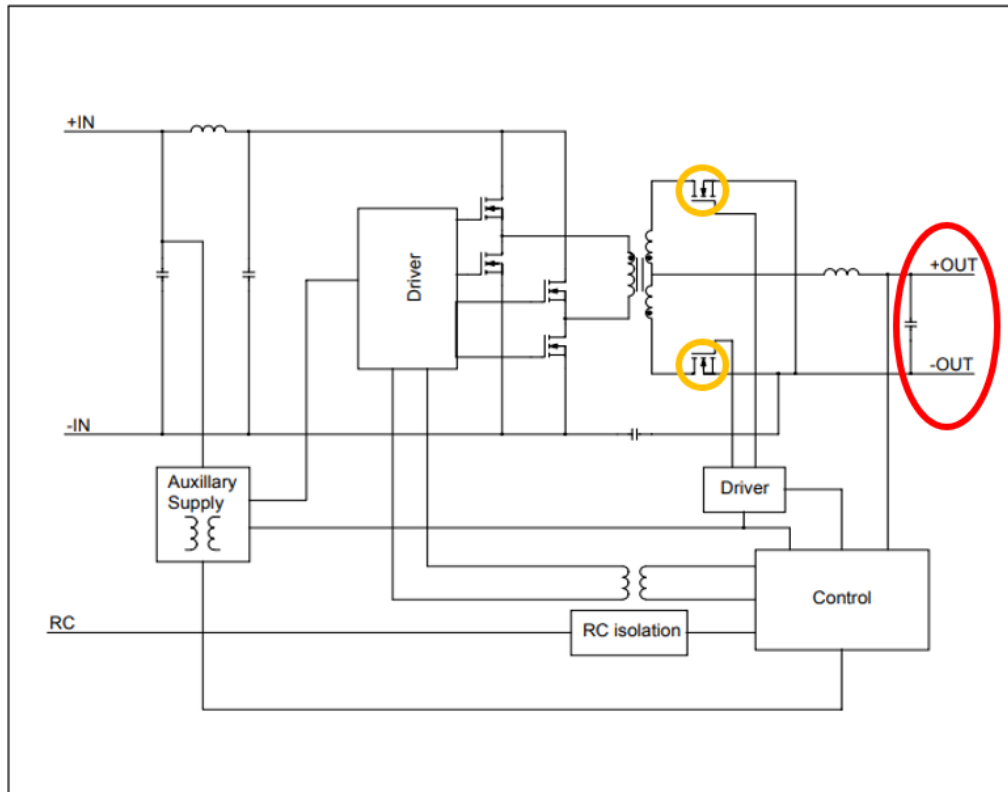


See EX1007 at 24 (annotated).

6. **Claim 7**

Ericsson-BMR renders obvious Claim 7. *See* EX1002 ¶¶99-101. As shown in Ericsson-BMR’s fundamental circuit diagram, the two components circled in orange are switches, as a POSITA would have recognized those symbols as the symbols for switches. *See* EX1002 ¶101; EX1008 at, *e.g.*, Fig. 2.13(b). And those two switches are electrically connected to, and switch on or off, conduction paths to the “OUT”

terminals of the circuit circled in red, such that a POSITA would have recognized those switches are output switches:



See EX1007 at 5 (annotated); EX1002 ¶101.

7. **BMR-2008**

The relevant teachings of BMR-2008 are substantially the same as the relevant teachings of Ericsson-BMR, including the symmetry and fundamental circuit diagram of a full-bridge converter. Compare EX1007 at, e.g., 1, 2, 5, 24, 31 with EX1026 at, e.g., 1, 4, 15, 20. As a result, Claims 1-5 and 7 are rendered obvious by BMR-2008 for the same reasons as they are rendered obvious by Ericsson-BMR set forth above. See EX1002 ¶¶102-103.

B. Ground II: Claim 1-5 And 7 Are Rendered Obvious By Ericsson-BMR In View Of Spiazzi Or, Alternatively, By BMR-2008 In View Of Spiazzi.

1. **Claim 1**

Claim 1 is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* EX1002 ¶¶104-112.

a. 1/[preamble]

Claim 1[preamble] is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VI.A.1.a; EX1002 ¶105.

b. 1/[a]

Claim 1[a] is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VI.A.1.b; EX1002 ¶106.

c. 1/[b]

Claim 1[b] is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VI.A.1.c; EX1002 ¶107.

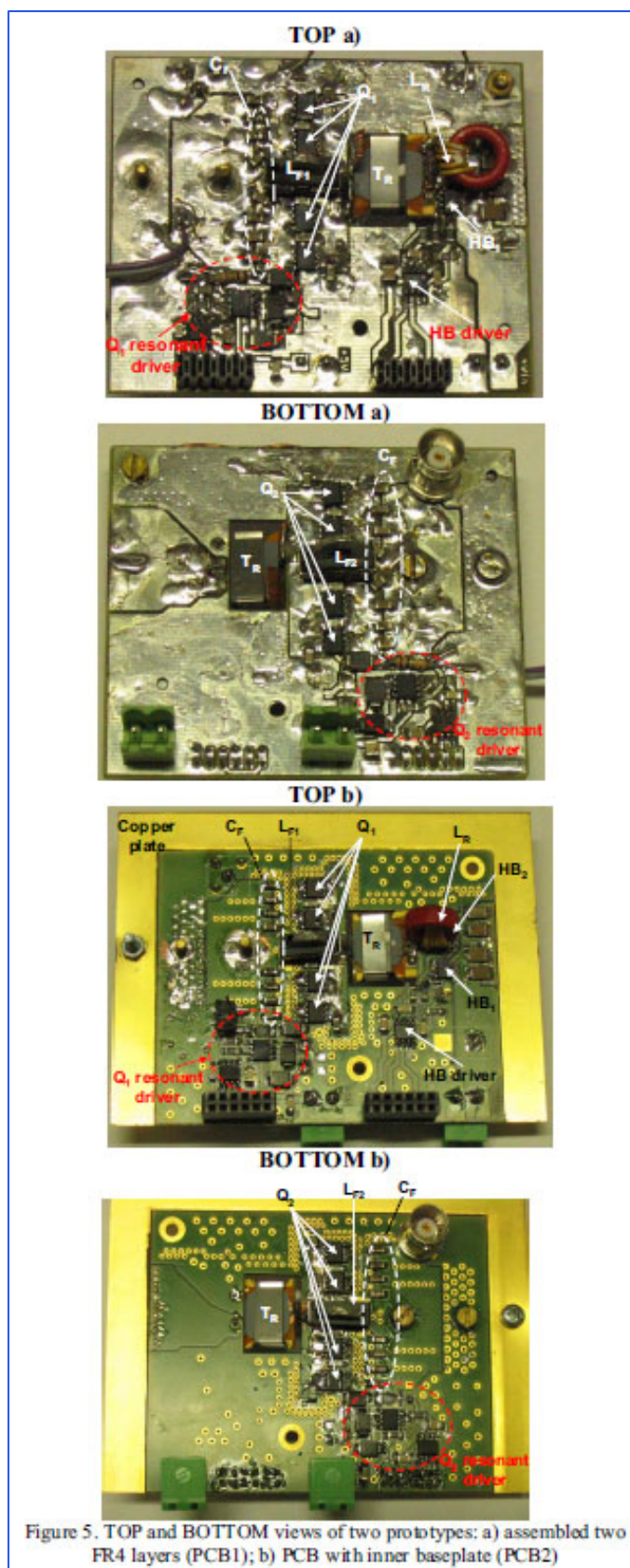
d. 1/[c]

Claim 1[c] is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VI.A.1.d; EX1002 ¶108.

e. 1/[d]

Claim 1[d] is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VI.A.1.e; EX1002 ¶¶109-110.

If Ericsson-BMR is found to have not taught or at least rendered obvious this element, Spiazzi teaches and renders obvious that Ericsson-BMR's components are power semiconductor devices on the top and bottom surfaces and act as output switches. Spiazzi's refers to "synchronous rectifier (SR) switches Q₁ and Q₂," which it teaches are comprised of "four SR MOSFETs," which are power semiconductor devices. *See* EX1011 at 1993-1994; *see also id.* at Fig. 1.a (circuit diagram confirming that Q₁ and Q₂ are output switches). The overlapping placement of the four MOSFET power semiconductor devices comprising the Q₁ output switch with the four MOSFET power semiconductor devices comprising Q₂ can be seen, for example, in Spiazzi's Figure 5 shown here:



See EX1011 at Fig. 5 (annotations in original). In view of Spiazzi's teachings, a POSITA would (to the extent it did not already) have found it obvious that the two sets of three components on the top and bottom of Ericsson's PCB were power semiconductor MOSFETs that comprised two output switches.

f. 1[e]

Claim 1[e] is rendered obvious by Ericsson-BMR in view of Spiazzi. See §VI.A.1.f; EX1002 ¶¶111-112.

Spiazzi further confirms that Ericsson-BMR's full-bridge circuit would produce substantially similar results of power dissipation on both sides of the Ericsson-BMR module. Spiazzi teaches a half-bridge converter⁵, which, like Ericsson-BMR's full-bridge converter, would have at least obviously applied balanced power cycles in order to avoid saturating the transformer. See EX1002 ¶112. Spiazzi then performs a thermal mapping of two different configurations of its power converter, and shows the top sides of the two different configurations in Figure 11. See EX1011 at 2000. Although only the top sides of the two different configurations are shown, Spiazzi teaches that “[s]imilar results were obtained for the downward surfaces.” See EX1011 at 1999. A POSITA would therefore have recognized that Ericsson-BMR, under similar cycling, would also have featured

⁵ See EX1011 at Fig. 1.a (“half-bridge resonant VRM”).

power dissipation levels Pt and Pb that would at least be “similar” and well within 150% of each other. *See id.*

2. **Claim 2**

Claim 2 is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VI.A.2; EX1002 ¶¶113-114.

3. **Claim 3**

Claim 3 is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VI.A.3; EX1002 ¶115.

4. **Claim 4**

Claim 4 is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VI.A.4; EX1002 ¶116.

5. **Claim 5**

Claim 7 is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VI.A.5; EX1002 ¶117.

6. **Claim 7**

Claim 7 is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VI.A.6; EX1002 ¶118.

7. **BMR-2008**

The relevant teachings of BMR-2008 are substantially the same as the relevant teachings of Ericsson-BMR. *Compare* EX1007 at, *e.g.*, 1, 2, 5, 24, 31 *with* EX1026 at, *e.g.*, 1, 4, 13, 15, 20. As a result, Claims 1-5 and 7 are rendered obvious by BMR-

2008 in view of Spiazzi for the same reasons as they are rendered obvious by Ericsson-BMR in view of Spiazzi set forth above. *See* EX1002 ¶¶119-120.

C. Ground III: Claim 1-7 Are Rendered Obvious By Ericsson-BMR In View Of Wanes, Or, Alternatively, By BMR-2008 In View Of Wanes

1. Claim 1

Claim 1 is rendered obvious by Ericsson-BMR in view of Wanes. *See* EX1002 ¶¶121-131.

a. 1/[preamble]

Claim 1[preamble] is rendered obvious by Ericsson-BMR in view of Wanes. *See* §VI.A.1.a; EX1002 ¶122.

b. 1/[a]

Claim 1[a] is rendered obvious by Ericsson-BMR in view of Wanes. *See* §VI.A.1.b; EX1002 ¶123.

c. 1/[b]

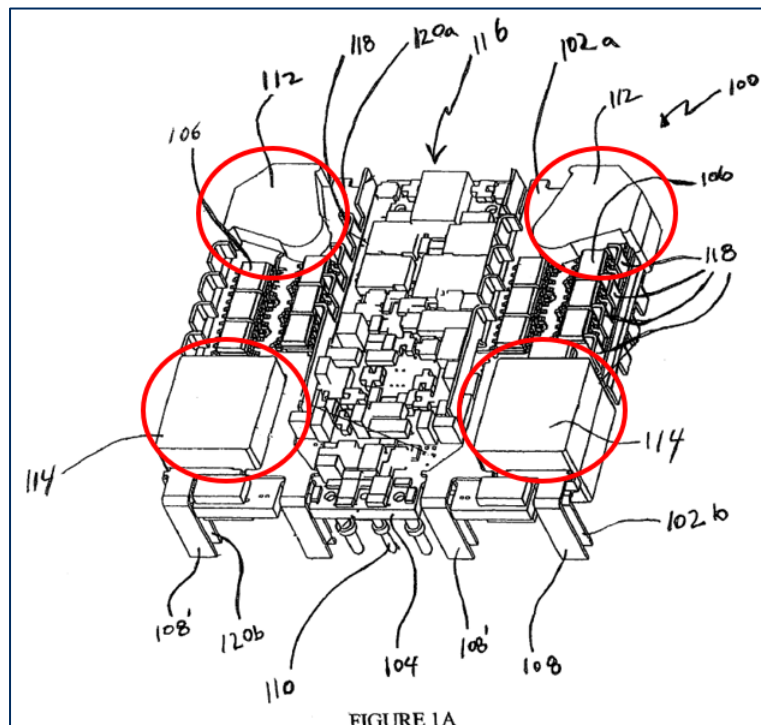
Claim 1[b] is rendered obvious by Ericsson-BMR in view of Wanes. *See* §VI.A.1.c; EX1002 ¶124. This is particularly true given that Wanes expressly teaches a plurality of conductive layers in the PCB, thus further supporting that a POSITA would have recognized and found obvious that Ericsson-BMR's golden PCB layers comprised a plurality of conductive layers. *See* EX1009 at 4:33-34 ("primary windings are embedded in internal tracks in *internal layers in PCB*").

d. l[c]

Claim 1[c] is rendered obvious by Ericsson-BMR in view of Wanes. *See* §VI.A.1.d; EX1002 ¶¶125-129.

If Ericsson-BMR is found to have not taught, or at least rendered obvious, that the windings of the transformer are formed by traces in one or more of the conductive layers of the PCB, Wanes teaches this. *See* EX1002, ¶¶127-128. With reference to elements 112 and 114 circled in red below in Figure 1A, Wanes teaches:

It will be appreciated that transformer 112 and inductor 114 both belong to a family of signal transforming components which are known in the art as “magnetics”. Magnetics typically have a winding such as winding 112A and 114A interacting with a magnetic core, such as 112C and 114B respectively.



EX1009 at 4:45-50, Fig. 1A (annotated). Wanes goes on to teach that “primary windings are embedded ... in internal layers in PCB 104,” where element 104 is the PCB as discussed in the previous element. *See* EX1009 at 4:10-12, 4:31-48, 9:44-51 (“Windings (not shown) are sandwiched within each PCB and encircle openings 414 and 416. Each winding of PCB 104 co-operates with a respective winding of the magnetics of transformer 112 and inductor 114....”). Because the winding traces carry current as part of the physics of the voltage conversion process, the layer of the PCB in which those winding traces are found are conductive.

A POSITA would have been motivated to form Ericsson-BMR’s windings in this manner for a number of reasons, including because: (i) it is more space efficient; (ii) as discussed above, Ericsson-BMR does not provide for the traces to be anywhere but the PCB (*see* §VI.A.1.d); and (iii) forming the windings in this manner was a well-known technique, and thus a POSITA would have had a reasonable expectation of success in doing so (*see, e.g.*, EX1019 at 1:54-60). *See* EX1002 ¶129.

e. 1[d]

Claim 1[d] is rendered obvious by Ericsson-BMR in view of Wanes. *See* §VI.A.1.e; EX1002 ¶130.

f. 1[e]

Claim 1[e] is rendered obvious by Ericsson-BMR in view of Wanes. *See* §VI.A.1.f; EX1002 ¶131.

2. **Claim 2**

Claim 2 is rendered obvious by Ericsson-BMR in view of Wanes. *See* §VI.A.2; EX1002 ¶132.

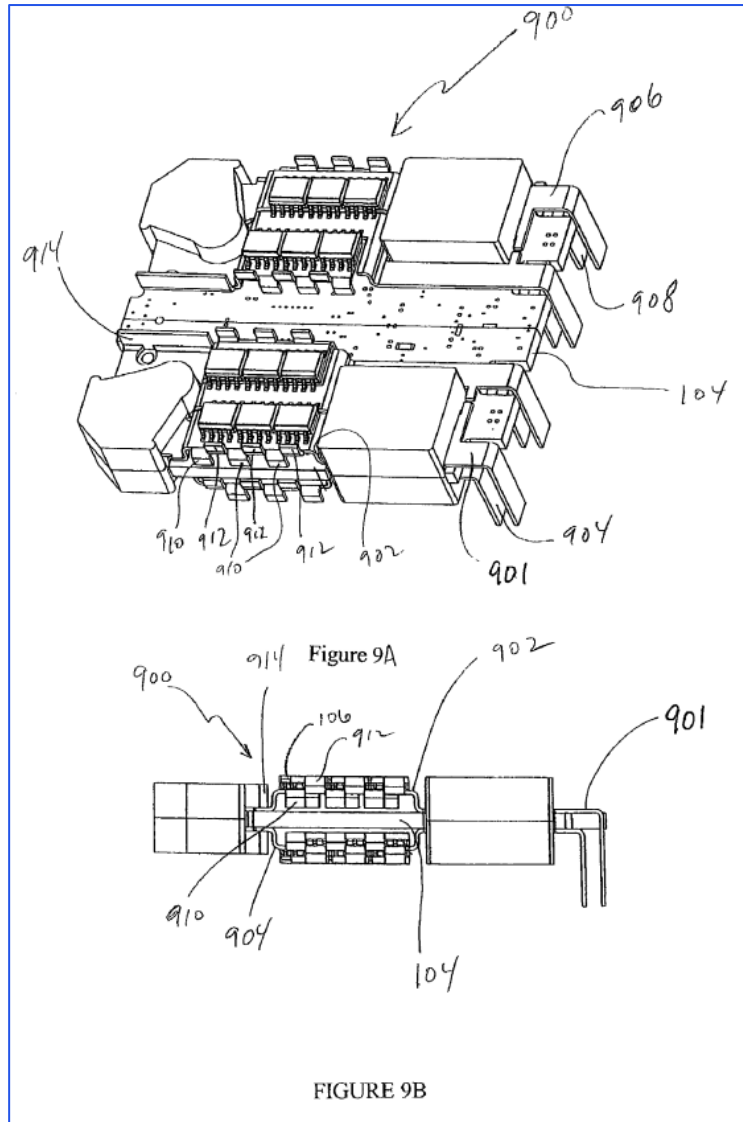
3. **Claim 3**

Claim 3 is rendered obvious by Ericsson-BMR in view of Wanes. *See* §VI.A.3; EX1002 ¶133.

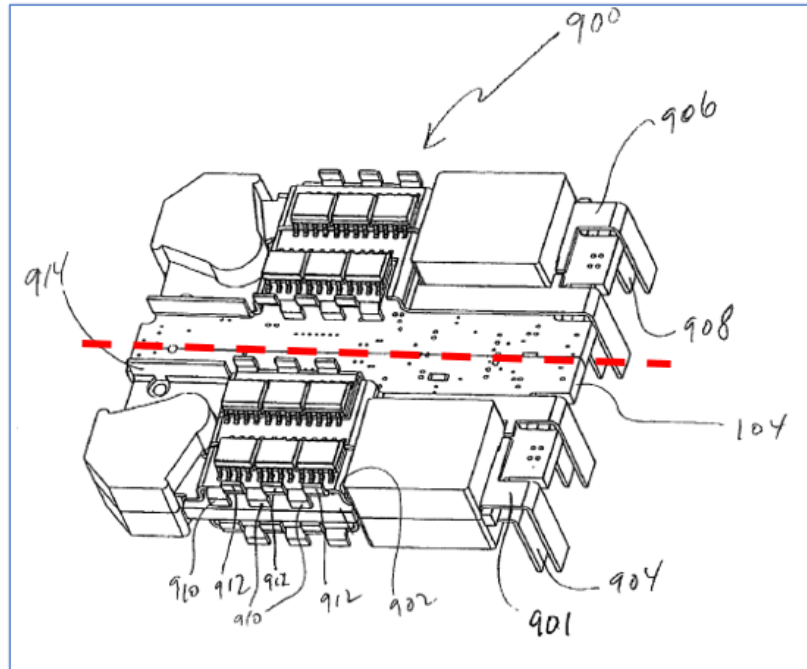
4. **Claim 4**

Claim 4 is rendered obvious by Ericsson-BMR in view of Wanes. *See* EX1002 ¶¶134-139.

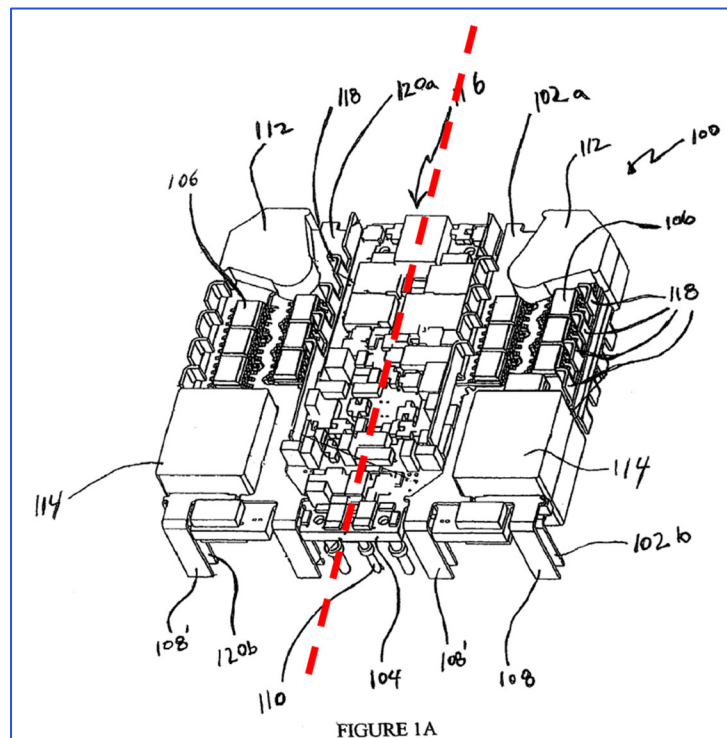
As background, Wanes teaches replicating a specific circuit topology four times. *See* EX1009 at 11:10-11 (“substrates 901, 904, 906, and 908 have similar configurations”). Two of the four instances of the common circuit topology directly overlap each other on top and bottom, as pictured below in Wanes’s Figure 9B by reference to 901 and 904, and the other two of the four instances of the common circuit topology mirror that setup, as pictured below in Wanes’s Figure 9A where elements 906/908 mirror 901/904:



See EX1009, Figs. 9A-B. For example, Elements 901 and 904 are together a claimed “cell,” and elements 906 and 908 are together an identical claimed “cell,” including because they are discrete, repeatable units comprised of electrical components that perform a certain function. As shown here in this annotated Figure 9A, each of the cells in this pair of cells has its components arranged in a pattern, and the pattern of components in the 901/904 cell is a mirror image of the pattern of components in the 906/908 cell:



The same mirror cell symmetry is shown, for example, in this annotated version of Figure 1A, where 120a and 120b are together one cell and 102a and 102b are together another cell:



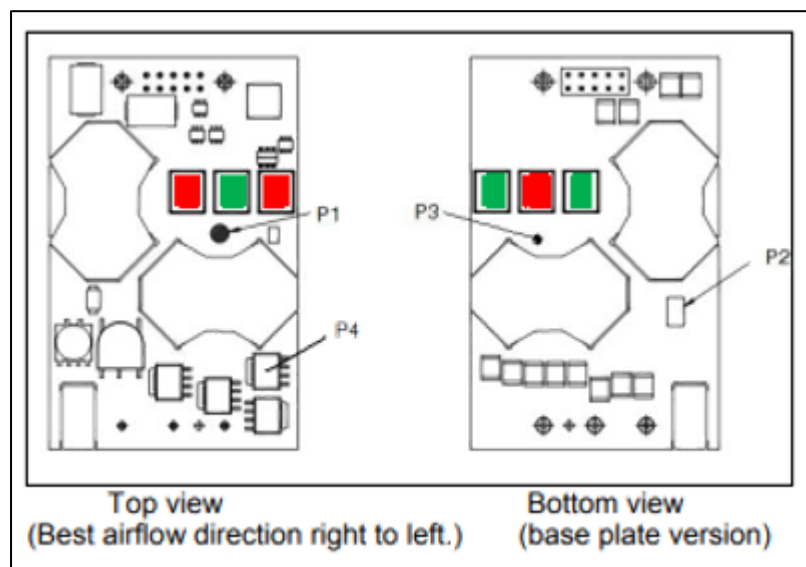
See EX1009, Fig. 1A (annotated), 3:66-67 (“Substrate 120 has a ***mirror image*** configuration of substrate 102.”); *see also, e.g.*, EX1009 at 10:47-58.

Separately, the Ericsson-BMR module is provided in “Industry standard Quarter-brick” format. *See* EX1007 at 1. As a POSITA would have been aware, in applications where a “quarter brick”-sized power converter was insufficient to provide necessary power to a system, one option to increase power would be to use the next standard size up after a “quarter brick,” which is known as a “half brick.” *See* EX1002 ¶¶137-138. Given Wanes’s teachings where the FETs are mirrored, one obvious approach to creating a “half brick” version of the Ericsson-BMR module would therefore have been to mirror the inverter and output FET power semiconductor devices of the Ericsson-BMR module on a single, larger board of half-brick size. These components would have been mirrored in a manner analogous to the mirroring of Wanes’s substrates 120a and 102b in Figure 1A. *See* EX1009 at Fig. 1A; *see also, e.g.*, EX1009 at Fig. 9A (substrates 901 mirrored with 908). *See* EX1002 ¶138.

In this combination of Ericsson-BMR and Wanes, the original inverter and output FET power semiconductor devices of the quarter-brick Ericsson-BMR converter would be a cell, and they would be mirrored on an extended PCB in accordance with Wanes’s teachings. A POSITA would have had a reasonable expectation of successfully being able to mirror the Ericsson-BMR cell in this

manner, as mirroring techniques were taught by Wanes. *See* EX1002 ¶138. A POSITA also would have been motivated to create this half-brick for a number of reasons. For example, this approach would allow a designer to “integrate redundant power-supply hardware.” *See* EX1018 at 2. Additionally, it would also allow a customer to service higher power applications. Additionally, Wanes’s entire power converter (element 100 in Figure 1A) operates as a unified power converter, thus teaching a POSITA the benefits of using mirrored cells for higher power outputs. *See* EX1009 at 4:22-44.

Additionally and independently, Wanes’s mirroring teachings provide further motivation to mirror Ericsson-BMR’s output FETs in a mirroring fashion as follows, where the red-highlighted FETs correspond to one output switch while the green-highlighted FETs correspond to the other output switch depicted in Ericsson-BMR’s fundamental circuit diagram (EX1007 at 5):

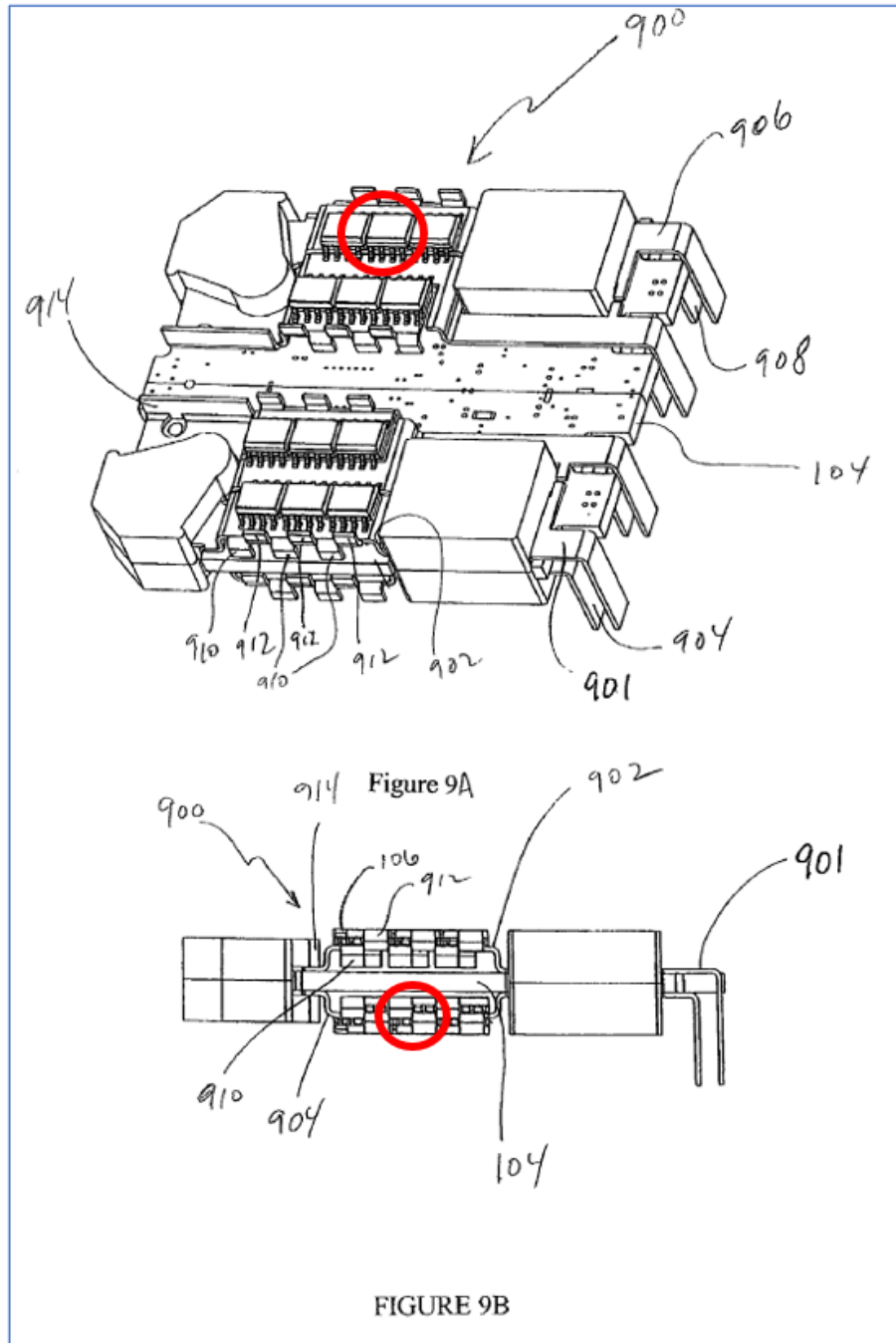


See EX1007 at 24 (annotated); EX1002 ¶139; EX1029 at 3 (additional evidence rendering obvious such mirroring). This arrangement also independently satisfies the claim element with respect to mirrored cells for the reason discussed above. *See* EX1002 ¶139.

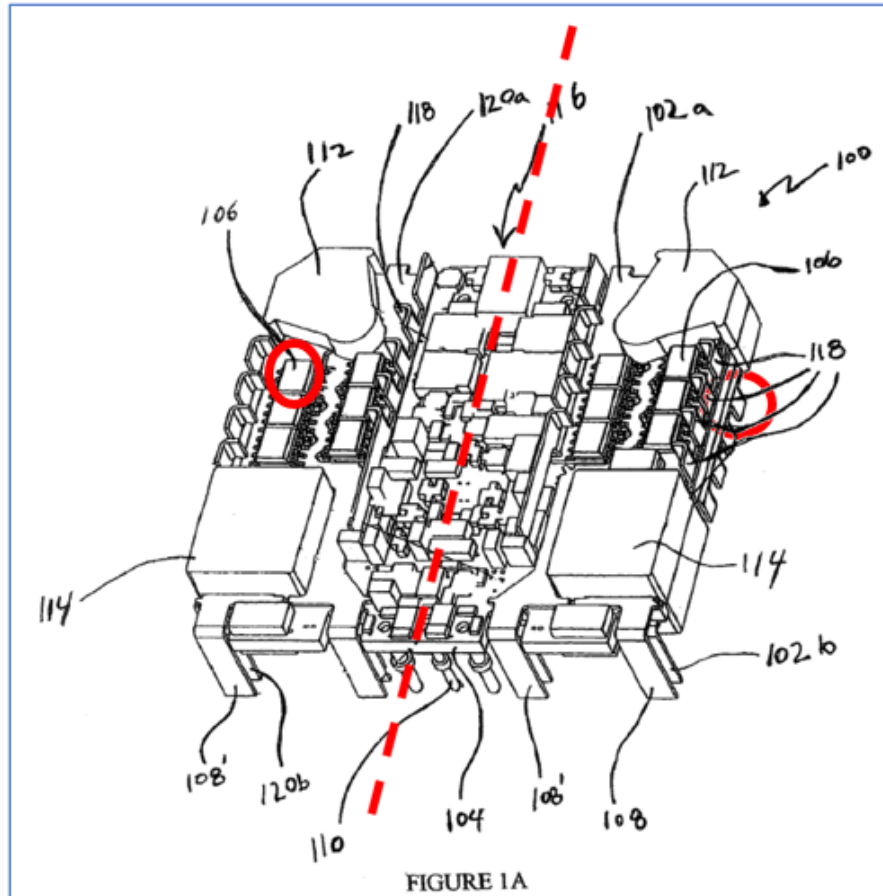
5. **Claim 5**

Claim 5 is rendered obvious by Ericsson-BMR in view of Wanes. *See* EX1002 ¶¶140-143.

In the first asserted embodiment of mirrored cells discussed in the context of Claim 4 (the half-brick-sized version of Ericsson BMR), the FETs would be mirrored as taught by Wanes. Wanes teaches, for example, that a FET component 106 in the top, 906 portion is located on an opposite surface of a respective FET component in the bottom, 904 portion circled here:

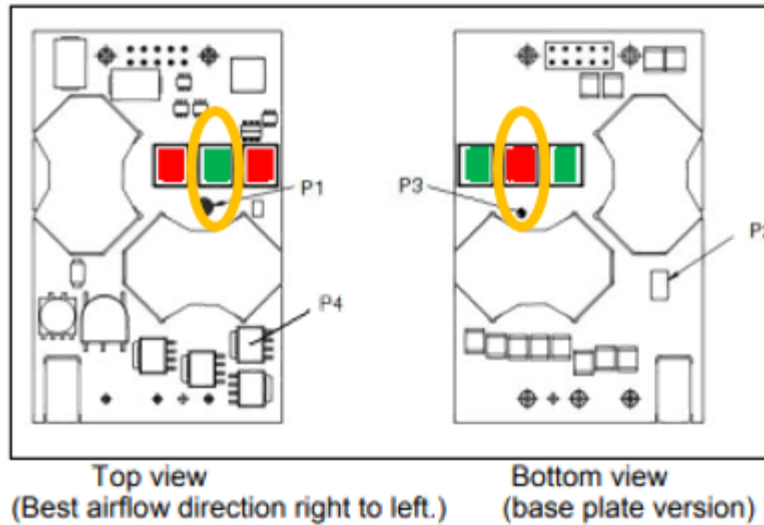


See EX1009 at Fig. 9A-B (annotated). Likewise here where FET 106 on 120a is located on a surface opposite a respective FET 106 component on 102b:



See EX1009 at Fig. 1A (annotated); *see also id.* at 3:66-67. In the asserted half-brick combination, Ericsson-BMR's FETs would be configured in this mirrored layout (as discussed in the context of Claim 4), so Ericsson-BMR's corresponding power semiconductor devices would satisfy this claim.

Additionally and independently, in the second asserted embodiment of mirrored cells asserted in this Ground, it can be seen that, for example, the green-highlighted middle MOSFET component of one of the cells is on the top surface of the PCB (circled in orange on the left), which is on an opposite surface of a respective red-highlighted middle MOSFET component of the other cell:

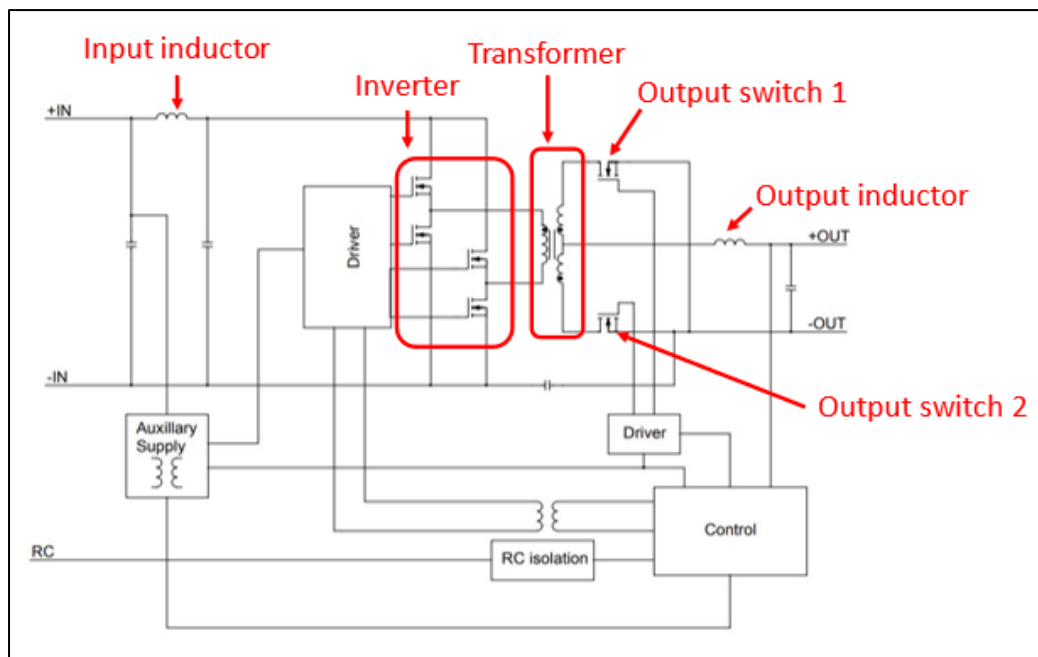
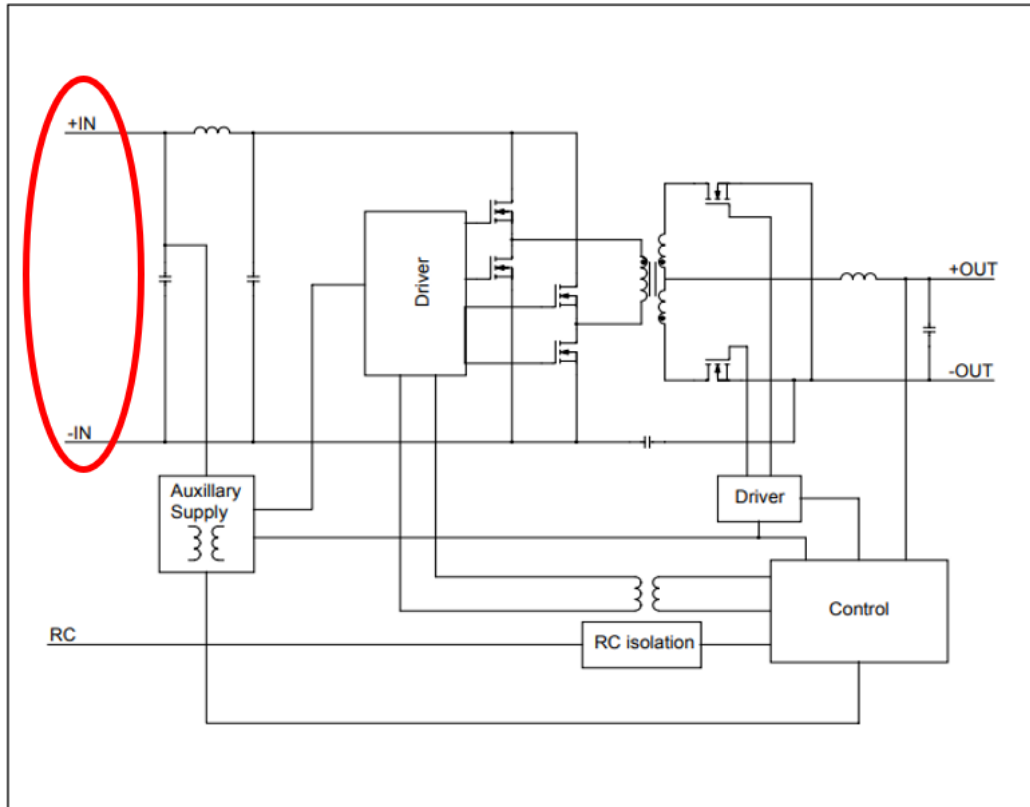


See EX1007 at 24 (annotated). A POSITA would have known about such mirroring techniques in the prior art and found them obvious to apply to Ericsson-BMR. See EX1002 ¶143; EX1029 at 3.

6. **Claim 6**

Claim 6 is rendered obvious by Ericsson-BMR in view of Wanes. See EX1002 ¶¶144-146.

In the half-brick asserted embodiment, each set of mirrored inverter and output FET power semiconductor devices are a cell, and they comprise an input cell because the inverter power semiconductor devices are used on the input side of the circuit:



See EX1007 at 5 (annotated); EX1002 ¶¶62, 146.

7. **Claim 7**

Claim 7 is rendered obvious by Ericsson-BMR in view of Wanes. *See* §VI.A.6; EX1002 ¶147.

8. **BMR-2008**

The relevant teachings of BMR-2008 are substantially the same as the relevant teachings of Ericsson-BMR. *Compare* EX1007 at, *e.g.*, 1, 2, 5, 24, 31 with EX1026 at, *e.g.*, 1, 4, 13, 15, 20. As a result, Claims 1-7 are rendered obvious by BMR-2008 in view of Wanes for the same reasons as they are rendered obvious by Ericsson-BMR in view of Wanes set forth above. *See* EX1002 ¶¶148-149.

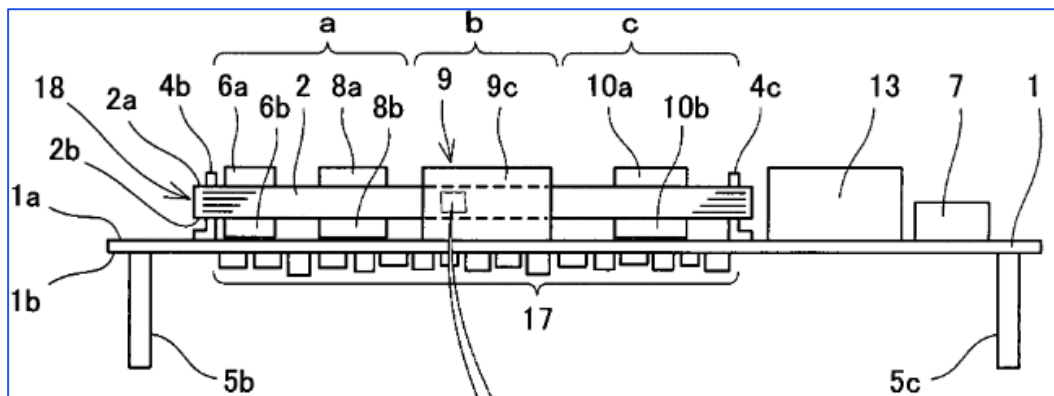
D. Ground IV: Claims 1-7 Are Rendered Obvious by Takeshima

1. **Claim 1**

Claim 1 is rendered obvious by Takeshima. *See* EX1002 ¶¶150-167.

a. 1[preamble]

Takeshima teaches and renders obvious the preamble. *See* EX1002 ¶¶151-152. An example of an apparatus taught by Takeshima can be seen (among other places) in Takeshima's Figure 2, a portion of which is shown here:



See EX1010 at Fig. 2 (cropped).

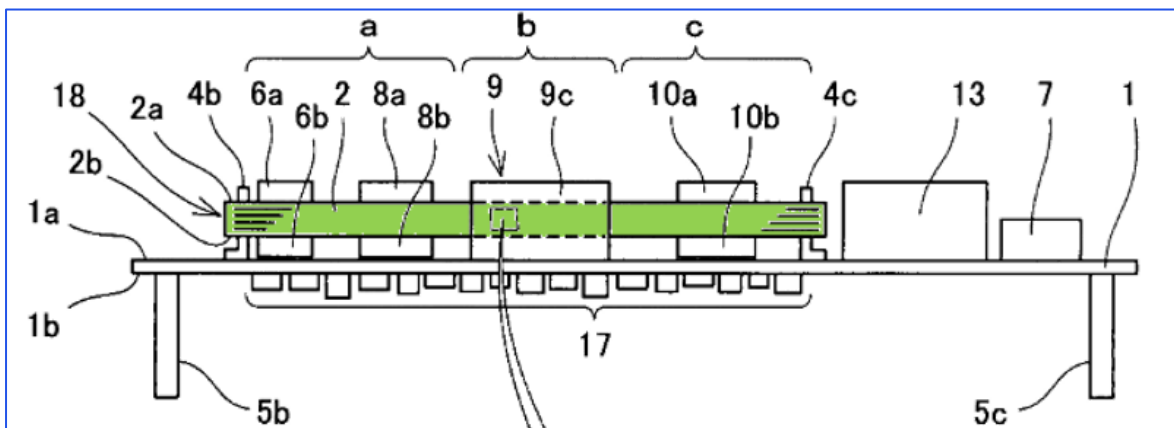
b. 1[a]

Takeshima teaches and renders obvious this element. See EX1002 ¶¶153-154. For example, the circuit in Takeshima's Figure 7 is "a circuit diagram of a switching power supply device ... that adopts a half-bridge type **converter** circuit." See EX1010 at 7:47-50. Half-bridge type converters were well-known power converter circuits. See EX1002 ¶154; EX1008 at 152-54.

c. 1[b]

Takeshima teaches and renders obvious this element. See EX1002 ¶¶155-158.

Takeshima teaches a PCB. See EX1010 at, e.g., 4:33 ("printed circuit board"), 6:38 (same). Takeshima's PCB can be seen, for example, as element 2 in Figure 2, highlighted here in green:



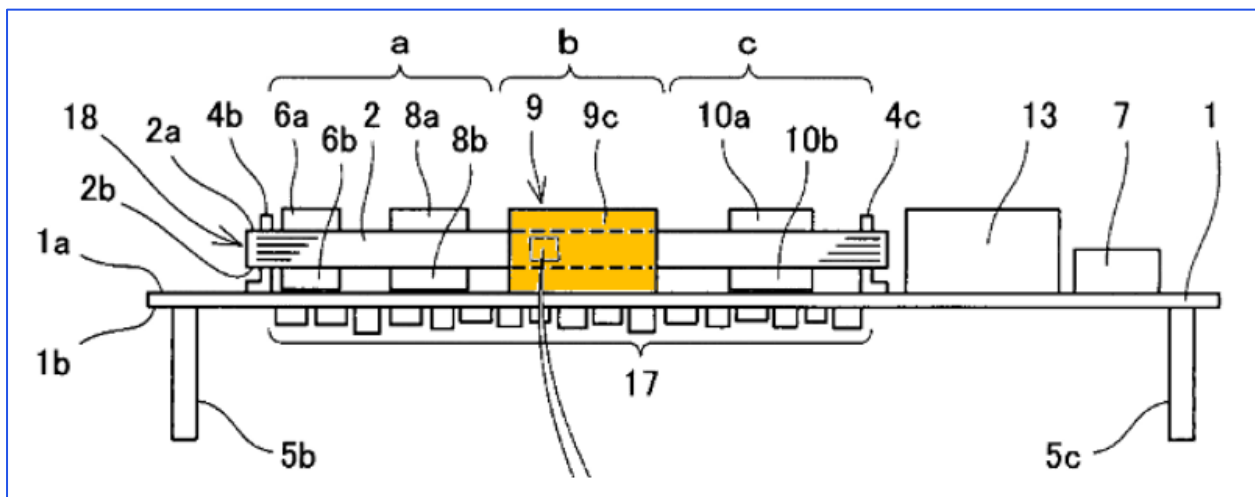
See EX1010 at Fig. 2 (annotated, cropped), 9:38-40. Takeshima's PCB is comprised of a plurality of layers. See EX1010 at, e.g., 9:40 ("**multi-layer** printed circuit board 2"). Takeshima teaches that this plurality of layers is conductive. See EX1010 at,

e.g., 9:47-50 (“The wiring, which is a constituting element of the multi-layer printed circuit board 2 but not shown in the figure, is composed of a plurality of wiring lines for electrically connecting a plurality of semiconductor elements or the like arranged on the multi-layer printed circuit board 2...”). As shown above above in Figure 2, the PCB has a top surface 2a and a bottom surface 2b. *See also* EX1010 at 10:51-67 (“first major surface 2a and a second major surface 2b of the multi-layer printed circuit board”).

d. 1/c]

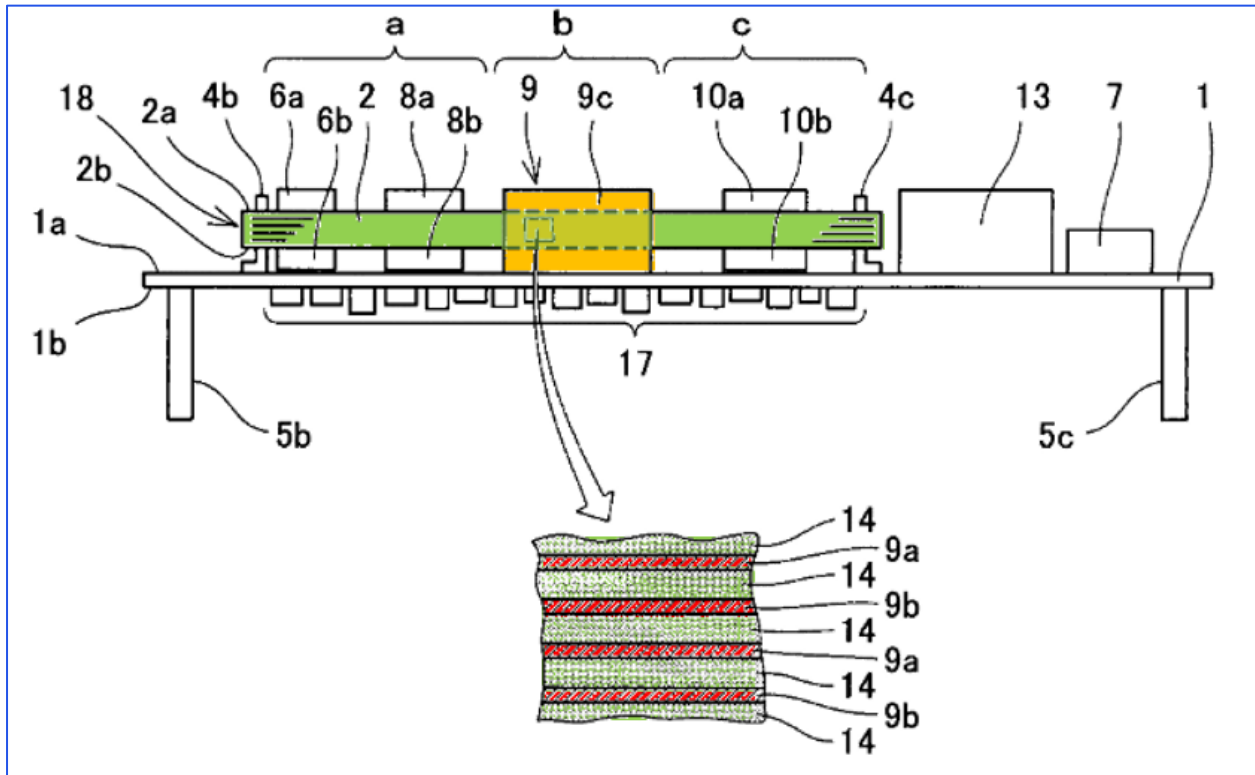
Takeshima teaches and renders obvious this element. *See* EX1002 ¶¶159-161.

Takeshima teaches a magnetic core, which is shown as element 9 in Figure 2 highlighted below in orange, that is magnetically coupled to windings:



See EX1010 at Fig. 2 (annotated, cropped), 9:3-5 (“The transformer secondary winding 9b of the transformer 9 is **magnetically** connected to the transformer primary winding 9a by the **transformer core** 9c.”).

Takeshima teaches that the windings are formed by traces in the conductive layers of the PCB, as shown by the zoomed in section in Figure 2, where the winding traces are highlighted in red.

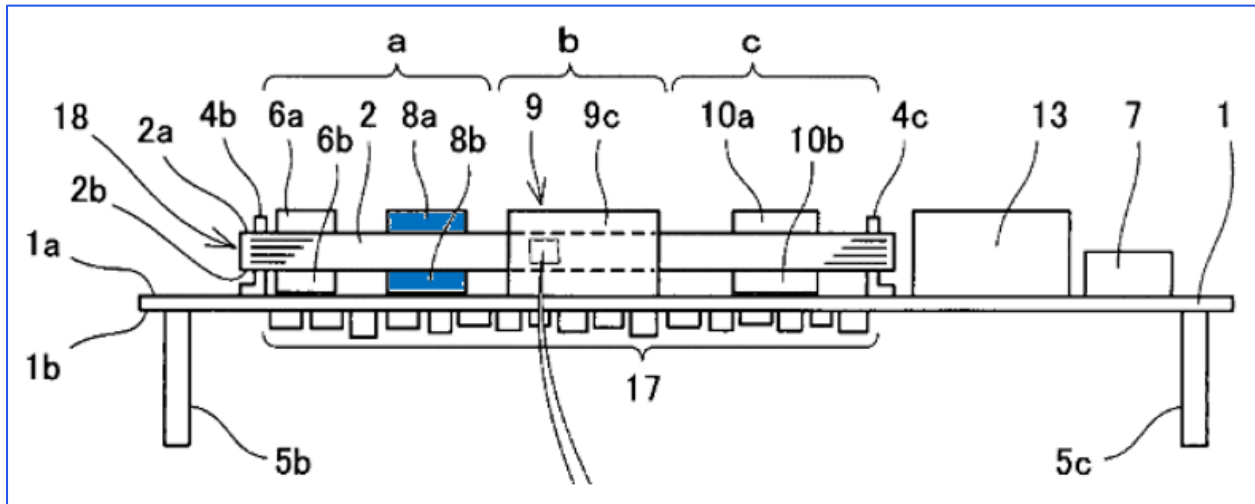


See EX1010 at Fig. 2 (annotated), 9:62-10:3 (“transformer primary winding **9a** and the transformer secondary winding **9b** are formed within the transformer winding region b of the multi-layer printed circuit board **2** in the following manner: spiral-shaped wiring lines formed in respective layers of the multi-layer printed circuit board **2** are stacked [on] each other with electrically insulative members **14** interposed therebetween....”)

e. 1[d]

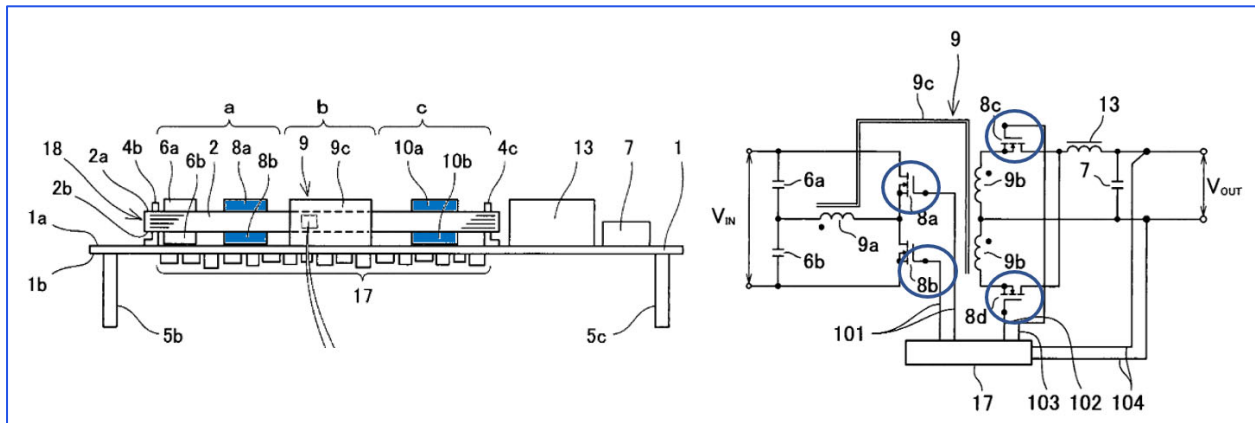
Takeshima teaches and renders obvious this element. See EX1002 ¶¶162-164.

As background, Takeshima teaches that “MOS field-effect transistors (hereafter abbreviated as ‘MOSFETs’) 8a and 8b” are placed on the top and bottom of the PCB, as shown here in this annotated Figure 2:



See EX1010 at Fig. 2 (annotated, cropped), 8:46-47, 10:51-55. Takeshima teaches that this layout could “advantage[ously]” employ a “half-bridge” converter circuit such as that shown in Figure 7, and further that “other converter circuits may be used.” See EX1010 at 7:47-50, 14:44-59. Accordingly, it would have been obvious to a POSITA to employ the half-bridge converter taught in Takeshima’s Figure 14, which is identical in layout to the half-bridge converter in Figure 7 except that Figure 7’s diodes 10a/10b are substituted with MOSFET switches (numbered 8c/8d in Figure 14) and control mechanism 17 additionally is used to control those MOSFET switches. See EX1002 ¶163. This would have been obvious at least because Takeshima’s Figure 14 circuit retains all of the benefits that Takeshima teaches are associated with half-bridge converters that are otherwise identical in Takeshima’s

Figure 7, while providing additional control by using MOSFET switches instead of diodes. *See* EX1002 ¶163. In this Ground, therefore, MOSFET switches 8a, 8b, 8c, and 8d in Figure 14 shown below on the right (circled in blue) would correspond to the placement in 8a, 8b, 10a, and 10b, respectively, in Takeshima's Figure 2 shown below on the left (highlighted in blue):



See EX1010 at Figs. 2, 14 (annotated, cropped).

These four MOSFET devices are a plurality of power semiconductor devices, for the same reasons that Ericsson-BMR's, Spiazzi's, and Wanes's MOSFETs/FETs are power semiconductor devices. *See* §§VI.A.1.e; VI.B.1.e; VI.C.1.e. As shown above on the left side, a first set of Takeshima's MOSFETs (8a and 8c) are mounted on the top surface of the PCB 2, and a second set of Takeshima's MOSFETs (8b and 8d) are mounted on the bottom surface of the PCB. As shown above on the right side, they are all electrically connected in the manner that would dissipate power during operation of the converter, at a level Pt on the top and at a level Pb on the bottom. *See* EX1002 ¶164; EX1008 at 2-3.

f. 1/e]

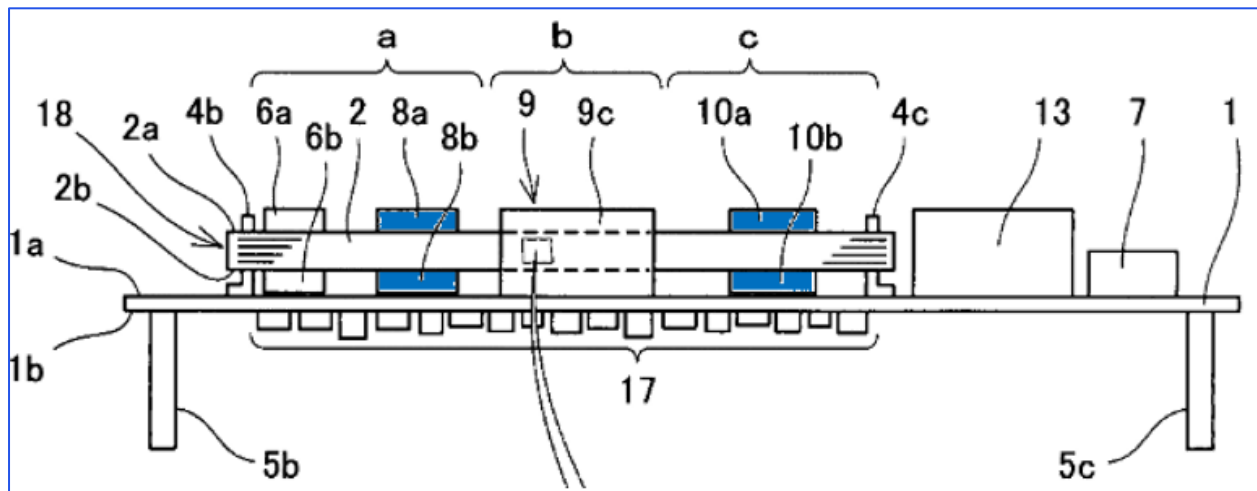
Takeshima teaches and renders obvious this element. *See* EX1002 ¶¶165-167.

A POSITA would have known to operate Takeshima’s half-bridge converter with balanced power cycles on the top and bottom sides in order to avoid saturating the transformer. *See* EX1002 ¶166; EX1008 at 152 (applying “volt-second balance”), 154 (“Utilization of the transformer core and windings is essentially the same as in the full-bridge,” which is discussed above with respect to Ericsson-BMR, *see* §VI.A.1.f), Fig. 6.21 (showing symmetric wave forms), Fig. 6.18; EX1010 at, *e.g.*, 11:44-51; EX1012 at Figs. 2 and 3 (equal $I_o/2$ current on top and bottom); Ground I, Claim 1 (discussion regarding not saturating the transformer). Because top-side MOSFETs 8a and 8c (*i.e.*, power semiconductors from the first set) would be subjected to equal or at least approximately equal voltage, current, and power cycles over time as identical bottom-side MOSFETs 8b and 8d (*i.e.*, power semiconductor devices from the second set), a POSITA would have expected them to dissipate power at levels P_t and P_b that were equal or at least approximately equal, for an open environment and configuration of Takeshima. *See* EX1002 ¶167; EX1015 at 9:19-23.

2. **Claim 2**

Takeshima renders obvious Claim 2. *See* EX1002 ¶¶168-170.

As shown in this annotated version of Figure 2, a plurality of power semiconductor devices in the first set (MOSFETs 8a and 8c) are each positioned on the top surface of the PCB in a position directly overlapping in one dimension the location of the plurality of power semiconductor devices in the second set (MOSFETs 8b and 8d⁶) that are positioned on the bottom side of the PCB:



See EX1010 at Fig. 2 (annotated, cropped). Takeshima further teaches that “MOSFETs 8a and 8b ... are arranged in the vicinity of a connecting terminal,” and further teaches that “10a and 10b are arranged in the vicinity of a connecting terminal, not particularly shown in the figure.” See EX1010 at 10:51-66. A POSITA would therefore have understood, or at least have found obvious, that the MOSFETs

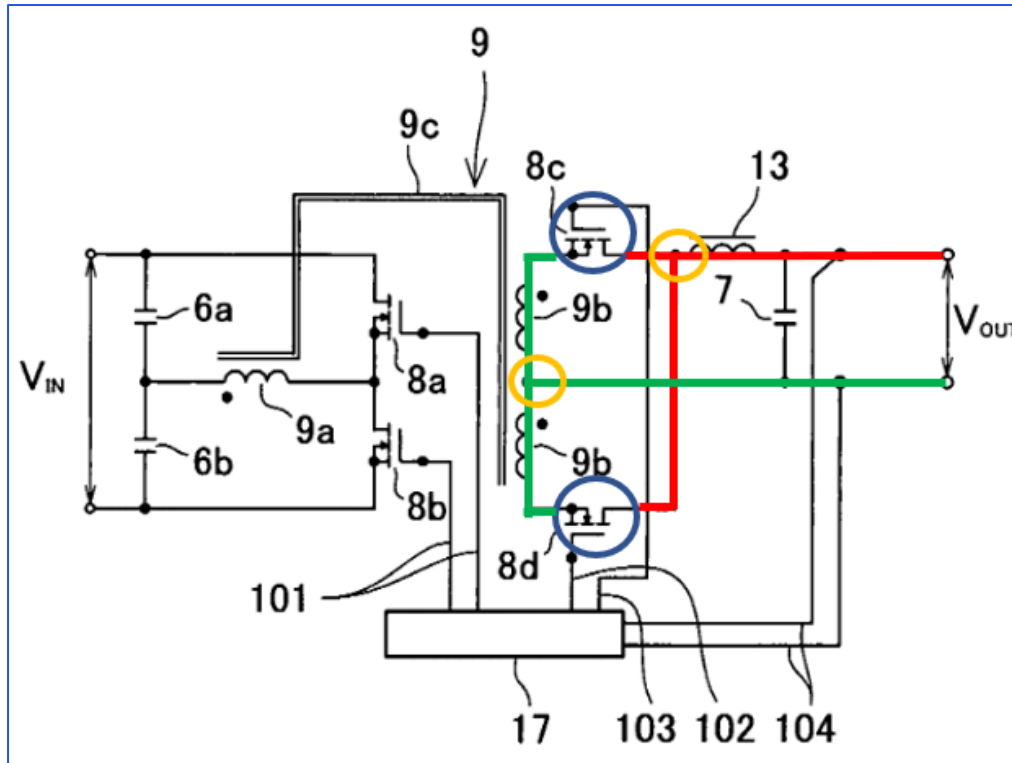
⁶ As discussed in Claim 1, in the asserted embodiment of Takeshima, diodes 10a and 10b in Takeshima’s Figure 2 have been replaced with MOSFET switches 8c and 8d in Takeshima’s Figure 14.

8a and 8b, and also 8c and 8d (which, again, replace 10a and 10b in the figure above) would also have directly overlapped in the second dimension, including because each pair is taught to be “in the vicinity” of the same connecting object, and further because it would make manufacturing simpler if the same optimized layout were used on both sides of the PCB, rather than having to optimize multiple different layouts for top and bottom sides of the PCB, and further because it was common to directly overlap related components in this manner. *See* EX1002 ¶¶170; *see also, e.g.*, EX1007 at 24; EX1009 at Fig. 9A-B.

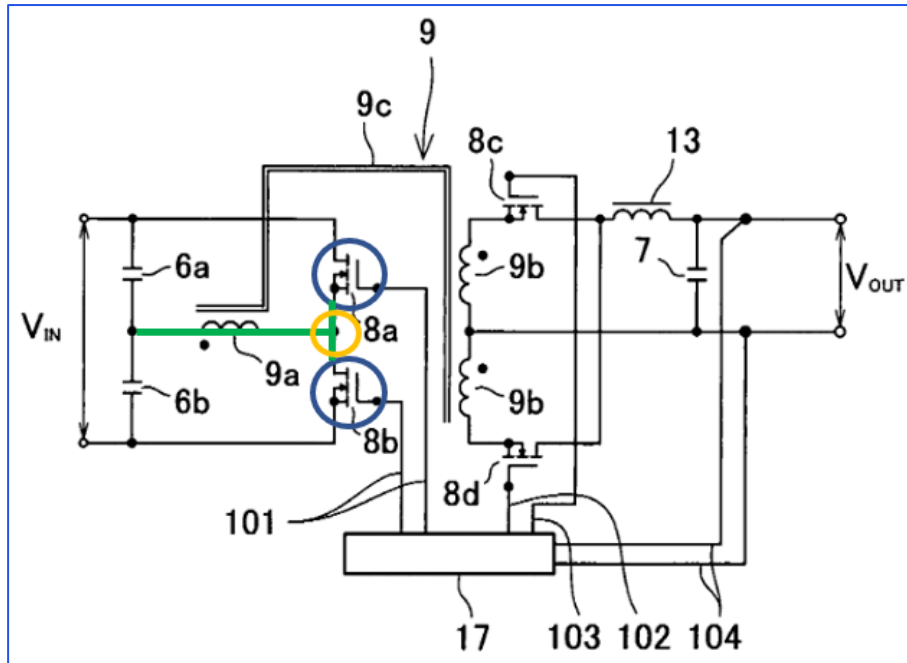
3. **Claim 3**

Takeshima renders obvious Claim 3. *See* EX1002 ¶¶171-173.

Takeshima’s half-bridge circuit shows that MOSFETs 8c on the top of the PCB and 8d on the bottom of the PCB (both circled in blue) would share respective vias because they connect (circled in orange) to the same output lines (highlighted in red and green), as shown here in annotated Figure 14:



See EX1010 at Fig. 14 (annotated), 19:29-32 (“The drain terminals of the MOSFETs 8c and 8d are connected to each other and further connected to one terminal (input side) of the inductance 13.”). Because MOSFETs 8c and 8d are on opposite sides of the PCB, a POSITA would have recognized and found obvious that they would be electrically connected using a respective set of conductive vias, because vias are used to connect components on different layers of a PCB. See EX1002 ¶173. Similarly, MOSFETs 8a and 8b (circled in blue) on the top and bottom of the PCB, respectively, also share (circled in orange) their respective via to element 9a (path highlighted in green), such that a plurality of semiconductor devices on the top side of the PCB (8a and 8c) share their respective vias with corresponding semiconductor devices on the bottom side of the PCB (8b and 8d, respectively):



See EX1010 at Fig. 14 (annotated); *see also* EX1010 at 15:56-64.

4. Claim 4

Takeshima renders obvious Claim 4. *See* EX1002 ¶¶174-178.

As background, Takeshima teaches as follows:

[1] It is possible to employ a configuration of a switching power supply device 300 as illustrated in FIG. 8, in which *two sets of power modules 18* and smoothing circuits are provided on a single main printed circuit board 1. Alternatively, although not particularly shown in the drawings, it is possible to employ a configuration in which *two sets of power modules 18 are integrated into a single component* and arranged, as a set of power module, on a main printed circuit board 1. In other words, the advantageous effects of the present invention can be

obtained equally in *various embodiments*, irrespective of the number of power modules 18 mounted on the main printed circuit board 1 or the number of circuits formed thereon.

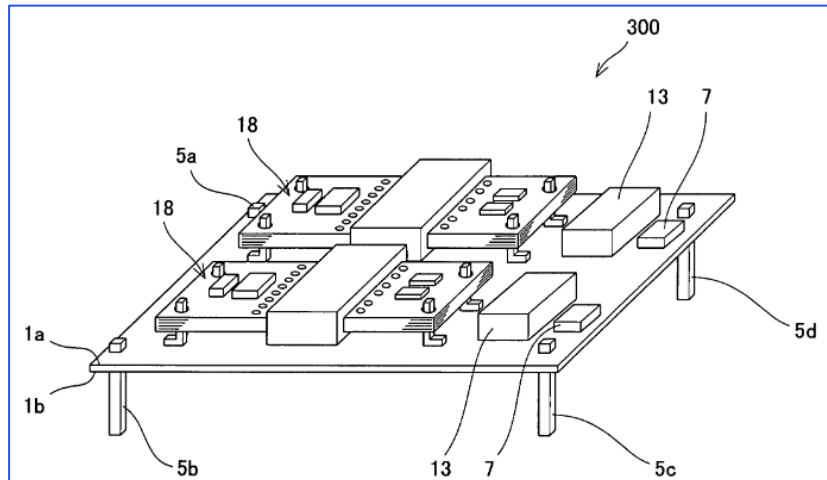


Fig. 8

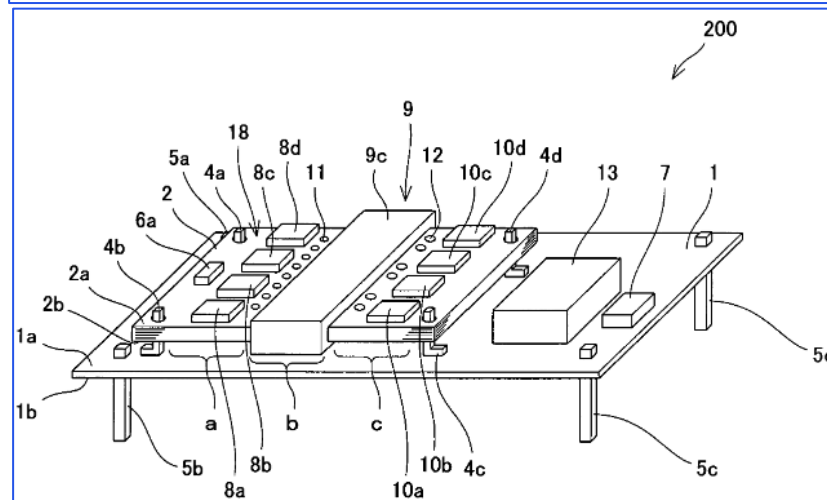


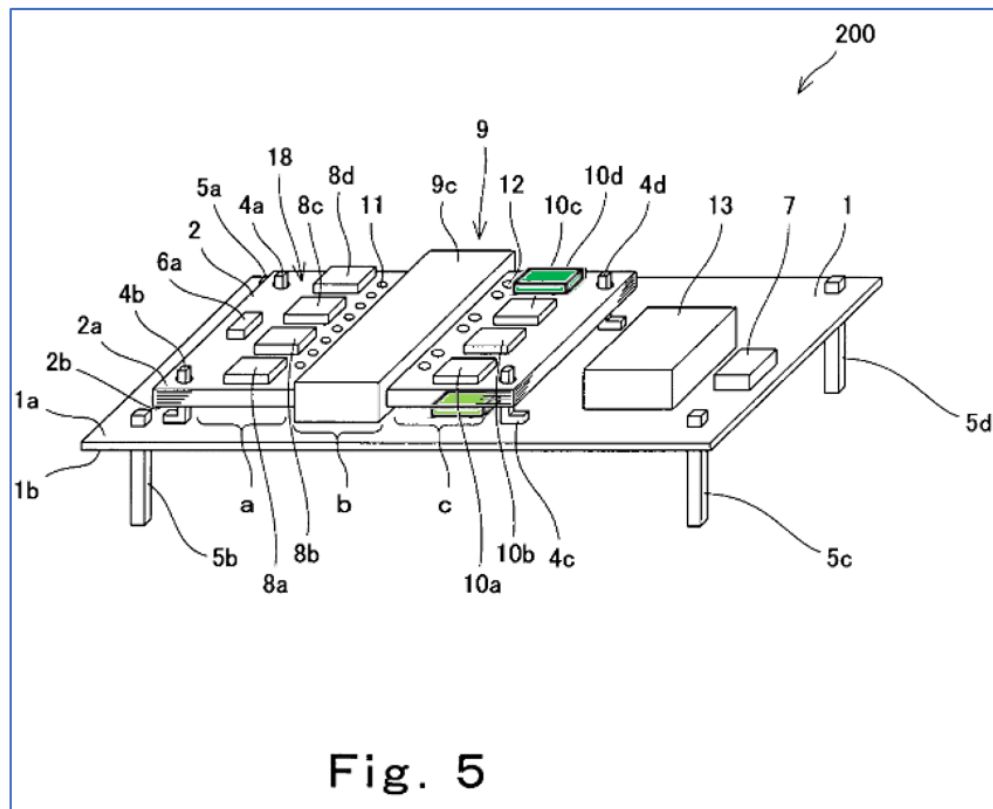
Fig. 5

See EX1010 at 14:60-15:8, Figs. 5 and 8. Takeshima thus teaches that the power converter discussed above in the context of Claims 1 and 2 (in the Figure 2 layout with Figure 14 half-bridge circuitry) would obviously have been mirrored with a second such power converter (as in Figure 8 above) and further that it would obviously have been integrated onto the same PCB 102 as shown in Figure 5 above. *See also* EX1010 at 11:44-51; EX1023 ¶¶51-52 (“symmetrical positions” and wiring patterns that “are substantially the same” are “desirable”); §VI.C.4 (additional reasons a POSITA would have been motivated to mirror Takeshima’s cell). Each of those power converters is a repeatable cell unit that share the same circuit topology and each include MOSFETs on each of the top and bottom sides of the PCB, in accordance with Claim 1[d]. Each cell also has its MOSFET components arranged in a pattern, and that pattern of components would be substantially a mirror image of the pattern of components in the other cell, as Takeshima teaches as shown above to mirror individual converter units. *See also* EX1010 at 7:47-50, 11:44-51 14:44-48, 14:56-59, Figs. 1-2, 7, 14 (additional teachings motivating a mirrored layout with an arranged pattern in accordance with this element).

5. **Claim 5**

Takeshima renders obvious Claim 5. *See* EX1002 ¶¶179-181. For example, as shown in this annotated version of Takeshima Figure 5 (which is analogous to the mirrored layout asserted herein that Takeshima teaches is “not particularly shown in

the drawings”⁷), Takeshima’s converter would be mirrored such that, for example, the dark-green-highlighted MOSFET on the top side of the top cell on the top half of the figure is on an opposite surface of the corresponding light-green-highlighted MOSFET that would be on the bottom side of the bottom cell on the bottom half of the figure (and which was not visible in the original figure because it is on the bottom side and was therefore added here to illustrate):



See EX1010 at Fig. 5 (annotated). This results from the fact that, in the asserted embodiment of Takeshima (Figure 2’s cell with Figure 14’s half-bridge circuit,

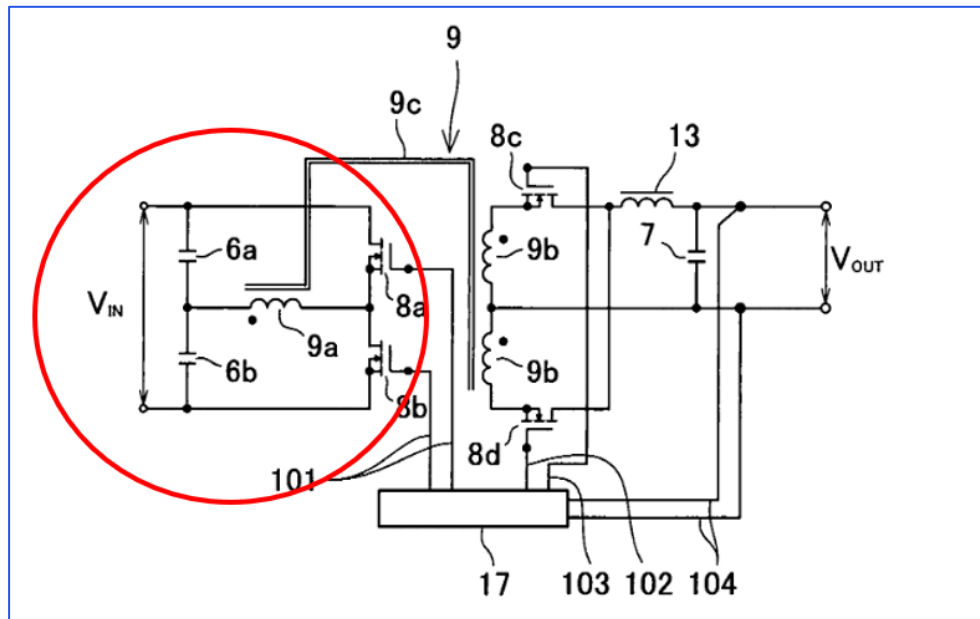
⁷ See EX1010 at 14:60-15:8.

mirrored as taught by Takeshima at 14:60-15:8 and Figures 5 and 8), the two cells are the same and they both have MOSFETs on the top and bottom surfaces of the PCB but are mirrored as discussed herein and as motivated by Takeshima itself. *See also* EX1010 at 14:60-15:8, Figs. 5 and 8.

6. **Claim 6**

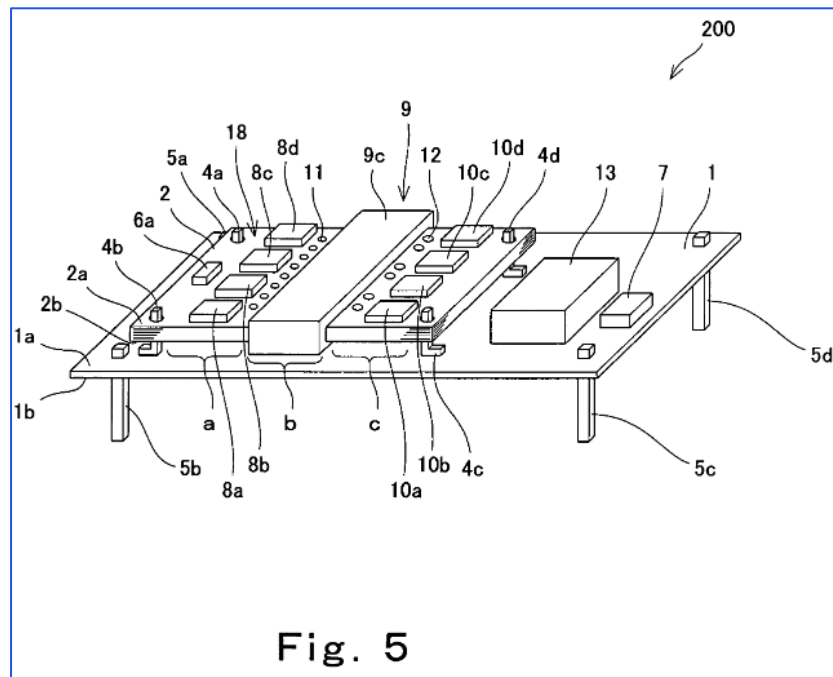
Takeshima renders obvious Claim 6. *See* EX1002 ¶¶182-184.

Takeshima refers to “primary-side inverter region a” in Figure 1, which would correspond to the input side of the converter circled here in red from Takeshima’s annotated Figure 14 (the applicable circuit in this Ground):



EX1010 at Fig. 14 (annotated), 9:60-61. Portions within that “primary-side inverter region a” comprise an input cell, including because they comprise repeatable units that take the input voltage that is input into the power converter, as shown above by

“ V_{IN} ”. See EX1002 ¶184; EX1010 at 9:60-61. In the asserted embodiment, the overall power converter that is mirrored (as taught in Takeshima at 14:60-15:8) is a cell, and therefore the cell comprises an input cell. The input cell portion of the cell would be on the primary-side inverter region, analogously illustrated in Takeshima’s Figure 5:

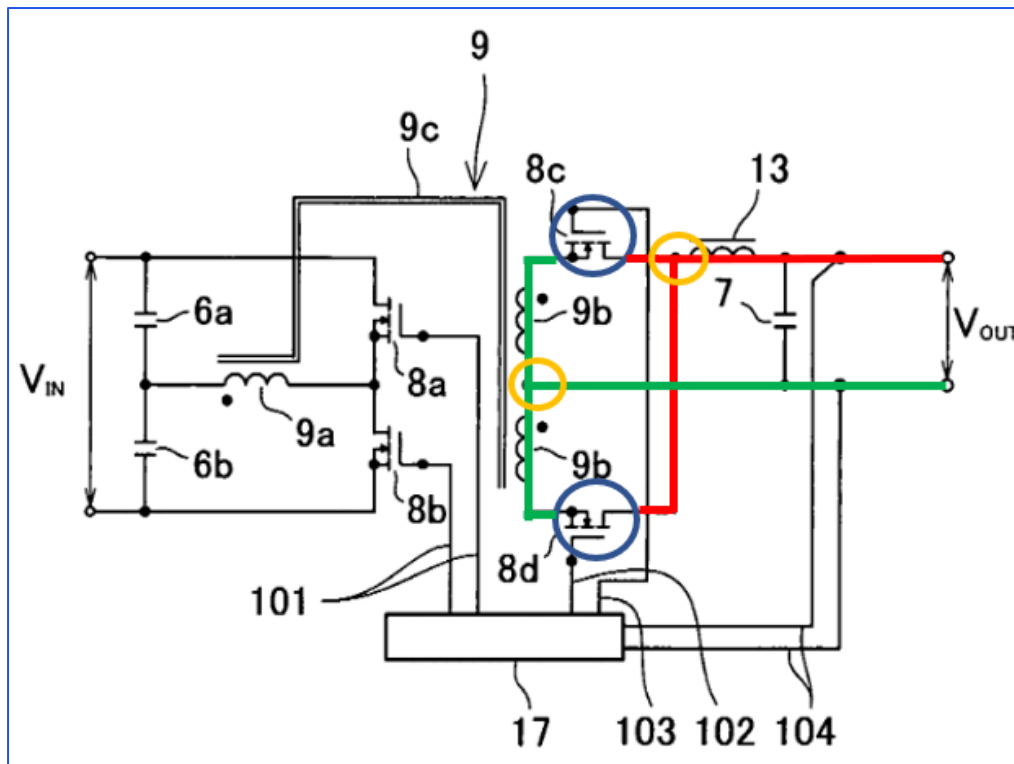


See EX1010 at Fig. 5.

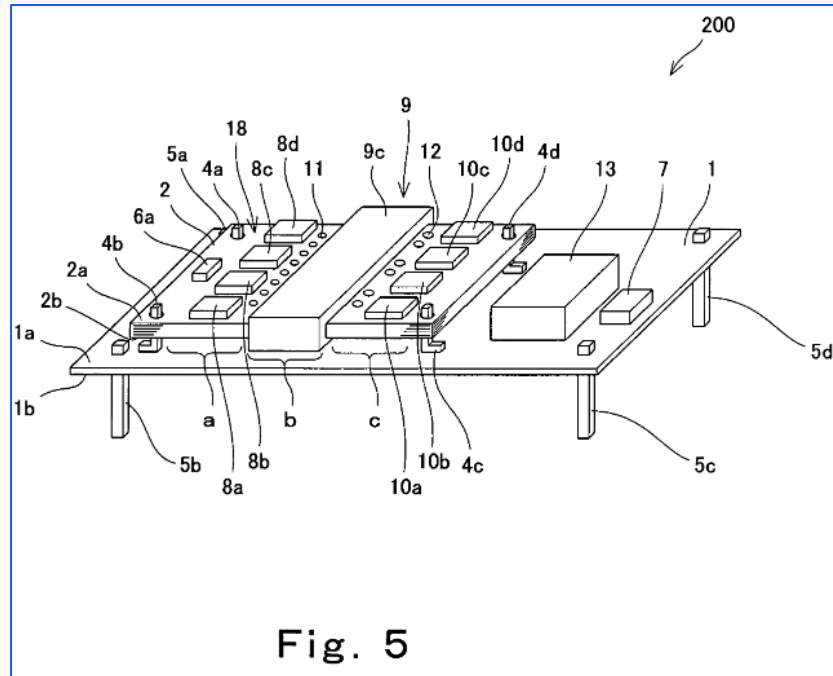
7. **Claim 7**

Takeshima renders obvious Claim 7. See EX1002 ¶¶185-187.

By reference again to the picture from Claim 3, power semiconductor devices that share their respective vias include 8c and 8d (circled in blue), which are MOSFET switches on the secondary winding side of the transformer, which is why they are connected to “ V_{OUT} ”:



See EX1010 at Fig. 14 (annotated), 19:36-37 (“A direct current voltage V_{OUT} is output from both ends of the output...”), 19:24-29. A POSITA would have recognized those symbols as the symbols for switches, and that they are responsible for the output of the transformer and are output switches. See EX1002 ¶187; EX1008 at, e.g., Fig. 2.13(b). The output switches would be on the “secondary-side rectification region c,” analogously illustrated in Takeshima’s Figure 5:



See EX1010 at 9:59-62, Fig. 5.

E. Ground V: Claims 1-7 Are Rendered Obvious by Takeshima in View of Spiazzi.

1. Claim 1

Claim 1 is rendered obvious by Takeshima in view of Spiazzi. See EX1002 ¶¶188-198.

a. 1[preamble]

Claim 1[preamble] is rendered obvious by Takeshima in view of Spiazzi. See §VI.D.1.a; EX1002 ¶189.

b. 1[a]

Claim 1[a] is rendered obvious by Takeshima in view of Spiazzi. See §VI.D.1.b; EX1002 ¶190.

c. 1[b]

Claim 1[b] is rendered obvious by Takeshima in view of Spiazzi. *See* §VI.D.1.c; EX1002 ¶191.

d. 1[c]

Claim 1[c] is rendered obvious by Takeshima in view of Spiazzi. *See* §VI.D.1.d; EX1002 ¶192.

e. 1[d]

Claim 1[d] is rendered obvious by Takeshima in view of Spiazzi. *See* §VI.D.1.e; EX1002 ¶193.

f. 1[e]

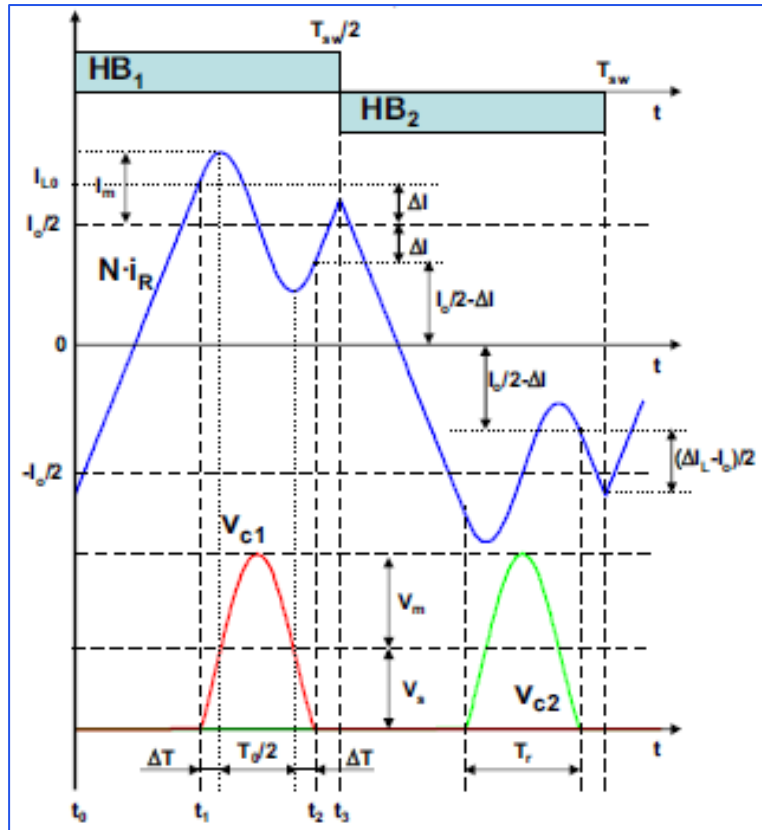
Takeshima and Spiazzi render this limitation obvious. *See* §VI.D.1.f; EX1002 ¶¶194-198.

As discussed above in Ground IV, Takeshima's half-bridge circuit would be powered over time with equal (or at least approximately equal) power on the top and bottom of the printed circuit board, such that a POSITA would have expected equal (or at least approximately equal) power dissipation levels P_t and P_b . *See* §VI.D.1.f. In combining Takeshima with Spiazzi in Spiazzi's environment, this result is confirmed, as explained below. *See* EX1002 ¶195.

Spiazzi teaches a half-bridge converter, similar to Takeshima's half-bridge converter circuit in Takeshima Figure 14. *See* EX1011 at Fig. 1.a ("half-bridge resonant VRM"). Spiazzi then performs a thermal mapping of two different

configurations of its power converter, and shows the top sides of the two different configurations in Figure 11. *See* EX1011 at 2000. Although only the top sides of the two different configurations are shown, Spiazzi teaches that “[s]*imilar results* were obtained for the downward surfaces.” *See* EX1011 at 1999. A POSITA would therefore have recognized that, when the portions of Takeshima converter relied upon in the asserted embodiment are operated in the environment of Spiazzi, the power dissipation levels P_t and P_b would indeed at least be “similar” and well within 150% of each other. *See id.*

A POSITA would have expected this result in Spiazzi’s environment because, as with Takeshima’s half-bridge converter, Spiazzi expressly recognizes that its half-bridge converter should be powered with equal current, voltage, and power on the top and bottom MOSFET switches. This is shown, for example, by the equal magnitude and width voltage curves and the equal (but inverted) current curve in the HB_1 and HB_2 phases (corresponding to top Q1 MOSFETs and bottom Q2 MOSFETs) shown in Spiazzi’s Figure 1.b:



See EX1011 at Fig. 1.b. Likewise, Spiazzi is a thermal analysis of the half-bridge power converter circuit described in EX1012⁸, which teaches regarding its circuit: “During the negative half cycle of a switching period T_{sw} , the behavior of the circuit **is the same** as during the positive half cycle. The only difference is that switches Q_1 and Q_2 change roles.” See EX1012 at 82; see also, e.g., EX1012 at Fig. 1. As a result, a POSITA would have expected equal power cycles over time on the top and bottom of the same sets of MOSFET components and, as a result, equal or at least

⁸ See EX1011 at 1993, 2000 (reference [1]).

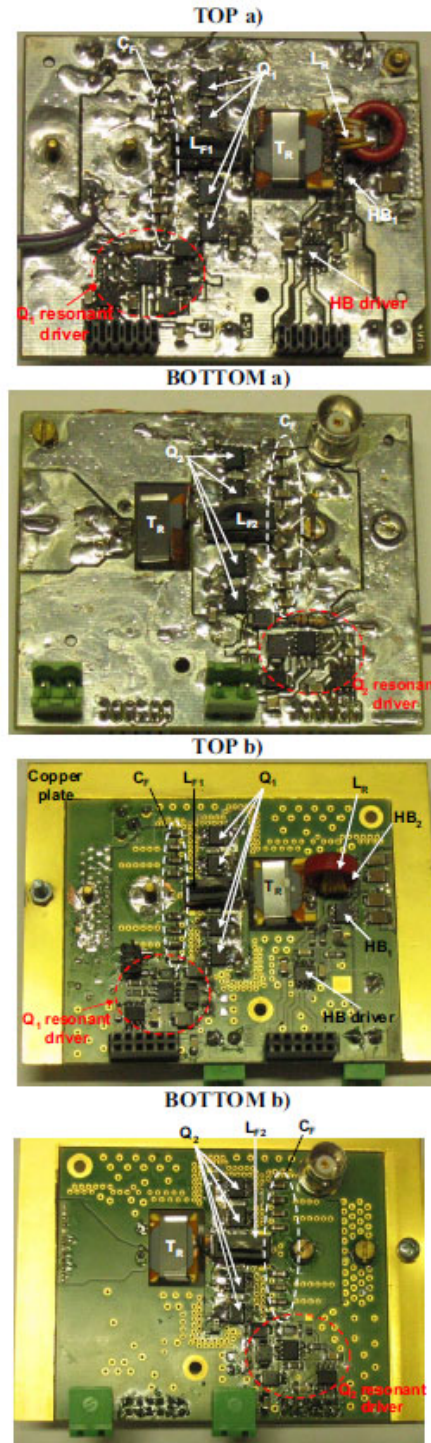
approximately equal power dissipation levels P_t and P_b on top and bottom. *See* EX1002 ¶¶195-198.

A POSITA would further have been motivated to create this combination because of the well-known benefits of addressing excess heat. *See, e.g.*, EX1023 ¶¶51-52 (“symmetrical positions” and “desirable” wiring patterns that “are substantially the same” allows for “heat generated from the semiconductor devices [to] be efficiently radiated through [] both sides of the power module” and provides for “longer life duration” of the power module).

2. **Claim 2**

Takeshima and Spiazzi render obvious Claim 2. *See* §VI.D.2; EX1002 ¶¶199-201.

As discussed above, Takeshima expressly shows direct overlap of MOSFET components in one dimension, and teaches or at least renders obvious that they would also overlap in the second dimension. See EX1010 at Fig. 2, 10:51-67. To the extent there was any doubt that Takeshima's MOSFETs would at least obviously have directly overlapped in that second dimension, such overlap would have been further motivated by virtue of Spiazzi's teachings as to the layout of MOSFET switches on the top and bottom of the PCB, as visual inspection of Spiazzi's two PCBs shows the two-dimensional overlap between the four MOSFETs on the top side of each PCB (Q1) and the corresponding set of four MOSFETs on the bottom side of each respective PCB (Q2). Such layouts were common and expected to a POSITA. See EX1002 ¶201; EX1011 at Fig. 5.



3. **Claim 3**

Claim 3 is rendered obvious by Takeshima in view of Spiazzi. *See* §VI.D.3; EX1002 ¶202.

4. **Claim 4**

Claim 4 is rendered obvious by Takeshima in view of Spiazzi. *See* §VI.D.4; EX1002 ¶203.

5. **Claim 5**

Claim 5 is rendered obvious by Takeshima in view of Spiazzi. *See* §VI.D.5; EX1002 ¶204.

6. **Claim 6**

Claim 6 is rendered obvious by Takeshima in view of Spiazzi. *See* §VI.D.6; EX1002 ¶205.

7. **Claim 7**

Claim 7 is rendered obvious by Takeshima in view of Spiazzi. *See* §VI.D.7; EX1002 ¶206.

F. Ground VI: Claims 1-7 Are Rendered Obvious By Takeshima In View Of Wanes

1. **Claim 1**

Claim 1 is rendered obvious by Takeshima in view of Wanes. *See* EX1002 ¶¶207-213.

a. 1/[preamble]

Claim 1[preamble] is rendered obvious by Takeshima in view of Wanes. *See* §VI.D.1.a; EX1002 ¶208.

b. 1/[a]

Claim 1[a] is rendered obvious by Takeshima in view of Wanes. *See* §VI.D.1.b; EX1002 ¶209.

c. 1/[b]

Claim 1[b] is rendered obvious by Takeshima in view of Wanes. *See* §VI.D.1.c; EX1002 ¶210.

d. 1/[c]

Claim 1[c] is rendered obvious by Takeshima in view of Wanes. *See* §VI.D.1.d; EX1002 ¶211.

e. 1/[d]

Claim 1[d] is rendered obvious by Takeshima in view of Wanes. *See* §VI.D.1.e; EX1002 ¶212.

f. 1/[e]

Claim 1[e] is rendered obvious by Takeshima in view of Wanes. *See* §VI.D.1.f; EX1002 ¶213. In the asserted embodiment, Takeshima's module is in the environment of Wanes, thus confirming equal or at least approximately equal power dissipation and thus satisfying this element. *See* EX1011 at 1999 ("Similar results

were obtained for the downward surfaces” when powering half-bridge circuits (such as that taught by Takeshima) similarly on top and bottom).

2. **Claim 2**

Takeshima in view of Wanes renders obvious Claim 2. *See* EX1002 ¶¶214-216.

Takeshima shows direct overlap in one dimension and teaches or at least renders obvious the overlap in the second dimension. *See* §VI.D.2. To the extent there is any doubt about the two-dimensional overlap of Takeshima’s relevant MOSFET components, Wanes renders such overlap obvious, as shown, for example, in Wanes’s Figures 1A and 9A-B. *See* EX1009 at Figs. 1A, 9A-B; §VI.C.4. A POSITA would have been motivated to apply, and had a reasonable expectation of success in applying, Wanes’s teachings of overlap to Takeshima because Takeshima already contemplates such overlap, and further because such layouts were common and expected to a POSITA. *See* EX1002 ¶216.

3. **Claim 3**

Claim 3 is rendered obvious by Takeshima in view of Wanes. *See* §VI.D.3; EX1002 ¶217.

4. **Claim 4**

Claim 4 is rendered obvious by Takeshima in view of Wanes. *See* §VI.D.4; EX1002 ¶218. Wanes confirms how a POSITA would have been motivated to apply, and had a reasonable expectation of success in applying, its teachings of mirroring

in a manner that Takeshima contemplates could be applied to its modules. *See* §VI.C.4; EX1010 at 14:60-15:8, Fig. 8; EX1002 ¶218.

5. **Claim 5**

Claim 5 is rendered obvious by Takeshima in view of Wanes. *See* §VI.D.4-VI.D.5; EX1002 ¶219. In this Ground, Takeshima's module is mirrored such that a component from the first cell that is mirrored would be located on an opposite surface of a respective components from the second, mirrored cells, as Wanes teaches to mirror. *See id.*

6. **Claim 6**

Claim 6 is rendered obvious by Takeshima in view of Wanes. *See* §VI.D.6; EX1002 ¶220.

7. **Claim 7**

Claim 7 is rendered obvious by Takeshima in view of Wanes. *See* §VI.D.7; EX1002 ¶221.

G. Ground VII: Claim 1-7 Are Rendered Obvious By Ericsson-BMR In View Of Takeshima, Or, Alternatively, By BMR-2008 In View Of Takeshima

1. **Claim 1**

Claim 1 is rendered obvious by Ericsson-BMR in view of Takeshima. *See* EX1002 ¶¶222-229.

a. 1[preamble]

Claim 1[preamble] is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VI.A.1.a; EX1002 ¶223.

b. 1[a]

Claim 1[a] is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VI.A.1.b; EX1002 ¶224.

c. 1[b]

Claim 1[b] is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VI.A.1.c; EX1002 ¶225.

d. 1[c]

Claim 1[c] is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VI.A.1.d; EX1002 ¶¶226-227. If Ericsson-BMR is found to have not taught, or at least rendered obvious, that the windings of the transformer are formed by traces in one or more of the conductive layers of the PCB, Takeshima teaches this, and a POSITA would have been motivated to form, and had a reasonable expectation of success in forming, Ericsson-BMR's windings in this manner for a number of reasons, including because it was well known to be more space efficient and further because, as discussed above, Ericsson-BMR does not provide for the traces to be anywhere but in the PCB. *See* §VI.D.1.d; §VI.C.1.d; EX1002 ¶227.

e. 1[d]

Claim 1[d] is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VI.A.1.e; EX1002 ¶228. Takeshima further confirms that Ericsson's output FETS⁹ could have been those that are placed symmetrically and that it would have been an obvious design choice for the output FETs used as output switches by Ericsson-BMR. *See* §VI.D.1.e; EX1002 ¶228.

f. 1[e]

Claim 1[e] is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VI.A.1.f; EX1002 ¶229.

2. **Claim 2**

Claim 2 is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VI.A.2; EX1002 ¶230.

3. **Claim 3**

Claim 3 is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VI.A.3; EX1002 ¶231.

4. **Claim 4**

Claim 4 is rendered obvious by Ericsson-BMR in view of Takeshima. *See* EX1002 ¶¶232-233. Takeshima teaches mirroring, so a POSITA would have been

⁹ For clarity, Ericsson's full-bridge circuit topology is still relied on in this Ground.

motivated to mirror, and had a reasonable expectation of success in mirroring, Ericsson-BMR's power modules in that manner and for the same reason that a POSITA would have found it obvious to mirror Takeshima's own power module. *See* §VI.D.4; EX1002 ¶233.

5. **Claim 5**

Claim 5 is rendered obvious by Ericsson-BMR in view of Takeshima, in the asserted embodiment where Ericsson-BMR's module is mirrored as taught by Takeshima. *See* §VI.A.5; § VI.D.5; EX1002 ¶¶234.

6. **Claim 6**

Claim 6 is rendered obvious by Ericsson-BMR in view of Takeshima, in the asserted embodiment where Ericsson-BMR's components (which comprises input cells) are mirrored as taught by Takeshima. *See* §VI.C.6; §§VI.D.4-VI.D.6; EX1002 ¶235.

7. **Claim 7**

Claim 7 is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VI.A.6; EX1002 ¶236.

8. **BMR-2008**

As noted above, the relevant teachings of BMR-2008 are substantially the same as the relevant teachings of Ericsson-BMR. *Compare* EX1007 at, *e.g.*, 1, 2, 5, 24, 31 *with* EX1026 at, *e.g.*, 1, 4, 13, 15, 20. As a result, Claims 1-7 are rendered obvious by BMR-2008 in view of Takeshima for the same reasons as they are

rendered obvious by Ericsson-BMR in view of Takeshima as set forth in above. *See* EX1002 ¶¶237-238.

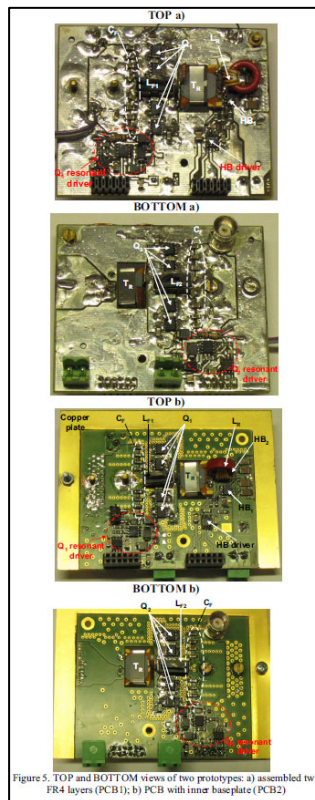
H. Ground VIII: Claims 1-7 Are Rendered Obvious By Spiazzi In View Of Wanes

1. **Claim 1**

Claim 1 is rendered obvious by Spiazzi in view of Wanes. *See* EX1002 ¶¶239-255.

a. *l[preamble]*

Claim 1[preamble] is rendered obvious by Spiazzi in view of Wanes. *See* EX1002 ¶¶ 240-241. Spiazzi teaches an apparatus, which can be seen, for example, in Figure 5:



EX1011 at Fig. 5 (annotations in original).

b. 1[a]

Claim 1[a] is rendered obvious by Spiazzi in view of Wanes. *See* EX1002 ¶¶242-243.

Spiazzi teaches a power converter, which it refers to as a Voltage Regulator Module (VRM). *See* EX1011 at 1993 (“High frequency dc-dc converters for Voltage Regulator Module (VRM) applications require a great attention on the physical realization....”); *see also id.* at 2000 (“In this paper, practical issues regarding the physical realization of a 1.8 MHz VRM described in [1] have been discussed in detail.”).

c. 1[b]

Claim 1[b] is rendered obvious by Spiazzi in view of Wanes. *See* EX1002 ¶¶244-245.

Spiazzi teaches that the power converter shown in Figure 5(a) is a “three layer PCB” while the power converter shown in Figure 5(b) is a PCB “built assembling two epoxy layers ... on both sides of 0.7 mm thick copper baseplate....” *See* EX1011 at 1995. The top and bottom surfaces of each PCB are visible in Figure 5:

EX1011 at Fig. 5 (annotations in original). As a POSITA would have recognized, at least the top and bottom layers of these PCBs are conductive, as that conductivity is what permits the electric components mounted thereon to interact with each other. Moreover, a POSITA would have known and found obvious that there are and would

obviously be an additional plurality of additional conductive layers, as taught by Spiazzi and Wanes, including because such plurality was common and would be used for additional purposes, such as planar magnetics windings. *See* EX1009 at 4:33-34 (“primary windings are embedded in internal tracks in internal *layers* in PCB 104.”).

d. 1[c]

Claim 1[c] is rendered obvious by Spiazzi in view of Wanes. *See* EX1002 ¶¶246-249.

Spiazzi teaches a magnetic core structure that is magnetically coupled to windings. *See* EX1011 at, *e.g.*, 1994 (“The core employed was a planar ER 14.5/3/7 3F4 material from Ferroxcube and the windings [were] constructed by” the following process.).

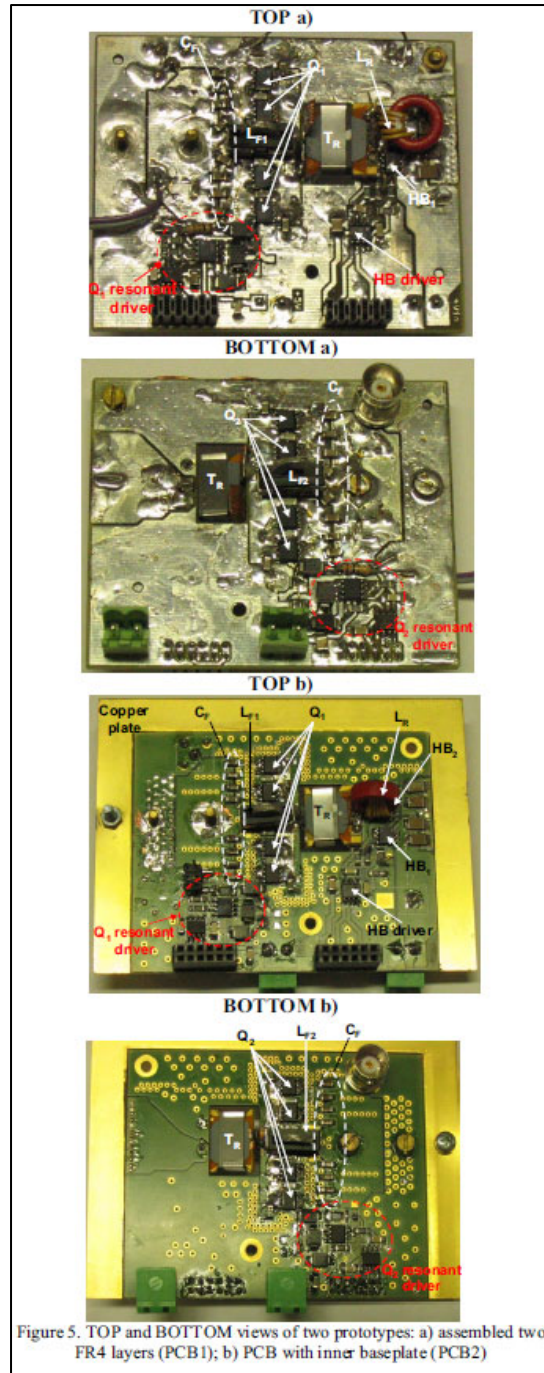
Spiazzi’s windings are not formed by traces in one or more of the conductive layers in the PCB. However, Wanes does teach the layout approach of using the converter PCB to form windings. *See* EX1009 at 4:10-12, 4:31-48 (“primary windings are embedded ... in internal layers in PCB **104**,” where element 104 is the PCB), 9:44-51 (“Windings (not shown) are sandwiched within each PCB and encircle openings 414 and 416. Each winding of PCB 104 co-operates with a respective winding of the magnetics of transformer 112 and inductor 114....”). A POSITA would have been motivated to form Spiazzi’s windings in the manner

described in Wanes for a number of reasons. *See* EX1002 ¶249. For example, forming windings as traces in the conductive layers was a well-known technique in the art (*see, e.g.*, EX1019 at 1:54-60) and it was known to be space efficient, so forming the traces in that manner would have been obvious to a POSITA, particularly as a layout used for R&D was moving towards potential commercialization. *See id.* Spiazzi is a research paper exploring “layout-dependent” issues affecting the “[p]ractical realization” of power converters, so Spiazzi obviously would have been motivated to investigate this common method of laying out windings given the well-known advantages. *See* EX1011 at 1993.

e. 1[d]

Claim 1[d] is rendered obvious by Spiazzi in view of Wanes. *See* EX1002 ¶¶250-251.

Spiazzi’s Figure 5 shows a set of four MOSFETs labelled Q_1 that are mounted on the top surface of the PCB and are overlapping with a set of four MOSFETs labelled Q_2 mounted on the bottom surface of the PCB:



EX1011 at Fig. 5 (annotations in original). Q_1 on these PCBs are each a first set of power semiconductor devices mounted on the top surface and electrically connected to dissipate power at a level, P_t , during operation of the converter, while Q_2 on these PCBs are each a second set of power semiconductor devices being mounted on the

bottom surface of the PCBs and electrically connected to dissipate power at a level, Pb, during operation of the converter. *See* EX1002 ¶251.

f. 1[e]

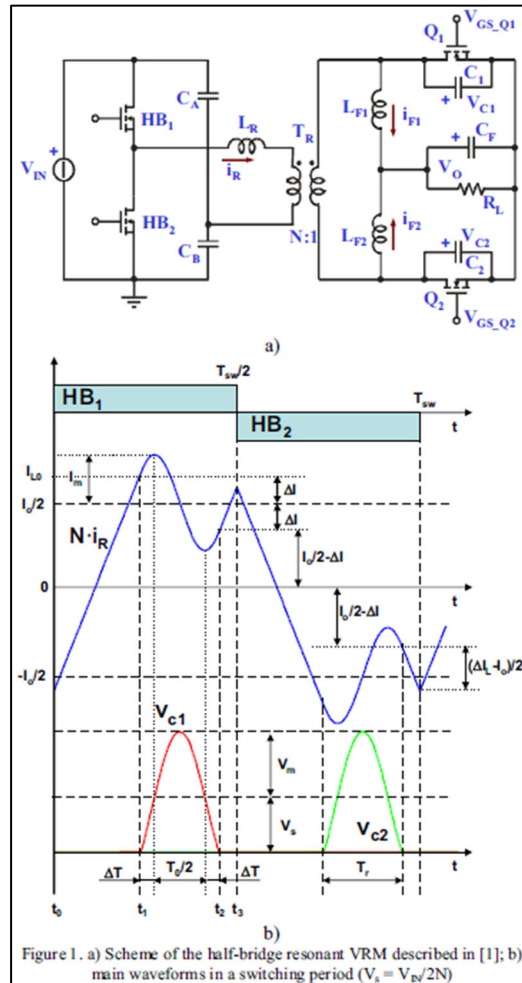
Claim 1[e] is rendered obvious by Spiazzi in view of Wanes. *See* EX1002 ¶¶252-255.

Spiazzi performs a thermal mapping of two different configurations of its power converter, and shows the top sides of the two different configurations in Figure 11. *See* EX1011 at 2000. Although only the top sides of the two different configurations are shown, Spiazzi teaches that “[s]imilar results were obtained for the downward surfaces.” *See* EX1011 at 1999. A POSITA would therefore have recognized that, in Spiazzi, the power dissipation levels Pt and Pb would at least be “similar” and well within 150% of each other on top and bottom. *See id.*; EX1002 ¶253.

A POSITA would have expected this result in Spiazzi’s physical environment and configuration because Spiazzi expressly recognizes that its half-bridge converter¹⁰ should be powered with equal current, voltage, and power on the top and bottom MOSFETs, as shown, for example, by the equal magnitude and width

¹⁰ Spiazzi teaches a half-bridge converter. *See* EX1011 at Fig. 1.a (“half-bridge resonant VRM”).

voltage curves as well as the equal (but inverted) current curve in the HB₁ and HB₂ phases (corresponding to top Q₁ MOSFETs and bottom Q₂ MOSFETs) shown in Spiazzi's Figure 1.b:



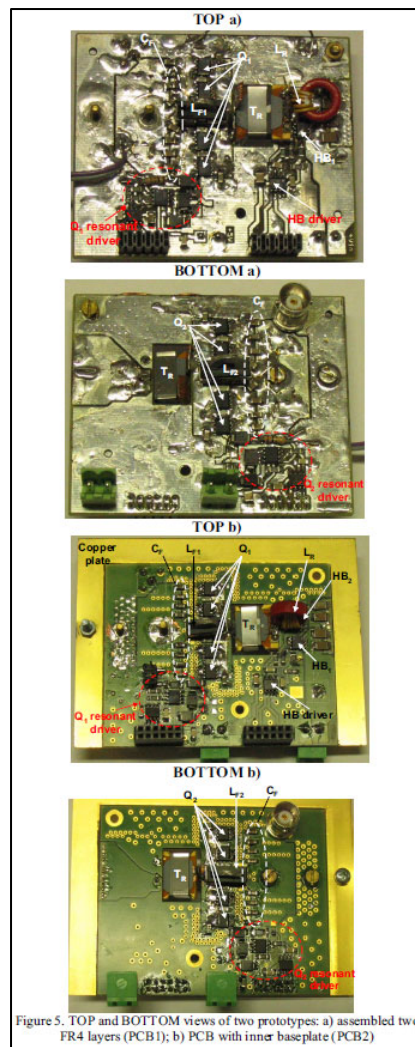
See EX1011 at Fig. 1.b; EX1002 ¶254. As noted above in §VI.E.1.f, Spiazzi is a thermal analysis of the power converter circuit described in EX1012¹¹, which teaches regarding its circuit: “During the negative half cycle of a switching period

¹¹ See EX1011 at 1993, 2000 (reference [1]).

T_{sw} , the behavior of the circuit *is the same* as during the positive half cycle. The only difference is that switches Q_1 and Q_2 change roles.” See EX1012 at 82; see also, e.g., EX1012 at Fig. 1.

2. Claim 2

Claim 2 is rendered obvious by Spiazzi in view of Wanes. See EX1002 ¶256. As can be seen in Figure 5, the plurality of power semiconductor devices in Q_1 of each PCB are each positioned in a location on the top surface that overlap the location on the bottom surface occupied by the power semiconductor devices in Q_2 :

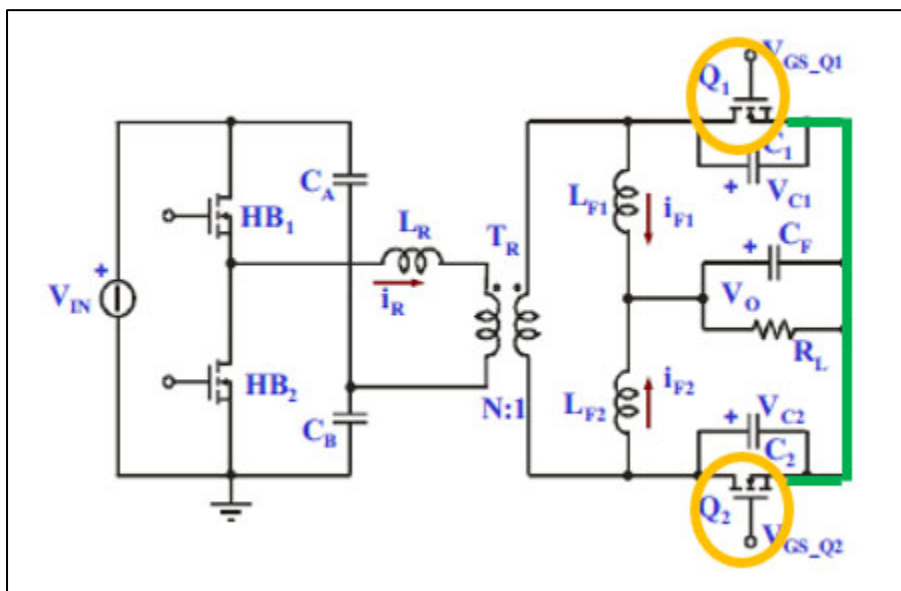


EX1011 at Fig. 5 (annotations in original).

3. **Claim 3**

Claim 3 is rendered obvious by Spiazzi in view of Wanes. See EX1002 ¶¶257-258.

As highlighted in green in this annotated version of Spiazzi's Figure 1(a), Spiazzi teaches that the four power semiconductor devices on the top side of each board (Q_1) share a connection with the four power semiconductor devices on the bottom side of the respective board (Q_2):



EX1011 at Fig. 1(a) (annotated). As a POSITA would have recognized or at least found obvious, shared respective sets of conductive vias in the PCB would have been used to connect the power semiconductor devices in Q_1 and Q_2 , because Q_1 power semiconductor devices are on the top side of the PCBs and Q_2 power semiconductor devices are on the bottom side of the PCBs.

4. **Claim 4**

Claim 4 is rendered obvious by Spiazzi in view of Wanes. *See* EX1002 ¶¶259-260.

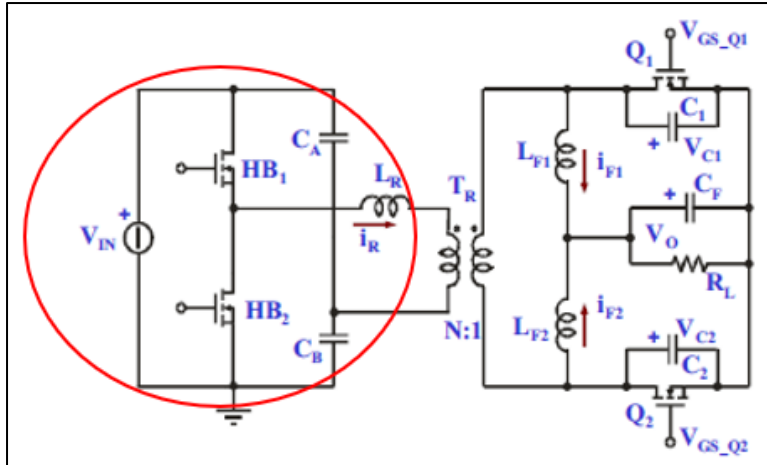
Each Spiazzi PCB can be considered in its entirety a repeatable cell, and Wanes teaches mirroring cells. *See* §VI.C.4. A POSITA would therefore have found it obvious, and had a reasonable expectation of success, in mirroring Spiazzi's cell for the same reasons as a POSITA would have found it obvious to mirror Ericsson-BMR's cell. *See* §VI.C.4; EX1002 ¶260.

5. **Claim 5**

Claim 5 is rendered obvious by Spiazzi in view of Wanes. *See* EX1002 ¶¶261-262. When Spiazzi's cells are mirrored as taught by Wanes, a component from the first cell would be located on an opposite surface of a respective component from the second cell, as a POSITA would have found obvious. *See* §VI.C.5; EX1002 ¶262.

6. **Claim 6**

Claim 6 is rendered obvious by Spiazzi in view of Wanes. *See* EX1002 ¶¶263-264. In this Ground, each Spiazzi converter is, in its entirety, considered a cell, and each converter is comprised of an input cell that receives an input voltage for regulation:



See EX1011 at Fig. 1(a) (annotated); EX1002 ¶264.

7. Claim 7

Claim 7 is rendered obvious by Spiazzi in view of Wanes. See EX1002 ¶¶265-266. Spiazzi teaches that Q_1 and Q_2 power semiconductor devices are “synchronous rectifier (SR) switches,” and they are used to regulate the output as shown in Spiazzi’s circuit diagram Figure 1(a). See EX1011 at 1993-1994; EX1002 ¶266.

VII. OBJECTIVE INDICIA

There are no objective indicia of non-obviousness with a provable nexus to the claimed invention that would impact the results of the analysis above. See EX1002 ¶¶267-274. Contrary to Patent Owner’s allegations, Petitioner did not copy Patent Owner’s power converters (nor has anyone else, to Petitioner’s knowledge), and there is no evidence that any purported success or praise of Patent Owner or its power converter modules has anything to do specifically with the technology claimed in the ’761 Patent.

VIII. NO DISCRETIONARY DENIAL

The Board should decline to exercise its discretion to deny institution of this Petition because the parallel district court case was stayed in its earliest stages, the Petition relies only on prior art not previously before the Examiner, and this is the first and only post-grant challenge to the '761 Patent.

IX. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1)

A. 37 C.F.R. §42.8(b)(1): Real Party-in-Interest

Delta Electronics, Inc. (“Petitioner”); and Delta Electronics (Americas), Ltd.; Delta Electronics (USA), Inc.; Cyntec Co., Ltd.; Delta Electronics (Thailand) Public Company Limited; and DET Logistics (USA) Corporation (collectively, “Delta”) are the real parties-in-interest.¹²

¹² The following entities are not real parties-in-interest but are being disclosed for transparency because they have also been, or may be, named as respondents in the related ITC investigation referenced in the Related Matters section: Hon Hai Precision Industry Co. Ltd.; Foxconn Industrial Internet Co. Ltd.; FII USA Inc.; Ingrasys Technology Inc.; Ingrasys Technology USA Inc.; Quanta Computer, Inc.; Quanta Computer USA Inc.; Quanta Cloud Technology, Inc.; Quanta Cloud Technology USA LLC; and QCH, Inc.

B. 37 C.F.R. §42.8(b)(2): Related Matters

The '761 Patent is the subject of ITC Investigation No. 337-TA-1370, filed July 12, 2023, and instituted on August 15, 2023. The '761 Patent is also the subject of Civil Action No. 2:23-CV-00323-JRG-RSP in the Eastern District of Texas, filed July 12, 2023, which was stayed less than two months after it was filed. This case may affect, or be affected by, decisions in the proceedings in the ITC and district court (and any related appeals) discussed above.

C. 37 C.F.R. §§ 42.8(b)(3) and (4): Counsel and Service Information

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Delta concurrently submits a Power of Attorney, 37 C.F.R. §42.10(b), and consents to electronic service directed to the following email address: 761_IPR_Delta@kirkland.com.

X. PAYMENT OF FEES UNDER 37 C.F.R. §42.103

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. 506092. Review of 7 claims is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition to be charged to the above-referenced deposit account.

XI. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies that the '761 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the claims on the grounds identified in this Petition. Petitioner certifies: (1) it is not the owner of the '761 Patent; (2) Petitioner (nor any real party-in-interest) has not filed a civil action challenging the validity of any claim of the '761 Patent; (3) Petitioner files this Petition within one year of the date it was served with a complaint asserting infringement of the '761 Patent; (4) estoppel provisions of 35 U.S.C. §315(e)(1) do not prohibit this IPR; and (5) this Petition is filed after the '761 Patent was granted.

XII. CONCLUSION

Petitioner requests cancellation of the Challenged Claims.

Petition for *Inter Partes* Review of U.S. Patent No. 9,516,761

Date: November 22, 2023

Respectfully submitted,

/Russell E. Levine/

Russell E. Levine, P.C. (Reg. No. 32,153)

KIRKLAND & ELLIS LLP

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Counsel for Petitioner

CLAIM LISTING

Claim Number	Claim Language
1[preamble]	An apparatus comprising:
1[a]	a power converter including
1[b]	a printed circuit board (“PCB”) comprising a plurality of conductive layers and having a top surface and a bottom surface;
1[c]	a magnetic core structure magnetically coupled to a winding formed by traces in one or more of the conductive layers in the PCB; and
1[d]	a plurality of power semiconductor devices, a first set of the power semiconductor devices being mounted on the top surface and electrically connected to dissipate power at a level, Pt, during operation of the converter, a second set of the power semiconductor devices being mounted on the bottom surface and electrically connected to dissipate power at a level. Pb, during operation of the converter;
1[e]	wherein the power semiconductor devices are distributed between the first and second sets to distribute heat generation during operation of the converter such that each level Pt, Pb is less than 150% of the other level Pb, Pt.
2	The apparatus of claim 1 wherein a plurality of the power semiconductor devices in the first set are each positioned in a location on the top surface substantially overlapping a location on the bottom surface occupied by a power semiconductor device in the second set.
3	The apparatus of claim 1 wherein the power semiconductor devices are electrically connected using a respective set of conductive vias in the PCB, and a plurality of the power semiconductor devices in the first set share their respective sets of conductive vias with corresponding power semiconductor devices in the second set.
4	The apparatus of claim 2 wherein the power converter further comprises circuitry including a pair of cells having a common

Petition for *Inter Partes* Review of U.S. Patent No. 9,516,761

	circuit topology and each including power semiconductor switches from each of the first and second sets; each cell having its respective components arranged in a pattern, wherein the pattern of components of one cell is substantially a mirror image of the pattern of components in the other cell.
5	The apparatus of claim 4 wherein a component from one of the cells is located on an opposite surface of a respective component from the other one of the cells.
6	The apparatus of claim 5 wherein the cells comprise input cells.
7	The apparatus of claim 3 wherein the power semiconductor devices comprise output switches.

CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing Petition complies with the type-volume limitations as mandated in 37 C.F.R. § 42.24, totaling 12,643 words. Counsel has relied upon the word count feature provided by Microsoft Word. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Dated: November 22, 2023

/Russell E. Levine/

Russell E. Levine, P.C. (Reg. No. 32,153)

KIRKLAND & ELLIS LLP

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Counsel for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that a copy of the foregoing document with accompanying Exhibits 1001-1024, 1026-1031 was caused to be served by First Class Mail, costs prepaid, to Patent Owner at the following address of record:

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