

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DELTA ELECTRONICS, INC.
Petitioner,

v.

VICOR CORPORATION,
Patent Owner.

Case IPR2024-00227

U.S. PATENT NO. 9,516,761

**DECLARATION OF STEVEN B. LEEB, PH.D. IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW**

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Exhibit No.	Description
1001	United States Patent No. 9,516,761 (“’761 Patent”)
1002	Declaration of Dr. Steven B. Leeb (<i>i.e.</i> , this declaration)
1003	<i>Curriculum Vitae</i> of Dr. Steven B. Leeb
1004	File History of U.S. Patent No. 9,516,761
1005	U.S. No. 8,966,747
1006	Declaration of Dr. Sylvia Hall-Ellis
1007	Ericsson BMR 453 series DC/DC converters Technical Specification (July 2010), <i>available at</i> https://web.archive.org/web/20101108165728/http://archive.ericsson.net/service/internet/picov/get?DocNo=28701-EN/LZT146395&Lang=EN&HighestFree=Y . (“Ericsson-BMR”)
1008	Robert W. Erickson and Dragan Maksimovic, <i>Fundamentals of Power Electronics</i> (2d ed. 2001). (“ <i>Fundamentals</i> ”)
1009	U.S. Patent 6,965,517 (“Wanes”)
1010	U.S. Patent 6,970,367 (“Takeshima”)
1011	G. Spiazzi, L. Rossetto, P. Mattavelli, P. Cova, and N. Delmonte, <i>Layout Considerations and Thermal Analysis of a 1.8 MHz Resonant VRM</i> , 2007 IEEE Industry Applications Annual Meeting, 1993 (2007). (“Spiazzi”)
1012	Laszlo Huber, Kevin Hsu, Milan M. Jovanovi, Dennis Solley, Gennady Gurov and Robert J. Porter, <i>1.8-MHz, 48-V Resonant VRM: Analysis, Design, and Performance Evaluation</i> , 21 IEEE Transactions on Power Electronics 79 (2006)
1013	Excerpts of Complainant Vicor Corporation’s Second Supplemental Objections And Responses To Respondents’ First Set Of Joint Interrogatories (Nos. 1-20)

1014	Picture of Ericsson BMR 453 series DC/DC converter, https://web.archive.org/web/20120131104718/http://www.ericsson.com/solutions/news/powermodules/2009/hires_BMR453_jan09.jpg .
1015	U.S. Patent No. 7,403,397
1016	Laszlo Balogh, Design Review: 140W, Multiple Output High Density DC/DC Converter, (1997), <i>available at</i> https://web.archive.org/web/20050129014555/http://focus.ti.com:80/lit/ml/slup117/slup117.pdf .
1017	J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, <i>Principles of Power Electronics</i> (1st ed. 1991) (<i>physical copy available upon request, select excerpts filed electronically</i>)
1018	<u>Power Modules: Digital DC/DC converter family integrates PMBus connectivity</u> (2009), <i>available at</i> https://web.archive.org/web/20090902060840/http://www.ericsson.com:80/technology/docs/article_PowerModules_digital_dc-dc.pdf
1019	U.S. Patent 6,466,454
1020	U.S. Patent 8,749,990
1021	Declaration of Nathaniel E. Frank-White authenticating Exhibits 1007, 1014, and 1018
1022	Declaration of Nathaniel E. Frank-White authenticating Exhibit 1016
1023	U.S. Patent Application No. 2011/0057713
1024	U.S. Patent 6,724,631
1025	Claim Chart for the Infringement of Independent Claim 1 and Dependent Claims 2, 3, 4, 5, 6, 7 of Complainant Vicor Corporation's United States Patent 9,516,761 by Delta U50SU4P162 High Power Density 48V / 12V Bi-Directional DC-DC Converter Power Module and Computing Systems Containing the Same
1026	Ericsson BMR 453 series DC/DC converters Technical Specification (September 2008) ("BMR-2008")

1027	Vishay Siliconix N-Channel 75 V (D-S) MOSFET SiE818DF Technical Specification (July 13, 2009), <i>available at</i> https://www.digikey.com/en/products/detail/vishay-siliconix/SIE818DF-T1-E3/1656715
1028	March 25, 2014 Claim Amendment in prosecution of U.S. Patent No. 8,966,747 (divisional of '761 patent)
1029	TDK Data Sheet: FReta iQD Series – Single Output Quarter Brick Bus Converter, <i>available at</i> https://www.datasheetarchive.com/datasheet?id=0c23ebb9024bd4c7b5c5d7b96a5c82316b8b34&type=M&term=iqd48025a120v007
1030	Vishay Siliconix N-Channel 40-V (D-S) MOSFET Si7884DP (Sept. 8, 2008), <i>available at</i> https://www.vishay.com/docs/68395/si7884bd.pdf .

DECLARATION OF STEVEN B. LEEB, PH.D.

1. I, Steven B. Leeb, make this declaration in connection with the proceedings identified above.

2. I have been retained on behalf of Petitioner Delta Electronics, Inc. (“Delta”) to offer my expert opinions in connection with the above-captioned proceeding relating to U.S. Patent 9,516,761 (the “’761 patent”).

3. I am being compensated for my time in connection with this inter partes review (IPR) at my standard consulting rate of \$750 per hour. No part of my compensation depends on the outcome of this proceeding.

4. I have been asked to provide my opinions as to whether claims 1-7 (the “Challenged Claims”) of the ’761 patent are invalid from the perspective of a person having ordinary skill as of May 11, 2011 and also as of April 2010.

5. In preparing this declaration, I have reviewed the ’761 patent (Ex. 1001), the file history of the ’761 patent (Ex. 1004), and all other materials referenced in this declaration. I have relied upon my education, training, knowledge, and experience in the art, and have considered the viewpoint of a person of ordinary skill in the art (POSITA) as of the dates listed above.

6. All emphasis and annotations below are added, unless noted otherwise.

I. BACKGROUND AND QUALIFICATIONS

7. I summarize in this section my educational background, career history, and other relevant qualifications. My resume is Exhibit 1003.

8. I am a tenured Professor in the Electrical Engineering and Computer Science Department at the Massachusetts Institute of Technology (“MIT”), and have a joint appointment as a faculty member in the Department of Mechanical Engineering at MIT. In 2004, I was appointed as a MacVicar Faculty Fellow, a program honoring MIT teachers and mentors who have made outstanding contributions to undergraduate education. I earned a Bachelor of Science (S.B.) degree, a Master of Science (S.M.) degree, an Electrical Engineering (E.E.) degree, and a Doctorate (Ph.D.) degree, from MIT in 1987, 1989, 1990, and 1993, respectively.

9. I have 34 years of experience in the field of electrical engineering and computer science, with particular experience in the field of power electronics and embedded control, including the study of electronic circuits and the control of electrical energy in circuits. From 1987 to 1991, I worked part-time as a United States Air Force (“USAF”) Reservist at the Wright Research and Development Center at Wright Patterson Air Force Base in Ohio, in its avionics branch, developing and studying power supplies for use in advanced avionics systems. During my time on the MIT faculty from 1993 to present. I have designed several

power electronic products that include microcontrollers and that employ advanced control techniques. My work in the area of power electronics has included extensive study, analysis, and use of control systems, power factor correction, monitoring power consumption, electronic circuits, voltage regulation, and voltage regulators.

10. As part of my research at MIT, I have developed power electronic circuits for power supplies, motor drives, induction heating units, and charging systems, among numerous other applications.

11. Since 1995, I have taught several courses at MIT that cover the use of power electronics and microcontrollers. I have taught graduate and undergraduate level courses at MIT in motor design, microcomputer control, power electronic circuit design, field theory, circuit analysis, signal processing, feedback control, and power systems. In these courses, I have taught extensively regarding the design of voltage regulators, converters, and protection circuits. I also have supervised over 150 theses and advanced undergraduate projects since I joined the MIT faculty in 1993. I have won the MIT Edgerton and Bose awards for excellence in teaching and research, MIT's Spira teaching award, and several other recognitions including a teaching award from an undergraduate student honor society (HKN).

12. I have authored or co-authored more than 200 technical publications and I am a named inventor on over 20 U.S. patents, with others pending, in the areas of power electronics, drives, and power systems design, analysis, monitoring, and control. My resume includes a sample list of these publications. For example, a paper that I co-authored, *Current and Voltage Reconstruction from Non-Contact Field Measurements*, in the IEEE Sensors Journal (Vol. 16, Issue 15), was recognized as one of the 25 most downloaded Sensors Journal papers in 2016. I have been invited to give plenary session papers and presentations, for example, at the IEEE Applied Power Electronics Conference (APEC) in 2004 for a paper I authored entitled *Putting Profit into Power Electronic Products with Digital Control*. Another recent paper that I co-authored, *Capacitor-less Photovoltaic (PV) Cell-Level Power Balancing using Diffusion Charge Redistribution*, received a “Best Presentation” award in its session at the APEC 2014 conference.

13. Some of my research work has been directed at systems involved with electric motors and drive systems for electric motors. Publications I have co-authored with examples of this work include, but are not limited to, *A Comparison of Switched Doubly-Fed Machine Drive Topologies for High Power Applications* presented at the 2015 IEEE International Electric Machines and Drives Conference, *Adaptive Control of Power Electronic Drives for Servomechanical Systems* in Volume 15, No. 6 of the IEEE Transactions on Power Electronics, and

Nonintrusive Induction Motor Speed Detection in Vol. 9, No. 2 of the IET Energy and Power Applications Journal.

14. In 1999, I co-founded Talking Lights, LLC, a company in Massachusetts. The company worked to commercialize inventions that I developed relating to a “Talking Lights” system. The system included electronic ballast circuits that modulated the arc in a fluorescent lamp and drivers that modulated the current in an LED lamp in order to transmit information and illumination to the blind or hard-of-hearing. As part of the design of these systems, I developed voltage regulators for these lighting ballasts. In 2003 and 2004, I co-developed commercial products that have passed regulatory approval with the Underwriters’ Laboratory and the Federal Communications Commission. The Talking Lights system has been sold commercially.

15. I received a National Science Foundation CAREER Award in 1996. In 1999, I was named Technology Review’s TR100 Outstanding Young Innovator. I also was named the IEEE Outstanding Young Power Electronics Engineer in 1999. I have received two R&D 100 awards for products I developed at Talking Lights, LLC. In 2007, I was named a Fellow of the Institute of Electrical and Electronics Engineers (“IEEE”). The IEEE is the professional organization for electrical engineering in general, and for power electronic circuit designers. The rank of “Fellow” is granted to members of the IEEE judged by an extensive review

process to have made “extraordinary accomplishments” in a field of IEEE’s interest. In 2021, I was appointed as the chair holder of the Emanuel E. Landsman Professorship at MIT.

II. LEGAL STANDARDS

16. I am not a lawyer or legal expert, and I do not offer any opinions regarding applicable legal standards. Below, I set forth my understanding of the law as it has been explained to me by counsel, and I have applied this understanding in forming my opinions in this declaration.

17. To invalidate a patent claim as obvious in the context of an IPR proceeding, the petitioner bears the burden of showing by a preponderance of the evidence that the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art to which the subject matter pertains at the time the claimed invention was made. Factors relevant to the determination of obviousness include (1) the scope and content of the prior art, (2) the level of ordinary skill in the art at the time of the invention, (3) differences between the claimed invention and the prior art, and (4) “secondary considerations” or objective evidence of obviousness or nonobviousness.

18. I am informed that some non-exclusive rationales that may support a conclusion of obviousness include:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of known technique to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- “Obvious to try” – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art;
- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

19. **Reason to Combine.** Obviousness can be established by showing that a person of ordinary skill in the art would have combined or modified the teachings of the prior art to produce the claimed invention and would have had a reasonable expectation of success in achieving the claimed subject matter. There is no requirement that the prior art provide an express teaching, suggestion, or motivation to combine elements of the prior art, but a determination of obviousness

requires more than showing that each element of a patent claim was independently known in the prior art. Rather, the petitioner in an IPR must identify some apparent reason why a person of ordinary skill in the art would have combined the elements or concepts from the prior art in the same way as in the claimed invention when considered as a whole. The motivation to combine may be implicit and may be found in the knowledge of a person of ordinary skill in the art, from the nature of the problem to be solved, market demand, or common sense.

20. **Hindsight.** A determination regarding obviousness must be based on the knowledge possessed by a person of ordinary skill in the art at the time when the invention was made, and one should not consider in hindsight what is known today or what is learned from the teachings of the patent. Thus, it is inappropriate to use hindsight reconstruction of references to reach the claimed invention without any explanations as to how or why the references would be combined to produce the claimed invention.

21. **Analogous Art.** An obviousness analysis cannot be based on nonanalogous art. The rationale behind this rule is that when art is directed to a different purpose than a claimed invention, an inventor would have less motivation or occasion to consider it. Art is analogous when it is from the same field of endeavor as the claimed invention, or if the art is not from the same field of endeavor, when it is reasonably pertinent to the particular problem faced by the

inventor. To be “reasonably pertinent,” art must “logically commend itself” to an inventor’s attention in considering his problem.

III. PRIORITY DATE AND LEVEL OF ORDINARY SKILL IN THE ART

22. I have been asked by counsel to perform my analysis from the perspective of one of ordinary skill in the art as of May 11, 2011 (the claimed priority date on the face of the patent) and as of April 2010 (which I understand from counsel is when Patent Owner contends was the date of conception). My opinions reflected below are the same under either date; however, if the April 2010 priority date applies, then I understand from counsel that Ericsson-BMR would no longer qualify as a prior art reference and therefore my opinions based on Ericsson-BMR would be moot. (I understand that BMR-2008 would still qualify as a prior art reference, however, so my opinions based on BMR-2008 would still apply, including the analysis based on its similarity in disclosure to Ericsson-BMR.)

23. I understand that Patent Owner has not yet provided any evidence or analysis in this proceeding regarding its alleged April 2010 date of conception. In the event that Patent Owner provides any such evidence, I reserve the right to analyze such evidence and form opinions regarding whether the ’761 patent is indeed entitled to that earlier claimed priority date. The fact that I have performed my analysis as of April 2010 (in addition to as of May 11, 2011) does not indicate

that I agree that April 2010 was the date of conception of the purported '761 patent inventions.

24. I understand that the Patent Owner has contended that a person of ordinary skill in the art ("POSITA") at the time of the '761 Patent (whether that date is May 11, 2011 or April 2010) would have at least a Master's degree in electrical engineering and two or more years of work experience relating to power electronics and the manufacture of power converters or printed circuit board design for power converters, and that additional education might compensate for less work experience, and vice-versa. *See* EX1013 at 79. I have applied this ordinary level of skill in my analysis. My opinion would not change, however, if a somewhat higher or lower level of ordinary skill in the art were applied.

25. I have been qualified as at least a person of ordinary skill in the art since well before 2010. I have also interacted extensively with and taught persons of ordinary skill in the art. My opinions set forth in this declaration are presented from the standpoint of one skilled in the art. Thus, where I specify in the analysis below that I am rendering my opinion, it should be understood that my opinion is from the perspective of a person having the level of ordinary skill in the art that I have described at the time of the invention.

IV. OVERVIEW OF OPINIONS

26. Below is a summary of my opinions as reflected in the more detailed analysis below:

Ground	Claims	Basis
I	1-5, 7	Obvious over Ericsson-BMR or, alternatively, BMR-2008
II	1-5, 7	Obvious over Ericsson-BMR in view of Spiazzi, or, alternatively, over BMR-2008 in view of Spiazzi
III	1-7	Obvious over Ericsson-BMR in view of Wanes, or, alternatively, over BMR-2008 in view of Wanes
IV	1-7	Obvious over Takeshima
V	1-7	Obvious over Takeshima in view of Spiazzi
VI	1-7	Obvious over Takeshima in view of Wanes
VII	1-7	Obvious over Ericsson-BMR in view of Takeshima, or, alternatively, over BMR-2008 in view of Takeshima
VIII	1-7	Obvious over Spiazzi in view of Wanes

V. CLAIM CONSTRUCTION

27. I understand that in construing or interpreting a patent claim, the words of the claim are normally given their ordinary and customary meaning, which is the meaning that words would have had to a person of ordinary skill in the art in question at the time of the invention. The person of ordinary skill in the art is deemed to read the claim term in the context of not only the particular claim in

which the disputed term appears, but also in the context of the entire patent, including the other claims and the specification, as well as the prosecution history of the patent.

28. For purposes of this declaration, I have been asked to apply Patent Owner's apparent understanding of the terms as reflected in its infringement contentions. *See* EX1025. I reserve the right to respond to any specific construction proposed by Patent Owner that may depart from its apparent understanding of the claims as reflected in its infringement contentions. However, my ultimate opinions of invalidity of the Challenged Claims would not change under any reasonable construction of the claims, to the extent that the claims can be understood by a POSITA.

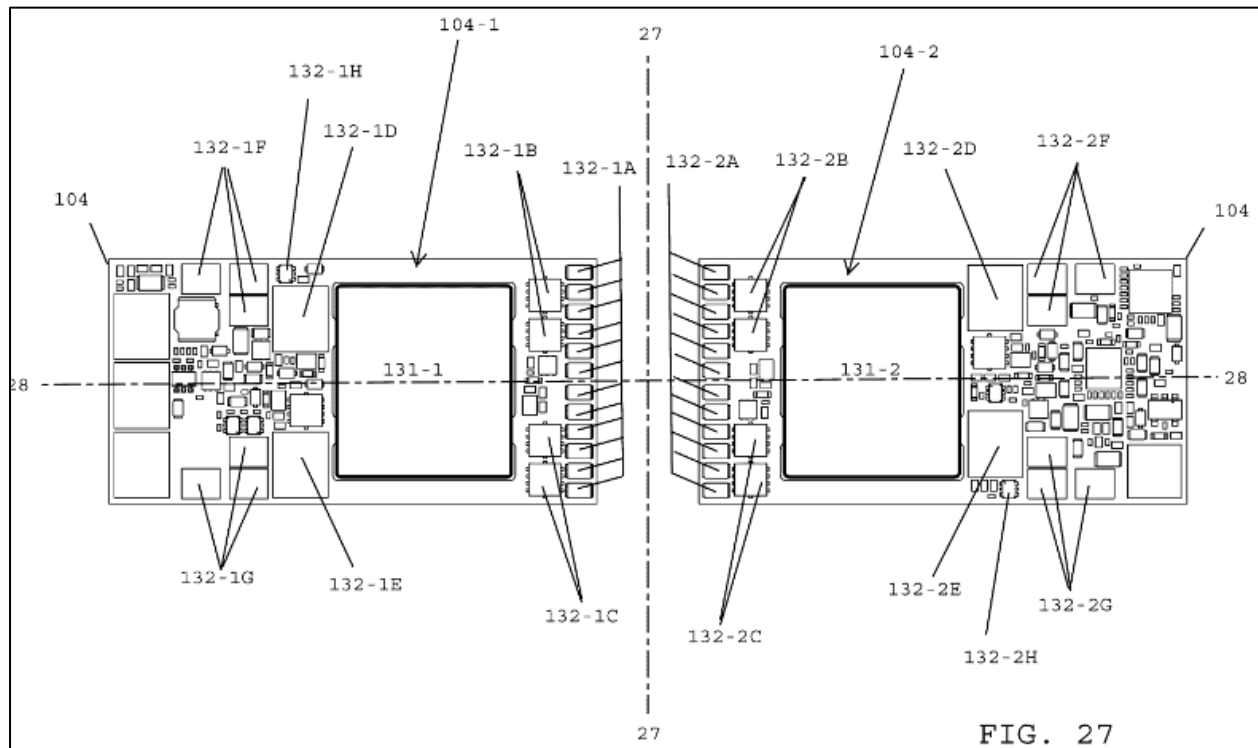
29. The fact that I have applied Patent Owner's apparent understanding of the terms does not mean that I necessarily agree that a POSITA would have understood the terms in the same manner, nor does it mean I necessarily agree that a POSITA would have found the scope of the claim terms definite.

VI. OVERVIEW OF THE '761 PATENT

A. Purported Invention

30. I agree with Patent Owner that the '761 patent relates generally to the layout, packaging, and manufacture of power converters and power modules. *See* EX1013 at 79; *see* Ex. 1001 at 1:16-20 ("FIELD OF THE INVENTION: ... power

converters”). For example, the ’761 patent describes the idea of the purported invention in the following quote, presented below for ease of reference with Figure 27:



Symmetrical Power Dissipation Between PCB Surfaces

The components may be arranged between the PCB surfaces according to heat dissipated during operation. For example, the heat dissipative components may be arranged in a manner that distributes the heat evenly between the two PCB surfaces allowing heat produced by power dissipating devices to be extracted from both surfaces of the PCB improving the thermal performance. This type of heat dissipation symmetry is also factored into the component layout shown in the power converter

of FIG. 27. For example, two input cells each using the same basic circuit topology are shown, one above and another below axis 28. As shown, the components of each input cell occupy both sides of the PCB in observance of other factors influencing component layout such as winding locations, etc. In this example, the upper input cell includes the two input FETs 132-1D and 132-2D, and the six input capacitors 132-1F and 132-2F. The lower input cell includes the two input FETs 132-1E and 132-2E, and the six input capacitors 132-1G and 132-2G. To ensure heat dissipation symmetry between the two surfaces, the cells may be arranged in mirror image layouts as shown. In FIG. 27, input FET 132-2E (top surface) in the lower cell corresponds to input FET 132-1D (bottom surface) in the upper cell. Similarly, lower cell input FET 132-1E (bottom surface) corresponds to upper cell input FET 132-2D (top surface). As can be seen, the significant power dissipative components of the input cells are arranged to have one component of one cell mounted on one surface with the respective component from the other cell mounted on the other surface. This type of symmetry may be seen in FIG. 27 with lower cell component 132-2H mounted on the top surface and the respective upper cell component 132-1H mounted on the bottom surface. In some examples, the FETs are arranged such that during operation, the power FETs on the top surface dissipate power at a level that is

comparable to the level of power dissipated by the power FETs on the bottom surface. Also, the level of power dissipated by the power FETs in the upper input cell is comparable to the level of power dissipated by the power FETs in the lower input cell. For example, the level of power dissipated by the power FETs on one surface is less than 150% of the level of power dissipated by the power FETs on the other surface. The level of power dissipated by the power FETs in the upper cell is less than 150% of the level of power dissipated by the power FETs in the lower cell, and vice versa.

See Ex. 1001 at 24:45-25:24.

B. Prosecution History

31. I have reviewed the prosecution history of the '761 patent, and I did not find any substantive discussion by the Examiner or applicant that affects the substance of my opinion. *See generally* Ex. 1004. During prosecution, there was neither discussion of the meaning of claim terms nor of the prior art references that form the basis of my opinion herein.

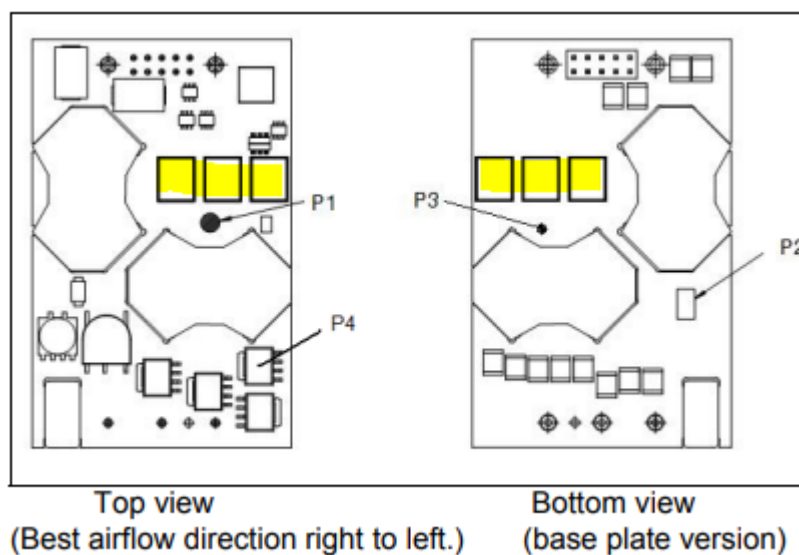
VII. SUMMARY OF THE PRIOR ART

A. Ericsson-BMR (Ex. 1007) And BMR-2008 (Ex. 1026)

32. Ericsson-BMR is a technical specification related to a product previously sold by third-party Ericsson for its BMR 453 series DC/DC power converter, pictured here (top and bottom sides):



See Ex. 1007 at 1. As explained more fully below in Ground I, Ericsson-BMR taught that its magnetic cores and certain of its power semiconductor devices are symmetrically disposed and overlapping each other on top and bottom. The symmetrically disposed and overlapping power semiconductor devices are shown in this highlighted figure from Ericsson-BMR:



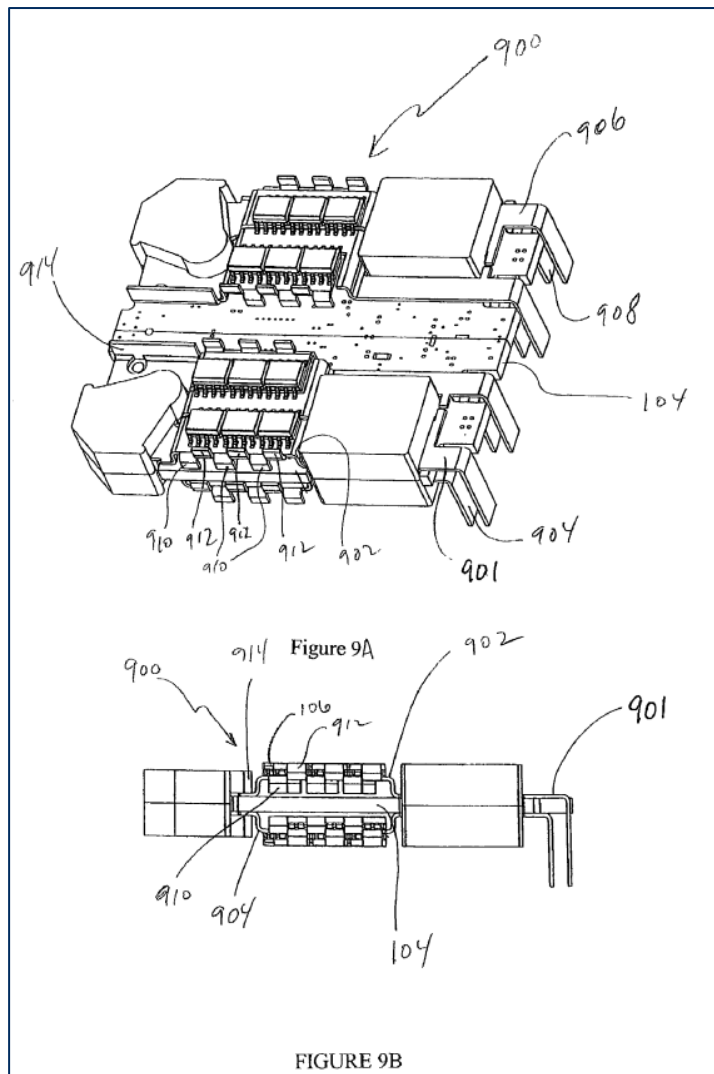
See Ex. 1007 at 24 (annotated).

33. Ericsson-BMR is analogous art to the '761 patent. For example, the Ericsson-BMR module is a power converter and is thus in the same field of endeavor as the '761 patent.

34. BMR-2008 is a technical specification that is substantially similar in relevant respect to Ericsson-BMR, and is therefore relevant and analogous art for the same reasons as Ericsson-BMR. *Compare* EX1026, *with* EX1007.

B. Wanes (Ex. 1009)

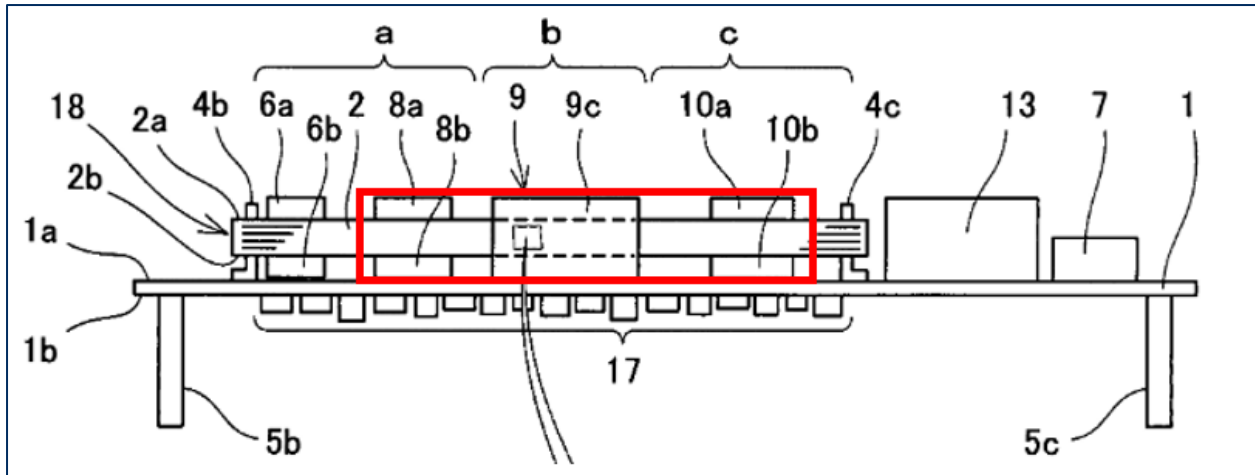
35. Wanes is a U.S. patent. *See* Ex. 1009 at Cover Page. As shown in Wanes, it was well known to a POSITA to symmetrically dispose cells of overlapping electrical components on the top and bottom of printed circuit boards and component mounting substates (Fig. 9B) and further mirror those components horizontally (Fig. 9A):



36. Wanes is analogous art to the '761 patent. For example, the Wanes module is a power converter and is thus in the same field of endeavor.

C. Takeshima (Ex. 1010)

37. Takeshima is a U.S. patent. Similar to Wanes and Ericsson-BMR, Takeshima also demonstrates that it was well-known in the art to symmetrically dispose cells of overlapping electrical components on the top and bottom of PCBs, as outlined in red below in this cropped version of Takeshima's Figure 2:

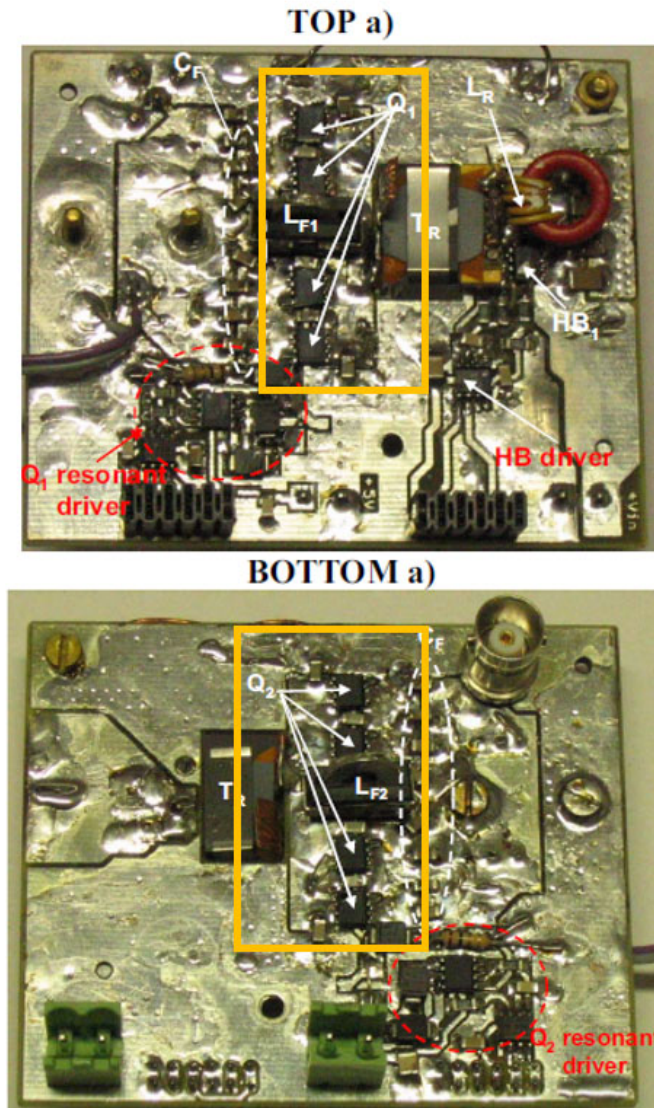


Ex. 1010, Fig. 2 (cropped and annotated).

38. Takeshima is analogous art to the '761 patent. For example, the Takeshima module is a power converter and is thus in the same field of endeavor.

D. Spiazzi (Ex. 1011)

39. Spiazzi is a 2007 conference paper. *See* Ex. 1011 at 1993. Like Ericsson-BMR, Wanes, and Takeshima, Spiazzi also demonstrates that it was well-known to a POSITA to symmetrically lay out overlapping MOSFETs on the top and bottom of a PCB, as shown (for example) by the layout of top-side MOSFETS Q1 relative to the bottom-side MOSFETs Q2, highlighted here within the orange box:



See Ex. 1011 at Fig. 5 (cropped, annotated with orange box). As its title “Layout Considerations and Thermal Analysis of a 1.8 MHz Resonant VRM [Voltage Regulator Module]” suggests, Spiazzi demonstrates that a POSITA was well aware that thermal management was important and that the layout of components on the top and bottom of a circuit board had direct implications on power dissipation. See Ex. 1011 at 1993.

40. Spiazzi is analogous art to the '761 patent. For example, the Spiazzi module is a power converter and is thus in the same field of endeavor.

41. As a further example, Spiazzi is relevant to the particular problem faced by the alleged inventors of the '761 patent regarding power dissipation. As Spiazzi explains in the very first sentence of this 2007 paper: “*Abstract* – Practical realization of modern high current and high switching frequency converters (with strong skin and proximity effects) requires a good control on layout-dependent parasitic components and on the power losses (thermal management), in order to meet the goal of high efficiency and reliability.” Ex. 1011 at 1993. A POSITA would therefore have plainly looked to Spiazzi in addressing the problems described in the '761 patent.

42. The same applies to the Ericsson-BMR / BMR-2008, Takeshima, and Wanes prior art discussed above, all of which also experience power dissipation and would thus similarly require efficient circuitry and appropriate layout to support proper thermal operation. A POSITA would have understood the importance of avoiding excessive power dissipation and that poor choices of component placement could aggravate thermal problems. *See, e.g.*, Ex. 1023 ¶ 52 (“[T]he heat generated from the semiconductor devices can be efficiently radiated through [] both sides of the power module [which helps create] a highly reliable power module with longer life duration....”).

E. *Fundamentals Of Power Electronics* (Ex. 1008)

43. *Fundamentals Of Power Electronics* (hereinafter, “*Fundamentals*”) is a textbook that reflects knowledge that was well known to a POSITA regarding the elementary principles of the operation of power electronics. This textbook is commonly used in teaching students. As discussed further below, *Fundamentals* details the proper and expected operation of certain types of power converter circuits used by the other prior art references discussed herein.

44. *Fundamentals* is analogous art to the ’761 patent. For example, *Fundamentals* teaches power conversion circuits and also teaches power dissipation characteristics and is thus in the same field of endeavor, and is also relevant to the particular problem faced by the alleged inventors of the ’761 patent.

45. *Fundamentals* is not one of the prior art references incorporated into any particular ground or combination discussed below. Rather, I rely on *Fundamentals* at various points to support with documentation my opinion regarding what was well-known to a POSITA about the operation of various power converter circuits.

VIII. GROUNDS

A. Ground I: Claims 1-5 And 7 Are Rendered Obvious By Ericsson-BMR Or, Alternatively, By BMR 2008

1. Claim 1

46. In my opinion, Ericsson-BMR renders obvious Claim 1.

a. 1[preamble]: An apparatus comprising:

47. In my opinion, Ericsson-BMR teaches the preamble.

48. The Ericsson-BMR apparatus can be seen, for example, on the first page of the document (showing the top and bottom sides of the apparatus):



See Ex. 1007 at 1.

b. 1[a]: a power converter including

49. In my opinion, Ericsson teaches this element.

50. For example, as shown in this cropped and highlighted portion of page 2, the Ericsson-BMR module has an input of 36-75 volts, and in various embodiments has an output of 3.3, 5, 9, or 12 volts:

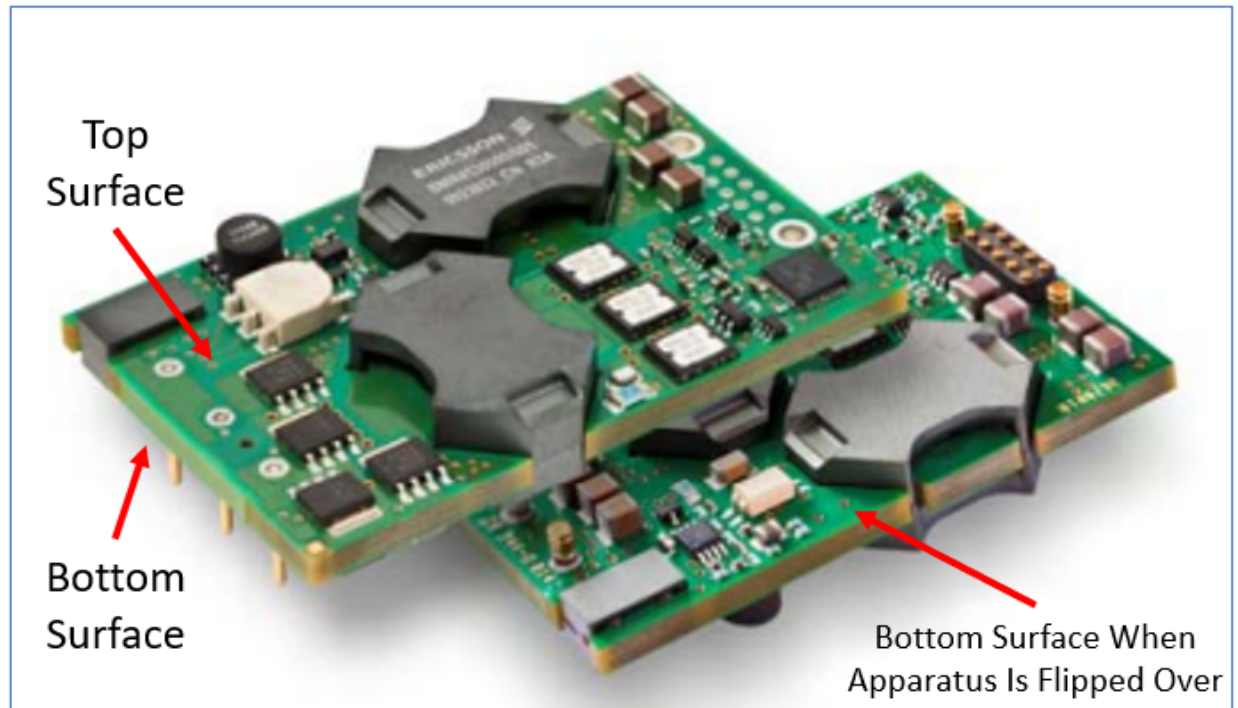
BMR 453 series DC/DC converters, Input 36-75 V, Output up to 60 A / 396 W											
Ordering Information Product Program											
<table> <tr> <th>Product program</th><th>Output</th></tr> <tr> <td>BMR4530002/003</td><td>3.3 V / 60 A, 198 W</td></tr> <tr> <td>BMR4530002/004</td><td>5 V / 60 A, 300 W</td></tr> <tr> <td>BMR4530000/002</td><td>9 V / 33 A, 297 W</td></tr> <tr> <td>BMR4530000/001</td><td>12 V / 33 A, 396 W</td></tr> </table>		Product program	Output	BMR4530002/003	3.3 V / 60 A, 198 W	BMR4530002/004	5 V / 60 A, 300 W	BMR4530000/002	9 V / 33 A, 297 W	BMR4530000/001	12 V / 33 A, 396 W
Product program	Output										
BMR4530002/003	3.3 V / 60 A, 198 W										
BMR4530002/004	5 V / 60 A, 300 W										
BMR4530000/002	9 V / 33 A, 297 W										
BMR4530000/001	12 V / 33 A, 396 W										
General Information Reliability The Mean Time full output power (T _A) of +40°C, w and Communica methods could b and failure rate v Ericsson Power Predicted MTBF											

See Ex. 1007 at 2 (annotated). A POSITA would have therefore recognized that Ericsson discloses a power converter, including because it converts direct current at one, higher voltage into a second, lower voltage. See also Ex. 1007 at, e.g., 1 (“DC/DC converters”).

c. **1[b]: a printed circuit board (“PCB”) comprising a plurality of conductive layers and having a top surface and a bottom surface**

51. In my opinion, Ericsson-BMR teaches this element.

52. Ericsson-BMR teaches a PCB that has a top surface and a bottom surface. Ericsson-BMR states that it is implemented using a PCB. See Ex. 1007 at 21 (“The sense traces should be located close to the *PCB* ground layer . . .”). Ericsson-BMR’s PCB is depicted, for example, as the green printed circuit board on the first page, which is green on both the top surface and bottom surfaces shown here:



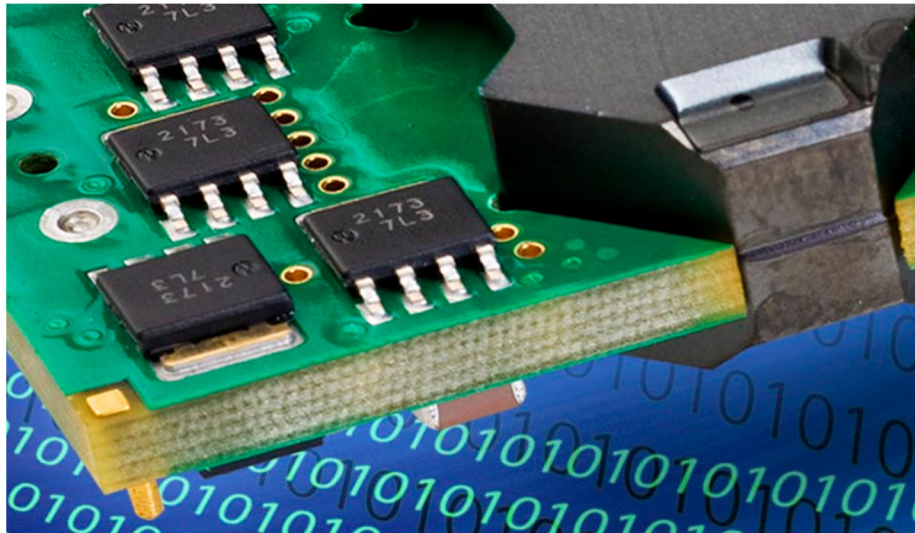
See Ex. 1007 at 1 (annotated)

53. As a POSITA would have recognized, Ericsson-BMR's PCB is comprised of a plurality of conductive layers, including the top and bottom layers that can be seen in the photos above. See Ex. 1007 at 1. Ericsson-BMR teaches that the "sense traces should be located close to the PCB *ground layer*," as opposed to another conductive "layer," and a POSITA would have recognized that "ground" indicates a conductive connection to ground voltage. See Ex. 1007 at 21.

54. The picture above also shows a series of gold striations in between the top and bottom conductive layers, which a POSITA would have known or at least obviously expected corresponded to an additional plurality of conductive layers:



See EX1007 at 1 (cropped). A clearer view of these layers can be seen in additional documentation regarding the Ericsson-BMR module:

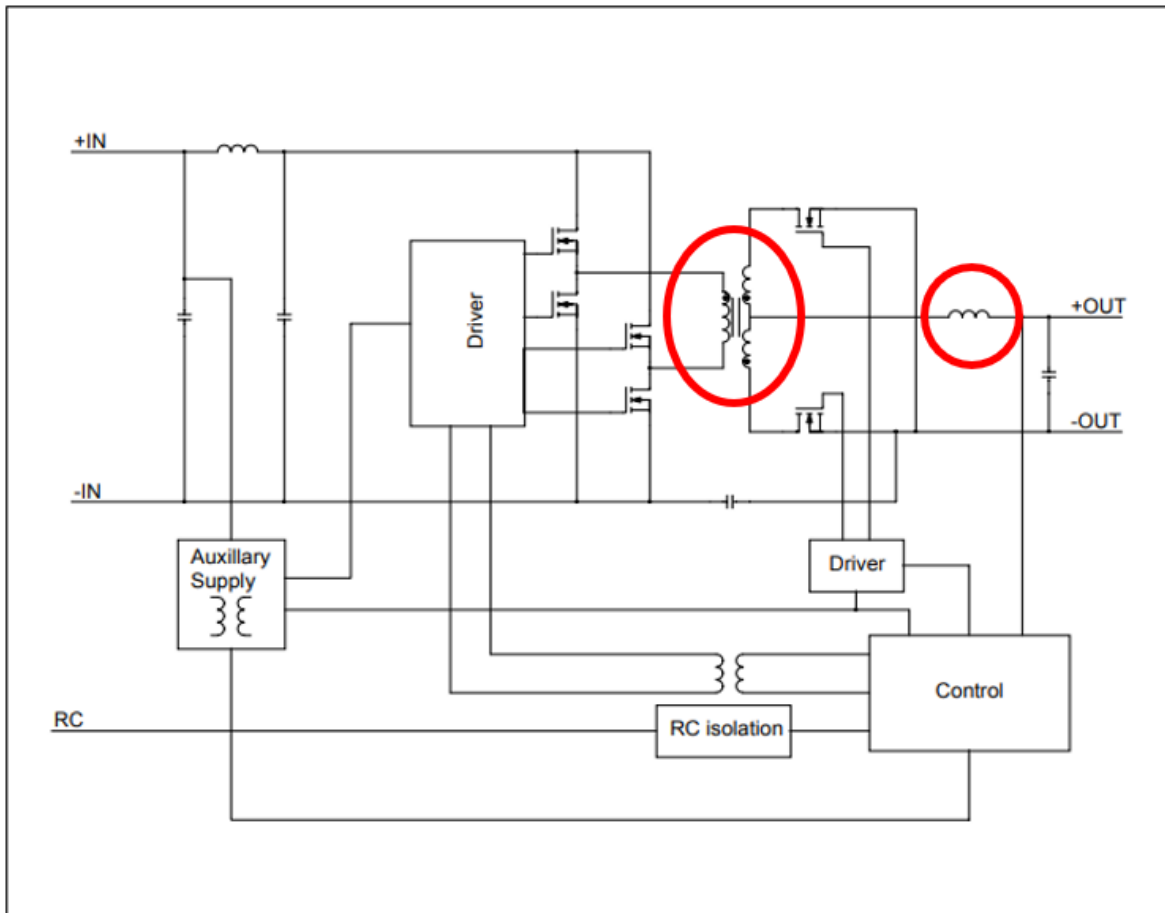


See EX1014 at 1.

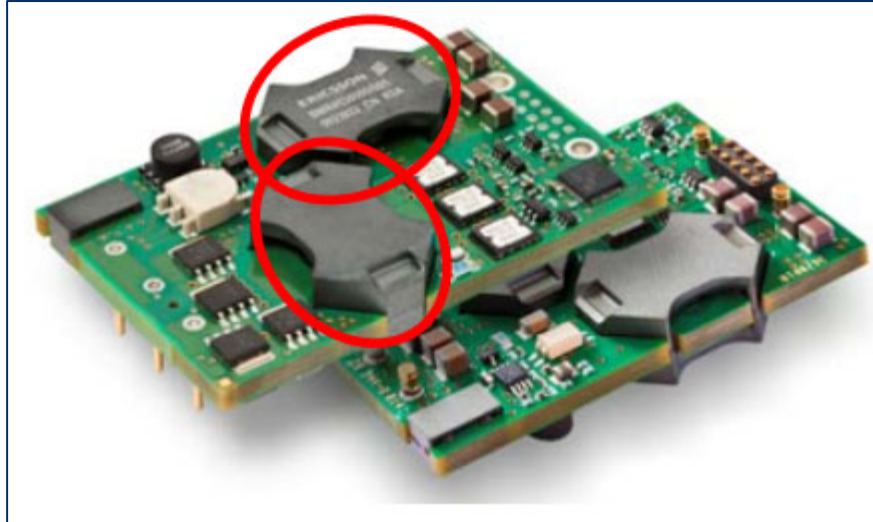
- d. **1[c]: a magnetic core structure magnetically coupled to a winding formed by traces in one or more of the conductive layers in the PCB; and**

55. In my opinion, Ericsson-BMR teaches and renders obvious this element.

56. As background, Ericsson-BMR teaches that the module employs the following fundamental circuit topology:

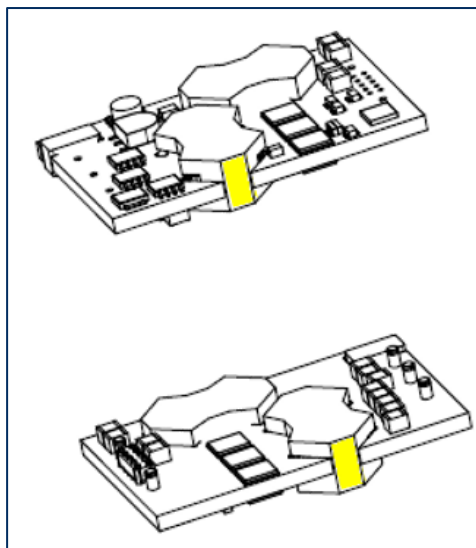


See Ex. 1007 at 5 (annotated). A POSITA would have recognized the symbols for the transformer and inductor, circle above in red, that use magnetics. See Ex. 1008 at Fig. 1.5. Thus, a POSITA would have expected that Ericsson-BMR's apparatus includes a magnetic core structure, which are circled here in red, magnetically coupled to windings:



A POSITA would recognize these black structures as magnetic cores because they are a common shape for these types of magnetic core components. *See, e.g.*, Ex. 1020 at Fig. 1A, 3:12-21 (planar magnetic of same shape).

57. A POSITA would have further recognized that the magnetically coupled windings are formed by traces in one or more of the conductive layers in the PCB, because the magnetic core extends through the PCB (as shown below), so there is nowhere else for the windings to be:



See Ex. 1007 at 31. This understanding of a POSITA is confirmed by higher resolution photos of the Ericsson-BMR unit from the time, which also show the magnetic core extending all the way to the surface of the PCB and through it. There is no other place for the magnetically coupled windings to be located other than as traces in the PCB layers:



See Ex. 1014 (annotated); see also Ex. 1018 at 6 (same disclosure).

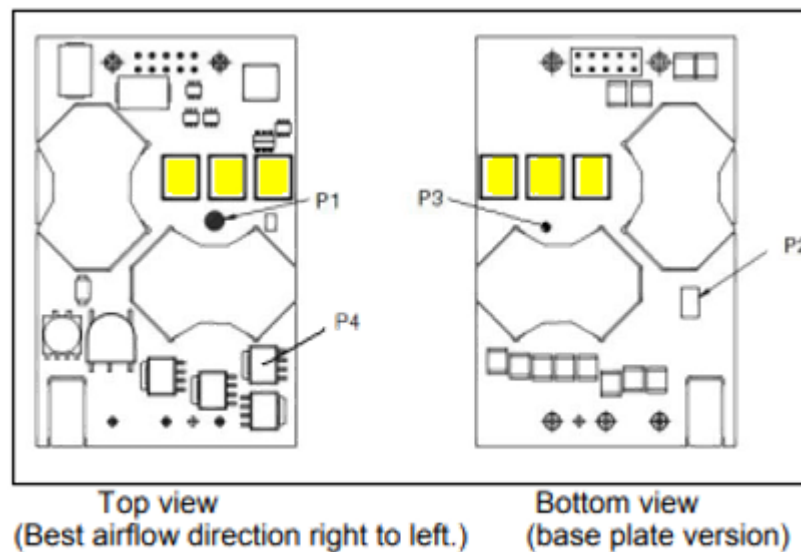
58. As a POSITA would have been aware, this use of the PCB to create the windings for a magnetic device, as shown in the photo above, was a standard way to apply planar magnetics. *See, e.g.*, Ex. 1020 at 3:13-16 (“In general, to apply the planar magnetics technology (called ‘ferrite core on board’) requires many layers of thick (‘heavy’ in the circuit board industry) copper clad to construct the powertrain, *including the transformer windings.*”).

59. It at least would have been obvious to a POSITA for the windings to have been formed by traces in one or more of the conductive layers in the PCB, including because (as discussed above) there is no other place in the Ericsson-BMR module for the windings. Using traces in the conductive layers in the PCB for the windings was well-known in the art. *See, e.g.*, Ex. 1019 at 1:54-60 (patent from 1999, more than a decade before the ’761 patent: “The windings of the magnetic elements ... are incorporated in the multilayer PCB.... In this way the footprint of the magnetic elements is reduced to the footprint of the transformer core.”).

- e. **1[d]: a plurality of power semiconductor devices, a first set of the power semiconductor devices being mounted on the top surface and electrically connected to dissipate power at a level, Pt, during operation of the converter, a second set of the power semiconductor devices being mounted on the bottom surface and electrically connected to dissipate power at a level, Pb, during operation of the converter;**

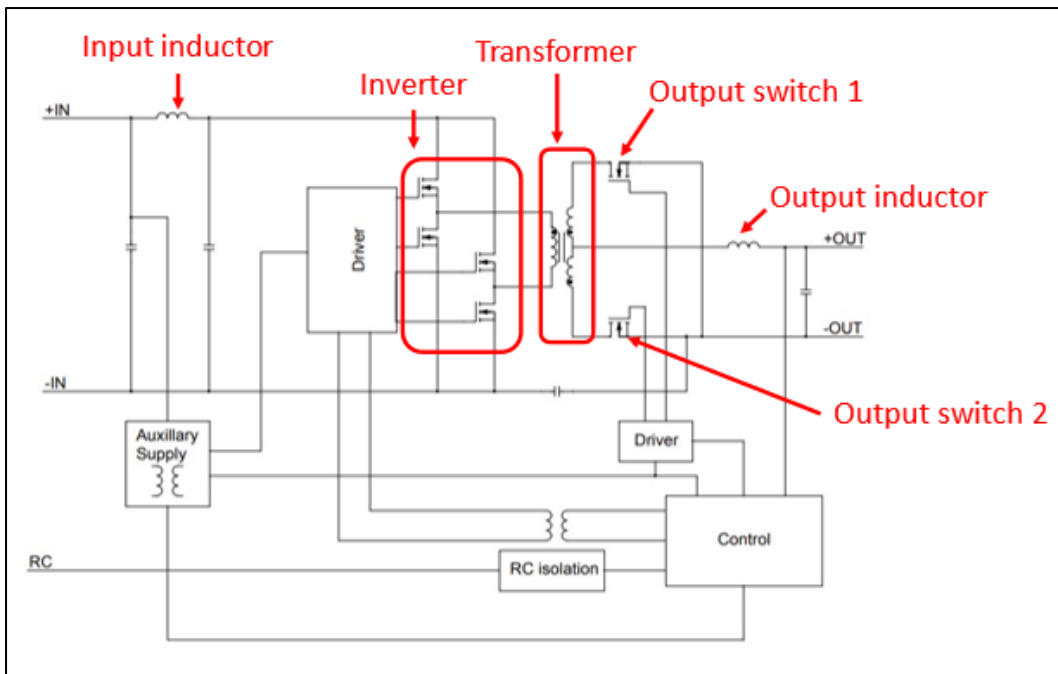
60. In my opinion, Ericsson-BMR renders this obvious.

61. A POSITA would at least have found it obvious that, as shown highlighted in yellow here, Ericsson-BMR's "Top view" has three power semiconductor devices mounted on the top surface, and Ericsson-BMR's "Bottom view" has three power semiconductor devices mounted on the bottom surface of the PCB:



See Ex. 1007 at 24. A POSITA would have found this obvious for the following reasons.

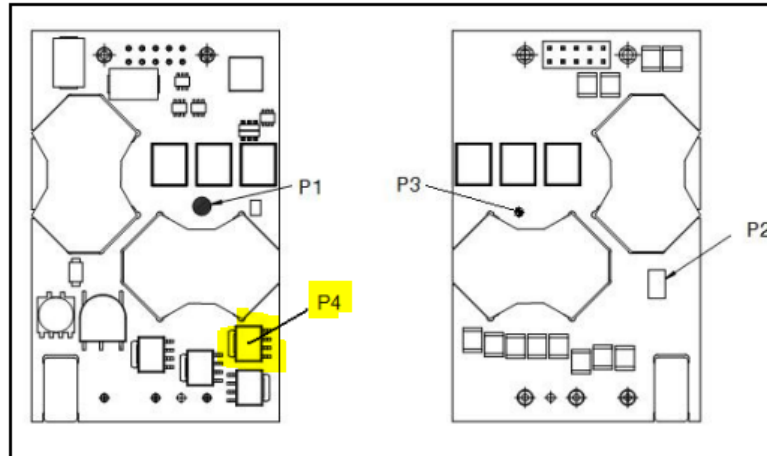
62. As background, Ericsson-BMR provides the following "fundamental circuit diagram" which is a functional representation of the components on the board:



See Ex. 1007 at 5 (annotated). Output switches 1 and 2 in the diagram above are on what is known as the “secondary” side of the transformer, in contrast to the input switches that form the inverter on the “primary” side of the transformer.

Ericsson-BMR teaches that P4 refers to a Primary MOSFET:

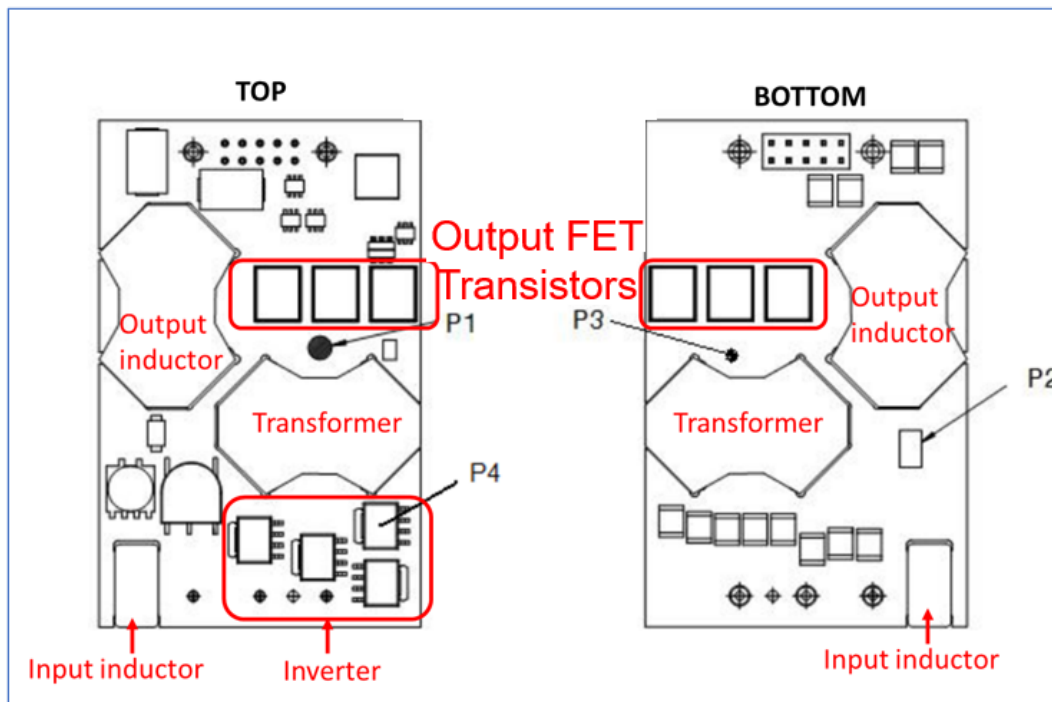
Position	Description	Max temperature
P1	PWB (reference point)	$T_{P1}=125^{\circ}\text{C}$
P2	Opto-coupler	$T_{P2}=105^{\circ}\text{C}$
P3	PWB (reference point for base-plate version)	$T_{P3}=125^{\circ}\text{C}$
P4	Primary MOSFET	$T_{P4}=125^{\circ}\text{C}$



See Ex. 1007 at 24 (annotated). There are three identical components next to this P4 component, which a POSITA would recognize as the other three inverter MOSFETS, consistent also with the photograph of the converter showing a total of four identical MOSFET devices in this position.

63. There are six identical power semiconductor devices on the board just above “P1” and “P3” shown in the diagram above. A POSITA would have at least found it obvious that three of the power semiconductor devices comprised one output switch, while the other three power semiconductor devices comprise the second output switch. Ericsson-BMR is a step-down converter. The converter’s output carries high current (up to 60A depending on the model). A POSITA would have known that multiple devices in parallel would comprise each output switch, since the three FETs can share effort to satisfy a high current requirement.

64. The four primary side inverter FETs interface directly to the transformer in the schematic. The transformer has been discussed above as a planar magnetic component in the middle of the board, physically near these FETs. Thus, a POSITA could ultimately identify the components on the Ericsson-BMR PCB as follows:

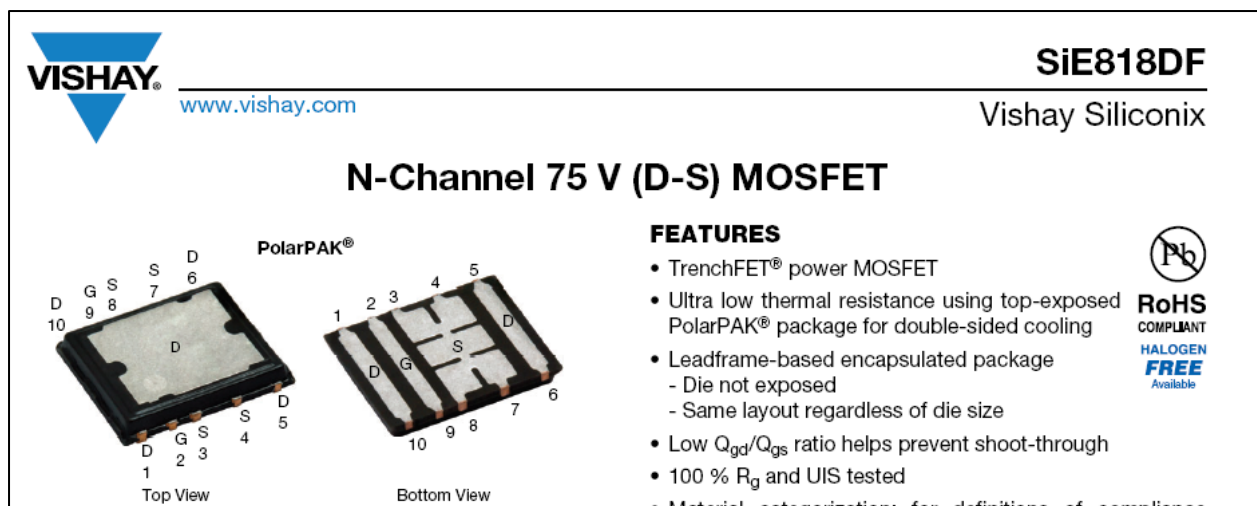


See Ex. 1007 at 24 (annotated).

65. This analysis is further supported by inspection of high-resolution photos of the Ericsson-BMR module from the time, which says “E818” at the top of each of output FET transistors:



See Ex. 1014 (cropped). A POSITA would have obviously expected that these components are power semiconductor devices. A POSITA would have been able to determine these semiconductor devices, labeled “E818” components in the picture, as a type of MOSFET power semiconductor device made for example, by Vishay. A data sheet for these E818 parts from this time lists the device specification and shows a picture of the E818 device that matches the top side MOSFET in the Ericsson-BMR picture:

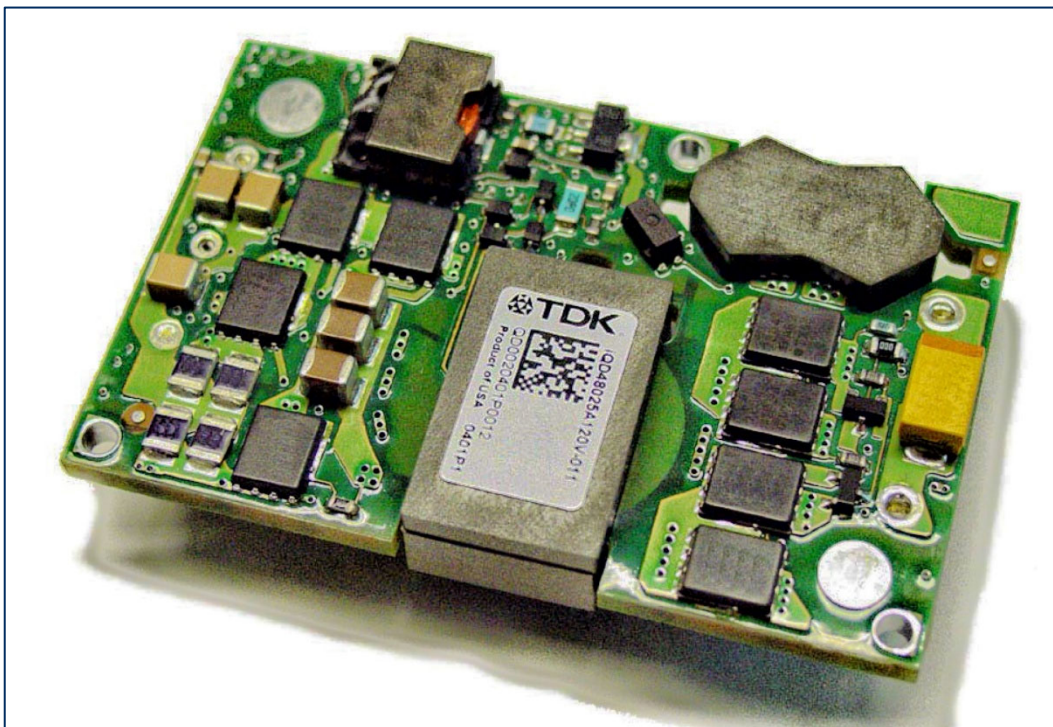


See Ex. 1027 at 1. This data sheet identifies applications of this MOSFET as including “synchronous rectification,” and a POSITA would have known that this

type of MOSFET transistor was used in two groups of three devices each to implement the secondary side rectifiers in this power converter module.

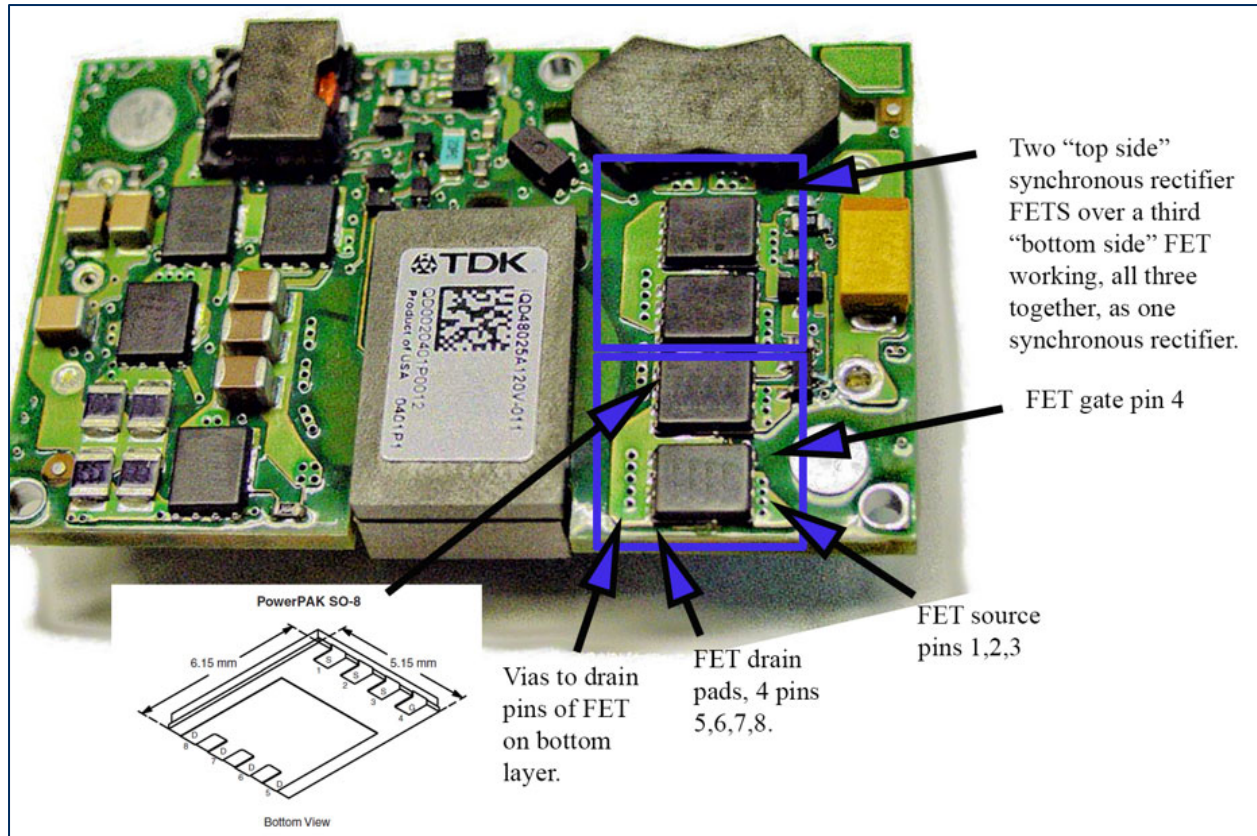
66. The power semiconductor devices are electrically connected and would dissipate some amount of power at a particular level (P_t for the top power semiconductor devices in the parlance of the '761 patent, and P_b for the bottom power semiconductor devices in the parlance of the '761 patent) during operation of the power converter. *See* Ex. 1008 at 2-3.

67. As a POSITA would have known, this type of arrangement of power semiconductor devices was common in prior art converters. For example, a picture of the TDK IQD48025A bus converter is shown below:



See Ex. 1029 at 1. Thus power converter seen in Exhibit 1029 is similar in structure and type to the Ericsson BMR series power converter discussed in Ericsson-BMR. This TDK converter is, according to the datasheet, provided in an “industry standard 300W quarter brick power module.” The converter is offered with either a 12 volt or 9.6 volt output (just like the BMR series). The converter in the picture is a 12 volt output “120” style converter according to the datasheet.

68. A POSITA would have recognized that the TDK power converter employed similar layout features, techniques, and circuit design in comparison to Ericsson’s BMR module depicted in Ericsson-BMR. The TDK converter includes a magnetic core in the center of the board that serves as a transformer that provides “isolation” as described in the datasheet. *See* Ex. 1029 at 12. The TDK power converter image shows four “synchronous rectifier” MOSFETs on the “top side” of the board as shown below:

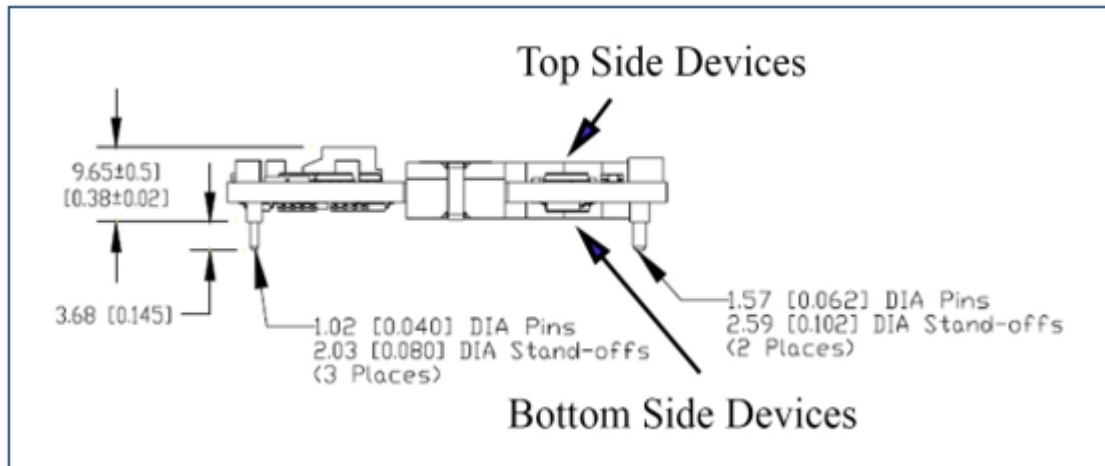


See Ex. 1029 at 1 (annotated).

69. The number 7884 is visible with careful inspection on the top synchronous rectifier in the photograph. The schematic of the synchronous rectifier MOSFET inset into the photograph in the annotation above shows the underside pinout for an “Si7884” MOSFET produced by manufacturers like Vishay at the time. See, e.g., Ex. 1030 at 1 (describing the “PowerPAK SO—8” packaged N-Channel MOSFET suitable for applications as a “Synchronous Rectifier”).

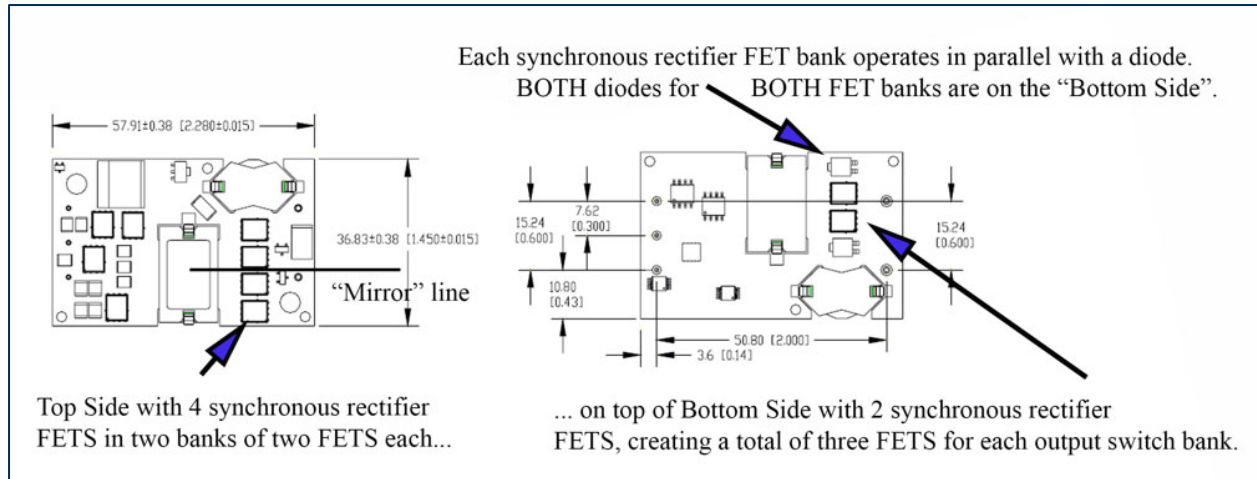
70. The TDK datasheet shows additional schematic drawings of the TDK converter. For example, this “side view” drawing shows that components are

mounted on both the top and bottom side of the board, with an annotation arrow pointing to “Top Side Devices” that include the 7884 synchronous rectifier MOSFETS:



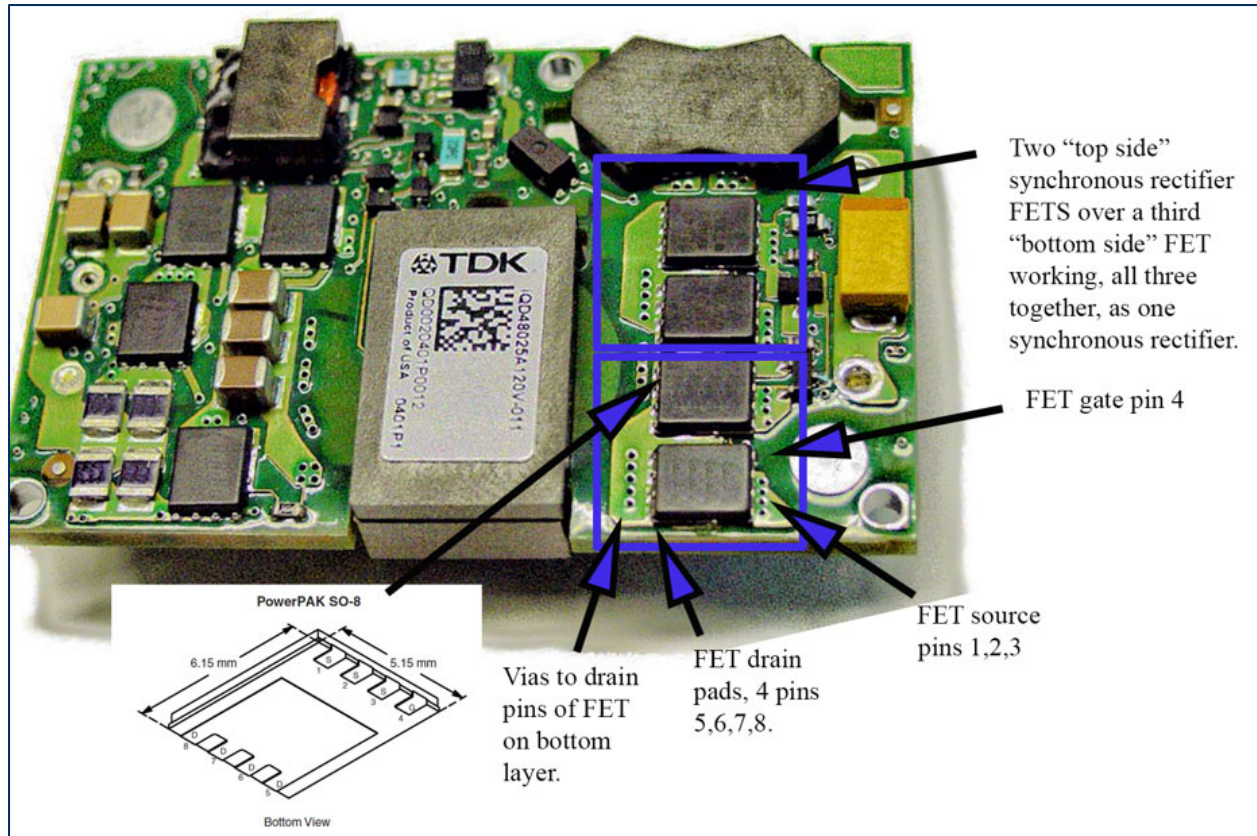
See Ex. 1029 at 3 (annotated).

71. The TDK datasheet also shows schematic drawings of the “top side” and “bottom side” of the converter, including component diagrams showing the four synchronous rectifier transistors on the top side, and two additional synchronous rectifier transistors on the bottom side underneath the top side synchronous rectifier transistors:



See Ex. 1029 at 3 (annotated). That is, the datasheet indicates a total of six synchronous rectifiers are employed in the TDK converter, similar to the components in the Ericsson-BMR module. Also, the datasheet drawings include drawings for packages that a POSITA would have recognized as corresponding to conventional or Schottky diodes on the bottom side, one for each bank of three synchronous rectifiers. The TDK converter thus includes four synchronous rectifiers on the top side dissipating power, and four other semiconductor devices including two synchronous rectifiers and two diodes on the bottom side that would also dissipate power.

72. The solder mask or light green coloration on the top side of the board, along with the clearly visible via holes on the PCB, would have indicated to a POSITA how the synchronous rectifiers are likely organized or electronically connected:



See Ex. 1029 at 1 (annotated).

73. The drains of the transistors are connected together as indicated by the blue boxes and annotations. In particular, the mounting arrangement, PCB via locations, and solder mask would have indicated to POSITA that the “lower two transistors” on the top side work together with one of the transistors on the “bottom side,” and also likely, or at least obviously, one of the diode rectifiers on the bottom side. Similarly, the “upper two transistors” in the upper blue box on the top side work together with the other transistor on the “bottom side” and its associated diode rectifier. This arrangement reveals a similar situation to the Ericsson-BMR module with an important difference. Again, the TDK converter, like the BMR,

uses a combination of “three and three” synchronous rectifier transistor MOSFETS to produce the output. As a POSITA would have readily appreciated, however, the arrangement in the TDK converter uses “two on the top and one on the bottom” for the transistors to produce each composite output switch from a collection of three MOSFETS and also a passive diode.

74. A POSITA would have been well aware that: collections of transistors could be used to form a composite switch in a power converter; that these collections of transistors could be arranged on the top and bottom of a printed circuit board or other electronic structure; and that individual transistors in the collections on one side of the printed circuit could be connected using PCB vias to transistors in the same composite switch on the other side of the printed circuit. The TDK converter deploys composite switches made with two transistors on the “top side” placed over a single additional transistor and passive diode on the “bottom side.” These two different examples (*i.e.*, Ericsson-BMR and the TDK converter) therefore demonstrate that the location of these transistors is a design choice selected by POSITA from a finite number of reasonable arrangement options that would produce predictable results with a high likelihood of successful implementation.

- f. **1[e]: wherein the power semiconductor devices are distributed between the first and second sets to distribute heat generation during operation of the**

converter such that each level Pt, Pb is less than 150% of the other level Pb, Pt.

75. In my opinion, Ericsson-BMR teaches and renders obvious this element.

76. As discussed in the previous element, there are three relevant power semiconductor devices on the top and bottom of the PCB, which would dissipate power during operation of the power converter. A POSITA would have known, or at least found obvious, that the current and voltage (and thus, power) through the top three power semiconductor devices would be equal (or at least approximately equal) over time to the bottom three power semiconductor devices, for the following reason.

77. As background, the circuit employed by Ericsson-BMR (pictured above on page 5 of Ericsson-BMR) uses a full-bridge inverter to drive the transformer primary and a center-tapped transformer secondary with synchronous rectification, similar to the full-bridge transformer-isolated buck converter shown in the *Fundamentals* textbook (Exhibit 1008) at Figure 6.18. A POSITA would have known, and found it obvious, to operate a full-bridge circuit with balanced AC excitation (*i.e.*, the four-switch inverter on the primary side of the transformer shown above would operate with balanced excitation of the primary) to avoid transformer saturation.

78. A POSITA would have known that to avoid saturation of the magnetic core material, the circuit must be operated such that there is little-to-no average voltage (or “DC voltage”) across the transformer terminals. As shown in *Fundamentals* (Ex. 1008) at Figure 6.18, a transformer was well-known to have a magnetizing inductance. The current (i_M) through this inductance is determined by the integral of voltage across the transformer primary:

$$i_M(t) = \frac{1}{L_M} \int v_T(t) \cdot dt$$

If v_T has a sufficient non-zero average, then i_M increases during the converter’s operation until it is large enough to saturate the magnetic material which comprises the core.

79. A POSITA would also have known that a power electronic converter is operated using a periodic switching command and that the waveforms of the converter are also periodic in nominal (or “steady-state”) operation. The voltage v_T is produced directly by the full-bridge input and a POSITA would have known that the full-bridge applies a voltage v_T that comprises values in the set $\{-V_{IN}, 0, V_{IN}\}$. For v_T to have zero average, the average of one period of v_T must also have zero average. This means that over one period, v_T must be equal to V_{IN} for the same amount of time that it is equal to $-V_{IN}$. A POSITA would have known that a common value for v_T in this converter which has zero average over one period is

$$v_T(t) = \begin{cases} V_{IN}, & t \in (0, DT_s) \\ 0, & t \in (DT_s, T_s) \\ -V_{IN}, & t \in (T_s, T_s + DT_s) \\ 0, & t \in (T_s + DT_s, 2T_s) \end{cases}$$

where t denotes time, $2T_s$ is the time of one switching period, and DT_s is the amount of time where v_t is equal to V_{IN} (equal to the time when $v_T = -V_{IN}$, to ensure zero average value over the entire full switching period $2T_s$). The primary voltage v_T is reflected through the transformer to the secondary windings. A POSITA would have known that when $v_T = V_{IN}$, one rectifier or switch device on the secondary side of the schematic must be on, since a MOSFET power semiconductor device serving as a synchronous rectifier cannot block a negative voltage between the Drain and Source terminals. When this rectifier (which may be and is in the BMR a composite of several transistors) is on, it carries the full output inductor current. Similarly, when $v_T = -V_{IN}$, the alternate synchronous rectifier is “on” and carries the full output inductor current. If $v_T = 0$, both synchronous rectifiers conduct and carry approximately one-half of the output inductor current. The result is that these devices support substantially identical current waveforms, phase-shifted in time by T_s . A POSITA would also have known that any differences in the current carried by the two rectifier devices is small. This entire description of operation was well known to a POSITA and is illustrated, for example, in the *Fundamentals* textbook (Exhibit 1008) at Figure 6.19 and the associated text description at pages 149-151 therein.

80. This basic knowledge regarding the proper way to drive a full-bridge circuit is reflected throughout the prior art. *See, e.g.*, Ex. 1008 at 148 (“So the magnetizing current is determined by the integral [over time] of the applied

winding voltage. The principle of inductor volt-second balance also applies: when the converter operates in steady-state, the dc component of voltage applies to the magnetizing inductance must be zero.... Otherwise, during each switching period there will be a net increase in magnetizing current, eventually leading to excessively large current and transformer saturation.”), 150 (“[T]he transformer causes $i_{D5}(t)$ [the current through the top power semiconductor device in their example] and $i_{D6}(t)$ [the current through bottom power semiconductor device] to be *equal* in magnitude”), Fig. 6.19 (showing symmetric wave forms for a full-bridge converter).

81. A POSITA would have recognized that the voltage, current, and power through the top three power semiconductor devices in the BMR is equal (or at least approximately equal) to the voltage, current, and power through the bottom three power semiconductor devices in the BMR over time. Therefore, a POSITA was well aware that the power dissipation levels of the top side three MOSFETS and of the bottom side three MOSFETS (P_t and P_b , respectively) are equal (or at least approximately equal) and therefore well within the mutual 150% threshold required by this claim element. This is the logical result that two sets of identical electrical structures being driven by the same power over time would have the same performance characteristics, as the prior art recognized and as a POSITA

would have been aware, for the relevant particular environment and configuration of elements.

82. Additionally, the TDK converter further supports that a POSITA would have known to balance the dissipation on the top and bottom of the converter. While the top side contains two of the three MOSFETS forming each synchronous rectifier and the bottom side includes the third, the bottom side also includes both of the diode rectifiers apparently employed in parallel with the synchronous rectifier MOSFETS. Therefore, the TDK converter presents four devices on the top side of the converter dissipating P_t , and four other devices on the bottom side dissipating P_b . While the four devices on the bottom consist of two FETS and two rectifiers, the placement of these power semiconductor devices further supports that a POSITA would have known that the components can be organized to help balance and equalize the dissipation on the top and bottom.

2. Claim 2

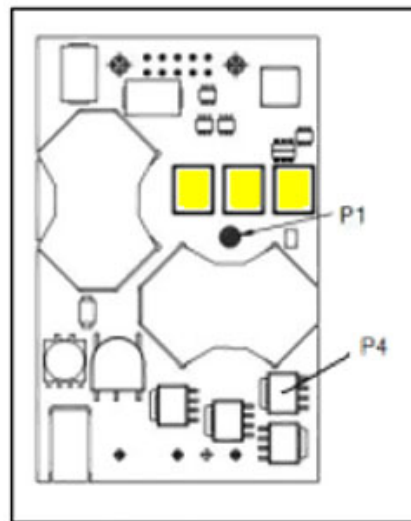
- a. The apparatus of claim 1 wherein a plurality of the power semiconductor devices in the first set are each positioned in a location on the top surface substantially overlapping a location on the bottom surface occupied by a power semiconductor device in the second set.**

83. In my opinion, Ericsson-BMR renders obvious Claim 2.

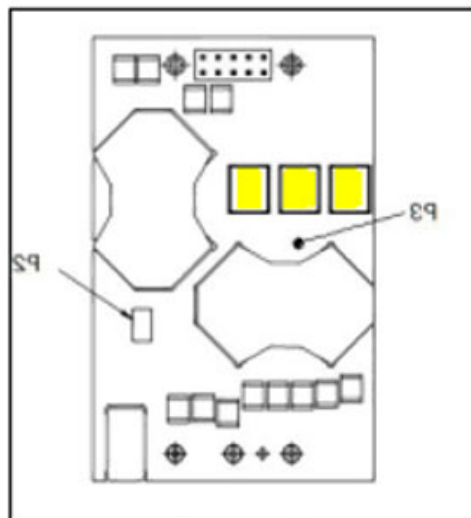
84. As discussed above, Ericsson-BMR renders obvious Claim 1. As discussed further below, in my opinion, Ericsson-BMR teaches wherein a plurality

of the power semiconductor devices in the first set are each positioned in a location on the top surface substantially overlapping a location on the bottom surface occupied by a power semiconductor device in the second set.

85. By reference to the the “Top view” and “Bottom view” of the Ericsson-BMR apparatus on page 24 of Exhibit 1007, turning over the “Bottom view” demonstrates that the three bottom power semiconductor devices (highlighted in yellow) are directly under, and thus substantially overlap, the three top power semiconductor devices:

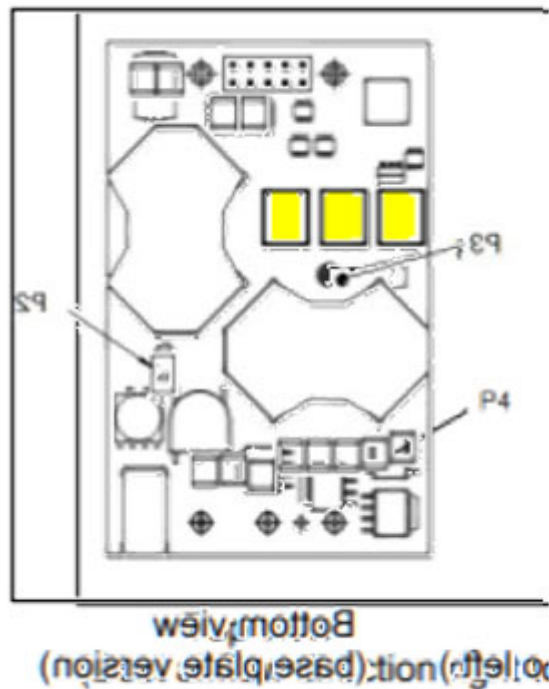


Top view
(Best airflow direction right to



Bottom view
(base plate version) (left)

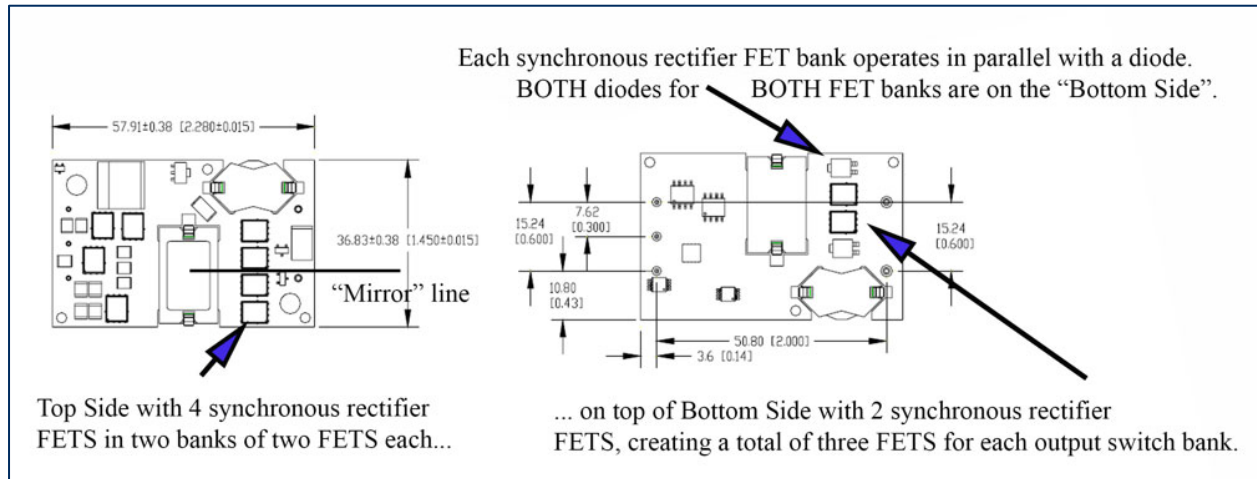
Ex. 1007 at 24 (modified). This is further confirmed by overlaying the images of the top and bottom views of the Ericsson-BMR, further confirming that the top three power semiconductor devices and the bottom three power semiconductor devices are directly overlapping each other (as are the planar magnet bowtie shapes as well, as expected):



Ex. 1007 at 24 (modified). A POSITA would have therefore understood that, in Ericsson-BMR's module, a plurality of the power semiconductor devices in the first set (*i.e.*, the top three power semiconductor devices, highlighted in yellow) are each positioned in a location on the top surface directly overlapping a location on the bottom surface occupied by a power semiconductor device in the second set (*i.e.*, the corresponding bottom three power semiconductor devices, also highlighted in yellow).

86. Similarly, the TDK converter also employs two banks of semiconductor devices as output rectifiers, including three MOSFETs in a "first set" and three MOSFETs in a "second set," where two of the MOSFETs in each

set are on the top side of the converter PCB, overlapping one MOSFET on the bottom side of the converter PCB, as shown below:



See Ex. 1029 at 3 (annotated).

3. Claim 3

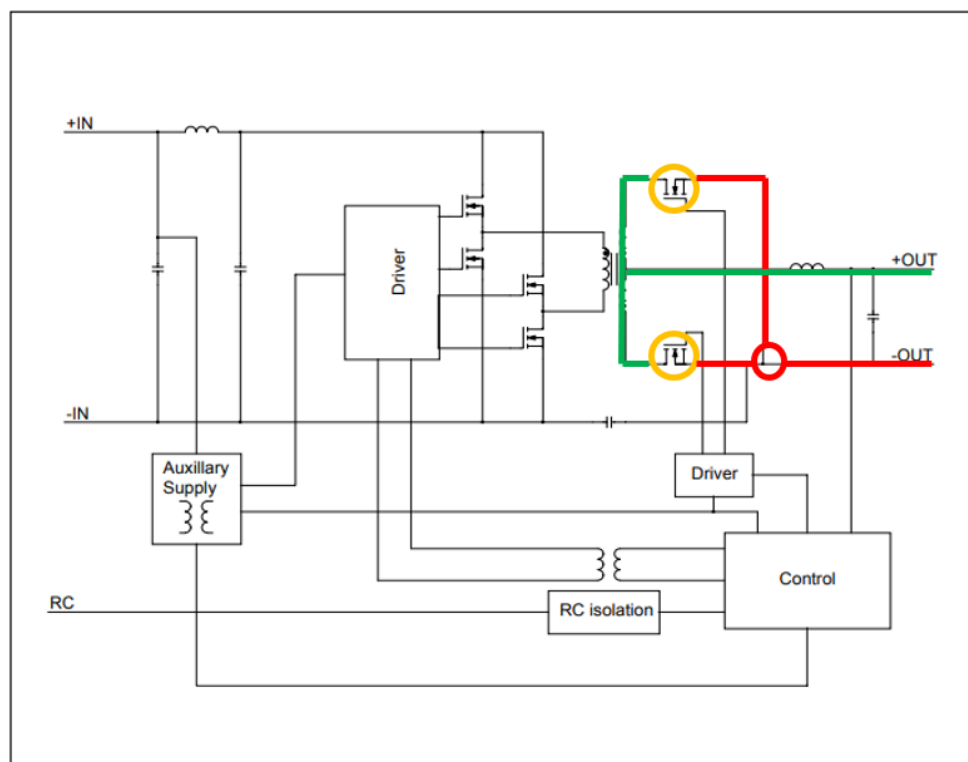
- a. The apparatus of claim 1 wherein the power semiconductor devices are electrically connected using a respective set of conductive vias in the PCB, and a plurality of the power semiconductor devices in the first set share their respective sets of conductive vias with corresponding power semiconductor devices in the second set.

87. In my opinion, Ericsson-BMR renders Claim 3 obvious.

88. As discussed above, Ericsson-BMR renders obvious Claim 1. As discussed further below, in my opinion, Ericsson-BMR teaches or at least renders obvious the power semiconductor devices are electrically connected using a respective set of conductive vias in the PCB, and a plurality of the power

semiconductor devices in the first set share their respective sets of conductive vias with corresponding power semiconductor devices in the second set.

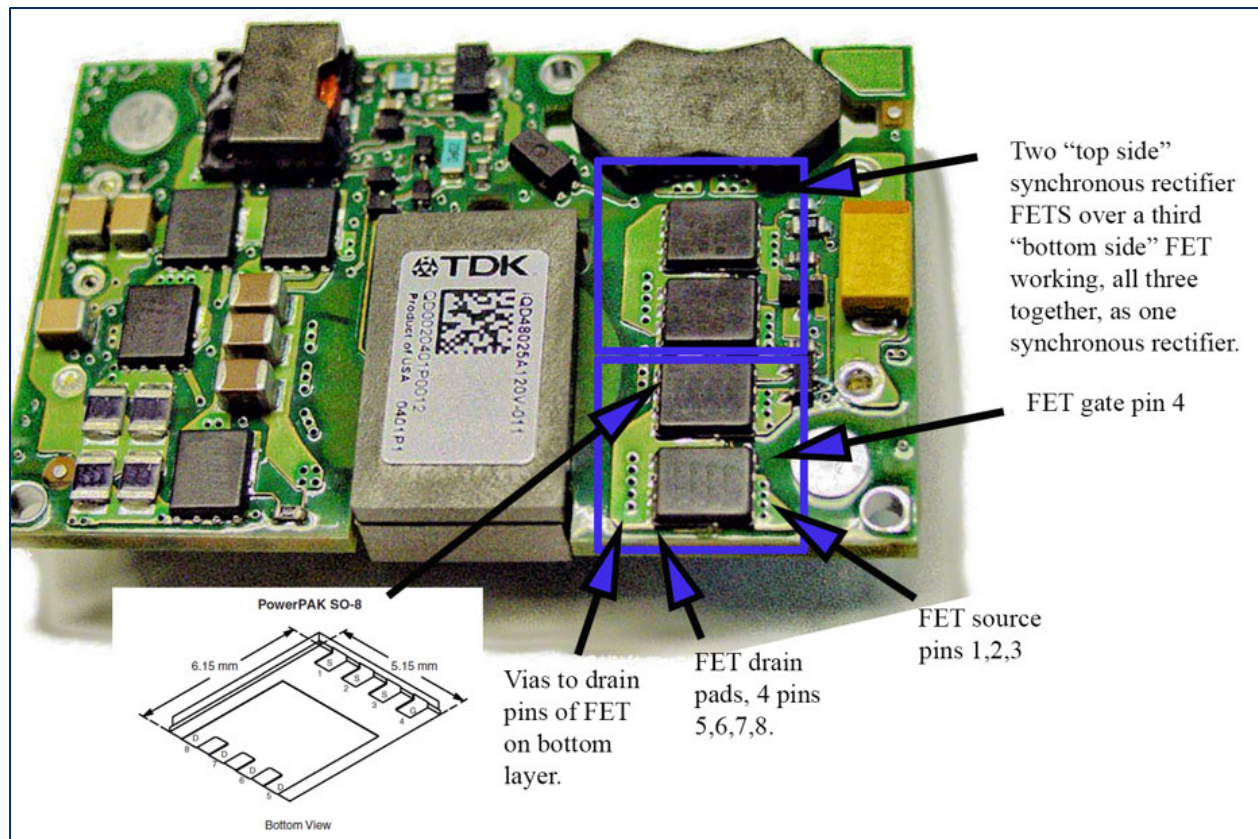
89. By reference to Ericsson-BMR's circuit diagram, the output power semiconductor set on the top of the schematic (circled in orange at the top of the diagram below) shares a common connection (circled and outlined in red, for example, and also shown in green) with the output power semiconductor set on the bottom of the secondary side in the schematic (circled in orange at the bottom of the diagram below):



See Ex. 1007 at 5 (annotated). As discussed above in Claim 1[d], the output switches are comprised of power semiconductor devices on the top and bottom of the power converter module. Therefore, in view of the connections depicted in the

circuit diagram above, power semiconductor devices in each of the first and second sets are electrically connected and share their respective sets of conductive connections with corresponding power semiconductor devices in the other set. As a POSITA was well aware, vias function as electrical connections through the PCB layers and were (and still are) a common approach for connections between components on different layers of a PCB. Thus, a POSITA would have expected, or at least found obvious, that the power semiconductor devices in the first set of the output FETs on the top side of Ericsson-BMR module shared their respective set of conductive vias with the power semiconductor devices in the second set of the output FETs on the bottom side of the Ericsson-BMR module.

90. The TDK converter further supports that it would have been obvious to a POSITA to have a plurality of power semiconductor devices in the first set (on top of the PCB) share their respective sets of conductive vias with corresponding power semiconductor devices in the second set (on the bottom of the PCB). In this picture from the TDK IQD datasheet, it is clear that the drain pin connections of the top two (a plurality) MOSFETs in one of the composite output rectifiers is connected to the drain pin of the third, bottom-side MOSFET (the third MOSFET synchronous rectifier in the second set):



See Ex. 1029 at 1 (annotated). That is, a POSITA would have known that there are a variety of well-known configurations that meet the additional limitation of Claim 3.

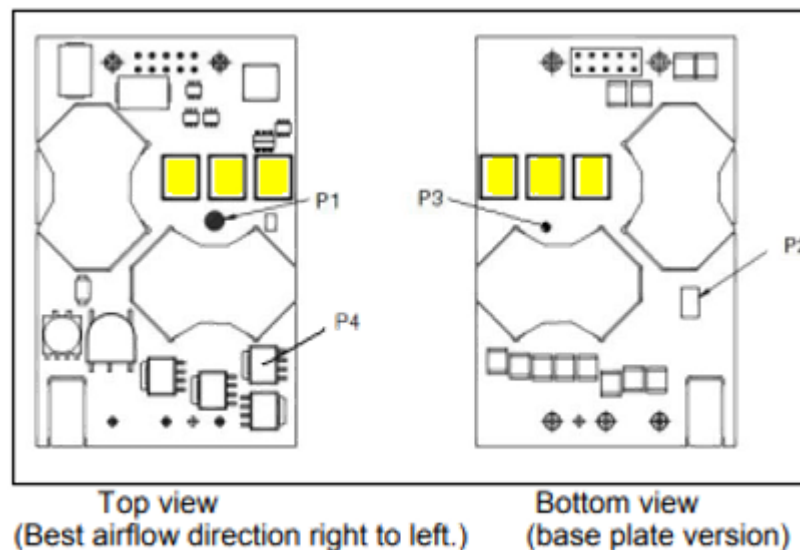
4. Claim 4

- a. The apparatus of claim 2 wherein the power converter further comprises circuitry including a pair of cells having a common circuit topology and each including power semiconductor switches from each of the first and second sets; each cell having its respective components arranged in a pattern, wherein the pattern of components of one cell is substantially a mirror image of the pattern of components in the other cell.

91. In my opinion, Ericsson-BMR renders obvious Claim 4.

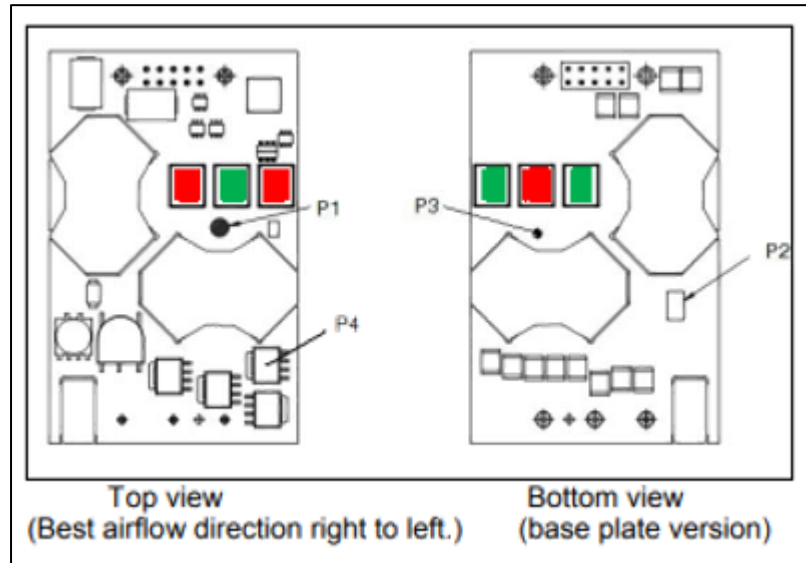
92. As discussed above, Ericsson-BMR renders obvious Claim 2. As discussed further below, in my opinion, Ericsson-BMR also renders obvious the claim limitation that the power converter further comprises circuitry including a pair of cells having a common circuit topology and each including power semiconductor switches from each of the first and second sets; each cell having its respective components arranged in a pattern, wherein the pattern of components of one cell is substantially a mirror image of the pattern of components in the other cell.

93. As discussed above in Claim 1[d], a POSITA would have recognized the six identical components highlighted below as two sets of three MOSFETs comprising the two output switches:



Ex. 1007 at 24 (annotated). However, Ericsson-BMR is not explicit as to which of the three MOSFETs on each side correspond to the two output switches shown in

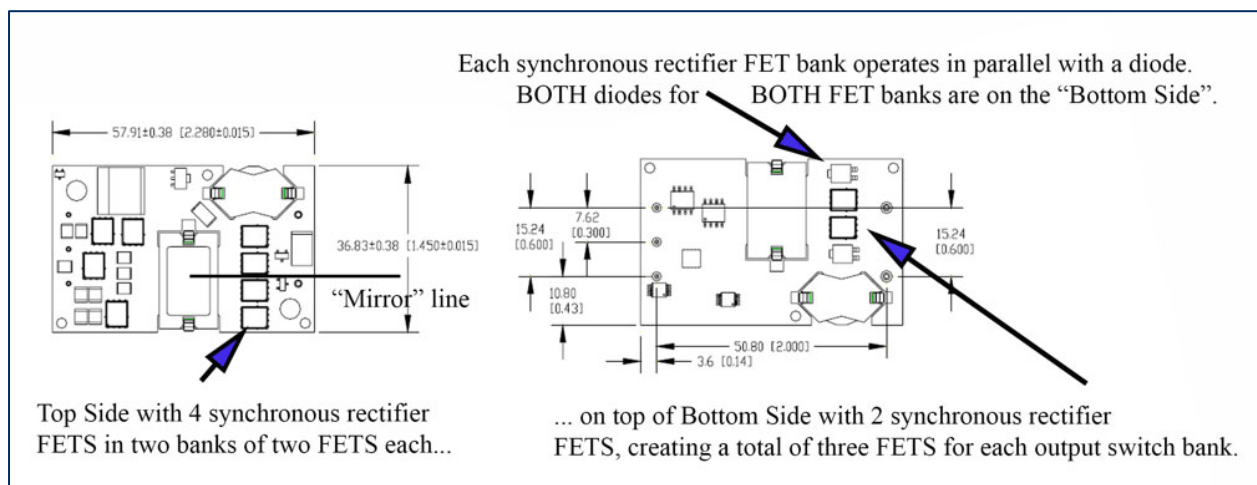
Ericsson-BMR's fundamental circuit diagram (Ex. 1007 at 5). There are a small number of possible combinations that could apply. From basic math, there are $C(6,3) = 20$ combinations (*i.e.*, there are 20 ways to choose three items of six). Ericsson-BMR does not teach away from any one of these combinations, and there would be no strong motivation for a POSITA against assigning the FETs as follows, where the green-highlighted FETs correspond to one output switch and the red-highlighted FETs correspond to the other output switch:



See Ex. 1007 at 24 (annotated). This arrangement would have been obvious to a POSITA at least because it was obvious to try, in particular a choice among a finite (*i.e.*, 20) set of combinations of readily identifiable, predictable solutions, with a reasonable expectation of success given the purpose of the FETs in the context of Ericsson-BMR's fundamental circuit diagram (Ex. 1007 at 5) that teaches the use of output switches.

94. In this arrangement, each of these output switches is a cell having the same circuit topology and each includes FET power semiconductor devices from the top and bottom surfaces (*i.e.*, from the first and second sets). Each cell has its respective components arranged in a pattern wherein the pattern of components of one cell is a mirror image, over an axis co-planar with the PCB, of the pattern of components in the other cell.

95. The TDK converter provides further evidence that this arrangement would have been obvious, and was well-known, to a POSITA. The TDK converter has its six output synchronous rectifier FETS organized in two cells with “two FETS on top” and “one FET on the bottom.” The connections would have been obvious to a POSITA from the photograph in the datasheet based on the vias and solder mask, and the diagrams in the datasheet show the arrangement on the top and bottom as shown below:



See Ex. 1029 at 3 (annotated). The two cells are “mirrored” around a “mirror line” added in the annotation as shown above.

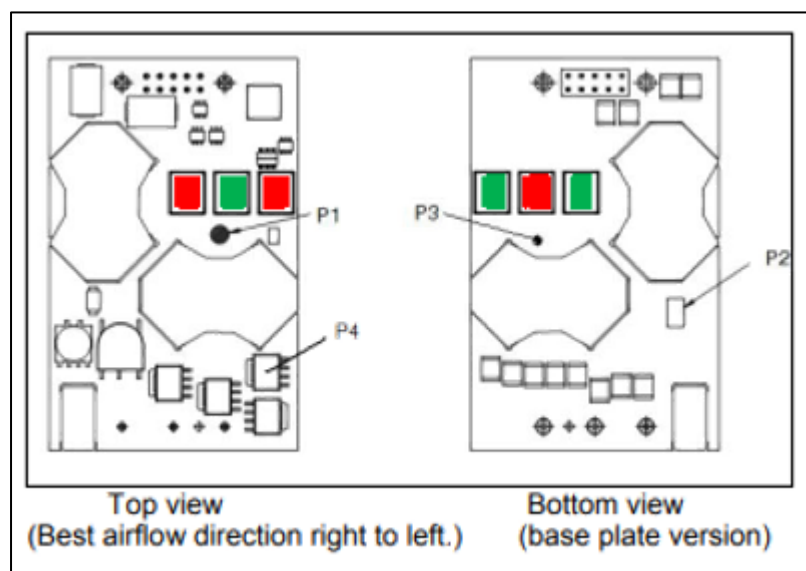
5. Claim 5

- a. The apparatus of claim 4 wherein a component from one of the cells is located on an opposite surface of a respective component from the other one of the cells.**

96. In my opinion, Ericsson-BMR renders obvious Claim 5.

97. As discussed above, Ericsson-BMR renders obvious Claim 4. As discussed further below, in my opinion, Ericsson-BMR renders obvious “a component from one of the cells is located on an opposite surface of a respective component from the other one of the cells.”

98. As discussed above in Claim 4, the (for example) middle MOSFET of the first output switch is on the opposite surface of the middle MOSFET of the second output switch, as indicated by the red/green distinction:



See Ex. 1007 at 24 (annotated). This arrangement is one of a finite number of obvious choices to a POSITA that would achieve predictable results, as discussed in the context of Claim 4. And, as also discussed in the context of Claim 4, the TDK converter taught two cells arranged around a mirror line where each cell included components on the top and the bottom of the PCB. Therefore, as with Claim 4, a POSITA would have known and found obvious to locate a component of one cell on an opposite surface of a respective component from the other cell.

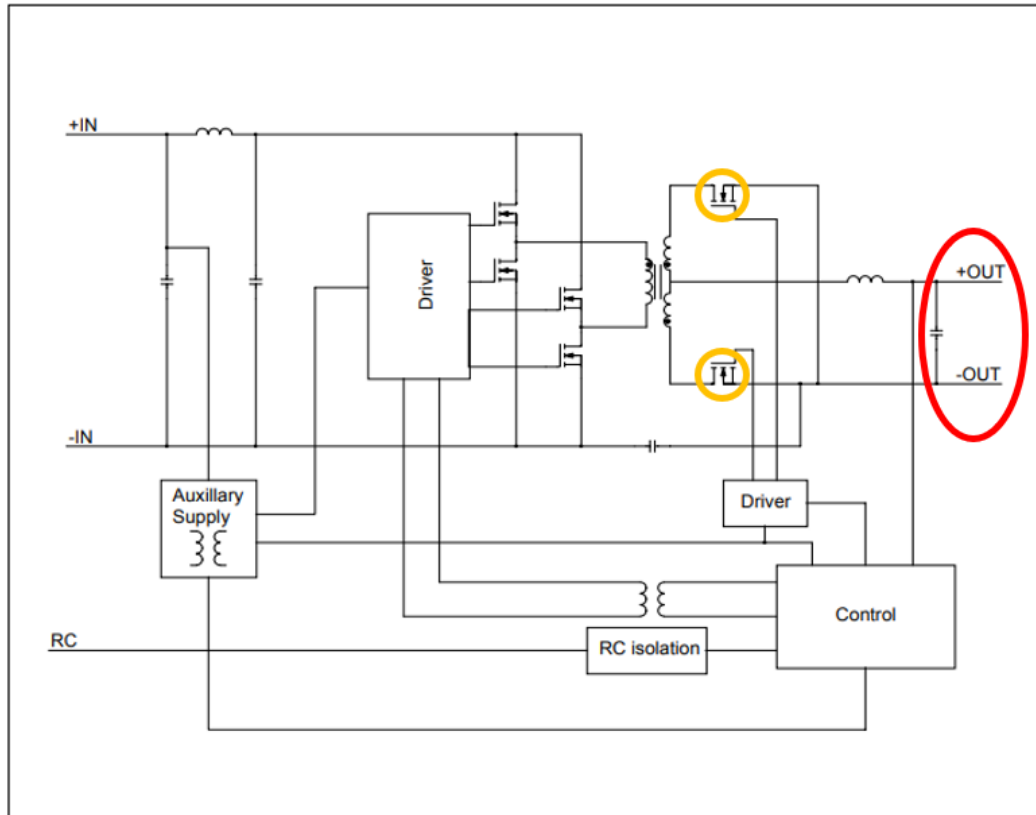
6. Claim 7

a. The apparatus of claim 3 wherein the power semiconductor devices comprise output switches.

99. In my opinion, Ericsson-BMR renders obvious Claim 7.

100. As discussed above, Ericsson-BMR renders obvious Claim 3. As discussed further below, in my opinion, Ericsson-BMR teaches or at least renders obvious the power semiconductor devices comprise output switches.

101. As shown in Ericsson-BMR's fundamental circuit diagram, the two components circled in orange are switches, as a POSITA would have recognized those symbols as the symbols for transistor switches. *See* Ex. 1008 at, *e.g.*, Fig. 2.13(b). And those two switches are electrically connected to, and switch on or off, conduction paths to the "OUT" terminals of the circuit circled in red, such that a POSITA would have recognized those switches as output switches providing rectification to create the output voltage:



And as discussed above in Claim 1[d], the two output switches are comprised of the six MOSFET devices on the top and bottom of the PCB. Thus, the MOSFET power semiconductor devices are output switches. *See also* Ex. 1029.

7. **BMR-2008**

102. The relevant teachings of BMR 2008 are substantially the same as the relevant teachings of Ericsson-BMR. *Compare* Ex. 1007 at, *e.g.*, 1, 2, 5, 24, 31 *with* Ex. 1026 at, *e.g.*, 1, 4, 15, 20. For example, BMR 2008 and Ericsson-BMR both teach the same top-bottom symmetry of output switch FETs, and the same fundamental circuit diagram. *See id.* The commonality of BMR 2008 and Ericsson-BMR would have been expected by a POSITA, as they both describe (for example)

similar output products in the same BMR453 product line, with substantially similar product specifications and nearly identical component layouts in the photographs and fundamental schematics provided in the documents.

103. As a result of the substantial similarity in teaches between Ericsson-BMR and BMR 2008, Claims 1-5 and 7 are rendered obvious by BMR 2008 for the same reasons as they are rendered obvious by Ericsson-BMR that I set forth above in this Ground.

B. Ground II: Claim 1-5, 7 Are Rendered Obvious By Ericsson-BMR In View Of Spiazzi Or, Alternatively, By BMR-2008 In View Of Spiazzi

1. Claim 1

104. In my opinion, Claim 1 is rendered obvious by Ericsson-BMR in view of Spiazzi.

a. 1[preamble]¹

¹ For sake of brevity, starting in this Ground, I omit the complete language associated with each claim element. For reference, a claim listing is provided as an appendix at the end of this declaration which matches claim language to element number, in the same manner as I have done above in previous Ground I.

105. In my opinion, Claim 1[preamble] is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VIII.A.1.a.

b. 1[a]

106. In my opinion, Claim 1[a] is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VIII.A.1.b.

c. 1[b]

107. In my opinion, Claim 1[b] is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VIII.A.1.c.

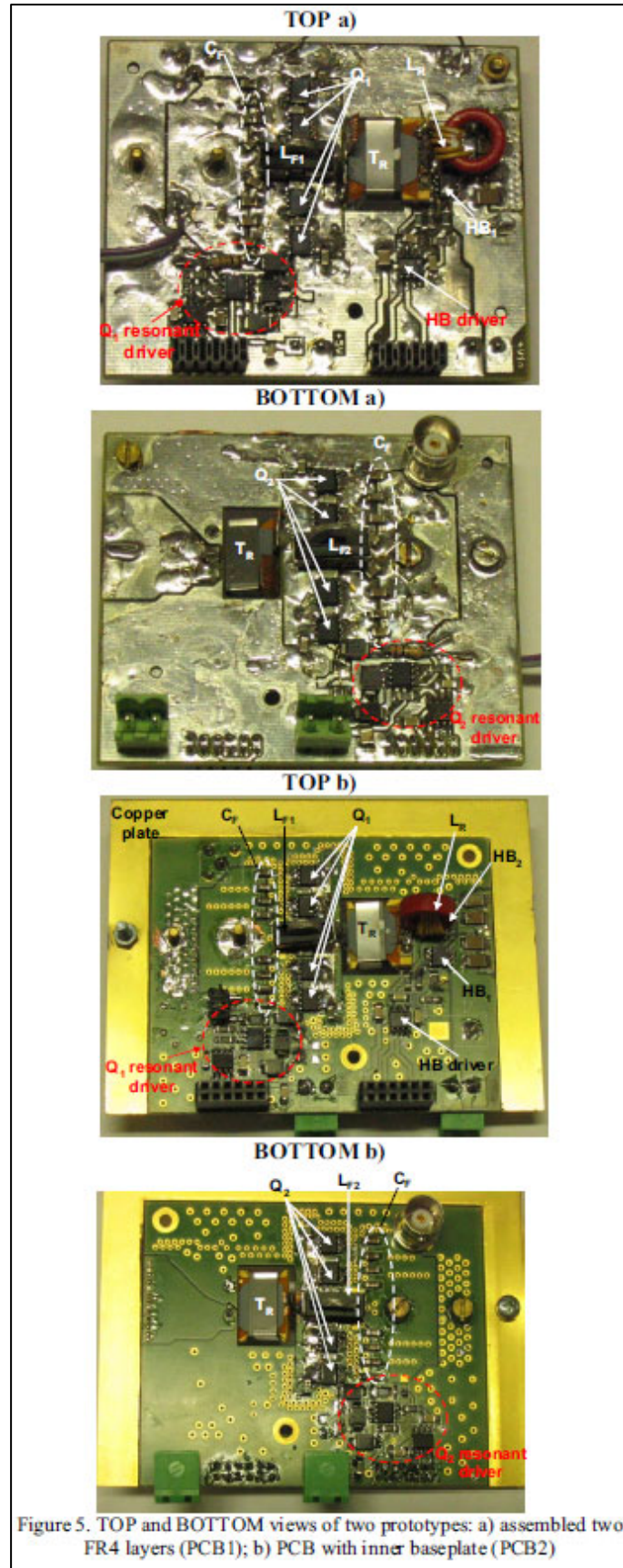
d. 1[c]

108. In my opinion, Claim 1[c] is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VIII.A.1.d.

e. 1[d]

109. In my opinion, Claim 1[d] is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VIII.A.1.e.

110. Spiazzi further confirms that, as a POSITA would have expected and found obvious, the overlapping devices in the Ericsson-BMR module are output FET power semiconductor devices. Spiazzi's Figure 5, for example, shows that in each of its two PCBs, the four output FETs (collectively labelled "Q1") on the top side of each board overlap with the four output FETs (collectively labelled "Q2") on the bottom side of each board:



Ex. 1011 at Fig. 5 (annotations in original).

f. 1[e]

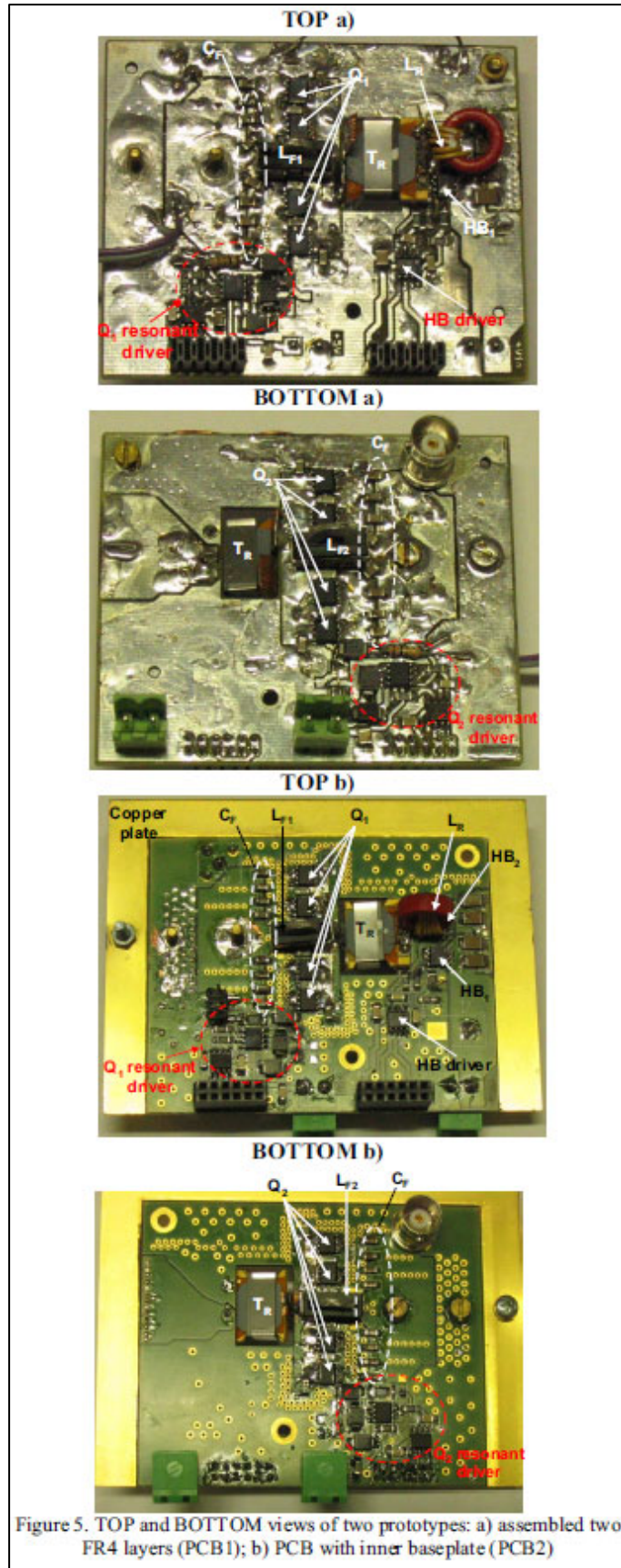
111. In my opinion, Claim 1[e] is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VIII.A.1.f.

112. Spiazzi further confirms that Ericsson-BMR's full-bridge circuit would produce substantially similar results of power dissipation on both sides of the Ericsson-BMR module. Spiazzi teaches a half-bridge converter, which, like Ericsson-BMR's full-bridge converter, would have at least obviously applied symmetrical power cycles in order to avoid saturating the transformer. *See* Ex. 1011 at Fig. 1.a ("half-bridge resonant VRM"). Spiazzi then performs a thermal mapping of two different configurations of its power converter, and shows the top sides of the two different configurations in Figure 11. *See* Ex. 1011 at 2000. Although only the top sides of the two different configurations are shown, Spiazzi teaches that "[s]imilar results were obtained for the downward surfaces." *See* Ex. 1011 at 1999. A POSITA would therefore have recognized that Ericsson-BMR, under similar cycling, would also have featured power dissipation levels P_t and P_b that would at least be "similar" and well within 150% of each other. *See id.*

2. Claim 2

113. In my opinion, Claim 2 is rendered obvious by Ericsson-BMR in view of Spiazzi. *See* §VIII.A.2.

114. Additionally, Spiazzi further teaches overlapping power semiconductor devices from the first (top) set and second (bottom) set. By reference to Spiazzi's Figure 5 shown below, a POSITA would have recognized that the green terminals and through-hole via patterns along the switches confirm alignment *See* §VIII.H.2.



See Ex. 1011 at Fig. 5 (annotations in original)

3. Claim 3

115. In my opinion, Claim 3 is rendered obvious by Ericsson-BMR in view of Spiazzi. See §VIII.A.3.

4. Claim 4

116. In my opinion, Claim 4 is rendered obvious by Ericsson-BMR in view of Spiazzi. See §VIII.A.4.

5. Claim 5

117. In my opinion, Claim 5 is rendered obvious by Ericsson-BMR in view of Spiazzi. See §VIII.A.5.

6. Claim 7

118. In my opinion, Claim 7 is rendered obvious by Ericsson-BMR in view of Spiazzi. See §VIII.A.6.

7. BMR-2008

119. The relevant teachings of BMR-2008 are substantially the same as the relevant teachings of Ericsson-BMR. Compare EX1007 at, e.g., 1, 2, 5, 24, 31 with EX1026 at, e.g., 1, 4, 13, 15, 20.

120. As a result, in my opinion, Claims 1-5 and 7 are rendered obvious by BMR-2008 in view of Spiazzi for the same reasons as they are rendered obvious by Ericsson-BMR in view of Spiazzi set forth in this Ground.

C. Ground III: Claim 1-7 Are Rendered Obvious By Ericsson-BMR In View Of Wanes, Or, Alternatively, By BMR-2008 In View Of Wanes

1. Claim 1

121. In my opinion, Claim 1 is rendered obvious by Ericsson-BMR in view of Wanes.

a. 1[preamble]

122. In my opinion, Claim 1[preamble] is taught by Ericsson-BMR in view of Wanes. *See* §VIII.A.1.a.

b. 1[a]

123. In my opinion, Claim 1[a] is taught by Ericsson-BMR in view of Wanes. *See* §VIII.A.1.b.

c. 1[b]

124. In my opinion, Claim 1[b] is taught by Ericsson-BMR in view of Wanes. *See* §VIII.A.1.c. *See also* Ex. 1009 at 4:33-34 (“primary windings are embedded in internal tracks in internal *layers* in PCB 104.”).

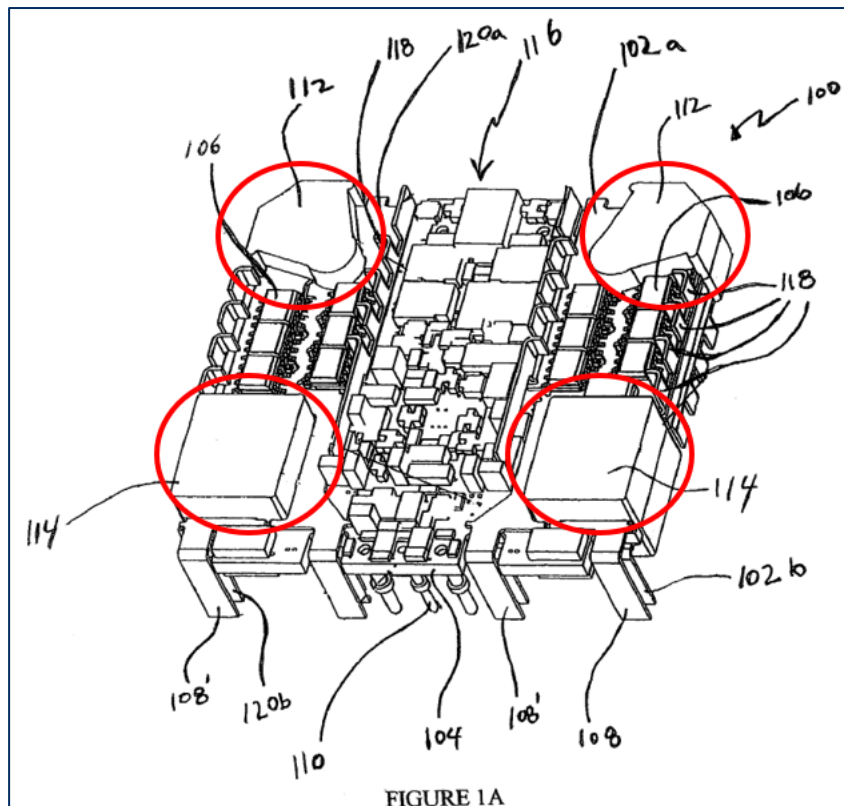
d. 1[c]

125. In my opinion, Claim 1[c] is taught and rendered obvious by Ericsson-BMR in view of Wanes. *See* §VIII.A.1.d.

126. If Ericsson-BMR is not found to have taught, or at least rendered obvious, this element, then in my opinion, Wanes teaches this.

127. Wanes teaches a magnetic core structure that is magnetically coupled to windings. For example, with reference to elements 112 and 114 circled in red below in Figure 1A, Wanes teaches:

It will be appreciated that transformer 112 and inductor 114 both belong to a family of signal transforming components which are known in the art as “magnetics”. Magnetics typically have a winding such a[s] winding 112A and 114A interacting with a magnetic core, such as 112C and 114B respectively.



Ex. 1009 at 4:45-50, Fig. 1A (annotated).

128. Wanes further teaches that the windings are formed by traces in one or more of the conductive layers in the PCB. For example, Wanes teaches that

“primary windings are embedded in internal layers in 104,” where element 104 is the PCB as discussed in the previous element. *See* Ex. 1009 at 4:10-12, 4:31-48, 9:44-51 (“Windings (not shown) are sandwiched within each PCB and encircle openings 414 and 416. Each winding of PCB 104 cooperates with a respective winding of the magnetics of transformer 112 and inductor 14....”). Because the winding traces carry current as part of the physics of the voltage conversion process, the layer of the PCB in which those winding traces are found are conductive.

129. A POSITA would have been motivated to form Ericsson-BMR’s windings in the manner described in Wanes for a number of reasons. For example: (1) it is more space efficient; and (2) as depicted above in the pictures of the Ericsson-BMR module (*e.g.*, Ex. 1007 at 1), the layers of the PCB provide the only space visible for the traces. *See* §VIII.A.1.d. Additionally, forming the windings in this manner was a well-known technique, and thus a POSITA would have had a reasonable expectation of success in doing so. *See, e.g.*, Ex. 1019 at 1:54-60.

e. 1[d]

130. In my opinion, Claim 1[d] is taught and rendered obvious by Ericsson-BMR in view of Wanes. *See* §VIII.A.1.e.

f. 1[e]

131. In my opinion, Claim 1[e] is taught and rendered obvious by Ericsson-BMR in view of Wanes. *See* §VIII.A.1.f.

2. Claim 2

132. In my opinion, Claim 2 is rendered obvious by Ericsson-BMR in view of Wanes. *See* §VIII.A.2.

3. Claim 3

133. In my opinion, Claim 3 is rendered obvious by Ericsson-BMR in view of Wanes. *See* §VIII.A.3.

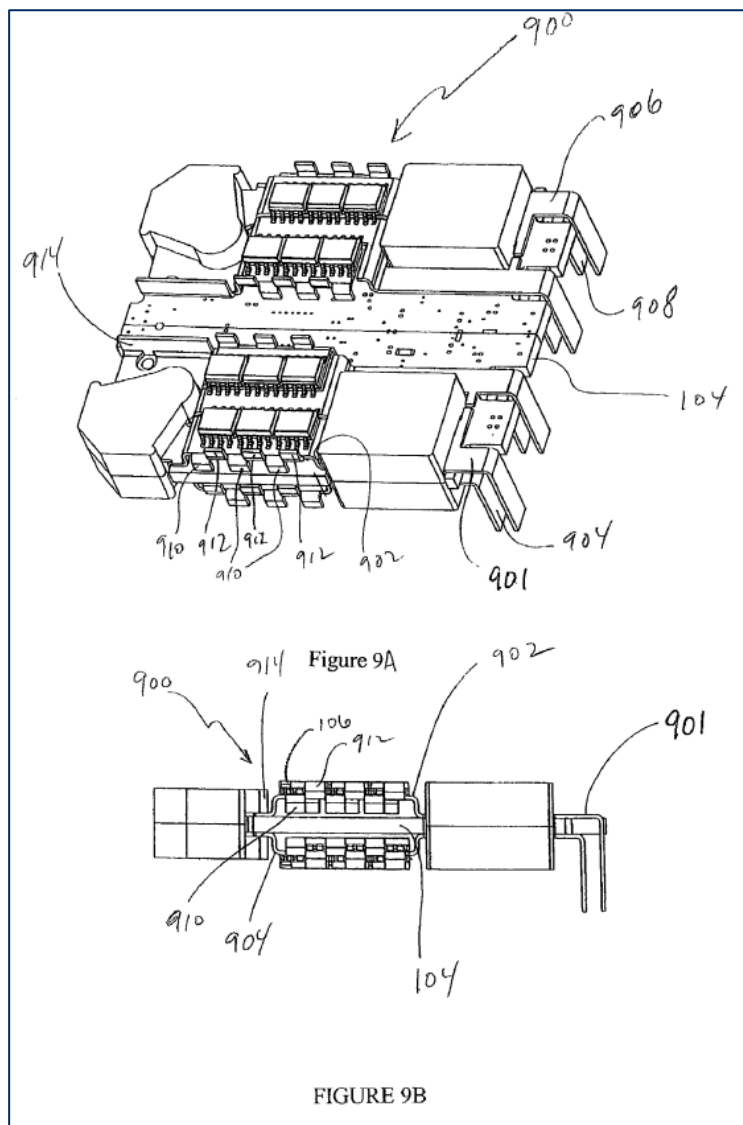
4. Claim 4

134. In my opinion, Claim 4 is rendered obvious by Ericsson-BMR in view of Wanes.

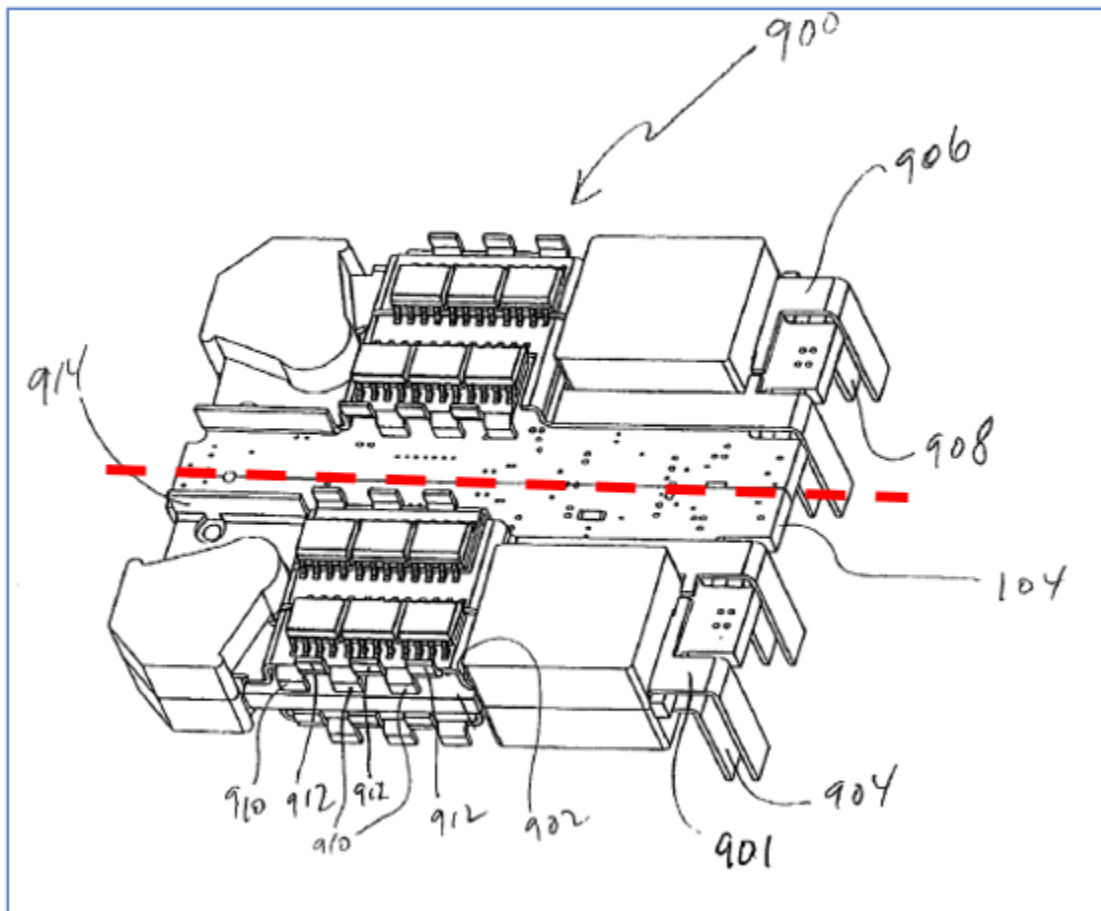
135. As discussed above, Ericsson-BMR in view of Wanes renders obvious Claim 2. As discussed further below, in my opinion, Ericsson-BMR in view of Wanes teaches and renders obvious the limitation “wherein the power converter further comprises circuitry including a pair of cells having a common circuit topology and each including power semiconductor switches from each of the first and second sets; each cell having its respective components arranged in a pattern, wherein the pattern of components of one cell is substantially a mirror image of the pattern of components in the other cell.”

136. As background, Wanes teaches replicating a specific circuit topology. One embodiment in Wanes, for example, replicates a topology four times. *See* Ex.

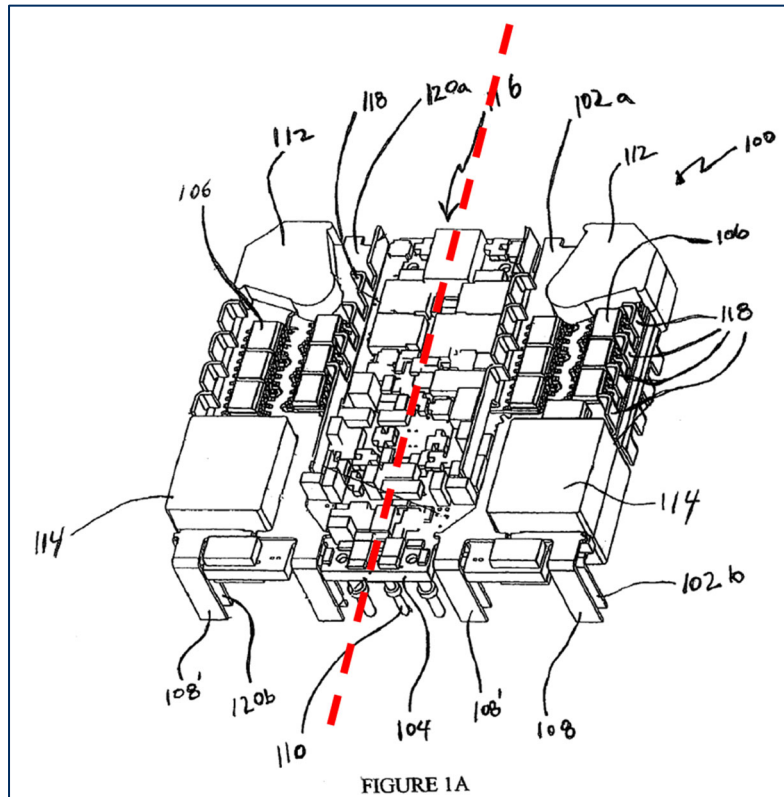
1009 at 11:10-11 (“substrates 901, 904, 906, and 908 have similar configurations”). Two of the four instances of the common circuit topology directly overlap each other on top and bottom, as pictured below in Wanes’s Figure 9B by reference to 901 and 904, and the other two of the four instances of the common circuit topology mirror that setup, as pictured below in Wanes’s Figure 9A where elements 906/908 mirror 901/904:



See Ex. 1009, Figs. 9A-B. For example, Elements 901 and 904 are together a claimed “cell,” and elements 906 and 908 are together an identical claimed “cell,” including because they are discrete, repeatable units comprised of electrical components that perform a certain function. As shown here in this annotated Figure 9A, each of the cells in this pair of cells has its components arranged in a pattern, and the pattern of components in the 901/904 cell is a mirror image of the pattern of components in the 906/908 cell:



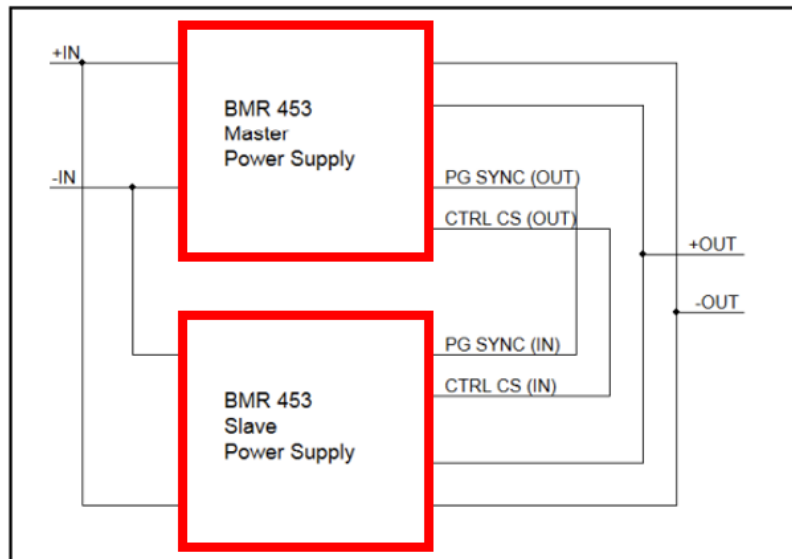
The same mirror cell symmetry is shown, for example, in this annotated version of Figure 1A, where 120a and 120b are together one cell and 102a and 102b are together another cell:



See Ex. 1009, Fig. 1A (annotated), 3:66-67 (“Substrate 120 has a *mirror image* configuration of substrate 102.”); see also, e.g., Ex. 1009 at 10:47-58.

137. The Ericsson-BMR module is provided in “Industry standard Quarter-brick” format. See Ex. 1007 at 1. The “quarter-brick” designation is one size of power converter in a family of commonly referenced “brick” power supply formats that would have been familiar to POSITA. See, e.g., Ex. 1029 at 1 (“quarter brick”). In applications where a “quarter brick” power supply is insufficient to

provide necessary power to a system, one option was to use multiple bricks to increase power delivery capability. Ericsson-BMR teaches that two Ericsson-BMR quarter brick cells can be connected and operated in parallel:



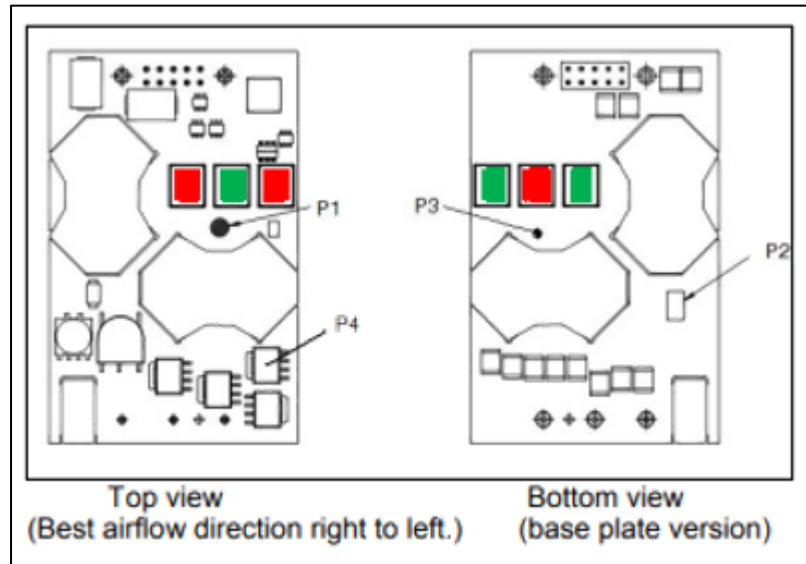
See EX1007 at 22 (annotated); *id.* (“Two BMR 453 xx00/xxx products can be directly connected....”). Arranging two Ericsson-BMR cells in this manner would essentially double the power available at the “OUT” terminals of the combined power supply in comparison to a single quarter-brick BMR 453 module. See EX1012 at 84 (“The 1.8-MHz, 48-V, 130-W VRM is implemented as **two 65-W VRM modules** connected in parallel.”).

138. As a POSITA would have been aware, another option to increase power would be to use the next standard size up after a “quarter brick,” which is known as a “half brick.” Given Waner’s teachings where the FETs are mirrored, one obvious approach to creating a “half brick” version of the Ericsson-BMR

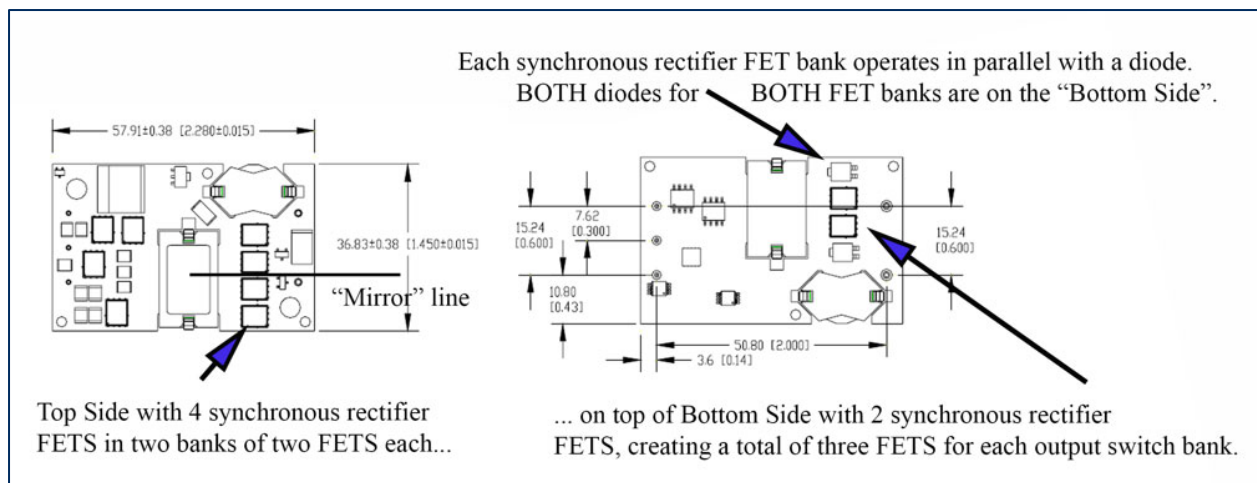
module would be to mirror the inverter and output FET power semiconductor devices of the Ericsson-BMR module on a single, larger board of half-brick size. These components would have been mirrored similar to the mirroring of Wanes's substrates 120a and 102b in Figure 1A. *See* Ex. 1009 at Fig. 1A; *see also, e.g.*, Ex. 1009 at Fig. 9A (substrates 901 mirrored with 908). In this combination of Ericsson-BMR and Wanes, the original inverter and output FET power semiconductor devices of the quarter-brick Ericsson-BMR converter would be a cell, and they would be mirrored on an extended PCB in accordance with Wanes's teachings. A POSITA would have had a reasonable expectation of successfully being able to mirror the Ericsson-BMR cell in this manner, as mirroring techniques were taught by Wanes. Moreover, Ericsson-BMR expressly teaches how to connect two Ericsson-BMR modules. *See* EX1007 at 22. A POSITA would have been motivated to create this half-brick for a number of reasons. For example, this approach would allow a designer to "integrate redundant power-supply hardware." *See* EX1018 at 2. Additionally, it would also allow a customer to service higher power applications. Additionally, Wanes's entire power converter (element 100 in Figure 1A) operates as a unified power converter, thus teaching a POSITA the benefits of using mirrored cells for higher power outputs. *See* Ex. 1009 at 4:22-44.

139. Additionally and independently, in view of Wanes's mirroring teachings, Ericsson-BMR's output FETs could have been arranged in a mirroring

fashion as follows, where the red-highlighted FETs correspond to one output switch while the green-highlighted FETs correspond to the other output switch depicted in Ericsson-BMR's fundamental circuit diagram (Ex. 1007 at 5):



See Ex. 1007 at 24 (annotated). This arrangement also satisfies the claim element with respect to mirrored cells for the reason discussed above. See §VIII.A.4. A POSITA would have known about such mirroring techniques in the prior art. See, e.g., Ex. 1029 at 3 (annotated)

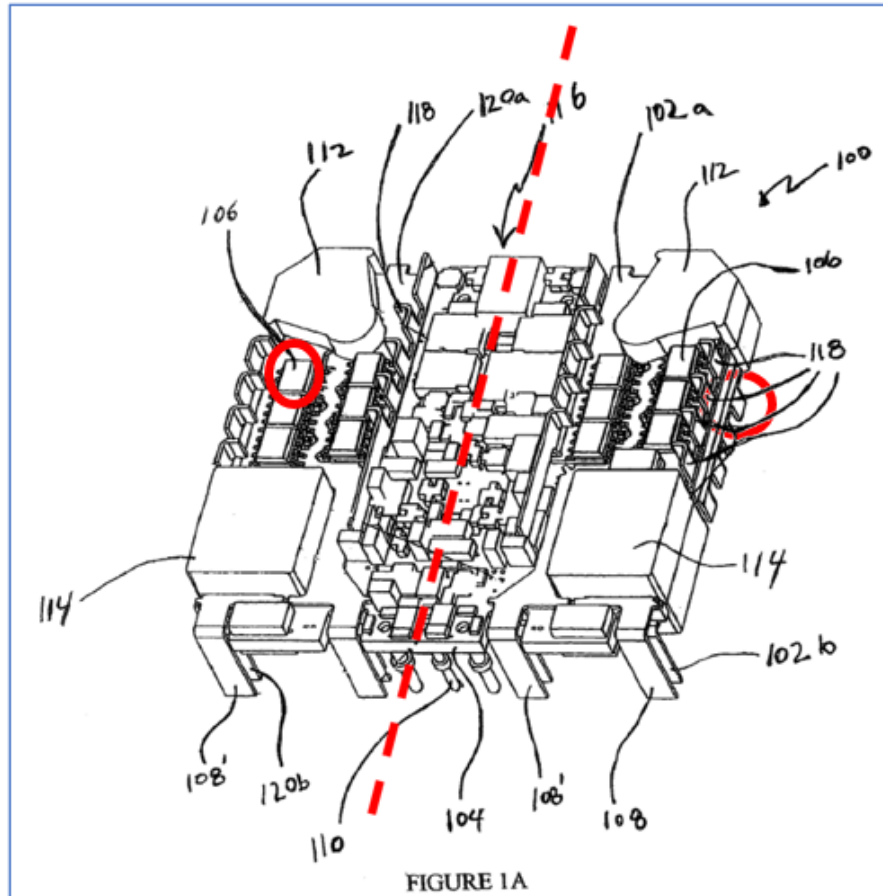


5. Claim 5

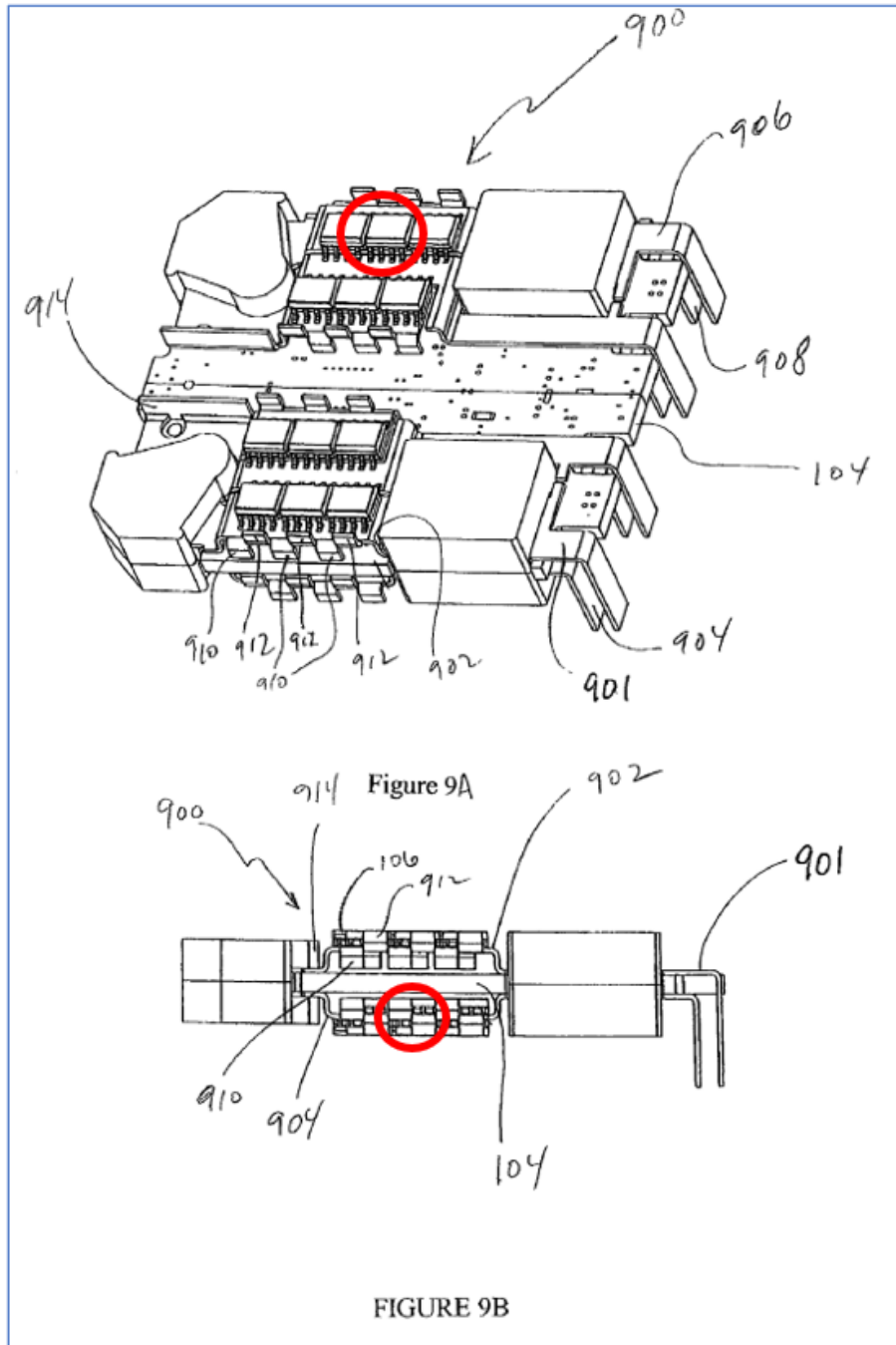
140. In my opinion, Claim 5 is rendered obvious by Ericsson-BMR in view of Wanes.

141. As discussed above, Ericsson-BMR in view of Wanes renders obvious Claim 4. As discussed further below, in my opinion, Ericsson-BMR in view of Wanes teaches and renders obvious wherein a component from one of the cells is located on an opposite surface of a respective component from the other one of the cells.

142. The first asserted embodiment of mirrored cells discussed above in which the original inverter and output FET power semiconductor devices of the Ericsson-BMR converter are a cell and mirrored in accordance with Wanes's satisfy this element. In this embodiment, they would be mirrored like (for example) substrates 120a and 102b in Wanes's Figure 1A (and like substrates 901 and 908 in Wanes's Figure 9A), such that a component from one of the cells would be located on an opposite surface of a respective component from the other one of the cells. To visualize, as shown below as an example, a FET component (element 106) in Wanes's substrate 120a is located on an opposite surface as a FET component in mirrored substrate 102b:



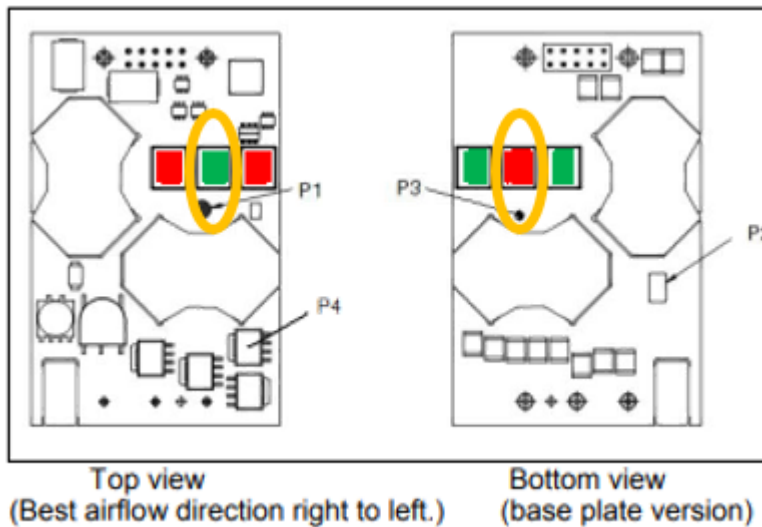
See Ex. 1007 at Fig. 1A (annotated), 4:3-6 (“Each substrate 102 carries electrical components, which, in the particular example as shown, are field effect transistors 106 (‘FETs’). Substrate 102 is configured to carry FETs 106....”). This can also be visualized in Wanes’s Figure 9A-B:



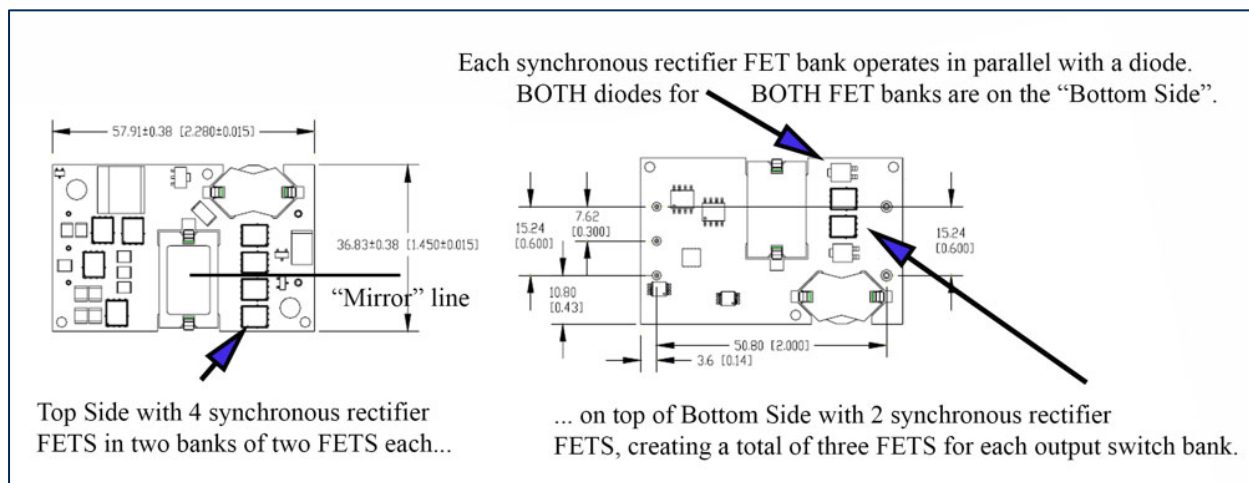
See Ex. 1007 at Figs. 9A-B (annotated); *see also id.* at 3:66-67.

143. In the second asserted embodiment of mirrored cells asserted in this Ground, it can be seen that, for example, the green-highlighted middle MOSFET component of one of the cells is on the top surface of the PCB (circled in orange on

the left), which is on an opposite surface of the respective red-highlighted middle MOSFET component of the other cell:



See Ex. 1007 at 24 (annotated); §VIII.A.5. Again, a POSITA would have known about such mirroring techniques in the prior art. See, e.g., Ex. 1029 at 3 (annotated):

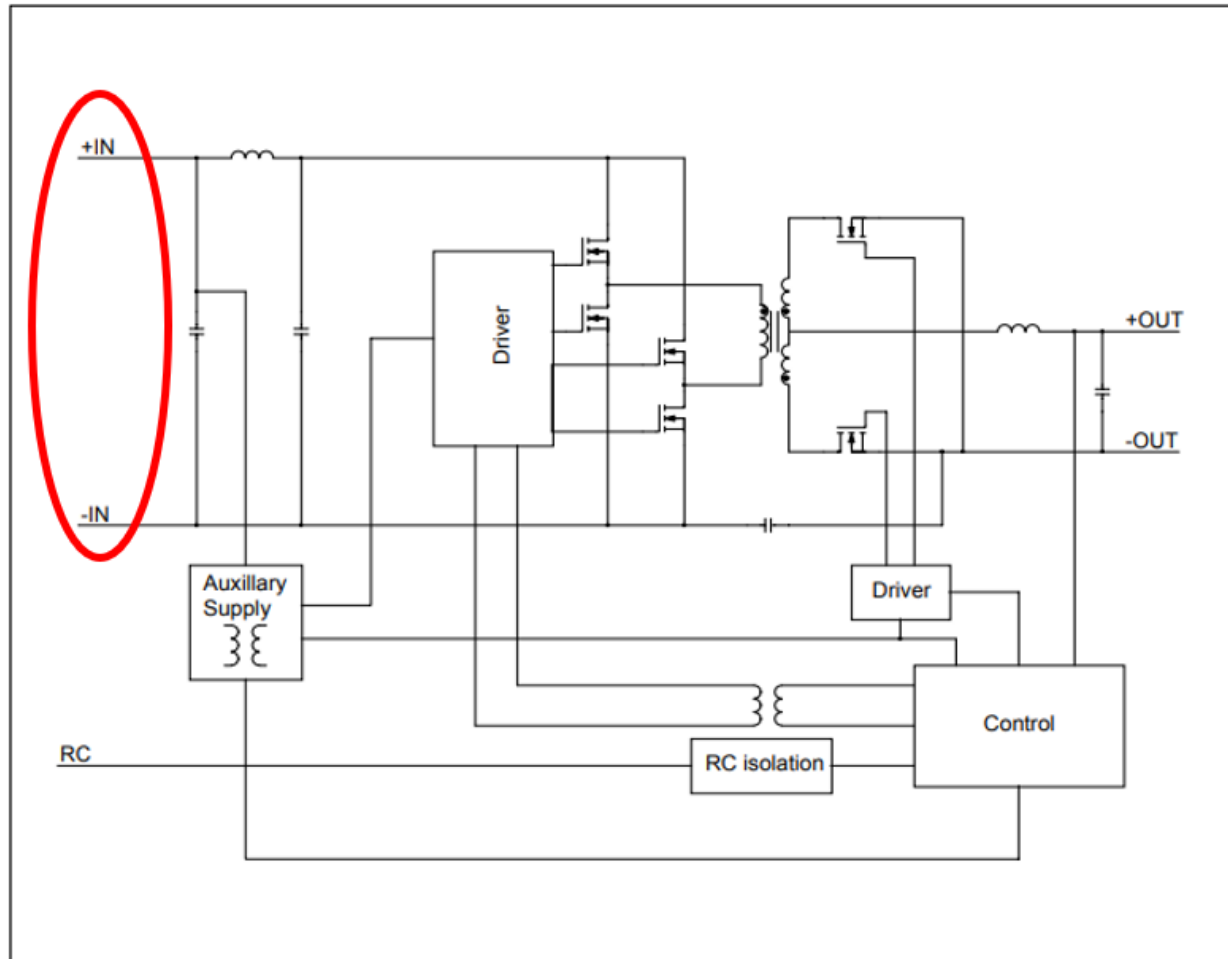


6. Claim 6

144. In my opinion, Claim 6 is rendered obvious by Ericsson-BMR in view of Wanes.

145. As discussed above, Ericsson-BMR in view of Wanes renders obvious Claim 5. As discussed further below, in my opinion, Ericsson-BMR in view of Wanes teaches and renders obvious wherein the cells comprise input cells.

146. In the embodiment in which Ericsson-BMR's inverter and output FET power semiconductor devices are mirrored as taught by Wanes, the mirrored power semiconductor devices are a cell and they comprise an an input cell because the inverters are used on the input side of the circuit:



See Ex. 1007 at 5 (annotated); Ex. 1007 at 25 (“Connections” table).

7. Claim 7

147. In my opinion, Claim 7 is rendered obvious by Ericsson-BMR in view of Wanes. See §VIII.A.6.

8. BMR-2008

148. The relevant teachings of BMR-2008 are substantially the same as the relevant teachings of Ericsson-BMR. Compare EX1007 at, e.g., 1, 2, 5, 24, 31 with EX1026 at, e.g., 1, 4, 13, 15, 20.

149. As a result, in my opinion, Claims 1-7 are rendered obvious by BMR-2008 in view of Wanes for the same reasons as they are rendered obvious by Ericsson-BMR in view of Wanes set forth in this Ground.

D. Ground IV: Claims 1-7 Are Rendered Obvious By Takeshima

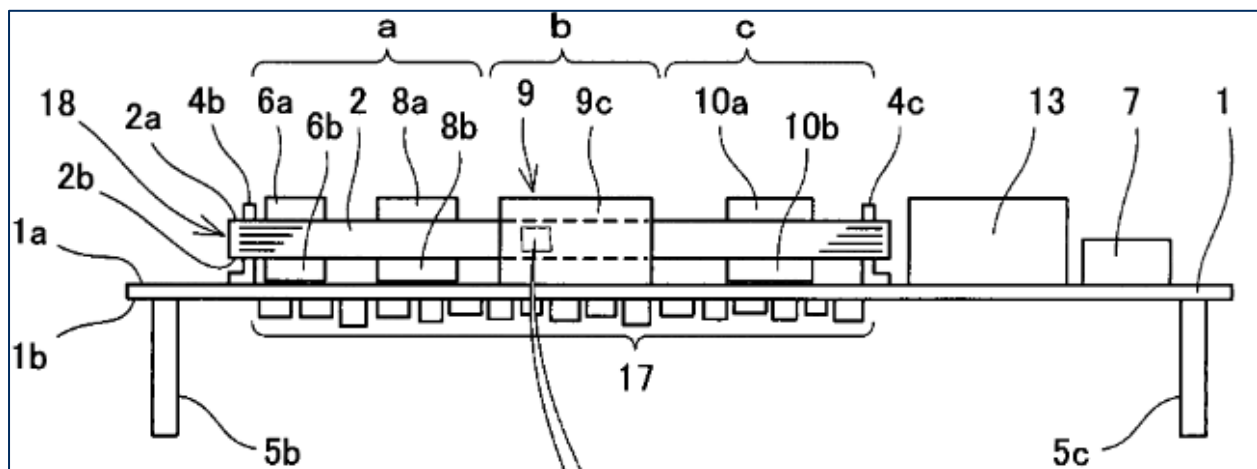
1. Claim 1

150. In my opinion, Takeshima renders obvious Claim 1.

a. 1[preamble]

151. In my opinion, Takeshima teaches the preamble.

152. An example of an apparatus taught by Takeshima can be seen (among other places) in Takeshima's Figure 2, a portion of which is shown here:



b. 1[a]

153. In my opinion, Takeshima teaches this element.

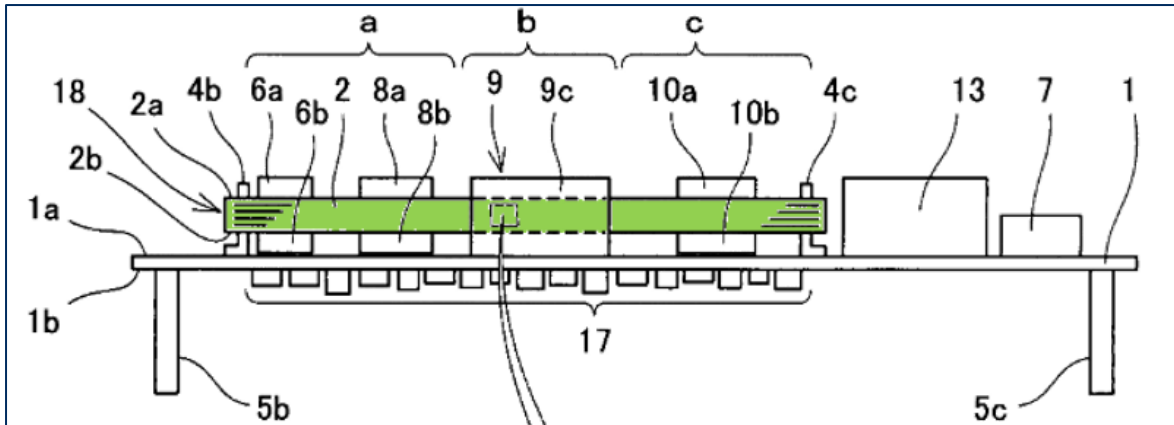
154. For example, the circuit in Takeshima's Figure 7 is "a circuit diagram of a switching power supply device a ... that adopts a half-bridge type *converter* circuit." See Ex. 1010 at 7:47-50. Half-bridge type converters were well-known

power converter circuits. *See* Ex. 1008 at 152-54. Takeshima also explicitly discusses its objective of providing “a high efficiency and small-sized switching power supply device that is capable of supplying a direct current at low voltage and high current and at a constant voltage irrespective of the power consumption of load.” *See* Ex. 1010 at 3:5-12. And Takeshima discusses that such switching power supply device(s) are power converter circuits. *See* Ex. 1010 at 1:11-21 (“[S]witching power supply device is one type of stabilized (regulated) direct current power supply, and is configured so as to ***output a direct current at a constant voltage by converting a direct current obtained from a power supply,*** such as a commercial power source or a storage battery, into a pulse voltage having a frequency higher than the audio frequency (about several hundred kilohertz) by a high-speed switching function of semiconductor devices such as transistors, and controlling the pulse width and the pulse interval of the pulse voltage.”).

c. 1[b]

155. In my opinion, Takeshima teaches this element.

156. Takeshima teaches a PCB. *See* Ex. 1010 at, *e.g.*, 4:33 (“printed circuit board”), 6:38 (same). Takeshima’s PCB can be seen, for example, as element 2 in Figure 2, highlighted here in green:



See Ex. 1010 at Fig. 2 (annotated), 9:38-40.

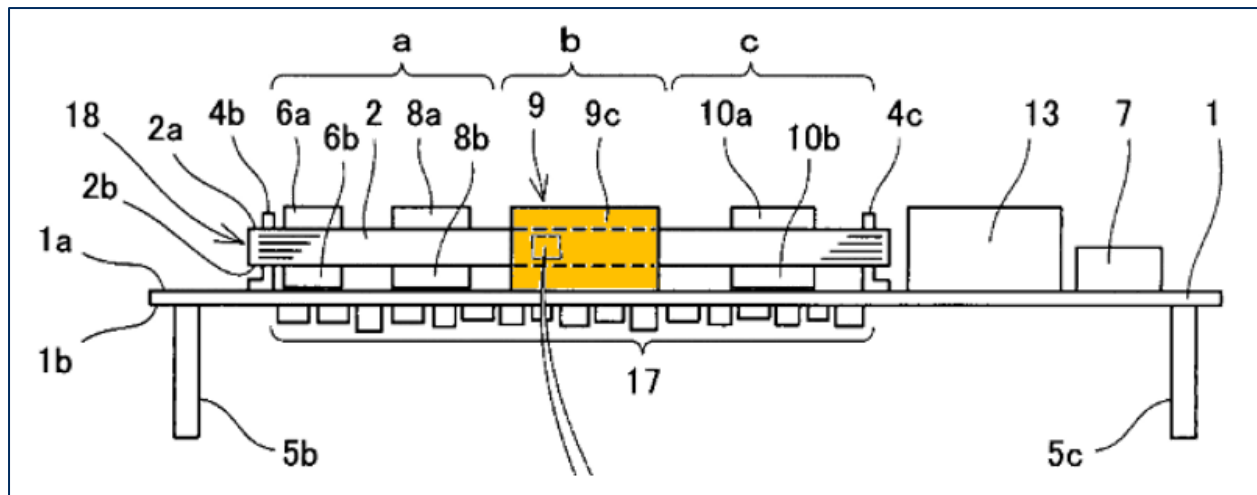
157. Takeshima's PCB is comprised of a plurality of layers. See Ex. 1010 at, e.g., 9:40 ("**multi-layer** printed circuit board 2"). Takeshima teaches that this plurality of layers is conductive. See Ex. 1010 at, e.g., 9:47-50 ("The wiring, which is a constituting element of the multi-layer printed circuit board 2 but not shown in the figure, is composed of a plurality of wiring lines for electrically connecting a plurality of semiconductor elements or the like arranged on a multi-layer printed circuit board 2....").

158. As shown above in Figure 2, the PCB has a top surface 2a and a bottom surface 2b. See also Ex. 1010 at 10:51-67 ("first major surface 2a and a second major surface 2b of the multi-layer printed circuit board").

d. 1[c]

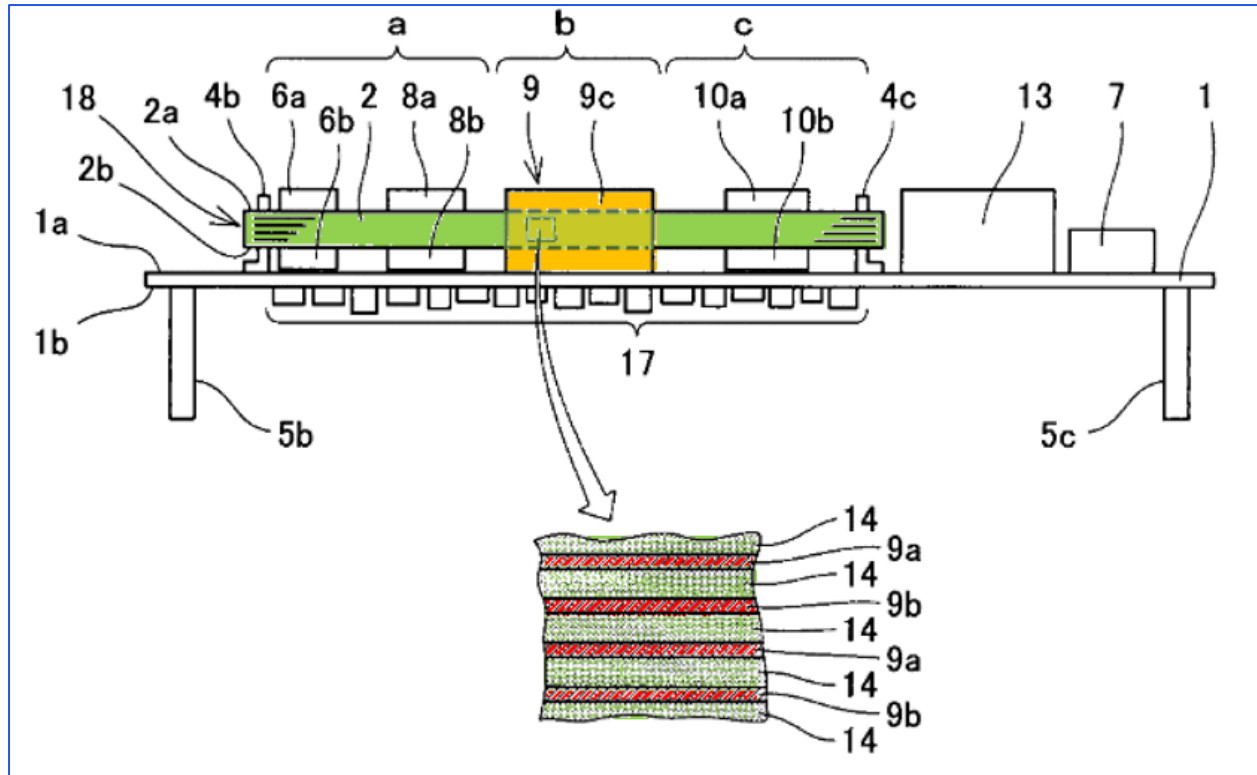
159. In my opinion, Takeshima teaches this element.

160. Takeshima teaches a magnetic core, which is shown as element 9 in Figure 2 highlighted below in orange, that is magnetically coupled to windings:



See Ex. 1010 at 9:3-5 (“The transformer secondary winding 9b of the transformer 9 is *magnetically* connected to the transformer primary winding 9a by the *transformer core* 9c).

161. Takeshima teaches that the windings are formed by traces in the conductive layers of the PCB, as shown by the zoomed-in section in Figure 2, where the winding traces are highlighted in red.

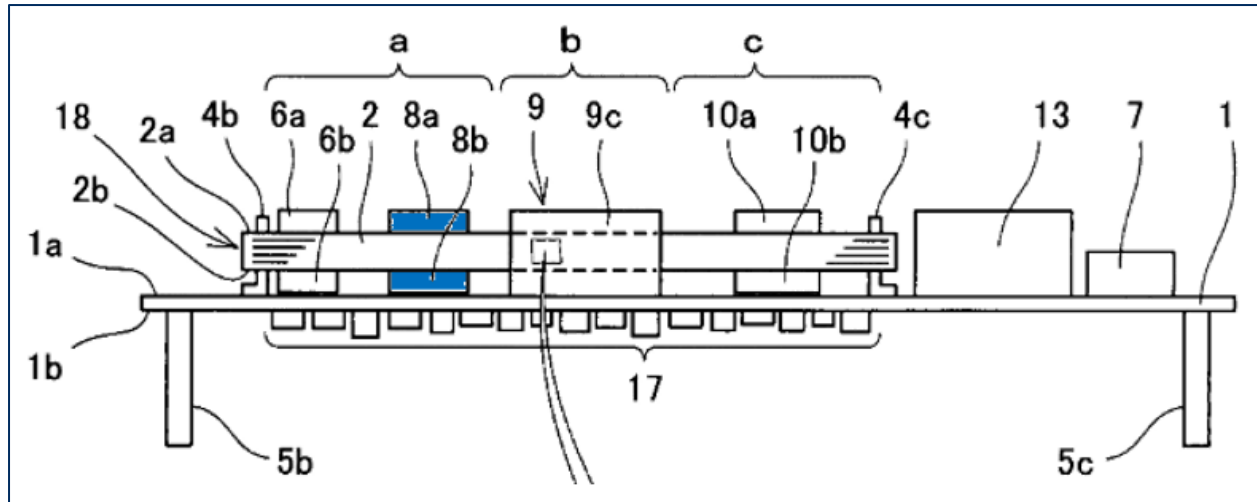


See Ex. 1010 at 9:62-10:3 (“transformer primary winding **9a** and the transformer secondary winding **9b** are formed within the transformer winding region **b** of the multi-layer printed circuit board **2** in the following manner: spiral-shaped wiring lines formed in respective layers of the multi-layer printed circuit board **2** are stacked [on] each other with electrically insulative members **14** interposed therebetween.”)

e. 1[d]

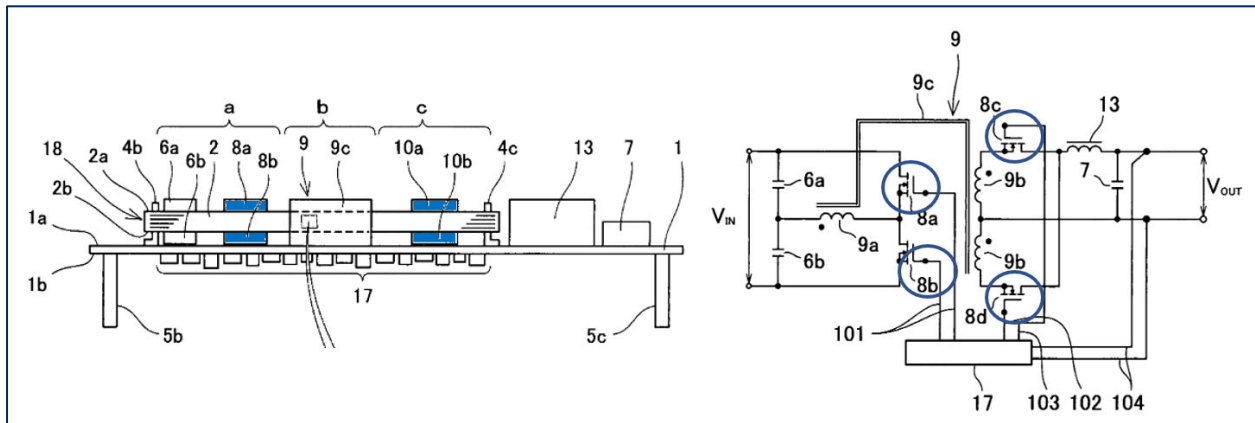
162. In my opinion, Takeshima renders this element obvious.

163. As background, Takeshima teaches that “MOS field-effect transistors (hereafter abbreviated as ‘MOSFETs’) **8a** and **8b**” are placed on the top and bottom of the PCB, as shown here in this annotated Figure 2:



See Ex. 1010 at Fig. 2 (annotated), 8:46-47, 10:51-55. Takeshima teaches that this layout could “advantage[ously]” employ a “half-bridge” converter circuit such as that shown in Figure 7, and further that “other converter circuits may be used.” See Ex. 1010 at 7:47-50, 14:44-59. Accordingly, it would have been obvious to a POSITA to employ the half-bridge converter taught in Takeshima’s Figure 14, which is identical in layout to the half-bridge converter in Figure 7 except that Figure 7’s diodes 10a/10b are replaced with MOSFET switches (numbered 8c/8d in Figure 14). A POSITA would have recognized that diodes are a type of switch, and therefore using the output FET switches in Takeshima’s Figure 14 converter would have been a natural fit and well within the ordinary skill in the art. Control mechanism 17 additionally is used to control those MOSFET switches. This would have been obvious because Takeshima’s Figure 14 circuit retains all of the benefits that Takeshima teaches are associated with half-bridge converters that are otherwise identical in Takeshima’s Figure 7, while providing additional control by

using MOSFET switches (which are also power semiconductor devices) instead of diodes. MOSFET switches 8a, 8b, 8c, and 8d in Figure 14 shown below on the right (circled in blue) would correspond to the placement in 8a, 8b, 10a, and 10b, respectively, in Takeshima's Figure 2 shown below on the left (highlighted in blue):



See Ex. 1010 at Figs. 2, 14 (annotated, cropped).

164. These four MOSFET devices are a plurality of power semiconductor devices, for the same reasons that Ericsson-BMR's and Wanes's MOSFETs/FETs are power semiconductor devices. See Grounds I, III. As shown above on the left side, a first set of Takeshima's MOSFETs (8a and 8c) are mounted on the top surface of the PCB 2, and a second set of Takeshima's MOSFETs (8b and 8d) are mounted on the bottom surface of the PCB. As shown above on the right side, they are all electrically connected in the manner that would dissipate power during operation of the converter, at a level Pt on the top by convention and at a level Pb on the bottom by convention. See Ex. 1008 at 2-3.

f. 1[e]

165. In my opinion, Takeshima teaches, or at least renders obvious, this element.

166. A POSITA would have known that the obvious way to operate Takeshima's half-bridge converter would be with symmetrical power cycles using 8A and 8B to avoid saturating the transformer. As with Ericsson-BMR's full-bridge converter discussed above, a POSITA would have known that the "Utilization of the transformer core and windings is essentially the same as in the full-bridge" as in a half-bridge such as that taught by Takeshima (*see* Ex. 1008 at 154), and that the "net volt-seconds...should equal zero" in the windings (Ex. 1008 at 152 and Figs. 6.18, 6.20, and 6.21); *see also* Ex. 1010 at, *e.g.*, 11:44-51.

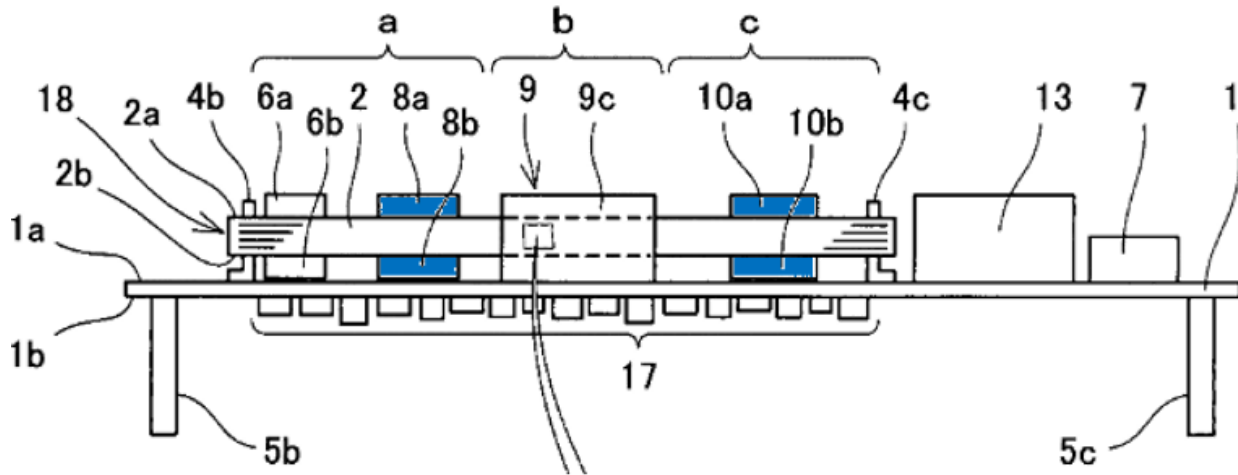
167. Because top-side MOSFETs 8a and 8c (*i.e.*, power semiconductors from the first set) would be subjected to equal or at least approximately equal voltage, current, and power cycles over time as identical bottom-side MOSFETs 8c and 8d (*i.e.*, power semiconductor devices from the second set), a POSITA would have expected them to dissipate power at levels P_t and P_b that were equal or at least approximately equal, as discussed in the context of Ground I, for a particular environment and configuration within Takeshima. *See, e.g.*, Ex. 1015 at 9:19-23.

2. Claim 2

168. In my opinion, Takeshima renders obvious Claim 2.

169. As discussed above, Takeshima renders obvious Claim 1. And as discussed further below, Takeshima teaches and renders obvious wherein a plurality of the power semiconductor devices in the first set are each positioned in a location on the top surface substantially overlapping a location on the bottom surface occupied by a power semiconductor device in the second set.

170. As shown in this annotated version of Figure 2, a plurality of power semiconductor devices in the first set (MOSFETs 8a and 8c) are each positioned on the top surface of the PCB in a position directly overlapping in one dimension the location of the plurality of power semiconductor devices in the second set (MOSFETs 8b and 8d²) that are positioned on the bottom side of the PCB:



² As discussed in Claim 1, in the asserted embodiment of Takeshima, diodes 10a and 10b in Takeshima's Figure 2 have been replaced with MOSFET switches 8c and 8d in Takeshima's Figure 14.

See Ex. 1010 at Fig. 2 (annotated). Takeshima further teaches that “MOSFETs 8a and 8b ... are arranged in the vicinity of a connecting terminal,” and further teaches that “diodes **10a** and **10b** are arranged in the vicinity of a connecting terminal, not particularly shown in the figure.” *See* Ex. 1010 at 10:51-66. A POSITA would therefore have understood, or at least have found obvious, that the MOSFETs 8a and 8b, and also 8c and 8d (which, again, replace 10a and 10b in the figure above) would also have directly overlapped in the second dimension, including because each pair is taught to be “in the vicinity” of the same connecting object, and further because it would make design and manufacturing simpler if the same optimized layout were used on both sides of the PCB, rather than having to optimize multiple different layouts for top and bottom sides of the PCB. It was also a known technique at that time to overlap and align related components in this manner. *See also, e.g.*, Ex. 1007 at 24; Ex. 1009 at Fig. 9A-B; Ex. 1029 at 3.

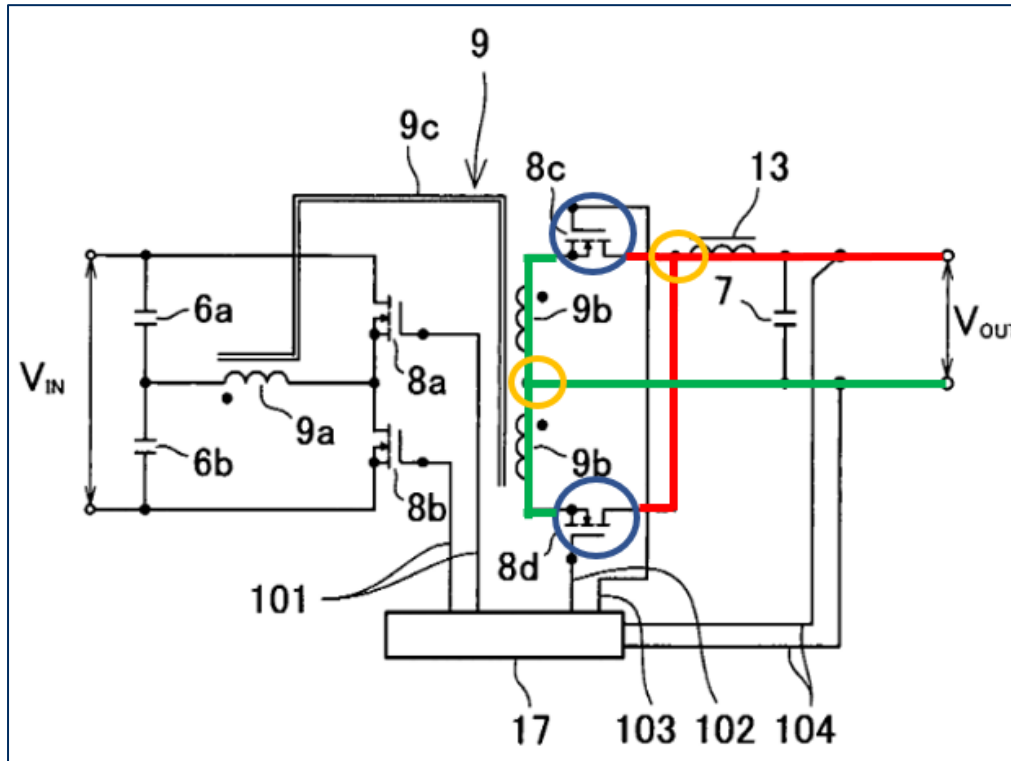
3. Claim 3

171. In my opinion, Takeshima renders obvious Claim 3.

172. As discussed above, Takeshima renders obvious Claim 1. And as discussed further below, Takeshima teaches and renders obvious wherein the power semiconductor devices are electrically connected using a respective set of conductive vias in the PCB, and a plurality of the power semiconductor devices in

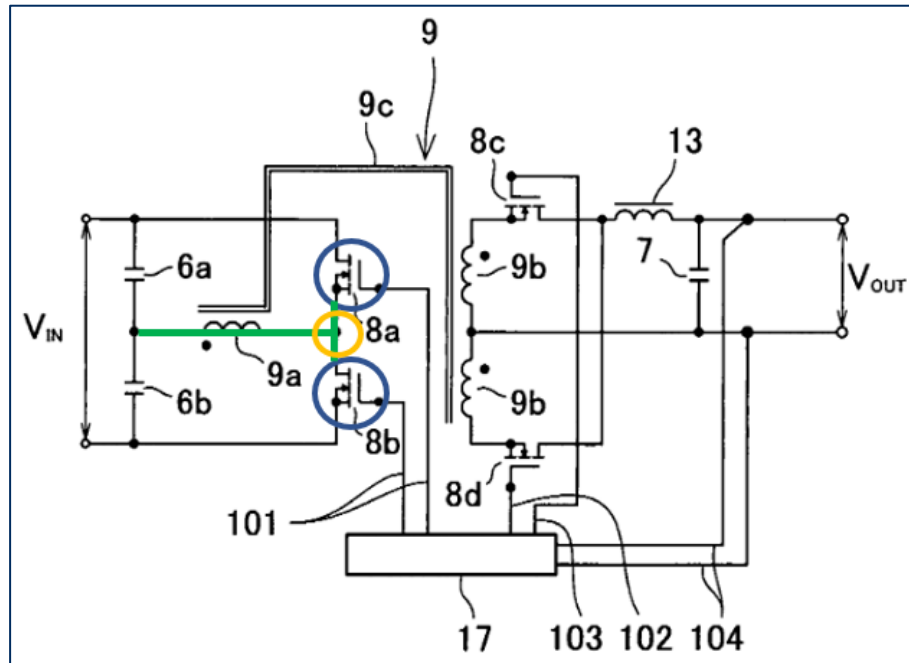
the first set share their respective sets of conductive vias with corresponding power semiconductor devices in the second set.

173. Similar to Ericsson-BMR's (and to Exhibit 1029's) full-bridge circuit (see Ground I, Claim 3), Takeshima's half-bridge circuit shows that MOSFETs 8c on the top of the PCB and 8d on the bottom of the PCB (both circled in blue) would share respective vias because they connect (circled in orange) to the same output lines (highlighted in red and green), as shown here in annotated Figure 14:



See Ex. 1010 at Fig. 14 (annotated), 19:29-30 (“The drain terminals of the MOSFETs 8c and 8d are connected to each other and further connected to one terminal (input side) of the inductance 13.”). Similarly, MOSFETs 8a and 8b (circled in blue) on the top and bottom of the PCB, respectively, also share

(connection circled in orange) their respective via to primary winding 9a (path highlighted in green):



See Ex. 1010 at Fig. 14 (annotated). Therefore, a plurality of semiconductor devices on the top side of the PCB (8a and 8c) share their respective vias with corresponding semiconductor devices on the bottom side of the PCB (8b and 8d, respectively), as vias are used to connect devices at different layers of a PCB.

4. Claim 4

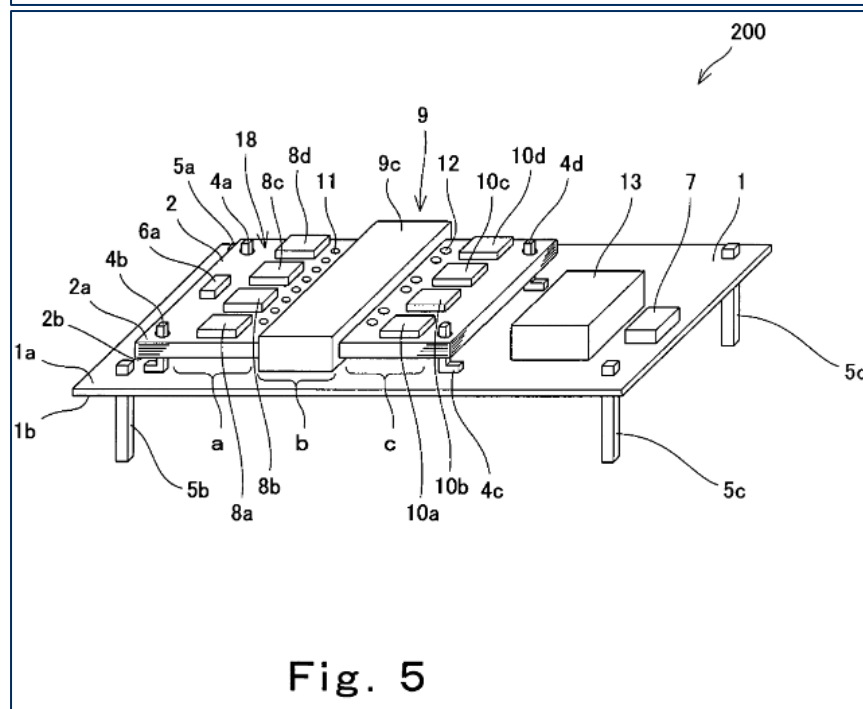
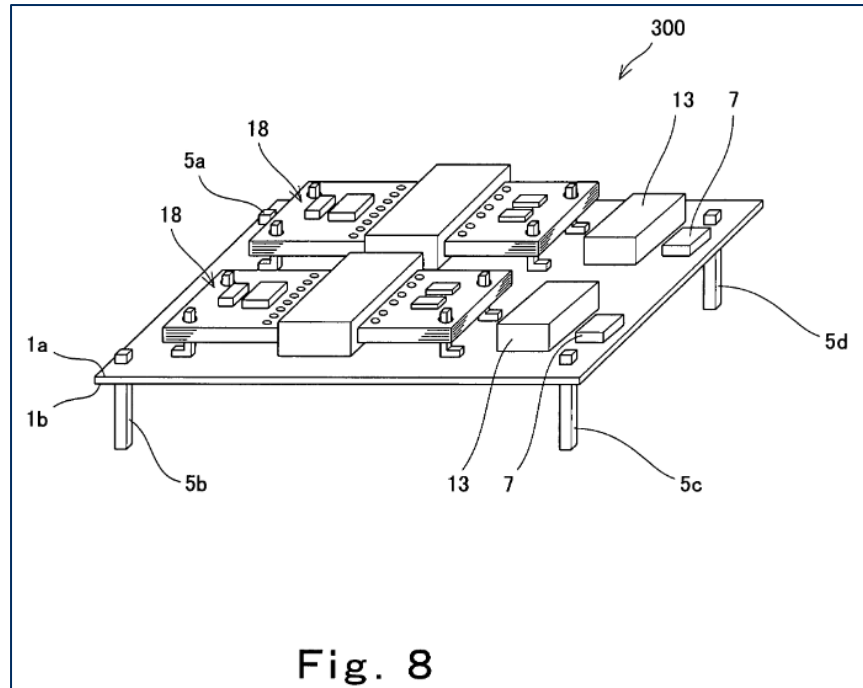
174. In my opinion, Takeshima renders obvious Claim 4.

175. As discussed above, Takeshima renders obvious Claim 2. And as discussed further below, Takeshima renders obvious wherein the power converter further comprises circuitry including a pair of cells having a common circuit topology and each including power semiconductor switches from each of the first

and second sets; each cell having its respective components arranged in a pattern, wherein the pattern of components of one cell is substantially a mirror image of the pattern of components in the other cell.

176. As background, Takeshima teaches as follows:

[I]t is possible to employ a configuration of a switching power supply device 300 as illustrated in FIG. 8, in which *two sets of power modules 18* and smoothing circuits are provided on a single main printed circuit board 1. Alternatively, although not particularly shown in the drawings, it is possible to employ a configuration in which *two sets of power modules 18 are integrated into a single component* and arranged, as a set of power module, on a main printed circuit board 1. In other words, the advantageous effects of the present invention can be obtained equally in *various embodiments*, irrespective of the number of power modules 18 mounted on the main printed circuit board 1 or the number of circuits formed thereon.



Ex. 1010 at 14:60-15:8, Figs. 5 and 8. Takeshima thus teaches that the power converter discussed above in the context of Claims 1 and 2 (in the Figure 2 layout with Figure 14 half-bridge circuitry) would obviously have been mirrored with a

second such power converter (as in Figure 8 above) and further that it would obviously have been integrated onto the same PCB 102 as shown in Figure 5 above. *See id.*; *see also* Ex. 1010 at 11:44-51 (“[T]he advantageous effects of the present invention become more apparent by adopting a configuration in which a further plurality of switching elements and rectifier elements are connected in parallel in order to output a direct current at a higher current.”); *see also* §VIII.C.4 (discussing additional reasons that a POSITA would have been motivated to mirror); Ex. 1023 ¶¶51-52 (semiconductor devices “disposed at symmetrical positions” and “wiring patterns and such in the respective semiconductor devices” that “are substantially the same” are “desirable”).

177. Takeshima’s Figure 2 power converters is a repeatable cell unit that has switches from both the top and bottom sets of power semiconductor devices arranged in the pattern depicted in Figure 2. When that cell unit duplicated (as in, for example, Figure 8), the duplicated cell would share the same circuit topology and also include switches from each of the top and bottom sets of power semiconductor devices on the PCB. That duplicated cell would be laid out in mirrored fashion (as in, for example, Figure 5), so the pattern of components in the second, duplicated cell would be a mirror image of the pattern of components in the first cell.

178. Many of Takeshima's teachings contemplate such mirroring and evidence a POSITA's reasonable expectation of success in mirroring. *See e.g.*, EX1010 at 7:47-50, 11:44-51 14:44-48, 14:56-59, Figs. 1-2, 7, 14 (additional teachings motivating a mirrored layout with an arranged pattern in accordance with this element).

5. Claim 5

179. In my opinion, Takeshima renders obvious Claim 5.

180. As discussed above, Takeshima renders obvious Claim 4. And as discussed further below, Takeshima teaches and renders obvious wherein a component from one of the cells is located on an opposite surface of a respective component from the other one of the cells.

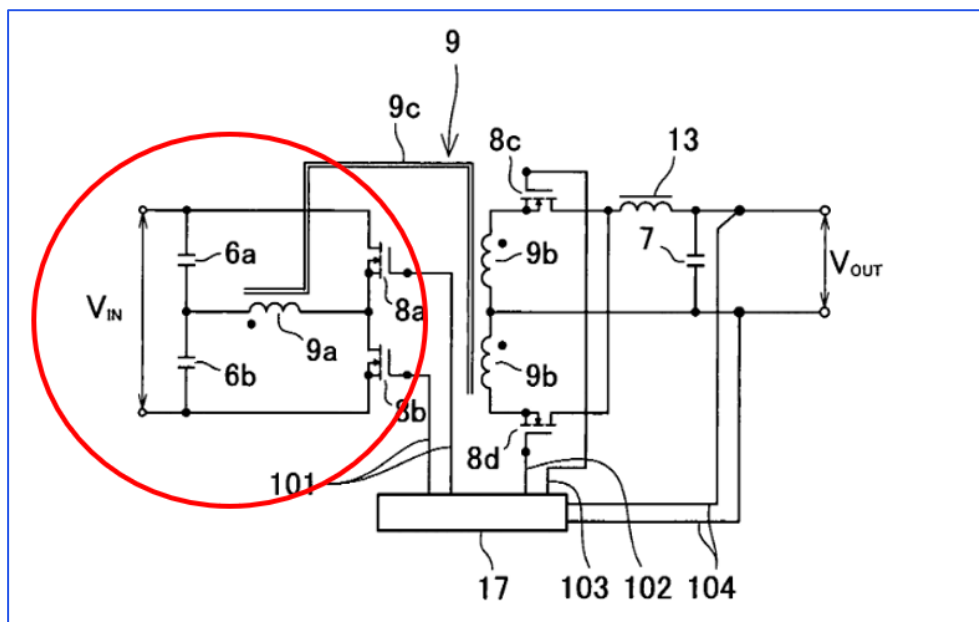
181. In the asserted embodiment of Takeshima (Figure 2's cell with Figure 14's half-bridge circuit, mirrored as taught by Takeshima at 14:60-15:8 and Figures 5 and 8), the two cells are the same and they both have MOSFETs on the top and bottom surfaces of the PCB. *See also* Ex. 1010 at 14:60-15:8, Figs. 5 and 8. Because they are the duplicate cells, a component on the top side of the first cell would be located on the opposite surface to a respective component on the bottom side of the second, duplicated cell. *See also* §VIII.C.5.

6. Claim 6

182. In my opinion, Takeshima renders obvious Claim 6.

183. As discussed above, Takeshima renders obvious Claim 5. As discussed further below, Takeshima teaches and renders obvious wherein the cells comprise input cells.

184. Takeshima refers to “primary-side inverter region a” in Figure 1, which is on the input side of the converter circled here in red from Takeshima’s annotated Figure 14 (the applicable circuit in this Ground):



This portion of the overall cell is an input cell as shown by “ V_{IN} ” above. The cell is a repeatable unit that processes the input voltage and current that is input into the power converter (again, as shown above by “ V_{IN} ”). A POSITA would have understood this cell to be on the “primary” winding side, *i.e.*, the input to the converter. In the asserted Ground, the overall power converter that is mirrored (as

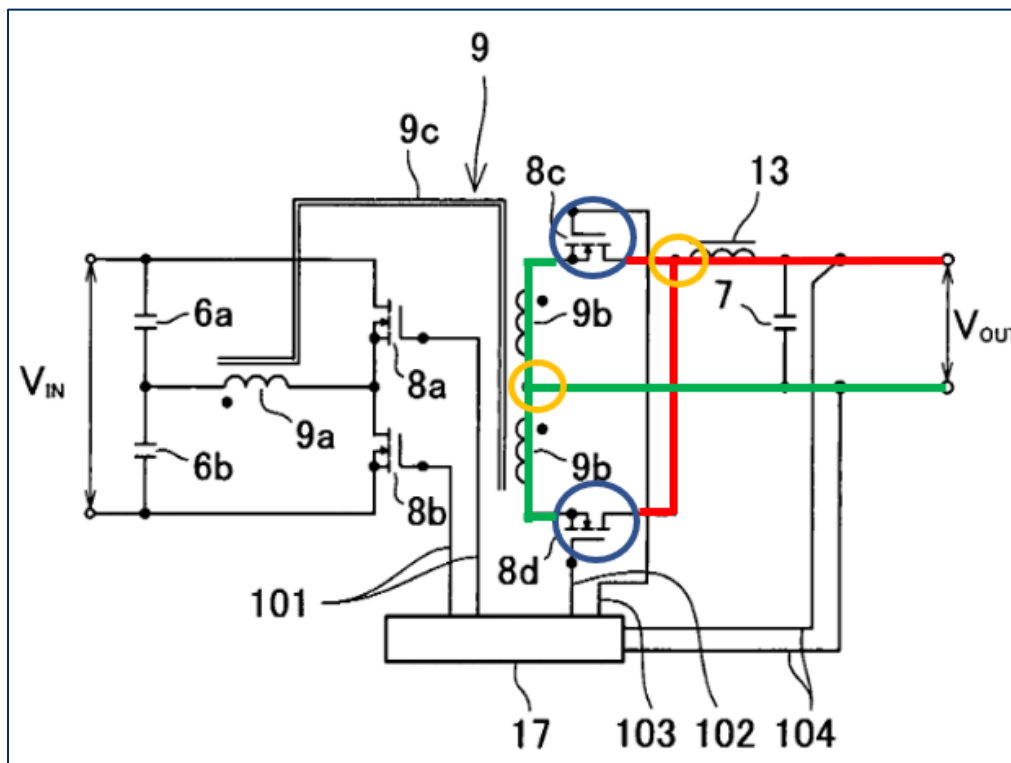
taught in Takeshima at 14:60-15:8) includes the repeated cell or “input cell” of the components responsible for energizing the input side of the transformer.

7. Claim 7

185. In my opinion, Takeshima renders obvious Claim 7.

186. As discussed above, Takeshima renders obvious Claim 3. And as discussed further below, Takeshima teaches and renders obvious wherein the power semiconductor devices comprise output switches.

187. By reference again to the picture from the Claim 3 analysis for Takeshima discussed above, the power semiconductor devices (circled in blue) are MOSFET output switches on the secondary winding side of the transformer and connected to “V_{OUT}”:



See Ex. 1010 at Fig. 14 (annotated), 19:36-37 (“A direct current voltage V_{OUT} is output from ends of the output....”), 19:24-28. As discussed in Ground I, for example, a POSITA would have recognized those symbols as the symbols for switches, and they are responsible for rectifying the transformer secondary waveforms to create the output voltage. Therefore, they are output switches. *See* Ex. 1008 at, *e.g.*, Fig. 2.13(b).

E. Ground V: Claims 1-7 Are Rendered Obvious by Takeshima in View of Spiazzi.

1. Claim 1

188. In my opinion, Claim 1 is rendered obvious by Takeshima in view of Spiazzi.

a. 1[preamble]

189. In my opinion, Claim 1[preamble] is rendered obvious by Takeshima in view of Spiazzi. *See* §VIII.D.1.a.

b. 1[a]

190. In my opinion, Claim 1[a] is rendered obvious by Takeshima in view of Spiazzi. *See* §VIII.D.1.b.

c. 1[b]

191. In my opinion, Claim 1[b] is rendered obvious by Takeshima in view of Spiazzi. *See* §VIII.D.1.c.

d. 1[c]

192. In my opinion, Claim 1[c] is rendered obvious by Takeshima in view of Spiazzi. *See* §VIII.D.1.d.

e. 1[d]

193. In my opinion, Claim 1[d] is rendered obvious by Takeshima in view of Spiazzi. *See* §VIII.D.1.e.

f. 1[e]

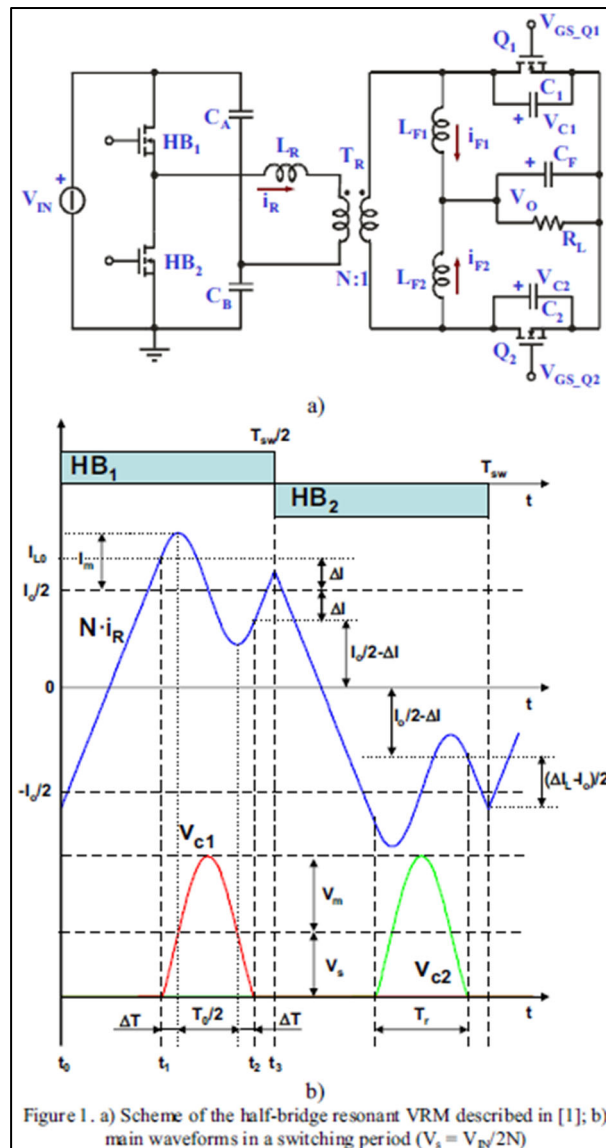
194. In my opinion, Takeshima and Spiazzi render this limitation obvious. *See* §VIII.D.1.f.

195. As discussed above, Takeshima's half-bridge circuit would be powered over time with equal (or approximately equal) power on the top and bottom of the printed circuit board, such that a POSITA would have expected equal (or at least approximately equal) power dissipation levels P_t and P_b . *See* §VIII.D.1.f. In combining Takeshima with Spiazzi, this result is confirmed, as explained below.

196. Spiazzi teaches a half-bridge converter, similar to Takeshima's half-bridge converter circuit in Takeshima Figure 14. *See* Ex. 1011 at Fig. 1.a ("half-bridge resonant VRM"). Spiazzi then performs a thermal mapping of two different configurations of its power converter, and shows the top sides of the two different configurations in Figure 11. *See* Ex. 1011 at 2000. Although only the top sides of the two different configurations are shown, Spiazzi teaches that "*/s/imilar results*

were obtained for the downward surfaces.” *See* Ex. 1011 at 1999. A POSITA would therefore have recognized that, when Takeshima’s circuit is operated in the manner and environment of Spiazzi, then the power dissipation levels P_t and P_b would at least be “similar” and well within 150% of each other. *See id.*

197. A POSITA would have expected this result in Spiazzi’s environment and configuration because, as with Takeshima’s half-bridge converter, Spiazzi expressly recognizes that its half-bridge converter should be powered with equal current, voltage, and power on the top and bottom MOSFET switches, as shown, for example, by the equal magnitude and width voltage curves as well as the equal (but inverted) current curve in the HB_1 and HB_2 phases (corresponding to top Q1 MOSFETs and bottom Q2 MOSFETs) shown in Spiazzi’s Figure 1.b. *See* Ex. 1011 at Fig. 1.b:



198. Spiazzi provides a thermal analysis of the power converter circuit described in Ex. 1012³, which teaches regarding its circuit: “During the negative half cycle of a switching period T_{sw} , the behavior of the circuit is the same as

³ See Ex. 1011 at 1993, 2000 (reference [1]).

during the positive half cycle. The only difference is that switches Q_1 and Q_2 change roles.” *See* Ex. 1012 at 82; *see also, e.g.*, EX1012 at Fig. 1.

2. Claim 2

199. In my opinion, Takeshima in view of Spiazzi renders obvious Claim 2.

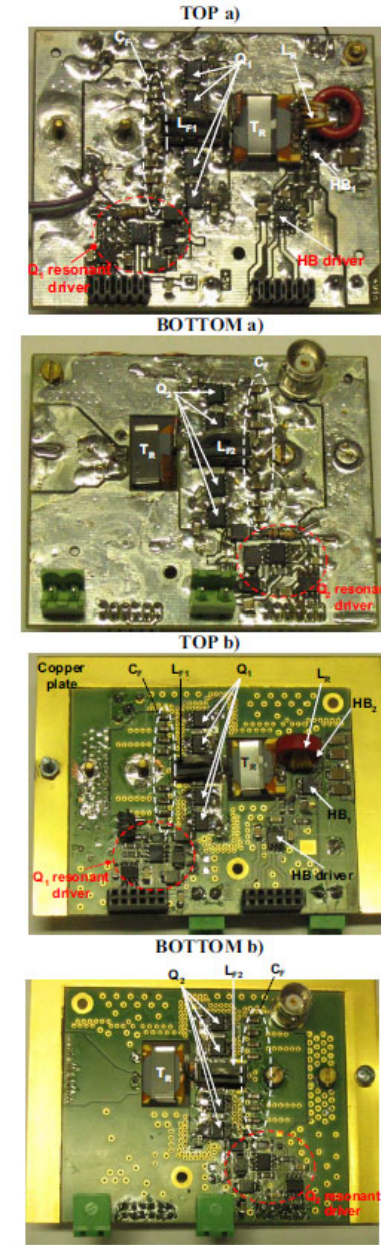
200. As discussed above, Takeshima in view of Spiazzi render obvious Claim 1. And as discussed further below, Takeshima in view of Spiazzi teach or at least render obvious wherein a plurality of the power semiconductor devices in the first set are each positioned in a location on the top surface substantially overlapping a location on the bottom surface occupied by a power semiconductor device in the second set. *See also* §VIII.D.2.

201. As discussed above in §VIII.D.2, Takeshima expressly shows direct overlap of the relevant MOSFET components in one dimension, and teaches or at least renders obvious that they would also overlap in the second dimension. *See* Ex. 1010 at Fig. 2, 10:51-66. Such overlap would have been further motivated by virtue of Spiazzi's teachings as to the layout of MOSFET switches on the top and bottom of the PCB. As shown here, Spiazzi's two PCBs show overlap between the four MOSFETs on the top side of each PCB (Q1) and the corresponding set of four MOSFETs on the bottom side of each respective PCB (Q2). Such layouts were common, as a POSITA would have known.

3. Claim 3

202. In my opinion, Claim 3 is rendered obvious by Takeshima in view of Spiazzi. *See* §VIII.D.3.

4. Claim 4



203. In my opinion, Claim 4 is rendered obvious by Takeshima in view of Spiazzi. *See* §VIII.D.4.

5. Claim 5

204. In my opinion, Claim 5 is rendered obvious by Takeshima in view of Spiazzi. *See* §VIII.D.5.

6. Claim 6

205. In my opinion, Claim 6 is rendered obvious by Takeshima in view of Spiazzi. *See* §VIII.D.6.

7. Claim 7

206. In my opinion, Claim 7 is rendered obvious by Takeshima in view of Spiazzi. *See* §VIII.D.7.

F. Ground VI: Claims 1-7 Are Rendered Obvious by Takeshima in View of Wanes

1. Claim 1

207. In my opinion, Claim 1 is rendered obvious by Takeshima in view of Wanes.

a. 1[preamble]

208. In my opinion, Claim 1[preamble] is rendered obvious by Takeshima in view of Wanes. *See* §VIII.D.1.a.

b. 1[a]

209. In my opinion, Claim 1[a] is rendered obvious by Takeshima in view of Wanes. *See* §VIII.D.1.b.

c. 1[b]

210. In my opinion, Claim 1[b] is rendered obvious by Takeshima in view of Wanes. *See* §VIII.D.1.c.

d. 1[c]

211. In my opinion, Claim 1[c] is rendered obvious by Takeshima in view of Wanes. *See* §VIII.D.1.d.

e. 1[d]

212. In my opinion, Claim 1[d] is rendered obvious by Takeshima in view of Wanes. *See* §VIII.D.1.e.

f. 1[e]

213. In my opinion, Claim 1[e] is rendered obvious by Takeshima in view of Wanes. *See* §VIII.D.1.f.

2. Claim 2

214. In my opinion, Takeshima in view of Wanes render obvious Claim 2.

215. As discussed above, Takeshima in view of Wanes render obvious Claim 1. And as discussed further below, Takeshima in view of Wanes teach and render obvious wherein a plurality of the power semiconductor devices in the first set are each positioned in a location on the top surface substantially overlapping a location on the bottom surface occupied by a power semiconductor device in the second set.

216. Takeshima expressly shows direct overlap in one dimension, and teaches or at least renders obvious the overlap in the second dimension. *See* §VIII.D.2. Wanes's further renders such overlap obvious, as shown, for example, in Wanes's Figures 1A and 9A-B. *See* §VIII.C.4. It was well-known in the art to overlap components for dense component placement, so a POSITA would have understood Wanes as confirming a reasonable expectation of success and rendering obvious Takeshima's overlap.

3. Claim 3

217. In my opinion, Claim 3 is rendered obvious by Takeshima in view of Wanes. *See* §VIII.D.3.

4. Claim 4

218. Claim 4 is rendered obvious by Takeshima in view of Wanes. *See* §VIII.D.4. Wanes teaches a POSITA to mirror, such that a POSITA would have been motivated to, and had a reasonable expectation of success in, mirroring a Takeshima cell in accordance with this claim. *See* §VIII.C.4; Ex. 1010 at 14:60-15:8, Fig. 8.

5. Claim 5

219. In my opinion, Claim 5 is rendered obvious by Takeshima in view of Wanes. *See* §VIII.D.5.

6. Claim 6

220. In my opinion, Claim 6 is rendered obvious by Takeshima in view of Wanes. *See* §VIII.D.6.

7. Claim 7

221. In my opinion, Claim 7 is rendered obvious by Takeshima in view of Wanes. *See* §VIII.D.7.

G. Ground VII: Claim 1-7 Are Rendered Obvious By Ericsson-BMR In View Of Takeshima, Or, Alternatively, By BMR 2008 In View Of Takeshima

1. Claim 1

222. In my opinion, Claim 1 is rendered obvious by Ericsson-BMR in view of Takeshima.

a. 1[preamble]

223. In my opinion, Claim 1[preamble] is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VIII.A.1.a.

b. 1[a]

224. In my opinion, Claim 1[a] is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VIII.A.1.b.

c. 1[b]

225. In my opinion, Claim 1[b] is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §§VIII.A.1.c; VIII.D.1.c.

d. 1[c]

226. In my opinion, Claim 1[c] is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VIII.A.1.d.

227. If Ericsson-BMR is not found to have taught, or at least rendered obvious, that the windings of the transformer are formed by traces in one or more of the conductive layers of the PCB, in my opinion, Takeshima teaches this, and a POSITA would have been motivated to form, and had a reasonable expectation of success in forming, Ericsson-BMR's windings in the manner taught by Takeshima for a number of reasons, including because it was well known to be more space efficient and further because, as discussed above, Ericsson-BMR does not provide for the traces to be anywhere but the PCB. *See* §VIII.D.1.d.

e. 1[d]

228. In my opinion, Claim 1[d] is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VIII.A.1.e. Takeshima further confirms that output FETs could be placed symmetrically. This would have been an obvious design choice for Ericsson-BMR's layout. *See* §VIII.D.1.e.

f. 1[e]

229. In my opinion, Claim 1[e] is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VIII.A.1.f.

2. Claim 2

230. In my opinion, Claim 2 is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VIII.A.2.

3. Claim 3

231. In my opinion, Claim 3 is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VIII.A.3.

4. Claim 4

232. In my opinion, Claim 4 is rendered obvious by Ericsson-BMR in view of Takeshima.

233. Takeshima teaches mirroring two power converter modules, and a POSITA would have been motivated to mirror, and had a reasonable expectation of success in mirroring, Ericsson-BMR's power modules in the same way and for the same reason that a POSITA would have found it obvious to mirror Takeshima's power module. *See* §VIII.D.4; §VIII.A.4.

5. Claim 5

234. In my opinion, Claim 5 is rendered obvious by Ericsson-BMR in view of Takeshima, in the asserted embodiment where Ericsson-BMR's module is mirrored as taught by Takeshima. *See* §VIII.A.5; §VIII.D.5.

6. Claim 6

235. In my opinion, Claim 6 is rendered obvious by Ericsson-BMR in view of Takeshima, in the asserted embodiment where Ericsson-BMR's module (which comprises input cells) is mirrored as taught by Takeshima. *See* §VIII.C.6.

7. Claim 7

236. In my opinion, Claim 7 is rendered obvious by Ericsson-BMR in view of Takeshima. *See* §VIII.A.6.

8. BMR-2008

237. As noted above, the relevant teachings of BMR-2008 are substantially the same as the relevant teachings of Ericsson-BMR. *Compare* EX1007 at, *e.g.*, 1, 2, 5, 24, 31 *with* EX1026 at, *e.g.*, 1, 4, 13, 15, 20.

238. Therefore, in my opinion, Claims 1-7 are rendered obvious by BMR-2008 in view of Takeshima for the same reasons as they are rendered obvious by Ericsson-BMR in view of Takeshima as set forth in this Ground.

H. Ground VIII: Claims 1-7 Are Rendered Obvious By Spiazzi In View Of Wanes

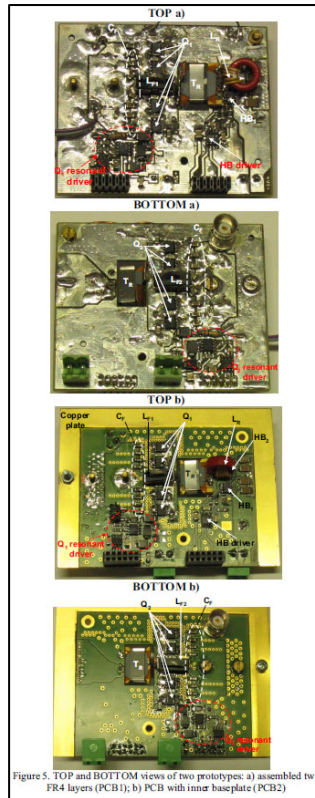
1. Claim 1

239. In my opinion, Claim 1 is rendered obvious by Spiazzi in view of Wanes.

a. 1[preamble]

240. In my opinion, Claim 1[preamble] is rendered obvious by Spiazzi in view of Wanes.

241. Spiazzi teaches an apparatus that can be seen, for example, in Figure 5:



Ex. 1011 at Fig. 5 (annotations in original).

b. 1[a]

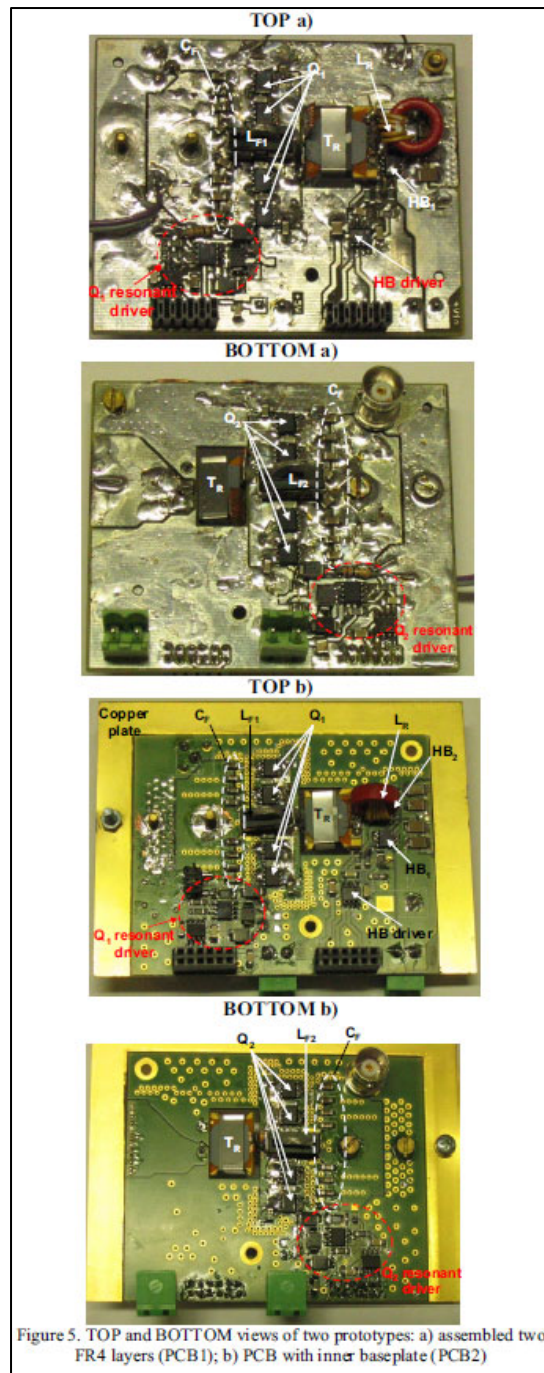
242. In my opinion, Claim 1[a] is rendered obvious by Spiazzi in view of Wanes.

243. Spiazzi teaches a power converter, which it refers to as a Voltage Regulator Module (VRM). *See* Ex. 11 at 1993 (“High frequency dc-dc converters for Voltage Regulator Module (VRM) applications require a great attention on the physical realization....”); *see also id.* at 2000 (“In this paper, practical issues regarding the physical realization of a 1.8 MHz VRM described in [1] have been discussed in detail.”).

c. 1[b]

244. In my opinion, Claim 1[b] is rendered obvious by Spiazzi in view of Wanes.

245. Spiazzi teaches that the power converter shown in Figure 5(a) is a “three layer PCB” while the power converter shown in Figure 5(b) is a PCB “built assembling two epoxy layers ... on both sides of 0.7 mm thick copper baseplate...” See Ex. 1011 at 1995. The top and bottom surfaces of each PCB are visible in Figure 5:



Ex. 1011 at Fig. 5 (annotations in original). As a POSITA would have recognized, at least the top and bottom layers of these PCBs are conductive, as that conductivity is what permits the electric components mounted thereon to interact

with each other. *See also* Ex. 1009 at 4:33-34 (“primary windings are embedded in internal tracks in internal *layers* in PCB 104.”).

d. 1[c]

246. In my opinion, Claim 1[c] is rendered obvious by Spiazzi in view of Wanes.

247. Spiazzi teaches a magnetic core structure that is magnetically coupled to windings. *See* Ex. 1011 at, *e.g.*, 1994 (“The core employed was a planar ER 14.5/3/7 3F4 material from Ferroxcube and the windings [were] constructed by” the following process.”).

248. Spiazzi’s windings are not formed by traces in one or more of the conductive layers in the PCB. However, Wanes does teach the layout approach of using the converter PCB to form windings. *See* Ex. 1009 at 4:10-12 (“primary windings are embedded in internal layers in 104,” where element 104 is the PCB), 4:31-48, 9:44-51 (“Windings (not shown) are sandwiched within each PCB and encircle openings 414 and 416. Each winding of PCB 104 cooperates with a respective winding of the magnetics of transformer 112 and inductor 14....”).

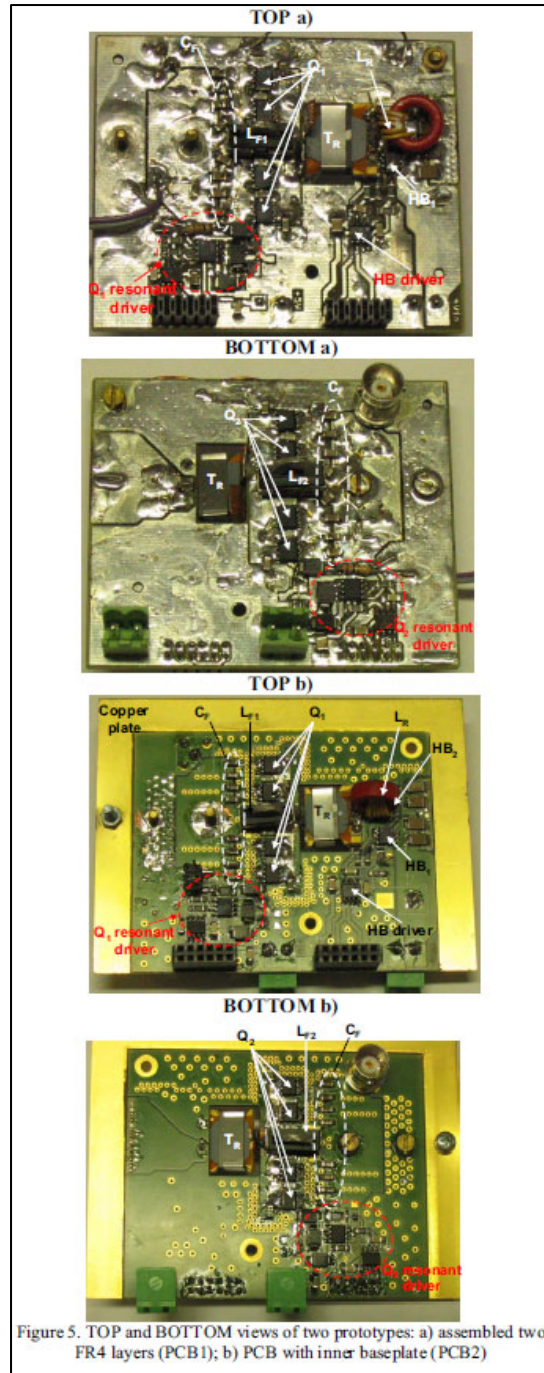
249. A POSITA would have been motivated to form Spiazzi’s windings in the manner described in Wanes for a number of reasons. For example, forming windings as traces in the conductive layers was a well-known technique in the art (*see, e.g.*, Ex. 1019 at 1:54-60) and it was known to be space efficient, so forming

the traces in that manner would have been obvious to a POSITA, particularly as a layout used for R&D was moving towards potential commercialization.

e. 1[d]

250. In my opinion, Claim 1[d] is rendered obvious by Spiazzi in view of Wanes.

251. Spiazzi's Figure 5 shows a set of four MOSFETs labelled Q1 that are mounted on the top surface of the PCB and are overlapping with a set of four MOSFETs labelled Q2 mounted on the bottom surface of the PCB:



Ex. 1011 at Fig. 5 (annotations in original). Q_1 on these PCBs are each a first set of power semiconductor devices mounted on the top surface and electrically connected to dissipate power at a level, P_t , during operation of the converter, while Q_2 on these PCBs are each a second set of power semiconductor devices being

mounted on the bottom surface of the PCBs and electrically connected to dissipate power at a level, P_b , during operation of the converter.

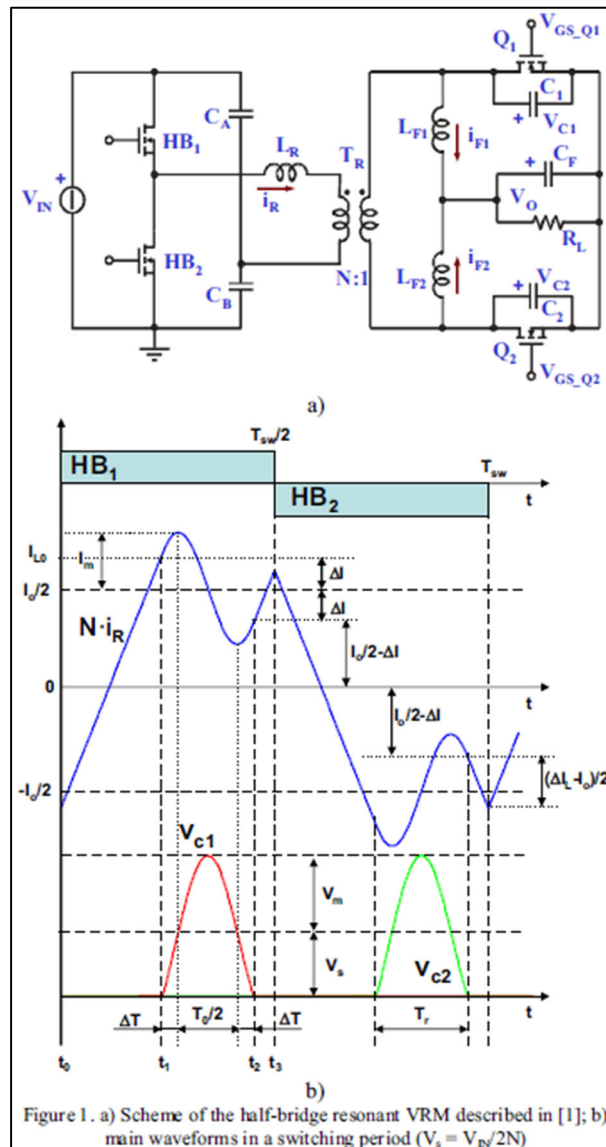
f. 1[e]

252. In my opinion, Claim 1[e] is rendered obvious by Spiazzi in view of Wanes.

253. As discussed in §VIII.E.1.f, Spiazzi teaches a half-bridge converter. *See* Ex. 1011 at Fig. 1.a (“half-bridge resonant VRM”). Spiazzi then performs a thermal mapping of two different configurations of its power converter, and shows the top sides of the two different configurations in Figure 11. *See* Ex. 1011 at 2000. Although only the top sides of the two different configurations are shown, Spiazzi teaches that “[s]imilar results were obtained for the downward surfaces.” *See* Ex. 1011 at 1999. A POSITA would therefore have recognized that, in Spiazzi, the power dissipation levels P_t and P_b would at least be “similar” and well within 150% of each other on top and bottom. *See id.*

254. A POSITA would have expected this result in Spiazzi’s physical environment and configuration because Spiazzi expressly recognizes that its half-bridge converter should be powered with equal current, voltage, and power on the top and bottom MOSFETs, as shown, for example, by the equal magnitude and width voltage curves as well as the equal (but inverted) current curve in the HB₁

and HB₂ phases (corresponding to top Q1 MOSFETs and bottom Q2 MOSFETs) shown in Spiazzi's Figure 1.b. See Ex. 1011 at Fig. 1.b:



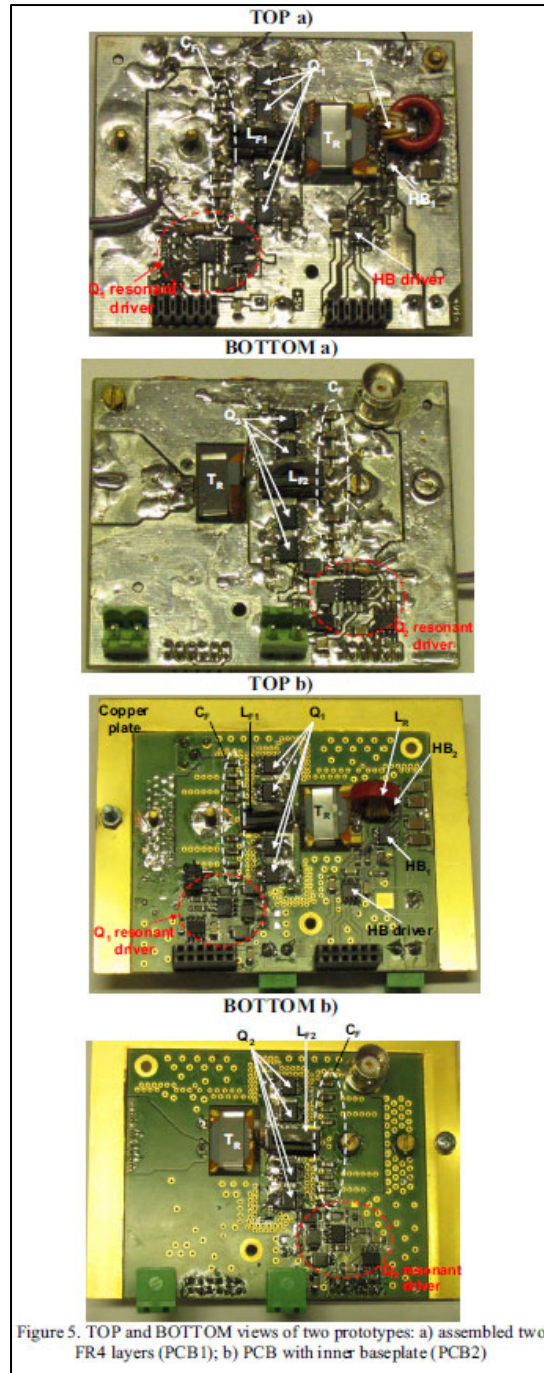
255. Spiazzi is a thermal analysis of the power converter circuit described in Ex. 1012⁴, which teaches regarding its circuit: “During the negative half cycle of

⁴ See Ex. 1011 at 1993, 2000 (reference [1]).

a switching period T_{sw} , the behavior of the circuit is the same as during the positive half cycle. The only difference is that switches Q_1 and Q_2 change roles.” See Ex. 1012 at 82; *see also, e.g.*, EX1012 at Fig. 1.

2. Claim 2

256. In my opinion, Claim 2 is rendered obvious by Spiazzi in view of Wanes. As can be seen in Figure 5, the plurality of power semiconductor devices in Q1 of each PCB are each positioned in a location on the top surface that overlap the location on the bottom surface occupied by the power semiconductor devices in Q2:

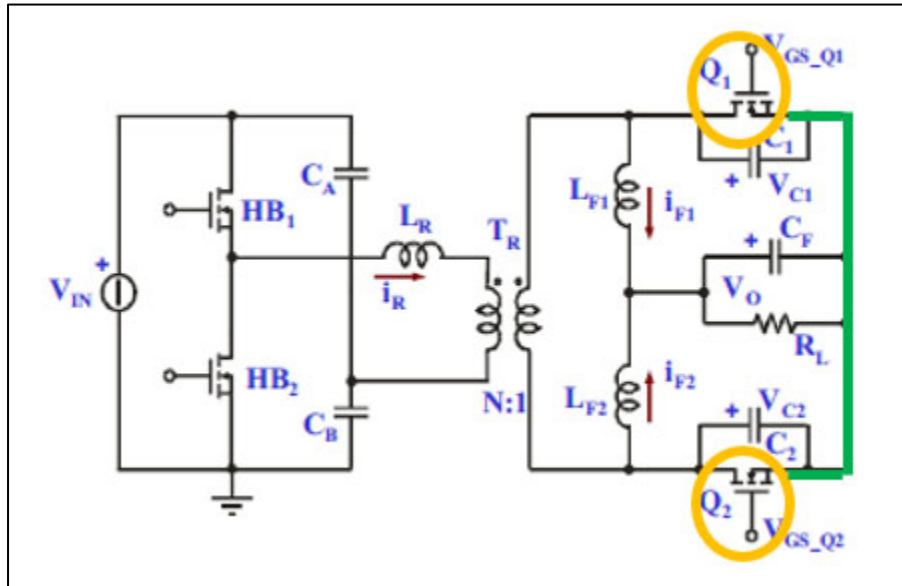


Ex. 1011 at Fig. 5 (annotations in original).

3. Claim 3

257. In my opinion, Claim 3 is rendered obvious by Spiazzi in view of Wanes.

258. As highlighted in green in this annotated version of Spiazzi's Figure 1(a), Spiazzi teaches that the four power semiconductor devices on the top side of each board (Q1) share a connection with the four power semiconductor devices on the bottom side of the respective board (Q2):



Ex. 1011 at Fig. 1(a) (annotated). As a POSITA would have recognized or at least found obvious, a shared set of respective set of conductive vias in the PCB would have been used to connect the power semiconductor devices in Q1 and Q2, because Q1 power semiconductor devices are on the top side of the PCBs and Q2 power semiconductor devices are on the bottom side of the PCBs.

4. Claim 4

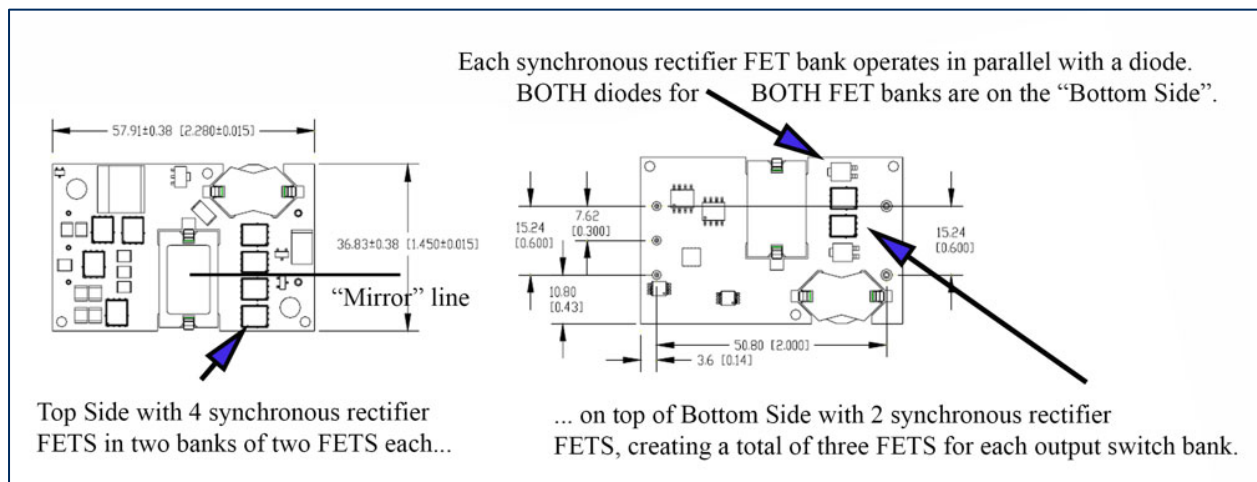
259. In my opinion, Claim 4 is rendered obvious by Spiazzi in view of Wanes.

260. Each Spiazzi PCB is, in its entirety a repeatable cell, and Wanes teaches mirroring cells. *See* §VIII.C.4. A POSITA would therefore have found it obvious, and had a reasonable expectation of success, in mirroring Spiazzi's cell for the same reasons as a POSITA would have found it obvious to mirror Ericsson-BMR's cell. *See* §VIII.C.4.

5. Claim 5

261. In my opinion, Claim 5 is rendered obvious by Spiazzi in view of Wanes.

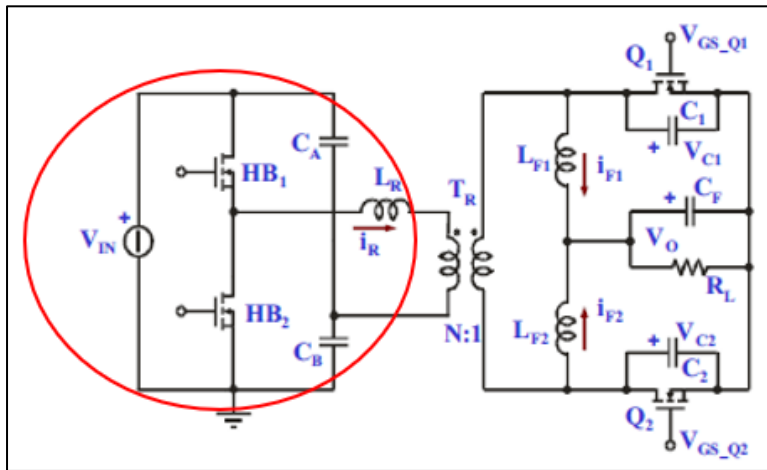
262. When Spiazzi's cells are mirrored as taught by Wanes, a component from the first cell would be located on an opposite surface of a respective component from the second cell. *See* §VIII.C.5; *see also* Ex. 1029 at 3 (annotated):



6. Claim 6

263. In my opinion, Claim 6 is rendered obvious by Spiazzi in view of Wanes.

264. In this Ground, each Spiazzi converter is, in its entirety, considered a cell, and each converter is comprised of an input cell that receives an input voltage for regulation:



See Ex. 1011 at Fig. 1(a) (annotated).

7. Claim 7

265. In my opinion, Claim 7 is rendered obvious by Spiazzi in view of Wanes.

266. Spiazzi teaches that Q_1 and Q_2 power semiconductor devices are “synchronous rectifier (SR) switches.” See Ex. 1011 at 1993; see also *id.* at, e.g., Fig. 1(a) (Q_1 and Q_2 are output switches in the circuit diagram).

IX. OBJECTIVE INDICIA OF NON-OBVIOUSNESS

267. I am not aware of any evidence of objective indicia (or “secondary considerations”) with a nexus to the Challenged Claims of the ’761 patent that would support a finding of non-obviousness or otherwise impact my analysis.

268. I am not aware of any evidence of commercial success of Patent Owner’s products due specifically to the alleged invention in the Challenged Claims, as opposed to other factors that may have contributed to any commercial success of those products (if there is any commercial success at all), such as marketing.

269. I am not aware of skepticism by those having ordinary skill in the art at the time of the alleged invention regarding the possibility, utility, or success of the alleged invention of the Challenged Claims, nor am I aware of praise of the alleged invention in the Challenged Claims. In fact, prior to my engagement by Petitioner for purposes of providing my opinion herein, I had never heard of the ’761 patent.

270. I am not aware of any unexpected results achieved by the alleged invention of the Challenged Claims. To the contrary, as explained above, the functional result claimed in the the Challenged Claims was the predictable result of symmetric PCB layouts as shown in the prior art discussed above.

271. I am not aware of any long-felt but unsolved need in the art that was satisfied by the alleged invention of the Challenged Claims.

272. I am not aware of any failure by others to make the alleged invention of the Challenged Claims.

273. I am not aware of any copying of the alleged invention in the Challenged Claims by others in the field. I understand from counsel that Patent Owner has accused Petitioner of copying Patent Owner's products, but I further understand that such alleged copying has not been proven.

274. I understand that Patent Owner has publicly alleged that "in 2021 a leading artificial intelligence ('AI') OEM licensed the Vicor Patents" that includes the '761 patent, but I am not aware of any evidence that any such licenses were entered into because of a desire to license the '761 patent, as opposed to a desire to license any other patents that may be covered by any such license (which I have not seen and I understand from counsel has not been made of record in this proceeding).

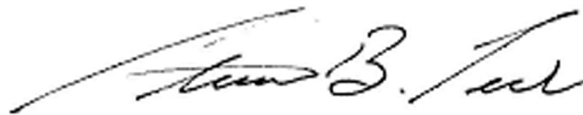
X. CONCLUSION

275. Based on the above, it is my opinion that the Challenged Claims of the '761 patent are obvious.

276. I hereby declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements are punishable by fine or imprisonment or both. *See* 18 U.S.C. § 1001.

Date: November 13, 2023

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Steven B. Leeb", written in a cursive style.

Steven B. Leeb, Ph.D.

APPENDIX: CLAIM LISTING

Claim Number	Claim Language
1[preamble]	An apparatus comprising:
1[a]	a power converter including
1[b]	a printed circuit board (PCB) comprising a plurality of conductive layers and having a top Surface and a bottom surface;
1[c]	a magnetic core structure magnetically coupled to a winding formed by traces in one or more of the conductive layers in the PCB; and
1[d]	a plurality of power semiconductor devices, a first set of the power semiconductor devices being mounted on the top Surface and electrically connected to dissipate power at a level, Pt, during operation of the converter, a second set of the power semiconductor devices being mounted on the bottom Surface and electrically connected to dissipate power at a level. Pb, during operation of the converter;
1[e]	wherein the power semiconductor devices are distributed between the first and second sets to distribute heat generation during operation of the converter Such that each level Pt, Pb is less than 150% of the other level Pb, Pt.
2	The apparatus of claim 1 wherein a plurality of the power semiconductor devices in the first set are each positioned in a location on the top surface Substantially overlapping a location on the bottom Surface occupied by a power semiconductor device in the second set.
3	The apparatus of claim 1 wherein the power semiconductor devices are electrically connected using a respective set of conductive vias in the PCB, and a plurality of the power semiconductor devices in the first set share their respective sets of conductive Vias with corresponding power semiconductor devices in the second set.
4	The apparatus of claim 2 wherein the power converter further comprises circuitry including a pair of cells having a common circuit

	topology and each including power semiconductor Switches from each of the first and second sets; each cell having its respective components arranged in a pattern, wherein the pattern of components of one cell is Substantially a mirror image of the pattern of components in the other cell.
5	The apparatus of claim 4 wherein a component from one of the cells is located on an opposite Surface of a respective component from the other one of the cells.
6	The apparatus of claim 5 wherein the cells comprise input cells.
7	The apparatus of claim 3 wherein the power semiconductor devices comprise output Switches.