8110667

THE UNITED STATES OF AMERICA

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UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

May 11, 2021

THIS IS TO CERTIFY THAT ANNEXED IS A TRUE COPY FROM THE RECORDS OF THIS OFFICE OF THE FILE WRAPPER AND CONTENTS OF:

APPLICATION NUMBER: *14/635,467*
FILING DATE: *March 02, 2015*
PATENT NUMBER: *9516761*
ISSUE DATE: *December 06, 2016*

Certified by

Under Secretary of Commerce
for Intellectual Property
and Director of the United States
Patent and Trademark Office

FISH.
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March 2, 2015

Attorney Docket No.: 00614-0168003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Presented for filing is a new divisional patent application of:

Inventor(s): PATRIZIO VINCIARELLI, MICHAEL B. LAFLEUR, SEAN TIMOTHY FLEMING, RUDOLPH F. MUTTER, and ANDREW T. D'AMICO

Title: PANEL-MOLDED ELECTRONIC ASSEMBLIES

This application claims the benefit of priority to the following application(s):

Application No.	Country	Filing Date (MM/DD/YYYY)
13/105,696	United States	05/11/2011

Enclosed are the following papers, including those required to receive a filing date under 37 C.F.R. § 1.53(b):

	Pages
Specification	43
Claims	22
Abstract	1
Drawing(s)	38

Enclosures:

— Application Data Sheet, 7 pages.
— Preliminary Amendment, 18 pages.
— New disclosure information, including:
Information disclosure statement, 1 page.
PTO-1449, 1 page.

Basic Filing Fee	$280
Search Fee	$600
Examination Fee	$720

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March 2, 2015

Total Claims 94	over 20	**74 x $80**	$5920
Independent Claims 6	over 3	**3 x $420**	$1260
Fee for Multiple Dependent claims			$0
Application size fee for each 50 pages over 100 Total Sheets: 104x .75 - 100/50 = 0x			$0
Surcharge - Late filing fee, search fee, examination fee or oath or declaration			$140
Total Filing fee			$8920

The filing fee in the amount of $8920 is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply all charges or credits to Deposit Account 06-1050, referencing Attorney Docket 00614-0168003.

If this application is found to be incomplete, or if a telephone conference would otherwise be helpful, please call the undersigned at (617) 542-5070.

Please direct all correspondence to the following:

26214
PTO Customer Number

Respectfully submitted,

/Rex I. Huang/

Rex I. Huang

Reg. No. 57,661
Enclosures
RIH/pxm
23361973.doc

PTO/AIA/14 (12-13)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00614-0168003
	Application Number	
Title of Invention	PANEL-MOLDED ELECTRONIC ASSEMBLIES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Patrizio		Vinciarelli	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Boston	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	294 Beacon Street		
Address 2			
City	Boston	State/Province	MA
Postal Code	02116	Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Michael	B.	LaFleur	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	East Hampstead	State/Province	NH	Country of Residence i	US

Mailing Address of Inventor:

Address 1	5 Atwood Drive		
Address 2			
City	East Hampstead	State/Province	NH
Postal Code	03826	Country i	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Sean	Timothy	Fleming	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00614-0168003
	Application Number	
Title of Invention	PANEL-MOLDED ELECTRONIC ASSEMBLIES	

City	Worcester	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	6 Mellor Avenue		
Address 2			
City	Worcester	State/Province	MA
Postal Code	01606	Country i	US

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Rudolph	F.	Mutter	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	North Andover	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	95 Phillips Common		
Address 2			
City	North Andover	State/Province	MA
Postal Code	01845	Country i	US

Inventor 5 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Andrew	T.	D'Amico	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	Beverly Hills	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	3046 Franklin Canyon Drive		
Address 2			
City	Beverly Hills	State/Province	CA
Postal Code	90210	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00614-0168003
	Application Number	
Title of Invention	PANEL-MOLDED ELECTRONIC ASSEMBLIES	

Customer Number	26214		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	PANEL-MOLDED ELECTRONIC ASSEMBLIES		
Attorney Docket Number	00614-0168003	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	38	Suggested Figure for Publication (if any)	7

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	26214		

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00614-0168003
	Application Number	
Title of Invention	PANEL-MOLDED ELECTRONIC ASSEMBLIES	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Division of	13105696	2011-05-11

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) [i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00614-0168003
	Application Number	
Title of Invention	PANEL-MOLDED ELECTRONIC ASSEMBLIES	

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	VLT, Inc.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00614-0168003
	Application Number	
Title of Invention	PANEL-MOLDED ELECTRONIC ASSEMBLIES	

Mailing Address Information:			
Address 1	560 Oakmead Parkway		
Address 2			
City	Sunnyvale	**State/Province**	CA
Country i	US	Postal Code	94086
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00614-0168003
	Application Number	
Title of Invention	PANEL-MOLDED ELECTRONIC ASSEMBLIES	

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications					
Signature	/Rex I. Huang/			Date (YYYY-MM-DD)	2015-03-02
First Name	Rex I.	Last Name	Huang	Registration Number	57661
Additional Signature may be generated within this form by selecting the Add button. Add					

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor	:	Patrizio Vinciarelli	Art Unit	:	Unknown
Serial No.	:	To be assigned	Examiner	:	Unknown
Filed	:	Herewith			
Title	:	PANEL-MOLDED ELECTRONIC ASSEMBLIES			

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Please consider the references listed on the enclosed PTO-SB-08 or Disclosure Form. Foreign patent document and non-patent literature are enclosed; cited U.S. patents and patent application publications will be provided on request.

Under 35 USC §120, this application relies on the earlier filing date of application serial number 13/105,696, filed on May 11, 2011. The references were submitted to and/or cited by the Office in the prior application and, therefore, are not provided in this application.

This statement is being filed with the application.

Apply any necessary charges or credits to deposit account 06-1050, referencing the above attorney docket number.

Respectfully submitted,

Date: March 2, 2015

/Rex I. Huang/
Rex I. Huang
Reg. No. 57,661

Customer Number 26214
Fish & Richardson P.C.
Telephone: (617) 542-5070
Facsimile: (877) 769-7945

23361950.doc

Substitute Disclosure Form	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 00614-0168003	Application No
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant VLT, Inc.	
		Filing Date	Group Art Unit

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1	2002/0096348	07/25/2002	Saxelby et al.			
	2	2004/0100778	05/27/2004	Vinciarelli et al.			
	3	2007/0241440	10/18/2007	Hoang et al.			
	4	2010/0197150	08/2010	Smejtek			
	5	2010/0246152	09/30/2010	Lin et al.			
	6	2012/0287582	11/15/2012	Vinciarelli et al.			
	7	4,366,342	12/1982	Breedlove			
	8	4,551,747	11/1985	Gilbert et al.			
	9	5,241,133	08/1993	Mullen et al.			
	10	5,728,600	03/17/1998	Saxelby, Jr. et al.			
	11	5,864,092	01/1999	Gore et al.			
	12	6,403,009	06/11/2002	Saxelby, Jr. et al.			
	13	6,830,959	12/2004	Estacio			
	14	6,940,013	09/06/2005	Vinciarelli et al.			
	15	7,361,844	04/22/2008	Vinciarelli et al.			
	16	7,972,143	07/2011	Smejtek			
	17	8,427,269	04/23/2013	Vinciarelli			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	18	WO1995/027308	10/12/1995	WIPO				

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	19	AFM Microelectronics Inc., "General Purpose Capacitors", www.afmmicroelectronics.com , 13 pages, published on or before July 26, 2010
	20	International Search Report and Written Opinion, PCT/US2012/37495, May 6, 2013, 18 pages.
	21	Kahn, "Technical Information: Multilayer Ceramic Capacitors – Materials and Manufacture", Microelectronics Inc., 9 pages, published on or before July 26, 2010
	22	U.S. Patent Application Serial No. 12/493,773, entitled "Encapsulation Method and Apparatus for Electronic Modules", Application and Preliminary Amendment filed June 29, 2009, 63 pages (24499-0009001)

Examiner Signature	Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor	:	Patrizio Vinciarelli	Art Unit	:	Unknown
Serial No.	:	To be assigned	Examiner	:	Unknown
Filed	:	Herewith			
Title	:	PANEL-MOLDED ELECTRONIC ASSEMBLIES			

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Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Prior to examination, please amend the application as indicated on the following pages.

Amendments to the Specification:

Please add the following new paragraph before "Field of the Invention" on page 1:

CLAIM OF PRIORITY

[001] This application is a divisional of and claims priority under 35 USC 121 to U.S. Application Serial No. 13/105,696, filed on May 11, 2011 (U.S. Patent No. 8,966,747 to be issued on March 3, 2015). This application is related to U.S. Patent Application Serial No._____, filed on March 2, 2015, titled "PANEL-MOLDED ELECTRONIC ASSEMBLIES," attorney docket 00614-0168002. The entire contents of the above applications are herein incorporated by reference.

Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. – 48. (Cancelled).

49. (Original) An apparatus comprising:

a first mold panel comprising

an exterior surface,

an interior surface defining an internal cavity,

a clamp region located at points along a circumference of the internal cavity, and

an opening,

the first mold panel being adapted to

(a) be engaged by pressure in the clamp region,

(b) receive in the cavity a circuit panel containing a plurality of components and mold compound to fill empty spaces in the internal cavity, and

(c) be cut after curing of the mold compound.

50. (Original) The apparatus of claim 49 wherein the interior surface in the region of the internal cavity is adapted to adhere to the mold compound.

51. (Original) The apparatus of claim 49 further comprising

a second mold panel comprising

an exterior surface,

an interior surface, and

a clamp region,

wherein the second mold panel is adapted to

(a) close against and mate with the first mold panel,

(b) be engaged by pressure in the clamp region, and

(c) be cut after curing of the mold compound.

52. (Original) The apparatus of claim 51 wherein the interior surface of the second mold further defines a second internal cavity, the clamp region of the second mold panel is located at points along a circumference of the second internal cavity, and the internal cavity of the first mold panel is adapted to receive a first side of the circuit panel and the second internal cavity is adapted to receive a second opposite side of the circuit panel.

53. (Original) The apparatus of claim 52 further comprising contours formed in the interior surface of at least one of the mold panels.

54. (Original) The apparatus of claim 53 wherein the contours are adapted to match predetermined characteristics of selected ones of the plurality of components.

55. (Original) The apparatus of claim 53 wherein the internal surface of the mold panel is adapted to adhere to the molding compound.

56. (Original) The apparatus of claim 55 wherein the contours form interlocking features with cured mold compound.

57. (Original) The apparatus of claim 53 wherein at least one of the mold panels comprises a non-ferrous metal.

58. (Original) The apparatus of claim 57 wherein at least one of the mold panels comprises aluminum.

59. (Original) The apparatus of claim 51 wherein at least one of the mold panels comprises a thermally conductive material.

60. (Original) The apparatus of claim 53 wherein at least one of the mold panels comprises a non-metallic substance.

61. (Original) The apparatus of claim 51 further comprising at least one channel connected to the internal cavity for allowing expansion of the mold compound.

62. (Original) The apparatus of claim 51 further comprising at least one channel connected to the internal cavity for injecting mold compound into the internal cavity.

63. (Original) The apparatus of claim 59 wherein the exterior surface of the mold panel comprises a plurality of fins.

64. (Original) The apparatus of claim 59 wherein the exterior surface of the mold panel comprises a flat surface.

65. (Original) The apparatus of claim 64 wherein the flat surface is adapted for a solder joint.

66. (Original) The apparatus of claim 49 wherein the internal cavity includes features formed in the interior surface and arranged in a predetermined pattern.

67. (Original) The apparatus of claim 49 wherein the internal cavity includes features formed in the interior surface along lines through which the mold panel maybe cut to establish a setback from a cut edge of the mold panel.

68. (Original) The apparatus of claim 49 wherein the mold panel further comprises at least one registration feature adapted to engage and establish a predetermined relationship with the circuit panel.

69. (Original) The apparatus of claim 49 wherein one or more selected portions of the mold panel are adapted for incorporation into one or more products, the products being formed by a process which uses the mold panel to contain the molding compound.

70. (Original) The apparatus of claim 59 wherein the exterior surface of the mold panel comprises a flat surface with one or more pins protruding from the flat surface.

71. (Original) The apparatus of claim 59 wherein the exterior surface of the mold panel comprises a flat surface having one or more holes in the flat surface.

72. (Original) The apparatus of claim 71 further comprising a pin inserted into a respective one of the one or more holes.

73. (Original) An apparatus comprising:

a panel assembly having external surfaces defined by a first mold panel and a second mold panel;

the first and second mold panels forming an internal cavity enclosing an internal circuit board, the internal circuit board having a first surface and second surface and a plurality of components in an active circuit area on at least one of the surfaces, the components being electrically connected to interconnects contained within the internal cavity;

the internal cavity being filled with mold compound in spaces unoccupied by the circuit board and components;

the panel assembly being adapted to have first selected portions of the first and second mold panels cut away to expose the interconnects and to have second selected portions of the respective mold panels situated near the active circuit area remain attached to the assembly following the cut.

74. (Original) The apparatus of claim 73 wherein the panel assembly includes a clamp region located at points along a circumference of the first and second internal cavities, and the first selected portions comprise the clamp region.

75. (Original) An apparatus comprising:

a panel assembly having external surfaces defined by a first mold panel and a second mold panel;

the first and second mold panels forming an internal cavity enclosing an internal circuit board, the internal circuit board having a first surface and second surface and a plurality of components electrically connected to form a plurality of individual circuits, each individual circuit being electrically connected to respective interconnects located along a respective circuit perimeter, the interconnects being contained within the cavity.

76. (Original) The apparatus of claim 75 wherein the panel assembly is adapted to be cut along the circuit perimeter separating the individual circuits, dividing the panel assembly into individual circuit modules, and exposing selected portions of the interconnects.

77. (Original) The apparatus of claim 75 wherein the panel assembly is constructed to retain an integral layered structure after being filled with mold compound which is subsequently cured, the layered structure comprising a first layer including a portion of the first mold, a second layer including a portion of the mold compound, a third layer including a portion of the circuit board, a fourth layer including a portion of the mold compound, and a fifth layer including a portion of the second mold.

78. (Original) The apparatus of claim 75 wherein the internal circuit board comprises a plurality of circuits having the same functionality.

79. (Original) The apparatus of claim 75 further comprising one or more conduits connecting the internal cavity to an external opening.

80. (Original) The apparatus of claim 75 wherein spaces unoccupied by the circuit board, components, and interconnects in the internal cavity are filled with mold compound.

81. (Original) The apparatus of claim 80 wherein the mold compound has been cured.

82. (Original) The apparatus of claim 81 wherein selected portions of at least one of the mold panels have been removed, the selected portions being located near the circuit perimeters.

83. (Original) An apparatus comprising:

a modular package having a first external surface, a second external surface opposite the first external surface, and a side wall extending along the perimeter of and connecting with the first and second external surfaces, the modular package including a first layer defining the first external surface and a second layer defining the second external surface, the first and second layers being separated by and in contact with cured mold compound; and

an electrical circuit located between the first and second layers and within the cured mold compound and including at least one electrical component electrically connected to a plurality of interconnects;

the side wall comprising a strip formed by the first layer, a strip formed by the second layer, and a strip formed by the cured mold compound; and

the interconnects being disposed within the side wall.

84. (Original) The apparatus of claim 83 wherein the first and second layers further comprise a non-ferrous metal.

85. (Original) The apparatus of claim 84 wherein the first and second layers further comprise aluminum.

86. (Original) The apparatus of claim 85 wherein the first external surface further comprises a plurality of fins.

87. (Original) The apparatus of claim 85 wherein the first external surface further comprises an essentially flat area.

88. (Original) The apparatus of claim 87 wherein the essentially flat area is adapted for a solder joint.

89. (Original) The apparatus of claim 83 wherein the electrical circuit further comprises a circuit board and the side wall further comprises a strip formed by the circuit board and an additional strip formed by cured mold compound.

90. (Original) The apparatus of claim 89 wherein the interconnects further comprise conductive features in the circuit board.

91. (Original) The apparatus of claim 90 wherein the circuit board comprises a multilayer printed circuit board ("PCB") and each of the interconnects comprises a plurality of conductive layers in the PCB.

92. (Original) The apparatus of claim 90 wherein each of the interconnects comprises a plurality of conductive vias in the circuit board.

93. (Original) The apparatus of claim 83 further comprising interlocking features comprising a contour formed in an interior surface of the first layer, the contour being filled with cured mold compound.

94. (Original) The apparatus of claim 91 wherein the circuit board includes a top surface and a bottom surface and the at least one electrical component comprises a set of top-side components mounted on the top surface and a set of bottom-side components mounted on the bottom surface.

95. (Original) The apparatus of claim 94 wherein

the top-side components include a number, T, of large-footprint components, the bottom-side components include a number, B, of large-footprint components, and the number T is approximately equal to the number B.

96. (Original) The apparatus of claim 95 wherein each of most of the top-side large-footprint components shares a respective set of conductive vias with a corresponding one of the bottom-side large-footprint components.

97. (Original) The apparatus of claim 95 wherein each of most of the top-side large-footprint components is located in a respective footprint shared by a corresponding one of the bottom-side large-footprint components.

98. (Original) The apparatus of claim 89 wherein the circuit board includes a top surface and a bottom surface, the at least one electrical component comprises a number, T, of large-footprint components mounted on the top surface, and most of the large-footprint components are distributed symmetrically in relation to an axis on the top surface.

99. (Original) The apparatus of claim 98 wherein the axis is along a midline of the top surface.

100. (Original) The apparatus of claim 98 wherein the axis is defined in relation to a predetermined component.

101. (Original) The apparatus of claim 83 further comprising:

an adapter for providing mechanical and electrical connections between the modular package and an external mounting surface, the adapter having a body and a plurality of electrical terminals supported by the body; and

electrical connections formed between the adapter terminals and respective interconnects on the modular package;

the adapter body being mechanically secured to the modular package;

the adapter terminals being arranged to mate with the external mounting surface.

102. (Original) The apparatus of claim 101 wherein the external mounting surface is a circuit board and the terminals comprise ends constructed and arranged to be inserted into conductive holes in the circuit board.

103. (Original) The apparatus of claim 101 wherein the external mounting surface is a circuit board and the terminals comprise ends constructed and arranged to be surface mount soldered to the circuit board.

104. (Original) The apparatus of claim 101 wherein the external mounting surface includes a connector and the terminals comprise ends constructed and arranged to mate with the connector.

105. (Original) The apparatus of claim 101 wherein the interconnects are disposed along a long edge of the modular package, the adapter is secured to the long edge of the modular package, and the first and second layers of the modular package are oriented perpendicular to the mounting surface.

106. (Original) The apparatus of claim 101 wherein the interconnects are disposed along opposite edges of the modular package, the adapter is secured to the opposite edges, and the first and second layers of the modular package are oriented essentially parallel to the mounting surface.

107. (Original) The apparatus of claim 106 wherein the adapter is constructed and arranged to maintain one of the first or second layers in contact with the mounting surface.

108. (Original) The apparatus of claim 83 wherein the interconnects further comprise a surface constructed and arranged for engagement with a connector terminal.

109. (Original) The apparatus of claim 83 wherein the interconnects further comprise a layer of metal plating.

110. (Original) An apparatus comprising:

a modular package having a first external surface, a second external surface opposite the first external surface, and a side wall extending along the perimeter of and connecting with the first and second external surfaces, the modular package including a first layer of metal defining the first external surface and a second layer of metal defining the second external surface, the first and second layers being separated by and in contact with cured mold compound; and

an electrical circuit for converting power, including a printed circuit board ("PCB"), a plurality of components including semiconductors mounted to the PCB, and a plurality of interconnects electrically connected to the components, the electrical circuit being located between the first and second layers and within the cured mold compound;

the side wall comprising a strip formed by the first layer, a strip formed by the second layer, a strip formed by the PCB, and one or more strips formed by the cured mold compound;

the interconnects being disposed within the side wall.

111. (Original) The apparatus of claim 110 wherein the first and second layers further comprise aluminum, and the first external surface further comprises a plurality of fins.

112. (Original) The apparatus of claim 110 wherein the first and second layers further comprise aluminum, and the first external surface comprises an essentially flat area.

113. (Original) The apparatus of claim 112 wherein the essentially flat area is adapted for a solder joint.

114. (Original) The apparatus of claim 110 wherein the PCB includes a top surface and a bottom surface, the semiconductors include large-footprint switches, a number, T, of top-side large-footprint switches are mounted on the top surface, a number, B, of bottom-side large-footprint switches are mounted on the bottom surface, and the number T is approximately equal to the number B.

115. (Original) The apparatus of claim 114 wherein each large-footprint switch is connected to one or more other components by a respective set of conductive vias in the PCB, and each of a plurality of the top-side large-footprint switches shares its respective set of conductive vias with a corresponding one of the bottom-side large-footprint switches.

116. (Original) The apparatus of claim 114 wherein each of most of the large-footprint switches is positioned on one surface in a location substantially overlapping a location on the other surface occupied by another large-footprint switch.

117. (Original) The apparatus of claim 110 wherein the PCB includes a top surface and a bottom surface, the semiconductors include large-footprint switches mounted on the top surface, most of the large-footprint components are distributed symmetrically between a left side of the top surface and an opposite right side of the top surface.

118. (Original) The apparatus of claim 110 wherein the PCB includes a top surface and a bottom surface, the semiconductors include large-footprint switches mounted on the top surface, and most of the large-footprint components are distributed symmetrically between quadrants on the top surface.

119. (Original) The apparatus of claim 118 wherein the components further comprise a transformer core, and the quadrants surround the transformer core.

120. (Original) The apparatus of claim 110 wherein the PCB includes a top surface and a bottom surface, the components include a set of high-profile components having similar heights, a number, T, of the high-profile components are mounted on the top surface, a number, B, of the high-profile components are mounted on the bottom surface, and the number T is approximately equal to the number B.

121. (Original) The apparatus of claim 120 wherein a spatial distribution of the high-profile components on the top surface roughly matches a spatial distribution of the high-profile components on the bottom surface.

122. (Original) The apparatus of claim 110 further comprising:

an adapter for providing mechanical and electrical connections between the modular package and an external mounting surface, the adapter having a body and a plurality of electrical terminals supported by the body; and

electrical connections formed between the adapter terminals and respective interconnects on the modular package,

the adapter body being mechanically secured to the modular package;

the adapter terminals being arranged to mate with the external mounting surface.

123. (Original) The apparatus of claim 122 wherein the external mounting surface is a circuit board and the terminals comprise ends constructed and arranged to be inserted into conductive holes in the circuit board.

124. (Original) The apparatus of claim 122 wherein the external mounting surface is a circuit board and the terminals comprise ends constructed and arranged to be surface mount soldered to the circuit board.

125. (Original) The apparatus of claim 122 wherein the external mounting surface includes a connector and the terminals comprise ends constructed and arranged to mate with the connector.

126. (Original) The apparatus of claim 122 wherein the interconnects are disposed along a long edge of the modular package, the adapter is secured to the long edge of the modular package, and the first and second layers of the modular package are oriented perpendicular to the mounting surface.

127. (Original) The apparatus of claim 122 wherein the interconnects are disposed along opposite edges of the modular package, the adapter is secured to the opposite edges, and the first and second layers of the modular package are oriented essentially parallel to the mounting surface.

128. (Original) The apparatus of claim 127 wherein the adapter is constructed and arranged to maintain one of the first or second layers in contact with the mounting surface.

129. (Original) The apparatus of claim 110 wherein the interconnects further comprise a surface constructed and arranged for engagement with a connector terminal.

130. (Original) The apparatus of claim 110 wherein the interconnects further comprise a layer of metal plating.

131. (Original) The apparatus of claim 110 wherein the first layer further comprises contours formed in an interior surface of the first layer, the contours including a first feature having a shape and an elevation to accommodate a first component on the PCB, the first component having a height greater than or less than other components on the PCB.

132. (Original) The apparatus of claim 131 wherein the first component includes a magnetic core structure and the elevation is a recess in the interior surface.

133. (Original) The apparatus of claim 131 wherein the first component includes a semiconductor switch and the elevation is a protrusion from the interior surface.

134. (Original) The apparatus of claim 110 further comprising interlocking features comprising a contour formed in an interior surface of the first layer, the contour being filled with cured mold compound.

135. (Original) The apparatus of claim 110 wherein the modular package further comprises a recess formed in the first layer adjacent one or more of the interconnects providing a setback between the first layer and the one or more interconnects.

136. (Original) An apparatus comprising:

a power converter including

a printed circuit board ("PCB") comprising a plurality of conductive layers and having a top surface and a bottom surface;

a magnetic core structure magnetically coupled to a winding formed by traces in one or more of the conductive layers in the PCB; and

a plurality of power semiconductor devices, a first set of the power semiconductor devices being mounted on the top surface and electrically connected to dissipate power at a level, Pt, during operation of the converter, a second set of the power semiconductor devices being mounted on the bottom surface and electrically connected to dissipate power at a level, Pb, during operation of the converter;

wherein the power semiconductor devices are distributed between the first and second sets to distribute heat generation during operation of the converter such that each level Pt, Pb is less than 150% of the other level Pb, Pt.

137. (Original) The apparatus of claim 136 wherein a plurality of the power semiconductor devices in the first set are each positioned in a location on the top surface substantially overlapping a location on the bottom surface occupied by a power semiconductor device in the second set.

138. (Original) The apparatus of claim 136 wherein the power semiconductor devices are electrically connected using a respective set of conductive vias in the PCB, and a plurality of the power semiconductor devices in the first set share their respective sets of conductive vias with corresponding power semiconductor devices in the second set.

139. (Original) The apparatus of claim 137 wherein the power converter further comprises circuitry including a pair of cells having a common circuit topology and each including power semiconductor switches from each of the first and second sets; each cell having its respective components arranged in a pattern, wherein the pattern of components of one cell is substantially a mirror image of the pattern of components in the other cell.

140. (Original) The apparatus of claim 139 wherein a component from one of the cells is located on an opposite surface of a respective component from the other one of the cells.

141. (Original) The apparatus of claim 140 wherein the cells comprise input cells.

142. (Original) The apparatus of claim 138 wherein the power semiconductor devices comprise output switches.

143. – 145. (Cancelled).

REMARKS

The Applicant asks that all claims be examined in view of the amendments to the claims.

Please apply any other necessary charges or credits to Deposit Account 06-1050, referencing the above attorney docket number.

Respectfully submitted,

Date: March 2, 2015

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PANEL-MOLDED ELECTRONIC ASSEMBLIES

FIELD OF THE INVENTION

[001] This invention relates to the field of encapsulating electronic assemblies and more particularly to encapsulated power converters.

BACKGROUND

[002] Contemporary electronic power systems require power converters capable of deployment at the point of load. Competing considerations require increasing power density, decreasing mounting area on customer motherboard, and lower cost.

[003] An encapsulated electronic module, such as an electronic power converter module for example, may comprise a printed circuit assembly over-molded with an encapsulant to form some or all of the package and exterior structure or surfaces of the module. Encapsulation in this manner may aid in conducting heat out of the over-molded components, i.e., components that are mounted on the printed circuit assembly and covered with encapsulant. In the case of an electronic power converter module, the printed circuit assembly may include one or more inductive components, such as inductors and transformers. Encapsulated electronic power converters capable of being surface mount soldered to a customer motherboard are described in Vinciarelli et al., *Power Converter Package and Thermal Management*, U.S. Patent No. 7,361,844, issued Apr. 22, 2008, (the "SAC Package Patent") (assigned to VLT, inc. of Sunnyvale, CA, the entire disclosure of which is incorporated herein by reference). Encapsulated electronic modules having at least one surface of a magnetic core structure exposed and methods for manufacturing the same are described in Vinciarelli et al., *Encapsulation Method and Apparatus for Electronic Modules*, U.S. Patent Application Ser. No.12/493,773, filed Jun. 29, 2009, (the "Exposed Core Application") (assigned to VI Chip Inc. of Andover, MA, the entire disclosure of which is incorporated herein by reference).

[004] Methods of over-molding both sides of a printed circuit board assembly while leaving opposing regions on both sides of the printed circuit board free of encapsulant are

described in Saxelby, et al., *Circuit Encapsulation Process,* U.S. Patent No. 5,728,600, issued Mar. 17, 1998 and Saxelby, et al., *Circuit Encapsulation*, U.S. Pat. No. 6,403,009, issued June 11, 2002 (collectively the "Molding Patents") (both assigned to VLT, Inc. of Sunnyvale, CA and incorporated by reference in their entirety).

[005] Leads for connecting the encapsulated power converter substrate to the customer motherboard are described in Vinciarelli et al., *Surface Mounting A Power Converter*, U.S. Patent No. 6,940,013, issued Sep. 6, 2005 (the "J-Lead Patent") (assigned to VLT, Inc. of Sunnyvale, CA, the entire disclosure of which is incorporated herein by reference).

SUMMARY

[006] In general, in one aspect, a method of making a plurality of electronic devices is provided. The method includes providing a plurality of mold panels, which when assembled, form an internal chamber; providing a substrate having a plurality of conductive traces and a plurality of components electrically connected to form at least one circuit, the substrate having at least one contact for making an electrical connection to the circuit; forming a panel assembly including the mold panels assembled with the substrate in the internal chamber and an encapsulant filling spaces between the substrate and interior surfaces of the chamber; curing the encapsulant; and cutting the panel assembly to expose at least a portion of the at least one contact and form a respective exposed contact.

[007] Implementations of the method may include one or more of the following features. The cutting can include making a first cut in at least one of the mold panels, and in the first cut, making a second narrower cut through the panel assembly. The curing can include raising the temperature of the panel assembly and the first cut is made before the panel assembly cools after the curing. The cutting can divide the panel assembly producing at least one module having a plurality of layers including respective portions of each of the panel molds, the substrate, and the encapsulant, and the module can contain the at least one circuit. The cutting can define at least one side of the module. The

cutting can defines two or more sides of the module. The method can further include treating the exposed contact to protect against oxidation. Treating the exposed contact can include applying a removable conformal coating to the exposed contact. Treating the exposed contact can include applying a layer of metal to the exposed contact. The metal applied to the exposed contact can include solder or a precious metal. Applying a layer of metal can include plating. The method can further include providing an adapter having at least one electrical terminal; and attaching the at least one electrical terminal to the exposed contact. The at least one contact can include a plurality of contacts; the module can include a plurality of exposed contacts; the adapter can have a plurality of electrical terminals arranged to match respective ones of the plurality of exposed contacts; and the adapter can be mechanically secured to the module. The mold panels can be metal. The respective portions of the mold panels can provide heat sink surfaces for the module. Contours can be provided in an internal surface of one or more of the mold panels. Providing the contours can include matching depths of portions of the internal surface to heights of one or more selected components. The selected components can include at least one magnetically permeable core and at least one semiconductor device. The traces and components can be electrically connected to form a plurality of separable circuits arranged in a pattern on the substrate; and the cutting can divide the panel assembly along spaces between the separable circuits into a plurality of modules each containing at least one respective circuit. The spaces between the separable circuits can have dimensions approximately matching a width of cuts produced by equipment used to cut the panel assembly. The at least one contact can include a plurality of contacts located in the spaces between the separable circuits. The plurality of contacts can be formed in the substrate. The plurality of contacts can be formed and buried below at least one surface of the substrate. The method can include treating at least one exterior surface of at least one of the mold panels for solderability. Forming the panel assembly can include dispensing encapsulant into a bottom panel mold; assembling the substrate into the bottom panel mold; dispensing encapsulant onto a top of the substrate; and assembling a top panel mold onto the substrate. The method can include centrifuging the assembly before curing the encapsulant. Forming the panel assembly can include assembling the substrate with a first substrate surface facing into a first panel mold, closing a second

panel mold onto the substrate covering a second substrate surface, providing one or more conduits to the internal chamber, and forcing encapsulant through the one or more conduits into the chamber. The method can further include centrifuging the assembly before curing the encapsulant. The method can further include providing a connector for removably mating with and providing electrical connection to the metal. The method can further include providing a center plate having an opening to accommodate the substrate. Forming a panel assembly can include positioning the substrate in the opening of the center plate and closing the mold panels against the center plate. The method can further include providing at least one opening in the center plate connected to the internal chamber by at least one conduit; and forcing the encapsulant through the at least one opening and at least one conduit into the internal chamber. Forming a panel assembly can include securing the mold panels together prior to curing the encapsulant.

[008] In general, in another aspect, a method of forming an electrical contact is provided. The method includes assembling a panel including a substrate having one or more conductive features enclosed within the panel and unexposed to an exterior surface of the panel, the one or more conductive features being located along a cut line; cutting the panel along the cut line exposing portions of the one or more conductive features for use as electrical connections to the substrate; and treating the portions of the one or more conductive features exposed from the cutting for preservation as electrical connections.

[009] Implementations of the method may include one or more of the following features. The treating can include applying solder to the portions of the one or more conductive features exposed from the cutting. The treating can include applying a conformal coating to the portions of the one or more conductive features exposed from the cutting to protect against oxidation. The treating can include applying a metal layer to the portions of the one or more conductive features exposed from the cutting. The treating can include soldering a lead of an adapter to the portions of the one or more conductive features exposed from the cutting. The method can further include covering at least one surface of the substrate in an area including the cut line and the conductive features prior to cutting the substrate. The covering can include encapsulating the substrate with a molding compound. The method can further include providing a

registration feature having a predetermined relationship to the substrate, and using the registration feature to align the cutting relative to the cut line. The method can further include establishing a pattern including at least one conductive layer in the substrate along the cut line to form the conductive features. The substrate can include a multilayer printed circuit board, and the pattern can include a plurality of conductive layers that are established along the cut line to form the conductive features. The method can further include establishing a pattern including at least one conductive via in the substrate along the cut line to form the conductive features. The conductive via can be filled with a conductive material. The conductive via can be buried in the substrate. The conductive via can be a through hole contacting the surfaces of the substrate. The through hole can be filled with a conductive material. The conductive features can be covered at the surfaces of the substrate by an insulative layer.

[010] In general, in another aspect, an apparatus including a first mold panel is provided. The first mold panel includes an exterior surface, an interior surface defining an internal cavity, a clamp region located at points along a circumference of the internal cavity, and an opening. The first mold panel is adapted to (a) be engaged by pressure in the clamp region, (b) receive in the cavity a circuit panel containing a plurality of components and mold compound to fill empty spaces in the internal cavity, and (c) be cut after curing of the mold compound.

[011] Implementations of the apparatus may include one or more of the following features. The interior surface in the region of the internal cavity can be adapted to adhere to the mold compound. The apparatus can further include a second mold panel. The second mold panel can include an exterior surface, an interior surface, and a clamp region, in which the second mold panel can be adapted to (a) close against and mate with the first mold panel, (b) be engaged by pressure in the clamp region, and (c) be cut after curing of the mold compound. The interior surface of the second mold can further define a second internal cavity, the clamp region of the second mold panel can be located at points along a circumference of the second internal cavity, and the internal cavity of the first mold panel can be adapted to receive a first side of the circuit panel and the second internal cavity can be adapted to receive a second opposite side of the circuit panel. The

apparatus can further include contours formed in the interior surface of at least one of the mold panels. The contours can be adapted to match predetermined characteristics of selected ones of the plurality of components. The internal surface of the mold panel can be adapted to adhere to the molding compound. The contours can form interlocking features with cured mold compound. One or more of the mold panels can include a non-ferrous metal, aluminum, or a thermally conductive material. One or more of the mold panels can include a non-metallic substance. The apparatus can further include at least one channel connected to the internal cavity for allowing expansion of the mold compound. The apparatus can further include at least one channel connected to the internal cavity for injecting mold compound into the internal cavity. The exterior surface of the mold panel can include a plurality of fins. The exterior surface of the mold panel can include a flat surface. The flat surface can be adapted for a solder joint. The internal cavity can include features formed in the interior surface and arranged in a predetermined pattern. The internal cavity can include features formed in the interior surface along lines through which the mold panel maybe cut to establish a setback from a cut edge of the mold panel. The mold panel can include at least one registration feature adapted to engage and establish a predetermined relationship with the circuit panel. One or more selected portions of the mold panel can be adapted for incorporation into one or more products, the products being formed by a process which uses the mold panel to contain the molding compound. The exterior surface of the mold panel can include a flat surface with one or more pins protruding from the flat surface. The exterior surface of the mold panel can include a flat surface having one or more holes in the flat surface. The apparatus can further include a pin inserted into a respective one of the one or more holes.

[012] In general, in another aspect, an apparatus including a panel assembly having external surfaces defined by a first mold panel and a second mold panel is provided. The first and second mold panels form an internal cavity enclosing an internal circuit board, the internal circuit board having a first surface and second surface and a plurality of components in an active circuit area on at least one of the surfaces, the components being electrically connected to interconnects contained within the internal cavity. The internal cavity is filled with mold compound in spaces unoccupied by the

circuit board and components, and the panel assembly is adapted to have first selected portions of the first and second mold panels cut away to expose the interconnects and to have second selected portions of the respective mold panels situated near the active circuit area remain attached to the assembly following the cut.

[013] Implementations of the apparatus may include one or more of the following features. The panel assembly can include a clamp region located at points along a circumference of the first and second internal cavities, and the first selected portions can include the clamp region.

[014] In general, in another aspect, an apparatus including a panel assembly having external surfaces defined by a first mold panel and a second mold panel is provided. The first and second mold panels form an internal cavity enclosing an internal circuit board, the internal circuit board having a first surface and second surface and a plurality of components electrically connected to form a plurality of individual circuits, each individual circuit being electrically connected to respective interconnects located along a respective circuit perimeter, the interconnects being contained within the cavity.

[015] Implementations of the apparatus may include one or more of the following features. The panel assembly can be adapted to be cut along the circuit perimeter separating the individual circuits, dividing the panel assembly into individual circuit modules, and exposing selected portions of the interconnects. The panel assembly can be constructed to retain an integral layered structure after being filled with mold compound which is subsequently cured, the layered structure comprising a first layer including a portion of the first mold, a second layer including a portion of the mold compound, a third layer including a portion of the circuit board, a fourth layer including a portion of the mold compound, and a fifth layer including a portion of the second mold. The internal circuit board can include a plurality of circuits having the same functionality. The apparatus can further include one or more conduits connecting the internal cavity to an external opening. Spaces unoccupied by the circuit board, components, and interconnects in the internal cavity can be filled with mold compound. The mold

compound has been cured. Selected portions of at least one of the mold panels have been removed, the selected portions being located near the circuit perimeters.

[016] In general, in another aspect, an apparatus including a modular package is provided. The modular package has a first external surface, a second external surface opposite the first external surface, and a side wall extending along the perimeter of and connecting with the first and second external surfaces. The modular package includes a first layer defining the first external surface and a second layer defining the second external surface, the first and second layers being separated by and in contact with cured mold compound. An electrical circuit is located between the first and second layers and within the cured mold compound and including at least one electrical component electrically connected to a plurality of interconnects. The side wall includes a strip formed by the first layer, a strip formed by the second layer, and a strip formed by the cured mold compound. The interconnects are disposed within the side wall.

[017] Implementations of the apparatus may include one or more of the following features. The first and second layers can include a non-ferrous metal or aluminum. The first external surface can include a plurality of fins. The first external surface can include an essentially flat area. The essentially flat area can be adapted for a solder joint. The electrical circuit can include a circuit board, and the side wall can include a strip formed by the circuit board and an additional strip formed by cured mold compound. The interconnects can include conductive features in the circuit board. The circuit board can include a multilayer printed circuit board ("PCB") and each of the interconnects can include a plurality of conductive layers in the PCB. Each of the interconnects can include a plurality of conductive vias in the circuit board. The apparatus can further include interlocking features. The interlocking features can include a contour formed in an interior surface of the first layer, the contour being filled with cured mold compound. The circuit board can include a top surface and a bottom surface and the at least one electrical component can include a set of top-side components mounted on the top surface and a set of bottom-side components mounted on the bottom surface. The top-side components can include a number, T, of large-footprint components, the bottom-side components can include a number, B, of large-footprint components, and the number T

can be approximately equal to the number B. Each of most of the top-side large-footprint components can share a respective set of conductive vias with a corresponding one of the bottom-side large-footprint components. Each of most of the top-side large-footprint components is located in a respective footprint shared by a corresponding one of the bottom-side large-footprint components. The circuit board can include a top surface and a bottom surface, the at least one electrical component can include a number, T, of large-footprint components mounted on the top surface, and most of the large-footprint components can be distributed symmetrically in relation to an axis on the top surface. The axis can be along a midline of the top surface. The axis can be defined in relation to a predetermined component. The apparatus can further include an adapter for providing mechanical and electrical connections between the modular package and an external mounting surface, the adapter having a body and a plurality of electrical terminals supported by the body; and electrical connections formed between the adapter terminals and respective interconnects on the modular package. The adapter body can be mechanically secured to the modular package, and the adapter terminals can be arranged to mate with the external mounting surface. The external mounting surface can be a circuit board and the terminals can include ends constructed and arranged to be inserted into conductive holes in the circuit board. The external mounting surface can be a circuit board and the terminals can include ends constructed and arranged to be surface mount soldered to the circuit board. The external mounting surface can include a connector and the terminals can include ends constructed and arranged to mate with the connector. The interconnects can be disposed along a long edge of the modular package, the adapter can be secured to the long edge of the modular package, and the first and second layers of the modular package can be oriented perpendicular to the mounting surface. The interconnects can be disposed along opposite edges of the modular package, the adapter can be secured to the opposite edges, and the first and second layers of the modular package can be oriented essentially parallel to the mounting surface. The adapter can be constructed and arranged to maintain one of the first or second layers in contact with the mounting surface. The interconnects can include a surface constructed and arranged for engagement with a connector terminal. The interconnects can include a layer of metal plating.

[018] In general, in another aspect, an apparatus includes a modular package having a first external surface, a second external surface opposite the first external surface, and a side wall extending along the perimeter of and connecting with the first and second external surfaces, the modular package including a first layer of metal defining the first external surface and a second layer of metal defining the second external surface, the first and second layers being separated by and in contact with cured mold compound; and an electrical circuit for converting power, including a printed circuit board ("PCB"), a plurality of components including semiconductors mounted to the PCB, and a plurality of interconnects electrically connected to the components, the electrical circuit being located between the first and second layers and within the cured mold compound. The side wall includes a strip formed by the first layer, a strip formed by the second layer, a strip formed by the PCB, and one or more strips formed by the cured mold compound. The interconnects are disposed within the side wall.

[019] Implementations of the apparatus may include one or more of the following features. The first and second layers can include aluminum, and the first external surface can include a plurality of fins. The first and second layers can include aluminum, and the first external surface can include an essentially flat area. The essentially flat area can be adapted for a solder joint. The PCB can include a top surface and a bottom surface, the semiconductors can include large-footprint switches. A number, T, of top-side large-footprint switches can be mounted on the top surface, a number, B, of bottom-side large-footprint switches can be mounted on the bottom surface, and the number T can be approximately equal to the number B. Each large-footprint switch can be connected to one or more other components by a respective set of conductive vias in the PCB, and each of a plurality of the top-side large-footprint switches can share its respective set of conductive vias with a corresponding one of the bottom-side large-footprint switches. Most of the large-footprint switches can be positioned on one surface in a location substantially overlapping a location on the other surface occupied by another large-footprint switch. The apparatus of claim 151 wherein the PCB includes a top surface and a bottom surface, the semiconductors include large-footprint switches mounted on the top surface, most of the large-footprint components are distributed symmetrically between a left side of the top surface and an opposite right side of the top surface. The PCB can

include a top surface and a bottom surface, the semiconductors can include large-footprint switches mounted on the top surface, and most of the large-footprint components can be distributed symmetrically between quadrants on the top surface. The components can include a transformer core. The quadrants can surround the transformer core. The PCB can include a top surface and a bottom surface, and the components can include a set of high-profile components having similar heights. A number, T, of the high-profile components can be mounted on the top surface, a number, B, of the high-profile components can be mounted on the bottom surface, and the number T can be approximately equal to the number B. A spatial distribution of the high-profile components on the top surface can roughly match a spatial distribution of the high-profile components on the bottom surface. The apparatus can further include an adapter for providing mechanical and electrical connections between the modular package and an external mounting surface, the adapter having a body and a plurality of electrical terminals supported by the body; and electrical connections formed between the adapter terminals and respective interconnects on the modular package. The adapter body can be mechanically secured to the modular package, and the adapter terminals can be arranged to mate with the external mounting surface. The external mounting surface can be a circuit board and the terminals can include ends constructed and arranged to be inserted into conductive holes in the circuit board. The external mounting surface can be a circuit board and the terminals can include ends constructed and arranged to be surface mount soldered to the circuit board. The external mounting surface can include a connector and the terminals can include ends constructed and arranged to mate with the connector. The interconnects can be disposed along a long edge of the modular package, the adapter can be secured to the long edge of the modular package, and the first and second layers of the modular package can be oriented perpendicular to the mounting surface. The interconnects can be disposed along opposite edges of the modular package, the adapter can be secured to the opposite edges, and the first and second layers of the modular package can be oriented essentially parallel to the mounting surface. The adapter can be constructed and arranged to maintain one of the first or second layers in contact with the mounting surface. The interconnects can include a surface constructed and arranged for engagement with a connector terminal. The interconnects can include a layer of metal

plating. The first layer can include contours formed in an interior surface of the first layer, the contours including a first feature having a shape and an elevation to accommodate a first component on the PCB, the first component having a height greater than or less than other components on the PCB. The first component can include a magnetic core structure and the elevation can be a recess in the interior surface. The first component can include a semiconductor switch and the elevation can be a protrusion from the interior surface. The apparatus can further include interlocking features having a contour formed in an interior surface of the first layer, the contour being filled with cured mold compound. The modular package can include a recess formed in the first layer adjacent one or more of the interconnects providing a setback between the first layer and the one or more interconnects.

[020] In general, in another aspect, an apparatus includes a power converter is provided. The power converter includes a printed circuit board ("PCB") having a plurality of conductive layers and having a top surface and a bottom surface; a magnetic core structure magnetically coupled to a winding formed by traces in one or more of the conductive layers in the PCB; and a plurality of power semiconductor devices. A first set of the power semiconductor devices is mounted on the top surface and electrically connected to dissipate power at a level, Pt, during operation of the converter, and a second set of the power semiconductor devices is mounted on the bottom surface and electrically connected to dissipate power at a level, Pb, during operation of the converter. The power semiconductor devices are distributed between the first and second sets to distribute heat generation during operation of the converter such that each level Pt, Pb is less than 150% of the other level Pb, Pt.

[021] Implementations of the apparatus may include one or more of the following features. A plurality of the power semiconductor devices in the first set can each be positioned in a location on the top surface substantially overlapping a location on the bottom surface occupied by a power semiconductor device in the second set. The power semiconductor devices can be electrically connected using a respective set of conductive vias in the PCB, and a plurality of the power semiconductor devices in the first set can share their respective sets of conductive vias with corresponding power semiconductor

devices in the second set. The power converter can include circuitry having a pair of cells that have a common circuit topology and each including power semiconductor switches from each of the first and second sets. Each cell can have its respective components arranged in a pattern, in which the pattern of components of one cell is substantially a mirror image of the pattern of components in the other cell. A component from one of the cells can be located on an opposite surface of a respective component from the other one of the cells. The cells can include input cells. The power semiconductor devices can include output switches.

[022] In general, in another aspect, a method of manufacturing a plurality of products is provided. The method includes inserting a plurality of components into a cavity formed by one or more molds; closing the one or more molds to form a seal around the cavity; filling the cavity with mold compound; curing the mold compound in the cavity to secure the components, cured mold compound, and molds together into an assembly; and cutting the assembly to separate the plurality of products from the assembly, the products each including a respective section of the one or more molds which remains as an integral part of each respective product.

[023] Implementations of the method may include one or more of the following features. The method can further include maintaining a predetermined alignment between the plurality of components and the one or more molds. The plurality of components can include a substrate having conductive features. The cutting can include exposing portions of the conductive features in each respective product.

[024] The details of one or more embodiments of the invention are set forth in the accompanying drawings and description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

[025] FIG. 1 shows an electronic module 100.

[026] FIG. 2 shows a panel assembly 120 comprising a plurality of electronic modules before singulation.

[027] FIG. 3 shows an exploded view of the panel assembly revealing the heat sink panels 121 and 122 and internal PCB panel 124.

[028] FIG. 4 shows the panel assembly 120 with the top heat sink panel 121 removed.

[029] FIG. 4A shows an exploded view of the PCB panel and lower heat sink panel in a modified panel assembly 120.

[030] FIG. 4B shows a cross-section of the panel assembly 120A along lines 4B-4B in Fig. 4A.

[031] FIG. 5 shows a plan view of the PCB panel 124 assembled with the bottom heat sink panel 122.

[032] FIG. 6 shows a cross-section of the panel assembly 120.

[033] FIG. 7 shows a partial cross section of the panel assembly closed in a mold.

[034] FIG. 8 shows another partial cross section of the panel assembly closed in a mold.

[035] FIG. 9A shows a plan view of the panel assembly 120 following singulation.

[036] FIGs. 9B, 9C show optional channels formed in the panel before singulation.

[037] FIGs. 10A, 10B show single modules 115, 115B after singulation.

[038] FIG. 11 shows an enlarged portion of the module 115 revealing details of exposed buried-embedded interconnects.

[039] FIG. 12 shows a cross section of the singulated module 115 of Fig. 10A.

[040] FIG. 13 shows a connector assembly.

[041] FIG. 14 shows an exploded view of the connector assembly.

[042] FIG. 15 shows a horizontal through-hole mount module 200.

[043] FIG. 16 shows an exploded view of the through-hole mount module 200.

[044] FIG. 17 shows a horizontal surface-mount module 300.

[045] FIG. 18 shows an exploded view of the surface-mount module 300.

[046] FIG. 19 shows an alternative horizontal surface-mount module 400.

[047] FIG. 20 shows a top view of the surface-mount module 400.

[048] FIG. 21 shows an exploded top view of module-connector set 500.

[049] FIG. 22 shows an exploded view of the connector set 503.

[050] FIG. 23 shows an exploded bottom view of module-connector set 500.

[051] FIG. 24 shows an isometric view of the module-connector set 500 assembled.

[052] FIG. 25 shows an alternative horizontal through-hole flush-mount module 600 exploded from a customer PCB.

[053] FIG. 25A shows an alternative horizontal through-hole flush-mount module 650 exploded from a customer PCB.

[054] FIG. 26 shows the horizontal through-hole flush-mount module 600 assembled onto a customer PCB.

[055] FIG. 27 shows top and bottom plan views of a section of a PCB illustrating symmetry of component layouts.

[056] FIG. 28 shows an exploded perspective view of a panel assembly 720 including a manifold plate.

[057] FIG. 29 is an exploded side view of the panel assembly 720 showing the PCB mated with the manifold plate.

[058] FIG. 30 shows a top plan view of the panel assembly 720.

[059] FIG. 31 shows a top plan view of the panel assembly 720 with the top heat sink panel removed.

[060] FIG. 32 shows a side view of the panel assembly 720 closed in a mold.

[061] Like references symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

I. Vertical PCB Package.

[062] Referring to Fig. 1, an electronic module 100, e.g. a power converter, is shown having a generally rectangular form factor with two large faces 114A, 114B covered by heat sinks 101, 102. As shown between the heat sinks 101 and 102, the module 100 includes a printed circuit board ("PCB") 104 having its large faces arranged generally coplanar to the two large faces 114A, 114B of the electronic module 100. Electronic components (Figs. 3, 5, 6) may be mounted to one or both sides of the PCB 104 and electrically interconnected, e.g. by conductive traces on or in the PCB 104 to form the module circuitry. Using a power converter as an example, the electronic components may include power transistors, control ICs, and discrete resistors and capacitors. One or

more magnetic core structures may be provided, which in combination with conductive traces on PCB 104, may form planar magnetic components such as inductors and transformers.

[063] The electronic components may protrude from one or both sides of the PCB 104 to varying degrees depending upon component size. Spaces between the faces of PCB 104 and the components on the PCB on one hand and the interior surfaces of the heat sinks on the other hand may be filled with molding compound, which when cured may form integral structural layers 105, 106 as shown in Fig. 1 and further provides a thermally conductive medium in which heat may be readily conducted away from the PCB and components to the heat sinks 101, 102. The interior surfaces of the heat sinks may be contoured to match the height of one or more of the components while maintaining an appropriate clearance for insulation and safety agency requirements. Contouring the heat sinks 101, 102 in this way: (1) to match the height of the magnetic core structure may be used as an alternate approach to the exposed core encapsulation method described in Vinciarelli, *Encapsulation Method and Apparatus for Electronic Modules*, U.S. Patent Application, Serial No. 12/493,773 filed June 29, 2009 (assigned to VI Chip Corp. of Andover, MA, the entire disclosure of which is incorporated herein by reference); (2) to match the height of lower profile components, such as power semiconductors, may (a) increase thermal performance in the case of heat dissipating components by replacing molding compound with heat sink metal; and (b) reduce cost generally by reducing the volume of molding compound required; and (c) further reduce cost by allowing less expensive molding compound to be used because of reduced thermal pathways through the encapsulant, easing the thermal conductivity requirements of the encapsulant (e.g., an encapsulant having a 1 degree Celsius per watt thermal resistance may be used with the contoured heat sink instead of an encapsulant having a 3 degrees Celsius per watt thermal resistance used without the contoured heat sink).

[064] A connector 103, including terminals 108, 109, 110 and standoffs 107, may be provided as shown along an edge of the PCB 104 to make electrical connections between the electronic module 100 and external circuitry. As shown in Fig. 1 with the connector 103 situated along one edge of the module 100, preferably one of the longest edges, the

module 100 may be mounted vertically, i.e. with its internal PCB 104 perpendicular to a chassis or another circuit board such as a motherboard. Using the vertical mount module construction illustrated in Fig. 1 for a power converter may provide advantages over the more conventional horizontal mounting technique. For example, using the vertical PCB arrangement may allow use of a magnetic core structure that is thicker than in a horizontal PCB configuration, e.g. because of height restrictions, enabling increased power throughput, as compared to a similar converter using a horizontal PCB orientation. The length of the magnetic path may be also reduced in the vertical PCB configuration further reducing losses in the magnetic components. Shorter windings may also be used further reducing transformer or inductor losses. Further details and variations of, and a process for making, the electronic module will be discussed below in connection with a panel molding process.

II. Panel Molding Process.

A. Overview

[065] The electronic module 100 shown in Fig. 1 may be fabricated using a panel molding process described with reference to Figs. 2- 9. The panel molding process may be used to produce a multiplicity of modules at a time. A PCB panel 124 may be provided with a plurality of individual circuits for building the electronic modules. Figs. 3, 4, and 5 show the PCB panel 124 populated with electronic components revealing a 3-by-4 pattern of twelve circuits to make twelve individual modules 115 (labeled 115A through 115L in Fig. 5). The illustrative example of Figs. 3-5, being for power converters, includes magnetic core structures 131 (Fig. 3) in addition to electronic components 132. As shown in Fig. 5, the pattern of individual circuits 115A-115L are arranged close together and separated by small spaces 135 preferably sufficient to allow the PCB panel to be cut during the singulation process without necessitating two cuts between modules or unnecessary waste of PCB material. The spacing may be adjusted based upon the cut dimensions produced by the equipment used to make the cuts.

[066] The PCB panel 124 containing the multiplicity of the electronic circuits (115A-115L in Fig. 5) may be assembled with matching heat sink panels 121, 122 as shown in

Fig. 3 to form a panel assembly 120 (Fig. 2). As shown in Figs. 3 and 6, the two heat sink panels 121 and 122 when assembled together may form an internal cavity 146, which completely encloses the populated PCB panel 124. Figs. 2 and 6 show that the heat sink panels 121 and 122 may be pressed together (e.g. by a mold press 161, 162 as shown in Fig. 7) to form a seal 123 (Figs. 2, 6-8) around the perimeter of the internal cavity 146. In this example, the heat sink panels 121 and 122 also function as mold panels by forming a mold cavity (e.g., the internal cavity 146) that may be filled at least in part by an encapsulant encapsulating the surfaces of the PCB panel 124 and the electronic components on the PCB panel 124.

B. Heat Sink Panels

[067] Referring to Fig. 2, the heat sink panels 121, 122 may include fins on the exterior surfaces as shown. The fins may be arranged in any direction relative to the panel or in any pattern and may vary in height, thickness, and spacing as required for the particular application. For example, modules 115 and 115B shown in Figs. 10A and 10B respectively illustrate longitudinal and transverse fin orientations. Alternatively, one or both of the heat sink panels may have a generally flat exterior surface omitting the fins altogether. For example, Figs. 17 and 25 show modules 315 and 615 produced when both heat sink panel exterior surfaces are flat and one is flat and one is finned, respectively. The thickness of the panels between the internal cavity and the external surface may be varied to suit the particular requirements of the application.

C. Heat Sink Internal Contours

[068] Referring to Fig. 3, the contoured interior surface of the bottom heat sink panel 122 is shown including a 3-by-4 repeating pattern of twelve (A through L) prominent recesses 141 and shallower recesses 142 and 143. Recesses 141 may be matched to the downward protruding portion of magnetic core structures 131. Similarly, recesses 142 and 143 may be matched to other downwardly protruding components on the PCB panel 124. Note that in the example of Fig. 3, because the core structure 131 protrudes from the PCB 124 more than the other components, the recesses 141 are deeper than recesses 142, 143. Although not visible in Fig. 3, the interior surface of heat sink panel 121 may

similarly include contour features to match the components and core structure on the upward facing side of the PCB panel 124 (e.g. as shown in the cross-section of Figs. 6, 7). Although the interior contour of panel 122 in Fig. 3 is shown including three recesses 141, 142, 143 repeated for each circuit (A through L in the 3-by-4 pattern), the interior contours of the heat sink panels 121 and 122 may range from simple flat surfaces (accommodating the height of the tallest component) to a complex arrangement of a multiplicity of recessed and protruding features (accommodating a multiplicity of component heights) which at the extreme could match every component individually.

[069] Additional features may be provided in the heat sink panels to facilitate the panel molding process, to enhance the mechanical integrity or performance of the finished module 100, or to satisfy safety agency clearance requirements for the finished product. By way of example undercut features, such as undercuts 148 shown in Figs. 6, 7, and 12 may be provided at each circuit site (i.e. within each individual module location) in the heat sink panels 121, 122. As shown the undercuts 148 may be provided in selected recesses, such as recesses 143-1 and 143-2, and may be dispersed along one or more of the boundary lines of each circuit 115. During encapsulation, molding compound fills the recesses and trenches and their respective undercuts 148. When cured, the hardened molding compound in the undercuts forms a dovetail-like joint securing the heat sinks to the encapsulated PCB 124. When provided at each circuit site, the undercuts secure the heat sinks 101, 102 to the PCB 104 in the individual module 115 providing mechanical integrity after singulation. Referring to the cross-section of a singulated module 115 in Fig. 12, dovetail interfaces 149-2 and 149-1 are shown securing the top and bottom heat sinks 101, 102 to the encapsulated PCB assembly.

[070] Additionally, clearance features may be provided in the heat sink panels to satisfy minimum safety agency clearances between electrical contacts on the PCB 124 and the metal heat sinks 121, 122. As shown in Figs. 6 and 7, trenches 147 may be provided in heat sink panels 121 and 122 along the side of each module 115 (the long side as shown in Figs. 6 and 7) where electrical contacts (discussed in more detail below) are exposed in or on the PCB 124. The trenches 147 may also include the undercut

features 148 discussed above. For example, cut trench 147 in Fig. 12 results in a recess 150 of the heat sink 101 away from the edge 104E of the PCB 104 after singulation.

D. PCB-Heat Sink Registration

[071] Registration features may be provided in one or both of the heat sink panels 121, 122 helping to correctly position the PCB panel 124 in the cavity 146 relative to the heat sink panels 121, 122 (which is particularly important when the panel is cut during the singulation process) and to correctly position the heat sink panels relative to each other during assembly and during subsequent molding processes. Referring to Figs. 3 and 4, beveled corners 144 may be provided in heat sink panel 122 to interface with matching indentations 133 which may be provided in PCB panel 124 for registration when assembled together (Figs. 4 and 5). Fig. 5, which is a top plan view of the PCB panel 124 assembled with the bottom heat sink 122, shows the beveled corners 144 interfacing with the indentations 133.

[072] Referring to Fig. 4A, a modified version of the assembly is shown. As shown, a registration pin 151 is press fit into a registration hole 152 in the lower heat sink panel 122 and a matching registration hole 134 is provided in the PCB panel 124. The completed panel assembly, including the lower heat sink panel 122, PCB panel 124, and upper heat sink panel 121, is shown in Fig. 4B in cross-section taken along the broken lines 4B-4B in Fig. 4A. As shown in Fig. 4B, the registration pin 151, which fits snugly in registration holes 152 and 134, provides registration for the PCB panel 124 relative to the lower heat sink panel 122. An indentation 153 may be provided in the opposite heat sink panel (121) to accommodate protrusion of the pin 151 past the PCB 124. As shown generally at 154 in Fig. 4B, the heat sink panels may include additional features to provide registration between the top and bottom heat sink panels. Although a registration pin is shown at one corner of the panel 122 in Fig. 4A, it will be appreciated that additional pins may be used at other locations. For example, Fig. 4 shows two registration holes 134, one on a corner and another in the middle of the opposite side of the PCB panel 124.

E. Encapsulation

[073] Fig. 6 shows a cross-sectional view (through lines 6-6 in Fig. 5) of the panel 120 through an opening 125 and a conduit 145 in the heat sink panels. The openings 125, which may be slot shaped as shown (Figs. 2, 3, 4, 5, 9), may be connected to the interior cavity 146 of the panel assembly 120 by conduits 145 for conveying molding compound or venting during the panel molding process. The openings may be formed in one of the heat sink panels, e.g. openings 125 in the top heat sink panel 121 as shown in Figs. 2, 3, 4, 5, and 9, or in both heat sink panels, e.g. openings 125B in the top and bottom heat sink panels 121, 122 as shown in Figs. 6 and 7. Referring to Fig. 6, the conduits 145 may be formed by recesses in the interior surfaces of heat sink panels 121 and 122, connecting the openings 125 to the interior cavity 146. The recesses forming the conduit 145 may be situated near the edge 124C of PCB panel 124 to allow the molding compound to flow over both top 124A and bottom 124B surfaces of the PCB 124.

[074] Fig. 7 shows an enlarged cross-section of one end of the panel assembly 120 closed between an upper mold press 161 and lower mold press 162 taken through some of the smaller components, e.g. components 132-1, 132-2, i.e. through lines 6-6 in Fig. 5. A channel 163 may be provided, e.g. between the upper mold press 161 and lower mold press 162 as shown, to interface with openings 125. Molding compound may be forced through the channel 163 under pressure after the panel assembly 120 is closed in the mold presses 161, 162. The dashed line 167 with directional arrows in Figs. 7 and 8 illustrates the flow of molding compound through the channel 163 into openings 125 through conduits145 over the top 124A and bottom 124B surfaces of the PCB panel 124 during encapsulation. The molding compound may be forced into the internal cavity 146 to fill all of the unoccupied spaces between the heat sinks 121, 122 and the PCB panel 124.

[075] Fig. 8 shows an enlarged cross-section of one end of the panel assembly 120 closed between an upper mold press 161 and lower mold press 162 taken through the magnetic core structures, i.e. through lines 8-8 in Fig. 5. Each magnetic core 131 is shown having an upper E-core 131-2 and a lower E-core 131-1 separated by a gap 131-3.

The cores have openings 131-4 to accommodate windings formed on the PCB 124. As shown, the lower core 131-1 and upper core 131-2 are accommodated by recesses 141-1 and 141-2 in the lower heat sink 122 and upper heat sink 121, respectively. As shown, compliant pads 136 may be provided on the surfaces of the cores 131-1 and 131-2 or in recesses 141-1, 141-2 to accommodate dimensional differences in the components. The compliant pads may be chosen for good thermal conduction and optionally adhesive properties facilitating heat removal from the cores into the heat sink while optionally providing structural integrity to the assembly. Gap Pad A2000 available from the Bergquist Company, 18930 West 78th St, Chanhassen, Mn 55317 is one example of the type of compliant pad that may be used. Alternatively and perhaps depending upon the tolerances involved, a phase change material may accommodate the dimensional difference during assembly and when cured afterward provide structural integrity between the heat sinks and the cores.

[076] Molding compound may be deposited in one or more of the recesses, e.g. recesses 141-1 or 141-2, in the internal cavity prior to assembly of the PCB panel 124 into one or both of the heat sink panels 121, 122 to ensure that the molding compound fills narrow spaces between the heat sink and the components, e.g. the cores 131-1, 131-2. One or more vent openings (not shown) may be provided in the heat sink panels, preferably at an end opposite the fill openings 125, to allow the molding compound to flow completely through the internal cavity 146. The cavity may be filled with encapsulant either (1) by transfer through one or more conduits, (2) by measured deposition of encapsulant during assembly of the panels, or (3) by both measured deposition during assembly and transfer through conduits.

[077] As shown in Figs. 4, 5, and 6, the border areas between the modules and around the periphery of the PCB panel 124 may be minimized to avoid wasted PCB material. Because the heat sink panels 121 and 122 close against each other rather than the PCB panel 124, areas on the PCB normally reserved for closing the mold may be eliminated further reducing PCB waste and thus overall cost.

[078] After the panels are assembled together and the interior cavities are filled with molding compound, the panel assembly 120 may be cured, e.g. by elevating the temperature.

F. Singulation

[079] Singulation is the process by which individual modules, e.g. singulated module 115 in Fig. 10A, are separated from the panel assembly 120, e.g. by cutting. The panel assembly 120 may be singulated after the molding compound is cured. The panel assembly 120 is separated from the upper and lower mold presses 161, 162 and may be cut, e.g. along lines 128, 129 as shown in Fig. 9A, to singulate the modules 115A-115L. For example, a narrow saw may be used to cut through the layers (e.g. as shown in Figs. 1, 10A, 10B, 12) of panel 120, which may include heat sink 101, cured molding compound 105, PCB 104, cured molding compound 106, and heat sink panel 102. For example, a 0.025 inch thick saw such as model number EAD-3350 available from Disco Corp., Ota-ku, Tokyo, Japan may be used. Referring to the cross-sectional views of Figs. 6 and 7, dashed lines 129 illustrate the lines along which the panel 120 may be cut to singulate modules 115D, 115E, and 115F. As shown, the cuts 129 (along the long side of the individual modules 115) go through the middle of the trenches 147. The trenches 147 may be made wide enough and the cuts 129 may be made at an appropriate distance from the edges of the trench 147 to ensure that a minimum thickness of cured molding compound remains in the trench after singulation to be mechanically robust. The trenches 147 may also be used to reduce the thickness of metal through which the saw must cut during singulation, e.g. by optionally providing trenches along the perimeter of each module.

G. Electrical Connections

[080] Interconnection features may be embedded in the PCB panel 124, preferably along the boundaries of the individual circuits, so that electrical contacts are at least in part formed by or exposed during singulation. To maximize the area on a PCB panel 124 available for circuitry, the interconnection features may preferably be buried in the PCB panel 124 below the top and bottom surface layers. For example, the interconnection

features may be formed in the inner conductive layers but not occupying valuable area on the surface conductive layers, potentially reducing setback and other spacing requirements. The interconnect features therefore are preferably formed in the PCB panel 124 before the panel 120 is assembled and exposed when the panels are cut, e.g. during singulation. The interconnection features may comprise a pattern of conductive layers or buried vias (frequently used to form connections between internal conductive layers) or both in the PCB situated along the circuit boundary, i.e. lying in the cut line, e.g. cut line 129 (Fig. 9A).

[081] Referring to Fig. 10A, a module 115 is shown after singulation. Exposed interconnects 111, 112, and 113 are shown embedded in the edge of the PCB 104 along one of the edges 116 of the module 115. As shown in Fig. 10A, longer connections 111 and 113 provide greater interconnect surface area and higher current carrying capacity, making them amenable for use as power connections, than shorter connections 112 which have less interconnect area and lower current carrying capacity, making them useful for control signal connections. Fig. 11 shows an enlarged view of a portion of the module 115 along edge 116 revealing detail of the two interconnections 111 after singulation. The width along the boundary and number of the conductive features arranged vertically through the PCB layers may be adjusted to provide the requisite contact area for each connection. In the example of Fig. 11, conductive features, e.g. conductive lands 111A through 111L, formed along the cut line on a plurality of the conductive layers of the PCB form a stack of conductive strips resembling a bar code after singulation. The stack of conductive lands may provide more contact area than possible with a single buried via. In Fig. 11, each interconnect 111 is made up of twelve lands, each land being formed on a respective one of twelve inner conductive layers. Note that Fig. 11 shows the twelve lands (111A through 111L) buried below the top 124A and bottom 124B surfaces of the PCB, i.e. not occupying surface area on those layers. During singulation, the saw cuts through the buried embedded lands, exposing the edges of the remaining conductive material forming the interconnects 111A through 111L shown in Fig. 11. Note that the buried embedded lands may be shared between two adjacent modules 115 on the panel 120, e.g. where the PCB patterns are laid out in mirror image to each other, allowing the modules to be laid out on the PCB panel close to a singulation cut width apart. Also, the

interconnect features may be aligned along a single module boundary as shown or may occupy two or more boundaries of each individual module in the panel. The exposed edges may then be used to form electrical connections immediately after singulation, i.e. before the cut interconnects oxidize or may be protected against oxidation, e.g. with a conformal coating, such as an organic solderability preservative ("OSP"), applied after singulation, to ensure subsequent ability to form electrical connections to the edges. For example, Entek Plus HT available from Enthone, Inc., a Division of Cookson Electronics, West Haven , CT 06516 may be used as an OSP to protect the interconnects.

[082] The number of lands, i.e. conductive layers, used to form each interconnect may be increased for better electrical connections or reduced for less critical connections. Although embedded conductive lands are shown in the example of Figs. 10A, 11, additional or alternative conductive features may be used to form the interconnects. For example, buried conductive vias located along the cut line may be used, either alone or in combination with the lands. The buried vias may be located so that the singulation cut leaves the walls of the conductive vias exposed resulting in vertical conductive strips, i.e. generally perpendicular to the PCB top and bottom surfaces 124A, 124B, in the PCB edge. Buried conductive vias may tend to fill with adhesive during fabrication of the PCB panel 124. Empty conductive vias, i.e. free of non-conductive adhesives, may be preferable for the resulting concave conductive features, i.e. embedded conductive half cylinders. Similarly, solid buried conductive vias or conductive vias filled with conductive material during the PCB manufacturing process may be preferable for the resulting continuous flat conductive surface.

[083] In the alternative to buried conductive features, conductive through-holes, which are generally free of adhesives following fabrication of the PCB panel 124 may be used along the cut line to form interconnects extending through the thickness of the PCB from top surface to bottom surface providing generally half-cylindrical interconnects. A penalty of using through-holes for the interconnects is the loss of surface area on the top and bottom of the PCB which may otherwise be used for setback or other safety and agency approval requirements. Preferably, the through-holes may be filled, for example with a conductive material such as solder or silver paste, or conductive pins may be

inserted into through holes and soldered to the through holes, to prevent molding compound from filling the through hole during the encapsulation process and to provide a greater contact surface area yielding generally flat conductive interconnects following singulation.

[084] The exposed interconnect features, e.g. 111A through 111L may be used to make a variety of electrical connections. For example, the exposed interconnects may be solder plated and then subsequently soldered to a motherboard, e.g. using surface mount soldering techniques. The interconnects may be soldered to a connector, such as connector 103 shown in Figs. 1, 13, 14. Alternatively, a lead frame or PCB may be soldered to the exposed interconnects 111, 112, 113 of the module quickly after singulation. Yet another alternative includes a precious metal such as gold or silver or other suitable conductive material deposited to the exposed contacts, e.g. by plating, to build up the contacts into a larger area, e.g. continuous conductive contacts, well suited to connectorized modules described in more detail below.

G1. Vertical Mount Connector

[085] Referring to Figs. 1, 13 and 14, a connector 103 suitable for attachment to the edge 116 of the module 115 is shown having a connector body 118 with a plurality of recesses 117 and a plurality of holes 119A, 119B, and 119C. A plurality of connector pins 108, 109, 110 may be inserted into holes 119A, 119B, 119C, respectively, from the top 118A. As shown, the holes may be contoured to provide a pressure fit having a gripping force suitable for retaining the pins. The broad top surfaces 108A, 109A, 110A of the pins are suitable for making solder connections to the exposed interconnects 111, 113, 112, respectively on the edge 116 of the PCB 104 of module 115. As shown, the recesses 117 provide countersinking for the top portions of the pins allowing the connector body to mount flush to the edge 116 of module 115 and allowing space for a solder joint between the pin and the respective interconnect. The interconnection features may preferably be provided along a long edge of the module 115 yielding a more stable vertical mount module 100 such as shown in Fig. 1. However, the interconnection

features may be deployed along any or all of the edges of the module 115 for different mounting configurations as discussed more fully below.

G2. Horizontal Through-Hole Mount

[086] Referring to Figs. 15 and 16, a horizontal mount component 200 suitable for through hole mounting in a motherboard is shown including a singulated module 215 and through-hole adapters 203A, 203B. The horizontal mount module 200 may be constructed in the same manner as described above for the module 100, except that the interconnects are preferably disposed along two edges of the module PCB and connectors adapted for horizontal mounting may be used. As shown in Fig. 16, the interconnects are disposed along the two shorter edges of the PCB 204 in module 215. However, the longer edges may be used instead of, or in addition to, the shorter edges for the interconnects. Although only one set of the interconnects 211, 212 is visible in the perspective view of Fig. 16, it will be understood that a second set, including two additional power interconnects, is disposed along the opposite hidden edge of the PCB.

[087] Through-hole adapters 203A and 203B, suitable for attachment to the edges of the singulated module 215 are shown having adapter bodies 218 supporting conductive terminals 208, 210 and 209, respectively. A portion of each terminal may be exposed on an internal surface via an opening in the adapter body optionally providing a small recess. In Fig. 16 for example, adapter 203B is shown having two power terminals 209, each having an exposed areas 209A recessed in openings in surface 218A of the adapter body 218. The exposed areas 209A align with their respective interconnects when the adapters 203A, 203B are assembled onto the module 215. The recesses provide countersinking for the exposed terminals allowing the internal surface 218A of the adapter body 218 to mount flush to the edge of module 215 and allowing space for a solder joint between the terminal and the respective interconnect. The adapter body 218 may include a flange 218B which may form a pressure fit with the adjacent edges of the modules 25. Additional features may be provided for maintaining the structural integrity of the module and connectors.

[088] As shown in Fig. 16, epoxy may be deposited along an internal edge of the connector body, e.g. in the shaded area 219 preferably aligned with the encapsulant layer 206 to secure the adapters 203A, 203B to the module 215. The horizontal mount module 200 may be readily adapted to match industry standard brick footprints for power converters, in particular the module 200 may fit within the standard $1/8^{th}$ brick footprint.

G3. Horizontal Surface-Mount

[089] Referring to Figs. 17 and 18, a horizontal-mount component 300 suitable for surface-mount soldering to a motherboard is shown including a singulated module 315 and surface-mount adapters 303A and 303B. The horizontal-mount module 300 may be constructed in the same manner as described above for the module 200 (Figs. 15, 16) substituting surface mount adapters 303A, 303B for through-hole adapters 203A, 203B. As shown in Fig. 17, the singulated module 315 may have flat heat sinks 301, 302 instead of the finned heat sinks (shown in Figs. 1-4, 6-12, 15-16). Although shown disposed along the two shorter edges in Figs. 17 and 18, the interconnects may be deployed along the longer edges of the PCB 304 in the singulated module 315 instead of, or in addition to, the longer edges.

[090] In Figs. 17 and 18, the surface-mount adapters are shown with smaller bodies 318 than the through-hole adapters (218: Fig. 15, 16) exposing the connections between the terminals and their respective interconnects during assembly and for post assembly inspection. The terminals 308, 309, 310 each may include a portion, e.g. solder pads 308A, 310A, 309A, adapted for connection, such as a solder joint, to a respective interconnect on the module, e.g. interconnect 311, 312, and 313 (not visible in Figs. 17 and 18). Holes 308B, 309B, 310B may be provided in solder pads 308A, 309A, 310A for better solder joints. Each terminal 308, 309, 310 may include a bend (e.g. 308C) to produce a surface-mount pad (e.g. 308D) for attachment, e.g. by surface-mount soldering, to a customer motherboard.

[091] The adapter bodies 318 may include flanges 318B, preferably along two or more sides to form a pressure fit with the adjacent edges of the modules 315. Additional features may be provided for maintaining the structural integrity of the module and

adapters. As shown in Fig. 18, epoxy may be deposited along an internal edge of the connector body, e.g. in the shaded area 319 preferably aligned with the encapsulant layer 306 to secure the adapters 303A, 303B to the module 315.

G4. Surface-Mount Lead Frame

[092] An alternate embodiment of a horizontal-mount component 400 suitable for surface-mount soldering to a motherboard is shown in Figs. 19 and 20 including a singulated module 415. The horizontal-mount module 400 may be constructed in the same manner as described above for the module 300 (Figs. 17, 18) substituting lead frame adapter 403 for the surface-mount adapters 303A, 303B. Like module 315 (Fig. 17), the singulated module 415 may have flat heat sinks 301, 302 instead of the finned heat sinks of the previous examples. However, in the example of Figs. 19 and 20, the interconnects are shown deployed along the longer sides of the singulated module 415. However, as noted above the interconnects may be deployed along any edges of the PCB 404 as desired in the singulated module 415.

[093] The surface-mount adapter is shown in Figs. 19 and 20 having a unitary rectangular frame-like body 418 supporting a plurality of terminals 408. The profile of the frame body 418 may as shown leave a portion of the terminals exposed for making connections to their respective interconnects during assembly and for post assembly inspection. The terminals 408 each may include a portion, e.g. solder pad 408A, adapted for connection, such as a solder joint, to a respective interconnect on the module (not visible in Figs. 19, 20). Although shown without holes in Fig. 19, the solder pads may optionally include holes such as those shown in Figs. 17 and 18. Each terminal 408 may include a bend (e.g. 408C) to produce a surface-mount pad (e.g. 408D) for attachment, e.g. by surface-mount soldering, to a customer motherboard.

[094] The opening in the frame body 418 may be sized to accommodate the perimeter edges of the singulated module 415 and optionally form a pressure fit. The frame body 418 may include recesses 417 for accommodating the terminals 408, allowing the interior surface 418A of the frame body 418 to rest flush against the module 415 surface. Additional features may be provided for maintaining the structural integrity

of the module and adapters. Gaps may be provided in the interior surface 418A to allow the application of epoxy to secure the frame body 418 to the module 415.

G5. Connectorized Module

[095] The modules 100, 200, 300, and 400 discussed above in connection with Figs. 1, and 15-20 are all examples in which connectors or adapters are mechanically and electrically connected to the interconnects on the singulated modules forming an integral modular component. Yet another option is to adapt the module to be removably mated with a connector that may be mounted on a customer circuit board. For example, the module interconnects may be plated up with an appropriate conductive material, such as silver or gold, to form contacts that may be reliably engaged with connector contacts, i.e. "connectorized." Referring to Figs. 21 and 22, a module-connector set 500 is shown including a connectorized module 515 in exploded view with a mating connector 503 into which the module 515 may be removably inserted.

[096] The connector 503 as shown includes a body 518 having side walls 518B creating an opening 518C adapted to receive the connectorized module 515. Terminals 508 formed, e.g. bends 508B (Fig. 22), to provide a pressure fit between a contact area 508A of each terminal 508 and a respective interconnect 511. The terminals as shown may be retained in recesses 517 in the interior surface 518A of the side walls 518B. The recesses 517 may provide support to keep the terminals 508 in place and allow the interior surfaces to engage the surfaces of the module 515. The terminals 508 may include a flat portion 508D (Figs. 22, 23) adapted for making a solder connection to surface contacts on a customer circuit board (not shown). The connector body may include a bottom surface 518D enhancing the structural integrity of the connector walls 518B which are subjected to the forces exerted by the terminals 508 against the interconnects 511. The bottom 518D may include openings as shown in Fig. 23 through which the terminals may be inserted during assembly of the connector 503. The bottom 518D may provide electrical insulation between the metal heat sink 502 and the customer circuit board (not shown) on which the connector 503 may be mounted. Alternatively, the bottom may be partially or completely removed to allow better conduction of heat

from the module 515 out through the customer circuit board. Yet another alternative is to use a thermally conductive material in the bottom 518D of the connector 503. Fig. 24 shows the connectorized module 515 inserted into the connector 503.

[097] As shown, the connector terminals 508 exert inward pressure from opposing ends of the module, however, the contacts may be arranged along a single side of the module with the connector body providing the necessary resistive force for the pressure fit. Although the connectorized module is shown having plated interconnects 511 forming contacts for engagement with the connector terminals, it should be appreciated by those of skill in the art that many variations are possible. For example, adapters of the type illustrated in connection with Figs. 15-20 may be used to provide contacts for a hybrid connectorized module allowing other orientations of the module relative to the connector and to the customer circuit board.

G6. Flush Mount

[098] A flush-mount technique may be used with the horizontal PCB-mounting techniques discussed above in connection with Figs. 15-24 to allow the bottom heat sink to come into contact with the customer PCB, e.g. for heat removal. As shown in Figs. 25 and 26, a through-hole mount module 600 is shown adapted for flush-mounting to a customer PCB 900. The module 600 as shown includes two through-hole adapters 603A, 603B attached to the singulated module 615. The singulated module 615 may, as shown, have a finned top heat sink 601 and a generally flat bottom heat sink 602 for flush mounting against the PCB 900. Similar to the adapters discussed above in connections with Figs. 16-20, through-hole adapters 603A, 603B have terminals, 608, 609, 610 which include features, such as solder pad 608A, adapted to be attached, e.g. by solder, to respective interconnects on the module 615. The terminals 608, 609, 610 may be adapted to be soldered into through holes 908, 909, 910, respectively, in the customer PCB 900. As shown in Figs. 25 and 26, the generally flat heat sink 602 may include recesses 602B to accommodate flanges 618B of the adapter bodies 618 allowing most of the surface of heat sink 602 to rest flush against the surface of the PCB 900. Epoxy or other adhesive may be used in the recess to secure the adapter body to the module. The recesses may be

an integral feature of the heat sink panel or may be added at an appropriate point during the manufacturing process, preferably before singulation.

[099] A thermally conductive material 901, e.g. thermal adhesive, may be applied between the PCB 900 and the module heat sink 602 to facilitate removal of heat through the PCB 900. Additionally, the PCB surface may include thermally conductive features to conduct heat away from the module 615. For some applications particularly involving smaller module sizes, it may be desirable to solder the bottom heat sink 602 to one or more pads on the PCB 900, in which case the heat sink may include a solderable finish, applied for example by plating. Threaded holes may be provided, preferably in the flush mount heat sink panel, allowing the module to be secured using screws to a customer board or cold plate. The flush-mount modification may allow taller heat sink fins to be used on the top of the module without increasing the module profile above the customer PCB which may provide better thermal management in some environments. Additionally, the flush-mount may provide a more robust shock and vibration resistant mechanical solution.

[0100] Another flush mount module 650 may include a plurality of pins 661 protruding from the bottom heat sink 652 for engagement in through holes 911 in the customer mother board 900 as shown in Fig. 25A. Similar to the flush mount module 600 of Figs. 25 and 26, the flush mount module 650 may include adapters 653A and 653B adapted for making electrical connections with through holes on the customer mother board 900. Instead of fins, the top heat sink 651 may include a flat surface to create a low-profile package as shown in Fig. 25A. The pins 661 may be formed as an integral part of the bottom heat sink panel instead of fins. Alternatively, blind holes may be provided in the heat sink panel into which the pins may be press fit at any suitable stage of the fabrication process. The pins 661 may be used to electrically connect the bottom heat sink 652 to the customer board, e.g. to ground, conduct heat out of the module into the customer board 900, and provide mechanical support. The through holes 908, 909, 910, 911 in the customer board may be sized to provide clearance between the hole and the respective pin to compensate for any dimensional variations. The pins 661 may optionally protrude beyond the bottom surface of the customer board 900 into forced

air along the bottom surface of the board for additional heat removal. Additionally, a heat sink component (not shown) may be fitted onto the protruding pins to help dissipate heat.

H. Heat Sink Setback

[0101] As internal components are reduced in height, e.g. reducing the thickness of the magnetic core, the depth of the interior cavity may be decreased bringing the heat sink panels closer together, reducing the encapsulant thickness and the resulting module thickness. However, reduction of the encapsulant thickness has the potentially undesirable effect of reducing the spacing between the electrical interconnects and the edges of the heat sink panels in the finished module. When desirable, e.g. to satisfy safety agency requirements, the separation between the exposed interconnects, e.g. interconnects 111, 112, 113, and the edge of the heat sink, e.g. heat sink 101B, may be increased using a setback, e.g. setback 155, between the edges of the heat sink panels and the edges of the module 115B as shown in Fig. 10B. The setback 155 may be created by making wide cuts through the heat sink panels 121, 122 along the singulation lines prior to singulation. The wide cuts preferably extend through the heat sink material, e.g. aluminum, and partially into the encapsulation material to form channels 128A and 129A in the panel assembly 120A as shown in Figs. 9B and 9C. If machined while the assembly is still hot from the encapsulation process, the channels 128A and 129A may be used to divide the heat sink panels into singulated module dimensions reducing stresses due to differential contraction between the heat sink and the encapsulant due to differences in thermal coefficients of expansion while the panel assembly cools. Stresses on the narrow saw may also be reduced by eliminating the heat sink metal through which the saw must cut during singulation as a result of the channels 128A, 129A.

I. Process Efficiencies

[0102] Using interconnection features that may be exposed during singulation allows the PCB panel 124, containing a plurality of modules, to be molded as a single unit. Providing embedded interconnects along the perimeter of the circuit that occupy little or no PCB surface area help reduce wasted PCB area that would otherwise be cut away,

allowing close to full utilization of the PCB for product which may save on cost. Encapsulating the PCB panel with the heat sink panels simplifies the structural aspects of the modules. Using interior contours in the heat sink to match component heights helps reduce the amount of molding compound required for encapsulation. Furthermore, controlling the distance between the magnetic cores and the internal surface of the heat sink can be used as an alternative to and eliminating the complications of the exposed core molding process described in the Exposed Core Application.

[0103] Furthermore, using the mold panels to form the mold cavity for encapsulating the PCB panel helps free the molding equipment from product specific requirements that may otherwise require customized molds, allowing a single piece of molding equipment to be used for a wide variety of product mixes. The finished products, e.g. modules 115 made using a standard panel size, may have diverse dimensions not only in the lateral (length and width) directions, but also in the vertical (thickness) direction (e.g. due to heat sink fin height or component thickness). However, because the lateral panel dimensions remain the same, and variations in thickness from panel to panel may be accommodated by the molding press, the same general purpose molding equipment may be used for a wide variety of products of diverse dimensions. Using power converters as an example, the same mold press may be used to encapsulate panels of power converters ranging in (1) footprint size from full size, to half, to quarter, to eighth size (or any other size), and in (2) thickness (height), and in (3) topology, e.g. isolated DC-DC regulating converter, non-isolated buck regulator, DC transformer, etc. to produce a large mix of products.

[0104] A panel molding manufacturing process for a mix of products may include some or all of the following steps. Select a specific product to build. Select the requisite blank heat sink panels, e.g. based upon fin orientation, spacing, and height for the specific product. Alternatively, machine the exterior of the heat sink blank panels to produce the requisite external surface (heat sink surface, mounting features such as threaded holes, fin orientation, thickness, and spacing). Machine the interior surfaces of the heat sink blanks to form the recesses and other features (i.e. the contours of interior cavity to match some or all component locations, size, and height), of the finished heat

sink panels required for the specific product, preferably under computer control. Select the appropriate PCB panel for the specific product. Select and assemble the magnetic cores and other components onto the PCB panel, e.g. by surface mount soldering, etc. Dispense a measured quantity of molding compound into the bottom heat sink panel. Press the bottom side of PCB panel up against bottom heat sink panel. Dispense a measured quantity of molding compound on the top side of the PCB panel. Press top heat sink panel into place on the PCB panel. Place the panel assembly on a rotary table away from the axis of rotation, preferably a large distance from the axis, and spin the rotary table and panel assembly to evacuate air bubbles in the interior cavity to achieve essentially void free fill of panel assembly with molding compound. Cure the molding compound. Cut the panel along the cut lines for singulation. Apply a conformal coating to protect the interconnects, or plate the interconnects, or attach a lead frame, motherboard, or connector to the exposed interconnects.

J. PCB Symmetries

[0105] The components may be symmetrically arranged on the PCB such as shown in the power converter example of Fig. 27. The top 104-2 and bottom 104-1 faces of a populated PCB 104 from an individual power converter module are shown in plan view in Fig. 27. The populated PCB 104 is shown rotated along the vertical axis 27 in Fig. 27 to show the symmetry of the components.

J1. Symmetrical Distribution between PCB Surfaces

[0106] Many of the larger components may be distributed equally between both faces of PCB 104 as shown in Fig. 27. For example, the four input field effect transistors (FETs) 132-2D, 132-2E, 132-1D, 132-1E are shown equally distributed between the top 104-2 and bottom 104-1 surfaces with two FETs on each surface. Similar equal distribution between the top 104-2 and bottom 104-1 surfaces of the PCB 104 are shown for the eight output FETs 132-2B, 132-2C, 132-1B, 132-1C with four output FETs on each surface; the twelve input capacitors, 132-2F, 132-2G, 132-1F, 132-1G, with six input capacitors on each surface; and twenty four output capacitors 132-2A, 132-1A with twelve output capacitors on each surface. Some of the FETs can function as switches.

Distributing larger components between the two surfaces of the PCB may decrease stresses on the PCB, e.g. due to differences in the coefficient of expansion of the encapsulant, e.g. while curing, which may improve the co-planarity and mechanical integrity of the device.

J2. Symmetrical Distribution on a PCB Surface

[0107] On each surface of the PCB, components having similar characteristics, such as size or in-circuit power dissipation, may be arranged symmetrically for example as shown in Fig. 27 with respect to horizontal axis 28. It can be seem that relative to the horizontal axis 28, which is drawn longitudinally through the midline of the top and bottom surfaces of PCB 104, many of the components are arranged symmetrically. For example, the six input capacitors 132-1F and 132-1G on the bottom surface 104-1 are symmetrically distributed in a mirror-image relationship to each other relative to longitudinal midline axis 28. The same basic mirror image relationship is true for the six input capacitors 132-2F and 132-2G on the top 104-2 surface of the PCB. Similarly, the mirror image relationship is shown for the following pairs of components: bottom-side input FETs 132-1D and 132-1E, topside input FETs 132-2D and 132-2E, bottom-side output FETs 132-1B and 132-1C, topside output FETs 132-2B and 132-2C and also within the bottom-side and top-side banks of output capacitors 132-1A and 132-2A.

[0108] Distributing larger components symmetrically on a surface especially with respect to the longitudinal axis of the PCB may also decrease stresses on the PCB, e.g. due to differences in the coefficient of expansion of the encapsulant, e.g. while curing, which may also improve the mechanical integrity of the device. Additionally, spreading the components out symmetrically on each surface helps to spread the heat produced by power dissipating devices using a greater surface area for heat extraction improving the thermal performance.

J3. Symmetrical Footprints between PCB Surfaces

[0109] In addition to being equally distributed between the top and bottom surfaces and being symmetrically distributed on each PCB surface, the components may also be

situated such that pairs of components (wherein each component on one surface has a respective counterpart on the other surface) may be arranged to occupy essentially the same space on the PCB, i.e. a component may occupy a space on one surface that substantially overlaps with the footprint of a component on the other surface. For example, input capacitors 132-1F on the bottom surface are in the same position as their counterparts 132-2F on the top surface, i.e. they share the same footprint on the PCB. The same relationship is generally true for: input capacitors 132-1G and 132-2G; output capacitors 132-1A and 132-2A; input FETs 132-1D and 132-2D; input FETs 132-1E and 132-2E; output FETs 132-1B and 132-2B; output FETs 132-1C and 132-2C; in which the pairs of components occupy the same basic footprint, albeit on opposite surfaces, of the PCB. One benefit of sharing footprints allows the pair of components to share a common set of conductive vias used to electrically connect the components on the PCB surfaces to internal conductive layers, e.g. used to form the windings of the transformer. Because each via is used for both components in the pair, the total number of vias for making connections to the pair of components may be reduced (by as much as a factor of two) increasing the area of conductive layers useable for making connections and thus reducing resistance. For example, assuming 6 vias are required for each output FET (a total of 12 vias for two FETs), using symmetrical footprint approach, the pair of FETs can share the same 6 vias (without increasing the via resistance) and because the number has been reduced the useable area for conductors may be increased. Alternatively, while reducing the total number of vias from 12 to some intermediate number, e.g. 8, the resistance of the vias may be decreased because of the increase in effective vias per FET while still increasing the area useable for conductors.

J4. Symmetrical Power Dissipation between PCB Surfaces

[0110] The components may be arranged between the PCB surfaces according to heat dissipated during operation. For example, the heat dissipative components may be arranged in a manner that distributes the heat evenly between the two PCB surfaces allowing heat produced by power dissipating devices to be extracted from both surfaces of the PCB improving the thermal performance. This type of heat dissipation symmetry is also factored into the component layout shown in the power converter of Fig. 27. For

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example, two input cells each using the same basic circuit topology are shown, one above and another below axis 28. As shown, the components of each input cell occupy both sides of the PCB in observance of other factors influencing component layout such as winding locations, etc. In this example, the upper input cell includes the two input FETs 132-1D and 132-2D, and the six input capacitors 132-1F and 132-2F. The lower input cell includes the two input FETs 132-1E and 132-2E, and the six input capacitors 132-1G and 132-2G. To ensure heat dissipation symmetry between the two surfaces, the cells may be arranged in mirror image layouts as shown. In Fig. 27, input FET 132-2E (top surface) in the lower cell corresponds to input FET 132-1D (bottom surface) in the upper cell. Similarly, lower cell input FET 132-1E (bottom surface) corresponds to upper cell input FET 132-2D (top surface). As can be seen, the significant power dissipative components of the input cells are arranged to have one component of one cell mounted on one surface with the respective component from the other cell mounted on the other surface. This type of symmetry may be seen in Fig. 27 with lower cell component 132-2H mounted on the top surface and the respective upper cell component 132-1H mounted on the bottom surface. In some examples, the FETs are arranged such that during operation, the power FETs on the top surface dissipate power at a level that is comparable to the level of power dissipated by the power FETs on the bottom surface. Also, the level of power dissipated by the power FETs in the upper input cell is comparable to the level of power dissipated by the power FETs in the lower input cell. For example, the level of power dissipated by the power FETs on one surface is less than 150% of the level of power dissipated by the power FETs on the other surface. The level of power dissipated by the power FETs in the upper cell is less than 150% of the level of power dissipated by the power FETs in the lower cell, and vice versa.

[0111] Laying out the components using any or all of the above symmetries produces several key benefits including, enhanced thermal performance, reducing top to bottom and side to side imbalances during encapsulation caused by asymmetrical distribution of components may enhance the co-planarity and structural integrity, and shared component footprints on top and bottom PCB surfaces may help reduce conduction losses and increase efficiency.

K. Center Plate Panel Assembly

[0112] In an alternate embodiment, an optional center plate 727 may be used between the top 721 and bottom 722 heat sink panels as illustrated in Fig. 28 through Fig. 32. The center plate 727, which may be made from aluminum, a molded high temperature plastic or any other material suitable for the molding process, includes an opening 729 in which the populated PCB panel 724 may sit during the panel molding process. As shown in the side view of Fig. 29 and the cross-sectional view of Fig. 32, the PCB panel 724 may sit entirely within the opening 729 and may have some high profile components, such as magnetic cores 131 and capacitors 132 (continuing with the power converter example), extending beyond the planar surfaces of the center plate. The recesses formed in the interior surfaces of the heat sink panels 721, 722 (described above) may accommodate portions of the components extending beyond the center plate surface. Conversely, protrusions from the interior surface of the heat sink panels may be used to reduce the distance between the heat sink and lower profile components. However, it may be preferable for ease of fabrication and tolerance control to avoid protrusions of the heat sink beyond the surface of the center plate which may put an upper limit on the thickness of the center plate in some embodiments.

[0113] As shown in the exploded perspective view of Fig. 28 and the top plan view of Fig. 31, registration features may be provided in the center plate 727. For example, registration pins 728 may mate with corresponding holes 734 in the PCB 724 to establish the horizontal position, i.e. in the X and Y directions, of the PCB relative to the center plate 727. Additional registration features such as the illustrated horizontal shelf 728A (Fig. 28), may be provided to establish the vertical position, i.e. in the Z direction, of the PCB relative to the center plate. The registration pins 728 may be long enough to extend beyond the upper surface of the PCB panel 724 in the upward direction and beyond the horizontal shelf in the downward direction to mate with holes (analogous to holes 152 and 153 in Fig. 4B) which may be provided in the top and bottom heat sink panels 721, 722 establishing the horizontal positions of the mold panels relative to the center plate 727. Provision of the registration features in the center plate may help relax certain precision requirements, the complexity, and thus the cost of the heat sink panels.

[0114] A cross-section of the panel assembly 720 closed in a mold press taken through line 32-32 in Figs. 30 and 31 is shown in Fig. 32. As shown, the upper mold press 761 engages the center plate 727 directly along its perimeter in regions 768 and engages the heat sink panels directly along their perimeters in regions 769. Preferably the mold press includes recessed surfaces 766 providing cavities 765 large enough to accommodate a full range of fin heights (or other heat sink panel features) supporting a diverse range of products. To compensate for dimensional differences between the thickness of the heat sink panels in regions 769 and the difference in elevation between interface regions 768 and 769 in the mold press, one or more compressible features may be provided at the interface between the heat sink panels 721, 722 and the center plate 727. For example, a small crushable feature 723 may be formed along the perimeter of and as an integral part of the heat sink panels as illustrated in Fig. 32. Alternatively a gasket may be used between the center plate and one or both of the heat sink panels. As the press closes on the panel assembly 720 the crushable features 723 are compressed until the press is closed securely against both the center plate 727 and the heat sink panels 721, 722. As shown in Fig. 31, the crushable features may extend along the perimeter of the interior cavity forming a seal between each heat sink panel and the center plate.

[0115] The center plate may preferably include an extension, e.g. extension 730, to at least one side of opening 729 providing space for one or more chambers 725 as shown in Figs. 30, 31, and 32. During the transfer molding process, encapsulation material may be forced from the chambers through one or more channels 726 (as shown in Figs 28 and 32) in the center plate into opening 729 and thus the cavity in which the populated PCB panel 724 is enclosed. An example of encapsulant flow through a chamber 725, channel 726, and into the interior cavity 746 is illustrated by the arrows 767 shown in Fig. 32.

[0116] In the center plate panel mold assembly, the top and bottom mold panels (i.e., heat sink panels 721, 722) close against the center plate instead of each other, reducing the thickness of the top and bottom mold panels, increasing the symmetry between, and reducing the complexity of, the top and bottom heat sink panels 721, 722, potentially simplifying the molding press, eliminating critical tolerance accumulations in the assembly, simplifying the process and reducing cost. For example, provision of the

chambers 725 and conduits 726 in the center plate 727 eliminates the need for sealing along a second axis, e.g. in a horizontal direction and allows for use of a simpler cull-on-plate molding press. Critical tolerances are reduced to the one vertical dimension of the heat sink panels which can be relaxed using a crushable feature or a compliant material on the surface that interfaces with the center plate. Additionally, the center plate 727 may be standardized allowing a single configuration to be used with a large variety of heat sink panels such that the center plate may be cost-effectively molded.

[0117] A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, non-metallic mold panels may be used. The center plate may be provided as a single-use consumable or may be modified to be used as a reusable fixture in the molding process. The center plate may be provided with or without the encapsulation channels. The registration holes in the heat sink panels may extend completely through the heat sink panels similar to hole 152 shown in Fig. 4B and the registration pins, e.g. pins 728 (Figs. 28 and 31), may extend completely through each of the heat sink panels allowing fasteners to be used in conjunction with the pins to hold the panel assembly together before and after the encapsulation process. The fasteners may function as or be used in conjunction with a seal around the pin to contain any encapsulant. Throughput through the mold press may be increased by using panel assemblies that are secured together and removed from the mold press before the panel has cooled or the encapsulant has set or both. The registration pins 728 and corresponding holes 734 may be used to align the panel assembly during the singulation process. In some examples, a panel assembly (e.g., 120) may be formed by dispensing encapsulant into a bottom panel mold (e.g., heat sink panel 122), assembling a substrate (e.g., PCB panel 124) into the bottom panel mold, dispensing encapsulant onto a top of the substrate, and assembling a top panel mold (e.g., heat sink panel 121) onto the substrate. In some examples, the surfaces of the PCB panel 124 may have conductive features that are covered by an insulative layer. Blank mold panels may be machined to provide some or all of the various features described above in an on-demand manufacturing system.

[0118] In some examples, the upper and lower heat sinks 121, 122 are clamped together by the upper and lower mold presses 161, 162 at respective clamp regions of the upper and lower heat sinks 121, 122. The clamp region of the upper heat sink 121 can be located at points along a circumference of an internal cavity defined by the interior surface of the upper heat sink 121. The clamp region of the lower heat sink 122 can be located at points along a circumference of an internal cavity defined by the interior surface of the lower heat sink 122. In some examples, the clamp regions are cut away from the panel assembly 120 to expose the interconnects 111, 112, and 113. After the cut, portions of the upper and lower heat sinks 121, 122 near an active circuit area remain attached to the panel assembly 120, allowing heat from the active circuit area during operation to be dissipated through the remaining portions of the upper and lower heat sinks 121, 122. The active circuit area can be, e.g., an area of the PCB panel 124 having active components, such as magnetic core structures 131 and electronic components 132. Interlocking contours, other than the undercuts 148 shown in Figs. 6, 7, and 12, can also be formed in the interior surface of the mold panel, the contour being filled with cured mold compound enhancing the structural integrity of the singulated module. In some examples, most of the large-footprint components (e.g., 132-2D, 132-2E, 132-2B, 132-2C) are distributed substantially symmetrically between quadrants surrounding the transformer core (e.g., 131-2) on a surface of the PCB panel 124. For example, in FIG. 27, the input FETs 132-2D and 132-2E are distributed substantially symmetrically between the upper-right and lower-right quadrants surrounding the transformer core 131-2. The output FETs 132-2B and 132-2C are distributed substantially symmetrically between the upper-left and lower-left quadrants surrounding the transformer core 131-2.

[0119] Accordingly, other embodiments are within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A method of making a plurality of electronic devices, comprising:

providing a plurality of mold panels, which when assembled, form an internal chamber;

providing a substrate having a plurality of conductive traces and a plurality of components electrically connected to form at least one circuit, the substrate having at least one contact for making an electrical connection to the circuit;

forming a panel assembly including the mold panels assembled with the substrate in the internal chamber and an encapsulant filling spaces between the substrate and interior surfaces of the chamber;

curing the encapsulant; and

cutting the panel assembly to expose at least a portion of the at least one contact and form a respective exposed contact.

2. The method of claim 1 wherein the cutting comprises making a first cut in at least one of the mold panels, and in the first cut, making a second narrower cut through the panel assembly.

3. The method of claim 2 wherein the curing comprises raising the temperature of the panel assembly and the first cut is made before the panel assembly cools after the curing.

4. The method of claim 1 wherein the cutting divides the panel assembly producing at least one module having a plurality of layers including respective portions of each of the panel molds, the substrate, and the encapsulant, and the module contains the at least one circuit.

5. The method of claim 4 wherein the cutting defines at least one side of the module.

6. The method of claim 4 wherein the cutting defines two or more sides of the module.

7. The method of claim 1 further comprising treating the exposed contact to protect against oxidation.

8. The method of claim 7 wherein the treating comprises applying a removable conformal coating to the exposed contact.

9. The method of claim 7 wherein the treating comprises applying a layer of metal to the exposed contact.

10. The method of claim 9 wherein the applying a layer of metal comprises applying solder.

11. The method of claim 9 wherein the applying a layer of metal comprises applying a precious metal.

12. The method of claim 9 wherein the applying a layer of metal comprises plating.

13. The method of claim 4 further comprising

providing an adapter having at least one electrical terminal; and

attaching the at least one electrical terminal to the exposed contact.

14. The method of claim 13 wherein

the at least one contact comprises a plurality of contacts;

the module comprises a plurality of exposed contacts;

the adapter has a plurality of electrical terminals arranged to match respective ones of the plurality of exposed contacts; and

the adapter is mechanically secured to the module.

15. The method of claim 4 wherein the mold panels are metal.

16. The method of claim 15 wherein the respective portions of the mold panels provide heat sink surfaces for the module.

17. The method of claim 1 wherein the providing mold panels further comprises providing contours in an internal surface of one or more of the mold panels.

18. The method of claim 17 wherein the providing contours further comprises matching depths of portions of the internal surface to heights of one or more selected components.

19. The method of claim 18 wherein the selected components include at least one magnetically permeable core and at least one semiconductor device.

20. The method of claim 4, wherein the traces and components are electrically connected to form a plurality of separable circuits arranged in a pattern on the substrate; and the cutting divides the panel assembly along spaces between the separable circuits into a plurality of modules each containing at least one respective circuit.

21. The method of claim 20 wherein the spaces between the separable circuits have dimensions approximately matching a width of cuts produced by equipment used to cut the panel assembly.

22. The method of claim 21 wherein the at least one contact comprises a plurality of contacts located in the spaces between the separable circuits.

23. The method of claim 22 wherein the plurality of contacts are formed in the substrate.

24. The method of claim 23 wherein the plurality of contacts are formed and buried below at least one surface of the substrate.

25. The method of claim 15 further comprising treating at least one exterior surface of at least one of the mold panels for solderability.

26. The method of claim 1 wherein forming the panel assembly comprises:

dispensing encapsulant into a bottom panel mold;

assembling the substrate into the bottom panel mold;

dispensing encapsulant onto a top of the substrate; and

assembling a top panel mold onto the substrate.

27. The method of claim 26 further comprising centrifuging the assembly before curing the encapsulant.

28. The method of claim 1 wherein forming the panel assembly comprises:

assembling the substrate with a first substrate surface facing into a first panel mold,

closing a second panel mold onto the substrate covering a second substrate surface,

providing one or more conduits to the internal chamber, and

forcing encapsulant through the one or more conduits into the chamber.

29. The method of claim 28 further comprising centrifuging the assembly before curing the encapsulant.

30. The method of claim 9 further comprising providing a connector for removably mating with and providing electrical connection to the metal.

31. The method of claim 1 further comprising:

providing a center plate having an opening to accommodate the substrate; and

wherein the forming a panel assembly includes positioning the substrate in the opening of the center plate and closing the mold panels against the center plate.

32. The method of claim 31 further comprising providing at least one opening in the center plate connected to the internal chamber by at least one conduit; and

forcing the encapsulant through the at least one opening and at least one conduit into the internal chamber.

33. The method of claim 32 wherein the forming a panel assembly further comprises securing the mold panels together prior to curing the encapsulant.

34. A method of forming an electrical contact comprising:

assembling a panel including a substrate having one or more conductive features enclosed within the panel and unexposed to an exterior surface of the panel, the one or more conductive features being located along a cut line;

cutting the panel along the cut line exposing portions of the one or more conductive features for use as electrical connections to the substrate; and

treating the portions of the one or more conductive features exposed from the cutting for preservation as electrical connections.

35. The method of claim 34 wherein the treating further comprises applying solder to the portions of the one or more conductive features exposed from the cutting.

36. The method of claim 34 wherein the treating further comprises applying a conformal coating to the portions of the one or more conductive features exposed from the cutting to protect against oxidation.

37. The method of claim 34 wherein the treating further comprises applying a metal layer to the portions of the one or more conductive features exposed from the cutting.

38. The method of claim 34 wherein the treating further comprises soldering a lead of an adapter to the portions of the one or more conductive features exposed from the cutting.

39. The method of claim 34 further comprising covering at least one surface of the substrate in an area including the cut line and the conductive features prior to cutting the substrate.

40. The method of claim 39 wherein the covering comprises encapsulating the substrate with a molding compound; and further comprising:

providing a registration feature having a predetermined relationship to the substrate, and

using the registration feature to align the cutting relative to the cut line.

41. The method of claim 34 further comprising establishing a pattern including at least one conductive layer in the substrate along the cut line to form the conductive features.

42. The method of claim 41 wherein the substrate comprises a multilayer printed circuit board and the establishing a pattern includes establishing a plurality of conductive layers along the cut line to form the conductive features.

43. The method of claim 34 further comprising establishing a pattern including at least one conductive via in the substrate along the cut line to form the conductive features.

44. The method of claim 43 wherein the conductive via is filled with a conductive material.

45. The method of claim 43 wherein the conductive via is buried in the substrate.

46. The method of claim 43 wherein the conductive via is a through hole contacting the surfaces of the substrate.

47. The method of claim 46 wherein the through hole is filled with a conductive material.

48. The method of claim 34 wherein the conductive features are covered at the surfaces of the substrate by an insulative layer.

49. An apparatus comprising:

a first mold panel comprising

an exterior surface,

an interior surface defining an internal cavity,

a clamp region located at points along a circumference of the internal cavity, and

an opening,

the first mold panel being adapted to

(a) be engaged by pressure in the clamp region,

(b) receive in the cavity a circuit panel containing a plurality of components and mold compound to fill empty spaces in the internal cavity, and

(c) be cut after curing of the mold compound.

50. The apparatus of claim 49 wherein the interior surface in the region of the internal cavity is adapted to adhere to the mold compound.

51. The apparatus of claim 49 further comprising

a second mold panel comprising

an exterior surface,

an interior surface, and

a clamp region,

wherein the second mold panel is adapted to

(a) close against and mate with the first mold panel,

(b) be engaged by pressure in the clamp region, and

(c) be cut after curing of the mold compound.

52. The apparatus of claim 51 wherein the interior surface of the second mold further defines a second internal cavity, the clamp region of the second mold panel is located at points along a circumference of the second internal cavity, and the internal cavity of the first mold panel is adapted to receive a first side of the circuit panel and the second internal cavity is adapted to receive a second opposite side of the circuit panel.

53. The apparatus of claim 52 further comprising contours formed in the interior surface of at least one of the mold panels.

54. The apparatus of claim 53 wherein the contours are adapted to match predetermined characteristics of selected ones of the plurality of components.

55. The apparatus of claim 53 wherein the internal surface of the mold panel is adapted to adhere to the molding compound.

56. The apparatus of claim 55 wherein the contours form interlocking features with cured mold compound.

57. The apparatus of claim 53 wherein at least one of the mold panels comprises a non-ferrous metal.

58. The apparatus of claim 57 wherein at least one of the mold panels comprises aluminum.

59. The apparatus of claim 51 wherein at least one of the mold panels comprises a thermally conductive material.

60. The apparatus of claim 53 wherein at least one of the mold panels comprises a non-metallic substance.

61. The apparatus of claim 51 further comprising at least one channel connected to the internal cavity for allowing expansion of the mold compound.

62. The apparatus of claim 51 further comprising at least one channel connected to the internal cavity for injecting mold compound into the internal cavity.

63. The apparatus of claim 59 wherein the exterior surface of the mold panel comprises a plurality of fins.

64. The apparatus of claim 59 wherein the exterior surface of the mold panel comprises a flat surface.

65. The apparatus of claim 64 wherein the flat surface is adapted for a solder joint.

66. The apparatus of claim 49 wherein the internal cavity includes features formed in the interior surface and arranged in a predetermined pattern.

67. The apparatus of claim 49 wherein the internal cavity includes features formed in the interior surface along lines through which the mold panel maybe cut to establish a setback from a cut edge of the mold panel.

68. The apparatus of claim 49 wherein the mold panel further comprises at least one registration feature adapted to engage and establish a predetermined relationship with the circuit panel.

69. The apparatus of claim 49 wherein one or more selected portions of the mold panel are adapted for incorporation into one or more products, the products being formed by a process which uses the mold panel to contain the molding compound.

70. The apparatus of claim 59 wherein the exterior surface of the mold panel comprises a flat surface with one or more pins protruding from the flat surface.

71. The apparatus of claim 59 wherein the exterior surface of the mold panel comprises a flat surface having one or more holes in the flat surface.

72. The apparatus of claim 71 further comprising a pin inserted into a respective one of the one or more holes.

73. An apparatus comprising:

a panel assembly having external surfaces defined by a first mold panel and a second mold panel;

the first and second mold panels forming an internal cavity enclosing an internal circuit board, the internal circuit board having a first surface and second surface and a plurality of components in an active circuit area on at least one of the surfaces, the components being electrically connected to interconnects contained within the internal cavity;

the internal cavity being filled with mold compound in spaces unoccupied by the circuit board and components;

the panel assembly being adapted to have first selected portions of the first and second mold panels cut away to expose the interconnects and to have second selected portions of the respective mold panels situated near the active circuit area remain attached to the assembly following the cut.

74. The apparatus of claim 73 wherein the panel assembly includes a clamp region located at points along a circumference of the first and second internal cavities, and the first selected portions comprise the clamp region.

75. An apparatus comprising:

a panel assembly having external surfaces defined by a first mold panel and a second mold panel;

the first and second mold panels forming an internal cavity enclosing an internal circuit board, the internal circuit board having a first surface and second surface and a plurality of components electrically connected to form a plurality of individual circuits, each individual circuit being electrically connected to respective interconnects located along a respective circuit perimeter, the interconnects being contained within the cavity.

76. The apparatus of claim 75 wherein the panel assembly is adapted to be cut along the circuit perimeter separating the individual circuits, dividing the panel assembly into individual circuit modules, and exposing selected portions of the interconnects.

77. The apparatus of claim 75 wherein the panel assembly is constructed to retain an integral layered structure after being filled with mold compound which is subsequently cured, the layered structure comprising a first layer including a portion of the first mold, a second layer including a portion of the mold compound, a third layer including a portion of the circuit board, a fourth layer including a portion of the mold compound, and a fifth layer including a portion of the second mold.

78. The apparatus of claim 75 wherein the internal circuit board comprises a plurality of circuits having the same functionality.

79. The apparatus of claim 75 further comprising one or more conduits connecting the internal cavity to an external opening.

80. The apparatus of claim 75 wherein spaces unoccupied by the circuit board, components, and interconnects in the internal cavity are filled with mold compound.

81. The apparatus of claim 80 wherein the mold compound has been cured.

82. The apparatus of claim 81 wherein selected portions of at least one of the mold panels have been removed, the selected portions being located near the circuit perimeters.

83. An apparatus comprising:

a modular package having a first external surface, a second external surface opposite the first external surface, and a side wall extending along the perimeter of and connecting with the first and second external surfaces, the modular package including a first layer defining the first external surface and a second layer defining the second external surface, the first and second layers being separated by and in contact with cured mold compound; and

an electrical circuit located between the first and second layers and within the cured mold compound and including at least one electrical component electrically connected to a plurality of interconnects;

the side wall comprising a strip formed by the first layer, a strip formed by the second layer, and a strip formed by the cured mold compound; and

the interconnects being disposed within the side wall.

84. The apparatus of claim 83 wherein the first and second layers further comprise a non-ferrous metal.

85. The apparatus of claim 84 wherein the first and second layers further comprise aluminum.

86. The apparatus of claim 85 wherein the first external surface further comprises a plurality of fins.

87. The apparatus of claim 85 wherein the first external surface further comprises an essentially flat area.

88. The apparatus of claim 87 wherein the essentially flat area is adapted for a solder joint.

89. The apparatus of claim 83 wherein the electrical circuit further comprises a circuit board and the side wall further comprises a strip formed by the circuit board and an additional strip formed by cured mold compound.

90. The apparatus of claim 89 wherein the interconnects further comprise conductive features in the circuit board.

91. The apparatus of claim 90 wherein the circuit board comprises a multilayer printed circuit board ("PCB") and each of the interconnects comprises a plurality of conductive layers in the PCB.

92. The apparatus of claim 90 wherein each of the interconnects comprises a plurality of conductive vias in the circuit board.

93. The apparatus of claim 83 further comprising interlocking features comprising a contour formed in an interior surface of the first layer, the contour being filled with cured mold compound.

94. The apparatus of claim 91 wherein the circuit board includes a top surface and a bottom surface and the at least one electrical component comprises a set of top-side components mounted on the top surface and a set of bottom-side components mounted on the bottom surface.

95. The apparatus of claim 94 wherein

the top-side components include a number, T, of large-footprint components, the bottom-side components include a number, B, of large-footprint components, and the number T is approximately equal to the number B.

96. The apparatus of claim 95 wherein each of most of the top-side large-footprint components shares a respective set of conductive vias with a corresponding one of the bottom-side large-footprint components.

97. The apparatus of claim 95 wherein each of most of the top-side large-footprint components is located in a respective footprint shared by a corresponding one of the bottom-side large-footprint components.

98. The apparatus of claim 89 wherein the circuit board includes a top surface and a bottom surface, the at least one electrical component comprises a number, T, of large-footprint components mounted on the top surface, and most of the large-footprint components are distributed symmetrically in relation to an axis on the top surface.

99. The apparatus of claim 98 wherein the axis is along a midline of the top surface.

100. The apparatus of claim 98 wherein the axis is defined in relation to a predetermined component.

101. The apparatus of claim 83 further comprising:

an adapter for providing mechanical and electrical connections between the modular package and an external mounting surface, the adapter having a body and a plurality of electrical terminals supported by the body; and

electrical connections formed between the adapter terminals and respective interconnects on the modular package;

the adapter body being mechanically secured to the modular package;

the adapter terminals being arranged to mate with the external mounting surface.

102. The apparatus of claim 101 wherein the external mounting surface is a circuit board and the terminals comprise ends constructed and arranged to be inserted into conductive holes in the circuit board.

103. The apparatus of claim 101 wherein the external mounting surface is a circuit board and the terminals comprise ends constructed and arranged to be surface mount soldered to the circuit board.

104. The apparatus of claim 101 wherein the external mounting surface includes a connector and the terminals comprise ends constructed and arranged to mate with the connector.

105. The apparatus of claim 101 wherein the interconnects are disposed along a long edge of the modular package, the adapter is secured to the long edge of the modular package, and the first and second layers of the modular package are oriented perpendicular to the mounting surface.

106. The apparatus of claim 101 wherein the interconnects are disposed along opposite edges of the modular package, the adapter is secured to the opposite edges, and the first and second layers of the modular package are oriented essentially parallel to the mounting surface.

107. The apparatus of claim 106 wherein the adapter is constructed and arranged to maintain one of the first or second layers in contact with the mounting surface.

108. The apparatus of claim 83 wherein the interconnects further comprise a surface constructed and arranged for engagement with a connector terminal.

109. The apparatus of claim 83 wherein the interconnects further comprise a layer of metal plating.

110. An apparatus comprising:

a modular package having a first external surface, a second external surface opposite the first external surface, and a side wall extending along the perimeter of and connecting with the first and second external surfaces, the modular package including a first layer of metal defining the first external surface and a second layer of metal defining the second external surface, the first and second layers being separated by and in contact with cured mold compound; and

an electrical circuit for converting power, including a printed circuit board ("PCB"), a plurality of components including semiconductors mounted to the PCB, and a plurality of interconnects electrically connected to the components, the electrical circuit being located between the first and second layers and within the cured mold compound;

the side wall comprising a strip formed by the first layer, a strip formed by the second layer, a strip formed by the PCB, and one or more strips formed by the cured mold compound;

the interconnects being disposed within the side wall.

111. The apparatus of claim 110 wherein the first and second layers further comprise aluminum, and the first external surface further comprises a plurality of fins.

112. The apparatus of claim 110 wherein the first and second layers further comprise aluminum, and the first external surface comprises an essentially flat area.

113. The apparatus of claim 112 wherein the essentially flat area is adapted for a solder joint.

114. The apparatus of claim 110 wherein the PCB includes a top surface and a bottom surface, the semiconductors include large-footprint switches, a number, T, of top-side large-footprint switches are mounted on the top surface, a number, B, of bottom-side large-footprint switches are mounted on the bottom surface, and the number T is approximately equal to the number B.

115. The apparatus of claim 114 wherein each large-footprint switch is connected to one or more other components by a respective set of conductive vias in the PCB, and each of a plurality of the top-side large-footprint switches shares its respective set of conductive vias with a corresponding one of the bottom-side large-footprint switches.

116. The apparatus of claim 114 wherein each of most of the large-footprint switches is positioned on one surface in a location substantially overlapping a location on the other surface occupied by another large-footprint switch.

117. The apparatus of claim 110 wherein the PCB includes a top surface and a bottom surface, the semiconductors include large-footprint switches mounted on the top surface, most of the large-footprint components are distributed symmetrically between a left side of the top surface and an opposite right side of the top surface.

118. The apparatus of claim 110 wherein the PCB includes a top surface and a bottom surface, the semiconductors include large-footprint switches mounted on the top surface, and most of the large-footprint components are distributed symmetrically between quadrants on the top surface.

119. The apparatus of claim 118 wherein the components further comprise a transformer core, and the quadrants surround the transformer core.

120. The apparatus of claim 110 wherein the PCB includes a top surface and a bottom surface, the components include a set of high-profile components having similar heights, a number, T, of the high-profile components are mounted on the top surface, a number, B, of the high-profile components are mounted on the bottom surface, and the number T is approximately equal to the number B.

121. The apparatus of claim 120 wherein a spatial distribution of the high-profile components on the top surface roughly matches a spatial distribution of the high-profile components on the bottom surface.

122. The apparatus of claim 110 further comprising:

an adapter for providing mechanical and electrical connections between the modular package and an external mounting surface, the adapter having a body and a plurality of electrical terminals supported by the body; and

electrical connections formed between the adapter terminals and respective interconnects on the modular package,

the adapter body being mechanically secured to the modular package;

the adapter terminals being arranged to mate with the external mounting surface.

123. The apparatus of claim 122 wherein the external mounting surface is a circuit board and the terminals comprise ends constructed and arranged to be inserted into conductive holes in the circuit board.

124. The apparatus of claim 122 wherein the external mounting surface is a circuit board and the terminals comprise ends constructed and arranged to be surface mount soldered to the circuit board.

125. The apparatus of claim 122 wherein the external mounting surface includes a connector and the terminals comprise ends constructed and arranged to mate with the connector.

126. The apparatus of claim 122 wherein the interconnects are disposed along a long edge of the modular package, the adapter is secured to the long edge of the modular package, and the first and second layers of the modular package are oriented perpendicular to the mounting surface.

127. The apparatus of claim 122 wherein the interconnects are disposed along opposite edges of the modular package, the adapter is secured to the opposite edges, and the first and second layers of the modular package are oriented essentially parallel to the mounting surface.

128. The apparatus of claim 127 wherein the adapter is constructed and arranged to maintain one of the first or second layers in contact with the mounting surface.

129. The apparatus of claim 110 wherein the interconnects further comprise a surface constructed and arranged for engagement with a connector terminal.

130. The apparatus of claim 110 wherein the interconnects further comprise a layer of metal plating.

131. The apparatus of claim 110 wherein the first layer further comprises contours formed in an interior surface of the first layer, the contours including a first feature having a shape and an elevation to accommodate a first component on the PCB, the first component having a height greater than or less than other components on the PCB.

132. The apparatus of claim 131 wherein the first component includes a magnetic core structure and the elevation is a recess in the interior surface.

133. The apparatus of claim 131 wherein the first component includes a semiconductor switch and the elevation is a protrusion from the interior surface.

134. The apparatus of claim 110 further comprising interlocking features comprising a contour formed in an interior surface of the first layer, the contour being filled with cured mold compound.

135. The apparatus of claim 110 wherein the modular package further comprises a recess formed in the first layer adjacent one or more of the interconnects providing a setback between the first layer and the one or more interconnects.

136. An apparatus comprising:

a power converter including

a printed circuit board ("PCB") comprising a plurality of conductive layers and having a top surface and a bottom surface;

a magnetic core structure magnetically coupled to a winding formed by traces in one or more of the conductive layers in the PCB; and

a plurality of power semiconductor devices, a first set of the power semiconductor devices being mounted on the top surface and electrically connected to dissipate power at a level, Pt, during operation of the converter, a second set of the power semiconductor devices being mounted on the bottom surface and electrically connected to dissipate power at a level, Pb, during operation of the converter;

wherein the power semiconductor devices are distributed between the first and second sets to distribute heat generation during operation of the converter such that each level Pt, Pb is less than 150% of the other level Pb, Pt.

137. The apparatus of claim 136 wherein a plurality of the power semiconductor devices in the first set are each positioned in a location on the top surface substantially overlapping a location on the bottom surface occupied by a power semiconductor device in the second set.

138. The apparatus of claim 136 wherein the power semiconductor devices are electrically connected using a respective set of conductive vias in the PCB, and a plurality of the power semiconductor devices in the first set share their respective sets of conductive vias with corresponding power semiconductor devices in the second set.

139. The apparatus of claim 137 wherein the power converter further comprises circuitry including a pair of cells having a common circuit topology and each including power semiconductor switches from each of the first and second sets; each cell having its respective components arranged in a pattern, wherein the pattern of components of one cell is substantially a mirror image of the pattern of components in the other cell.

140. The apparatus of claim 139 wherein a component from one of the cells is located on an opposite surface of a respective component from the other one of the cells.

141. The apparatus of claim 140 wherein the cells comprise input cells.

142. The apparatus of claim 138 wherein the power semiconductor devices comprise output switches.

143. A method of manufacturing a plurality of products comprising:

inserting a plurality of components into a cavity formed by one or more molds;

closing the one or more molds to form a seal around the cavity;

filling the cavity with mold compound;

curing the mold compound in the cavity to secure the components, cured mold compound, and molds together into an assembly; and

cutting the assembly to separate the plurality of products from the assembly, the products each including a respective section of the one or more molds which remains as an integral part of each respective product.

144. The method of claim 143 further comprising maintaining a predetermined alignment between the plurality of components and the one or more molds.

145. The method of claim 143 wherein the plurality of components include a substrate having conductive features; and the cutting comprises exposing portions of the conductive features in each respective product.

ABSTRACT

A method of encapsulating a panel of electronic components such as power converters reduces wasted printed circuit board area. The panel, which may include a plurality of components, may be cut into one or more individual pieces after encapsulation with the mold forming part of the finished product, e.g. providing heat sink fins or a surface mount solderable surface. Interconnection features provided along boundaries of individual circuits are exposed during the singulation process providing electrical connections to the components without wasting valuable PCB surface area. The molds may include various internal features such as registration features accurately locating the circuit board within the mold cavity, interlocking contours for structural integrity of the singulated module, contours to match component shapes and sizes enhancing heat removal from internal components and reducing the required volume of encapsulant, clearance channels providing safety agency spacing and setbacks for the interconnects. Wide cuts may be made in the molds after encapsulation reducing thermal stresses and reducing the thickness of material to be cut during subsequent singulation. External mold features can include various fin configurations for heat sinks, flat surfaces for surface mounting or soldering, etc. Blank mold panels may be machined to provide some or all of the above features in an on-demand manufacturing system. Connection adapters may be provided to use the modules in vertical or horizontal mounting positions in connector, through-hole, surface-mount solder variations. The interconnects may be plated to provide a connectorized module that may be inserted into a mating connector.

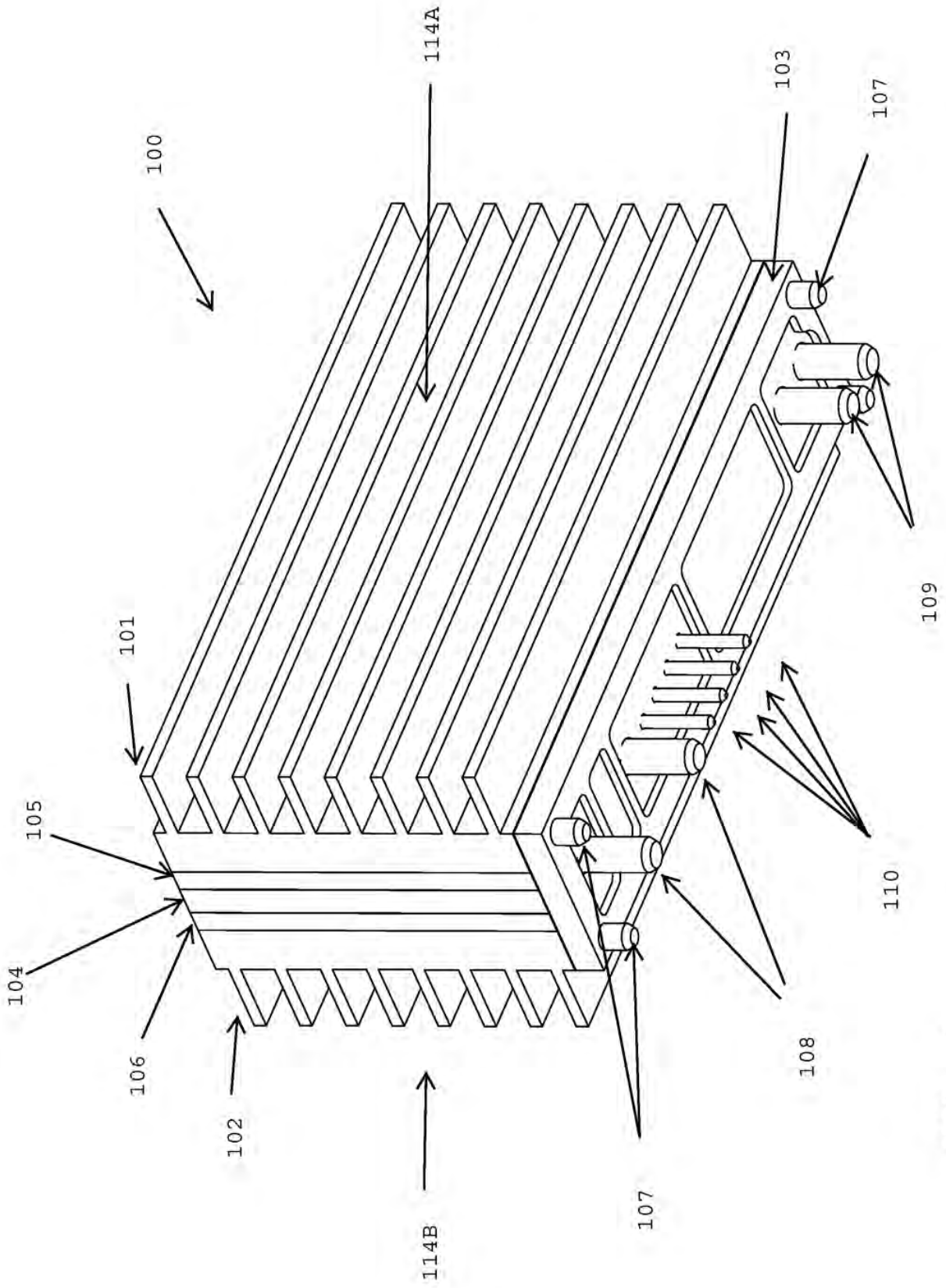


FIG. 1

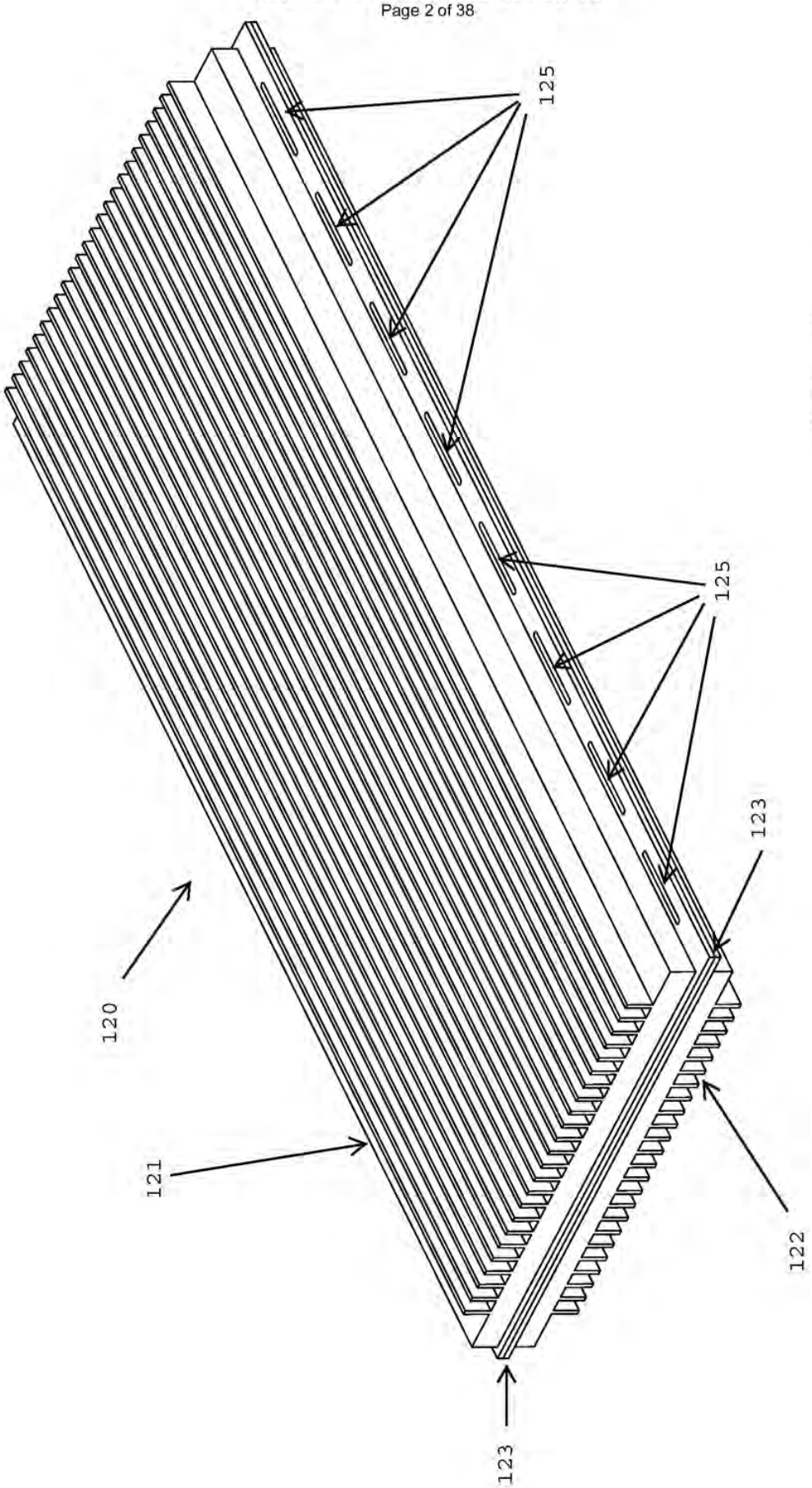


FIG. 2

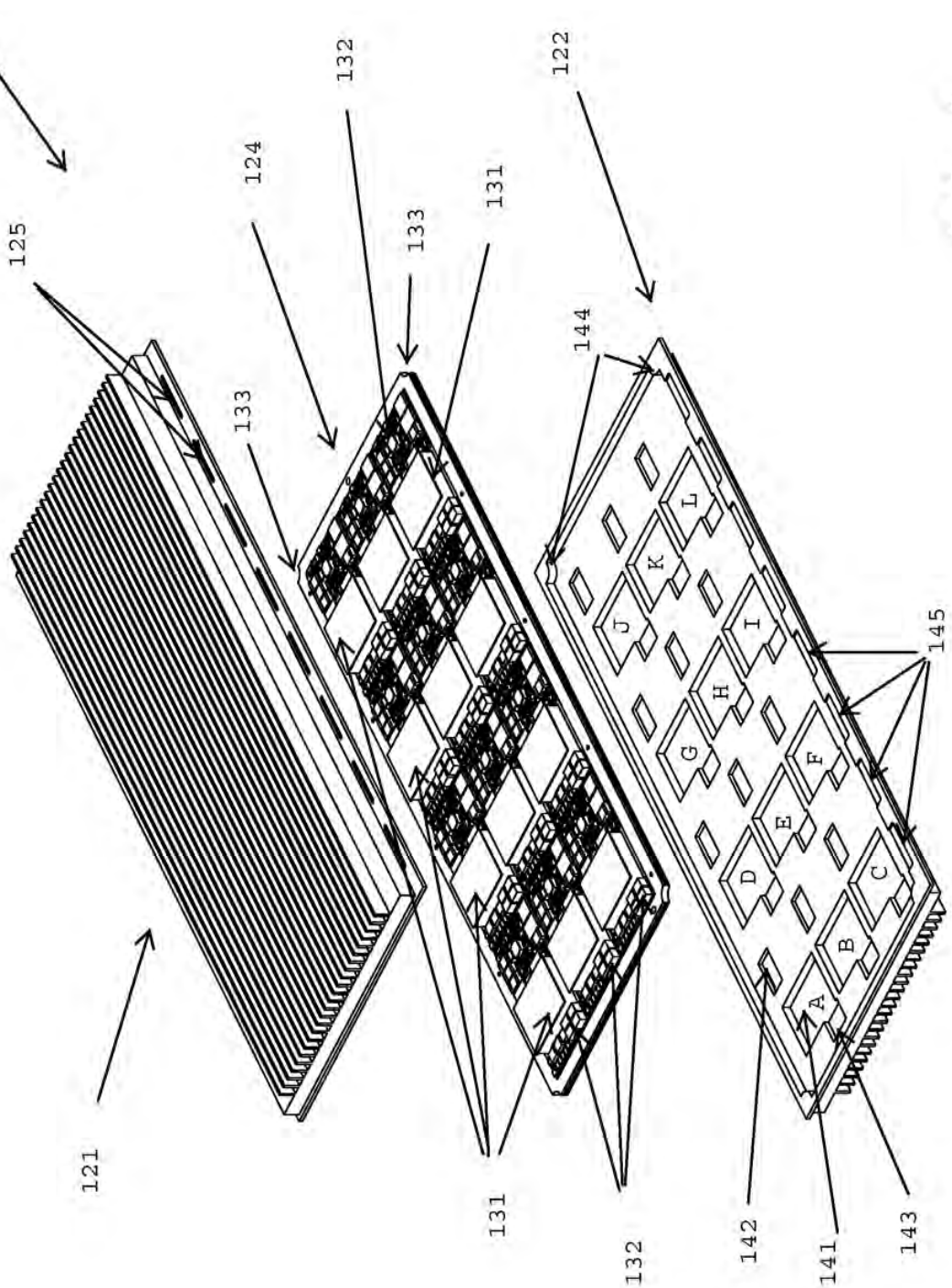

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FIG. 3

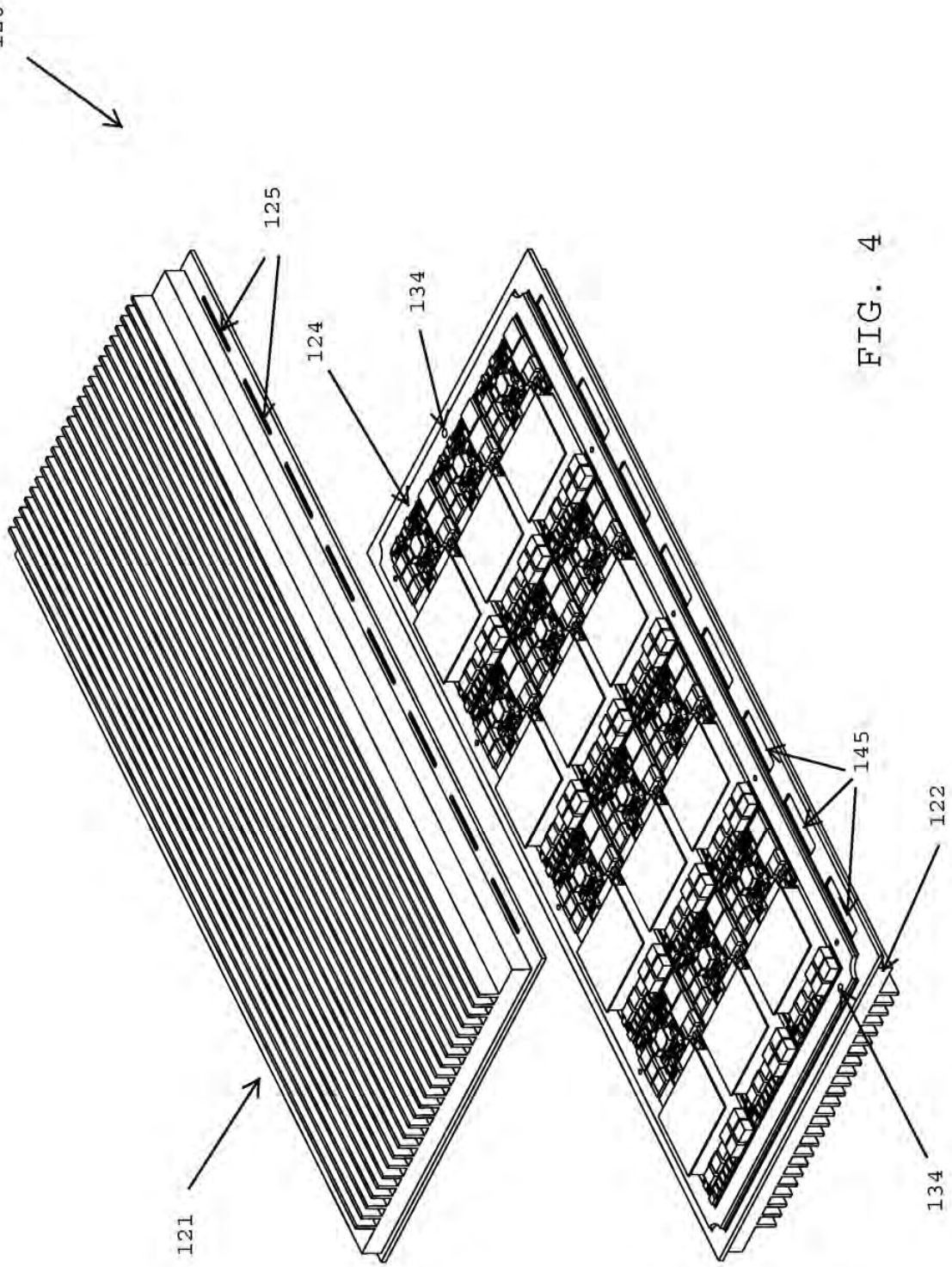


FIG. 4

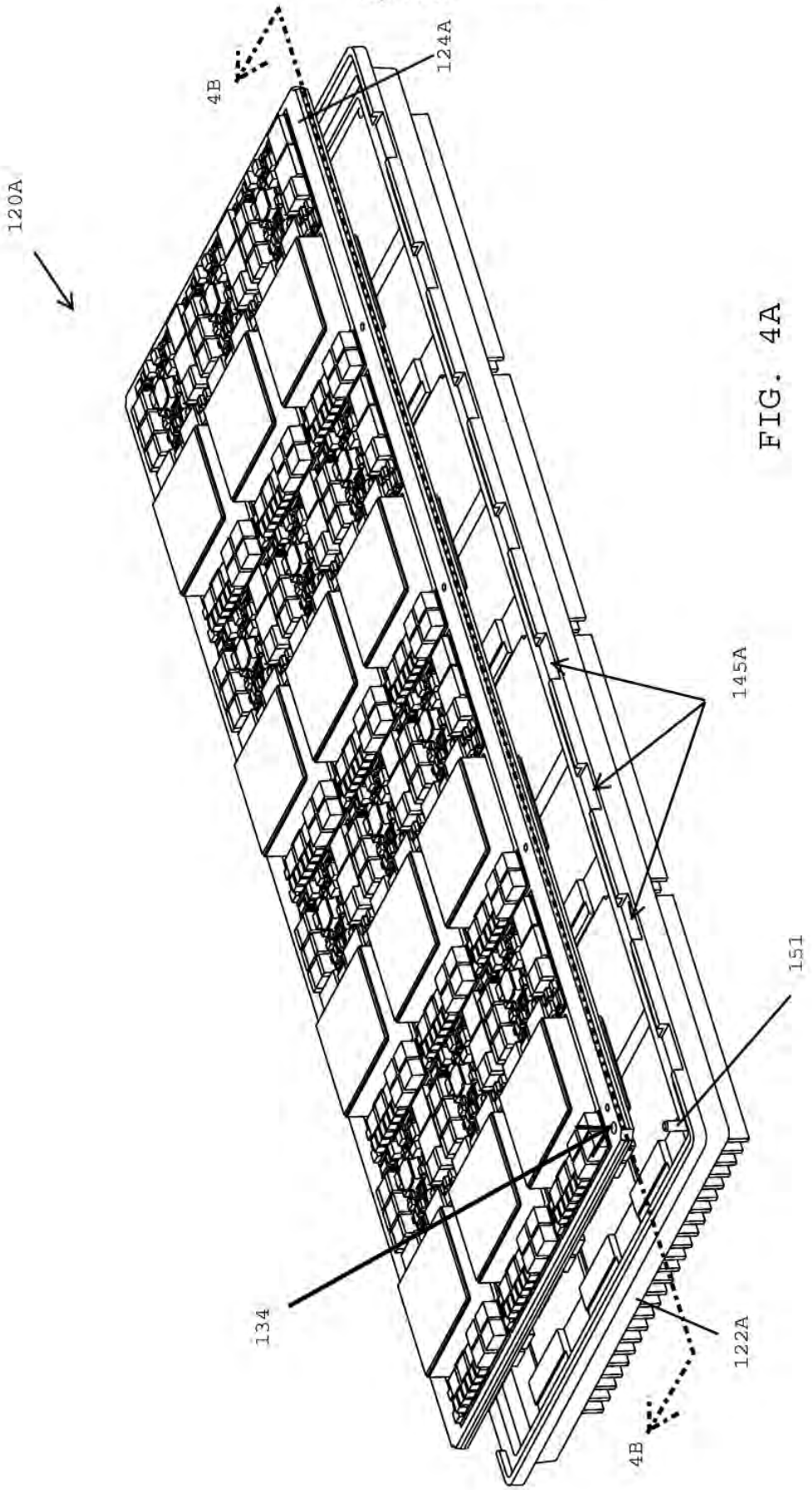


FIG. 4A

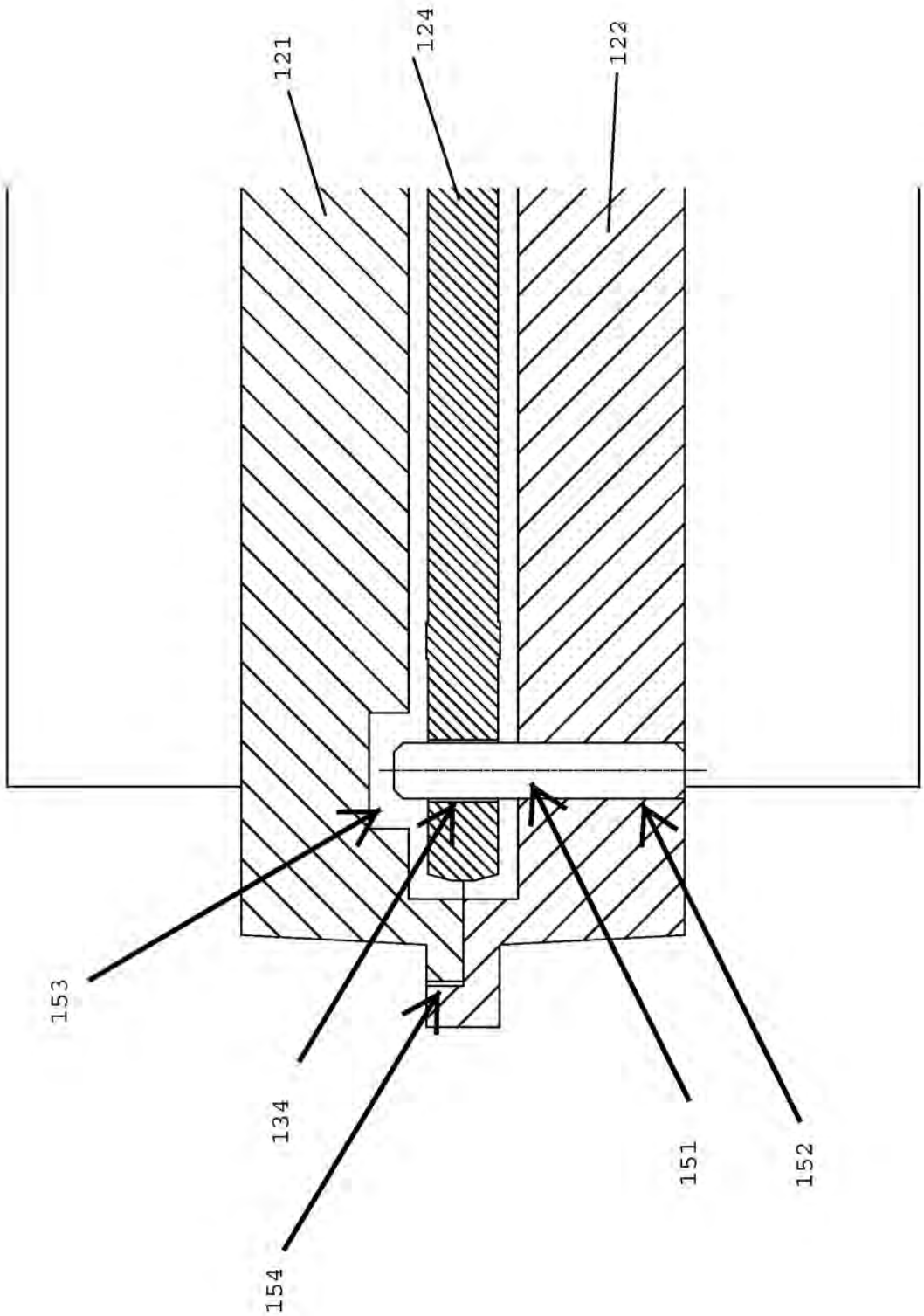


FIG. 4B

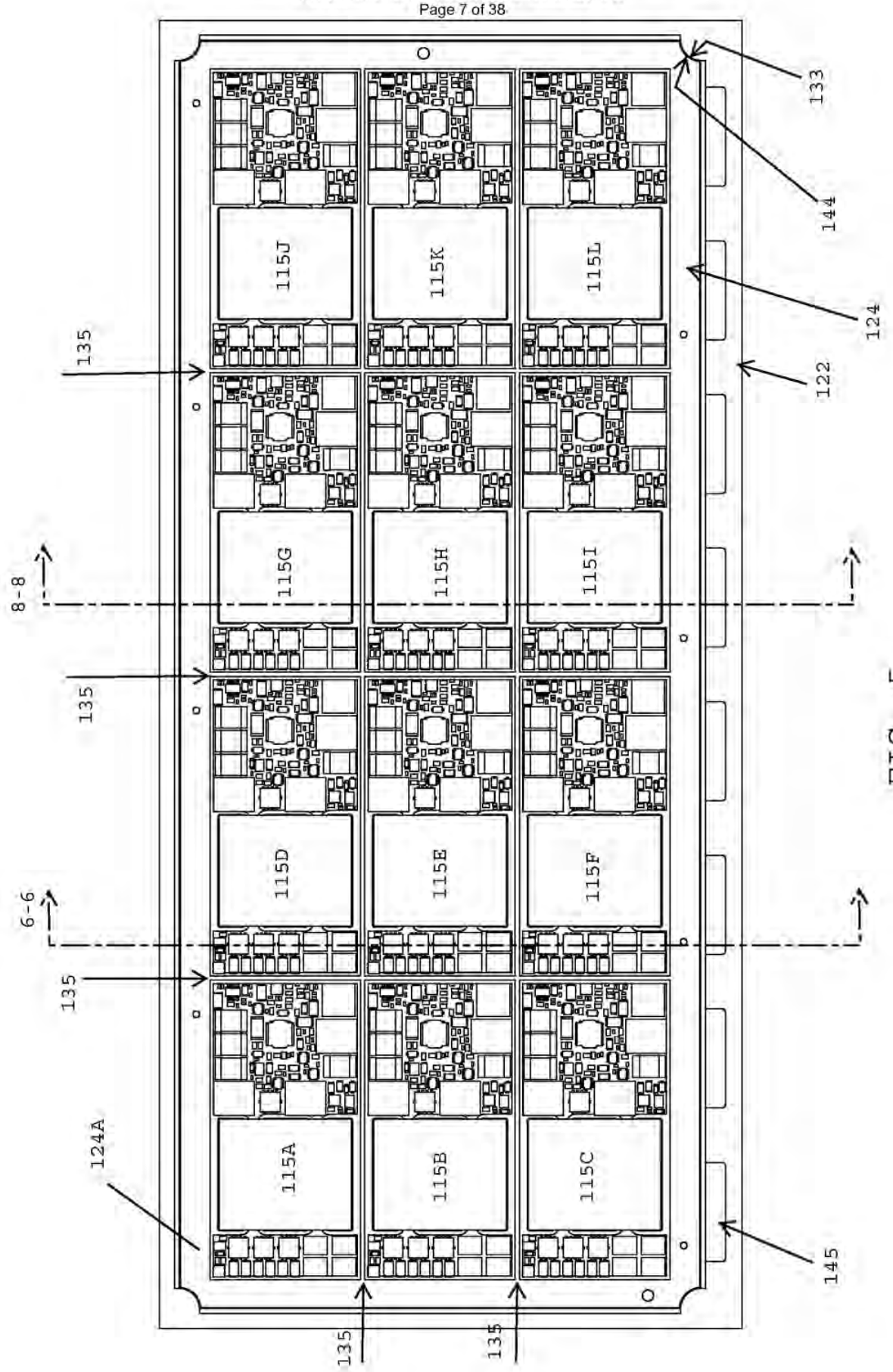

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FIG. 5

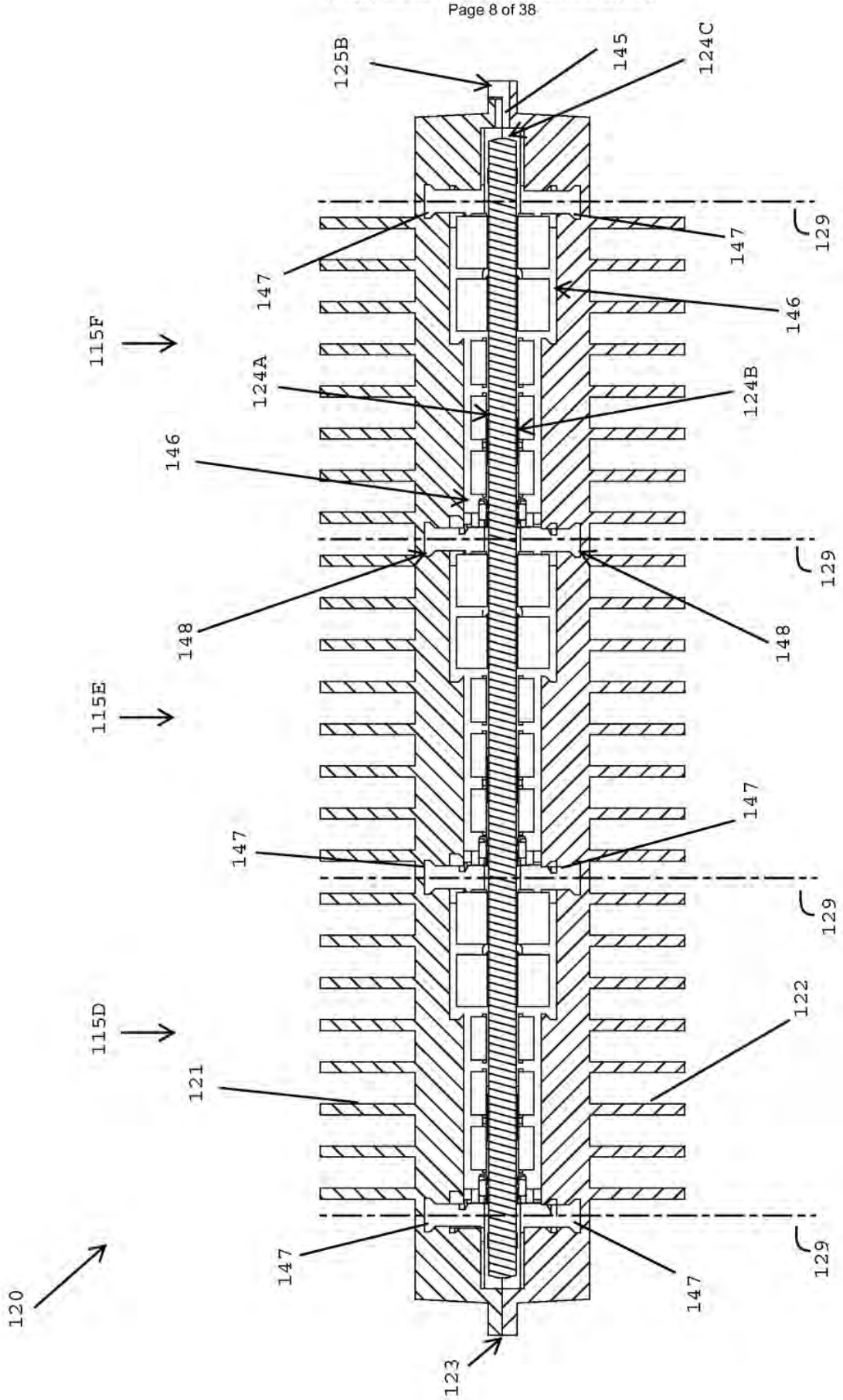

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FIG. 6

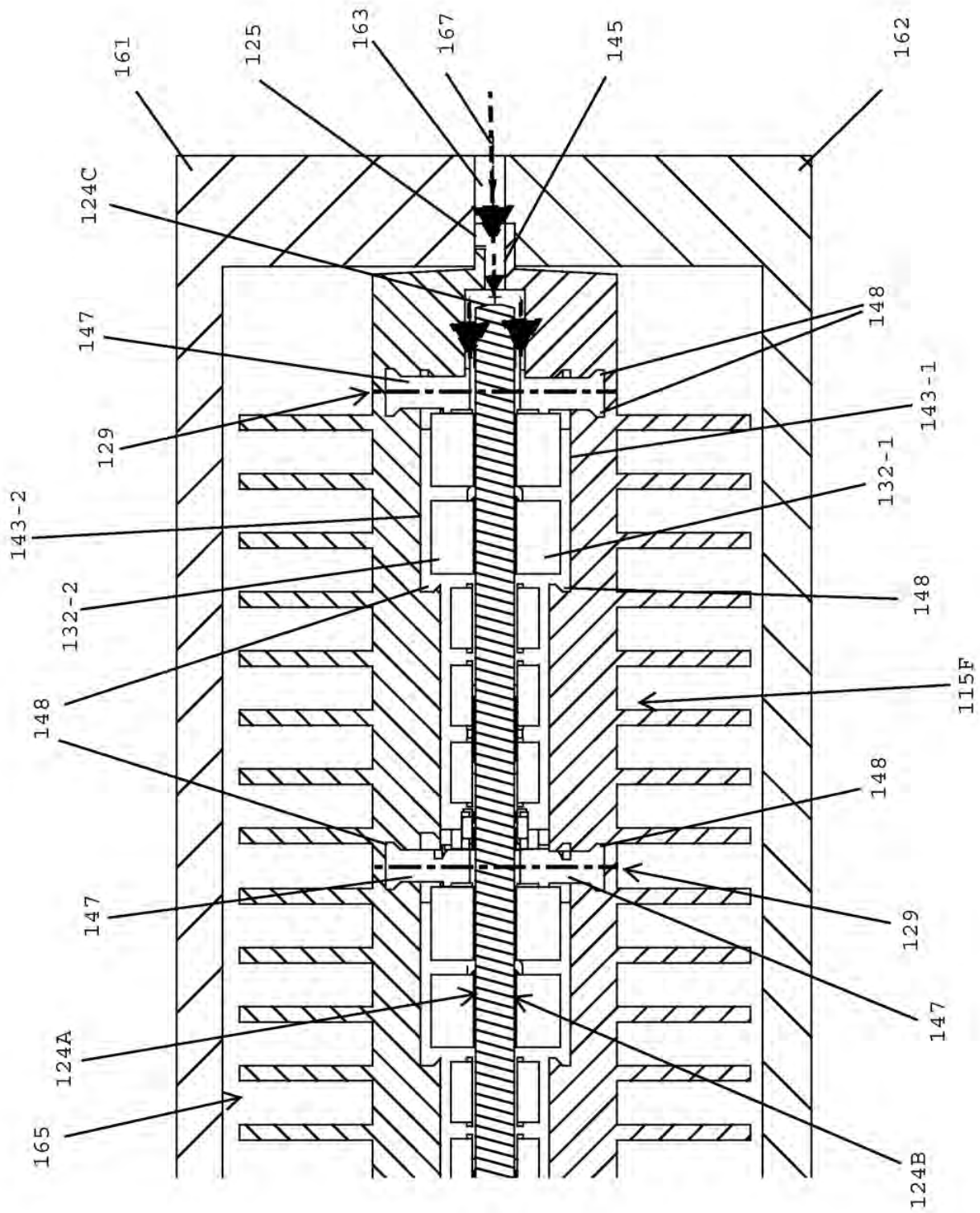

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124B

FIG. 7

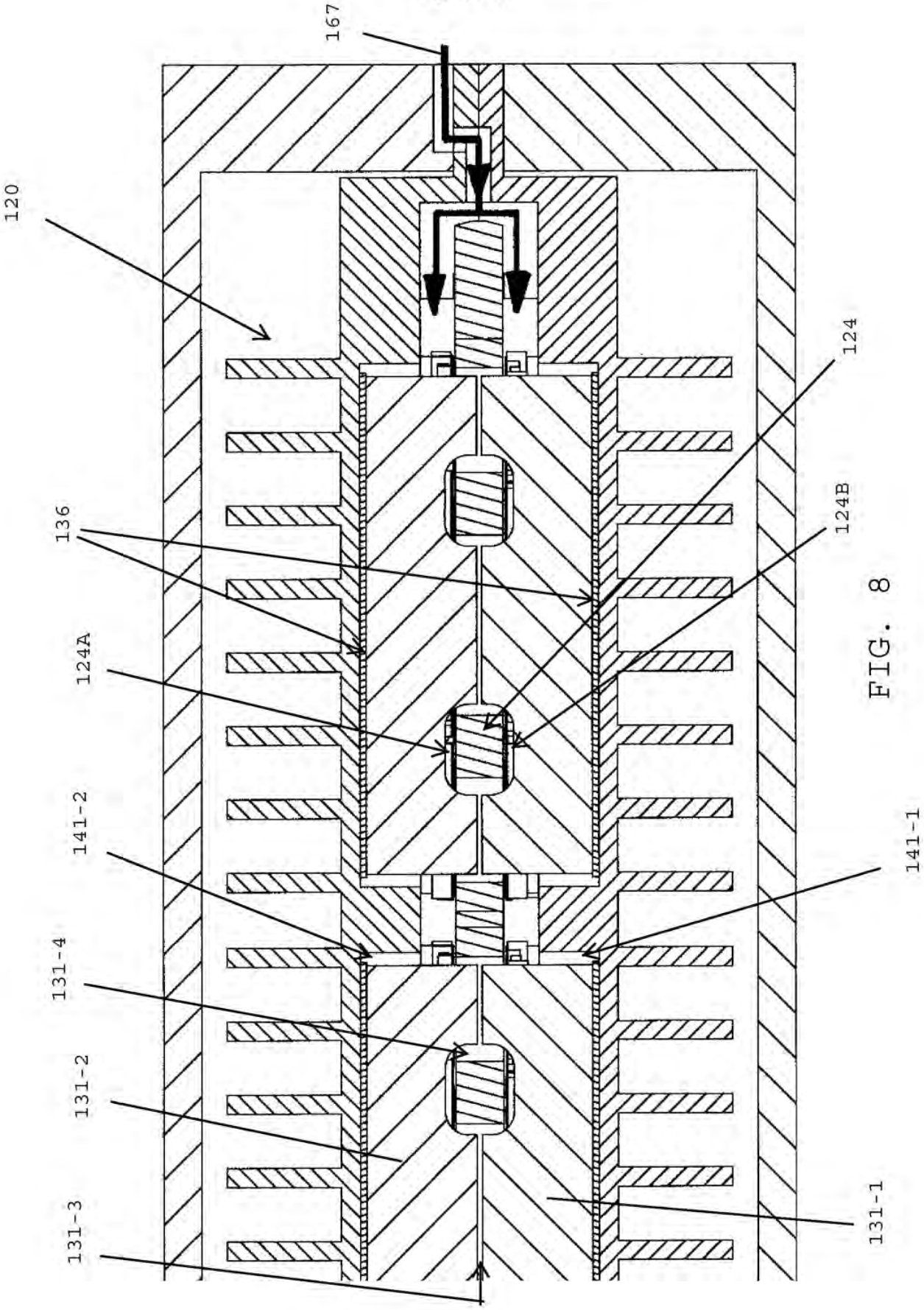


FIG. 8

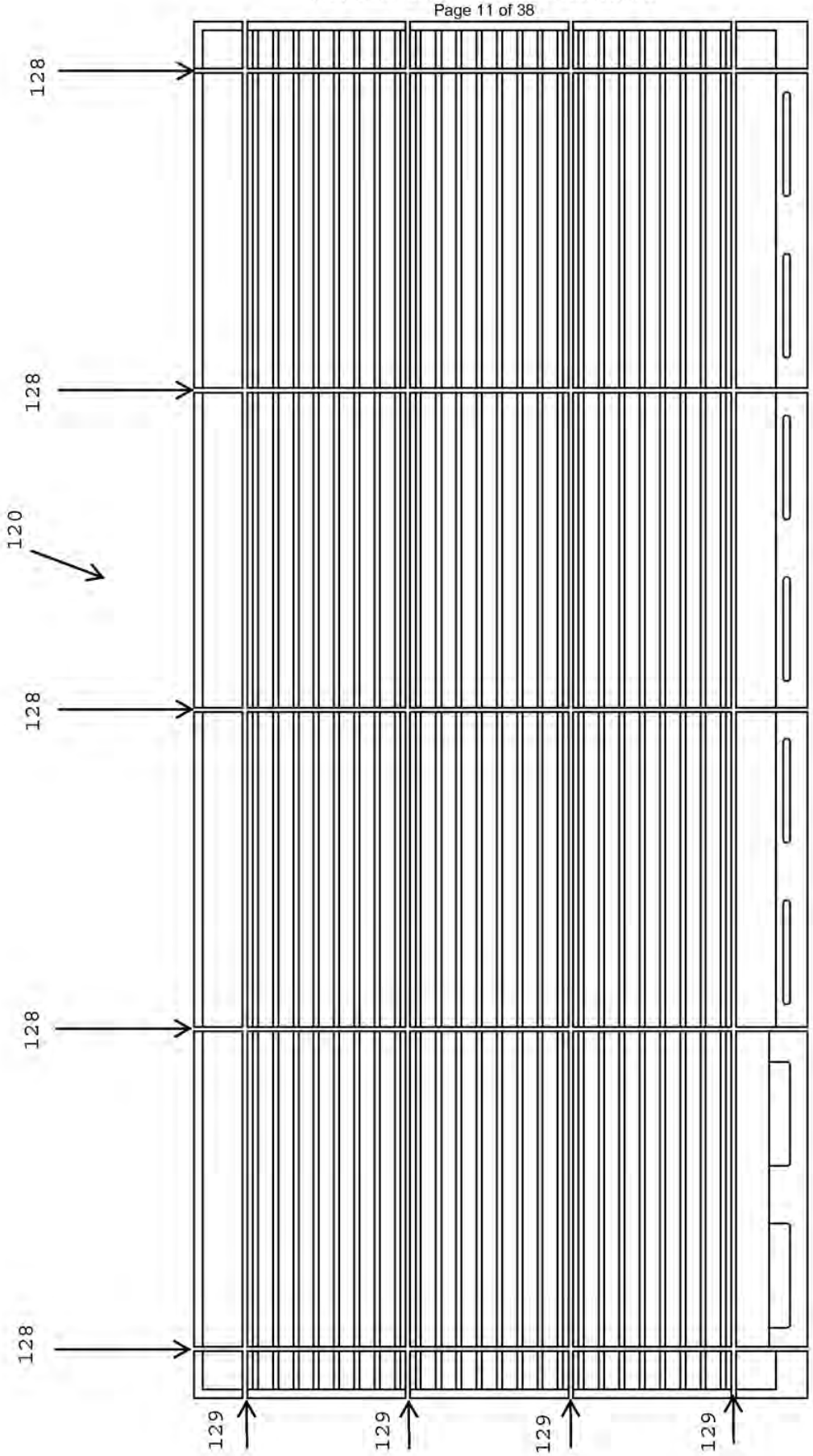


FIG. 9A

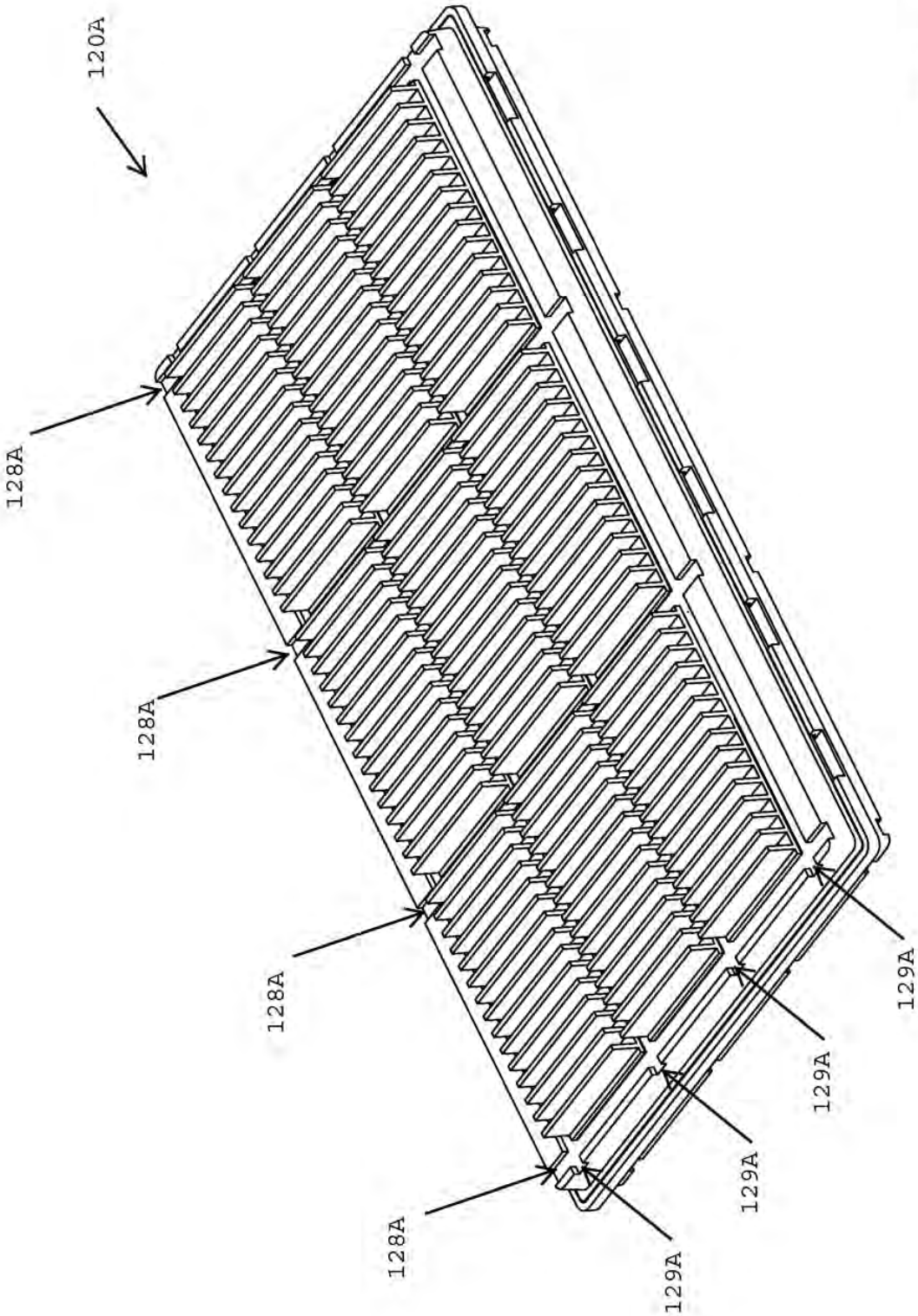


FIG. 9B

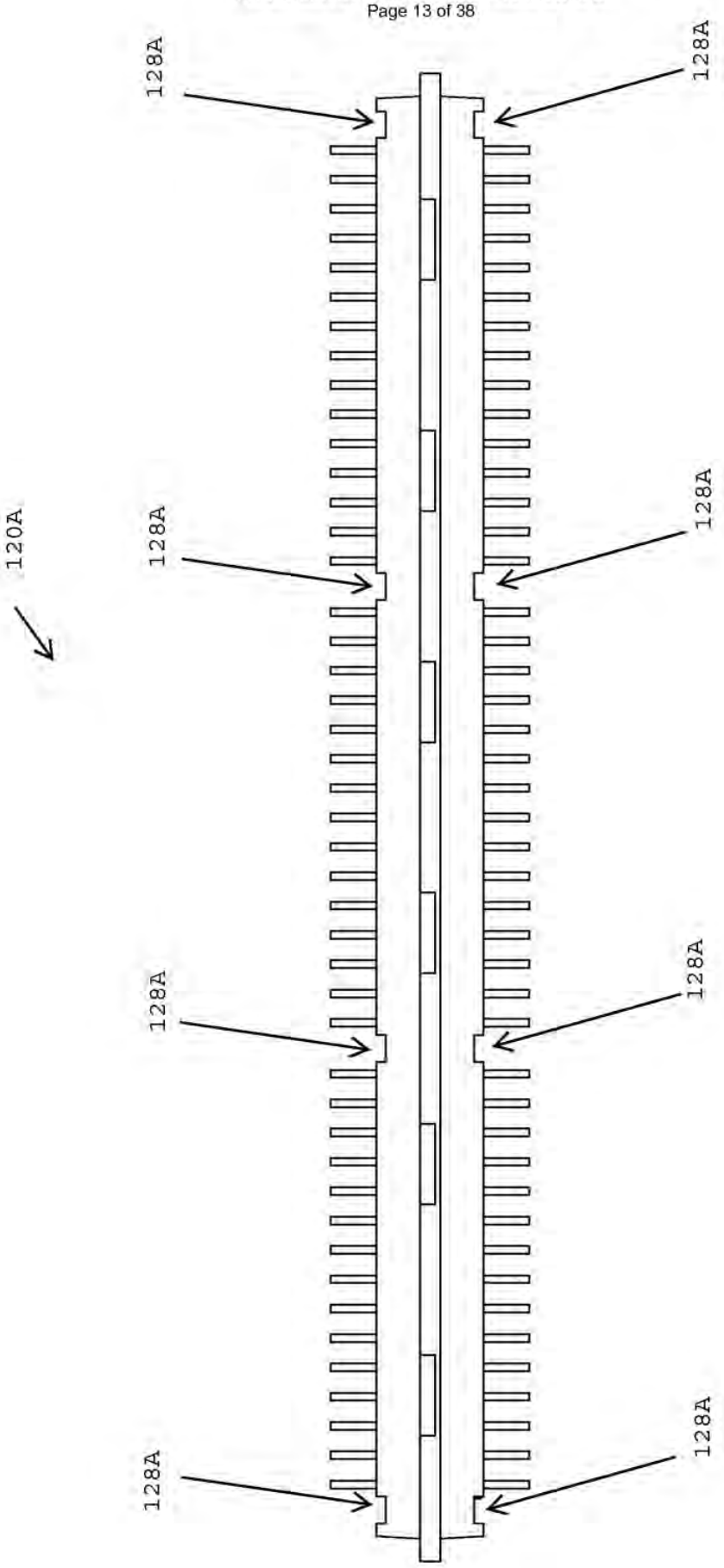


FIG. 9C

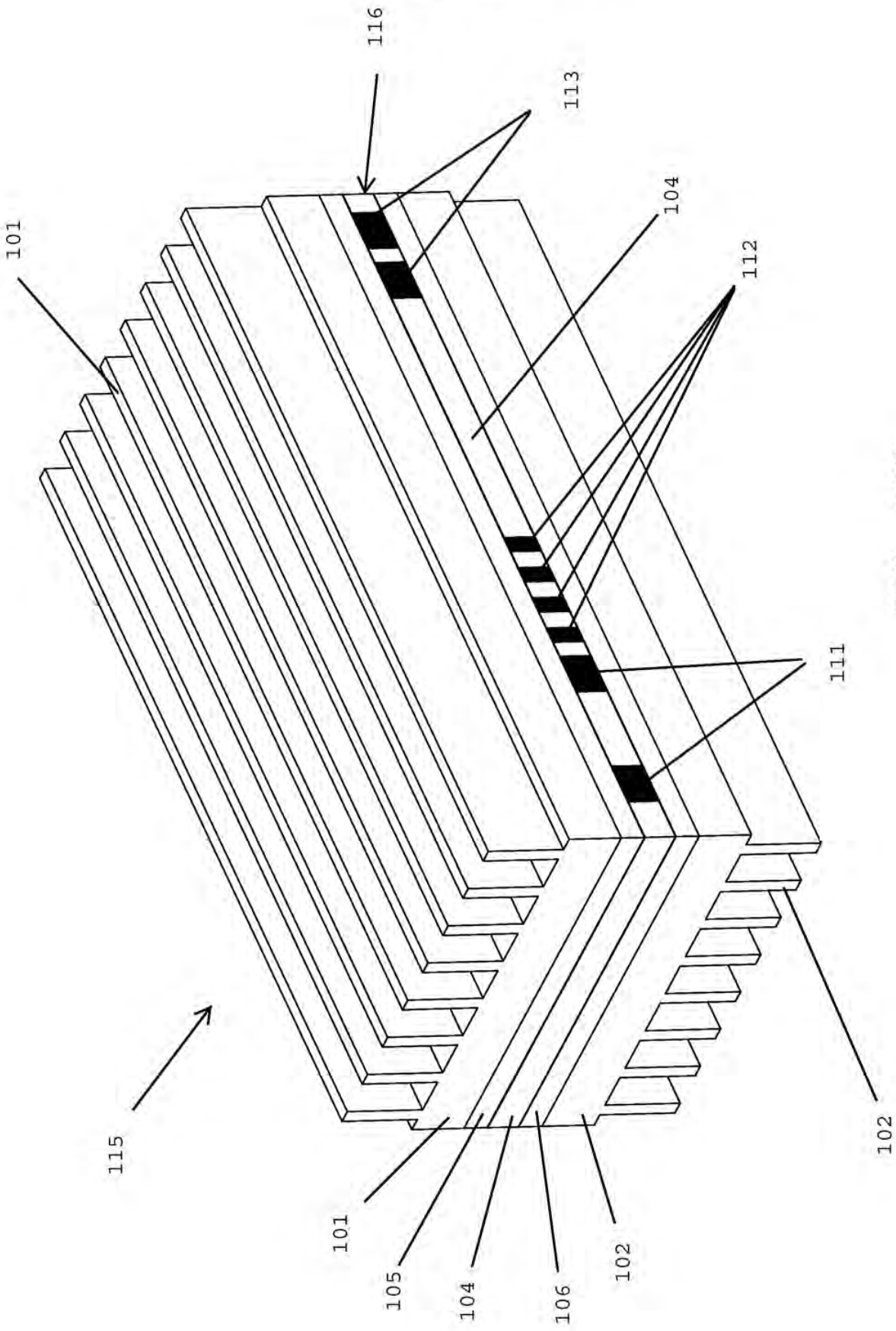


FIG. 10A

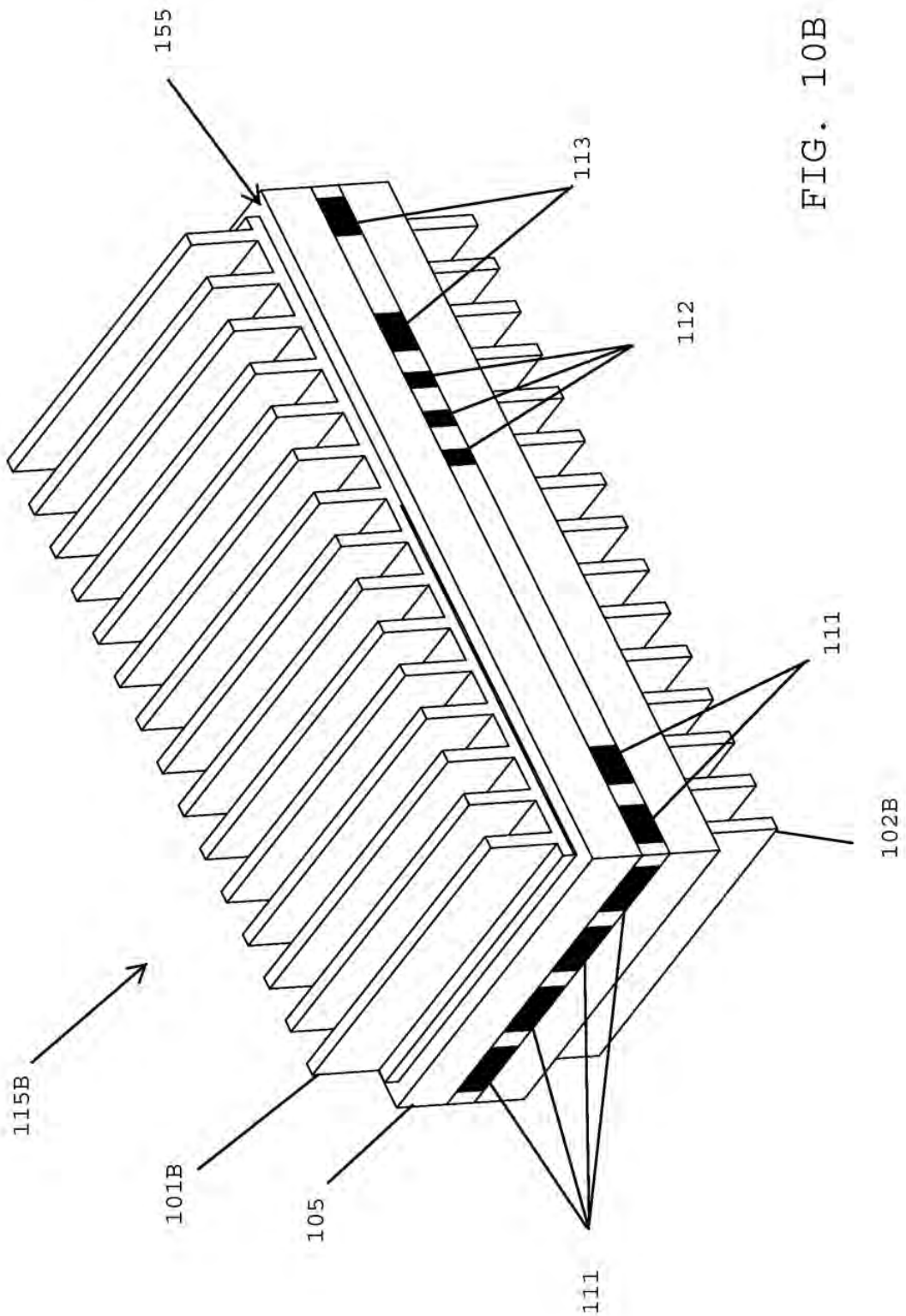


FIG. 10B

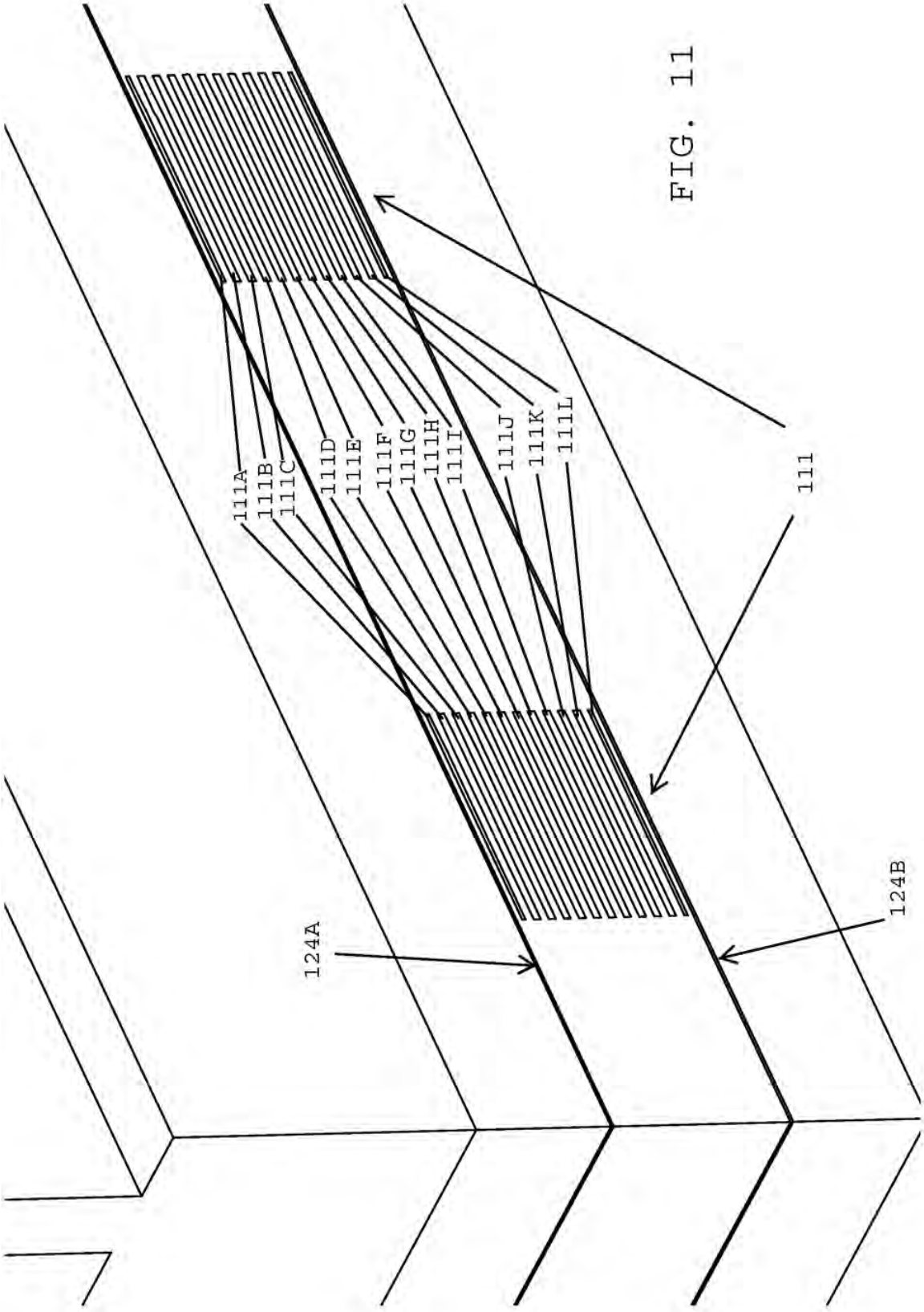

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FIG. 11

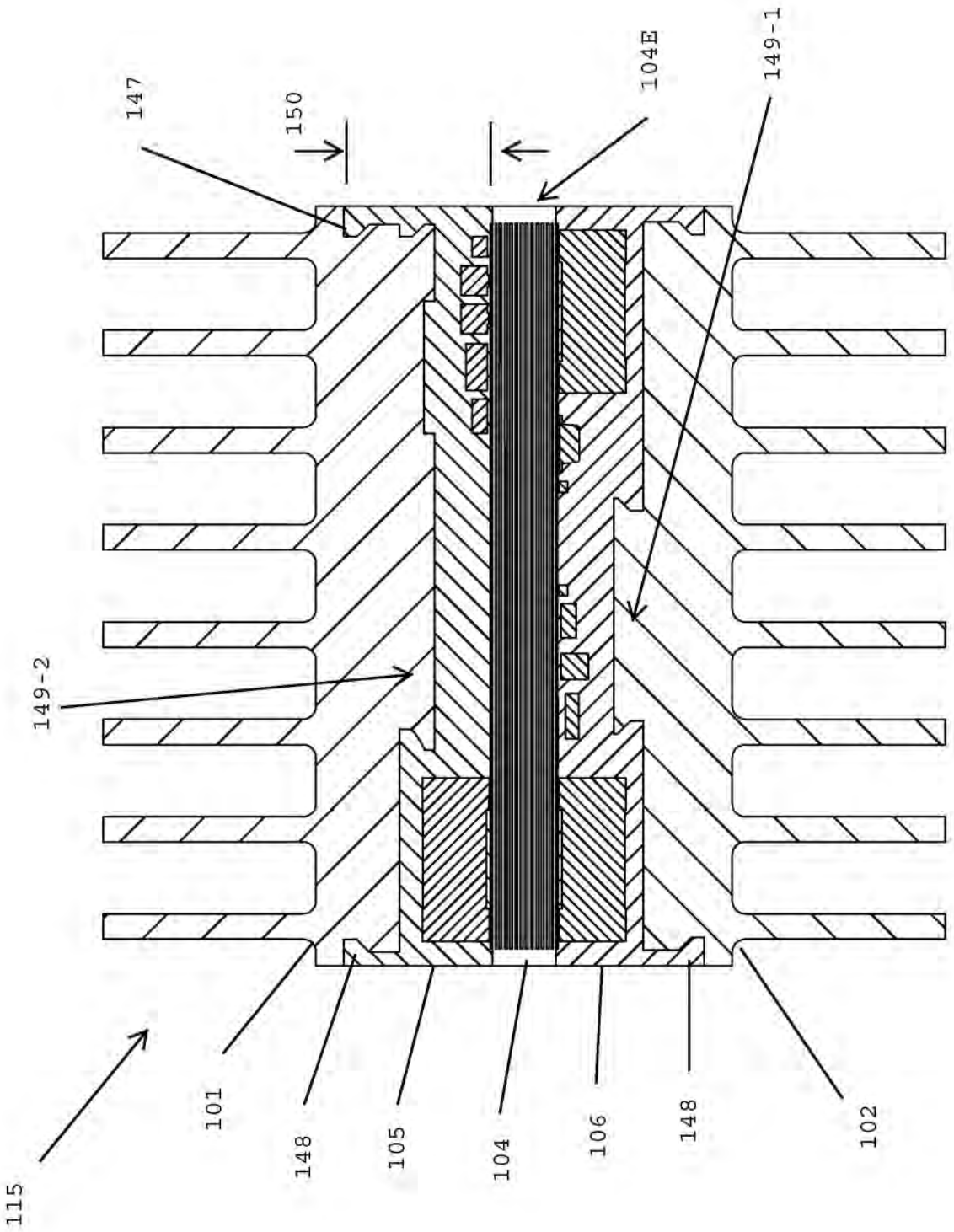


FIG. 12

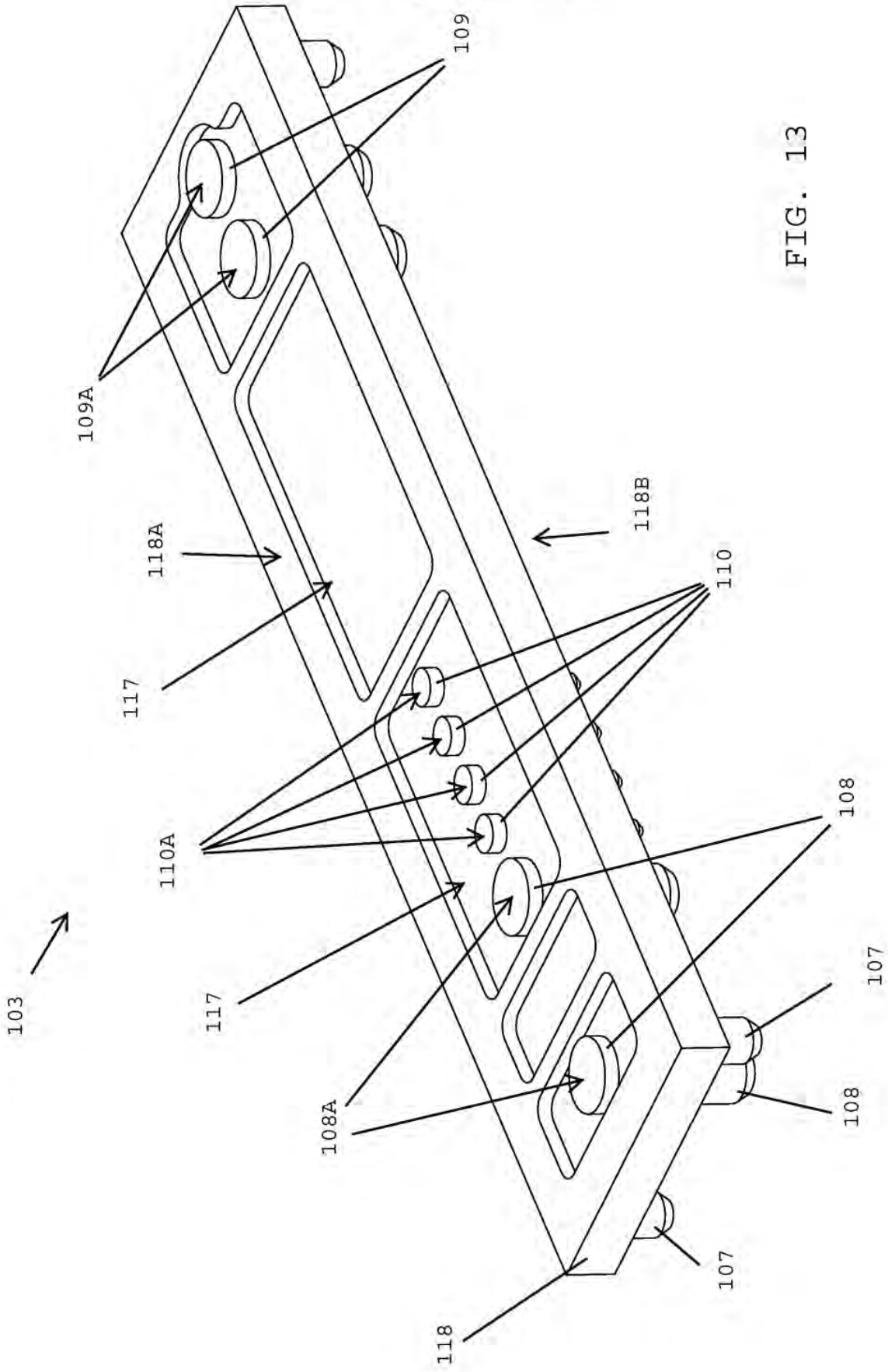

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FIG. 13

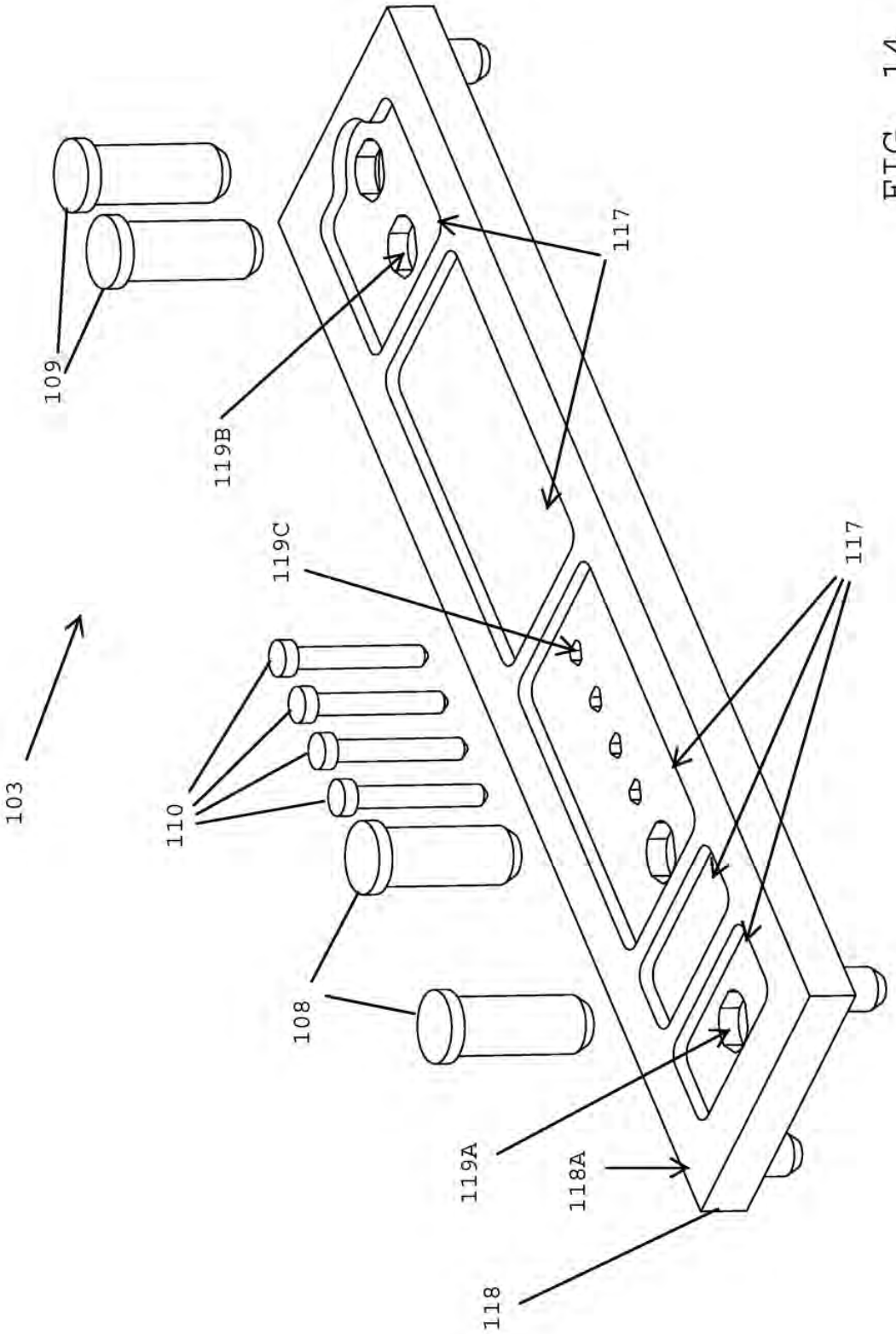


FIG. 14

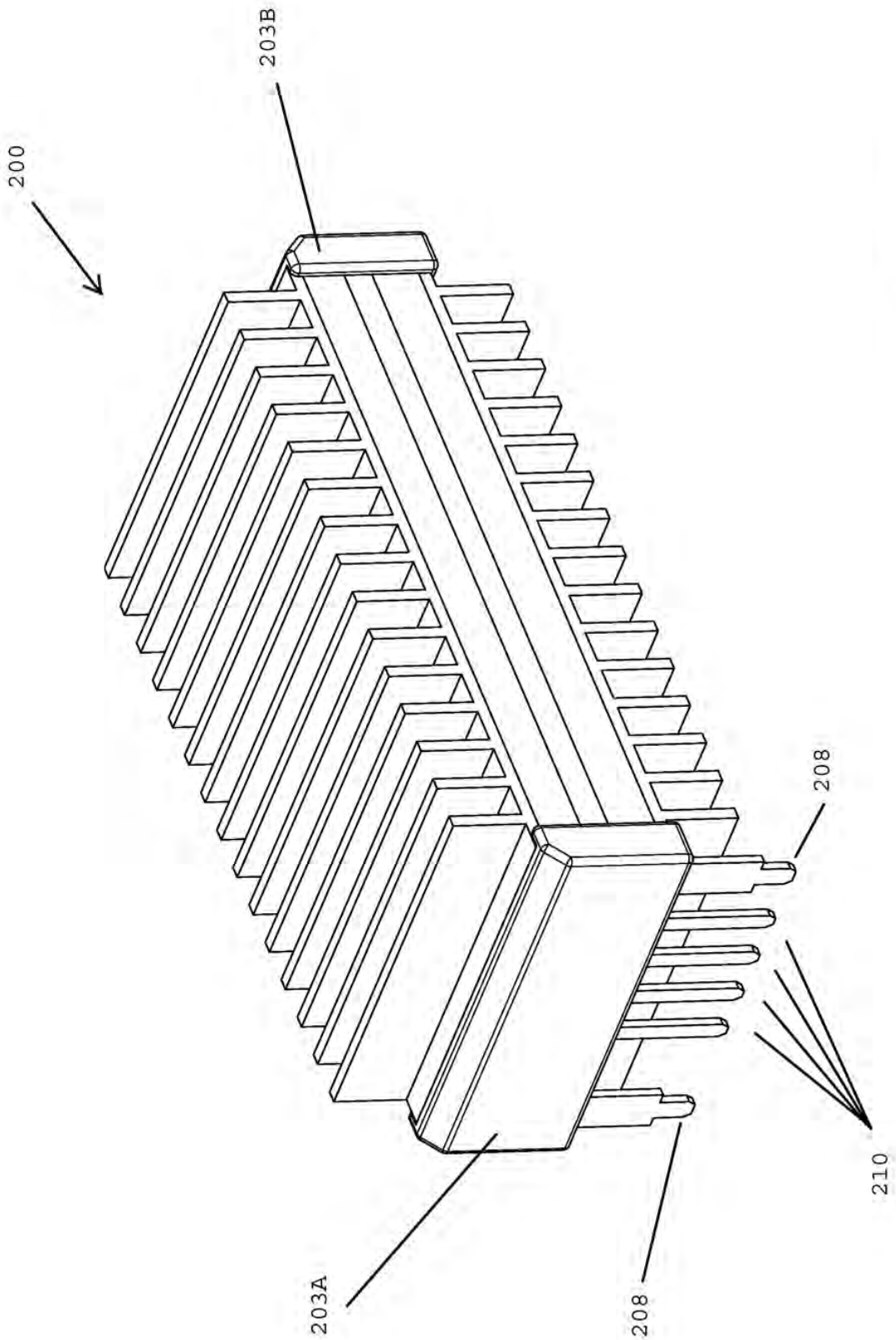


FIG. 15

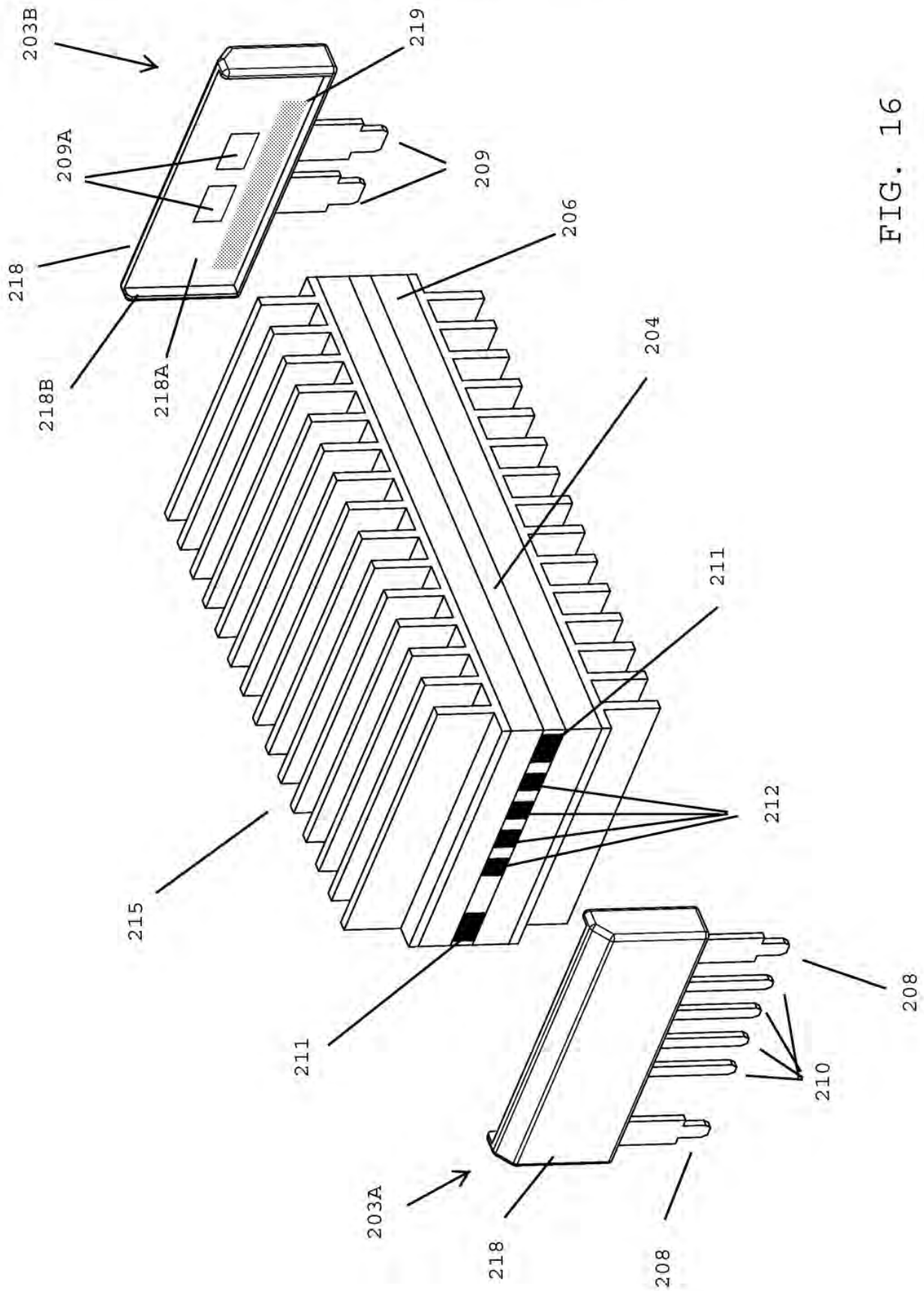

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FIG. 16

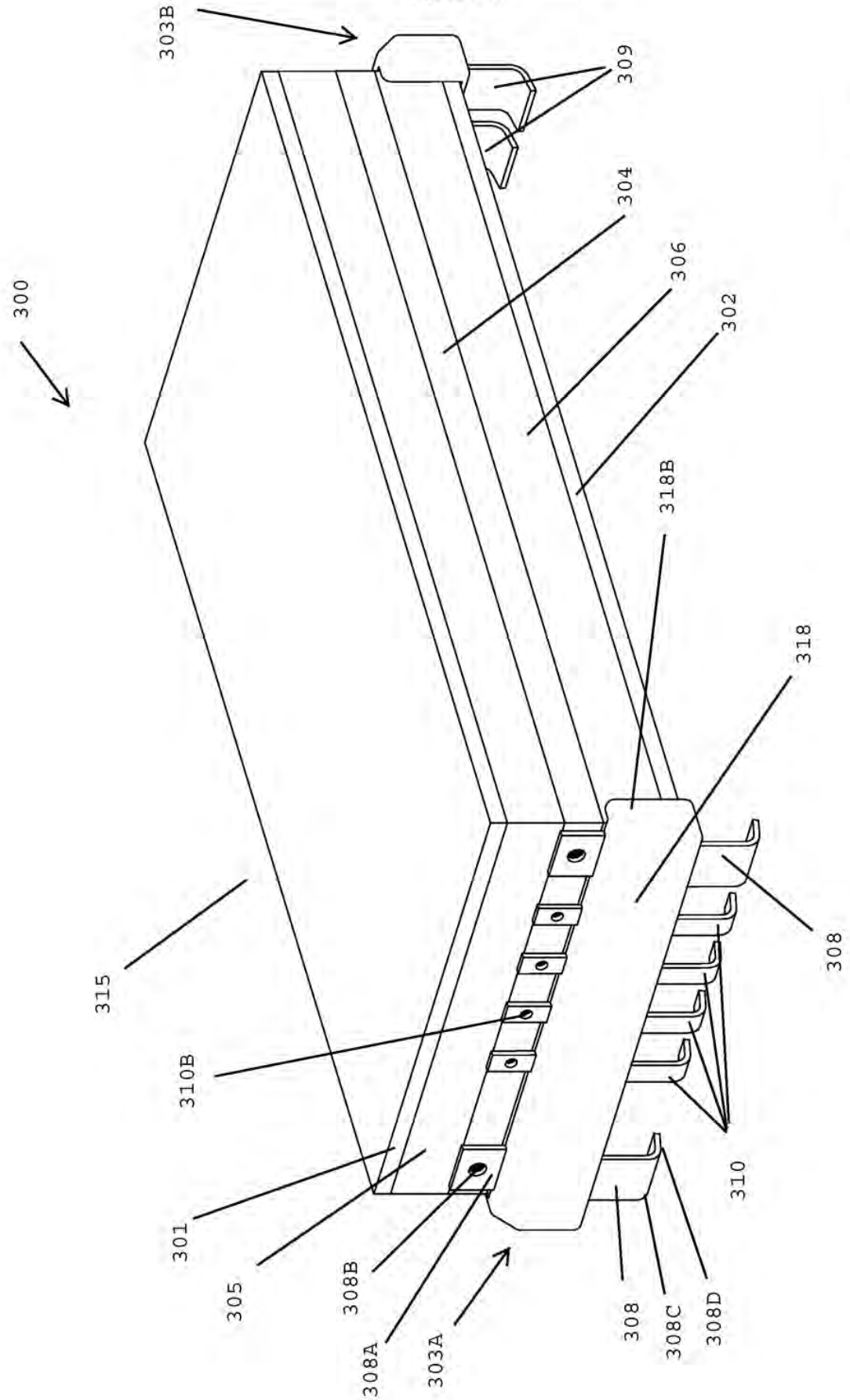

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FIG. 17

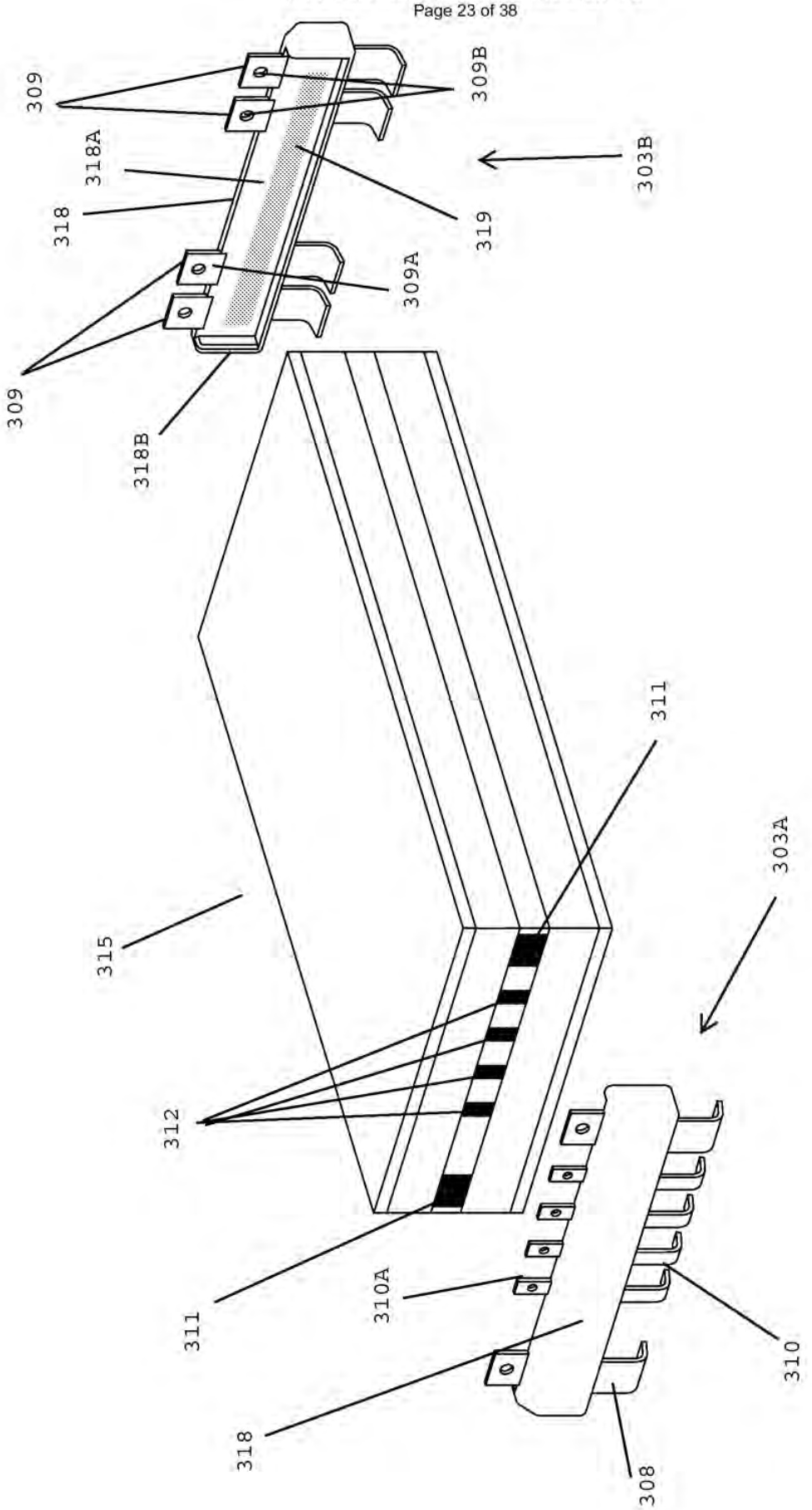

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FIG. 18

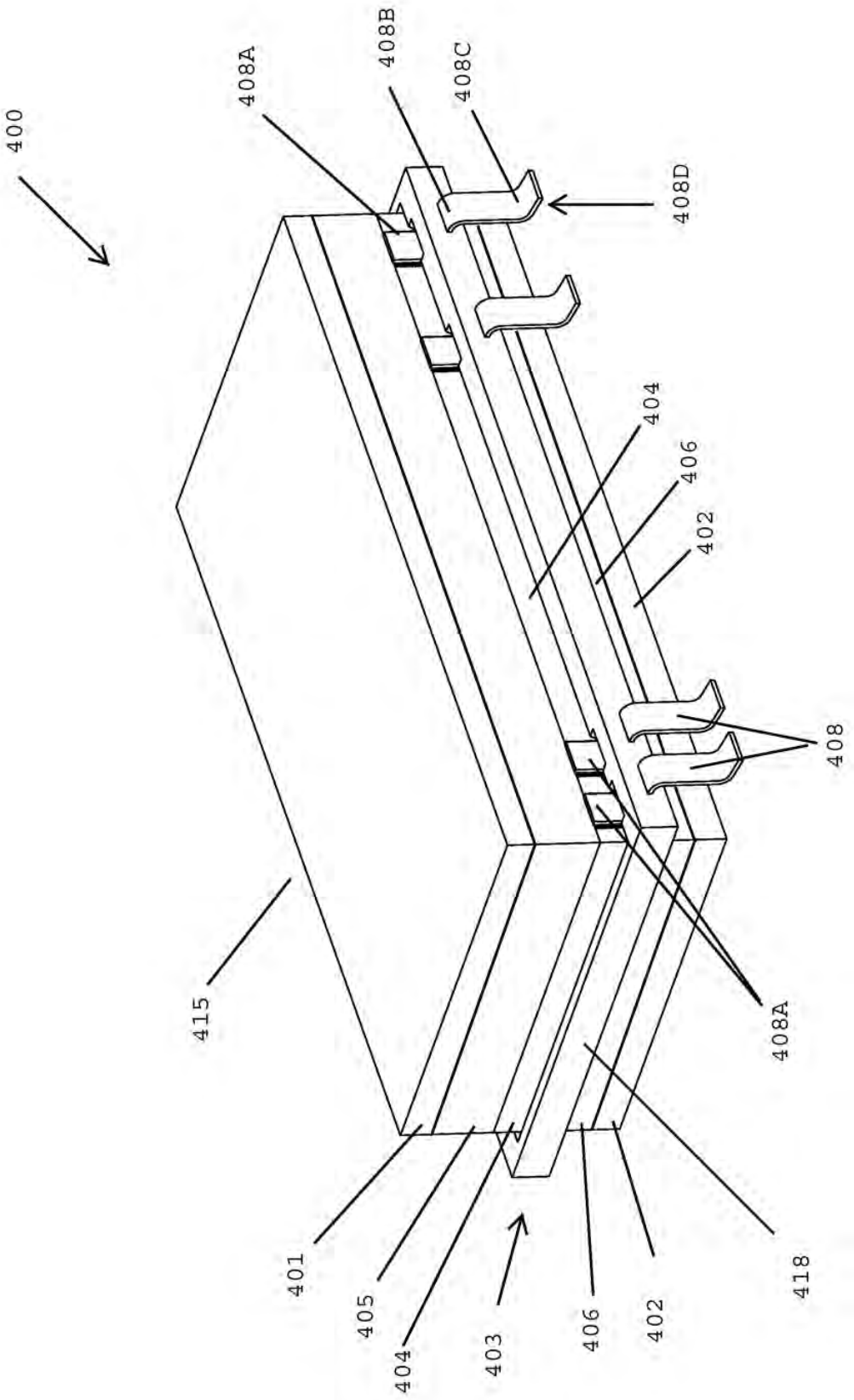

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FIG. 19

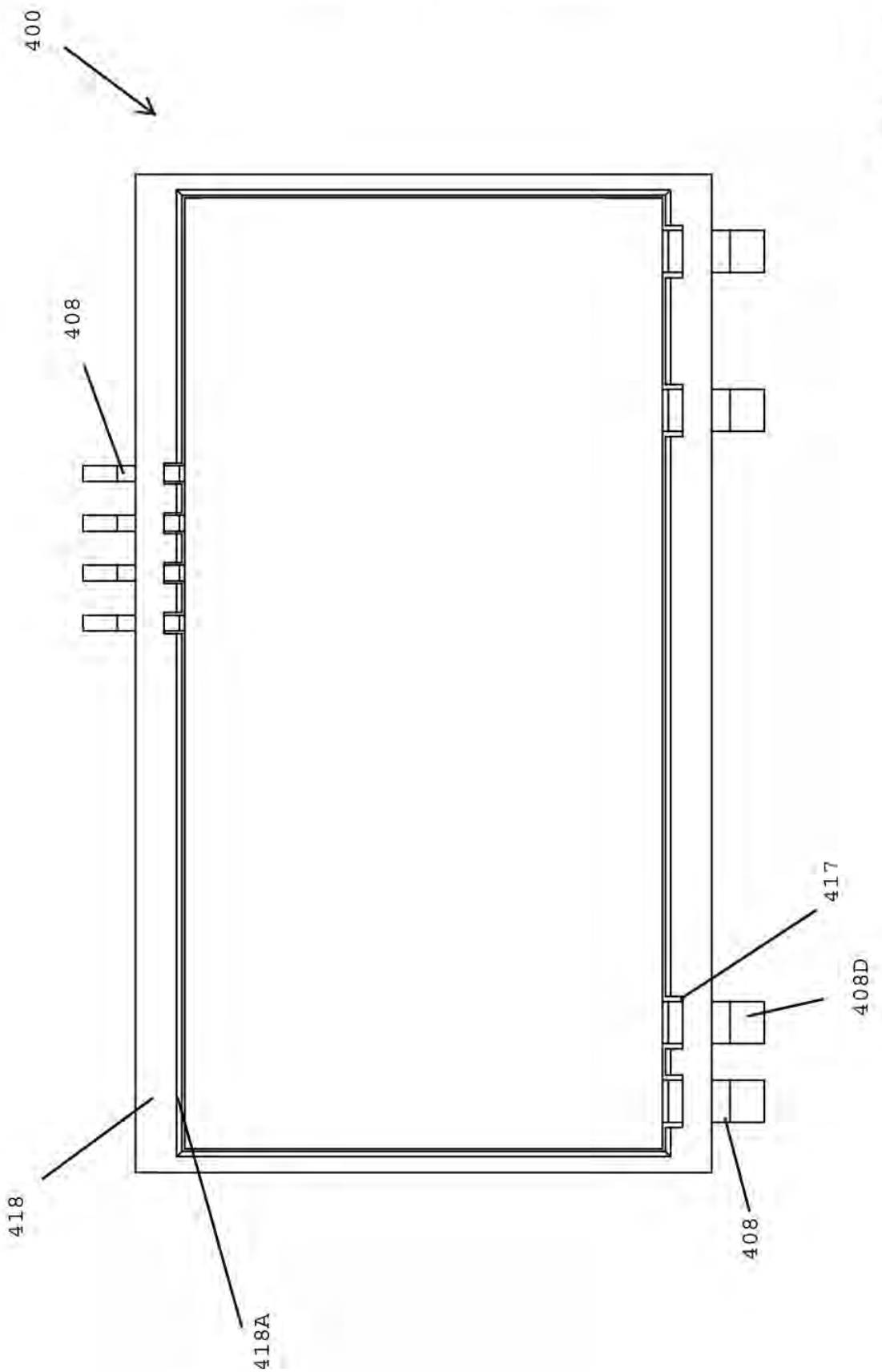


FIG. 20

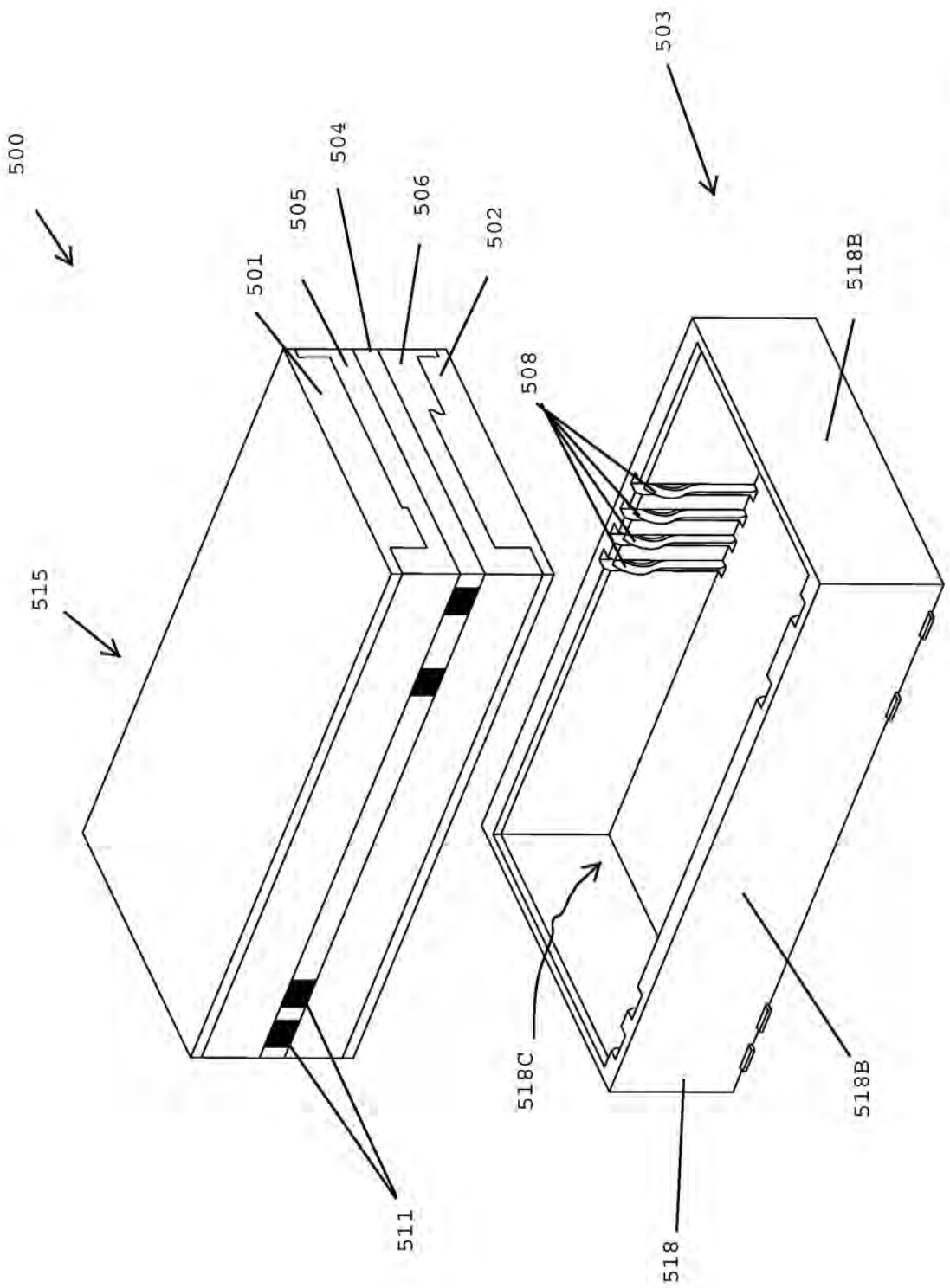


FIG. 21

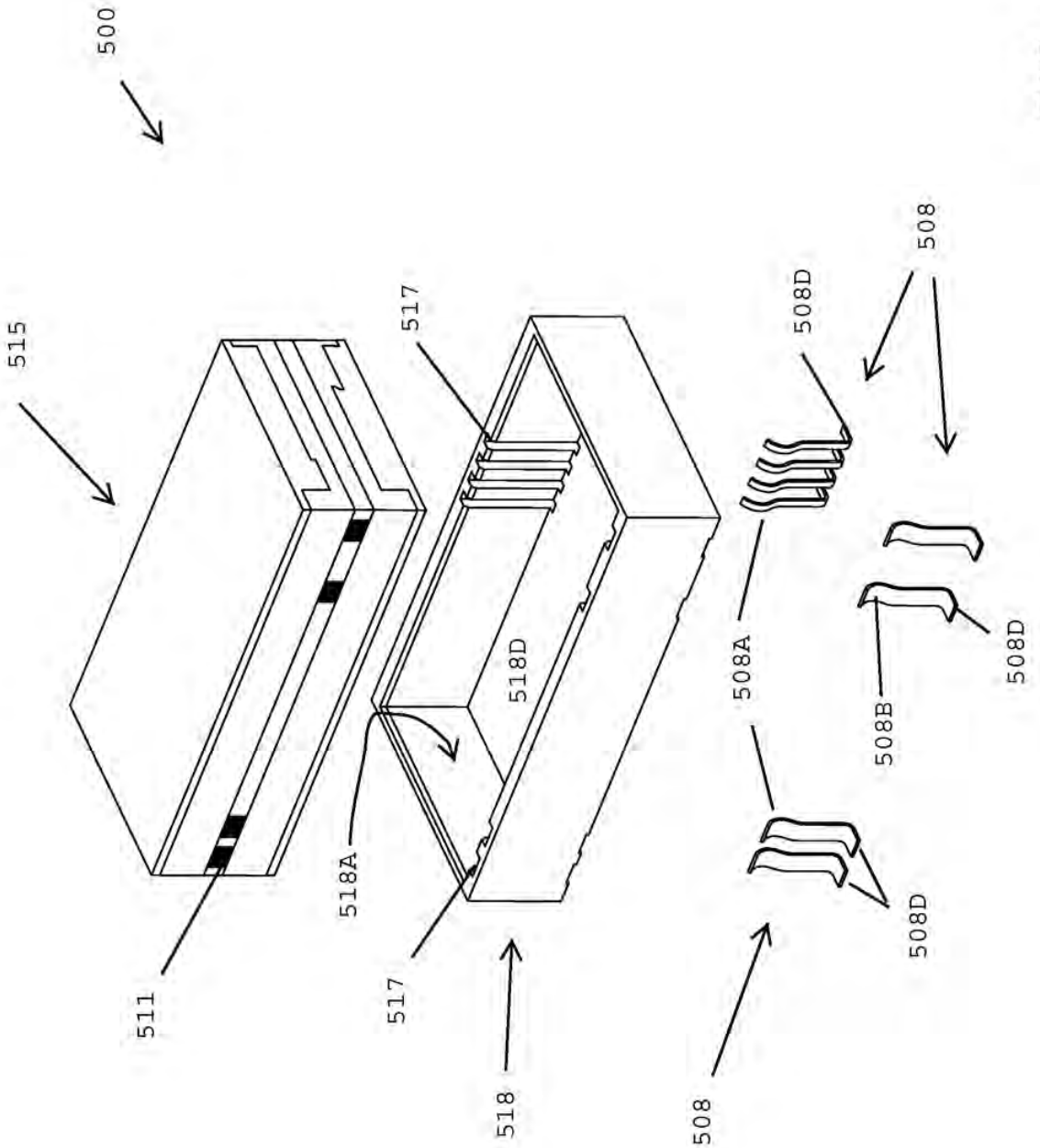

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FIG. 22

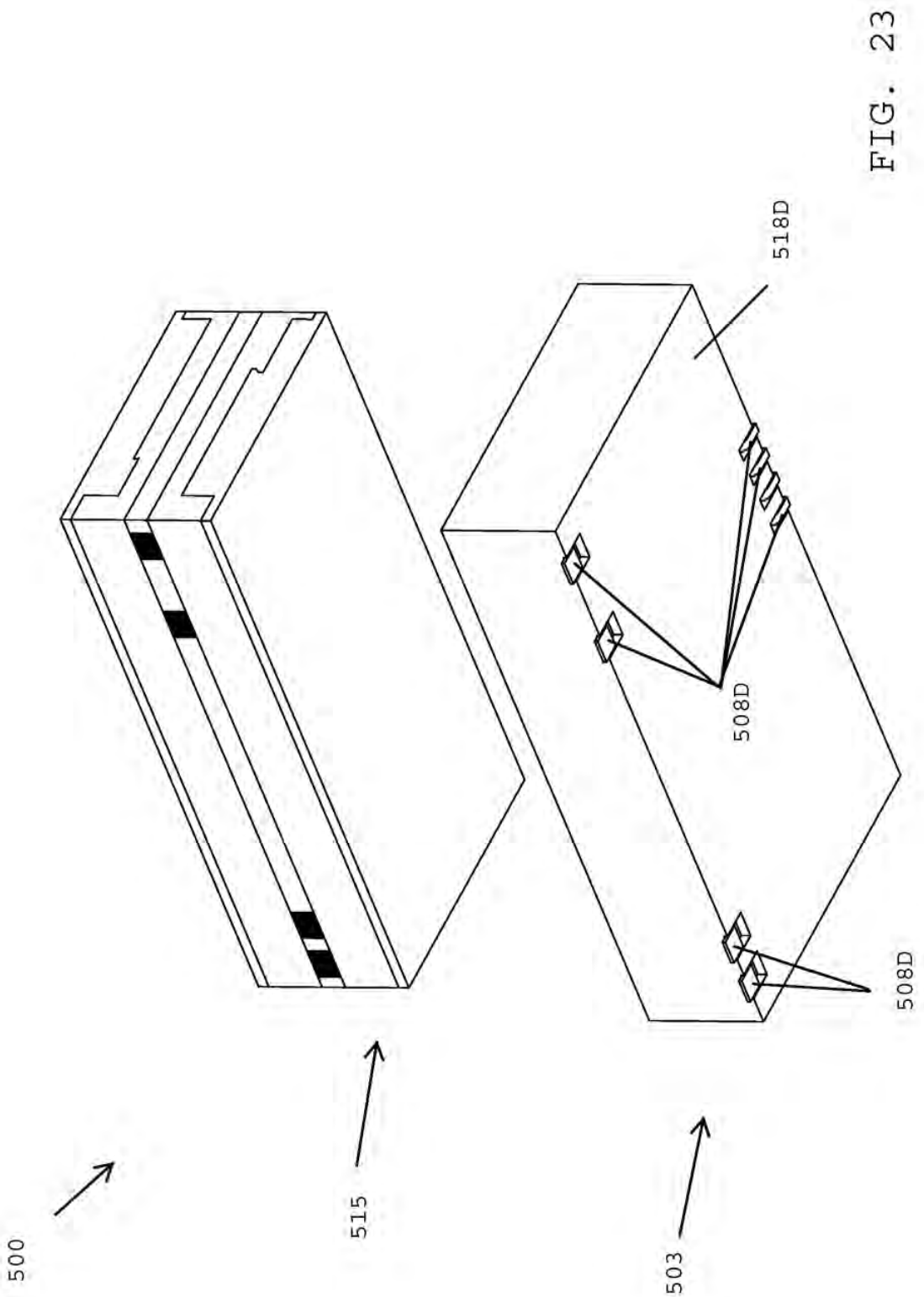


FIG. 23

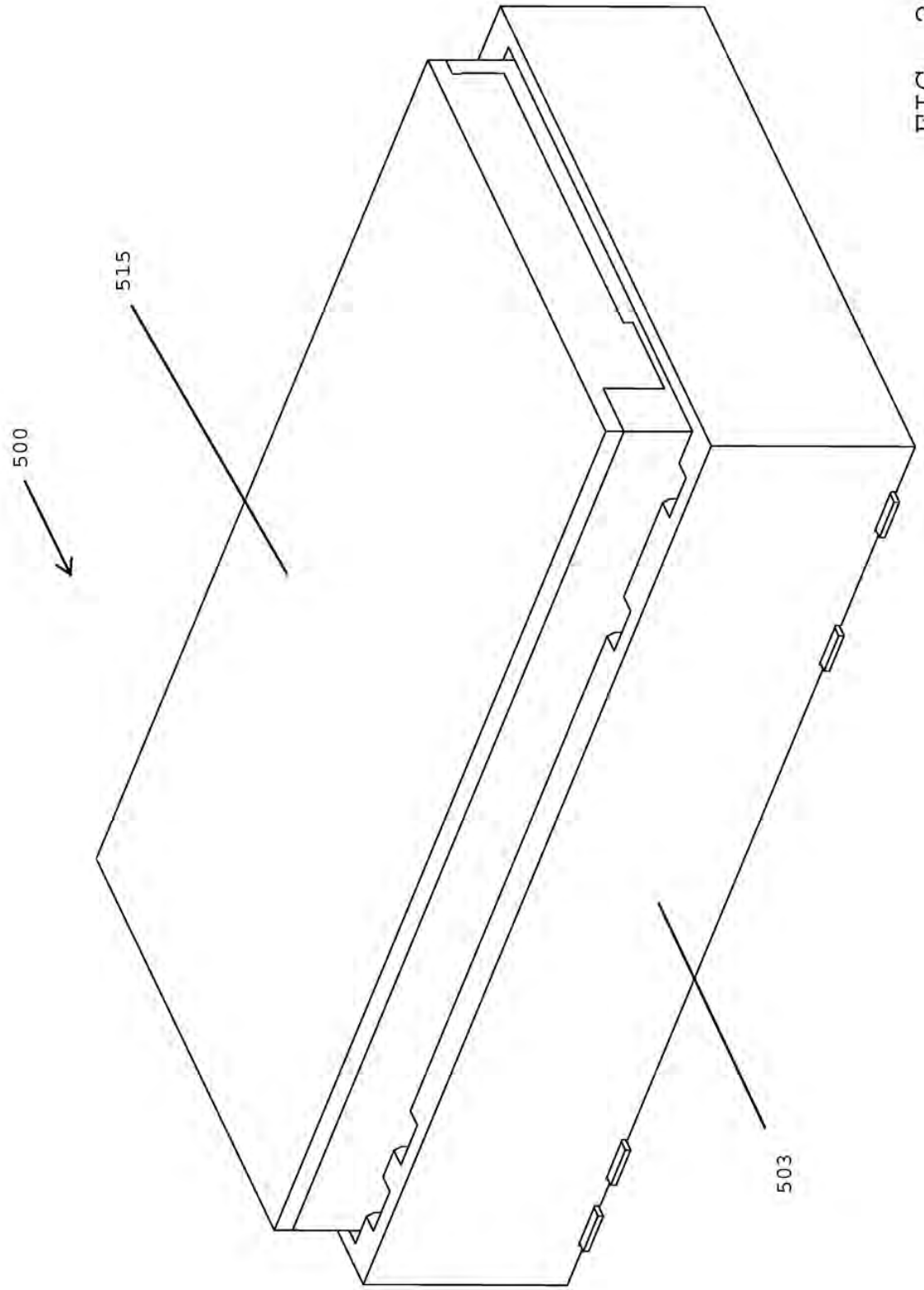


FIG. 24

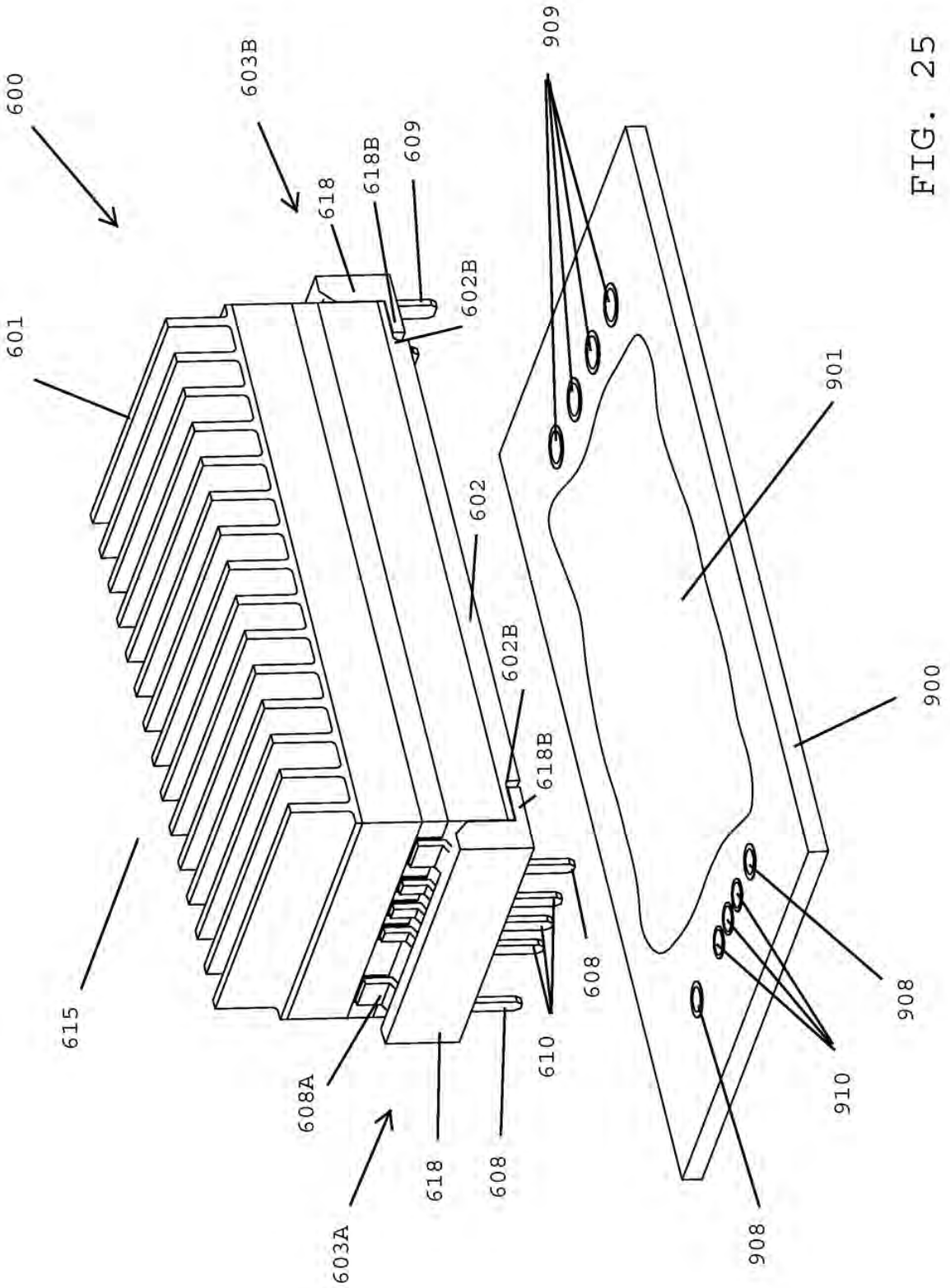

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FIG. 25

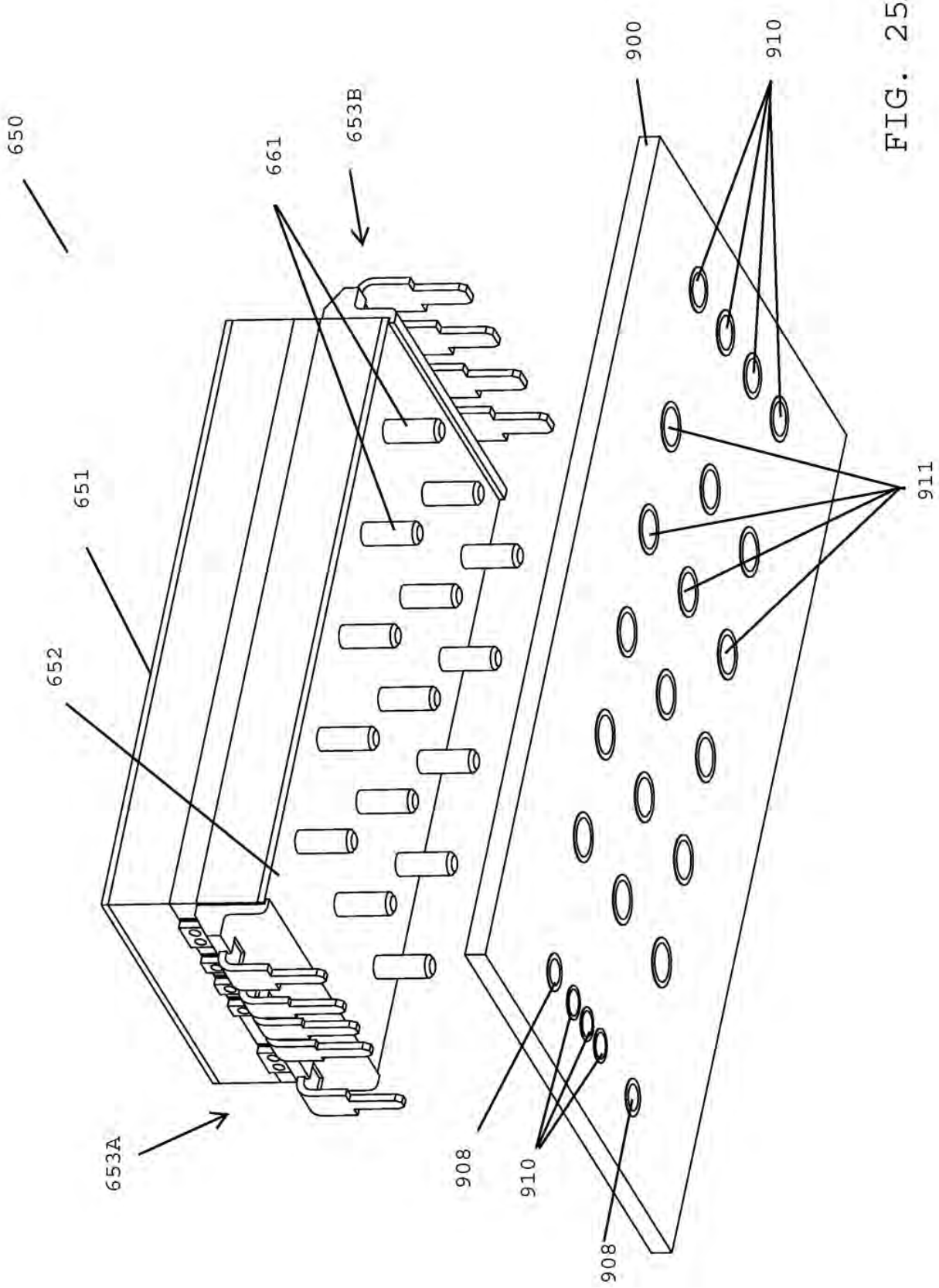


FIG. 25A

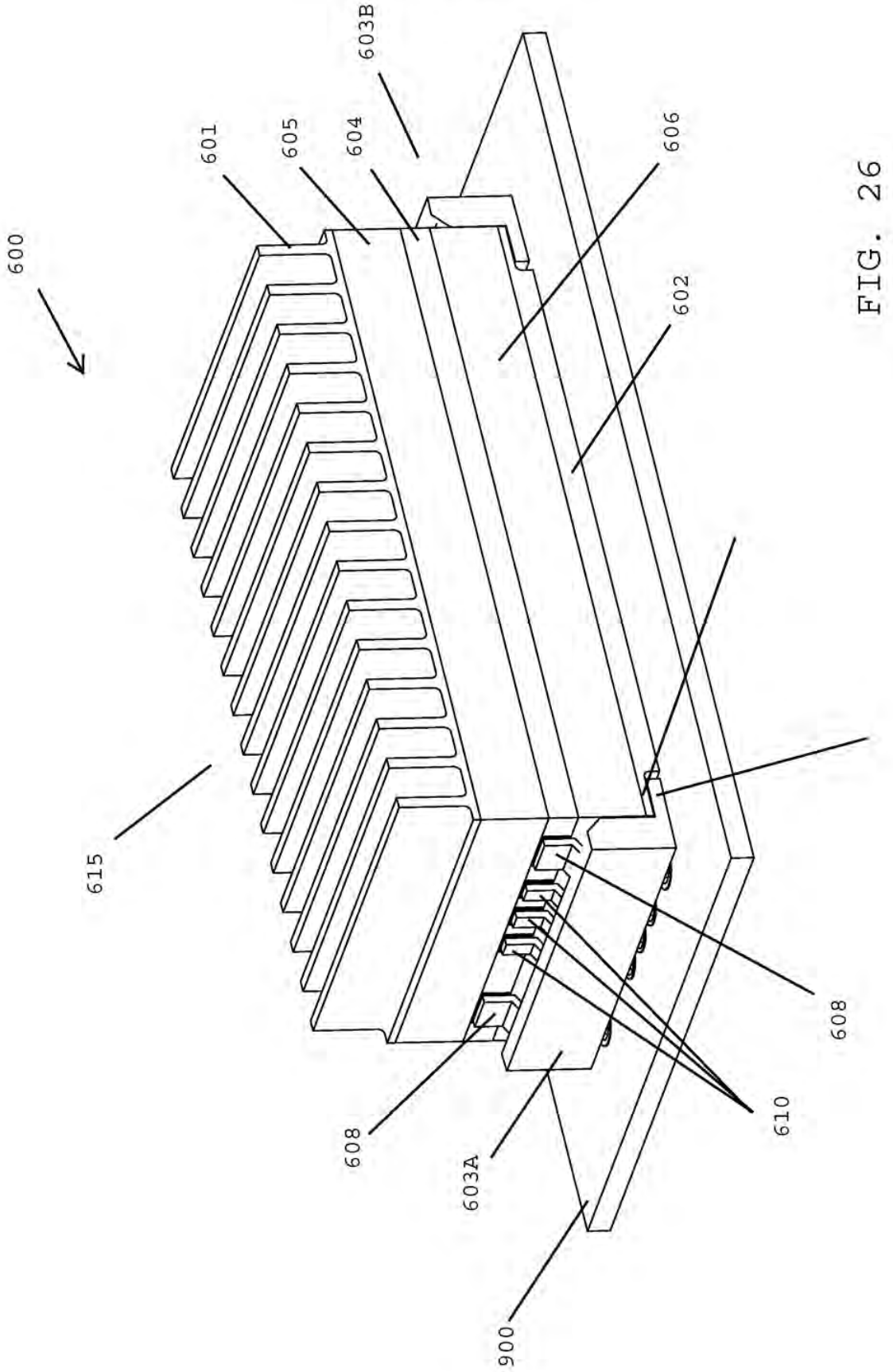


FIG. 26

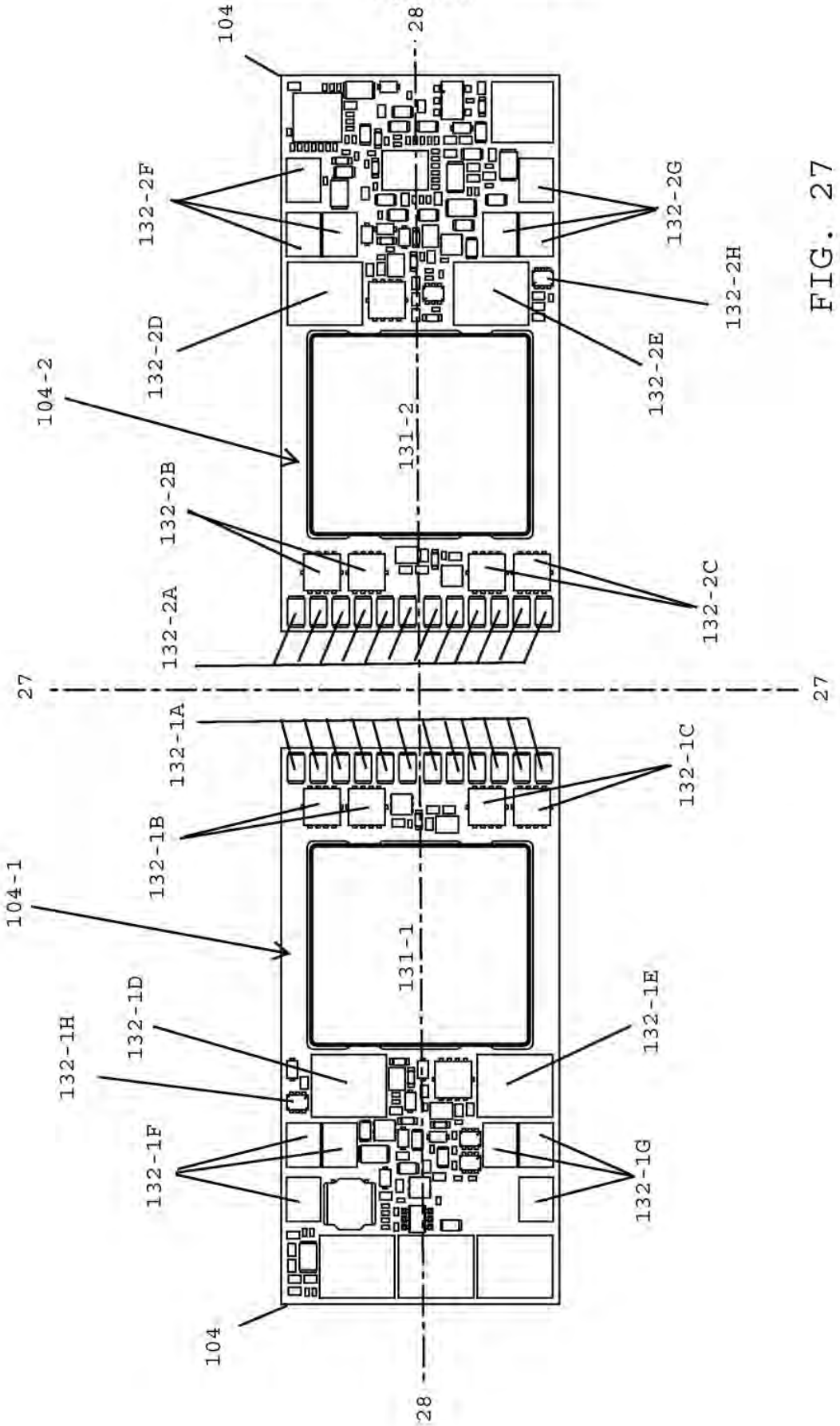

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FIG. 27

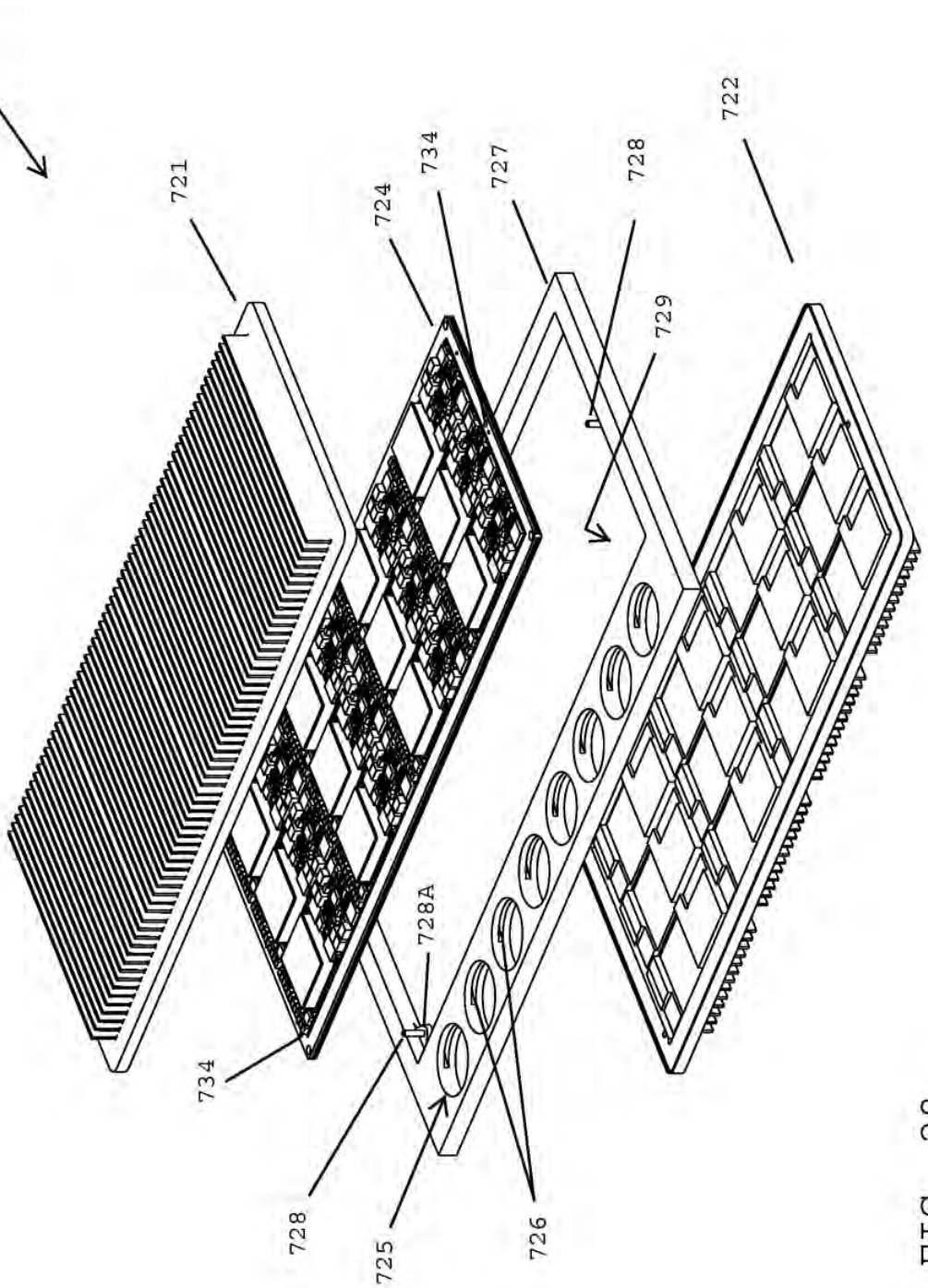


FIG. 28

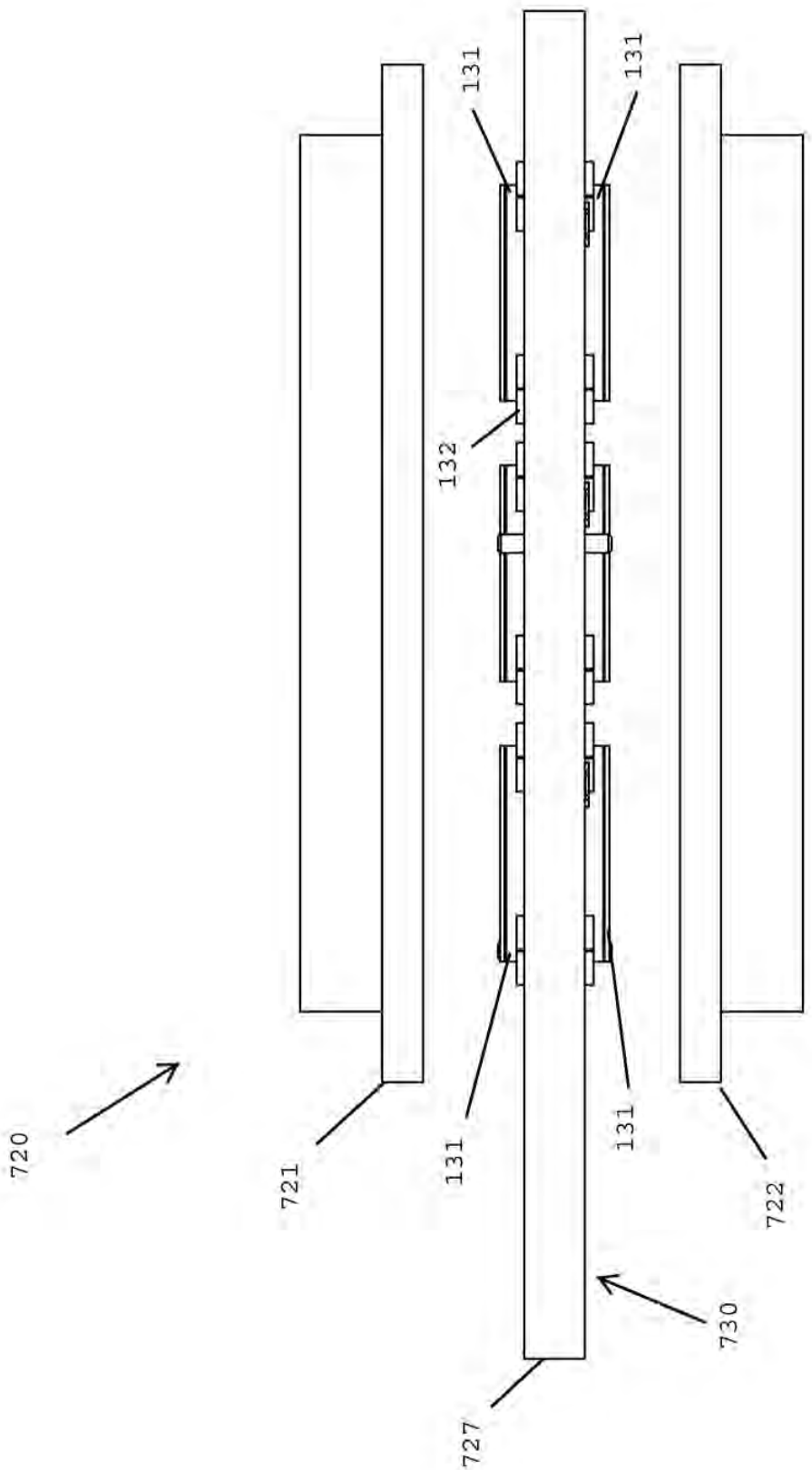


FIG. 29

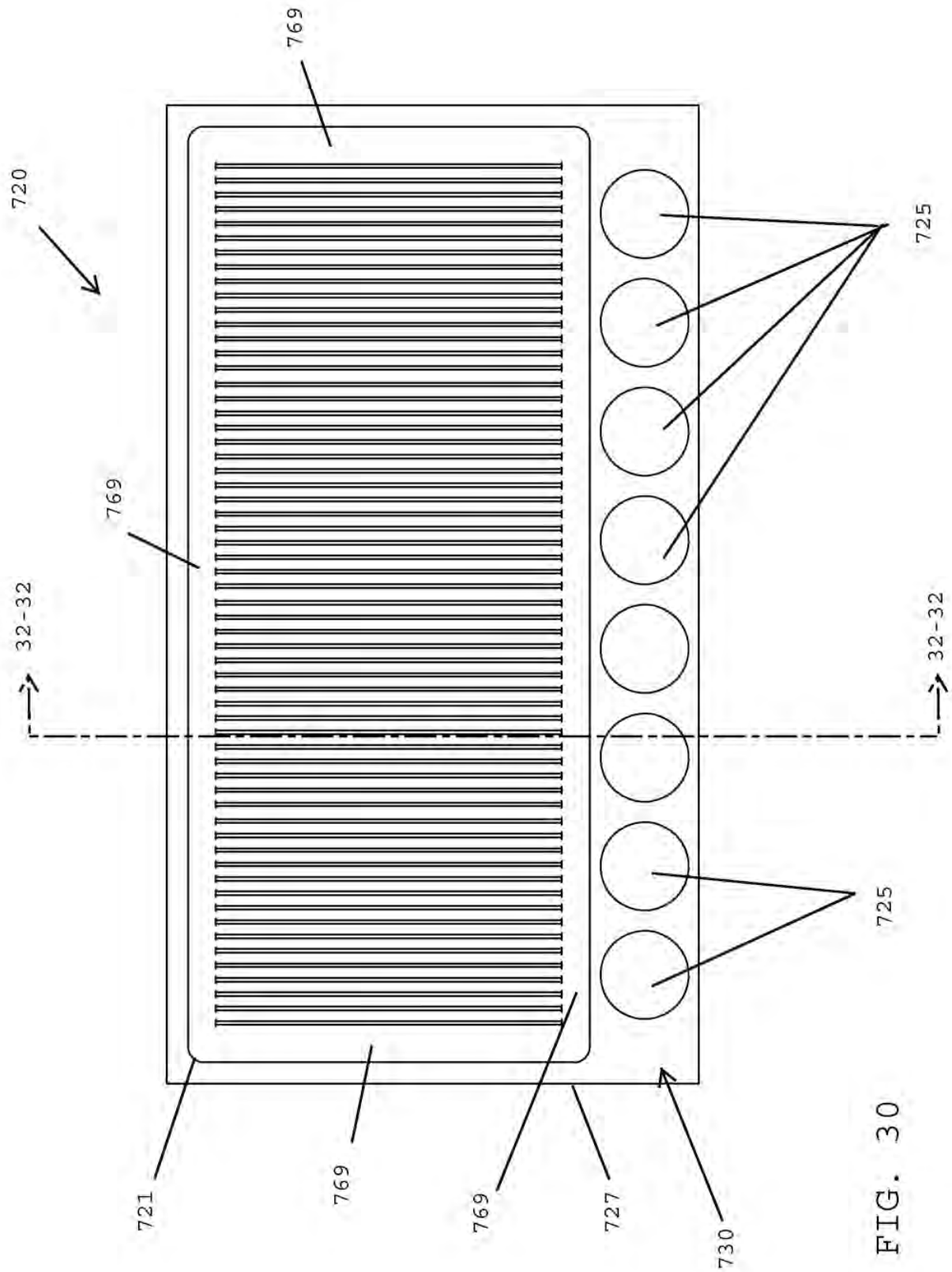


FIG. 30

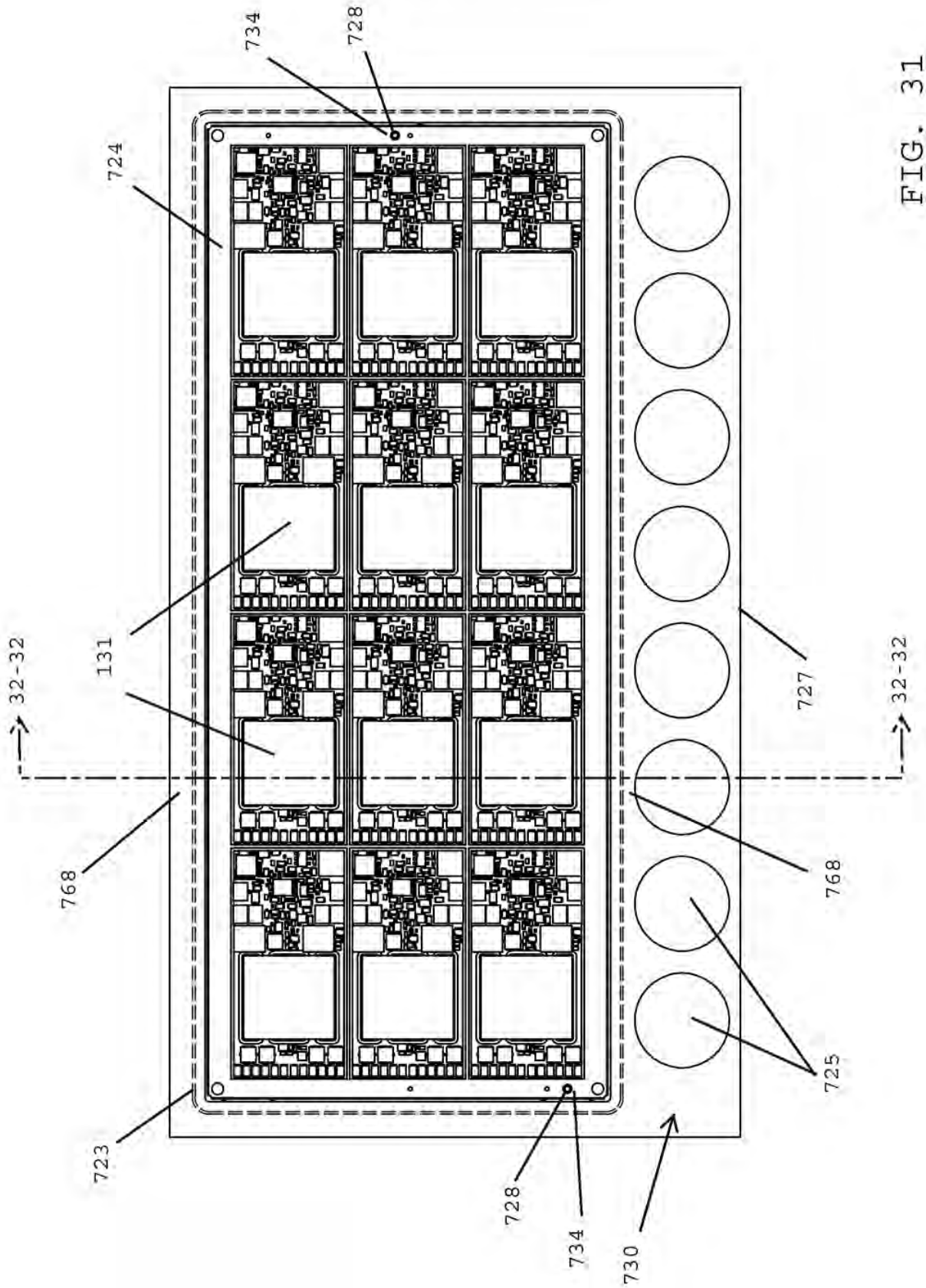


FIG. 31

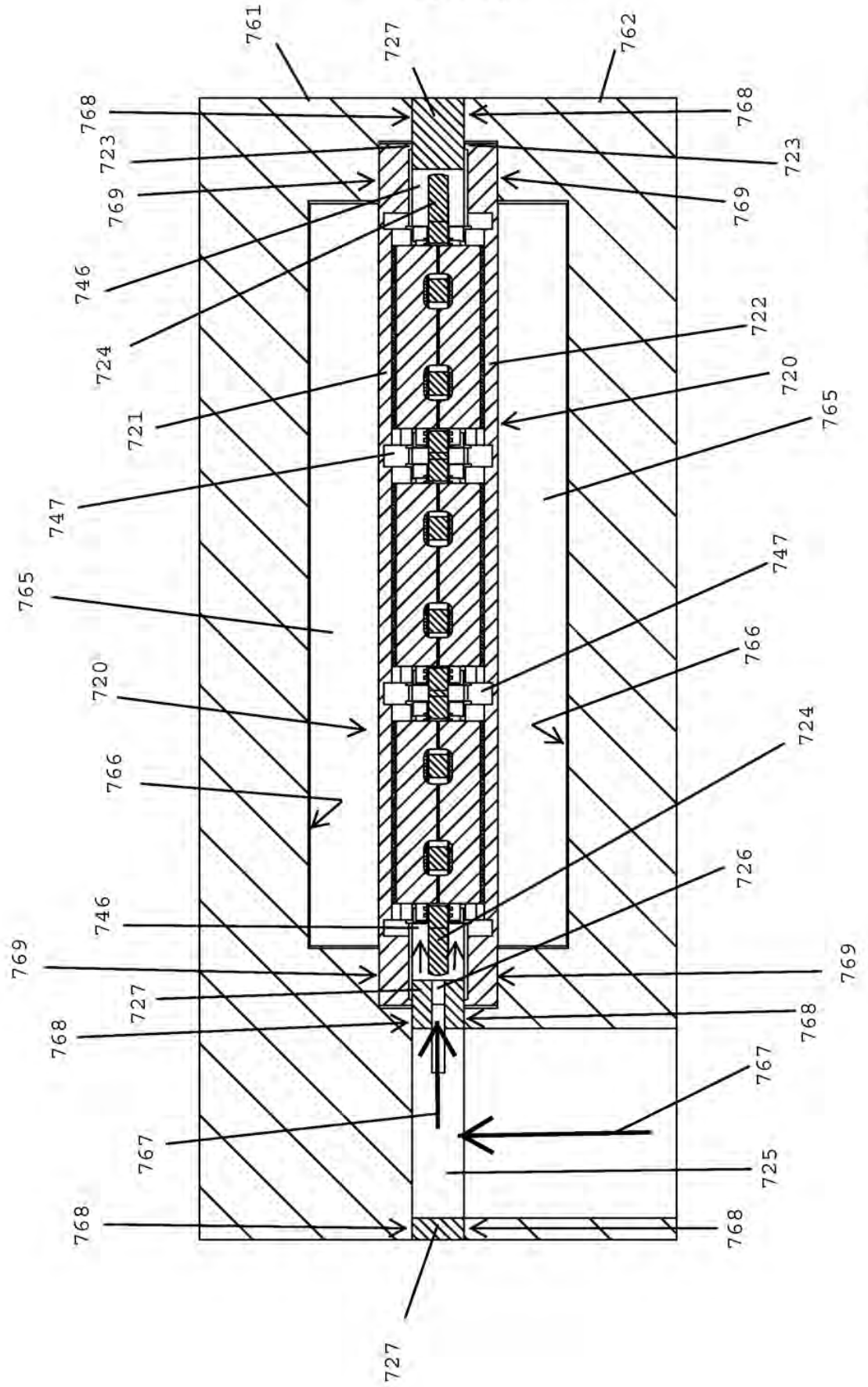

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FIG. 32

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	PANEL-MOLDED ELECTRONIC ASSEMBLIES
First Named Inventor/Applicant Name:	Patrizio Vinciarelli
Filer:	Rex I. Huang/Paul Micele
Attorney Docket Number:	00614-0168003

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Claims in Excess of 20	1202	74	80	5920
Independent claims in excess of 3	1201	3	420	1260
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Late Filing Fee for Oath or Declaration	1051	1	140	140
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**8920**

Electronic Acknowledgement Receipt	
EFS ID:	21636070
Application Number:	14635467
International Application Number:	
Confirmation Number:	1058
Title of Invention:	PANEL-MOLDED ELECTRONIC ASSEMBLIES
First Named Inventor/Applicant Name:	Patrizio Vinciarelli
Customer Number:	26214
Filer:	Rex I. Huang/Devon Weide
Filer Authorized By:	Rex I. Huang
Attorney Docket Number:	00614-0168003
Receipt Date:	02-MAR-2015
Filing Date:	
Time Stamp:	15:52:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$8920
RAM confirmation Number	2985
Deposit Account	061050
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	PAP.pdf	97784 1d917180a5d2cae6ec6c1f0f935cde69090 1fd0	no	2
Warnings:					
Information:					
2	Application Data Sheet	ADS.pdf	1561417 9b1c76088e90d01694fd0e08aa58be0f66723 1349	no	8
Warnings:					
Information:					
3		IDS.pdf	121284 bc03a14f1442a2533cea529967b1916ed155 612c	yes	2

Multipart Description/PDF files in .zip description

Document Description	Start	End
Transmittal Letter	1	1
Information Disclosure Statement (IDS) Form (SB08)	2	2

Warnings:					
Information:					
4		PrelimAmend.pdf	112475 9aa18b6875be799ed68cf6231029bb8b9b 44af9a	yes	18

Multipart Description/PDF files in .zip description

Document Description	Start	End
Preliminary Amendment	1	1
Specification	2	2
Claims	3	17
Applicant Arguments/Remarks Made in an Amendment	18	18

Warnings:

Information:					
5		Application.pdf	337659 36ac0d11a2bf2cd68475b1c037bd3197389e04f0	yes	65

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	42
	Claims	43	64
	Abstract	65	65

Warnings:					
Information:					
6	Drawings-only black and white line drawings	Figures.pdf	1569484 c7492fa1faa7d19e3c0e771c5d9a3db0da1b253a	no	38
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Information:					
		Total Files Size (in bytes):	3840338		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DocCode - SCORE

SCORE Placeholder Sheet for IFW Content

Application Number: 14635467 Document Date: 03/02/2015

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

- Drawings – Other than Black and White Line Drawings

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

To access the documents in the SCORE database, refer to instructions below.

At the time of document entry (noted above):

- Examiners may access SCORE content via the eDAN interface.
- Other USPTO employees can bookmark the current SCORE URL (http://Score.uspto.gov/ScoreAccessWeb/).
- External customers may access SCORE content via the Public and Private PAIR interfaces.

Form Revision Date: September 30, 2013

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/635,467	Filing Date 03/02/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 03/02/2015

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 94	Minus	** 94	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 6	Minus	***6	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/CORALIA BETANCOURT/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date
14/635,467	03/02/2015

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 26214

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☐ The address associated with the above-mentioned Customer Number

OR

☑ The address associated with Customer Number: 26214

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

VLT, Inc.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	Mar. 3, 2015
Name	Andrew D'Amico		
Title	V.P., Intellectual Property		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	21745517
Application Number:	14635467
International Application Number:	
Confirmation Number:	1058
Title of Invention:	PANEL-MOLDED ELECTRONIC ASSEMBLIES
First Named Inventor/Applicant Name:	Patrizio Vinciarelli
Customer Number:	26214
Filer:	Rex I. Huang/Paul Micele
Filer Authorized By:	Rex I. Huang
Attorney Docket Number:	00614-0168003
Receipt Date:	12-MAR-2015
Filing Date:	
Time Stamp:	09:28:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		168003POA.pdf	189258 286e863a8604148 1a57a72bb593acaa2950 2589f	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	1
	Power of Attorney	2	2
Warnings:			
Information:			
	Total Files Size (in bytes):	189258	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	14/635,467
Filing Date	03/02/2015
First Named Inventor	Patrizio Vinciarelli
Title	PANEL-MOLDED ELECTRONIC ASSEMBLIES
Art Unit	
Examiner Name	
Attorney Docket Number	00614-0168003

SIGNATURE of Applicant or Patent Practitioner

Signature	/Rex I. Huang/	Date (Optional)	2015-03-12
Name	Rex I. Huang	Registration Number	57661
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/635,467	03/02/2015	1742	8920	00614-0168003	94	6

CONFIRMATION NO. 1058

26214
FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

FILING RECEIPT



Date Mailed: 03/19/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Patrizio Vinciarelli, Boston, MA;
Michael B. LaFleur, East Hampstead, NH;
Sean Timothy Fleming, Worcester, MA;
Rudolph F. Mutter, North Andover, MA;
Andrew T. D'Amico, Beverly Hills, CA;

Applicant(s)

VLT, Inc., Sunnyvale, CA

Power of Attorney: The patent practitioners associated with Customer Number 26214

Domestic Priority data as claimed by applicant

This application is a DIV of 13/105,696 05/11/2011 PAT 8966747

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 03/16/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/635,467**

Projected Publication Date: 06/25/2015

Non-Publication Request: No

Early Publication Request: No

Title

PANEL-MOLDED ELECTRONIC ASSEMBLIES

Preliminary Class

264

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/635,467	03/02/2015	Patrizio Vinciarelli	00614-0168003

CONFIRMATION NO. 1058

26214
FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

NOTICE



Date Mailed: 03/19/2015

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Patrizio Vinciarelli
  Michael B. LaFleur
  Sean Timothy Fleming
  Rudolph F. Mutter
  Andrew T. D'Amico

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/635,467

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	94 minus 20 =	* 74			OR	x 80 =	5920
INDEPENDENT CLAIMS (37 CFR 1.16(h))	6 minus 3 =	* 3				x 420 =	1260
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	8780

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor	:	Patrizio Vinciarelli	Art Unit	:	Unknown
Serial No.	:	14/635,467	Examiner	:	Unknown
Filed	:	March 2, 2015	Conf. No.	:	1058

Title : PANEL-MOLDED ELECTRONIC ASSEMBLIES

MAIL STOP MISSING PARTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO INFORMATIONAL NOTICE TO APPLICANT

In response to the Informational Notice to Applicant dated March 19, 2015, applicant as a large entity submits herewith the following:

☒ Declaration in compliance with 37 CFR §1.63.

Please apply any necessary charges or credits to Deposit Account 06 1050, referencing the above attorney docket number.

Respectfully submitted,

Date: April 3, 2015_____

/Rex I. Huang/_____
Rex I. Huang
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	PANEL-MOLDED ELECTRONIC ASSEMBLIES

As the below named inventor, I hereby declare that:

This declaration is directed to: [X] The attached application, or

[ ] United States application or PCT international application number 14/635,467

filed on March 2, 2015.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: Patrizio Vinciarelli Date (Optional): March 5, 2015

Signature:

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Michael B. LaFleur Date (Optional): March 2, 2015

Signature:

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LEGAL NAME OF INVENTOR

Inventor: Sean Timothy Fleming Date (Optional): 3/5/13

Signature:

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LEGAL NAME OF INVENTOR

Inventor: Rudolph F. Mutter Date (Optional): 3/5/15

Signature:

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LEGAL NAME OF INVENTOR

Inventor: Andrew T. D'Amico Date (Optional): March 3, 2015

Signature:

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PANEL-MOLDED ELECTRONIC ASSEMBLIES

FIELD OF THE INVENTION

[001] This invention relates to the field of encapsulating electronic assemblies and more particularly to encapsulated power converters.

BACKGROUND

[002] Contemporary electronic power systems require power converters capable of deployment at the point of load. Competing considerations require increasing power density, decreasing mounting area on customer motherboard, and lower cost.

[003] An encapsulated electronic module, such as an electronic power converter module for example, may comprise a printed circuit assembly over-molded with an encapsulant to form some or all of the package and exterior structure or surfaces of the module. Encapsulation in this manner may aid in conducting heat out of the over-molded components, i.e., components that are mounted on the printed circuit assembly and covered with encapsulant. In the case of an electronic power converter module, the printed circuit assembly may include one or more inductive components, such as inductors and transformers. Encapsulated electronic power converters capable of being surface mount soldered to a customer motherboard are described in Vinciarelli et al., *Power Converter Package and Thermal Management*, U.S. Patent No. 7,361,844, issued Apr. 22, 2008, (the "SAC Package Patent") (assigned to VLT, inc. of Sunnyvale, CA, the entire disclosure of which is incorporated herein by reference). Encapsulated electronic modules having at least one surface of a magnetic core structure exposed and methods for manufacturing the same are described in Vinciarelli et al., *Encapsulation Method and Apparatus for Electronic Modules*, U.S. Patent Application Ser. No.12/493,773, filed Jun. 29, 2009, (the "Exposed Core Application") (assigned to VI Chip Inc. of Andover, MA, the entire disclosure of which is incorporated herein by reference).

[004] Methods of over-molding both sides of a printed circuit board assembly while leaving opposing regions on both sides of the printed circuit board free of encapsulant are

described in Saxelby, et al., *Circuit Encapsulation Process,* U.S. Patent No. 5,728,600, issued Mar. 17, 1998 and Saxelby, et al., *Circuit Encapsulation*, U.S. Pat. No. 6,403,009, issued June 11, 2002 (collectively the "Molding Patents") (both assigned to VLT, Inc. of Sunnyvale, CA and incorporated by reference in their entirety).

[005] Leads for connecting the encapsulated power converter substrate to the customer motherboard are described in Vinciarelli et al., *Surface Mounting A Power Converter*, U.S. Patent No. 6,940,013, issued Sep. 6, 2005 (the "J-Lead Patent") (assigned to VLT, Inc. of Sunnyvale, CA, the entire disclosure of which is incorporated herein by reference).

SUMMARY

[006] In general, in one aspect, a method of making a plurality of electronic devices is provided. The method includes providing a plurality of mold panels, which when assembled, form an internal chamber; providing a substrate having a plurality of conductive traces and a plurality of components electrically connected to form at least one circuit, the substrate having at least one contact for making an electrical connection to the circuit; forming a panel assembly including the mold panels assembled with the substrate in the internal chamber and an encapsulant filling spaces between the substrate and interior surfaces of the chamber; curing the encapsulant; and cutting the panel assembly to expose at least a portion of the at least one contact and form a respective exposed contact.

[007] Implementations of the method may include one or more of the following features. The cutting can include making a first cut in at least one of the mold panels, and in the first cut, making a second narrower cut through the panel assembly. The curing can include raising the temperature of the panel assembly and the first cut is made before the panel assembly cools after the curing. The cutting can divide the panel assembly producing at least one module having a plurality of layers including respective portions of each of the panel molds, the substrate, and the encapsulant, and the module can contain the at least one circuit. The cutting can define at least one side of the module. The

cutting can defines two or more sides of the module. The method can further include treating the exposed contact to protect against oxidation. Treating the exposed contact can include applying a removable conformal coating to the exposed contact. Treating the exposed contact can include applying a layer of metal to the exposed contact. The metal applied to the exposed contact can include solder or a precious metal. Applying a layer of metal can include plating. The method can further include providing an adapter having at least one electrical terminal; and attaching the at least one electrical terminal to the exposed contact. The at least one contact can include a plurality of contacts; the module can include a plurality of exposed contacts; the adapter can have a plurality of electrical terminals arranged to match respective ones of the plurality of exposed contacts; and the adapter can be mechanically secured to the module. The mold panels can be metal. The respective portions of the mold panels can provide heat sink surfaces for the module. Contours can be provided in an internal surface of one or more of the mold panels. Providing the contours can include matching depths of portions of the internal surface to heights of one or more selected components. The selected components can include at least one magnetically permeable core and at least one semiconductor device. The traces and components can be electrically connected to form a plurality of separable circuits arranged in a pattern on the substrate; and the cutting can divide the panel assembly along spaces between the separable circuits into a plurality of modules each containing at least one respective circuit. The spaces between the separable circuits can have dimensions approximately matching a width of cuts produced by equipment used to cut the panel assembly. The at least one contact can include a plurality of contacts located in the spaces between the separable circuits. The plurality of contacts can be formed in the substrate. The plurality of contacts can be formed and buried below at least one surface of the substrate. The method can include treating at least one exterior surface of at least one of the mold panels for solderability. Forming the panel assembly can include dispensing encapsulant into a bottom panel mold; assembling the substrate into the bottom panel mold; dispensing encapsulant onto a top of the substrate; and assembling a top panel mold onto the substrate. The method can include centrifuging the assembly before curing the encapsulant. Forming the panel assembly can include assembling the substrate with a first substrate surface facing into a first panel mold, closing a second

panel mold onto the substrate covering a second substrate surface, providing one or more conduits to the internal chamber, and forcing encapsulant through the one or more conduits into the chamber. The method can further include centrifuging the assembly before curing the encapsulant. The method can further include providing a connector for removably mating with and providing electrical connection to the metal. The method can further include providing a center plate having an opening to accommodate the substrate. Forming a panel assembly can include positioning the substrate in the opening of the center plate and closing the mold panels against the center plate. The method can further include providing at least one opening in the center plate connected to the internal chamber by at least one conduit; and forcing the encapsulant through the at least one opening and at least one conduit into the internal chamber. Forming a panel assembly can include securing the mold panels together prior to curing the encapsulant.

[008] In general, in another aspect, a method of forming an electrical contact is provided. The method includes assembling a panel including a substrate having one or more conductive features enclosed within the panel and unexposed to an exterior surface of the panel, the one or more conductive features being located along a cut line; cutting the panel along the cut line exposing portions of the one or more conductive features for use as electrical connections to the substrate; and treating the portions of the one or more conductive features exposed from the cutting for preservation as electrical connections.

[009] Implementations of the method may include one or more of the following features. The treating can include applying solder to the portions of the one or more conductive features exposed from the cutting. The treating can include applying a conformal coating to the portions of the one or more conductive features exposed from the cutting to protect against oxidation. The treating can include applying a metal layer to the portions of the one or more conductive features exposed from the cutting. The treating can include soldering a lead of an adapter to the portions of the one or more conductive features exposed from the cutting. The method can further include covering at least one surface of the substrate in an area including the cut line and the conductive features prior to cutting the substrate. The covering can include encapsulating the substrate with a molding compound. The method can further include providing a

registration feature having a predetermined relationship to the substrate, and using the registration feature to align the cutting relative to the cut line. The method can further include establishing a pattern including at least one conductive layer in the substrate along the cut line to form the conductive features. The substrate can include a multilayer printed circuit board, and the pattern can include a plurality of conductive layers that are established along the cut line to form the conductive features. The method can further include establishing a pattern including at least one conductive via in the substrate along the cut line to form the conductive features. The conductive via can be filled with a conductive material. The conductive via can be buried in the substrate. The conductive via can be a through hole contacting the surfaces of the substrate. The through hole can be filled with a conductive material. The conductive features can be covered at the surfaces of the substrate by an insulative layer.

[010] In general, in another aspect, an apparatus including a first mold panel is provided. The first mold panel includes an exterior surface, an interior surface defining an internal cavity, a clamp region located at points along a circumference of the internal cavity, and an opening. The first mold panel is adapted to (a) be engaged by pressure in the clamp region, (b) receive in the cavity a circuit panel containing a plurality of components and mold compound to fill empty spaces in the internal cavity, and (c) be cut after curing of the mold compound.

[011] Implementations of the apparatus may include one or more of the following features. The interior surface in the region of the internal cavity can be adapted to adhere to the mold compound. The apparatus can further include a second mold panel. The second mold panel can include an exterior surface, an interior surface, and a clamp region, in which the second mold panel can be adapted to (a) close against and mate with the first mold panel, (b) be engaged by pressure in the clamp region, and (c) be cut after curing of the mold compound. The interior surface of the second mold can further define a second internal cavity, the clamp region of the second mold panel can be located at points along a circumference of the second internal cavity, and the internal cavity of the first mold panel can be adapted to receive a first side of the circuit panel and the second internal cavity can be adapted to receive a second opposite side of the circuit panel. The

apparatus can further include contours formed in the interior surface of at least one of the mold panels. The contours can be adapted to match predetermined characteristics of selected ones of the plurality of components. The internal surface of the mold panel can be adapted to adhere to the molding compound. The contours can form interlocking features with cured mold compound. One or more of the mold panels can include a non-ferrous metal, aluminum, or a thermally conductive material. One or more of the mold panels can include a non-metallic substance. The apparatus can further include at least one channel connected to the internal cavity for allowing expansion of the mold compound. The apparatus can further include at least one channel connected to the internal cavity for injecting mold compound into the internal cavity. The exterior surface of the mold panel can include a plurality of fins. The exterior surface of the mold panel can include a flat surface. The flat surface can be adapted for a solder joint. The internal cavity can include features formed in the interior surface and arranged in a predetermined pattern. The internal cavity can include features formed in the interior surface along lines through which the mold panel maybe cut to establish a setback from a cut edge of the mold panel. The mold panel can include at least one registration feature adapted to engage and establish a predetermined relationship with the circuit panel. One or more selected portions of the mold panel can be adapted for incorporation into one or more products, the products being formed by a process which uses the mold panel to contain the molding compound. The exterior surface of the mold panel can include a flat surface with one or more pins protruding from the flat surface. The exterior surface of the mold panel can include a flat surface having one or more holes in the flat surface. The apparatus can further include a pin inserted into a respective one of the one or more holes.

[012] In general, in another aspect, an apparatus including a panel assembly having external surfaces defined by a first mold panel and a second mold panel is provided. The first and second mold panels form an internal cavity enclosing an internal circuit board, the internal circuit board having a first surface and second surface and a plurality of components in an active circuit area on at least one of the surfaces, the components being electrically connected to interconnects contained within the internal cavity. The internal cavity is filled with mold compound in spaces unoccupied by the

circuit board and components, and the panel assembly is adapted to have first selected portions of the first and second mold panels cut away to expose the interconnects and to have second selected portions of the respective mold panels situated near the active circuit area remain attached to the assembly following the cut.

[013] Implementations of the apparatus may include one or more of the following features. The panel assembly can include a clamp region located at points along a circumference of the first and second internal cavities, and the first selected portions can include the clamp region.

[014] In general, in another aspect, an apparatus including a panel assembly having external surfaces defined by a first mold panel and a second mold panel is provided. The first and second mold panels form an internal cavity enclosing an internal circuit board, the internal circuit board having a first surface and second surface and a plurality of components electrically connected to form a plurality of individual circuits, each individual circuit being electrically connected to respective interconnects located along a respective circuit perimeter, the interconnects being contained within the cavity.

[015] Implementations of the apparatus may include one or more of the following features. The panel assembly can be adapted to be cut along the circuit perimeter separating the individual circuits, dividing the panel assembly into individual circuit modules, and exposing selected portions of the interconnects. The panel assembly can be constructed to retain an integral layered structure after being filled with mold compound which is subsequently cured, the layered structure comprising a first layer including a portion of the first mold, a second layer including a portion of the mold compound, a third layer including a portion of the circuit board, a fourth layer including a portion of the mold compound, and a fifth layer including a portion of the second mold. The internal circuit board can include a plurality of circuits having the same functionality. The apparatus can further include one or more conduits connecting the internal cavity to an external opening. Spaces unoccupied by the circuit board, components, and interconnects in the internal cavity can be filled with mold compound. The mold

compound has been cured. Selected portions of at least one of the mold panels have been removed, the selected portions being located near the circuit perimeters.

[016] In general, in another aspect, an apparatus including a modular package is provided. The modular package has a first external surface, a second external surface opposite the first external surface, and a side wall extending along the perimeter of and connecting with the first and second external surfaces. The modular package includes a first layer defining the first external surface and a second layer defining the second external surface, the first and second layers being separated by and in contact with cured mold compound. An electrical circuit is located between the first and second layers and within the cured mold compound and including at least one electrical component electrically connected to a plurality of interconnects. The side wall includes a strip formed by the first layer, a strip formed by the second layer, and a strip formed by the cured mold compound. The interconnects are disposed within the side wall.

[017] Implementations of the apparatus may include one or more of the following features. The first and second layers can include a non-ferrous metal or aluminum. The first external surface can include a plurality of fins. The first external surface can include an essentially flat area. The essentially flat area can be adapted for a solder joint. The electrical circuit can include a circuit board, and the side wall can include a strip formed by the circuit board and an additional strip formed by cured mold compound. The interconnects can include conductive features in the circuit board. The circuit board can include a multilayer printed circuit board ("PCB") and each of the interconnects can include a plurality of conductive layers in the PCB. Each of the interconnects can include a plurality of conductive vias in the circuit board. The apparatus can further include interlocking features. The interlocking features can include a contour formed in an interior surface of the first layer, the contour being filled with cured mold compound. The circuit board can include a top surface and a bottom surface and the at least one electrical component can include a set of top-side components mounted on the top surface and a set of bottom-side components mounted on the bottom surface. The top-side components can include a number, T, of large-footprint components, the bottom-side components can include a number, B, of large-footprint components, and the number T

can be approximately equal to the number B. Each of most of the top-side large-footprint components can share a respective set of conductive vias with a corresponding one of the bottom-side large-footprint components. Each of most of the top-side large-footprint components is located in a respective footprint shared by a corresponding one of the bottom-side large-footprint components. The circuit board can include a top surface and a bottom surface, the at least one electrical component can include a number, T, of large-footprint components mounted on the top surface, and most of the large-footprint components can be distributed symmetrically in relation to an axis on the top surface. The axis can be along a midline of the top surface. The axis can be defined in relation to a predetermined component. The apparatus can further include an adapter for providing mechanical and electrical connections between the modular package and an external mounting surface, the adapter having a body and a plurality of electrical terminals supported by the body; and electrical connections formed between the adapter terminals and respective interconnects on the modular package. The adapter body can be mechanically secured to the modular package, and the adapter terminals can be arranged to mate with the external mounting surface. The external mounting surface can be a circuit board and the terminals can include ends constructed and arranged to be inserted into conductive holes in the circuit board. The external mounting surface can be a circuit board and the terminals can include ends constructed and arranged to be surface mount soldered to the circuit board. The external mounting surface can include a connector and the terminals can include ends constructed and arranged to mate with the connector. The interconnects can be disposed along a long edge of the modular package, the adapter can be secured to the long edge of the modular package, and the first and second layers of the modular package can be oriented perpendicular to the mounting surface. The interconnects can be disposed along opposite edges of the modular package, the adapter can be secured to the opposite edges, and the first and second layers of the modular package can be oriented essentially parallel to the mounting surface. The adapter can be constructed and arranged to maintain one of the first or second layers in contact with the mounting surface. The interconnects can include a surface constructed and arranged for engagement with a connector terminal. The interconnects can include a layer of metal plating.

[018] In general, in another aspect, an apparatus includes a modular package having a first external surface, a second external surface opposite the first external surface, and a side wall extending along the perimeter of and connecting with the first and second external surfaces, the modular package including a first layer of metal defining the first external surface and a second layer of metal defining the second external surface, the first and second layers being separated by and in contact with cured mold compound; and an electrical circuit for converting power, including a printed circuit board ("PCB"), a plurality of components including semiconductors mounted to the PCB, and a plurality of interconnects electrically connected to the components, the electrical circuit being located between the first and second layers and within the cured mold compound. The side wall includes a strip formed by the first layer, a strip formed by the second layer, a strip formed by the PCB, and one or more strips formed by the cured mold compound. The interconnects are disposed within the side wall.

[019] Implementations of the apparatus may include one or more of the following features. The first and second layers can include aluminum, and the first external surface can include a plurality of fins. The first and second layers can include aluminum, and the first external surface can include an essentially flat area. The essentially flat area can be adapted for a solder joint. The PCB can include a top surface and a bottom surface, the semiconductors can include large-footprint switches. A number, T, of top-side large-footprint switches can be mounted on the top surface, a number, B, of bottom-side large-footprint switches can be mounted on the bottom surface, and the number T can be approximately equal to the number B. Each large-footprint switch can be connected to one or more other components by a respective set of conductive vias in the PCB, and each of a plurality of the top-side large-footprint switches can share its respective set of conductive vias with a corresponding one of the bottom-side large-footprint switches. Most of the large-footprint switches can be positioned on one surface in a location substantially overlapping a location on the other surface occupied by another large-footprint switch. The apparatus of claim 151 wherein the PCB includes a top surface and a bottom surface, the semiconductors include large-footprint switches mounted on the top surface, most of the large-footprint components are distributed symmetrically between a left side of the top surface and an opposite right side of the top surface. The PCB can

include a top surface and a bottom surface, the semiconductors can include large-footprint switches mounted on the top surface, and most of the large-footprint components can be distributed symmetrically between quadrants on the top surface. The components can include a transformer core. The quadrants can surround the transformer core. The PCB can include a top surface and a bottom surface, and the components can include a set of high-profile components having similar heights. A number, T, of the high-profile components can be mounted on the top surface, a number, B, of the high-profile components can be mounted on the bottom surface, and the number T can be approximately equal to the number B. A spatial distribution of the high-profile components on the top surface can roughly match a spatial distribution of the high-profile components on the bottom surface. The apparatus can further include an adapter for providing mechanical and electrical connections between the modular package and an external mounting surface, the adapter having a body and a plurality of electrical terminals supported by the body; and electrical connections formed between the adapter terminals and respective interconnects on the modular package. The adapter body can be mechanically secured to the modular package, and the adapter terminals can be arranged to mate with the external mounting surface. The external mounting surface can be a circuit board and the terminals can include ends constructed and arranged to be inserted into conductive holes in the circuit board. The external mounting surface can be a circuit board and the terminals can include ends constructed and arranged to be surface mount soldered to the circuit board. The external mounting surface can include a connector and the terminals can include ends constructed and arranged to mate with the connector. The interconnects can be disposed along a long edge of the modular package, the adapter can be secured to the long edge of the modular package, and the first and second layers of the modular package can be oriented perpendicular to the mounting surface. The interconnects can be disposed along opposite edges of the modular package, the adapter can be secured to the opposite edges, and the first and second layers of the modular package can be oriented essentially parallel to the mounting surface. The adapter can be constructed and arranged to maintain one of the first or second layers in contact with the mounting surface. The interconnects can include a surface constructed and arranged for engagement with a connector terminal. The interconnects can include a layer of metal

plating. The first layer can include contours formed in an interior surface of the first layer, the contours including a first feature having a shape and an elevation to accommodate a first component on the PCB, the first component having a height greater than or less than other components on the PCB. The first component can include a magnetic core structure and the elevation can be a recess in the interior surface. The first component can include a semiconductor switch and the elevation can be a protrusion from the interior surface. The apparatus can further include interlocking features having a contour formed in an interior surface of the first layer, the contour being filled with cured mold compound. The modular package can include a recess formed in the first layer adjacent one or more of the interconnects providing a setback between the first layer and the one or more interconnects.

[020] In general, in another aspect, an apparatus includes a power converter is provided. The power converter includes a printed circuit board ("PCB") having a plurality of conductive layers and having a top surface and a bottom surface; a magnetic core structure magnetically coupled to a winding formed by traces in one or more of the conductive layers in the PCB; and a plurality of power semiconductor devices. A first set of the power semiconductor devices is mounted on the top surface and electrically connected to dissipate power at a level, Pt, during operation of the converter, and a second set of the power semiconductor devices is mounted on the bottom surface and electrically connected to dissipate power at a level, Pb, during operation of the converter. The power semiconductor devices are distributed between the first and second sets to distribute heat generation during operation of the converter such that each level Pt, Pb is less than 150% of the other level Pb, Pt.

[021] Implementations of the apparatus may include one or more of the following features. A plurality of the power semiconductor devices in the first set can each be positioned in a location on the top surface substantially overlapping a location on the bottom surface occupied by a power semiconductor device in the second set. The power semiconductor devices can be electrically connected using a respective set of conductive vias in the PCB, and a plurality of the power semiconductor devices in the first set can share their respective sets of conductive vias with corresponding power semiconductor

devices in the second set. The power converter can include circuitry having a pair of cells that have a common circuit topology and each including power semiconductor switches from each of the first and second sets. Each cell can have its respective components arranged in a pattern, in which the pattern of components of one cell is substantially a mirror image of the pattern of components in the other cell. A component from one of the cells can be located on an opposite surface of a respective component from the other one of the cells. The cells can include input cells. The power semiconductor devices can include output switches.

[022] In general, in another aspect, a method of manufacturing a plurality of products is provided. The method includes inserting a plurality of components into a cavity formed by one or more molds; closing the one or more molds to form a seal around the cavity; filling the cavity with mold compound; curing the mold compound in the cavity to secure the components, cured mold compound, and molds together into an assembly; and cutting the assembly to separate the plurality of products from the assembly, the products each including a respective section of the one or more molds which remains as an integral part of each respective product.

[023] Implementations of the method may include one or more of the following features. The method can further include maintaining a predetermined alignment between the plurality of components and the one or more molds. The plurality of components can include a substrate having conductive features. The cutting can include exposing portions of the conductive features in each respective product.

[024] The details of one or more embodiments of the invention are set forth in the accompanying drawings and description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

[025] FIG. 1 shows an electronic module 100.

[026] FIG. 2 shows a panel assembly 120 comprising a plurality of electronic modules before singulation.

[027] FIG. 3 shows an exploded view of the panel assembly revealing the heat sink panels 121 and 122 and internal PCB panel 124.

[028] FIG. 4 shows the panel assembly 120 with the top heat sink panel 121 removed.

[029] FIG. 4A shows an exploded view of the PCB panel and lower heat sink panel in a modified panel assembly 120.

[030] FIG. 4B shows a cross-section of the panel assembly 120A along lines 4B-4B in Fig. 4A.

[031] FIG. 5 shows a plan view of the PCB panel 124 assembled with the bottom heat sink panel 122.

[032] FIG. 6 shows a cross-section of the panel assembly 120.

[033] FIG. 7 shows a partial cross section of the panel assembly closed in a mold.

[034] FIG. 8 shows another partial cross section of the panel assembly closed in a mold.

[035] FIG. 9A shows a plan view of the panel assembly 120 following singulation.

[036] FIGs. 9B, 9C show optional channels formed in the panel before singulation.

[037] FIGs. 10A, 10B show single modules 115, 115B after singulation.

[038] FIG. 11 shows an enlarged portion of the module 115 revealing details of exposed buried-embedded interconnects.

[039] FIG. 12 shows a cross section of the singulated module 115 of Fig. 10A.

[040] FIG. 13 shows a connector assembly.

[041] FIG. 14 shows an exploded view of the connector assembly.

[042] FIG. 15 shows a horizontal through-hole mount module 200.

[043] FIG. 16 shows an exploded view of the through-hole mount module 200.

[044] FIG. 17 shows a horizontal surface-mount module 300.

[045] FIG. 18 shows an exploded view of the surface-mount module 300.

[046] FIG. 19 shows an alternative horizontal surface-mount module 400.

[047] FIG. 20 shows a top view of the surface-mount module 400.

[048] FIG. 21 shows an exploded top view of module-connector set 500.

[049] FIG. 22 shows an exploded view of the connector set 503.

[050] FIG. 23 shows an exploded bottom view of module-connector set 500.

[051] FIG. 24 shows an isometric view of the module-connector set 500 assembled.

[052] FIG. 25 shows an alternative horizontal through-hole flush-mount module 600 exploded from a customer PCB.

[053] FIG. 25A shows an alternative horizontal through-hole flush-mount module 650 exploded from a customer PCB.

[054] FIG. 26 shows the horizontal through-hole flush-mount module 600 assembled onto a customer PCB.

[055] FIG. 27 shows top and bottom plan views of a section of a PCB illustrating symmetry of component layouts.

[056] FIG. 28 shows an exploded perspective view of a panel assembly 720 including a manifold plate.

[057] FIG. 29 is an exploded side view of the panel assembly 720 showing the PCB mated with the manifold plate.

[058] FIG. 30 shows a top plan view of the panel assembly 720.

[059] FIG. 31 shows a top plan view of the panel assembly 720 with the top heat sink panel removed.

[060] FIG. 32 shows a side view of the panel assembly 720 closed in a mold.

[061] Like references symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

I. Vertical PCB Package.

[062] Referring to Fig. 1, an electronic module 100, e.g. a power converter, is shown having a generally rectangular form factor with two large faces 114A, 114B covered by heat sinks 101, 102. As shown between the heat sinks 101 and 102, the module 100 includes a printed circuit board ("PCB") 104 having its large faces arranged generally coplanar to the two large faces 114A, 114B of the electronic module 100. Electronic components (Figs. 3, 5, 6) may be mounted to one or both sides of the PCB 104 and electrically interconnected, e.g. by conductive traces on or in the PCB 104 to form the module circuitry. Using a power converter as an example, the electronic components may include power transistors, control ICs, and discrete resistors and capacitors. One or

more magnetic core structures may be provided, which in combination with conductive traces on PCB 104, may form planar magnetic components such as inductors and transformers.

[063] The electronic components may protrude from one or both sides of the PCB 104 to varying degrees depending upon component size. Spaces between the faces of PCB 104 and the components on the PCB on one hand and the interior surfaces of the heat sinks on the other hand may be filled with molding compound, which when cured may form integral structural layers 105, 106 as shown in Fig. 1 and further provides a thermally conductive medium in which heat may be readily conducted away from the PCB and components to the heat sinks 101, 102. The interior surfaces of the heat sinks may be contoured to match the height of one or more of the components while maintaining an appropriate clearance for insulation and safety agency requirements. Contouring the heat sinks 101, 102 in this way: (1) to match the height of the magnetic core structure may be used as an alternate approach to the exposed core encapsulation method described in Vinciarelli, *Encapsulation Method and Apparatus for Electronic Modules*, U.S. Patent Application, Serial No. 12/493,773 filed June 29, 2009 (assigned to VI Chip Corp. of Andover, MA, the entire disclosure of which is incorporated herein by reference); (2) to match the height of lower profile components, such as power semiconductors, may (a) increase thermal performance in the case of heat dissipating components by replacing molding compound with heat sink metal; and (b) reduce cost generally by reducing the volume of molding compound required; and (c) further reduce cost by allowing less expensive molding compound to be used because of reduced thermal pathways through the encapsulant, easing the thermal conductivity requirements of the encapsulant (e.g., an encapsulant having a 1 degree Celsius per watt thermal resistance may be used with the contoured heat sink instead of an encapsulant having a 3 degrees Celsius per watt thermal resistance used without the contoured heat sink).

[064] A connector 103, including terminals 108, 109, 110 and standoffs 107, may be provided as shown along an edge of the PCB 104 to make electrical connections between the electronic module 100 and external circuitry. As shown in Fig. 1 with the connector 103 situated along one edge of the module 100, preferably one of the longest edges, the

module 100 may be mounted vertically, i.e. with its internal PCB 104 perpendicular to a chassis or another circuit board such as a motherboard. Using the vertical mount module construction illustrated in Fig. 1 for a power converter may provide advantages over the more conventional horizontal mounting technique. For example, using the vertical PCB arrangement may allow use of a magnetic core structure that is thicker than in a horizontal PCB configuration, e.g. because of height restrictions, enabling increased power throughput, as compared to a similar converter using a horizontal PCB orientation. The length of the magnetic path may be also reduced in the vertical PCB configuration further reducing losses in the magnetic components. Shorter windings may also be used further reducing transformer or inductor losses. Further details and variations of, and a process for making, the electronic module will be discussed below in connection with a panel molding process.

II. Panel Molding Process.

A. Overview

[065] The electronic module 100 shown in Fig. 1 may be fabricated using a panel molding process described with reference to Figs. 2- 9. The panel molding process may be used to produce a multiplicity of modules at a time. A PCB panel 124 may be provided with a plurality of individual circuits for building the electronic modules. Figs. 3, 4, and 5 show the PCB panel 124 populated with electronic components revealing a 3-by-4 pattern of twelve circuits to make twelve individual modules 115 (labeled 115A through 115L in Fig. 5). The illustrative example of Figs. 3-5, being for power converters, includes magnetic core structures 131 (Fig. 3) in addition to electronic components 132. As shown in Fig. 5, the pattern of individual circuits 115A-115L are arranged close together and separated by small spaces 135 preferably sufficient to allow the PCB panel to be cut during the singulation process without necessitating two cuts between modules or unnecessary waste of PCB material. The spacing may be adjusted based upon the cut dimensions produced by the equipment used to make the cuts.

[066] The PCB panel 124 containing the multiplicity of the electronic circuits (115A-115L in Fig. 5) may be assembled with matching heat sink panels 121, 122 as shown in

Fig. 3 to form a panel assembly 120 (Fig. 2). As shown in Figs. 3 and 6, the two heat sink panels 121 and 122 when assembled together may form an internal cavity 146, which completely encloses the populated PCB panel 124. Figs. 2 and 6 show that the heat sink panels 121 and 122 may be pressed together (e.g. by a mold press 161, 162 as shown in Fig. 7) to form a seal 123 (Figs. 2, 6-8) around the perimeter of the internal cavity 146. In this example, the heat sink panels 121 and 122 also function as mold panels by forming a mold cavity (e.g., the internal cavity 146) that may be filled at least in part by an encapsulant encapsulating the surfaces of the PCB panel 124 and the electronic components on the PCB panel 124.

B. Heat Sink Panels

[067] Referring to Fig. 2, the heat sink panels 121, 122 may include fins on the exterior surfaces as shown. The fins may be arranged in any direction relative to the panel or in any pattern and may vary in height, thickness, and spacing as required for the particular application. For example, modules 115 and 115B shown in Figs. 10A and 10B respectively illustrate longitudinal and transverse fin orientations. Alternatively, one or both of the heat sink panels may have a generally flat exterior surface omitting the fins altogether. For example, Figs. 17 and 25 show modules 315 and 615 produced when both heat sink panel exterior surfaces are flat and one is flat and one is finned, respectively. The thickness of the panels between the internal cavity and the external surface may be varied to suit the particular requirements of the application.

C. Heat Sink Internal Contours

[068] Referring to Fig. 3, the contoured interior surface of the bottom heat sink panel 122 is shown including a 3-by-4 repeating pattern of twelve (A through L) prominent recesses 141 and shallower recesses 142 and 143. Recesses 141 may be matched to the downward protruding portion of magnetic core structures 131. Similarly, recesses 142 and 143 may be matched to other downwardly protruding components on the PCB panel 124. Note that in the example of Fig. 3, because the core structure 131 protrudes from the PCB 124 more than the other components, the recesses 141 are deeper than recesses 142, 143. Although not visible in Fig. 3, the interior surface of heat sink panel 121 may

similarly include contour features to match the components and core structure on the upward facing side of the PCB panel 124 (e.g. as shown in the cross-section of Figs. 6, 7). Although the interior contour of panel 122 in Fig. 3 is shown including three recesses 141, 142, 143 repeated for each circuit (A through L in the 3-by-4 pattern), the interior contours of the heat sink panels 121 and 122 may range from simple flat surfaces (accommodating the height of the tallest component) to a complex arrangement of a multiplicity of recessed and protruding features (accommodating a multiplicity of component heights) which at the extreme could match every component individually.

[069] Additional features may be provided in the heat sink panels to facilitate the panel molding process, to enhance the mechanical integrity or performance of the finished module 100, or to satisfy safety agency clearance requirements for the finished product. By way of example undercut features, such as undercuts 148 shown in Figs. 6, 7, and 12 may be provided at each circuit site (i.e. within each individual module location) in the heat sink panels 121, 122. As shown the undercuts 148 may be provided in selected recesses, such as recesses 143-1 and 143-2, and may be dispersed along one or more of the boundary lines of each circuit 115. During encapsulation, molding compound fills the recesses and trenches and their respective undercuts 148. When cured, the hardened molding compound in the undercuts forms a dovetail-like joint securing the heat sinks to the encapsulated PCB 124. When provided at each circuit site, the undercuts secure the heat sinks 101, 102 to the PCB 104 in the individual module 115 providing mechanical integrity after singulation. Referring to the cross-section of a singulated module 115 in Fig. 12, dovetail interfaces 149-2 and 149-1 are shown securing the top and bottom heat sinks 101, 102 to the encapsulated PCB assembly.

[070] Additionally, clearance features may be provided in the heat sink panels to satisfy minimum safety agency clearances between electrical contacts on the PCB 124 and the metal heat sinks 121, 122. As shown in Figs. 6 and 7, trenches 147 may be provided in heat sink panels 121 and 122 along the side of each module 115 (the long side as shown in Figs. 6 and 7) where electrical contacts (discussed in more detail below) are exposed in or on the PCB 124. The trenches 147 may also include the undercut

features 148 discussed above. For example, cut trench 147 in Fig. 12 results in a recess 150 of the heat sink 101 away from the edge 104E of the PCB 104 after singulation.

D. PCB-Heat Sink Registration

[071] Registration features may be provided in one or both of the heat sink panels 121, 122 helping to correctly position the PCB panel 124 in the cavity 146 relative to the heat sink panels 121, 122 (which is particularly important when the panel is cut during the singulation process) and to correctly position the heat sink panels relative to each other during assembly and during subsequent molding processes. Referring to Figs. 3 and 4, beveled corners 144 may be provided in heat sink panel 122 to interface with matching indentations 133 which may be provided in PCB panel 124 for registration when assembled together (Figs. 4 and 5). Fig. 5, which is a top plan view of the PCB panel 124 assembled with the bottom heat sink 122, shows the beveled corners 144 interfacing with the indentations 133.

[072] Referring to Fig. 4A, a modified version of the assembly is shown. As shown, a registration pin 151 is press fit into a registration hole 152 in the lower heat sink panel 122 and a matching registration hole 134 is provided in the PCB panel 124. The completed panel assembly, including the lower heat sink panel 122, PCB panel 124, and upper heat sink panel 121, is shown in Fig. 4B in cross-section taken along the broken lines 4B-4B in Fig. 4A. As shown in Fig. 4B, the registration pin 151, which fits snugly in registration holes 152 and 134, provides registration for the PCB panel 124 relative to the lower heat sink panel 122. An indentation 153 may be provided in the opposite heat sink panel (121) to accommodate protrusion of the pin 151 past the PCB 124. As shown generally at 154 in Fig. 4B, the heat sink panels may include additional features to provide registration between the top and bottom heat sink panels. Although a registration pin is shown at one corner of the panel 122 in Fig. 4A, it will be appreciated that additional pins may be used at other locations. For example, Fig. 4 shows two registration holes 134, one on a corner and another in the middle of the opposite side of the PCB panel 124.

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E. Encapsulation

[073] Fig. 6 shows a cross-sectional view (through lines 6-6 in Fig. 5) of the panel 120 through an opening 125 and a conduit 145 in the heat sink panels. The openings 125, which may be slot shaped as shown (Figs. 2, 3, 4, 5, 9), may be connected to the interior cavity 146 of the panel assembly 120 by conduits 145 for conveying molding compound or venting during the panel molding process. The openings may be formed in one of the heat sink panels, e.g. openings 125 in the top heat sink panel 121 as shown in Figs. 2, 3, 4, 5, and 9, or in both heat sink panels, e.g. openings 125B in the top and bottom heat sink panels 121, 122 as shown in Figs. 6 and 7. Referring to Fig. 6, the conduits 145 may be formed by recesses in the interior surfaces of heat sink panels 121 and 122, connecting the openings 125 to the interior cavity 146. The recesses forming the conduit 145 may be situated near the edge 124C of PCB panel 124 to allow the molding compound to flow over both top 124A and bottom 124B surfaces of the PCB 124.

[074] Fig. 7 shows an enlarged cross-section of one end of the panel assembly 120 closed between an upper mold press 161 and lower mold press 162 taken through some of the smaller components, e.g. components 132-1, 132-2, i.e. through lines 6-6 in Fig. 5. A channel 163 may be provided, e.g. between the upper mold press 161 and lower mold press 162 as shown, to interface with openings 125. Molding compound may be forced through the channel 163 under pressure after the panel assembly 120 is closed in the mold presses 161, 162. The dashed line 167 with directional arrows in Figs. 7 and 8 illustrates the flow of molding compound through the channel 163 into openings 125 through conduits145 over the top 124A and bottom 124B surfaces of the PCB panel 124 during encapsulation. The molding compound may be forced into the internal cavity 146 to fill all of the unoccupied spaces between the heat sinks 121, 122 and the PCB panel 124.

[075] Fig. 8 shows an enlarged cross-section of one end of the panel assembly 120 closed between an upper mold press 161 and lower mold press 162 taken through the magnetic core structures, i.e. through lines 8-8 in Fig. 5. Each magnetic core 131 is shown having an upper E-core 131-2 and a lower E-core 131-1 separated by a gap 131-3.

The cores have openings 131-4 to accommodate windings formed on the PCB 124. As shown, the lower core 131-1 and upper core 131-2 are accommodated by recesses 141-1 and 141-2 in the lower heat sink 122 and upper heat sink 121, respectively. As shown, compliant pads 136 may be provided on the surfaces of the cores 131-1 and 131-2 or in recesses 141-1, 141-2 to accommodate dimensional differences in the components. The compliant pads may be chosen for good thermal conduction and optionally adhesive properties facilitating heat removal from the cores into the heat sink while optionally providing structural integrity to the assembly. Gap Pad A2000 available from the Bergquist Company, 18930 West 78th St, Chanhassen, Mn 55317 is one example of the type of compliant pad that may be used. Alternatively and perhaps depending upon the tolerances involved, a phase change material may accommodate the dimensional difference during assembly and when cured afterward provide structural integrity between the heat sinks and the cores.

[076] Molding compound may be deposited in one or more of the recesses, e.g. recesses 141-1 or 141-2, in the internal cavity prior to assembly of the PCB panel 124 into one or both of the heat sink panels 121, 122 to ensure that the molding compound fills narrow spaces between the heat sink and the components, e.g. the cores 131-1, 131-2. One or more vent openings (not shown) may be provided in the heat sink panels, preferably at an end opposite the fill openings 125, to allow the molding compound to flow completely through the internal cavity 146. The cavity may be filled with encapsulant either (1) by transfer through one or more conduits, (2) by measured deposition of encapsulant during assembly of the panels, or (3) by both measured deposition during assembly and transfer through conduits.

[077] As shown in Figs. 4, 5, and 6, the border areas between the modules and around the periphery of the PCB panel 124 may be minimized to avoid wasted PCB material. Because the heat sink panels 121 and 122 close against each other rather than the PCB panel 124, areas on the PCB normally reserved for closing the mold may be eliminated further reducing PCB waste and thus overall cost.

[078] After the panels are assembled together and the interior cavities are filled with molding compound, the panel assembly 120 may be cured, e.g. by elevating the temperature.

F. Singulation

[079] Singulation is the process by which individual modules, e.g. singulated module 115 in Fig. 10A, are separated from the panel assembly 120, e.g. by cutting. The panel assembly 120 may be singulated after the molding compound is cured. The panel assembly 120 is separated from the upper and lower mold presses 161, 162 and may be cut, e.g. along lines 128, 129 as shown in Fig. 9A, to singulate the modules 115A-115L. For example, a narrow saw may be used to cut through the layers (e.g. as shown in Figs. 1, 10A, 10B, 12) of panel 120, which may include heat sink 101, cured molding compound 105, PCB 104, cured molding compound 106, and heat sink panel 102. For example, a 0.025 inch thick saw such as model number EAD-3350 available from Disco Corp., Ota-ku, Tokyo, Japan may be used. Referring to the cross-sectional views of Figs. 6 and 7, dashed lines 129 illustrate the lines along which the panel 120 may be cut to singulate modules 115D, 115E, and 115F. As shown, the cuts 129 (along the long side of the individual modules 115) go through the middle of the trenches 147. The trenches 147 may be made wide enough and the cuts 129 may be made at an appropriate distance from the edges of the trench 147 to ensure that a minimum thickness of cured molding compound remains in the trench after singulation to be mechanically robust. The trenches 147 may also be used to reduce the thickness of metal through which the saw must cut during singulation, e.g. by optionally providing trenches along the perimeter of each module.

G. Electrical Connections

[080] Interconnection features may be embedded in the PCB panel 124, preferably along the boundaries of the individual circuits, so that electrical contacts are at least in part formed by or exposed during singulation. To maximize the area on a PCB panel 124 available for circuitry, the interconnection features may preferably be buried in the PCB panel 124 below the top and bottom surface layers. For example, the interconnection

features may be formed in the inner conductive layers but not occupying valuable area on the surface conductive layers, potentially reducing setback and other spacing requirements. The interconnect features therefore are preferably formed in the PCB panel 124 before the panel 120 is assembled and exposed when the panels are cut, e.g. during singulation. The interconnection features may comprise a pattern of conductive layers or buried vias (frequently used to form connections between internal conductive layers) or both in the PCB situated along the circuit boundary, i.e. lying in the cut line, e.g. cut line 129 (Fig. 9A).

[081] Referring to Fig. 10A, a module 115 is shown after singulation. Exposed interconnects 111, 112, and 113 are shown embedded in the edge of the PCB 104 along one of the edges 116 of the module 115. As shown in Fig. 10A, longer connections 111 and 113 provide greater interconnect surface area and higher current carrying capacity, making them amenable for use as power connections, than shorter connections 112 which have less interconnect area and lower current carrying capacity, making them useful for control signal connections. Fig. 11 shows an enlarged view of a portion of the module 115 along edge 116 revealing detail of the two interconnections 111 after singulation. The width along the boundary and number of the conductive features arranged vertically through the PCB layers may be adjusted to provide the requisite contact area for each connection. In the example of Fig. 11, conductive features, e.g. conductive lands 111A through 111L, formed along the cut line on a plurality of the conductive layers of the PCB form a stack of conductive strips resembling a bar code after singulation. The stack of conductive lands may provide more contact area than possible with a single buried via. In Fig. 11, each interconnect 111 is made up of twelve lands, each land being formed on a respective one of twelve inner conductive layers. Note that Fig. 11 shows the twelve lands (111A through 111L) buried below the top 124A and bottom 124B surfaces of the PCB, i.e. not occupying surface area on those layers. During singulation, the saw cuts through the buried embedded lands, exposing the edges of the remaining conductive material forming the interconnects 111A through 111L shown in Fig. 11. Note that the buried embedded lands may be shared between two adjacent modules 115 on the panel 120, e.g. where the PCB patterns are laid out in mirror image to each other, allowing the modules to be laid out on the PCB panel close to a singulation cut width apart. Also, the

interconnect features may be aligned along a single module boundary as shown or may occupy two or more boundaries of each individual module in the panel. The exposed edges may then be used to form electrical connections immediately after singulation, i.e. before the cut interconnects oxidize or may be protected against oxidation, e.g. with a conformal coating, such as an organic solderability preservative ("OSP"), applied after singulation, to ensure subsequent ability to form electrical connections to the edges. For example, Entek Plus HT available from Enthone, Inc., a Division of Cookson Electronics, West Haven , CT 06516 may be used as an OSP to protect the interconnects.

[082] The number of lands, i.e. conductive layers, used to form each interconnect may be increased for better electrical connections or reduced for less critical connections. Although embedded conductive lands are shown in the example of Figs. 10A, 11, additional or alternative conductive features may be used to form the interconnects. For example, buried conductive vias located along the cut line may be used, either alone or in combination with the lands. The buried vias may be located so that the singulation cut leaves the walls of the conductive vias exposed resulting in vertical conductive strips, i.e. generally perpendicular to the PCB top and bottom surfaces 124A, 124B, in the PCB edge. Buried conductive vias may tend to fill with adhesive during fabrication of the PCB panel 124. Empty conductive vias, i.e. free of non-conductive adhesives, may be preferable for the resulting concave conductive features, i.e. embedded conductive half cylinders. Similarly, solid buried conductive vias or conductive vias filled with conductive material during the PCB manufacturing process may be preferable for the resulting continuous flat conductive surface.

[083] In the alternative to buried conductive features, conductive through-holes, which are generally free of adhesives following fabrication of the PCB panel 124 may be used along the cut line to form interconnects extending through the thickness of the PCB from top surface to bottom surface providing generally half-cylindrical interconnects. A penalty of using through-holes for the interconnects is the loss of surface area on the top and bottom of the PCB which may otherwise be used for setback or other safety and agency approval requirements. Preferably, the through-holes may be filled, for example with a conductive material such as solder or silver paste, or conductive pins may be

inserted into through holes and soldered to the through holes, to prevent molding compound from filling the through hole during the encapsulation process and to provide a greater contact surface area yielding generally flat conductive interconnects following singulation.

[084] The exposed interconnect features, e.g. 111A through 111L may be used to make a variety of electrical connections. For example, the exposed interconnects may be solder plated and then subsequently soldered to a motherboard, e.g. using surface mount soldering techniques. The interconnects may be soldered to a connector, such as connector 103 shown in Figs. 1, 13, 14. Alternatively, a lead frame or PCB may be soldered to the exposed interconnects 111, 112, 113 of the module quickly after singulation. Yet another alternative includes a precious metal such as gold or silver or other suitable conductive material deposited to the exposed contacts, e.g. by plating, to build up the contacts into a larger area, e.g. continuous conductive contacts, well suited to connectorized modules described in more detail below.

G1. Vertical Mount Connector

[085] Referring to Figs. 1, 13 and 14, a connector 103 suitable for attachment to the edge 116 of the module 115 is shown having a connector body 118 with a plurality of recesses 117 and a plurality of holes 119A, 119B, and 119C. A plurality of connector pins 108, 109, 110 may be inserted into holes 119A, 119B, 119C, respectively, from the top 118A. As shown, the holes may be contoured to provide a pressure fit having a gripping force suitable for retaining the pins. The broad top surfaces 108A, 109A, 110A of the pins are suitable for making solder connections to the exposed interconnects 111, 113, 112, respectively on the edge 116 of the PCB 104 of module 115. As shown, the recesses 117 provide countersinking for the top portions of the pins allowing the connector body to mount flush to the edge 116 of module 115 and allowing space for a solder joint between the pin and the respective interconnect. The interconnection features may preferably be provided along a long edge of the module 115 yielding a more stable vertical mount module 100 such as shown in Fig. 1. However, the interconnection

features may be deployed along any or all of the edges of the module 115 for different mounting configurations as discussed more fully below.

G2. Horizontal Through-Hole Mount

[086] Referring to Figs. 15 and 16, a horizontal mount component 200 suitable for through hole mounting in a motherboard is shown including a singulated module 215 and through-hole adapters 203A, 203B. The horizontal mount module 200 may be constructed in the same manner as described above for the module 100, except that the interconnects are preferably disposed along two edges of the module PCB and connectors adapted for horizontal mounting may be used. As shown in Fig. 16, the interconnects are disposed along the two shorter edges of the PCB 204 in module 215. However, the longer edges may be used instead of, or in addition to, the shorter edges for the interconnects. Although only one set of the interconnects 211, 212 is visible in the perspective view of Fig. 16, it will be understood that a second set, including two additional power interconnects, is disposed along the opposite hidden edge of the PCB.

[087] Through-hole adapters 203A and 203B, suitable for attachment to the edges of the singulated module 215 are shown having adapter bodies 218 supporting conductive terminals 208, 210 and 209, respectively. A portion of each terminal may be exposed on an internal surface via an opening in the adapter body optionally providing a small recess. In Fig. 16 for example, adapter 203B is shown having two power terminals 209, each having an exposed areas 209A recessed in openings in surface 218A of the adapter body 218. The exposed areas 209A align with their respective interconnects when the adapters 203A, 203B are assembled onto the module 215. The recesses provide countersinking for the exposed terminals allowing the internal surface 218A of the adapter body 218 to mount flush to the edge of module 215 and allowing space for a solder joint between the terminal and the respective interconnect. The adapter body 218 may include a flange 218B which may form a pressure fit with the adjacent edges of the modules 25. Additional features may be provided for maintaining the structural integrity of the module and connectors.

[088] As shown in Fig. 16, epoxy may be deposited along an internal edge of the connector body, e.g. in the shaded area 219 preferably aligned with the encapsulant layer 206 to secure the adapters 203A, 203B to the module 215. The horizontal mount module 200 may be readily adapted to match industry standard brick footprints for power converters, in particular the module 200 may fit within the standard $1/8^{th}$ brick footprint.

G3. Horizontal Surface-Mount

[089] Referring to Figs. 17 and 18, a horizontal-mount component 300 suitable for surface-mount soldering to a motherboard is shown including a singulated module 315 and surface-mount adapters 303A and 303B. The horizontal-mount module 300 may be constructed in the same manner as described above for the module 200 (Figs. 15, 16) substituting surface mount adapters 303A, 303B for through-hole adapters 203A, 203B. As shown in Fig. 17, the singulated module 315 may have flat heat sinks 301, 302 instead of the finned heat sinks (shown in Figs. 1-4, 6-12, 15-16). Although shown disposed along the two shorter edges in Figs. 17 and 18, the interconnects may be deployed along the longer edges of the PCB 304 in the singulated module 315 instead of, or in addition to, the longer edges.

[090] In Figs. 17 and 18, the surface-mount adapters are shown with smaller bodies 318 than the through-hole adapters (218: Fig. 15, 16) exposing the connections between the terminals and their respective interconnects during assembly and for post assembly inspection. The terminals 308, 309, 310 each may include a portion, e.g. solder pads 308A, 310A, 309A, adapted for connection, such as a solder joint, to a respective interconnect on the module, e.g. interconnect 311, 312, and 313 (not visible in Figs. 17 and 18). Holes 308B, 309B, 310B may be provided in solder pads 308A, 309A, 310A for better solder joints. Each terminal 308, 309, 310 may include a bend (e.g. 308C) to produce a surface-mount pad (e.g. 308D) for attachment, e.g. by surface-mount soldering, to a customer motherboard.

[091] The adapter bodies 318 may include flanges 318B, preferably along two or more sides to form a pressure fit with the adjacent edges of the modules 315. Additional features may be provided for maintaining the structural integrity of the module and

adapters. As shown in Fig. 18, epoxy may be deposited along an internal edge of the connector body, e.g. in the shaded area 319 preferably aligned with the encapsulant layer 306 to secure the adapters 303A, 303B to the module 315.

G4. Surface-Mount Lead Frame

[092] An alternate embodiment of a horizontal-mount component 400 suitable for surface-mount soldering to a motherboard is shown in Figs. 19 and 20 including a singulated module 415. The horizontal-mount module 400 may be constructed in the same manner as described above for the module 300 (Figs. 17, 18) substituting lead frame adapter 403 for the surface-mount adapters 303A, 303B. Like module 315 (Fig. 17), the singulated module 415 may have flat heat sinks 301, 302 instead of the finned heat sinks of the previous examples. However, in the example of Figs. 19 and 20, the interconnects are shown deployed along the longer sides of the singulated module 415. However, as noted above the interconnects may be deployed along any edges of the PCB 404 as desired in the singulated module 415.

[093] The surface-mount adapter is shown in Figs. 19 and 20 having a unitary rectangular frame-like body 418 supporting a plurality of terminals 408. The profile of the frame body 418 may as shown leave a portion of the terminals exposed for making connections to their respective interconnects during assembly and for post assembly inspection. The terminals 408 each may include a portion, e.g. solder pad 408A, adapted for connection, such as a solder joint, to a respective interconnect on the module (not visible in Figs. 19, 20). Although shown without holes in Fig. 19, the solder pads may optionally include holes such as those shown in Figs. 17 and 18. Each terminal 408 may include a bend (e.g. 408C) to produce a surface-mount pad (e.g. 408D) for attachment, e.g. by surface-mount soldering, to a customer motherboard.

[094] The opening in the frame body 418 may be sized to accommodate the perimeter edges of the singulated module 415 and optionally form a pressure fit. The frame body 418 may include recesses 417 for accommodating the terminals 408, allowing the interior surface 418A of the frame body 418 to rest flush against the module 415 surface. Additional features may be provided for maintaining the structural integrity

of the module and adapters. Gaps may be provided in the interior surface 418A to allow the application of epoxy to secure the frame body 418 to the module 415.

G5. Connectorized Module

[095] The modules 100, 200, 300, and 400 discussed above in connection with Figs. 1, and 15-20 are all examples in which connectors or adapters are mechanically and electrically connected to the interconnects on the singulated modules forming an integral modular component. Yet another option is to adapt the module to be removably mated with a connector that may be mounted on a customer circuit board. For example, the module interconnects may be plated up with an appropriate conductive material, such as silver or gold, to form contacts that may be reliably engaged with connector contacts, i.e. "connectorized." Referring to Figs. 21 and 22, a module-connector set 500 is shown including a connectorized module 515 in exploded view with a mating connector 503 into which the module 515 may be removably inserted.

[096] The connector 503 as shown includes a body 518 having side walls 518B creating an opening 518C adapted to receive the connectorized module 515. Terminals 508 formed, e.g. bends 508B (Fig. 22), to provide a pressure fit between a contact area 508A of each terminal 508 and a respective interconnect 511. The terminals as shown may be retained in recesses 517 in the interior surface 518A of the side walls 518B. The recesses 517 may provide support to keep the terminals 508 in place and allow the interior surfaces to engage the surfaces of the module 515. The terminals 508 may include a flat portion 508D (Figs. 22, 23) adapted for making a solder connection to surface contacts on a customer circuit board (not shown). The connector body may include a bottom surface 518D enhancing the structural integrity of the connector walls 518B which are subjected to the forces exerted by the terminals 508 against the interconnects 511. The bottom 518D may include openings as shown in Fig. 23 through which the terminals may be inserted during assembly of the connector 503. The bottom 518D may provide electrical insulation between the metal heat sink 502 and the customer circuit board (not shown) on which the connector 503 may be mounted. Alternatively, the bottom may be partially or completely removed to allow better conduction of heat

from the module 515 out through the customer circuit board. Yet another alternative is to use a thermally conductive material in the bottom 518D of the connector 503. Fig. 24 shows the connectorized module 515 inserted into the connector 503.

[097] As shown, the connector terminals 508 exert inward pressure from opposing ends of the module, however, the contacts may be arranged along a single side of the module with the connector body providing the necessary resistive force for the pressure fit. Although the connectorized module is shown having plated interconnects 511 forming contacts for engagement with the connector terminals, it should be appreciated by those of skill in the art that many variations are possible. For example, adapters of the type illustrated in connection with Figs. 15-20 may be used to provide contacts for a hybrid connectorized module allowing other orientations of the module relative to the connector and to the customer circuit board.

G6. Flush Mount

[098] A flush-mount technique may be used with the horizontal PCB-mounting techniques discussed above in connection with Figs. 15-24 to allow the bottom heat sink to come into contact with the customer PCB, e.g. for heat removal. As shown in Figs. 25 and 26, a through-hole mount module 600 is shown adapted for flush-mounting to a customer PCB 900. The module 600 as shown includes two through-hole adapters 603A, 603B attached to the singulated module 615. The singulated module 615 may, as shown, have a finned top heat sink 601 and a generally flat bottom heat sink 602 for flush mounting against the PCB 900. Similar to the adapters discussed above in connections with Figs. 16-20, through-hole adapters 603A, 603B have terminals, 608, 609, 610 which include features, such as solder pad 608A, adapted to be attached, e.g. by solder, to respective interconnects on the module 615. The terminals 608, 609, 610 may be adapted to be soldered into through holes 908, 909, 910, respectively, in the customer PCB 900. As shown in Figs. 25 and 26, the generally flat heat sink 602 may include recesses 602B to accommodate flanges 618B of the adapter bodies 618 allowing most of the surface of heat sink 602 to rest flush against the surface of the PCB 900. Epoxy or other adhesive may be used in the recess to secure the adapter body to the module. The recesses may be

an integral feature of the heat sink panel or may be added at an appropriate point during the manufacturing process, preferably before singulation.

[099] A thermally conductive material 901, e.g. thermal adhesive, may be applied between the PCB 900 and the module heat sink 602 to facilitate removal of heat through the PCB 900. Additionally, the PCB surface may include thermally conductive features to conduct heat away from the module 615. For some applications particularly involving smaller module sizes, it may be desirable to solder the bottom heat sink 602 to one or more pads on the PCB 900, in which case the heat sink may include a solderable finish, applied for example by plating. Threaded holes may be provided, preferably in the flush mount heat sink panel, allowing the module to be secured using screws to a customer board or cold plate. The flush-mount modification may allow taller heat sink fins to be used on the top of the module without increasing the module profile above the customer PCB which may provide better thermal management in some environments. Additionally, the flush-mount may provide a more robust shock and vibration resistant mechanical solution.

[0100] Another flush mount module 650 may include a plurality of pins 661 protruding from the bottom heat sink 652 for engagement in through holes 911 in the customer mother board 900 as shown in Fig. 25A. Similar to the flush mount module 600 of Figs. 25 and 26, the flush mount module 650 may include adapters 653A and 653B adapted for making electrical connections with through holes on the customer mother board 900. Instead of fins, the top heat sink 651 may include a flat surface to create a low-profile package as shown in Fig. 25A. The pins 661 may be formed as an integral part of the bottom heat sink panel instead of fins. Alternatively, blind holes may be provided in the heat sink panel into which the pins may be press fit at any suitable stage of the fabrication process. The pins 661 may be used to electrically connect the bottom heat sink 652 to the customer board, e.g. to ground, conduct heat out of the module into the customer board 900, and provide mechanical support. The through holes 908, 909, 910, 911 in the customer board may be sized to provide clearance between the hole and the respective pin to compensate for any dimensional variations. The pins 661 may optionally protrude beyond the bottom surface of the customer board 900 into forced

air along the bottom surface of the board for additional heat removal. Additionally, a heat sink component (not shown) may be fitted onto the protruding pins to help dissipate heat.

H. Heat Sink Setback

[0101] As internal components are reduced in height, e.g. reducing the thickness of the magnetic core, the depth of the interior cavity may be decreased bringing the heat sink panels closer together, reducing the encapsulant thickness and the resulting module thickness. However, reduction of the encapsulant thickness has the potentially undesirable effect of reducing the spacing between the electrical interconnects and the edges of the heat sink panels in the finished module. When desirable, e.g. to satisfy safety agency requirements, the separation between the exposed interconnects, e.g. interconnects 111, 112, 113, and the edge of the heat sink, e.g. heat sink 101B, may be increased using a setback, e.g. setback 155, between the edges of the heat sink panels and the edges of the module 115B as shown in Fig. 10B. The setback 155 may be created by making wide cuts through the heat sink panels 121, 122 along the singulation lines prior to singulation. The wide cuts preferably extend through the heat sink material, e.g. aluminum, and partially into the encapsulation material to form channels 128A and 129A in the panel assembly 120A as shown in Figs. 9B and 9C. If machined while the assembly is still hot from the encapsulation process, the channels 128A and 129A may be used to divide the heat sink panels into singulated module dimensions reducing stresses due to differential contraction between the heat sink and the encapsulant due to differences in thermal coefficients of expansion while the panel assembly cools. Stresses on the narrow saw may also be reduced by eliminating the heat sink metal through which the saw must cut during singulation as a result of the channels 128A, 129A.

I. Process Efficiencies

[0102] Using interconnection features that may be exposed during singulation allows the PCB panel 124, containing a plurality of modules, to be molded as a single unit. Providing embedded interconnects along the perimeter of the circuit that occupy little or no PCB surface area help reduce wasted PCB area that would otherwise be cut away,

allowing close to full utilization of the PCB for product which may save on cost. Encapsulating the PCB panel with the heat sink panels simplifies the structural aspects of the modules. Using interior contours in the heat sink to match component heights helps reduce the amount of molding compound required for encapsulation. Furthermore, controlling the distance between the magnetic cores and the internal surface of the heat sink can be used as an alternative to and eliminating the complications of the exposed core molding process described in the Exposed Core Application.

[0103] Furthermore, using the mold panels to form the mold cavity for encapsulating the PCB panel helps free the molding equipment from product specific requirements that may otherwise require customized molds, allowing a single piece of molding equipment to be used for a wide variety of product mixes. The finished products, e.g. modules 115 made using a standard panel size, may have diverse dimensions not only in the lateral (length and width) directions, but also in the vertical (thickness) direction (e.g. due to heat sink fin height or component thickness). However, because the lateral panel dimensions remain the same, and variations in thickness from panel to panel may be accommodated by the molding press, the same general purpose molding equipment may be used for a wide variety of products of diverse dimensions. Using power converters as an example, the same mold press may be used to encapsulate panels of power converters ranging in (1) footprint size from full size, to half, to quarter, to eighth size (or any other size), and in (2) thickness (height), and in (3) topology, e.g. isolated DC-DC regulating converter, non-isolated buck regulator, DC transformer, etc. to produce a large mix of products.

[0104] A panel molding manufacturing process for a mix of products may include some or all of the following steps. Select a specific product to build. Select the requisite blank heat sink panels, e.g. based upon fin orientation, spacing, and height for the specific product. Alternatively, machine the exterior of the heat sink blank panels to produce the requisite external surface (heat sink surface, mounting features such as threaded holes, fin orientation, thickness, and spacing). Machine the interior surfaces of the heat sink blanks to form the recesses and other features (i.e. the contours of interior cavity to match some or all component locations, size, and height), of the finished heat

sink panels required for the specific product, preferably under computer control. Select the appropriate PCB panel for the specific product. Select and assemble the magnetic cores and other components onto the PCB panel, e.g. by surface mount soldering, etc. Dispense a measured quantity of molding compound into the bottom heat sink panel. Press the bottom side of PCB panel up against bottom heat sink panel. Dispense a measured quantity of molding compound on the top side of the PCB panel. Press top heat sink panel into place on the PCB panel. Place the panel assembly on a rotary table away from the axis of rotation, preferably a large distance from the axis, and spin the rotary table and panel assembly to evacuate air bubbles in the interior cavity to achieve essentially void free fill of panel assembly with molding compound. Cure the molding compound. Cut the panel along the cut lines for singulation. Apply a conformal coating to protect the interconnects, or plate the interconnects, or attach a lead frame, motherboard, or connector to the exposed interconnects.

J. PCB Symmetries

[0105] The components may be symmetrically arranged on the PCB such as shown in the power converter example of Fig. 27. The top 104-2 and bottom 104-1 faces of a populated PCB 104 from an individual power converter module are shown in plan view in Fig. 27. The populated PCB 104 is shown rotated along the vertical axis 27 in Fig. 27 to show the symmetry of the components.

J1. Symmetrical Distribution between PCB Surfaces

[0106] Many of the larger components may be distributed equally between both faces of PCB 104 as shown in Fig. 27. For example, the four input field effect transistors (FETs) 132-2D, 132-2E, 132-1D, 132-1E are shown equally distributed between the top 104-2 and bottom 104-1 surfaces with two FETs on each surface. Similar equal distribution between the top 104-2 and bottom 104-1 surfaces of the PCB 104 are shown for the eight output FETs 132-2B, 132-2C, 132-1B, 132-1C with four output FETs on each surface; the twelve input capacitors, 132-2F, 132-2G, 132-1F, 132-1G, with six input capacitors on each surface; and twenty four output capacitors 132-2A, 132-1A with twelve output capacitors on each surface. Some of the FETs can function as switches.

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Distributing larger components between the two surfaces of the PCB may decrease stresses on the PCB, e.g. due to differences in the coefficient of expansion of the encapsulant, e.g. while curing, which may improve the co-planarity and mechanical integrity of the device.

J2. Symmetrical Distribution on a PCB Surface

[0107] On each surface of the PCB, components having similar characteristics, such as size or in-circuit power dissipation, may be arranged symmetrically for example as shown in Fig. 27 with respect to horizontal axis 28. It can be seem that relative to the horizontal axis 28, which is drawn longitudinally through the midline of the top and bottom surfaces of PCB 104, many of the components are arranged symmetrically. For example, the six input capacitors 132-1F and 132-1G on the bottom surface 104-1 are symmetrically distributed in a mirror-image relationship to each other relative to longitudinal midline axis 28. The same basic mirror image relationship is true for the six input capacitors 132-2F and 132-2G on the top 104-2 surface of the PCB. Similarly, the mirror image relationship is shown for the following pairs of components: bottom-side input FETs 132-1D and 132-1E, topside input FETs 132-2D and 132-2E, bottom-side output FETs 132-1B and 132-1C, topside output FETs 132-2B and 132-2C and also within the bottom-side and top-side banks of output capacitors 132-1A and 132-2A.

[0108] Distributing larger components symmetrically on a surface especially with respect to the longitudinal axis of the PCB may also decrease stresses on the PCB, e.g. due to differences in the coefficient of expansion of the encapsulant, e.g. while curing, which may also improve the mechanical integrity of the device. Additionally, spreading the components out symmetrically on each surface helps to spread the heat produced by power dissipating devices using a greater surface area for heat extraction improving the thermal performance.

J3. Symmetrical Footprints between PCB Surfaces

[0109] In addition to being equally distributed between the top and bottom surfaces and being symmetrically distributed on each PCB surface, the components may also be

situated such that pairs of components (wherein each component on one surface has a respective counterpart on the other surface) may be arranged to occupy essentially the same space on the PCB, i.e. a component may occupy a space on one surface that substantially overlaps with the footprint of a component on the other surface. For example, input capacitors 132-1F on the bottom surface are in the same position as their counterparts 132-2F on the top surface, i.e. they share the same footprint on the PCB. The same relationship is generally true for: input capacitors 132-1G and 132-2G; output capacitors 132-1A and 132-2A; input FETs 132-1D and 132-2D; input FETs 132-1E and 132-2E; output FETs 132-1B and 132-2B; output FETs 132-1C and 132-2C; in which the pairs of components occupy the same basic footprint, albeit on opposite surfaces, of the PCB. One benefit of sharing footprints allows the pair of components to share a common set of conductive vias used to electrically connect the components on the PCB surfaces to internal conductive layers, e.g. used to form the windings of the transformer. Because each via is used for both components in the pair, the total number of vias for making connections to the pair of components may be reduced (by as much as a factor of two) increasing the area of conductive layers useable for making connections and thus reducing resistance. For example, assuming 6 vias are required for each output FET (a total of 12 vias for two FETs), using symmetrical footprint approach, the pair of FETs can share the same 6 vias (without increasing the via resistance) and because the number has been reduced the useable area for conductors may be increased. Alternatively, while reducing the total number of vias from 12 to some intermediate number, e.g. 8, the resistance of the vias may be decreased because of the increase in effective vias per FET while still increasing the area useable for conductors.

J4. Symmetrical Power Dissipation between PCB Surfaces

[0110] The components may be arranged between the PCB surfaces according to heat dissipated during operation. For example, the heat dissipative components may be arranged in a manner that distributes the heat evenly between the two PCB surfaces allowing heat produced by power dissipating devices to be extracted from both surfaces of the PCB improving the thermal performance. This type of heat dissipation symmetry is also factored into the component layout shown in the power converter of Fig. 27. For

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example, two input cells each using the same basic circuit topology are shown, one above and another below axis 28. As shown, the components of each input cell occupy both sides of the PCB in observance of other factors influencing component layout such as winding locations, etc. In this example, the upper input cell includes the two input FETs 132-1D and 132-2D, and the six input capacitors 132-1F and 132-2F. The lower input cell includes the two input FETs 132-1E and 132-2E, and the six input capacitors 132-1G and 132-2G. To ensure heat dissipation symmetry between the two surfaces, the cells may be arranged in mirror image layouts as shown. In Fig. 27, input FET 132-2E (top surface) in the lower cell corresponds to input FET 132-1D (bottom surface) in the upper cell. Similarly, lower cell input FET 132-1E (bottom surface) corresponds to upper cell input FET 132-2D (top surface). As can be seen, the significant power dissipative components of the input cells are arranged to have one component of one cell mounted on one surface with the respective component from the other cell mounted on the other surface. This type of symmetry may be seen in Fig. 27 with lower cell component 132-2H mounted on the top surface and the respective upper cell component 132-1H mounted on the bottom surface. In some examples, the FETs are arranged such that during operation, the power FETs on the top surface dissipate power at a level that is comparable to the level of power dissipated by the power FETs on the bottom surface. Also, the level of power dissipated by the power FETs in the upper input cell is comparable to the level of power dissipated by the power FETs in the lower input cell. For example, the level of power dissipated by the power FETs on one surface is less than 150% of the level of power dissipated by the power FETs on the other surface. The level of power dissipated by the power FETs in the upper cell is less than 150% of the level of power dissipated by the power FETs in the lower cell, and vice versa.

[0111] Laying out the components using any or all of the above symmetries produces several key benefits including, enhanced thermal performance, reducing top to bottom and side to side imbalances during encapsulation caused by asymmetrical distribution of components may enhance the co-planarity and structural integrity, and shared component footprints on top and bottom PCB surfaces may help reduce conduction losses and increase efficiency.

K. Center Plate Panel Assembly

[0112] In an alternate embodiment, an optional center plate 727 may be used between the top 721 and bottom 722 heat sink panels as illustrated in Fig. 28 through Fig. 32. The center plate 727, which may be made from aluminum, a molded high temperature plastic or any other material suitable for the molding process, includes an opening 729 in which the populated PCB panel 724 may sit during the panel molding process. As shown in the side view of Fig. 29 and the cross-sectional view of Fig. 32, the PCB panel 724 may sit entirely within the opening 729 and may have some high profile components, such as magnetic cores 131 and capacitors 132 (continuing with the power converter example), extending beyond the planar surfaces of the center plate. The recesses formed in the interior surfaces of the heat sink panels 721, 722 (described above) may accommodate portions of the components extending beyond the center plate surface. Conversely, protrusions from the interior surface of the heat sink panels may be used to reduce the distance between the heat sink and lower profile components. However, it may be preferable for ease of fabrication and tolerance control to avoid protrusions of the heat sink beyond the surface of the center plate which may put an upper limit on the thickness of the center plate in some embodiments.

[0113] As shown in the exploded perspective view of Fig. 28 and the top plan view of Fig. 31, registration features may be provided in the center plate 727. For example, registration pins 728 may mate with corresponding holes 734 in the PCB 724 to establish the horizontal position, i.e. in the X and Y directions, of the PCB relative to the center plate 727. Additional registration features such as the illustrated horizontal shelf 728A (Fig. 28), may be provided to establish the vertical position, i.e. in the Z direction, of the PCB relative to the center plate. The registration pins 728 may be long enough to extend beyond the upper surface of the PCB panel 724 in the upward direction and beyond the horizontal shelf in the downward direction to mate with holes (analogous to holes 152 and 153 in Fig. 4B) which may be provided in the top and bottom heat sink panels 721, 722 establishing the horizontal positions of the mold panels relative to the center plate 727. Provision of the registration features in the center plate may help relax certain precision requirements, the complexity, and thus the cost of the heat sink panels.

[0114] A cross-section of the panel assembly 720 closed in a mold press taken through line 32-32 in Figs. 30 and 31 is shown in Fig. 32. As shown, the upper mold press 761 engages the center plate 727 directly along its perimeter in regions 768 and engages the heat sink panels directly along their perimeters in regions 769. Preferably the mold press includes recessed surfaces 766 providing cavities 765 large enough to accommodate a full range of fin heights (or other heat sink panel features) supporting a diverse range of products. To compensate for dimensional differences between the thickness of the heat sink panels in regions 769 and the difference in elevation between interface regions 768 and 769 in the mold press, one or more compressible features may be provided at the interface between the heat sink panels 721, 722 and the center plate 727. For example, a small crushable feature 723 may be formed along the perimeter of and as an integral part of the heat sink panels as illustrated in Fig. 32. Alternatively a gasket may be used between the center plate and one or both of the heat sink panels. As the press closes on the panel assembly 720 the crushable features 723 are compressed until the press is closed securely against both the center plate 727 and the heat sink panels 721, 722. As shown in Fig. 31, the crushable features may extend along the perimeter of the interior cavity forming a seal between each heat sink panel and the center plate.

[0115] The center plate may preferably include an extension, e.g. extension 730, to at least one side of opening 729 providing space for one or more chambers 725 as shown in Figs. 30, 31, and 32. During the transfer molding process, encapsulation material may be forced from the chambers through one or more channels 726 (as shown in Figs 28 and 32) in the center plate into opening 729 and thus the cavity in which the populated PCB panel 724 is enclosed. An example of encapsulant flow through a chamber 725, channel 726, and into the interior cavity 746 is illustrated by the arrows 767 shown in Fig. 32.

[0116] In the center plate panel mold assembly, the top and bottom mold panels (i.e., heat sink panels 721, 722) close against the center plate instead of each other, reducing the thickness of the top and bottom mold panels, increasing the symmetry between, and reducing the complexity of, the top and bottom heat sink panels 721, 722, potentially simplifying the molding press, eliminating critical tolerance accumulations in the assembly, simplifying the process and reducing cost. For example, provision of the

chambers 725 and conduits 726 in the center plate 727 eliminates the need for sealing along a second axis, e.g. in a horizontal direction and allows for use of a simpler cull-on-plate molding press. Critical tolerances are reduced to the one vertical dimension of the heat sink panels which can be relaxed using a crushable feature or a compliant material on the surface that interfaces with the center plate. Additionally, the center plate 727 may be standardized allowing a single configuration to be used with a large variety of heat sink panels such that the center plate may be cost-effectively molded.

[0117] A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, non-metallic mold panels may be used. The center plate may be provided as a single-use consumable or may be modified to be used as a reusable fixture in the molding process. The center plate may be provided with or without the encapsulation channels. The registration holes in the heat sink panels may extend completely through the heat sink panels similar to hole 152 shown in Fig. 4B and the registration pins, e.g. pins 728 (Figs. 28 and 31), may extend completely through each of the heat sink panels allowing fasteners to be used in conjunction with the pins to hold the panel assembly together before and after the encapsulation process. The fasteners may function as or be used in conjunction with a seal around the pin to contain any encapsulant. Throughput through the mold press may be increased by using panel assemblies that are secured together and removed from the mold press before the panel has cooled or the encapsulant has set or both. The registration pins 728 and corresponding holes 734 may be used to align the panel assembly during the singulation process. In some examples, a panel assembly (e.g., 120) may be formed by dispensing encapsulant into a bottom panel mold (e.g., heat sink panel 122), assembling a substrate (e.g., PCB panel 124) into the bottom panel mold, dispensing encapsulant onto a top of the substrate, and assembling a top panel mold (e.g., heat sink panel 121) onto the substrate. In some examples, the surfaces of the PCB panel 124 may have conductive features that are covered by an insulative layer. Blank mold panels may be machined to provide some or all of the various features described above in an on-demand manufacturing system.

[0118] In some examples, the upper and lower heat sinks 121, 122 are clamped together by the upper and lower mold presses 161, 162 at respective clamp regions of the upper and lower heat sinks 121, 122. The clamp region of the upper heat sink 121 can be located at points along a circumference of an internal cavity defined by the interior surface of the upper heat sink 121. The clamp region of the lower heat sink 122 can be located at points along a circumference of an internal cavity defined by the interior surface of the lower heat sink 122. In some examples, the clamp regions are cut away from the panel assembly 120 to expose the interconnects 111, 112, and 113. After the cut, portions of the upper and lower heat sinks 121, 122 near an active circuit area remain attached to the panel assembly 120, allowing heat from the active circuit area during operation to be dissipated through the remaining portions of the upper and lower heat sinks 121, 122. The active circuit area can be, e.g., an area of the PCB panel 124 having active components, such as magnetic core structures 131 and electronic components 132. Interlocking contours, other than the undercuts 148 shown in Figs. 6, 7, and 12, can also be formed in the interior surface of the mold panel, the contour being filled with cured mold compound enhancing the structural integrity of the singulated module. In some examples, most of the large-footprint components (e.g., 132-2D, 132-2E, 132-2B, 132-2C) are distributed substantially symmetrically between quadrants surrounding the transformer core (e.g., 131-2) on a surface of the PCB panel 124. For example, in FIG. 27, the input FETs 132-2D and 132-2E are distributed substantially symmetrically between the upper-right and lower-right quadrants surrounding the transformer core 131-2. The output FETs 132-2B and 132-2C are distributed substantially symmetrically between the upper-left and lower-left quadrants surrounding the transformer core 131-2.

[0119] Accordingly, other embodiments are within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A method of making a plurality of electronic devices, comprising:

providing a plurality of mold panels, which when assembled, form an internal chamber;

providing a substrate having a plurality of conductive traces and a plurality of components electrically connected to form at least one circuit, the substrate having at least one contact for making an electrical connection to the circuit;

forming a panel assembly including the mold panels assembled with the substrate in the internal chamber and an encapsulant filling spaces between the substrate and interior surfaces of the chamber;

curing the encapsulant; and

cutting the panel assembly to expose at least a portion of the at least one contact and form a respective exposed contact.

2. The method of claim 1 wherein the cutting comprises making a first cut in at least one of the mold panels, and in the first cut, making a second narrower cut through the panel assembly.

3. The method of claim 2 wherein the curing comprises raising the temperature of the panel assembly and the first cut is made before the panel assembly cools after the curing.

4. The method of claim 1 wherein the cutting divides the panel assembly producing at least one module having a plurality of layers including respective portions of each of the panel molds, the substrate, and the encapsulant, and the module contains the at least one circuit.

5. The method of claim 4 wherein the cutting defines at least one side of the module.

6. The method of claim 4 wherein the cutting defines two or more sides of the module.

7. The method of claim 1 further comprising treating the exposed contact to protect against oxidation.

8. The method of claim 7 wherein the treating comprises applying a removable conformal coating to the exposed contact.

9. The method of claim 7 wherein the treating comprises applying a layer of metal to the exposed contact.

10. The method of claim 9 wherein the applying a layer of metal comprises applying solder.

11. The method of claim 9 wherein the applying a layer of metal comprises applying a precious metal.

12. The method of claim 9 wherein the applying a layer of metal comprises plating.

13. The method of claim 4 further comprising

providing an adapter having at least one electrical terminal; and

attaching the at least one electrical terminal to the exposed contact.

14. The method of claim 13 wherein

the at least one contact comprises a plurality of contacts;

the module comprises a plurality of exposed contacts;

the adapter has a plurality of electrical terminals arranged to match respective ones of the plurality of exposed contacts; and

the adapter is mechanically secured to the module.

15. The method of claim 4 wherein the mold panels are metal.

16. The method of claim 15 wherein the respective portions of the mold panels provide heat sink surfaces for the module.

17. The method of claim 1 wherein the providing mold panels further comprises providing contours in an internal surface of one or more of the mold panels.

18. The method of claim 17 wherein the providing contours further comprises matching depths of portions of the internal surface to heights of one or more selected components.

19. The method of claim 18 wherein the selected components include at least one magnetically permeable core and at least one semiconductor device.

20. The method of claim 4, wherein the traces and components are electrically connected to form a plurality of separable circuits arranged in a pattern on the substrate; and the cutting divides the panel assembly along spaces between the separable circuits into a plurality of modules each containing at least one respective circuit.

21. The method of claim 20 wherein the spaces between the separable circuits have dimensions approximately matching a width of cuts produced by equipment used to cut the panel assembly.

22. The method of claim 21 wherein the at least one contact comprises a plurality of contacts located in the spaces between the separable circuits.

23. The method of claim 22 wherein the plurality of contacts are formed in the substrate.

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24. The method of claim 23 wherein the plurality of contacts are formed and buried below at least one surface of the substrate.

25. The method of claim 15 further comprising treating at least one exterior surface of at least one of the mold panels for solderability.

26. The method of claim 1 wherein forming the panel assembly comprises:

dispensing encapsulant into a bottom panel mold;

assembling the substrate into the bottom panel mold;

dispensing encapsulant onto a top of the substrate; and

assembling a top panel mold onto the substrate.

27. The method of claim 26 further comprising centrifuging the assembly before curing the encapsulant.

28. The method of claim 1 wherein forming the panel assembly comprises:

assembling the substrate with a first substrate surface facing into a first panel mold,

closing a second panel mold onto the substrate covering a second substrate surface,

providing one or more conduits to the internal chamber, and

forcing encapsulant through the one or more conduits into the chamber.

29. The method of claim 28 further comprising centrifuging the assembly before curing the encapsulant.

30. The method of claim 9 further comprising providing a connector for removably mating with and providing electrical connection to the metal.

31. The method of claim 1 further comprising:

providing a center plate having an opening to accommodate the substrate; and

wherein the forming a panel assembly includes positioning the substrate in the opening of the center plate and closing the mold panels against the center plate.

32. The method of claim 31 further comprising providing at least one opening in the center plate connected to the internal chamber by at least one conduit; and

forcing the encapsulant through the at least one opening and at least one conduit into the internal chamber.

33. The method of claim 32 wherein the forming a panel assembly further comprises securing the mold panels together prior to curing the encapsulant.

34. A method of forming an electrical contact comprising:

assembling a panel including a substrate having one or more conductive features enclosed within the panel and unexposed to an exterior surface of the panel, the one or more conductive features being located along a cut line;

cutting the panel along the cut line exposing portions of the one or more conductive features for use as electrical connections to the substrate; and

treating the portions of the one or more conductive features exposed from the cutting for preservation as electrical connections.

35. The method of claim 34 wherein the treating further comprises applying solder to the portions of the one or more conductive features exposed from the cutting.

36. The method of claim 34 wherein the treating further comprises applying a conformal coating to the portions of the one or more conductive features exposed from the cutting to protect against oxidation.

37. The method of claim 34 wherein the treating further comprises applying a metal layer to the portions of the one or more conductive features exposed from the cutting.

38. The method of claim 34 wherein the treating further comprises soldering a lead of an adapter to the portions of the one or more conductive features exposed from the cutting.

39. The method of claim 34 further comprising covering at least one surface of the substrate in an area including the cut line and the conductive features prior to cutting the substrate.

40. The method of claim 39 wherein the covering comprises encapsulating the substrate with a molding compound; and further comprising:

providing a registration feature having a predetermined relationship to the substrate, and

using the registration feature to align the cutting relative to the cut line.

41. The method of claim 34 further comprising establishing a pattern including at least one conductive layer in the substrate along the cut line to form the conductive features.

42. The method of claim 41 wherein the substrate comprises a multilayer printed circuit board and the establishing a pattern includes establishing a plurality of conductive layers along the cut line to form the conductive features.

43. The method of claim 34 further comprising establishing a pattern including at least one conductive via in the substrate along the cut line to form the conductive features.

44. The method of claim 43 wherein the conductive via is filled with a conductive material.

45. The method of claim 43 wherein the conductive via is buried in the substrate.

46. The method of claim 43 wherein the conductive via is a through hole contacting the surfaces of the substrate.

47. The method of claim 46 wherein the through hole is filled with a conductive material.

48. The method of claim 34 wherein the conductive features are covered at the surfaces of the substrate by an insulative layer.

49. An apparatus comprising:

a first mold panel comprising

an exterior surface,

an interior surface defining an internal cavity,

a clamp region located at points along a circumference of the internal cavity, and

an opening,

the first mold panel being adapted to

(a) be engaged by pressure in the clamp region,

(b) receive in the cavity a circuit panel containing a plurality of components and mold compound to fill empty spaces in the internal cavity, and

(c) be cut after curing of the mold compound.

50. The apparatus of claim 49 wherein the interior surface in the region of the internal cavity is adapted to adhere to the mold compound.

51. The apparatus of claim 49 further comprising

a second mold panel comprising

an exterior surface,

an interior surface, and

a clamp region,

wherein the second mold panel is adapted to

(a) close against and mate with the first mold panel,

(b) be engaged by pressure in the clamp region, and

(c) be cut after curing of the mold compound.

52. The apparatus of claim 51 wherein the interior surface of the second mold further defines a second internal cavity, the clamp region of the second mold panel is located at points along a circumference of the second internal cavity, and the internal cavity of the first mold panel is adapted to receive a first side of the circuit panel and the second internal cavity is adapted to receive a second opposite side of the circuit panel.

53. The apparatus of claim 52 further comprising contours formed in the interior surface of at least one of the mold panels.

54. The apparatus of claim 53 wherein the contours are adapted to match predetermined characteristics of selected ones of the plurality of components.

55. The apparatus of claim 53 wherein the internal surface of the mold panel is adapted to adhere to the molding compound.

56. The apparatus of claim 55 wherein the contours form interlocking features with cured mold compound.

57. The apparatus of claim 53 wherein at least one of the mold panels comprises a non-ferrous metal.

58. The apparatus of claim 57 wherein at least one of the mold panels comprises aluminum.

59. The apparatus of claim 51 wherein at least one of the mold panels comprises a thermally conductive material.

60. The apparatus of claim 53 wherein at least one of the mold panels comprises a non-metallic substance.

61. The apparatus of claim 51 further comprising at least one channel connected to the internal cavity for allowing expansion of the mold compound.

62. The apparatus of claim 51 further comprising at least one channel connected to the internal cavity for injecting mold compound into the internal cavity.

63. The apparatus of claim 59 wherein the exterior surface of the mold panel comprises a plurality of fins.

64. The apparatus of claim 59 wherein the exterior surface of the mold panel comprises a flat surface.

65. The apparatus of claim 64 wherein the flat surface is adapted for a solder joint.

66. The apparatus of claim 49 wherein the internal cavity includes features formed in the interior surface and arranged in a predetermined pattern.

67. The apparatus of claim 49 wherein the internal cavity includes features formed in the interior surface along lines through which the mold panel maybe cut to establish a setback from a cut edge of the mold panel.

68. The apparatus of claim 49 wherein the mold panel further comprises at least one registration feature adapted to engage and establish a predetermined relationship with the circuit panel.

69. The apparatus of claim 49 wherein one or more selected portions of the mold panel are adapted for incorporation into one or more products, the products being formed by a process which uses the mold panel to contain the molding compound.

70. The apparatus of claim 59 wherein the exterior surface of the mold panel comprises a flat surface with one or more pins protruding from the flat surface.

71. The apparatus of claim 59 wherein the exterior surface of the mold panel comprises a flat surface having one or more holes in the flat surface.

72. The apparatus of claim 71 further comprising a pin inserted into a respective one of the one or more holes.

73. An apparatus comprising:

a panel assembly having external surfaces defined by a first mold panel and a second mold panel;

the first and second mold panels forming an internal cavity enclosing an internal circuit board, the internal circuit board having a first surface and second surface and a plurality of components in an active circuit area on at least one of the surfaces, the components being electrically connected to interconnects contained within the internal cavity;

the internal cavity being filled with mold compound in spaces unoccupied by the circuit board and components;

the panel assembly being adapted to have first selected portions of the first and second mold panels cut away to expose the interconnects and to have second selected portions of the respective mold panels situated near the active circuit area remain attached to the assembly following the cut.

74. The apparatus of claim 73 wherein the panel assembly includes a clamp region located at points along a circumference of the first and second internal cavities, and the first selected portions comprise the clamp region.

75. An apparatus comprising:

a panel assembly having external surfaces defined by a first mold panel and a second mold panel;

the first and second mold panels forming an internal cavity enclosing an internal circuit board, the internal circuit board having a first surface and second surface and a plurality of components electrically connected to form a plurality of individual circuits, each individual circuit being electrically connected to respective interconnects located along a respective circuit perimeter, the interconnects being contained within the cavity.

76. The apparatus of claim 75 wherein the panel assembly is adapted to be cut along the circuit perimeter separating the individual circuits, dividing the panel assembly into individual circuit modules, and exposing selected portions of the interconnects.

77. The apparatus of claim 75 wherein the panel assembly is constructed to retain an integral layered structure after being filled with mold compound which is subsequently cured, the layered structure comprising a first layer including a portion of the first mold, a second layer including a portion of the mold compound, a third layer including a portion of the circuit board, a fourth layer including a portion of the mold compound, and a fifth layer including a portion of the second mold.

78. The apparatus of claim 75 wherein the internal circuit board comprises a plurality of circuits having the same functionality.

79. The apparatus of claim 75 further comprising one or more conduits connecting the internal cavity to an external opening.

80. The apparatus of claim 75 wherein spaces unoccupied by the circuit board, components, and interconnects in the internal cavity are filled with mold compound.

81. The apparatus of claim 80 wherein the mold compound has been cured.

82. The apparatus of claim 81 wherein selected portions of at least one of the mold panels have been removed, the selected portions being located near the circuit perimeters.

83. An apparatus comprising:

a modular package having a first external surface, a second external surface opposite the first external surface, and a side wall extending along the perimeter of and connecting with the first and second external surfaces, the modular package including a first layer defining the first external surface and a second layer defining the second external surface, the first and second layers being separated by and in contact with cured mold compound; and

an electrical circuit located between the first and second layers and within the cured mold compound and including at least one electrical component electrically connected to a plurality of interconnects;

the side wall comprising a strip formed by the first layer, a strip formed by the second layer, and a strip formed by the cured mold compound; and

the interconnects being disposed within the side wall.

84. The apparatus of claim 83 wherein the first and second layers further comprise a non-ferrous metal.

85. The apparatus of claim 84 wherein the first and second layers further comprise aluminum.

86. The apparatus of claim 85 wherein the first external surface further comprises a plurality of fins.

87. The apparatus of claim 85 wherein the first external surface further comprises an essentially flat area.

88. The apparatus of claim 87 wherein the essentially flat area is adapted for a solder joint.

89. The apparatus of claim 83 wherein the electrical circuit further comprises a circuit board and the side wall further comprises a strip formed by the circuit board and an additional strip formed by cured mold compound.

90. The apparatus of claim 89 wherein the interconnects further comprise conductive features in the circuit board.

91. The apparatus of claim 90 wherein the circuit board comprises a multilayer printed circuit board ("PCB") and each of the interconnects comprises a plurality of conductive layers in the PCB.

92. The apparatus of claim 90 wherein each of the interconnects comprises a plurality of conductive vias in the circuit board.

93. The apparatus of claim 83 further comprising interlocking features comprising a contour formed in an interior surface of the first layer, the contour being filled with cured mold compound.

94. The apparatus of claim 91 wherein the circuit board includes a top surface and a bottom surface and the at least one electrical component comprises a set of top-side components mounted on the top surface and a set of bottom-side components mounted on the bottom surface.

95. The apparatus of claim 94 wherein

the top-side components include a number, T, of large-footprint components, the bottom-side components include a number, B, of large-footprint components, and the number T is approximately equal to the number B.

96. The apparatus of claim 95 wherein each of most of the top-side large-footprint components shares a respective set of conductive vias with a corresponding one of the bottom-side large-footprint components.

97. The apparatus of claim 95 wherein each of most of the top-side large-footprint components is located in a respective footprint shared by a corresponding one of the bottom-side large-footprint components.

98. The apparatus of claim 89 wherein the circuit board includes a top surface and a bottom surface, the at least one electrical component comprises a number, T, of large-footprint components mounted on the top surface, and most of the large-footprint components are distributed symmetrically in relation to an axis on the top surface.

99. The apparatus of claim 98 wherein the axis is along a midline of the top surface.

100. The apparatus of claim 98 wherein the axis is defined in relation to a predetermined component.

101. The apparatus of claim 83 further comprising:

an adapter for providing mechanical and electrical connections between the modular package and an external mounting surface, the adapter having a body and a plurality of electrical terminals supported by the body; and

electrical connections formed between the adapter terminals and respective interconnects on the modular package;

the adapter body being mechanically secured to the modular package;

the adapter terminals being arranged to mate with the external mounting surface.

102. The apparatus of claim 101 wherein the external mounting surface is a circuit board and the terminals comprise ends constructed and arranged to be inserted into conductive holes in the circuit board.

103. The apparatus of claim 101 wherein the external mounting surface is a circuit board and the terminals comprise ends constructed and arranged to be surface mount soldered to the circuit board.

104. The apparatus of claim 101 wherein the external mounting surface includes a connector and the terminals comprise ends constructed and arranged to mate with the connector.

105. The apparatus of claim 101 wherein the interconnects are disposed along a long edge of the modular package, the adapter is secured to the long edge of the modular package, and the first and second layers of the modular package are oriented perpendicular to the mounting surface.

106. The apparatus of claim 101 wherein the interconnects are disposed along opposite edges of the modular package, the adapter is secured to the opposite edges, and the first and second layers of the modular package are oriented essentially parallel to the mounting surface.

107. The apparatus of claim 106 wherein the adapter is constructed and arranged to maintain one of the first or second layers in contact with the mounting surface.

108. The apparatus of claim 83 wherein the interconnects further comprise a surface constructed and arranged for engagement with a connector terminal.

109. The apparatus of claim 83 wherein the interconnects further comprise a layer of metal plating.

110. An apparatus comprising:

a modular package having a first external surface, a second external surface opposite the first external surface, and a side wall extending along the perimeter of and connecting with the first and second external surfaces, the modular package including a first layer of metal defining the first external surface and a second layer of metal defining the second external surface, the first and second layers being separated by and in contact with cured mold compound; and

an electrical circuit for converting power, including a printed circuit board ("PCB"), a plurality of components including semiconductors mounted to the PCB, and a plurality of interconnects electrically connected to the components, the electrical circuit being located between the first and second layers and within the cured mold compound;

the side wall comprising a strip formed by the first layer, a strip formed by the second layer, a strip formed by the PCB, and one or more strips formed by the cured mold compound;

the interconnects being disposed within the side wall.

111. The apparatus of claim 110 wherein the first and second layers further comprise aluminum, and the first external surface further comprises a plurality of fins.

112. The apparatus of claim 110 wherein the first and second layers further comprise aluminum, and the first external surface comprises an essentially flat area.

113. The apparatus of claim 112 wherein the essentially flat area is adapted for a solder joint.

114. The apparatus of claim 110 wherein the PCB includes a top surface and a bottom surface, the semiconductors include large-footprint switches, a number, T, of top-side large-footprint switches are mounted on the top surface, a number, B, of bottom-side large-footprint switches are mounted on the bottom surface, and the number T is approximately equal to the number B.

115. The apparatus of claim 114 wherein each large-footprint switch is connected to one or more other components by a respective set of conductive vias in the PCB, and each of a plurality of the top-side large-footprint switches shares its respective set of conductive vias with a corresponding one of the bottom-side large-footprint switches.

116. The apparatus of claim 114 wherein each of most of the large-footprint switches is positioned on one surface in a location substantially overlapping a location on the other surface occupied by another large-footprint switch.

117. The apparatus of claim 110 wherein the PCB includes a top surface and a bottom surface, the semiconductors include large-footprint switches mounted on the top surface, most of the large-footprint components are distributed symmetrically between a left side of the top surface and an opposite right side of the top surface.

118. The apparatus of claim 110 wherein the PCB includes a top surface and a bottom surface, the semiconductors include large-footprint switches mounted on the top surface, and most of the large-footprint components are distributed symmetrically between quadrants on the top surface.

119. The apparatus of claim 118 wherein the components further comprise a transformer core, and the quadrants surround the transformer core.

120. The apparatus of claim 110 wherein the PCB includes a top surface and a bottom surface, the components include a set of high-profile components having similar heights, a number, T, of the high-profile components are mounted on the top surface, a number, B, of the high-profile components are mounted on the bottom surface, and the number T is approximately equal to the number B.

121. The apparatus of claim 120 wherein a spatial distribution of the high-profile components on the top surface roughly matches a spatial distribution of the high-profile components on the bottom surface.

122. The apparatus of claim 110 further comprising:

an adapter for providing mechanical and electrical connections between the modular package and an external mounting surface, the adapter having a body and a plurality of electrical terminals supported by the body; and

electrical connections formed between the adapter terminals and respective interconnects on the modular package,

the adapter body being mechanically secured to the modular package;

the adapter terminals being arranged to mate with the external mounting surface.

123. The apparatus of claim 122 wherein the external mounting surface is a circuit board and the terminals comprise ends constructed and arranged to be inserted into conductive holes in the circuit board.

124. The apparatus of claim 122 wherein the external mounting surface is a circuit board and the terminals comprise ends constructed and arranged to be surface mount soldered to the circuit board.

125. The apparatus of claim 122 wherein the external mounting surface includes a connector and the terminals comprise ends constructed and arranged to mate with the connector.

126. The apparatus of claim 122 wherein the interconnects are disposed along a long edge of the modular package, the adapter is secured to the long edge of the modular package, and the first and second layers of the modular package are oriented perpendicular to the mounting surface.

127. The apparatus of claim 122 wherein the interconnects are disposed along opposite edges of the modular package, the adapter is secured to the opposite edges, and the first and second layers of the modular package are oriented essentially parallel to the mounting surface.

128. The apparatus of claim 127 wherein the adapter is constructed and arranged to maintain one of the first or second layers in contact with the mounting surface.

129. The apparatus of claim 110 wherein the interconnects further comprise a surface constructed and arranged for engagement with a connector terminal.

130. The apparatus of claim 110 wherein the interconnects further comprise a layer of metal plating.

131. The apparatus of claim 110 wherein the first layer further comprises contours formed in an interior surface of the first layer, the contours including a first feature having a shape and an elevation to accommodate a first component on the PCB, the first component having a height greater than or less than other components on the PCB.

132. The apparatus of claim 131 wherein the first component includes a magnetic core structure and the elevation is a recess in the interior surface.

133. The apparatus of claim 131 wherein the first component includes a semiconductor switch and the elevation is a protrusion from the interior surface.

134. The apparatus of claim 110 further comprising interlocking features comprising a contour formed in an interior surface of the first layer, the contour being filled with cured mold compound.

135. The apparatus of claim 110 wherein the modular package further comprises a recess formed in the first layer adjacent one or more of the interconnects providing a setback between the first layer and the one or more interconnects.

136. An apparatus comprising:

a power converter including

a printed circuit board ("PCB") comprising a plurality of conductive layers and having a top surface and a bottom surface;

a magnetic core structure magnetically coupled to a winding formed by traces in one or more of the conductive layers in the PCB; and

a plurality of power semiconductor devices, a first set of the power semiconductor devices being mounted on the top surface and electrically connected to dissipate power at a level, Pt, during operation of the converter, a second set of the power semiconductor devices being mounted on the bottom surface and electrically connected to dissipate power at a level, Pb, during operation of the converter;

wherein the power semiconductor devices are distributed between the first and second sets to distribute heat generation during operation of the converter such that each level Pt, Pb is less than 150% of the other level Pb, Pt.

137. The apparatus of claim 136 wherein a plurality of the power semiconductor devices in the first set are each positioned in a location on the top surface substantially overlapping a location on the bottom surface occupied by a power semiconductor device in the second set.

138. The apparatus of claim 136 wherein the power semiconductor devices are electrically connected using a respective set of conductive vias in the PCB, and a plurality of the power semiconductor devices in the first set share their respective sets of conductive vias with corresponding power semiconductor devices in the second set.

139. The apparatus of claim 137 wherein the power converter further comprises circuitry including a pair of cells having a common circuit topology and each including power semiconductor switches from each of the first and second sets; each cell having its respective components arranged in a pattern, wherein the pattern of components of one cell is substantially a mirror image of the pattern of components in the other cell.

140. The apparatus of claim 139 wherein a component from one of the cells is located on an opposite surface of a respective component from the other one of the cells.

141. The apparatus of claim 140 wherein the cells comprise input cells.

142. The apparatus of claim 138 wherein the power semiconductor devices comprise output switches.

143. A method of manufacturing a plurality of products comprising:

inserting a plurality of components into a cavity formed by one or more molds;

closing the one or more molds to form a seal around the cavity;

filling the cavity with mold compound;

curing the mold compound in the cavity to secure the components, cured mold compound, and molds together into an assembly; and

cutting the assembly to separate the plurality of products from the assembly, the products each including a respective section of the one or more molds which remains as an integral part of each respective product.

144. The method of claim 143 further comprising maintaining a predetermined alignment between the plurality of components and the one or more molds.

145. The method of claim 143 wherein the plurality of components include a substrate having conductive features; and the cutting comprises exposing portions of the conductive features in each respective product.

ABSTRACT

A method of encapsulating a panel of electronic components such as power converters reduces wasted printed circuit board area. The panel, which may include a plurality of components, may be cut into one or more individual pieces after encapsulation with the mold forming part of the finished product, e.g. providing heat sink fins or a surface mount solderable surface. Interconnection features provided along boundaries of individual circuits are exposed during the singulation process providing electrical connections to the components without wasting valuable PCB surface area. The molds may include various internal features such as registration features accurately locating the circuit board within the mold cavity, interlocking contours for structural integrity of the singulated module, contours to match component shapes and sizes enhancing heat removal from internal components and reducing the required volume of encapsulant, clearance channels providing safety agency spacing and setbacks for the interconnects. Wide cuts may be made in the molds after encapsulation reducing thermal stresses and reducing the thickness of material to be cut during subsequent singulation. External mold features can include various fin configurations for heat sinks, flat surfaces for surface mounting or soldering, etc. Blank mold panels may be machined to provide some or all of the above features in an on-demand manufacturing system. Connection adapters may be provided to use the modules in vertical or horizontal mounting positions in connector, through-hole, surface-mount solder variations. The interconnects may be plated to provide a connectorized module that may be inserted into a mating connector.

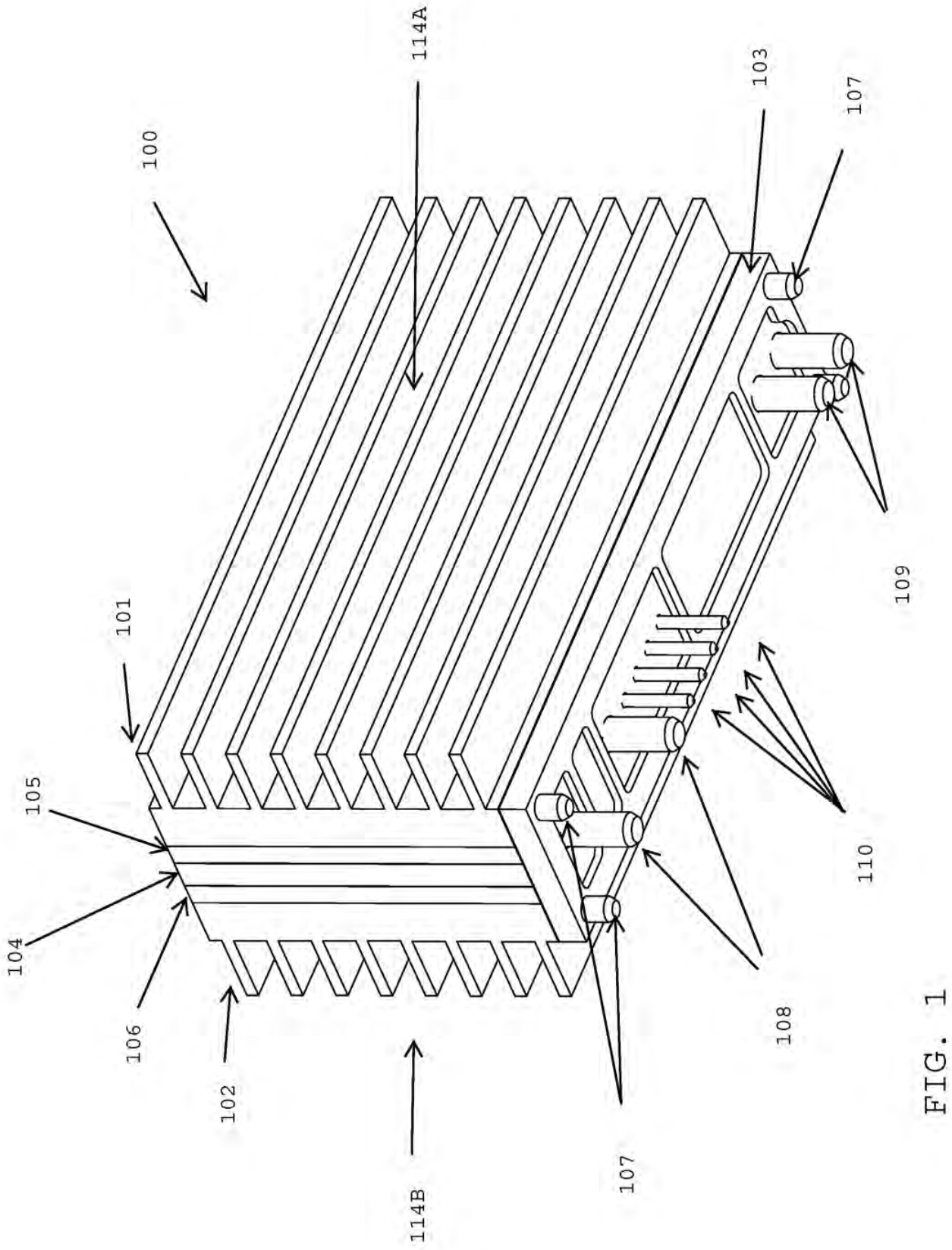


FIG. 1

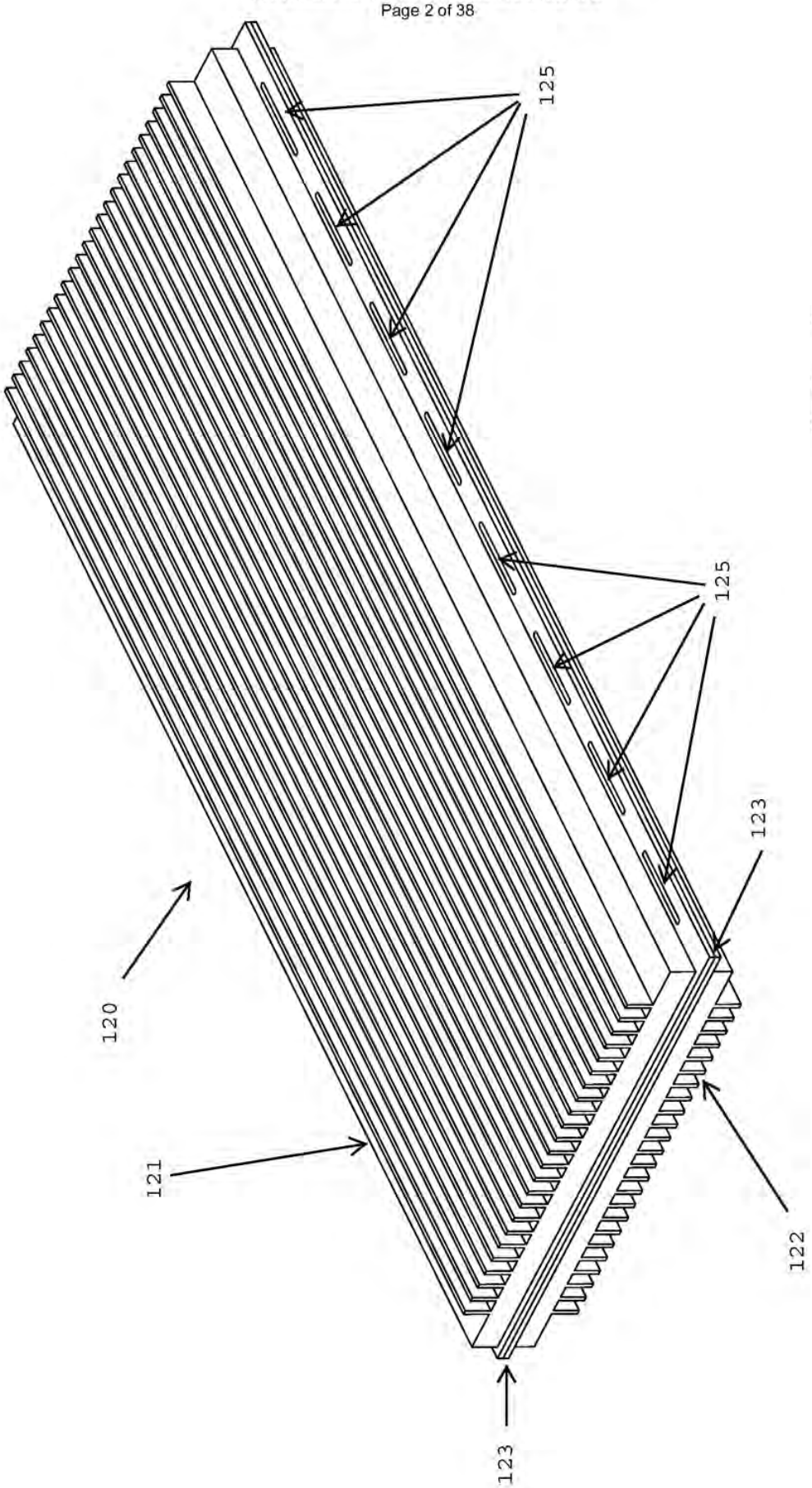


FIG. 2

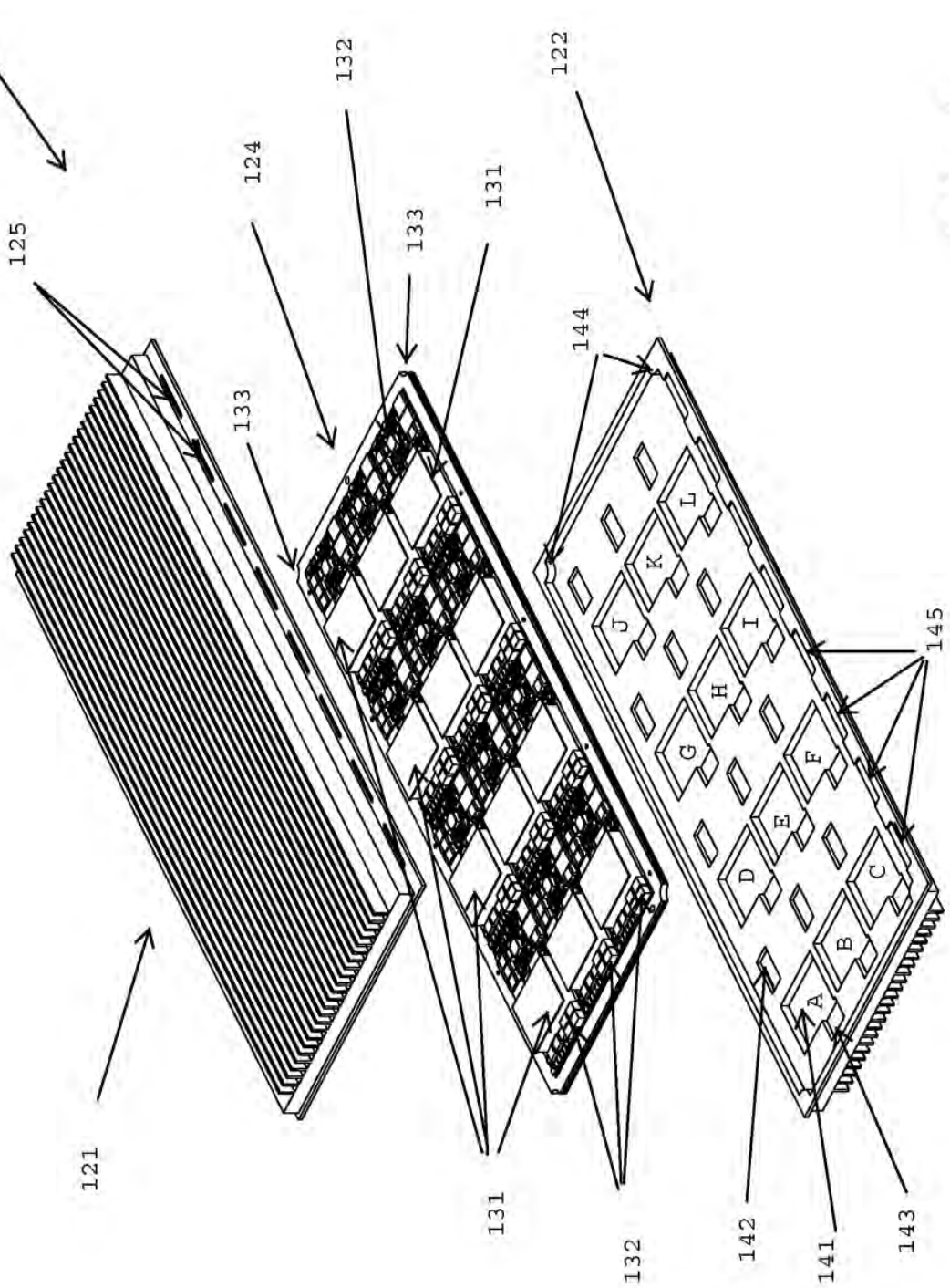

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FIG. 3

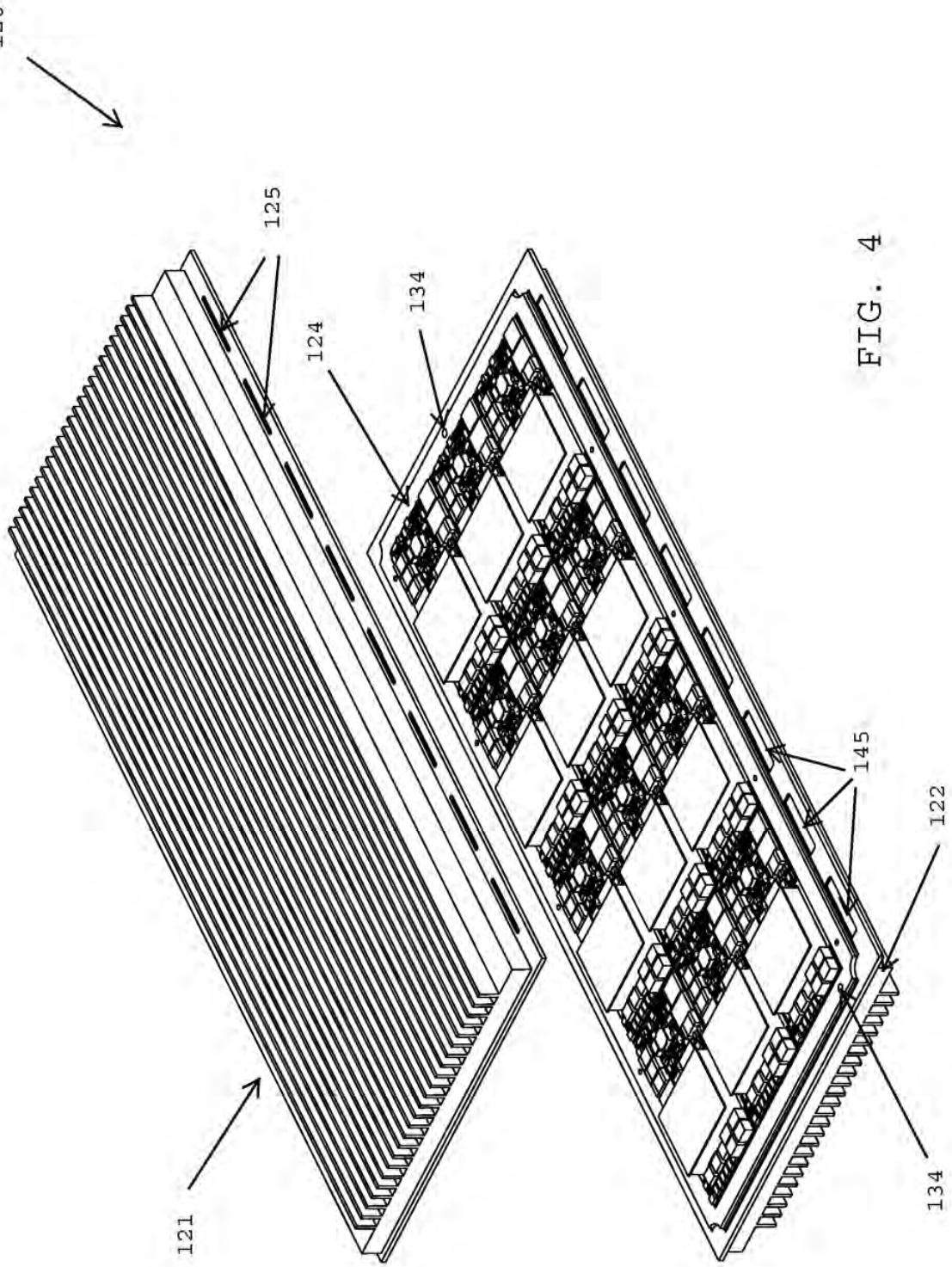


FIG. 4

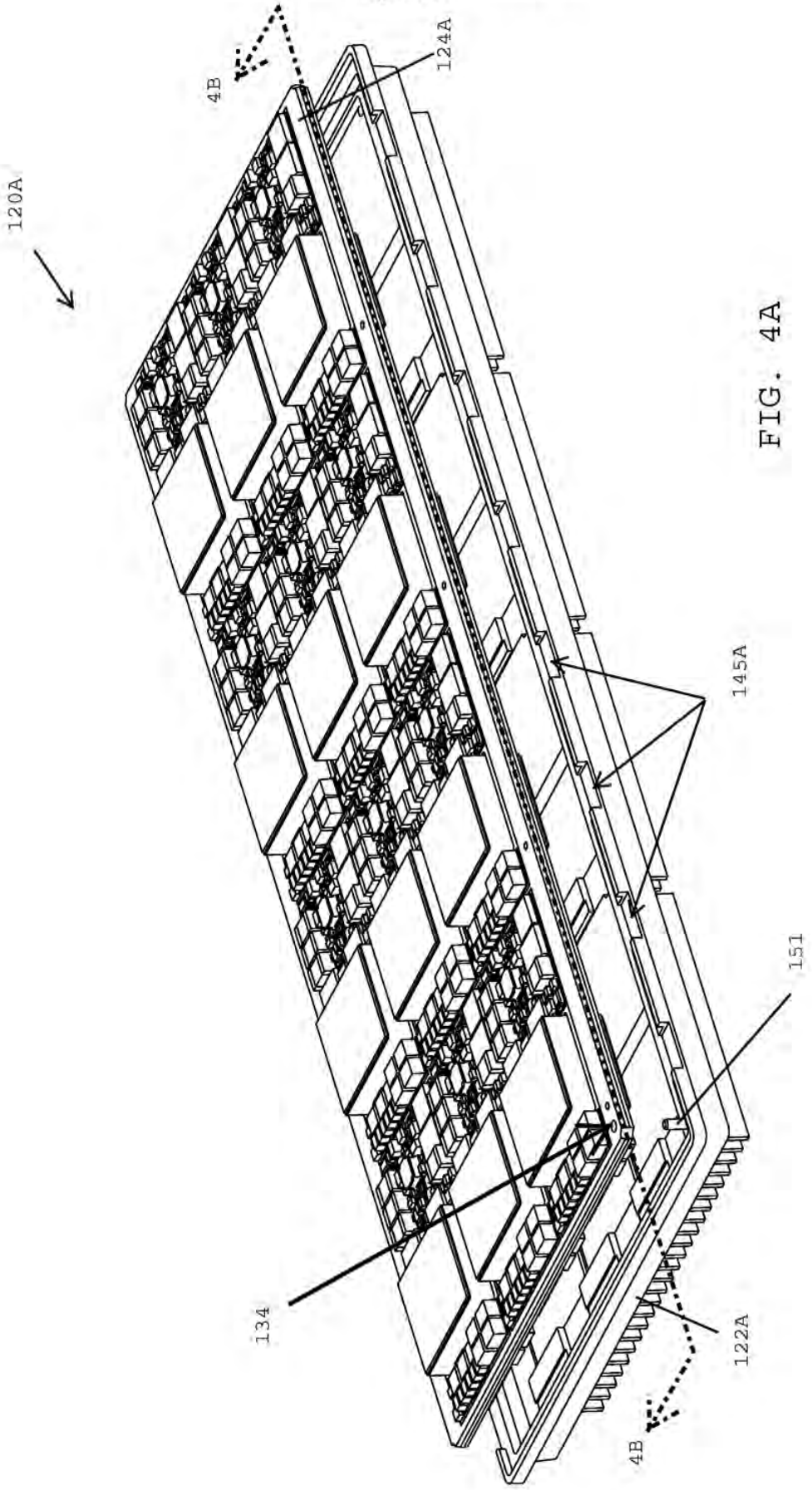


FIG. 4A

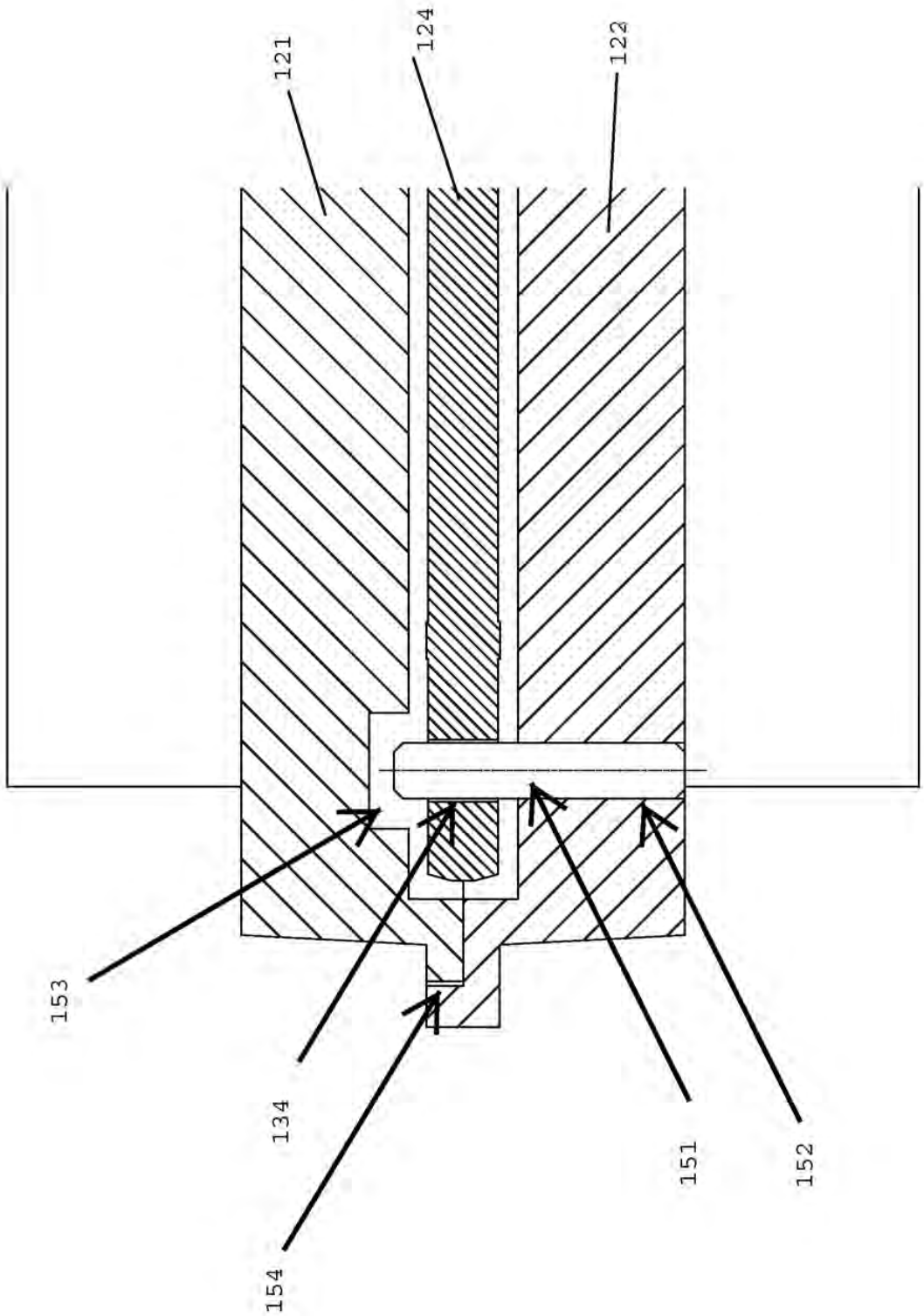


FIG. 4B

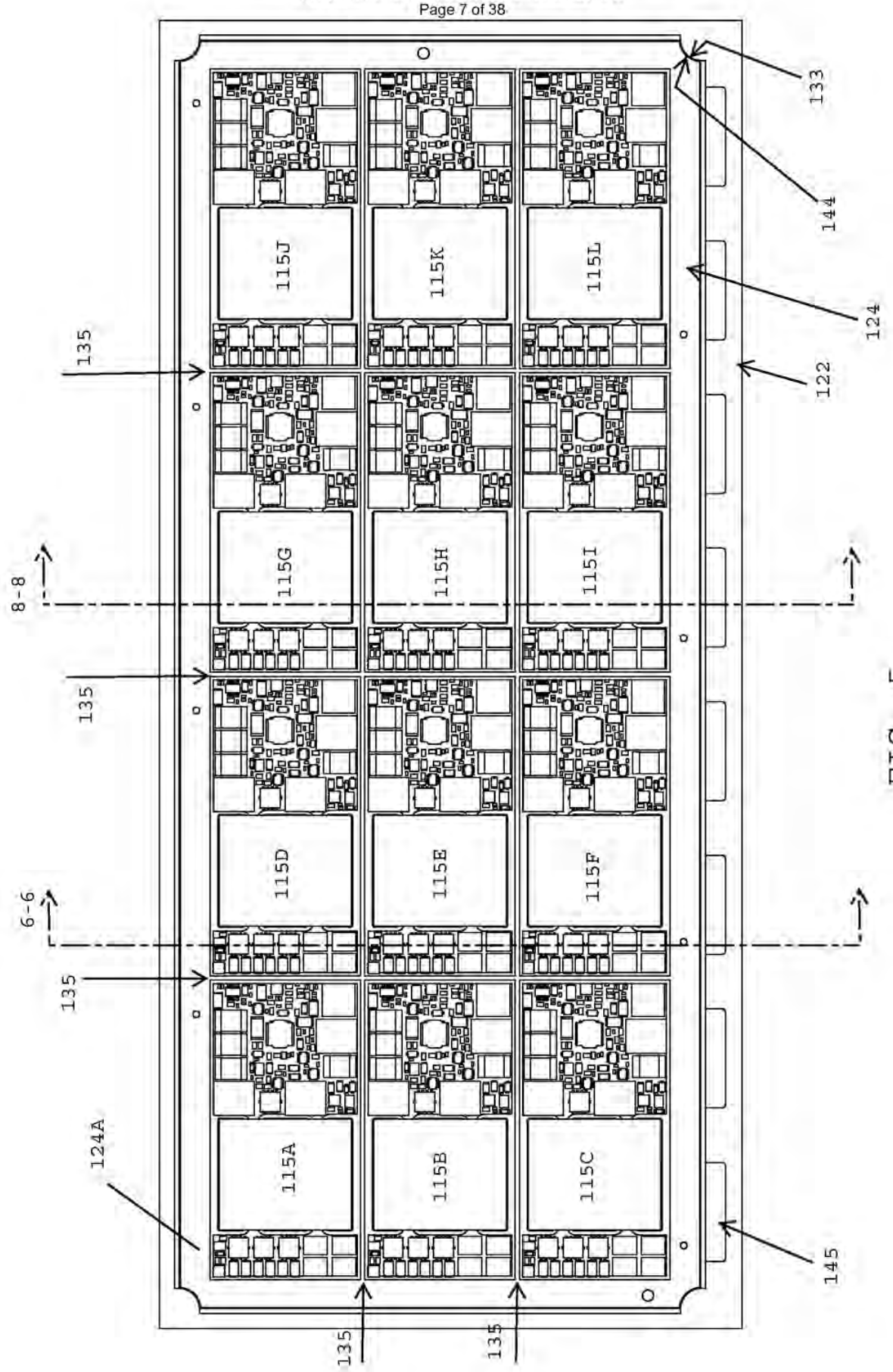

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FIG. 5

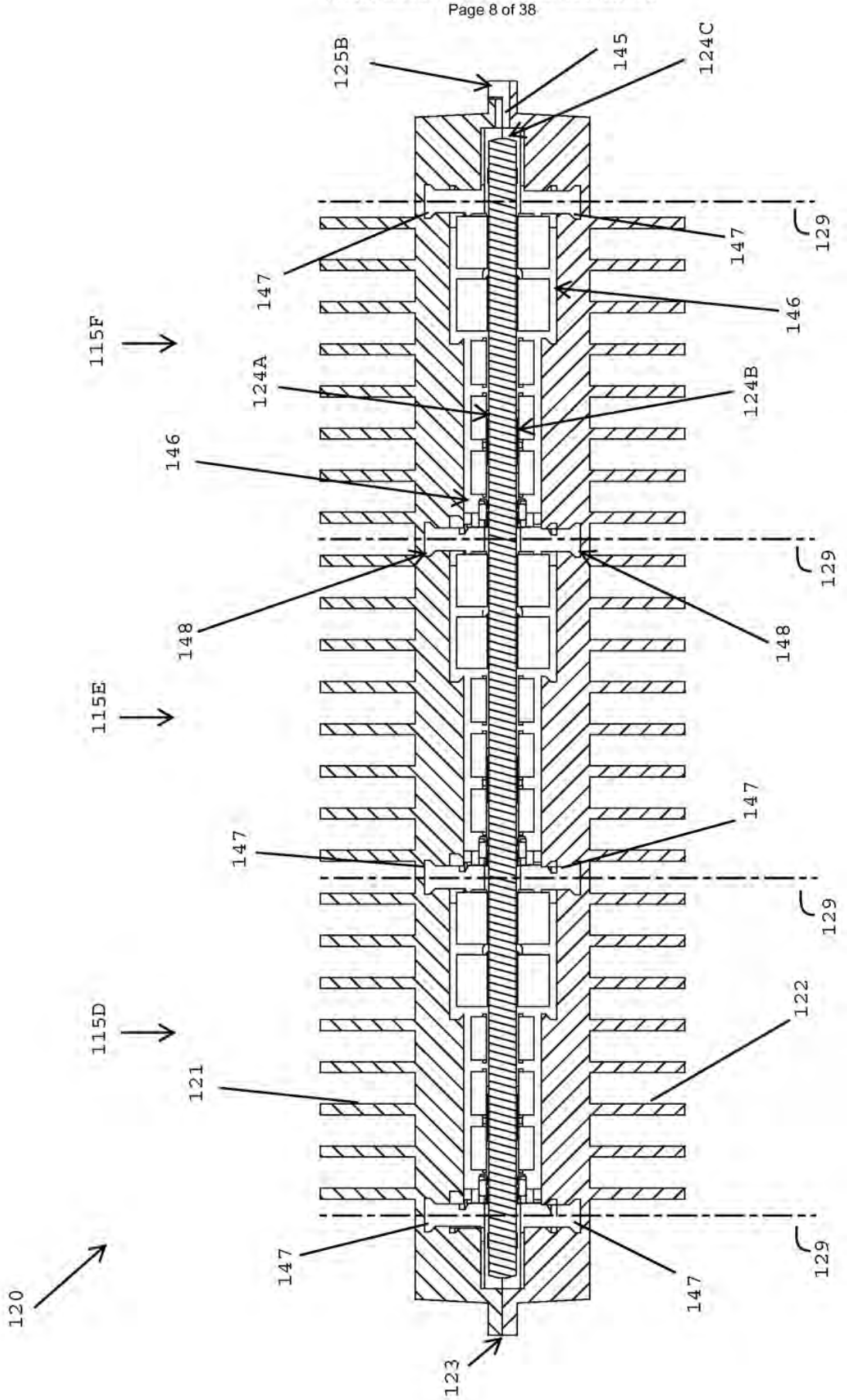

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FIG. 6

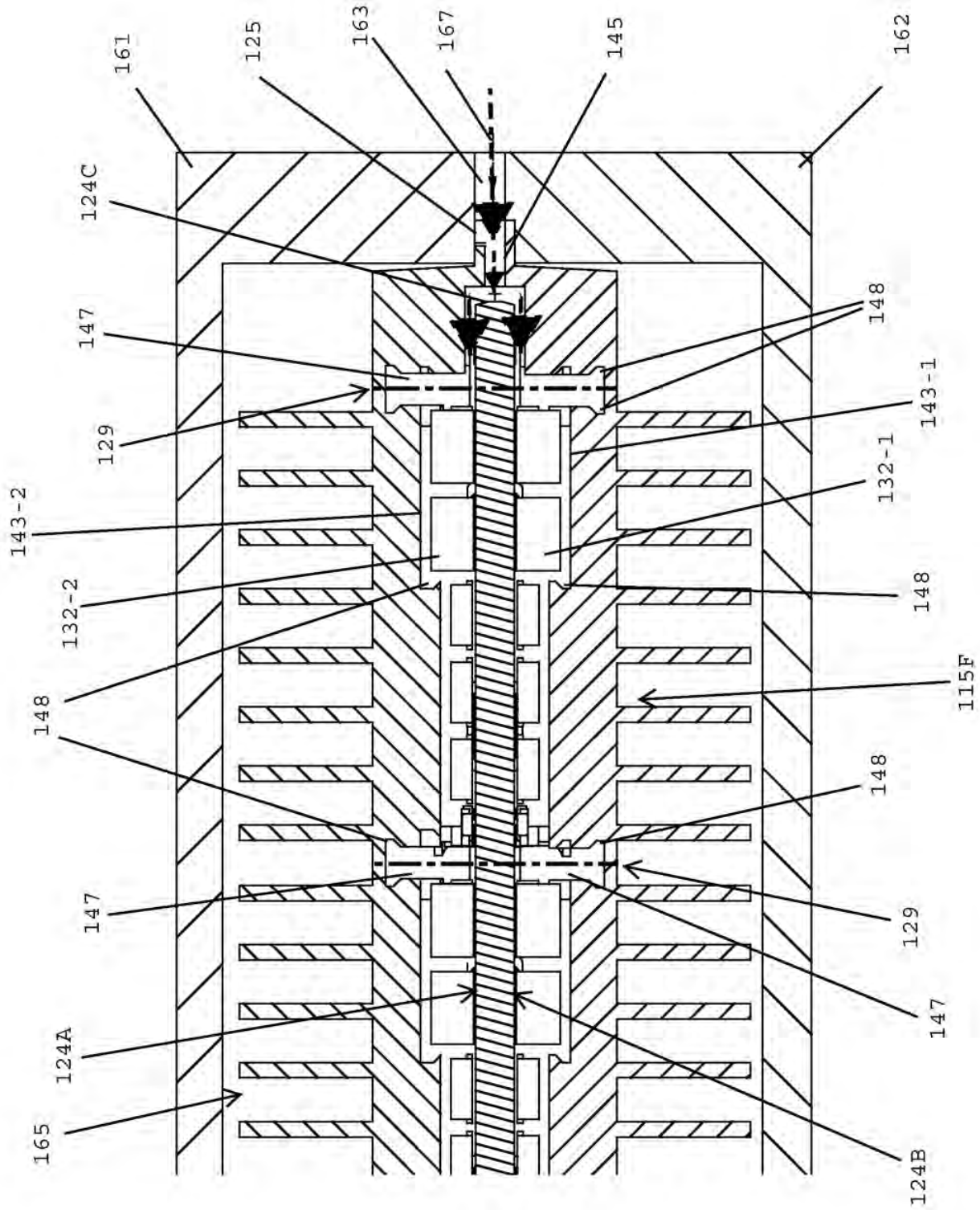

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FIG. 7

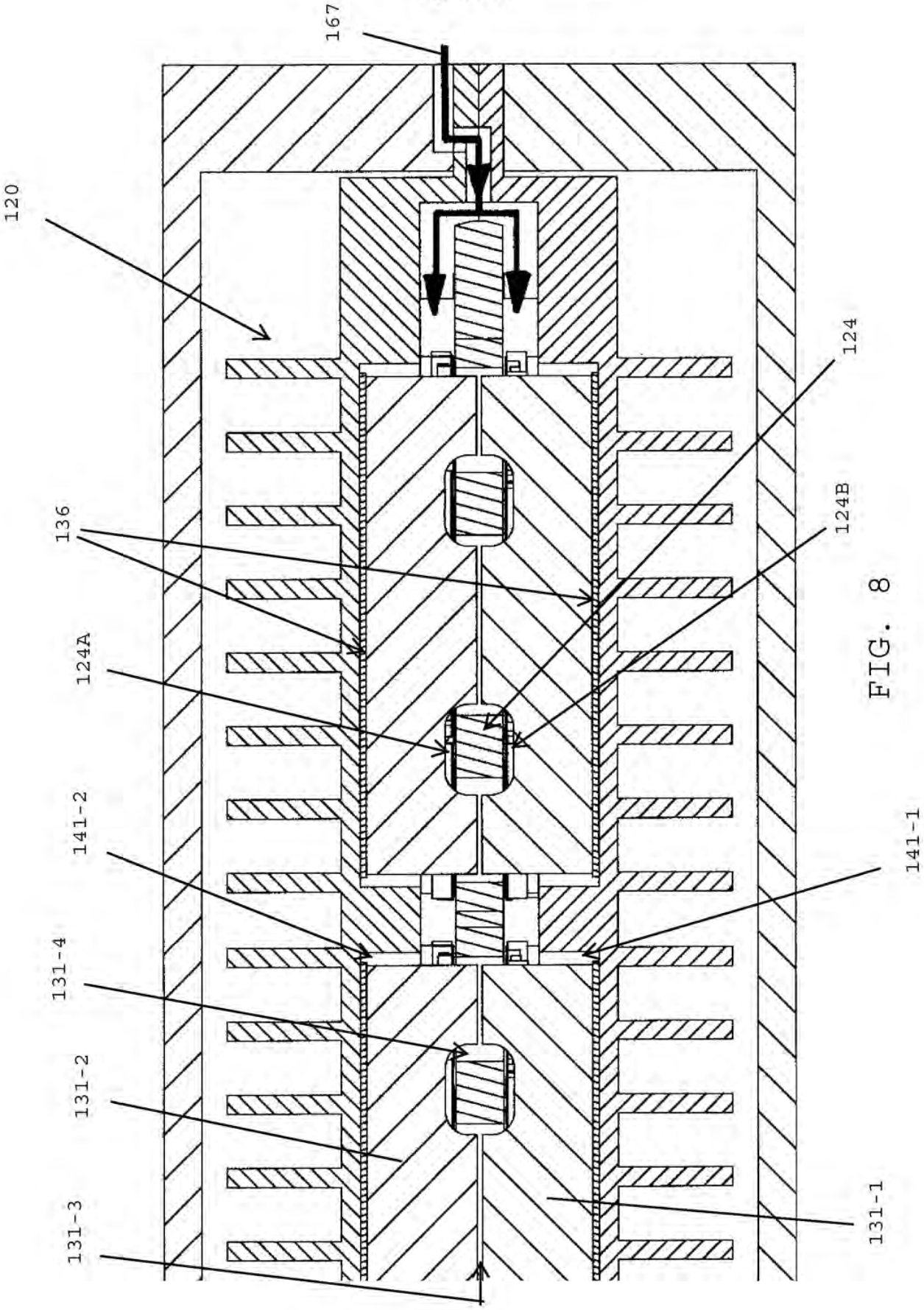


FIG. 8

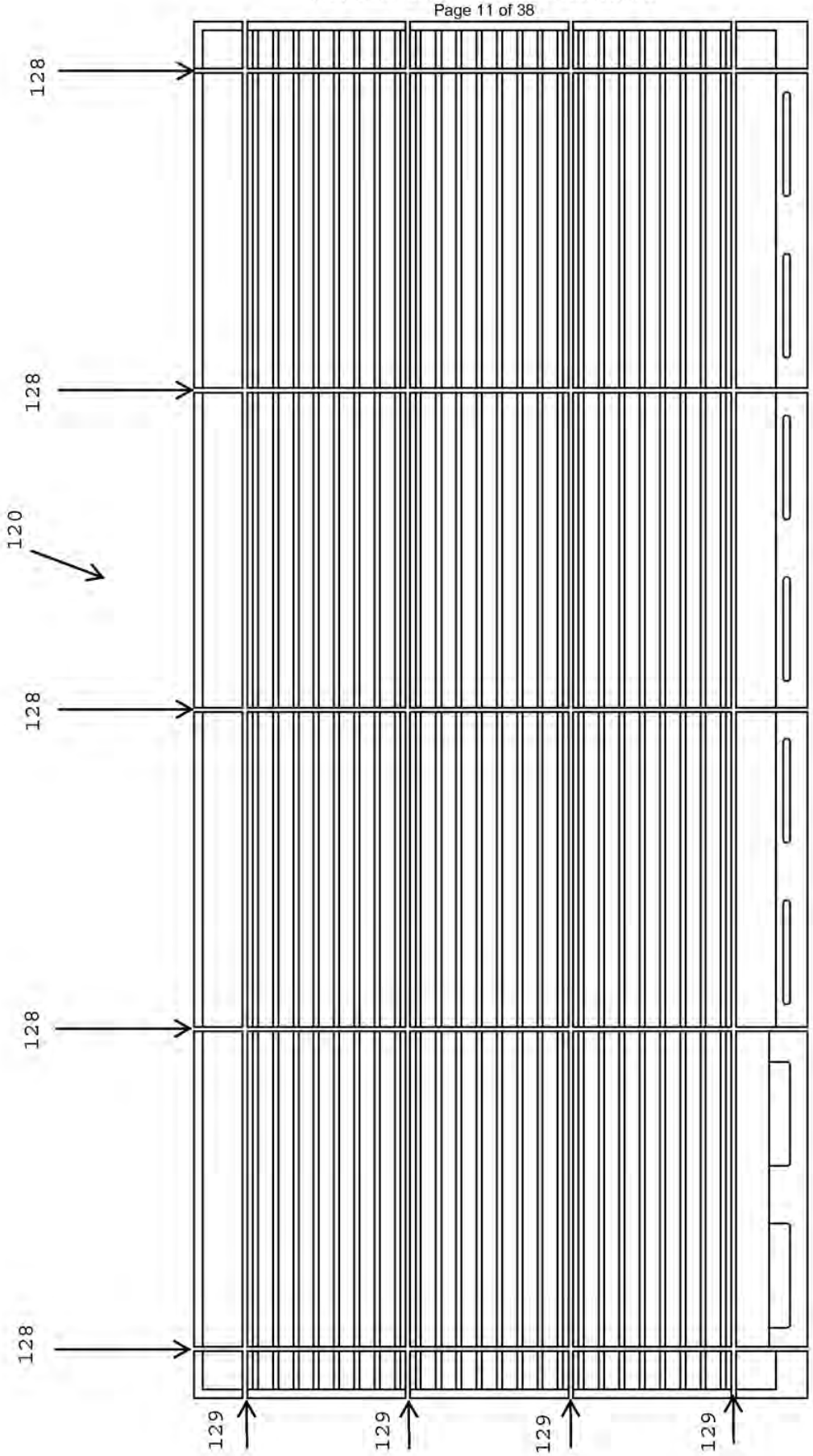


FIG. 9A

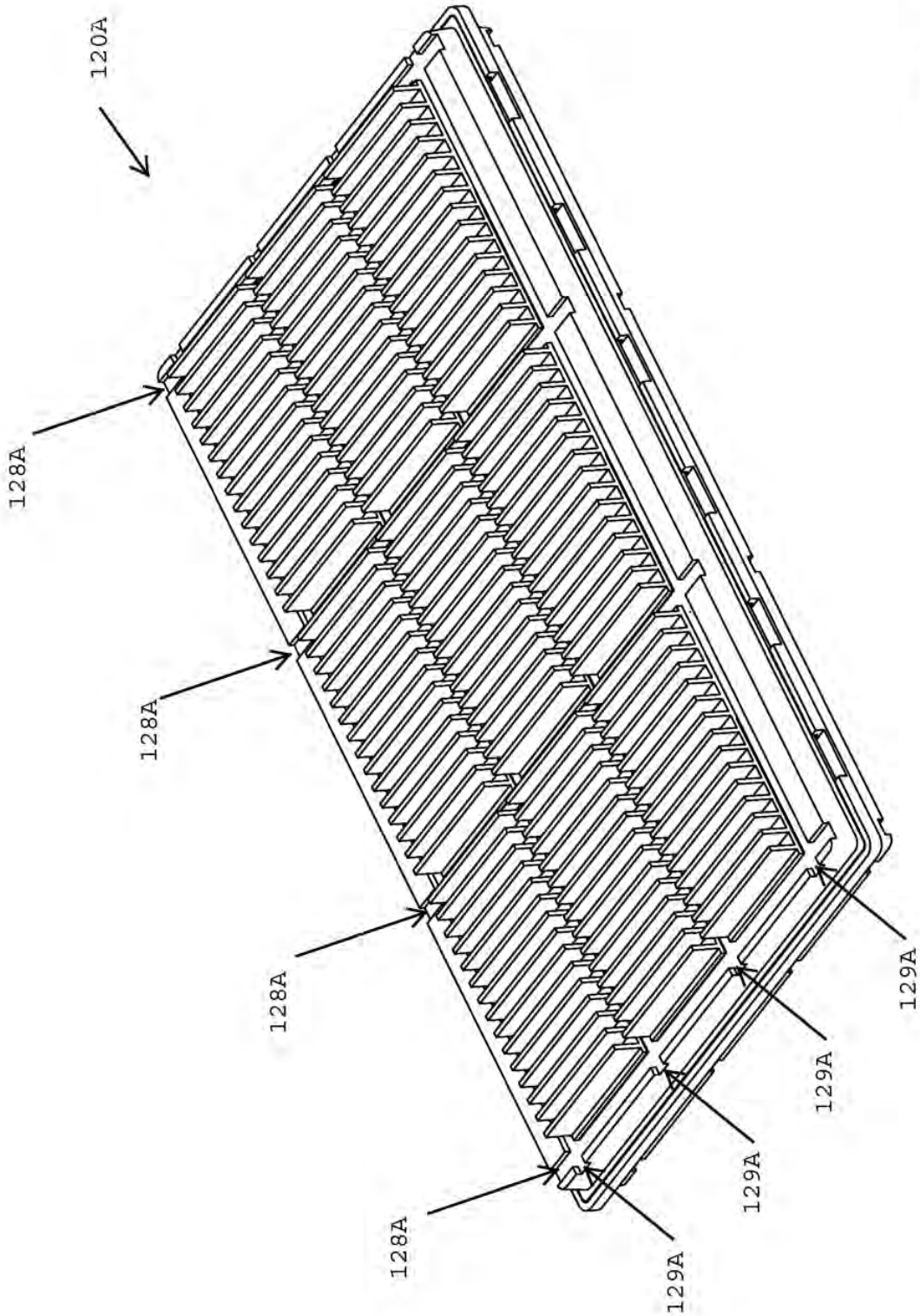


FIG. 9B

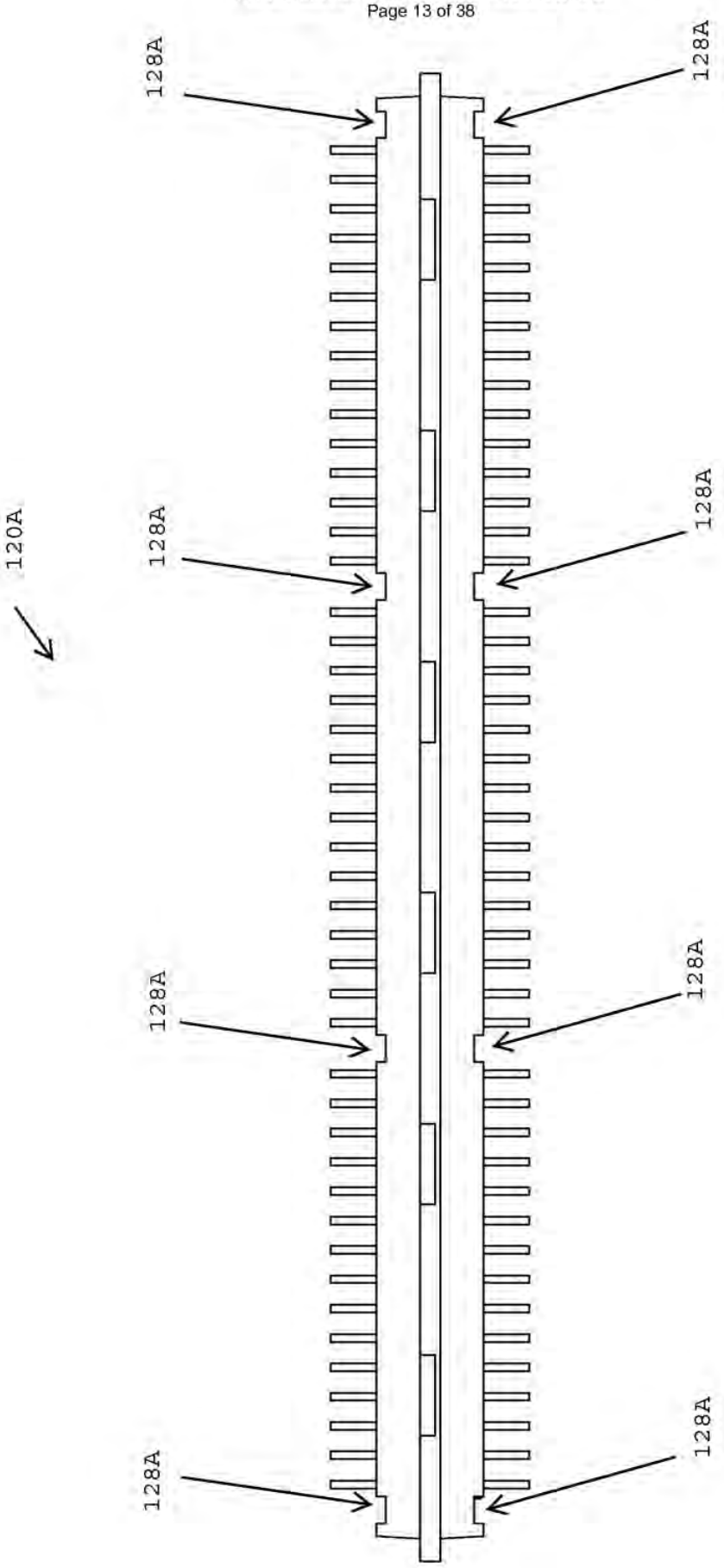


FIG. 9C

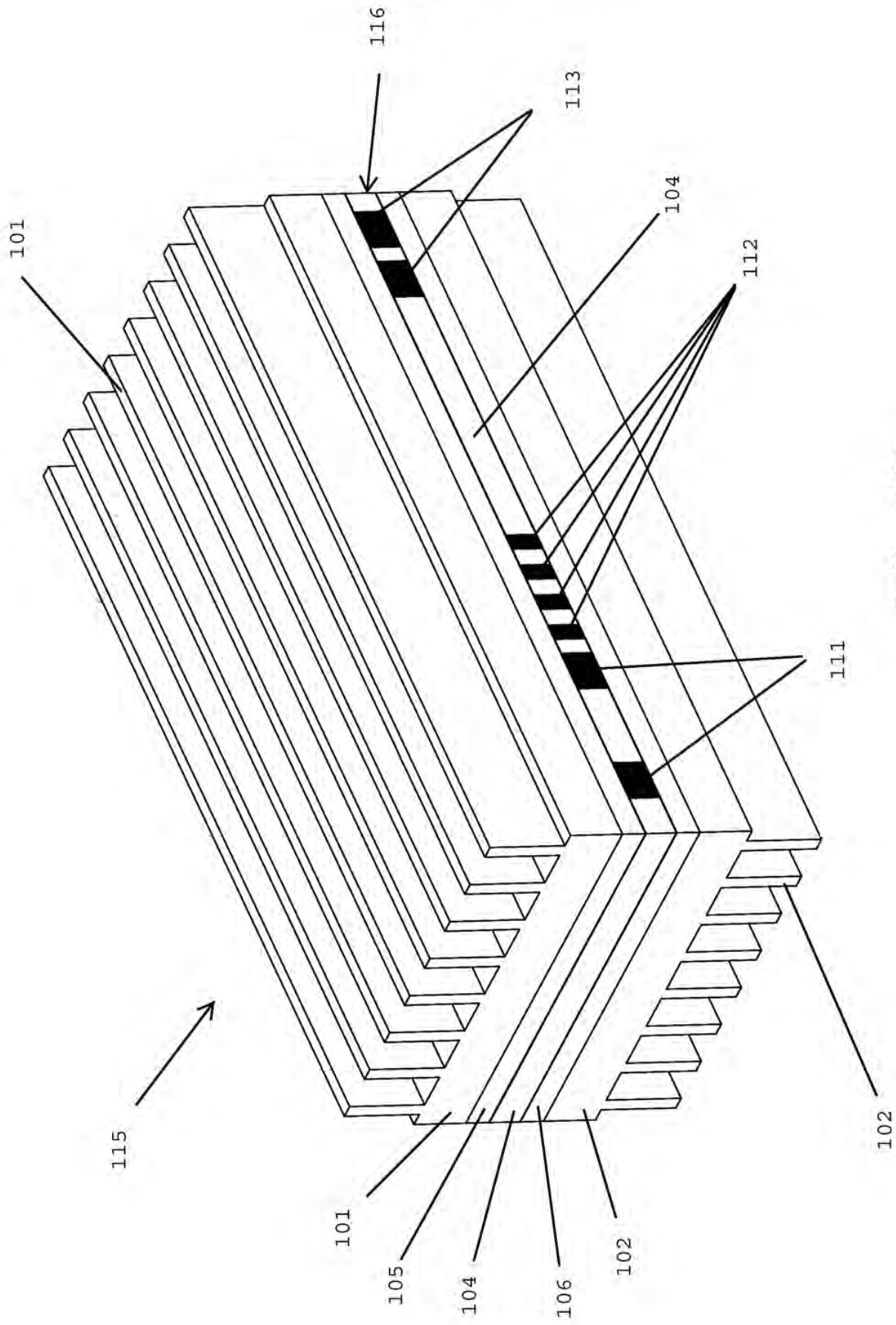


FIG. 10A

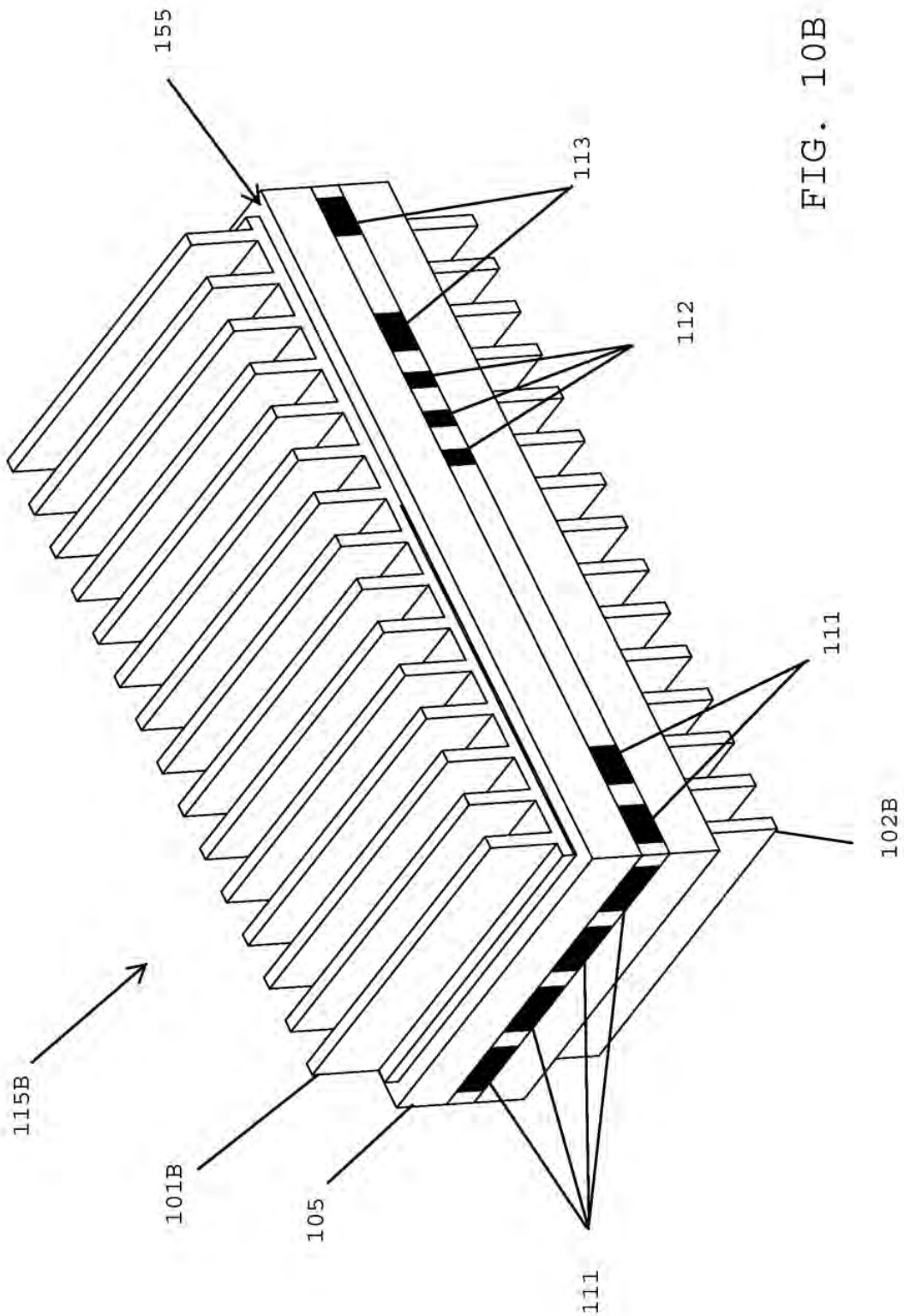


FIG. 10B

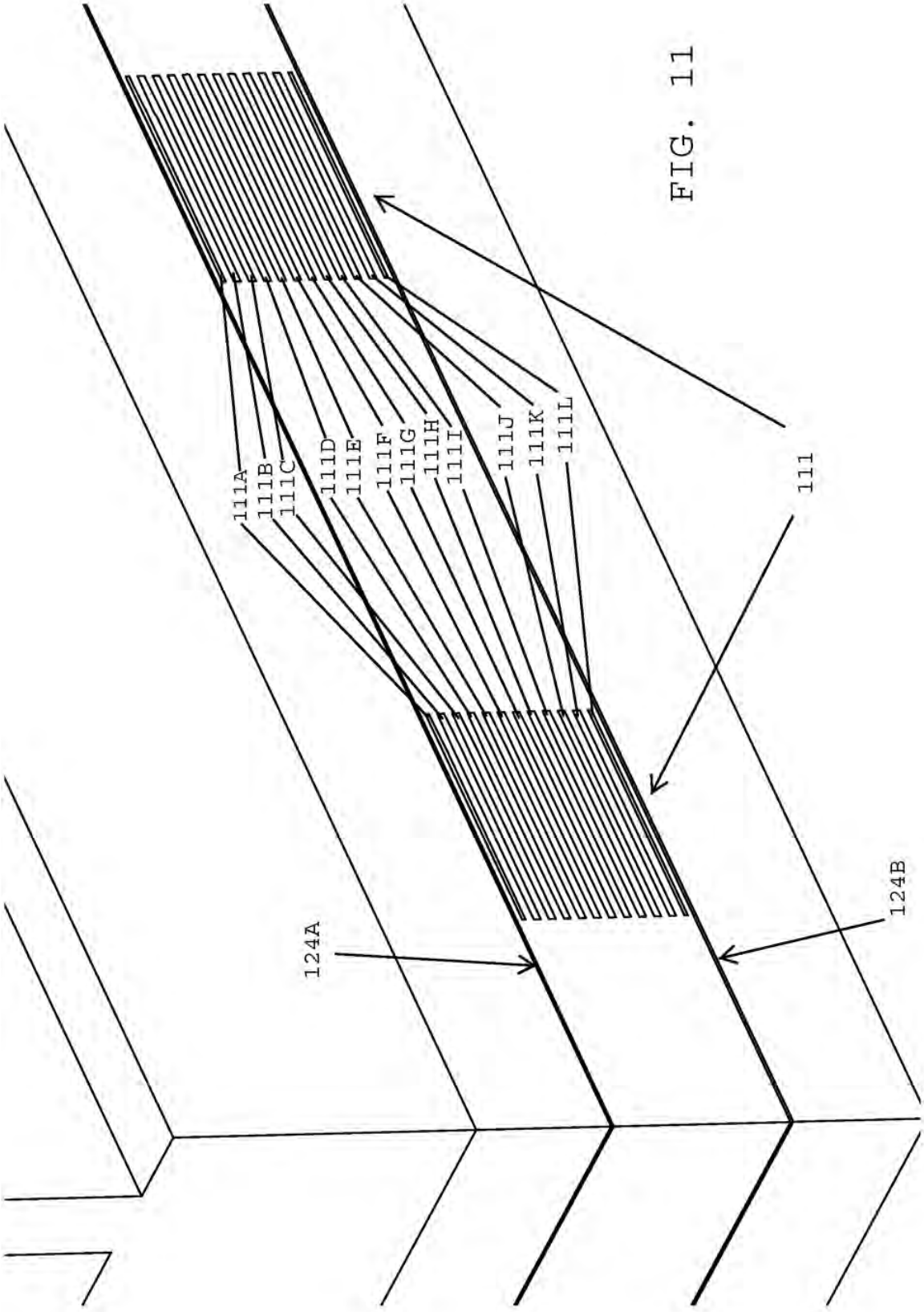

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FIG. 11

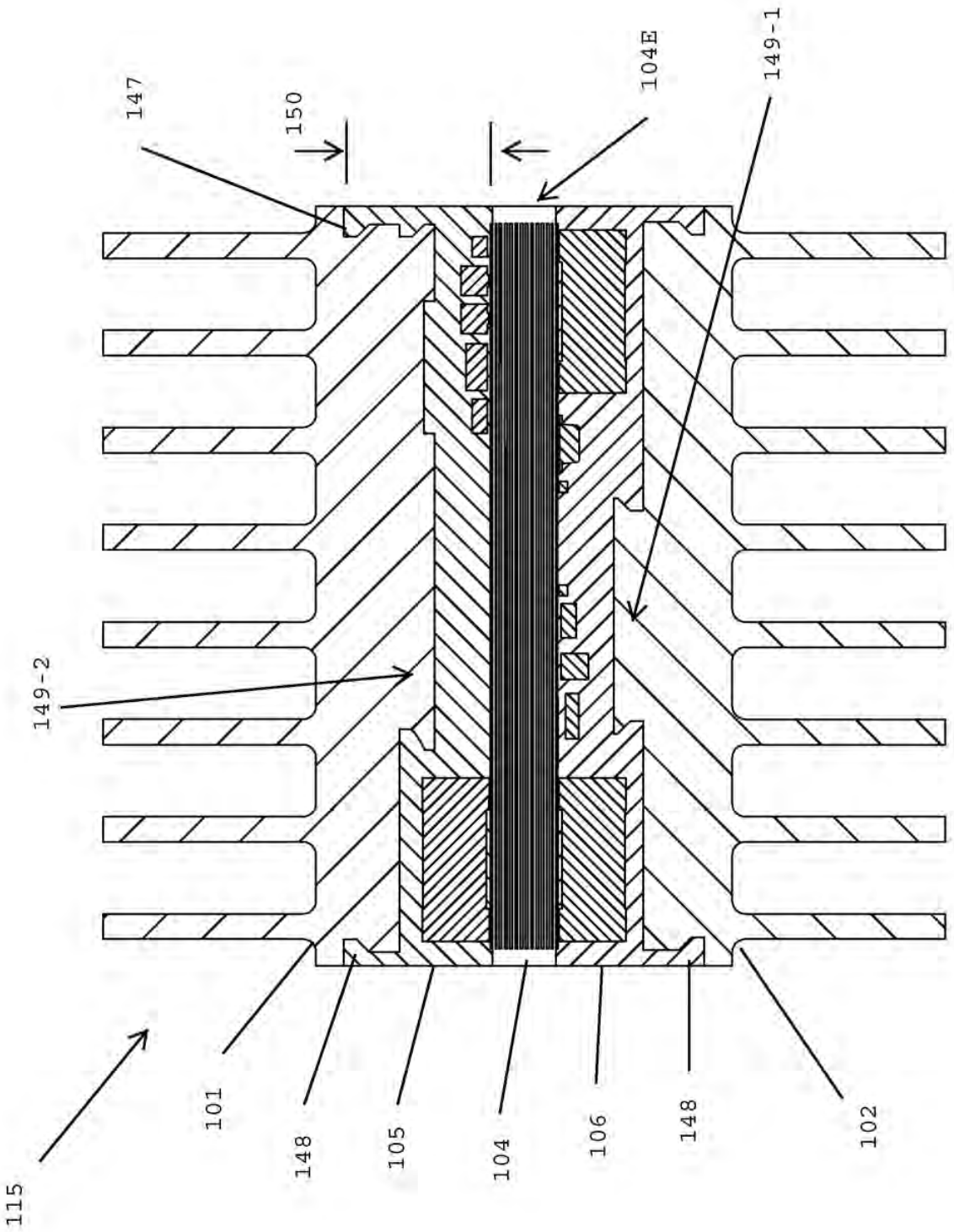


FIG. 12

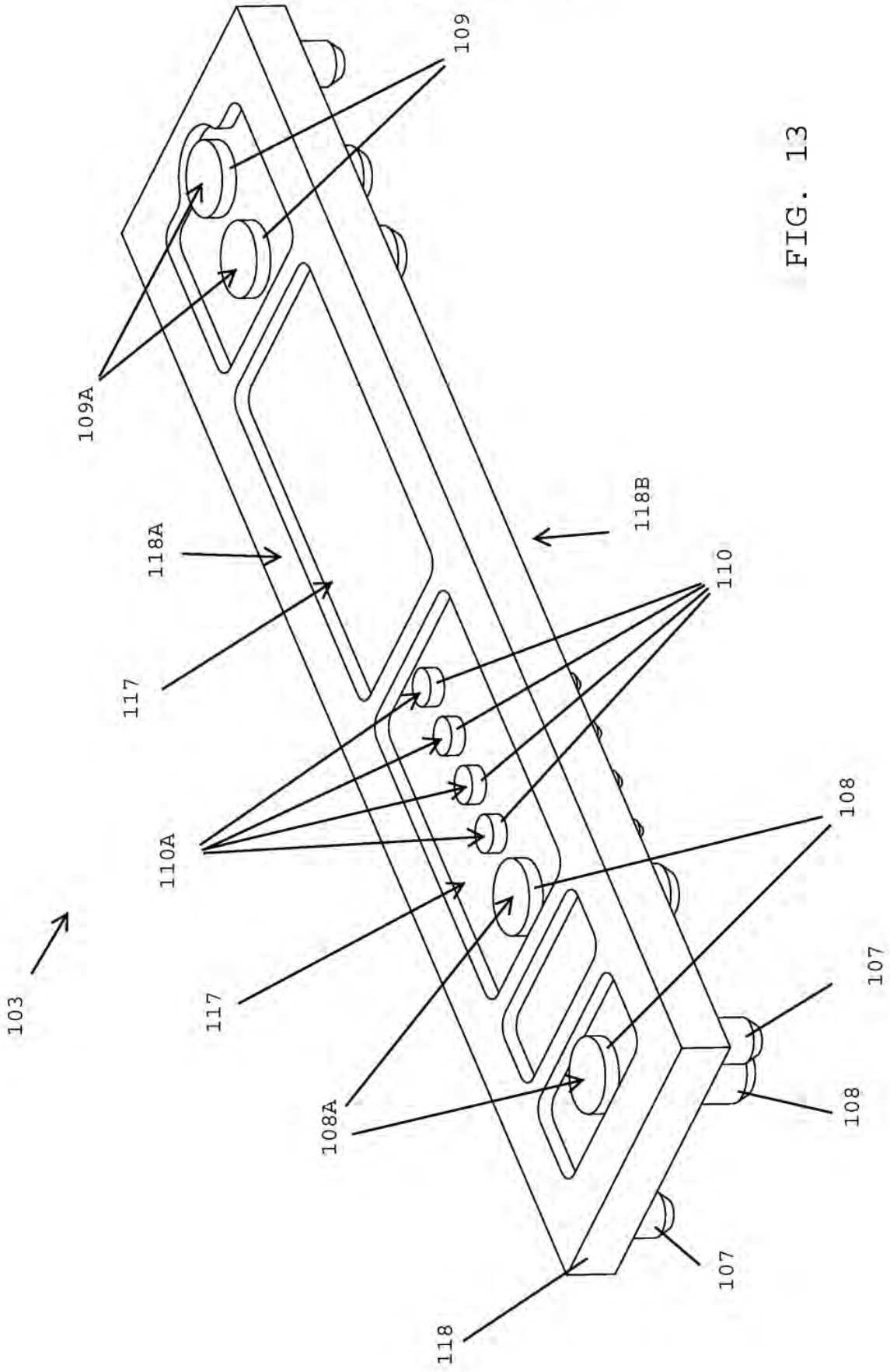

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FIG. 13

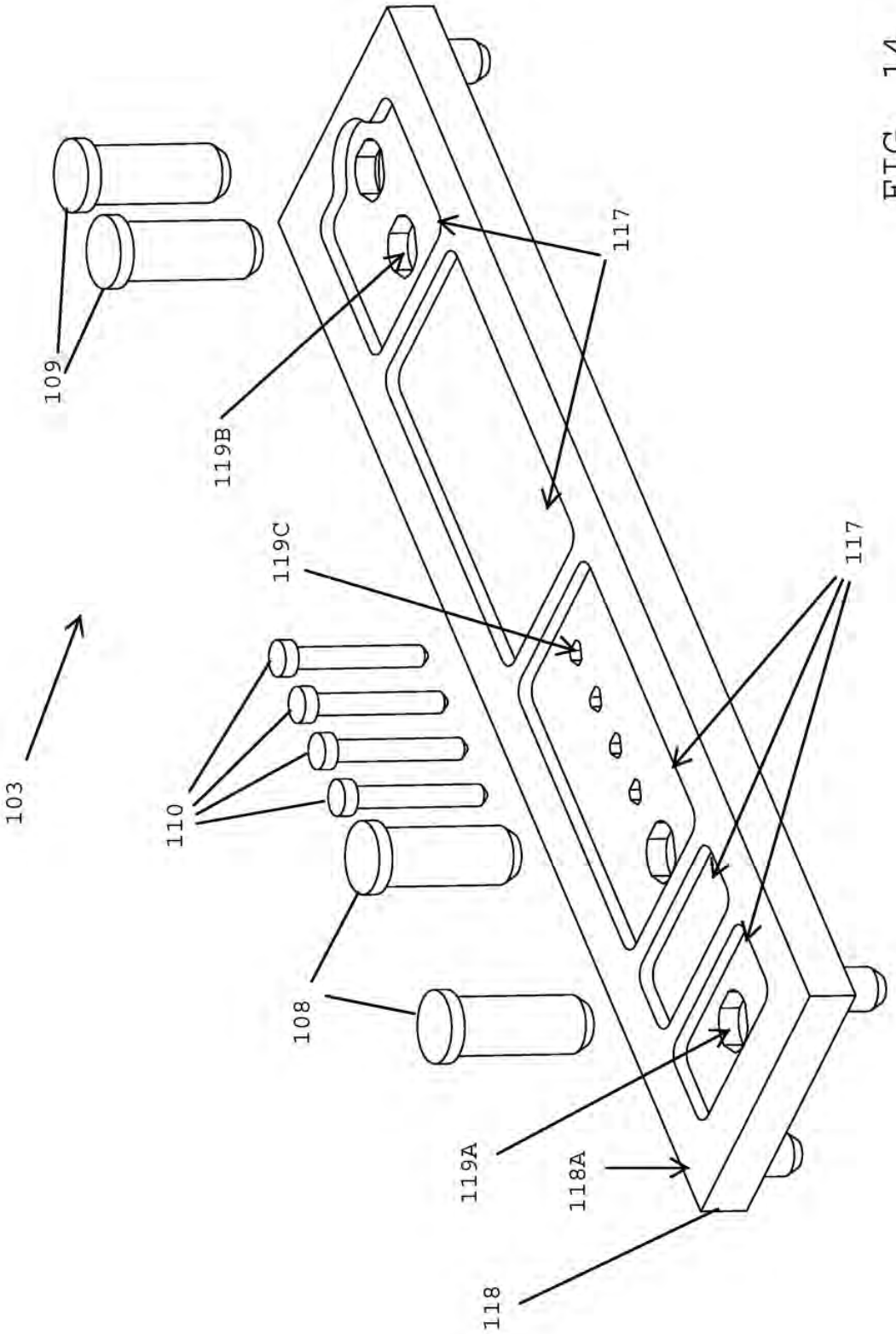


FIG. 14

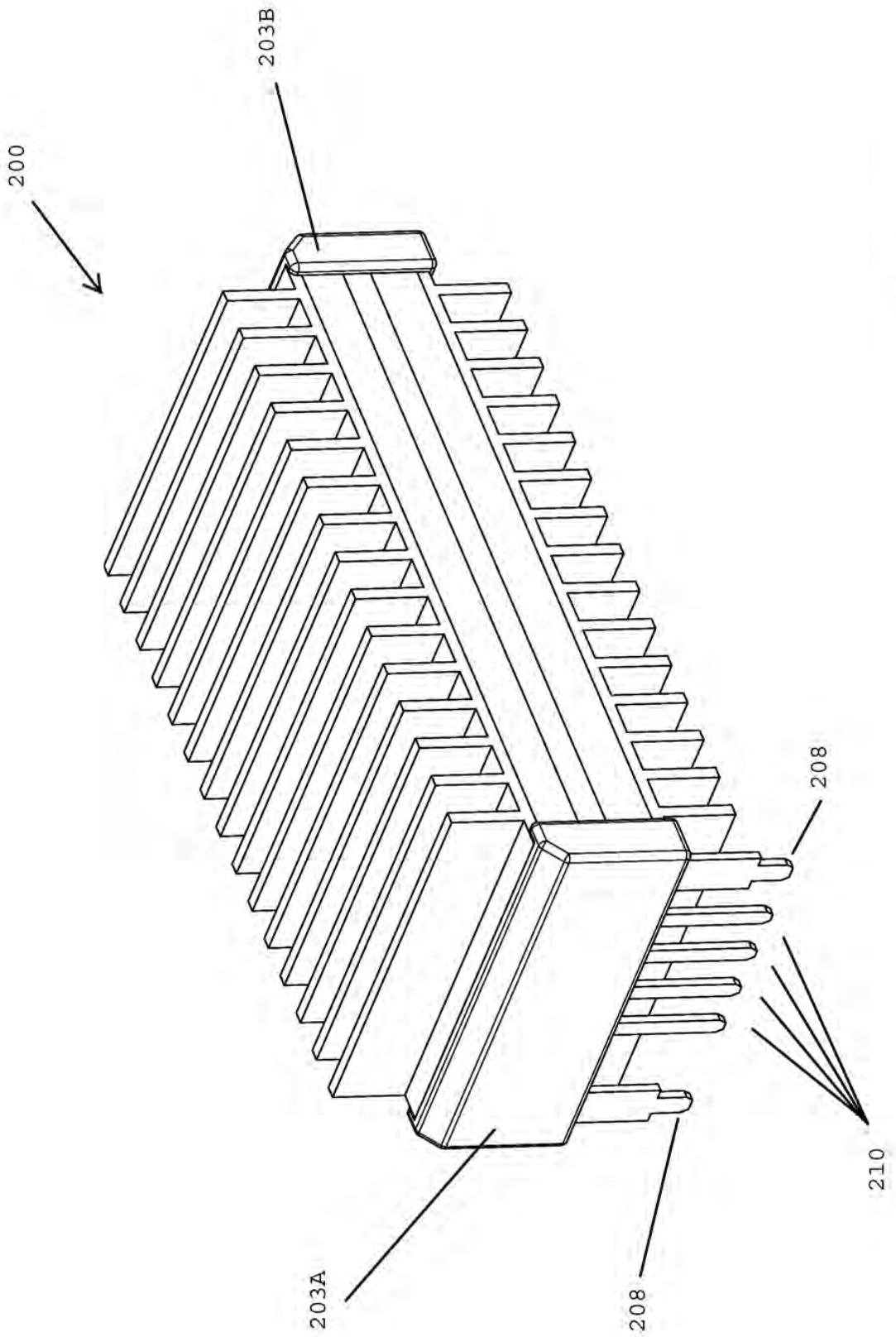


FIG. 15

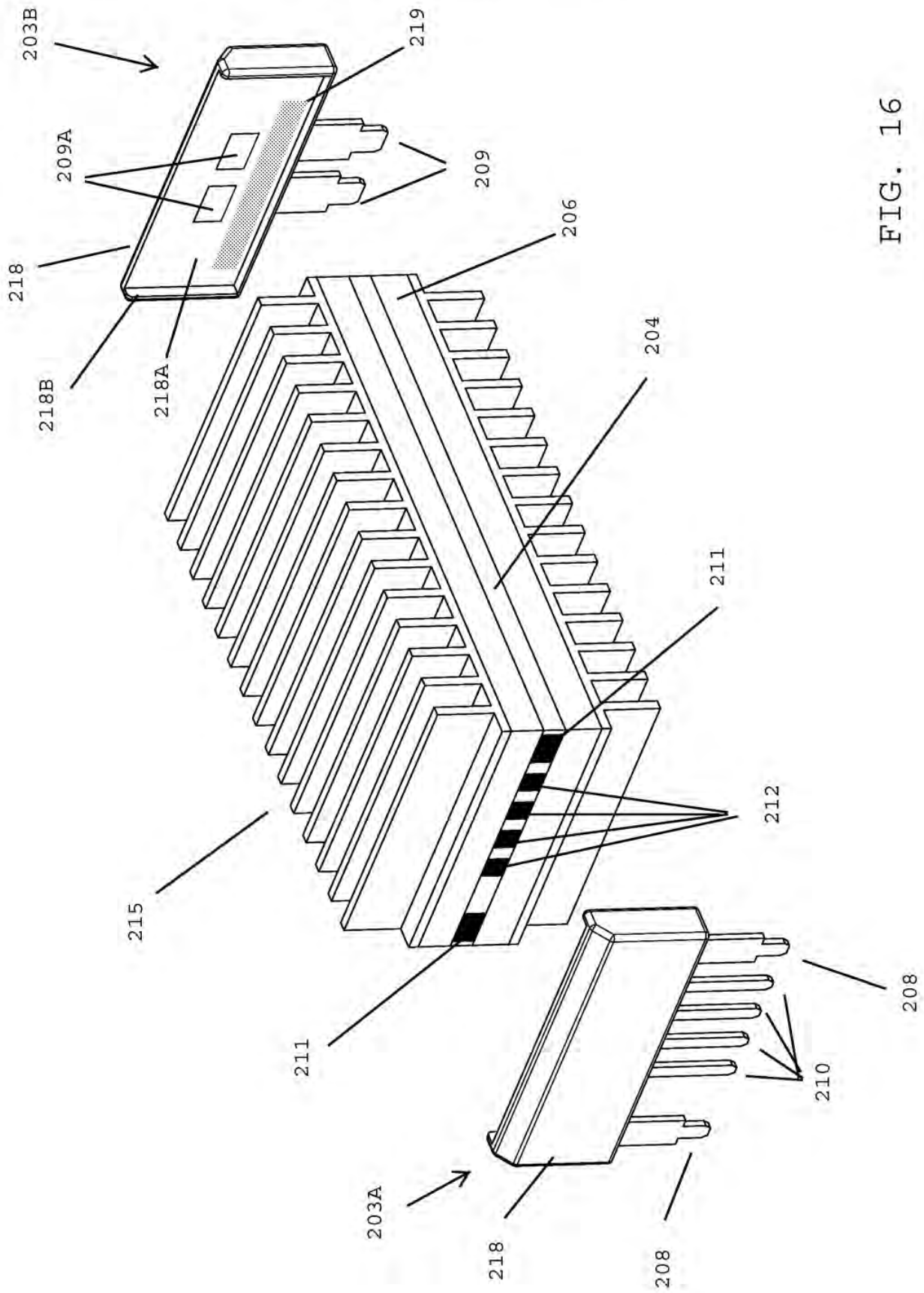

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FIG. 16

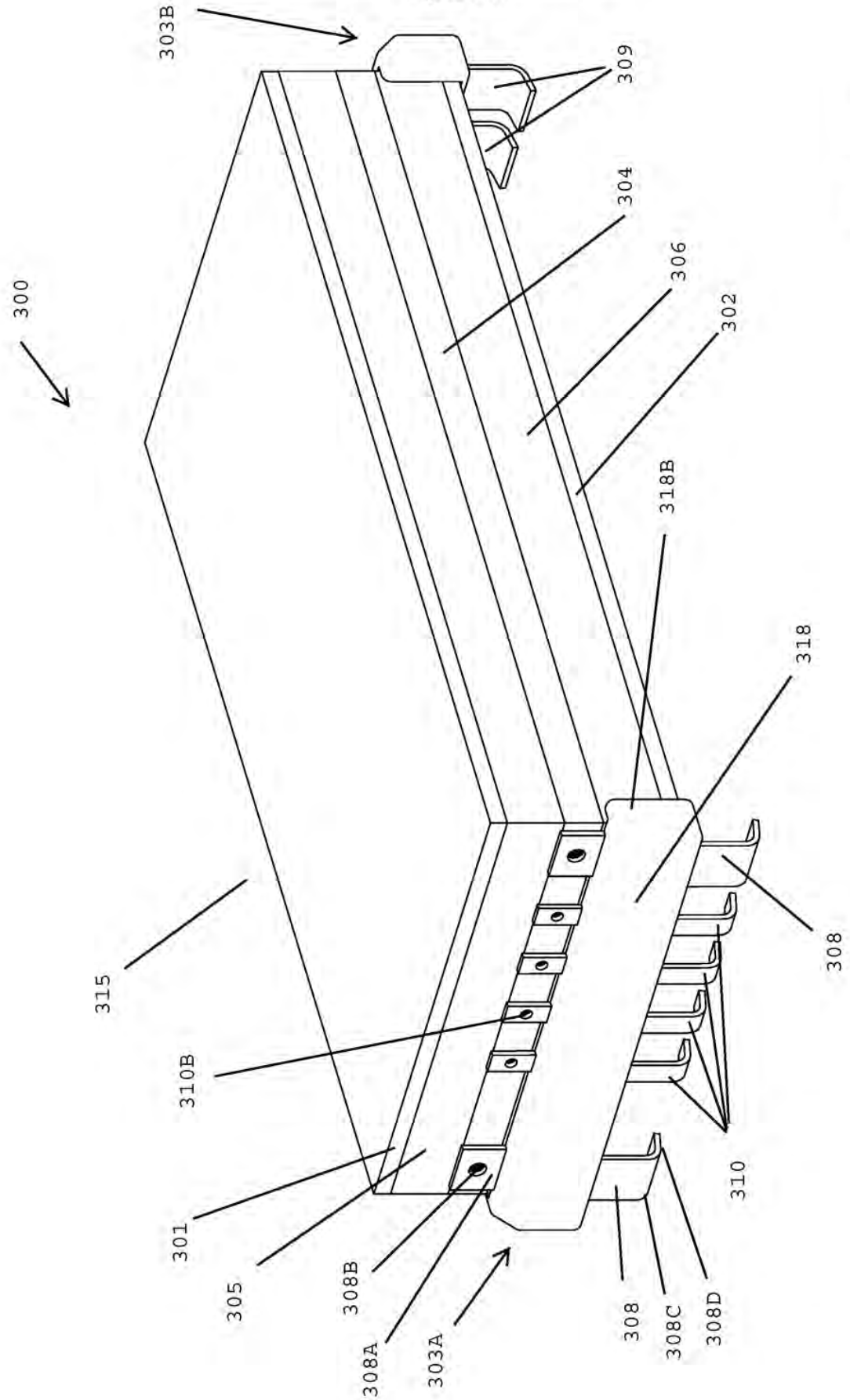

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FIG. 17

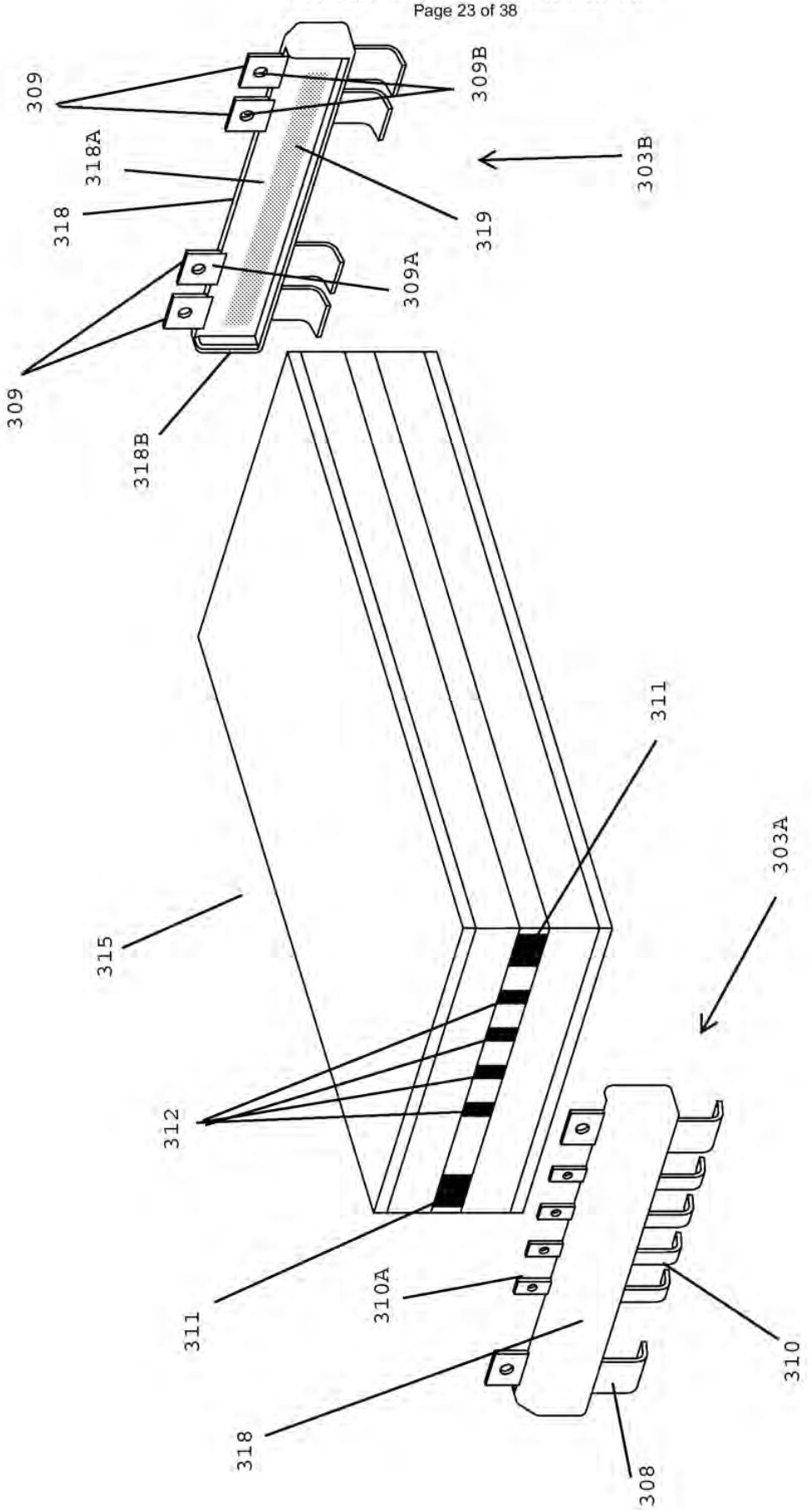

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FIG. 18

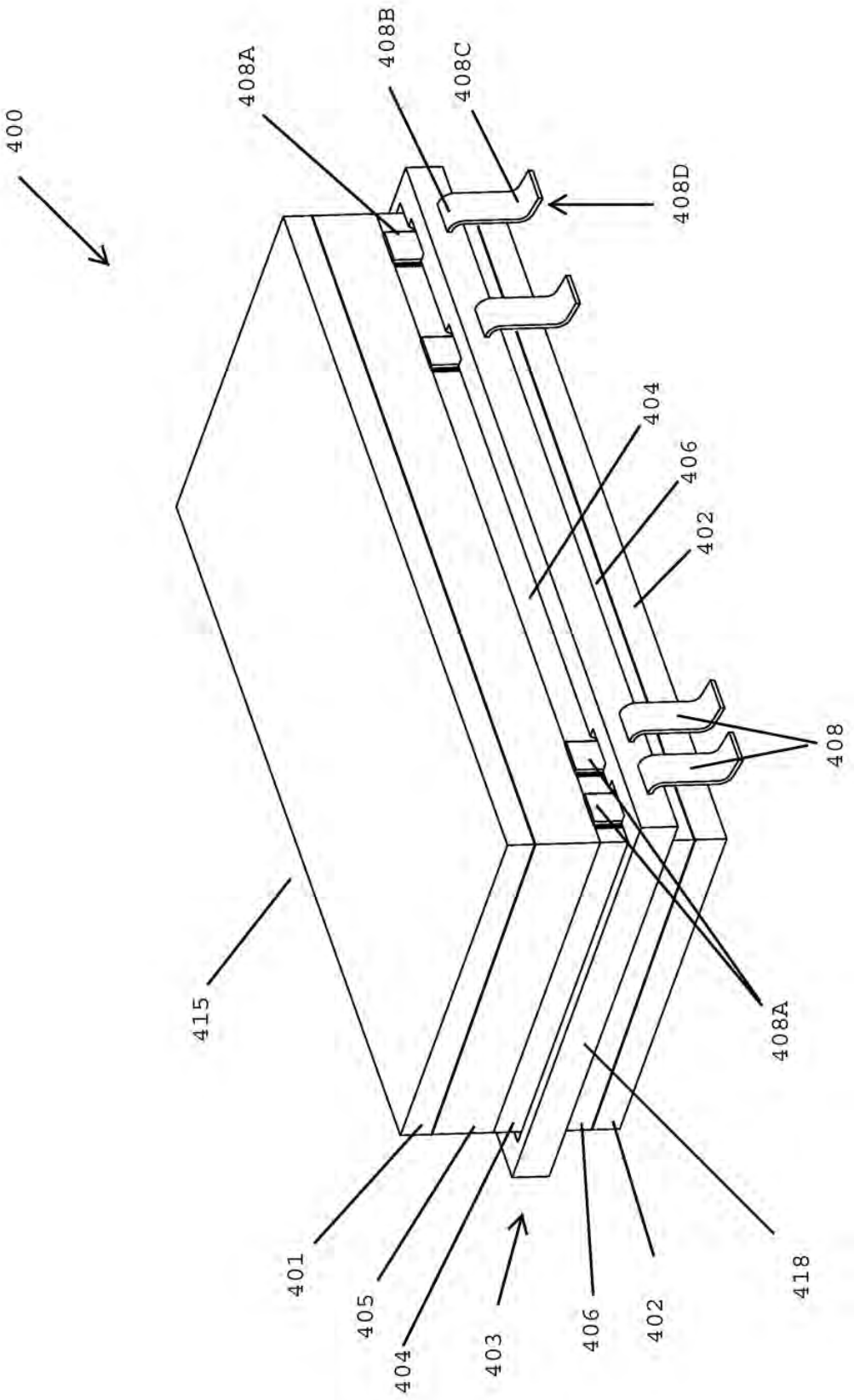

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FIG. 19

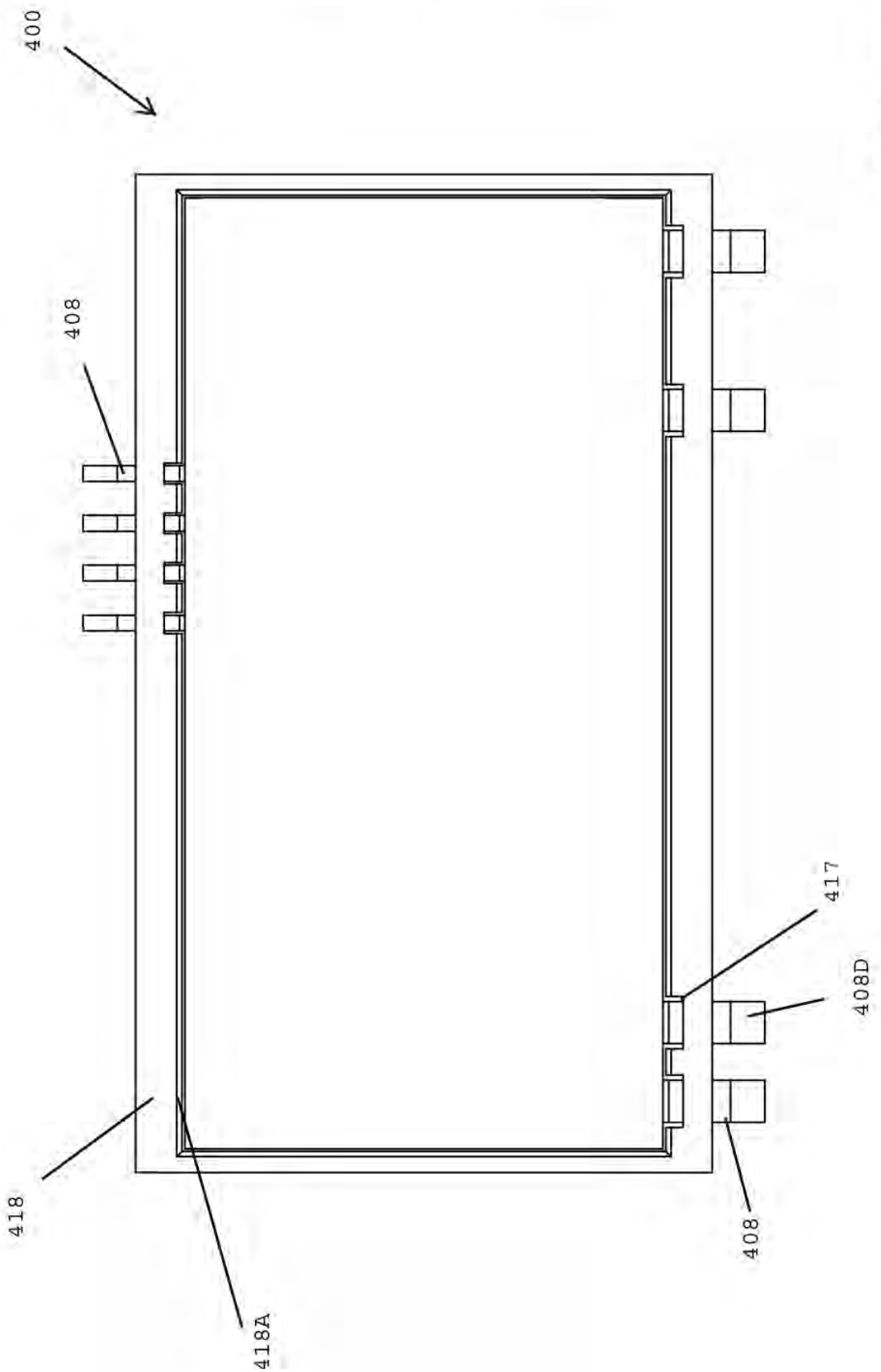


FIG. 20

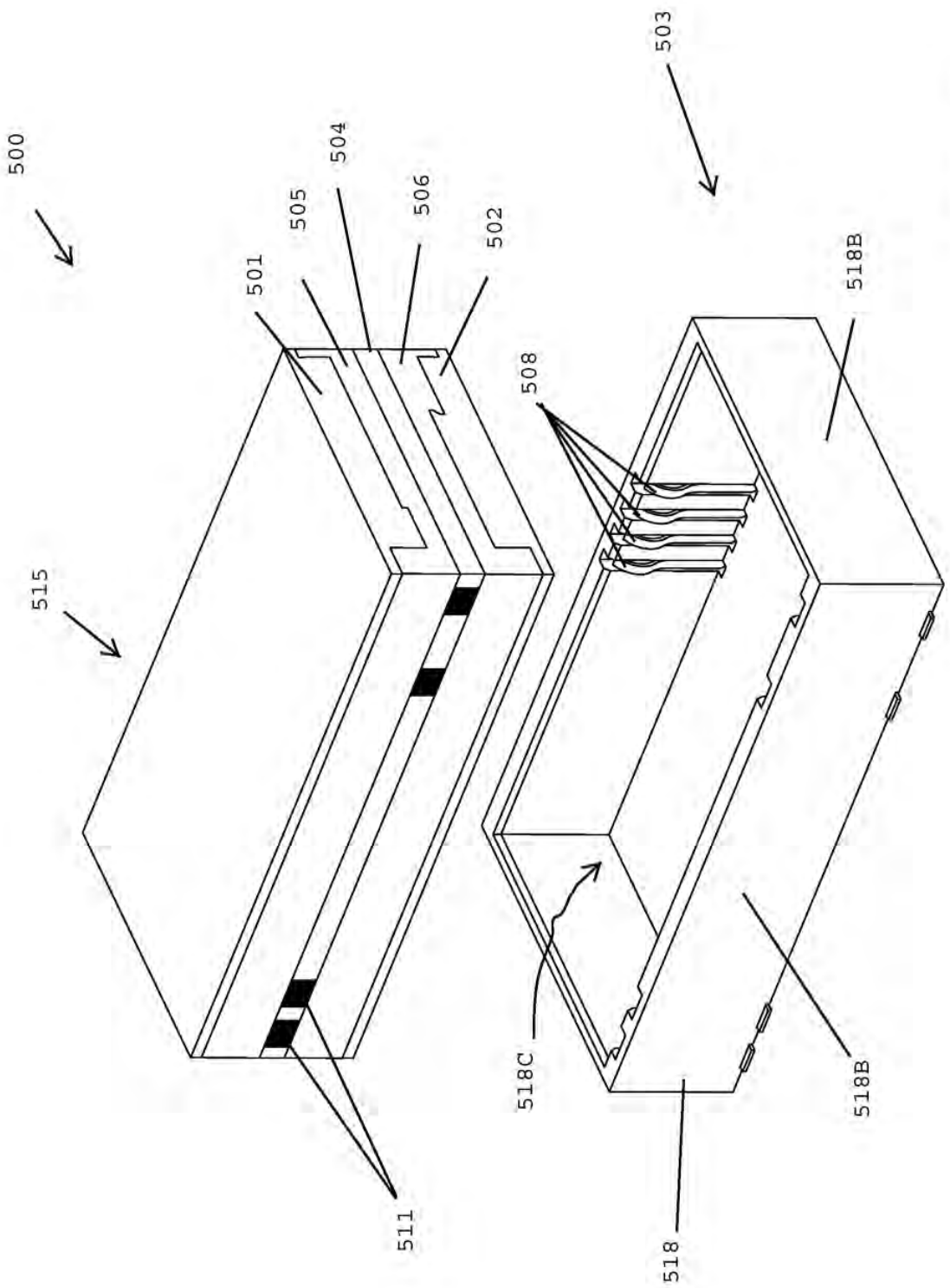


FIG. 21

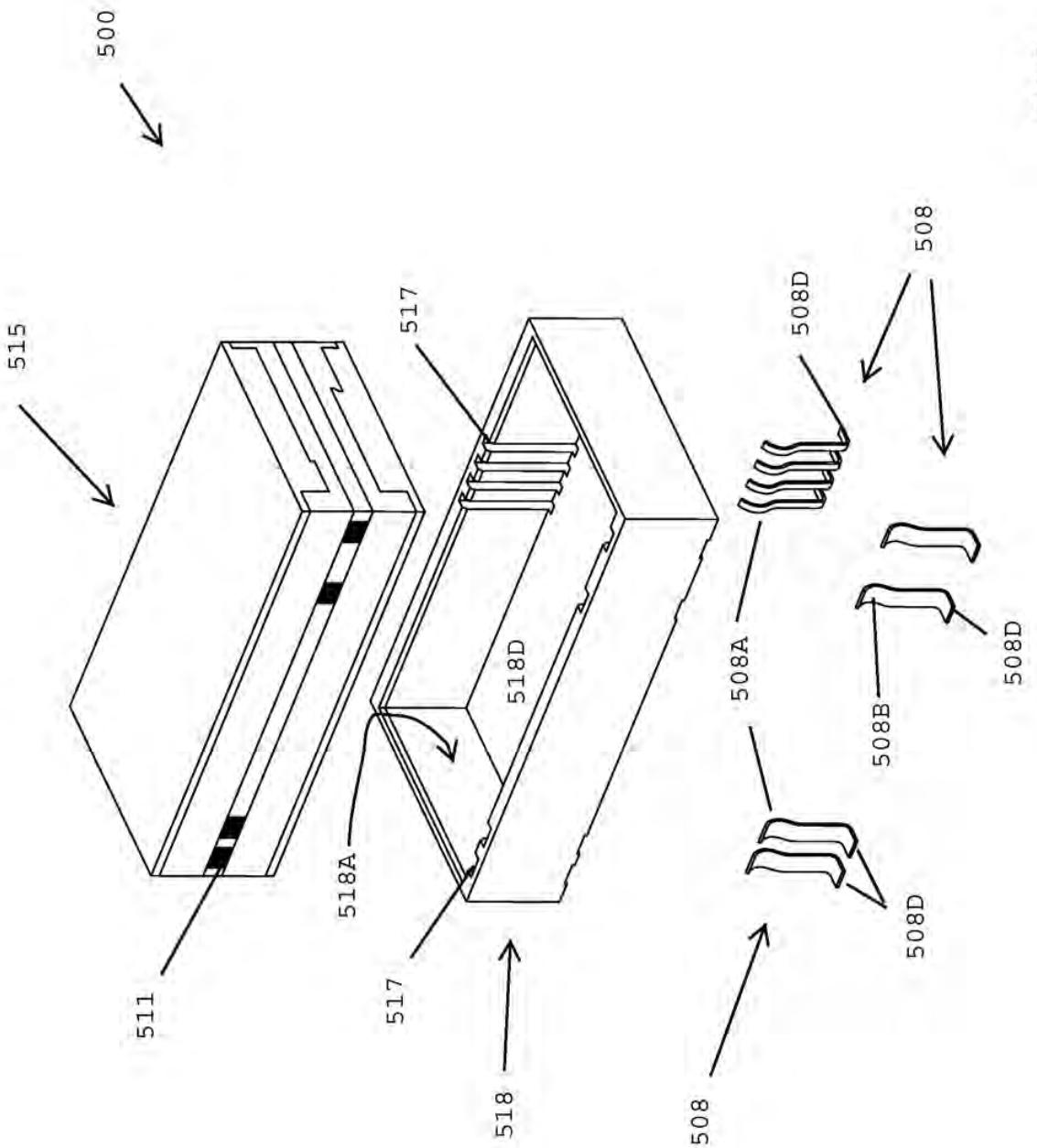

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FIG. 22

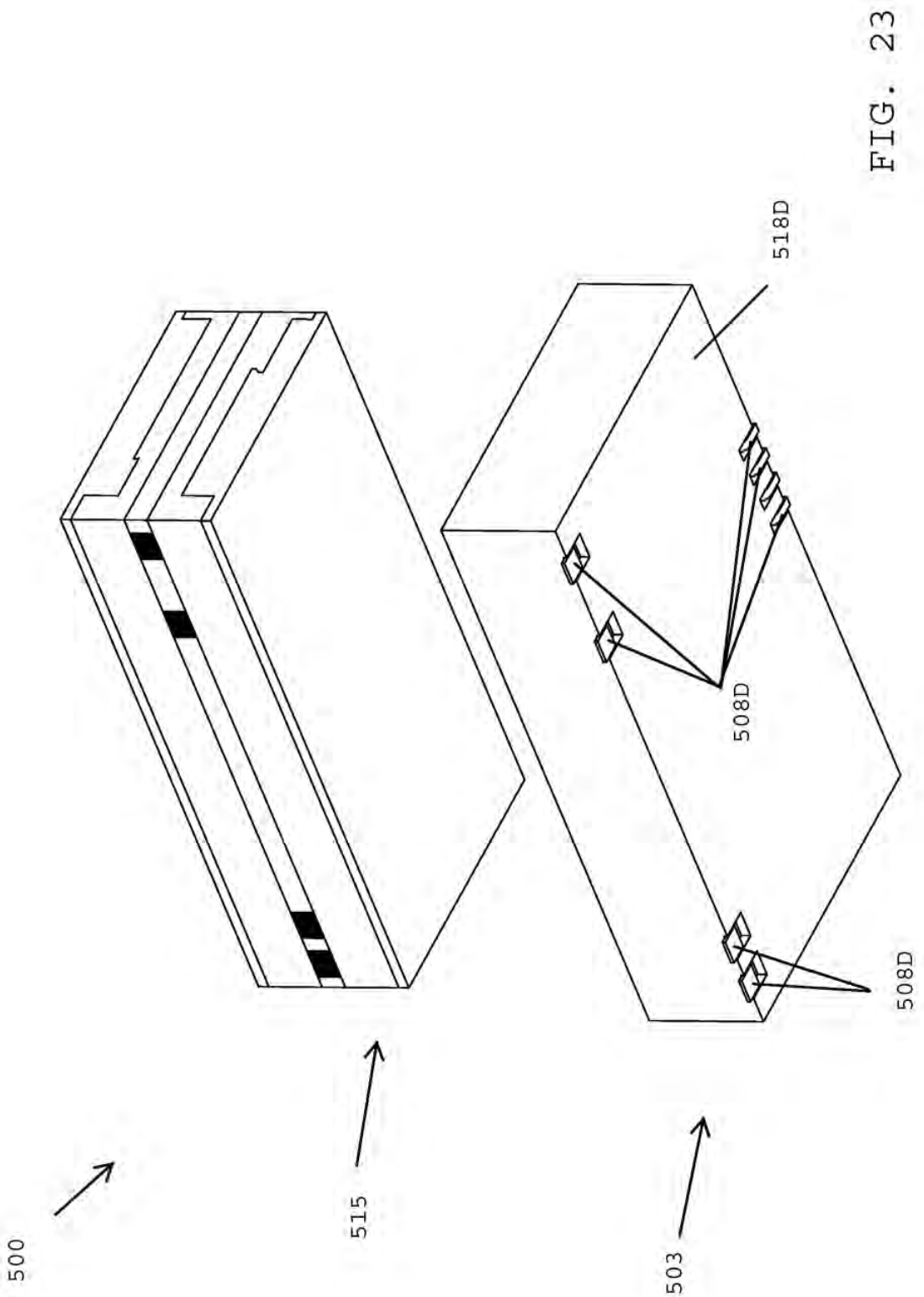


FIG. 23

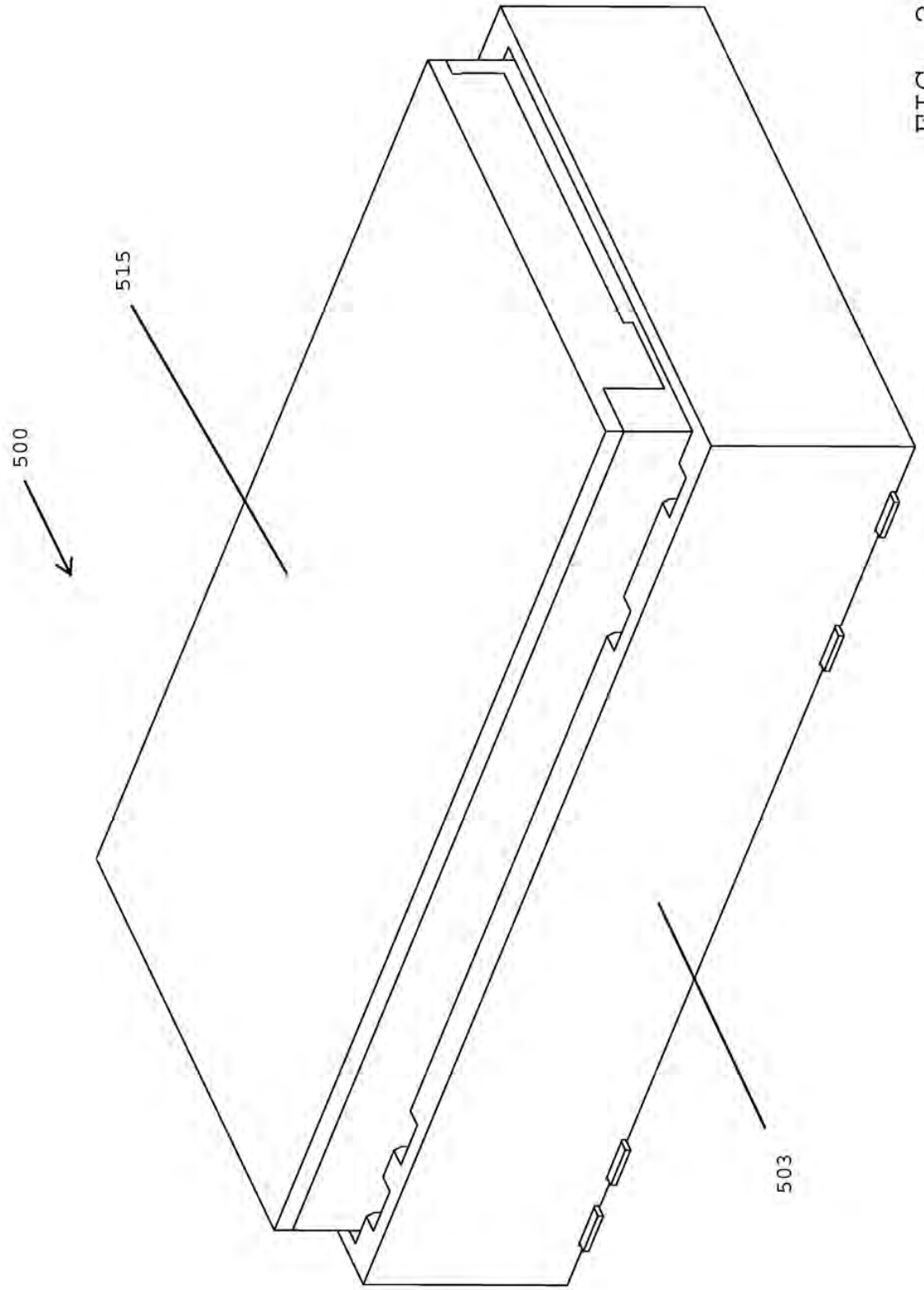


FIG. 24

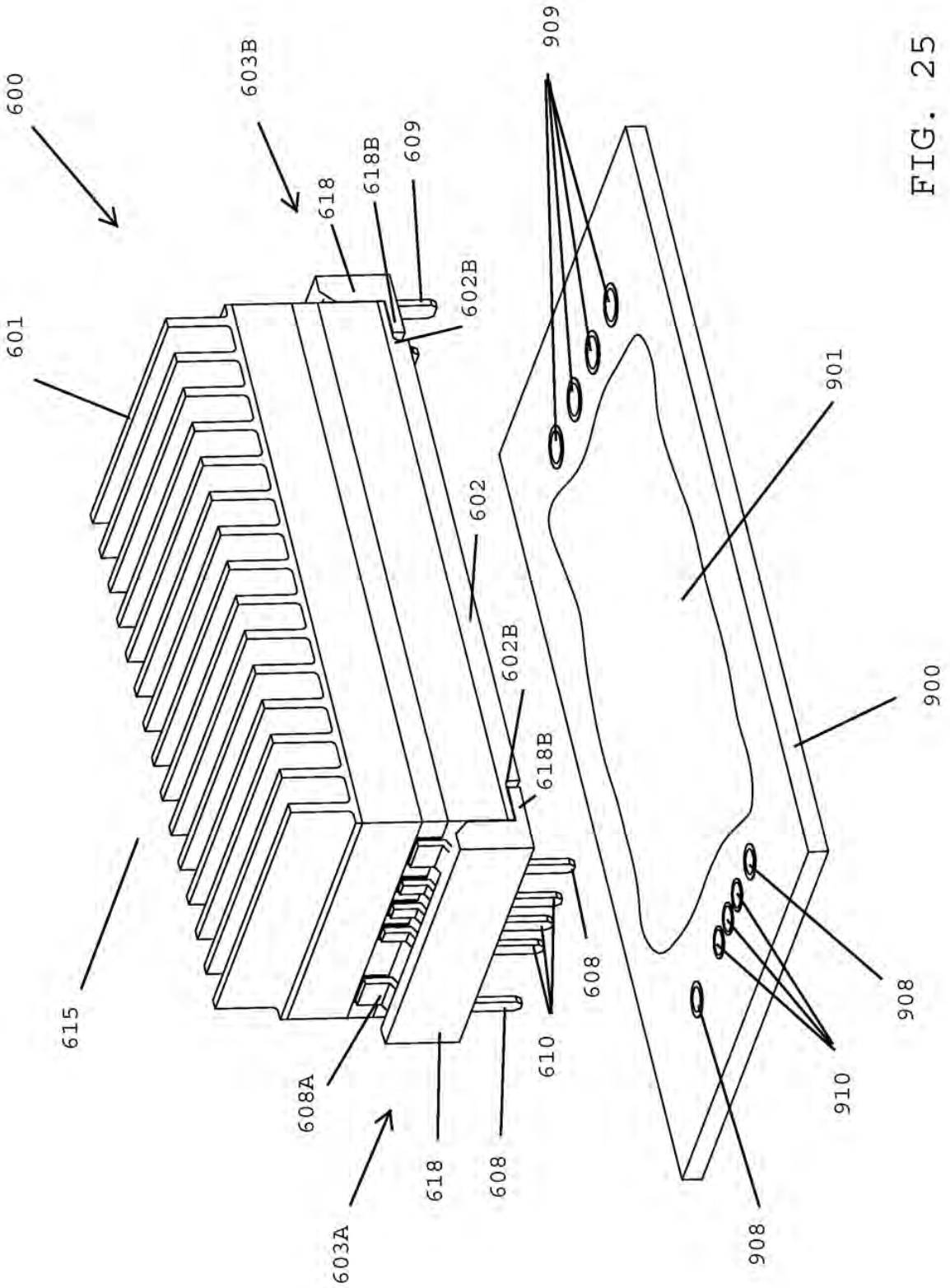

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FIG. 25

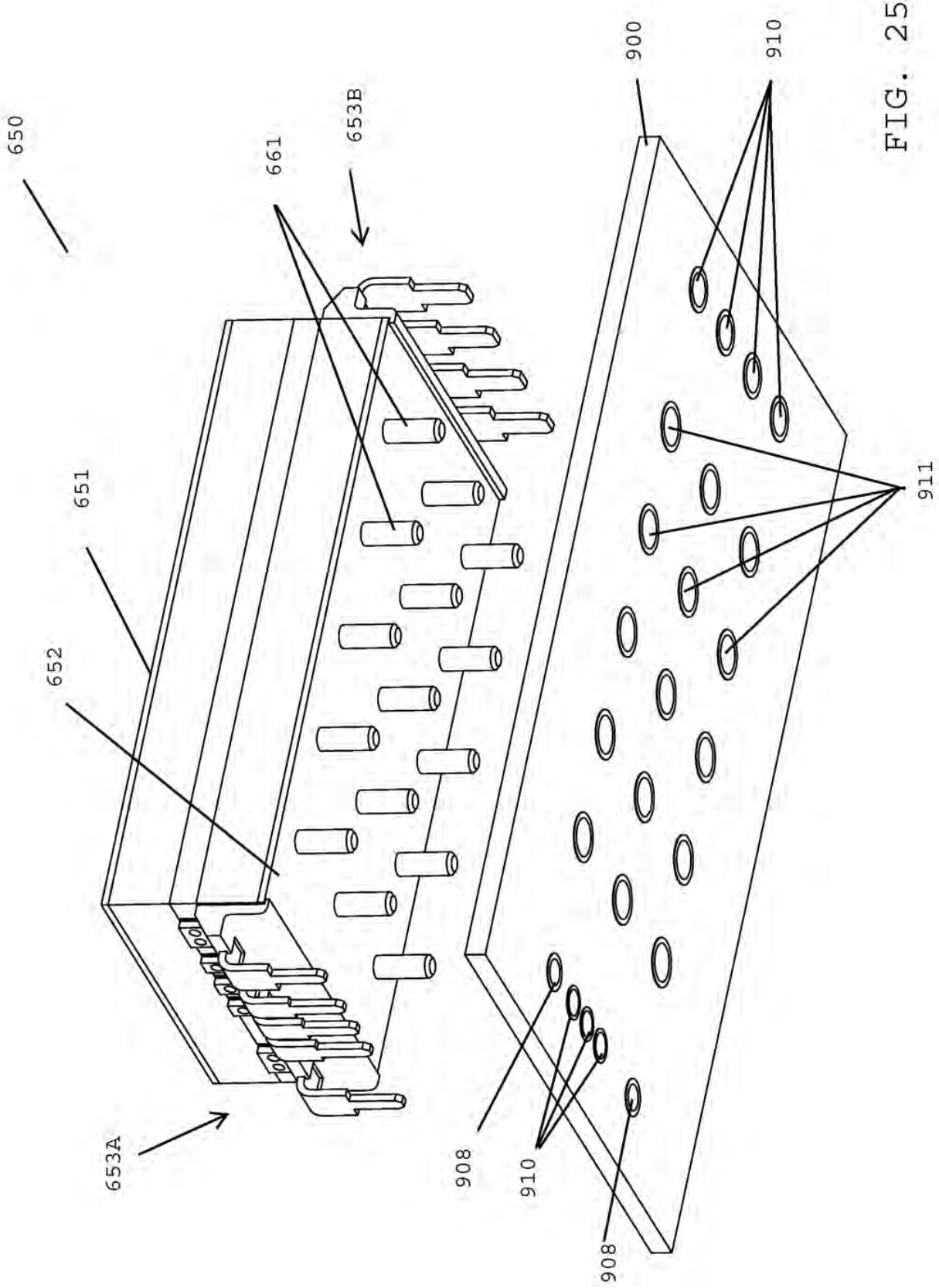


FIG. 25A

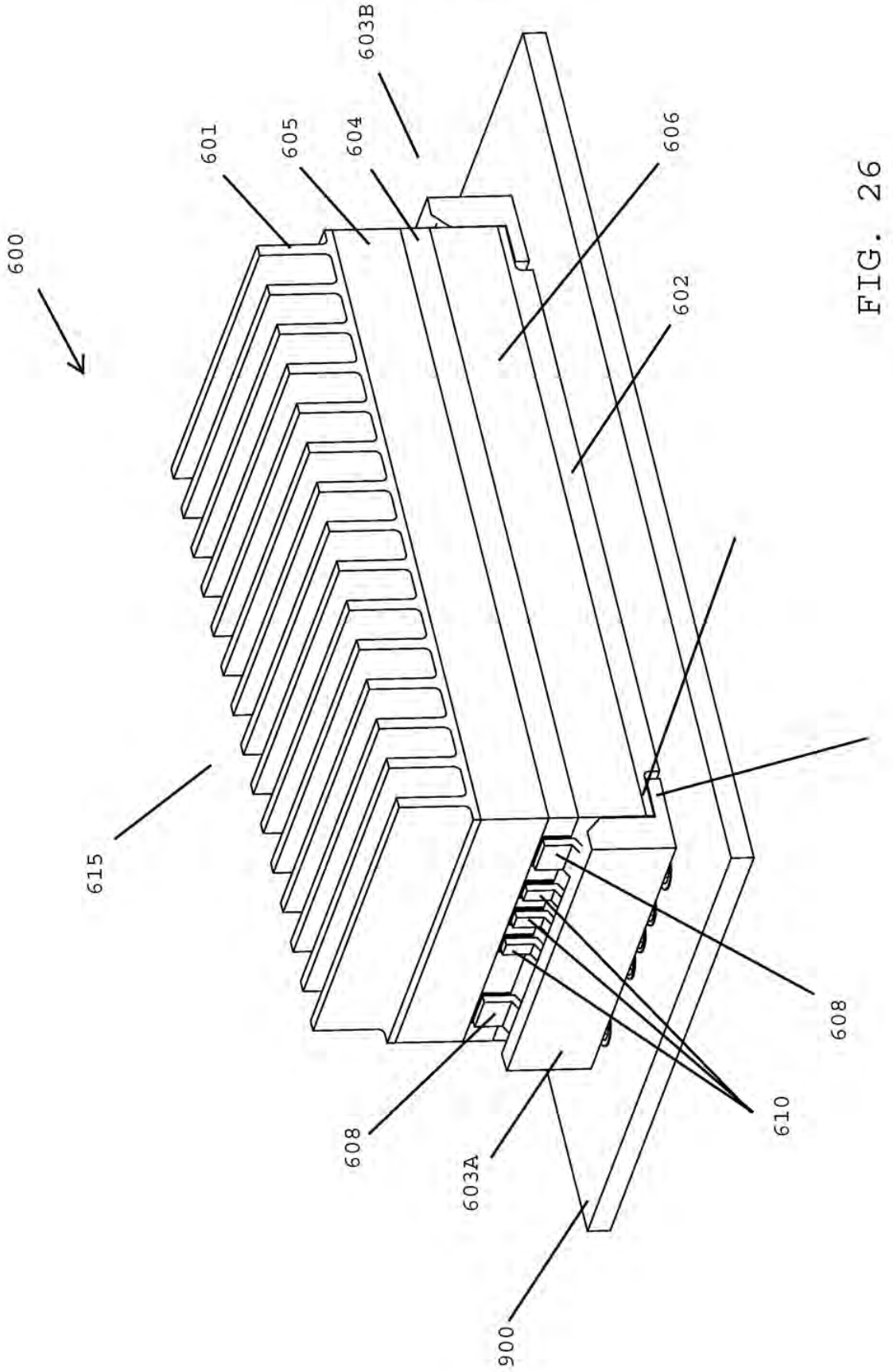


FIG. 26

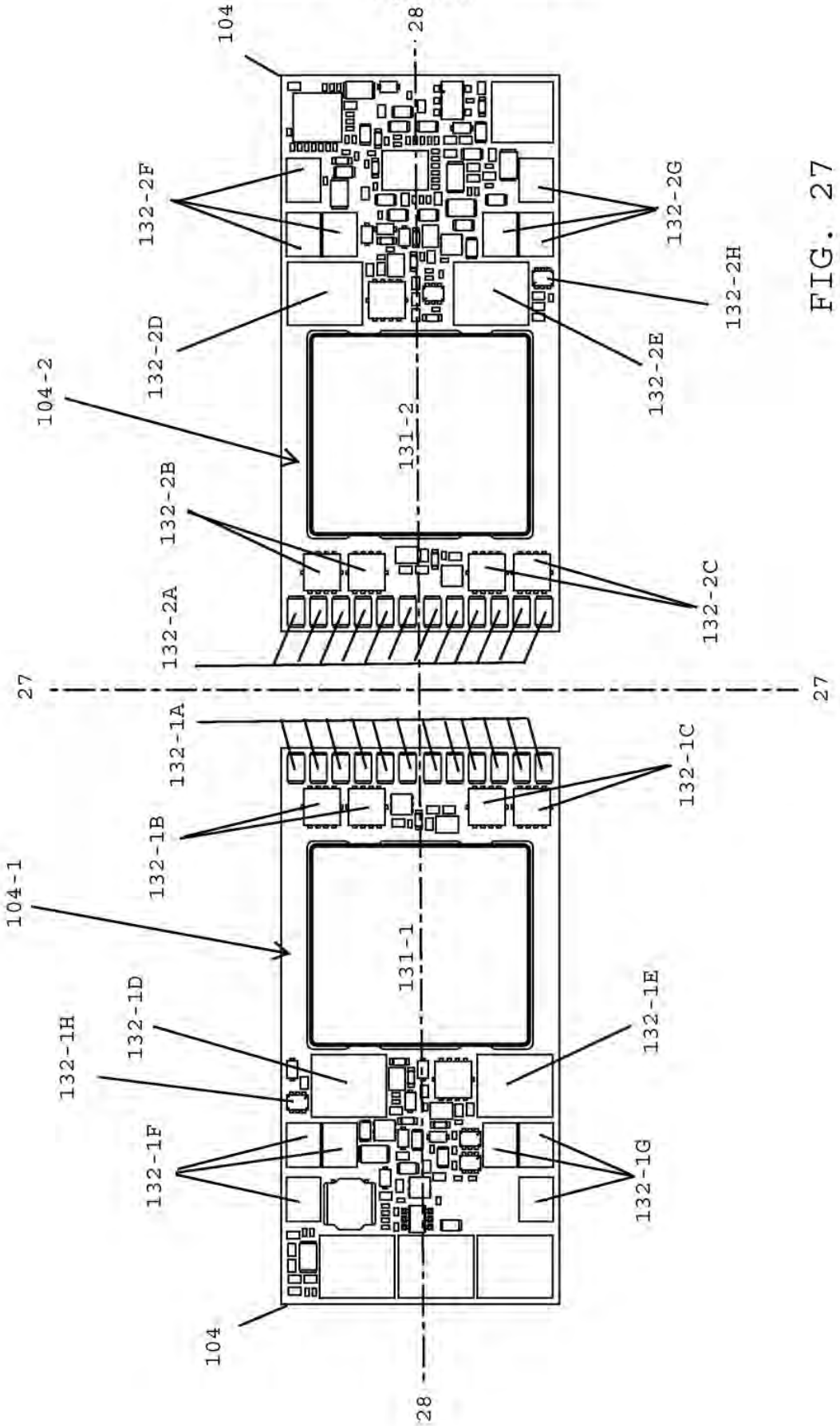

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FIG. 27

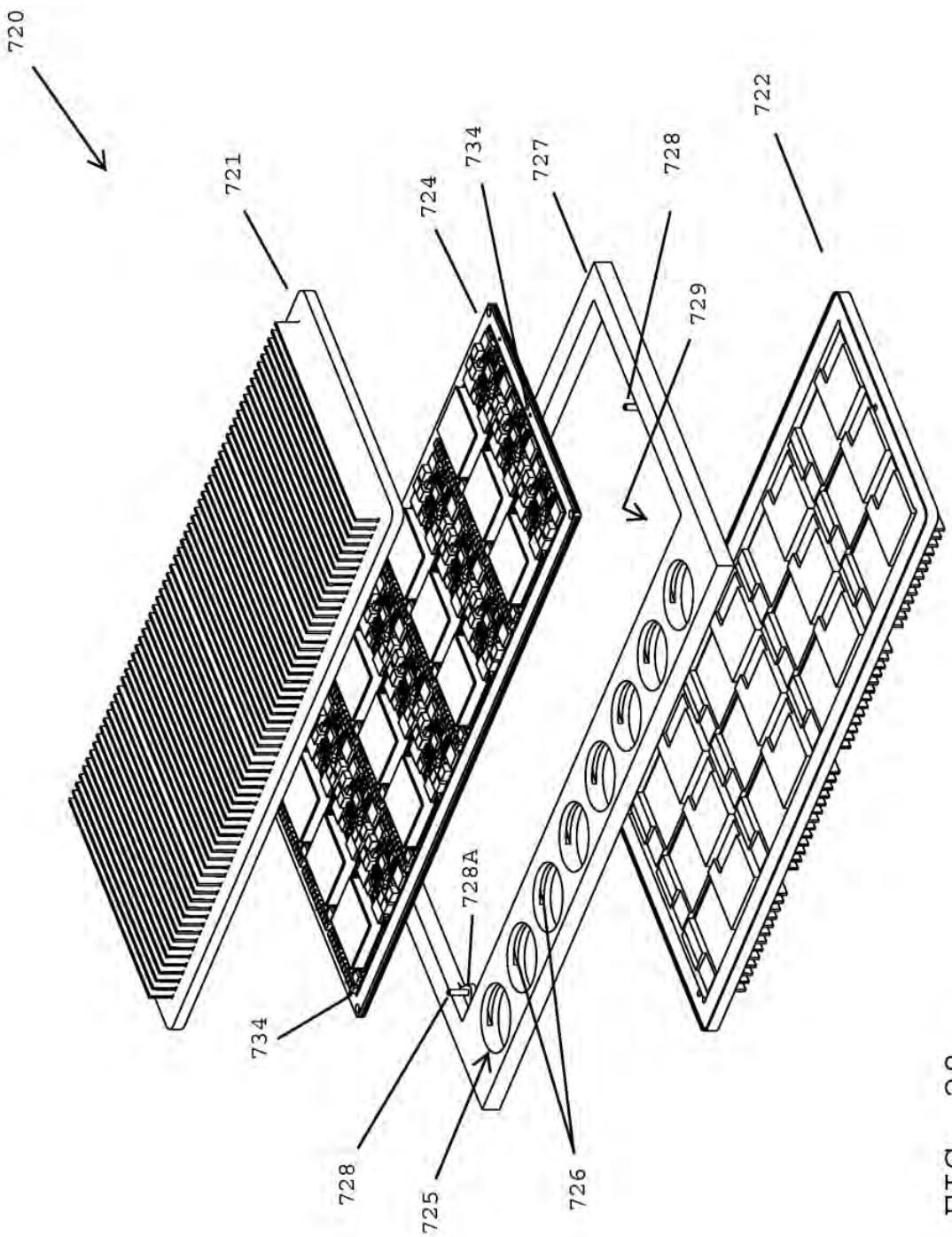


FIG. 28

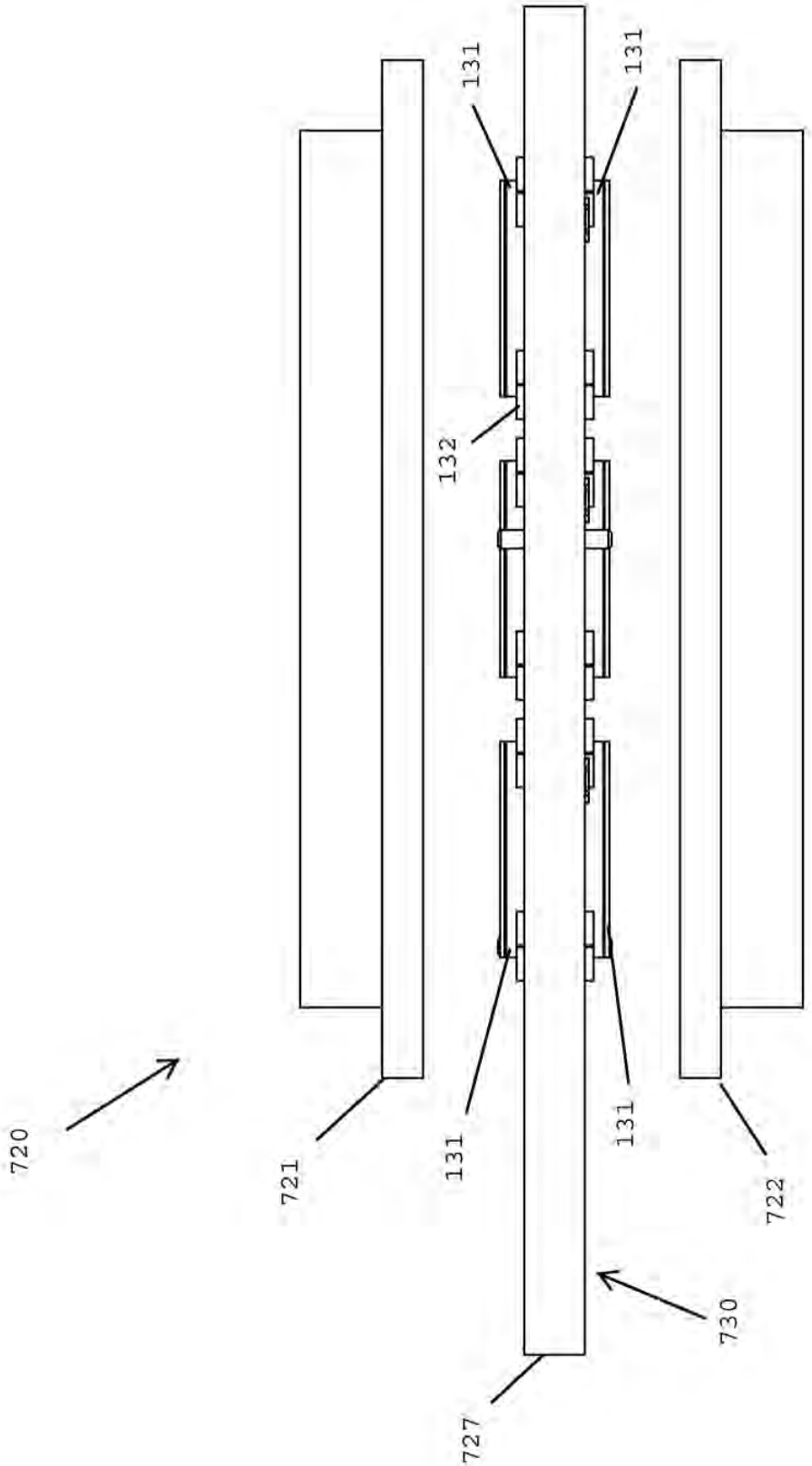


FIG. 29

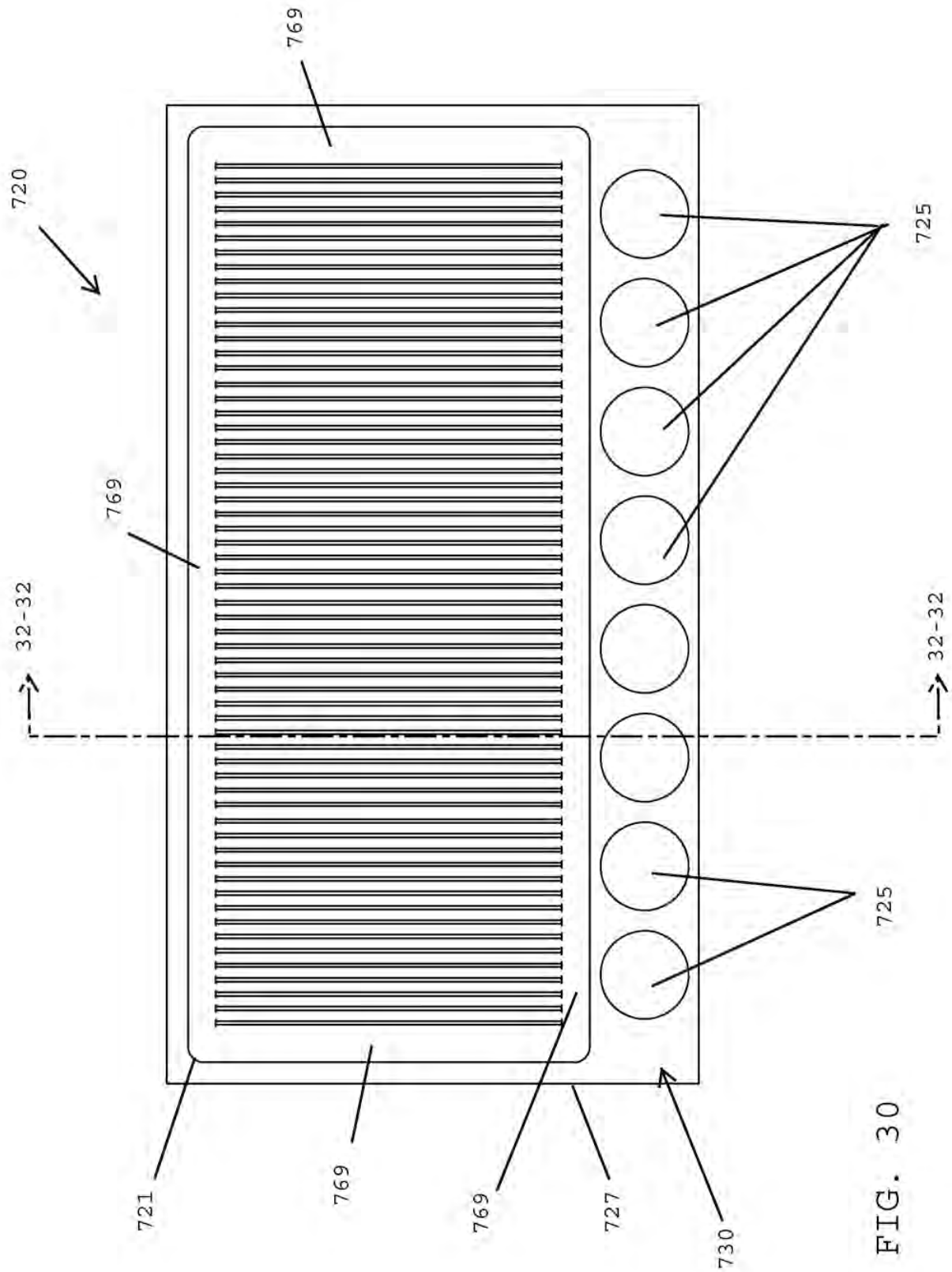


FIG. 30

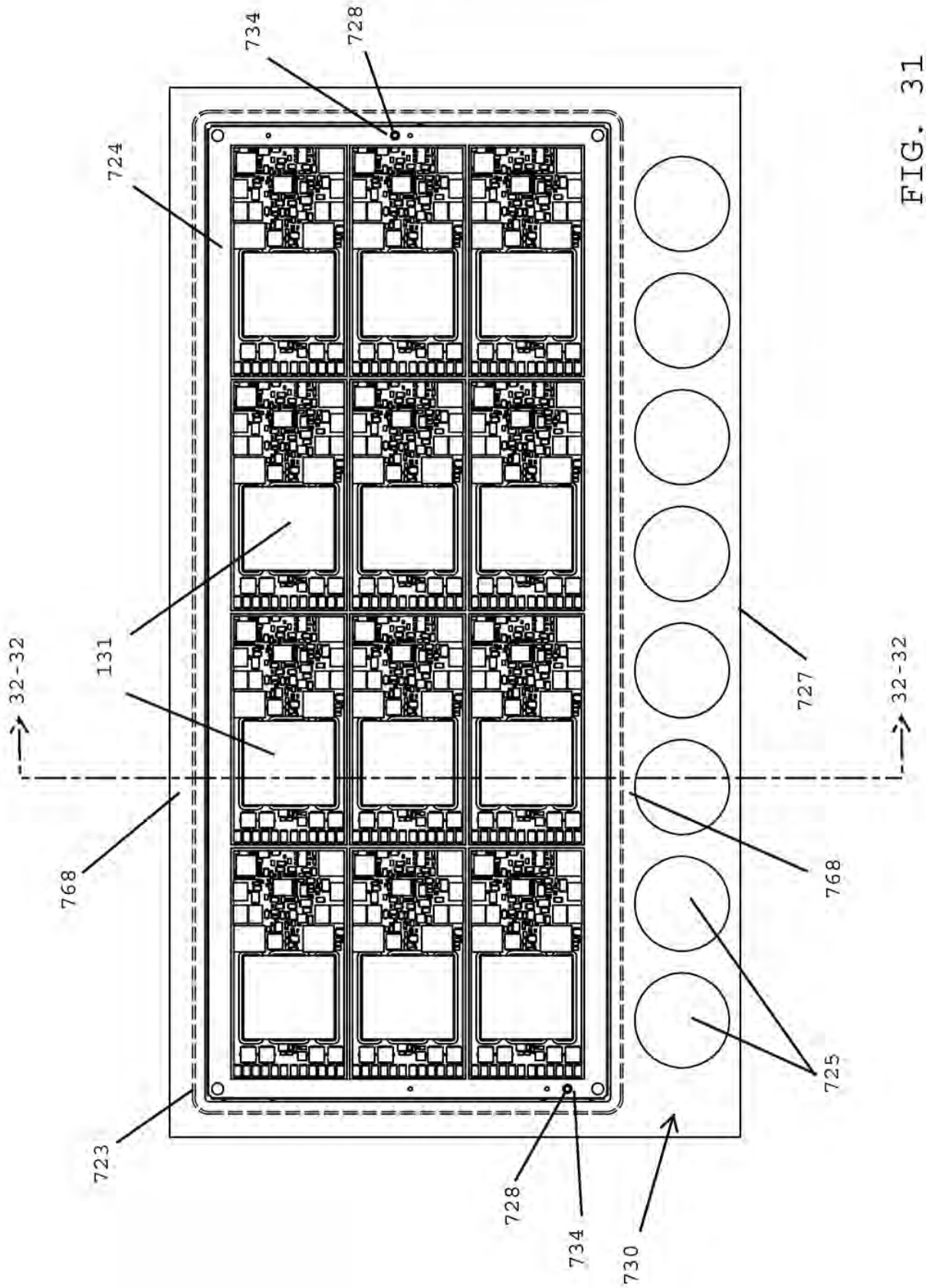


FIG. 31

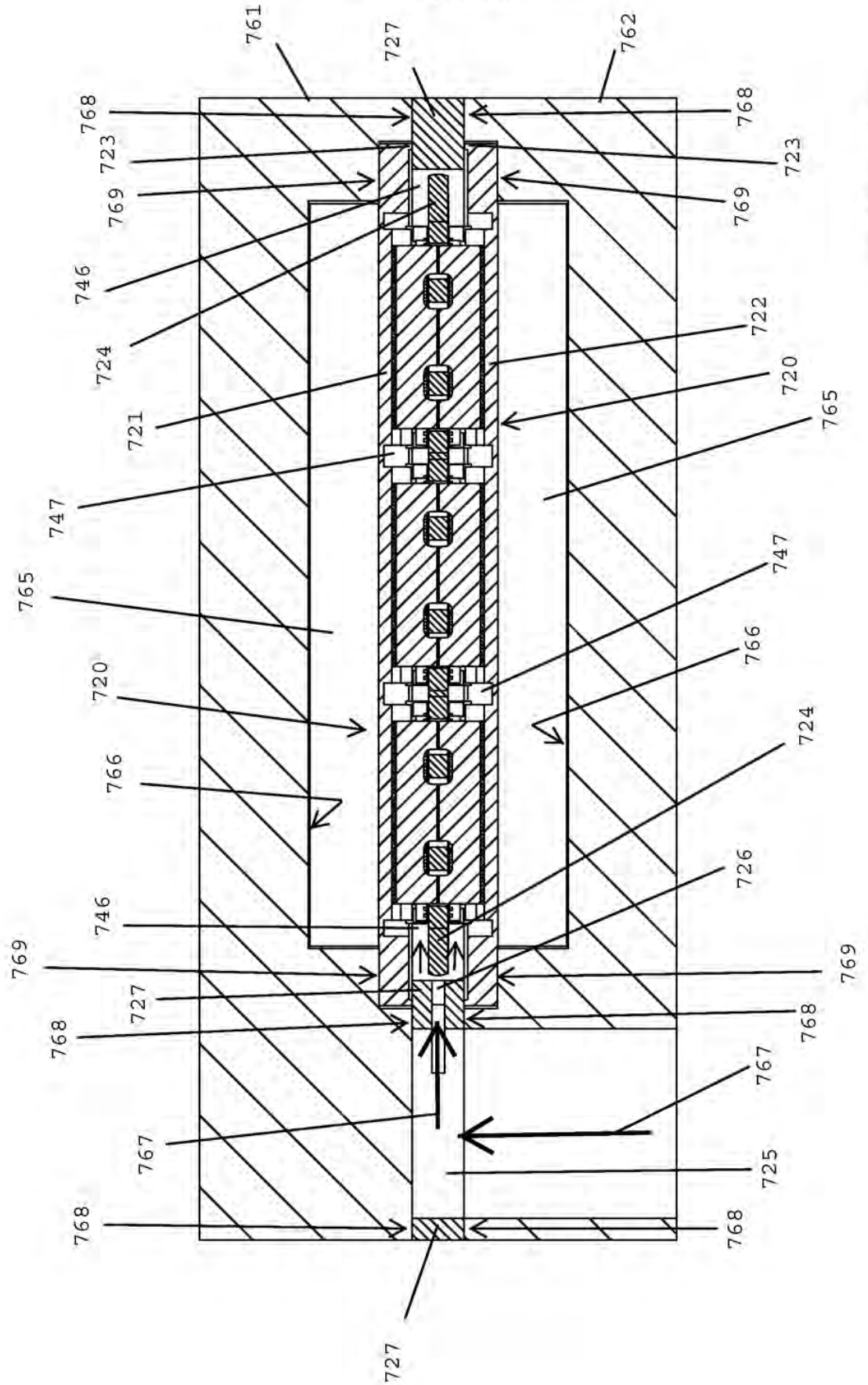

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FIG. 32

Electronic Acknowledgement Receipt

EFS ID:	21966996
Application Number:	14635467
International Application Number:	
Confirmation Number:	1058
Title of Invention:	PANEL-MOLDED ELECTRONIC ASSEMBLIES
First Named Inventor/Applicant Name:	Patrizio Vinciarelli
Customer Number:	26214
Filer:	INDRANIL SARKAR/Paul Micele
Filer Authorized By:	INDRANIL SARKAR
Attorney Docket Number:	00614-0168003
Receipt Date:	03-APR-2015
Filing Date:	02-MAR-2015
Time Stamp:	14:55:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		168003.pdf	3158169 7f0c69bf2fed754970c59b5Ba01760fb920f[illegible] edR	yes	109

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	Document Description	**Start**	**End**
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/635,467	03/02/2015	Patrizio Vinciarelli	00614-0168003

CONFIRMATION NO. 1058

26214
FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

PUBLICATION NOTICE



Title:PANEL-MOLDED ELECTRONIC ASSEMBLIES

Publication No.US-2015-0181727-A1
Publication Date:06/25/2015

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Substitute Disclosure Form	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 00614-0168003	Application No. 14/635,467
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant VLT, Inc.	
		Filing Date March 2, 2015	Group Art Unit

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1.	7,030,469	4/18/2006	Mahadevan et al.			

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	2.							

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	3.	

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Substitute Disclosure Form

Electronic Acknowledgement Receipt

EFS ID:	24019781
Application Number:	14635467
International Application Number:	
Confirmation Number:	1058
Title of Invention:	PANEL-MOLDED ELECTRONIC ASSEMBLIES
First Named Inventor/Applicant Name:	Patrizio Vinciarelli
Customer Number:	26214
Filer:	Rex I. Huang/Rita Liston
Filer Authorized By:	Rex I. Huang
Attorney Docket Number:	00614-0168003
Receipt Date:	09-NOV-2015
Filing Date:	02-MAR-2015
Time Stamp:	10:40:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		00614_0168003_IDS.pdf	172576 bc6f10fb4e5bb74f6522ae75373dd2c3a81 27c6	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	1
	Information Disclosure Statement (IDS) Form (SB08)	2	2
Warnings:			
Information:			
	Total Files Size (in bytes):	172576	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
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National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor	:	Patrizio Vinciarelli	Art Unit	:	Unknown
Serial No.	:	14/635,467	Examiner	:	Unknown
Filed	:	March 2, 2015	Conf. No.	:	1058
Title	:	PANEL-MOLDED ELECTRONIC ASSEMBLIES			

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Please consider the reference listed on the enclosed PTO-SB-08 or Disclosure Form. The cited U.S. patent will be provided on request.

This statement is being filed within three months of the filing date of the application or before the receipt of a first action on the merits.

Apply any necessary charges or credits to deposit account 06-1050, referencing the above attorney docket number.

Please contact the undersigned if there are any questions regarding this Statement.

Respectfully submitted,

Date: November 9. 2015_____

/Rex I. Huang/_____
Rex I. Huang
Reg. No. 57,661

Customer Number 26214
Fish & Richardson P.C.
Telephone: (617) 542-5070
Facsimile: (877) 769-7945

23457650.doc

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/635,467	03/02/2015	Patrizio Vinciarelli	00614-0168003	1058

26214 7590 11/19/2015
FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
ARBES, CARL J	

ART UNIT	PAPER NUMBER
3729	

NOTIFICATION DATE	DELIVERY MODE
11/19/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No. 14/635,467	Applicant(s) VINCIARELLI ET AL.	
	Examiner CARL ARBES	Art Unit 3729	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *49-142* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *49-142* are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 49-72, drawn to an apparatus including a mold panel, classified in H05K 5/064.

II. Claims 73-135, drawn to an apparatus including a panel assembly, classified in H05K 5/064.

III. Claims136-142, drawn to an apparatus including a power converter, classified in H05K 5/0047.

The inventions are distinct, each from the other because of the following reasons:

Inventions I, II and III are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different designs, modes of operation, and effects (MPEP § 802.01 and § 806.06). In the instant case, the different inventions In Group I the alleged invention is directed to *inter alia* a clamp region located at point along a circumference... whereas in Group II the alleged invention is directed to contain a plurality of components in an active circuit area and whereas Group III alleged invention is directed to power converter including a circuit board. Moreover even though Groups I and II have the same or similar PC classifications nevertheless the searches and future prosecutions for the Groups would be divergent

.Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because one or more of the following reasons apply:

Cf Remarks hereinaboive).

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention.**

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out

supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be corrected in compliance with 37 CFR 1.48(a) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. A request to correct inventorship under 37 CFR 1.48(a) must be accompanied by an application data sheet in accordance with 37 CFR 1.76 that identifies each inventor by his or her legal name and by the processing fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CARL ARBES whose telephone number is (571)272-4563. The examiner can normally be reached on M,T,R,F 8:00--6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, P Vo can be reached on 571-272-4419. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/CARL ARBES/
Primary Examiner, Art Unit 3729

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1058

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/635,467	03/02/2015	029	3729	00614-0168003

APPLICANTS
VLT, Inc., Sunnyvale, CA;

INVENTORS
Patrizio Vinciarelli, Boston, MA;
Michael B. LaFleur, East Hampstead, NH;
Sean Timothy Fleming, Worcester, MA;
Rudolph F. Mutter, North Andover, MA;
Andrew T. D'Amico, Beverly Hills, CA;

**** CONTINUING DATA ***************************
This application is a DIV of 13/105,696 05/11/2011 PAT 8966747

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
03/16/2015

Foreign Priority claimed ☐ Yes ☐ No 35 USC 119(a-d) conditions met ☐ Yes ☐ No Verified and Acknowledged _____ Examiner's Signature	☐ Met after Allowance _____ Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		MA	38	94	6

ADDRESS
FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022
UNITED STATES

TITLE
PANEL-MOLDED ELECTRONIC ASSEMBLIES

FILING FEE RECEIVED		
8920	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07)

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14635467	VINCIARELLI ET AL.
	Examiner	Art Unit
	CARL ARBES	3729

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/12/2015								
	1	-								
	2	-								
	3	-								
	4	-								
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CLAIM		DATE								
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CLAIM		DATE								
Final	Original	11/12/2015								
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CLAIM		DATE								
Final	Original	11/12/2015								
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	110	÷								
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	112	÷								
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U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1.	5,557,142	09/1996	Gilmore			
	2.	6,734,552	05/2004	Combs			
	3.	7,015,587	03/2006	Poddar			
	4.	7,049,682	05/2006	Mathews			
	5.	7,198,987	04/2007	Warren			
	6.	8,138,584	03/2012	Wang			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	7.							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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Application Number:	14635467
International Application Number:	
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First Named Inventor/Applicant Name:	Patrizio Vinciarelli
Customer Number:	26214
Filer:	Rex I. Huang/Rita Liston
Filer Authorized By:	Rex I. Huang
Attorney Docket Number:	00614-0168003
Receipt Date:	24-NOV-2015
Filing Date:	02-MAR-2015
Time Stamp:	14:46:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		00614_0168003_IDS_112415.pdf	173691 2cf7b57a4f2bac2a7bff3485099f23773ac92a84	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	1
	Information Disclosure Statement (IDS) Form (SB08)	2	2
Warnings:			
Information:			
	Total Files Size (in bytes):	173691	

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Serial No.	:	14/635,467	Examiner	:	Unknown
Filed	:	March 2, 2015	Conf. No.	:	1058
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Please contact the undersigned if there are any questions regarding this Statement.

Respectfully submitted,

Date: November 24, 2015

/Rex I. Huang/
Rex I. Huang
Reg. No. 57,661

Customer Number 26214
Fish & Richardson P.C.
Telephone: (617) 542-5070
Facsimile: (877) 769-7945

23462685.doc

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor :	Patrizio Vinciarelli	Art Unit :	3729
Serial No. :	14/635,467	Examiner :	Carl J. Arbes
Filed :	March 2, 2015	Conf. No. :	1058
Title :	PANEL-MOLDED ELECTRONIC ASSEMBLIES		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO RESTRICTION REQUIREMENT

In response to the restriction requirement made in the action dated November 19, 2015, identified Group III (claims 136-142) is elected for examination. The election is made without traverse.

Please apply any necessary charges or credits to Deposit Account No. 06-1050, referencing the above attorney docket number.

Respectfully submitted,

Date: December 8, 2015

/Rex I. Huang/
Rex I. Huang
Reg. No. 57,661

Customer Number 26214
Fish & Richardson P.C.
Telephone: (617) 542-5070
Facsimile: (877) 769-7945

23467443.doc

Electronic Acknowledgement Receipt

EFS ID:	24297369
Application Number:	14635467
International Application Number:	
Confirmation Number:	1058
Title of Invention:	PANEL-MOLDED ELECTRONIC ASSEMBLIES
First Named Inventor/Applicant Name:	Patrizio Vinciarelli
Customer Number:	26214
Filer:	Rex I. Huang/Rita Liston
Filer Authorized By:	Rex I. Huang
Attorney Docket Number:	00614-0168003
Receipt Date:	08-DEC-2015
Filing Date:	02-MAR-2015
Time Stamp:	15:49:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	00614_0168003_Resp_RR.pdf	63100 3edb7e3dbd2c78a7f3191ceddde6cbe555f2841a	no	1
Warnings:					
Information:					

Total Files Size (in bytes):	63100

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Substitute Disclosure Form	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 00614-0168003	Application No. 14/635,467
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant VLT, Inc.	
		Filing Date March 2, 2015	Group Art Unit 3729

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1.	2003/0011054	01/16/2003	Jeun et al.			
	2.	2006/0097831	05/11/2006	Lotfi et al.			
	3.	2010/0259909	10/14/2010	Ho et al.			
	4.	4,326,765	04/27/1982	Brancaleone			
	5.	4,326,765	04/27/1982	Brancaleone			
	6.	6,184,585	02/06/2001	Martinez et al.			
	7.	7,554,181	06/30/2009	Satou et al.			
	8.						

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	9.							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	10.	

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Substitute Disclosure Form

Electronic Acknowledgement Receipt

EFS ID:	24959769
Application Number:	14635467
International Application Number:	
Confirmation Number:	1058
Title of Invention:	PANEL-MOLDED ELECTRONIC ASSEMBLIES
First Named Inventor/Applicant Name:	Patrizio Vinciarelli
Customer Number:	26214
Filer:	Rex I. Huang/Rita Liston
Filer Authorized By:	Rex I. Huang
Attorney Docket Number:	00614-0168003
Receipt Date:	19-FEB-2016
Filing Date:	02-MAR-2015
Time Stamp:	10:02:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		06547_0168003_IDS.pdf	173818 d516e69d7ac9262b6bd40c58a104d5eac4da2fad	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	1
	Information Disclosure Statement (IDS) Form (SB08)	2	2
Warnings:			
Information:			
	Total Files Size (in bytes):	173818	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor	:	Patrizio Vinciarelli	Art Unit	:	3729
Serial No.	:	14/635,467	Examiner	:	Carl J. Arbes
Filed	:	March 2, 2015	Conf. No.	:	1058
Title	:	PANEL-MOLDED ELECTRONIC ASSEMBLIES			

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Please consider the references listed on the enclosed PTO-SB-08 or Disclosure Form. Cited U.S. patents and patent application publications will be provided on request.

This statement is being filed before the receipt of a first action on the merits. No fee is believed to be due.

Apply any necessary charges or credits to deposit account 06-1050, referencing the above attorney docket number.

Please contact the undersigned if there are any questions regarding this Statement.

Respectfully submitted,

Date: February 19, 2016

/Rex I. Huang/
Rex I. Huang
Reg. No. 57,661

Customer Number 26214
Fish & Richardson P.C.
Telephone: (617) 542-5070
Facsimile: (877) 769-7945

23490939.doc

Substitute Disclosure Form	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 00614-0168003	Application No. 14/635,467
Information Disclosure Statement by Applicant (Use several sheets if necessary)		Applicant VLT, Inc.	
(37 CFR §1.98(b))		Filing Date March 2, 2015	Group Art Unit 3729

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1.	5,471,366	11/28/1995	Ozawa			
	2.						
	3.						
	4.						
	5.						
	6.						
	7.						
	8.						

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	9.							

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	10.	

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Substitute Disclosure Form

Electronic Acknowledgement Receipt

EFS ID:	24959830
Application Number:	14635467
International Application Number:	
Confirmation Number:	1058
Title of Invention:	PANEL-MOLDED ELECTRONIC ASSEMBLIES
First Named Inventor/Applicant Name:	Patrizio Vinciarelli
Customer Number:	26214
Filer:	Rex I. Huang/Rita Liston
Filer Authorized By:	Rex I. Huang
Attorney Docket Number:	00614-0168003
Receipt Date:	19-FEB-2016
Filing Date:	02-MAR-2015
Time Stamp:	10:08:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	1449.pdf	104835 b992039b640f70ccf3071aa031e5523c922b5d36	no	1

Warnings:	
Information:	

This is not an USPTO supplied IDS fillable form	
Total Files Size (in bytes):	104835

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
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Substitute Disclosure Form	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 00614-0168003	Application No. 14/635,467
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant VLT, Inc.	
		Filing Date March 2, 2015	Group Art Unit 3729

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1.						
	2.						

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	3.							

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	4.	USPTO Office Action; U.S. Patent Application Serial No. 13/105,696; mailed 09/25/2013
	5.	USPTO Office Action; U.S. Patent Application Serial No. 14/116,642; mailed 02/09/2016
	6.	USPTO Office Action; U.S. Patent Application Serial No. 14/635,420; mailed 10/22/2015.

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Substitute Disclosure Form

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105,696	05/11/2011	Patrizio Vinciarelli	00614-0168001	3765

26214 7590 09/25/2013
FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
ARBES, CARL J	
ART UNIT	PAPER NUMBER
3729	

NOTIFICATION DATE	DELIVERY MODE
09/25/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No. 13/105,696	Applicant(s) VINCIARELLI ET AL.	
	Examiner CARL ARBES	Art Unit 3729	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2013*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *34-48 and 146-152* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *34-48 and 146-148* is/are rejected.

8)☒ Claim(s) *149-152* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *11 May 2011* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *herein*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

4) ☐ Other: _____.

> The following is a quotation of 35 U.S.C. 112(b):
> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.
>
> The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 38, 39, 45 and 146 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention. To the extent that the language ...attaching a lead of an adapter... is not understood claim 38 is held to be unclear, vague and indefinite. Where is "an adapter" defined? What is its purpose or function? What does it adapt? With respect claim 39 what does the language ... covering at least one surface of the substrate in the area... mean? Covering the surface with what? Is the surface covered with air? Is the surface covered with paint? If so what type? Claim 39 is held to be unclear, vague and indefinite. As applied to claim 45 it is not understood what Applicants intend when they recite...the conductive via is buried in the substrate.... By definition a via a conductive or non-conductive hole or region that in located in a substrate. That substantially all conductive vias are "buried in substrates". What is it that Applicants intend by this language? Claim 45 is held to be unclear, vague and indefinite.

Claims 34-47,146 and 147 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gilbert et al (Pat No. 4,551,747); hereinafter Gilbert et al.

Gilbert et al teach a carrier apparatus (40) for mounting logic components on the surface of a circuit board (41) The carrier includes bonding structures defining top and bottom surfaces and further defining cavity (50) in the bottom surface for receipt of a logic component (51). A recessed cover portion (56) is attached to the housing. Apparatus (40) includes means for mounting housing onto a circuit board such that cover (56) does not make contact with the surface of the circuit board (41). Housing also includes means for electrically interconnecting component (51) to circuit board (41). (Cf. Abstract). Additionally Gilbert et al teach substrate dielectric layer (46) positioned adjacent first dielectric layer (42) Layer (46) is provided with die cavity (50) for reception of logic components. Layer (46) also includes

also includes elongated electroplated signal leads or traces (48) (Cf. Col. 7). Additionally Gilbert et al teach that substrate dielectric layer (46) have a plurality of spaced, vertically extending, semi-cylindrical indentations or castellations (60) along the edges thereof. (Cf. Col. 8). It would have been obvious to produce layers having vias with conductive material therein and which are integrated to make carrier (40) and then cutting these vias to produce a portion conductive castellations. As applied to claim 35 inasmuch as Gilbert et al teach applying solder paste (70) in cylindrical spaces (69) the limitation recited in said claim 35 is held to have been obvious in view of Gilbert et al. As applied to claim 36 inasmuch as Gilbert et al teach that castellations are gold-plated in order to prevent oxidation (Cf Col. 8) it is held that the limitation recited in said claim 36 would have been obvious in view of Gilbert et al. As applied to claim 37. Gilbert et al teach applying metal layer to one or more conductive features exposed to the cutting Cf e.g .Fig 2-5 and corresponding disclosure) and therefore the limitation recited in said 37 is held to have been obvious in view of Gilbert et al. As applied to claim 38 Gilbert et al teach solder paste (70) used to secure and electrically connect castellation (60) to signal traces (71) (Cf. Col. 9 and Fig.8) and therefore the limitation recited in said claim 38 is held to have been obvious. As applied to claim 40 before dicing (or cutting) the semiconductor wafer (20) there must be some means of determining where to cut so as to expose the conductive features after the cuts are made. A PHOSITA would have understood this without the use of undue skill in this art. Therefore it is held to have been obvious to provide a registration feature having a predetermined relationship to the substrate and using this registration feature to properly align the cutting relative to the cut line. As applied to claim 41-44 inasmuch as Gilbert et al teach providing conductive features in the layers of substrates along the cut lines and are filled with a conductive material e.g. (60, 70) (Cf. e.g. Figs 2,(Cf. e.g. Figs 2,,3, 15 and 17) it is held that the limitations recited in said claims 41-44 would have been obvious in view of Gilbert et al. As applied to claim 45-47 inasmuch as Gilbert et al teach providing vias that contact the surface of the substrate and are filled with conductive material (Cf. e.g. Figs. 1-3, 15 and 17) it would have been obvious to provide that conductive vias are buried, that they contact the surface of the substrate and are filled with a conductive material. As applied to claims 146 and 147 inasmuch as Gilbert et al teach a leadless chip carrier apparatus that can be

connected to a circuit board (Cf. Col. 9 and Fig. 8) it is held that the limitation recited in said claims 146 and 147 would have been obvious in view of Gilbert et al.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 34-39, 41 and 43-47 are further rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Estacio (Pat No. 6,830,959 B2); hereinafter Estacio.

Estacio teaches a semiconductor package with a semiconductor having a side electrical connection. Additionally Estacio teaches semiconductor (20) having a plurality of semiconductor dies (24) formed therein described by scribe lines (22). Each cavity (28) extends partially or entirely through semiconductor wafer (20). These cavities can be formed by means of a photolithographic and etching, well as wet or dry etching, by laser etching or by water-jet etching processes. (Cf. Col. 4). Additionally Estacio teaches dicing (using a saw or a laser) and bumping the semiconductor the castellated recesses (34) receive solder that is placed in the bottom of the recess. (Cf. Col. 5) If indeed Estacio does not specifically teach dicing the semiconductor wafer before the or cavities are diced (to provide castellations) a person of ordinary skill in this art i.e. a PHOSITA would have been able to fill the non-ndiced cavities with conductive material and then dice the cavities to provide the castellations. As applied to claim 35 Estacio teaches solder bumps i.e. 66(a), 66(b) wherein solder bump 66(b)t couples with solder bump (34). (Cf Col. 7) and therefore it is held that the limitation recited iin said claim 35 it would have been obvious in view of Estacio. As applied to claim 36 even if Estacion does not teach a conformal coating to one or more of the conductive features exposed from the cutting (dicing) nevertheless a PHOSITA with the use of ordinary skill would have been able to use such a coating in order to protect the conductive features from oxidation's harmful effects. As applied to claim 37 Estacio teaches solder joint (68) to castellations that are formed in the semiconductor die and this joint is connect to solder bump (32). (Cf. Col. 7). Hence it would have been obvious to apply a conductive layer to the portions of one or more

conductive features exposed from the cutting and hence said claim 37 is held to have been made obvious. As applied to claim 40 before dicing (or cutting) the semiconductor wafer (20) there must be some means of determining where to cut so as to expose the conductive features after the cuts are made. A PHOSITA would have understood this without the use of undue skill in this art. Therefore it is held to have been obvious to provide a registration feature having a predetermined relationship to the substrate and using this registration feature to properly align the cutting relative to the cut line before dicing (or cutting) the semiconductor wafer (20) there had be some means of determining where to cut so as to expose the conductive features after the cuts are made. A PHOSITA would have understood this without the use of undue skill in this art. As applied to claims 39 and 41 instead of cutting the substrate to provide castellations first and then placing conductive material into the cavities or vias a PHIOSITA using only ordinary skill in this art would have been able to introduce the conductive material into the vias first and then cut the substrates to provide conductive castellations on the edges of the substrate. Using only a limited number of attempts the PHOSITA would have been able to accomplish what is recited in said claims 39 and 41. As applied to claims 43-47 inasmuch as Estacio teaches providing conductive vias along. the cut line and filling the vias with conductive material (Cf. e.g. Fig. 1(h) & 3(k) and related disclosure) it is held that the limitation recited in said claims 43-47 would have been obvious in view of Estacio. .

Claims 48 and 148 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gilbert et al in view of Mullen, III et al (Pat. No. 5,241,133); hereinafter Mullen, III et al.

The teaching of Gilbert et al has been provide above and is not repeated. Mullen, III et al teach a leadless pad array chip carrier including a circuit board, an array of solder pads on the bottom side of the circuit board Plastic cover is transfer molded about the semiconductor device.(Cf. Abstract). It would have been obvious to combine he two teachings and to substitute the molded material taught by Mullen, III et al for the lid 956) taught by Gilbert et al since encapsulation of a semiconductor is a patentable equivalent of providing a lid. That is each of these commonly used means is used to protect the semiconductor from exterior environmental conditions. As applied to claim 148 inasmuch as Mullen, III et

al teach encapsulating the surface of the printed circuit board it is held that the limitation recited in said claim 148 would have been obvious in view of the cited prior art.

Claims 149-152 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CARL ARBES whose telephone number is (571)272-4563. The examiner can normally be reached on M, T, R and F from 8 to 6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, D. Banks, can be reached on (571) 272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://portal.uspto.gov/external/portal. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/C. J. Arbes/

Primary Examiner, Art Unit 3729

Notice of References Cited	Application/Control No. 13/105,696	Applicant(s)/Patent Under Reexamination VINCIARELLI ET AL.	
	Examiner CARL ARBES	Art Unit 3729	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-4,366,342	12-1982	Breedlove, James G.	174/557
*	B	US-4,551,747	11-1985	Gilbert et al.	257/691
*	C	US-5,241,133	08-1993	Mullen et al.	174/534
*	D	US-5,864,092	01-1999	Gore et al.	174/51
*	E	US-6,830,959 B2	12-2004	Estacio, Maria Cristina B.	438/113
*	F	US-2010/0197150 A1	08-2010	Smejtek, Dalibor	439/61
*	G	US-7,972,143 B2	07-2011	Smejtek, Dalibor	439/61
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Substitute Form PTO-1449 (Modified) U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 00614-0168001	Application No. 13/105,696
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	Applicant Patrizio Vinciarelli et al.	
	Filing Date May 11, 2011	Group Art Unit

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1	5,728,600	03/17/1998	Saxelby, Jr. et al.	437	207	
	2	6,403,009	06/11/2002	Saxelby, Jr. et al.	264	272.15	
	3	6,940,013	09/06/2005	Vinciarelli et al.	174	52.1	
	4	7,361,844	04/22/2008	Vinciarelli et al.	174	260	
	5						
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	7						
	8						
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Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	12							
	13							
	14							
	15							
	16							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	17	U.S. Patent Application Serial No. 12/493,773, entitled "Encapsulation Method and Apparatus for Electronic Modules", Application and Preliminary Amendment filed June 29, 2009, 63 pages
	18	
	19	
	20	

Examiner Signature /Carl Arbes/	Date Considered 9/20/13

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form (PTO-1449)

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.A./

Substitute Disclosure Form / U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 00614-0168001	Application No. 13/105,696
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	Applicant: Patrizio Vinciarelli et al.	
	Filing Date: May 11, 2011	Group Art Unit: ~~2835~~

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1	2002/0096348	07/25/2002	Saxelby et al.			
	2	2004/0100778	05/27/2004	Vinciarelli et al.			
	3	2007/0241440	10/18/2007	Hoang et al.			
	4	2010/0246152	09/30/2010	Lin et al.			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	5	WO1995/027308	10/12/1995	WIPO				

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document 9/20/13
	6	International Search Report and Written Opinion, PCT/US2012/37495, May 6, 2013, 18 pages.

Examiner Signature	Date Considered
/Carl Arbes/	

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.A./

Substitute Form PTO-1449 (Modified) U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 00614-0168001	Application No. 13/105,696
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	Applicant Patrizio Vinciarelli et al.	
	Filing Date May 11, 2011	Group Art Unit

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
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Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	12							
	13							
	14							
	15							
	16							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	17	AFM Microelectronics Inc., "General Purpose Capacitors", www.afmmicroelectronics.com , 13 pages, published on or before July 26, 2010
	18	Kahn, "Technical Information: Multilayer Ceramic Capacitors – Materials and Manufacture", Microelectronics Inc., 9 pages, published on or before July 26, 2010
	19	
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Examiner Signature /Carl Arbes/	Date Considered 9/20/13

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form (PTO-1449)

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.A./

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/116,642	07/24/2014	Patrizio Vinciarelli	00614-0169US1	5649

26214 7590 02/09/2016
FISH & RICHARDSON P.C. (VLT, INC)
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
SHRESTHA, SAGAR	

ART UNIT	PAPER NUMBER
2835	

NOTIFICATION DATE	DELIVERY MODE
02/09/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No. 14/116,642	Applicant(s) VINCIARELLI ET AL.	
	Examiner SAGAR SHRESTHA	Art Unit 2835	AIA (First Inventor to File) Status No

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/19/2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *146-183* is/are pending in the application.

5a) Of the above claim(s) *146-158 and 162-181* is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *159-161 and 182* is/are rejected.

8)☒ Claim(s) *183* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *11/08/2013* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP §

717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/forms/. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

3. Claim 159, 160 and 161 are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claims 110, 118, 119 and 122 of copending Application No. 14/635,467 (reference application). Although the claims at issue are not identical, they are not patentably distinct from each other because the co-pending application teaches all the limitations

Regarding claim 159, claim 110 of co-pending application No. 14/635,467 discloses all the limitations recited in claim 159 of the instant application.

Regarding claim 160 and 161, claims 118, 119 and 122 of co-pending application No. 14/635,467 discloses all the limitations recited in claim 160 and 161 of the instant application.

This is a provisional nonstatutory double patenting rejection because the patentably indistinct claims have not in fact been patented.

Claim Rejections - 35 USC § 103

4. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 159, 160, 182 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Ozawa (US 5,471,366; Ozawa hereinafter) in view of Vinciarelli et al. (US 2004/0100778; Vinciarelli hereinafter).

Regarding claim 159, Ozawa (figs. 2-6) discloses an apparatus comprising:

a modular package (34, fig. 3) having a first external surface (top external surface of 34), a second external surface (bottom external surface of 34) opposite the first external surface, and a side wall (side wall of 34) extending along the perimeter of and connecting with the first and second external surfaces, the first and second external surfaces each being defined at least in part by a respective layer of cured mold compound (Figs. 2. 3); and

an electrical circuit, including a printed circuit board ("PCB") (31, figs, 2-5), a plurality of components including semiconductors (32_{-1} - 32_{-4}, figs. 2, 3, Col. 4: lines 45-54) mounted to the PCB and a plurality of interconnects electrically connected to the components, the electrical circuit being located within the cured mold compound (figs. 2, 3, col. 4: lines 45-64 and col.5: lines 6-23);

the side wall comprising a strip formed by the PCB between strips formed by the layers of cured mold compound defining the first and second external surfaces (the side wall comprises of PCB strips in between strips formed by the first external surface and second external surface, Figs. 2, 3) ;

the interconnects being disposed within the side wall (figs. 2, 3, col. 4: lines 45-64 and col.5: lines 6-23).

Ozawa does not explicitly disclose that an electrical circuit for power converting.

Vinciarelli teaches an electrical circuit for converting power (Par. [0014]).

It would have been obvious to one of ordinary skill in the art before the invention was filed to include the power converting circuit of Vinciarelli into the circuit of the apparatus of Ozawa in order to increase the usage of the apparatus. The modified apparatus could also be used as a power converter.

Regarding claim 160, Ozawa discloses the apparatus as set forth in claim 159.

Ozawa does not explicitly disclose the electrical circuit further comprises a magnetic core, and at least one of the first and second external surfaces is also defined by a surface of the magnetic core.

Vinciarelli (fig. 5B) teaches the electrical circuit further comprises a magnetic core, and the first external surface is defined by a surface of the magnetic core (fig. 5B, Par. [0052]).

It would have been obvious to one of ordinary skill in the art before the invention was filed to include the magnetic core of power converting circuit of Vinciarelli into the circuit of the apparatus of Ozawa in order to increase the usage of the apparatus. The modified apparatus could also be used as a power converter.

Regarding claim 182, Ozawa (figs. 2-5) discloses the apparatus of claim 159, comprising a portion of a mold panel, in which a surface of the portion of the mold panel forms at least a portion of the first external surface (figs. 2-5, Col. 5: lines 6-23 and Col.6: lines 63-67).

6. Claim 161 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Ozawa and Vinciarelli as applied to claim 160, and in further view of Brancaleone (US 4,326,765; Brancaleone hereinafter).

Regarding claim 161, the modified apparatus of Ozawa discloses the apparatus as set forth in claim 160.

The modified apparatus of Ozawa does not disclose the apparatus of claim 160 further comprising: an adapter for providing mechanical and electrical connections between the modular package and an external mounting substrate, the adapter having a body and a plurality of electrical terminals; and electrical connections formed between the adapter terminals and respective interconnects on the modular package, the

adapter body being mechanically secured to the modular package and covering the electrical connections; the adapter terminals being arranged to mate with the external mounting substrate.

Brancaleone (figs. 1, 2) teaches a modular package comprises an adapter (16) for providing mechanical and electrical connections between the modular package and an external mounting substrate (12), the adapter having a body (fig. 1) and a plurality of electrical terminals (30); and electrical connections formed between the adapter terminals and respective interconnects on the modular package (figs. 1, 2), the adapter body being mechanically secured to the modular package and covering the electrical connections; the adapter terminals being arranged to mate with the external mounting substrate (figs. 1, 2).

It would have been obvious to one of ordinary skill in the art before the claimed invention was filed to incorporate the adapter of Brancaleone onto the modified apparatus of Ozawa in order to make the connecting and disconnecting mechanism of the apparatus on the external circuit easier and convenient, and provide easy replacement of the apparatus in the external circuit as suggested by Brancaleone (Col. 4: lines 34-48).

7. Claims 159, 160 and 182 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Saxelby (US 2002/0096348; Saxelby hereinafter) in view of Vinciarelli et al. (US 2004/0100778; Vinciarelli hereinafter).

Regarding claim 159, Saxelby (figs 1-21) disclose an apparatus comprising:

a modular package (9, figs. 5a,5b) having a first external surface, a second external surface opposite the first external surface (modular package has top external surface and bottom external surface opposite to the first external surface, figs. 5a, 5b) , and a side wall extending along the perimeter of and connecting with the first and second external surfaces (modular package 9 has side wall around the perimeter of the modular package 9), the first and second external surfaces each being defined at least in part by a respective layer of cured mold compound (figs. 2a-5b, par. [0040]); and

an electrical circuit, including a printed circuit board ("PCB") (20, figs. 2a-5b), a plurality of components (12, 14, 15, 17, 18) including semiconductors mounted to the PCB (20) and a plurality of interconnects electrically connected to the components (figs. 4-6a, par. [0040] ~ [0041]), the electrical circuit being located within the cured mold compound (figs. 4-6a, par. [0040] ~ [004]);

the side wall comprising a strip formed by the PCB between strips formed by the layers of cured mold compound defining the first and second external surfaces (the sidewall comprises PCB strips formed between the strips formed by the first and the second external surfaces, fig. 5a, 5b, Par. [0040]);

the interconnects being disposed within the side wall (fig. 5a, 5b, Par. [0040]).

Saxelby does not explicitly disclose that an electrical circuit for power converting.

Vinciarelli teaches an electrical circuit for converting power (Par. [0014]).

It would have been obvious to one of ordinary skill in the art before the invention was filed to include the power converting circuit of Vinciarelli into the circuit of the

apparatus of Saxelby in order to increase the usage of the apparatus. The modified apparatus could also be used as a power converter.

Regarding claim 160, Saxelby discloses the apparatus as set forth in claim 159.

Saxelby does not explicitly disclose the electrical circuit further comprises a magnetic core, and at least one of the first and second external surfaces is also defined by a surface of the magnetic core.

Vinciarelli (fig. 5B) teaches the electrical circuit further comprises a magnetic core, and the first external surface is defined by a surface of the magnetic core (fig. 5B, Par. [0052]).

It would have been obvious to one of ordinary skill in the art before the invention was filed to include the magnetic core of power converting circuit of Vinciarelli into the circuit of the apparatus of Saxelby in order to increase the usage of the apparatus. The modified apparatus could also be used as a power converter.

Regarding claim 182, Saxelby (figs. 2a-5b) disclose that the apparatus of claim 159, comprising a portion of a mold panel (figs. 2a-5b), in which a surface of the portion of the mold panel forms at least a portion of the first external surface (the portion of the mold panel above the circuit board 20 formed a portion of the first external surface, figs. 2a-5b).

8. Claim 161 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Saxelby and Vinciarelli as applied to claim 160, and in further view of Brancaleone (US 4,326,765; Brancaleone hereinafter).

Regarding claim 161, the modified apparatus of Saxelby discloses the apparatus as set forth in claim 160.

The modified apparatus of Saxelby does not disclose the apparatus of claim 160 further comprising: an adapter for providing mechanical and electrical connections between the modular package and an external mounting substrate, the adapter having a body and a plurality of electrical terminals; and electrical connections formed between the adapter terminals and respective interconnects on the modular package, the adapter body being mechanically secured to the modular package and covering the electrical connections; the adapter terminals being arranged to mate with the external mounting substrate.

Brancaleone (figs. 1, 2) teaches a modular package comprises an adapter (16) for providing mechanical and electrical connections between the modular package and an external mounting substrate (12), the adapter having a body (fig. 1) and a plurality of electrical terminals (30); and electrical connections formed between the adapter terminals and respective interconnects on the modular package (figs. 1, 2), the adapter body being mechanically secured to the modular package and covering the electrical connections; the adapter terminals being arranged to mate with the external mounting substrate (figs. 1, 2).

It would have been obvious to one of ordinary skill in the art before the claimed invention was filed to incorporate the adapter of Brancaleone onto the modified apparatus of Saxelby in order to make the connecting and disconnecting mechanism of the apparatus on the external circuit easier and convenient, and provide easy

replacement of the apparatus in the external circuit as suggested by Brancaleone (Col. 4: lines 34-48).

Allowable Subject Matter

9. Claim 183 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding dependent claim 183, the prior art of record, taken alone or in combination, fails to teach or fairly suggest, in combining with other limitations recited within the claim and in the independent claim 159, a combination of limitations that a first set of the power semiconductor devices being mounted on the top surface and electrically connected to dissipate power at a level, Pt, during operation of the converter, a second set of the power semiconductor devices being mounted on the bottom surface and electrically connected to dissipate power at a level, Pb, during operation of the converter, wherein the power semiconductor devices are distributed between the first and second sets to distribute heat generation during operation of the converter such that each level Pt, Pb is less than 150% of the other level Pb, Pt. None of the reference art of record discloses or renders obvious such a combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure are listed in the form 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SAGAR SHRESTHA whose telephone number is (571)270-1236. The examiner can normally be reached on mon-fri: 9:00am to 5:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jinhee Lee can be reached on 5712721977. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. S/
Examiner, Art Unit 2835

/HOA C NGUYEN/
Primary Examiner, Art Unit 2847

Notice of References Cited	Application/Control No. 14/116,642	Applicant(s)/Patent Under Reexamination VINCIARELLI ET AL.	
	Examiner SAGAR SHRESTHA	Art Unit 2835	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-5,471,366 A	11-1995	Ozawa; Takashi	H01L23/3677	174/521
*	B	US-2006/0097831 A1	05-2006	Lotfi; Ashraf W.	H01F27/027	336/84C
*	C	US-2003/0011054 A1	01-2003	Jeun, Gi-young	H01L21/565	257/678
*	D	US-6,184,585 B1	02-2001	Martinez; Roberto	H01L23/49575	257/666
*	E	US-7,554,181 B2	06-2009	Satou; Yukihiro	H01L23/49575	257/676
*	F	US-2010/0259909 A1	10-2010	Ho; Dominique	H01F19/08	361/767
*	G	US-4,326,765 A	04-1982	Brancaleone; Salvatore T.	H05K7/1092	439/225
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
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	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Substitute Disclosure Form / U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No.	Application No.
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	00614-0169US1	14/116,642
	Applicant: Patrizio Vinciarelli et al.	
	Filing Date: July 24, 2014	Group Art Unit: 2835

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
/S.S./	1.	5,557,142	09/1996	Gilmore			
/S.S./	2.	6,734,552	05/2004	Combs			
/S.S./	3.	7,015,587	03/2006	Poddar			
/S.S./	4.	7,049,682	05/2006	Mathews			
/S.S./	5.	7,198,987	04/2007	Warren			
/S.S./	6.	8,138,584	03/2012	Wang			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	7.							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	8.	

Examiner Signature	Date Considered
/Sagar Shrestha/	02/02/2016

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

Substitute Disclosure Form	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 00614-0169US1	Application No. 14/116,642
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		First Named Inventor Patrizio Vinciarelli	
		Filing Date November 8, 2013	Group Art Unit

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
/S.S./	1	2010/0197150	08/2010	Smejtek			
/S.S./	2	2012/0287582	11/15/2012	Vinciarelli et al.			
/S.S./	3	4,366,342	12/1982	Breedlove			
/S.S./	4	4,551,747	11/1985	Gilbert et al.			
/S.S./	5	5,241,133	08/1993	Mullen et al.			
/S.S./	6	5,728,600	03/17/1998	Saxelby, Jr. et al.			
/S.S./	7	5,864,092	01/1999	Gore et al.			
/S.S./	8	6,403,009	06/11/2002	Saxelby, Jr. et al.			
/S.S./	9	6,830,959	12/2004	Estacio			
/S.S./	10	6,940,013	09/06/2005	Vinciarelli et al.			
/S.S./	11	7,361,844	04/22/2008	Vinciarelli et al.			
/S.S./	12	7,972,143	07/2011	Smejtek			
/S.S./	13	8,427,269	04/23/2013	Vinciarelli			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	14							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
/S.S./	15	AFM Microelectronics Inc., "General Purpose Capacitors", www.afmmicroelectronics.com , 13 pages, published on or before July 26, 2010.
/S.S./	16	Kahn, "Technical Information: Multilayer Ceramic Capacitors – Materials and Manufacture", Microelectronics Inc., 9 pages, published on or before July 26, 2010.

Examiner Signature	Date Considered
/Sagar Shrestha/	/Sagar Shrestha/

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Patrizio Vinciarelli et al.	Art Unit	: Unknown
Serial No.	: Not yet assigned	Examiner	: Unknown
Filed	: Herewith		
Title	: PANEL-MOLDED ELECTRONIC ASSEMBLIES		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Please consider the references listed on the enclosed PTO-SB-08 or Disclosure Form. A foreign patent document is enclosed; cited U.S. patent application publications will be provided on request.

This statement is being filed with the application. Please apply any necessary charges or credits to deposit account 06-1050, referencing the above attorney docket number.

Respectfully submitted,

Date: November 8, 2013_____ /Rex I. Huang/_____
Rex I. Huang
Reg. No. 57,661

Customer Number 26214
Fish & Richardson P.C.
Telephone: (617) 542-5070
Facsimile: (877) 769-7945

23118549.doc

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

Substitute Disclosure Form / U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No.	Application No.
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	00614-0169US1	Not yet assigned
	Applicant: Patrizio Vinciarelli et al.	
	Filing Date: Herewith	Group Art Unit: Unknown

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
/S.S./	1	2002/0096348	07/2002	Saxelby, Jr. et al.			
/S.S./	2	2004/0100778	05/2004	Vinciarelli et al.			
/S.S./	3	2010/0246152	09/2010	Lin et al.			
/S.S./	4	2007/0241440	10/2007	Hoang et al.			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
/S.S./	5	1995/027308	10/1995	WIPO				

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
/S.S./	6	International search report and written opinion mailed May 6, 2013 in international application no. PCT/US12/37495, 24 pgs.

Examiner Signature	Date Considered
/Sagar Shrestha/	02/03/2016

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.S./

Substitute Disclosure Form / U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No.	Application No.
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	00614-0169US1	14/116,642
	Applicant: Patrizio Vinciarelli et al.	
	Filing Date: July 24, 2014	Group Art Unit

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
/S.S./	1.	7,030,469	4/18/2006	Mahadevan et al.			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	2.							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	3.	

Examiner Signature	Date Considered
/Sagar Shrestha/	02/02/2016

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/635,420	03/02/2015	Patrizio Vinciarelli	00614-0168002	6226

26214 7590 10/22/2015
FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
ARBES, CARL J	

ART UNIT	PAPER NUMBER
3729	

NOTIFICATION DATE	DELIVERY MODE
10/22/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No. 14/635,420	Applicant(s) VINCIARELLI ET AL.	
	Examiner CARL ARBES	Art Unit 3729	AIA (First Inventor to File) Status No

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-33* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-33* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *02 March 2015* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *herein*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-33 are further rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention. .To the extent that Applicant 's recitation of the language ...providing a plurality of mold panels which when assembled, form an internal chamber,.... (Cf. Claim 1) is not understood, the Claims are held to unclear, vague and indefinite. What is a plurality of mold panels? What is a "panel assembly""? What is a "panel"? What is an internal chamber?

Claims 1 and 5-12, assuming that these Claims are based on and enabling disclosure and are furthermore clear and definite, are further rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Mahadevan et al. (Pat. No. 7,030,469 B2); hereinafter Mahadevan et al.

Mahadevan et al teach a method of forming a semiconductor package by forming a conductive layer (42, 64) over a mold encapsulant (35, 62). Semiconductor package (2, 50) includes a semiconductor electrically connected to a lead frame (10,52).by wire-bonding two device portions (2, 4, 6, 8) of lead frame (10) together and cutting wire-bond (32) by forming groove (40). In overlying encapsulant (35) to form two wires (33). Conductive layer (42) is electrically coupled to each of the two

wires (33). (Cf. Abstract). Additionally Mahadevan et al teach that each ground pad of a device is electrically coupled to a ground pad of an adjacent device to form grounded electrical connections or ground wire bonds (32). By aligning the ground wire bonds in the direction that a mold encapsulant will flow during a subsequent molding process the ground wire bonds (32) tend to keep their shapes and not collapse.(Cf. Col. 4). Additionally Mahadevan et al teach a plurality of lags (12-15), a plurality of conductive traces (16, 18, 20 & 22) and a plurality of components (24, 25, 26 and 27) that are electrically connected to form a circuit.(Cf. Col. 3). Additionally Mahadevan et al teach that wire bonding or electrically coupling the semiconductor dies, flags/panels and ground pads the devices are encapsulated. Within a perimeter (34). (Cf. Col. 4). Additionally Mahadevan et al teach that the encasulant can be a solid that is heated to form a liquid and then cooled to form a solid. The encapsulant (35) must enclose at least the grounded wire bond (32) and associated wire device portions (2, 8) since the grounded wire bonds (32) are severed being encapsulated. Additionally Mahadevan et al teach forming a "V" groove that does not extend through the entire lead-frame (10) .(Cf Col. 5). Additionally Mahadevan et al teach cutting (or sawing) device portions with each device portion has a semiconductor die and one ground wire on each side of the semiconductor die. (Cf. Col. 6). Additionally Mahadevan et al teach providing a grounded wire (61) that is electrically coupled to a grounding plane and forms a loop. Second semiconductor (57) is placed of spacer (55) which is placed on semiconductor (54).Semiconductor die (57) is electrically coupled by second wire bond (59). The two semiconductors and wire bonds are encapsulated with the same encasulant that was used for the embodiments showing no stacking of semiconductors (Cf. Col. 8). It would have been obvious to provide a plurality of mold panels, which when assembled would have formed an internal chamber inasmuch as Mahadevan et al teach that the prior art is aware of individually molded packages such as quad-flat-no-lead) components. (Cf. Col 9). As applied to Claims 5 and 6 inasmuch as Mahadevan et al teach cutting (or sawing) portions with each device portion having a semiconductor die the limitation recited in said Claims 5 and 6 are held to have been obvious. As applied to Claims 7-12 a PHOSITA with the used of ordinary skill in this art would treat the exposed contact with a removable conformable coating e.g. a solder or a precious plated metal coating in

order to prevent oxidation and hence the limitation recited in said Claims 7-12 would have been obvious in view of Mahadevan et al teaching.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CARL ARBES whose telephone number is (571)272-4563. The examiner can normally be reached on M, T, R and F from 8 to 6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, P Vo, can be reached on (571) 272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://portal.uspto.gov/external/portal. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/CARL ARBES/

Primary Examiner, Art Unit 3729

Notice of References Cited	Application/Control No. 14/635,420	Applicant(s)/Patent Under Reexamination VINCIARELLI ET AL.	
	Examiner CARL ARBES	Art Unit 3729	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-5,557,142 A	09-1996	Gilmore; Peter B.	H01L23/552	174/521
*	B	US-6,734,552 B2	05-2004	Combs; Edward G.	H01L23/4334	257/707
*	C	US-7,015,587 B1	03-2006	Poddar; Anindya	H01L25/0657	257/666
*	D	US-7,030,469 B2	04-2006	Mahadevan; Dave S.	H01L21/561	257/659
*	E	US-7,049,682 B1	05-2006	Mathews; Douglas Jay	H01L23/552	257/659
*	F	US-7,198,987 B1	04-2007	Warren; Robert W.	H01L23/552	257/E23.114
*	G	US-8,138,584 B2	03-2012	Wang; Zhi-jie	H01L21/561	257/659
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Substitute Disclosure Form / U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 00614-0168002	Application No
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	Applicant VLT, Inc.	
	Filing Date	Group Art Unit

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1	2002/0096348	07/25/2002	Saxelby et al.			
	2	2004/0100778	05/27/2004	Vinciarelli et al.			
	3	2007/0241440	10/18/2007	Hoang et al.			
	4	2010/0197150	08/2010	Smejtek			
	5	2010/0246152	09/30/2010	Lin et al.			
	6	2012/0287582	11/15/2012	Vinciarelli et al.			
	7	4,366,342	12/1982	Breedlove			
	8	4,551,747	11/1985	Gilbert et al.			
	9	5,241,133	08/1993	Mullen et al.			
	10	5,728,600	03/17/1998	Saxelby, Jr. et al.			
	11	5,864,092	01/1999	Gore et al.			
	12	6,403,009	06/11/2002	Saxelby, Jr. et al.			
	13	6,830,959	12/2004	Estacio			
	14	6,940,013	09/06/2005	Vinciarelli et al.			
	15	7,361,844	04/22/2008	Vinciarelli et al.			
	16	7,972,143	07/2011	Smejtek			
	17	8,427,269	04/23/2013	Vinciarelli			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	18	WO1995/027308	10/12/1995	WIPO				

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	19	AFM Microelectronics Inc., "General Purpose Capacitors", www.afmmicroelectronics.com , 13 pages, published on or before July 26, 2010
	20	International Search Report and Written Opinion, PCT/US2012/37495, May 6, 2013, 18 pages.
	21	Kahn, "Technical Information: Multilayer Ceramic Capacitors – Materials and Manufacture", Microelectronics Inc., 9 pages, published on or before July 26, 2010
	22	U.S. Patent Application Serial No. 12/493,773, entitled "Encapsulation Method and Apparatus for Electronic Modules", Application and Preliminary Amendment filed June 29, 2009, 63 pages (24499-0009001)

Examiner Signature /Carl Arbes/	Date Considered 10/13/15

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.A./

Electronic Acknowledgement Receipt

EFS ID:	25033128
Application Number:	14635467
International Application Number:	
Confirmation Number:	1058
Title of Invention:	PANEL-MOLDED ELECTRONIC ASSEMBLIES
First Named Inventor/Applicant Name:	Patrizio Vinciarelli
Customer Number:	26214
Filer:	Rex I. Huang/Rita Liston
Filer Authorized By:	Rex I. Huang
Attorney Docket Number:	00614-0168003
Receipt Date:	26-FEB-2016
Filing Date:	02-MAR-2015
Time Stamp:	13:33:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		00614_0168003_IDS_022616.pdf	173663 bf82ff298fbd7aa9a5f1329b0bcfeb2a708ad2f2	yes	2

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
2	Non Patent Literature	USPTO_Office_Action_13105696_092513.pdf	725621 831761d5223aa6f3036598868f2c6c01dd056884	no	11
Warnings:					
Information:					
3	Non Patent Literature	USPTO_Office_Action_14116642_020916.pdf	168209 498f8fdfe75162e0d6e85fecc91941 6add4c7c05e	no	20
Warnings:					
Information:					
4	Non Patent Literature	USPTO_Office_Action_14635420_102215.pdf	70936 1181fde06b36d668358de049b157a7b96e1bdc8b	no	7
Warnings:					
Information:					
		Total Files Size (in bytes):	1138429		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor	:	Patrizio Vinciarelli	Art Unit	:	3729
Serial No.	:	14/635,467	Examiner	:	Carl J. Arbes
Filed	:	March 2, 2015	Conf. No.	:	1058
Title	:	PANEL-MOLDED ELECTRONIC ASSEMBLIES			

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Please consider the references listed on the enclosed PTO-SB-08 or Disclosure Form. The Applicant believes that the Office has access to the Office actions cited in the disclosure form but would be glad to provide copies of the Office actions on request.

This statement is being filed before the receipt of a first action on the merits.

Apply any necessary charges or credits to deposit account 06-1050, referencing the above attorney docket number.

Please contact the undersigned if there are any questions regarding this Statement.

Respectfully submitted,

Date: February 26, 2016

/Rex I. Huang/
Rex I. Huang
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23494610.doc

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/635,467	03/02/2015	Patrizio Vinciarelli	00614-0168003	1058

26214 7590 03/11/2016
FISH & RICHARDSON P.C. (VLT, INC)
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
ARBES, CARL J	

ART UNIT	PAPER NUMBER
3729	

NOTIFICATION DATE	DELIVERY MODE
03/11/2016	ELECTRONIC

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Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No. 14/635,467	Applicant(s) VINCIARELLI ET AL.	
	Examiner CARL ARBES	Art Unit 3729	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *49-142* is/are pending in the application.

5a) Of the above claim(s) *49-135* is/are withdrawn from consideration.

6)☒ Claim(s) *136-142* is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *02 March 2015* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *herein*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

Applicants' Replay to the office's Restriction has been reviewed. The Restriction filed on 19 November 2015 is held to have been proper when made and continues to be proper. In view of this holding and further in view of Applicants' response thereto the Restriction is now **made Final**. Applicants therefore are required to cancel all non-elected claims or take other appropriate action.

An Office Action on the merits of Claims 136-142 follows.

This application is in condition for allowance except for the following formal matters:

In addition to the Restriction comments hereinabove. Applicants are requested to amend the Tile of this Application to e.g. –POWER CONVERTER INCLUDING A PRINTED CIRCUIT BOARD—or the like.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 25 USPQ 74, 453 O.G. 213, (Comm'r Pat. 1935).

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CARL ARBES whose telephone number is (571)272-4563. The examiner can normally be reached on M, T, R and F from 8 to 6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, P Vo, can be reached on (571) 272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://portal.uspto.gov/external/portal. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/CARL ARBES/

Primary Examiner, Art Unit 3729

Notice of References Cited	Application/Control No. 14/635,467	Applicant(s)/Patent Under Reexamination VINCIARELLI ET AL.	
	Examiner CARL ARBES	Art Unit 3729	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-5,990,776 A	11-1999	Jitaru; Ionel	H01F27/2804	336/200
*	B	US-6,903,938 B2	06-2005	Waffenschmidt; Eberhard	H05K1/165	336/200
*	C	US-7,701,051 B2	04-2010	Bayerer; Reinhold	H01L23/5385	257/700
*	D	US-7,994,888 B2	08-2011	Ikriannikov; Alexandr	H01F3/08	336/192
*	E	US-8,299,882 B2	10-2012	Ikriannikov; Alexandr	H01F17/06	336/192
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Substitute Disclosure Form / U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No.	Application No.
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	00614-0168003	14/635,467
	Applicant: VLT, Inc.	
	Filing Date: March 2, 2015	Group Art Unit

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1.	7,030,469	4/18/2006	Mahadevan et al.			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	2.							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	3.	

Examiner Signature	Date Considered
/Carl Arbes/	2/26/16

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.A./

Substitute Disclosure Form / U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 00614-0168003	Application No
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	Applicant VLT, Inc.	
	Filing Date	Group Art Unit

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1	2002/0096348	07/25/2002	Saxelby et al.			
	2	2004/0100778	05/27/2004	Vinciarelli et al.			
	3	2007/0241440	10/18/2007	Hoang et al.			
	4	2010/0197150	08/2010	Smejtek			
	5	2010/0246152	09/30/2010	Lin et al.			
	6	2012/0287582	11/15/2012	Vinciarelli et al.			
	7	4,366,342	12/1982	Breedlove			
	8	4,551,747	11/1985	Gilbert et al.			
	9	5,241,133	08/1993	Mullen et al.			
	10	5,728,600	03/17/1998	Saxelby, Jr. et al.			
	11	5,864,092	01/1999	Gore et al.			
	12	6,403,009	06/11/2002	Saxelby, Jr. et al.			
	13	6,830,959	12/2004	Estacio			
	14	6,940,013	09/06/2005	Vinciarelli et al.			
	15	7,361,844	04/22/2008	Vinciarelli et al.			
	16	7,972,143	07/2011	Smejtek			
	17	8,427,269	04/23/2013	Vinciarelli			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	18	WO1995/027308	10/12/1995	WIPO				

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	19	AFM Microelectronics Inc., "General Purpose Capacitors", www.afmmicroelectronics.com , 13 pages, published on or before July 26, 2010
	20	International Search Report and Written Opinion, PCT/US2012/37495, May 6, 2013, 18 pages.
	21	Kahn, "Technical Information: Multilayer Ceramic Capacitors – Materials and Manufacture", Microelectronics Inc., 9 pages, published on or before July 26, 2010
	22	U.S. Patent Application Serial No. 12/493,773, entitled "Encapsulation Method and Apparatus for Electronic Modules", Application and Preliminary Amendment filed June 29, 2009, 63 pages (24499-0009001)

Examiner Signature	/Carl Arbes/	Date Considered 2/26/16

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Substitute Disclosure Form

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14635467	VINCIARELLI ET AL.
	Examiner	Art Unit
	CARL ARBES	3729

CPC- SEARCHED		
Symbol	Date	Examiner
h05K 7/02	2/26/16	cja
H01F 5/003		cja
H01L 23/34		cja

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Substitute Disclosure Form / U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 00614-0168003	Application No. 14/635,467
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	Applicant VLT, Inc.	
	Filing Date March 2, 2015	Group Art Unit

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1.	5,557,142	09/1996	Gilmore			
	2.	6,734,552	05/2004	Combs			
	3.	7,015,587	03/2006	Poddar			
	4.	7,049,682	05/2006	Mathews			
	5.	7,198,987	04/2007	Warren			
	6.	8,138,584	03/2012	Wang			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	7.							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Signature /Carl Arbes/	Date Considered 2/26/16

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14635467	VINCIARELLI ET AL.
	Examiner	Art Unit
	CARL ARBES	3729

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/12/2015	03/04/2016							
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CLAIM		DATE								
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	71	÷	N							
	72	÷	N							

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CLAIM		DATE								
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CLAIM		DATE								
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	143	-	-							
	144	-	-							

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CLAIM		DATE								
Final	Original	11/12/2015	03/04/2016							
	145	-	-							

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L6	968	circuit adj3 board and magnetic and core and semiconductors	USPAT	OR	OFF	2016/03/06 13:57

3/6/2016 2:46:51 PM

Substitute Disclosure Form / U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No.	Application No.
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	00614-0168003	14/635,467
	Applicant: VLT, Inc.	
	Filing Date: March 2, 2015	Group Art Unit: 3729

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1.						
	2.						

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	3.							

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	4.	USPTO Office Action; U.S. Patent Application Serial No. 13/105,696; mailed 09/25/2013
	5.	USPTO Office Action; U.S. Patent Application Serial No. 14/116,642; mailed 02/09/2016
	6.	USPTO Office Action; U.S. Patent Application Serial No. 14/635,420; mailed 10/22/2015.

Examiner Signature	Date Considered
/Carl Arbes/	2/26/16

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	Applicant: VLT, Inc.	
	Filing Date: March 2, 2015	Group Art Unit: 3729

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1.	2003/0011054	01/16/2003	Jeun et al.			
	2.	2006/0097831	05/11/2006	Lotfi et al.			
	3.	2010/0259909	10/14/2010	Ho et al.			
	4.	4,326,765	04/27/1982	Brancaleone			
	5.	4,326,765	04/27/1982	Brancaleone			
	6.	6,184,585	02/06/2001	Martinez et al.			
	7.	7,554,181	06/30/2009	Satou et al.			
	8.						

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Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	9.							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1058

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/635,467	03/02/2015	029	3729	00614-0168003

APPLICANTS
VLT, Inc., Sunnyvale, CA;

INVENTORS
Patrizio Vinciarelli, Boston, MA;
Michael B. LaFleur, East Hampstead, NH;
Sean Timothy Fleming, Worcester, MA;
Rudolph F. Mutter, North Andover, MA;
Andrew T. D'Amico, Beverly Hills, CA;

**** CONTINUING DATA ***************************
This application is a DIV of 13/105,696 05/11/2011 PAT 8966747

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
03/16/2015

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /CARL J ARBES/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		MA	38	94	6

ADDRESS
FISH & RICHARDSON P.C. (VLT, INC)
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022
UNITED STATES

TITLE
PANEL-MOLDED ELECTRONIC ASSEMBLIES

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
8920	No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Substitute Disclosure Form / U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No.	Application No.
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Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1.	5,471,366	11/28/1995	Ozawa			
	2.						
	3.						
	4.						
	5.						
	6.						
	7.						
	8.						

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	9.							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	10.	

Examiner Signature	Date Considered
/Carl Arbes/	2/26/16

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.A./

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor	:	Patrizio Vinciarelli	Art Unit	:	3729
Serial No.	:	14/635,467	Examiner	:	Carl J. Arbes
Filed	:	March 2, 2015	Conf. No.	:	1058
Title	:	PANEL-MOLDED ELECTRONIC ASSEMBLIES			

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO ACTION OF MARCH 11, 2016

Please consider the following reply.

Amendments to the Specification:

Please replace the title beginning at page 1, line 1 with the following amended title:

~~PANEL-MOLDED ELECTRONIC ASSEMBLIES~~ ENCAPSULATED MODULAR POWER CONVERTER WITH SYMMETRIC HEAT DISTRIBUTION

List of claims (replacing prior versions).

1. – 48. (Canceled).

49. - 135. (Canceled)

136. (Previously Presented) An apparatus comprising:

a power converter including

a printed circuit board ("PCB") comprising a plurality of conductive layers and having a top surface and a bottom surface;

a magnetic core structure magnetically coupled to a winding formed by traces in one or more of the conductive layers in the PCB; and

a plurality of power semiconductor devices, a first set of the power semiconductor devices being mounted on the top surface and electrically connected to dissipate power at a level, Pt, during operation of the converter, a second set of the power semiconductor devices being mounted on the bottom surface and electrically connected to dissipate power at a level, Pb, during operation of the converter;

wherein the power semiconductor devices are distributed between the first and second sets to distribute heat generation during operation of the converter such that each level Pt, Pb is less than 150% of the other level Pb, Pt.

137. (Previously Presented) The apparatus of claim 136 wherein a plurality of the power semiconductor devices in the first set are each positioned in a location on the top surface substantially overlapping a location on the bottom surface occupied by a power semiconductor device in the second set.

138. (Previously Presented) The apparatus of claim 136 wherein the power semiconductor devices are electrically connected using a respective set of conductive vias in the

PCB, and a plurality of the power semiconductor devices in the first set share their respective sets of conductive vias with corresponding power semiconductor devices in the second set.

139. (Previously Presented) The apparatus of claim 137 wherein the power converter further comprises circuitry including a pair of cells having a common circuit topology and each including power semiconductor switches from each of the first and second sets; each cell having its respective components arranged in a pattern, wherein the pattern of components of one cell is substantially a mirror image of the pattern of components in the other cell.

140. (Previously Presented) The apparatus of claim 139 wherein a component from one of the cells is located on an opposite surface of a respective component from the other one of the cells.

141. (Previously Presented) The apparatus of claim 140 wherein the cells comprise input cells.

142. (Previously Presented) The apparatus of claim 138 wherein the power semiconductor devices comprise output switches.

REMARKS

Claims 136-142 are allowed,

Claims 49-135 have been canceled.

The title has been amended.

Apply any necessary charges or credits to Deposit Account 06-1050, referencing the above attorney docket number.

Respectfully submitted,

Date: May 5, 2016

/Rex I. Huang/
Rex I. Huang
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23501494.doc

Electronic Acknowledgement Receipt

EFS ID:	25702775
Application Number:	14635467
International Application Number:	
Confirmation Number:	1058
Title of Invention:	PANEL-MOLDED ELECTRONIC ASSEMBLIES
First Named Inventor/Applicant Name:	Patrizio Vinciarelli
Customer Number:	26214
Filer:	Rex I. Huang/Rita Liston
Filer Authorized By:	Rex I. Huang
Attorney Docket Number:	00614-0168003
Receipt Date:	06-MAY-2016
Filing Date:	02-MAR-2015
Time Stamp:	10:40:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		00614_0168003_Resp_Quayle.pdf	72099 d528b81075ee6e31a62aaf997c72cd451abda73d	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Response after Ex Parte Quayle Action	1	1
	Specification	2	2
	Claims	3	4
	Applicant Arguments/Remarks Made in an Amendment	5	5
Warnings:			
Information:			
	Total Files Size (in bytes):	72099	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/635,467	Filing Date 03/02/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	05/06/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 7	Minus	** 94	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***6	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/ANNETTE SMITH/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Substitute Disclosure Form	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 00614-0168003	Application No. 14/635,467
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant VLT, Inc.	
		Filing Date March 2, 2015	Group Art Unit 3729

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1.						

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	2.							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	3.	Reply to Action of September 25, 2013; U.S. Patent Application Serial No. 13/105,696; Examiner Arbes; mailed March 25, 2014
	4.	USPTO Notice of Allowance; U.S. Patent Application Serial No. 13/105,696; Examiner Arbes; mailed November 18, 2014
	5.	Reply to Action of October 15, 2015; U.S. Patent Application Serial No. 14/635,420; Examiner Arbes; mailed November 13, 2015
	6.	USPTO Notice of Allowance; U.S. Patent Application Serial No. 14/635,420; Examiner Arbes; mailed February 17, 2016
	7.	USPTO Supplemental Notice of Allowance; U.S. Patent Application Serial No. 14/635,420; Examiner Arbes; mailed April 27, 2016
	8.	

Examiner Signature	Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Patrizio Vinciarelli et al.	Art Unit	: 3729
Serial No.	: 13/105,696	Examiner	: Carl J. Arbes
Filed	: May 11, 2011	Conf. No.	: 3765
Title	: PANEL-MOLDED ELECTRONIC ASSEMBLIES		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO ACTION OF SEPTEMBER 25, 2013

Please consider the following reply.

List of claims (replacing prior versions).

1-33. (Cancelled)

34. (Currently Amended) A method of forming an electrical contact comprising:

assembling a panel ~~including a substrate~~ , the panel having a printed circuit board having planar surfaces and one or more electrical components mounted on one or more of the planar surfaces, the panel having one or more conductive features enclosed within the panel and unexposed to an exterior surface of the panel, the one or more conductive features being located along a cut line;

cutting the panel along the cut line exposing portions of the one or more conductive features for use as electrical connections to the printed circuit board ~~substrate~~; and

treating the portions of the one or more conductive features exposed from the cutting for preservation as electrical connections.

35. (Original) The method of claim 34 wherein the treating further comprises applying solder to the portions of the one or more conductive features exposed from the cutting.

36. (Original) The method of claim 34 wherein the treating further comprises applying a conformal coating to the portions of the one or more conductive features exposed from the cutting to protect against oxidation.

37. (Original) The method of claim 34 wherein the treating further comprises applying a metal layer to the portions of the one or more conductive features exposed from the cutting.

38. (Previously Presented) The method of claim 34 wherein the treating further comprises attaching a lead of an adapter to the portions of the one or more conductive features exposed from the cutting.

39. (Currently Amended) The method of claim 34 further comprising covering at least one surface of the printed circuit board ~~substrate~~ in an area including the cut line and the conductive features prior to cutting the printed circuit board ~~substrate~~.

40. (Currently Amended) The method of claim 39 wherein the covering comprises encapsulating the printed circuit board ~~substrate~~ with a molding compound; and further comprising:

providing a registration feature having a predetermined relationship to the printed circuit board ~~substrate~~, and

using the registration feature to align the cutting relative to the cut line.

41. (Currently Amended) The method of claim 34 further comprising establishing a pattern including at least one conductive layer in the ~~substrate~~ printed circuit board along the cut line to form the conductive features.

42. (Currently Amended) The method of claim 41 wherein the ~~substrate~~ printed circuit board comprises a multilayer printed circuit board and the establishing a pattern includes establishing a plurality of conductive layers along the cut line to form the conductive features.

43. (Currently Amended) The method of claim 34 further comprising establishing a pattern including at least one conductive via in the ~~substrate~~ printed circuit board along the cut line to form the conductive features.

44. (Original) The method of claim 43 wherein the conductive via is filled with a conductive material.

45. (Currently Amended) The method of claim 43 wherein the conductive via is buried in the printed circuit board ~~substrate~~.

46. (Currently Amended) The method of claim 43 wherein the conductive via is a through hole contacting the surfaces of the printed circuit board ~~substrate~~.

47. (Original) The method of claim 46 wherein the through hole is filled with a conductive material.

48. (Currently Amended) The method of claim 34 wherein the conductive features are covered at the surfaces of the printed circuit board ~~substrate~~ by an insulation layer.

Claims 49-145 (Cancelled)

146. (Previously Presented) The method of claim 38 wherein the attaching further comprises soldering.

147. (Previously Presented) The method of claim 34 further comprising providing an adapter having one or more electrical terminals and wherein the treating comprises attaching the one or more electrical terminals to the portions of the one or more conductive features exposed from the cutting.

148. (Currently Amended) The method of claim 34 wherein ~~the substrate comprises a printed circuit board having planar surfaces, and~~ the assembling further comprises encapsulating the planar surfaces of the printed circuit board.

149. (Previously Presented) The method of claim 148 wherein the assembling further comprises forming a plurality of circuits on the printed circuit board and the cutting further comprises separating the plurality of circuits from the panel.

150. (Previously Presented) The method of claim 149 wherein at least one of the conductive features is positioned along a cutline between two adjacent circuits of the plurality of circuits.

151. (Previously Presented) The method of claim 150 wherein the at least one conductive feature is electrically connected to each of the two adjacent circuits, the cutting leaves a respective portion of the at least one conductive feature exposed in each of the two adjacent circuits to form a respective electrical connection.

152. (Previously Presented) The method of claim 149 further comprising attaching an electrically conductive member to selected ones of the exposed portions.

153. (New) A method of forming an electrical contact comprising:

assembling a panel including a substrate having one or more conductive features enclosed within the panel and unexposed to an exterior surface of the panel, the one or more conductive features being located along a cut line;

cutting the panel along the cut line exposing portions of the one or more conductive features for use as electrical connections to the substrate; and

treating the portions of the one or more conductive features exposed from the cutting for preservation as electrical connections;

wherein the substrate comprises a printed circuit board having planar surfaces, and the assembling further comprises encapsulating the planar surfaces of the printed circuit board;

wherein the assembling further comprises forming a plurality of circuits on the printed circuit board and the cutting further comprises separating the plurality of circuits from the panel.

154. (New) The method of claim 153 wherein at least one of the conductive features is positioned along a cutline between two adjacent circuits of the plurality of circuits.

155. (New) The method of claim 154 wherein the at least one conductive feature is electrically connected to each of the two adjacent circuits, the cutting leaves a respective portion of the at least one conductive feature exposed in each of the two adjacent circuits to form a respective electrical connection.

156. (New) The method of claim 153 further comprising attaching an electrically conductive member to selected ones of the exposed portions.

Remarks

The Applicant acknowledges that claims 149-152 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. New claim 153 includes the features of claims 34, 148, and 149, and thus is allowable. New claims 154-156 have features that correspond to claims 150-152, respectively. The other claims are also patentable for at least the reasons set forth below.

The comments of the Applicant below are each preceded by related comments of the Examiner (in small, bold type).

Claim Rejections – 35 USC § 112

Claims 38, 39, 45 and 146 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention. To the extent that the language ... attaching a lead of an adapter. .. is not understood claim 38 is held to be unclear, vague and indefinite. Where is "an adapter" defined? What is its purpose or function? What does it adapt? With respect claim 39 what does the language ... covering at least one surface of the substrate in the area ... mean? Covering the surface with what? Is the surface covered with air? Is the surface covered with paint? If so what type? Claim 39 is held to be unclear, vague and indefinite. As applied to claim 45 it is not understood what Applicants intend when they recite ... the conductive via is buried in the substrate.... By definition a via a conductive or non-conductive hole or region that in located in a substrate. That substantially all conductive vias are "buried in substrates". What is it that Applicants intend by this language? Claim 45 is held to be unclear, vague and indefinite.

MPEP 2111 states that the Patent and Trademark Office determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." In re Am. Acad. of Sci. Tech. Ctr., 367 F.3d 1359, 1364[, 70 USPQ2d 1827] (Fed. Cir. 2004).

Claim 38 is supported by, for example, FIGS. 15-20 and paragraphs 86, 87, 89, and 92 of the specification. An example of an adapter is shown in FIG. 16 and described in paragraph 86. In this example, the adapter is a through-hole adapter 203A or 203B whose purpose is to allow

the exposed interconnects 211, 212 to be electrically connected to conductive terminals 208, 210 and 209, which are suitable for through hole mounting in a motherboard. An example of an adapter 308A or 308B that is suitable for surface-mount soldering to a motherboard is shown in FIG. 18. The meaning of the term "adapter" in claim 38 is clear and definite in light of the specification as it would be interpreted by one of ordinary skill in the art.

Claim 39 is supported by, for example, paragraph 3 of the specification, which provides an example in which the printed circuit board is covered by an encapsulant. The original claim 40 provides an example of encapsulating with a molding compound. The meaning of the phrase "covering at least one surface of the printed circuit board in an area" in claim 39 is clear and definite in light of the specification as it would be interpreted by one of ordinary skill in the art.

Claim 45 is supported by, for example, paragraph 80 of the specification, which states "the interconnection features may preferably be buried in the PCB panel 124 below the top and bottom surface layers." A buried via may become exposed when the printed circuit is cut. For example, as described in paragraph 82, "The buried vias may be located so that the singulation cut leaves the walls of the conductive vias exposed resulting in vertical conductive strips." The meaning of the phrase "the conductive via is buried in the printed circuit board" in claim 45 is clear and definite in light of the specification as it would be interpreted by one of ordinary skill in the art.

Claims 34-47,146 and 147 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gilbert et al (Pat No. 4,551,747); hereinafter Gilbert et al.

Claim 34 recites "assembling a panel, ... the panel having one or more conductive features enclosed within the panel and unexposed to an exterior surface of the panel" and "cutting the panel along the cut line exposing portions of the one or more conductive features" (emphasis added). These features are not disclosed and would not have been made obvious by Gilbert.

Without conceding that the reference discloses any features of the claims, Gilbert discloses "each of the layers of the carrier apparatus 40 includes a plurality of spaced, vertically extending semi-cylindrical indentations or castellations 60 along the edge thereof" and "[t]he

castellations 60 are metalized along a portion thereof so as to provide electrical pathways from the fourth layer to the signal traces of the second layer" (col. 8, lines 20-33). Gilbert does not disclose or suggest that the indentations or castellations 60 are generated by first forming metalized features that are enclosed within the layers and unexposed to an exterior surface, then cutting the layers to expose portions of the conductive features. Gilbert discloses a first dielectric layer 42 includes a metalized planar rectangular surface area 44 that is electroplated (col. 7, lines 22-25), and a second layer 46 that includes elongated spaced electroplated signal leads or traces 48 (col. 7, lines 32-33). Gilbert also discloses that the castellations are gold electroplated to prevent oxidation (col. 8, lines 36-38). Thus, a person of ordinary skill in the art may reasonably conclude that Gilbert's carrier apparatus can be generated by first forming the semi-cylindrical indentations or castellations, then electroplating the metal features. Therefore, Gilbert does not disclose or suggest assembling a panel having one or more conductive features enclosed within the panel and unexposed to an exterior surface of the panel, and cutting the panel to expose portions of the one or more conductive features, as recited in claim 1.

Claim 34 is patentable over Gilbert for at least the above reasons.

Claim Rejections – 35 USC § 103

Claims 34-39, 41 and 43-47 are further rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Estacio (Pat No. 6,830,959 B2); hereinafter Estacio.

Claim 34 recites "assembling a panel, the panel having a printed circuit board having planar surfaces and one or more electrical components mounted on one or more of the planar surfaces," "the panel having one or more conductive features enclosed within the panel and unexposed to an exterior surface of the panel," and "cutting the panel along the cut line exposing portions of the one or more conductive features."

Without conceding that the reference discloses any features of the claims, Estacio discloses a semiconductor die package with semiconductor die having side electrical connection (title). Estacio does not disclose or suggest a panel having a printed circuit board, let alone cutting the panel along the cut line exposing portions of one or more conductive features. The processing of a semiconductor die package is very different from the processing of a printed circuit board. It would not have been obvious to a person of ordinary skill in the art to apply the

technique taught by Estacio, which is suitable for processing a semiconductor die package, to processing a printed circuit board as recited in claim 34.

Claim 34 is patentable over Estacio for at least the above reasons.

Claims 48 and 148 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gilbert et al in view of Mullen, III et al (Pat. No. 5,241,133); hereinafter Mullen, III et al.

The features in claim 34 missing in Gilbert are also not disclosed or suggested by Mullen. Claim 34 is patentable over the combination of Gilbert and Mullen. Claims 48 and 148 are patentable over the combination of Gilbert and Mullen for at least the same reasons as those applied to claim 34.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Any circumstance in which the applicant has addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner. Any circumstance in which the applicant has made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims. Any circumstance in which the applicant has amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

The fee of $320 for the excess claims and the fee of $1400 for the extension of time are being paid with this reply on the electronic filing system. Apply those fees and any other necessary charges or credits to deposit account 06-1050, referencing the above attorney docket number.

Respectfully submitted,

Date: March 25, 2014

/Rex I. Huang/
Rex I. Huang
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UNITED STATES PATENT AND TRADEMARK OFFICE

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NOTICE OF ALLOWANCE AND FEE(S) DUE

26214 7590 11/18/2014
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MINNEAPOLIS, MN 55440-1022

EXAMINER	
ARBES, CARL J	
ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 11/18/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105,696	05/11/2011	Patrizio Vinciarelli	00614-0168001	3765

TITLE OF INVENTION: METHOD OF FORMING AN ELECTRICAL CONTACT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/18/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26214 7590 11/18/2014
FISH & RICHARDSON P.C.
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MINNEAPOLIS, MN 55440-1022

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105,696	05/11/2011	Patrizio Vinciarelli	00614-0168001	3765

TITLE OF INVENTION: METHOD OF FORMING AN ELECTRICAL CONTACT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/18/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
ARBES, CARL J	3729	029-832000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105,696	05/11/2011	Patrizio Vinciarelli	00614-0168001	3765

26214 7590 11/18/2014

FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
ARBES, CARL J	
ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 11/18/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/105,696	Applicant(s) VINCIARELLI ET AL.	
	Examiner CARL ARBES	Art Unit 3729	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *25 March 2014*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *34-48 and 146-156*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date herein
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/CARL ARBES/
Primary Examiner, Art Unit 3729

Examimer's Amendment

The Title of this application has been amended to –Method of Forming an Electrical Contact--.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CARL ARBES whose telephone number is (571)272-4563. The examiner can normally be reached on M, T, R and F from 8 to 6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, P Vo, can be reached on (571) 272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://portal.uspto.gov/external/portal. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/CARL ARBES/

Primary Examiner, Art Unit 3729

Substitute Disclosure Form / U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No.	Application No.
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	00614-0168001	13/105,696
	First Named Inventor: Patrizio Vinciarelli	
	Filing Date: May 11, 2011	Group Art Unit: 3729

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1	8,427,269	04/23/2013	Vinciarelli			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	2							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	3	

Examiner Signature	Date Considered
/Carl Arbes/	11/13/14

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.A./

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor	: Patrizio Vinciarelli	Art Unit	: 3729
Serial No.	: 14/635,420	Examiner	: Carl J. Arbes
Filed	: March 02, 2015	Conf. No.	: 6226
Title	: PANEL-MOLDED ELECTRONIC ASSEMBLIES		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO ACTION OF OCTOBER 15, 2015

Please consider the following reply.

Please amend the claims according to the following listing of claims, which replaces all prior versions of the claims:

1. (Original) A method of making a plurality of electronic devices, comprising:

providing a plurality of mold panels, which when assembled, form an internal chamber;

providing a substrate having a plurality of conductive traces and a plurality of components electrically connected to form at least one circuit, the substrate having at least one contact for making an electrical connection to the circuit;

forming a panel assembly including the mold panels assembled with the substrate in the internal chamber and an encapsulant filling spaces between the substrate and interior surfaces of the chamber;

curing the encapsulant; and

cutting the panel assembly to expose at least a portion of the at least one contact and form a respective exposed contact.

2. (Original) The method of claim 1 wherein the cutting comprises making a first cut in at least one of the mold panels, and in the first cut, making a second narrower cut through the panel assembly.

3. (Original) The method of claim 2 wherein the curing comprises raising the temperature of the panel assembly and the first cut is made before the panel assembly cools after the curing.

4. (Currently Amended) The method of claim 1 wherein the cutting divides the panel assembly producing at least one module having a plurality of layers including respective portions of each of the mold panels ~~panel molds~~, the substrate, and the encapsulant, and the module contains the at least one circuit.

5. (Original) The method of claim 4 wherein the cutting defines at least one side of the module.

6. (Original) The method of claim 4 wherein the cutting defines two or more sides of the module.

7. (Original) The method of claim 1 further comprising treating the exposed contact to protect against oxidation.

8. (Original) The method of claim 7 wherein the treating comprises applying a removable conformal coating to the exposed contact.

9. (Original) The method of claim 7 wherein the treating comprises applying a layer of metal to the exposed contact.

10. (Original) The method of claim 9 wherein the applying a layer of metal comprises applying solder.

11. (Original) The method of claim 9 wherein the applying a layer of metal comprises applying a precious metal.

12. (Original) The method of claim 9 wherein the applying a layer of metal comprises plating.

13. (Original) The method of claim 4 further comprising

providing an adapter having at least one electrical terminal; and

attaching the at least one electrical terminal to the exposed contact.

14. (Original) The method of claim 13 wherein

the at least one contact comprises a plurality of contacts;

the module comprises a plurality of exposed contacts;

the adapter has a plurality of electrical terminals arranged to match respective ones of the plurality of exposed contacts; and

the adapter is mechanically secured to the module.

15. (Original) The method of claim 4 wherein the mold panels are metal.

16. (Original) The method of claim 15 wherein the respective portions of the mold panels provide heat sink surfaces for the module.

17. (Original) The method of claim 1 wherein the providing mold panels further comprises providing contours in an internal surface of one or more of the mold panels.

18. (Original) The method of claim 17 wherein the providing contours further comprises matching depths of portions of the internal surface to heights of one or more selected components.

19. (Original) The method of claim 18 wherein the selected components include at least one magnetically permeable core and at least one semiconductor device.

20. (Original) The method of claim 4, wherein the traces and components are electrically connected to form a plurality of separable circuits arranged in a pattern on the substrate; and the cutting divides the panel assembly along spaces between the separable circuits into a plurality of modules each containing at least one respective circuit.

21. (Original) The method of claim 20 wherein the spaces between the separable circuits have dimensions approximately matching a width of cuts produced by equipment used to cut the panel assembly.

22. (Original) The method of claim 21 wherein the at least one contact comprises a plurality of contacts located in the spaces between the separable circuits.

23. (Original) The method of claim 22 wherein the plurality of contacts are formed in the substrate.

24. (Original) The method of claim 23 wherein the plurality of contacts are formed and buried below at least one surface of the substrate.

25. (Original) The method of claim 15 further comprising treating at least one exterior surface of at least one of the mold panels for solderability.

26. (Original) The method of claim 1 wherein forming the panel assembly comprises:
dispensing encapsulant into a bottom panel mold;
assembling the substrate into the bottom panel mold;
dispensing encapsulant onto a top of the substrate; and
assembling a top panel mold onto the substrate.

27. (Original) The method of claim 26 further comprising centrifuging the assembly before curing the encapsulant.

28. (Original) The method of claim 1 wherein forming the panel assembly comprises:
assembling the substrate with a first substrate surface facing into a first panel mold,
closing a second panel mold onto the substrate covering a second substrate surface,
providing one or more conduits to the internal chamber, and
forcing encapsulant through the one or more conduits into the chamber.

29. (Original) The method of claim 28 further comprising centrifuging the assembly before curing the encapsulant.

30. (Original) The method of claim 9 further comprising providing a connector for removably mating with and providing electrical connection to the metal.

31. (Original) The method of claim 1 further comprising:
providing a center plate having an opening to accommodate the substrate; and
wherein the forming a panel assembly includes positioning the substrate in the opening of the center plate and closing the mold panels against the center plate.

32. (Original) The method of claim 31 further comprising providing at least one opening in the center plate connected to the internal chamber by at least one conduit; and

forcing the encapsulant through the at least one opening and at least one conduit into the internal chamber.

33. (Original) The method of claim 32 wherein the forming a panel assembly further comprises securing the mold panels together prior to curing the encapsulant.

34. – 145. (Cancelled).

REMARKS

The Applicant thanks Examiner Carl Arbes for the telephone interview held on November 13, 2015. Claim 1, figures 3, 6, 9A, and 10A, paragraphs 79 and 81 of the specification, and the Mahadevan reference were discussed. An agreement was reached that claims 1-33 are definite and meet the requirements of 35 U.S.C. 112. No agreement was reached regarding the rejections under 35 U.S.C. 103(a).

The comments of the Applicant below are each preceded by related comments of the Examiner (in small, bold type).

Claim Rejections – 35 USC 112(b) or USC 112

Claims 1-33 are further rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

The meaning of the terms "mold panels," "panel assembly," "panel," and "internal chamber" are clear and definite.

For example, FIG. 3 of the specification shows a panel assembly 120. Paragraph 66 of the specification states "The PCB panel 124 containing the multiplicity of the electronic circuits (115A-115L in Fig. 5) may be assembled with matching heat sink panels 121, 122 as shown in Fig. 3 to form a panel assembly 120 (Fig. 2). As shown in Figs. 3 and 6, the two heat sink panels 121 and 122 when assembled together may form an internal cavity 146, which completely encloses the populated PCB panel 124. ... In this example, the heat sink panels 121 and 122 also function as mold panels by forming a mold cavity (e.g., the internal cavity 146)."

Thus, claims 1-33 meet the requirements under 35 U.S.C. 112.

Claim Rejections – 35 USC 103(a)

Claims 1 and 5-12, assuming that these Claims are based on and enabling disclosure and are furthermore clear and definite, are further rejected under U.S.C. 103(a) as being unpatentable over Mahadevan et al. (Pat. No. 7,030,469 B2); hereinafter Mahadevan et al.

Claim 1

Claim 1 recites "cutting the panel assembly to expose at least a portion of the at least one contact and form a respective exposed contact." The "panel assembly" in claim 1 includes the mold panels. Mahadevan does not disclose or suggest cutting a panel assembly that includes mold panels.

Mahadevan discloses an example in which a conductive layer 42 is deposited on the surface of a mold encapsulant 32, and then the conductive layer 42 and the mold encapsulant 32 are cut to singulate the device portions (FIG.8 and column 6, lines 18-46). Mahadevan discloses another example in which a mold encapsulant is formed over semiconductor dies, a conductive layer 64 is formed over the mold encapsulant, and the package is singulated after forming the conductive layer 64 (FIG. 10 and column 8, lines 10-29). In Mahadevan, a conductive layer 42 or 64 is formed over the encapsulant prior to singulation. This implies that the encapsulant is separated from the mold panels prior to singulation. In Mahadevan, there is no reason to cut the mold panels after the mold panels have been separated from the encapsulant. Rather, a person skilled in the art would understand that, after separating the mold panels from the encapsulant, the mold panels can be reused.

Therefore, "cutting the panel assembly to expose at least a portion of the at least one contact and form a respective exposed contact" as recited in claim 1 would not have been made obvious by Mahadevan.

Claim 1 is patentable over Mahadevan for at least the above reasons.

Claim 2

Claim 2 recites "the cutting comprises making a first cut in at least one of the mold panels, and in the first cut, making a second narrower cut through the panel assembly." As discussed above, Mahadevan does not disclose or suggest cutting any mold panel.

Claim 4

Claim 4 recites "the cutting divides the panel assembly producing at least one module having a plurality of layers including respective portions of each of the mold panels, the substrate, and the encapsulant."

Mahadevan discloses an example in which the cutting produces a singulated device that includes the semiconductor die 12 and the encapsulant 35 (FIG. 9 and column 6, lines 48-51), but the singulated device does not include a portion of a mold panel. Mahadevan discloses another example in which the cutting produces a singulated package that includes semiconductor dies 55 and 57 and the encapsulant 62 (FIG. 10 and column 8, lines 26-28), but the singulated package does not include a portion of a mold panel.

All dependent claims are patentable for at least the same reasons as the claims on which they depend are patentable.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Apply any necessary charges or credits to Deposit Account 06-1050, referencing the above attorney docket number.

Respectfully submitted,

Date: November 13, 2015

/Rex I. Huang/
Rex I. Huang
Reg. No. 57,661

Customer Number 26214
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Facsimile: (877) 769-7945

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NOTICE OF ALLOWANCE AND FEE(S) DUE

26214 7590 02/17/2016
FISH & RICHARDSON P.C. (VLT, INC)
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
ARBES, CARL J	
ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 02/17/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/635,420	03/02/2015	Patrizio Vinciarelli	00614-0168002	6226

TITLE OF INVENTION: METHOD OF MAKING A PLURALITY OF ELECTRONIC ASSEMBLIES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	05/17/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26214 7590 02/17/2016
FISH & RICHARDSON P.C. (VLT, INC)
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/635,420	03/02/2015	Patrizio Vinciarelli	00614-0168002	6226

TITLE OF INVENTION: METHOD OF MAKING A PLURALITY OF ELECTRONIC ASSEMBLIES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	05/17/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
ARBES, CARL J	3729	029-832000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
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NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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26214 7590 02/17/2016
FISH & RICHARDSON P.C. (VLT, INC)
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MINNEAPOLIS, MN 55440-1022

EXAMINER	
ARBES, CARL J	

ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 02/17/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/635,420	Applicant(s) VINCIARELLI ET AL.	
	Examiner CARL ARBES	Art Unit 3729	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *13 November 2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-33*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/CARL ARBES/
Primary Examiner, Art Unit 3729

The present application is being examined under the pre-AIA first to invent provisions.

Examiner's Amendment

The Title of this Application has been amended to—METHOD OF MAKING A PLURALITY OF ELECTRONIC ASSEMBLIES—

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CARL ARBES whose telephone number is (571)272-4563. The examiner can normally be reached on M, T, R and F from 8 to 6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, P Vo, can be reached on (571) 272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://portal.uspto.gov/external/portal. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/CARL ARBES/

Primary Examiner, Art Unit 3729

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

26214 7590 04/27/2016
FISH & RICHARDSON P.C. (VLT, INC)
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER
ARBES, CARL J

ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 04/27/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/635,420	03/02/2015	Patrizio Vinciarelli	00614-0168002	6226

TITLE OF INVENTION: METHOD OF MAKING A PLURALITY OF ELECTRONIC ASSEMBLIES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	07/27/2016

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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26214 7590 04/27/2016
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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/635,420	03/02/2015	Patrizio Vinciarelli	00614-0168002	6226

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EXAMINER	ART UNIT	CLASS-SUBCLASS
ARBES, CARL J	3729	029-832000

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3 _____

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Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ARBES, CARL J	

ART UNIT	PAPER NUMBER
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The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/635,420	Applicant(s) VINCIARELLI ET AL.	
	Examiner CARL ARBES	Art Unit 3729	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *26 February 2016*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-33*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   Certified copies:
   a) ☐ All b) ☐ Some *c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date here
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/CARL ARBES/
Primary Examiner, Art Unit 3729

The present application is being examined under the pre-AIA first to invent provisions.

Examiner's Reasons for an Allowance

COMES NOW the Patent Office, by an Examiner and states at least a reason for an Allowance of this Application, to wit: that the Prior Art neither anticipates nor in any reasonable combination, suggests a method of making a plurality of electronic devices including providing a plurality of mold panels which when assembled form an internal chamber, providing a substrate having a plurality of conductive traces and a plurality of components electrically connected to form at least one circuit, the substrate having at least one contact for making an electrical connection to the circuit, forming a panel assembly including the mold panels assembled with the substrate in the internal chamber and an encapsulant filling spaces between the substrate and the interior surfaces of the chamber, curing the encapsulant and cutting the panel assembly to expose at least a portion of the at least one contact and form a respective exposed contact.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CARL ARBES whose telephone number is (571)272-4563. The examiner can normally be reached on M, T, R and F from 8 to 6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, P Vo, can be reached on (571) 272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://portal.uspto.gov/external/portal. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/CARL ARBES/

Primary Examiner, Art Unit 3729

Substitute Disclosure Form	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 00614-0168002	Application No. 14/635,420
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant VLT, Inc.	
		Filing Date March 2, 2015	Group Art Unit 3729

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1.	2003/0011054	01/16/2003	Jeun et al.			
	2.	2006/0097831	05/11/2006	Lotfi et al.			
	3.	2010/0259909	10/14/2010	Ho et al.			
	4.	4,326,765	04/27/1982	Brancaleone			
	5.	4,326,765	04/27/1982	Brancaleone			
	6.	6,184,585	02/06/2001	Martinez et al.			
	7.	7,554,181	06/30/2009	Satou et al.			
	8.						

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	9.							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	10.	USPTO Office Action; U.S. Patent Application Serial No. 13/105,696; mailed 09/25/2013
	11.	USPTO Office Action; U.S. Patent Application Serial No. 14/116,642; mailed 02/09/2016

Examiner Signature	/Carl Arbes/	Date Considered	4/5/16

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.A./

Electronic Patent Application Fee Transmittal

Application Number:	14635467
Filing Date:	02-Mar-2015
Title of Invention:	ENCAPSULATED MODULAR POWER CONVERTER WITH SYMMETRIC HEAT DISTRIBUTION
First Named Inventor/Applicant Name:	Patrizio Vinciarelli
Filer:	Rex I. Huang/Rita Liston
Attorney Docket Number:	00614-0168003

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	25769457
Application Number:	14635467
International Application Number:	
Confirmation Number:	1058
Title of Invention:	ENCAPSULATED MODULAR POWER CONVERTER WITH SYMMETRIC HEAT DISTRIBUTION
First Named Inventor/Applicant Name:	Patrizio Vinciarelli
Customer Number:	26214
Filer:	Rex I. Huang/Rita Liston
Filer Authorized By:	Rex I. Huang
Attorney Docket Number:	00614-0168003
Receipt Date:	13-MAY-2016
Filing Date:	02-MAR-2015
Time Stamp:	10:52:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	8619
Deposit Account	061050
Authorized User	FISH & RICHARDSON P C
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

Charge any Additional Fees required under 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		00614_0168003_Trans_Draw.pdf	588552 53e475cb299fd1711a852c519c0166df74d13dd	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	1	
	Drawings-only black and white line drawings		2	2	
Warnings:					
Information:					
2		00614_0168003_IDS_051316.pdf	178491 89ed878dc01e91b68dd1b1bf918d311032ad0a85	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
3	Non Patent Literature	0168001_Resp_13105696_032514.pdf	126599 d80d0f60e3e3af3fcd326a61a6db55474f05e22c	no	10
Warnings:					
Information:					
4	Non Patent Literature	0168001_USPTO_Notice_of_Allowance_13105696_111814.pdf	568575 326a27d0aaf4bf78856425789566800ad6e09884c2	no	7
Warnings:					
Information:					
5	Non Patent Literature	00614_0168002_Reply_111315_.pdf	89794 df19deleb52d41d0de42a1954d18621d26c6385a	no	9
Warnings:					

Information:					
6	Non Patent Literature	0168002_USPTO_Notice_of_Allowance_14635420_021716.pdf	82432 d6a0a289rcaecb5fc28d04e5eb0746c613c1149	no	6
Warnings:					
Information:					
7	Non Patent Literature	0168002_Supp_USPTO_Notice_of_Allowance_14635420_042716.pdf	98123 4cdaaf503928c8c6fcb3cc46581614a109094558	no	7
Warnings:					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	30752 b1e52f51ee0f088dc91c50f65759cd2b77453da2	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1763318		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor	:	Patrizio Vinciarelli	Art Unit	:	3729
Serial No.	:	14/635,467	Examiner	:	Carl J. Arbes
Filed	:	March 2, 2015	Conf. No.	:	1058

Title : ENCAPSULATED MODULAR POWER CONVERTER WITH SYMMETRIC HEAT DISTRIBUTION

MAIL STOP PGPUB-DRAWINGS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF FORMAL DRAWINGS

Please substitute the enclosed one (1) sheet of formal drawing (FIG. 26) for the corresponding drawing presently in the application.

Apply any necessary charges or credits to Deposit Account 06-1050, referencing the above attorney docket number.

Respectfully submitted,

Date: May 13, 2016

/Rex I. Huang/
Rex I. Huang
Reg. No. 57,661

Customer Number 26214
Fish & Richardson P.C.
Telephone: (617) 542-5070
Facsimile: (877) 769-7945

23523542.doc

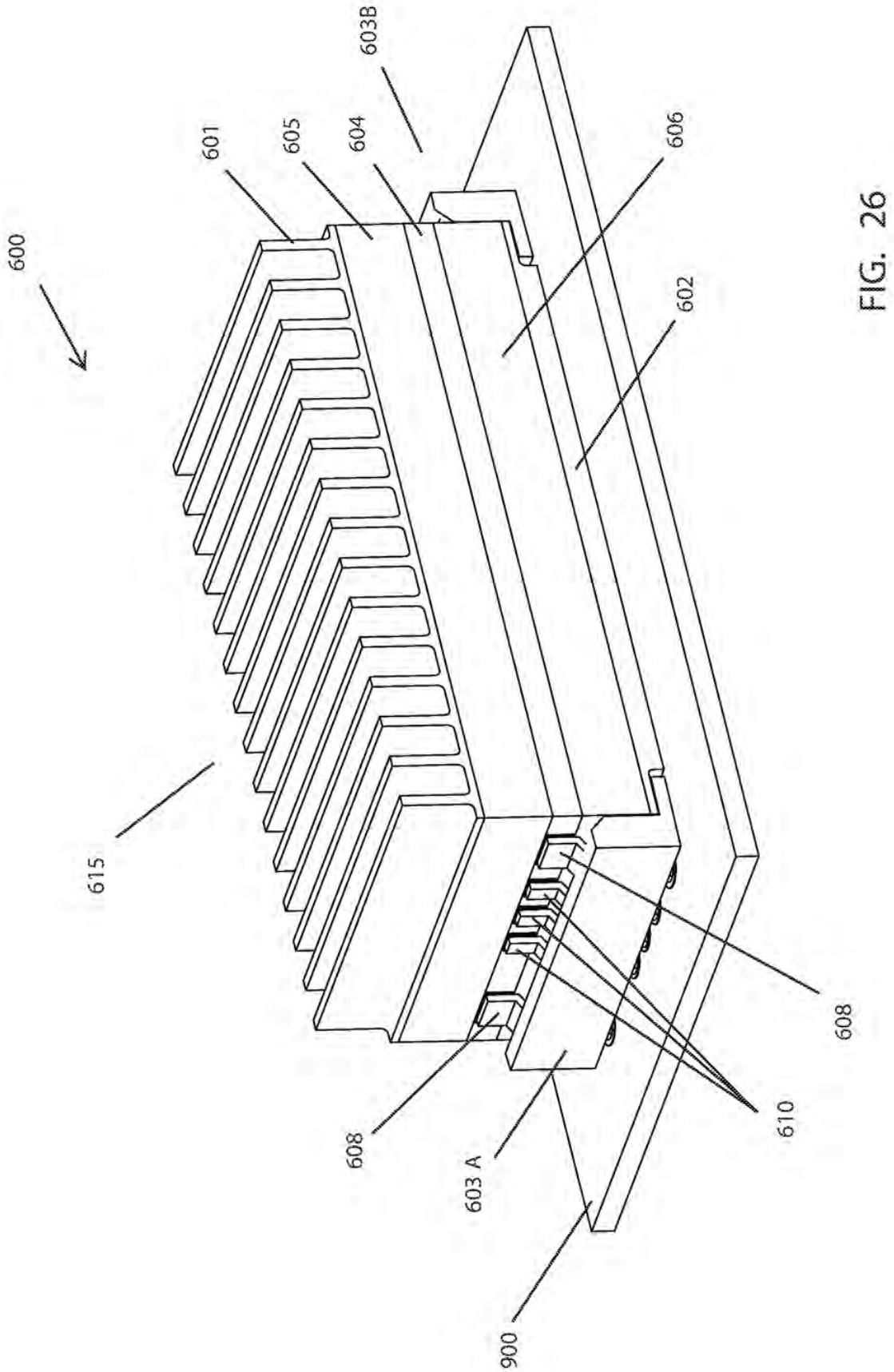


FIG. 26

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor :	Patrizio Vinciarelli	Art Unit :	3729
Serial No. :	14/635,467	Examiner :	Carl J. Arbes
Filed :	March 2, 2015	Conf. No. :	1058
Title :	ENCAPSULATED MODULAR POWER CONVERTER WITH SYMMETRIC HEAT DISTRIBUTION		

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Please consider the references listed on the enclosed PTO-SB-08 or Disclosure Form. Foreign patent documents and non-patent literature are enclosed; cited U.S. patents and patent application publications will be provided on request.

This statement is being filed after a first action on the merits, but before receipt of a final action or a notice of allowance. A late submission fee in the amount of $180, specified by 37 CFR §1.17(p), is being paid with this statement.

Apply any necessary charges or credits to deposit account 06-1050, referencing the above attorney docket number.

Please contact the undersigned if there are any questions regarding this Statement.

Respectfully submitted,

Date: May 13, 2016

/Rex I. Huang/
Rex I. Huang
Reg. No. 57,661

Customer Number 26214
Fish & Richardson P.C.
Telephone: (617) 542-5070
Facsimile: (877) 769-7945

23523532.doc

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

26214 7590 07/18/2016
FISH & RICHARDSON P.C. (VLT, INC)
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER
ARBES, CARL J

ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 07/18/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/635,467	03/02/2015	Patrizio Vinciarelli	00614-0168003	1058

TITLE OF INVENTION: ENCAPSULATED MODULAR POWER CONVERTER WITH SYMMETRIC HEAT DISTRIBUTION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/18/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26214 7590 07/18/2016
FISH & RICHARDSON P.C. (VLT, INC)
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/635,467	03/02/2015	Patrizio Vinciarelli	00614-0168003	1058

TITLE OF INVENTION: ENCAPSULATED MODULAR POWER CONVERTER WITH SYMMETRIC HEAT DISTRIBUTION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/18/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
ARBES, CARL J	3729	029-832000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29
- ❑ Applicant asserting small entity status. See 37 CFR 1.27
- ❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/635,467	03/02/2015	Patrizio Vinciarelli	00614-0168003	1058

26214 7590 07/18/2016
FISH & RICHARDSON P.C. (VLT, INC)
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
ARBES, CARL J	
ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 07/18/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/635,467	Applicant(s) VINCIARELLI ET AL.	
	Examiner CARL ARBES	Art Unit 3729	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *06 May 2016*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *136-142*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____.
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date herein
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/CARL ARBES/
Primary Examiner, Art Unit 3729

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1058

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/635,467	03/02/2015	029	3729	00614-0168003

APPLICANTS
VLT, Inc., Sunnyvale, CA;

INVENTORS
Patrizio Vinciarelli, Boston, MA;
Michael B. LaFleur, East Hampstead, NH;
Sean Timothy Fleming, Worcester, MA;
Rudolph F. Mutter, North Andover, MA;
Andrew T. D'Amico, Beverly Hills, CA;

**** CONTINUING DATA ***************************
This application is a DIV of 13/105,696 05/11/2011 PAT 8966747

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
03/16/2015

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /CARL J ARBES/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		MA	38	94	6

ADDRESS
FISH & RICHARDSON P.C. (VLT, INC)
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022
UNITED STATES

TITLE
ENCAPSULATED MODULAR POWER CONVERTER WITH SYMMETRIC HEAT DISTRIBUTION

FILING FEE RECEIVED		
8920	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Substitute Disclosure Form / U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No.	Application No.
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	00614-0168003	14/635,467
	Applicant: VLT, Inc.	
	Filing Date: March 2, 2015	Group Art Unit: 3729

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1.						

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	2.							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	3.	Reply to Action of September 25, 2013; U.S. Patent Application Serial No. 13/105,696; Examiner Arbes; mailed March 25, 2014
	4.	USPTO Notice of Allowance; U.S. Patent Application Serial No. 13/105,696; Examiner Arbes; mailed November 18, 2014
	5.	Reply to Action of October 15, 2015; U.S. Patent Application Serial No. 14/635,420; Examiner Arbes; mailed November 13, 2015
	6.	USPTO Notice of Allowance; U.S. Patent Application Serial No. 14/635,420; Examiner Arbes; mailed February 17, 2016
	7.	USPTO Supplemental Notice of Allowance; U.S. Patent Application Serial No. 14/635,420; Examiner Arbes; mailed April 27, 2016
	8.	

Examiner Signature	Date Considered
/Carl Arbes/	7/5/16

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.A./

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14635467	VINCIARELLI ET AL.
	Examiner	Art Unit
	CARL ARBES	3729

CPC							
Symbol						Type	Version
H05K		3	/	284		F	2013-01-01
Y10T		29	/	49117		A	2015-01-15
Y10T		29	/	49126		A	2015-01-15
Y10T		29	/	4913		A	2015-01-15
Y10T		29	/	49133		A	2015-01-15
Y10T		29	/	49144		A	2015-01-15
Y10T		29	/	49155		A	2015-01-15
H01R		43	/	24		I	2013-01-01
H05K		5	/	064		I	2013-01-01
B29C		45	/	14639		I	2013-01-01
B29C		45	/	0055		I	2013-01-01
B29C		2045	/	0058		A	2013-01-01
B29C		2793	/	0009		A	2013-01-01
B29C		2793	/	0027		A	2013-01-01
B29C		2793	/	009		A	2013-01-01
H05K		7	/	209		I	2013-01-01
B23P		15	/	007		I	2013-01-01
B29C		45	/	1679		I	2013-01-01
B29C		2045	/	169		A	2013-01-01
H01F		27	/	24		I	2013-01-01
H01F		27	/	2804		I	2013-01-01
H01F		2027	/	2809		A	2013-01-01
H05K		1	/	0298		I	2013-01-01
H05K		1	/	115		I	2013-01-01
H05K		1	/	181		I	2013-01-01
H05K		5	/	0004		I	2013-01-01
H05K		5	/	0065		I	2013-01-01
H05K		5	/	0217		I	2013-01-01
H05K		5	/	0247		I	2013-01-01
H05K		5	/	04		I	2013-01-01
H05K		7	/	1427		I	2013-01-01

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	7	
/CARL ARBES/ Primary Examiner.Art Unit 3729	7/5/16	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	7 & 7

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14635467	VINCIARELLI ET AL.
	Examiner	**Art Unit**
	CARL ARBES	3729

CPC Combination Sets					
Symbol			**Type**	**Set**	**Ranking**	**Version**
	/					
	/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	7	
/CARL ARBES/ Primary Examiner.Art Unit 3729	7/5/16	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	7 & 7

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14635467	VINCIARELLI ET AL.
	Examiner	Art Unit
	CARL ARBES	3729

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
		H 0 5 K 3/34 (2006.01.01)	

CROSS REFERENCE(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	7	
/CARL ARBES/ Primary Examiner.Art Unit 3729	7/5/16	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	7 & 7

U.S. Patent and Trademark Office — Part of Paper No. 13

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14635467	VINCIARELLI ET AL.
	Examiner	**Art Unit**
	CARL ARBES	3729

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		20		39		58		77		96		115		134
	2		21		40		59		78		97		116		135
	3		22		41		60		79		98		117	1	136
	4		23		42		61		80		99		118	2	137
	5		24		43		62		81		100		119	3	138
	6		25		44		63		82		101		120	4	139
	7		26		45		64		83		102		121	5	140
	8		27		46		65		84		103		122	6	141
	9		28		47		66		85		104		123	7	142
	10		29		48		67		86		105		124		
	11		30		49		68		87		106		125		
	12		31		50		69		88		107		126		
	13		32		51		70		89		108		127		
	14		33		52		71		90		109		128		
	15		34		53		72		91		110		129		
	16		35		54		73		92		111		130		
	17		36		55		74		93		112		131		
	18		37		56		75		94		113		132		
	19		38		57		76		95		114		133		

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	7	
/CARL ARBES/ Primary Examiner.Art Unit 3729	7/5/16	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	7 & 7

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14635467	VINCIARELLI ET AL.
	Examiner	Art Unit
	CARL ARBES	3729

CPC- SEARCHED		
Symbol	Date	Examiner
h05K 7/02	7/5/16	cja
H01F 5/003		cja
H01L 23/34		cja
B23P 15/007		cja
B29C 45/0055; 45/14639; 45/1679;		cja
B29C 2045/169; 2045/0058		cja
B29C 2793/0009; 2793/0027; 2793/009		cja
H01F/ 27/24; 27/2804		cja
H01F 2027/2809		cja
H01R 43/24		c ja
H05K 1/0298; 1/115; 1/181		cja
H05K 3/284		cja
H05K 5/0004; 5/0065; 5/0217; 5/0247; 5/04; 5/064		cja
H05K 7/1427; 7/209		cja
Y10T 29/49117; 29/49126; 29/4913; 29/49133; 29/49144		cja

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
B23P	15/007	7/5/16	cja
B29C	45/0055; 45/14639; 45/1679		cja
H01F	27/24; 27/2804		cja
H01R	43/24		cja
H05K	1/0298; 1/115; 1/181		cja
H05K	3/284		cja
H05K	5/0004; 5/0065; 5/0217; 5/0247; 5/04; 5/064		cja
H05K	7/1427; 7/209		cja

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26214 7590 07/18/2016

FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/635,467	03/02/2015	Patrizio Vinciarelli	00614-0168003	1058

TITLE OF INVENTION: ENCAPSULATED MODULAR POWER CONVERTER WITH SYMMETRIC HEAT DISTRIBUTION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	LARGE	$960	$0		$960	10/18/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
ARBES, CARL J.	3729	

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

[ ] Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

[ ] "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

1 Fish & Richardson P.C.

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE
VLT, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)
Sunnyvale, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): [ ] Individual [X] Corporation or other private group entity [ ] Government

4a. The following fee(s) are submitted:

[X] Issue Fee

[ ] Publication Fee (No small entity discount permitted)

[X] Advance Order - # of Copies 5

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

[ ] A check in the amount of the fee(s) is enclosed.

[ ] Payment by credit card. Form PTO-2038 is attached.

[X] The Director is hereby authorized to charge the required fee(s), or credit any overpayment, to Deposit Account Number 06-1050

5. **Change in Entity Status** (from status indicated above)

[ ] Applicant certifying micro entity status. See 37 CFR 1.29 — **NOTE**: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

[ ] Applicant asserting small entity status. See 37 CFR 1.27 — **NOTE**: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

[ ] Applicant changing to regular undiscounted fee status. — **NOTE**: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Rex I. Huang/ Date October 17, 2016

Typed or printed name Rex I. Huang Registration No. 57,661

23577623.doc

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor :	Patrizio Vinciarelli	Art Unit :	3729
Serial No. :	14/635,467	Examiner :	Carl J. Arbes
Filed :	March 2, 2015	Confirmation No. :	1058
		Notice of Allowance Date: 7/18/2016	
Title :	ENCAPSULATED MODULAR POWER CONVERTER WITH SYMMETRIC HEAT DISTRIBUTION		

MAIL STOP ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER ALLOWANCE
PURSUANT TO 37 C.F.R. §1.312

Please amend the application as indicated on the following pages. This amendment is being filed concurrently with the payment of the issue fee.

Amendments to the Specification:

Please replace paragraph [001] with the following amended paragraph:

~~CLAIM OF PRIORITY~~ CROSS-REFERENCE TO RELATED APPLICATIONS

[001] This application is a divisional of and claims priority under 35 USC 121 to U.S. Application Serial No. 13/105,696, filed on May 11, 2011, now issued as [[(]] U.S. Patent No. 8,966,747 ~~to be issued on March 3, 2015~~). This application is related to U.S. Patent Application Serial No. 14/635,420, filed on March 2, 2015, now issued as U.S. Patent No. 9,439,297. ~~titled "PANEL-MOLDED ELECTRONIC ASSEMBLIES," attorney docket 00614-0168002.~~ The entire contents of the above applications are herein incorporated by reference.

REMARKS

The "Cross-Reference to Related Applications" section has been amended.

Please apply any necessary charges or credits to Deposit Account 06-1050, referencing the above attorney docket number.

Respectfully submitted,

Date: October 17, 2016

/Rex I. Huang/
Rex I. Huang
Reg. No. 57,661

Customer Number 26214
Fish & Richardson P.C.
Telephone: (617) 542-5070
Facsimile: (877) 769-7945

23578020.doc

Electronic Patent Application Fee Transmittal

Application Number:	14635467
Filing Date:	02-Mar-2015
Title of Invention:	ENCAPSULATED MODULAR POWER CONVERTER WITH SYMMETRIC HEAT DISTRIBUTION
First Named Inventor/Applicant Name:	Patrizio Vinciarelli
Filer:	Rex I. Huang/Rita Liston
Attorney Docket Number:	00614-0168003

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	5	3	15
		Total in USD ($)		**975**

Electronic Acknowledgement Receipt

EFS ID:	27236524
Application Number:	14635467
International Application Number:	
Confirmation Number:	1058
Title of Invention:	ENCAPSULATED MODULAR POWER CONVERTER WITH SYMMETRIC HEAT DISTRIBUTION
First Named Inventor/Applicant Name:	Patrizio Vinciarelli
Customer Number:	26214
Filer:	Rex I. Huang/Elizabeth Doherty
Filer Authorized By:	Rex I. Huang
Attorney Docket Number:	00614-0168003
Receipt Date:	17-OCT-2016
Filing Date:	02-MAR-2015
Time Stamp:	17:22:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$975
RAM confirmation Number	101816INTEFSW00004822061050
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		00614_0168003_Resp_NOA.pdf	195516 5c6f4cddc52bd5ac2e71934e247d2eb3a72	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Post Allowance Communication - Incoming	1	1
	Issue Fee Payment (PTO-85B)	2	2

Warnings:

Information:

2		00614_0168003_Amendment.pdf	73346 562820cc6127807ff6e9582666662919224c	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment after Notice of Allowance (Rule 312)	1	1
	Specification	2	2
	Applicant Arguments/Remarks Made in an Amendment	3	3

Warnings:

Information:

3	Fee Worksheet (SB06)	fee-info.pdf	32327 d502e08f633a82f	no	2

Warnings:

Information:

Total Files Size (in bytes):	301189

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor :	Patrizio Vinciarelli	Art Unit :	3729
Serial No. :	14/635,467	Examiner :	Carl J. Arbes
Filed :	March 2, 2015	Confirmation No. :	1058
		Notice of Allowance Date: July 18, 2016	
Title :	ENCAPSULATED MODULAR POWER CONVERTER WITH SYMMETRIC HEAT DISTRIBUTION		

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REPLY TO NOTICE OF ALLOWANCE

In response to the Notice of Allowance dated July 18, 2016, enclosed is a completed Part B - Fee(s) Transmittal.

The issue fee, as well as the fee for 5 advanced copies of the patent, are being paid with this reply on the Electronic Filing System. Apply the fee and any other necessary charges or credits to Deposit Account 06 1050, referencing the above attorney docket number.

Respectfully submitted,

Date: October 17, 2016

/Rex I. Huang/
Rex I. Huang
Reg. No. 57,661

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Fish & Richardson P.C.
Telephone: (617) 542-5070
Facsimile: (877) 769-7945

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/CARL J ARBES/

Amendments to the Specification:

Please replace paragraph [001] with the following amended paragraph:

~~CLAIM OF PRIORITY~~ CROSS-REFERENCE TO RELATED APPLICATIONS

[001] This application is a divisional of and claims priority under 35 USC 121 to U.S. Application Serial No. 13/105,696, filed on May 11, 2011, now issued as [[(]] U.S. Patent No. 8,966,747 ~~to be issued on March 3, 2015~~). This application is related to U.S. Patent Application Serial No. 14/635,420, filed on March 2, 2015, now issued as U.S. Patent No. 9,439,297. ~~titled "PANEL-MOLDED ELECTRONIC ASSEMBLIES," attorney docket 00614-0168002.~~ The entire contents of the above applications are herein incorporated by reference.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/635,467	03/02/2015	Patrizio Vinciarelli	00614-0168003	1058

26214 7590 11/09/2016
FISH & RICHARDSON P.C. (VLT, INC)
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
ARBES, CARL J	

ART UNIT	PAPER NUMBER
3729	

NOTIFICATION DATE	DELIVERY MODE
11/09/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Response to Rule 312 Communication	Application No.	Applicant(s)
	14/635,467	VINCIARELLI ET AL.
	Examiner	Art Unit
	CARL ARBES	3729

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

1. ☒ The amendment filed on _____ under 37 CFR 1.312 has been considered, and has been:

a) ☐ entered.

b) ☒ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

/CARL ARBES/
Primary Examiner, Art Unit 3729

Amendments to the Specification:

Please add the following new paragraph before "Field of the Invention" on page 1:

CLAIM OF PRIORITY

[001] This application is a divisional of and claims priority under 35 USC 121 to U.S. Application Serial No. 13/105,696, filed on May 11, 2011 (U.S. Patent No. 8,966,747 to be issued on March 3, 2015). This application is related to U.S. Patent Application Serial No. 14/635,420, filed on March 2, 2015, titled "PANEL-MOLDED ELECTRONIC ASSEMBLIES," attorney docket 00614-0168002. The entire contents of the above applications are herein incorporated by reference.

Change(s) applied to document, /R.L./ 8/2/2016

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/635,467	12/06/2016	9516761	00614-0168003	1058

26214 7590 11/16/2016

FISH & RICHARDSON P.C. (VLT, INC)
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Patrizio Vinciarelli, Boston, MA;
VLT, Inc., Sunnyvale, CA;
Michael B. LaFleur, East Hampstead, NH;
Sean Timothy Fleming, Worcester, MA;
Rudolph F. Mutter, North Andover, MA;
Andrew T. D'Amico, Beverly Hills, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.