

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DELTA ELECTRONICS, INC.,

Petitioner

v.

VICOR CORPORATION,

Patent Owner

Patent No. 9,516,761

Inter Partes Review No.
IPR2024-00227

DECLARATION OF SYLVIA HALL-ELLIS, PH.D.

I. INTRODUCTION

1. My name is Sylvia D. Hall-Ellis. I have been retained as an expert on behalf of Delta Electronics, Incorporated (“Petitioner”).

2. I have written this Declaration on behalf of Petitioner to provide my expert opinion regarding the authenticity and public availability of several publications. My Declaration sets forth my opinions in detail and provides the basis for my opinions regarding the public availability of these publications.

3. I reserve the right to supplement or amend my opinions, and basis for them, in response to any additional evidence, testimony, discovery, argument, and/or other additional information that may be provided to me after the date of this Declaration.

4. I am being compensated for my time spent working on this matter at my normal consulting rate of \$350 per hour, plus reimbursement for any additional reasonable expenses. My compensation is not in any way tied to the content of this Declaration, the substance of my opinions, or the outcome of this litigation. I have no other interests in this proceeding or with any of the parties.

5. All of the materials that I considered are discussed explicitly in this Declaration.

II. QUALIFICATIONS

6. I am currently an Adjunct Professor in the School of Information at San José State University. I obtained a Master of Library Science from the University of North Texas in 1972 and a Ph.D. in Library Science from the University of Pittsburgh in 1985. Over the last 50-plus years, I have held various positions in the field of library and information resources. I was first employed as a librarian in 1966 and have been involved in the field of library sciences since, holding numerous positions.

7. I am a member of the American Library Association (ALA) and its Association for Library Collections & Technical Services (ALCTS) Division, and I served on the Committee on Cataloging: Resource and Description (which wrote the new cataloging rules) and as the chair of the Committee for Education and Training of Catalogers and the Competencies and Education for a Career in Cataloging Interest Group. I also served as the Chair of the ALCTS Division's Task Force on Competencies and Education for a Career in Cataloging. Additionally, I have served as the Chair for the ALA Office of Diversity's Committee on Diversity, as a member of the REFORMA National Board of Directors, as a member of the Editorial Board for the ALCTS premier cataloging journal, *Library Resources and Technical Services*, as a Co-Chair of the Library Research Round Table (LRRT) for the

American Library Association, and as a member of the LRRT Nominating Committee.

8. I have also given over one hundred presentations in the field, including several on library cataloging systems and Machine-Readable Cataloging (“MARC”) standards. My current research interests include library cataloging systems, metadata, and organization of electronic resources.

9. My full curriculum vitae is attached hereto as Appendix A.

III. LIBRARY CATALOGING PRACTICES

A. MARC RECORDS AND THE ONLINE LIBRARY CATALOG

10. I am fully familiar with the library cataloging standard known as the MARC standard, which is an industry-wide standard method of storing and organizing library catalog information.¹ MARC was first developed in the 1960s by the Library of Congress. A MARC-compatible library is one that has a catalog consisting of individual MARC records for each of its items. Today, MARC is the primary communications protocol for the transfer and storage of bibliographic metadata in libraries.

11. MARC is a framework into which descriptive bibliographic data are transcribed to interact with the software in online library catalogs to provide access

¹ The full text of the standard is available from the Library of Congress at <http://www.loc.gov/marc/bibliographic/> (last visited August 25, 2023).

to books, journals, and other resources in the collection. The bibliographic data provide points of access and can be searched by a person of ordinary skill in the art at the time of the invention (“POSITA,” see paragraphs 35-37 below) to identify and obtain resources in the library collection. An information seeker (or POSITA) can search a local online library catalog or the holdings of a group of libraries in a state or region or in the global catalog WorldCat.

12. MARC records are not designed for public viewing. Although a significant number of libraries provide access to the MARC version of a bibliographic record, the public display is designed to show information in a succinct manner that is quickly understood and useful to the information seeker. Libraries determine the default search for the online catalog to make the entry of search terms efficient and result in a successful search. Information seekers can enter a keyword, title, author, or standard number for the item. Libraries may also provide a search capability called “Summon” that allows the information seeker to enter known information about the item to conduct a search.

13. Since at least the early 1970s and continuing to the present day, MARC has been the primary communications protocol for the transfer and storage of bibliographic metadata in libraries.² As explained by the Library of Congress:

² A complete history of the development of MARC can be found in *MARC: Its History and Implications* by Henrietta D. Avram (Washington, DC: Library of Congress, 1975) and available online from the Hathi Trust (<https://babel>).

You could devise your own method of organizing the bibliographic information, but you would be isolating your library, limiting its options, and creating much more work for yourself. Using the MARC standard prevents duplication of work and allows libraries to better share bibliographic resources. Choosing to use MARC enables libraries to acquire cataloging data that is predictable and reliable. If a library were to develop a “home-grown” system that did not use MARC records, it would not be taking advantage of an industry-wide standard whose primary purpose is to foster communication of information.

Using the MARC standard also enables libraries to make use of commercially available library automation systems to manage library operations. Many systems are available for libraries of all sizes and are designed to work with the MARC format. Systems are maintained and improved by the vendor so that libraries can benefit from the latest advances in computer technology. The MARC standard also allows libraries to replace one system with another with the assurance that their data will still be compatible.

Why Is a MARC Record Necessary? LIBRARY OF CONGRESS.³

hathitrust.org/cgi/pt?id=mdp.39015034388556;view=1up;seq=1; last visited August 25, 2023).

³ <http://www.loc.gov/marc/umb/um01to06.html#part2>

14. Thus, almost every major library in the world is MARC-compatible. See, e.g., *MARC Frequently Asked Questions (FAQ)*, LIBRARY OF CONGRESS.⁴ (“MARC is the acronym for MACHine-Readable Cataloging. It defines a data format that emerged from a Library of Congress-led initiative that began fifty years ago. It provides the mechanism by which computers exchange, use, and interpret bibliographic information, and its data elements make up the foundation of most library catalogs used today.”). MARC is the ANSI/NISO Z39.2-1994 standard (reaffirmed in 2016) for Information Interchange Format. The full text of the standard is available from the Library of Congress.⁵

15. Examining the MARC records for a specific item reveals the comprehensive data transcribed about a particular item at the time that cataloging and classification occurred. In addition to the creator, title, subjects, and standard numbers, additional information may provide additional and relevant data depending on the type of resource. Understanding the full extent of bibliographic data for an item and the points of access associated with it provides essential information that can be used to determine the indexing and public availability for documents described in this Declaration.

⁴ <https://www.loc.gov/marc/faq.html>

⁵ <http://www.loc.gov/marc/bibliographic/>

B. MARC RECORDS

16. A MARC record comprises several fields, each of which contains specific data about the work. Each field is identified by a standardized, unique, three-digit code corresponding to the type of data that follow. For example, a work's title is recorded in Field 245; the primary author of the work is transcribed in Field 100; an item's International Standard Book Number ("ISBN") consisting of ten or thirteen digits is transcribed in Field 020; an item's International Standard Serial Number ("ISSN") is transcribed in Field 022; the Library of Congress classification notation is recorded in Field 050; and the publication date is recorded in Field 260 under the subfield "c." If a work is a periodical, then its publication frequency is recorded in Field 310, and the publication dates (e.g., the first and last publication) are recorded in Field 362, which is also referred to as the enumeration/chronology field.⁶

17. The library that created the record is recorded in Field 040 in subfield "a" with a unique library code. When viewing the MARC record online via Online Computer Library Center's ("OCLC") bibliographic database, hovering over this code with the mouse reveals the full name of the library. I used this method of "mousing over" the library codes in the OCLC database to identify the originating library for the MARC records discussed in this Declaration. Where this "mouse

⁶ <http://www.loc.gov/marc/bibliographic/bd3xx.html>

over” option was not available, I consulted the Directory of OCLC Libraries to identify the institution that created the MARC record.⁷

18. MARC records also include several fields that include subject matter classification information. An overview of MARC record fields is available through the Library of Congress.⁸ For example, 6XX fields are termed “Subject Access Fields.”⁹ Among these, for example, is the 650 field; this is the “Subject Added Entry – Topical Term” field.¹⁰ The 650 field is a “[s]ubject added entry in which the entry element is a topical term.” These entries “are assigned to a bibliographic record to provide access according to generally accepted thesaurus-building rules (e.g., *Library of Congress Subject Headings* (LCSH), *Medical Subject Headings* (MeSH)).” *Id.* Further, MARC records include call numbers, which themselves include a classification number. For example, the 050 field is the “Library of Congress Call Number.”¹¹ A defined portion of the Library of Congress Call (LCC) Number is the classification number, and “source of the classification number is *Library of Congress Classification* and the *LC Classification-Additions and Changes*.” Thus, included in the 050 field is a subject matter classification. Further,

⁷ <https://www.oclc.org/en/contacts/libraries.html>

⁸ <http://www.loc.gov/marc/bibliographic/>

⁹ <http://www.loc.gov/marc/bibliographic/bd6xx.html>

¹⁰ <http://www.loc.gov/marc/bibliographic/bd650.html>

¹¹ <http://www.loc.gov/marc/bibliographic/bd050.html>

the 082 field is the “Dewey Decimal Call Number.”¹² A defined portion of the Dewey Decimal Call (DDC) Number is the classification number, and “source of the classification number is the *Dewey Decimal Classification and Relative Index*.” Thus, included in the 082 field is a subject matter classification. Each item in a library has a single classification number. A library selects a classification scheme (e.g., the Library of Congress classification scheme just described or a similar scheme such as the Dewey Decimal classification scheme) and uses it consistently. When the Library of Congress assigns the LCC classification number, it appears as part of the 050 field. When the Library of Congress assigns the DDC classification number, it appears as part of the 082 field. If a local library assigns the classification number, it appears in a 090 field. In either scenario, the MARC record includes a classification number that represents a subject matter classification.

C. OCLC

19. The OCLC was created “to establish, maintain and operate a computerized library network and to promote the evolution of library use, of libraries themselves, and of librarianship, and to provide processes and products for the benefit of library users and libraries, including such objectives as increasing availability of library resources to individual library patrons and reducing the rate of rise of library per-unit costs, all for the fundamental public purpose of furthering

¹² <http://www.loc.gov/marc/bibliographic/bd082.html>

ease of access to and use of the ever-expanding body of worldwide scientific, literary and educational knowledge and information.”¹³ Among other services, OCLC and its members are responsible for maintaining the WorldCat database (<http://www.worldcat.org/>), used by independent and institutional libraries throughout the world.

20. OCLC also provides its members online access to MARC records through its OCLC bibliographic database. When an OCLC member institution acquires a work, it creates a MARC record for this work in its computer catalog system in the ordinary course of its business. MARC records created at the Library of Congress are tape-loaded into the OCLC database through a subscription to MARC Distribution Services daily or weekly. Once the MARC record is created by a cataloger at an OCLC member institution or is tape-loaded from the Library of Congress, the MARC record is then made available to any other OCLC members online, and therefore made available to the public. Accordingly, once the MARC record is created by a cataloger at an OCLC member institution or is tape-loaded from the Library of Congress or another library anywhere in the world, any publication corresponding to the MARC record has been cataloged and indexed according to its subject matter such that a person interested in that subject matter

¹³ Third Article, Amended Articles of Incorporation of OCLC Online Computer Library Center, Incorporated (available at <https://www.oclc.org/content/dam/oclc/membership/articles-of-incorporation.pdf>).

could, with reasonable diligence, locate and access the publication through any library with access to the OCLC bibliographic database or through the Library of Congress.

21. When an OCLC member institution creates a new MARC record, OCLC automatically supplies the date of creation for that record. The date of creation for the MARC record appears in the fixed Field (008), characters 00 through 05. The MARC record creation date reflects the date on which, or shortly after which, the item was first acquired or cataloged. Initially, Field 005 of the MARC record is automatically populated with the date the MARC record was created in year, month, day format (YYYYMMDD) (some of the newer library catalog systems also include hour, minute, second (HHMMSS)). Thereafter, the library's computer system may automatically update the date in Field 005 every time the library updates the MARC record (*e.g.*, to reflect that an item has been moved to a different shelving location within the library). Field 005 is visible when viewing a MARC record via an appropriate computerized interface, but when a MARC record is printed to hardcopy, no "005" label appears. The initial Field 005 date (*i.e.*, the date the MARC record was created) does appear, however, next to the label "Entered."¹⁴ The date

¹⁴ Field 005 is visible when viewing a MARC record via an appropriate computerized interface. But when a MARC record is printed directly to hardcopy from the OCLC database, the "005" label is not shown. The date in the 005 field instead appears next to the label "Replaced."

upon which the most recent update to Field 005 occurred also appears, next to the label “Replaced.” Thus, when an item’s MARC record has been printed to hardcopy—as is the case with the MARC attachments to this Declaration—the date reflected next to the label “Entered” is necessarily on or after the date the library first cataloged and indexed the underlying item.

22. Once one library has cataloged and indexed a publication by creating a MARC record for that publication, other libraries that receive the publication do not create additional MARC records—the other libraries instead rely on the original MARC record. They may update or revise the MARC record to ensure accuracy, but they do not replace or duplicate it. This practice does more than save libraries from duplicating labor. It also enhances the accuracy of MARC records. Further, it allows librarians around the world to know that a particular MARC record is authoritative (in contrast, a hypothetical system wherein duplicative records were created would result in confusion as to which record is authoritative).

23. Catalogers can create MARC records for all types of print, online, and digital resources. The date of creation of the MARC record by a cataloger at an OCLC member institution reflects when the underlying item is accessible to the public. Upwards of two-thirds to three-quarters of book sales and magazine subscriptions to libraries come from a jobber or wholesaler for online and print resources. These resellers make it their business to provide items to their customers

as fast as possible, often providing turnaround times of only a single day after publication. Libraries purchase a significant portion of the balance of their books and journals directly from publishers themselves, which provide delivery on a similarly expedited schedule. In general, libraries make these purchases throughout the year and shelve the newly received items as soon thereafter as possible to make them available to their patrons.

24. In preparing this Declaration, I used authoritative databases, such as the OCLC bibliographic database and the Library of Congress Online Catalog, to confirm citation details of the various publications discussed.

25. *Indexing.* A researcher may discover material relevant to his or her topic in a variety of ways. One common means of discovery is to search for relevant information in an index of periodical and other publications. Having found relevant material, the researcher will then normally obtain it online, look for it in libraries, or purchase it from a publisher, a bookstore, a document delivery service, or other provider. Sometimes, the date of a document's public accessibility will involve both indexing and library date information. However, date information for indexing entries is often unavailable. This is especially true for online indices.

26. Indexing services use a wide variety of controlled vocabularies to provide subject access and other means of discovering the content of documents. The formats in which these access terms are presented vary from service to service.

27. Online indexing services commonly provide bibliographic information, abstracts, and full-text copies of the indexed publications, along with a list of the documents cited in the indexed publication. These services also often provide lists of publications that cite a given document. A citation of a document is evidence that the document was publicly available and in use by researchers no later than the publication date of the citing document.

28. Before the widespread development of online databases to index articles in journals, magazines, conference papers, and technical Declarations, libraries purchased printed volumes of indices. Graduate library school education mandated that students learn about the bibliographic control of disciplines, the prominent indexing volumes, and searching strategies required to use them effectively and efficiently. Half of the courses that I studied in library school were focused on bibliography and resources in academic disciplines.

29. Librarians consulted with information seekers to verify citations, check availability in union catalogs, printed books catalogs, the OCLC database, and make formal requests for materials (e.g., books, conference proceedings, journal articles). Requests were transmitted using Telex machines, rudimentary email systems, and the United States Postal Service. During my career, I have performed and supervised staff who handled these resource sharing tasks.

30. A citation of a document by another is evidence that the document was

publicly available and in use no later than the publication date of the citing document.

IV. PRELIMINARIES

31. *Scope of this Declaration.* I am not an attorney and will not offer opinions on the law. I am, however, rendering my expert opinion on the authenticity of the documents referenced herein and on when and how each of these documents was disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art, exercising reasonable diligence, could have located the documents before on or around the listed dates of their respective publications below.

32. I am informed by counsel that a printed publication qualifies as publicly accessible as of the date it was disseminated or otherwise made available such that a person interested in and ordinarily skilled in the relevant subject matter could locate it through the exercise of ordinary diligence.

33. While I understand that the determination of public accessibility under the foregoing standard rests on a case-by-case analysis of the facts particular to an individual publication, I also understand that a printed publication is rendered “publicly accessible” if it is cataloged and indexed by a library such that a person interested in the relevant subject matter could locate it (*i.e.*, I understand that cataloging and indexing by a library is sufficient, though there are other ways that a

printed publication may qualify as publicly accessible). One manner of sufficient indexing is indexing according to subject matter category. I understand that the cataloging and indexing by a single library of a single instance of a particular printed publication is sufficient, even if the single library is in a foreign country. I understand that, even if access to a library is restricted, a printed publication that has been cataloged and indexed therein is publicly accessible so long as a presumption is raised that the portion of the public concerned with the relevant subject matter would know of the printed publication. I also understand that the cataloging and indexing of information that would guide a person interested in the relevant subject matter to the printed publication, such as the cataloging and indexing of an abstract for the printed publication, is sufficient to render the printed publication publicly accessible.

34. I understand that routine business practices, such as general library cataloging and indexing practices, can be used to establish an approximate date on which a printed publication became publicly accessible.

35. *Persons of ordinary skill in the art.* I am told by counsel that the subject matter of this proceeding generally relates to the layout, packaging, and manufacture of power converters and power modules.

36. I have been informed by counsel that a “person of ordinary skill in the art at the time of the inventions” is a hypothetical person who is presumed to be

familiar with the relevant field and its literature at the time of the inventions. This hypothetical person is also a person of ordinary creativity, capable of understanding the scientific principles applicable to the pertinent field.

37. I am told by counsel that persons of ordinary skill in this subject matter or art would have had at least a master's degree in electrical engineering and two or more years of work experience relating to power electronics and the manufacture of power converters or printed circuit board design for power converters, with more experience potentially substituting for education or vice versa.

38. It is my opinion that such a person would have been engaged in research, learning through study and practice in the field and possibly through formal instruction the bibliographic resources relevant to his or her research. In the 2010-2011 timeframe, such a person would have had access to a vast array of long-established print resources.

**V. DOCUMENT 1: ATTACHMENT 1 (EXHIBIT 1016)
("BALOGH")**

39. Attached hereto as Attachment 1 is a copy of a technical report, *Design Review: 140W, Multiple Output High Density DC/DC Converter*, prepared by Laszlo Balogh and distributed by Texas Instruments (hereafter "Balogh") with a 1997 publication date and a 2011 copyright date. The Balogh document was presented at the Power Supply Design Seminar in 1997 as Topic 6. The Texas Instruments website lists the Balogh document as a top resource for the 1990s (see Attachment

1A). The Balogh document¹⁵ can be downloaded from the Texas Instruments website. The Balogh document is further identified as SLUP117 and numbered A122010 on page 26. Attachment 1 is a true and correct copy of the Balogh document that I downloaded from the Texas Instruments website.

40. The text in Attachment 1 is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Attachment 1 was found on the website of the corporation responsible for its content and is a true and correct copy in a condition that creates no suspicion about its authenticity.

41. In view of the above, it is my opinion that the Balogh document was publicly available by December 31, 1997, because by that date it had been uploaded to the Texas Instruments website and could be downloaded free of charge. For these reasons, it is my opinion that Attachment 1 was published and accessible to the public by December 31, 1997.

VI. DOCUMENT 2: ATTACHMENT 2 (EXHIBIT 1008) ("ERICKSON")

42. Attached hereto as Attachment 2 is a copy of a book, *Fundamentals of Power Electronics*, 2nd edition, by Robert W. Erickson and Dragan Maksimović (hereafter "Erickson") and issued by Kluwer Academic with a 2001 copyright date.

¹⁵ <https://www.ti.com/seclit/ml/slup117/slup117.pdf>

Attachment 2 is a true and correct copy of the title page, copyright page, and table of contents as held by the Steenbock Library at the University of Wisconsin – Madison. I obtained Attachment 2 from the Steenbock Library at the University of Wisconsin – Madison and Attachment 2 is a copy of the entire book. I confirmed this by matching the ISBN numbers and other information in Attachment 2A with Attachment 2. The text in Attachment 2 is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Attachment 2 is a true and correct copy in a condition that creates no suspicion about its authenticity.

43. Attached hereto as Attachment 2A is a true and correct copy of the MARC record for this monograph from the Steenbock Library at the University of Wisconsin – Madison online catalog. Library ownership is indicated by the presence of the library’s code (“GZM”) in the 049 field. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on March 30, 2015, as shown in the 005 field (“20150330”). I personally identified and retrieved the library catalog record which is Attachment 2A.

44. Attached hereto as Attachment 2B is a true and correct copy of the MARC record for the book titled *Fundamentals of Power Electronics*, 2nd edition, obtained from the OCLC bibliographic database. I personally identified and

retrieved the MARC record that is Attachment 2B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 2B, that library code is “DLC,” which means that the MARC record for this book was created at the Library of Congress as part of the Cataloging in Publication (CIP) Program.¹⁶ The MARC record prepared as part of the CIP Program tracked the receipt, final cataloging, and shelf-ready preparation of the Erickson book (see Attachment 2C). As shown in field 955, the book bibliographic data for the book were verified upon receipt (March 13, 2001). It would have been able to be located by a person of ordinary skill in the art using the library catalog system and was thus publicly accessible as of this date.

45. As can be seen in the “Entered” field in the MARC record for this exhibit, a cataloger at the Library of Congress created OCLC record number 45270412 on January 25, 2000, as shown in the “Entered” field (“20000125”). The library continues to update and enhance this MARC record to meet current cataloging rules. The most recent enhancement to Attachment 2B occurred on January 26, 2023, as shown in the “Replaced” field (“20230126”). I personally identified and retrieved the MARC record that is Attachment 2B.

46. Attachment 2B further includes an entry in field 050 (“TK7881.15 \$b .E75 2001”)—as described above, this includes a subject matter classification

¹⁶ <https://www.loc.gov/programs/cataloging-in-publication/about-this-program/>

number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 082 (“621.381”), a subject matter consistent with the Dewey Decimal classification system. Attachment 2B further includes a descriptor term reading “Power electronics” (see Attachment 2D, Library of Congress subject heading sh85105978) in the 650 field. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 2B was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entry. Further, as of October 25, 2000, the MARC record attached hereto as Attachment 2B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that added this book to its collection, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

47. Further supporting my opinion that Attachment 2 was publicly accessible to ordinarily skilled and interested researchers in the field is the fact that the book titled *Fundamentals of Power Electronics*, 2nd edition, was registered with the U.S. Copyright Office as item TX0005348560 on February 16, 2001, and indicated a publication date of December 21, 2000, (see Attachment 2E, U. S. Copyright Office Public Catalog). As noted above, this would have provided a

POSITA with keyword searching capabilities and other tools to locate this book.

48. Attachment 2B indicates that the Erickson book cataloged at the Library of Congress is currently available from 258 libraries. In view of above, the Erickson monograph was publicly available on or shortly after March 13, 2001, because by that date it had been cataloged and indexed at the Library of Congress, made part of the OCLC bibliographic database, and received in the Steenbock Library at the University of Wisconsin – Madison. For these reasons, it is my opinion that Attachment 2 was published and accessible to the public on or shortly after March 13, 2001.

VII. DOCUMENT 3: ATTACHMENT 3 (EXHIBIT 1017) (“KASSAKIAN”)

49. Attached hereto as Attachment 3 is a copy of a book, *Principles of Power Electronics*, 1st edition, by John G. Kassakian, Martin F. Schlecht, and George C. Verghes (hereafter “Kassakian”) and issued by Addison-Wesley with a 1991 copyright date. Attachment 3 is a true and correct copy of the title page, copyright page, and table of contents as held by the Karl F. Wendt Engineering Library at the University of Wisconsin – Madison. I obtained Attachment 3 from the Karl F. Wendt Engineering Library at the University of Wisconsin – Madison and Attachment 3 is a copy of the entire book. I confirmed this by matching the ISBN numbers and other information in Attachment 3A with Attachment 3. The text in Attachment 3 is complete; no pages are missing, and the text on each page

appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Attachment 3 is a true and correct copy in a condition that creates no suspicion about its authenticity.

50. Attached hereto as Attachment 3A is a true and correct copy of the MARC record for this monograph from the Karl F. Wendt Engineering Library at the University of Wisconsin – Madison online catalog. Library ownership is indicated by the presence of the library’s code (“GZM”) in the 049 field. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on March 23, 2018, as shown in the 005 field (“20180323”). I personally identified and retrieved the library catalog record which is Attachment 3A.

51. The International Standard Book Number (ISBN) on Attachment 3 (0-201-09689-7) matches the ISBN in field 020 of Attachment 3A. Therefore, Attachment 3 is the same book as the one that the cataloger at the Karl F. Wendt Engineering Library at the University of Wisconsin – Madison used to create the MARC record that is Attachment 3. Therefore, the book titled *Principles of Power Electronics*, 1st edition, was present and cataloged in the Karl F. Wendt Engineering Library at the University of Wisconsin – Madison on October 23, 1997. It would have been able to be located by a person of ordinary skill in the art using the library catalog system and was thus publicly accessible as of this date.

52. Attached hereto as Attachment 3B is a true and correct copy of the MARC record for the book titled *Principles of Power Electronics*, 1st edition, obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 3B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 3B, that library code is “DLC,” which means that the MARC record for this book was created at the Library of Congress as part of the Cataloging in Publication (CIP) Program.¹⁷ The MARC record prepared as part of the CIP Program tracked the receipt, final cataloging, and shelf-ready preparation of the Erickson book (see Attachment 3C). As shown in field 955, the book bibliographic data for the book were verified upon receipt (July 8, 1991). It would have been able to be located by a person of ordinary skill in the art using the library catalog system and was thus publicly accessible as of this date.

53. As can be seen in the “Entered” field in the MARC record for this exhibit, a cataloger at the Library of Congress created OCLC record number 22207160 on July 25, 1990, as shown in the “Entered” field (“19900725”). The library continues to update and enhance this MARC record to meet current cataloging rules. The most recent enhancement to Attachment 3B occurred on April 2, 2023, as shown in the “Replaced” field (“20230402”). I personally identified and

¹⁷ <https://www.loc.gov/programs/cataloging-in-publication/about-this-program/>

retrieved the MARC record that is Attachment 3B.

54. Attachment 3B further includes an entry in field 050 (“TK7881.15 \$b .K37 1991”)—as described above, this includes a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 080 (“621.38”), a subject matter consistent with the Dewey Decimal classification system. Attachment 3B further includes a descriptor term reading “Power electronics” (see Attachment 2D, Library of Congress subject heading sh85105978) in the 650 field. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 3B was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 080 entry, and the field 650 entry. Further, as of July 25, 1990, the MARC record attached hereto as Attachment 3B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that added this book to its collection, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

55. Further supporting my opinion that Attachment 3 was publicly accessible to ordinarily skilled and interested researchers in the field is the fact that the book titled *Principles of Power Electronics*, 1st edition, was registered with the

U. S. Copyright Office as item TX0003202575 on December 9, 1991, and indicated a publication date of October 3, 1991, (see Attachment 3C, U. S. Copyright Office Public Catalog). As noted above, this would have provided a POSITA with keyword searching capabilities and other tools to locate this book.

56. Attachment 3B indicates that the Kassakian book as cataloged in the Library of Congress is currently available from 297 libraries. In view of above, the Kassakian monograph was publicly available on or shortly after July 8, 1991, because by that date it had been received, cataloged and indexed at the Library of Congress and made part of the OCLC bibliographic database. For these reasons, it is my opinion that Attachment 3 was published and accessible to the public on or shortly after July 8, 1991.

VIII. DOCUMENT 4: ATTACHMENT 4 (EXHIBIT 1012) (“HUBER 2006”)

57. Attached hereto as Attachment 4 is a copy of the journal article titled “1.8-MHz, 48-V Resonant VRM: Analysis, Design, and Performance Evaluation” by L. Huber, Kevin Hsu, Milan M. Jovanovic, Denis James Solley, Gennady Gurov, and Robert M. Porter (hereafter “Huber 2006”). The Huber 2006 article was published in Volume 21, Issue 1 of the titled *IEEE Transactions on Power Electronics*. The Huber 2006 article appears beginning on page 79 of this issue dated January 2006. Attachment 4 is a true and correct copy of the Huber 2006 article (pages 79-88). Specifically, the text of the article is complete; no pages are missing,

and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. The Huber 2006 article was available from the *IEEE Xplore* database¹⁸ and the digital repositories *ResearchGate*¹⁹ and *Semantic Scholar*.²⁰ Attachment 4 was found within the custody of the publisher – a place where an authentic copy of this open access journal would likely be. Attachment 4 is a true and correct copy in a condition that creates no suspicion about its authenticity.

58. Attached hereto as Attachment 4A is a true and correct copy of the MARC record for the journal titled *IEEE Transactions on Power Electronics* at the Linda Hall Library of Science, Engineering & Technology (Kansas City, Missouri). Library ownership is indicated by the presence of the library's code ("LHL") in field 049. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to Attachment 4A occurred on September 6, 2023, as shown in field 005 ("20230906"). I personally identified and retrieved the MARC record that is Attachment 4A.

59. Based on finding a copy of Attachment 4 in the Linda Hall Library of

¹⁸ <https://ieeexplore.ieee.org/document/1566692>

¹⁹ https://www.researchgate.net/publication/3280837_18-MHz_48-V_Resonant_VRM_Analysis_Design_and_Performance_Evaluation

²⁰ <https://www.semanticscholar.org/paper/1.8-MHz%2C-48-V-Resonant-VRM%3A-Analysis%2C-Design%2C-and-Huber-Hsu/4683796795b1de89f2a028406e53b86912d007f0>

Science, Engineering & Technology and MARC record in its online library catalog attached as Attachment 4A, it is my opinion that the Huber 2006 article published in the journal titled *IEEE Transactions on Power Electronics* was publicly available on or shortly after January 23, 2006, as shown by the library's stamp on the cover. In common practice these stamps are applied at or around the time the volume is entered into the library's collection and the volume is made available to library patrons within a short time thereafter. Attachment 4A also shows that Exhibit 1012 was catalogued with a descriptor term reading "Power electronics \$v Periodicals" (see Attachment 2D, Library of Congress subject heading sh85105978 and Attachment 4B, Library of Congress subject heading sh85099890) in the 650 field.

60. As noted in the holdings information (362 field), the Linda Hall Library of Science, Engineering & Technology has received the journal titled *IEEE Transactions on Power Electronics* since January 1986 and continues to receive the publication. In view of the MARC record for Attachment 4 the Huber 2006 article was publicly on or shortly after January 23, 2006, because the serial title had been received, cataloged, and indexed at the Linda Hall Library of Science, Engineering & Technology and made part of its online catalog database.

61. Attached hereto as Attachment 4C is a true and correct copy of the MARC record for the journal titled *IEEE Transactions on Power Electronics* obtained from the OCLC bibliographic database. As previously noted, the library

that created the record is recorded in field 040 with a unique library code. For Attachment 4C, that library code is “NSD,” which means that the MARC record for this serial was cataloged as part of the National Serials Data Program at the Library of Congress. As can be seen in the “Entered” field in the MARC record for this exhibit, a cataloger at the Library of Congress created OCLC record number 12760678 on November 5, 1985, as shown in the “Entered” field (“19851105”). The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. The most recent enhancement to Attachment 4C occurred on June 15, 2023, as shown in the “Replaced” field (“20230615”). I personally identified and retrieved the MARC record that is Attachment 4C. The “BLvl” entry in Attachment 4C is “s,” which indicates that the journal titled *IEEE Transactions on Power Electronics* is a serial publication. Field 310 of Attachment 4C reads “Monthly, \$b <Feb. 2013-.” Accordingly, the MARC record for Attachment 4 corresponds to the journal titled *IEEE Transactions on Power Electronics* from the time the serial title began and includes the date of the Huber 2006 article.

62. Attachment 4C includes an entry in field 050 (“TK7881.15 \$b I34”)—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 082 (“621.31/7”), a subject matter

consistent with the Dewey Decimal classification system. Attachment 4C further includes a descriptor term reading “Power electronics \$v Periodicals” (see Attachment 2D, Library of Congress subject heading sh85105978 and Attachment 4B, Library of Congress subject heading sh85099890) in the 650 field. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 4C was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entry. As of November 5, 1985, the MARC record attached hereto as Attachment 4C was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that subscribed to the serial, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

63. Attachment 4C indicates that the journal titled *IEEE Transactions on Power Electronics* as cataloged at the Library of Congress is currently available from 349 libraries. In view of the above, this issue of the journal titled *IEEE Transactions on Power Electronics* was publicly available on or shortly after January 23, 2006, because by that date it had been cataloged and indexed at the Library of Congress, made part of the OCLC bibliographic database, and received at the Linda Hall Library of Science, Engineering & Technology. For these reasons, it is my opinion

that Attachment 4 was published and accessible to the public on or shortly after January 23, 2006.

**IX. DOCUMENT 5: ATTACHMENT 5 (EXHIBIT 1011)
("SPIAZZI")**

64. Attached hereto as Attachment 5 is a copy of a conference paper published in the five-volume set titled *2007 IEEE Industry Applications Annual Meeting* found in the King Library at San José State University (San José, California). The conference paper titled "Layout Considerations and Thermal Analysis of a 1.8 MHz Resonant VRM" by G. Spiazzi, L. Rossetto, P. Mattavelli, P. Cova, and N. Delmonte (hereafter "Spiazzi") appears beginning on page 1993 in volume 5. The 2007 IEEE Industry Applications Annual Meeting was held on September 23-27, 2007, in New Orleans, Louisiana. Attachment 5 is a true and correct copy of the Spiazzi conference paper (volume 5, pages 1993-2000). I obtained this copy of the conference paper from the King Library at San José State University. Specifically, the text of the Spiazzi conference paper is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Attachment 5 was found within the custody of a library – a place where, if authentic, a copy of this five-volume conference proceedings set would likely be. Attachment 5 is a true and correct copy in a condition that creates no suspicion about authenticity.

65. The Spiazzi conference paper is also available in the *IEEE Xplore* database²¹ and the digital repositories *ResearchGate*²² and *Semantic Scholar*.²³ The *IEEE Xplore* database indicates that the Spiazzi conference paper was added and publicly available on October 15, 2007. The five-volume set titled *2007 IEEE Industry Applications Annual Meeting* was published electronically and is available as an on-demand print publication from Curran Associates, Incorporated.²⁴

66. Attached hereto as Attachment 5A is a true and correct copy of the MARC record for the five-volume set of conference proceedings titled *2007 IEEE Industry Applications Annual Meeting* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 5A. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 5A, that library code is “COO,” which means that the MARC record for this five-volume conference proceedings set was cataloged in the Mann Library at Cornell University (Ithaca, New York). As can be seen in the “Entered” field in the MARC record for this exhibit, a cataloger in the Mann Library at Cornell University created OCLC record number 5698741 on

²¹ <https://ieeexplore.ieee.org/document/4348051>

²² https://www.researchgate.net/publication/224290247_Layout_Considerations_and_Thermal_Analysis_of_a_18_MHz_Resonant_VRM

²³ <https://www.semanticscholar.org/paper/Layout-Considerations-and-Thermal-Analysis-of-a-1.8-Spiazzi-Rossetto/a7d497acf4e2eb1d398375173123e351ee2d0459>

²⁴ <https://www.proceedings.com/01951.html>

November 15, 1979, for the monographic serial as shown in the “Entered” field (“19791115”). The library continues to update this MARC record the MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on February 8, 2022, as shown in the “Replaced” field (“20220208”).

67. Attachment 5A further includes an entry in field 050 (“TK5 \$b .I2”)—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 082 (“621.3/05”)—as described above, a subject matter classification number consistent with the Dewey Decimal classification system. Attachment 5A also shows that Attachment 5 was catalogued with two descriptor terms reading “Electrical engineering \$v Congresses” (see Attachment 5B, Library of Congress subject heading sh2008102881) and “Electric power \$v Congresses” (Attachment 5C, Library of Congress subject heading sh2008102884) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 5A was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entries. Further, as of November 15, 1979, the MARC record attached hereto as Attachment 5A was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that acquired the five-volume conference

proceedings set, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

68. Attachment 5A indicates that the five-volume conference proceedings set titled *2007 IEEE Industry Applications Annual Meeting* as cataloged in the Mann Library at Cornell University is currently available from 155 libraries. In view of the above, the five-volume conference proceedings set titled *2007 IEEE Industry Applications Annual Meeting* was publicly available on or shortly after October 15, 2007, because by that date it had been received, cataloged, and indexed in the King Library at San José State University as part of the *IEEE Xplore* database. For these reasons, it is my opinion that Attachment 5 was published and publicly accessible on or shortly after October 15, 2007.

X. SUMMARY OF OPINIONS

69. In view of the foregoing, it is my opinion that the publication described above were publicly available no later than the corresponding date listed in the table below:

Exhibit	Publication	Publicly Available No Later Than
1016	Balogh, Laszlo. <i>Design Review: 140W, Multiple Output High Density DCIDC Converter</i> . TI Literature Number: SLUP117. Dallas, TX: Texas Instruments, c2017, 1997.	December 31, 1997
1008	Erickson, Robert W., and Dragan Maksimović. <i>Fundamentals of Power Electronics</i> . 2nd ed. Norwell, MA: Kluwer Academic, ©2001.	March 13, 2001
1017	Kassakian, John G., Martin F. Schlecht, and George C. Verghes. <i>Principles of Power Electronics</i> . 1st ed. Reading, MA: Addison-Wesley, ©1992.	July 8, 1991
1012	Huber, L., Kevin Hsu, Milan M. Jovanovic, Denis James Solley, Gennady Gurov, and Robert M. Porter. “1.8-MHz, 48-V Resonant VRM: Analysis, Design, and Performance Evaluation.” <i>IEEE Transactions on Power Electronics</i> , vol. 21, issue 1 (January 2006): 79-88.	January 23, 2006
1011	Spiazzi, G., L. Rossetto, P. Mattavelli, P. Cova, and N. Delmonte. “Layout Considerations and Thermal Analysis of a 1.8 MHz Resonant VRM.” <i>2007 IEEE Industry Applications Annual Meeting</i> (vol. 5, pp. 1993-2000). 5 vols. New York: Institute of Electrical and Electronics Engineers, ©2007.	October 15, 2007

70. In signing this Declaration, I recognize that the Declaration will be filed as evidence in a case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

71. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1034 of Title 18 of the United States Code.

DATED: November 10, 2023

By: /s/ Sylvia D. Hall-Ellis
Sylvia D. Hall-Ellis, Ph.D.

CURRICULUM VITAE SYLVIA D. HALL-ELLIS

EDUCATION

Ph.D., University of Pittsburgh, Pittsburgh, Pennsylvania, 1985
M.P.S., University of Denver, Denver, Colorado, 2014
Post Graduate Studies, University of Texas – San Antonio, Texas, 1975-1976
M.L.S., University of North Texas, Denton, Texas, 1972
B.A., Rockford University, Rockford, Illinois, 1971

PROFESSIONAL EXPERIENCE

- 1981- Consultant for higher education, non-profit organizations, and corporations.**
- 2002- Adjunct Professor, School of Information, San José State University, San José, California.** Serve as part-time faculty member teaching graduate students in technical services (cataloging, bibliographic control, classification), “core courses,” and special topics.
- 2014-2016 Director, Grants and Resource Development, Colorado Community College System.**
Provided leadership and vision to foster the continued growth of rigorous scholarship, innovative projects, and creative work for statewide system, 13 campuses, and 50 teaching sites serving 155,000 students. Responsible for leadership and ensured efficient functioning of contract and grants in compliance with state & federal requirements and successful implementation and management. Served as a subject matter expert and liaison for college Grant Directors for all issues relating to grants and subcontracts.
- 2010-2014 Senior Grant Administrator, Morgridge College of Education, University of Denver (Colorado).** Provided leadership and vision to foster continued growth of rigorous scholarship, innovative research, and creative work in the Morgridge College of Education. Ensure that contract and grants processes function effectively and efficiently for 60 faculty and researchers with a focus on the successful progression and efficient management of grants totaling \$13M. Worked effectively and collegially with Department Chairs and Program Coordinators on operational grant-related management activities and with a broad range of internal and external constituencies. Supported the dissemination and promotion of faculty research and scholarship to outside constituents at conferences and through publications. Assisted Principal Investigators and grant project teams by coaching, mentoring, and financial management.
- 2011-2013 Interim Director & Assistant Dean, Westminster Law Library, Sturm College of Law, University of Denver.** Planned, organized, and directed all administrative activities for the library serving students, faculty, and alumni; oversaw the employment, retention, promotion, transfer and termination of library personnel; represented the library at professional conferences and public meetings; created and promoted a climate and culture of acceptance for new programs and services, a positive high-quality image of the law library, and that reflect the organization’s values, encourage excellent performance, and reward high productivity and innovation; provided leadership and set strategic direction of the organization; ensured that the library provided excellent customer service through solution-oriented staff response to patron needs and by responsiveness and continuous improvement of the organization; promoted, developed, and maintained positive working relationships with colleagues and customers including key stakeholders and groups, higher education institutions, the legal community, other regional libraries and districts statewide, and national library organizations.

- 2007-2014** **Associate Professor, Library & Information Science, Morgridge College of Education, University of Denver (Colorado).** Served in leadership role and worked collaboratively in program, college, campus and community environments. Advised and supervised students, taught core and specialized courses at the graduate level in an integrative, student-centered learning environment. Served on LIS, College, and University committees, and maintained working relationships with colleagues in other academic units and information professionals in the Rocky Mountain region and beyond. Served on and chair doctoral student dissertation committees. Oversaw and facilitated the College and LIS graduate student association.
- 2002-2007** **Assistant Professor, Library & Information Science, College of Education, University of Denver (Colorado).** Served as tenure-track faculty member teaching graduate students in “core courses,” resource description and access, service learning, and independent studies. Advised graduate students, participate on LIS and College committees, and serve on doctoral student dissertation committees. Oversaw and facilitated the LIS graduate student association and alumni association.
- 2000-2002** **Affiliate Faculty, Library & Information Science, College of Education, University of Denver (Colorado).** Served as part-time faculty member teaching graduate students in technical services (cataloging, bibliographic control, classification), “core courses,” and special topics. Oversaw and facilitated the LIS graduate student association and alumni association.
- 2000-2001** **Special Assistant to the Secretary’s Regional Representative, U.S. Department of Education, Region VIII, Denver, Colorado.** Served as the principal advisor and representative of the U. S. Secretary of Education’s Regional Representative (SRR). Ensured the implementation of major goals of the SRR and the Secretary. Provided leadership on behalf of the SRR in contacts with high-level officials in Region VIII requiring sensitive policy interpretation in communication with senior Department officials to solve problems and resolve issues raised by State and local education officials. Served as the primary contact for School-to-Work/Career, Children’s Health Insurance Program, and Safe and Drug-Free Schools. Delivered technical assistance to local education agencies and institutions of higher education in technology, professional development, and school construction.
- 1999-2000** **Catalog Librarian, Jefferson County Public Library, Lakewood, Colorado.** Performed original, copy cataloging and classification of library materials (English and Spanish) using standard library protocols; completed original descriptive cataloging and subject analysis; enhanced brief catalog and authority records in III.
- 1997-1999** **Development Officer, McREL International, Aurora, Colorado.** Served as senior member of corporate management team in strategic planning, development of proposals and contracts, implementation, and evaluation of new services, products, and programs for educational agencies. Provided creative leadership to corporate committees to solicit ideas, identify goals and objectives, plan, develop, present, and evaluate professional development opportunities.
- 1995-1997** **Education Specialist, Education Service Center, Region One, Edinburg, Texas.** Served as member of Administrative Cabinet team in strategic planning, development of proposals and contracts, implementation, and evaluation of telecommunications capabilities, services, products, and programs for 40 school districts serving 283,000 students in 7 counties. Provided creative leadership to regional and state committees to solicit ideas, identify strategic goals and objectives, plan, develop, present, and evaluate funding opportunities and professional development for 400 librarians.

- 1993-1996** **Assistant Professor of Library Science, Sam Houston State University, Huntsville, Texas.** Served as faculty member teaching 400 graduate students in technical services (cataloging, bibliographic control, classification), automation, and networking. Participated in distance education program and coordinated annual conference. Conducted university and Texas Library Association-funded field research focused on library collection development and academic achievement.
- 1992-1993** **Head Librarian, Rocky Mountain College of Art & Design, Denver, Colorado.** Responsible for the daily operation, selection and acquisition of materials, formulation of policies for library operations, media center, and photography/slides archives. Designed and implemented library automation and delivery of electronic resources to college community.
- 1981-1985** **Development Officer, PRLC, Inc., Pittsburgh, Pennsylvania.** Served as senior member of corporate management team in strategic planning, development of proposals and contracts, implementation, and evaluation of new services, products, and programs for 100 institutional member organizations. Coordinated the development of proposals and contracts totaling \$4,000,000 annually. Provided creative leadership to corporate committees to solicit ideas, identify goals and objectives, plan, develop, present, and evaluate professional development opportunities.
- 1981** **Director of Library Development, Pennsylvania Department of Education, Harrisburg, Pennsylvania.** Responsible for statewide development, technical assistance, professional development, resource sharing, children's services, institutional library services, networking, and state aid program for all libraries throughout the Commonwealth. Functioned as liaison to Governor's Advisory Council, LSCA Advisory Council, District Administrators, private colleges, universities, consortia managers, and network directors. Supervised \$14,000,000 formula-based state aid program and \$3,000,000 grant awards to individual libraries, consortia, and networks.
- 1978-1981** **Assistant Director, Southern Tier Library System, Corning, New York.** Coordinated operation of system-wide programs (technical assistance, professional development, resource sharing, technical services, outreach) to 40 public libraries in 5 counties serving 500,000 residents. Solicited ideas, identified goals, sponsored, and evaluated professional development opportunities and technical assistance sessions.
- 1976-1978** **Division Librarian for Technical Services, Corpus Christi Public Libraries, Corpus Christi, Texas.** Provided leadership in acquisitions, cataloging, serials control, and processing for main library and 4 branches serving 250,000 residents. Participated as senior member of library management team. Compiled and prepared technical evaluations, reports, and statistical analyses of Division operations to measure the achievement and cost of annual goals, objectives, and staff performance.
- 1975-1976** **System Coordinator, San Antonio Major Resource Center, San Antonio, Texas.** Served as senior member of the management team for District X Office, charged to provide technical assistance, resource sharing, media services, and professional development to librarians and staff representing 30 public library jurisdictions in 21 counties serving 1,500,000 residents. Functioned as liaison to System Director, staff, and members of governing bodies with the System Board of Directors and the Texas State Library and Historical Commission. Prepared LSCA grant applications and monitored awards totaling \$1,100,000 annually.

- 1973-1975** **Bilingual Branch Librarian, San Antonio Public Library, San Antonio, Texas.** Worked as librarian providing reference, information, and readers' advisory services in branch serving 50,000 Spanish-speaking residents in southwest San Antonio. Participated in collection development and resource acquisition activities, specializing in children's work, Spanish language resources, and multicultural studies.
- 1972-1973** **Librarian, Holding Institute, Laredo, Texas.** Worked as high school librarian serving 500 boarding students in Spanish-speaking environment of private school. Provided reference, research assistance, and library instruction to students and 35 faculty members.
- 1966-1971** **Rockford Public Library, Rockford, Illinois.** Worked in branches as part-time as a Library Assistant, Clerk, and Page in city library serving 150,000 residents.

PUBLICATIONS

Editor-reviewed Monographs (Completed and in Progress)

- Hall-Ellis, Sylvia D., and Mary Beth Weber. *Contemporary Cataloging in an RDA Environment: A Handbook for Students and Practitioners*. Chicago, IL: American Library Association. Under contract & In development.
- RDA Testing: Lessons Learned and Challenges Revealed*. Sylvia D. Hall-Ellis and Robert O. Ellett, Jr., eds. Binghamton, N.Y.: Haworth, 2012. 128 p.
- Hall-Ellis, Sylvia D., Stacey L. Bowers, Christopher D. Hudson, and M. Claire Williamson. *Librarian's Handbook for Seeking, Writing, and Managing Grants*. Santa Barbara, Calif.: Libraries Unlimited, 2011. 315 p.
- Hall-Ellis, Sylvia D., with Ann Jerabek, and Merrie W. Valliant. *Contemporary Cataloging: A Handbook for Practitioners and Students*. Open access text. Athens, GA: University of Georgia System Regents, 2011. 767 p.
- Grealy, Deborah S. and Sylvia D. Hall-Ellis. *From Research to Practice: The Scholarship of Teaching and Learning in LIS Education*. Westport, Conn.: Libraries Unlimited, 2009. 175 p.
- Hall-Ellis, Sylvia D. with J. Ann Jerabek. *Grants for School Libraries*. Westport, Conn.: Libraries Unlimited, 2003. 197 p.
- Hall-Ellis, Sylvia D., Doris Meyer, Frank W. Hoffmann, with J. Ann Jerabek. *Grant Writing for Small Libraries and School Library Media Centers*. Boulder, Colo.: NetLibrary, 2001. 173 p.
- Hall-Ellis, Sylvia D., Doris Meyer, Frank W. Hoffmann, with J. Ann Jerabek. *Grant Writing for Small Libraries and School Library Media Centers*. Englewood, Colo.: Libraries Unlimited, 2000. 173 p.

Editor-reviewed Chapters (Completed and In Progress)

- Hall-Ellis, Sylvia D. "Prepared to Lead: Talent, Skills, and Competencies." In *Telling the Technical Services Story*. Chicago, IL: American Library Association, 2020. Program Presentation for Re-Accreditation by the American Library Association, School of Information, San Jose State University, 2022.
- Hall-Ellis, Sylvia D. "Grant Writing and Sponsored Research Funding for Academic Librarians." In *The New Librarianship*. Vol. 4. Bradford Lee Eden, ed. New York: Scarecrow Press, 2015. (pp. 163-174)
- Hall-Ellis, Sylvia D. "Organizing Information: Technical Services." In *Information Services Today: An Introduction*. Sandra Hirsch, ed. Lanham, Md.: Rowman and Littlefield, 2015. (pp. 139-148)
- Hall-Ellis, Sylvia D. "Metadata, MARC, and More." In *Rethinking Technical Services, Considering Our Profession and Ourselves: What's the Future of Our Profession?* Mary Beth Weber, ed. Lanham, Md.: Rowman and Littlefield, 2015. (pp. 29-55)
- Hall-Ellis, Sylvia D., ed. "Contingent Faculty: Non-Tenure Track Faculty Series." In the *Faculty Personnel Guidelines Relating to Appointment, Promotion, and Tenure*. November 2011. Denver, Colo.: University of Denver, 2011. 42 p.
- Hall-Ellis, Sylvia D., ed. "Standard VII: Information Resources." In the *Sturm College of Law Self-Study Presentation for Accreditation by the American Bar Association*. Denver, Colo.: University of Denver, Sturm College of Law, 2011. 20 p.

Hall-Ellis, Sylvia D. "Applying for Grants from Foundations, Corporations, or Government." In *The Volunteers' Guide to Fundraising: Raise Money for Your School Team, Library or Community Group*. 1st ed. Ilona M. Bray, ed. Berkeley, Calif.: Nolo, 2011. (pp. 1-38 on accompanying disc)

Hall-Ellis, Sylvia D., ed. "Standard III: The Faculty." In the *Library and Information Science Program Self-Study Document for Accreditation by the American Library Association*. Denver, Colo.: University of Denver, Morgridge College of Education, 2010. 22 p.

Hall-Ellis, Sylvia D. "Library and Information Science Programs and Education for Catalogers and Metadata Specialists: Challenges for the Twenty-first Century." In *Conversations with Catalogers in the Twenty-First Century*. Elaine R. Sanchez, ed. Santa Barbara, Calif.: ABC-CLIO, 2010. (pp. 226-254)

Hall-Ellis, Sylvia D., ed. "Standard III: The Faculty." In the *Library and Information Science Program Self-Study Document for Accreditation by the American Library Association*. Denver, Colo.: University of Denver, College of Education, 2003. 15 p.

Lesesne, Teri S. and Sylvia D. Hall-Ellis. "The Selection, Evaluation, and Integration of Culturally Authentic Texts: A Case for Making the Online Catalog Reflect Parallel Cultures." In *Literacy: Traditional, Cultural, Technological*. Pittsburgh, Pa.: International Association of School Librarianship, 1995. (pp. 110-113)

Lesesne, Teri S. and Sylvia D. Hall-Ellis. *The Selection, Evaluation, and Integration of Culturally Authentic Texts: A Case for Making the Online Catalog Reflect Parallel Cultures*. In *Conference Proceedings of the 23rd Annual International Association of School Librarianship*, Pittsburgh, Pennsylvania, July 17-22, 1994. ERIC Document ED374816. 17 p.

Hall-Ellis, Sylvia D. "Curriculum Folio for School Library Media Specialist Programs." In the *National Council for Accreditation of Teacher Education Self-Study for Sam Houston State University*. Huntsville, Tex.: Sam Houston State University, College of Education and Applied Science, 1994. 25 p.

Bruntjen, Scott and Sylvia D. Hall. "Attempting to Automate: Lessons Learned Over Five Years." In *Advances in Library Administration*. Volume 4. Weston, Conn.: JAI Press, 1985. (pp. 177-192)

Peer-Reviewed Journal Articles (Completed and In Progress)

Hall-Ellis-Sylvia D. "Job Design for Cataloging and Metadata Librarians." Submitted to *Journal of Library Administration*. In progress.

Hall-Ellis, Sylvia D. "The Relationship of Situational Leadership and the Dreyfus Model of Skill Acquisition for Supervisors in Cataloging and Metadata Services." To be submitted to *Library Resources and Technical Services*. In progress.

Hall-Ellis, Sylvia D. *The Relationship of Core Competencies on Learning Outcomes and Employers' Expectations for Catalog Librarians and Metadata Specialists*. To be submitted to the *Journal of Education for Library and Information Science*. In progress.

Hall-Ellis, Sylvia D. "Building Cataloger Competencies: The Dreyfus Model as a Prototype for the Education and Professional Development of Catalog Librarians and Metadata Specialists in Bibliographic Control." To be submitted to the *Cataloging & Classification Quarterly*. In progress.

Hall-Ellis, Sylvia D. "Descriptive Impressions of Entry-Level Cataloger and Metadata Specialists Positions, 2000-2016: Reflections and Trends." To be submitted to *Library Resources and Technical Services*. In progress.

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- Littauer, Marita, and Florence Littauer. *Enriquece tu Comunicación. Miami, Fla.: Editorial Unilit, 2008. 978-0-7899-1521-4, \$11.99 [*Críticas*, August 2008]*
- Martínez, Guillermo. *La Muerte Lenta de Luciana B.* New York: Rayo Planeta, 2008. 978-0-06-156551-9, \$14.95 [*Críticas*, May 2008]
- Matthews, Joseph R. *The Evaluation and Measurement of Library Services*. Westport, Conn.: Libraries Unlimited, 2007. 978-1-59158-532-9, \$50.00 [*Colorado Libraries*, April 2008]
- Gómez-Jurado, Juan. *A Masacre de Virginia Tech: Anatomía de una Mente Torturada*. Barcelona: Ediciones El Andén, 2007. 978-84-935789-4-7, €16.50 [*Críticas*, February, 2008]
- Matthews, Joseph R. *Library Assessment in Higher Education*. Westport, Conn.: Libraries Unlimited, 2007. 978-1-59158-531-2, \$45.00 [*Colorado Libraries*, February 2008]
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- Bardach, Ann Louise. *Cuba Confidential: Love and Vengeance in Miami and Havana*. New York: Random, 2002. 0-375-50489-3, \$25.95 [*Library Journal*, 2002]
- Swan, James. *Fundraising for Libraries: 25 Proven Ways to Get More Money for Your Library*. New York: Neal Schuman, 2002. 1-55570-433-6, \$69.95 [*Colorado Libraries*, 2002]
- Puig de Lange, Victoria. *Sol Con Agua*. Nashville, Tenn.: Editorial Vistazo/Ediciones Reio Negro, 2002. 0-9724506-0-2, \$17.75 [*Críticas*, 2002]
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- Vargas Lizano, Isabel. *Y Si Quieres Saber de Mi Pasado*. Con la colaboración de J.C. Vales. Madrid: Santillana Ediciones Generales, S.L., 2002. 84-03-09278-4, \$18.95 [*Críticas*, 2002]
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Cooper, Gail and Garry Cooper. *New Virtual Field Trips.* Englewood, Colo.: Libraries Unlimited, 2001. 1-56308-887-8, \$27.50 [*Colorado Libraries*, 2001]

NATIONAL SERVICE & PROFESSIONAL AFFILIATIONS

American Library Association, Life Member

Association for Library Collections & Technical Services (now CORE)
Cataloging, Classification, and Metadata Section
ALCTS Editorial Board, Member, 2015-2019
Committee on Cataloging: Description and Access, Member, 2008-2012
Test Site for RDA, Manager, 2009-2011
Nominating Committee, Member, 2007-2008
Committee for Education and Training of Catalogers, Chair, 2006-2007, Member, 2003-2007
Competencies & Education for a Career in Cataloging Interest Group, Chair, 2010-2012; Member, 2010-
President's Program Committee, 2015-2016
Education Committee, Member, 2005-2007
Task Force on Competencies and Education for a Career in Cataloging, Chair, 2007-2009
2007 Annual Meeting Pre-conference, "What They Don't Teach in Library School: Competencies,
Education and Employer Expectations for a Career in Cataloging," Steering Committee Chair
Fundraising Committee, Member, 2004-2006
Office of Diversity
Committee on Diversity, Chair, 2010-2011
Diversity Research Advisory Committee, Member, 2009-2010
Spectrum Scholar Mentor, 2009
Diversity Grants Review Committee, Member, 2007, 2010, 2012
Office of Statistics and Research
Research and Statistics Committee, Member, 2005-2007; Intern, 2003-2005
Library Research Round Table
Nominating Committee, 2022-2023
Membership Committee, 2019-2021
Board of Directors, Member At-Large, 2009-2012
Office of Accreditation
Accreditation Panel Member (training completed 2004)
Accreditation Review Panel Member (training completed 2004)

REFORMA, Life Member

National Board of Directors, 2005-2013
National Fundraising Chair, 2005-2013
National Recruiting and Mentoring Committee, 2008-2010
Colorado Chapter, Secretary, 2004-2005
Colorado Chapter Liaison to National Board of Directors, 2004-2013

American Association of Law Libraries (AALL), Life Member Online Audiovisual Catalogers Association (OLAC) Colorado Association of Law Librarians (CoALL)

American Association of University Women Association for Library and Information Science Education (ALISE)

University of Denver ALISE Representative, 2003-2008; 2010-2011
Membership Advisory Committee, 2007-2010
Technical Services Education Special Interest Group, 2003-
Garfield Doctoral Dissertation Award Reviewer, 2012
Garfield Doctoral Dissertation Scholarship Reviewer, 2014

American Association of University Professors (AAUP), 2006-

American Grant Writers Association, 2014- Grant Professionals Institute, 2016- National Grants Management Association, 2014-

Grant Reviewer (National and Regional Team Leader), U.S. Department of Education, 1998- Grant Reviewer, Broadband Technologies Opportunity Program, U.S. Department of Commerce, 2009
Grant Reviewer, Institute of Museum and Library Services, 1998-2000
Grant Reviewer, Colorado Department of Education, 2014-
Grant Reviewer, Colorado State Library, 1998-
Grant Reviewer, American Association of Community Colleges *Working Connections* program, 1999
Peer Reviewer, *Journal for Library and Information Science Education*, 2005-
Peer Reviewer, *Journal of Library Metadata*, 2009
Peer Reviewer, *International Journal of Library and Information Science*, 2011
Regular Columnist, *The Bottom Line*, 2013-2016
Book Reviewer, *Library Journal*, 2001
Book Reviewer, *Críticas*, 2002-2009
Book Reviewer, *Colorado Libraries*, 2000-2012

REGIONAL SERVICE & PROFESSIONAL AFFILIATIONS

Mountain Plains Library Association

Professional Development Grants Committee, Member, 2005-2006
Professional Development Policy and Guidelines Sub-committee Chair, 2006

Colorado Association of Libraries

"Student Voices" Column Editor, *Colorado Libraries*, 2005-2006
Conference Planning Committee, Member, 2002
Technical Services and Automation Division, Chair, 2002-2003; Member, 2000-
Academic Libraries Division, Peer Review Conference Papers Committee, Member, 2007-2009
Education Committee, Member, 1988-1993
Diverse Populations Committee, Member, 2009-2013

SERVICE TO THE UNIVERSITY OF DENVER

Center for Teaching and Learning Faculty Advisory Board, 2007-2008; 2010-2012
Center for Community Engagement and Service Learning Advisory Board, 2007-2012
Faculty Senate
Executive Committee, 2008-2013
Nominations, Rules & Credentials Committee, Chair, 2008-2013; Member 2007-2013
Appointment, Promotion, and Tenure Revision Committee, 2010-2012
Grievance Policy Committee Member, 2007-2010
Law Library Director Search Committee Chair, 2012-2013
PROF Grant Review, College Representative to the University Review Team, 2006, 2008
Project Homeless Connect Evaluations, Principal Investigator, 2006-2009
University Technology Council, 2007-2009
University of Denver Hyde Interviews for Incoming Freshmen, 2003-2012

SERVICE TO THE MORGRIDGE COLLEGE OF EDUCATION

Appointment, Tenure & Review Committee
Member, voting, 2003-2005; 2007- 2009
Chair, Clinical Faculty Promotion & Tenure Policy Subcommittee, 2008-2009
Member, Community Engagement Subcommittee, 2007-2009
Member, Tenure Review Panel, 2003
Advancement and Alumni Relations Committee, Chair, 2003-2007; Member, 2002-2007
College Building Committee Member, 2004-2010

College of Education Student Association, Faculty Advisor, 2004-2007; 2009-2010
Faculty Senator, 2007-2013
Research and Scholarship Committee, Chair, 2008-2009; Member, 2002-2003, 2008-2009
Research and Grant Mentoring Committee, Chair, 2009-2010
Research Task Force Member, 2010-2012
Search Committee Member, Assistant Professor for Curriculum & Instruction, 2010-2011
Workload Task Force Member, 2010-2011

SERVICE TO THE LIBRARY & INFORMATION SCIENCE PROGRAM

Library and Information Science Student and Alumni Association, Faculty Advisor, 2002-2008
ALA Student Chapter, Faculty Advisor, 2005-2008
Beta Phi Mu Phi Chapter, Faculty Advisor, 2004-2014
Steering Committee Member, Accreditation by the American Library Association, 2001-2004
Search Committee Member, Associate Professor for LIS, 2006
Search Committee Chair, Assistant Professors for LIS, 2003, 2005, 2006, 2007
Search Committee Ex-Officio Member, Director for LIS, 2004

SERVICE TO SAM HOUSTON STATE UNIVERSITY

Rio Roundup: South Texas Literature Conference, Conference Coordinator, 1993
External Relations, Fund Raising, Grants Committee, Chair, 1993-1995
Advisory Council Committee, Chair, 1993-1995
Students, Admissions, and Advisement Committee, Chair, 1994
Institutional Effectiveness Committee, Member, 1993-1995

SERVICE TO THE COLLEGE OF EDUCATION AND APPLIED SCIENCE

Faculty Affairs Committee, Member, 1993-1995
Curriculum Committee, Member, 1993-1995
Continuing Education Committee, Member, 1993-1995

SERVICE TO THE COMMUNITY

French Teacher & Student Exchange with Laon, France, Monarch High School, Boulder Valley School District (Boulder, Colorado), 2017-
Denver/Boulder Games 2022, Board of Directors, Secretary-Treasurer, 2015-2018
United Way Campaign Committee, College of Education, 2006
Arapahoe County, Election Judge for the County Clerk and Recorder, 2000-2005
Arthritis Foundation, Rocky Mountain Chapter, Certified Educator & Trainer, 1999-2008
Bonfils Blood Center, Silver Level Donor, 2000-2016
Denver Museum of Natural History, Docent, 1992
Tech Prep of the Lower Rio Grande Valley, Inc. (Harlingen, Texas) Board of Directors, 1995-1997
Executive Committee, 1996-1997; Chair, Development Committee, 1995-1997; Chair, Fiscal Agency Committee, 1995-1996; Chair, Colleges and Universities Committee, 1996-1997
Gilpin County (Colorado) Public Library Board of Trustees, 1986-1989; Vice President, 1987-1989
City of Central (Colorado) Economic Development Committee, 1987-1989
Columbine Family Health Centers, Inc. (Nederland and Black Hawk, Colorado) Board of Directors, 1988-1989

CERTIFICATION

Permanent Public Librarian Certificate - Pennsylvania, New York, Texas
Westlaw Expert Witness, 2008-
Certified Grant Writer®, 2016-

AWARDS AND HONORS

Advanced Practitioner for Service Learning and Community Engagement, University of Denver, 2011
Platinum Star Alumnae, College of Information, Library Science & Technologies, University of North Texas, 2009
Commendation for Integration of Technologies in Teaching & Learning Environment, University of Denver, 2006
Outstanding Adjunct Faculty Member Award, College of Education, University of Denver, 2002
Beta Phi Mu, Pi, University of Pittsburgh, 1985
Alpha Lambda Sigma, University of North Texas, 1972
Albert Nelson Marquis Lifetime Achievement Award, Who's Who in America
Who's Who in American Women
Who's Who of Women Executives
Dictionary of International Biography
Who's Who in the East
Who's Who in the South and Southwest
Who's Who in the World
Who's Who of Online Professionals
Who's Who in Library and Information Science
2,000 Notable Women
Who's Who of Emerging Leaders
Who's Who in Professional and Executive Women
Who's Who in American Education
International Who's Who of Professional and Business Women
International Leaders in Achievement
International Educator of the Year
Who's Who in Finance and Industry
Who's Who in Finance and Business

Invited International and National Conference Presentations

Driscoll, Margaret, Christy Confetti Higgins, Scott Brown, and Sylvia D. Hall-Ellis. *A View from Within: Open House Tour of Three Canvas Core Courses*. Presentation to be delivered at the School of Information, San José State University Professional Development Seminar, San José, California, October 17, 2019.

Hall-Ellis, Sylvia D. *Invest in Me -- I'm Your Future: Succession Planning for Libraries*. Keynote presentation delivered at the ALCTS President's Symposium, Boston, Mass., January 8, 2016.

Seidel, Kent E. and Sylvia D. Hall-Ellis. *Making Grants Work for You: Strategies for Doctoral Students and Early Career Scholars*. Presentation delivered at the University Council for Educational Administration, Early Career Scholars Session, Indianapolis, Ind., November 9, 2013.

Hall-Ellis, Sylvia D. *So You Want to be a Manager; Leadership Skills and Competencies for Technical Services Managers and Administrators*. Presentation delivered at the 138th Annual Conference, American Library Association, Chicago, Ill., June 29, 2013.

Seidel, Kent E., Karen S. Riley, Lyndsay Agans, Susan Korach, and Sylvia D. Hall-Ellis. *Making Grants Work for You (Instead of Just Working for Grants)*. A panel discussion delivered at the University Council for Educational Administration, Early Career Scholars Session, Denver, Colo., November 17, 2012.

Hall-Ellis, Sylvia D. *After the Great TS Reorganization: The Westminster Law Library*. Presentation delivered at the 137th Annual Conference, American Library Association, Anaheim, Calif., June 23, 2012.

- Hall-Ellis, Sylvia D. *Conversations with Catalogers in the 21st Century*. A panel discussion sponsored by the ALCTS Competencies for a Career in Cataloging Interest Group, delivered at the 137th Annual Conference, American Library Association, Anaheim, Calif., June 22, 2012.
- Hall-Ellis, Sylvia D., moderator. *Mid-Career Leaders Program*. A panel discussion sponsored by the ALA Committee on Diversity delivered at the 136th Annual Conference, American Library Association, New Orleans, La., June 26, 2011.
- Hall-Ellis, Sylvia D., moderator. *Diversity Town Hall*. A community conversation sponsored by the ALA Committee on Diversity delivered at the 136th Annual Conference, American Library Association, New Orleans, La., June 24, 2011.
- LaBarre, Kathryn, Sylvia D. Hall-Ellis, Karen Anderson, Rick Hasenyager, Christopher Cronin, and Penny Baker. *Briefings from RDA Test Participants*. A panel discussion delivered at the Midwinter Conference, American Library Association, San Diego, Calif., January 7, 2011.
- Miksa, Shawne, Marjorie Bloss, and Sylvia D. Hall-Ellis. *Educating the Next Generation of Catalogers: Teaching RDA*. A panel discussion delivered at the 97th Annual Conference, Association for Library and Information Science Education, San Diego, Calif., January 7, 2011.
- Hall-Ellis, Sylvia D., Robert Maxwell, John Hostage, and George Prager. *RDA Panel: What Cataloging Managers Need to Know*. Presentation delivered at the 103rd Annual Conference, American Association of Law Librarians, Denver, Colo., July 12, 2010.
- Hall-Ellis, Sylvia D. and Stacey L. Bowers. *Catalogers in the RDA Environment: Skill Sets, Expectations and Challenges*. Presentation delivered at the 103rd Annual Conference, American Association of Law Librarians, Denver, Colo., July 11, 2010.
- Hall-Ellis, Sylvia D. *Comfortable in Your Cataloging and Metadata Specialist Skin? Or, So You Want to Hire a Cataloger*. Presentation delivered to the ALCTS Research Group at the 134th Annual Conference, American Library Association, Chicago, Ill., July 11, 2009.
- Perez, Megan, Sylvia D. Hall-Ellis, and Denise Anthony. *From Novice to Expert: Collaboration for Succession Planning*. A “hot topic” presentation delivered at the 14th ACRL Conference, Seattle, Wash., March 13, 2009.
- Hall-Ellis, Sylvia D. *Cataloging in the RDA Environment: Skill Sets, Expectations and Challenges*. Presentation delivered to the ALCTS Research and Publications Committee at the Midwinter Conference, American Library Association, Denver, Colo., January 24, 2009.
- Hall-Ellis, Sylvia D. *LIS Cataloging Education for the 21st Century: Expectations and Challenges*. A panel discussion held at the 95th Annual Conference, Association for Library and Information Science Education, Denver, Colo., January 23, 2009.
- Chu, Clara, Sylvia D. Hall-Ellis, and Mark Winston. *The Doctoral Degree & Building a Career*. A panel discussion delivered at the ALA Office of Diversity Spectrum Doctoral Fellows E.J. Josey Leadership Institute, Midwinter Conference, American Library Association, Denver, Colo., January 20, 2009.
- Hall-Ellis, Sylvia D. and Robert O. Ellett, Jr. *Fundamentals of Cataloging Course: An Overview of the ALCTS Online Course*. Presentation delivered to the ALCTS Big Heads Group, 133rd Annual Conference, American Library Association, Anaheim, Calif., June 30, 2008.

Hall-Ellis, Sylvia D. *Employers' Expectations for Technical Services Librarians: What We Don't Know.*

Presentation delivered to the ALCTS Research and Publications Committee Program, 133rd Annual Conference, American Library Association, Anaheim, Calif., June 28, 2008.

Hall-Ellis, Sylvia D., Virginia R. Maloney, and Mary Stansbury. *Institutional Responses to Engaged Scholarship: The Carnegie Foundation Engaged University Classification at Two Universities.* Presentation delivered to the 94th Annual Conference, Association for Library and Information Science Education, Philadelphia, Pa., January 11, 2008.

Hall-Ellis, Sylvia D. *Puzzles, Problems, and Predicaments.* Presentation delivered to the ALCTS Research Discussion Group, 132nd Annual Conference, American Library Association, Washington, D.C., June 23, 2007.

Hall-Ellis, Sylvia D. *Cataloging Education: A New Emphasis for the Library and Information Science Curriculum.* Presentation delivered to the ALCTS Pre-conference, 132nd Annual Conference, American Library Association, Washington, D.C., June 22, 2007. <http://www.loc.gov/catdir/cpsocareercat.html>

Ellett, Jr., Robert O. and Sylvia D. Hall-Ellis. *Copy Cataloging Done Smarter.* Presentation delivered to the International Conference on Interdisciplinary Information Sciences and Technologies (InSciT2006), October 25-28, 2006.

Hall-Ellis, Sylvia D. and Robert O. Ellett, Jr. *Cooperative Cataloging: Challenges and Opportunities for Defense Libraries.* Presentation delivered to the 1st Annual Conference of Defense Libraries, Spanish Ministry of Defense, Madrid, Spain, July 7, 2006.

Hall-Ellis, Sylvia D. *Cataloger Competencies: Do the Employers Require What the Professors Teach?* Presentation delivered to the ALCTS CCS Heads of Cataloging Discussion Group, 131st Annual Conference, American Library Association, New Orleans, La., June 26, 2006.

Grealy, Deborah S. and Sylvia D. Hall-Ellis. *From Research to Practice: The Scholarship of Teaching and Learning in LIS Education.* Presentation delivered to the at the 92nd Annual Conference, Association for Library and Information Science Education, San Antonio, Tex., January 18, 2006.

Hall-Ellis, Sylvia D. *Employers' Expectations for Entry-Level Catalogers: What Position Announcement Data Indicate.* Research paper delivered to the Technical Services Special Interests Group, 91st Annual Conference, Association for Library and Information Science Education, Boston, Mass., January 12, 2005.
<http://dlist.sir.arizona.edu/>

Hall-Ellis, Sylvia D. *Common Errors in MARC Records Prepared by LIS Students: What Does It Mean?* Research paper delivered to the ALCTS CCS Cataloging Norms Discussion Group, Mid-Winter Conference, 90th American Library Association, San Diego, Calif., January 10, 2004.

Hall-Ellis, Sylvia D. *Visual Arts as Foundation for Successful Library Automation: The Rocky Mountain College of Art & Design Experience.* Paper delivered at the 6th Annual Conference of Higher Education, Charleston, S. C., 1993.

Hall, Sylvia D. *Design Elements for Bibliographic Databases: An Overview.* Paper delivered at the 14th Online National Conference, New York, 1983.

Invited Regional Conference Presentations

- Hall-Ellis, Sylvia D., Hudson, Christopher D., Brittany Cronin, and Kathryn Michaels. "The Colorado Law Project: Meeting the Public's Need for Legal Information." Panel discussion delivered at the Mountain Plains Library Association Conference, Billings, Mont., April 9, 2011.
- Grealy, Deborah S. and Sylvia D. Hall-Ellis. *Education for Information Professionals in New Mexico: Library & Information Science Graduate Education at the University of Denver*. Presentation delivered at the New Mexico Library Education Summit, Las Vegas, N.M., September 26, 2005.
- Hall-Ellis, Sylvia D. *Public Library-School Library Partnerships*. Presentation delivered at the 3rd Annual Colorado Association of Libraries Conference with the Mountain Plains Library Association, Denver, Colo., October 22, 2004.
- Hall-Ellis, Sylvia D. *Learn All You Can – Educational Partnership Opportunities for the Lewis and Clark Bicentennial Commemoration*. Paper delivered at the 3rd Annual Lewis and Clark Bicentennial Council National Planning Conference, Bismarck, N.D., April 26, 1998.

Invited State Conference Presentations

- Grealy, Deborah S. and Sylvia D. Hall-Ellis. *Academic Library Leadership Changes: Using Succession Planning and Mentoring*. Presentation delivered at the Minnesota Library Education Conference, St. Cloud, Minn., October 10, 2013.
- Hall-Ellis, Sylvia D., Merrie Valliant, and Melissa Powell. *RDA: What Is It and What Do You Need To Do With It At Your Library?* Presentation delivered at the Colorado Library Consortium Spring Conference, Ft. Morgan, Colo., April 26, 2013.
- Hall-Ellis, Sylvia D. *Service Learning and the Library & Information Science Graduate Education at the University of Denver*. Presentation delivered at the 4th LEADS Scholars Orientation, Denver, Colo., August 5, 2009.
- Hall-Ellis, Sylvia D. *Service Learning: Enhancement to Library & Information Science Graduate Education at the University of Denver*. Presentation delivered at the 3rd LEADS Scholars Orientation, Denver, Colo., June 2008.
- Hall-Ellis, Sylvia D. *Law Librarianship: A Community Conversation*. Sponsored by the Colorado Association of Law Libraries. Paper delivered at the Colorado Supreme Court Library, Denver, Colo., May 14, 2008.
- Hall-Ellis, Sylvia D. *Opportunities and Challenges in Law Librarianship: A Community Conversation*. Presentation delivered at the Sturm College of Law, Denver, Colo., November 7, 2007.
- Ellis, Sylvia D. *Grant Writing Resources for Nursing Professionals*. Presentation delivered at the Presbyterian / St. Luke's Health One Medical Center 1st Annual Research Symposium, Denver, Colo., October 17, 2007.
- Hall-Ellis, Sylvia D. *Project Homeless Connect 4 Event Evaluation – Insights and Lessons Learned*. Presentation delivered at the Homelessness Research Symposium: What is DU Doing about Homelessness in Denver, Denver, Colo., September 14, 2007.
- Hall-Ellis, Sylvia D. *Service Learning and the Library & Information Science Graduate Education at the University of Denver*. Presentation delivered at the 2nd LEADS Scholars Orientation, Denver, Colo., August 10, 2007.

Hall-Ellis, Sylvia D. *Education for Information Professionals in a Digital Environment: Library & Information Science Graduate Education at the University of Denver*. Presentation delivered at the 15th Spring Mountains and Plains Parapros Conference, Denver, Colo., February 24, 2007.

Hall-Ellis, Sylvia D. *Public Library Service to Spanish-Speaking and Latino Residents in Denver: A Case Study*. Presentation delivered at the 4th Annual Colorado Association of Libraries Conference, Denver, Colo., November 10, 2005.

Hall-Ellis, Sylvia D. *Education for Information Professionals in a Digital Environment: Library & Information Science Graduate Education at the University of Denver*. Presentation delivered at the 14th Annual Mountains and Plains Parapros Conference, Aurora, Colo., July 29, 2005.

Hall-Ellis, Sylvia D. *Educational Opportunities: Library & Information Science Graduate Education at the University of Denver*. Presentation delivered at the 13th Annual Mountains and Plains Parapros Conference, Centennial, Colo., August 6, 2004.

Hall-Ellis, Sylvia D. *Library Education & Training: Focus on the West: An LIS Faculty Member's Personal Response*. Presentation delivered at the 1st Annual Colorado Association of Libraries Conference, Keystone, Colo., October 18, 2002.

Hall-Ellis, Sylvia D. *Grant Writing for School Librarians*. Presentation delivered at the 2002 Annual Colorado Education Media Association Conference, Colorado Springs, Colo., February 15, 2002.

Hall-Ellis, Sylvia D. *Grants – Opportunities for the Future*. Paper delivered at the Southeast Regional Accountability Annual Conference, Lamar, Colo., November 12, 1998.

Hall-Ellis, Sylvia D. *The Texas Library Connection and Interlibrary Loan: An Experiment in Resource Sharing*. Paper delivered at the Texas Computer Educators' Association Annual Conference, Austin, Tex., February 6, 1997.

Hall-Ellis, Sylvia D. *Finding Grant Sources on the Internet: A Guide for Librarians*. Paper delivered at the 2nd Annual Institute for School Library Personnel, Pharr-San Juan-Alamo North High School, Pharr, Tex., July 29, 1996.

Hall-Ellis, Sylvia D. *Mathematical and Logical Thinking: A Critical Intelligence*. Paper delivered at the 3rd Annual Paraprofessional Conference at the University of Texas - Pan American, Edinburg, Tex., March 8, 1996.

Hall-Ellis, Sylvia D. *Cataloging Trends and Issues: Update Session*. Paper delivered at the 1st Annual Institute for School Library Personnel, South Texas Community College, McAllen, Tex., July 19, 1995.

Hall-Ellis, Sylvia D. *Grant Writing: Tips and Encouragement for School Librarians*. Paper delivered at the 1st Annual Institute for School Library Personnel, South Texas Community College, McAllen, Tex., July 18 and 19, 1995.

Hall-Ellis, Sylvia D. *How to Become an Expert Grant Writer*. Paper delivered at the 3rd Annual High School Principals' Academy, South Padre Island, Port Isabel, Tex., June 19, 1995.

Texas Library Study: Results from Regions I and II. Paper delivered at the 3rd Annual Technology Conference, Texas A&M University, College Station, Tex., November 18, 1994.

Hall-Ellis, Sylvia D. *Academic Achievement and Middle School Students*. Paper delivered at the 8th Annual Young Adult Conference, Sam Houston State University, Huntsville, Tex., November 5, 1994.

Hall-Ellis, Sylvia D. *Multimedia Resources for Library Leaders*. Paper delivered at the Institute for Librarians in A Multicultural Environment, Sam Houston State University, Huntsville, Tex., June 10, 1994.

Hall-Ellis, Sylvia D. *Finding the Resource: Empowering the User, or, the Case for Curriculum Based Subject Access to Learning Resource Center Collections*. Paper delivered at the 81st Annual Texas Library Association Conference, Corpus Christi, Tex., April 12-16, 1994.

Hall-Ellis, Sylvia D. and William H. Pichette. *Sam Houston State University Makes Use of OCLC/AMIGOS Collection Analysis CD*. Paper delivered at the 81st Annual Texas Library Association Conference, Corpus Christi, Tex., April 12-16, 1994.

Hall, Sylvia D. *Funding and Library Development in Pennsylvania: A Symbiotic Relationship*. Paper delivered at the Annual Graduate Student Colloquia, University of Pittsburgh, School of Library and Information Science, 1982.

Hall, Sylvia D. *Leadership for Public Library Trustees*. Paper delivered for the Trustees Division, Pennsylvania Library Association Annual Conference, Lancaster, Penn., 1981.

Seminar and Professional Development Presentations

Taylor, Meredith, and Sylvia D. Hall-Ellis. *Talent Management and Succession Planning*. ALCTS eForum, held March 22, 2017.

Hirsh, Sandra, Heather O'Brien, Michelle Holschuh Simmons, Michael Krasulski, and Sylvia D. Hall-Ellis. *Information Services Today: An Introduction. Part 3: Information Services: Roles in the Digital Age*. Rowan and Littlefield in partnership with Library Journal webinar, recorded February 5, 2015.

Hall-Ellis, Sylvia D. and Jennifer Sweda. *Copy Cataloging in an RDA Environment*. ALCTS eForum, held May 14 and 15, 2013.

Hall-Ellis, Sylvia D. *Law Librarianship: A Community Conversation*. Sponsored by the Colorado Association of Law Libraries, presented at the Colorado Supreme Court Library, Denver, Colo., May 14, 2008.

Hall-Ellis, Sylvia D. and Beatrice Z. Gerrish. *Reading and Libraries: Recent Research in Reading*. Presentation at the Ricks Center for Gifted Education, Denver, Colo., March 4, 2008.

Hall-Ellis, Sylvia D. *Cataloger Competencies: Do the Employers Require What the Professors Teach?* Presentation for the School of Library and Information Science, San José State University, February 12, 2008.

Hall-Ellis, Sylvia D. and Robert O. Ellett, Jr. *Cooperative Cataloging: Rules, Tools, and Conventions for Building a Multi-institutional Catalog*. Sponsored for the Spanish Ministry of Defense, Madrid, Spain, July 10, 2006.

Hall-Ellis, Sylvia D. *Cash for Kids: Grant Writing Opportunities for Youth Services Librarians*. Sponsored by the Colorado Young Adult Librarians; presented at Bemis Memorial Library, Littleton, Colo., November 13, 2002.

Hall-Ellis, Sylvia D. *MARC Records and Authority Control: Planning for Bibliographic Database Migration*. Sponsored and held at the Douglas County Public Library, Castle Rock, Colo., May 28, 2002.

Grant Writing: A Refresher for Librarians. Sponsored by Library and Information Science Program, College of Education, University of Denver; presented at University Center at Chaparral, August 12, 2000.

Hall-Ellis, Sylvia D. *Shaking the Money Tree – Basic Grant Writing for Colorado Educators*. Sponsored by the Office of Educational Telecommunications of the Colorado Department of Education.

Pikes Peak Community College, Colorado Springs, Colo., November 16, 1998.

Pueblo School District 60, Pueblo, Colo., November 12, 1998.

University of Northern Colorado, Greeley, Colo., November 10, 1998.
United Technology Educational Partnership, Grand Junction, Colo., November 9, 1998.

Hall-Ellis, Sylvia D. *Cataloging Multimedia, Kits, Globes and Map Materials in USMARC*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., April 24, 1997 and December 12, 1996.

Hall-Ellis, Sylvia D. *New Standards for School Library Media Centers*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., April 15, 1997.

Hall-Ellis, Sylvia D. *The School Library Media Specialist in the 21st Century: Visions for the Future*. Sponsored and hosted by Pharr-San Juan-Alamo Independent School District, Pharr, Tex., April 4, 1997.

Hall-Ellis, Sylvia D. *Cataloging Sound Recordings and Audio Materials in USMARC*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., March 20, 1997 and November 21, 1996.

Hall-Ellis, Sylvia D. *Evaluating and Selecting CD-ROMS for School Library Media Collections*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., March 18, 1997.

Hall-Ellis, Sylvia D. *Cataloging Audiovisual Materials in USMARC*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., February 27, 1997, November 7, 1996 and October 24, 1996.

Hall-Ellis, Sylvia D. *Introduction to Dialog: Basic Searching Strategies*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., February 14, 1997.

Hall-Ellis, Sylvia D. *Cataloging Books in USMARC*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., January 30, 1997, October 10, 1996, September 26, 1996 and August 8, 1996.

Hall-Ellis, Sylvia D. *Advanced Internet Searching Techniques for Librarians*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., January 21, 1997.

Hall-Ellis, Sylvia D. *Texas Library Connection Full-Text Searching*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., December 13, 1996 and October 25, 1996.

Hall-Ellis, Sylvia D. *Developing Evaluation Strategies for Grants and Proposals*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., December 10, 1996.

Hall-Ellis, Sylvia D. *Developing Needs Assessment for Grants and Proposals*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., November 12, 1996.

Hall-Ellis, Sylvia D. *Texas Library Connection Union Catalog Searching*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., November 8, 1996 and September 6, 1996.

Hall-Ellis, Sylvia D. *Grant Resources on the Internet*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., October 23, 1996.

Hall-Ellis, Sylvia D. *Preparing a Response to the Telecommunications Infrastructure Fund Board: Needs Assessment, Professional Development Framework, and Evaluation Strategies*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., October 16, 1996.

Hall-Ellis, Sylvia D. *Texas Library Connection: Building the Districtwide Bibliographic Database*. Sponsored and hosted by Mercedes Independent School District, Mercedes, Tex., September 13, 1996 and August 8, 1996. Sponsored and hosted by Los Fresnos Consolidated Independent School District, Los Fresnos, Tex., August 12, 1996.

Hall-Ellis, Sylvia D. *School-to-Work and Special Education: An Inclusive Partnership for Success*. Sponsored and hosted by the Office of Special Education, Region One Education Service Center, Edinburg, Tex., September 11, 1996.

Hall-Ellis, Sylvia D. *Telecommunications Infrastructure Fund Board: An Overview of Funding for Secondary Schools*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., August 31, 1996.

Hall-Ellis, Sylvia D. *Cataloging Books, Multimedia, and Realia in USMARC*. Sponsored and hosted by Edinburg Consolidated Independent School District, Edinburg, Tex., August 6, 1996.

Hall-Ellis, Sylvia D. *Internet Resources for Grant Writers*. Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., April 20, 1996.

Hall-Ellis, Sylvia D. *Enhanced Grant Writing Skills for Mathematics Educators: Writing Skills for Campus Teams*. Sponsored and hosted by the Office of General Education, Region One Education Service Center, Edinburg, Tex., March 22, 1996.

Hall-Ellis, Sylvia D. *Internet Resources for Grant Writers*. Sponsored and hosted by the College of Education and Applied Science, Sam Houston State University, Huntsville, Tex., March 9, 1996.

Hall-Ellis, Sylvia D. *Grant Writing for Mathematics Educators: A Development Process for Campus Teams*. Sponsored and hosted by the Office of General Education, Region One Education Service Center, Edinburg, Tex., March 4, 1996.

Hall-Ellis, Sylvia D. *Shaking the Money Tree: Preparing Successful Technology Grant Applications*. Sponsored and hosted by the Office of Technology and Media Services, Region One Education Service Center, Edinburg, Tex., February 29, 1996 and April 29, 1996.

Hall-Ellis, Sylvia D. *District-wide Technology Planning: Technical Assistance for the Texas Education Agency Initiative*. Sponsored and hosted by the Office of Technology and Media, Region One Education Service Center, Edinburg, Tex., February 2, 1996.

Hall-Ellis, Sylvia D. *Enhanced Grant Writing Skills*. Sponsored and hosted by Pharr-San Juan-Alamo Independent School District, Pharr, Tex., January 27, 1996.

Hall-Ellis, Sylvia D. *United States Copyright Act of 1976, Video Transmissions, Computer Software and the Internet*. Sponsored and hosted by the Office of Technology and Media, Region One Education Service Center, Edinburg, Tex., January 24, 1996.

Hall-Ellis, Sylvia D. *The Grant Writing Development Process*. Sponsored and hosted by Pharr-San Juan-Alamo Independent School District, Pharr, Tex., January 20, 1996.

Hall-Ellis, Sylvia D. *MARC Cataloging of Materials for Library Media Centers*. Sponsored and hosted by the Office of Media Services, Region One Education Service Center for the Donna Independent School District, Donna, Tex., August 17, 1995.

Hall-Ellis, Sylvia D. *Classification*. Sponsored by AJ Seminars, Rockville, Maryland; presented at University Hilton Hotel, Houston, Tex., May 10, 1995.

Hall-Ellis, Sylvia D. *Library Technical Services*. Sponsored by AJ Seminars, Rockville, Maryland; presented at University Hilton Hotel, Houston, Tex., April 26, 1995.

Hall-Ellis, Sylvia D. *Grant Writing: An Introduction for Public School Administrators*. Sponsored and hosted by the Office of Administrative Services, Region One Education Service Center, Edinburg, Tex., April 19, 1995.

Hall-Ellis, Sylvia D. *The School Library Media Specialist in the 21st Century: Visions for the Future*. Sponsored and hosted by the United Independent School District, Laredo, Tex., March 31, 1995.

Hall-Ellis, Sylvia D. *Using USMARC*. Sponsored by AJ Seminars, Rockville, Maryland; presented at University Hilton Hotel, Houston, Tex., March 29, 1995.

Hall-Ellis, Sylvia D. *Library Media Center Policies and Guidelines: How to Prepare for School Board Adoption*. Sponsored and hosted by the Office of Technology and Media Services, La Joya Independent School District, La Joya, Tex., March 10, 1995.

Hall-Ellis, Sylvia D. *Developing District-wide Policies and Guidelines for Library Media Centers*. Sponsored and hosted by the Office of Technology and Media Services, La Joya Independent School District, La Joya, Tex., January 10, 1995.

Hall-Ellis, Sylvia D. *MARC Cataloging of Audiovisual Materials for Library Media Centers*. Sponsored and hosted by the Office of Library Media and Technology Services, Cypress-Fairbanks Independent School District, Houston, Tex., December 1, 1994.

Hall-Ellis, Sylvia D. *The School Library Media Specialist in the 21st Century: Visions for the Future*. Sponsored and hosted by United Independent School District, Laredo, Tex., October 14, 1994.

Hall-Ellis, Sylvia D. *The School Library Media Specialist in the 21st Century: Visions for the Future*. Sponsored and hosted by the Laredo Independent School District, Laredo, Tex., October 7, 1994.

Hall-Ellis, Sylvia D. *MARC Cataloging for Library Media Centers*. Sponsored by the Office of Library Media and Technology Services, Cypress-Fairbanks Independent School District, Houston, Tex., October 5, 1994.

Hall-Ellis, Sylvia D. *Jump to the Head of the Class: Undergraduate Library Resources Available at Sam Houston State University*. Sponsored by the Office of the Associate Vice President for Student Services, Sam Houston State University, Huntsville, Tex., October 4, 1994.

Hall-Ellis, Sylvia D. *CD-ROMs - 1994's Newest and the Best for Secondary Level Media Centers*. Sponsored and hosted by Clear Lake Independent School District, Houston, Tex., June 3, 1994.

Hall-Ellis, Sylvia D. *Introduction to Classification*. Sponsored by AJ Seminars, Rockville, Maryland; presented at Holiday Inn, Market Center, Dallas, Tex., May 18, 1994.

Hall-Ellis, Sylvia D. *Basic Descriptive Cataloging*. Sponsored by AJ Seminars, Rockville, Maryland; presented at University Hilton Hotel, Houston, Tex., May 4, 1994.

Hall-Ellis, Sylvia D. *Shaking the Money Tree - Part II: Writing Successful Grant Applications*. Sponsored by Donna Independent School District, Donna, Texas, and Region One Education Service Center Edinburg, Texas; presented at South Texas Community College Library, McAllen, Tex., April 29, 1994.

Hall-Ellis, Sylvia D. *Using MARC*. Sponsored by AJ Seminars, Rockville, Maryland; presented at Holiday Inn, Market Center, Dallas, Tex., April 6, 1994.

Hall-Ellis, Sylvia D. *Automated Authority Control*. Sponsored by AJ Seminars, Rockville, Maryland; presented at University Hilton Hotel, Houston, Tex., March 23, 1994.

Hall-Ellis, Sylvia D. *Automating the District School Library Media Centers: Choices and Opportunities*. Sponsored and hosted by the Office of Technology and Library Media Services, Fort Bend Independent School District, Sugar Land, Tex., March 4, 1994.

Hall-Ellis, Sylvia D. *Shaking the Money Tree - Part I: Preparing Successful Grant Applications*. Sponsored and hosted by the Office of Library Media Services, Donna Independent School District, Donna, Tex., February 4, 1994.

GRADUATE COURSES TAUGHT

San José State University, School of Library and Information Science

INFO 249 – Advanced Cataloging and Classification (Fall 2015, 2016; Summer 2016)
INFO 287 – Special Topics in Cataloging and Classification (Spring 2017, 2018, 2019, 2020, 2021, 2022, 2023; Fall 2020, 2021, 2022, 2023)
LIBR 248 – Beginning Cataloging and Classification (Summer 2002, 2003, 2004, 2005, 2006)
LIBR 249 – Advanced Cataloging and Classification (Summer 2003; Fall 2014; Summer 2015)

University of Denver, University College

Grant Writing Certificate Seminar for Non-Profit Organizations (Fall 2020, 2021; Spring 2021)

University of Denver, Morgridge College of Education HED

5991 – Grant Writing in Higher Education (Spring 2011)
LIS 4010 – Organization of Information (Fall 2002-2009; Winter 2005; Spring 2004-2006)
LIS 4020 – Professional Principles and Ethics (Summer 2000)
LIS 4040 – Management of Libraries and Information Centers (Fall 2010; Spring 2003, 2009 (DS); Winter 2005)
LIS 4070 – Cataloging and Classification (Winter 2008, 2009, 2010, 2011, 2012; Fall 2009 (DS)) LIS
4321 – Collection Management (Spring 2005)
LIS 4326 – LIS Research (Winter 2009 (DS); Spring 2009 (DS))
LIS 4350 – Adult Materials and Services (Summer 2006, 2009)
LIS 4379 – Social Sciences Resources (Spring 2009)
LIS 4400 – Cataloging and Classification (Spring 2000, 2001; Winter 2002-2009; Summer 2005, 2006 – course renumbered LIS 4070, September 2007)
LIS 4401 – Descriptive Cataloging (Winter 2001; Spring 2002, 2003, 2006-2009; Summer 2005)
LIS 4402 – Subject Cataloging (Spring 2001, 2009; Summer 2005, 2006, 2007, 2008)
LIS 4403 – Classification Schemes (Fall 2007, 2008, 2009 (DS)) LIS
LIS 4405 – Authority Control (Winter 2009)
LIS 4510 – Materials and Services for Children (Winter 2004; Summer 2005)
LIS 4620 – Grant Writing and Fundraising (Summer 2000, 2002, 2004, 2010; Winter 2006; Fall 2006-2009)
LIS 4700 – Seminar in Technical Services (Fall 2001)
LIS 4700 – Seminar in Public Libraries (Summer 2002)
LIS 4804 – Management of Electronic Records (Spring 2004; Fall 2005)
LIS 4902 – Capstone Projects (Winter 2003, Spring 2008, 2009, 2011)
LIS 4910 – Independent Study (every quarter Winter 2000 through Spring 2011)
LIS 4920 – Service Learning (every quarter Summer 2004 through Spring 2011)
RMS 4954 – Grant Writing (Summer 2013, 2014)
RMS 4959 – Content Analysis Methodology (Spring 2015)
QRM 4978 – Grant Writing (Summer 2011, 2012)

Rutgers University, School of Communication and Information

SC&I 522 – Cataloging and Classification (Summer 2013)

University of Arizona, College of Behavioral and Social Sciences

LIS 602 – Cataloging and Classification (Summer 1995)
LIS 612 – Advanced Online Search and Retrieval (Summer 1995)

Sam Houston State University, College of Education & Applied Science

LIS 532 - Cataloging and Classification (Fall 1993, 1994, 1995)
LIS 563 - Advanced Cataloging and Classification (Summer 1994)
LIS 567 - Research Methods (Spring 1994, Spring 1995)
LIS 591 - Educational Technology (Spring 1994, 1995)
LIS 596 - Networking and Computer Technologies in Education (Fall 1993, Summer 1994, Fall 1995)

Dissertations at the University of Denver

Bowers, Stacey L. *Library Anxiety of Law School Students: A Study Utilizing the Multidimensional Library Anxiety Scale*. Chair, May 5, 2010.

Fattor, Melissa M. *Student Engagement Differences by Ethnicity and Scale for Ninth Grade Students*. Chair, November 1, 2010.

Fulton, Roseanne. *A Case Study of Culturally Responsive Teaching in Middle School Mathematics*. Kent Seidel, Chair, June 18, 2009, Outside Chair.

Grealy, Deborah S. *Tribes and Territories in Library and Information Studies Education*. Bruce Uhrmacher, Chair, June 10, 2008, Committee Member.

McCord, J. Michael. *Developing a Standard of Care for Educational Malpractice*. Chair, April 15, 2011.

Priebe, Sarah J. *Distinguishing Effects of Domain and General Knowledge on Passage Fluency and Comprehension*. Jan Keenan, Chair. July 21, 2011, Outside Chair.

Snyder-Mondragon, Sandra M. *Institutional Factors that Impact the Retention of Graduate Students of Color in Schools of Library and Information Science: A Metaregression of Accredited Library School Statistics on Student Retention and Graduation Rates*. Kathy Green, Chair, July 24, 2009, Committee Member.

Taylor, Karen Pickles. *Effective Teaching*. Elinor Katz, Chair, July 15, 2009, Outside Chair.

Thompson, Jennifer. *Distinguishing a Western Women's College: A History of the Curriculum and Student Experience at Colorado Women's College*. Edith W. King, Chair, July 16, 2010, Committee Member.

Walker, Emelda. *Influence of Organizational Factors on Job Satisfaction of Disability Service Providers at Postsecondary Institutions*. Chair, April 29, 2010.

Dissertation Proposals at the University of Denver

Bowers, Stacey L. *Library Anxiety of Law School Students: A Study Utilizing the Multidimensional Library Anxiety Scale*. Chair, November 5, 2009.

McCord, J. Michael. *Developing a Standard of Care for Educational Malpractice*. Edith W. King, Chair. April 23, 2010.

Thompson, Jennifer. *History of Colorado Women's College*. Edith W. King, Chair, October 30, 2008. Committee Member.

Walker, Emelda. *Influence of Organizational Factors on Job Satisfaction of Disability Service Providers at Postsecondary Institutions*. Chair, July 21, 2009.

Dissertations at Other Institutions

Rodríguez-Mori, Howard. *The Information Behavior of Puerto Rican Immigrants to Central Florida, 2003-2009: Grounded Analysis of Six Case Studies Use of Social Networks during the Migration Process*. Kathleen Burnett, Chair, April 10, 2009, Florida State University, Committee Member.

Schwartz, Brian *More than a Look-up Skill: Medical Information Literacy Education in Osteopathic Medical Schools*. D. Mirah Dow, Chair, July 18, 2017. Emporia State University, Committee Member.

Snow, Karen. *A Study of the Perception of Cataloging Quality among Catalogers*. Shawne D. Miksa, Chair, August 1, 2011. University of North Texas, Committee Member.

Dissertation Proposals at Other Institutions

- Schwartz, Brian *More than a Look-up Skill: Medical Information Literacy Education in Osteopathic Medical Schools*. D. Mirah Dow, Chair, December 4, 2015. Emporia State University, Committee Member.
- Snow, Karen. *A Study of the Perception of Cataloging Quality among Catalogers*. Shawne D. Miksa, Chair, May 11, 2010. University of North Texas, Committee Member.

Master's Thesis at the University of Denver

- Hemingson, Jeff. *Recital Paper*. Lamont School of Music, February 2010, Outside Chair.

Capstones at the University of Denver

- Anthony, Alisa. *Correlation of Library and Information Science Program outcomes and Vacant Position Qualifications Listed on the Colorado State Library Jobline by Employers During the Period September 1, 2000 through August 31, 2002*. Chair, Winter Quarter, 2003.
- Borden, Donna M. *Improving Emergency Communications Systems: Is a Radio Communications Network the Answer?* Fall Quarter, 2014.
- Bowden, Heather L.M. *Exploring Biological Models for Long-term Data Preservation*. Chair, Spring Quarter, 2008.
- Casenada, Cassandra Y. *Challenges to the Recruitment, Education, and Retention of Librarians of Color*. Chair, Spring Quarter, 2008.
- Chang, Jennifer C. *Legal Research Practice and Preference: A Law Firm Perspective*. Chair, Spring Quarter 2011.
- Ellis, Megan S. Fitzgerald. *Design of a Public Library Adult Volunteer Recruitment Program and Training Curriculum*. Chair, Winter Quarter, 2003.
- Kircher, Kathy. *Development of a Library Pathfinder for Exobiology and Posting it on the Internet*. Chair, Winter Quarter, 2003.
- Melhado, Loretta. *Design of St. John's Episcopal Church Library*. Chair, Spring Quarter, 2008.
- Radcliff, Kathy. *Original Cataloging of Archival materials in the HERS Collection in Penrose Library*. Chair, Winter Quarter, 2003.
- Sass, Carol Ann. *ACT Periodical Index: Access to Catholic Thinking Periodical Index: Web Index to Select Catholic Periodicals*. Spring Quarter 2000.
- Stone, Sergio D. *Conducting Community Analysis for the Bemis Public Library (Littleton, Colorado) Using 2002 U.S. Census Data and the Online Outcome-Based Evaluation Toolkit*. Chair, Winter Quarter, 2003.
- Tureson, Tamara. *Design and Use of an Information Audit Tool for Use in a Law Library*. Chair, Winter Quarter, 2003.
- Tweed, Beth. *Evaluation of Email Reference Service in a Consumer Health Library Environment*. Chair, Winter Quarter, 2003.

GRANTS AND CONTRACTS

Student Learning in Agriculture STEM through Teacher Professional Development. Research team: Stanton Gartin (PI) and Cyndi Hofmeister, Northeast Junior College; Jeff Cash, Cheryl Sánchez, Anne-Marie Crampton, Lamar Community College; Suzanna Spears, Morgan Community College; Jack Wiley, Kerry Gabrielson, Trinidad State Junior College; Michael J. Miller, Colorado State University; Michael Womochil (Co-PI), Casey Sacks, and Sylvia D. Hall-Ellis, Colorado Community College System. U.S. Department of Agriculture, Agriculture and Food Research Initiative, Food, Agriculture, Natural Resources and Human Sciences Education and Literacy Initiative, \$404,460 (2017-2020)

Leading and Achieving: the Colorado Agriculture Regional Consortium. Research team: Jack Wiley (PI), Kerry Gabrielson, Trinidad State Junior College; Jeff Cash (PI), Cheryl Sánchez, Anne-Marie Crampton, Lamar Community College; Suzanna Spears, Morgan Community College; Cyndi Hofmeister, Northeast Junior College; Michael Womochil (Co-PI), Casey Sacks, and Sylvia D. Hall-Ellis, Colorado Community College System. U.S. Department of Agriculture, Hispanic Serving Institutions Education Grants Program, \$504,414 (2017-2020)

Cyber Prep Program Planning Grant. Research team: Debbie Sagen (PI), Brenda Lauer, Pikes Peak Community College; Gretchen Martin, Koiosa Insights; and, Sylvia D. Hall-Ellis, Colorado Community College System. U.S. Department of Commerce, Regional Alliances and Multi-stakeholder Partnerships to Stimulate (RAMPS) Cybersecurity Education and Workforce Development, \$199,681 (2016-2018)

Career and Technical Education in Colorado: Pathways to Education and Employment. Research team: Heather McKay (PI), Rutgers University; Sarah Heath, Casey Sacks, Sylvia D. Hall-Ellis, Colorado Community College System. U.S. Department of Education, Institute of Education Sciences, \$1,400,000 (2017-2021)

Pre-Alliance Planning Grant Colorado Community College Alliance. Research team: Victor Vialpondo (PI) and Janel Highfill, Community College of Aurora; Heidi Loshbaugh (Co-PI), Community College of Denver; Rick Reeves, Bill McGreevy, Liz Cox, and Kristin Aslin, Red Rocks Community College; Cathy Pellish, Front Range Community College; Samuel DeVries, Arapahoe Community College; Sylvia D. Hall-Ellis, Colorado Community College System. National Science Foundation, Louis Stokes Alliance for Minority Participation (LSAMP), \$86,817 (2016-2017)

Towards Scalable Differentiated Instruction Using Technology-enabled, Competency-based, Dynamic Scaffolding. Research team: Karen Wilcox (PI) and Vijay Kumar, Center for Computational Engineering, Massachusetts Institute of Technology; Flora McMartin, Broad-based Knowledge; Quinsigamond Community College; and, Casey Sacks, and Sylvia D. Hall-Ellis, Colorado Community College System. U.S. Department of Education, First in the World Developmental Grant, \$2,891,882 (2015-2019)

Colorado Strategic Partnerships Emergency Grant. Research team: Elise Lowe-Vaughn (PI), Amy Hodson, Celia Hardin, Barbara McBride, James Newby, Christopher Dewhurst, Nina Holland, Kate Anderson, MaryAnn Roe, Chrystalynn Chrystalynn, Elaine Edon, Mona Barnes, Tom Morgan, Rob Hanni, and Marie Valenzuela, Colorado Department of Labor and Employment; Steve Anton, Joelle Brouner, and, Katie Griego, Colorado Department of Human Services; Rebecca Holmes, Judith Martinez, and Jennifer Jirous, Colorado Department of Education; Emily Templin Lesh, Colorado Workforce Development Council; Cory Everett, Colorado Department of Regulatory Agencies; and, Casey Sacks and Sylvia D. Hall-Ellis, Colorado Community College System. U.S. Department of Labor, Strategic Partnerships Emergency Grant, \$5,000,000 (2015-2017)

CAEL Jump Start Program: Competency-Based Education. Research team: Jerry Migler (PI), Casey Sacks, Debra Cohn, Thomas Hartman, and Sylvia D. Hall-Ellis, Colorado Community College System; Matt Jamison, Front Range Community College; Mike Coste, Red Rocks Community College; Amanda Corum, Pueblo Community College; Janet Colvin, Pikes Peak Community College; and, MaryAnn Matheny, Community College of Denver. Council for Adult and Experiential Learning, \$15,000 (2015)

Summit on the Redesign of Developmental Education. Research team: Jerry Migler (PI), Casey Sacks, and Sylvia D. Hall-Ellis, Colorado Community College System; Chip Nava, Pueblo Community College; Kim Moultny, Arapahoe Community College; Debbie Ulibarri, Trinidad State Junior College; and, Kris Bernard, Front Range Community College. American Association of Community Colleges, \$15,000 (2015-2016)

Equity in Excellence at Colorado Community Colleges. Research team: Keith Howard (PI) and Sylvia D. Hall-Ellis, Colorado Community College System; Estela Mata Bensimon, Center for Urban Education, University of Southern California; and Kerry Gabrielson, Trinidad State Junior College. Colorado Department of Higher Education, Colorado Opportunity Scholarship Program, \$150,000 (2015-2016)

MBA High School of Business in Colorado. Research team: Laurie Urich (PI) and Sylvia D. Hall-Ellis, Colorado Community College System; Rudolph Sumpter and Beatrice Gerrish, Boulder Valley Schools; Keith Curry Lance, RSL Research Group. Colorado Department of Higher Education, Colorado Opportunity Scholarship Program, \$501,295 (2015-2016)

Fullbridge Program in Colorado. Research team: Keith Howard (PI) and Sylvia D. Hall-Ellis, Colorado Community College System; Suzanna Spears, Fort Morgan Community College; and, Cheryl Sánchez and Anne-Marie Compton, Lamar Community College. Colorado Department of Higher Education, Colorado Opportunity Scholarship Program, \$300,000 (2015-2017)

Colorado Community College System Alternative Credit Program. Research team: Jerry Migler (PI), Keith Howard, and Sylvia D. Hall-Ellis, Colorado Community College System. American Council on Education, \$13,000 (2015)

Internationalization in Higher Education. Researcher: Samuel D. Museus. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Internationalization, \$8,000 (2014-2015)

International Perspectives on Bilingual Education. Researcher: Sharolyn Pollard-Durodola. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Internationalization, \$3,700 (2014-2015)

Cultivating Culturally Relevant and Responsive Curriculum and Pedagogy in College. Researcher: Samuel Museus. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, iRise Grant, \$5,000 (2014-2015)

Project EMERGE (Educational Model for Evaluation and Replicability in Gifted Environments). Research team: Norma Hafenstein (PI) and Bruce Uhrmacher. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Lynde and Harry Bradley Foundation, \$235,000 (2014-2015)

Collecting Asian American Refugee Stories. Researcher: Samuel Museus. Technical reviewer for MCE: Sylvia D. Hall-Ellis. American Educational Research Association, Research Grant, \$5,000 (2014-2015)

Developing Expertise in Teaching K-5 Mathematics. Research team: Julie Sarama (PI) and Douglas H. Clements (Co-PI), in partnership with the School of Education at the University of Michigan. Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Science Foundation, \$130,344 (2013-2015)

Investigation of the Long-Term Outcomes for Special Education Students. Researcher: Antonio Olmos-Gallos. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Jefferson County School District, Office of Assessment, \$40,000 (2014)

Refugee Community Collaboration. Researcher: Vicki Tomlin (PI) in partnership with the African Community Center and Jewish Family Service. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Community Engagement and Service Learning, \$14,854 (2014-2015)

Access to Mathematics for All. Research team: Richard S. Kitchen (PI), Nicole M. Russell (Co-PI), and Terrence Blackman (Co-PI), Curriculum Studies and Teaching Program, Morgridge College of Education; Álvaro Árias (Co-PI, Department of Mathematics); and, James Gray (Co-PI), Department of Mathematics, Community College of Aurora. Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Science Foundation, The Robert Noyce Scholarship Program, Capacity Building Project, \$349,926 (2014-2016)

Cognitive Test Battery for Intellectual Disabilities. Research team: Karen Riley (PI), Lyndsay Agans, Jessica Lerner, and Karin Dittrick-Nathan in partnership with David Hessel (PI), The MIND Institute at the University of California – Davis, and Elizabeth Berry-Kravis, Rush University Medical Center. Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Institutes of Health, Outcome Measures for Use in Treatment Trials for Individuals with Intellectual and Developmental Disabilities (R01), \$2,499,996 (\$588,672 at DU) (2014- 2019)

Broadening Participation in Engineering among Women and Latino/as: A Longitudinal, Multi-Site Study. Researcher: Patton Garriott (PI) in partnership with the University of North Dakota and the University of Missouri. Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Science Foundation, HER Core Research, \$677,390 (\$69,992 at DU) (2014-2019)

Designing a Teacher Evaluation System to Improve Teacher Effectiveness for Culturally and Linguistically Diverse Learners. Research team: María del Carmen Salazar (PI), Jessica Lerner, and Kathy Green. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Professional Research Opportunities for Faculty, \$29,988 (2014-2016)

Developing a College-Going Culture in Latina/O Families: Exploring the Influence of Funds of Knowledge on Family Outreach Programs. Researcher: Judy Marquez Kiyama. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Professional Research Opportunities for Faculty, \$18,720 (2014-2016)

Assessment of Quality of Life in Neural Implantation Surgery for the Treatment of Parkinson's Disease. Researcher: Cynthia McRae. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Internationalization, \$3,967 (2014-2015)

Pura Vida: Cloud Forest, Curriculum and Cross-Cultural Study. Research team: Norma Hafenstein (PI) and Bruce Uhrmacher (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Internationalization, \$8,000 (2014-2015)

Online Course Development for Curriculum and Instruction. Researcher: Ruth Chao. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Teaching and Learning, \$3,000 (2014)

Online Course Development for Curriculum and Instruction. Researcher: María del Carmen Salazar. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Teaching and Learning, \$3,000 (2014)

Online Course Development for Curriculum and Instruction. Researcher: Jessica Lerner. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Teaching and Learning, \$3,000 (2014)

Online Course Development for Curriculum and Instruction. Researcher: Duan Zhang. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Teaching and Learning, \$3,000 (2014)

The Mathematics Education of African Americans, 1866 – 1954. Researcher: Nicole M. Russell. Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Academy of Education, Spencer Foundation Postdoctoral Fellowship, \$55,000 (2014-2016)

Early Childhood Care and Education Study. Research team: Carrie Germeroth (PI), Melissa Mincic, and Douglas H. Clements. Technical reviewer for MCE: Sylvia D. Hall-Ellis. State of North Dakota, Department of Public Instruction, \$73,500 (2013-2014)

Graduate Level Specialty in Addiction Counselor Training with Emphasis on Integration of Native American Specific Content. Research team: Ruth Chao (PI) and Michael J. Faragher (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. The Galena Foundation, \$289,732 (2013-2016)

The Collecting Asian American and Pacific Islander Refugee Stories (CARS) Project. Researcher: Samuel Museus. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Community Engagement and Service Learning, \$15,000 (2014)

Parents in Transition: A Multiple Case Study of Parent and Family Orientation Programs. Researcher: Judy Marquéz Kiyama. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Faculty Research Fund, \$1,500 (2014-2015)

The Sistah Network: Black Women Graduate Students Supporting and Retaining Each Other. Researcher: Nicole M. Russell. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Faculty Research Fund, \$2,708 (2014-2015)

Evaluation of the Northeast Denver Babies Ready for College Program. Research team: Carrie Germeroth (PI), Melissa Mincic, and Douglas H. Clements. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Mile High Montessori, \$9,922 (2013-2014)

Developing Teaching Expertise in K-5 Mathematics. Research team: Julie Sarama (PI) and Douglas Clements (University of Denver), in partnership with Timothy Boerst (PI), Meghan Shaughnessy, Deborah Ball, Hyman Bass (School of Education at the University of Michigan). Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Science Foundation, \$449,827 (\$130,344 at the University of Denver) (2013-2015)

Early Learning Care and Education Study Program Grant for the State of North Dakota. Research team: Carrie Germeroth (PI), Melissa Mincic, and Sheridan Green. Technical reviewer for MCE: Sylvia D. Hall-Ellis. State of North Dakota Department of Public Instruction, \$73,500 (2013-2014)

Local Professional Learning Community for School Leaders. Research team: Susan Korach (PI), Kristina Hesbol, and Rebecca McClure. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Education Development Center, \$10,950 (2013)

Healthy Eaters, Lifelong Movers 2: Implementing Evidence-Based School Environment, Policy, and Curricular Changes to Increase Opportunities for Healthy Eating and Physical Activity in Low Income, Rural Colorado. Research team: Elaine Berlansky, University of Colorado at Denver (PI), Nicholas Cutforth, University of Denver (Co-PI), and Allison Reeds. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Health Foundation, \$3,103,108 (2013-2017)

Hughes Rare Books Library Room Renovation in the Sturm College of Law. Project team: Patti H. Marks, Sylvia D. Hall-Ellis, and Leigh Elliott. Mabel T. Hughes Charitable Trust, \$34,000 (2013-2014)

The Promise Center Partnership with the Marsico Institute for Early Learning and Literacy and the City and County of Denver. Research team: Karen Riley (PI), Douglas H. Clements (Co-PI), and Sheridan Green. Technical reviewer for MCE: Sylvia D. Hall-Ellis. The Piton Foundation, \$223,468 (2013-2014)

Center of Excellence for Problem Gambling. Research team: Ruth Chao (PI) and J. Mike Faragher. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Department of Behavioral Health, \$68,021 (2012-2013)

United Way Implementation and Validation Review. Research team: Douglas H. Clements (PI), Amanda Moreno, and Sheridan Green. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Mile High United Way, \$19,737 (2013)

Math/Science Partnership in Rural Districts. Research team: Kristen Bunn (PI, Eagle County Schools), Paul Michalec (Co-PI), and Alegra Reiber. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Department of Education, Colorado's Mathematics and Science Partnership Program, \$750,000 (2013-2014)

Mathematics and Science Education of African Americans. Research team: Nicole Russell (PI), Sylvia D. Hall-Ellis, Steve Fisher (Penrose Library). Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Professional Research Opportunities for Faculty, \$29,994 (2013-2015)

Online Course Development for Curriculum and Instruction. Researcher: Nicole Russell. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Teaching and Learning, \$3,000 (2013)

Discourse and Opportunity: Undocumented Students and Higher Education Policy. Researcher: Ryan Gildersleeve. Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Academy of Education, Spencer Foundation Postdoctoral Fellowship, \$55,000 (2012-2014)

An Anthropological Study of the Latino Graduation Ceremony. Researcher: Ryan Gildersleeve. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Spencer Foundation, \$39,900 (2012-2013)

Fragile-X and Pharmaceutical Company: Clinical Trial of AFQ056. University of California – Davis Children's Hospital MIND Institute (Sacramento), Children's Hospital Denver, and Rush Children's Hospital at Rush University Medical Center (Chicago). Karen Riley, PI. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Novartis Pharmaceuticals Corporation, \$394,206 (2012-2014)

Project Engage, Phase 2, a DAPRA Grant in partnership with Total Immersion Systems, Inc., and Texas A&M University. Research team: Karen Riley (PI) and Lyndsay Agans (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. U.S. Department of Defense, \$60,000 (2011-2013)

International School Psychology Practicum Exchange. Researcher: Gloria L. Miller. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Community Engagement and Service Learning, \$14,951 (2012-2013)

Online Course Development for Curriculum and Instruction. Research team: Bruce Uhrmacher (PI) and Norma Hafenstein (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Teaching and Learning, \$18,193 (2012-2014)

Writers in the Schools. Research team: Karen Riley (PI) and Amanda Moreno (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Humanities, \$4,965 (2012-2013)

Learning Ecosystem Validation Grant. Research team: Karen Riley (PI), Lyndsay Agans, Kent Seidel, and Shimelis Assefa. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Bill & Melinda Gates Foundation, \$315,000 (2012-2013)

Project Words of Oral Reading and Language Development (WORLD). Research team: Jorge E. Gonzalez (PI), Texas A&M University; Laura Saenz (Co-PI), University of Texas – Pan American; and, Sharolyn Pollard-Durodola (Co-PI), University of Denver. Technical reviewer for MCE: Sylvia D. Hall-Ellis. U.S. Department of Education, Institute of Education Sciences, \$53,354 (2012-2015); award \$640,718, transfer from Texas A&M University

Increasing the Efficacy of an Early Mathematics Curriculum with Scaffolding Designed to Promote Self-Regulation. Research team: Douglas H. Clements (PI) and Julie Sarama (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. U.S. Department of Education, Institute of Education Sciences, \$1,445,315 (2008-2014); award \$4,541,975, transfer from University at Buffalo, The State University of New York

Using Rule Space and Poset-based Adaptive Testing Methodologies to Identify Ability Patterns in Early Mathematics and Create a Comprehensive Mathematics Ability Test. Research team: Douglas H. Clements (PI) and Julie Sarama (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Science Foundation, \$323,791 (2010-2014); award \$1,194,944, transfer from University at Buffalo, The State University of New York

Comprehensive Postdoctoral Training in Scientific Education Research. Researcher: Julie Sarama (PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. U.S. Department of Education, Institute of Education Sciences, \$133,458 (2010-2014); award \$613,353, transfer from University at Buffalo, The State University of New York

Longitudinal Study of a Successful Scaling Up Project: Extending TRIAD. Research team: Douglas H. Clements (PI), Julie Sarama (Co-PI), and Abt Associates (Carolyn Layzer, Fatih Unlu, Laurie Bozzi, Lily Fesler, Alina Martinez, Cristofer Price, James van Orden). Technical reviewer for MCE: Sylvia D. Hall-Ellis. Institute of Education Sciences, \$384,940 (2011-2015; award \$1,250,286, transfer from University at Buffalo, The State University of New York

Early Childhood Education in the Context of Mathematics, Science, and Literacy. Research team: Julie Sarama (PI), Douglas H. Clements (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Science Foundation, \$990,020 (2010-2014; award \$2,285,228, transfer from University at Buffalo, The State University of New York

Early Childhood Clearinghouse Information Center Redesign. Research team: Karen Riley (PI) and Amanda Moreno (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. Office of the Lt. Governor of Colorado, \$12,000 (2012-2013)

Morgridge Rural Educational Leadership Initiative. Research team: Lyndsay Agans (PI), Linda Brookhart (Co-PI), Susan Korach, and Rebecca McClure. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Morgridge Family Foundation, \$100,000 (2012-2014)

Center of Excellence for Problem Gambling. Research team: Patrick Sherry (PI) and J. Mike Faragher. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Department of Behavioral Health, \$55,000 (2012-2013)

Intermodal Transportation Institute Research Initiatives. Researcher: Patrick Sherry. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University Transportation Centers Program, Research and Innovative Technology Administration, U.S. Department of Transportation. \$600,000 (2012-2014)

Mile High United Way Social Innovation Fund Early Literacy Initiative. Gloria L. Miller, PI, Amanda Moreano, Kim Hartnett-Edwards, and Sheridan Green. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Mile High United Way, \$89,992 (2012-2013)

International School Psychology Practicum Exchange. Researcher: Gloria L. Miller. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Community Engagement and Service Learning, \$1,000 (2012-2013)

Refugee Student Art Outreach. Researcher: Karin Ditttrick-Nathan. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Faculty Research Fund, \$3,000 (2012-2013)

Resistance, Resilience, and Reciprocity: Centering the Voices of Black Doctoral Women with Faculty Aspirations. Researcher: Nicole M. Russell. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Faculty Research Fund, \$2,965 (2012-2013)

Assessing Learning through Student Notebooks. Research team: Keith Miller, Nancy Sasaki, and Kathy Green.

Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Professional Research Opportunities for Faculty, \$30,000 (2012-2014)

International School Psychology Practicum Exchange. Researcher: Gloria L. Miller. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Internationalization, \$2,000 (2012-2013)

ELO in Colorado. Research team: Cynthia Hazel and Duan Zhang. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Legacy Foundation, \$150,000 (2012-2013)

Creating Online LIS Courses. Research team: Mary C. Stansbury (PI), Shimelis Assefa, Denise Anthony, Xiao Hu, and Krystyna Matusiak. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Teaching and Learning, \$15,000 (2011-2013)

Maritime Piracy Seminar. Researcher: Ved Nanda, The Nanda Center, Sturm College of Law. Technical reviewer for Sturm College of Law: Sylvia D. Hall-Ellis. Arsenault Family Foundation, \$15,000 (2012-2013).

Early Childhood Librarianship: An Interdisciplinary, Experiential Learning MLIS. Researcher: Mary C. Stansbury (PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. Laura Bush's 21st Century Librarians Program, Institute for Museums and Library Services, \$249,066 (2012-2014)

Learning Ecosystem Planning Grant. Research team: Karen Riley (PI), Lyndsay Agans, Kent Seidel, and Shimelis Assefa. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Bill & Melinda Gates Foundation, \$281,217 (2011-2012)

Advanced Service Learning Practitioner Faculty Grant, Sylvia D. Hall-Ellis, University of Denver, Center for Community Engagement and Service Learning, \$400 (2011)

Evaluating and Enhancing the EspeciallyMe Program. Research team: Lori D. Patton and Nicole Russell. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Community Engagement and Service Learning, Public Good Fellowship Grant, \$24,780 (2012)

Choosing Excellence: Let Every Child Bloom. Research team: Shimelis Assefa (PI) and Mary C. Stansbury (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Community Engagement and Service Learning, Public Good Grant, \$7,657 (2012)

K-8 STEM Content Specific Professional Development to Improve Elementary Student Achievement. Research team: Kent Seidel (PI), Nicole Russell (Co-PI), Kimberly Hartnett-Edwards, Paul Michalec, Jeff Farmer, Keith Miller, Alegra Reiber, and Nancy Sasaki. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Department of Education, Improving Teacher Quality Grant, (Title II ESEA), \$307,299 (2011-2012)

Building a Better Principal Pipeline to Boost Student Achievement. Researcher: Susan Korach. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Denver Public Schools; a subcontract from the Wallace Foundation Grant, \$170,000 (2011-2017)

Center of Excellence for Problem Gambling. Research team: J. Mike Faragher (Co-PI) and Bobbie Vollmer (PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Department of Behavioral Health, \$79,999 (2011-2012)

An Exploration of Novice Teachers' Core Competencies: Impacts on Student Achievement, and Effectiveness of Preparation. Research team: Kent Seidel (PI), Kathy Green (Co-PI), Kimberly Hartnett-Edwards, and Duan Zhang. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Institute of Education Sciences, Effective Teachers and Effective Teaching, \$990,987 (2012-2015)

Project Engage, a DAPRA Grant in partnership with Total Immersion Systems, Inc., and Texas A&M University.

Research team: Karen Riley (PI) and Lyndsay Agans (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. U.S. Department of Defense, \$49,964 (2011-2014)

User-centered Evaluation of Music Search Engines. Researcher: Xiao Hu. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Faculty Research Fund, \$2,931 (2011-2012)

Educational Practicum in Vietnam and China to Promote the Inclusion of Young Children with Disabilities.

Researcher: Gloria L. Miller. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Internationalization, \$5,000 (2011-2012)

Evaluation of Colorado's Enhancing Quality in Infant-Toddler (EQIT) Initiative. Research team: Virginia R.

Maloney and Amanda Moreno. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Buell Foundation, \$395,884 (2011-2013)

Creating Engaging Environments to Teach Pre-Algebra Mathematics to Elementary Students. Research team:

Álvaro Arias, Mario López, María del Carmen Salazar, and Lyndsay Agans. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver Interdisciplinary Grant, \$60,000 (2011-2012)

Morgridge Education Technology Accessible (META) Resource Project. Research team: Lyndsay Agans (PI) and

Shimelis Assefa (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. Morgridge Family Foundation, \$36,000 (2011)

MCE Connect: A 21st Century Framework for Faculty Development. Research team: Bruce Uhrmacher (PI),

Shimelis Assefa (Co-PI), Lyndsay Agans (Co-PI), Kimberly Hartnett-Edwards, Norma Hafenstein, Xiao Hu, Paul Michalec (Co-PI), María del Carmen Salazar (Co-PI), and Sandra Snyder-Mondragon. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Teaching and Learning, \$22,355 (2011-2012)

Parent Education and Parent Leadership and Advocacy. Research team: Virginia Maloney (PI) and Amanda

Moreno, Marsico Institute for Early Learning and Literacy. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Health Foundation, \$27,358 (2010-2011)

Intentional School Culture. Researcher: Cynthia Hazel. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Denver Public Schools, \$38,040 (2010-2011)

Healthy Eaters, Lifelong Movers: Implementing Evidence-Based School Environment, Policy, and Curricular Changes to Increase Opportunities for Healthy Eating and Physical Activity in Low Income, Rural Colorado.

Research team: Elaine Berlansky, University of Colorado at Denver (PI), Nicholas Cutforth, University of Denver (Co-PI), and Allison Reeds. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Health Foundation, \$1,683,277 (2011-2014)

Second Life Learning Community. Research team: Don McCubbrey (PI), Sylvia D. Hall-Ellis (Co-PI), Walter

LaMendola, and Paul Novak. University of Denver, Center for Teaching and Learning, \$13,000 (2010-2011)

Reintroducing the Value of Law Librarians to Academic and Public Librarians in Colorado through the

Identification and Use of Emerging Technologies. Research team: Sylvia D. Hall-Ellis (Co-PI), Stacey L.

Bowers (PI), and Christopher Hudson, in partnership with Denver Public Library, Arapahoe Library District, and the Colorado State Supreme Court Library. University of Denver, Center for Community Engagement and Service Learning, \$5,773 (2010-11)

Reintroducing the Value of Law Librarians to Public Librarians through the Identification and Use of Emerging

Technologies and Resources. Research team: Stacey Bowers (PI) and Sylvia D. Hall-Ellis (Co-PI). American Association of Libraries, Wolters Kluwer Law & Business Grant Program, \$2,725 (2010-2011)

Faculty Service Learning Pod. Research team: María del Carmen Salazar and Nicholas Cutforth (Curriculum and Instruction Program), Frank Tuitt (Higher Education Program), Cynthia Hazel and Gloria Miller (Child, Family, and School Psychology Program), and Sylvia D. Hall-Ellis (Library and Information Science Program). University of Denver, Center for Community Engagement and Service Learning, \$8,000 (2010-2011)

Lincoln Collaborative. Research team: Antonio Esquibel (Principal, Lincoln High School), María del Carmen Salazar (Curriculum and Instruction Program), and Sylvia D. Hall-Ellis. School Improvement Grant, Denver Public Schools, \$375,000 (2010-2012)

Future LEADers of America: Leaders III. Research team: Denver Public Library (Kristen Svendsen, PI), the University of Denver (Sylvia D. Hall-Ellis), the Colorado Chapter of REFORMA (Orlando Archibeque), and the Colorado Association of Libraries (Martin Garner). Laura Bush's Recruiting Librarians for the 21st Century Program, Institute for Museums and Library Services, \$988,366 (2009-2012)

Teaching for Success in the Library Environment: LIS 4030 in Library 2.0. Research team: Deborah S. Grealy (PI) and Sylvia D. Hall-Ellis (Co-PI). University of Denver, Center for Teaching and Learning, \$ 9,350 (2009-10)

Writing Group Faculty Grant, Sylvia D. Hall-Ellis, University of Denver, Center for Community Engagement and Service Learning, \$750 (2008-2009)

Collaborative Learning Faculty Grant, Sylvia D. Hall-Ellis, University of Denver, Center for Teaching and Learning, \$1,500 (2008)

Connecting Information Literacy to Learning. Research team: Lori Micho, Merrie Valliant, Amanda Samland, and Sylvia D. Hall-Ellis. Colorado State Library, LSTA Discretionary Grant Program, \$19,548 (2008-2009)

Law Librarianship Fellows Program. Research team: Sylvia D. Hall-Ellis (PI), Stacey Bowers (Co-PI), and Christopher Hudson, Westminster Law Library. Laura Bush's 21st Century Librarians Program, Institute for Museums and Library Services, \$999,370 (2008-2012)

Grant Writing in a Cooperative Learning Environment. Sylvia D. Hall-Ellis. University of Denver, Center for Teaching and Learning, \$2,000 (2008-2009)

Project Homeless Connect 6 Event Evaluation. Research team: Sylvia D. Hall-Ellis and Duan Zhang. University of Denver Center for Community Engagement and Service Learning, \$9,785 (2008)

Project Ecuador: International Learning Service Libraries – A Faculty Development Experience in Ecuador. Sylvia D. Hall-Ellis, Office of Internationalization, University of Denver, \$600 (2007)

Project Ecuador: International Learning Service Libraries – A Faculty Development Experience in Ecuador. Sylvia D. Hall-Ellis, International Service Learning Office, University of Denver, \$400 (2007)

Project Homeless Connect 5 Event Evaluation. Research team: Sylvia D. Hall-Ellis and Duan Zhang. University of Denver Center for Community Engagement and Service Learning, \$1,000 (2007)

Project Homeless Connect 4 Event Evaluation. Research team: Sylvia D. Hall-Ellis and Duan Zhang. University of Denver Center for Community Engagement and Service Learning, \$4,595 (2007)

Future LEADers of America: Leaders II. Research team: Denver Public Library (Kristen Svendsen, PI), the University of Denver (Sylvia D. Hall-Ellis), and the Colorado Chapter of REFORMA (Orlando Archibeque). Laura Bush's Recruiting Librarians for the 21st Century Program, Institute for Museums and Library Services, \$988,518 (2007-2010)

Strategic Planning Assistance for the Denver Medical Library. Sylvia D. Hall-Ellis. Denver Medical Library, Inc., \$30,000 (2006-2007)

Destiny Software for JMAC Student Lab. Sylvia D. Hall-Ellis, gift from the Sagebrush Corporation, Minneapolis, Minnesota, \$10,000 (2006)

Libraries: Tools for Education and Development Worldwide: A Faculty Development Experience in France. Sylvia D. Hall-Ellis, Office of Internationalization, University of Denver, \$800 (2005)

Denver Public Library: Opportunities for Change. Sylvia D. Hall-Ellis, Colorado Community Based Research Network, \$2,000 (2005)

Future LEADers of America. Research team: Denver Public Library (Letty Icolari and Steve Taylor, PIs), Emporia State University (Jim Agee), and the University of Denver (Sylvia D. Hall-Ellis). Recruiting Librarians for the 21st Century Program, Institute for Museums and Library Services, \$670,315 (2005-2008)

American Association of University Professors Summer Institute Professional Development Grant. Sylvia D. Hall-Ellis, American Association of University Professors, \$300 (2005)

Beta Phi Mu Alumni Tea. Sylvia D. Hall-Ellis, gift from the Office of Alumni and Parent and Relations, University of Denver, \$2,000 (2005)

Spectrum Software for LIS Student Lab. Sylvia D. Hall-Ellis, gift from the Sagebrush Corporation, Minneapolis, Minnesota, \$5,000 (2005)

Developing Research Capacity in Community Organizations and Residents through Training and Technical Assistance. Nicholas J. Cutforth (PI) and Sylvia D. Hall-Ellis. Piton Foundation, \$25,000 (2005-2006)

Libraries: Tools for Education and Development Worldwide: A Faculty Development Experience in Argentina. Sylvia D. Hall-Ellis, Office of Internationalization, University of Denver, \$500 (2004)

Developing Research Capacity in Community Organizations and Residents through Training and Technical Assistance. Research team: Nicholas J. Cutforth (PI), Gary Lichtenstein and Sylvia D. Hall-Ellis, Piton Foundation, \$25,000 (2003-2004)

Increasing Spanish-Speaking and Hispanic Diversity among Library and Information Science Students at the University of Denver: Development of a Student Recruitment Model. Researcher: Sylvia D. Hall-Ellis (PI), Office of Multicultural Excellence, University of Denver, \$2,750 (2003-2004)

Collection Development Enrichment to Support the Cataloging & Classification Specialization and School Librarianship within the Library & Information Science Program at the University of Denver. Research team: Sylvia D. Hall-Ellis (PI) and Deborah S. Grealy. Women's Library Association, University of Denver, \$4,000 (2003)

Collection Development Enrichment to Support the Library & Information Science Program at the University of Denver. Research team: Deborah S. Grealy (PI) and Sylvia D. Hall-Ellis. Women's Library Association, University of Denver, \$4,000 (2001)

Wireless LAN for Library Education. Research team: Deborah S. Grealy (PI) and Sylvia Hall-Ellis. University of Denver, Center for Teaching and Learning, \$24,000 (2001-2002)

Upward Bound – A Program for South Texas Youth. Research team: Monte Churchill, Executive Director of Community Relations; Gary R. Saucedo, Outreach Coordinator; Raymond Hernandez, (PI) Associate Dean for Student Success; and Sylvia D. Hall-Ellis, South Texas Community College (McAllen, Texas). U.S. Department of Education, Office of Postsecondary Education, \$2,672,003 (1999-2003)

Write Now! Improving Elementary Students' Writing Skills. Research team: Caryl G. Thomason, Assistant Superintendent (PI); Karen Tankersley, Principal; and, Hal Anderson, Director of Technology, Cheyenne Mountain School District 12 (Colorado Springs, Colorado); and Sylvia D. Hall-Ellis. Colorado Department of Education, Educational Telecommunications Unit, \$189,453 (1999-2001)

Operation Quick Start -- Distance Learning in Rural Colorado. Research team: Randal Weigum, Technology Coordinator (PI); Bonnie Barns, Director of Federal Programs and Staff Development; and, Adam "Joe" Raskop, Executive Director, Southeastern Board of Cooperative Educational Services (Lamar, Colorado); and Sylvia D. Hall-Ellis. Colorado Department of Education, Educational Telecommunications Unit, \$400,000 (1999-2001)

Advanced Technological Training for Information Professionals for the 21st Century. Research team: Mario Reyna, Division of Business Director (PI) and Sylvia D. Hall-Ellis, South Texas Community College (McAllen, Texas). Phi Delta Kappa and the National Science Foundation, \$250,000 (1999-2001)

Working Connections – Training Information Technologies Professionals for the 21st Century. Research team: Mario Reyna, Division of Business Director (PI) and Sylvia D. Hall-Ellis, South Texas Community College (McAllen, Texas). Microsoft Corporation and the American Association of Community Colleges, \$1,147,775 (1999-2001)

The ROAD (Research Oriented Amplification of Development to Literacy) Program. Research team: Deborah J. Leong (PI), Metropolitan State University; Elena Bodrova, Metropolitan State University; Dmitri Semenov, Robert J. Marzano, and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). Hewlett-Packard Foundation, \$25,000 (1998-1999)

Press to Literacy. Research team: Deborah J. Leong (PI), Metropolitan State University; Elena Bodrova, Metropolitan State University; Dmitri Semenov, Robert J. Marzano, and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). The Denver Post and the Robert S. McCormick Foundation, \$49,818 (1998-1999)

International Telementor Center. Research team: David Neils, David B. Frost (PI), and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). Hewlett-Packard Philanthropy, \$100,000 (1998-1999)

America Reads: Providing Tutor Training for the America Reads Challenge. Research team: Louis F. Cicchinelli (PI) and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). U.S. Department of Education, Office of Educational Research and Improvement, \$306,000 (1998-1999)

Comprehensive School Reform. Research team: Louis F. Cicchinelli (PI), J. Timothy Waters, and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). U.S. Department of Education, Office of Educational Research and Improvement, \$285,000 (1998-1999)

Sustainable Energy Education (SEE) Program for Grades 4-8: Preparing Today's Youth for Lifelong Learning and Responsible Actions in Energy Conservation. Research team: Mary Gromko, Colorado Department of Education; Gene McCarthy, Rocky Flats Field Office, U.S. Department of Energy; Gina Kissell, National Renewable Energy Laboratory; and Barbara L. McCombs (PI), Janet L. Bishop, and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). State of Colorado Governor's Office for Energy Conservation, \$499,936 (1997-1999)

Review of Kansas Curriculum Standards in Mathematics and Language Arts. Research team: Robert J. Marzano (PI), John S. Kendall, David B. Frost, and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). Submitted to the Kansas State Department of Education, \$25,903 (1998)

International Telementor Center. Research team: David Neils, John Kuglin, Chris Rapp, David B. Frost (PI), and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). Hewlett-Packard Company, \$54,752 (1998)

Genesis Mission: Education Public Outreach. Developed in partnership by the Jet Propulsion Laboratory, California Institute of Technology, Los Alamos National Laboratory, Lockheed Martin Astronautics, and the Mid-continent Regional Educational Laboratory (Aurora, Colorado). Research team: John T. Sutton (PI), Alice Krueger, Martha Henry, Greg Rawls, Shae Isaacs, Jeff Johnson, Deb Jordan, Arlene Mitchell, David B. Frost, Jana Caldwell, J. Timothy Waters, and Sylvia D. Hall-Ellis. National Aeronautics and Space Administration, \$139,700,000; subcontract award, \$4,750,000 (1997-2007)

North Dakota Mathematics Assessment Project. Developed in partnership by the North Dakota Department of Education and Mid-continent Regional Educational Laboratory (Mid-continent Regional Educational Laboratory). Research team: Ann Clapper, Clarence Bina, Greg Gallagher, North Dakota Department of Education; Don Burger (PI), Hillary Michaels, and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). U.S. Office of Education, \$1,618,214; subcontract award, \$389,076 (1997-2001)

Pacific Resources for Education and Learning Distance Education: Project Evaluation. Developed in partnership by the Pacific Educational Community, the Pacific Resources for Education and Learning (PREL), and Mid-continent Regional Educational Laboratory (McREL). Research team: John W. Kofel (PI), Executive Director, PREL; J. Timothy Waters, Executive Director; Joan Buttram, Robert Keller, and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). U.S. Office of Education, Star Schools Program, \$10,000,000; subcontract award, \$500,000 (1997-2002)

Identification of Bilingual Gifted and Talented Children: A Comprehensive School Grants for Bilingual Education. Developed in partnership by Hidalgo (Texas) ISD, Los Fresnos (Texas) CISD, Progreso (Texas) ISD, University of Texas – Pan American (Edinburg, Texas), and Education Service Center, Region One (Edinburg, Texas). Research team: Hilda Medrano, Dean, College of Education, University of Texas – Pan American; Linda Phemister (PI), Janie Navarro, and Sylvia D. Hall-Ellis, Education Service Center, Region One. U.S. Department of Education, Office of Bilingual Education and Minority Languages Affairs, \$1,670,633 (1997-2002)

Academics 2000: First Things First -- The Texas Goals 2000. Developed for Jim Hogg (Hebbronville, Texas) County ISD, Mirando City (Texas) ISD, and San Isidro (Texas) ISD. Research team: Hilda Medrano, Dean, College of Education, University of Texas - Pan American (Edinburg, Texas); Angie Lehmann, Amy Mares, Ellen Gonzalez (PI), and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg, Texas). Texas Education Agency, \$339,987 (1997-2000)

Southwestern Bell's Learning Communities Initiative. Developed for Tech Prep of the Rio Grande Valley, Inc. (Harlingen, Texas); the Center for Professional Teacher Development, University of Texas – Brownsville; Teach for America – Rio Grande Valley (McAllen, Texas); and Education Service Center, Region One (Edinburg, Texas). Research team: Patricia G. Bubb, Executive Director (PI), Tech Prep of the Rio Grande Valley; Martin Winchester, Executive Director, Teach for America – Rio Grande Valley; Aileen Johnson, Director, School of Education, University of Texas – Brownsville; and Sylvia D. Hall-Ellis. Southwestern Bell Foundation, \$100,000 (1997-1998)

Texas School to Work: Regional Implementation. Developed for Tech Prep of the Rio Grande Valley, Inc. (Harlingen), South Texas Community College (McAllen), Texas State Technical College (Harlingen), Texas Southmost College (Brownsville), Empowerment Zone of the Rio Grande Valley (Mercedes), Project VIDA (Weslaco), Youth Fair Chance (McAllen), and Education Service Center, Region One (Edinburg). Research team: Patricia G. Bubbs (PI), Tech Prep of the Rio Grande Valley; Stephen Vassberg, Texas State Technical College; Ellen Trevino, Youth Fair Chance; Wanda Garza, Project VIDA; Leonardo Olivares, University of Texas – Pan American; Michael Bell, South Texas Community College; and Sylvia D. Hall-Ellis. Texas Workforce Commission, \$4,250,000 (1997-2002).

Comprehensive Bilingual Education Grant for Hidalgo ISD and Roma ISD. Developed for Hidalgo (Texas) ISD, Roma (Texas) ISD, College of Education, University of Texas – Pan American (Edinburg, Texas), and Education Service Center, Region One (Edinburg, Texas). Research team: Tomas Thomas (PI), Director, Office of Bilingual Education and Sylvia D. Hall-Ellis. U.S. Department of Education, Office of Bilingual Education and Minority Languages Affairs, \$1,531,361 (1997-2002)

Lopez High School, Porter High School, Rivera High School, Central Middle School, and Perkins Middle School, Brownsville (Texas) Independent School District. Telecommunications Infrastructure Fund Board, \$1,473,611 (1997-1998)

Donna High School, Todd Middle School, and Solis Middle School, Donna (Texas) Independent School District. Telecommunications Infrastructure Fund Board, \$704,052 (1997-1998)

Memorial Middle School and Nellie Schunior Middle School, La Joya Independent School District (Texas). Telecommunications Infrastructure Fund Board, \$293,641 (1997-1998)

Martin High School, Christen Middle School, Cigarroa Middle School, Lamar Middle School, Laredo (Texas) Independent School District. Telecommunications Infrastructure Fund Board, \$1,200,000 (1997-1998).

Lasara Middle School, Lasara (Texas) Independent School District. Telecommunications Infrastructure Fund Board, \$246,210 (1997-1998)

Los Fresnos High School and Resaca Middle School, Los Fresnos (Texas) Consolidated Independent School District. Telecommunications Infrastructure Fund Board, \$500,000 (1997-1998)

Lyford Junior High School, Lyford (Texas) Independent School District. Telecommunications Infrastructure Fund Board, \$354,997 (1997-1998)

Travis Middle School, McAllen (Texas) Independent School District. Telecommunications Infrastructure Fund Board, \$269,139 (1997-1998)

Mission High School, Mission (Texas) Independent School District. Telecommunications Infrastructure Fund Board, \$297,010 (1997-1998)

Progreso High School, Progreso (Texas) Independent School District. Telecommunications Infrastructure Fund Board, \$300,000 (1997-1998)

San Perlita High School, San Perlita (Texas) Independent School District. Telecommunications Infrastructure Fund Board, \$293,490 (1997-1998)

Myra Green Junior High School, Raymondville (Texas) Independent School District. Telecommunications Infrastructure Fund Board, \$225,000 (1997-1998)

Rio Grande City High School, Ringgold Middle School, Gruella Middle School, Rio Grande City (Texas) Independent School District. Telecommunications Infrastructure Fund Board, \$809,934 (1997-1998)

Rio Hondo Junior High School, Rio Hondo (Texas) Independent School District. Telecommunications Infrastructure Fund Board, \$297,024 (1997-1998)

Roma High School, Roma (Texas) Independent School District. Telecommunications Infrastructure Fund Board, \$333,178 (1997-1998)

San Benito High School, Miller Jordan Junior High School, San Benito (Texas) Consolidated Independent School District. Telecommunications Infrastructure Fund Board, \$547,000 (1997-1998)

Santa Maria High School and Santa Maria Middle School, Santa Maria (Texas) Independent School District. Telecommunications Infrastructure Fund Board, \$400,000 (1997-1998)

Salvador High School, United Independent School District (Laredo, Texas). Telecommunications Infrastructure Fund Board, \$250,879 (1997-1998)

Weslaco High School, Cabaza Middle School, Cuellar Middle School, Weslaco (Texas) Independent School District. Telecommunications Infrastructure Fund Board, \$874,242 (1997-1998)

Principals' Assessment and Training Center. Developed for Education Service Center, Region One (Edinburg, Texas). Research team: Roberto Zamora, Leonel Barrera, William H. Parry, and Sylvia D. Hall-Ellis. Texas Principals' Leadership Initiative, Texas Association of Secondary School Principals, Texas Association of Elementary School Principals, and the Sid Richardson Foundation. \$461,439 (1996-1998)

The Texas Library Connection -- Integrating and Sharing Resources. Developed for Hidalgo County Library System (McAllen), Cameron County Library System (Brownsville), South Texas Community College (McAllen), the University of Texas - Pan American (Edinburg), University of Texas - Brownsville, and Education Service Center, Region One (Edinburg). Research team: William R. McGee, Coordinator, Hidalgo County Library System; Joe Garcia, Director, Cameron County Library System; Michael D. Bell, Library Director, South Texas Community College; Eleanor Folger Foster, University Library, University of Texas - Pan American; Jaime Vela (PI), Director of Instructional Technology and Media Services, Ron Pontius, Instructional Technology, and Fabiola Fuentes, Media Services, Education Service Center, Region One; and Sylvia D. Hall-Ellis. Office of Library Media Services, Technology Services, Texas Education Agency. \$8,000 (1996-1997)

Developing Leadership Communities for Improving Algebra I for All Students. Developed for a partnership of the Region One Statewide Systemic Initiative Team. Research team: Noel Villarreal (PI), Eduardo Cancino, and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg). Texas Statewide Systemic Initiative for Reform in Mathematics, Science and Technology Education to The Charles A. Dana Center for Mathematics and Science Education, The University of Texas at Austin. \$25,000 (1996-1997)

Academics 2000: First Things First -- The Texas Goals 2000. Developed for Edinburg (Texas) CISD. Research team: Hilda Medrano, Dean, College of Education, University of Texas - Pan American (Edinburg); Helen Jones, Director (PI), Gifted and Talented Education, Edinburg CISD; and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg). Texas Education Agency, \$750,000 (1996-2001)

Texas Teachers Empowered for Achievement in Mathematics (TEXTEAM) Institute for Algebra I. Developed for Hidalgo ISD, Jim Hogg (Hebbronville) County ISD, La Joya ISD, La Villa ISD, Lyford ISD, Mission CISD, Pharr-San Juan-Alamo ISD, Rio Hondo ISD, San Isidro ISD, San Perlita ISD, Santa Maria ISD, Santa Rosa, Sharyland ISD, Valley View ISD, Webb (Laredo) CISD, Weslaco ISD, and Zapata County (Zapata) ISD. Research team: Noel Villarreal (PI), Chuck McInteer, Ellen M. Gonzalez, Education Service Center, Region One (Edinburg); and Sylvia D. Hall-Ellis. Charles A. Dana Center for Mathematics and Science Education, University of Texas - Austin, \$15,975 (1996)

Community Learning Center for La Villa, Texas. Developed for Edcouch-Elsa Independent School District. Research team: Noe Gonzalez (PI), Assistant Superintendent, Edcouch-Elsa Independent School District, and Sylvia D. Hall-Ellis. Delta Region Subzone, Rio Grande Valley (Texas) Rural Empowerment Zone, \$325,000 (1996-1997)

Monte Alto (Texas) Community Learning Center. Developed for Monte Alto Independent School District. Research team: Homero A. Diaz (PI), Superintendent, Monte Alto Independent School District, and Sylvia D. Hall-Ellis. Delta Region Subzone, Rio Grande Valley (Texas) Rural Empowerment Zone, \$300,000 (1996-1997)

Community Learning Center for La Villa, Texas. Developed for La Villa Independent School District. Research team: Sam Gonzalez (PI), Assistant Superintendent, La Villa Independent School District; and Sylvia D. Hall-Ellis. Delta Region Subzone, Rio Grande Valley (Texas) Rural Empowerment Zone, \$325,000 (1996-1997)

Building Project for Taylor Elementary. Developed for Mercedes (Texas) Independent School District. Research team: Mrs. Denise Rivera, Librarian, and Eduardo Infante, Principal, Taylor Elementary School; Ismael S. Cantu (PI), Federal Programs Director, Mercedes Independent School District; and Sylvia D. Hall-Ellis. Delta Region Subzone, Rio Grande Valley (Texas) Rural Empowerment Zone, \$375,000 (1996-1997)

Border Education Network (BEN) - Distance Education through Cable Television. Developed for Edinburg (Texas) Consolidated Independent School District. Research team: Noe Torres (PI), Library Media Specialist, Magdalena Rosas, Library Media and Technology Coordinator, Edinburg Consolidated Independent School District; and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg). Edinburg (Texas) Consolidated School District, \$250,000 (1996-1997)

Multiservice One-Stop Open Enrollment Charter School. Developed for the Information Referral Resource Assistance, Inc. (McAllen, Texas). Research team: Pablo Perez and Aguié Pena (PI), Executive Director, Information Referral Resource Assistance, Inc.; Roberto Zamora and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg). Texas Education Agency, \$3,066,000 (1996-2001)

Project OK: A Community Youth Opportunities Grant for Summer, 1996. Developed for McAllen (Texas) Independent School District, St. Joseph the Worker Catholic Church, and the Office of Adult Education, Education Service Center, Region One. Research team: Father Bart Flatt, St. Joseph the Worker Catholic Church; Noe Calvillo (PI), Office of Adult Education; Maria Louisa Garcia, McAllen Independent School District; and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg). Texas Protective and Regulatory Agency through the Office of the Mayor, City of McAllen, \$350,000 (1996-2001).

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Johnson & Wales University, Denver Campus, 2007-2009.
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Denver Medical Library, Inc., 2006-2010.
Bemis Public Library (Littleton), Ergonomic Design and Facilities Enhancement Consultant, 2003.
Curtis Park Community Center (Denver), Community Technology Center Evaluation and Proposal Development Consultant, 2003.
Colorado Community Based Research Network (Denver), Funding Research Associate, 2002.
Our Lady of the Rosary Academy (Edgewater), Learning Resource Center Development Project Consultant, 2001-2003
University of Southern Colorado (Pueblo). Technology Integration and Curriculum Enhancement into Higher Education Learning Environment. Proposal Development Consultant, 2000.
Jefferson County Library System (Lakewood), 1999-2000.
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ATTACHMENT 1



Power Supply Design Seminar

Design Review: 140W, Multiple Output High Density DC/DC Converter

Topic Categories:

Design Reviews – Full Power Supply
Specific Power Topologies
Push-Pull Power Stage

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Design Review: 140W, Multiple Output High Density DC/DC Converter

By Laszlo Balogh

ABSTRACT

This seminar topic reviews the most common solutions used in multiple output power supply designs. In the focus of the detailed design review is the current-fed push-pull converter, one of the most cost effective solution available for the practicing designer. A step-by-step design procedure will guide the reader through the most important decisions and their effect on the ultimate performance of the circuit. Measurement results, in particular cross-regulation data without using any post regulation technique concludes the topic.

INTRODUCTION

Designing multi-output converters presents a remarkable challenge for the power supply designer. There is no comparable power supply design task where specification, topology selection and the choice of output voltage regulation technique would have a more profound effect on the performance, cost and complexity of the final circuitry.

Converters utilizing a single primary power stage and generating more than one isolated output voltage are called multi-output converters. These circuits provide isolation and several output voltages using one high frequency isolation transformer as opposed to individual power modules for each output as it is frequently done in distributed power systems. The decreased system complexity of the multi-output approach is realized primarily on the account of output voltage regulation accuracy. Several approaches have been explored for multi-output converters to address complexity, overall efficiency, output voltage and cross-regulation issues. These circuit solutions can be divided into two radically different groups.

The first group of multi-output converters regulate their main output, from which the feedback signal is generated, with very good accuracy. Their auxiliary outputs are regulated with lesser accuracy

since they are not part of a closed loop regulation scheme. These solutions tend to be the most economical ones but their application can be limited because of their inadequate output voltage accuracy. The best known topologies of this category are the flyback, forward and current or voltage-fed push-pull converters.

The second circuit family provides a remedy for those applications where tight voltage regulation of **each** output is necessary. These approaches can be based on almost any topology since they are utilizing some sort of post regulation technique to regulate the auxiliary outputs of a multiple output converter. Accordingly, these solutions are differentiated by the post-regulation technique they are employing. Post regulation of the auxiliary outputs can be achieved by linear post-regulators, individual DC/DC converters, magamp circuits or switchmode Secondary Side Post Regulators (SSPR). All of these techniques are based on closed loop output voltage regulation of their respective outputs.

Before reviewing these power supplies a little bit closer, Figure 1 can be used to position the different solutions on the Cost/Complexity vs. Performance plane. For simplicity and for fair comparison, a three output forward converter is used where it was possible. In each case, it was assumed that the main output is regulated directly by the PWM controller of the power supply. The performance scores of the different solutions were based on expected efficiency and output voltage regulation characteristic. The cost/complexity score was determined by the number of power components (MOSFET and diode switches, inductive components, energy storage capacitors), by the number of integrated circuits required and by the number of control loops employed in that particular solution.

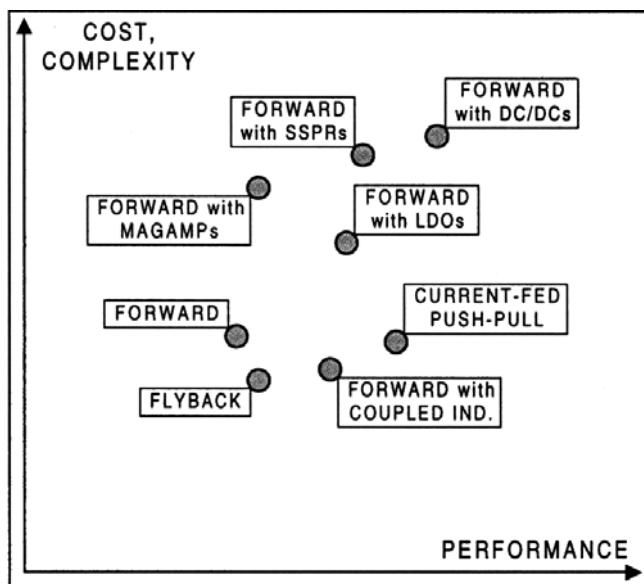


Figure 1. Cost/Complexity vs. Performance Comparison for Three Output Isolated Converters

As Figure 1 shows, better performance requires more elaborate solutions which are more complex and more costly. As the specified output voltage accuracies increase for a given multi-output power supply, the solution offers less and less possible simplification. The best performing solution, a forward converter with individual DC/DC converters for the auxiliary outputs, has striking resemblance in complexity and in the number of converters employed, to the starting point, where individual converters have been used for each outputs. The point to make here is that multi-output converters can not offer cost savings and simpler solutions unless the power supply output specification is relaxed accordingly.

TOPOLOGY OVERVIEW

Solutions Without Post Regulator

Generally, any isolated topology with several secondary windings in the transformer can provide multiple output voltages. These circuits employ a single primary side power stage including the input filter, energy storage capacitor, a high frequency power switch, usually a MOSFET transistor and a PWM controller. On the secondary side, isolated by the transformer, are the output components, rectifiers,

energy storage capacitors and output inductors where it is applicable. Among those outputs, one is distinguished as the **main** output whose output voltage is regulated by a feedback loop. The fundamental element of the feedback loop is the voltage error amplifier. Its output provides the feedback signal which is transmitted to the primary side over the isolation barrier. On the primary side, the feedback signal is received by the PWM controller and ultimately determines the duty-cycle of the power switch. It is important to emphasize, that in all of these cases, there is only one controlled quantity, the duty-cycle of the MOSFET, which allows control of only one output parameter, which is the output voltage of the main output. Thus, the output voltage of the main output is accurately regulated.

On the other hand, the auxiliary outputs are not directly regulated by the PWM modulator. The nominal auxiliary output voltages are determined by the turns ratio of the output windings. Their voltage regulation accuracy is a function of the coupling among the **secondary** windings, the voltage drop difference among the rectifier diodes and the voltage drop on the parasitic resistance of the series components of those outputs. These parasitic resistive components, secondary winding resistance, rectifier diode equivalent series resistance, the resistance of the output inductor and the wiring or trace resistance represent a load dependent voltage drop between the secondary winding and the actual output of the power supply. As the load current changes, the auxiliary output voltages will vary accordingly, causing the well know cross regulation error.

Flyback Converter

The flyback converter with multiple output windings is the simplest implementation for multi-output power supply. Typical application area for this solution is the low power, low current, multi-output power conversion where semi-regulated output voltages are acceptable and noise requirements are significantly relaxed. To improve noise performance, additional LC post-filters can be added to the outputs. Figure 2 shows a typical circuit diagram of a multi-output flyback converter.

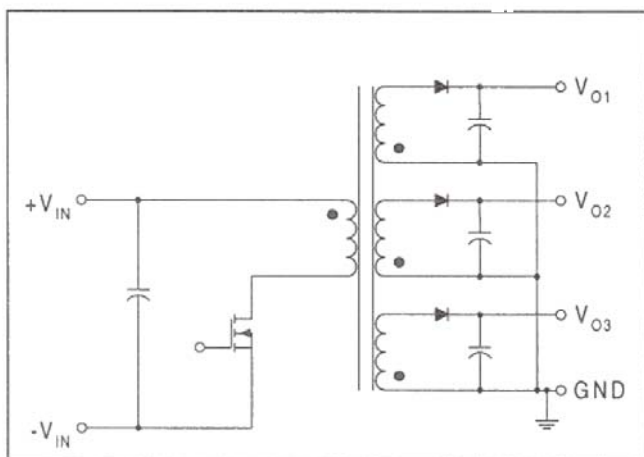


Figure 2. Multi-Output Flyback Converter

The advantages of this solution are:

- simple, economical approach
- only one magnetic component
- smallest number of semiconductors
- fair overall efficiency
- single control loop system

The disadvantages are:

- semi-regulated auxiliary outputs
- power throughput is limited by the flyback transformer
- high stress on the energy storage capacitors
- meeting output noise specifications frequently requires post filters
- right half-plane zero in continuous conduction mode limits the control loop bandwidth

Forward Converter with Individual Outputs

The forward converter of Figure 3 is rarely used because it utilizes a large number of inductive components. Furthermore, the outputs of the forward converter have more parasitic resistances than the flyback output circuits due to the additional filter inductors. Thus, the cross regulation among the outputs are usually worse than in the flyback converter. Balancing the fact of the poorer output tolerances, the forward converter offers better noise performance. The output filter inductor stores energy and it ensures continuous current flow to the load. Consequently, less output capacitance is required and lower noise specification can be achieved.

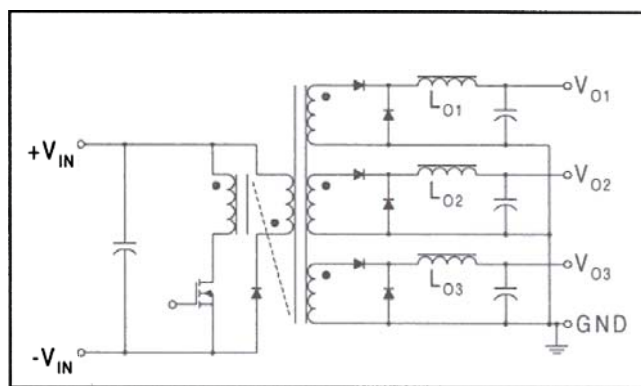


Figure 3. Forward Converter with Individual Output Inductors

This solution offers the following benefits:

- simple, well understood power stage
- good for medium power multi-output converters
- continuous current flow to the outputs
- low noise outputs
- good overall efficiency (single stage power conversion)
- single control loop system

The most significant drawbacks are:

- semi-regulated auxiliary outputs
- poor cross-regulation characteristic especially in discontinuous conduction mode of the output filter inductors
- large number of magnetic components

As mentioned before, this solution is rarely found in multi-output power supplies. Remarkably, the fundamental reason for that unpopularity is not the deficiencies of the topology, but the improvements offered by the circuit described in the next section.

Forward Converter with Coupled Inductors

The forward converter with coupled filter inductors is well accepted for multi-output power supplies. As shown in Figure 4, the output inductors are wound on a single core. This technique allows all outputs to be dynamically coupled through the shared magnetic core. The coupled inductor stores energy like traditional output inductors and also works like a transformer, improving cross regulation among the outputs. In addition to the performance improvement, using a coupled inductor reduces the number of costly, magnetic components.

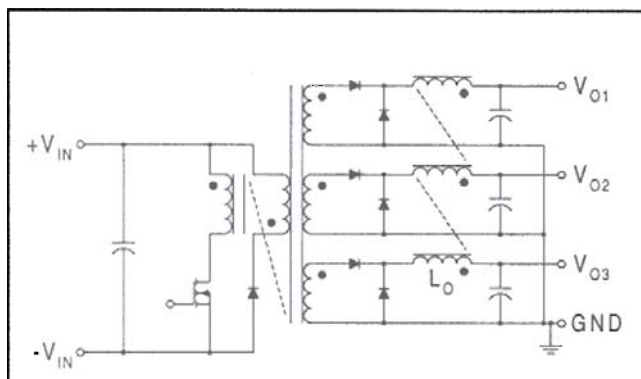


Figure 4. Coupled Output Inductors in Multi-Output Forward Converter

In comparison, this circuit has a similar set of advantages and disadvantages as the forward converter with individual output inductors. Additionally, this approach is more cost effective and offers better output voltage regulation due to the coupled output inductors. Therefore, this approach is almost exclusively preferred over individual output inductors.

Current-Fed Push-Pull Converter

As one can conclude from the forward converter examples, adding series components to the output circuits, such as filter inductors or current sense resistors will have a negative impact on output voltage and cross regulation properties. On the other hand, having no output inductor, like in the flyback converter, causes higher component stresses, more output noise and limits the output power capability of the converter.

These seemingly antagonistic requirements are conquered in the current-fed push-pull converter shown in Figure 5. The output circuit resembles the flyback configuration since there is no output filter inductor. That minimizes the output voltage regulation error caused by the excess parasitic resistances. Furthermore, the push-pull transformer is driven by a 50%-50% duty-cycle bipolar signal providing continuous power flow to the outputs. That optimizes the core utilization in the isolation transformer as well as reduces output component stresses, noise and makes this circuit suitable for high power applications. The cross regulation of a current-fed push-pull converter is significantly better than any of the previously mentioned topologies.

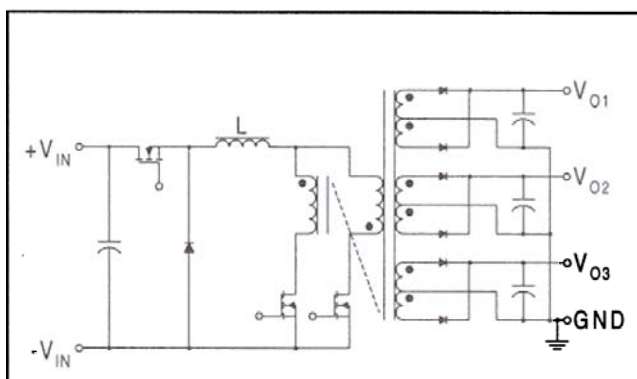


Figure 5. Three-Output Current-Fed Push-Pull Converter

The current-fed push-pull converter has the following advantages:

- single winding inductor serves any number of outputs
- few secondary side parasitic components (R_{diode} and R_{sec})
- continuous current flow to the outputs
- good cross regulation characteristic
- good for medium to high power multi-output converters
- low noise outputs
- good overall efficiency (despite the two stage power conversion)
- single control loop system (push-pull stage is free running)

Disadvantages:

- semi-regulated auxiliary outputs
- highest number of controlled switches in the semi-regulated circuit family
- two stage power conversion

This circuit will be further analyzed and a detailed design procedure is presented later in this paper.

Solutions With Post Regulators

In many applications, especially at lower output voltages, adequate output voltage tolerances can not be achieved without some sort of post regulation of the auxiliary (not directly regulated) outputs. These power supplies might employ any topology with multiple output windings. The main output is still regulated by direct feedback and pulse width modulation of the primary switch in the isolating power stage. Once post regulation is considered, tight cross regulation among the outputs is not critical, however

it might be beneficial to reduce power dissipation and/or optimize the design of the selected post regulator. The four most popular post regulation techniques are reviewed next.

Linear Post Regulator

Linear post-regulators are extensively used for low current outputs. A typical application with a multiple output forward converter is shown in Figure 6. Since linear regulators require a minimum voltage drop across the pass element, their application is usually restricted by power dissipation at higher output currents. This voltage drop together with the load current represent a relatively large variable power loss. Although, a low drop out (LDO) linear regulator requires smaller voltage drop between its input and output terminals, this advantage can be utilized only at the minimum input voltage. Unless the input voltage is tightly regulated, at high input voltage the maximum power dissipation of the traditional and the LDO linear regulator is the same.

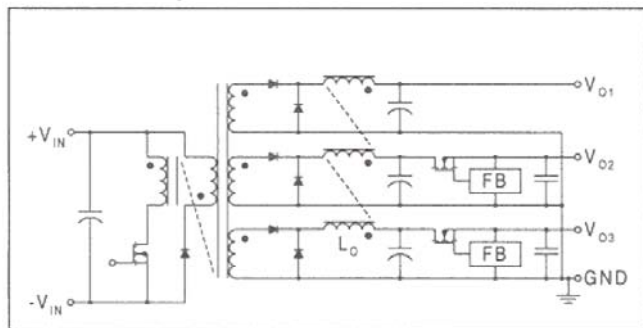


Figure 6. Typical Linear Post-Regulator Application

The most significant advantages of using linear post-regulators are:

- simple, cost effective and highly integrated at low currents
- low noise auxiliary outputs
- voltage regulation is independent from the main converter's duty-ratio
- independent overload and short circuit protection

The drawbacks involve:

- limited efficiency
- high dissipation across pass element in overload

DC/DC Switching Post Regulator

DC/DC converters, usually simple buck converters, provide efficient, local regulation of the auxiliary

outputs in a multi-output power supply. As Figure 7 indicates, this technique employs two cascaded switch mode power converters. The two converters operate independently and offer a great degree of flexibility for the system designer. Since the buck post regulator works from a semi-regulated input voltage, its operating conditions and efficiency can be easily optimized. Synchronization is desirable in most of the cases to reduce interaction between the main converter and the post regulators.

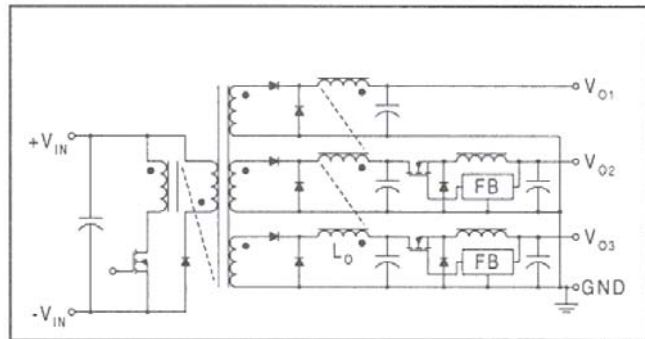


Figure 7. Buck DC/DC Post Regulator Simplified Schematic

The switch mode post regulators offer the following advantages:

- high efficiency
- high accuracy
- independent over-load and short circuit protection
- voltage regulation is independent from the main converter's duty-ratio

The list of disadvantages includes:

- complex circuitry
- costly
- usually requires additional bias voltage for controller and/or floating buck driver

Magamp Post Regulator

Magamp circuits are very popular in medium to high power application where the limited efficiency of the linear regulators are not acceptable. The saturable reactor in the magamp post regulator functions as a magnetic switch. Before the core of the magamp inductor saturates, it represents a large impedance in series to the secondary winding of the isolation transformer preventing power transfer to that output. By properly positioning the operating point of the magnetic core on the B-H curve, a vari-

able portion of the secondary pulse can be blocked. Thus the effective duty-ratio for the buck inductor can be further modulated, allowing precise regulation of the auxiliary output voltage.

A typical application is depicted in Figure 8.

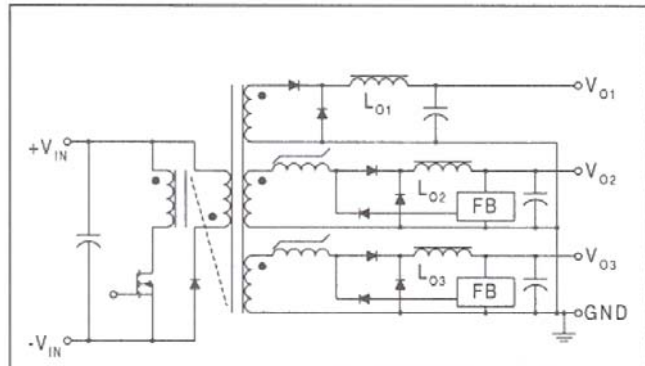


Figure 8. Typical Magamp Post-Regulator Implementation

The magamp advantages are:

- good accuracy
- high efficiency at nominal output current

The disadvantages are:

- large number of inductive components
- high cost
- limited operating frequency
- troublesome short circuit protection and no load operation
- auxiliary output duty-cycle is limited by the main output duty-ratio

Secondary Side Post Regulators (SSPR)

Integrated circuit manufacturers recently developed several controllers which allow using a cost effective, N-channel MOSFET switch in place of the saturable reactor of the magamp circuit. These solutions are referred to as Secondary Side Post Regulators or SSPRs, in the literature. While the distinct implementations might differ slightly, they can be represented by the simplified schematic of Figure 9. The SSPR circuits address most of the major drawbacks of the magamp solutions. They are compatible with higher switching frequencies, allow easy operation at light load and in short circuit conditions. In addition, they are less expensive and usually take up less board area.

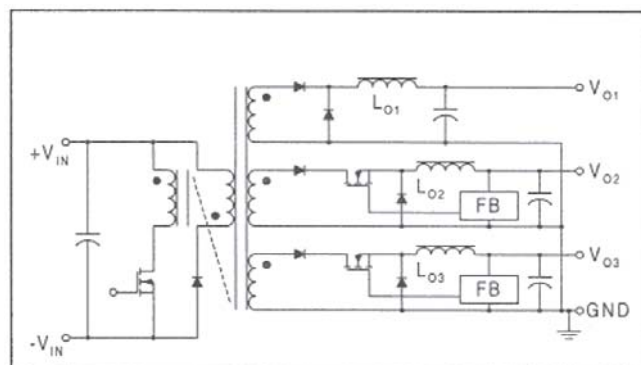


Figure 9. Secondary Side Post Regulator (SSPR) Circuit Diagram

SSPR applications profit from:

- high accuracy
- high efficiency under all load conditions
- high frequency operation
- fast transient response
- independent over-load and short circuit protection
- moderate cost

The most significant shortcomings are:

- usually requires additional bias voltage for controller and/or floating buck driver
- high parts count
- large number of controlled switches
- auxiliary output duty-cycle is limited by the main output duty-ratio

DESIGN REVIEW

The following design review focuses on the design procedure of a three-output DC/DC converter. The first step in any successful design is to determine the power supply specification. The most important parameters are listed in the next paragraph:

Specification Overview

Input DC Voltage:	12V ... 15V
Output DC Voltages:	28V±0.5V@ 0.5A ... 4A 12V±0.5V@ 0.2A ... 0.2A 5V±0.25V@ 0.2A ... 1.5A
Output Power:	17.5W ... 143.5W
Efficiency:	>85%
Isolation:	none
Noise:	100mV _{pp} @28V 100mV _{pp} @12V 50mV _{pp} @5V
Target Size:	2.25"x1.3"x0.5"
Power Density:	~100W/in ³

Step-By-Step Design Procedure

Topology Selection

The first step is to examine the output voltages, currents, power ratings and their respective tolerance bands. Simple calculations translate the specifications into the following output characteristics:

$V_{O1} = 28V \pm 1.8\%$	$I_{O1} = 4A$	$P_{O1} = 112W$
$V_{O2} = 12V \pm 4.2\%$	$I_{O2} = 2A$	$P_{O2} = 24W$
$V_{O3} = 5V \pm 5\%$	$I_{O3} = 1.5A$	$P_{O3} = 7.5W$

Assuming that V_{O1} is regulated directly by the power supply's PWM controller, the other output voltage tolerances are adequately relaxed to consider a solution without post regulators. Also note that the currents of the auxiliary outputs are low, therefore voltage drop on the parasitic resistors of the circuits can be kept under control to meet output voltage tolerances including cross-regulation errors.

The next factor influencing the circuit selection is the efficiency and power density goals. Although, the flyback converter appears very attractive because of its simplicity and low parts count, it would be difficult to meet the anticipated 85% efficiency goal especially at high switching frequency which seems inevitable to reach the targeted power density. Furthermore, the flyback approach would require higher than necessary output capacitance values to handle ripple currents due to the high switched current waveform of the output stage. More than likely, additional LC filter stages would also be required to meet the output noise specifications.

The forward converter is the next candidate to explore. Because of its simplicity and lower number of magnetic components, only the coupled filter inductor version is contemplated. This solution can be used at high switching frequency and it has a continuous power flow towards the outputs due to the filter inductor. The output capacitor stresses are reasonable and in continuous conduction mode of the output inductor, the voltage regulation of the auxiliary outputs can be achieved. What makes this implementation less attractive is the duty-cycle limitation determined by the reset time requirements of the isolation transformer and the interaction between leakage inductances and turns ratios between

the transformer and the coupled filter inductor windings. Moreover, the coupled filter inductor represents additional load dependent voltage drop in series to the auxiliary outputs.

Ultimately, the current-fed push-pull converter has been selected for this application. As Figure 5 showed, the outputs have minimum number of components, thus cross regulation specification can be met easier than in the forward converters. Also, continuous power flow to the outputs are insured considering the push-pull transistors operate at a nominal 50%-50% duty-ratio all the time. The core utilization of the isolation transformer is optimal because of the first and third quadrant operation, and lack of duty-cycle modulation in the push-pull stage. A single winding inductor resides on the primary side which allows simpler inductor design and better optimization. Consequently, high efficiency and power density can be achieved using the current-fed push-pull solution.

Operating Frequency

The switching frequency has the utmost influence on the efficiency and size of the power supply. Usually, higher efficiency can be achieved at lower or moderate frequencies as the switching losses of the semiconductors are lower. On the other hand, the size of the reactive components is getting smaller as the operating frequency increases. The trade-off between size and efficiency has to be evaluated very carefully. Remember, that in many applications the final size of the power supply must include the bulk of the heatsink as well. Volume gained in component sizes can be easily forfeited to larger heatsinks as switching losses increase at higher operating frequencies. Therefore, the choice of clock frequency shall be based on the detailed analysis of the switching and conduction losses in the circuit, calculated later in this paper.

Control Technique

The underlying operating principle of the current-fed push-pull converter is that a current source, i.e. the buck stage, feeds an ideal "switched mode transformer" comprised by the push-pull circuit. By adjusting the source current to the transformer, the output voltage is regulated across the load. Since the basic objective is regulating the inductor current, the

best suited control technique is average current mode control. Average current mode control offers short circuit and overload protection, inherent rejection of input voltage changes, fast transient response and easy current loop setup since slope compensation is not required. Furthermore, using current mode control simplifies the compensation network around the voltage error amplifier. In order to implement average current mode control, the current of the buck inductor has to be sensed and that information is processed by a dedicated current error amplifier. To maximize the overall efficiency of the solution, a low value current sense resistor is desirable. Therefore, the control circuit should also include a current sense amplifier. Ultimately, voltage regulation is accomplished by employing a voltage error amplifier. Another necessity of the control circuit is to be able to drive the floating MOSFET switch of the buck converter and the two ground referenced MOSFET switches of the push-pull power stage. Traditionally, such a controller had to be built from several integrated circuits. Fortunately, all these requirements can be effortlessly addressed using the UC3827-1

integrated circuit, dedicated to control the current-fed push-pull converter.

Power Components

Figure 10 shows the final schematic of the power components and their respective reference designators.

MOSFET Transistors

The first step is to analyze the operating conditions and losses of the semiconductors on the primary side, which can be separated into switching and conduction losses. The conduction losses are determined by the RMS current of the MOSFET switches and by the average current in D4. Assuming an infinite inductor value, i.e. small ripple current in the buck inductor, the current waveforms are depicted in Figure 11, where I_L is the DC current in the buck inductor, D_{BUCK} is the duty ratio of the buck converter and t_D is the overlap time of the conduction intervals of the push-pull switches.

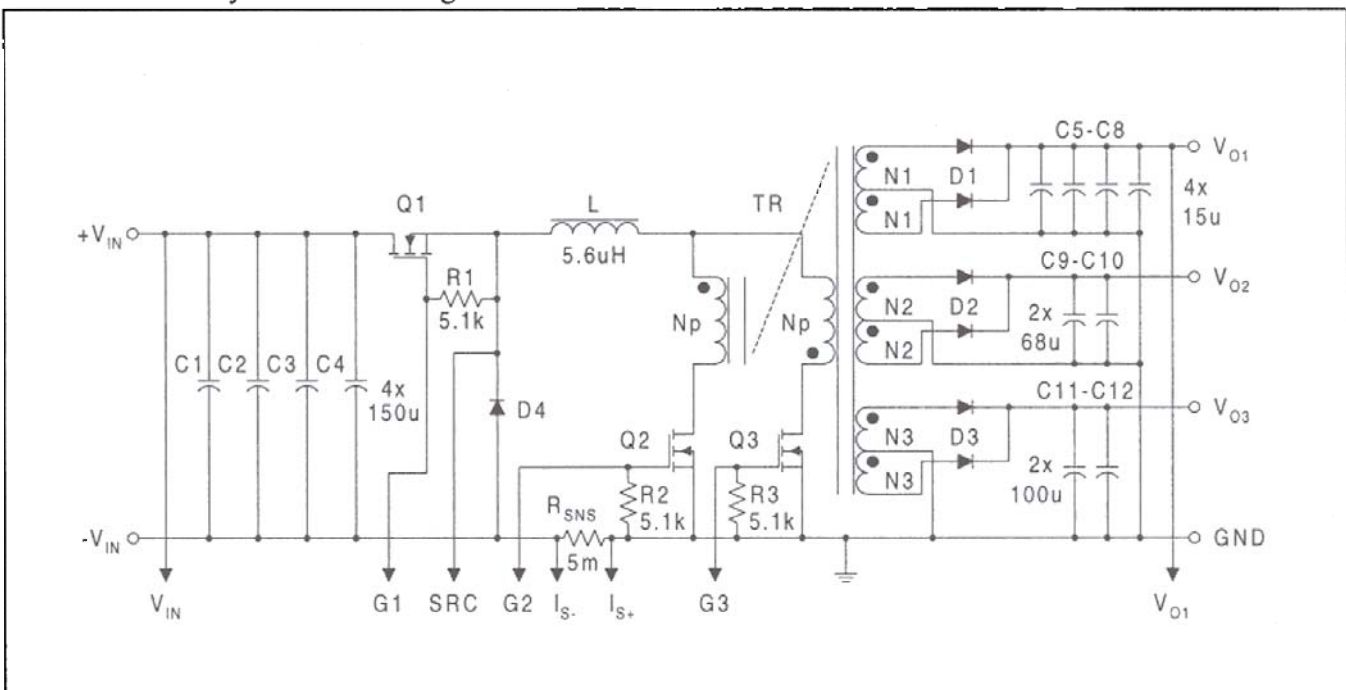


Figure 10. Three-Output Current-Fed Push-Pull Converter

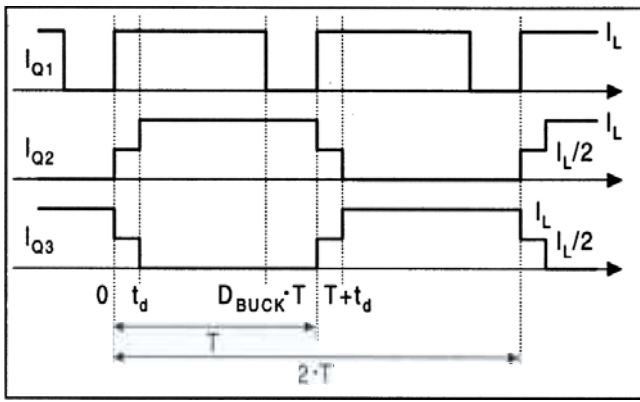


Figure 11. Current-Fed Push-Pull Converter Current Waveforms

In all buck derived topologies, efficiency can be maximized if the switch duty ratio is maximized. That condition is fulfilled if the output voltage of the buck converter is just slightly lower than the minimum input voltage of the converter. Assuming $D_{BUCK,MAX} = 0.9$, the buck output voltage, i.e. the voltage at the centertap terminal of the push-pull transformer, V_{CT} can be calculated:

$$V_{CT} = V_{IN,MIN} \cdot D_{BUCK,MAX} \quad (1)$$

Therefore, D_{BUCK} for any input voltage is given as:

$$D_{BUCK} = \frac{V_{CT}}{V_{IN}} \quad (2)$$

The efficiency of the push-pull stage can be maximized if t_D is minimized. Note, that during the period when Q2 and Q3 conduct simultaneously, there is no energy transfer to the outputs. Therefore, the overlap interval shall be minimized to maintain efficiency and maximum utilization of the push-pull transformer. On the other hand, t_D must be longer than the estimated turn-on time of Q2 (or Q3). The switching times of a MOSFET transistor can be estimated based on the device parameters according to:

$$t_{ON} = \frac{Q_{GD} \cdot R_{GATE}}{V_{GATE} - V_{TH}} \quad (3)$$

$$t_{OFF} = \frac{Q_{GD} \cdot R_{GATE}}{V_{TH}} \quad (4)$$

To ensure that the turn-on switching actions of Q2 (or Q3) are fully completed and both switches are ON by the end of the t_D interval, $t_D > t_{ON}$ must be se-

lected. To provide proper margins under all operating conditions, $t_D = 150ns$ was chosen for this design.

The switch RMS currents and the diode average current value can be determined from the current waveforms. The derivation yields the following expressions:

$$I_{RMS,Q1} = I_L \cdot \sqrt{D_{BUCK}} \quad (5)$$

$$I_{RMS,Q2} = I_{RMS,Q3} = I_L \cdot \sqrt{0.5 - \frac{t_D}{4 \cdot T}} \quad (6)$$

$$I_{AVE,D4} = I_L \cdot (1 - D_{BUCK}) \quad (7)$$

The conduction losses are calculated at 125°C worst case junction temperature according to:

$$P_{COND,Q1} = 1.6 \cdot R_{DS(on)} \cdot I_{RMS,Q1}^2 \quad (8)$$

$$P_{COND,Q2} = P_{COND,Q3} = 1.6 \cdot R_{DS(on),Q2} \cdot I_{RMS,Q2}^2 \quad (9)$$

$$P_{COND,D4} = V_{FWD,D4} \cdot I_{AVE,D4}$$

The MOSFET switching losses are broken down as gate charge loss, C_{OSS} loss, turn-on and turn-off losses as given by the following equations:

$$P_{GATE} = Q_{GATE} \cdot V_{GATE} \cdot f_s$$

$$P_{COSS} = \frac{1}{2} \cdot C_{OSS} \cdot V_{OFF}^2 \cdot f_s$$

$$P_{ON+OFF} = \frac{1}{2} \cdot V_{OFF} \cdot I_L \cdot (t_{ON} + t_{OFF}) \cdot f_s$$

where Q_{GATE} is the total gate charge, V_{GATE} is the gate drive voltage, f_s is the clock frequency, C_{OSS} is the drain-source capacitance of the MOSFET, t_{ON} and t_{OFF} are the switching times estimated in (3) and (4). V_{OFF} is the drain voltage during the off-time of the transistor which equals:

$$V_{OFF,Q1} = V_{IN}$$

$$V_{OFF,Q2} = V_{OFF,Q3} = 2 \cdot V_{CT}$$

The switching losses for the buck freewheeling diode can be neglected since a Schottky rectifier is considered. Schottky rectifiers are inherently free from the reverse recovery phenomena which is the

major source of switching losses in the rectifier diodes.

In order to see the effect of the die size and to find the optimum balance between switching and conduction losses versus operating frequency, two different MOSFETs, a 24m Ω IRFZ44N and an 8m Ω IRF3205 were examined. After collecting all device parameters, (5) through (15) were evaluated quantitatively at full load and nominal input voltage. The losses of the buck transistor and one of the push-pull transistors for this application are shown in Figure 12.

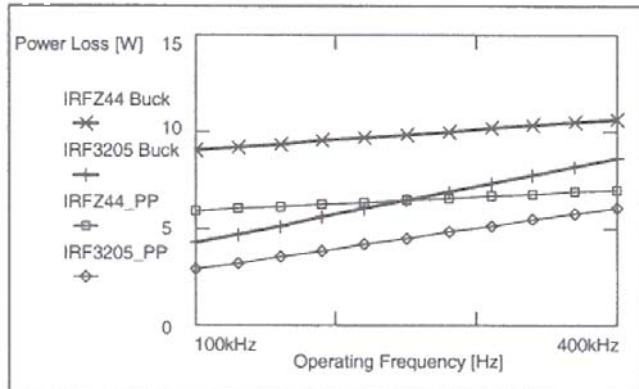


Figure 12. MOSFET Losses vs. Frequency

The graph shows the power dissipation from 100kHz to 400kHz which was considered the practical clock frequency range for this application. In this frequency range, the larger MOSFET offers significantly lower losses due to lower conduction losses. Note, that examining the trends in the graph suggest that at even higher switching frequencies the two curve pairs would cross each other. Above the crossover points the higher $R_{DS(on)}$ device would be more desirable because of the lower switching losses. The clock frequency where the two curves cross is a function of the device currents and supply voltages. In this application the MOSFETs are carrying high currents and working with low voltages, and therefore, the crossover point is at very high frequency. Another conclusion of Figure 12 is that the operating frequency should be kept as low as possible in order to improve efficiency. Taking into account the desired size and power density, a 200kHz clock frequency and the IRF3205 MOSFETs have been selected for Q1, Q2 and Q3 switches.

Rectifier Diodes

Next, the rectifier diodes, D1 through D4 will be selected. Since the input side of the circuit processes high current and low voltage levels, it is most common to use a Schottky rectifier. Schottky diodes are usually selected by their forward voltage drop at their rated current. While low voltage drop is definitely an essential parameter here, there is one more important property to consider. That is the maximum junction temperature of the device.

Part Number	V _{fwd} @25°C and 25A	T _{J,MAX}
MBR2535CT	0.76V	150°C
MBR2535CTL	0.55V	125°C
MBR2515L ("ORING" diode)	0.45V	100°C

Table 1. Schottky Diode Parameters

For instance, comparing the three Motorola Schottky rectifiers in Table 1 reveals that lower forward voltage drop and maximum junction temperature are traded against each other in Schottky technology. Therefore, it is important to check both parameters. In this design, MBR2535CTL is used as the freewheeling diodes of the buck stage (D4) and the rectifier diode of the 5V output (D3).

The other two output rectifiers, D1 and D2 employ ultrafast epitaxial diodes. A unique property of the current-fed push-pull stage is that the reverse voltage across the rectifier diodes is independent of the input voltage. Due to the symmetrical waveform of the transformer windings and the lack of output inductors, all diodes block twice their respective output voltages. Leaving sufficient safety margin for possible switching spikes, D1 must be rated for at least 100V while D2 is at least a 50V diode. Ultimately, D1 and D2 have been selected as the BYQ28-100 from Philips Semiconductors.

Transformer Design

The following section is dedicated to define the transformer turns ratios. The fundamental problem in the turns ratio selection is to find the smallest number of turns which provide sufficient resolution to set the required output voltages. In order to obtain fairly accurate results, the calculation has to take into account the voltage drop across the rectifier diodes. There-

fore, the following parameters have to be found based on the diode datasheets:

- V_{D1} , the forward voltage drop of the rectifier diode at the rated output current of the 28V output, V_{O1} .
- V_{D2} , the forward voltage drop of the rectifier diode at the rated output current of the 12V output, V_{O2} .
- V_{D3} , the forward voltage drop of the rectifier diode at the rated output current of the 5V output, V_{O3} .

The process is somewhat iterative and starts by selecting the number of turns for the lowest output voltage, N3. Once N3 is chosen, using the nominal output voltage values, the required number of turns for the other outputs can be obtained according to:

$$N1 = \frac{V_{O1,NOM} + V_{D1}}{V_{O3,NOM} + V_{D3}} \cdot N3 \quad (16)$$

$$N2 = \frac{V_{O2,NOM} + V_{D2}}{V_{O3,NOM} + V_{D3}} \cdot N3 \quad (17)$$

$$Np = \frac{V_{CT}}{V_{O3,NOM} + V_{D3}} \cdot N3 \quad (18)$$

After all the number of turns are found, the actual value of the output voltages can be determined. For this calculation, assume that V_{O1} always equals its nominal value (28V) because that output is directly regulated by the feedback loop. For the other outputs, the following equations prevail:

$$V_{O2} = (V_{O1} + V_{D1}) \cdot \frac{N2}{N1} - V_{D2} \quad (19)$$

$$V_{O3} = (V_{O1} + V_{D1}) \cdot \frac{N3}{N1} - V_{D3} \quad (20)$$

$$V_{CT} = (V_{O1} + V_{D1}) \cdot \frac{Np}{N1} \quad (21)$$

The results from solving equations (16) through (21) for this particular application, are summarized in Table 2.

N3	N1	N2	Np	V _{O1}	V _{O2}	V _{O3}	V _{CT}
1	3	6	2	28V	13.65V	4.57V	9.63V
2	5	11	4	28V	12.34V	5.01V	10.51V
3	7	16	6	28V	12.8V	4.85V	10.02V
3	8	17	6	28V	11.84V	5.17V	10.84V
4	10	22	8	28V	12.34V	5.01V	10.51V
5	12	27	10	28V	12.04V	5.10V	10.7V
7	17	38	14	28V	12.13V	5.07V	10.65V
16	39	88	32	28V	12.01V	5.01V	10.51V

Table 2. Different Turns Ratio and Output Voltage Variations

Table 2 demonstrates the iterative nature of turns ratio selection. The calculations are executed starting with different number of turns for N3, then the results is compared to the regulation range given in the power supply specification.

The inaccuracies are caused by rounding the number of turns, thus recalculating the actual output voltages with integer turns is essential. For this example, the second row has already provided an acceptable solution, the rest of Table 2 is just for demonstration purposes. As the number of turns for N3 increased, the resolution increases, and the voltages close in on the nominal values. The best resolution has been achieved in the last row. Although, N3 = 16 looks rather arbitrary pick for V_{O3} , it is not. Close to optimum resolution can be reached when the voltage across one turn in the transformer equals the lowest voltage drop across the rectifier diodes. The problem with this approach is that the resulting number of turns are usually too high for practical purposes.

Next the transformer core is selected based on the maximum volt-second product the transformer has to withstand:

$$V \cdot S = V_{CT} \cdot (T - t_D) \quad (22)$$

Although, the details of the core selection are not discussed here, two alternative winding structures are worthwhile mentioning.

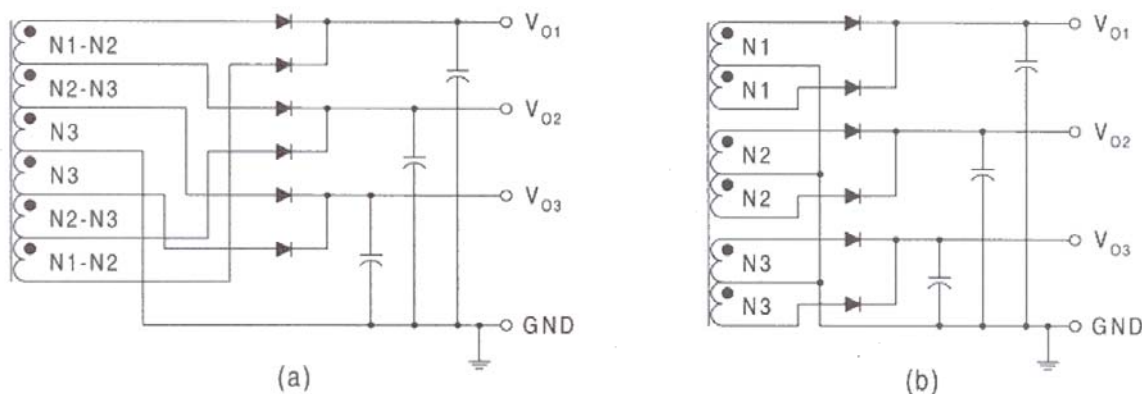


Figure 13. Different Output Winding Arrangements

Version (a) of Figure 13 shows an incremental winding structure, where the different output voltages are generated by tapping the N1 winding at the required number of turns. Version (b) indicates individual windings for each outputs. To decide which solution gives better cross regulation, the following equivalent circuits are introduced in Figure 14.

Estimating cross regulation properties starts at calculating the voltage across a single turn in the transformer, V_{1T} . For this, all parasitic resistor values and the current through them must be known. The transformer winding resistances can be estimated using the average turn length and the wire cross section or can be measured once the transformer is wound. The diode parameters can be read from the diode manufacturers' datasheet. The unknown cur-

rents I_1 , I_2 and I_3 can be calculated from the load currents and from the effective duty-ratio of the push-pull converter:

$$I_1 = \frac{I_{O1}}{D_{EFF}} \quad (23)$$

$$I_2 = \frac{I_{O2}}{D_{EFF}} \quad (24)$$

$$I_3 = \frac{I_{O3}}{D_{EFF}} \quad (25)$$

where

$$D_{EFF} = 1 - \frac{t_D}{T} \quad (26)$$

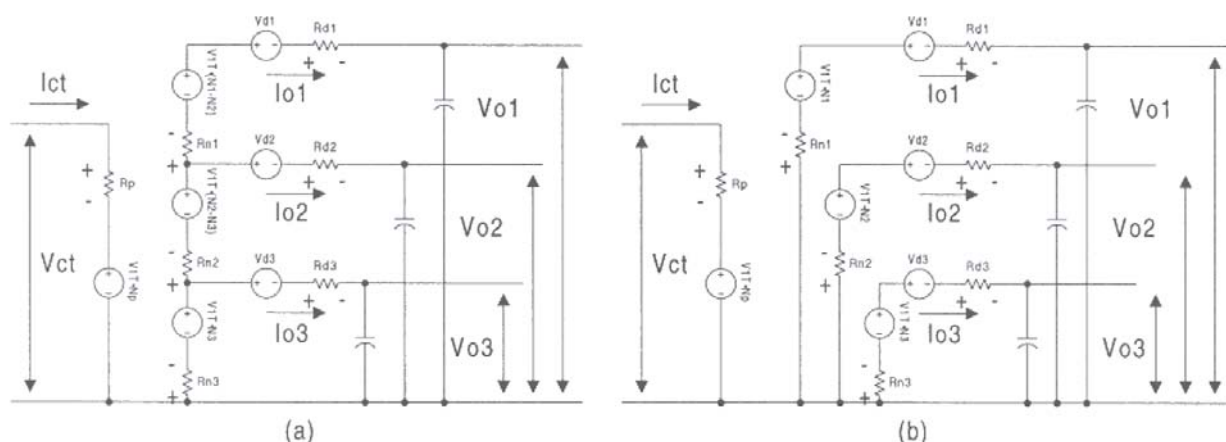


Figure 14. Equivalent Output Circuits

Until this point the equations are identical for both equivalent circuits. Hereafter, the relationships for version (b) are determined. Similar equations can be derived and solved for (a) the results of which will also be presented later. Assuming that V_{O1} is regulated, the voltage across a single turn is given as:

$$V_{1T} = \frac{V_{O1} + V_{D1} + I_{O1} \cdot (R_{D1} - R_{N1})}{N1} \quad (27)$$

The unregulated output voltages can be obtained from:

$$V_{O2} = V_{1T} \cdot N2 - V_{D2} - I_{O2} \cdot (R_{N2} + R_{D2}) \quad (28)$$

$$V_{O3} = V_{1T} \cdot N3 - V_{D3} - I_{O3} \cdot (R_{N3} + R_{D3}) \quad (29)$$

The incremental winding structure shown in Figure 14(a), can be analyzed using the same approach. In this case, the single secondary winding has 11 turns in three sections. The first section is composed of $N3 = 2$ turns, after which the secondary is tapped to supply the 5V output, V_{O3} . The middle section has 3 turns which, together with the 2 turns of the first section, comprises $N2 = 5$ turns. Thus, the series connection of the first and second section provides for the 12V output, V_{O2} . The third section of the secondary winding has 6 turns. Similarly, this section is connected in series to the first two winding sections. The total number of turns in the three section is then $N1 = 11$ turns which is required to supply the 28V output, V_{O1} . Note that the parasitic resistances shall be determined for each individual sections separately.

The predicted cross regulations for both (a) and (b) versions, using the numerical values of this application, are summarized in Table 3.

Load Currents			Version (a)		Version (b)	
I_{O1}	I_{O2}	I_{O3}	V_{O2}	V_{O3}	V_{O2}	V_{O3}
min	min	min	12.272V	4.98V	12.317V	4.992V
min	min	max	12.22V	4.891V	12.317V	4.87V
min	max	min	12.12V	4.939V	12.226V	4.992V
max	min	min	12.094V	4.905V	12.35V	5.005V
min	max	max	12.068V	4.85V	12.226V	4.87V
max	min	max	12.042V	4.816V	12.35V	4.883V
max	max	min	11.941V	4.864V	12.259V	5.005V
max	max	max	11.889V	4.775V	12.259V	4.883V

Table 3. Cross Regulation Predictions

Several conclusions can be drawn from the data listed in Table 3. First of all, cross regulation is better in (b) because there is no cross regulation effect between the auxiliary outputs. For instance, V_{O2} in equation (28) does not contain any term which would depend on I_{O3} . Furthermore, the numbers show that the cross regulation between the regulated output and each of the auxiliary outputs is improved as well. That can be explained by the fact that the voltage drop on R_{N2} and R_{N3} is not changing when I_{O1} varies. The cross regulation error is caused by the variation in the term V_{1T} only, when the load is changing on the main output. All these conclusions warrant the choice of output configuration (b) for this design.

There are some warnings which have to be made at this point. The numbers above are just rough estimates on cross regulation error and the transformer leakage inductances will definitely make them worse. Therefore, it is very important that the transformer is optimized for minimum leakage inductance. Among all the different techniques to reduce leakage inductance, interleaving and using the lowest number of layers are the most important ones. Be aware also that the transformer windings carry high frequency currents. Minimizing the number of layers will have a beneficial effect on the ratio between AC and DC resistances of the windings. Also important to remember is that coupling between the different windings is maximized if they occupy the same width in the bobbin and the vertical distance is minimized between them.

Finally, it is noteworthy to mention that for a two-output application versions (a) and (b) provide almost identical cross regulation. In that case, the most optimal layout of the transformer windings should be considered as the guiding rule.

Buck Inductor

The second, and last magnetic component of the current-fed push-pull converter is the buck inductor which is much easier to design. To improve performance, the buck inductor is designed to stay in continuous conduction mode at minimum output power. Therefore, the maximum ripple current is calculated from:

$$\Delta I_{L,MAX} = \frac{2 \cdot P_{OUT,MIN}}{V_{CT} \cdot D_{EFF}} \quad (30)$$

The largest ripple current occurs at $V_{IN,MAX}$ hence the minimum inductance of the buck inductor is given as:

$$L = \frac{V_{IN,MAX} - V_{CT}}{\Delta I_{L,MAX}} \cdot D_{BUCK,MIN} \cdot T \quad (31)$$

where

$$D_{BUCK,MIN} = \frac{V_{CT}}{V_{IN,MAX}} \quad (32)$$

The peak inductor current is calculated at maximum input voltage and full output power according to:

$$I_{L,PEAK} = \frac{P_{OUT,MAX}}{V_{CT} \cdot D_{EFF}} + \frac{1}{2} \cdot \Delta I_{L,MAX} \quad (33)$$

Note, that in buck derived topologies the average inductor current is independent from the input voltage. It is always equal to the DC output current. As the input voltage changes, the varying duty-ratio of the buck switch will cause the average input current to change. That is why the peak inductor current is calculated at full load current and at maximum input voltage where the largest ripple current amplitude occurs. Substituting the application parameters, the inductor value is found to be $5.4\mu H$ and it is rated for at least 16A.

As the reader might have already realized, the core selection procedure, core loss analysis are not discussed in this article. For those intricate details, refer to Lloyd Dixon's numerous and excellent publications on magnetic design.

Energy Storage Capacitors

The next components to select are the filter capacitors. Starting on the output side and assuming infinite buck inductance, the waveforms of C_{O1} (C5-C8), C_{O2} (C9-C10) and C_{O3} (C11-C12) can be approximated by the ones of Figure 15.

The output capacitors are determined by the ripple voltage specification, V_{PP} , and by their RMS current handling capability. The switching frequency ripple is due to the voltage drop caused by current flowing through the equivalent series resistor (ESR) of the capacitor and due to the fact that the capacitor supplies the load current while power flow from the

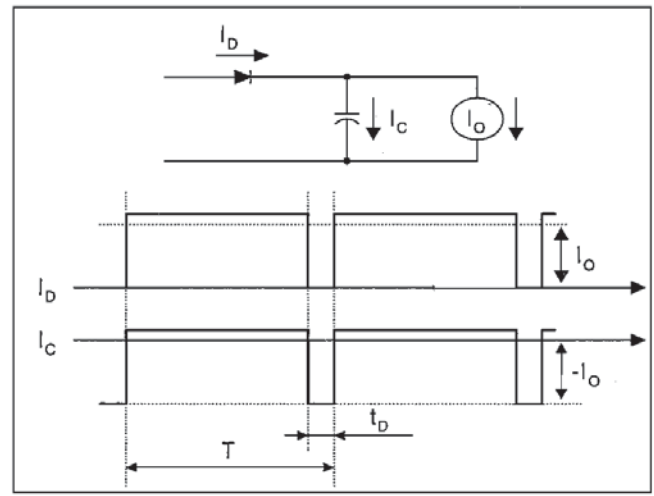


Figure 15. Output Capacitor Current Waveforms

input is interrupted, i.e. during t_D in this particular design. As a starting point, half of the specified ripple amplitude has been allocated for voltage drop across the ESR of the capacitors, approximately twenty percent for voltage decay during the gap time and the remaining amplitude is reserved to cover spikes caused by the switching actions in the circuit. Based on these assumptions, the following relationships can be established:

$$C_{O,MIN} = \frac{I_o \cdot t_D}{0.2 \cdot V_{PP}} \quad (34)$$

$$ESR_{MAX} = \frac{0.5 \cdot V_{PP}}{I_o \cdot \left(1 + \frac{t_D}{T - t_D}\right)} \quad (35)$$

The output capacitor RMS currents can be determined from the current waveforms of Figure 15, yielding:

$$I_{C,RMS} = I_o \cdot \sqrt{\left(1 + \frac{t_D}{T - t_D}\right) \cdot \frac{t_D}{T}} \quad (36)$$

Substituting the output current ratings and respective ripple voltages, equations (34), (35) and (36) give the minimum capacitance, maximum ESR and RMS current requirements listed in Table 4:

	C_{O1}	C_{O2}	C_{O3}
$C_{O,MIN}$	30 μF	15 μF	23 μF
ESR_{MAX}	12m Ω	24m Ω	16m Ω
$I_{C,RMS}$	0.7A	0.35A	0.26A

Table 4. Output Capacitor Requirements

The actual output capacitance values listed in the schematic, Figure 10, were chosen to provide the required ESR values. Following this approach to calculate output capacitance requirements allows the use of a very small LC post-filter stage if necessary because that post filter stage will not have to work at the switching frequency. It would be used only to suppress the switching spikes which are much higher frequency signals.

On the input side, the filter capacitor is designed following a similar approach. For the buck converter the input capacitor stresses are the highest at $D = 0.5$. In this application $D = 0.5$ is never reached, thus the calculation is executed at maximum input voltage, where the duty ratio is the closest to 50%. The capacitor current waveform is indicated in Figure 16.

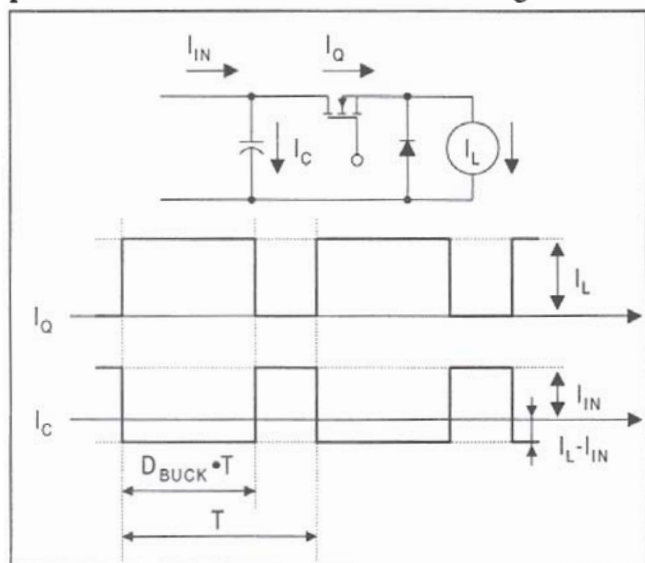


Figure 16. Input Capacitor Current Waveforms

Allowing 200mV ripple on the input capacitor and following the same guidelines established for the output capacitors, the capacitor parameters can be found from the modified equations (37) through (39).

$$C_{IN,MIN} = \frac{I_L \cdot (D - D^2) \cdot T}{0.2 \cdot V_{PP}} \quad (37)$$

$$ESR_{MAX} = \frac{0.5 \cdot V_{PP}}{I_L} \quad (38)$$

$$I_{C,RMS} = I_L \cdot \sqrt{D - D^2} \quad (39)$$

Substituting for the worst case conditions, the minimum input capacitance value equals 450μF, the maximum acceptable ESR is 6.3mΩ and the capaci-

tor RMS current rating has to be higher than 7.6A. These numbers required several parallel connected capacitors at the input as shown in Figure 10.

Current Sense Resistor

Lastly, the current sense resistor value is calculated. In order to minimize power dissipation and taking advantage of the internal current sense amplifier of the UC3827, the current sense resistor is chosen to furnish only a 100mV signal at maximum current in the circuit. This maximum current shall be determined to give sufficient margin for parameter tolerances. Therefore, instead of the calculated 16A peak inductor current, $I_{MAX} = 20A$ is taken into consideration.

Accordingly, the sense resistor value and its power dissipation is defined as:

$$R_{SENSE} = \frac{0.1V}{I_{MAX}} \quad (40)$$

$$P_{RSENSE} = R_{SENSE} \cdot I_{MAX}^2 \quad (41)$$

which yields 5mΩ at a 2W power rating.

UC3827 Current/Voltage-Fed Push-Pull Controller

First the block diagram and the basic functions of the integrated controller are presented. Figure 17 shows the internal architecture of the UC3827 used in this design. The IC operates within the 10V to 20V supply voltage range and includes all of the usual housekeeping functions, undervoltage lockout, soft start circuitry, an externally accessible 5V reference and synchronizable oscillator. The push-pull control section comprises of the push-pull latch, the delay block and two ground referenced high current gate drive outputs serving the two MOSFETs of the push-pull converter. The delay circuit in the UC3827-1 provides a user programmable interval for overlapping conduction time between the push and pull outputs for current-fed operation. In another version of this controller, the UC3827-2, the delay circuit provides a dead time between the conduction intervals for voltage-fed operation.

The buck pulse width modulator section consists of a PWM comparator, a current limit comparator, a PWM latch and a high voltage, floating driver stage. The PWM comparator inputs receive the control signal from the output of the current error amplifier and

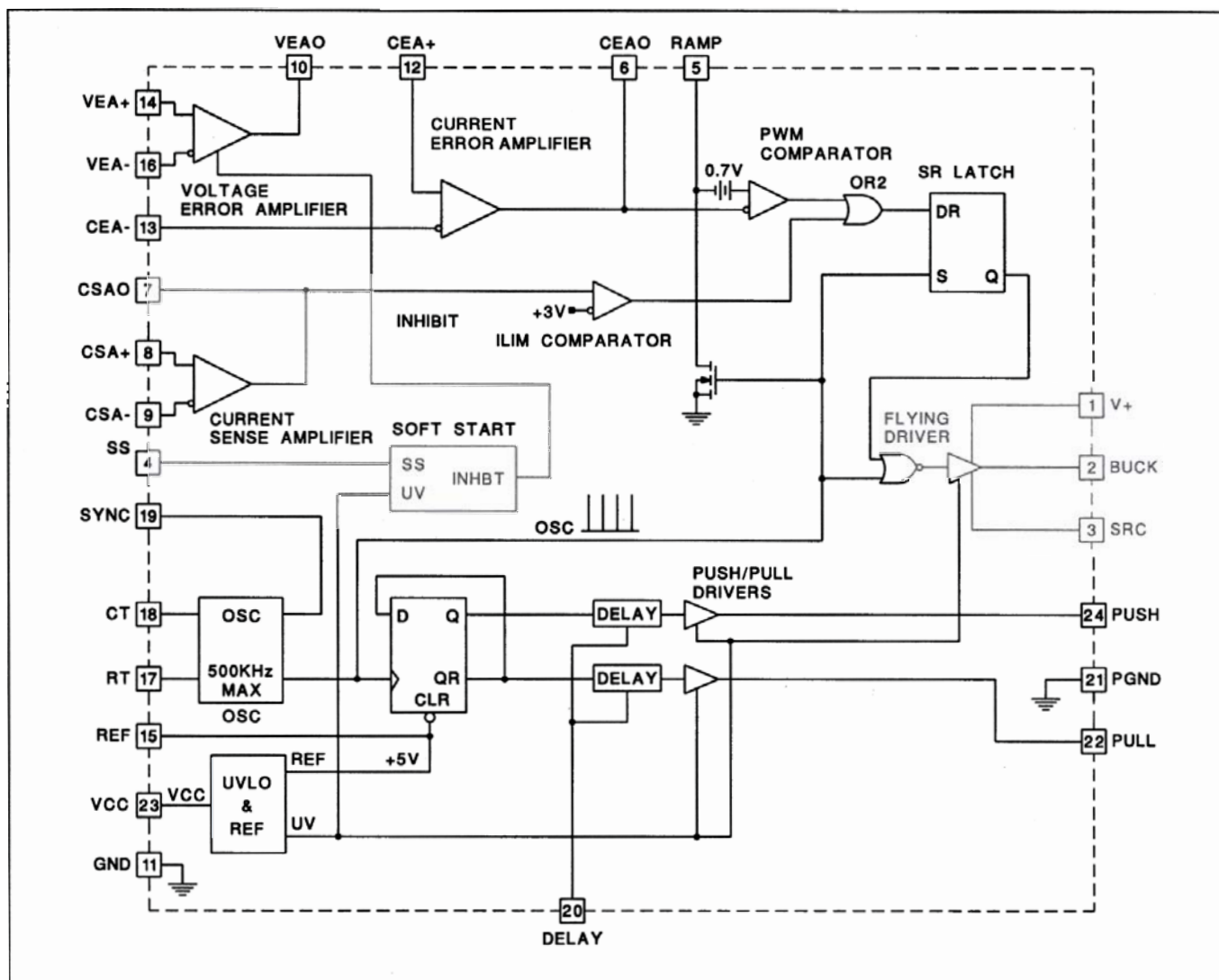


Figure 17. UC3827 Block Diagram

the ramp signal straight from the RAMP pin. The output of the PWM comparator determines the pulse width of the gate drive signal. An external MOSFET transistor is then turned on and off accordingly by the floating gate driver of the UC3827. The operating voltage of the floating driver can exceed the IC's bias supply, thus it can directly interface to an external switch up to 72V input voltage.

The converter's output voltage is regulated by the voltage error amplifier. Note, that all three amplifiers of the UC3827 are uncommitted amplifiers, i.e. all inputs and outputs are available. That makes the IC extremely adaptable to any control technique including voltage mode control with or without input voltage feedforward, voltage mode control with average current mode short circuit protection, traditional peak

current mode control or even average current mode control. These different control techniques can be implemented by modifying the interconnections among the amplifier pins.

The different setup possibilities are depicted in the next few figures.

The first version as shown in Figure 18, is simple voltage mode control. The voltage error amplifier output is compared to the sawtooth waveform of the timing capacitor to determine the pulse width of the gate drive signal. Since the other two amplifiers are not used, their outputs are forced to a neutral state, not to influence the circuit operation. Accordingly, the current sense amplifier output is forced to ground while the current error amplifier output is forced high.

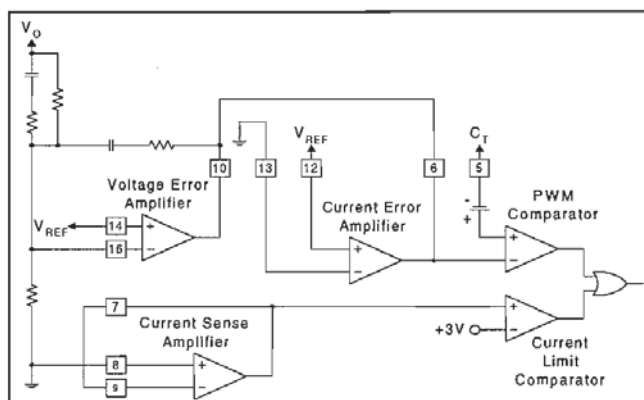


Figure 18. Simple Voltage Mode Control

Note, that the voltage and the current amplifier outputs are directly connected externally to the chip. The amplifiers of the UC3827 are designed with current limited asymmetrical outputs. The sink capability of the amplifiers is greater than their source capability. Therefore, OR connection of the amplifiers is possible without using diodes. This feature will be exploited several times later in other configurations. The advantages of voltage mode control are its simplicity and stable operation at light load when narrow duty-cycle is required. The disadvantages are that it can not protect the switches against excessive current stresses during overload condition and the output voltage is susceptible to rapid input voltage changes.

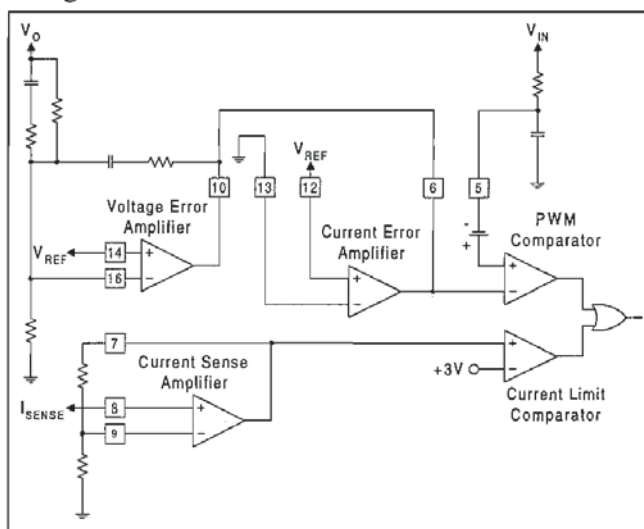


Figure 19. Voltage Mode Control with Input Voltage Feedforward And Peak Current Limit

The second arrangement in Figure 19, shows voltage mode control with input voltage feedforward and current protection of the main switch. For input voltage feedforward, the oscillator waveform is re-

placed by another sawtooth waveform, generated from the input voltage by a resistor and a capacitor. As shown in Figure 17, the ramp capacitor is discharged at the end of every switching cycle by an internal circuit driven from the clock synchronization pulse. Since the resistor is connected between the input voltage and the capacitor, the charge current of the capacitor varies with the input voltage producing a variable slope ramp signal. That signal is connected than to the RAMP pin providing the input voltage feedforward function. Current protection of the main switch is provided by the current sense amplifier and the current limit comparator. In this example, a positive polarity current sense signal is amplified by the current sense amplifier. The output of the current sense amplifier is compared to a 3V internal reference. If the current exceeds the level required to produce 3V at the output of the current sense amplifier, the gate drive signal is terminated immediately providing pulse-by-pulse primary side current limiting. This voltage mode method maintains the benefits of the previous one. Moreover, input voltage feedforward technique provides rejection of input voltage variation, while utilizing the current limit circuit can prevent catastrophic failures of the semiconductors.

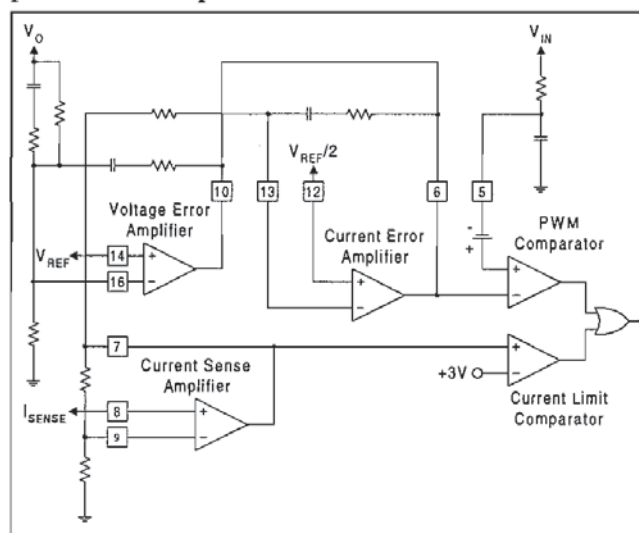


Figure 20. Voltage Mode Control With Input Voltage Feedforward And Average Current Mode Overload Protection

In Figure 20, another very popular voltage mode setup is displayed. In this version, two parallel control loops can be recognized. Under normal operation, the voltage loop which still incorporates input

voltage feedforward, determines the necessary pulse width. The voltage error amplifier is in its active mode while the current error amplifier idles. As the current increases in the converter the amplified current signal reaches the preset level on the noninverting input of the current error amplifier. At that point, the current loop takes over the duty cycle control and the voltage error amplifier becomes disengaged. In addition to all the benefits of the previous implementations, this circuit provides average current mode control during overload and short circuit condition when the voltage loop is open. That allows precise control of short circuit current and full protection of the entire circuit.

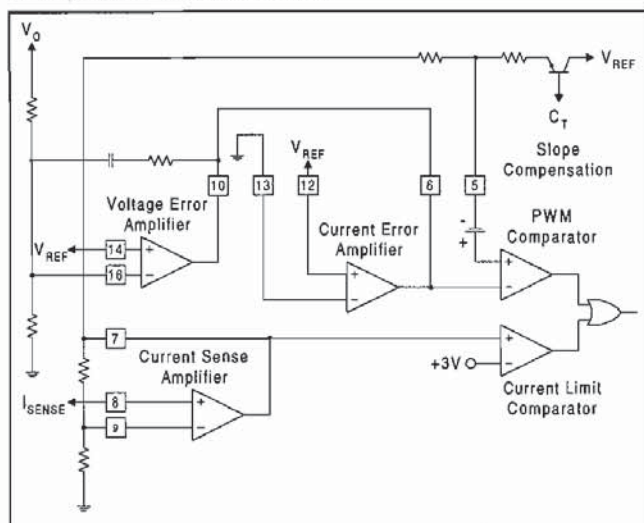


Figure 21. Peak Current Mode Control

In peak current mode control, the ramp pin receives the sum of the amplified current information and slope compensation as shown in Figure 21. The current sense amplifier is left in the circuit to allow using a low value current sense resistor and in order to utilize the whole control range of the amplifiers. Furthermore, the current limit comparator can provide additional current protection for the switching transistors. Note, that the compensation network around the voltage error amplifier is simplified accentuating the single pole transfer function of the power stage in current mode control. Peak current mode control offers simple voltage loop compensation, inherent input voltage feedforward and current protection. The known disadvantages are noise sensitivity, multiple control loops, the need of slope compensation and the troublesome operation under light

load condition due to the leading edge spike in the current waveform.

Average current mode control is considered the ultimate control technique in power supply design. A typical implementation is demonstrated in Figure 22.

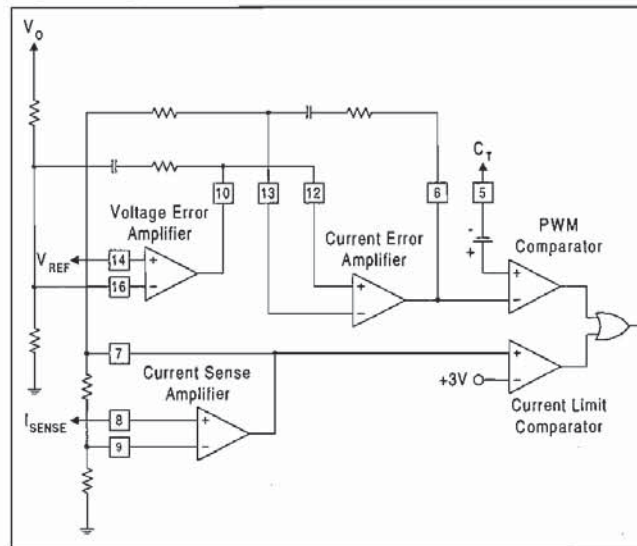


Figure 22. Average Current Mode Control

In this traditional setup, the voltage error amplifier processes the output voltage information through the feedback divider. The voltage error amplifier output signal, proportional to the voltage error, sets the reference value for the current error amplifier. The current error amplifier compares the amplified current signal to the voltage error signal and produces a current error voltage. This voltage, at the output of the current error amplifier is the control voltage for the PWM comparator. As Figure 22 reveals, the PWM comparator utilizes the timing capacitor waveform to determine the pulse width of the drive signal. Thus, average current mode control is less noise sensitive and more stable at light load than peak current mode control. Additional advantage of this technique is that slope compensation is not required for stable operation. As mentioned before, the major benefit using average current mode control is the precise control of the short circuit current and full protection of the entire circuit.

UC3827-1 Setup

This application employs the UC3827-1 integrated circuit for simple, cost effective implementation of all control functions. The schematic diagram is detailed in Figure 23. Power to the IC is provided

through a low value resistor which forms a low pass filter with the IC's local energy storage capacitors. The VCC pin is filtered by an electrolytic and a parallel connected high frequency ceramic capacitors. The bootstrap supply for the floating driver has its own 1 μ F local ceramic bypass capacitor. The bootstrap diode, D5 separates the gate drive circuit from the ground referenced control section during the ON time of the buck MOSFET transistor. Note, that the floating driver has its gate current limiting resistor in the source return path. This technique is used extensively in all floating driver circuits because the

source pin is inevitably forced to a negative potential when the freewheeling diode of the buck converter conducts. Placing the resistor to the source return lead, as shown in Figure 23, prevents the excessive negative voltage on the SRC pin and limits the current in those instances. The output drivers of the UC3827 are rated for 1A (BUCK) and 0.8A (PUSH and PULL) peak currents. Taking into consideration the internal gate resistances of the IRF3205s, 3 Ω gate resistors are used in this design to limit power dissipation and to damp oscillations in the gate drive circuits.

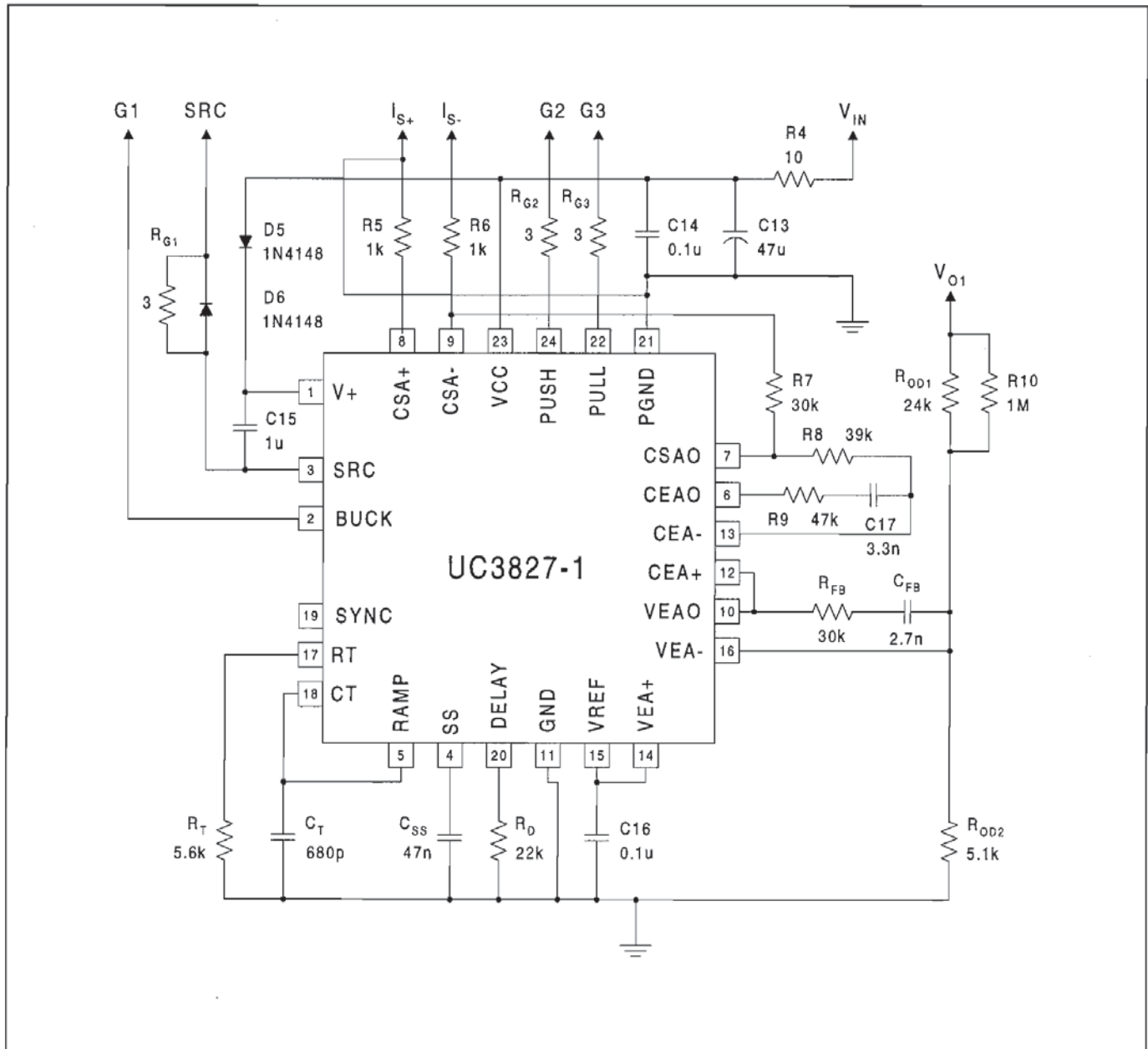


Figure 23. Controller Schematic

The clock frequency is set at the RT and CT pins of the UC3827. First the timing capacitor value is selected. It is important to keep in mind, that a stable clock is crucial for proper operation. Too small of a capacitor value will make the oscillator noise sensitive while too large of a value will increase power dissipation in the clock circuit and induce large current peaks in the sensitive analog circuitry during the discharge of C_T . This design uses a 680pF timing capacitor as a cautious compromise. The timing resistor value is calculated from the timing equation given in the datasheet:

$$R_T = \frac{0.77}{f_s \cdot C_T} \quad (42)$$

where f_s is 200kHz, C_T is 680pF and the equation yields a 5.6k Ω timing resistor.

Next the overlapping conduction time of the push-pull outputs are designed. Again, using the relationship from the datasheet:

$$R_D = t_D \cdot 150 \frac{\Omega}{\text{ns}} \quad (43)$$

where t_D is in nanoseconds. Using $t_D=150\text{ns}$, R_D equals to 22.5k Ω .

The UC3827 incorporates a soft-start function. The ramp up time of the error amplifier output voltage depends on how quickly the soft-start capacitor is charged from approximately 0.3V to 3V which is the useful control range of that amplifier. Using the typical value of the soft start capacitor charge current, I_{SS} , the soft start interval equals:

$$t_{SS} = \frac{C_{SS}}{I_{SS}} \cdot (3V - 0.3V) \quad (44)$$

Using a 0.047 μF soft start capacitor gives approximately 10ms soft start duration.

The current sense amplifier gain is calculated from the I_{MAX} and R_{SENSE} values. The 3V threshold of the current limit comparator shall be triggered when I_{MAX} is reached which requires a current sense amplifier gain of:

$$A_{CSA} = \frac{3V}{I_{MAX} \cdot R_{SENSE}} \quad (45)$$

yielding $A_{CSA}=30$.

Next the gain of the average current loop is investigated. The gain at the switching frequency can be defined using the slope matching technique as described in reference [3]. In this method, the representation of the buck inductor current downslope at the output of the current error amplifier is made equal (or smaller) to the slope of the timing capacitor voltage waveform. The maximum gain at the switching frequency can be obtained from:

$$A_{CEA,MAX} = \frac{\Delta C_T}{T} \cdot \frac{L}{V_{CT}} \cdot \frac{1}{R_{SENSE} \cdot A_{CSA}} \quad (46)$$

where ΔC_T is the amplitude of the timing capacitor waveform, T is the switching period, L is the buck inductor, V_{CT} is the voltage on the center tap of the push-pull transformer during energy transfer, R_{SENSE} is the current sense resistance and A_{CSA} is the gain of the current sense amplifier. The result of (46) is $A_{CEA,MAX}=1.75$. The actual gain, as shown in Figure 23, is set by R9 and R8 to 47k Ω /39k Ω =1.2 to provide some margin for component tolerances and variation in operating conditions. The capacitor, C17 was added to the feedback loop of the amplifier to boost the DC gain of the amplifier. The zero introduced by C17 was placed to $f_z=1\text{kHz}$. The required capacitance is given by:

$$C17 = \frac{1}{\omega_z \cdot R9} \quad (47)$$

The resultant capacitor value is 3.3nF.

The feedback divider has to be calculated next. The noninverting input of the voltage error amplifier is directly connected to the 5V reference of the chip. Therefore, the feedback divider has to provide 5V at the noninverting input of the amplifier at nominal output voltage, $V_{O1}=28V$. Selecting the lower member of the divider, $R_{OD2}=5.1\text{k}\Omega$, R_{OD1} is defined as:

$$R_{OD1} = \frac{(V_{O1} - V_{REF})}{V_{REF}} \cdot R_{OD2} \quad (48)$$

For exactly 28V output voltage, $R_{OD1}=23.46\text{k}\Omega$, which is realized by the parallel combination of a 24k Ω and a 1M Ω resistors.

Closing the voltage loop is the last step in the paper design phase. This article's primary focus is to give a practical design review, thus the loop stability analysis are omitted. For optimum loop design refer to reference [3], while a short-cut to a conservative solution with low crossover frequency of the voltage loop will be briefly explained here. For this simplified calculation, the first step is to simplify the outputs. The equivalent single output shall be normalized to the main output of the power supply then the equivalent output capacitor, ESR and load impedance values can be determined. Once the outputs are normalized to a single output rated to full power, the output impedances shall be transformed back to the primary side of the transformer. Be careful, the impedances transform by the square of the turns ratio. Now the problem is simplified to closing the voltage loop of a buck converter. If we take into consideration and assume that the average current loop is closed and stable, the control to output transfer function **at low frequencies** can be looked at as a voltage controlled current source (G_M stage) with a gain of:

$$G_{M,CONTROL \rightarrow OUTPUT} = \frac{I_{MAX}}{\Delta V_{EAO}} \quad (49)$$

The G_M stage is terminated by the transformed output capacitor in series with its ESR and by the load impedance as shown in Figure 24.

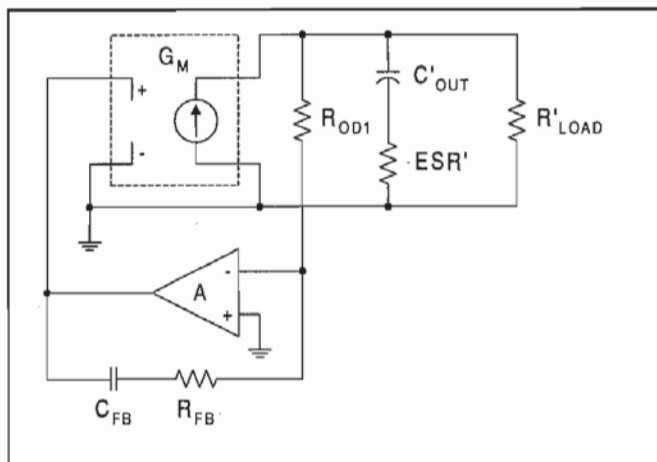


Figure 24. Voltage Loop Equivalent Circuit

From this equivalent circuit, the poles and zeros of the power stage are given and the compensation components of the voltage amplifier can be calculated. For a crossover frequency of $f_0=2\text{kHz}$, the re-

quired error amplifier gain at f_0 is approximately 2dB in this application, therefore the feedback resistor equals to $R_{FB}=30\text{k}\Omega$.

The zero in the error amplifier's feedback path is placed close to the crossover frequency to increase the DC accuracy of the voltage regulation. The capacitor value is given as:

$$C_{FB} = \frac{1}{\omega_0 \cdot R_{FB}} \quad (50)$$

which gives approximately $C_{FB}=2.7\text{nF}$.

Please, keep in mind, that this short-cut in closing the voltage loop works only at low frequencies i.e. when the voltage loop crossover frequency is in the couple of kilohertz range. This method does not account for any high frequency and second order effects nor the double pole at half of the switching frequency caused by the sampled data system.

Measurement Results

This chapter highlights some of the measurement data obtained from the breadboard. First, a couple of the characteristic waveforms of the circuit are displayed. Figure 25 shows the switched waveform at the source of Q1 and the inductor current waveform. One of the push-pull transistor's voltage and current waveforms is shown in Figure 26. Figure 27 gives the waveforms at the anodes of the output rectifier diodes, D1, D2 and D3 respectively.

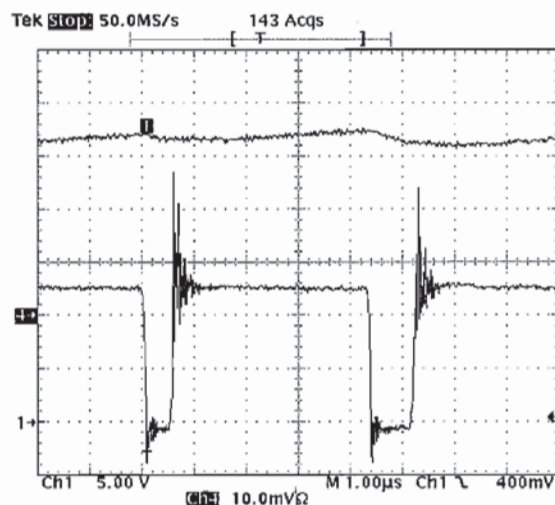


Figure 25. Buck Transistor Voltage and Inductor Current (5A/div) Waveforms

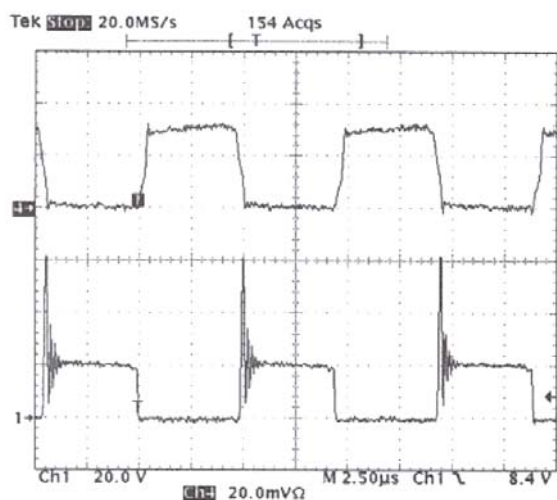


Figure 26. Q2 Current (10A/div) and Voltage Waveforms

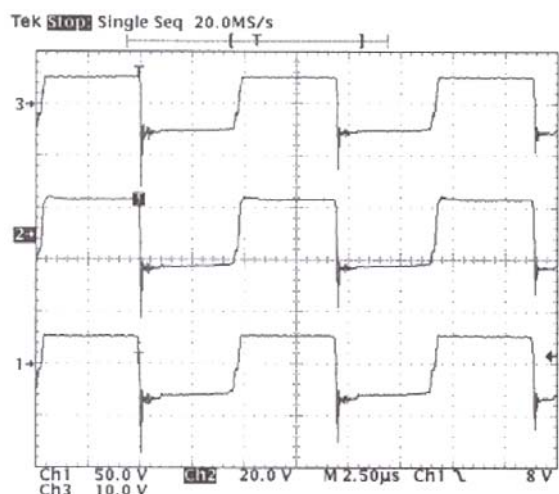


Figure 27. D1, D2 and D3 Switching Waveforms

The next three charts report cross regulation data. Figure 28 is the regulation of the 28V main output. Similar curves are generated for the two auxiliary outputs as shown in Figure 29 and Figure 30. The output regulation of V_{O3} is very close to the predicted value. On the other hand, V_{O2} performed worst than expected. The very likely cause of that relatively poor cross regulation behavior is the higher than expected resistances of N1 and N2, the 28V and 12V output windings of the prototype transformer. As Figure 31 shows, this effect also has an impact on the circuit efficiency demonstrated by the decreasing efficiency at higher load currents.

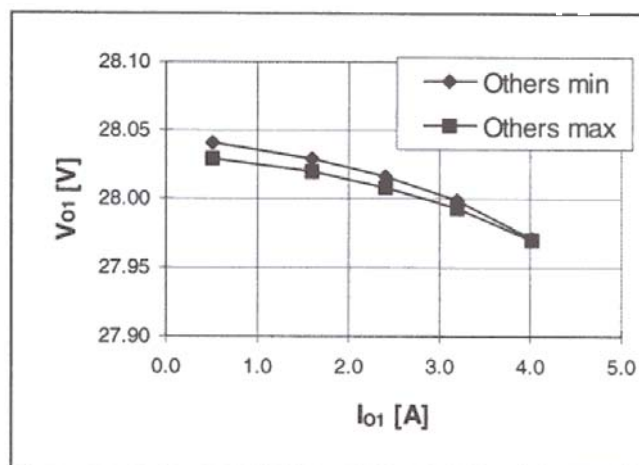


Figure 28. V_{O1} Line Regulation vs. Load Current

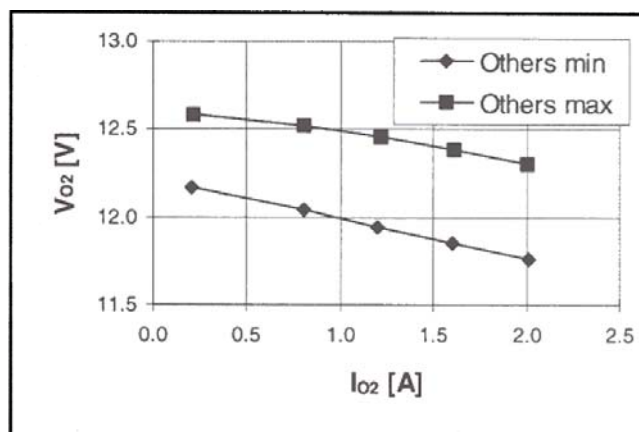


Figure 29. V_{O2} Line Regulation vs. Load Current

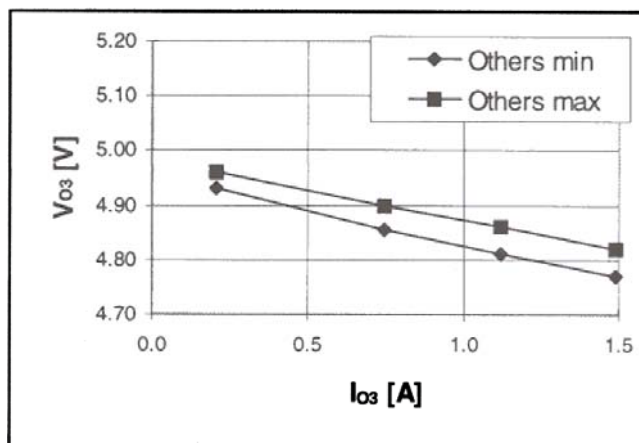


Figure 30. V_{O3} Line Regulation vs. Load Current

The efficiency of the circuit is indicated in Figure 31. On the horizontal axis, the summed output power of all three outputs is normalized to the maximum output power of 143W.

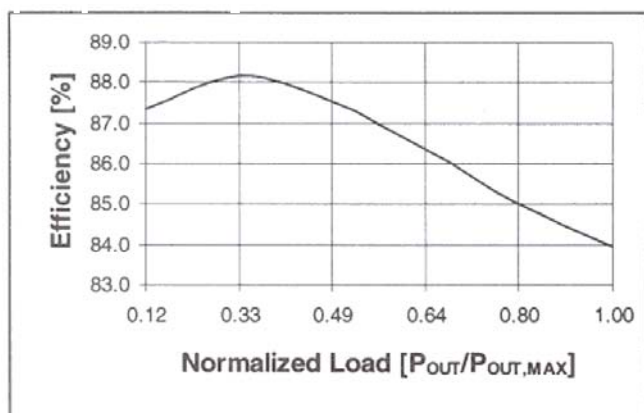


Figure 31. Efficiency vs. Normalized Load

As the graph shows, the efficiency peaks at about 88% then decreases due to the increasing resistive power losses. At full load, the efficiency is 84% which is close to the desired 85%. Once the circuit is built on a printed circuit board using the final planar magnetic components and optimized layout, it is very likely that the efficiency goal will be met.

SUMMARY

This topic has presented the most frequently used topologies for multi-output power supply design. Pros and cons of each implementation have been

listed in addition to the most popular application areas. The detailed design review of a three output current-fed push-pull converter culminated in the description of a step-by-step design procedure to insure meeting certain power supply specifications. The completed prototype circuit and the measurement results proved the effectiveness of the presented approach and the benefits of the selected topology.

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ATTACHMENT 1A

TI *Live!* POWER SUPPLY DESIGN SEMINAR

BASIC DESIGN PRINCIPLES
ADVANCED POWER-SUPPLY CONCEPTS
"REAL-WORLD" APPLICATION EXAMPLES

Here at TI, we are passionate about power. Browse through three decades of training content based on topics from our Power Supply Design Seminars (PSDS). Over the years, we have cultivated a reputation for being an essential training opportunity for power supply design engineers. The series provides technical and practical topics which combine new power-supply concepts, basic design principles, and "real-world" application examples. All content is accessible with a myTI login account.

[Top resources](#) | [2022 to 2020](#) | [2018 to 2010](#) | [2008 to 2000](#) | [1990s](#) | [1980s](#)

The top 10 resources from the past 30 years

Title	Year	White paper	Presentation	Video
Designing an LLC resonant half-bridge power converter	2010	Download (https://ti.com/lit/slup263)	Download (https://ti.com/lit/slup256)	—
Switch-mode power converter compensation made easy	2016	Download (https://ti.com/lit/slup340)	Download (https://ti.com/lit/slup341)	View (https://training.ti.com/switch-mode-power-compensation-made-easy?cu=1127730)
Under the hood of flyback SMPS designs	2010	Download (https://ti.com/lit/slup261)	Download (https://ti.com/lit/slup254)	—
Survey of resonant converter topologies	2018	Download (https://ti.com/lit/slup376)	Download (https://ti.com/lit/slup377)	View (https://training.ti.com/psds2018#sect)
Flyback transformer design considerations of efficiency and EMI	2016	Download (http://www.ti.com/lit/slup338)	Download (http://www.ti.com/lit/slup339)	View (https://training.ti.com/flyback-transformer-considerations-efficiency-and-emi?cu=1127)
Common mistakes in DC/DC converters and how to fix them	2018	Download (https://ti.com/lit/slup384)	Download (https://ti.com/lit/slup385)	View (https://training.ti.com/psds2018#sect)
Power-conversion techniques for complying with automotive emissions requirements	2020	Download (https://ti.com/lit/slup389)	Download (https://ti.com/lit/slup395)	View (https://training.ti.com/power-conversion-techniques-complying-with-automotive-emissions-requirements?content=1132272)

↑ Title	↑ Year	↑ White paper	↑ Presentation	↑ Video
Common mistakes in flyback power supplies and how to fix them	2020	Download (http://www.ti.com/lit/slup392)	Download (http://www.ti.com/lit/slup398)	View (https://training.ti.com/common-mistakes-fly-supplies-and-how-fix-them?context=1139938-1)
Constructing your power supply – layout considerations	2004	Download (https://ti.com/lit/slup230)	–	–
Power Factor Correction (PFC) circuit basics	2020	Download (https://ti.com/lit/slup390)	Download (https://ti.com/lit/slup396)	View (https://training.ti.com/power-factor-correction-circuit-basics?context=1139938-1140211)

2022 to 2020 resources

↑ Title	↑ Year	↑ White paper	↑ Presentation	↑ Video
Optimizing GaN-based high-voltage, high-power designs	2022	Download (https://ti.com/lit/slup412)	Download (https://ti.com/lit/slup405)	View (https://training.ti.com/node/1)
Supercapacitor and battery backup power supply design	2022	Download (https://www.ti.com/lit/ml/slup411/slup411.pdf)	Download (https://ti.com/lit/slup402)	View (https://training.ti.com/node/1)
Isolated gate-driver bias supply design considerations	2022	Download (https://ti.com/lit/slup401)	Download (https://ti.com/lit/slup401)	View (https://training.ti.com/node/1) (https://training.ti.com/node/114)
Low-noise and low-ripple techniques for a high-efficiency, low-loss supply without an LDO	2022	Download (https://ti.com/lit/slup409)	Download (https://ti.com/lit/slup404)	View (https://training.ti.com/node/1)
Advanced power converter features for reducing EMI	2022	Download (http://www.ti.com/lit/slup408)	Download (http://www.ti.com/lit/slup403)	View (https://training.ti.com/node/1)
Common mistakes in power supply layout and how to avoid them	2022	Download (https://ti.com/lit/slup407)	Download (https://ti.com/lit/slup406)	View (https://training.ti.com/node/1)
Power-conversion techniques for complying with automotive emissions requirements	2020	Download (https://www.ti.com/lit/slup389)	Download (https://www.ti.com/lit/slup395)	View (https://training.ti.com/power-cc-techniques-complying-automotive-emissions-requirements?context=1139938-11)
Power Factor Correction (PFC) circuit basics	2020	Download (https://www.ti.com/lit/slup390)	Download (https://www.ti.com/lit/slup396)	View (https://training.ti.com/power-factor-circuit-basics?context=1139938-11)
Voltage regulator design and optimization for high-current, fast-slew-rate load transients	2020	Download (https://www.ti.com/lit/slup391)	Download (https://www.ti.com/lit/slup397)	View (https://training.ti.com/voltage-regulator-optimization-high-current-fast-slew-rate-load-transients?context=1139938-1139912)
Common mistakes in flyback power supplies and how to fix them	2020	Download (https://www.ti.com/lit/slup392)	Download (https://www.ti.com/lit/slup398)	View (https://training.ti.com/common-mistakes-flyback-power-supplies-and-how-fix-them?context=1139945)
Designing a high-power bidirectional AC/DC power supply using SiC FETs	2020	Download (https://www.ti.com/lit/slup393)	Download (https://www.ti.com/lit/slup399)	View (https://training.ti.com/designing-a-high-power-bidirectional-acdc-power-supply-using-sic-fets?context=1139938-1139911)
Practical EMI considerations for low-power AC/DC supplies	2020	Download (https://www.ti.com/lit/slup394)	Download (https://www.ti.com/lit/slup400)	View (https://training.ti.com/practical-emi-considerations-for-low-power-acdc-supplies?context=11399)

2018 to 2016 resources

↑↓ Title	↑↓ Year	↑↓ White paper	↑↓ Presentation	↑↓ Video
Survey of resonant converter topologies	2018	Download (https://ti.com/lit/slup376)	Download (https://ti.com/lit/slup377)	View
Common mistakes in DC/DC converters and how to fix them	2018	Download (https://ti.com/lit/slup385)	Download (https://ti.com/lit/slup385)	View (https://training.ti.com/psds2018#secti
Considerations for measuring loop gain in power supplies	2018	Download (https://ti.com/lit/slup386)	Download (https://ti.com/lit/slup387)	View (https://training.ti.com/psds2018#secti
Control and design challenges for synchronous rectifiers	2018	Download (https://ti.com/lit/slup378)	Download (https://ti.com/lit/slup379)	View (https://training.ti.com/psds2018#secti
Comparison of GaN- and silicon FET-based active clamp flyback converters	2018	Download (https://ti.com/lit/slup380)	Download (https://ti.com/lit/slup381)	View (https://training.ti.com/psds2018#secti
Power solutions for class-D audio amplifiers	2018	Download (https://ti.com/lit/slup382)	Download (https://ti.com/lit/slup383)	View (https://training.ti.com/psds2018#secti
Bidirectional DC/DC converter topology comparison and design	2016	Download (https://ti.com/lit/slup342)	Download (https://ti.com/lit/slup343)	View (https://training.ti.com/bidirectional-dcdc-conve comparison-and-design?cu=1127730)
Design of a high-frequency series capacitor buck converter	2016	Download (https://ti.com/lit/slup336)	Download (https://ti.com/lit/slup337)	View (https://training.ti.com/design-high-frequency-se buck-converter?cu=1127730)
Design review of 350-W CCM PFC + LLC module	2016	—	Download (https://ti.com/lit/slup361)	View (https://training.ti.com/design-review-350-w-ccm-cu=1127730)
Design review of a 2-kW parallelable power-supply module	2016	Download (https://ti.com/lit/slup348)	Download (https://ti.com/lit/slup349)	View (https://training.ti.com/design-review-2-kw-parall supply-module?cu=1127730)
Designing low-EMI power converters for industrial & automotive systems	2016	—	Download (https://ti.com/lit/slup362)	View (https://training.ti.com/designing-low-emi-powe industrial-automotive-systems?cu=1127730)
Flyback transformer design considerations of efficiency and EMI	2016	Download (https://ti.com/lit/slup338)	Download (https://ti.com/lit/slup339)	View (https://training.ti.com/flyback-transformer considerations-efficiency-and-emi?cu=1127730)
Introduction to isolated topologies	2016	—	Download (https://ti.com/lit/slup357)	View (https://training.ti.com/introduction-isolated-t-cu=1127730)
Introduction to USB Type-C® & power delivery	2016	—	Download (https://ti.com/lit/slup360)	View (https://training.ti.com/introduction-usb-type-c-p-cu=1127730)
Power systems - design tools	2016	—	Download (https://ti.com/lit/slup358)	View (https://training.ti.com/power-systems-desi-cu=1127730)
Seven things to know about PMBus	2016	—	Download (https://ti.com/lit/slup359)	View (https://training.ti.com/seven-things-know-ab-cu=1127730)
SiC and GaN applied to high-frequency power	2016	Download (https://ti.com/lit/slup344)	Download (https://ti.com/lit/slup345)	View (https://training.ti.com/sic-and-gan-applied-high-power?cu=1127730)
Switch-mode power converter compensation made easy	2016	Download (https://ti.com/lit/slup340)	Download (https://ti.com/lit/slup341)	View (https://training.ti.com/switch-mode-power-c-compensation-made-easy?cu=1127730)
Under the hood of a noninverting buck-boost converter	2016	Download (https://ti.com/lit/slup346)	Download (https://ti.com/lit/slup347)	View (https://training.ti.com/under-hood-noninverting-converter?cu=1127730)

2014 to 2010 resources

Title	Year	White paper	Presentation
Choosing the right fixed-frequency buck regulator control strategy	2014	Download (https://ti.com/lit/slup317)	Download (https://ti.com/lit/slup317)
Choosing the right variable frequency buck regulator control strategy	2014	Download (https://ti.com/lit/slup319)	Download (https://ti.com/lit/slup319)
Control challenges for low-power AC/DC converters	2014	Download (https://ti.com/lit/slup325)	Download (https://ti.com/lit/slup325)
Examining wireless power transfer	2014	Download (https://ti.com/lit/slup321)	Download (https://ti.com/lit/slup321)
GaN FET-based CCM totem-pole bridgeless PFC	2014	Download (https://ti.com/lit/slup327)	Download (https://ti.com/lit/slup327)

↑ Title	↑ Year	↑ White paper	↑ Presentation
LLC converter small-signal modeling	2014	Download (https://ti.com/lit/slup329)	Download (https://ti.com/lit/slup329)
Under the hood of a multiphase-synchronous-rectified boost converter	2014	Download (https://ti.com/lit/slup323)	Download (https://ti.com/lit/slup323)
A design review of a full-featured 350-W offline power converter	2012	Download (https://ti.com/lit/slup300)	Download (https://ti.com/lit/slup300)
Accelerating power-supply compliance to specification	2012	Download (https://ti.com/lit/slup308)	Download (https://ti.com/lit/slup308)
Advanced digital controls improve PFC performance	2012	Download (https://ti.com/lit/slup310)	Download (https://ti.com/lit/slup310)
Design and optimization of a high-performance LLC converter	2012	Download (https://ti.com/lit/slup306)	Download (https://ti.com/lit/slup306)
Exposing the inner behavior of a quasi-resonant flyback converter	2012	Download (https://ti.com/lit/slup302)	Download (https://ti.com/lit/slup302)
Input EMI filter design for offline phase-dimmable LED power supplies	2012	Download (https://ti.com/lit/slup298)	Download (https://ti.com/lit/slup298)
Practical magnetic design: inductors and coupled inductors	2012	Download (https://ti.com/lit/slup304)	Download (https://ti.com/lit/slup304)
Designing a solar-cell-driven LED outdoor lighting system	2010	Download (https://ti.com/lit/slup267)	Download (https://ti.com/lit/slup267)
Designing an LLC resonant half-bridge power converter	2010	Download (https://ti.com/lit/slup263)	Download (https://ti.com/lit/slup263)
Designing magnetic components for optimum performance in low-cost AC/DC converter applications	2010	Download (https://ti.com/lit/slup265)	—
Dual half-bridge DC/DC converter with wide-range ZVS and zero-circulating current	2010	Download (https://ti.com/lit/slup266)	Download (https://ti.com/lit/slup266)
Incorporating active-clamp technology to maximize efficiency in flyback and forward designs	2010	Download (https://ti.com/lit/slup262)	Download (https://ti.com/lit/slup262)
Power factor correction using buck topology — efficiency benefits and practical design considerations	2010	Download (https://ti.com/lit/slup264)	Download (https://ti.com/lit/slup264)
Under the hood of flyback SMPS designs	2010	Download (https://ti.com/lit/slup261)	Download (https://ti.com/lit/slup261)

2008 to 2004 resources

Title	Year	White paper	Presentation
Applying digital technology to PWM control-loop designs	2008	Download (https://ti.com/lit/slup274)	Download (https://ti.com/lit/slup274)
High power factor and high efficiency — you can have both	2008	Download (https://ti.com/lit/slup268)	Download (https://ti.com/lit/slup268)
High-voltage energy storage: the key to efficient holdup	2008	Download (https://ti.com/lit/slup272)	Download (https://ti.com/lit/slup272)
Improving system efficiency with a new intermediate-bus architecture	2008	Download (https://ti.com/lit/slup271)	Download (https://ti.com/lit/slup271)
Under the hood of a DC/DC boost converter	2008	Download (https://ti.com/lit/slup270)	Download (https://ti.com/lit/slup270)
Understanding noise-spreading techniques and their effects in switch-mode power applications	2008	Download (https://ti.com/lit/slup269)	Download (https://ti.com/lit/slup269)
Using PMBus™ for improved system-level power management	2008	Download (https://ti.com/lit/slup273)	Download (https://ti.com/lit/slup273)
An interleaving PFC pre-regulator for high-power converters	2006	Download (https://ti.com/lit/slup279)	Download (https://ti.com/lit/slup279)

↕ Title	↕ Year	↕ White paper	↕ Presentation
Designing a digital power supply	2006	Download (https://ti.com/lit/slup281)	Download (https://ti.com/lit/slup281)
Designing planar magnetics	2006	Download (https://ti.com/lit/slup278)	Download (https://ti.com/lit/slup278)
Feedback in the fast lane — modeling extending current-mode control in high-frequency converters	2006	Download (https://ti.com/lit/slup277)	Download (https://ti.com/lit/slup277)
Green-mode power by the milli-watt	2006	—	Download (https://ti.com/lit/slup277)
Improving power supply efficiency — the global perspective	2006	Download (https://ti.com/lit/slup275)	Download (https://ti.com/lit/slup275)
Software design for digital power programming 101 for analog designers	2006	Download (https://ti.com/lit/slup280)	Download (https://ti.com/lit/slup280)
Compensating DC/DC converters with ceramic output capacitors	2004	Download (https://ti.com/lit/slup233)	—
Constructing your power supply — layout considerations	2004	Download (https://ti.com/lit/slup230)	—
Design review: a step-by-step approach to AC line-powered converters	2004	Download (https://ti.com/lit/slup229)	—
Interleaving contributes unique benefits to forward and flyback converters	2004	Download (https://ti.com/lit/slup231)	—
Safety considerations in power supply design	2004	Download (https://ti.com/lit/slup227)	—
Sequencing power supplies in multiple voltage rail environments	2004	Download (https://ti.com/lit/slup228)	—

2002 to 2000 resources

Title	Year	White paper	Presentation
Achieving high-efficiency with a multi-output CCM flyback supply using self-drive synchronous rectifiers	2002	Download (https://ti.com/lit/slup204)	—
Designing high-power factor off-line power supplies	2002	Download (https://ti.com/lit/slup203)	—
Paralleling power — choosing and applying the best technique for load sharing	2002	Download (https://ti.com/lit/slup207)	—
Transformer and inductor design for optimum circuit performance	2002	Download (https://ti.com/lit/slup205)	—
Under the hood of low-voltage DC/DC converters	2002	Download (https://ti.com/lit/slup206)	—
Understanding and optimizing electromagnetic compatibility in switch-mode power supplies	2002	Download (https://ti.com/lit/slup202)	—
Coupled filter inductors in multiple output buck regulators provide dramatic performance improvement	2001	Download (https://ti.com/lit/slup082)	—
Deriving the equivalent electrical circuit from the magnetic device physical properties	2001	Download (https://ti.com/lit/slup198)	—
Design and application guide for high-speed MOSFET gate drive circuits	2001	Download (https://ti.com/lit/slup169)	—
Designing stable control loops	2001	Download (https://ti.com/lit/slup173)	—
High-efficiency, regulated charge pumps for high-current applications	2001	Download (https://ti.com/lit/slup172)	—
How to design a transformer with fractional turns	2001	Download (https://ti.com/lit/slup200)	—
Magnetics design handbook (complete book)	2001	Download (https://ti.com/lit/slup132)	—
The effects of leakage inductance on switching power supply performance	2001	Download (https://ti.com/lit/slup199)	—

↑ Title	↑ Year	↑ White paper	↑ Presentation
A more accurate current-mode control model	2000	Download (https://ti.com/lit/slup122)	—
Frequency Response Measurements for Switching Power Supplies	2000	Download (https://ti.com/lit/slup121)	—
Hot swap power management	2000	Download (https://ti.com/lit/slup119)	Download (https://ti.com/lit/slup119)
Unique cascaded power converter topology for high-current low-output voltage applications	2000	Download (https://ti.com/lit/slup118)	—

1990s Resources

↑ Title	↑ Year	↑ White paper
A unique four quadrant flyback converter	1997	Download (https://ti.com/lit/slup122)
Current sensing solutions for power supply designers	1997	Download (https://ti.com/lit/slup121)
Design review: 140-W, multiple-output high-density DC/DC converter	1997	Download (https://ti.com/lit/slup119)
Control-loop cookbook	1996	Download (https://ti.com/lit/slup118)
Design considerations for active clamp and reset technique	1996	Download (https://ti.com/lit/slup117)
Design review: 100-W, 400-kHz, DC/DC converter with current doubler synchronous rectification achieves 92-% efficiency	1996	Download (https://ti.com/lit/slup116)
Fueling the megaprocessors — empowering dynamic energy management	1996	Download (https://ti.com/lit/slup115)
A 250-kHz, 500-W power factor correction circuit employing zero-voltage transitions	1994	Download (https://ti.com/lit/slup114)
Active clamp and reset technique enhances forward converter performance	1994	Download (https://ti.com/lit/slup113)
Design review: 500-Watt, 40-W/in ³ phase-shifted ZVT power converter	1993	Download (https://ti.com/lit/slup112)
Designing a phase-shifted Zero-Voltage Transition (ZVT) power converter	1993	Download (https://ti.com/lit/slup111)
Distributed power systems	1993	Download (https://ti.com/lit/slup110)
Snubber circuits: theory, design and application	1993	Download (https://ti.com/lit/slup109)
Fixed-frequency, resonant-switched pulse width modulation with phase-shifted control	1991	Download (https://ti.com/lit/slup108)
Load sharing with paralleled power supplies	1991	Download (https://ti.com/lit/slup107)
Practical considerations in high-performance MOSFET, IGBT and MCT gate drive circuits	1991	Download (https://ti.com/lit/slup106)
Average current-mode control of switching power supplies	1990	Download (https://ti.com/lit/slup105)
Isolating the control loop	1990	Download (https://ti.com/lit/slup104)
Optimizing the design of a high-power-factor switching preregulator	1990	Download (https://ti.com/lit/slup103)

1980s Resources

Title	Year	White paper
High-power-factor preregulator for off-line power supplies	1988	Download (https://ti.com/lit/slup102)
Resonant-mode converter topologies	1988	Download (https://ti.com/lit/slup101)
Design review: 150-Watt current-mode flyback	1986	Download (https://ti.com/lit/slup100)
Design review: A 300-W, 300-KHz current-mode half-bridge converter with multiple outputs using coupled inductors	1986	Download (https://ti.com/lit/slup99)
Practical considerations in current-mode power supplies	1986	Download (https://ti.com/lit/slup98)
The right-half-plane zero — a simplified explanation	1986	Download (https://ti.com/lit/slup97)

↕ Title	↕ Year	↕ White paper
Current-mode control of switching power supplies	1985	Download (https://ti.com)
Closing the feedback loop	1984	Download (https://ti.com)
Switching power supply topology review	1984	Download (https://ti.com)
250-Watt off-line forward converter — design review	1983	Download (https://ti.com)
Line input AC to DC conversion and input filter capacitor selection	1983	Download (https://ti.com)

ATTACHMENT 2

Fundamentals of Power Electronics

SECOND EDITION

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John G. Kassakian

Martin F. Schlecht

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Massachusetts Institute of Technology



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1.8-MHz, 48-V Resonant VRM: Analysis, Design, and Performance Evaluation

Laszlo Huber, *Member, IEEE*, Kevin Hsu, Milan M. Jovanović, *Fellow, IEEE*, Dennis J. Solley, Gennady Gurov, and Robert M. Porter

Abstract—A detailed analysis of operation and a basic design procedure for a new high-frequency (HF) resonant-converter technology with phase-shifted regulation is presented. The new HF resonant technology has a good potential to be a cost-effective solution for the voltage regulation modules (VRMs) for the next generations of microprocessor systems. The new HF resonant technology is employed in the development of a 1.8-MHz, 48-V, 130-W (0.95–1.7 V, 100 A) VRM. Experimental results are provided.

Index Terms—High-frequency (HF), phase-shifted regulations, resonant converter, voltage regulation modules (VRMs).

I. INTRODUCTION

TO FURTHER increase the processing speed and efficiency, future generations of microprocessor systems require lower operating voltages (below 1 V) at higher load currents (above 130 A) with high slew rates (up to 150 A/ μ s) [1]. High load currents with high slew rates and tighter output-voltage regulation windows require voltage regulation modules (VRMs) with fast transient responses. To achieve a fast transient response, the power conversion must be performed at higher switching frequencies (above 1 MHz). Higher switching frequencies enable controls with higher bandwidth feedback, which in turn require less output capacitance. As a result, only surface mount ceramic capacitors can be used at the output, which are less expensive and potentially more reliable than the commonly used electrolytic and tantalum capacitors. Further, at increased power levels, the 48-V distribution bus voltage is more feasible than the 12-V distribution bus voltage in order to keep the distribution losses low, especially for the high-end server and workstation applications [2]. To meet all these requirements, new high-performance VRM topologies and control technologies are needed.

Recently, a new high-frequency (HF) resonant-converter technology with phase-shifted regulation was introduced in [3] and [4]. This HF resonant technology has proven to be a cost-effective solution for VRMs for the next generation of microprocessor systems.

To facilitate the understanding of the new resonant technology, in this paper a detailed analysis of operation and a basic design procedure for the new HF resonant converter

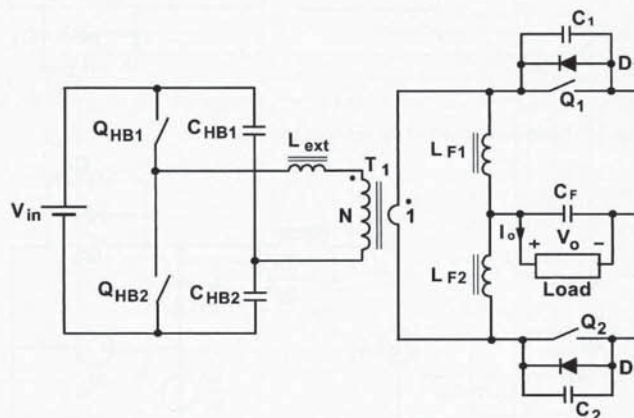


Fig. 1. Simplified circuit diagram of the new resonant converter [3], [4].

with phase-shifted regulation are presented. The new HF resonant-converter technology with phase-shifted regulation is employed in the development of a 1.8-MHz, 48-V, 130-W (0.95–1.7 V, 100 A) resonant VRM.

The paper is organized as follows. In Section II, a detailed analysis of operation is performed. In Section III, a basic design procedure is given. The implementation of the 1.8-MHz, 48-V, 130-W resonant VRM is presented in Section IV. Experimental results are provided in Section V.

II. ANALYSIS

A. Principle of Operation

The simplified circuit diagram of the new resonant converter with phase-shifted regulation is shown in Fig. 1. This is an isolated converter with a half-bridge inverter on the primary side and a current-doubler rectifier on the secondary side. The primary-side half-bridge inverter operates in open loop with 50% duty cycle and generates a rectangular (trapezoidal) ac voltage. The secondary-side current-doubler rectifier uses synchronous rectifiers Q_1 and Q_2 . Diodes D_1 and D_2 represent the body diodes of the synchronous rectifiers. For the resonant operation, an external inductor L_{ext} is added in series with the transformer primary winding, and capacitors C_1 and C_2 ($C_1 = C_2 = C$) are added in parallel to the synchronous rectifiers.

To simplify the analysis, it is assumed that output-filter inductances L_{F1} and L_{F2} and output-filter capacitance C_F are sufficiently large, so that they can be represented with current sources $I_o/2$ and a voltage source V_o , respectively, as shown in the equivalent circuit in Fig. 2. Also, it is assumed that synchronous rectifiers Q_1 and Q_2 are ideal, except for their output

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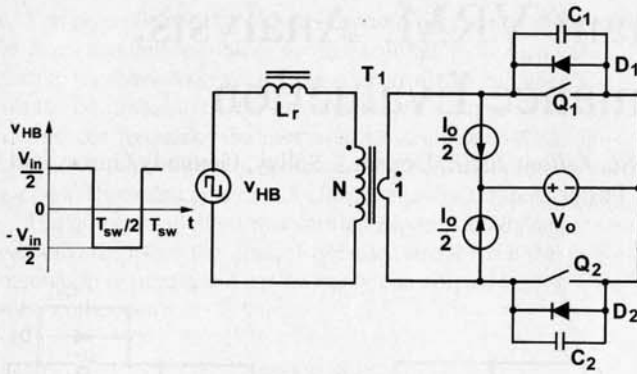


Fig. 2. Equivalent circuit of the new resonant converter.

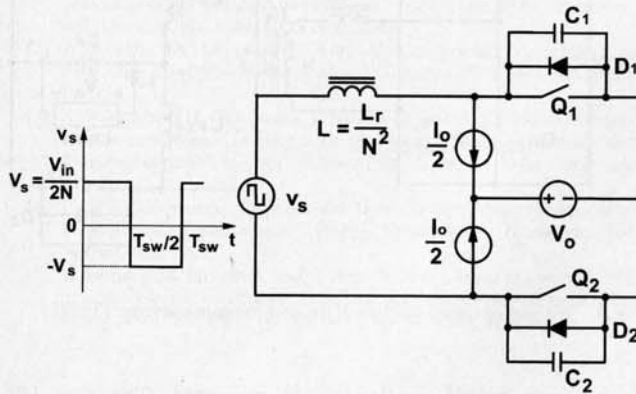
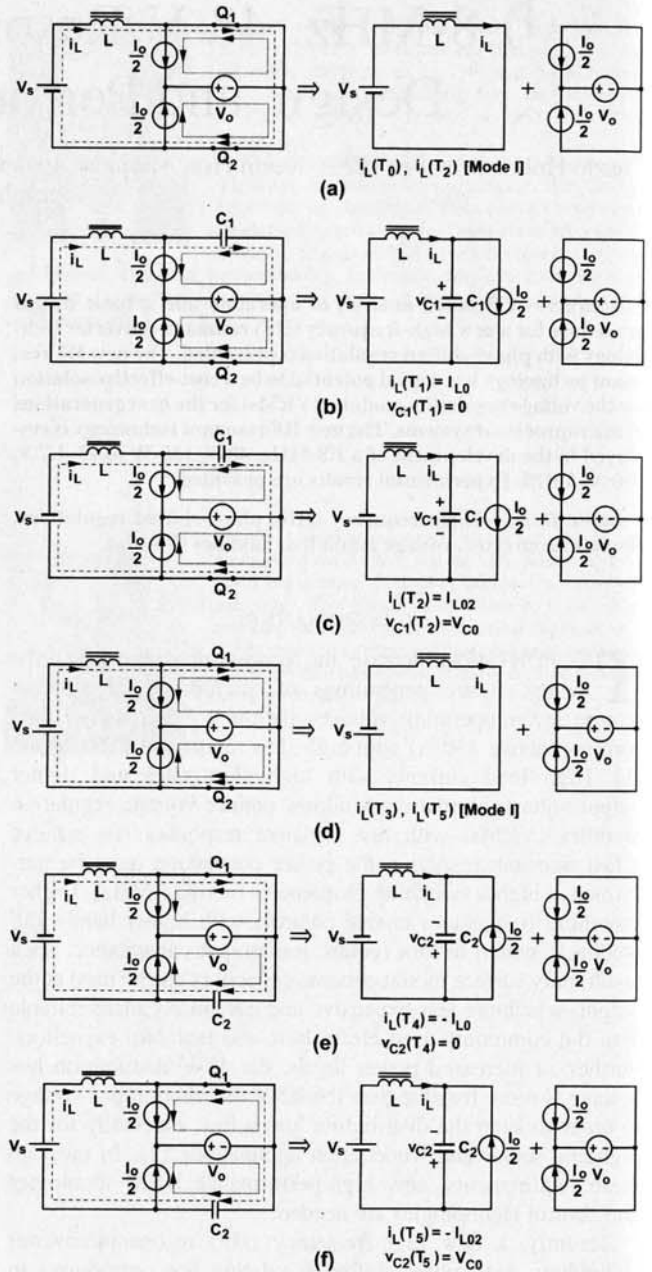


Fig. 3. Simplified equivalent circuit of the new resonant converter.

capacitances, which are included into the parallel resonant capacitances C_1 and C_2 . Finally, it is assumed that the magnetizing inductance of transformer T_1 is sufficiently large, so that it can be neglected, while the leakage inductance of the transformer is lumped with external inductance L_{ext} . The total primary-side inductance is denoted as resonant inductance L_r , as shown in Fig. 2. For simplicity, in Fig. 2, the primary-side half-bridge inverter in Fig. 1 is replaced by a rectangular ac voltage source v_{HB} . To further simplify the analysis, transformer T_1 in Fig. 2 is eliminated by transferring the whole primary-side circuit to the secondary side, as shown in Fig. 3. In Fig. 3, the transferred L_r from the primary side to the secondary side is denoted as L , while the transferred ac voltage source is denoted as v_s .

Under steady-state operation, six topological stages can be identified within a switching cycle T_{sw} , as shown in Fig. 4. These six topological stages can be arranged in two modes of operation. In the first mode of operation, the sequence of topological stages is (a) $\rightarrow$ (b) $\rightarrow$ (a) $\rightarrow$ (d) $\rightarrow$ (e) $\rightarrow$ (d), while in the second mode of operation the sequence of topological stages is (a) $\rightarrow$ (b) $\rightarrow$ (c) $\rightarrow$ (d) $\rightarrow$ (e) $\rightarrow$ (f). Key waveforms in the two modes of operation are presented in Figs. 5 and 6. In Mode I, shown in Fig. 5, the resonant voltage on capacitors C_1 and C_2 reaches zero before ac voltage v_s changes direction, while in Mode II, shown in Fig. 6, the resonant voltage on capacitors C_1 and C_2 reaches zero after ac voltage v_s changes direction. In Fig. 5, the solid-line and dotted-line waveforms of inductor current i_L and capacitor voltages v_{C1} and v_{C2} illustrate the operation at maximum load and zero load, respectively. In Fig. 6, only the waveforms at maximum load are presented. Ini-

Fig. 4. Topological stages: (a) $T_0 - T_1$, $T_2 - T_3$ [Mode I], (b) $T_1 - T_2$, (c) $T_2 - T_3$ [Mode II], (d) $T_3 - T_4$, $T_5 - T_6$ [Mode I], (e) $T_4 - T_5$, and (f) $T_5 - T_6$ [Mode II].

tial values of inductor current i_L and capacitor voltages v_{C1} and v_{C2} in each topological stage are also shown in Fig. 4.

During interval $[T_0 - T_1]$, Fig. 4(a), both switches, Q_1 and Q_2 , are on and the inductor current linearly increases as

$$i_L(t) = i_L(T_0) + \frac{V_s}{L}(t - T_0). \quad (1)$$

At $t = T_1$, switch Q_1 turns off and a resonance starts between L and C_1 . The equivalent resonant circuit is shown in Fig. 4(b). This is a series resonant circuit with a capacitor-parallel load. The initial conditions are

$$i_L(T_1) = I_{L0} \quad \text{and} \quad v_{C1}(T_1) = 0. \quad (2)$$

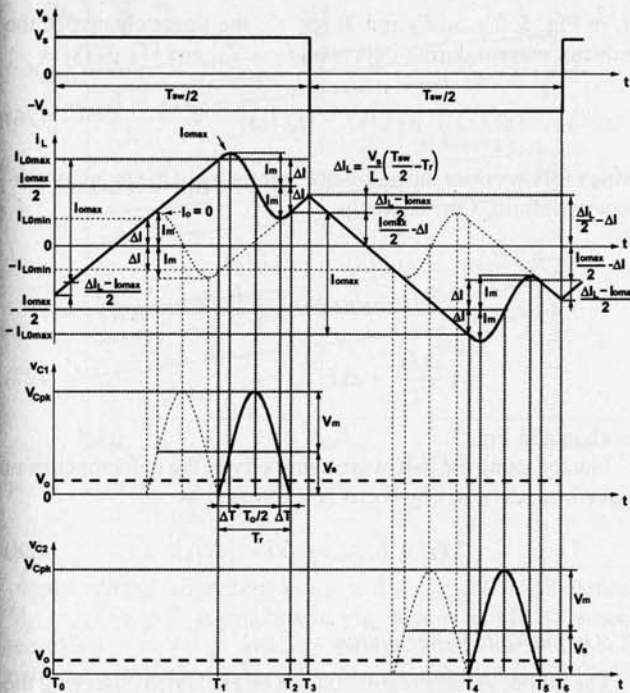


Fig. 5. Key waveforms in Mode I.

During the resonance, the inductor current and the capacitor voltage vary as [5]

$$i_L(t) = \frac{I_o}{2} + \Delta I \cdot \cos \omega_o(t - T_1) + \frac{V_s}{Z_c} \cdot \sin \omega_o(t - T_1) \quad (3)$$

and

$$v_{C1}(t) = V_s - V_s \cdot \cos \omega_o(t - T_1) + Z_c \Delta I \cdot \sin \omega_o(t - T_1) \quad (4)$$

where ΔI is defined as

$$\Delta I = I_{L0} - \frac{I_o}{2}; \quad (5)$$

$$\omega_o = \frac{2\pi}{T_o} = \frac{1}{\sqrt{LC}} \quad (6)$$

is the angular resonant frequency, and

$$Z_c = \sqrt{\frac{L}{C}} \quad (7)$$

is the characteristic impedance of the series resonant circuit in Fig. 4(b). Using the trigonometric angle-sum and angle-difference relationships, (3) and (4) can be rewritten as

$$i_L(t) = \frac{I_o}{2} + I_m \cdot \cos [\omega_o(t - T_1) - \Delta\theta] \quad (8)$$

and

$$v_{C1}(t) = V_s + V_m \cdot \sin [\omega_o(t - T_1) - \Delta\theta] \quad (9)$$

where

$$V_m = \sqrt{V_s^2 + (Z_c \Delta I)^2} \quad (10)$$

$$I_m = \frac{V_m}{Z_c} \quad (11)$$

and

$$\Delta\theta = \omega_o \Delta T = \arctan \frac{V_s}{Z_c \Delta I}; \quad 0 \leq \Delta\theta \leq \frac{\pi}{2}. \quad (12)$$

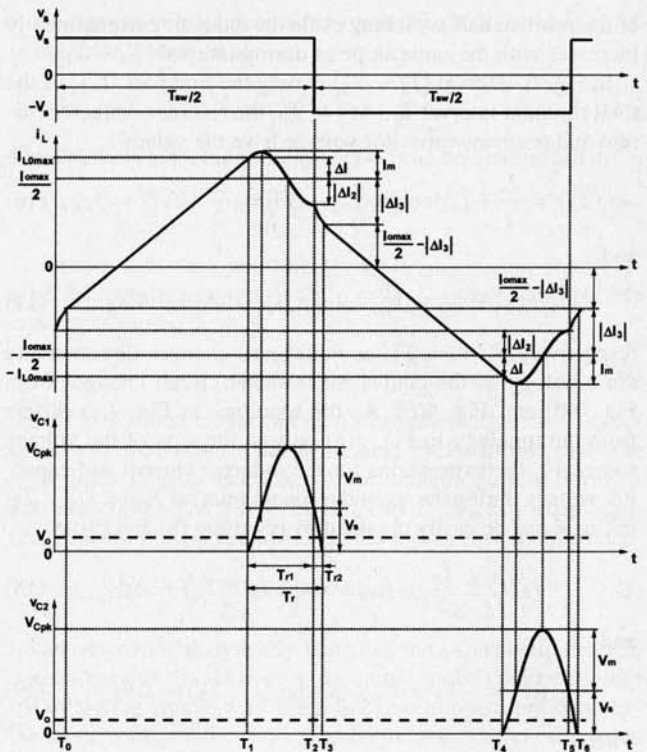
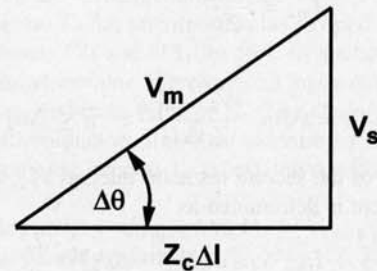


Fig. 6. Key waveforms in Mode II.


Fig. 7. Relationship between V_m , V_s , $Z_c \Delta I$, and $\Delta\theta$.

The relationship between V_m , V_s , $Z_c \Delta I$, and $\Delta\theta$, defined in (10) and (12) is also shown in Fig. 7.

The sinusoidal waveforms of the inductor current and capacitor voltage determined in (8) and (9), respectively, can be easily recognized in Figs. 5 and 6 during interval $[T_1 - T_2]$. In Fig. 5, interval $[T_1 - T_2]$ is the total resonant interval

$$T_r = \frac{T_o}{2} + 2 \cdot \Delta T. \quad (13)$$

At the beginning and at the end of the resonant interval T_r in Fig. 5, the resonant-inductor current is determined as

$$i_L(T_1) = \frac{I_o \max}{2} + \Delta I \quad (14)$$

and

$$i_L(T_2) = \frac{I_o \max}{2} - \Delta I \quad (15)$$

respectively, whereas, the resonant-capacitor voltage is equal to zero. Therefore, at $t = T_2$, switch Q_1 can be turned on with zero-voltage switching (ZVS). If $T_2 < T_3$, from T_2 until the end

of the positive half switching cycle the inductor current linearly increases with the same slope as during interval $[T_0 - T_1]$.

In Fig. 6, interval $[T_1 - T_2]$ is only the first part, T_{r1} , of the total resonant interval T_r . At $t = T_2$, the resonant-inductor current and resonant-capacitor voltage have the values

$$i_L(T_2) = \frac{I_o}{2} + I_m \cdot \cos[\omega_o T_{r1} - \Delta\theta] = \frac{I_o}{2} + \Delta I_2 = I_{L02} \quad (16)$$

and

$$v_{C1}(T_2) = V_s + V_m \cdot \sin[\omega_o T_{r1} - \Delta\theta] = V_{C0} \quad (17)$$

respectively. At $t = T_2$, ac voltage v_s changes direction and the topology of the equivalent resonant circuit changes from Fig. 4(b) and Fig. 4(c). As the topology in Fig. 4(c) differs from the topology in Fig. 4(b) only in the sign of the voltage source V_s , the expressions for the inductor current and capacitor voltage during the second resonant interval $T_{r2} = [T_2 - T_3]$ in Fig. 6 can be easily obtained by rewriting (8) and (9) as

$$i_L(t) = \frac{I_o}{2} + I_{m2} \cdot \cos[\omega_o(t - T_2) - \Delta\theta_2] \quad (18)$$

and

$$v_{C1}(t) = -V_s + V_{m2} \cdot \sin[\omega_o(t - T_2) - \Delta\theta_2] \quad (19)$$

where

$$V_{m2} = \sqrt{V_s^2 + (Z_c \Delta I_2)^2} \quad (20)$$

$$I_{m2} = \frac{V_{m2}}{Z_c} \quad (21)$$

and

$$\Delta\theta_2 = \omega_o \Delta T_2 = \tan^{-1} \frac{-V_s - V_{C0}}{Z_c \Delta I_2}; \quad \pi \leq \Delta\theta_2 \leq 2\pi. \quad (22)$$

At the end of the second resonant interval T_{r2} , the resonant inductor current is determined as

$$i_L(T_3) = \frac{I_o}{2} + I_{m2} \cdot \cos[\omega_o T_{r2} - \Delta\theta_2] = \frac{I_o}{2} + \Delta I_3 \quad (23)$$

whereas, the value of the resonant-capacitor voltage is zero, as shown in Fig. 6. Therefore, at $t = T_3$, switch Q_1 can be turned on with zero-voltage switching (ZVS). It should be noted in both Fig. 5 and Fig. 6 that at $t = T_1$, when switch Q_1 turns off, the switch current is equal to only ΔI , which means that the switch turns off with almost zero current switching (ZCS).

During the negative half cycle of a switching period T_{sw} , the behavior of the circuit is the same as during the positive half cycle. The only difference is that switches Q_1 and Q_2 change roles.

The total linear increase/decrease of the inductor current during a half switching cycle in both Figs. 5 and 6 is obtained as

$$\Delta I_L = \frac{V_s}{L} \left(\frac{T_{sw}}{2} - T_r \right). \quad (24)$$

It should be noted in Fig. 5 that if $T_3 = T_2$ and $T_6 = T_5$, i.e., if the termination of the resonant interval coincides with the end of a half switching cycle, $\Delta I_L = I_{o \max}$, because

$$i_L(T_3) - i_L(T_4) = \left(\frac{I_{o \max}}{2} - \Delta I \right) + \left(\frac{I_{o \max}}{2} + \Delta I \right) = I_{o \max}. \quad (25)$$

If, in Fig. 5, $T_3 > T_2$ and $T_6 > T_5$, the linear change of the inductor current during intervals $[T_3 - T_2]$ and $[T_6 - T_5]$ is

$$i_L(T_3) - i_L(T_2) = |i_L(T_6) - i_L(T_5)| = \frac{\Delta I_L - I_{o \max}}{2} \quad (26)$$

which follows from the half-wave symmetry of the inductor current waveform. Consequently

$$\begin{aligned} i_L(T_3) &= -i_L(T_6) = -i_L(T_0) \\ &= \frac{\Delta I_L - I_{o \max}}{2} + \left(\frac{I_{o \max}}{2} - \Delta I \right) \\ &= \frac{\Delta I_L}{2} - \Delta I \end{aligned} \quad (27)$$

as shown in Fig. 5.

Finally, using the half-wave symmetry of the inductor current waveform, ΔI_L in Fig. 6 can be expressed as

$$\Delta I_L = I_{o \max} + \Delta I - |\Delta I_3|. \quad (28)$$

B. Output Voltage Regulation

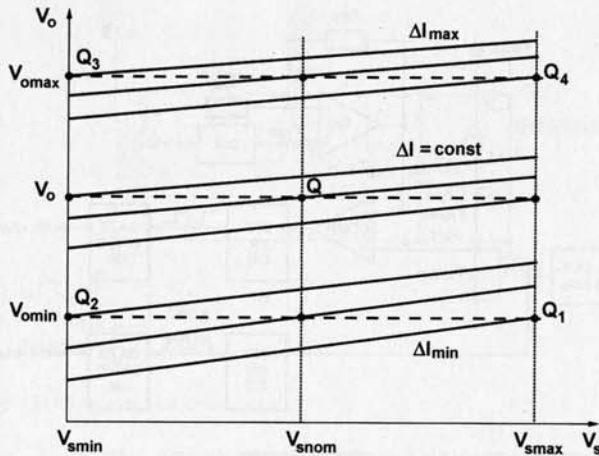
The output voltage regulation can be explained observing the waveforms in Fig. 5. The output voltage is equal to the average voltage across capacitor C_1 (or C_2) during a switching period T_{sw}

$$V_o = \frac{V_s}{\pi} \cdot \frac{T_o}{T_{sw}} \left(\frac{\pi}{2} + \tan^{-1} \frac{V_s}{Z_c \Delta I} + \frac{Z_c \Delta I}{V_s} \right). \quad (29)$$

It follows from (29) that the regulation of output voltage V_o versus load current variations, at a constant input voltage V_s , can be achieved by keeping ΔI constant. Because $\Delta I = I_{L0} - I_o/2$, as defined in (5), with increasing I_o , I_{L0} should also increase in order to keep ΔI constant. As illustrated in Fig. 5, the waveform of the ac component of the inductor current, $i_L - I_o/2$, which charges and discharges the resonant capacitor during the resonant interval T_r is the same at $I_{o \max}$ and $I_o = 0$. Therefore, the corresponding waveforms of the resonant-capacitor voltage at $I_{o \max}$ and $I_o = 0$ are identical and the output voltage is the same at $I_{o \max}$ and $I_o = 0$. However, the waveforms of the inductor current and capacitor voltage at $I_{o \max}$ are phase shifted compared to the corresponding waveforms at $I_o = 0$. In fact, with increasing load current the resonant interval T_r is more phase shifted with respect to the beginning of a half switching cycle.

Comparing the waveforms in Figs. 5 and 6, it can be seen that the phase shift of the resonant interval T_r in Fig. 6 is larger than the maximum possible phase shift in Fig. 5. In fact, by extending the operation of the circuit from Mode I in Fig. 5 to Mode II in Fig. 6, an additional phase shift can be achieved, i.e., the operation range of the circuit can be extended to larger load currents without changing the values of the resonant inductance and resonant capacitance. Because of the two resonant intervals, the output voltage in Mode II cannot be expressed in a simple closed form such as (29) in Mode I. Nevertheless, the output voltage regulation in Mode II is similar to the output voltage regulation in Mode I.

To facilitate the understanding of the output voltage regulation versus input voltage and load current variations in the whole

Fig. 8. $V_o = f(V_s, \Delta I)$ characteristics.

output-voltage range from $V_{o\min}$ to $V_{o\max}$, (29) which defines $V_o = f(V_s, \Delta I)$ is graphed in Fig. 8 as a family of characteristics $V_o = f(V_s)$ with ΔI used as a parameter. The four extreme operating points, $Q_1 - Q_4$, are also defined in Fig. 8. From Fig. 8, the following relationships can be observed:

- at $\Delta I = \text{constant}$, V_o increases approximately linearly with increasing V_s ;
- the slope of characteristics $V_o = f(V_s)$ slightly decreases with increasing V_o ;
- at $V_s = \text{constant}$, ΔI increases with increasing V_o ;
- at $V_o = \text{constant}$, ΔI decreases with increasing V_s ;
- $\Delta I = \Delta I_{\min}$ at $V_{s\max}$ and $V_{o\min}$ (operating point Q_1);
- $\Delta I = \Delta I_{\max}$ at $V_{s\min}$ and $V_{o\max}$ (operating point Q_3).

III. DESIGN

After selecting the switching frequency f_{sw} , the key design parameters are the turns ratio of the transformer N , the resonant inductance L , and the resonant capacitance C . Design constraints are defined in the four extreme operating points $Q_1 - Q_4$ in Fig. 8. To use the characteristics $V_o = f(V_s, \Delta I)$ in Fig. 8, first the turns ratio of the transformer should be selected.

After selecting the turns ratio of the transformer, resonant inductance L and resonant capacitance C can be obtained by considering the four extreme operating points in Fig. 8.

First, operating point $Q_1 = Q(V_{s\max}, V_{o\min})$ is considered. In operating point Q_1 , the regulation parameter $\Delta I = \Delta I_{\min}$. It follows from Fig. 5 and (12) that ΔI must have a positive value, i.e., $\Delta I \geq 0$. In addition, it follows from Fig. 8 that a larger $\Delta I_{\min}$ in operating point Q_1 results in a larger $\Delta I_{\max}$ in operating point Q_3 . Obviously, a larger $\Delta I_{\max}$ means larger rms values of the inductor current and switch current. Therefore, to obtain the smallest possible $\Delta I_{\max}$, the minimum value of the regulation parameter ΔI should be selected as

$$\Delta I_{\min} = 0. \quad (30)$$

It should be noted in Fig. 5 that at $\Delta I = 0$, ΔT increases to $T_o/4$, therefore, $T_r = T_o$, and the inductor-current waveform during the resonant interval T_r becomes a full sine wave, while the capacitor-voltage waveform becomes a full cosine wave.

The output voltage in operating point Q_1 at $\Delta I = \Delta I_{\min} = 0$ is obtained from (29) as

$$V_{o\min} = V_{s\max} \cdot \frac{T_o}{T_{sw}}. \quad (31)$$

Finally, from (31), the resonant period can be determined as

$$T_o = T_{sw} \cdot \frac{V_{o\min}}{V_{s\max}}. \quad (32)$$

Second, operating point $Q_2 = Q(V_{s\min}, V_{o\min})$ is considered. In operating point Q_2 , at $I_o = I_{o\max}$, the following time constraint can be defined:

$$T_1 - T_0 + T_r = \frac{T_{sw}}{2}, \quad (33)$$

which means that the termination of resonant interval T_r coincides with the end of a half switching cycle. In this case, the total linear increase/decrease of the inductor current during a half switching cycle, ΔI_L , is equal to $I_{o\max}$ as explained in (25). Substituting (13) and (12) in (24), ΔI_L is determined as

$$\Delta I_L = \frac{V_s}{L} \left(\frac{T_{sw}}{2} - \frac{T_o}{2} - \frac{T_o}{\pi} \cdot a \tan \frac{V_s}{Z_c \Delta I} \right). \quad (34)$$

It can be proven analytically that ΔI_L in (34) has minimum in operating point Q_2 . However, the same can be concluded with the following simple reasoning. Because in operating point Q_2 the input voltage is $V_s = V_{s\min}$, the inductor current increases with a minimum slope equal to $V_{s\min}/L$; therefore, the inductor current needs the longest time interval to increase by $I_{o\max}$. Further, along the vertical characteristic $V_s = V_{s\min}$ in Fig. 8, resonant interval T_r has maximum value in operating point Q_2 , as follows from (12) and (13). In fact, in operating point Q_2 , ΔI has a minimum value, therefore, ΔT has a maximum value, resulting in a maximum value of T_r . The longest time interval needed for the inductor current to increase by $I_{o\max}$ and the maximum resonant interval T_r satisfy the constraint defined in (33).

Substituting $\Delta I_L = I_{o\max}$ and $V_s = V_{s\min}$ in (34), it follows that in operating point Q_2

$$\frac{V_{s\min}}{L} \left(\frac{T_{sw}}{2} - \frac{T_o}{2} - \frac{T_o}{\pi} \cdot a \tan \frac{V_{s\min}}{Z_c \Delta I_{Q2}} \right) = I_{o\max}. \quad (35)$$

The product $Z_c \Delta I_{Q2}$ in (35) can be determined from (29), i.e.,

$$V_{o\min} = \frac{V_{s\min}}{\pi} \cdot \frac{T_o}{T_{sw}} \left(\frac{\pi}{2} + A \tan \frac{V_{s\min}}{Z_c \Delta I_{Q2}} + \frac{Z_c \Delta I_{Q2}}{V_{s\min}} \right). \quad (36)$$

After substituting $Z_c \Delta I_{Q2}$ from (36) in (35), the resonant inductance is obtained as

$$L = \frac{V_{s\min}}{I_{o\max}} \cdot \left[\frac{T_{sw}}{2} - \frac{T_o}{2} \cdot \left(1 + \frac{2}{\pi} \cdot a \tan \frac{V_{s\min}}{Z_c \Delta I_{Q2}} \right) \right]. \quad (37)$$

If the design includes Mode II in Fig. 6, then $I_{o\max}$ in (37) represents the maximum load current in Mode I in Fig. 5, which is, typically, 50%–75% of the total maximum load current.

Finally, the resonant capacitance is determined directly from (32) and (37) as

$$C = \frac{1}{L} \cdot \left(\frac{T_o}{2\pi} \right)^2. \quad (38)$$

Third, operating point $Q_3 = Q(V_{s\min}, V_{o\max})$ is considered. It can be proven analytically that the switches in Fig. 3

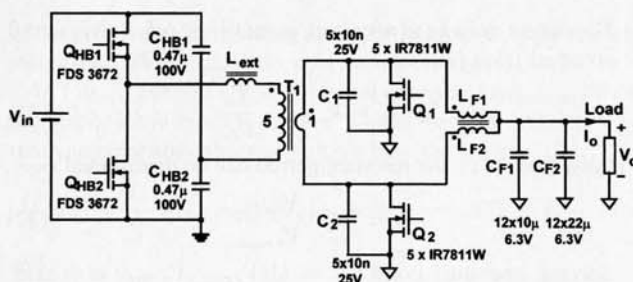


Fig. 9. Simplified circuit diagram of a 1.8-MHz, 48-V, 65-W VRM module.

have maximum voltage stress in operating point Q_3 . The voltage stress on the switches is determined by the peak value of the resonant-capacitor voltage, defined in Figs. 5 and 6 as

$$V_{Cpk} = V_s + V_m. \quad (39)$$

Substituting V_m from (10) in (39), the maximum voltage stress on the switches is determined as

$$V_{Qmax} = V_{smin} + \sqrt{V_{smin}^2 + (Z_c \Delta I_{max})^2}. \quad (40)$$

The maximum voltage stress on the switches determined by (40) is used for checking the proper selection of the turns ratio of the transformer. If the maximum voltage stress on the switches is smaller than the breakdown voltage of the switches with enough safety margin, it can be concluded that the turns ratio of the transformer was properly selected.

IV. IMPLEMENTATION OF 1.8-MHz, 48-V VRM

The 1.8-MHz, 48-V, 130-W VRM is implemented as two 65-W VRM modules connected in parallel. The current-source property of the VRM topology (L_{ext}) allows paralleling of two or more modules without special current-sharing precautions. The two VRM modules are implemented on the same printed circuit board (PCB). Each VRM module occupies half of the PCB area.

A. 65-W VRM Module

The simplified circuit diagram of one 1.8-MHz, 48-V, 65-W VRM module is shown in Fig. 9. The input voltage range is $48 \text{ V} \pm 10\% = 43.2\text{--}52.8 \text{ V}$. The output voltage range is 0.95–1.7 V. The maximum load current per VRM module is 50 A at 0.95–1.3-V output voltage range, while at 1.3–1.7-V output voltage range, the maximum load current is determined by the maximum output power of 65 W.

The primary-side half-bridge inverter is implemented with FDS3672 (100 V, 7.5 A, 22 mΩ) MOSFETs from Fairchild. Each of the secondary-side synchronous rectifiers Q_1 and Q_2 is implemented with five parallel IRF7811W (30 V, 14 A, 9 mΩ) MOSFETs from IR.

Transformer T_1 is implemented with planar cores PC50ER14.5/6-Z from TDK and with helical windings. The turns ratio of the transformer is $N = 5$. The primary-side magnetizing and leakage inductance of the transformer is around 25 μH and 90 nH, respectively. External resonant inductance L_{ext} is implemented with a toroidal core T37-2

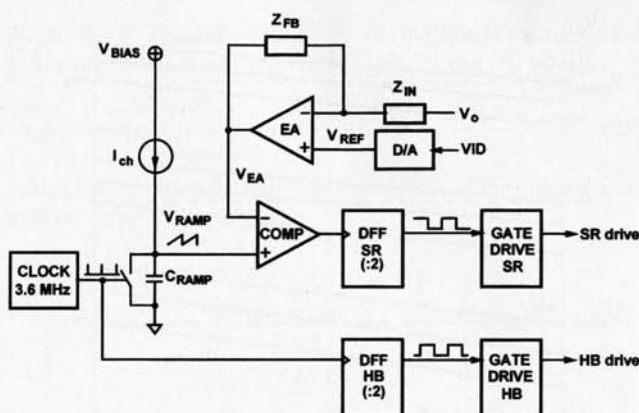


Fig. 10. Functional block diagram of the control circuit.

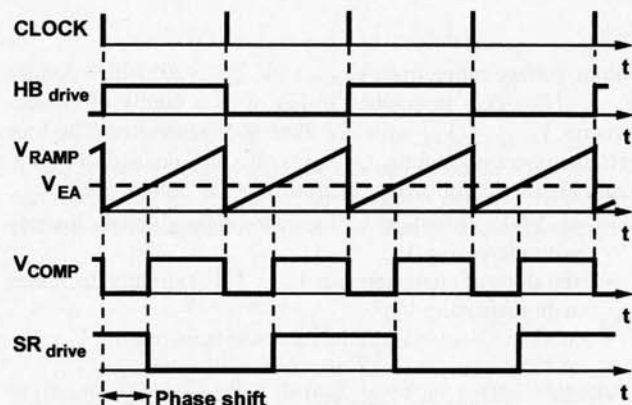


Fig. 11. Key waveforms of the control circuit.

from Micrometals and nine turns, two strands of $\phi 0.6$ wire. The inductance of L_{ext} is around 330 nH. Therefore, the total primary-side resonant inductance is around 420 nH.

Output-filter inductances L_{F1} and L_{F2} are coupled. They are implemented with two stacked planar EI cores 14/3.5/5 (3F3), with 1-mil air gap, and with single turn copper bars. The inductance of each L_{F1} and L_{F2} is around 80 nH.

Finally, output-filter capacitance C_F is implemented with surface mount ceramic capacitors. The whole output-capacitance bank is arranged in a 3×8 matrix form.

B. Control Circuit

The functional block diagram of the control circuit is shown in Fig. 10. Key waveforms are presented in Fig. 11. The clock signal in Fig. 10 has a frequency equal to 3.6 MHz. The two D flip-flops, DFF SR and DFF HB, operate as frequency dividers by 2. Therefore, the frequency of the SR and HB gate drive signals is equal to 1.8 MHz. The phase-shifted control is achieved by phase shifting the SR control pulses with respect to the HB control pulses. With increasing load current, error-amplifier voltage v_{EA} increases and, through the comparator, the phase shift of the SR control pulses increases with respect to the HB control pulses.

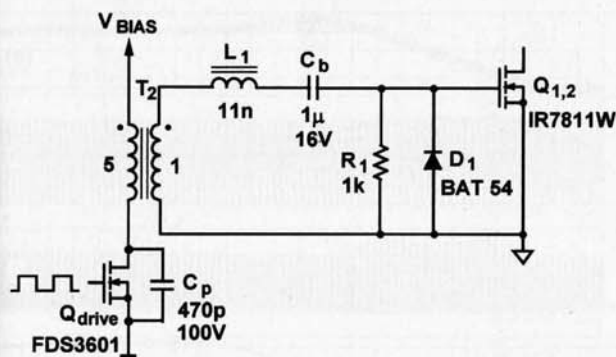


Fig. 12. Resonant gate drive circuit.

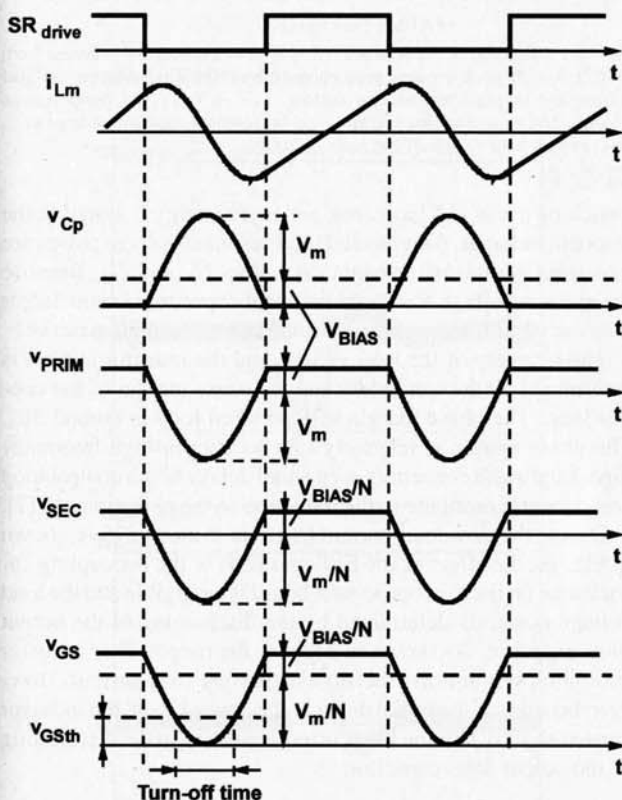
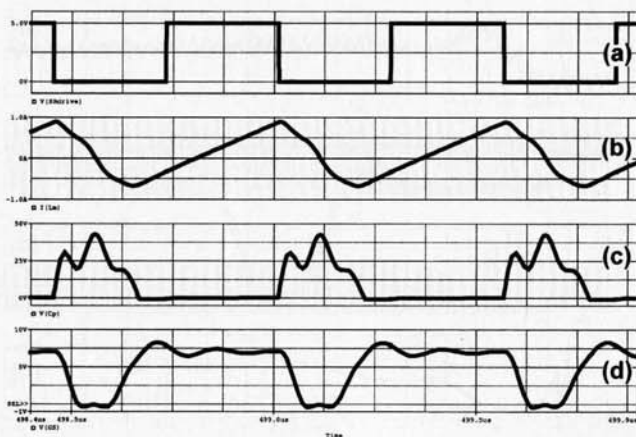


Fig. 13. Key waveforms of the resonant gate drive circuit.

C. Gate-Drive Circuit

The HB gate drive signals are applied to the gates of the HB switches through a gate-drive transformer. The HB switches operate with partial ZVS switching.

The SR gate drive signals are applied to the gates of the SRs through a resonant circuit. A resonant gate drive for the SRs at 1.8-MHz switching frequency is absolutely necessary because of the large input capacitance of the SR MOSFETs. The circuit diagram of the resonant gate drive for the SR's is shown in Fig. 12. Transformer T_2 is implemented with planar cores PC50ER9.5/5-Z from TDK with 4-mil gap. The turns ratio of the transformer is $N = 5$. The primary-side magnetizing inductance L_m is around 2 μH , while the leakage inductance is around 220 nH. Key waveforms are presented in Fig. 13. The waveforms in Fig. 13 are obtained for the simplified case when

Fig. 14. Key waveforms of the improved resonant gate-drive circuit obtained by PSPICE simulation: (a) SR_{drive} , (b) i_{Lm} , (c) v_{Cp} , and (d) v_{GS} .

$L_1 = 0$ and when the leakage inductance of T_2 is neglected. The basic operation of the resonant gate drive circuit in Fig. 12 is similar to the basic operation of the main resonant converter in Fig. 3. This can be concluded by comparing the waveforms of the resonant inductor current i_{Lm} and resonant capacitor voltage v_{Cp} in Fig. 13 with the corresponding waveforms in Fig. 5. It should be noted that the total resonant capacitance in Fig. 12 consists of capacitance C_p and the gate-source capacitance of the SR reflected to the primary side of the transformer. Bias capacitor C_b , resistor R_1 , and diode D_1 in Fig. 12 form a peak detector circuit, which automatically provides a bias voltage for the SR.

An improvement of the gate-drive voltage waveform can be achieved by adding inductor L_1 as shown in Fig. 12. By proper selection of inductance L_1 , a third harmonic can be injected in the gate-drive voltage waveform, which results in steeper edges and in an increased pulse width. Key waveforms of the improved resonant gate-drive circuit, obtained by PSPICE simulation, are presented in Fig. 14.

It should be noted that the width of the SR gate-drive pulses is critical for the proper operation of the resonant VRM. The resonant gate drive circuit in Fig. 12 generates gate-drive pulses of a constant width. However, the optimal width of the gate drive pulses varies with both the input and output voltages, as follows from (12) and (13). Therefore, with the resonant gate drive circuit in Fig. 12, optimal gate drive pulses can be obtained only for a narrow range of input and output voltages. Otherwise, if the generated pulse width is greater than the optimal pulse width, the body diode of the SR will conduct; or, if the generated pulse width is smaller than the optimal pulse width, the SR will turn on with hard switching. In both cases, the efficiency of the VRM will be reduced. Finally, if the generated pulse width is insufficient, the resonant VRM will oscillate. In applications, where the reduction of the efficiency is not acceptable, instead of the RCD bias circuit in Fig. 12, a controlled bias circuit has to be employed. A possible solution to take into account the effect of the input voltage on the SR gate drive is to design the auxiliary voltage supply V_{BIAS} to be proportional to the input voltage. If V_{BIAS} is generated as an isolated nonregulated voltage supply operating in an open loop, V_{BIAS} will be proportional to the input voltage. The effect of the output voltage can be taken into

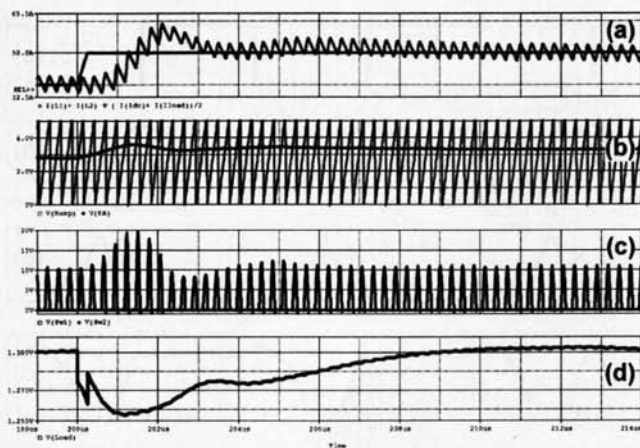


Fig. 15. Operation of the resonant VRM at fast load-current transient from 75 to 100 A with 100-A/ μ s slew rate, obtained by PSPICE simulation: (a) load current and output-filter inductor current $i_{LF1} + i_{LF2}$, (b) ramp voltage v_{RAMP} and error-amplifier voltage v_{EA} , (c) resonant-capacitor voltage v_{C1} , v_{C2} , and (d) load voltage (Time scale: 1 μ s/div).

account by a voltage-controlled voltage source connected in series with the secondary winding of the gate-drive transformer and controlled by the output voltage.

D. Load-Current Transients

Load-current transients are specified as fast load-current transients 75–100 A and 100–75 A with a 100 A/ μ s slew rate, and as slow load-current transients 0–75 A and 75–0 A with a 10 A/ μ s slew rate. The key requirement during the load-current transients is the maximum deviation of the output voltage, which is specified as $\pm 7\%$ of the desired output voltage.

The operation of the resonant VRM at fast and slow load-current transients is illustrated in Figs. 15 and 16, respectively. The waveforms in Figs. 15 and 16 are obtained by PSPICE simulation at the nominal input voltage of 48 V and the nominal output voltage of 1.3 V. The load includes 120- μ F decoupling capacitance on the microprocessor board. The connector between the VRM and the microprocessor board is modeled with 0.6-m Ω resistance and 400-pH inductance connected in series.

During the fast load-current transient from 75 to 100 A, shown in Fig. 15, the load voltage exhibits an initial drop, which is caused by the equivalent series inductance (ESL) and equivalent series resistance (ESR) of the decoupling capacitance on the microprocessor board. After the initial drop, the load voltage is determined by the discharging of the output filter capacitor because the output filter inductor current cannot follow the fast-increasing load current. The ramp-up of the output filter inductor current is mainly determined by the speed of the control loop. The closed loop bandwidth is around 125 kHz. As shown in Fig. 15, the rise time of the output filter inductor current is around five–six clock periods. If the response of the inductor current to the step change of the load current is approximated as a second-order system with the oscillation frequency close to the control loop bandwidth, the rise time of the inductor current can be approximated as a quarter of the oscillation period [6], i.e., $1/(4 \cdot f_c) \approx 2 \mu$ s. It should be noted in Fig. 15 that during the ramp-up of the inductor current, the increased error-amplifier voltage increases the phase shift of the SR control pulses with respect to the beginning of the

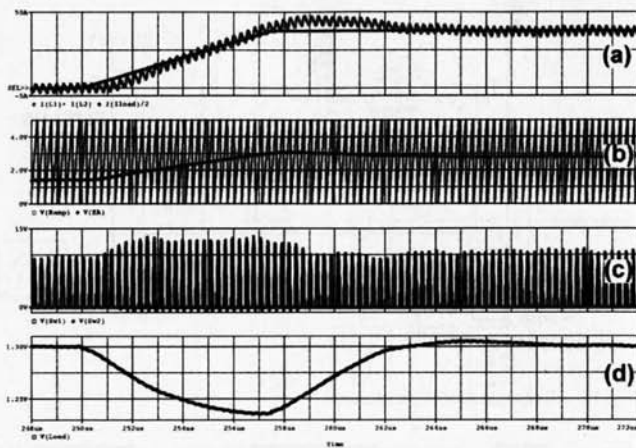


Fig. 16. Operation of the resonant VRM at slow load-current transient from 0 to 75 A with 10-A/ μ s slew rate, obtained by PSPICE simulation: (a) load current and output-filter inductor current $i_{LF1} + i_{LF2}$, (b) ramp voltage v_{RAMP} and error-amplifier voltage v_{EA} , (c) resonant-capacitor voltage v_{C1} , v_{C2} , and (d) load voltage (Time scale: 1 μ s/div).

switching cycle, ΔI increases, and more energy is stored in the resonant inductor. As a result, larger resonant voltage pulses are generated across the resonant capacitors C_1 and C_2 . Because the average voltage across the resonant capacitors is now larger than the output voltage, the inductor current will increase.

The recovery of the load voltage and the inductor current is determined by the bandwidth and the phase margin of the control loop. The phase margin of the closed loop is around 30° . The phase margin is relatively low because in high-frequency high-bandwidth converters even small delays of the control loop components contribute to the reduction of the phase margin [7].

During the slow load-current transient from 0 to 75 A, shown in Fig. 16, the effect of the ESL and ESR of the decoupling capacitance on the microprocessor board is negligible and the load voltage is mainly determined by the discharging of the output filter capacitor. As shown in Fig. 16, the output filter inductor current closely follows the slow increasing load current. However, because of the initial delay in the control loop, the inductor current slightly lags the load current, resulting in the discharging of the output filter capacitor.

E. Over-Load Protection

Typical VRM specifications require to shut down the converter in the case of an overload. The inherent current limiting feature of the resonant VRM (due to the series inductance) is very useful. In the case of an overload, the output voltage drops and the current limiting feature limits the instantaneous power delivered to the load at a level slightly higher than maximum power level of the converter. After that, an under-voltage protection mechanism shuts down the converter.

V. EXPERIMENTAL RESULTS

Efficiency measurements at nominal output voltage $V_o = 1.3$ V are shown in Fig. 17. These measurements were obtained before the output connector. The resistance of the output connector is 0.5–0.6 m Ω . Therefore, the maximum power loss of the output connector is around 5–6 W. The efficiency at the nominal input voltage of 48 V, at 50–100 A load current is around

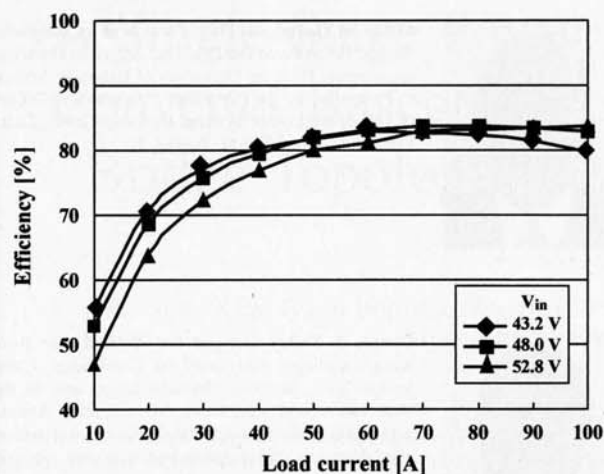


Fig. 17. Efficiency measurements at nominal output voltage $V_o = 1.3$ V.

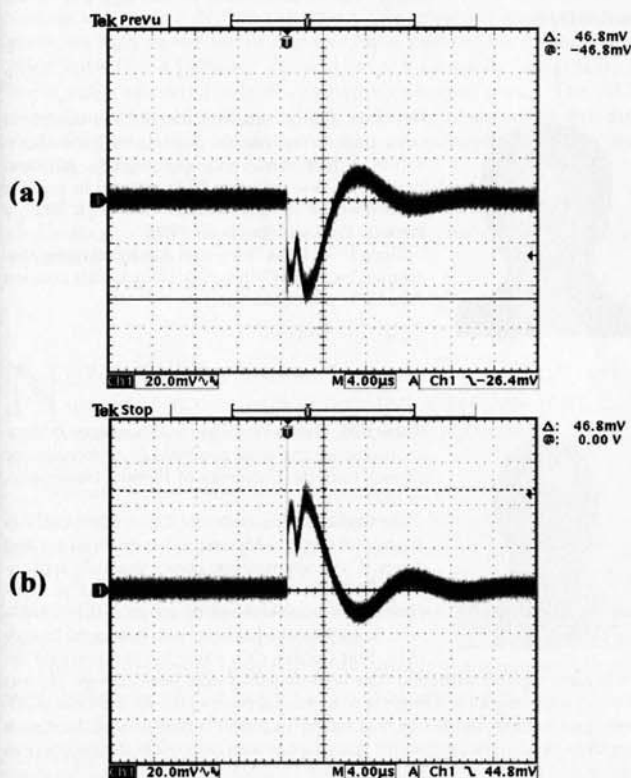


Fig. 18. Output voltage waveform at fast load-current transient (a) 75–100 A and (b) 100–75 A with 100 A/μs slew rate ($V_{in} = 48$ V, $V_o = 1.3$ V).

82%–84% before the output connector and around 80%–82% after the output connector.

Transient-response measurements obtained at nominal input voltage of 48 V and nominal output voltage of 1.3 V are shown in Figs. 18 and 19. Fig. 18(a) and (b) show the output voltage waveforms at fast load-current transients 75–100 A and 100–75 A, respectively, with a 100-A/μs slew rate, while Fig. 19(a) and (b) show the output voltage waveforms at slow load-current transients 0–75 A and 75–0 A, respectively, with a 10-A/μs slew rate. The maximum deviation of the output

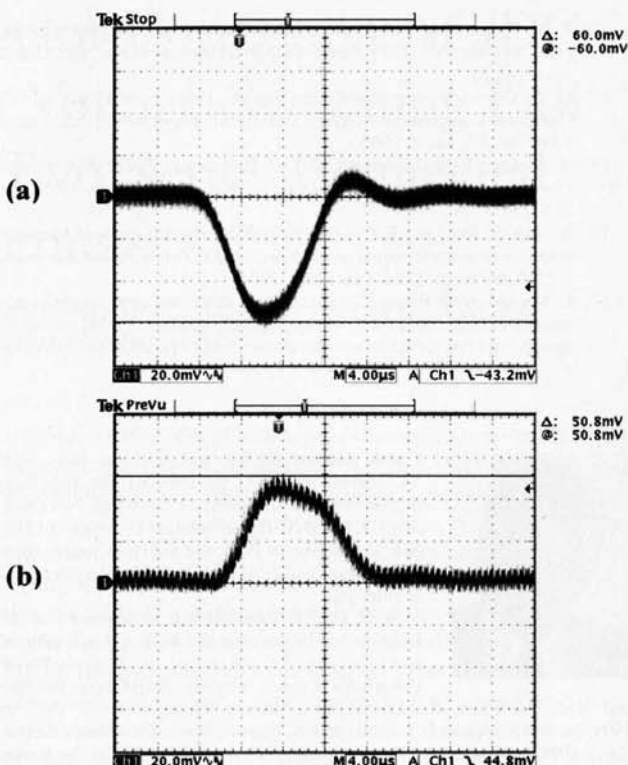


Fig. 19. Output voltage waveform at slow load-current transient (a) 0–75 A and (b) 75–0 A with 10-A/μs slew rate ($V_{in} = 48$ A, $V_o = 1.3$ V).

voltage at fast and slow load-current transients is around 47 mV and 60 mV, respectively. These results satisfy the specification requirement (7% of 1.3 V = 91 mV) with a large margin.

VI. CONCLUSION

The main features of the new high-frequency resonant converter technology with phase-shifted regulation [3], [4] can be summarized as follows:

- simple isolated topology: half-bridge inverter + current-doubler rectifier with synchronous rectifiers (SRs);
- topology suitable to utilize parasitics of components and layout;
- phase-shifted control with overlapping conduction of resonant SRs;
- resonant gate drive of resonant SRs;
- ZVS and partial ZCS of resonant SRs;
- only surface mount ceramic capacitors at the output;
- fast transient response;
- efficiency measured before the output connector around 82–84%;
- inherent current limit protection (due to series inductance);
- cost-effective.

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market segment.



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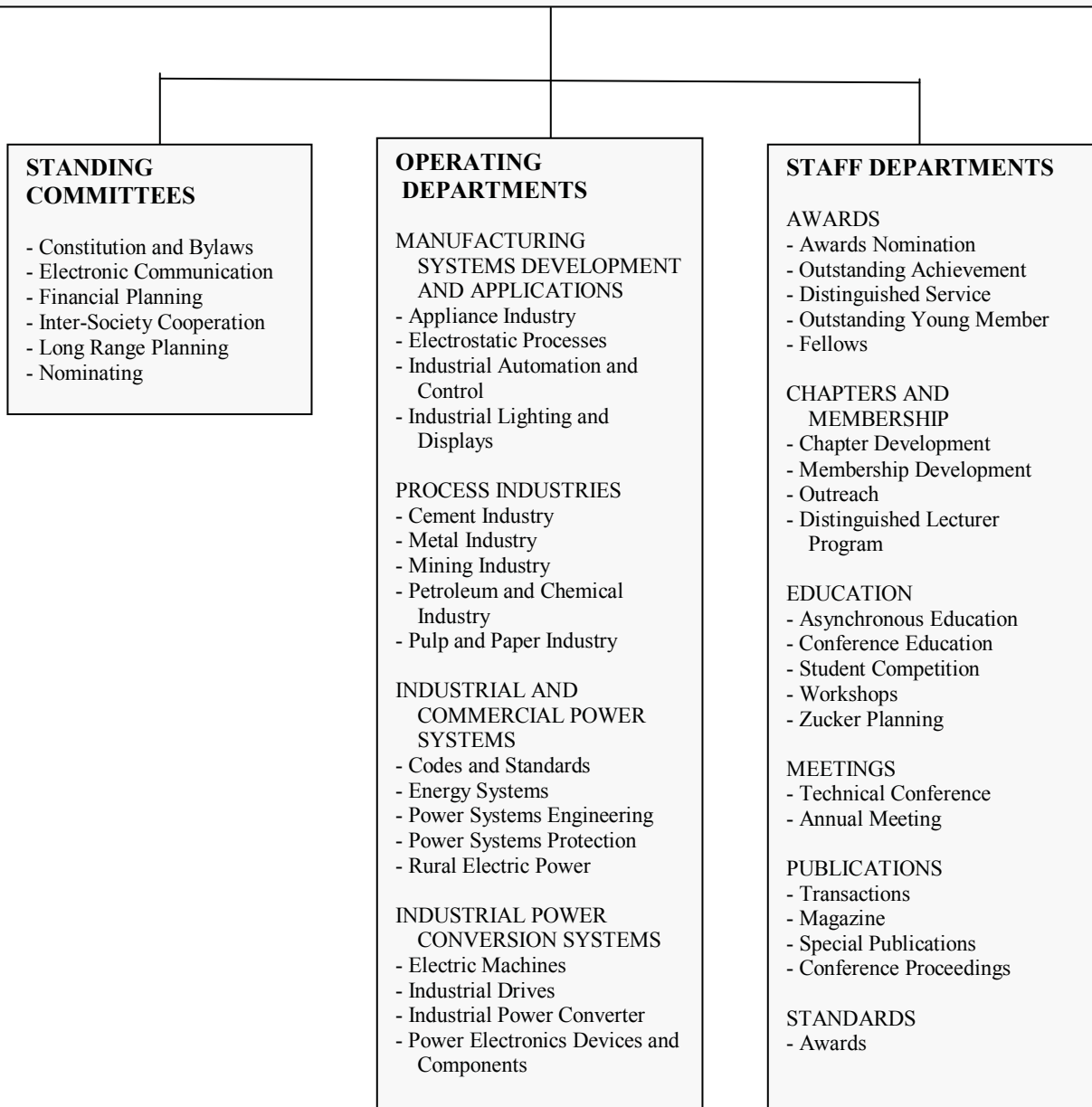
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Layout Considerations and Thermal Analysis of a 1.8 MHz Resonant VRM

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Abstract - Practical realization of modern high current and high switching frequency converters (with strong skin and proximity effects) requires a good control on layout-dependent parasitic components and on the power losses (thermal management), in order to meet the goal of high efficiency and reliability. In this paper, the physical realization of a VRM rated at 1.3 V - 50 A and switching at 1.8 MHz is analyzed in detail and discussed. Three prototypes, with same layout but different PCB structures and SR MOSFETs, have been tested. Moreover, an accurate thermal model was developed and experimentally validated in order to predict the maximum temperature of critical components.

I. INTRODUCTION

High frequency dc-dc converters for Voltage Regulator Module (VRM) applications require a great attention on the physical realization, in order to have a good control on layout-dependent parasitic components and on the power losses (thermal management). In fact, the combination of low voltage, high current at the output side and high switching frequency (strong skin and proximity effects), makes the goal of high efficiency and reliability a great challenge.

The aim of this paper is to analyze and discuss the physical realization of the 1.8 MHz VRM described in [1], by investigating both layout and thermal issues. It will be shown that component placement and routing have a strong impact not only on parasitic components, but also on the overall converter efficiency, thus affecting the thermal management. Three prototypes, with same layout but different PCB structures and SR MOSFETs (IRF7836 from International Rectifier and STS12NH3LL from STMicroelectronics), have been tested. Moreover, an accurate thermal model was developed in order to predict the maximum temperature of critical components.

In section II a brief review of the converter operation is given, while in section III the parasitic components are analyzed through discussion of different layout choices. Section IV reports an analysis of the converter losses distribution through suitable measurements. Section V reports the developed thermal model and its simulations, while section VI shows the results of thermal measurement of the PCB structures.

II. CONVERTER DESCRIPTION

The scheme of the 1.8 MHz resonant VRM described in [1] and its main waveforms are shown in Fig. 1, while table I reports specifications and main component values. As we can see, the primary switches operate with 50% duty-cycle supplying a fixed-frequency, fixed-amplitude, square-wave voltage to the converter. When the synchronous rectifier (SR) switches Q_1 and Q_2 are both conducting, the transformer secondary winding is short circuited so that the current i_R in the resonant inductor L_R has a pure triangular waveform. Then, switches Q_1 and Q_2 are alternatively turned off for a fixed amount of time, thus allowing the resonance between L_R and C_1 (C_2) to occur. The amplitude of the resonant voltages V_{C1} and V_{C2} is controlled by changing the delay of the SR turn off interval as respect to the primary switch drive signal, while the mean value of the voltage across the resonant capacitors is equal to the output voltage. From [1], the voltage conversion ratio is given by:

$$M = \frac{V_o}{V_s} = \frac{f_{sw}}{f_0} \frac{1}{\pi} \left(\frac{\pi}{2} + a \tan \left(\frac{V_s}{Z_c \Delta I} \right) + \frac{Z_c \Delta I}{V_s} \right) \quad (1)$$

where $Z_c = \sqrt{\frac{L_R}{N^2 C}}$ is the characteristic impedance,

$f_0 = \frac{1}{T_0} = \frac{N}{2\pi\sqrt{L_R C}}$ is the resonant frequency and

$V_s = V_{IN}/2N$. The quantity ΔI in (1) is defined as:

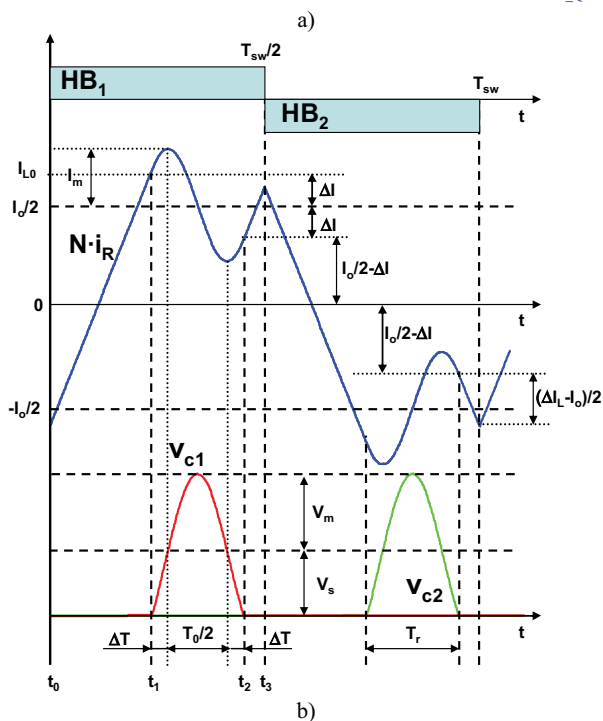
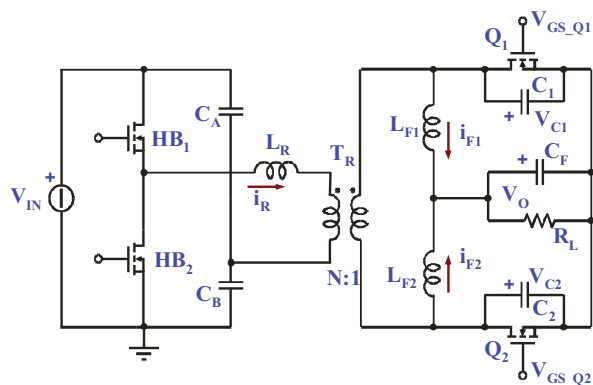
$$\Delta I = I_{L0} - \frac{I_o}{2}$$

where I_{L0} is the value of the resonant current reflected to the transformer secondary side at the SR's turn off instant, while I_o is the load current. From (1), it is possible to see that, in order to maintain the same voltage conversion ratio when the load is varying, it is sufficient to keep ΔI constant, by controlling the delay between the primary switch driving signal and the SR turn off instants.

For further details on the converter behavior and on the design criteria the interested reader should refer to the original paper [1]. Here, what we want to discuss, are some issues related to the physical realization of the converter prototype mainly related to the control of the parasitic components and to the thermal management. Moreover, no

TABLE I. CONVERTER SPECIFICATIONS AND COMPONENT VALUES

$V_{in} = 48 \text{ V} \pm 10\%$	$V_o = 1.3 \text{ V}$	$I_o = 50 \text{ A}$
$N = 5$	$L_R = 390 \text{ nH}$	$L_F = 100 \text{ nH}$
$C_1 = C_2 = 4 \times 10 \text{ nF} + 2 \times 4.7 \text{ nF}$	$C_F = 16 \times 10 \text{ }\mu\text{F}$	$C_A = C_B = 2 \times 470 \text{ nF}$

Figure 1. a) Scheme of the half-bridge resonant VRM described in [1]; b) main waveforms in a switching period ($V_s = V_{IN}/2N$)

electrical isolation between primary and secondary circuits was kept in order to simplify the control signal management.

III. CONTROL OF PARASITIC COMPONENTS

The key parameters for any high-frequency resonant converter are the resonant components, especially the resonant inductance. The latter, in fact, depends on parasitic components like the transformer leakage inductance, and the PCB trace inductance. The problem is exacerbated by the very high switching frequency that enhances skin and

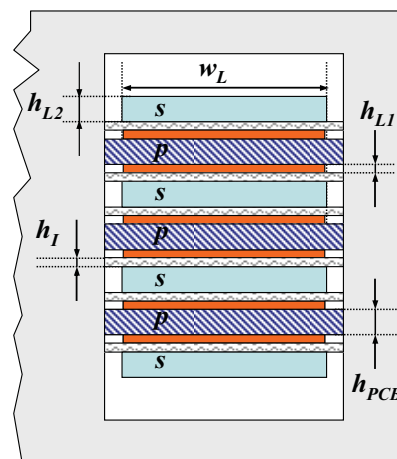


Figure 2. Transformer layer arrangement: p = primary layer, s = secondary layer (ER14.5/3/7 core 3F4 material)

proximity effects (at 1.8 MHz, the skin depth in copper at 100 °C is only 57 μm). Thus, a low leakage transformer is mandatory, calling for a high interleaved structure. The core employed was a planar ER 14.5/3/7 3F4 material from Ferroxcube and the windings were constructed by stacking thin double layer PCB sheets, for the primary five turns, and copper stamps for the single secondary turn. The layer arrangement is shown in Fig. 2 (from top to bottom): 1 turn secondary (copper stamp), 2 turns primary (first PCB sheet), 1 turn secondary (copper stamp), 1 turn primary (second PCB sheet with parallel connected traces, each on one side), 1 turn secondary (copper stamp), 2 turns primary (third PCB sheet), 1 turn secondary (copper stamp). All the primary turns are series connected while the four secondary stamps are parallel connected in order to reduce both dc and ac resistances. The winding physical dimensions are:

Copper stamp thickness h_{L2} :	200 μm
PCB trace thickness h_{L1} :	100 μm
PCB thickness h_{PCB} :	220 μm
Isolation sheet thickness h_I :	80 μm
Stamp and trace width w_L :	2.49 mm

Such arrangement gave a total leakage inductance of 61 nH, while the magnetizing inductance was 21 μH .

As far as the PCB trace inductances are concerned, they depend on both primary and secondary current paths, just like the losses associated to the PCB trace routing. One of the first layout we have experimented, used four SR MOSFETs parallel connected for each Q_1 and Q_2 all located on the same side of the PCB (see Fig. 3), with a ground plane on the opposite side of the PCB. Such arrangement gave high secondary losses mainly due to the strong proximity effect that causes a non uniform current distribution in the transformer secondary traces. Moreover, the strong vertical magnetic field produced by the secondary current (35 A peak, almost triangular current at 1.8 MHz) is likely to induce eddy currents on the ground plane, with associated losses. After a time consuming trial and error process, it has been recognized

that the only way to reduce both secondary parasitic inductance and ac resistance was to force the secondary current to flow on opposite layers in order to minimize the volume of the high magnetic field region (this provision gives benefit also from the electromagnetic compatibility point of view, by reducing the leakage magnetic field). Moreover, in order to force the current to spread over a large area on the PCB, the SR MOSFETs have been distributed and interleaved with the resonant capacitors C_1 and C_2 , each constituted by a parallel connection of four 10 nF and two 4.7 nF caps (5% tolerance).

As far as the position of the filter inductors L_{F1} and L_{F2} (one turn on a planar E14/3.5/5 core, 3F4 material from Ferroxcube) is concerned, they have been initially located on the edge of the PCB, as shown in Fig. 4 (prototype with two parallel connected SR MOSFETs for Q_1 and Q_2). Once again, such arrangement yield unacceptable performance in terms of power losses mainly due to a wrong current path (large area) and unequal current path length toward the resonant capacitors. The solution was to put the filter inductors in the middle of the SR MOSFETs in order to be equally displaced, as respect to the resonant capacitors, and to distribute symmetrically the filter capacitors C_F (eight 10 μ F caps on each side of the PCB).

Another crucial issue, strictly related to the converter losses, regards the techniques for removing the produced heat from the components in order to keep them at a reasonable maximum temperature. Having power components on both sides of the PCB, the only way to remove the heat was to

have a dissipating layer in between the two component layers, that was also used as ground connection at secondary side. Two different layouts were tested for the power stage: one using two layers of standard FR4 PCB (0.8 mm thickness) joined together to form an equivalent three layer PCB (see Fig. 5a) with an equivalent total inner layer thickness of 0.14 mm (PCB1), and the other built assembling two epoxy layers (0.5 mm thickness) on both sides of 0.7 mm thick copper baseplate shown in Fig. 5b (PCB2). As we can see, in the primary half bridge the layout employed followed the same philosophy used for the secondary circuit, i.e. the primary current follows a direct and return paths on different sides of the PCB (note the connection of the transformer to the capacitive node between C_A and C_B on the bottom layer). The resonant inductor was constructed with five turns of a Litz wire wound on a toroidal core (Micrometal T50-14 Powder Core).

Beside the components already mentioned above, the PCB includes the driver for the half bridge switches HB_1 and HB_2 (LM5101A from National) and a resonant driver for each SR MOSFET, different from the one proposed in [1], that was discussed in [2]. The latter employs a couple P-MOS and N-MOS on the same package (IRF7319) and exploits the internal 10 nH parasitic inductance (plus any external contribution from traces and layout) for charging and discharging in a resonant manner the SR MOSFET's gate equivalent capacitance.

The control signals, generated by a separate control circuit, are coupled with the power stage through the two connectors shown at the bottom edge of the PCB.

Finally, it is important to note that, even if the transformer secondary current loop has been minimized, the associated strong magnetic field could still cause significant losses due to eddy currents induced in the baseplate, whose thickness is not negligible (0.7 mm). In order to mitigate this problem, the baseplate was removed just inside the high field region.

IV. LOSSES DISTRIBUTION

In this section we want to discuss the converter power losses distribution that will be used for the thermal simulation of the PCBs. Due to the strong dependence on the layout, losses calculation is just an exercise, without any correlation with the reality. The only way is to measure them on the prototype, which is usually not an easy task. Fortunately, the resonant current resembles a triangular waveform, especially at nominal power: exploiting this similarity, we measured the losses of different components by operating the primary half-bridge with a short-circuit realized in different locations of the circuit (at the transformer's primary, at the transformer's secondary, by substituting the SR MOSFETs with copper strips, and by driving the SR MOSFETs with a constant V_{GS} voltage) and measuring the input power. The input voltage was adjusted any time in order to have a 7 A peak triangular resonant current i_R at primary side that roughly corresponds to the value measured at nominal power. The primary current has been measured with a small current transformer (6.4 mm

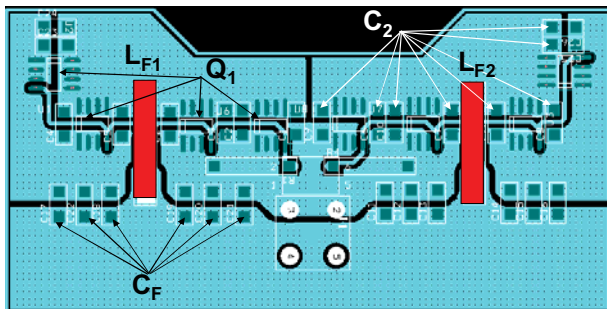


Figure 3. One experimented layout at the transformer secondary side with SR MOSFETs at the same PCB side (TOP view)

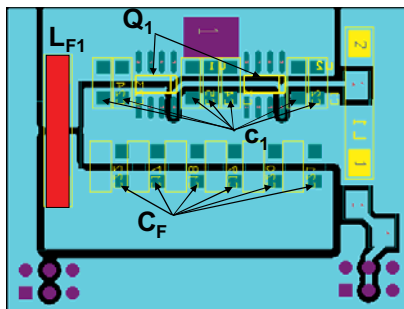


Figure 4. Other experimented layout showing one filter inductance located at the edge of the PCB (TOP view)

external diameter toroidal core with 1:10 turn ratio) with the secondary winding short circuited around a high bandwidth current probe. In this way, the 60 nH current probe inductance has been reduced by a factor of 100, becoming negligible as

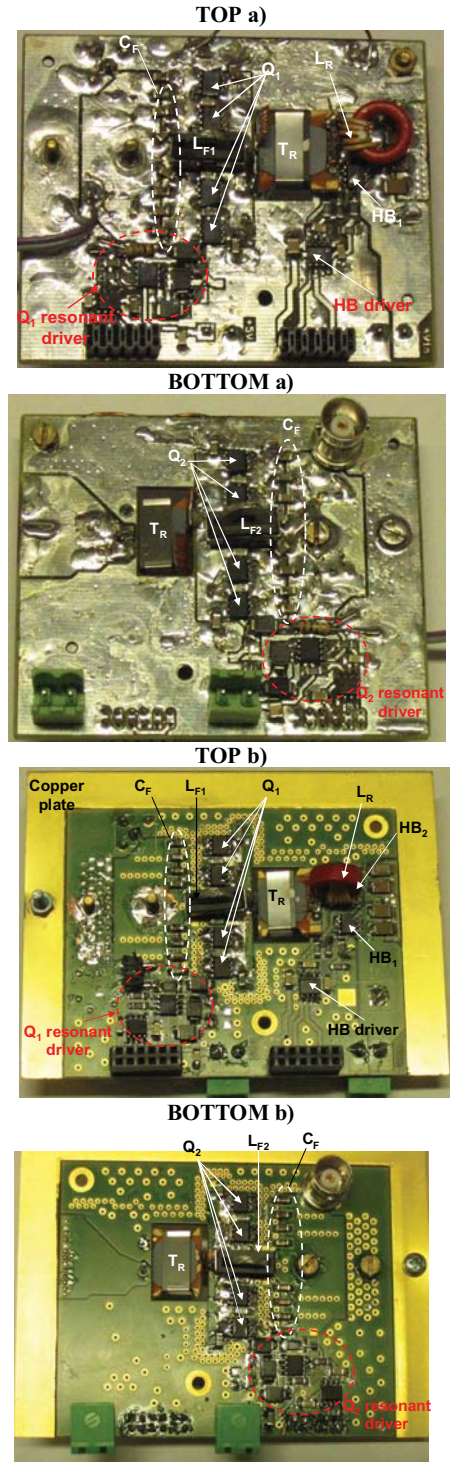


Figure 5. TOP and BOTTOM views of two prototypes: a) assembled two FR4 layers (PCB1); b) PCB with inner baseplate (PCB2)

compared to the resonant inductance L_R . Moreover, only a small loop was needed to accommodate for the current transformer. This procedure assumes that there is no dependence of the losses on the voltage, since all the switches operate with soft commutations. The short circuit at the transformer's primary allowed to estimate the total power dissipated by the resonant inductor L_R and the half bridge switches HB_1 and HB_2 (the individual contribution was then estimated calculating the MOSFET conduction losses from their R_{DS} value @ $t_j = 125^\circ\text{C}$). At the same time, it has been possible to measure the equivalent resonant inductance ($L_R + L_{\text{trace_primary}} = 285\text{ nH}$) from the knowledge of the input voltage needed to achieve the desired 7 A peak triangular resonant current. The short circuit at the transformer's secondary allowed to estimate the power dissipated by the transformer as well as its leakage inductance ($L_{\text{leak}} = 61\text{ nH}$). The short circuit created at the secondary side by substituting the SR MOSFETs with copper strips allowed to estimate the losses caused by the transformer secondary current loop (0.27 W) as well as its parasitic inductance (42 nH). Lastly, the short circuit created at the secondary side by driving the SR MOSFETs with a constant V_{GS} voltage, allowed to calculate their associated losses. As we can see, the overall resonant inductance was roughly 390 nH with the overall parasitic inductance weighting for almost 26% of the total value.

The results of the power loss measurements are summarized in table II in the case of PCB2 with IRF7836 SR MOSFETs: the resonant driver dissipation was simply measured thanks to the use of a separate power supply for them, while the power dissipation of the half-bridge driver was estimated from the MOSFET total gate charge ($Q_g = 28\text{ nC}$ extrapolated for $V_{GS} = 10\text{ V}$, $V_{DS} = 48\text{ V}$ for IRF7855)

TABLE II. DISSIPATED POWER FOR THE MAIN HEATING COMPONENTS ESTIMATED FROM MEASUREMENTS

Component	Ref. name	$I_{\text{out}}=30\text{A}$ Power [W]	$I_{\text{out}}=40\text{A}$ Power [W]	$I_{\text{out}}=50\text{A}$ Power [W]
Primary MOSFET 1	IRF7855	0.32	0.51	0.72
Primary MOSFET 2	IRF7855	0.32	0.51	0.72
Primary driver	LM5101A	1.0	1.0	1.0
Primary inductor	-	0.43	0.68	0.95
Transformer	-	0.9	1.5	2.1
Secondary inductor	-	0.18	0.32	0.5
Secondary traces	-	0.15	0.22	0.27
Secondary MOSFET 1	IRF7836	0.087	0.11	0.21
Secondary MOSFET 2	IRF7836	0.087	0.11	0.21
Secondary MOSFET 3	IRF7836	0.087	0.11	0.21
Secondary MOSFET 4	IRF7836	0.087	0.11	0.21
Secondary driver	IRF7319	1.0	1.0	1.0

and the well known formula:

$$P_{pd} = Q_g V_{GS} f_s$$

The described power loss analysis was not able to find all the contributions (resonant capacitors, output filter inductors and capacitors, output traces, etc.) so that the remaining power loss has been estimated by subtracting the total measured losses (6.4 W) from the total power loss measured at nominal conditions, i.e. with the converter delivering 65 W power at 1.3 V and 50 A (~ 12 W).

The converter efficiency of the power stage only (driver losses not included) measured at different output current values is reported in Fig. 6 for three different prototypes: PCB1 and PCB2 with IRF7836 SR MOSFETs and PCB2 with STS12NH3LL SR MOSFETs. As we can see, with IRF7836 SR MOSFETs the power stage efficiency at nominal power is 86% for PCB1 and 84% for PCB2 showing the influence of the thicker baseplate of PCB2 with associated eddy current losses, while with STS12NH3LL SR MOSFETs (lower total gate charge but higher $R_{DS(on)}$) the efficiency is close to 81% (in this case it was not possible to reach the nominal output current due to control saturation).

By including the driver losses, the overall efficiency drops of 3 points. It is important to mention that the efficiency measured at different times showed a uncertainty of $\pm 1\%$.

V. THERMAL SIMULATIONS

5.1 Single device model

The first step in the thermal modeling was to build-up a thermal finite element model (FEM) of the single SMD chip (see Fig. 7). We took, as a reference structure, that of bondless SO-8 STS12NH3LL power MOSFETs used as synchronous rectifiers, whose data were almost totally known either from literature or SEM (Scanning Electron Microscopy) inspection. Such a model was implemented using a commercial software tool (COMSOL

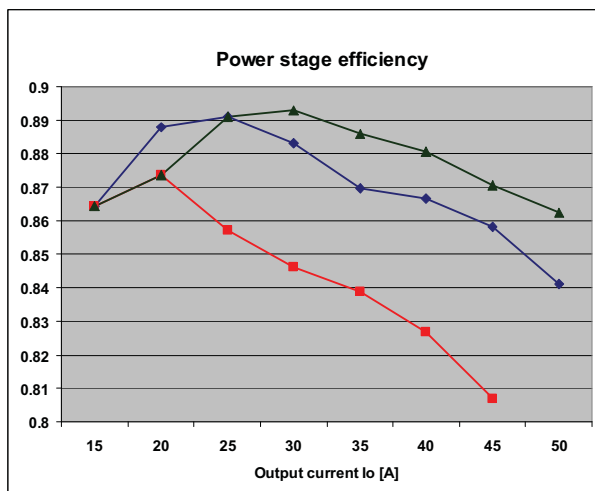


Figure 6. Comparison of the converter efficiency for three different prototypes: PCB1 (upper trace) and PCB2 (middle trace) with IRF7836 SR MOSFETs and PCB2 with STS12NH3LL SR MOSFETs (lower trace)

Multiphysics™), able to carry out multi-physics 3D simulations. The heat transfer module has been used, which includes Fourier conduction and convection equations [3].

As can be seen from Fig. 7, drain and source contacts are directly connected to the leads, by means of metal flanges and only the gate contact is wire bonded. The 3D structure of the packaged chip features elements with very different shapes (in particular, internal connections were done by thin metal layers), which required different meshing techniques for proper FEM treatment.

In this model the unknown parameters were the thermal resistance of the interface between the silicon die and the aluminum flanges (which is the sum of the thermal resistance of the solder layer plus the two Si-solder and solder-Al thermal contact resistances), the thermal conductivity of the package plastic lid, and the thermal convection coefficient. We estimate the values of these parameters by fitting experimental thermal data obtained from a suitable testing board, following the procedure explained in [4], until we obtained a worst-case difference of 10% between simulated and measured temperature variations on the test board.

5.2 Converter Thermal Model

The main scope of the model was to establish the maximum temperatures reached in the various board's layers and interfaces in thermal steady state, then the silicon die was treated as a uniform power source. Moreover, again following the procedure described in [4], from the accurate (and very complex, from the computational point of view) model of the chip, we built-up a simplified model, consisting in an homogeneous parallelepiped with the same external surfaces of the real package, without leads, with the power generated by an inner volume, properly placed inside the package, in order to obtain the same temperature distribution as calculated by the accurate model (see Fig. 8).

The other main heating components on the board were the MOSFETs at the primary section, the two MOSFET's

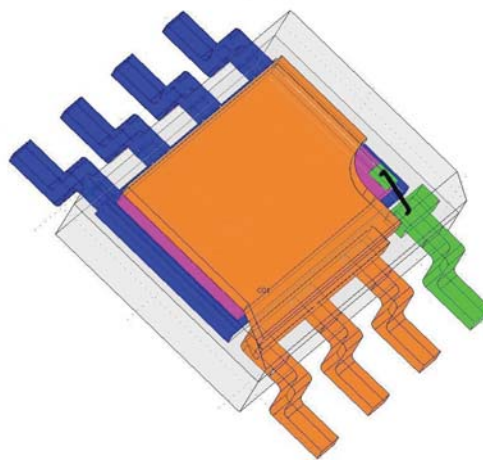


Figure 7. 3D FEM model of a the STS12NH3LL power MOSFET: drain and source metallization are directly connected to the leads, without wire bonding

drivers, the HF transformer, the three inductors and the filter capacitors. For SO-8 MOSFET and driver chips we used the same structure as well as the STS12NH3LL, with different thermally resistive layer between the inner volume where the heat is generated and the board, to account for different junction to ambient thermal resistance reported in the datasheets.

The inductors were designed with simplified structures (cores with same geometrical dimensions of the real ones, but simplified winds). The transformer geometry was simplified as the SO-8 packages with three layers on each side of the PCB in place of the core and a trench in the PCB around the core. The capacitors were modeled as simple ceramic parallelepipeds with same geometrical dimensions of the real ones.

The secondary section of the circuit was replicated on the two sides of the board.

Heat transfers by conduction through the mounted packages to the board were modeled according to:

$$\nabla \cdot (-k \nabla T) = Q$$

where Q is the heat generated per volume unit and k is the thermal conductivity. Q was considered negligible in the circuit board, except that in the interconnection lines of the secondary section. The inductors were modeled to generate heat mostly in the copper winds. In previous simulations of 3D FEM electro-thermal models of inductors operating with AC currents at 1.8 MHz, we observed that a little amount (5-10 %) of the total heat is produced by eddy currents in the core. Then, we considered a similar power dissipation in the inductors in the steady state simulations of the converters.

The thermal conductivities of the components were chosen to be similar to:

- IC epoxy resin (1.2 W/(m·K)), for the top layer of the chips;
- Al-Si (160 W/(m·K)), for the inner layer of the chips;
- FR4 (0.3 W/(m·K)), for the PCB1 board;
- Epoxy resin (0.5 W/(m·K)), for dielectric layers of the PCB2 board;
- Copper (400 W/(m·K)), for the ground plane (baseplate in the PCB2 board) and interconnection lines;

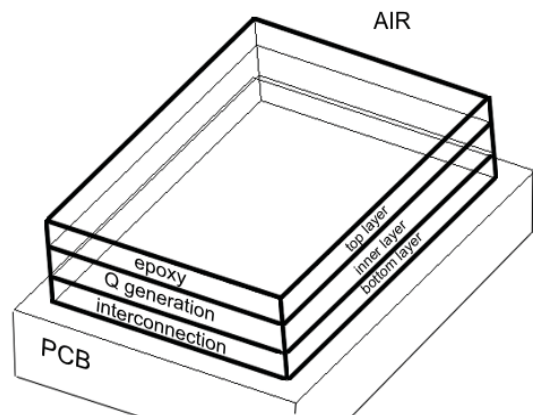


Figure 8. MOSFET simplified 3D model

- Copper, for the wound inductors;
- Ferrite (1 W/(m·K)), for magnetic cores;
- Ceramic (25 W/(m·K)), for capacitors.

The thermal conductivities of the chips bottom layers were chosen as fitting parameters to match the thermal resistances between junctions and ambient of each chip.

During thermal measurements, the board was clamped with a metal bench vise. The vise acted like heat sink with fixed temperature, then we set the temperature on the two edge in contact with the vise.

Heat dissipates from all air-exposed surfaces through natural air convection, which was modeled using a heat transfer coefficient, h :

$$q = h(T_{inf} - T)$$

where q is heat flux through the surface, T_{inf} is the external temperature and T is the point temperature on the surface. Fig. 9 illustrates the imposed boundary conditions.

To reduce the computational complexity, the thin conducting layers of the interconnection lines were modeled using a 2D shell approximation, according to:

$$\nabla \cdot (-d_s k \nabla_s T) = 0$$

where d_s is the layer's thickness (35 μm in our case), and ∇_s represents the nabla operator projected onto the direction of the plane. The model uses a general heat transfer application mode of Comsol Multiphysics to describe the 3D heat transfer as well as the 2D shell heat transfer in stationary state.

In order to consider Joule effect heat generation at 2D modeled interconnection layers, it is possible to set an heat flux at the boundaries representing these layers. We did this for secondary interconnection lines, although the electric measurements showed a little amount of power losses, if compared with the ones of other components.

We built-up two models, corresponding to the two versions of the converter, i.e. PCB1 and PCB2 previously described, with IRF7836 SR MOSFETs. As an example, Fig. 10 shows the simulated thermal distribution obtained on the upper side of the two models by imposing the same dissipated power for the components, as reported in table II, which were estimated

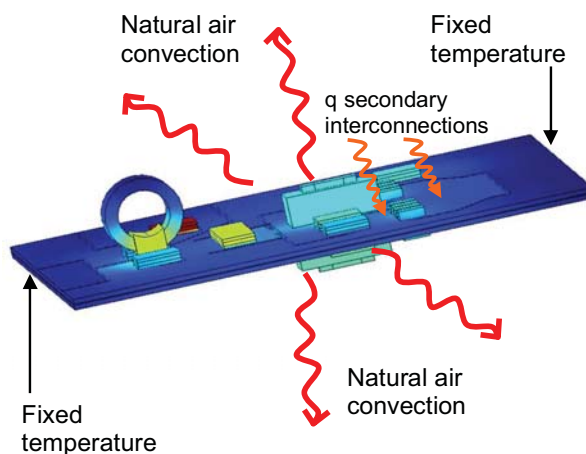


Figure 9. Thermal boundary conditions of the converter 3D FEM model

by the electrical measurements described in section IV.

The simulations were done first determining the fitting parameters for the PCB1 solution at $I_{out} = 50$ A. All other simulations were done using the same parameters.

The solution with integrated baseplate (PCB2) showed better behavior either in term of thermal uniformity and maximum temperatures.

VI. THERMAL MEASUREMENTS

A comparison between the two technological solutions of the converter was carried out from the thermal point of view, biasing them at different output current levels (30, 40 and 50 A) and detecting the thermal image of the board surfaces, by means of a Flir A20 infrared thermocamera.

A preliminary series of thermal measurements was carried out by means of k-thermocouples placed on the top of the heating components, to adjust in the thermocamera software the value of the emissivity of the various surfaces (the effect of the thermocouple itself was also estimated). The ambient temperature was 26 °C, input and output voltage were fixed at 48 V and 1.3 V, respectively.

Fig. 11 shows, as an example, the thermal map of the up-side of the converter measured with the IR camera for the two solutions (top: PCB1; down: PCB2) with 50 A of load current. Similar results were obtained for the downward surfaces.

It should be pointed out that the surface temperature is correctly represented by the color scale in the IR map only at

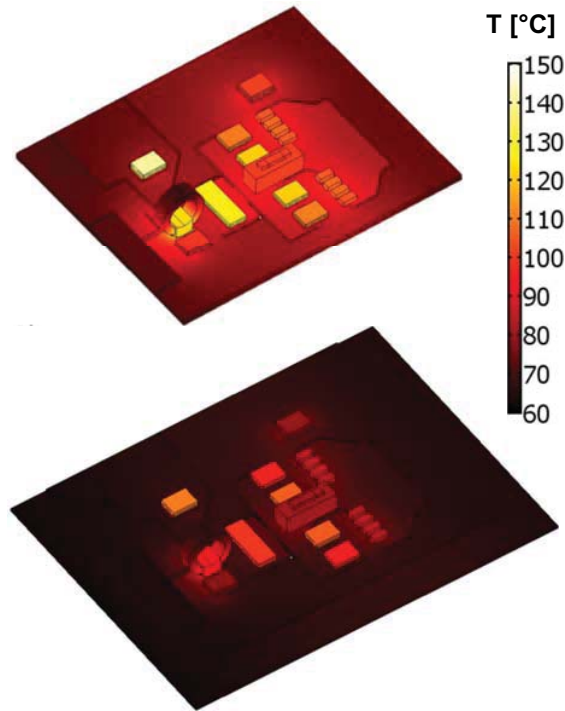


Fig. 10. Boundary thermal map of the up-side of the converter operating with 50 A load current (top: PCB1 solution; bottom: PCB2 solution)

the reference points, were a calibration of the emissivity was performed. This clearly appears, for instance, in the empty areas, which seem colder in the PCB1 than in PCB2, because the metallized surface (visible in Fig. 5a) is not passivated and has a very low emissivity.

Table III reports the measured and simulated temperatures at different points of the upper surface of the two boards for three different levels of load current (30, 40, and 50 A).

The measurement results confirm the better thermal behavior of the solution with integrated baseplate (PCB2) forecasted by FEM simulations: better thermal distribution over the board, a lower peak temperature of active and passive components and a lower mean temperature on the board.

The match between measured and simulated data is quite good: because some unknown parameters in the FEM thermal model were adjusted to fit the measured temperatures in the FR4 board at 50 A load current, the agreement for PCB1 is better than for PCB2. Nevertheless the differences in temperature increase over the ambient temperature are, in any

TABLE III. TEMPERATURES MEASURED (SIMULATED) AT THE SURFACE OF THE HEATING COMPONENTS IN THE TWO BOARDS AT DIFFERENT CURRENT LEVELS.

Component (test point)	T [°C] (PCB1)			T [°C] (PCB2)		
	I_{out} 30A	I_{out} 40A	I_{out} 50A	I_{out} 30A	I_{out} 40A	I_{out} 50A
Primary MOSFET 1	74 (72)	81 (80)	96 (102)	51 (54)	57 (60)	70 (75)
Primary MOSFET 2	75 (73)	82 (82)	96 (100)	51 (54)	57 (60)	70 (77)
Primary driver	123 (124)	129 (129)	143 (143)	97 (95)	102 (99)	114 (118)
Primary inductor wound	83 (82)	98 (98)	123 (122)	67 (62)	79 (73)	106 (94)
Primary inductor core	54 (53)	59 (60)	68 (69)	46 (47)	52 (55)	68 (67)
Transformer	82 (79)	96 (98)	121 (126)	68 (63)	81 (77)	108 (100)
Secondary inductor	73 (69)	84 (85)	104 (101)	63 (56)	74 (66)	96 (81)
Secondary MOSFET 1	72 (70)	85 (81)	107 (110)	59 (61)	70 (68)	93 (97)
Secondary MOSFET 2	76 (75)	90 (88)	116 (121)	64 (65)	77 (73)	103 (106)
Secondary MOSFET 3	78 (75)	93 (88)	118 (121)	64 (66)	77 (74)	102 (105)
Sec. MOSFET 4	75 (71)	88 (82)	110 (111)	60 (62)	70 (69)	91 (96)
Sec. driver	80 (79)	86 (86)	99 (102)	64 (63)	71 (67)	84 (80)
Board primary region	59 (58)	62 (62)	71 (73)	46 (48)	51 (50)	62 (64)
Board secondary region	59 (60)	67 (70)	83 (86)	48 (49)	54 (54)	68 (67)
Corner of the board	53 (53)	59 (59)	71 (74)	46 (47)	51 (51)	64 (64)

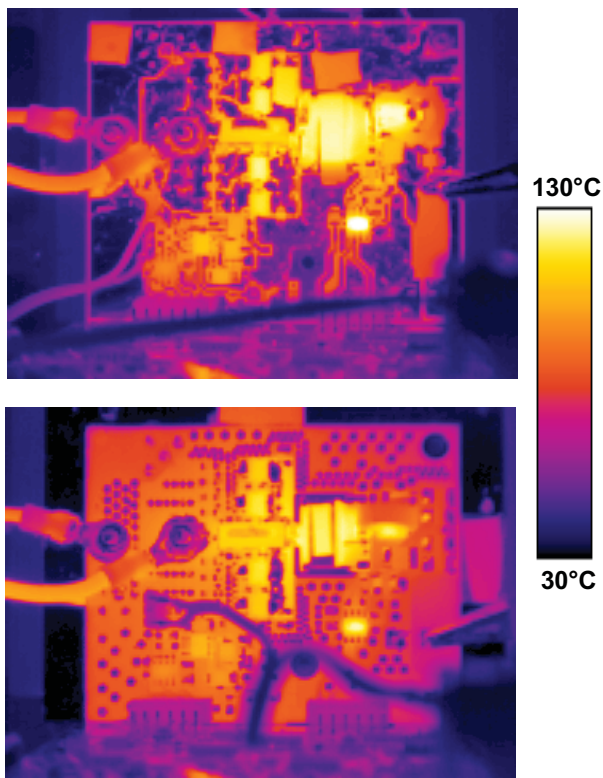


Figure 11. Thermal map of the up-side of the converter measured with the IR camera for the two solutions (top: PCB1; bottom: PCB2) with 50 A load current.

case, lower than 10% on the whole board, except for some points of magnetic components, probably due to the approximated models adopted for these elements.

This results confirm the validity of our simulation approach for thermal analysis and design of new power converter layouts and demonstrated the suitability of the final solution for the considered 1.8 MHz VRM.

The version of PCB2 mounting STS12NH3LL SR MOSFETs was also thermally characterized: we found a temperature distribution similar to that of the version with IRF7836, but about 15 °C higher (in the case of 50 A load current) in the SR MOSFET area. This higher heating was likely due to the lower efficiency, caused by the higher R_{DSon} of these MOSFETs.

CONCLUSIONS

In this paper, practical issues regarding the physical realization of a 1.8 MHz VRM described in [1] have been discussed in detail. The objective was to gain control on the layout-dependent parasitic components as well as to efficiently manage the dissipated power. In order to forecast the critical component temperature a FEM model of the whole converter has been developed. The complete model was based on a detailed thermal model of the single chips, which was validated by a comparison with measured temperatures on an *ad-hoc* designed and fabricated test board. The converter model was then simplified to meet a reasonable computational dimension.

Thermal measurements, by infrared thermocamera, allowed us to adjust some unknown model parameters, so that a mismatch within 10% in temperature variation between simulations and measurements was reached in the whole converter. The thermal model was built for the two PCBs with different technology. Thermal measurements were performed at different load current levels for both the PCBs and, in the case of PCB2 (the one with integrated copper baseplate), with different SR MOSFETs. The comparison shows that the PCB with integrated baseplate has a better thermal distribution over the board, a lower peak temperature of the active and passive components and a lower mean temperature on the board, confirming the results of FEM simulations.

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