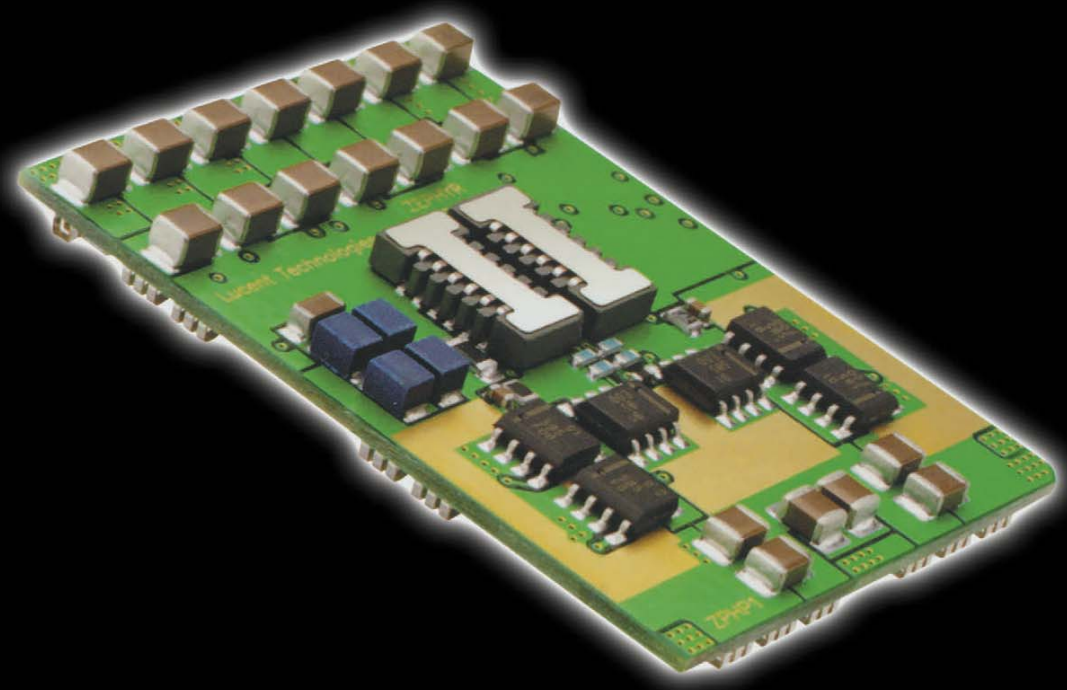
Robert W. Erickson
Dragan Maksimović

Fundamentals of Power Electronics

Second Edition



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Fundamentals of Power Electronics

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Fundamentals of Power Electronics

SECOND EDITION

Robert W. Erickson
Dragan Maksimović
University of Colorado
Boulder, Colorado

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Printed on acid-free paper.

Dedicated to
Linda, William, and Richard
Lidija, Filip, Nikola, and Stevan

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Preface

The objective of the First Edition was to serve as a textbook for introductory power electronics courses where the fundamentals of power electronics are defined, rigorously presented, and treated in sufficient depth so that students acquire the knowledge and skills needed to design practical power electronic systems. The First Edition has indeed been adopted for use in power electronics courses at a number of schools. An additional goal was to contribute as a reference book for engineers who practice power electronics design, and for students who want to develop their knowledge of the area beyond the level of introductory courses. In the Second Edition, the basic objectives and philosophy of the First Edition have not been changed. The modifications include addition of a number of new topics aimed at better serving the expanded audience that includes students of introductory and more advanced courses, as well as practicing engineers looking for a reference book and a source for further professional development. Most of the chapters have been significantly revised and updated. Major additions include a new Chapter 10 on input filter design, a new Appendix B covering simulation of converters, and a new Appendix C on Middlebrook's Extra Element Theorem. In addition to the introduction of new topics, we have made major revisions of the material to improve the flow and clarity of explanations and to provide additional specific results, in chapters covering averaged switch modeling, dynamics of converters operating in discontinuous conduction mode, current mode control, magnetics design, pulse-width modulated rectifiers, and resonant and soft-switching converters.

A completely new Chapter 10 covering input filter design has been added to the second addition. The problem of how the input filter affects the dynamics of the converter, often in a manner that degrades stability and performance of the converter system, is explained using Middlebrook's Extra Element Theorem. This design-oriented approach is explained in detail in the new Appendix C. Simple conditions are derived to allow filter damping so that converter transfer functions are not changed. Complete results for optimum filter damping are presented. The chapter concludes with a discussion about the design of multiple-section filters, illustrated by a design example.

Computer simulation based on the averaged switch modeling approach is presented in Appendix B, including PSpice models for continuous and discontinuous conduction mode, and current-mode control. Extensive simulation examples include: finding the dc conversion ratio and efficiency of a SEPIC, plotting the transient response of a buck-boost converter, comparing the control-to-output transfer functions of a SEPIC operating in CCM and DCM, determining the loop gain, line-to-output transfer function, and load transient response of a closed-loop buck voltage regulator, finding the input current

waveform and THD of a DCM boost rectifier, and comparing the transfer functions and output impedances of buck converters operating with current programmed control and with duty cycle control. The major purpose of Appendix B is to supplement the text discussions, and to enable the reader to effectively use averaged models and simulation tools in the design process. The role of simulation as a design verification tool is emphasized. In our experience of teaching introductory and more advanced power electronics courses, we have found that the use of simulation tools works best with students who have mastered basic concepts and design-oriented analytical techniques, so that they are able to make correct interpretations of simulation results and model limitations. This is why we do not emphasize simulation in introductory chapters. Nevertheless, Appendix B is organized so that simulation examples can be introduced together with coverage of the theoretical concepts of Chapters 3, 7, 9, 10, 11, 12, and 18.

Middlebrook's Extra Element Theorem is presented in Appendix C, together with four tutorial examples. This valuable design-oriented analytical tool allows one to examine effects of adding an extra element to a linear system, without solving the modified system all over again. The theorem has many practical applications in the design of electronic circuits, from solving circuits by inspection, to quickly finding effects of unmodeled parasitic elements. In particular, in the Second Edition, Middlebrook's Extra Element Theorem is applied to the input filter design of Chapter 10, and to resonant inverter design in Chapter 19.

In Chapter 7, we have revised the section on circuit averaging and averaged switch modeling. The process of circuit averaging and deriving averaged switch models has been explained to allow readers not only to use the basic models, but also to construct averaged models for other applications of interest. Examples of extensions of the averaged switch modeling approach include modeling of switch conduction and switching losses. Related to the revision of Chapter 7, in Appendix B we have included new material on simulation of converters based on the averaged switch modeling approach.

Chapter 8 contains a new substantial introduction that explains the engineering design process and the need for design-oriented analysis. The discussions of design-oriented methods for construction of frequency response have been revised and expanded. A new example has been added, involving approximate analysis of a damped input filter.

Chapter 11 on dynamics of DCM (discontinuous conduction mode) converters, and Chapter 12 on current-mode control, have been thoroughly revised and updated. Chapter 11 includes a simplified derivation of DCM averaged switch models, as well as an updated discussion of high-frequency DCM dynamics. Chapter 12 includes a new, more straightforward explanation and discussion of current-mode dynamics, as well as new complete results for transfer functions and model parameters of all basic converters.

The chapters on magnetics design have been significantly revised and reorganized. Basic magnetics theory necessary for informed design of magnetic components in switching power converters is presented in Chapter 13. The description of the proximity effect has been completely revised, to explain this important but complex subject in a more intuitive manner. The design of magnetic components based on the copper loss constraint is described in Chapter 14. A new step-by-step design procedure is given for multiple-winding inductors, and practical design examples are included for the design of filter inductors, coupled inductors and flyback transformers. The design of magnetic components (transformers and ac inductors) based on copper and core loss considerations is described in Chapter 15.

To improve their logical flow, the chapters covering pulse-width modulated rectifiers have been combined into a single Chapter 18, and have been completely reorganized. New sections on current control based on the critical conduction mode, as well as on operation of the CCM boost and DCM flyback as PWM rectifiers, have been added.

Part V consists of Chapter 19 on resonant converters and Chapter 20 on soft-switching converters. The discussion of resonant inverter design, a topic of importance in the field of high-frequency electronic ballasts, has been expanded and explained in a more intuitive manner. A new resonant inverter

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design example has also been added to Chapter 19. Chapter 20 contains an expanded tutorial explanation of switching loss mechanisms, new charts illustrating the characteristics of quasi-square-wave and multiresonant converters, and new up-to-date sections about soft-switching converters, including the zero-voltage transition full-bridge converter, the auxiliary switch approach, and the auxiliary resonant commutated pole approach for dc–dc converters and dc–ac inverters.

The material of the Second Edition is organized so that chapters or sections of the book can be selected to offer an introductory one-semester course, but yet enough material is provided for a sequence of more advanced courses, or for individual professional development. At the University of Colorado, we cover the material from the Second Edition in a sequence of three semester-long power electronics courses. The first course, intended for seniors and first-year graduate students, covers Chapters 1 to 6, Sections 7.1, 7.2, 7.5, and 7.6 from Chapter 7, Chapters 8 and 9, and Chapters 13 to 15. A project-oriented power electronics design laboratory is offered in parallel with this course. This course serves as a prerequisite for two follow-up courses. The second course starts with Section 7.4, proceeds to Appendices B and C, Chapters 10, 11 and 12, and concludes with the material of Chapters 16 to 18. In the third course we cover resonant and soft-switching techniques of Chapters 19 and 20.

The website for the Second Edition contains comprehensive supporting materials for the text, including solved problems and slides for instructors. Computer simulation files can be downloaded from this site, including a PSpice library of averaged switch models, and simulation examples.

This text has evolved from courses developed over seventeen years of teaching power electronics at the University of Colorado. These courses, in turn, were heavily influenced by our previous experiences as graduate students at the California Institute of Technology, under the direction of Profs. Slobodan Ćuk and R. D. Middlebrook, to whom we are grateful. We appreciate the helpful suggestions of Prof. Arthur Witulski of the University of Arizona. We would also like to thank the many readers of the First Edition, students, and instructors who offered their comments and suggestions, or who pointed out errata. We have attempted to incorporate these suggestions wherever possible.

Robert W. Erickson
Dragan Maksimović
Boulder, Colorado

1

Introduction

1.1 INTRODUCTION TO POWER PROCESSING

The field of power electronics is concerned with the processing of electrical power using electronic devices [1–7]. The key element is the *switching converter*, illustrated in Fig. 1.1. In general, a switching converter contains power input and control input ports, and a power output port. The raw input power is processed as specified by the control input, yielding the conditioned output power. One of several basic functions can be performed [2]. In a *dc–dc converter*, the dc input voltage is converted to a dc output voltage having a larger or smaller magnitude, possibly with opposite polarity or with isolation of the input and output ground references. In an ac–dc *rectifier*, an ac input voltage is rectified, producing a dc output voltage. The dc output voltage and/or ac input current waveform may be controlled. The inverse process, dc–ac *inversion*, involves transforming a dc input voltage into an ac output voltage of controllable magnitude and frequency. Ac–ac *cycloconversion* involves converting an ac input voltage to a given ac output voltage of controllable magnitude and frequency.

Control is invariably required. It is nearly always desired to produce a well-regulated output

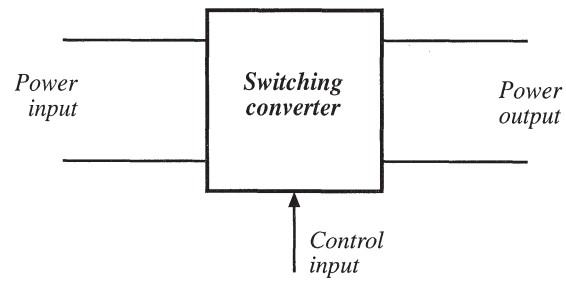


Fig. 1.1 The switching converter, a basic power processing block.

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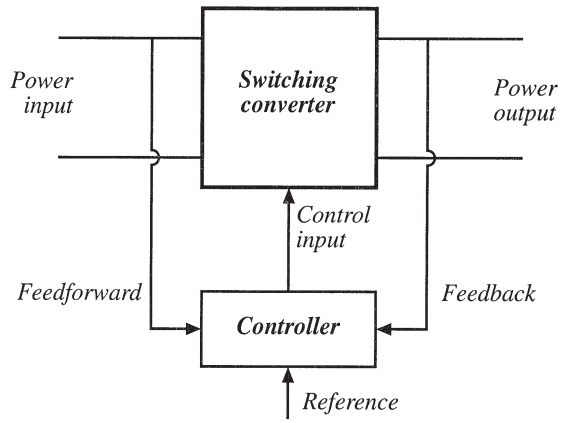


Fig. 1.2 A controller is generally required.

voltage, in the presence of variations in the input voltage and load current. As illustrated in Fig. 1.2, a controller block is an integral part of any power processing system.

High efficiency is essential in any power processing application. The primary reason for this is usually not the desire to save money on one's electric bills, nor to conserve energy, in spite of the nobility of such pursuits. Rather, high efficiency converters are necessary because construction of low-efficiency converters, producing substantial output power, is impractical. The efficiency of a converter having output power P_{out} and input power P_{in} is

$$\eta = \frac{P_{out}}{P_{in}} \tag{1.1}$$

The power lost in the converter is

$$P_{loss} = P_{in} - P_{out} = P_{out}\left(\frac{1}{\eta} - 1\right) \tag{1.2}$$

Equation (1.2) is plotted in Fig. 1.3. In a converter that has an efficiency of 50%, power P_{loss} is dissipated by the converter elements and this is equal to the output power, P_{out}. This power is converted into heat, which must be removed from the converter. If the output power is substantial, then so is the loss power. This leads to a large and expensive cooling system, it causes the electronic elements within the converter to operate at high temperature, and it reduces the system reliability. Indeed, at high output powers, it may be impossible to adequately cool the converter elements using current technology.

Increasing the efficiency is the key to obtaining higher output powers. For example, if the converter efficiency is 90%, then the converter loss power is equal to only 11%

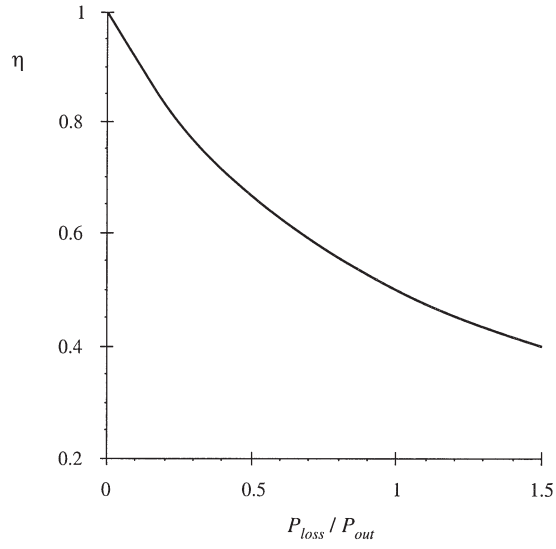


Fig. 1.3 Converter power loss vs. efficiency.

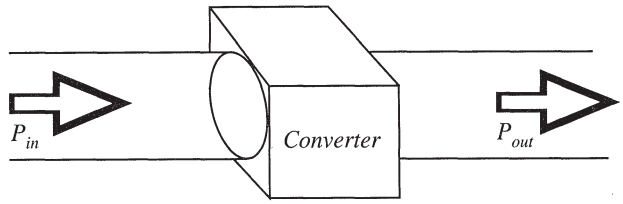


Fig. 1.4 A goal of current converter technology is to construct converters of small size and weight, which process substantial power at high efficiency.

of the output power. Efficiency is a good measure of the success of a given converter technology. Figure 1.4 illustrates a converter that processes a large amount of power, with very high efficiency. Since very little power is lost, the converter elements can be packaged with high density, leading to a converter of small size and weight, and of low temperature rise.

How can we build a circuit that changes the voltage, yet dissipates negligible power? The various conventional circuit elements are illustrated in Fig. 1.5. The available circuit elements fall broadly into the classes of resistive elements, capacitive elements, magnetic devices including inductors and transformers, semiconductor devices operated in the linear mode (for example, as class *A* or class *B* amplifiers), and semiconductor devices operated in the switched mode (such as in logic devices where transistors operate in either saturation or cutoff). In conventional signal processing applications, where efficiency is not the primary concern, magnetic devices are usually avoided wherever possible, because of their large size and the difficulty of incorporating them into integrated circuits. In contrast, capacitors and magnetic devices are important elements of switching converters, because ideally they do not consume power. It is the resistive element, as well as the linear-mode semiconductor device, that is avoided [2]. Switched-mode semiconductor devices are also employed. When a semiconductor device operates in the off state, its current is zero and hence its power dissipation is zero. When the semiconductor device operates in the on (saturated) state, its voltage drop is small and hence its power dissipation is also small. In either event, the power dissipated by the semiconductor device is low. So capacitive and inductive elements, as well as switched-mode semiconductor devices, are available for synthesis of high-efficiency converters.

Let us now consider how to construct the simple dc-dc converter example illustrated in Fig. 1.6. The input voltage V_g is 100 V. It is desired to supply 50 V to an effective 5 Ω load, such that the dc load current is 10 A.

Introductory circuits textbooks describe a low-efficiency method to perform the required function: the voltage divider circuit illustrated in Fig. 1.7(a). The dc–dc converter then consists simply of a

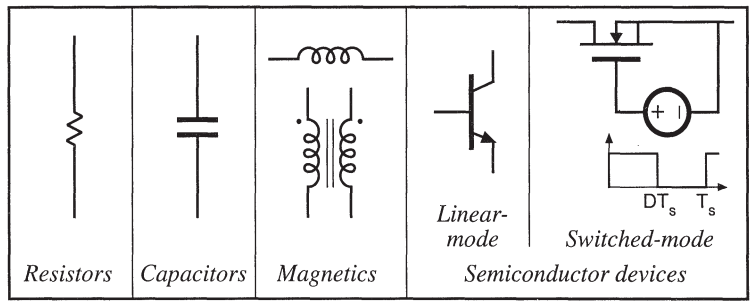


Fig. 1.5 Devices available to the circuit designer [2].

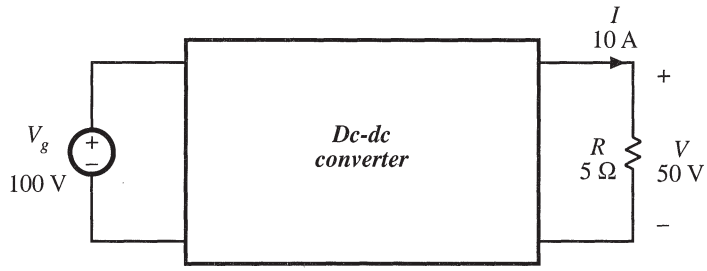


Fig. 1.6 A simple power processing example: construction of a 500 W dc–dc converter.

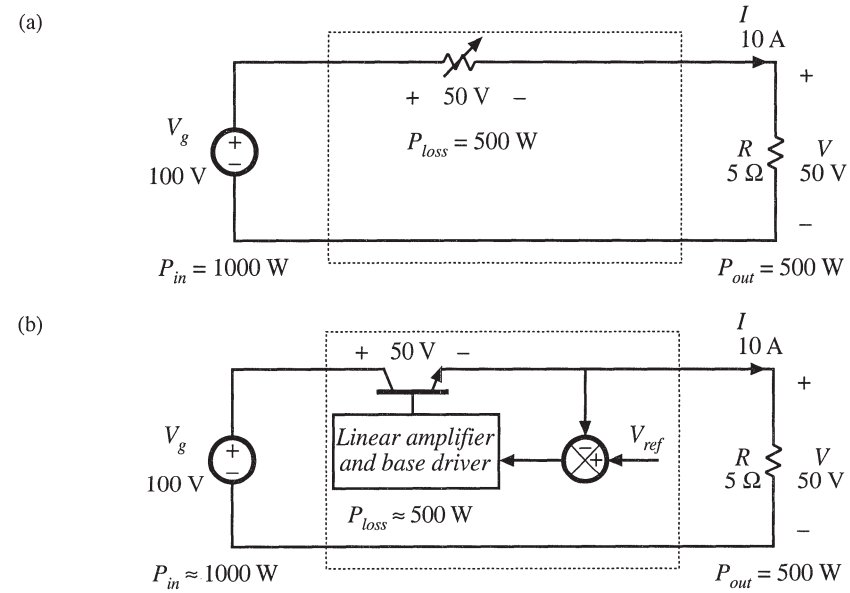


Fig. 1.7 Changing the dc voltage via dissipative means: (a) voltage divider, (b) series pass regulator.

variable resistor, whose value is adjusted such that the required output voltage is obtained. The load current flows through the variable resistor. For the specified voltage and current levels, the power P_{loss} dissipated in the variable resistor equals the load power P_{out} = 500 W. The source V_g supplies power P_{in} = 1000 W. Figure 1.7(b) illustrates a more practical implementation known as the linear series-pass regulator. The variable resistor of Fig. 1.7(a) is replaced by a linear-mode power transistor, whose base current is controlled by a feedback system such that the desired output voltage is obtained. The power dissipated by the linear-mode transistor of Fig. 1.7(b) is approximately the same as the 500 W lost by the variable resistor in Fig. 1.7(a). Series-pass linear regulators generally find modern application only at low power levels of a few watts.

Figure 1.8 illustrates another approach. A single-pole double-throw (SPDT) switch is connected as shown. The switch output voltage $v_s(t)$ is equal to the converter input voltage V_g when the switch is in position 1, and is equal to zero when the switch is in position 2. The switch position is varied periodically, as illustrated in Fig. 1.9, such that $v_s(t)$ is a rectangular waveform having frequency f_s and period $T_s = 1/f_s$. The duty cycle D is defined as the fraction of time in which the switch occupies position 1. Hence, $0 \le D \le 1$. In practice, the SPDT switch is realized using switched-mode semiconductor devices,

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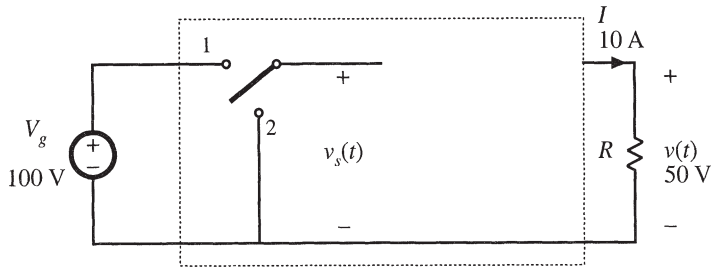


Fig. 1.8 Insertion of SPDT switch which changes the dc component of the voltage.

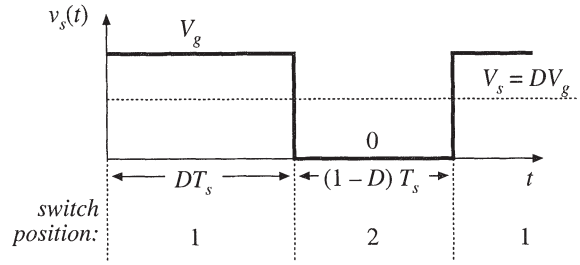


Fig. 1.9 Switch output voltage waveform $v_s(t)$.

which are controlled such that the SPDT switching function is attained.

The switch changes the dc component of the voltage. Recall from Fourier analysis that the dc component of a periodic waveform is equal to its average value. Hence, the dc component of $v_s(t)$ is

$$V_s = \frac{1}{T_s}\int_0^{T_s} v_s(t)dt = DV_g \tag{1.3}$$

Thus, the switch changes the dc voltage, by a factor equal to the duty cycle D. To convert the input voltage $V_g = 100$ V into the desired output voltage of $V = 50$ V, a duty cycle of $D = 0.5$ is required.

Again, the power dissipated by the switch is ideally zero. When the switch contacts are closed, then their voltage is zero and hence the power dissipation is zero. When the switch contacts are open, then the current is zero and again the power dissipation is zero. So we have succeeded in changing the dc voltage component, using a device that is ideally lossless.

In addition to the desired dc component V_s, the switch output voltage waveform $v_s(t)$ also contains undesirable harmonics of the switching frequency. In most applications, these harmonics must be removed, such that the output voltage $v(t)$ is essentially equal to the dc component $V = V_s$. A low-pass filter can be employed for this purpose. Figure 1.10 illustrates the introduction of a single-section L–C low-pass filter. If the filter corner frequency f_0 is sufficiently less than the switching frequency f_s, then the filter essentially passes only the dc component of $v_s(t)$. To the extent that the switch, inductor, and capacitor elements are ideal, the efficiency of this dc–dc converter can approach 100%.

In Fig. 1.11, a control system is introduced for regulation of the output voltage. Since the output voltage is a function of the switch duty cycle, a control system can be constructed that varies the duty cycle to cause the output voltage to follow a given reference. Figure 1.11 also illustrates a typical way in which the SPDT switch is realized using switched-mode semiconductor devices. The converter power stage developed in Figs. 1.8 to 1.11 is called the *buck converter*, because it reduces the dc voltage.

Converters can be constructed that perform other power processing functions. For example, Fig.

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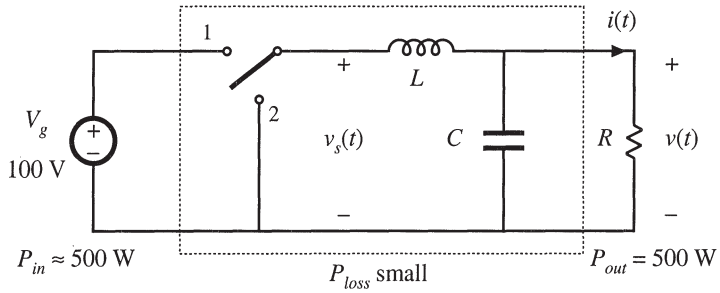


Fig. 1.10 Addition of *L–C* low-pass filter, for removal of switching harmonics.

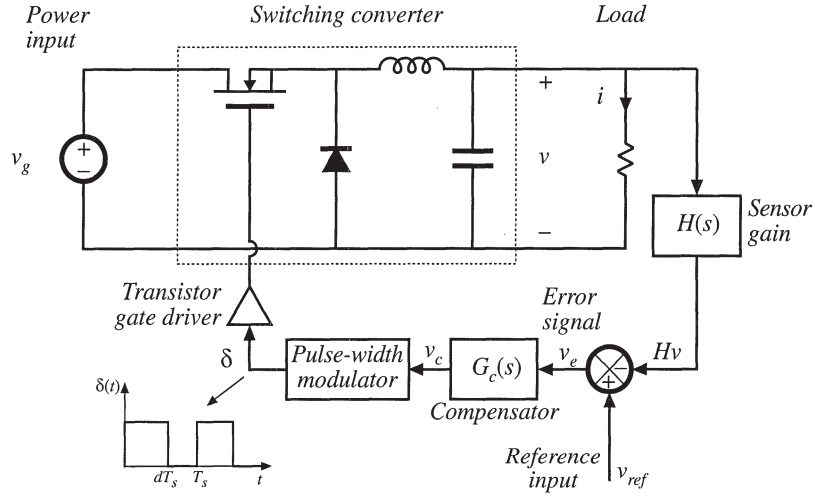


Fig. 1.11 Addition of control system to regulate the output voltage.

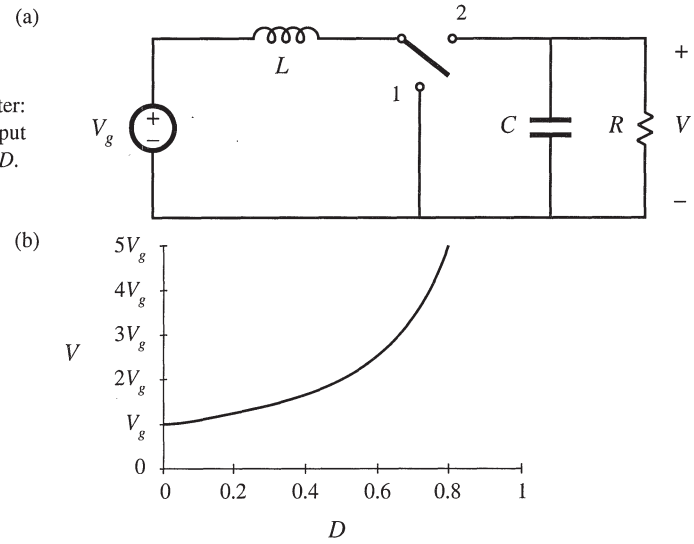


Fig. 1.12 The boost converter: (a) ideal converter circuit, (b) output voltage V vs. transistor duty cycle D.

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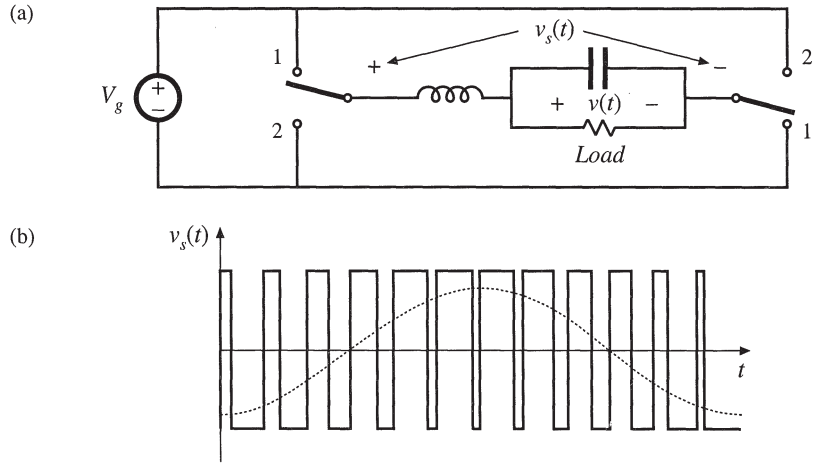


Fig. 1.13 A bridge-type dc-1øac inverter: (a) ideal inverter circuit, (b) typical pulse-width-modulated switch voltage waveform $v_s(t)$, and its low-frequency component.

1.12 illustrates a circuit known as the *boost converter*, in which the positions of the inductor and SPDT switch are interchanged. This converter is capable of producing output voltages that are greater in magnitude than the input voltage. In general, any given input voltage can be converted into any desired output voltage, using a converter containing switching devices embedded within a network of reactive elements.

Figure 1.13(a) illustrates a simple dc–1øac inverter circuit. As illustrated in Fig. 1.13(b), the switch duty cycle is modulated sinusoidally. This causes the switch output voltage $v_s(t)$ to contain a low-frequency sinusoidal component. The *L–C* filter cutoff frequency f_0 is selected to pass the desired low-frequency components of $v_s(t)$, but to attenuate the high-frequency switching harmonics. The controller modulates the duty cycle such that the desired output frequency and voltage magnitude are obtained.

1.2 SEVERAL APPLICATIONS OF POWER ELECTRONICS

The power levels encountered in high-efficiency switching converters range from (1) less than one watt, in dc–dc converters within battery-operated portable equipment, to (2) tens, hundreds, or thousands of watts in power supplies for computers and office equipment, to (3) kilowatts to Megawatts, in variable-speed motor drives, to (4) roughly 1000 Megawatts in the rectifiers and inverters that interface dc transmission lines to the ac utility power system. The converter systems of several applications are illustrated in this section.

A power supply system for a laptop computer is illustrated in Fig. 1.14. A lithium battery powers the system, and several dc–dc converters change the battery voltage into the voltages required by the loads. A buck converter produces the low-voltage dc required by the microprocessor. A boost converter increases the battery voltage to the level needed by the disk drive. An inverter produces high-voltage high-frequency ac to drive lamps that light the display. A charger with transformer isolation converts the ac line voltage into dc to charge the battery. The converter switching frequencies are typically in the vicinity of several hundred kilohertz; this leads to substantial reductions in the size and weight of the reactive elements. *Power management* is used, to control sleep modes in which power consumption is reduced and battery life is extended. In a *distributed power system*, an intermediate dc voltage appears at the computer backplane. Each printed circuit card contains high-density dc–dc converters that produce

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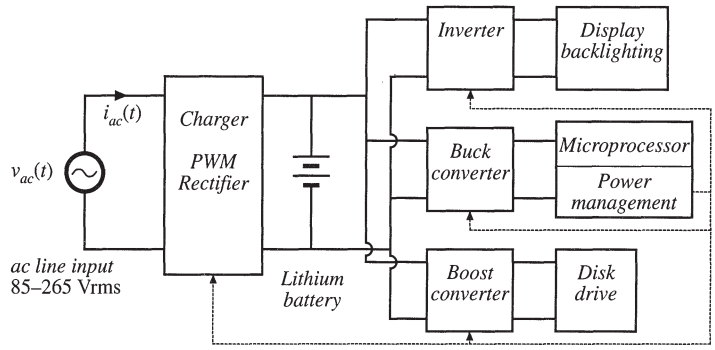


Fig. 1.14 A laptop computer power supply system.

locally-regulated low voltages. Commercial applications of power electronics include off-line power systems for computers, office and laboratory equipment, uninterruptable ac power supplies, and electronic ballasts for gas discharge lighting.

Figure 1.15 illustrates a power system of an earth-orbiting spacecraft. A solar array produces the main power bus voltage V_{bus}. DC–DC converters convert V_{bus} to the regulated voltages required by the spacecraft payloads. Battery charge/discharge controllers interface the main power bus to batteries; these controllers may also contain dc–dc converters. Aerospace applications of power electronics include the power systems of aircraft, spacecraft, and other aerospace vehicles.

Figure 1.16 illustrates an electric vehicle power and drive system. Batteries are charged by a converter that draws high power-factor sinusoidal current from a single-phase or three-phase ac line. The batteries supply power to variable-speed ac motors to propel the vehicle. The speeds of the ac motors are controlled by variation of the electrical input frequency. Inverters produce three-phase ac output voltages of variable frequency and variable magnitude, to control the speed of the ac motors and the vehicle. A dc–dc converter steps down the battery voltage to the lower dc levels required by the electronics of the system. Applications of motor drives include speed control of industrial processes, such as control of compressors, fans, and pumps; transportation applications such as electric vehicles, subways, and locomotives; and motion control applications in areas such as computer peripherals and industrial robots.

Power electronics also finds application in other diverse industries, including dc power supplies,

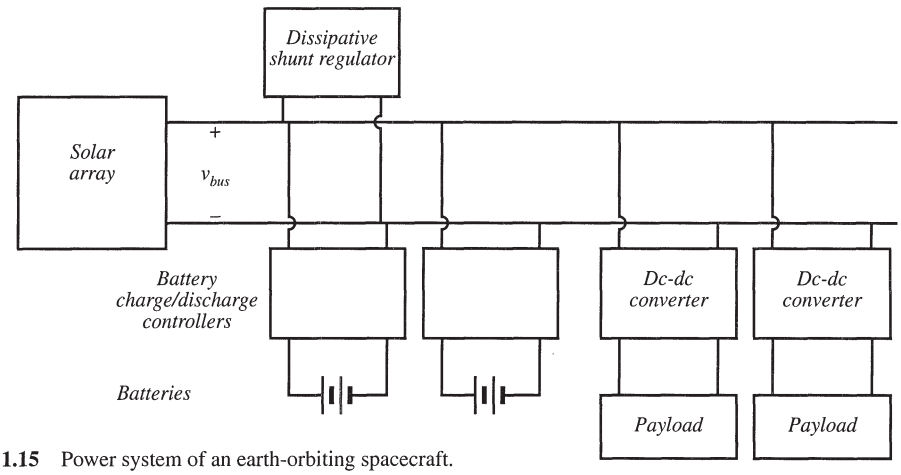


Fig. 1.15 Power system of an earth-orbiting spacecraft.

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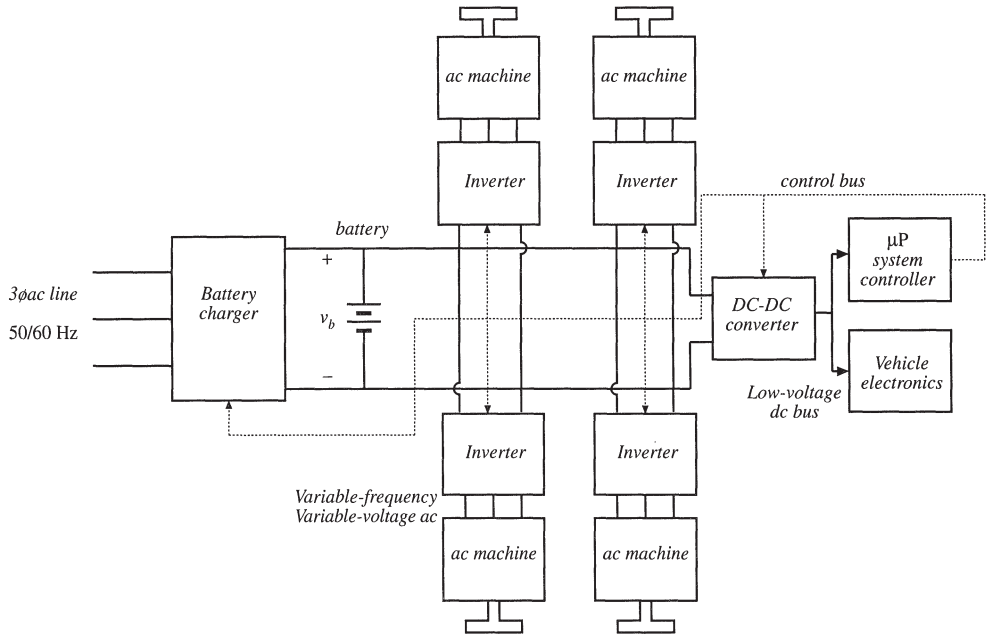


Fig. 1.16 An electric vehicle power and drive system.

uninterruptable power supplies, and battery chargers for the telecommunications industry; inverter systems for renewable energy generation applications such as wind and photovoltaic power; and utility power systems applications including high-voltage dc transmission and static *VAR* (reactive volt-ampere) compensators.

1.3 ELEMENTS OF POWER ELECTRONICS

One of the things that makes the power electronics field interesting is its incorporation of concepts from a diverse set of fields, including:

- analog circuits
- electronic devices
- control systems
- power systems
- magnetics
- electric machines
- numerical simulation

Thus, the practice of power electronics requires a broad electrical engineering background. In addition, there are fundamental concepts that are unique to the power electronics field, and that require specialized study.

The presence of high-frequency switching makes the understanding of switched-mode converters not straightforward. Hence, converter modeling is central to the study of power electronics. As introduced in Eq. (1.3), the dc component of a periodic waveform is equal to its average value. This ideal can

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be generalized, to predict the dc components of all converter waveforms via averaging. In Part I of this book, averaged equivalent circuit models of converters operating in steady state are derived. These models not only predict the basic ideal behavior of switched-mode converters, but also model efficiency and losses. Realization of the switching elements, using power semiconductor devices, is also discussed.

Design of the converter control system requires models of the converter dynamics. In Part II of this book, the averaging technique is extended, to describe low-frequency variations in the converter waveforms. Small-signal equivalent circuit models are developed, which predict the control-to-output and line-to-transfer functions, as well as other ac quantities of interest. These models are then employed to design converter control systems and to lend an understanding of the well-known current-programmed control technique.

The magnetic elements are key components of any switching converter. The design of high-power high-frequency magnetic devices having high efficiency and small size and weight is central to most converter technologies. High-frequency power magnetics design is discussed in Part III.

Pollution of the ac power system by rectifier harmonics is a growing problem. As a result, many converter systems now incorporate low-harmonic rectifiers, which draw sinusoidal currents from the utility system. These modern rectifiers are considerably more sophisticated than the conventional diode bridge: they may contain high-frequency switched-mode converters, with control systems that regulate the ac line current waveform. Modern rectifier technology is treated in Part IV.

Resonant converters employ quasi-sinusoidal waveforms, as opposed to the rectangular waveforms of the buck converter illustrated in Fig. 1.9. These resonant converters find application where high-frequency inverters and converters are needed. Resonant converters are modeled in Part V. Their loss mechanisms, including the processes of zero-voltage switching and zero-current switching, are discussed.

References

[1] W. E. Newell, "Power Electronics—Emerging from Limbo," *IEEE Power Electronics Specialists Conference*, 1973 Record, pp. 6-12.

[2] R. D. Middlebrook, "Power Electronics: An Emerging Discipline," *IEEE International Symposium on Circuits and Systems*, 1981 Proceedings, April 1981.

[3] R. D. Middlebrook, "Power Electronics: Topologies, Modeling, and Measurement," *IEEE International Symposium on Circuits and Systems*, 1981 Proceedings, April 1981.

[4] S. Cuk, "Basics of Switched-Mode Power Conversion: Topologies, Magnetics, and Control," in *Advances in Switched-Mode Power Conversion,* vol. 2, pp. 279--310, Irvine: Teslaco, 1981.

[5] N. Mohan, "Power Electronics Circuits: An Overview," *IEEE IECON*, 1988 Proceedings, pp. 522-527.

[6] B. K. Bose, "Power Electronics—A Technology Review," *Proceedings of the IEEE*, vol. 80, no. 8, August 1992, pp. 1303-1334.

[7] M. Nishihara, "Power Electronics Diversity," *International Power Electronics Conference* (Tokyo), 1990 Proceedings, pp. 21-28.

Part I

Converters in Equilibrium

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2

Principles of Steady-State Converter Analysis

2.1 INTRODUCTION

In the previous chapter, the buck converter was introduced as a means of reducing the dc voltage, using only nondissipative switches, inductors, and capacitors. The switch produces a rectangular waveform $v_s(t)$ as illustrated in Fig. 2.1. The voltage $v_s(t)$ is equal to the dc input voltage V_g when the switch is in position 1, and is equal to zero when the switch is in position 2. In practice, the switch is realized using

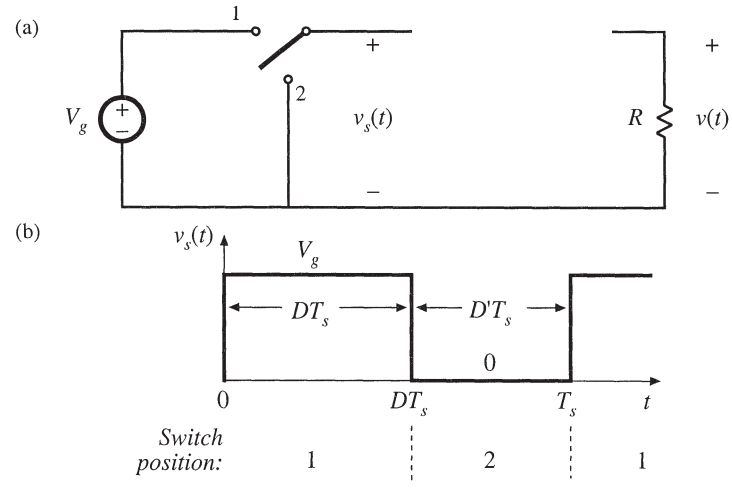


Fig. 2.1 Ideal switch, (a), used to reduce the voltage dc component, and (b) its output voltage waveform $v_s(t)$.

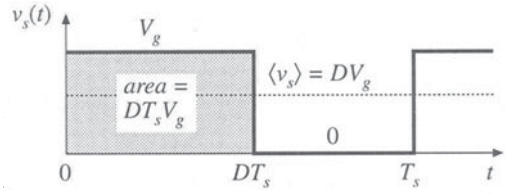


Fig. 2.2 Determination of the switch output voltage dc component, by integrating and dividing by the switching period.

power semiconductor devices, such as transistors and diodes, which are controlled to turn on and off as required to perform the function of the ideal switch. The switching frequency f_s, equal to the inverse of the switching period T_s, generally lies in the range of 1 kHz to 1 MHz, depending on the switching speed of the semiconductor devices. The duty ratio D is the fraction of time that the switch spends in position 1, and is a number between zero and one. The complement of the duty ratio, D', is defined as $(1 - D)$.

The switch reduces the dc component of the voltage: the switch output voltage $v_s(t)$ has a dc component that is less than the converter dc input voltage V_g. From Fourier analysis, we know that the dc component of $v_s(t)$ is given by its average value $\langle v_s \rangle$, or

$$\langle v_s \rangle = \frac{1}{T_s}\int_0^{T_s} v_s(t)\,dt \tag{2.1}$$

As illustrated in Fig. 2.2, the integral is given by the area under the curve, or DT_sV_g. The average value is therefore

$$\langle v_s \rangle = \frac{1}{T_s}\left(DT_sV_g\right) = DV_g \tag{2.2}$$

So the average value, or dc component, of $v_s(t)$ is equal to the duty cycle times the dc input voltage V_g. The switch reduces the dc voltage by a factor of D.

What remains is to insert a low-pass filter as shown in Fig. 2.3. The filter is designed to pass the dc component of $v_s(t)$, but to reject the components of $v_s(t)$ at the switching frequency and its harmonics. The output voltage $v(t)$ is then essentially equal to the dc component of $v_s(t)$:

$$v \approx \langle v_s \rangle = DV_g \tag{2.3}$$

The converter of Fig. 2.3 has been realized using lossless elements. To the extent that they are ideal, the inductor, capacitor, and switch do not dissipate power. For example, when the switch is closed, its voltage drop is zero, and the current is zero when the switch is open. In either case, the power dissipated by the switch is zero. Hence, efficiencies approaching 100% can be obtained. So to the extent that the components are ideal, we can realize our objective of changing dc voltage levels using a lossless network.

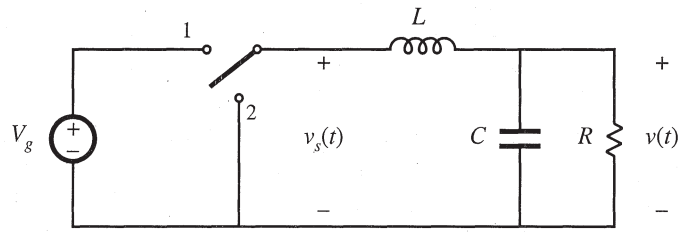


Fig. 2.3 Insertion of low-pass filter, to remove the switching harmonics and pass only the dc component of $v_s(t)$ to the output.

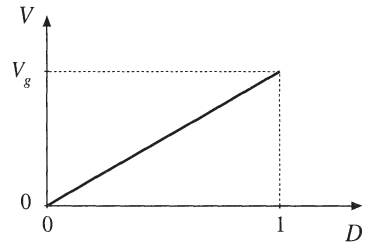


Fig. 2.4 Buck converter dc output voltage V vs. duty cycle D.

The network of Fig. 2.3 also allows control of the output. Figure 2.4 is the control characteristic of the converter. The output voltage, given by Eq. (2.3), is plotted vs. duty cycle. The buck converter has a linear control characteristic. Also, the output voltage is less than or equal to the input voltage, since $0 \leq D \leq 1$. Feedback systems are often constructed that adjust the duty cycle D to regulate the converter output voltage. Inverters or power amplifiers can also be built, in which the duty cycle varies slowly with time and the output voltage follows.

The buck converter is just one of many possible switching converters. Two other commonly used converters, which perform different voltage conversion functions, are illustrated in Fig. 2.5. In the boost converter, the positions of the inductor and switch are reversed. It is shown later in this chapter that the boost converter steps the voltage up: $V \geq V_g$. Another converter, the buck-boost converter, can either increase or decrease the magnitude of the voltage, but the polarity is inverted. So with a positive input voltage, the ideal buck-boost converter can produce a negative output voltage of any magnitude. It may at first be surprising that dc output voltages can be produced that are greater in magnitude than the input, or that have opposite polarity. But it is indeed possible to produce any desired dc output voltage using a passive network of only inductors, capacitors, and embedded switches.

In the above discussion, it was possible to derive an expression for the output voltage of the buck converter, Eq. (2.3), using some simple arguments based on Fourier analysis. However, it may not be immediately obvious how to directly apply these arguments to find the dc output voltage of the boost, buck–boost, or other converters. The objective of this chapter is the development of a more general method for analyzing any switching converter comprised of a network of inductors, capacitors, and switches [1-8].

The principles of *inductor volt-second balance* and *capacitor charge balance* are derived; these can be used to solve for the inductor currents and capacitor voltages of switching converters. A useful approximation, the *small–ripple* or *linear–ripple approximation*, greatly facilitates the analysis. Some simple methods for selecting the filter element values are also discussed.

2.2 INDUCTOR VOLT-SECOND BALANCE, CAPACITOR CHARGE BALANCE, AND THE SMALL-RIPPLE APPROXIMATION

Let us more closely examine the inductor and capacitor waveforms in the buck converter of Fig. 2.6. It is impossible to build a perfect low-pass filter that allows the dc component to pass but completely removes the components at the switching frequency and its harmonics. So the low-pass filter must allow at least some small amount of the high-frequency harmonics generated by the switch to reach the output. Hence, in practice the output voltage waveform $v(t)$ appears as illustrated in Fig. 2.7, and can be expressed as

$$v(t) = V + v_{ripple}(t) \tag{2.4}$$

So the actual output voltage $v(t)$ consists of the desired dc component V, plus a small undesired ac com-

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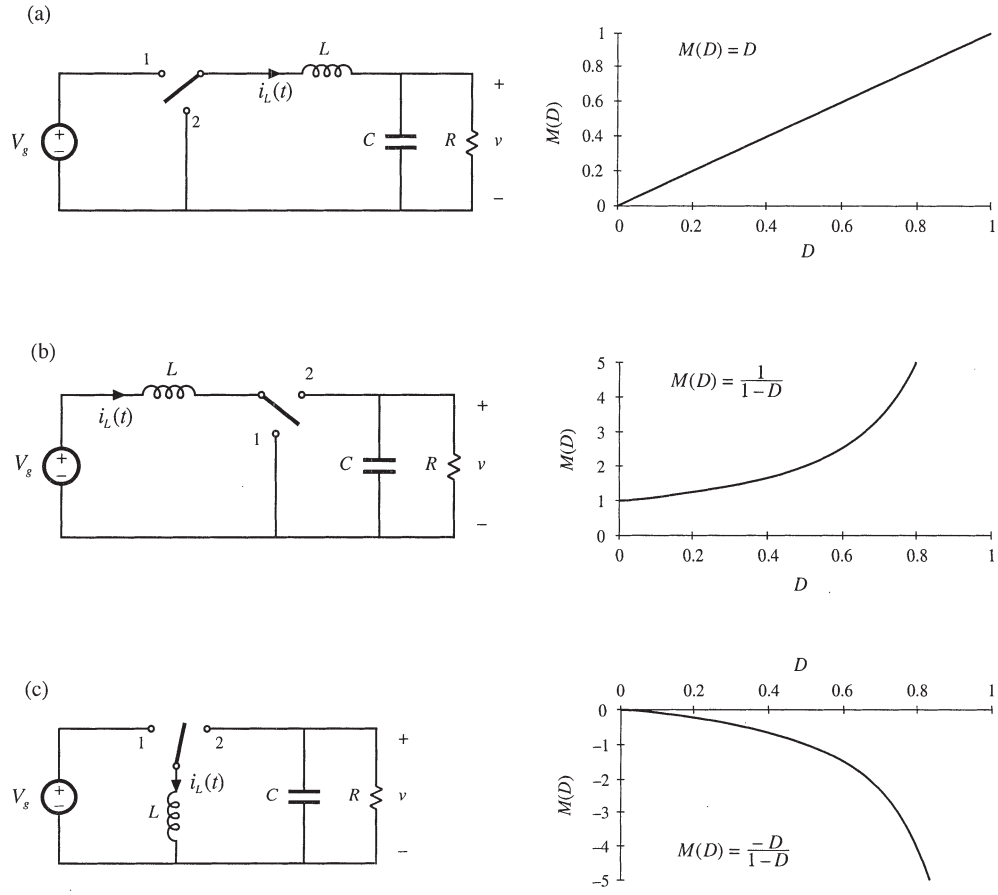


Fig. 2.5 Three basic converters and their dc conversion ratios $M(D) = V/V_g$: (a) buck, (b) boost, (c) buck–boost.

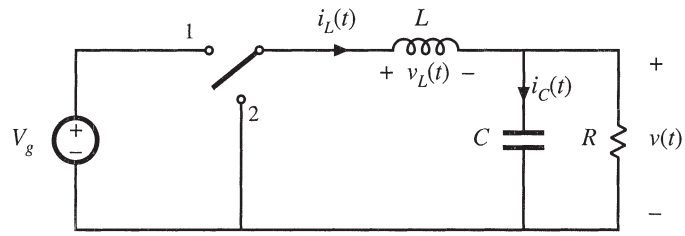


Fig. 2.6 Buck converter circuit, with the inductor voltage $v_L(t)$ and capacitor current $i_C(t)$ waveforms specifically identified.

ponent $v_{ripple}(t)$ arising from the incomplete attenuation of the switching harmonics by the low-pass filter. The magnitude of $v_{ripple}(t)$ has been exaggerated in Fig. 2.7.

The output voltage switching ripple should be small in any well-designed converter, since the object is to produce a dc output. For example, in a computer power supply having a 3.3 V output, the switching ripple is normally required to be less than a few tens of millivolts, or less than 1% of the dc component V. So it is nearly always a good approximation to assume that the magnitude of the switching

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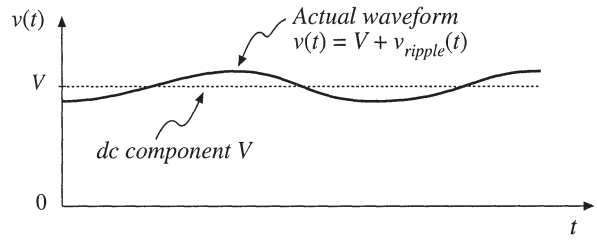


Fig. 2.7 Output voltage waveform $v(t)$, consisting of dc component V and switching ripple $v_{ripple}(t)$.

ripple is much smaller than the dc component:

$$\left| v_{ripple} \right| \ll V \tag{2.5}$$

Therefore, the output voltage $v(t)$ is well approximated by its dc component V, with the small ripple term $v_{ripple}(t)$ neglected:

$$v(t) \approx V \tag{2.6}$$

This approximation, known as the small-ripple approximation, or the linear-ripple approximation, greatly simplifies the analysis of the converter waveforms and is used throughout this book.

Next let us analyze the inductor current waveform. We can find the inductor current by integrating the inductor voltage waveform. With the switch in position 1, the left side of the inductor is connected to the input voltage V_g, and the circuit reduces to Fig. 2.8(a). The inductor voltage $v_L(t)$ is then given by

$$v_L = V_g - v(t) \tag{2.7}$$

As described above, the output voltage $v(t)$ consists of the dc component V, plus a small ac ripple term $v_{ripple}(t)$. We can make the small ripple approximation here, Eq. (2.6), to replace $v(t)$ with its dc component V:

$$v_L \approx V_g - V \tag{2.8}$$

So with the switch in position 1, the inductor voltage is essentially constant and equal to $V_g - V$, as shown in Fig. 2.9. By knowledge of the inductor voltage waveform, the inductor current can be found by use of the definition

$$v_L(t) = L \frac{di_L(t)}{dt} \tag{2.9}$$

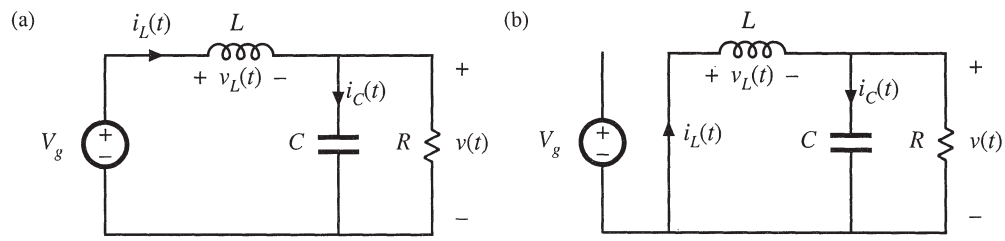


Fig. 2.8 Buck converter circuit: (a) while the switch is in position 1, (b) while the switch is in position 2.

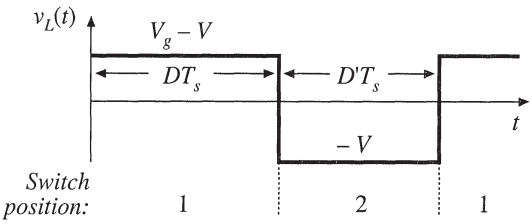


Fig. 2.9 Steady-state inductor voltage waveform, buck converter.

Thus, during the first interval, when $v_L(t)$ is approximately $(V_g - V)$, the slope of the inductor current waveform is

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} \approx \frac{V_g - V}{L} \tag{2.10}$$

which follows by dividing Eq. (2.9) by L, and substituting Eq. (2.8). Since the inductor voltage $v_L(t)$ is essentially constant while the switch is in position 1, the inductor current slope is also essentially constant and the inductor current increases linearly.

Similar arguments apply during the second subinterval, when the switch is in position 2. The left side of the inductor is then connected to ground, leading to the circuit of Fig. 2.8(b). It is important to consistently define the polarities of the inductor current and voltage; in particular, the polarity of $v_L(t)$ is defined consistently in Figs. 2.7, 2.8(a), and 2.8(b). So the inductor voltage during the second subinterval is given by

$$v_L(t) = -v(t) \tag{2.11}$$

Use of the small ripple approximation, Eq. (2.6), leads to

$$v_L(t) \approx -V \tag{2.12}$$

So the inductor voltage is also essentially constant while the switch is in position 2, as illustrated in Fig. 2.9. Substitution of Eq. (2.12) into Eq. (2.9) and solution for the slope of the inductor current yields

$$\frac{di_L(t)}{dt} \approx -\frac{V}{L} \tag{2.13}$$

Hence, during the second subinterval the inductor current changes with a negative and essentially constant slope.

We can now sketch the inductor current waveform (Fig. 2.10). The inductor current begins at some initial value $i_L(0)$. During the first subinterval, with the switch in position 1, the inductor current increases with the slope given in Eq. (2.10). At time $t = DT_s$, the switch changes to position 2. The current then decreases with the constant slope given by Eq. (2.13). At time $t = T_s$, the switch changes back to

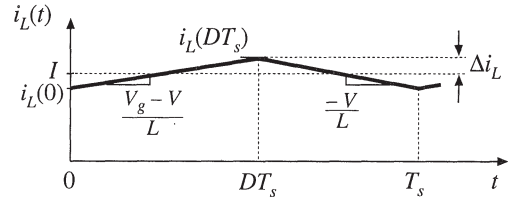


Fig. 2.10 Steady-state inductor current waveform, buck converter.

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position 1, and the process repeats.

It is of interest to calculate the inductor current ripple Δi_L. As illustrated in Fig. 2.10, the peak inductor current is equal to the dc component I plus the peak-to-average ripple Δi_L. This peak current flows through not only the inductor, but also through the semiconductor devices that comprise the switch. Knowledge of the peak current is necessary when specifying the ratings of these devices.

Since we know the slope of the inductor current during the first subinterval, and we also know the length of the first subinterval, we can calculate the ripple magnitude. The $i_L(t)$ waveform is symmetrical about I, and hence during the first subinterval the current increases by $2\Delta i_L$ (since Δi_L is the peak ripple, the peak-to-peak ripple is $2\Delta i_L$). So the change in current, $2\Delta i_L$, is equal to the slope (the applied inductor voltage divided by L) times the length of the first subinterval (DT_s):

$$\begin{aligned} &\text{(change in } i_L\text{)} = \text{(slope)(length of subinterval)} \\ &\left(2\Delta i_L\right) = \left(\frac{V_g - V}{L}\right)\left(DT_s\right) \end{aligned} \tag{2.14}$$

Solution for Δi_L yields

$$\Delta i_L = \frac{V_g - V}{2L} DT_s \tag{2.15}$$

Typical values of Δi_L lie in the range of 10% to 20% of the full-load value of the dc component I. It is undesirable to allow Δi_L to become too large; doing so would increase the peak currents of the inductor and of the semiconductor switching devices, and would increase their size and cost. So by design the inductor current ripple is also usually small compared to the dc component I. The small-ripple approximation $i_L(t) \approx I$ is usually justified for the inductor current.

The inductor value can be chosen such that a desired current ripple Δi_L is attained. Solution of Eq. (2.15) for the inductance L yields

$$L = \frac{V_g - V}{2\Delta i_L} DT_s \tag{2.16}$$

This equation is commonly used to select the value of inductance in the buck converter.

It is entirely possible to solve converters exactly, without use of the small-ripple approximation. For example, one could use the Laplace transform to write expressions for the waveforms of the circuits of Figs. 2.8(a) and 2.8(b). One could then invert the transforms, match boundary conditions, and find the periodic steady-state solution of the circuit. Having done so, one could then find the dc components of the waveforms and the peak values. But this is a great deal of work, and the results are nearly always intractable. Besides, the extra work involved in writing equations that exactly describe the ripple is a waste of time, since the ripple is small and is undesired. The small-ripple approximation is easy to apply, and quickly yields simple expressions for the dc components of the converter waveforms.

The inductor current waveform of Fig. 2.10 is drawn under steady-state conditions, with the converter operating in equilibrium. Let's consider next what happens to the inductor current when the converter is first turned on. Suppose that the inductor current and output voltage are initially zero, and an input voltage V_g is then applied. As shown in Fig. 2.11, $i_L(0)$ is zero. During the first subinterval, with the switch in position 1, we know that the inductor current will increase, with a slope of $(V_g - v)/L$ and with v initially zero. Next, with the switch in position 2, the inductor current will change with a slope of $-v/L$; since v is initially zero, this slope is essentially zero. It can be seen that there is a net increase in inductor current over the first switching period, because $i_L(T_s)$ is greater than $i_L(0)$. Since the inductor current

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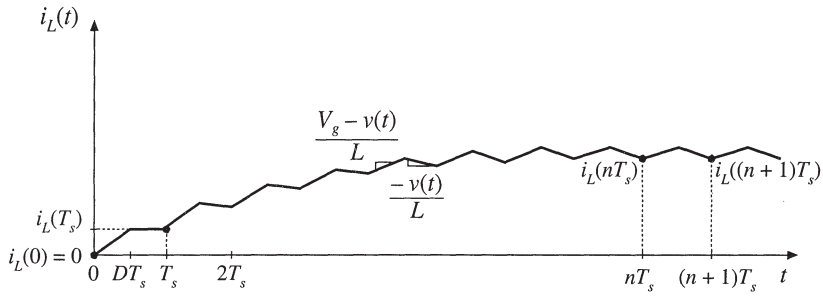


Fig. 2.11 Inductor current waveform during converter turn-on transient.

flows to the output, the output capacitor will charge slightly, and v will increase slightly. The process repeats during the second and succeeding switching periods, with the inductor current increasing during each subinterval 1 and decreasing during each subinterval 2.

As the output capacitor continues to charge and v increases, the slope during subinterval 1 decreases while the slope during subinterval 2 becomes more negative. Eventually, the point is reached where the increase in inductor current during subinterval 1 is equal to the decrease in inductor current during subinterval 2. There is then no net change in inductor current over a complete switching period, and the converter operates in steady state. The converter waveforms are periodic: $i_L(nT_s) = i_L((n + 1)T_s)$. From this point on, the inductor current waveform appears as in Fig. 2.10.

The requirement that, in equilibrium, the net change in inductor current over one switching period be zero leads us to a way to find steady-state conditions in any switching converter: the principle of *inductor volt-second balance*. Given the defining relation of an inductor:

$$v_L(t) = L\frac{di_L(t)}{dt} \tag{2.17}$$

Integration over one complete switching period, say from $t = 0$ to T_s, yields

$$i_L(T_s) - i_L(0) = \frac{1}{L}\int_0^{T_s} v_L(t)dt \tag{2.18}$$

This equation states that the net change in inductor current over one switching period, given by the left-hand side of Eq. (2.18), is proportional to the integral of the applied inductor voltage over the interval. In steady state, the initial and final values of the inductor current are equal, and hence the left-hand side of Eq. (2.18) is zero. Therefore, in steady state the integral of the applied inductor voltage must be zero:

$$0 = \int_0^{T_s} v_L(t)dt \tag{2.19}$$

The right-hand side of Eq. (2.19) has the units of volt-seconds or flux-linkages. Equation (2.19) states that the total area, or net volt-seconds, under the $v_L(t)$ waveform must be zero.

An equivalent form is obtained by dividing both sides of Eq. (2.19) by the switching period T_s:

$$0 = \frac{1}{T_s}\int_0^{T_s} v_L(t)dt = \langle v_L \rangle \tag{2.20}$$

The right-hand side of Eq. (2.20) is recognized as the average value, or dc component, of $v_L(t)$. Equation

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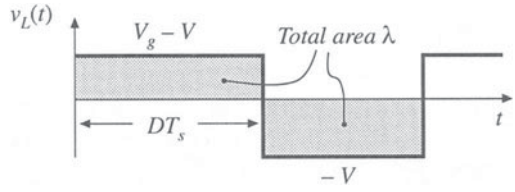


Fig. 2.12 The principle of inductor volt-second balance: in steady state, the net volt-seconds applied to an inductor (i.e., the total area λ) must be zero.

(2.20) states that, in equilibrium, the applied inductor voltage must have zero dc component.

The inductor voltage waveform of Fig. 2.9 is reproduced in Fig. 2.12, with the area under the $v_L(t)$ curve specifically identified. The total area λ is given by the areas of the two rectangles, or

$$\lambda = \int_0^{T_s} v_L(t)\,dt = \left(V_g - V\right)\left(DT_s\right) + \left(-V\right)\left(D'T_s\right) \tag{2.21}$$

The average value is therefore

$$\left\langle v_L \right\rangle = \frac{\lambda}{T_s} = D\left(V_g - V\right) + D'\left(-V\right) \tag{2.22}$$

By equating $\langle v_L \rangle$ to zero, and noting that $D + D' = 1$, one obtains

$$0 = DV_g - \left(D + D'\right)V = DV_g - V \tag{2.23}$$

Solution for V yields

$$V = DV_g \tag{2.24}$$

which coincides with the result obtained previously, Eq. (2.3). So the principle of inductor volt-second balance allows us to derive an expression for the dc component of the converter output voltage. An advantage of this approach is its generality—it can be applied to any converter. One simply sketches the applied inductor voltage waveform, and equates the average value to zero. This method is used later in this chapter, to solve several more complicated converters.

Similar arguments can be applied to capacitors. The defining equation of a capacitor is

$$i_C(t) = C\,\frac{dv_C(t)}{dt} \tag{2.25}$$

Integration of this equation over one switching period yields

$$v_C(T_s) - v_C(0) = \frac{1}{C}\int_0^{T_s} i_C(t)\,dt \tag{2.26}$$

In steady state, the net change over one switching period of the capacitor voltage must be zero, so that the left-hand side of Eq. (2.26) is equal to zero. Therefore, in equilibrium the integral of the capacitor current over one switching period (having the dimensions of amp-seconds, or charge) should be zero. There is no net change in capacitor charge in steady state. An equivalent statement is

$$0 = \frac{1}{T_s}\int_0^{T_s} i_C(t)\,dt = \langle i_C \rangle \tag{2.27}$$

The average value, or dc component, of the capacitor current must be zero in equilibrium.

This should be an intuitive result. If a dc current is applied to a capacitor, then the capacitor will charge continually and its voltage will increase without bound. Likewise, if a dc voltage is applied to an inductor, then the flux will increase continually and the inductor current will increase without bound. Equation (2.27), called the principle of *capacitor amp-second balance* or *capacitor charge balance*, can be used to find the steady-state currents in a switching converter.

2.3 BOOST CONVERTER EXAMPLE

The boost converter, Fig. 2.13(a), is another well-known switched-mode converter that is capable of producing a dc output voltage greater in magnitude than the dc input voltage. A practical realization of the switch, using a MOSFET and diode, is shown in Fig. 2.13(b). Let us apply the small-ripple approximation and the principles of inductor volt-second balance and capacitor charge balance to find the steady-state output voltage and inductor current for this converter.

With the switch in position 1, the right-hand side of the inductor is connected to ground, resulting in the network of Fig. 2.14(a). The inductor voltage and capacitor current for this subinterval are given by

$$\begin{aligned} v_L &= V_g \\ i_C &= -\frac{v}{R} \end{aligned} \tag{2.28}$$

Use of the linear ripple approximation, $v \approx V$, leads to

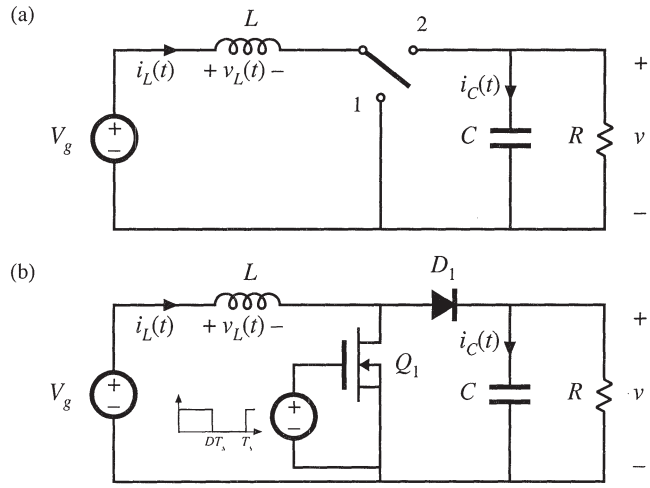


Fig. 2.13 Boost converter: (a) with ideal switch, (b) practical realization using MOSFET and diode.

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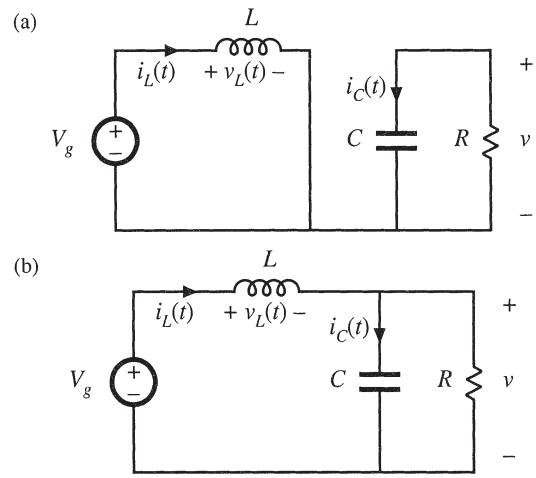


Fig. 2.14 Boost converter circuit, (a) while the switch is in position 1, (b) while the switch is in position 2.

$$\begin{aligned} v_L &= V_g \\ i_C &= -\frac{V}{R} \end{aligned} \tag{2.29}$$

With the switch in position 2, the inductor is connected to the output, leading to the circuit of Fig. 2.14(b). The inductor voltage and capacitor current are then

$$\begin{aligned} v_L &= V_g - v \\ i_C &= i_L - \frac{v}{R} \end{aligned} \tag{2.30}$$

Use of the small-ripple approximation, $v \approx V$ and $i_L \approx I$, leads to

$$\begin{aligned} v_L &= V_g - V \\ i_C &= I - \frac{V}{R} \end{aligned} \tag{2.31}$$

Equations (2.29) and (2.31) are used to sketch the inductor voltage and capacitor current waveforms of Fig. 2.15.

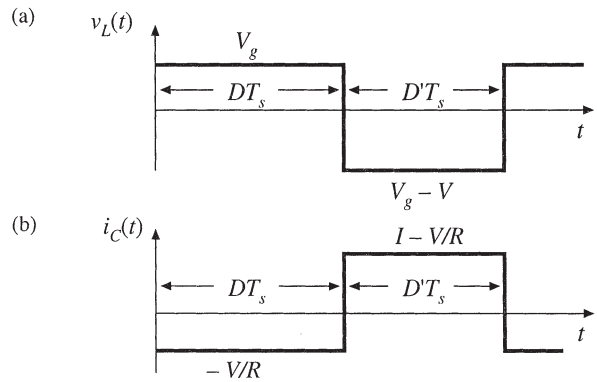


Fig. 2.15 Boost converter voltage and current waveforms.

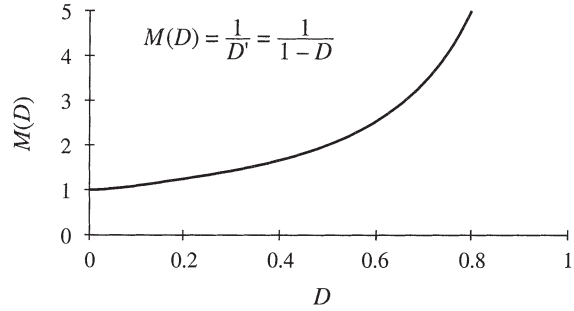


Fig. 2.16 Dc conversion ratio $M(D)$ of the boost converter.

It can be inferred from the inductor voltage waveform of Fig. 2.15(a) that the dc output voltage V is greater than the input voltage V_g. During the first subinterval, $v_L(t)$ is equal to the dc input voltage V_g, and positive volt-seconds are applied to the inductor. Since, in steady-state, the total volt-seconds applied over one switching period must be zero, negative volt-seconds must be applied during the second subinterval. Therefore, the inductor voltage during the second subinterval, $(V_g - V)$, must be negative. Hence, V is greater than V_g.

The total volt-seconds applied to the inductor over one switching period are:

$$\int_0^{T_s} v_L(t)dt = \left(V_g\right)DT_s + \left(V_g - V\right)D'T_s \tag{2.32}$$

By equating this expression to zero and collecting terms, one obtains

$$V_g(D + D') - VD' = 0 \tag{2.33}$$

Solution for V, and by noting that $(D + D') = 1$, yields the expression for the output voltage,

$$V = \frac{V_g}{D'} \tag{2.34}$$

The voltage conversion ratio $M(D)$ is the ratio of the output to the input voltage of a dc-dc converter. Equation (2.34) predicts that the voltage conversion ratio is given by

$$M(D) = \frac{V}{V_g} = \frac{1}{D'} = \frac{1}{1 - D} \tag{2.35}$$

This equation is plotted in Fig. 2.16. At $D = 0$, $V = V_g$. The output voltage increases as D increases, and in the ideal case tends to infinity as D tends to 1. So the ideal boost converter is capable of producing any output voltage greater than the input voltage. There are, of course, limits to the output voltage that can be produced by a practical boost converter. In the next chapter, component nonidealities are modeled, and it is found that the maximum output voltage of a practical boost converter is indeed limited. Nonetheless, very large output voltages can be produced if the nonidealities are sufficiently small.

The dc component of the inductor current is derived by use of the principle of capacitor charge balance. During the first subinterval, the capacitor supplies the load current, and the capacitor is partially discharged. During the second subinterval, the inductor current supplies the load and, additionally, recharges the capacitor. The net change in capacitor charge over one switching period is found by integrating the $i_C(t)$ waveform of Fig. 2.15(b),

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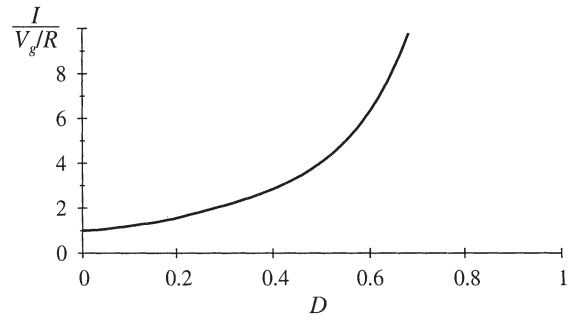


Fig. 2.17 Variation of inductor current dc component I with duty cycle, boost converter.

$$\int_0^{T_s} i_C(t)\,dt = \left(-\frac{V}{R}\right)DT_s + \left(I - \frac{V}{R}\right)D'T_s \tag{2.36}$$

Collecting terms, and equating the result to zero, leads the steady-state result

$$-\frac{V}{R}\left(D + D'\right) + ID' = 0 \tag{2.37}$$

By noting that $(D + D') = 1$, and by solving for the inductor current dc component I, one obtains

$$I = \frac{V}{D'R} \tag{2.38}$$

So the inductor current dc component I is equal to the load current, V/R, divided by D'. Substitution of Eq. (2.34) to eliminate V yields

$$I = \frac{V_g}{D'^2R} \tag{2.39}$$

This equation is plotted in Fig. 2.17. It can be seen that the inductor current becomes large as D approaches 1.

This inductor current, which coincides with the dc input current in the boost converter, is greater than the load current. Physically, this must be the case: to the extent that the converter elements are ideal, the converter input and output powers are equal. Since the converter output voltage is greater than the input voltage, the input current must likewise be greater than the output current. In practice, the inductor current flows through the semiconductor forward voltage drops, the inductor winding resistance, and other sources of power loss. As the duty cycle approaches one, the inductor current becomes very large and these component nonidealities lead to large power losses. In consequence, the efficiency of the boost converter decreases rapidly at high duty cycle.

Next, let us sketch the inductor current $i_L(t)$ waveform and derive an expression for the inductor current ripple Δi_L. The inductor voltage waveform $v_L(t)$ has been already found (Fig. 2.15), so we can sketch the inductor current waveform directly. During the first subinterval, with the switch in position 1, the slope of the inductor current is given by

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g}{L} \tag{2.40}$$

Likewise, when the switch is in position 2, the slope of the inductor current waveform is

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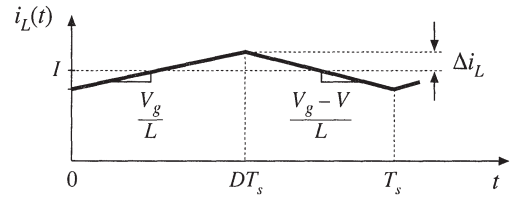


Fig. 2.18 Boost converter inductor current waveform $i_L(t)$.

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g - V}{L} \tag{2.41}$$

The inductor current waveform is sketched in Fig. 2.18. During the first subinterval, the change in inductor current, $2\Delta i_L$, is equal to the slope multiplied by the length of the subinterval, or

$$2\Delta i_L = \frac{V_g}{L} DT_s \tag{2.42}$$

Solution for Δi_L leads to

$$\Delta i_L = \frac{V_g}{2L} DT_s \tag{2.43}$$

This expression can be used to select the inductor value L such that a given value of Δi_L is obtained.

Likewise, the capacitor voltage $v(t)$ waveform can be sketched, and an expression derived for the output voltage ripple peak magnitude Δv. The capacitor current waveform $i_C(t)$ is given in Fig. 2.15. During the first subinterval, the slope of the capacitor voltage waveform $v(t)$ is

$$\frac{dv_C(t)}{dt} = \frac{i_C(t)}{C} = \frac{-V}{RC} \tag{2.44}$$

During the second subinterval, the slope is

$$\frac{dv_C(t)}{dt} = \frac{i_C(t)}{C} = \frac{I}{C} - \frac{V}{RC} \tag{2.45}$$

The capacitor voltage waveform is sketched in Fig. 2.19. During the first subinterval, the change in capacitor voltage, $-2\Delta v$, is equal to the slope multiplied by the length of the subinterval:

$$-2\Delta v = \frac{-V}{RC} DT_s \tag{2.46}$$

Solution for Δv yields

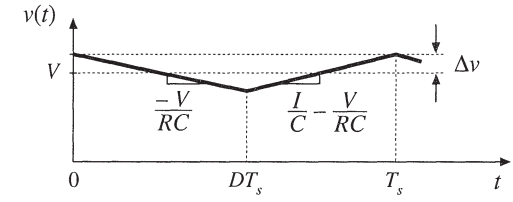


Fig. 2.19 Boost converter output voltage waveform $v(t)$.

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$$\Delta v = \frac{V}{2RC} DT_s \tag{2.47}$$

This expression can be used to select the capacitor value C to obtain a given output voltage ripple peak magnitude Δv.

2.4 ĆUK CONVERTER EXAMPLE

As a second example, consider the Ćuk converter of Fig. 2.20(a). This converter performs a dc conversion function similar to the buck-boost converter: it can either increase or decrease the magnitude of the dc voltage, and it inverts the polarity. A practical realization using a transistor and diode is illustrated in Fig. 2.20(b).

This converter operates via capacitive energy transfer. As illustrated in Fig. 2.21, capacitor C_1 is connected through L_1 to the input source while the switch is in position 2, and source energy is stored in C_1. When the switch is in position 1, this energy is released through L_2 to the load.

The inductor currents and capacitor voltages are defined, with polarities assigned somewhat arbitrarily, in Fig. 2.20(a). In this section, the principles of inductor volt-second balance and capacitor charge balance are applied to find the dc components of the inductor currents and capacitor voltages. The voltage and current ripple magnitudes are also found.

During the first subinterval, while the switch is in position 1, the converter circuit reduces to Fig. 2.21(a). The inductor voltages and capacitor currents are:

$$\begin{aligned} v_{L1} &= V_g \\ v_{L2} &= -v_1 - v_2 \\ i_{C1} &= i_2 \\ i_{C2} &= i_2 - \frac{v_2}{R} \end{aligned} \tag{2.48}$$

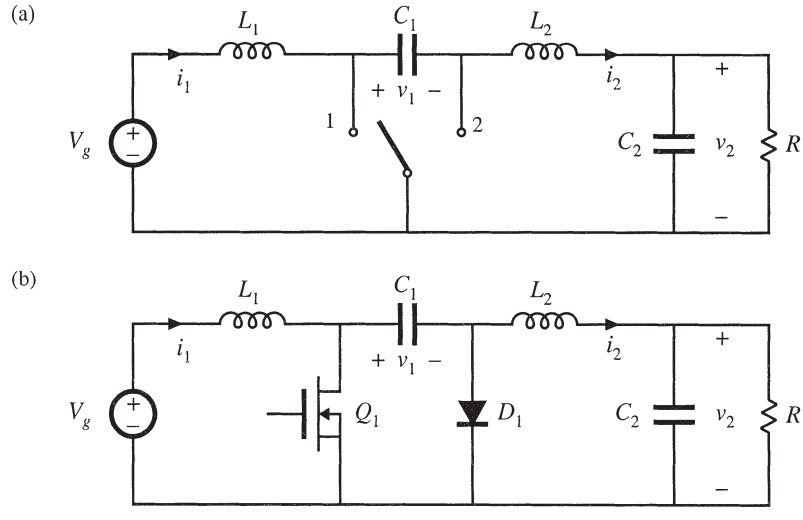


Fig. 2.20 Ćuk converter: (a) with ideal switch, (b) practical realization using MOSFET and diode.

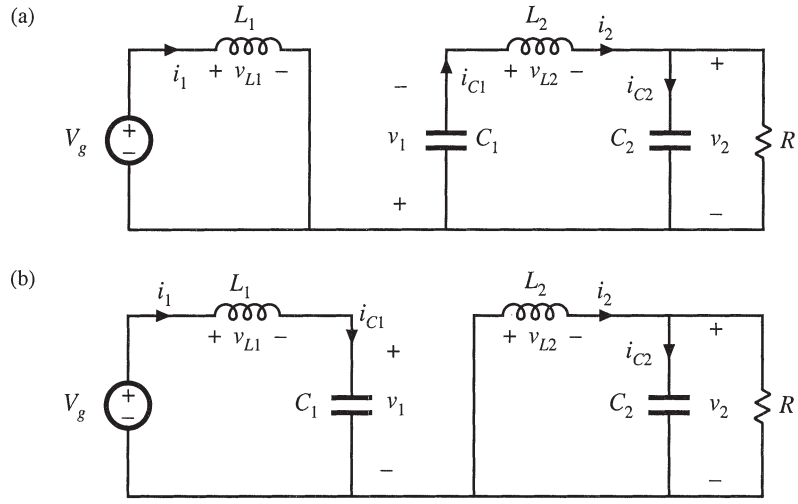


Fig. 2.21 Ćuk converter circuit: (a) while switch is in position 1, (b) while switch is in position 2.

We next assume that the switching ripple magnitudes in $i_1(t)$, $i_2(t)$, $v_1(t)$, and $v_2(t)$ are small compared to their respective dc components I_1, I_2, V_1, and V_2. We can therefore make the small-ripple approximation, and Eq. (2.48) becomes

$$\begin{aligned} v_{L1} &= V_g \\ v_{L2} &= -V_1 - V_2 \\ i_{C1} &= I_2 \\ i_{C2} &= I_2 - \frac{V_2}{R} \end{aligned} \tag{2.49}$$

During the second subinterval, with the switch in position 2, the converter circuit elements are connected as in Fig. 2.21(b). The inductor voltages and capacitor currents are:

$$\begin{aligned} v_{L1} &= V_g - v_1 \\ v_{L2} &= -v_2 \\ i_{C1} &= i_1 \\ i_{C2} &= i_2 - \frac{v_2}{R} \end{aligned} \tag{2.50}$$

We again make the small-ripple approximation, and hence Eq. (2.50) becomes

$$\begin{aligned} v_{L1} &= V_g - V_1 \\ v_{L2} &= -V_2 \\ i_{C1} &= I_1 \\ i_{C2} &= I_2 - \frac{V_2}{R} \end{aligned} \tag{2.51}$$

Equations (2.49) and (2.51) are used to sketch the inductor voltage and capacitor current waveforms in Fig. 2.22.

The next step is to equate the dc components, or average values, of the waveforms of Fig. 2.22

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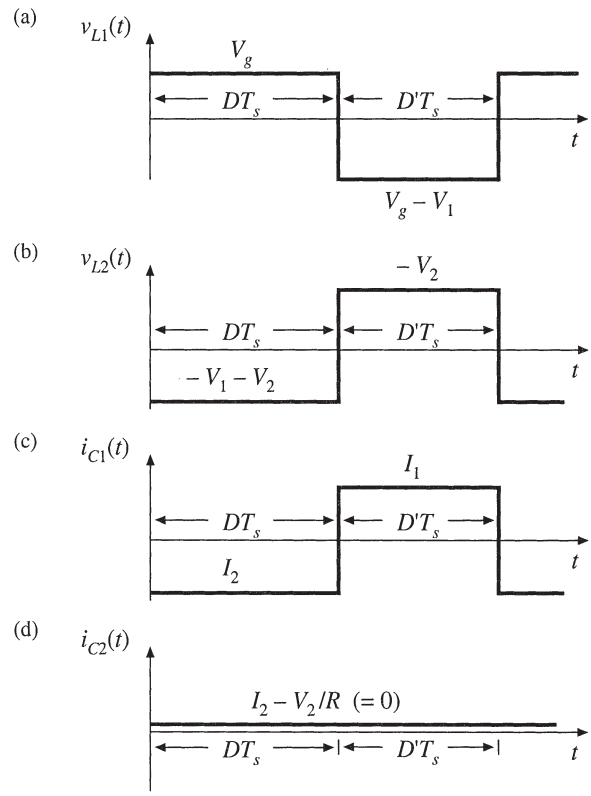


Fig. 2.22 Ćuk converter waveforms: (a) inductor voltage $v_{L1}(t)$, (b) inductor voltage $v_{L2}(t)$, (c) capacitor current $i_{C1}(t)$, (d) capacitor current $i_{C2}(t)$.

to zero, to find the steady-state conditions in the converter. The results are:

$$\begin{aligned}
\langle v_{L1} \rangle &= DV_g + D'(V_g - V_1) = 0 \\
\langle v_{L2} \rangle &= D(-V_1 - V_2) + D'(-V_2) = 0 \\
\langle i_{C1} \rangle &= DI_2 + D'I_1 = 0 \\
\langle i_{C2} \rangle &= I_2 - \frac{V_2}{R} = 0
\end{aligned} \tag{2.52}$$

Solution of this system of equations for the dc components of the capacitor voltages and inductor currents leads to

$$\begin{aligned}
V_1 &= \frac{V_g}{D'} \\
V_2 &= -\frac{D}{D'} V_g \\
I_1 &= -\frac{D}{D'} I_2 = \left(\frac{D}{D'}\right)^2 \frac{V_g}{R} \\
I_2 &= \frac{V_2}{R} = -\frac{D}{D'} \frac{V_g}{R}
\end{aligned} \tag{2.53}$$

The dependence of the dc output voltage V_2 on the duty cycle D is sketched in Fig. 2.23.

The inductor current waveforms are sketched in Fig. 2.24(a) and 2.24(b), and the capacitor C_1

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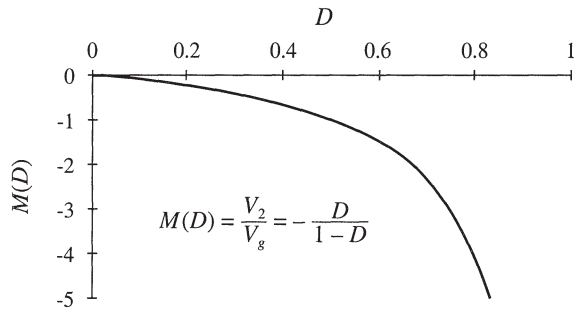


Fig. 2.23 Dc conversion ratio $M(D) = -V/V_g$ of the Ćuk converter.

voltage waveform $v_1(t)$ is sketched in Fig. 2.24(c). During the first subinterval, the slopes of the waveforms are given by

$$\begin{aligned}\frac{di_1(t)}{dt} &= \frac{v_{L1}(t)}{L_1} = \frac{V_g}{L_1} \\ \frac{di_2(t)}{dt} &= \frac{v_{L2}(t)}{L_2} = \frac{-V_1 - V_2}{L_2} \\ \frac{dv_1(t)}{dt} &= \frac{i_{C1}(t)}{C_1} = \frac{I_2}{C_1}\end{aligned} \tag{2.54}$$

Equation (2.49) has been used here to substitute for the values of v_{L1}, v_{L2}, and i_{C1} during the first subinterval. During the second interval, the slopes of the waveforms are given by

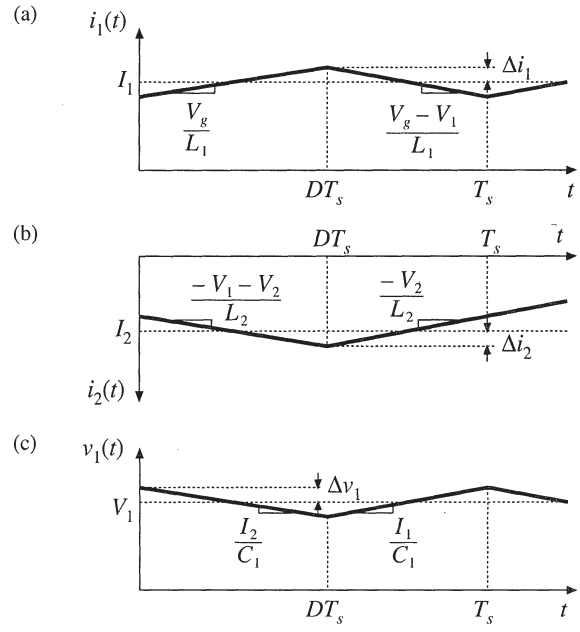


Fig. 2.24 Ćuk converter waveforms: (a) inductor current $i_1(t)$, (b) inductor current $i_2(t)$, (c) capacitor voltage $v_1(t)$.

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$$\begin{aligned}\frac{di_1(t)}{dt} &= \frac{v_{L1}(t)}{L_1} = \frac{V_g - V_1}{L_1} \\ \frac{di_2(t)}{dt} &= \frac{v_{L2}(t)}{L_2} = \frac{-V_2}{L_2} \\ \frac{dv_1(t)}{dt} &= \frac{i_{C1}(t)}{C_1} = \frac{I_1}{C_1}\end{aligned} \tag{2.55}$$

Equation (2.51) was used to substitute for the values of v_{L1}, v_{L2}, and i_{C1} during the second subinterval.

During the first subinterval, the quantities $i_1(t)$, $i_2(t)$, and $v_1(t)$ change by $2\Delta i_1$, $-2\Delta i_2$, and $-2\Delta v_1$, respectively. These changes are equal to the slopes given in Eq. (2.54), multiplied by the subinterval length DT_s, yielding

$$\begin{aligned}\Delta i_1 &= \frac{V_g D T_s}{2L_1} \\ \Delta i_2 &= \frac{V_1 + V_2}{2L_2} DT_s \\ \Delta v_1 &= \frac{-I_2 D T_s}{2C_1}\end{aligned} \tag{2.56}$$

The dc relationships, Eq. (2.53), can now be used to simplify these expressions and eliminate V_1, V_2, and I_1, leading to

$$\begin{aligned}\Delta i_1 &= \frac{V_g D T_s}{2L_1} \\ \Delta i_2 &= \frac{V_g D T_s}{2L_2} \\ \Delta v_1 &= \frac{V_g D^2 T_s}{2D'RC_1}\end{aligned} \tag{2.57}$$

These expressions can be used to select values of L_1, L_2, and C_1, such that desired values of switching ripple magnitudes are obtained.

Similar arguments cannot be used to estimate the switching ripple magnitude in the output capacitor voltage $v_2(t)$. According to Fig. 2.22(d), the current $i_{C2}(t)$ is continuous: unlike v_{L1}, v_{L2}, and i_{C1}, the capacitor current $i_{C2}(t)$ is nonpulsating. If the switching ripple of $i_2(t)$ is neglected, then the capacitor current $i_{C2}(t)$ does not contain an ac component. The small-ripple approximation then leads to the conclusion that the output switching ripple Δv_2 is zero.

Of course, the output voltage switching ripple is not zero. To estimate the magnitude of the output voltage ripple in this converter, we must not neglect the switching ripple present in the inductor current $i_2(t)$, since this current ripple is the only source of ac current driving the output capacitor C_2. A simple way of doing this in the Ćuk converter and in other similar converters is discussed in the next section.

2.5 ESTIMATING THE OUTPUT VOLTAGE RIPPLE IN CONVERTERS CONTAINING TWO-POLE LOW-PASS FILTERS

A case where the small ripple approximation is not useful is in converters containing two-pole low-pass filters, such as in the output of the Ćuk converter (Fig. 2.20) or the buck converter (Fig. 2.25). For these

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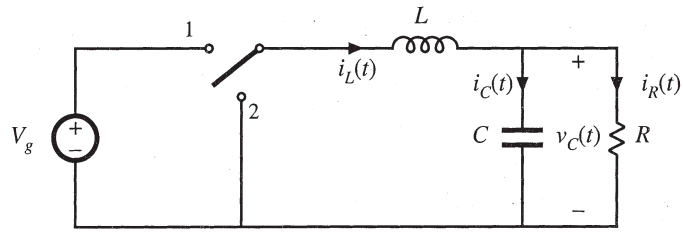


Fig. 2.25 The buck converter contains a two-pole output filter.

converters, the small-ripple approximation predicts zero output voltage ripple, regardless of the value of the output filter capacitance. The problem is that the only component of output capacitor current in these cases is that arising from the inductor current ripple. Hence, inductor current ripple cannot be neglected when calculating the output capacitor voltage ripple, and a more accurate approximation is needed.

An improved approach that is useful for this case is to estimate the capacitor current waveform $i_C(t)$ more accurately, accounting for the inductor current ripple. The capacitor voltage ripple can then be related to the total charge contained in the positive portion of the $i_C(t)$ waveform.

Consider the buck converter of Fig. 2.25. The inductor current waveform $i_L(t)$ contains a dc component I and linear ripple of peak magnitude Δi_L, as shown in Fig. 2.10. The dc component I must flow entirely through the load resistance R (why?), while the ac switching ripple divides between the load resistance R and the filter capacitor C. In a well-designed converter, in which the capacitor provides significant filtering of the switching ripple, the capacitance C is chosen large enough that its impedance at the switching frequency is much smaller than the load impedance R. Hence nearly all of the inductor current ripple flows through the capacitor, and very little flows through the load. As shown in Fig. 2.26, the capacitor current waveform $i_C(t)$ is then equal to the inductor current waveform with the dc component removed. The current ripple is linear, with peak value Δi_L.

When the capacitor current $i_C(t)$ is positive, charge is deposited on the capacitor plates and the capacitor voltage $v_C(t)$ increases. Therefore, between the two zero-crossings of the capacitor current waveform, the capacitor voltage changes between its minimum and maximum extrema. The waveform is symmetrical, and the total change in v_C is the peak-to-peak output voltage ripple, or $2\Delta v$.

This change in capacitor voltage can be related to the total charge q contained in the positive

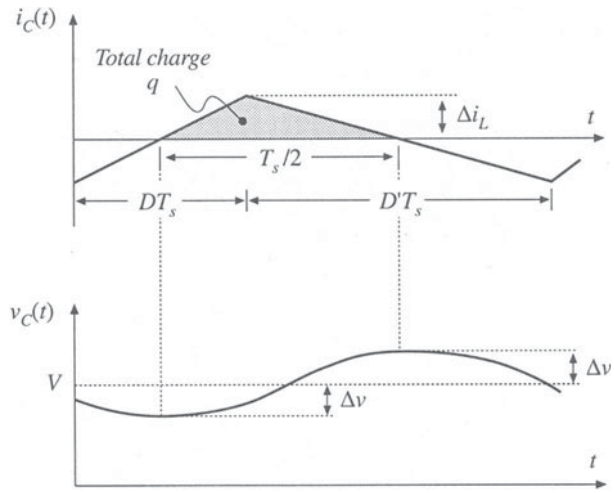


Fig. 2.26 Output capacitor voltage and current waveforms, for the buck converter in Fig. 2.25.

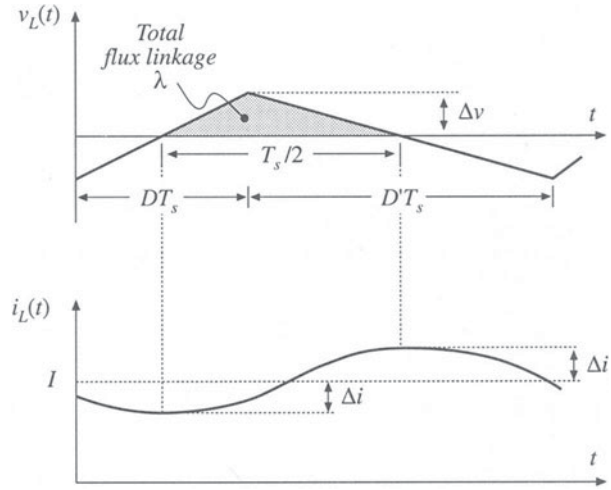


Fig. 2.27 Estimating inductor current ripple when the inductor voltage waveform is continuous.

portion of the capacitor current waveform. By the capacitor relation $Q = CV$,

$$q = C(2\Delta v) \tag{2.58}$$

As illustrated in Fig. 2.26, the charge q is the integral of the current waveform between its zero crossings. For this example, the integral can be expressed as the area of the shaded triangle, having a height Δi_L. Owing to the symmetry of the current waveform, the zero crossings occur at the centerpoints of the DT_s and $D'T_s$ subintervals. Hence, the base dimension of the triangle is $T_s/2$. So the total charge q is given by

$$q = \tfrac{1}{2}\Delta i_L \frac{T_s}{2} \tag{2.59}$$

Substitution of Eq. (2.58) into Eq. (2.59), and solution for the voltage ripple peak magnitude Δv yields

$$\Delta v = \frac{\Delta i_L T_s}{8C} \tag{2.60}$$

This expression can be used to select a value for the capacitance C such that a given voltage ripple Δv is obtained. In practice, the additional voltage ripple caused by the capacitor equivalent series resistance (esr) must also be included.

Similar arguments can be applied to inductors. An example is considered in Problem 2.9, in which a two-pole input filter is added to a buck converter as in Fig. 2.32. The capacitor voltage ripple cannot be neglected; doing so would lead to the conclusion that no ac voltage is applied across the input filter inductor, resulting in zero input current ripple. The actual inductor voltage waveform is identical to the ac portion of the input filter capacitor voltage, with linear ripple and with peak value Δv as illustrated in Fig. 2.27. By use of the inductor relation $\lambda = Li$, a result similar to Eq. (2.60) can be derived. The derivation is left as a problem for the student.

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2.6 SUMMARY OF KEY POINTS

1. The dc component of a converter waveform is given by its average value, or the integral over one switching period, divided by the switching period. Solution of a dc-dc converter to find its dc, or steady-state, voltages and currents therefore involves averaging the waveforms.
2. The linear- (or small-) ripple approximation greatly simplifies the analysis. In a well-designed converter, the switching ripples in the inductor currents and capacitor voltages are small compared to the respective dc components, and can be neglected.
3. The principle of inductor volt-second balance allows determination of the dc voltage components in any switching converter. In steady state, the average voltage applied to an inductor must be zero.
4. The principle of capacitor charge balance allows determination of the dc components of the inductor currents in a switching converter. In steady state, the average current applied to a capacitor must be zero.
5. By knowledge of the slopes of the inductor current and capacitor voltage waveforms, the ac switching ripple magnitudes may be computed. Inductance and capacitance values can then be chosen to obtain desired ripple magnitudes.
6. In converters containing multiple-pole filters, continuous (nonpulsating) voltages and currents are applied to one or more of the inductors or capacitors. Computation of the ac switching ripple in these elements can be done using capacitor charge and/or inductor flux-linkage arguments, without use of the small-ripple approximation.
7. Converters capable of increasing (boost), decreasing (buck), and inverting the voltage polarity (buck-boost and Ćuk) have been described. Converter circuits are explored more fully in the problems and in a later chapter.

REFERENCES

[1] S. ĆUK, "Basics of Switched-Mode Power Conversion: Topologies, Magnetics, and Control," in *Advances in Switched-Mode Power Conversion*, Vol. 2, pp. 279-310, Irvine, CA: Teslaco, 1981.

[2] N. MOHAN, T. UNDELAND, and W. ROBBINS, *Power Electronics: Converters, Applications, and Design*, 2nd edit., New York: John Wiley & Sons, 1995.

[3] J. KASSAKIAN, M. SCHLECHT, and G. VERGESE, *Principles of Power Electronics*, Reading, MA: Addison-Wesley, 1991.

[4] R. SEVERNS and G. E. BLOOM, *Modern Dc-to-dc Switch Mode Power Converter Circuits*, New York: Van Nostrand Reinhold, 1985.

[5] D. HART, *Introduction to Power Electronics*, New York: Prentice Hall, 1997.

[6] M. RASHID, *Power Electronics: Circuits, Devices, and Applications*, 2nd edit., New York: Prentice Hall, 1993.

[7] P. KREIN, *Elements of Power Electronics*, New York: Oxford University Press, 1998.

[8] K. KIT SUM, *Switch Mode Power Conversion—Basic Theory and Design*, New York: Marcel Dekker, 1984.

PROBLEMS

2.1 Analysis and design of a buck-boost converter: A buck-boost converter is illustrated in Fig. 2.28(a), and a practical implementation using a transistor and diode is shown in Fig. 2.28(b).

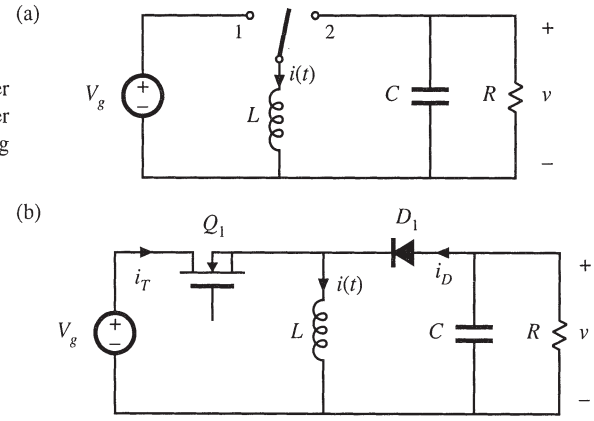


Fig. 2.28 Buck-boost converter of Problem 2.1: (a) ideal converter circuit, (b) implementation using MOSFET and diode.

(a) Find the dependence of the equilibrium output voltage V and inductor current I on the duty ratio D, input voltage V_g, and load resistance R. You may assume that the inductor current ripple and capacitor voltage ripple are small.

(b) Plot your results of part (a) over the range $0 \leq D \leq 1$.

(c) Dc design: for the specifications

$V_g = 30$ V $\qquad V = -20$ V

$R = 4\ \Omega \qquad f_s = 40$ kHz

(*i*) Find D and I

(*ii*) Calculate the value of L that will make the peak inductor current ripple Δi equal to ten percent of the average inductor current I.

(*iii*) Choose C such that the peak output voltage ripple Δv is 0.1 V.

(d) Sketch the transistor drain current waveform $i_T(t)$ for your design of part (c). Include the effects of inductor current ripple. What is the peak value of i_T? Also sketch $i_T(t)$ for the case when L is decreased such that Δi is 50% of I. What happens to the peak value of i_T in this case?

(e) Sketch the diode current waveform $i_D(t)$ for the two cases of part (d).

2.2 In a certain application, an unregulated dc input voltage can vary between 18 and 36 V. It is desired to produce a regulated output of 28 V to supply a 2 A load. Hence, a converter is needed that is capable of both increasing and decreasing the voltage. Since the input and output voltages are both positive, converters that invert the voltage polarity (such as the basic buck-boost converter) are not suited for this application.

One converter that is capable of performing the required function is the nonisolated SEPIC (single-ended primary inductance converter) shown in Fig. 2.29. This converter has a conversion ratio $M(D)$ that can both buck and boost the voltage, but the voltage polarity is not inverted. In the normal converter operating mode, the transistor conducts during the first subinterval ($0 < t < DT_s$), and the diode conducts during the second subinterval ($DT_s < t < T_s$). You may assume that all elements are ideal.

(a) Derive expressions for the dc components of each capacitor voltage and inductor current, as functions of the duty cycle D, the input voltage V_g, and the load resistance R.

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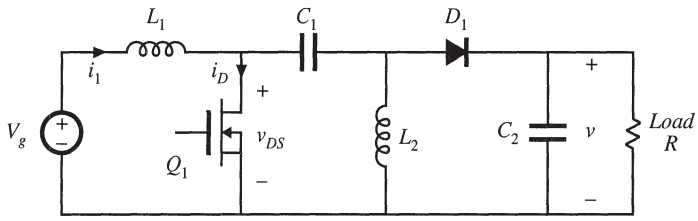


Fig. 2.29 SEPIC of Problems 2.2 and 2.3.

(b) A control circuit automatically adjusts the converter duty cycle D, to maintain a constant output voltage of $V = 28$ V. The input voltage slowly varies over the range 18 V $\le V_g \le$ 36 V. The load current is constant and equal to 2 A. Over what range will the duty cycle D vary? Over what range will the input inductor current dc component I_1 vary?

2.3 For the SEPIC of Problem 2.2,

(a) Derive expressions for each inductor current ripple and capacitor voltage ripple. Express these quantities as functions of the switching period T_s; the component values L_1, L_2, C_1, C_2; the duty cycle D; the input voltage V_g; and the load resistance R.

(b) Sketch the waveforms of the transistor voltage $v_{DS}(t)$ and transistor current $i_D(t)$, and give expressions for their peak values.

2.4 The switches in the converter of Fig. 2.30 operate synchronously: each is in position 1 for $0 < t < DT_s$, and in position 2 for $DT_s < t < T_s$. Derive an expression for the voltage conversion ratio $M(D) = V/V_g$. Sketch $M(D)$ vs. D.

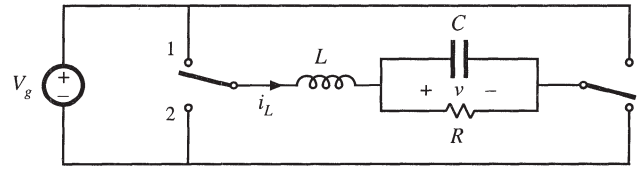


Fig. 2.30 H-bridge converter of Problems 2.4 and 2.6.

2.5 The switches in the converter of Fig. 2.31 operate synchronously: each is in position 1 for $0 < t < DT_s$, and in position 2 for $DT_s < t < T_s$. Derive an expression for the voltage conversion ratio $M(D) = V/V_g$. Sketch $M(D)$ vs. D.

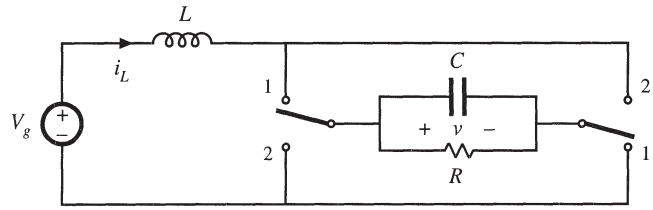


Fig. 2.31 Current-fed bridge converter of Problems 2.5, 2.7, and 2.8.

2.6 For the converter of Fig. 2.30, derive expressions for the inductor current ripple Δi_L and the capacitor voltage ripple Δv_C.

2.7 For the converter of Fig. 2.31, derive an analytical expression for the dc component of the inductor cur-

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rent, I, as a function of D, V_g, and R. Sketch your result vs. D.

2.8 For the converter of Fig. 2.31, derive expressions for the inductor current ripple Δi_L and the capacitor voltage ripple Δv_C.

2.9 To reduce the switching harmonics present in the input current of a certain buck converter, an input filter consisting of inductor L_1 and capacitor C_1 is added as shown in Fig. 2.32. Such filters are commonly used to meet regulations limiting conducted electromagnetic interference (EMI). For this problem, you may assume that all inductance and capacitance values are sufficiently large, such that all ripple magnitudes are small.

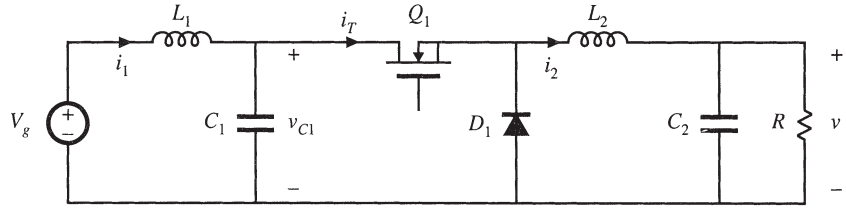


Fig. 2.32 Addition of L–C input filter to buck converter, Problem 2.9.

(a) Sketch the transistor current waveform $i_T(t)$.

(b) Derive analytical expressions for the dc components of the capacitor voltages and inductor currents.

(c) Derive analytical expressions for the peak ripple magnitudes of the input filter inductor current and capacitor voltage.

(d) Given the following values:

Input voltage	$V_g = 48$ V
Output voltage	$V = 36$ V
Switching frequency	$f_s = 100$ kHz
Load resistance	$R = 6\ \Omega$

Select values for L_1 and C_1 such that (*i*) the peak voltage ripple on C_1, Δv_{C1}, is two percent of the dc component V_{C1}, and (*ii*) the input peak current ripple Δi_1 is 20 mA.

Extra credit problem: Derive exact analytical expressions for (*i*) the dc component of the output voltage, and (*ii*) the peak-to-peak inductor current ripple, of the ideal buck-boost converter operating in steady state. Do not make the small-ripple approximation.

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3

Steady-State Equivalent Circuit Modeling, Losses, and Efficiency

Let us now consider the basic functions performed by a switching converter, and attempt to represent these functions by a simple equivalent circuit. The designer of a converter power stage must calculate the network voltages and currents, and specify the power components accordingly. Losses and efficiency are of prime importance. The use of equivalent circuits is a physical and intuitive approach which allows the well-known techniques of circuit analysis to be employed. As noted in the previous chapter, it is desirable to ignore the small but complicated switching ripple, and model only the important dc components of the waveforms.

The dc transformer is used to model the ideal functions performed by a dc-dc converter [1–4]. This simple model correctly represents the relationships between the dc voltages and currents of the converter. The model can be refined by including losses, such as semiconductor forward voltage drops and on-resistances, inductor core and copper losses, etc. The resulting model can be directly solved, to find the voltages, currents, losses, and efficiency in the actual nonideal converter.

3.1 THE DC TRANSFORMER MODEL

As illustrated in Fig. 3.1, any switching converter contains three ports: a power input, a power output, and a control input. The input power is processed as specified by the control input, and then is output to the load. Ideally, these functions are performed with 100% efficiency, and hence

$$P_{in} = P_{out} \tag{3.1}$$

or,

$$V_g I_g = VI \tag{3.2}$$

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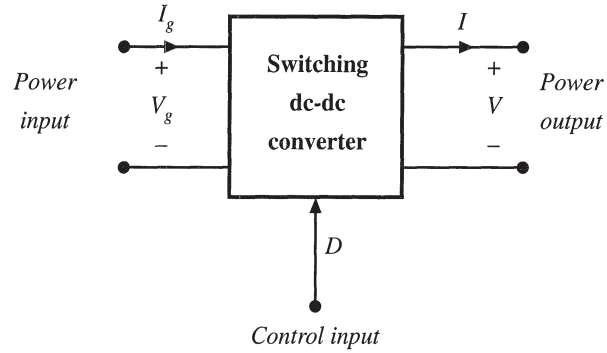


Fig. 3.1 Switching converter terminal quantities.

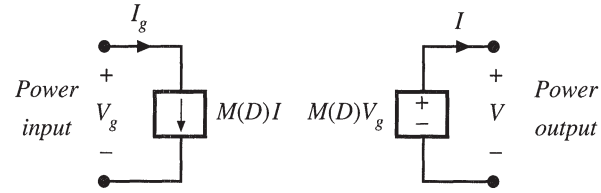


Fig. 3.2 A switching converter equivalent circuit using dependent sources, corresponding to Eqs. (3.3) and (3.4).

These relationships are valid only under equilibrium (dc) conditions: during transients, the net stored energy in the converter inductors and capacitors may change, causing Eqs. (3.1) and (3.2) to be violated.

In the previous chapter, we found that we could express the converter output voltage in an equation of the form

$$V = M(D)V_g \tag{3.3}$$

where $M(D)$ is the equilibrium conversion ratio of the converter. For example, $M(D) = D$ for the buck converter, and $M(D) = 1/(1 - D)$ for the boost converter. In general, for ideal PWM converters operating in the continuous conduction mode and containing an equal number of independent inductors and capacitors, it can be shown that the equilibrium conversion ratio M is a function of the duty cycle D and is independent of load.

Substitution of Eq. (3.3) into Eq. (3.2) yields

$$I_g = M(D)I \tag{3.4}$$

Hence, the converter terminal currents are related by the same conversion ratio.

Equations (3.3) and (3.4) suggest that the converter could be modeled using dependent sources, as in Fig. 3.2. An equivalent but more physically meaningful model (Fig. 3.3) can be obtained through the realization that Eqs. (3.1) to (3.4) coincide with the equations of an ideal transformer. In an ideal transformer, the input and output powers are equal, as stated in Eqs. (3.1) and (3.2). Also, the output voltage is equal to the turns ratio times the input voltage. This is consistent with Eq. (3.3), with the turns ratio taken to be the equilibrium conversion ratio $M(D)$. Finally, the input and output currents should be related by the same turns ratio, as in Eq. (3.4).

Thus, we can model the ideal dc-dc converter using the ideal dc transformer model of Fig. 3.3.

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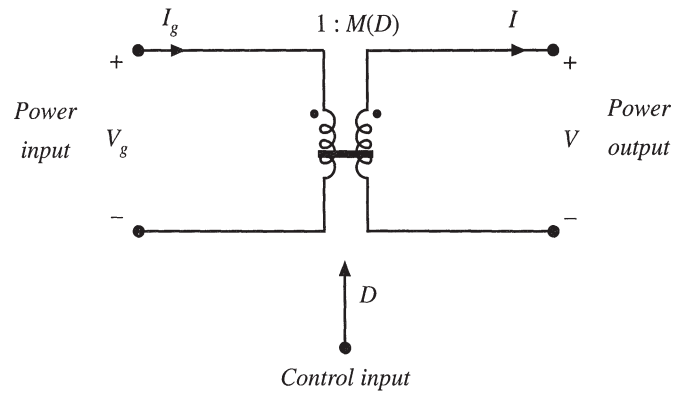


Fig. 3.3 Ideal dc transformer model of a dc-dc converter operating in continuous conduction mode, corresponding to Eqs. (3.1) to (3.4).

This symbol represents the first-order dc properties of any switching dc-dc converter: transformation of dc voltage and current levels, ideally with 100% efficiency, controllable by the duty cycle D. The solid horizontal line indicates that the element is ideal and capable of passing dc voltages and currents. It should be noted that, although standard magnetic-core transformers cannot transform dc signals (they saturate when a dc voltage is applied), we are nonetheless free to define the idealized model of Fig. 3.3 for the purpose of modeling dc-dc converters. Indeed, the absence of a physical dc transformer is one of the reasons for building a dc-dc switching converter. So the properties of the dc-dc converter of Fig. 3.1 can be modeled using the equivalent circuit of Fig. 3.3. An advantage of this equivalent circuit is that, for constant duty cycle, it is time invariant: there is no switching or switching ripple to deal with, and only the important dc components of the waveforms are modeled.

The rules for manipulating and simplifying circuits containing transformers apply equally well to circuits containing dc-dc converters. For example, consider the network of Fig. 3.4(a), in which a resistive load is connected to the converter output, and the power source is modeled by a Thevenin-equivalent voltage source V_1 and resistance R_1. The converter is replaced by the dc transformer model in Fig. 3.4(b). The elements V_1 and R_1 can now be pushed through the dc transformer as in Fig. 3.4(c); the volt-

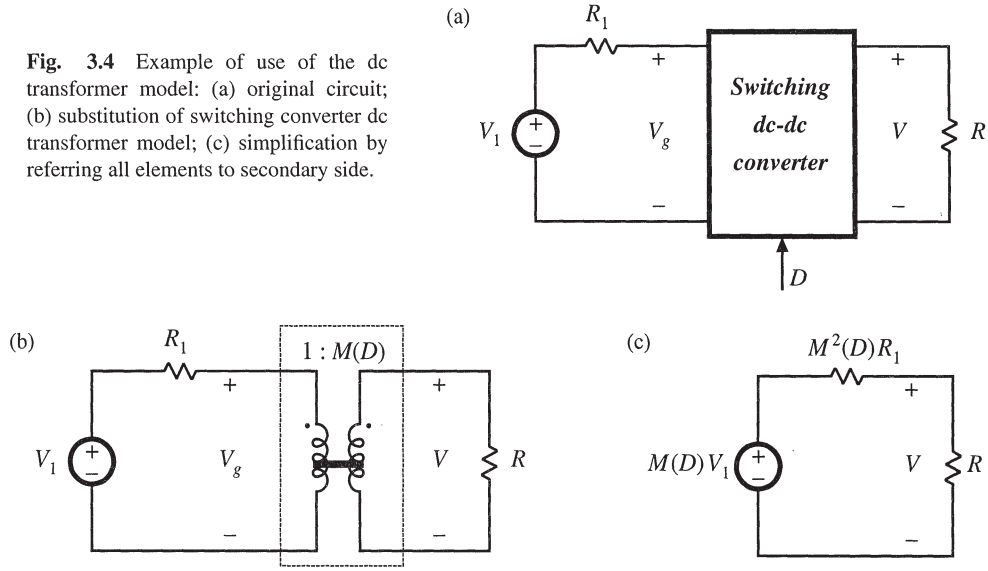


Fig. 3.4 Example of use of the dc transformer model: (a) original circuit; (b) substitution of switching converter dc transformer model; (c) simplification by referring all elements to secondary side.

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age source V_1 is multiplied by the conversion ratio $M(D)$, and the resistor R_1 is multiplied by $M^2(D)$. This circuit can now be solved using the voltage divider formula to find the output voltage:

$$V = M(D)V_1 \frac{R}{R + M^2(D)R_1} \tag{3.5}$$

It should be apparent that the dc transformer/equivalent circuit approach is a powerful tool for understanding networks containing converters.

3.2 INCLUSION OF INDUCTOR COPPER LOSS

The dc transformer model of Fig. 3.3 can be extended, to model other properties of the converter. Nonidealities, such as sources of power loss, can be modeled by adding resistors as appropriate. In later chapters, we will see that converter dynamics can be modeled as well, by adding inductors and capacitors to the equivalent circuit.

Let us consider the inductor copper loss in a boost converter. Practical inductors exhibit power loss of two types: (1) *copper loss*, originating in the resistance of the wire, and (2) *core loss*, due to hysteresis and eddy current losses in the magnetic core. A suitable model that describes the inductor copper loss is given in Fig. 3.5, in which a resistor R_L is placed in series with the inductor. The actual inductor then consists of an ideal inductor, L, in series with the copper loss resistor R_L.

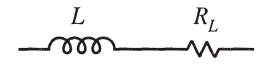


Fig. 3.5 Modeling inductor copper loss via series resistor R_L.

The inductor model of Fig. 3.5 is inserted into the boost converter circuit in Fig. 3.6. The circuit can now be analyzed in the same manner as used for the ideal lossless converter, using the principles of inductor volt-second balance, capacitor charge balance, and the small-ripple approximation. First, we draw the converter circuits during the two subintervals, as in Fig. 3.7.

For $0 < t < DT_s$, the switch is in position 1 and the circuit reduces to Fig. 3.7(a). The inductor voltage $v_L(t)$, across the ideal inductor L, is given by

$$v_L(t) = V_g - i(t)R_L \tag{3.6}$$

and the capacitor current $i_C(t)$ is

$$i_C(t) = -\frac{v(t)}{R} \tag{3.7}$$

Next, we simplify these equations by assuming that the switching ripples in $i(t)$ and $v(t)$ are small compared to their respective dc components I and V. Hence, $i(t) \approx I$ and $v(t) \approx V$, and Eqs. (3.6) and (3.7)

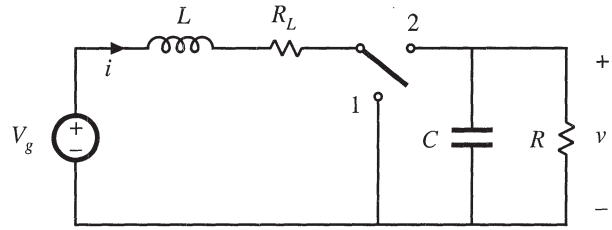


Fig. 3.6 Boost converter circuit, including inductor copper resistance R_L.

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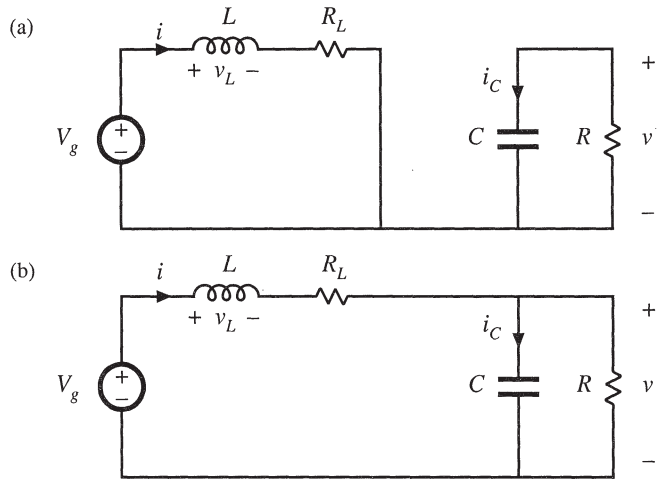


Fig. 3.7 Boost converter circuits during the two subintervals, including inductor copper loss resistance R_L: (a) with the switch in position 1, (b) with the switch in position 2.

become

$$\begin{aligned} v_L(t) &= V_g - IR_L \\ i_C(t) &= -\frac{V}{R} \end{aligned} \tag{3.8}$$

For $DT_s < t < T_s$, the switch is in position 2 and the circuit reduces to Fig. 3.7(b). The inductor current and capacitor voltage are then given by

$$\begin{aligned} v_L(t) &= V_g - i(t)R_L - v(t) \approx V_g - IR_L - V \\ i_C(t) &= i(t) - \frac{v(t)}{R} \approx I - \frac{V}{R} \end{aligned} \tag{3.9}$$

We again make the small-ripple approximation.

The principle of inductor volt-second balance can now be invoked. Equations (3.8) and (3.9) are used to construct the inductor voltage waveform $v_L(t)$ in Fig. 3.8. The dc component, or average value, of the inductor voltage $v_L(t)$ is

$$\langle v_L(t) \rangle = \frac{1}{T_s} \int_0^{T_s} v_L(t)dt = D\left(V_g - IR_L\right) + D'\left(V_g - IR_L - V\right) \tag{3.10}$$

By setting $\langle v_L \rangle$ to zero and collecting terms, one obtains

$$0 = V_g - IR_L - D'V \tag{3.11}$$

(recall that $D + D' = 1$). It can be seen that the inductor winding resistance R_L adds another term to the inductor volt-second balance equation. In the ideal boost converter ($R_L = 0$) example of Chapter 2, we were able to solve this equation directly for the voltage conversion ratio V/V_g. Equation (3.11) cannot be immediately solved in this manner, because the inductor current I is unknown. A second equation is needed, to eliminate I.

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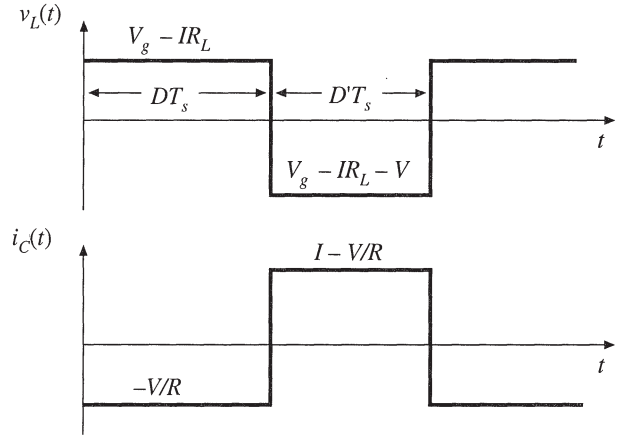


Fig. 3.8 Inductor voltage and capacitor current waveforms, for the nonideal boost converter of Fig. 3.6.

The second equation is obtained using capacitor charge balance. The capacitor current $i_C(t)$ waveform is given in Fig. 3.8. The dc component, or average value, of the capacitor current waveform is

$$\langle i_C(t) \rangle = D\left(-\frac{V}{R}\right) + D'\left(I - \frac{V}{R}\right) \tag{3.12}$$

By setting $\langle i_C \rangle$ to zero and collecting terms, one obtains

$$0 = D'I - \frac{V}{R} \tag{3.13}$$

We now have two equations, Eqs. (3.11) and (3.13), and two unknowns, V and I. Elimination of I and solution for V yields

$$\frac{V}{V_g} = \frac{1}{D'} \frac{1}{\left(1 + \frac{R_L}{D'^2 R}\right)} \tag{3.14}$$

This is the desired solution for the converter output voltage V. It is plotted in Fig. 3.9 for several values of R_L/R. It can be seen that Eq. (3.14) contains two terms. The first, $1/D'$, is the ideal conversion ratio, with $R_L = 0$. The second term, $1/(1 + R_L/D'^2R)$, describes the effect of the inductor winding resistance. If R_L is much less than D'^2R, then the second term is approximately equal to unity and the conversion ratio is approximately equal to the ideal value $1/D'$. However, as R_L is increased in relation to D'^2R, then the second term is reduced in value, and V/V_g is reduced as well.

As the duty cycle D approaches one, the inductor winding resistance R_L causes a major qualitative change in the V/V_g curve. Rather than approaching infinity at $D = 1$, the curve tends to zero. Of course, it is unreasonable to expect that the converter can produce infinite voltage, and it should be comforting to the engineer that the prediction of the model is now more realistic. What happens at $D = 1$ is that the switch is always in position 1. The inductor is never connected to the output, so no energy is transferred to the output and the output voltage tends to zero. The inductor current tends to a large value, limited only by the inductor resistance R_L. A large amount of power is lost in the inductor winding resistance, equal to V_g^2/R_L, while no power is delivered to the load; hence, we can expect that the converter efficiency tends to zero at $D = 1$.

Another implication of Fig. 3.9 is that the inductor winding resistance R_L limits the maximum

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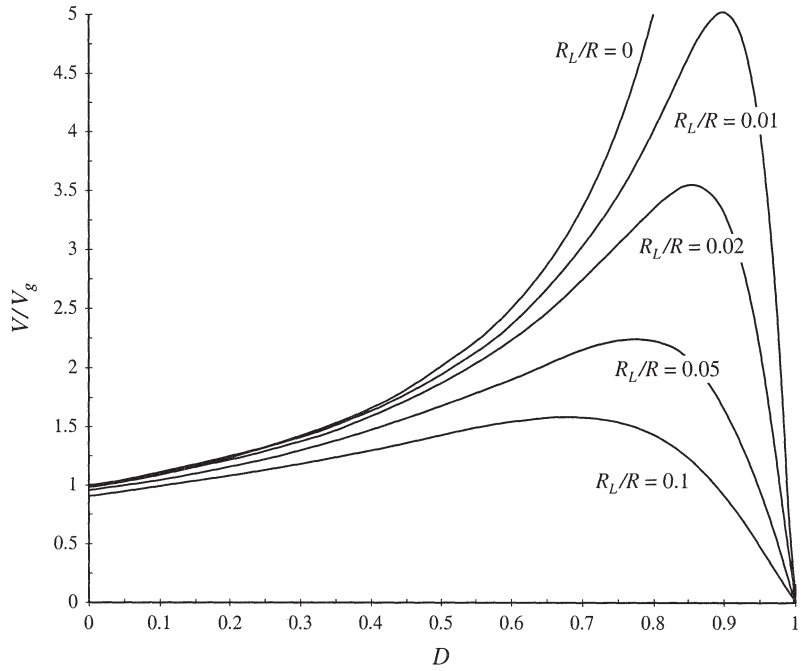


Fig. 3.9 Output voltage vs. duty cycle, boost converter with inductor copper loss.

voltage that the converter can produce. For example, with $R_L/R = 0.02$, it can be seen that the maximum V/V_g is approximately 3.5. If it is desired to obtain $V/V_g = 5$, then according to Fig. 3.9 the inductor winding resistance R_L must be reduced to less than 1% of the load resistance R. The only problem is that decreasing the inductor winding resistance requires building a larger, heavier, more expensive inductor. So it is usually important to optimize the design, by correctly modeling the effects of loss elements such as R_L, and choosing the smallest inductor that will do the job. We now have the analytical tools needed to do this.

3.3 CONSTRUCTION OF EQUIVALENT CIRCUIT MODEL

Next, let us refine the dc transformer model, to account for converter losses. This will allow us to determine the converter voltages, currents, and efficiency using well-known techniques of circuit analysis.

In the previous section, we used the principles of inductor volt-second balance and capacitor charge balance to write Eqs. (3.11) and (3.13), repeated here:

$$\begin{aligned} \langle v_L \rangle &= 0 = V_g - IR_L - D'V \\ \langle i_C \rangle &= 0 = D'I - \frac{V}{R} \end{aligned} \tag{3.15}$$

These equations state that the dc components of the inductor voltage and capacitor current are equal to zero. Rather than algebraically solving the equations as in the previous section, we can reconstruct a circuit model based on these equations, which describes the dc behavior of the boost converter with inductor copper loss. This is done by constructing a circuit whose Kirchoff loop and node equations are

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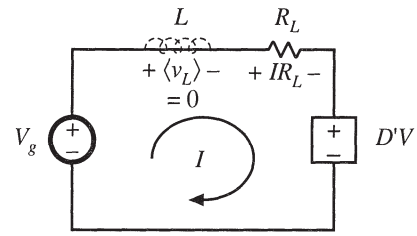


Fig. 3.10 Circuit whose loop equation is identical to Eq. (3.16), obtained by equating the average inductor voltage $\langle v_L \rangle$ to zero.

identical to Eqs. (3.15).

3.3.1 Inductor Voltage Equation

$$\langle v_L \rangle = 0 = V_g - IR_L - D'V \tag{3.16}$$

This equation was derived by use of Kirchoff's voltage law to find the inductor voltage during each subinterval. The results were averaged and set to zero. Equation (3.16) states that the sum of three terms having the dimensions of voltage are equal to $\langle v_L \rangle$, or zero. Hence, Eq. (3.16) is of the same form as a loop equation; in particular, it describes the dc components of the voltages around a loop containing the inductor, with loop current equal to the dc inductor current I.

So let us construct a circuit containing a loop with current I, corresponding to Eq. (3.16). The first term in Eq. (3.16) is the dc input voltage V_g, so we should include a voltage source of value V_g as shown in Fig. 3.10. The second term is a voltage drop of value IR_L, which is proportional to the current I in the loop. This term corresponds to a resistance of value R_L. The third term is a voltage $D'V$, dependent on the converter output voltage. For now, we can model this term using a dependent voltage source, with polarity chosen to satisfy Eq. (3.16).

3.3.2 Capacitor Current Equation

$$\langle i_C \rangle = 0 = D'I - \frac{V}{R} \tag{3.17}$$

This equation was derived using Kirchoff's current law to find the capacitor current during each subinterval. The results were averaged, and the average capacitor current was set to zero.

Equation (3.17) states that the sum of two dc currents are equal to $\langle i_C \rangle$, or zero. Hence, Eq. (3.17) is of the same form as a node equation; in particular, it describes the dc components of currents

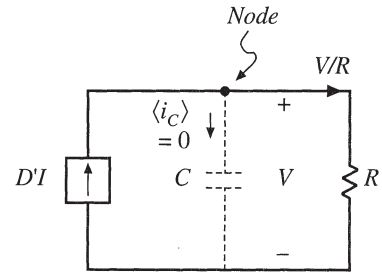


Fig. 3.11 Circuit whose node equation is identical to Eq. (3.17), obtained by equating the average capacitor current $\langle i_C \rangle$ to zero.

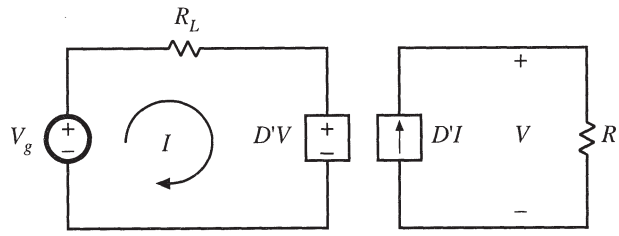


Fig. 3.12 The circuits of Figs. 3.10 and 3.11, drawn together.

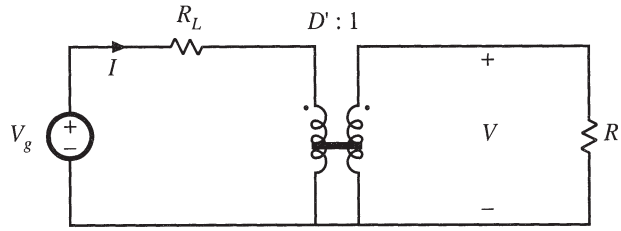


Fig. 3.13 Equivalent circuit model of the boost converter, including a D':1 dc transformer and the inductor winding resistance R_L.

flowing into a node connected to the capacitor. The dc capacitor voltage is V.

So now let us construct a circuit containing a node connected to the capacitor, as in Fig. 3.11, whose node equation satisfies Eq. (3.17). The second term in Eq. (3.17) is a current of magnitude V/R, proportional to the dc capacitor voltage V. This term corresponds to a resistor of value R, connected in parallel with the capacitor so that its voltage is V and hence its current is V/R. The first term is a current $D'I$, dependent on the dc inductor current I. For now, we can model this term using a dependent current source as shown. The polarity of the source is chosen to satisfy Eq. (3.17).

3.3.3 Complete Circuit Model

The next step is to combine the circuits of Figs. 3.10 and 3.11 into a single circuit, as in Fig. 3.12. This circuit can be further simplified by recognizing that the dependent voltage and current sources constitute an ideal dc transformer, as discussed in Section 3.1. The $D'V$ dependent voltage source depends on V, the voltage across the dependent current source. Likewise, the $D'I$ dependent current source depends on I, the current flowing through the dependent voltage source. In each case, the coefficient is D'. Hence, the dependent sources form a circuit similar to Fig. 3.2; the fact that the voltage source appears on the primary rather than the secondary side is irrelevant, owing to the symmetry of the transformer. They are therefore equivalent to the dc transformer model of Fig. 3.3, with turns ratio D':1. Substitution of the ideal dc transformer model for the dependent sources yields the equivalent circuit of Fig. 3.13.

The equivalent circuit model can now be manipulated and solved to find the converter voltages and currents. For example, we can eliminate the transformer by referring the V_g voltage source and R_L resistance to the secondary side. As shown in Fig. 3.14, the voltage source value is divided by the effective turns ratio D', and the resistance R_L is divided by the square of the turns ratio, D'^2. This circuit can be solved directly for the output voltage V, using the voltage divider formula:

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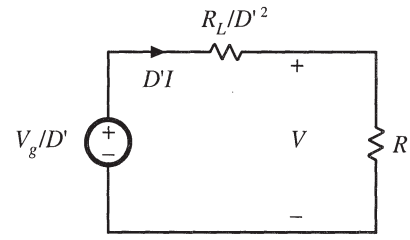


Fig. 3.14 Simplification of the equivalent circuit of Fig. 3.13, by referring all elements to the secondary side of the transformer.

$$V = \frac{V_g}{D'} \frac{R}{R + \frac{R_L}{D'^2}} = \frac{V_g}{D'} \frac{1}{1 + \frac{R_L}{D'^2 R}} \tag{3.18}$$

This result is identical to Eq. (3.14). The circuit can also be solved directly for the inductor current I, by referring all elements to the transformer primary side. The result is:

$$I = \frac{V_g}{D'^2 R + R_L} = \frac{V_g}{D'^2 R} \frac{1}{1 + \frac{R_L}{D'^2 R}} \tag{3.19}$$

3.3.4 Efficiency

The equivalent circuit model also allows us to compute the converter efficiency η. Figure 3.13 predicts that the converter input power is

$$P_{in} = (V_g)\,(I) \tag{3.20}$$

The load current is equal to the current in the secondary of the ideal dc transformer, or $D'I$. Hence, the model predicts that the converter output power is

$$P_{out} = (V)\,(D'I) \tag{3.21}$$

Therefore, the converter efficiency is

$$\eta = \frac{P_{out}}{P_{in}} = \frac{(V)\,(D'I)}{(V_g)\,(I)} = \frac{V}{V_g} D' \tag{3.22}$$

Substitution of Eq. (3.18) into Eq. (3.22) to eliminate V yields

$$\eta = \frac{1}{1 + \frac{R_L}{D'^2 R}} \tag{3.23}$$

This equation is plotted in Fig. 3.15, for several values of R_L/R. It can be seen from Eq. (3.23) that, to obtain high efficiency, the inductor winding resistance R_L should be much smaller that D'^2R, the load resistance referred to the primary side of the ideal dc transformer. This is easier to do at low duty cycle, where D' is close to unity, than at high duty cycle where D' approaches zero. It can be seen from Fig.

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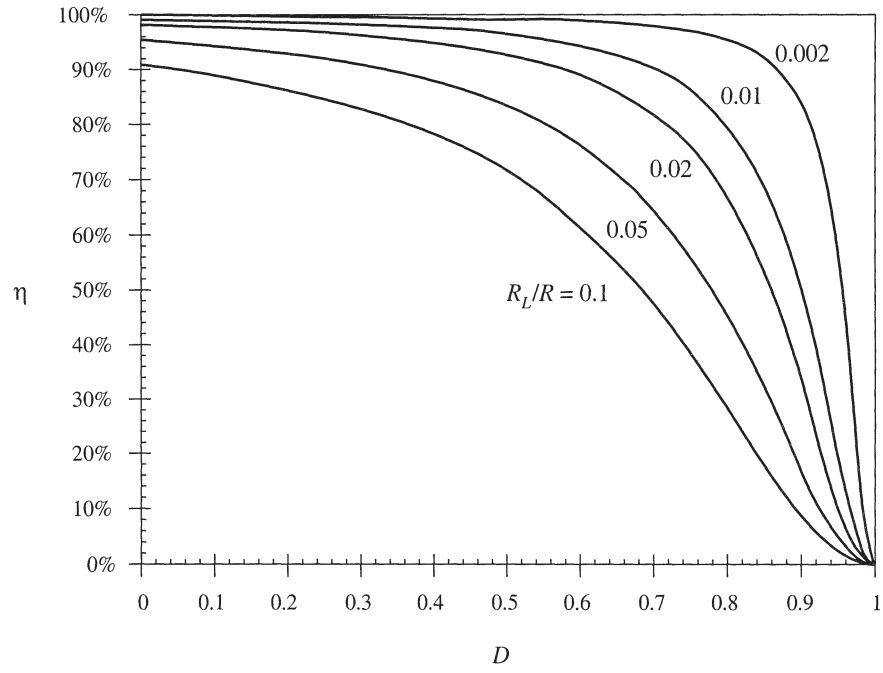


Fig. 3.15 Efficiency vs. duty cycle, boost converter with inductor copper loss.

3.15 that the efficiency is typically high at low duty cycles, but decreases rapidly to zero near $D = 1$.

Thus, the basic dc transformer model can be refined to include other effects, such as the inductor copper loss. The model describes the basic properties of the converter, including (a) transformation of dc voltage and current levels, (b) second-order effects such as power losses, and (c) the conversion ratio M. The model can be solved to find not only the output voltage V, but also the inductor current I and the efficiency η. All of the well-known techniques of circuit analysis can be employed to solve the model, making this a powerful and versatile approach.

The example considered so far is a relatively simple one, in which there is only a single loss element, R_L. Of course, real converters are considerably more complicated, and contain a large number of loss elements. When solving a complicated circuit to find the output voltage and efficiency, it behooves the engineer to use the simplest and most physically meaningful method possible. Writing a large number of simultaneous loop or node equations is not the best approach, because its solution typically requires several pages of algebra, and the engineer usually makes algebra mistakes along the way. The practicing engineer often gives up before finding the correct solution. The equivalent circuit approach avoids this situation, because one can simplify the circuit via well-known circuit manipulations such as pushing the circuit elements to the secondary side of the transformer. Often the answer can then be written by inspection, using the voltage divider rule or other formulas. The engineer develops confidence that the result is correct, and does not contain algebra mistakes.

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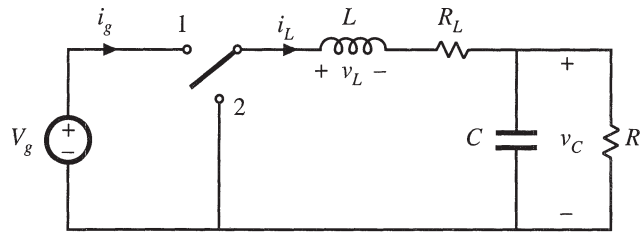


Fig. 3.16 Buck converter example.

3.4 HOW TO OBTAIN THE INPUT PORT OF THE MODEL

Let's try to derive the model of the buck converter of Fig. 3.16, using the procedure of Section 3.3. The inductor winding resistance is again modeled by a series resistor R_L.

The average inductor voltage can be shown to be

$$\langle v_L \rangle = 0 = DV_g - I_L R_L - V_C \tag{3.24}$$

This equation describes a loop with the dc inductor current I_L. The dc components of the voltages around this loop are: (*i*) the DV_g term, modeled as a dependent voltage source, (*ii*) a voltage drop $I_L R_L$, modeled as resistor R_L, and (*iii*) the dc output voltage V_C.

The average capacitor current is

$$\langle i_C \rangle = 0 = I_L - \frac{V_C}{R} \tag{3.25}$$

This equation describes the dc currents flowing into the node connected to the capacitor. The dc component of inductor current, I_L, flows into this node. The dc load current V_C/R (i.e., the current flowing through the load resistor R) flows out of this node. An equivalent circuit that models Eqs. (3.24) and (3.25) is given in Fig. 3.17. This circuit can be solved to determine the dc output voltage V_C.

What happened to the dc transformer in Fig. 3.17? We expect the buck converter model to contain a dc transformer, with turns ratio equal to the dc conversion ratio, or 1:D. According to Fig. 3.2, the secondary of this transformer is equivalent to a dependent voltage source, of value DV_g. Such a source does indeed appear in Fig. 3.17. But where is the primary? From Fig. 3.2, we expect the primary of the dc transformer to be equivalent to a dependent current source. In general, to derive this source, it is necessary to find the dc component of the converter input current $i_g(t)$.

The converter input current waveform $i_g(t)$ is sketched in Fig. 3.18. When the switch is in position 1, $i_g(t)$ is equal to the inductor current. Neglecting the inductor current ripple, we have $i_g(t) \approx I_L$. When the switch is in position 2, $i_g(t)$ is zero. The dc component, or average value, of $i_g(t)$ is

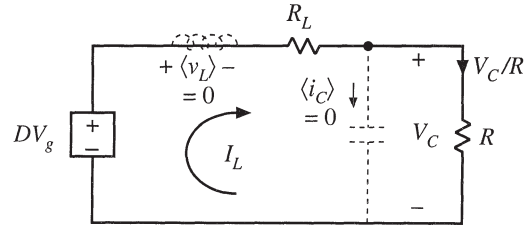


Fig. 3.17 Equivalent circuit derived from Eqs. (3.24) and (3.25).

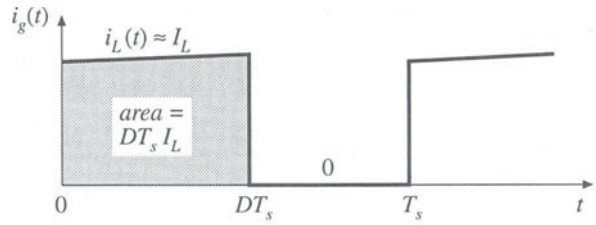


Fig. 3.18 Converter input current waveform $i_g(t)$.

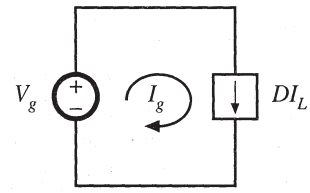


Fig. 3.19 Converter input port dc equivalent circuit.

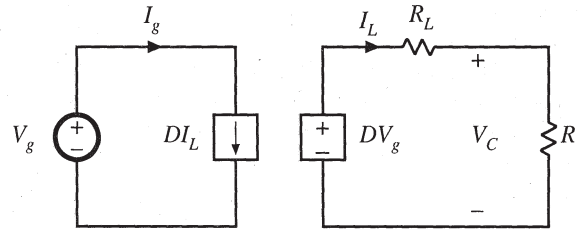


Fig. 3.20 The circuits of Figs. 3.17 and 3.19, drawn together.

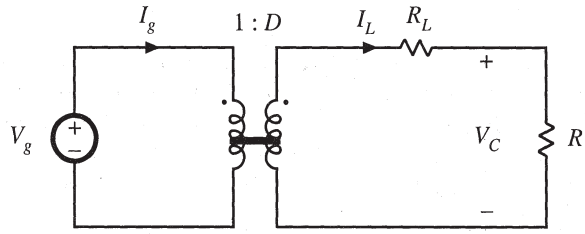


Fig. 3.21 Equivalent circuit of the buck converter, including a 1:D dc transformer and the inductor winding resistance R_L.

$$I_g = \frac{1}{T_s}\int_0^{T_s} i_g(t)\,dt = DI_L \tag{3.26}$$

The integral of $i_g(t)$ is equal to the area under the $i_g(t)$ curve, or DT_sI_L according to Fig. 3.18. The dc component I_g is therefore $(DT_sI_L)/T_s = DI_L$. Equation (3.26) states that I_g, the dc component of current drawn by the converter out of the V_g source, is equal to DI_L. An equivalent circuit is given in Fig. 3.19.

A complete model for the buck converter can now be obtained by combining Figs. 3.17 and 3.19 to obtain Fig. 3.20. The dependent current and voltage sources can be combined into a dc transformer, since the DV_g dependent voltage source has value D times the voltage V_g across the dependent current source, and the current source is the same constant D times the current I_L through the dependent voltage source. So, according to Fig. 3.2, the sources are equivalent to a dc transformer with turns ratio 1:D, as shown in Fig. 3.21.

In general, to obtain a complete dc equivalent circuit that models the converter input port, it is necessary to write an equation for the dc component of the converter input current. An equivalent circuit

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corresponding to this equation is then constructed. In the case of the buck converter, as well as in other converters having pulsating input currents, this equivalent circuit contains a dependent current source which becomes the primary of a dc transformer model. In the boost converter example of Section 3.3, it was unnecessary to explicitly write this equation, because the input current $i_g(t)$ coincided with the inductor current $i(t)$, and hence a complete equivalent circuit could be derived using only the inductor voltage and capacitor current equations.

3.5 EXAMPLE: INCLUSION OF SEMICONDUCTOR CONDUCTION LOSSES IN THE BOOST CONVERTER MODEL

As a final example, let us consider modeling semiconductor conduction losses in the boost converter of Fig. 3.22. Another major source of power loss is the conduction loss due to semiconductor device forward voltage drops. The forward voltage of a metal oxide semiconductor field-effect transistor (MOSFET) or bipolar junction transistor (BJT) can be modeled with reasonable accuracy as an on-resistance R_{on}. In the case of a diode, insulated-gate bipolar transistor (IGBT), or thyristor, a voltage source plus an on-resistance yields a model of good accuracy; the on-resistance may be omitted if the converter is being modeled at a single operating point.

When the gate drive signal is high, the MOSFET turns on and the diode is reverse-biased. The circuit then reduces to Fig. 3.23(a). In the conducting state, the MOSFET is modeled by the on-resistance R_{on}. The inductor winding resistance is again represented as in Fig. 3.5. The inductor voltage and capacitor current are given by

$$\begin{aligned} v_L(t) &= V_g - iR_L - iR_{on} \approx V_g - IR_L - IR_{on} \\ i_C(t) &= -\frac{v}{R} \approx -\frac{V}{R} \end{aligned} \tag{3.27}$$

The inductor current and capacitor voltage have again been approximated by their dc components.

When the gate drive signal is low, the MOSFET turns off. The diode becomes forward-biased by the inductor current, and the circuit reduces to Fig. 3.23(b). In the conducting state, the diode is modeled in this example by voltage source V_D and resistance R_D. The inductor winding resistance is again modeled by resistance R_L. The inductor voltage and capacitor current for this subinterval are

$$\begin{aligned} v_L(t) &= V_g - iR_L - V_D - iR_D - v \approx V_g - IR_L - V_D - IR_D - V \\ i_C(t) &= i - \frac{v}{R} \approx I - \frac{V}{R} \end{aligned} \tag{3.28}$$

The inductor voltage and capacitor current waveforms are sketched in Fig. 3.24.

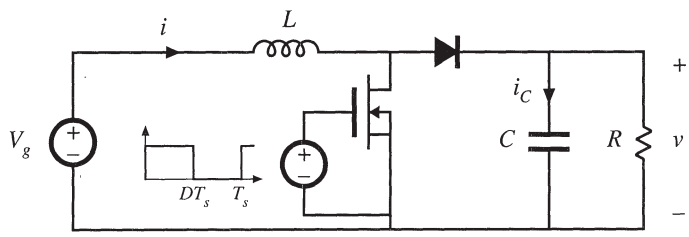


Fig. 3.22 Boost converter example.

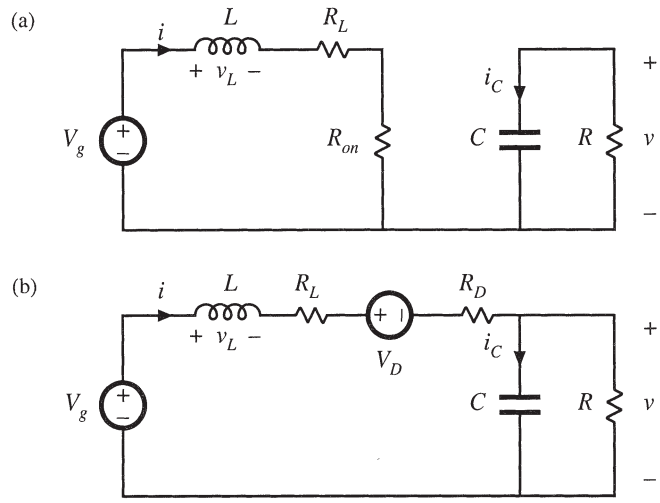


Fig. 3.23 Boost converter circuits: (a) when MOSFET conducts, (b) when diode conducts.

The dc component of the inductor voltage is given by

$$\langle v_L \rangle = D\left(V_g - IR_L - IR_{on}\right) + D'\left(V_g - IR_L - V_D - IR_D - V\right) = 0 \tag{3.29}$$

By collecting terms and noting that $D + D' = 1$, one obtains

$$V_g - IR_L - IDR_{on} - D'V_D - ID'R_D - D'V = 0 \tag{3.30}$$

This equation describes the dc components of the voltages around a loop containing the inductor, with loop current equal to the dc inductor current I. An equivalent circuit is given in Fig. 3.25.

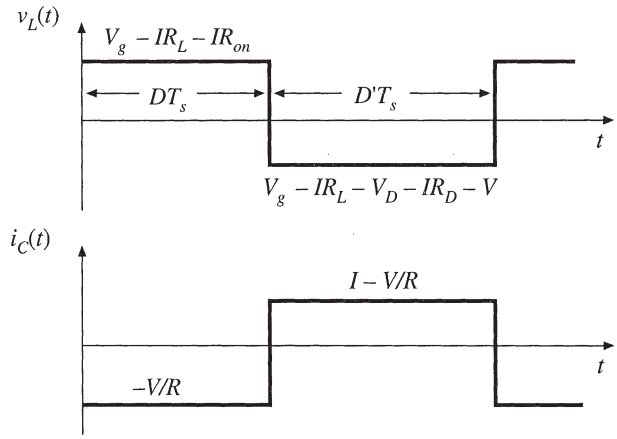


Fig. 3.24 Inductor voltage $v_L(t)$ and capacitor current $i_C(t)$ waveforms, for the converter of Fig. 3.22.

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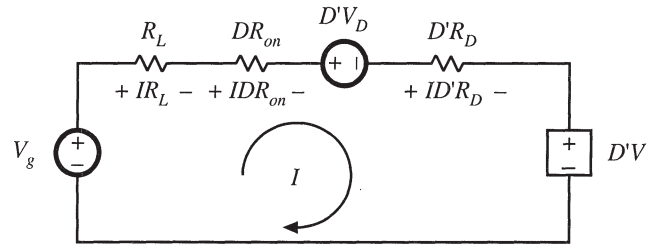


Fig. 3.25 Equivalent circuit corresponding to Eq. (3.30).

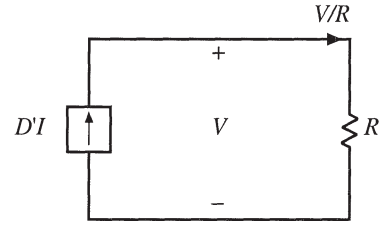


Fig. 3.26 Equivalent circuit corresponding to Eq. (3.32).

The dc component of the capacitor current is

$$\langle i_C \rangle = D\left(-\frac{V}{R}\right) + D'\left(I - \frac{V}{R}\right) = 0 \tag{3.31}$$

Upon collecting terms, one obtains

$$D'I - \frac{V}{R} = 0 \tag{3.32}$$

This equation describes the dc components of the currents flowing into a node connected to the capacitor, with dc capacitor voltage equal to V. An equivalent circuit is given in Fig. 3.26.

The two circuits are drawn together in 3.27. The dependent sources are combined into an ideal D':1 transformer in Fig. 3.28, yielding the complete dc equivalent circuit model.

Solution of Fig. 3.28 for the output voltage V yields

$$V = \left(\frac{1}{D'}\right)\left(V_g - D'V_D\right)\left(\frac{D'^2R}{D'^2R + R_L + DR_{on} + D'R_D}\right) \tag{3.33}$$

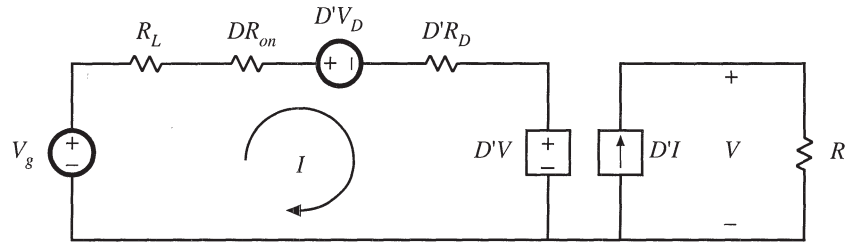


Fig. 3.27 The circuits of Figs. 3.25 and 3.26, drawn together.

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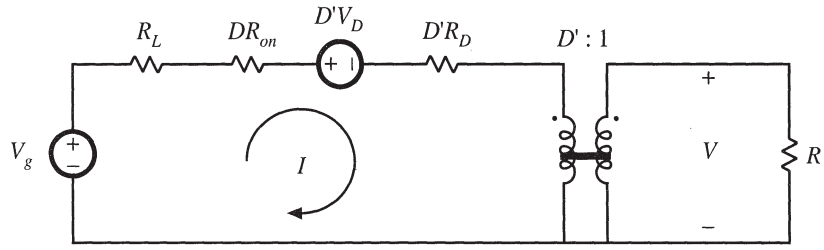


Fig. 3.28 Equivalent circuit model of the boost converter of Fig. 3.22, including ideal dc transformer, inductor winding resistance, and MOSFET and diode conduction losses.

Dividing by V_g gives the voltage conversion ratio:

$$\frac{V}{V_g} = \left(\frac{1}{D'}\right)\left(1 - \frac{D'V_D}{V_g}\right)\left(\frac{1}{1 + \dfrac{R_L + DR_{on} + D'R_D}{D'^2R}}\right) \tag{3.34}$$

It can be seen that the effect of the loss elements V_D, R_L, R_{on}, and R_D is to decrease the voltage conversion ratio below the ideal value ($1/D'$).

The efficiency is given by $\eta = P_{out}/P_{in}$. From Fig. 3.28, $P_{in} = V_g I$ and $P_{out} = VD'I$. Hence,

$$\eta = D'\frac{V}{V_g} = \frac{\left(1 - \dfrac{D'V_D}{V_g}\right)}{\left(1 + \dfrac{R_L + DR_{on} + D'R_D}{D'^2R}\right)} \tag{3.35}$$

For high efficiency, we require

$$\begin{aligned} V_g/D' &\gg V_D \\ D'^2R &\gg R_L + DR_{on} + D'R_D \end{aligned} \tag{3.36}$$

It may seem strange that the equivalent circuit model of Fig. 3.28 contains effective resistances DR_{on} and $D'R_D$, whose values vary with duty cycle. The reason for this dependence is that the semiconductor on-resistances are connected in the circuit only when their respective semiconductor devices conduct. For example, at $D = 0$, the MOSFET never conducts, and the effective resistance DR_{on} disappears from the model. These effective resistances correctly model the average power losses in the elements. For instance, the equivalent circuit predicts that the power loss in the MOSFET on-resistance is I^2DR_{on}. In the actual circuit, the MOSFET conduction loss is I^2R_{on} while the MOSFET conducts, and zero while the MOSFET is off. Since the MOSFET conducts with duty cycle D, the average conduction loss is DI^2R_{on}, which coincides with the prediction of the model.

In general, to predict the power loss in a resistor R, we must calculate the root-mean-square current I_{rms} through the resistor, rather than the average current. The average power loss is then given by $I_{rms}{}^2R$. Nonetheless, the average model of Fig. 3.28 correctly predicts average power loss, provided that the inductor current ripple is small. For example, consider the MOSFET conduction loss in the buck converter. The actual transistor current waveform is sketched in Fig. 3.29, for several values of inductor current ripple Δi. Case (a) corresponds to use of an infinite inductance L, leading to zero inductor current ripple. As shown in Table 3.1, the MOSFET conduction loss is then given by $I_{rms}{}^2R_{on} = DI^2R_{on}$, which

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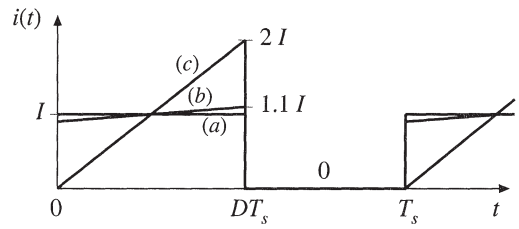


Fig. 3.29 Transistor current waveform, for various filter inductor values: (a) with a very large inductor, such that $\Delta i \approx 0$; (b) with a typical inductor value, such that $\Delta i = 0.1I$; (c) with a small inductor value, chosen such that $\Delta i = I$.

agrees exactly with the prediction of the average model. Case (b) is a typical choice of inductance L, leading to an inductor current ripple of $\Delta i = 0.1I$. The exact MOSFET conduction loss, calculated using the rms value of MOSFET current, is then only 0.33% greater than the prediction of the average model. In the extreme case (c) where $\Delta i = I$, the actual conduction loss is 33% greater than that predicted by the average model. Thus, the dc (average) model correctly predicts losses in the component nonidealities, even though rms currents are not calculated. The model is accurate provided that the inductor current ripple is small.

Table 3.1 Effect of inductor current ripple on MOSFET conduction loss

Inductor current ripple	MOSFET rms current	Average power loss in R_{on}
(a) $\Delta i = 0$	$I\sqrt{D}$	DI^2R_{on}
(b) $\Delta i = 0.1i$	$(1.00167)I\sqrt{D}$	$(1.0033)DI^2R_{on}$
(c) $\Delta i = I$	$(1.155)I\sqrt{D}$	$(1.3333)DI^2R_{on}$

3.6 SUMMARY OF KEY POINTS

1. The dc transformer model represents the primary functions of any dc-dc converter: transformation of dc voltage and current levels, ideally with 100% efficiency, and control of the conversion ratio M via the duty cycle D. This model can be easily manipulated and solved using familiar techniques of conventional circuit analysis.
2. The model can be refined to account for loss elements such as inductor winding resistance and semiconductor on-resistances and forward voltage drops. The refined model predicts the voltages, currents, and efficiency of practical nonideal converters.
3. In general, the dc equivalent circuit for a converter can be derived from the inductor volt-second balance and capacitor charge balance equations. Equivalent circuits are constructed whose loop and node equations coincide with the volt-second and charge balance equations. In converters having a pulsating input current, an additional equation is needed to model the converter input port; this equation may be obtained by averaging the converter input current.

REFERENCES

[1] R. D. MIDDLEBROOK, "A Continuous Model for the Tapped-Inductor Boost Converter," *IEEE Power Electronics Specialists Conference*, 1975 Record, pp. 63-79, June 1975.

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[2] S. M. ĆUK, "Modeling, Analysis, and Design of Switching Converters," Ph.D. thesis, California Institute of Technology, November 1976.

[3] G. WESTER and R. D. MIDDLEBROOK, "Low-Frequency Characterization of Switched Dc–Dc Converters," *IEEE Transactions on Aerospace and Electronic Systems*, Vol. AES-9, pp. 376–385, May 1973.

[4] R. D. MIDDLEBROOK and S. M. ĆUK, "Modeling and Analysis Methods for Dc-to-Dc Switching Converters," *IEEE International Semiconductor Power Converter Conference*, 1977 Record, pp. 90-111.

PROBLEMS

3.1 In the buck-boost converter of Fig. 3.30, the inductor has winding resistance R_L. All other losses can be ignored.

(a) Derive an expression for the nonideal voltage conversion ratio V/V_g.

(b) Plot your result of part (a) over the range $0 \le D \le 1$, for $R_L/R = 0$, 0.01, and 0.05.

(c) Derive an expression for the efficiency. Manipulate your expression into a form similar to Eq. (3.35)

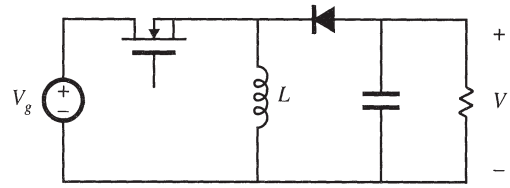


Fig. 3.30 Nonideal buck–boost converter, Problems 3.1 and 3.2.

3.2 The inductor in the buck-boost converter of Fig. 3.30 has winding resistance R_L. All other losses can be ignored. Derive an equivalent circuit model for this converter. Your model should explicitly show the input port of the converter, and should contain two dc transformers.

3.3 In the converter of Fig. 3.31, the inductor has winding resistance R_L. All other losses can be ignored. The switches operate synchronously: each is in position 1 for $0 < t < DT_s$, and in position 2 for $DT_s < t < T_s$.

(a) Derive an expression for the nonideal voltage conversion ratio V/V_g.

(b) Plot your result of part (a) over the range $0 \le D \le 1$, for $R_L/R = 0$, 0.01, and 0.05.

(c) Derive an expression for the efficiency. Manipulate your expression into a form similar to Eq. (3.35)

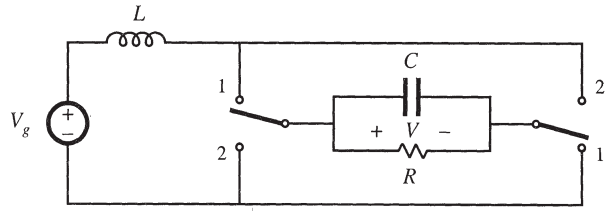


Fig. 3.31 Nonideal current-fed bridge converter, Problems 3.3 and 3.4.

3.4 The inductor in the converter of Fig. 3.31 has winding resistance R_L. All other losses can be ignored. Derive an equivalent circuit model for this converter.

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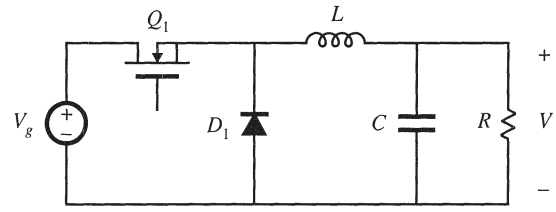


Fig. 3.32 Nonideal buck converter, Problem 3.5.

3.5 In the buck converter of Fig. 3.32, the MOSFET has on-resistance R_{on} and the diode forward voltage drop can be modeled by a constant voltage source V_D. All other losses can be neglected.

(a) Derive a complete equivalent circuit model for this converter.

(b) Solve your model to find the output voltage V.

(c) Derive an expression for the efficiency. Manipulate your expression into a form similar to Eq. (3.35).

3.6 To reduce the switching harmonics present in the input current of a certain buck converter, an input filter is added as shown in Fig. 3.33. Inductors L_1 and L_2 contain winding resistances R_{L1} and R_{L2}, respectively. The MOSFET has on-resistance R_{on}, and the diode forward voltage drop can be modeled by a constant voltage V_D plus a resistor R_D. All other losses can be ignored.

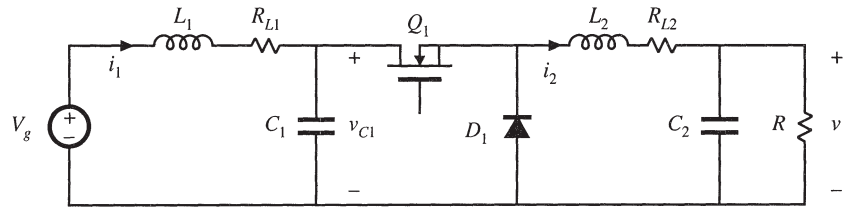


Fig. 3.33 Buck converter with input filter, Problem 3.6.

(a) Derive a complete equivalent circuit model for this circuit.

(b) Solve your model to find the dc output voltage V.

(c) Derive an expression for the efficiency. Manipulate your expression into a form similar to Eq. (3.35).

3.7 A 1.5 V battery is to be used to power a 5 V, 1 A load. It has been decided to use a buck-boost converter in this application. A suitable transistor is found with an on-resistance of 35 mΩ, and a Schottky diode is found with a forward drop of 0.5 V. The on-resistance of the Schottky diode may be ignored. The power stage schematic is shown in Fig. 3.34.

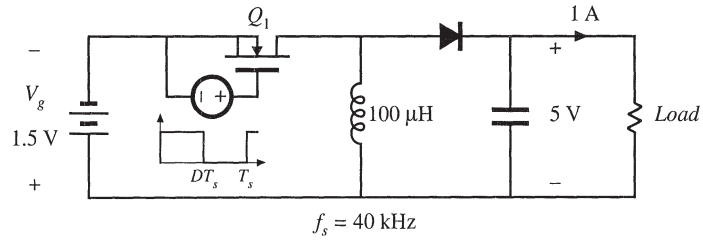


Fig. 3.34 Nonideal buck-boost converter powering a 5 V load from a 1.5 V battery, Problem 3.7

(a) Derive an equivalent circuit that models the dc properties of this converter. Include the transistor and diode conduction losses, as well as the inductor copper loss, but ignore all other sources of loss. Your model should correctly describe the converter dc input port.

(b) It is desired that the converter operate with at least 70% efficiency under nominal conditions (i.e., when the input voltage is 1.5 V and the output is 5 V at 1 A). How large can the inductor winding resistance be? At what duty cycle will the converter then operate? *Note*: there is an easy way and a not-so-easy way to analytically solve this part.

(c) For your design of part (b), compute the power loss in each element.

(d) Plot the converter output voltage and efficiency over the range $0 \leq D \leq 1$, using the value of inductor winding resistance which you selected in part (b).

(e) Discuss your plot of part (d). Does it behave as you expect? Explain.

For Problems 3.8 and 3.9, a transistor having an on-resistance of 0.5 Ω is used. To simplify the problems, you may neglect all losses other than the transistor conduction loss. You may also neglect the dependence of MOSFET on-resistance on rated blocking voltage. These simplifying assumptions reduce the differences between converters, but do not change the conclusions regarding which converter performs best in the given situations.

3.8 It is desired to interface a 500 V dc source to a 400 V, 10 A load using a dc-dc converter. Two possible approaches, using buck and buck-boost converters, are illustrated in Fig. 3.35. Use the assumptions described above to:

(a) Derive equivalent circuit models for both converters, which model the converter input and output ports as well as the transistor conduction loss.

(b) Determine the duty cycles that cause the converters to operate with the specified conditions.

(c) Compare the transistor conduction losses and efficiencies of the two approaches, and conclude which converter is better suited to the specified application.

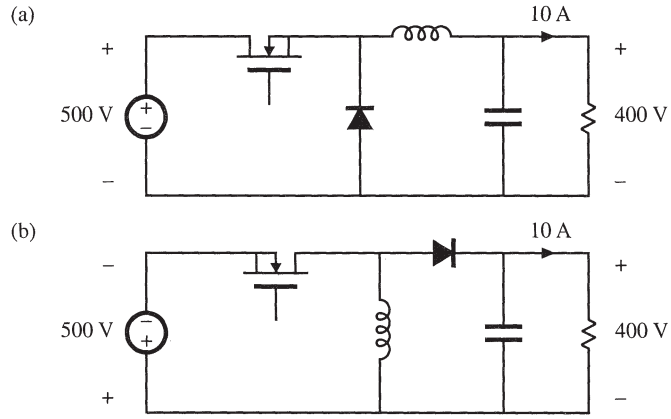


Fig. 3.35 Problem 3.8: interfacing a 500 V source to a 400 V load, using (a) a buck converter, (b) a buck-boost converter.

3.9 It is desired to interface a 300 V battery to a 400 V, 10 A load using a dc-dc converter. Two possible approaches, using boost and buck-boost converters, are illustrated in Fig. 3.36. Using the assumptions described above (before Problem 3.8), determine the efficiency and power loss of each approach. Which converter is better for this application?

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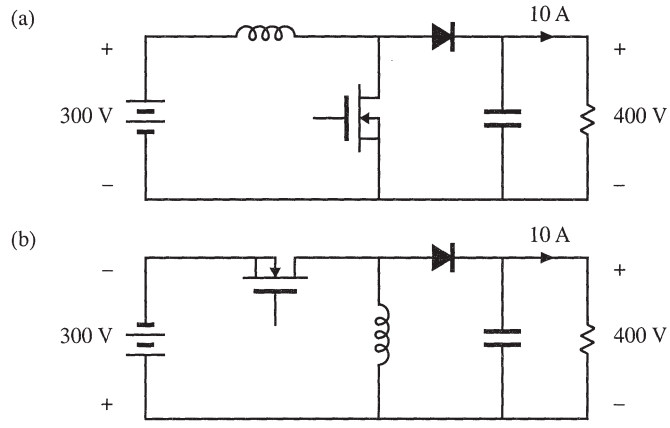


Fig. 3.36 Problem 3.9: interfacing a 300 V battery to a 400 V load, using: (a) a boost converter, (b) a buck–boost converter.

3.10 A buck converter is operated from the rectified 230 V ac mains, such that the converter dc input voltage is

$$V_g = 325 \text{ V} \pm 20\%$$

A control circuit automatically adjusts the converter duty cycle D, to maintain a constant dc output voltage of $V = 240$ V dc. The dc load current I can vary over a 10:1 range:

$$10 \text{ A} \leq I \leq 1 \text{ A}$$

The MOSFET has an on-resistance of 0.8 Ω. The diode conduction loss can be modeled by a 0.7 V source in series with a 0.2 Ω resistor. All other losses can be neglected.

(a) Derive an equivalent circuit that models the converter input and output ports, as well as the loss elements described above.

(b) Given the range of variation of V_g and I described above, over what range will the duty cycle vary?

(c) At what operating point (i.e., at what value of V_g and I) is the converter power loss the largest? What is the value of the efficiency at this operating point?

3.11 In the Ćuk converter of Fig. 3.37, the MOSFET has on-resistance R_{on} and the diode has a constant forward voltage drop V_D. All other losses can be neglected.

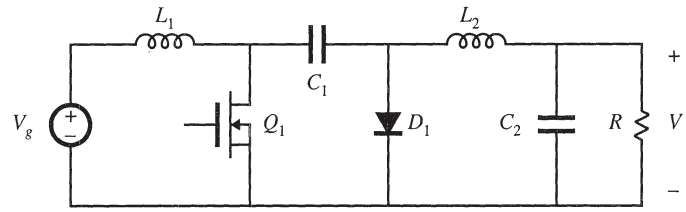


Fig. 3.37 Ćuk converter, Problem 3.11.

(a) Derive an equivalent circuit model for this converter. *Suggestion*: if you don't know how to handle some of the terms in your dc equations, then temporarily leave them as dependent sources. A more physical representation of these terms may become apparent once dc transformers are incorporated into the model.

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(b) Derive analytical expressions for the converter output voltage and for the efficiency.

(c) For $V_D = 0$, plot V/V_g vs. D over the range $0 \le D \le 1$, for (*i*) $R_{on}/R = 0.01$, and (*ii*) $R_{on}/R = 0.05$.

(d) For $V_D = 0$, plot the converter efficiency over the range $0 \le D \le 1$, for (*i*) $R_{on}/R = 0.01$, and (*ii*) $R_{on}/R = 0.05$.

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4

Switch Realization

We have seen in previous chapters that the switching elements of the buck, boost, and several other dc-dc converters can be implemented using a transistor and diode. One might wonder why this is so, and how to realize semiconductor switches in general. These are worthwhile questions to ask, and switch implementation can depend on the power processing function being performed. The switches of inverters and cycloconverters require more complicated implementations than those of dc-dc converters. Also, the way in which a semiconductor switch is implemented can alter the behavior of a converter in ways not predicted by the ideal-switch analysis of the previous chapters—an example is the discontinuous conduction mode treated in the next chapter. The realization of switches using transistors and diodes is the subject of this chapter.

Semiconductor power devices behave as single-pole single-throw (SPST) switches, represented ideally in Fig. 4.1. So, although we often draw converter schematics using ideal single-pole double-throw (SPDT) switches as in Fig. 4.2(a), the schematic of Fig. 4.2(b) containing SPST switches is more realistic. The realization of a SPDT switch using two SPST switches is not as trivial as it might at first seem, because Fig. 4.2(a) and 4.2(b) are not exactly equivalent. It is possible for both SPST switches to be simultaneously in the on state or in the off state, leading to behavior not predicted by the SPDT switch of Fig. 4.2(a). In addition, it is possible for the switch state to depend on the applied voltage or current waveforms—a familiar example is the diode. Indeed, it is common for these phenomena to occur in converters operating at light load, or occasionally at heavy load, leading to the discontinuous conduction mode previously mentioned. The converter properties are then significantly modified.

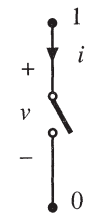


Fig. 4.1 SPST switch, with defined voltage and current polarities.

How an ideal switch can be realized using semiconductor devices depends on the polarity of the voltage that the devices must block in the off state, and on the polarity of the current that the devices

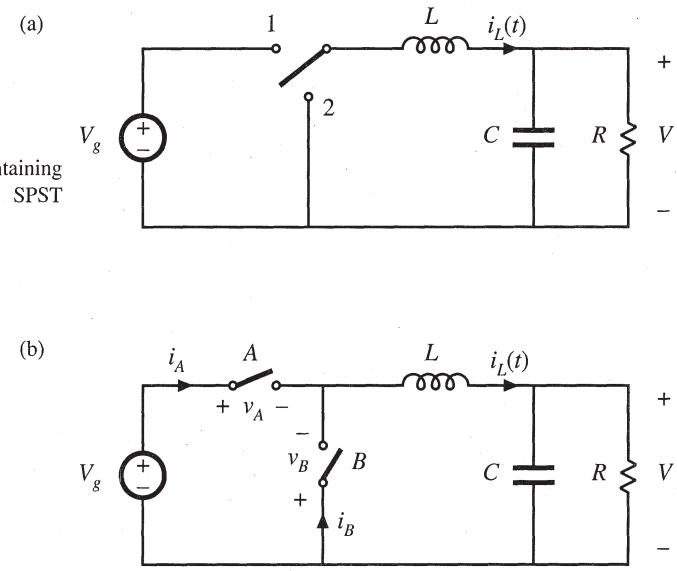


Fig. 4.2 Buck converter: (a) containing SPDT switch, (b) containing two SPST switches.

must conduct in the on state. For example, in the dc–dc buck converter of Fig. 4.2(b), switch A must block positive voltage V_g when in the off state, and must conduct positive current i_L when in the on state. If, for all intended converter operating points, the current and blocking voltage lie in a single quadrant of the plane as illustrated in Fig. 4.3, then the switch can be implemented in a simple manner using a transistor or a diode. Use of single-quadrant switches is common in dc–dc converters. Their operation is discussed briefly here.

In inverter circuits, two-quadrant switches are required. The output current is ac, and hence is sometimes positive and sometimes negative. If this current flows through the switch, then its current is ac, and the semiconductor switch realization is more complicated. A two-quadrant SPST switch can be realized using a transistor and diode. The dual case also sometimes occurs, in which the switch current is always positive, but the blocking voltage is ac. This type of two-quadrant switch can be constructed using a different arrangement of a transistor and diode. Cycloconverters generally require four-quadrant switches, which are capable of blocking ac voltages and conducting ac currents. Realizations of these elements are also discussed in this chapter.

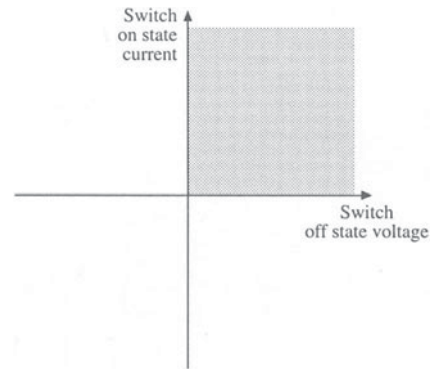


Fig. 4.3 A single-quadrant switch is capable of conducting currents of a single polarity, and of blocking voltages of a single polarity.

Next, the synchronous rectifier is examined. The reverse-conducting capability of the metal oxide semiconductor field-effect transistor (MOSFET) allows it to be used where a diode would normally be required. If the MOSFET on-resistance is sufficiently small, then its conduction loss is less than that obtained using a diode. Synchronous rectifiers are sometimes used in low-voltage high-current applications to obtain improved efficiency. Several basic references treating single-, two-, and four-quadrant

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switches are listed at the end of this chapter [1–8].

Several power semiconductor devices are briefly discussed in Section 4.2. Majority-carrier devices, including the MOSFET and Schottky diode, exhibit very fast switching times, and hence are preferred when the off state voltage levels are not too high. Minority-carrier devices, including the bipolar junction transistor (BJT), insulated-gate bipolar transistor (IGBT), and thyristors [gate turn-off (GTO) and MOS-controlled thyristor (MCT)] exhibit high breakdown voltages with low forward voltage drops, at the expense of reduced switching speed.

Having realized the switches using semiconductor devices, switching loss can next be discussed. There are a number of mechanisms that cause energy to be lost during the switching transitions [11]. When a transistor drives a clamped inductive load, it experiences high instantaneous power loss during the switching transitions. Diode stored charge further increases this loss, during the transistor turn-on transition. Energy stored in certain parasitic capacitances and inductances is lost during switching. Parasitic ringing, which decays before the end of the switching period, also indicates the presence of switching loss. Switching loss increases directly with switching frequency, and imposes a maximum limit on the operating frequencies of practical converters.

4.1 SWITCH APPLICATIONS

4.1.1 Single-Quadrant Switches

The ideal SPST switch is illustrated in Fig. 4.1. The switch contains power terminals 1 and 0, with current and voltage polarities defined as shown. In the on state, the voltage v is zero, while the current i is zero in the off state. There is sometimes a third terminal C, where a control signal is applied. Distinguishing features of the SPST switch include the control method (active vs. passive) and the region of the i–v plane in which they can operate.

A passive switch does not contain a control terminal C. The state of the switch is determined by the waveforms $i(t)$ and $v(t)$ applied to terminals 0 and 1. The most common example is the diode, illustrated in Fig. 4.4. The ideal diode requires that $v(t) \le 0$ and $i(t) \ge 0$. The diode is off ($i = 0$) when $v < 0$, and is on ($v = 0$) when $i > 0$. It can block negative voltage but not positive voltage. A passive SPST switch can be realized using a diode provided that the intended operating points [i.e., the values of $v(t)$ and $i(t)$ when the switch is in the on and off states] lie on the diode characteristic of Fig. 4.4(b).

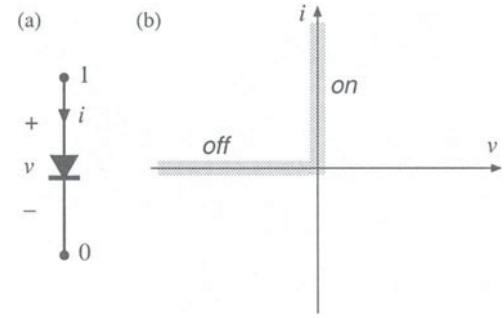


Fig. 4.4 Diode symbol (a), and its ideal characteristic (b).

The conducting state of an active switch is determined by the signal applied to the control terminal C. The state does not directly depend on the waveforms $v(t)$ and $i(t)$ applied to terminals 0 and 1. The BJT, MOSFET, IGBT, GTO, and MCT are examples of active switches. Idealized characteristics $i(t)$ vs. $v(t)$ for the BJT and IGBT are sketched in Fig. 4.5. When the control terminal causes the transistor to be in the off state, $i = 0$ and the device is capable of blocking positive voltage: $v \ge 0$. When the control terminal causes the transistor to be in the on state, $v = 0$ and the device is capable of conducting positive current: $i \ge 0$. The reverse-conducting and

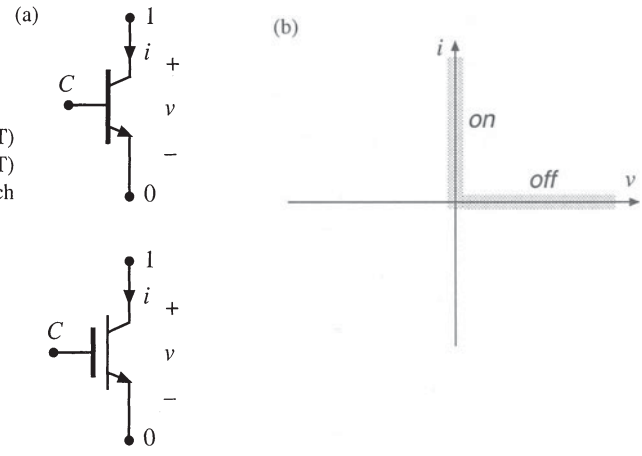


Fig. 4.5 Bipolar junction transistor (BJT) and insulated gate bipolar transistor (IGBT) symbols (a), and their idealized switch characteristics (b).

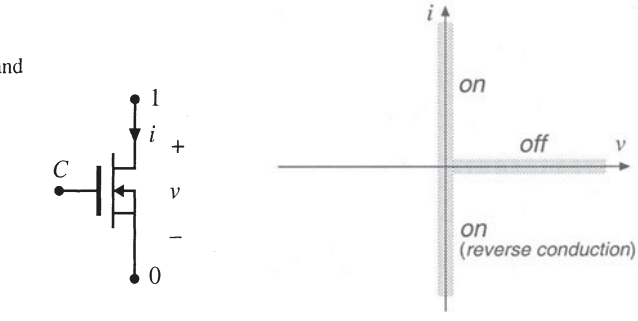


Fig. 4.6 Power MOSFET symbol (a), and its idealized switch characteristics (b).

reverse-blocking characteristics of the BJT and IGBT are poor or nonexistent, and have essentially no application in the power converter area. The power MOSFET (Fig. 4.6) has similar characteristics, except that it is able to conduct current in the reverse direction. With one notable exception (the synchronous rectifier discussed later), the MOSFET is normally operated with $i \geq 0$, in the same manner as the BJT and IGBT. So an active SPST switch can be realized using a BJT, IGBT, or MOSFET, provided that the intended operating points lie on the transistor characteristic of Fig. 4.5(b).

To determine how to implement an SPST switch using a transistor or diode, one compares the switch operating points with the *i*–*v* characteristics of Figs. 4.4(b), 4.5(b), and 4.6(b). For example, when it is intended that the SPDT switch of Fig. 4.2(a) be in position 1, SPST switch *A* of Fig. 4.2(b) is closed, and SPST switch *B* is opened. Switch *A* then conducts the positive inductor current, $i_A = i_L$, and switch *B* must block negative voltage, $v_B = -V_g$. These switch operating points are illustrated in Fig. 4.7. Likewise, when it is intended that the SPDT switch of Fig. 4.2(a) be in position 2, then SPST switch *A* is opened and switch *B* is closed. Switch *B* then conducts the positive inductor current, $i_B = i_L$, while switch *A* blocks positive voltage, $v_A = V_g$.

By comparison of the switch *A* operating points of Fig. 4.7(a) with Figs. 4.5(b) and 4.6(b), it can be seen that a transistor (BJT, IGBT, or MOSFET) could be used, since switch *A* must block positive voltage and conduct positive current. Likewise, comparison of Fig. 4.7(b) with Fig. 4.4(b) reveals that switch *B* can be implemented using a diode, since switch *B* must block negative voltage and conduct positive current. Hence a valid switch realization is given in Fig. 4.8.

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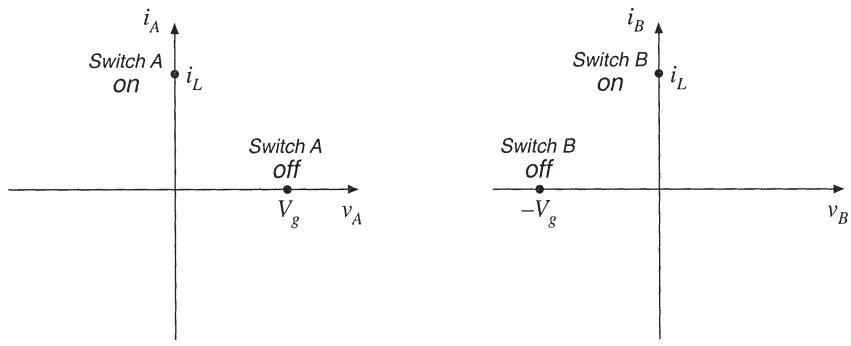


Fig. 4.7 Operating points of switch *A*, (a), and switch *B*, (b), in the buck converter of Fig. 4.2(b).

Figure 4.8 is an example of a single-quadrant switch realization: the devices are capable of conducting current of only one polarity, and blocking voltage of only one polarity. When the controller turns the transistor on, the diode becomes reverse-biased since $v_B = -V_g$. It is required that V_g be positive; otherwise, the diode will be forward-biased. The transistor conducts current i_L. This current should also be positive, so that the transistor conducts in the forward direction.

When the controller turns the transistor off, the diode must turn on so that the inductor current can continue to flow. Turning the transistor off causes the inductor current $i_L(t)$ to decrease. Since $v_L(t) = L\, di_L(t)/dt$, the inductor voltage becomes sufficiently negative to forward-bias the diode, and the diode turns on. Diodes that operate in this manner are sometimes called *freewheeling diodes*. It is required that i_L be positive; otherwise, the diode cannot be forward-biased since $i_B = i_L$. The transistor blocks voltage V_g; this voltage should be positive to avoid operating the transistor in the reverse blocking mode.

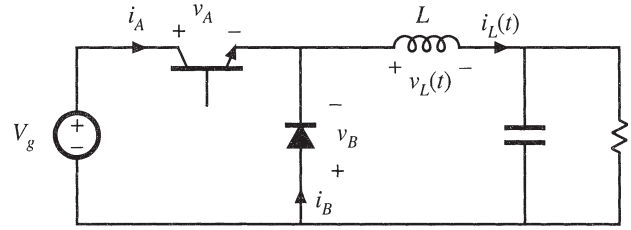


Fig. 4.8 Implementation of the SPST switches of Fig. 4.2(b) using a transistor and diode.

4.1.2 Current-Bidirectional Two-Quadrant Switches

In any number of applications such as dc-ac inverters and servo amplifiers, it is required that the switching elements conduct currents of both polarities, but block only positive voltages. A current-bidirectional two-quadrant SPST switch of this type can be realized using a transistor and diode, connected in an anti-parallel manner as in Fig. 4.9.

The MOSFET of Fig. 4.6 is also a two-quadrant switch. However, it should be noted here that

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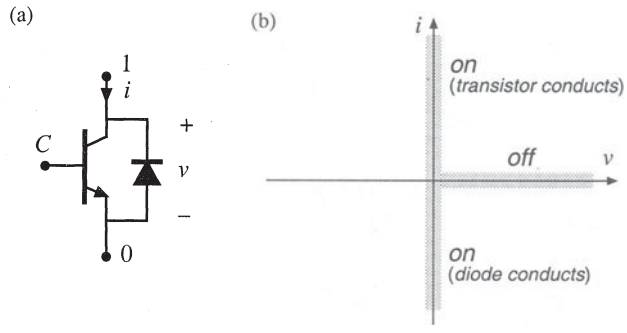


Fig. 4.9 A current-bidirectional two-quadrant SPST switch: (a) implementation using a transistor and antiparallel diode, (b) idealized switch characteristics.

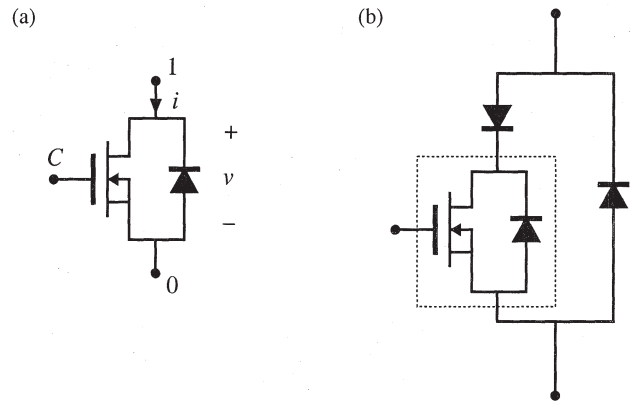


Fig. 4.10 The power MOSFET inherently contains a built-in body diode: (a) equivalent circuit, (b) addition of external diodes to prevent conduction of body diode.

practical power MOSFETs inherently contain a built-in diode, often called the *body diode*, as illustrated in Fig. 4.10. The switching speed of the body diode is much slower than that of the MOSFET. If the body diode is allowed to conduct, then high peak currents can occur during the diode turn-off transition. Most MOSFETs are not rated to handle these currents, and device failure can occur. To avoid this situation, external series and antiparallel diodes can be added as in Fig. 4.10(b). Power MOSFETs can be specifically designed to have a fast-recovery body diode, and to operate reliably when the body diode is allowed to conduct the rated MOSFET current. However, the switching speed of such body diodes is still somewhat slow, and significant switching loss due to diode stored charge (discussed later in this chapter) can occur.

A SPDT current-bidirectional two-quadrant switch can again be derived using two SPST switches as in Fig. 4.2(b). An example is given in Fig. 4.11. This converter operates from positive and negative dc supplies, and can produce an ac output voltage $v(t)$ having either polarity. Transistor Q_2 is driven with the complement of the Q_1 drive signal, so that Q_1 conducts during the first subinterval $0 < t < DT_s$, and Q_2 conducts during the second subinterval $DT_s < t < T_s$.

It can be seen from Fig. 4.11 that the switches must block voltage $2V_g$. It is required that V_g be positive; otherwise, diodes D_1 and D_2 will conduct simultaneously, shorting out the source.

It can be shown via inductor volt-second balance that

$$v_0 = (2D - 1)V_g \tag{4.1}$$

This equation is plotted in Fig. 4.12. The converter output voltage v_0 is positive for $D > 0.5$, and negative for $D < 0.5$. By sinusoidal variation of the duty cycle,

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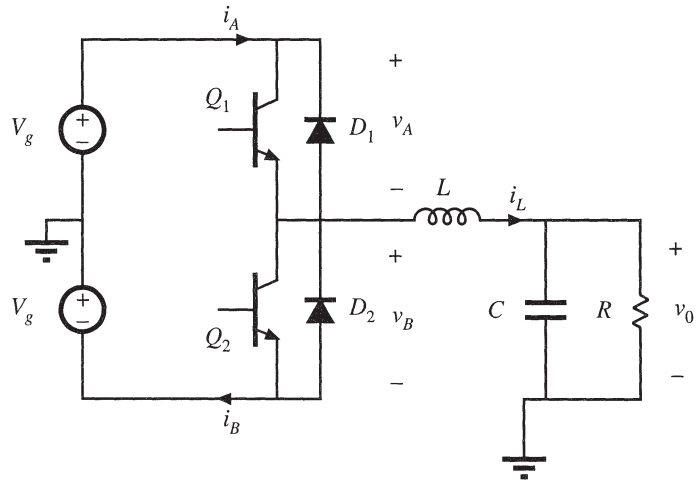


Fig. 4.11 Inverter circuit using two-quadrant switches.

$$D(t) = 0.5 + D_m \sin(\omega t) \tag{4.2}$$

with D_m being a constant less that 0.5, the output voltage becomes sinusoidal. Hence this converter could be used as a dc–ac inverter.

The load current is given by v_0/R; in equilibrium, this current coincides with the inductor current i_L,

$$i_L = \frac{v_0}{R} = (2D - 1)\frac{V_g}{R} \tag{4.3}$$

The switches must conduct this current. So the switch current is also positive when $D > 0.5$, and negative when $D < 0.5$. With high-frequency duty cycle variations, the L–C filter may introduce a phase lag into the inductor current waveform, but it is nonetheless true that switch currents of both polarities occur. So the switch must operate in two quadrants of the plane, as illustrated in Fig. 4.13. When i_L is positive, Q_1 and D_2 alternately conduct. When i_L is negative, Q_2 and D_1 alternately conduct.

A well-known dc–3øac inverter circuit, the *voltage-source inverter* (VSI), operates in a similar manner. As illustrated in Fig. 4.14, the VSI contains three two-quadrant SPDT switches, one per phase. These switches block the dc input voltage V_g, and must conduct the output ac phase currents i_a, i_b, and i_c,

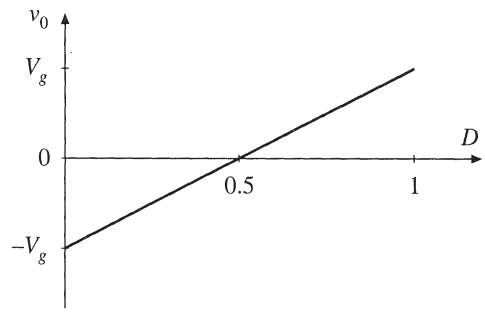


Fig. 4.12 Output voltage vs. duty cycle, for the inverter of Fig. 4.11. This converter can produce both positive and negative output voltages.

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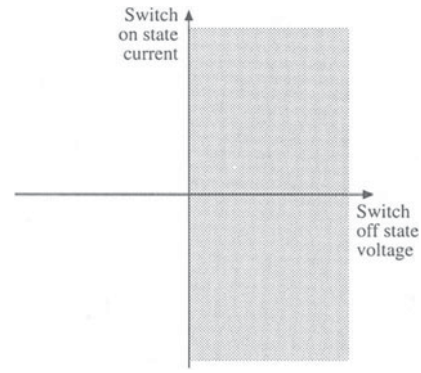


Fig. 4.13 The switches in the inverter of Fig. 4.11 must be capable of conducting both positive and negative current, but need block only positive voltage.

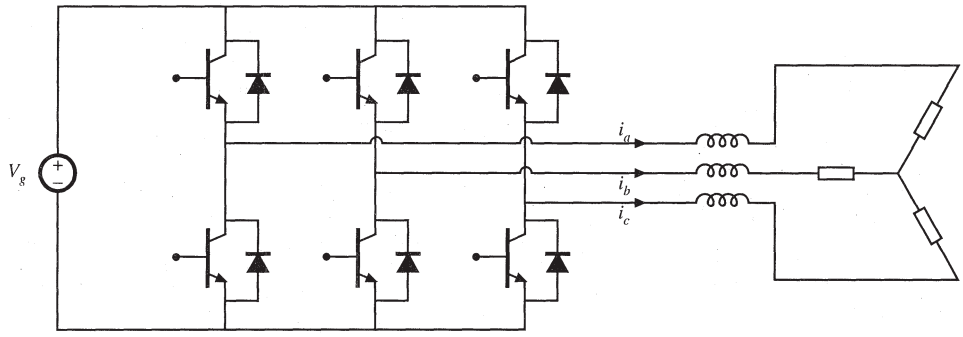


Fig. 4.14 The dc-3øac voltage-source inverter requires two-quadrant switches.

respectively.

Another current-bidirectional two-quadrant switch example is the bidirectional battery charger/discharger illustrated in Fig. 4.15. This converter can be used, for example, to interface a battery to the main power bus of a spacecraft. Both the dc bus voltage v_{bus} and the battery voltage v_{batt} are always positive. The semiconductor switch elements block positive voltage v_{bus}. When the battery is being charged, i_L is positive, and Q_1 and D_2 alternately conduct current. When the battery is being discharged, i_L is negative, and Q_2 and D_1 alternately conduct. Although this is a dc–dc converter, it requires two-quadrant switches because the power can flow in either direction.

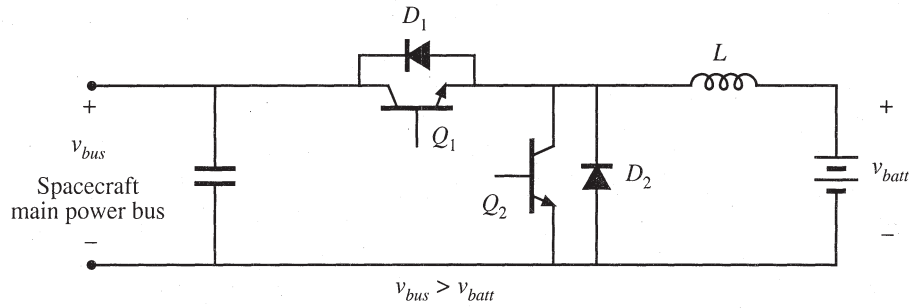


Fig. 4.15 Bidirectional battery charger/discharger, based on the dc-dc buck converter.

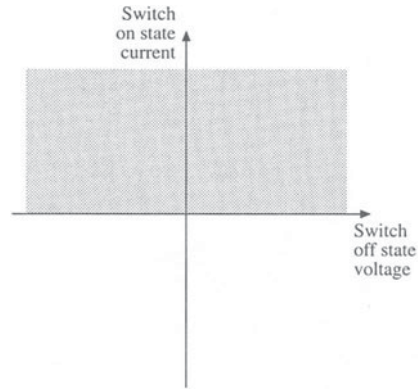


Fig. 4.16 Voltage-bidirectional two-quadrant switch properties.

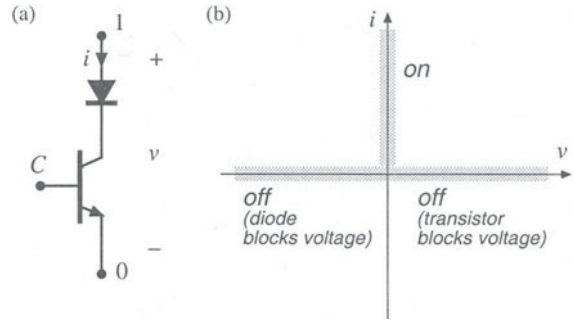


Fig. 4.17 A voltage-bidirectional two-quadrant SPST switch: (a) implementation using a transistor and series diode, (b) idealized switch characteristics.

4.1.3 Voltage-Bidirectional Two-Quadrant Switches

Another type of two-quadrant switch, having the voltage-bidirectional properties illustrated in Fig. 4.16, is sometimes required. In applications where the switches must block both positive and negative voltages, but conduct only positive current, an SPST switch can be constructed using a series-connected transistor and diode as in Fig. 4.17. When it is intended that the switch be in the off state, the controller turns the transistor off. The diode then blocks negative voltage, and the transistor blocks positive voltage. The series connection can block negative voltages up to the diode voltage rating, and positive voltages up to the transistor voltage rating. The silicon-controlled rectifier is another example of a voltage-bidirectional two-quadrant switch.

A converter that requires this type of two-quadrant switch is the dc-3øac buck-boost inverter shown in Fig. 4.18 [4]. If the converter functions in inverter mode, so that the inductor current $i_L(t)$ is always positive, then all switches conduct only positive current. But the switches must block the output ac line-to-line voltages, which are sometimes positive and sometimes negative. Hence voltage-bidirectional two-quadrant switches are required.

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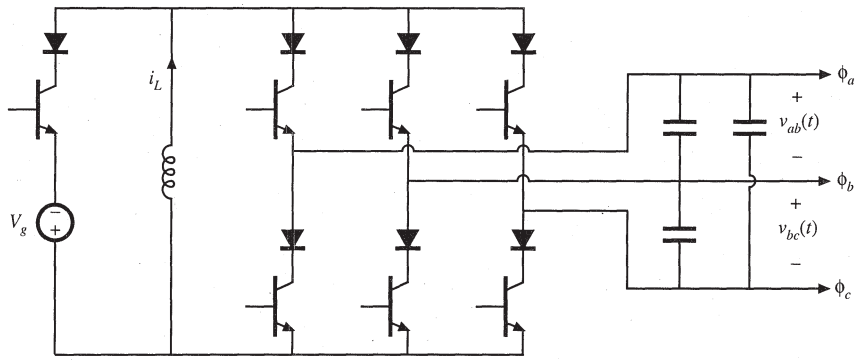


Fig. 4.18 Dc–3øac buck–boost inverter.

4.1.4 Four-Quadrant Switches

The most general type of switch is the four-quadrant switch, capable of conducting currents of either polarity and blocking voltages of either polarity, as in Fig. 4.19. There are several ways of constructing a four-quadrant switch. As illustrated in Fig. 4.20(b), two current-bidirectional two-quadrant switches described in Section 4.1.2 can be connected back-to-back. The transistors are driven on and off simultaneously. Another approach is the antiparallel connection of two voltage-bidirectional two-quadrant switches described in Section 4.1.3, as in Fig. 4.20(a). A third approach, using only one transistor but additional diodes, is given in Fig. 4.20(c).

Cycloconverters are a class of converters requiring four-quadrant switches. For example, a 3øac-to-3øac matrix converter is illustrated in Fig. 4.21. Each of the nine SPST switches is realized using one of the semiconductor networks of Fig. 4.20. With proper control of the switches, this converter can produce a three-phase output of variable fre-

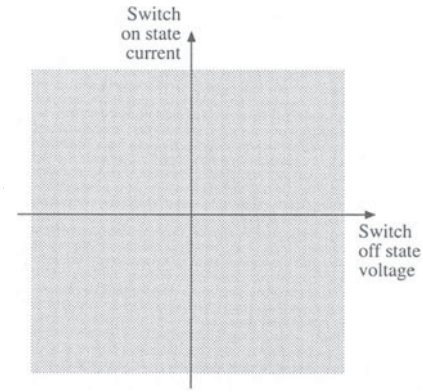


Fig. 4.19 A four-quadrant switch can conduct either polarity of current, and can block either polarity of voltage.

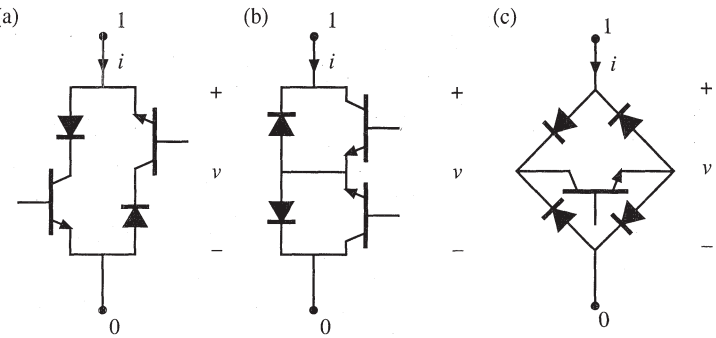


Fig. 4.20 Three ways of implementing a four-quadrant SPST switch.

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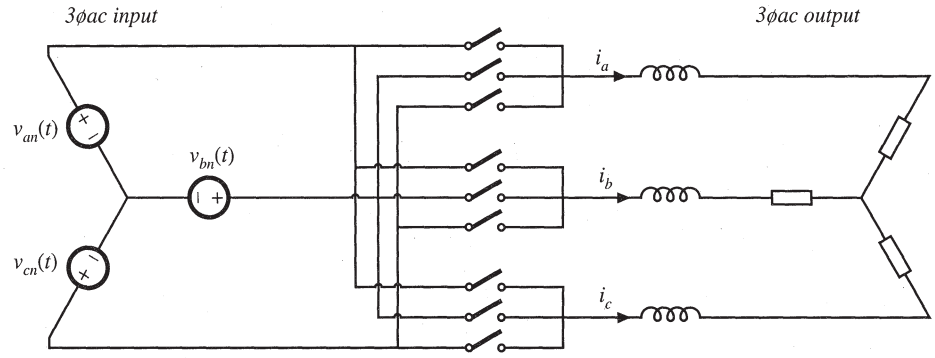


Fig. 4.21 A 3øac–3øac matrix converter, which requires nine SPST four-quadrant switches.

quency and voltage, from a given three-phase ac input. Note that there are no dc signals in this converter: all of the input and output voltages and currents are ac, and hence four-quadrant switches are necessary.

4.1.5 Synchronous Rectifiers

The ability of the MOSFET channel to conduct current in the reverse direction makes it possible to employ a MOSFET where a diode would otherwise be required. When the MOSFET is connected as in Fig. 4.22(a) [note that the source and drain connections are reversed from the connections of Fig. 4.6(a)], the characteristics of Fig. 4.22(b) are obtained. The device can now block negative voltage and conduct positive current, with properties similar to those of the diode in Fig. 4.4. The MOSFET must be controlled such that it operates in the on state when the diode would normally conduct, and in the off state when the diode would be reverse-biased.

Thus, we could replace the diode in the buck converter of Fig. 4.8 with a MOSFET, as in Fig. 4.23. The BJT has also been replaced with a MOSFET in the figure. MOSFET Q_2 is driven with the complement of the Q_1 control signal.

The trend in computer power supplies is reduction of output voltage levels, from 5 V to 3.3 V and lower. As the output voltage is reduced, the diode conduction loss increases; in consequence, the diode conduction loss is easily the largest source of power loss in a 3.3 V power supply. Unfortunately, the diode junction contact potential limits what can be done to reduce the forward voltage drop of diodes. Schottky diodes having reduced junction potential can be employed; nonetheless, low-voltage power

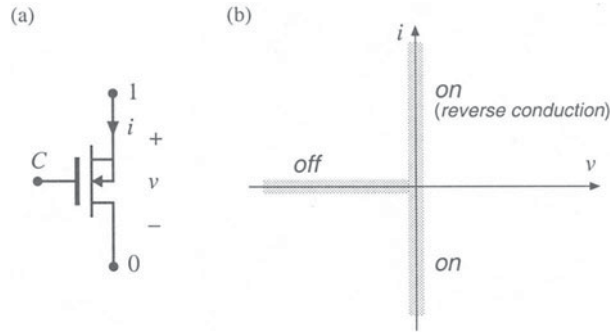


Fig. 4.22 Power MOSFET connected as a synchronous rectifier, (a), and its idealized switch characteristics, (b).

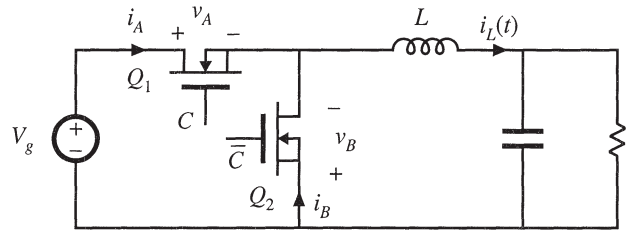


Fig. 4.23 Buck converter, implemented using a synchronous rectifier.

supplies containing diodes that conduct the output current must have low efficiency.

A solution is to replace the diodes with MOSFETs operated as synchronous rectifiers. The conduction loss of a MOSFET having on-resistance R_{on} and operated with rms current is I_{rms}, is $I_{rms}{}^2 R_{on}$. The on-resistance can be decreased by use of a larger MOSFET. So the conduction loss can be reduced as low as desired, if one is willing to pay for a sufficiently large device. Synchronous rectifiers find widespread use in low-voltage power supplies.

4.2 A BRIEF SURVEY OF POWER SEMICONDUCTOR DEVICES

The most fundamental challenge in power semiconductor design is obtaining a high breakdown voltage, while maintaining low forward voltage drop and on-resistance. A closely related issue is the longer switching times of high-voltage low–on-resistance devices. The tradeoff between breakdown voltage, on-resistance, and switching times is a key distinguishing feature of the various power devices.

The breakdown voltage of a reverse-biased *p–n* junction and its associated depletion region is a function of doping level: obtaining a high breakdown voltage requires low doping concentration, and hence high resistivity, in the material on at least one side of the junction. This high-resistivity region is usually the dominant contributor to the on-resistance of the device, and hence high-voltage devices must have higher on-resistance than low-voltage devices. In *majority carrier* devices, including the MOSFET and Schottky diode, this accounts for the first-order dependence of on-resistance on rated voltage. However, *minority carrier* devices, including the diffused-junction *p–n* diode, the bipolar junction transistor (BJT), the insulated-gate bipolar transistor (IGBT), and the thyristor family (SCR, GTO, MCT), exhibit another phenomenon known as *conductivity modulation*. When a minority-carrier device operates in the on state, minority carriers are injected into the lightly doped high-resistivity region by the forward-biased *p–n* junction. The resulting high concentration of minority carriers effectively reduces the apparent resistivity of the region, reducing the on-resistance of the device. Hence, minority-carrier devices exhibit lower on-resistances than comparable majority-carrier devices.

However, the advantage of decreased on-resistance in minority-carrier devices comes with the disadvantage of decreased switching speed. The conducting state of any semiconductor device is controlled by the presence or absence of key charge quantities within the device, and the turn-on and turn-off switching times are equal to the times required to insert or remove this controlling charge. Devices operating with conductivity modulation are controlled by their injected minority carriers. The total amount of controlling minority charge in minority-carrier devices is much greater than the charge required to control an equivalent majority-carrier device. Although the mechanisms for inserting and removing the controlling charge of the various devices can differ, it is nonetheless true that, because of their large amounts of minority charge, minority-carrier devices exhibit switching times that are significantly longer than those of majority-carrier devices. In consequence, majority-carrier devices find application at lower volt-

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age levels and higher switching frequencies, while the reverse is true of minority-carrier devices.

Modern power devices are fabricated using up-to-date processing techniques. The resulting small feature size allows construction of highly interdigitated devices, whose unwanted parasitic elements are less significant. The resulting devices are more rugged and well-behaved than their predecessors.

A detailed description of power semiconductor device physics and switching mechanisms is beyond the scope of this book. Selected references on power semiconductor devices are listed in the reference section [9-19].

4.2.1 Power Diodes

As discussed above, the diffused-junction p–n diode contains a lightly doped or intrinsic high-resistivity region, which allows a high breakdown voltage to be obtained. As illustrated in Fig. 4.24(a), this region comprises one side of the p–n^- junction (denoted n^-); under reverse-biased conditions, essentially all of the applied voltage appears across the depletion region inside the n^- region. On-state conditions are illustrated in Fig. 4.24(b). Holes are injected across the forward-biased junction, and become minority carriers in the n^- region. These minority carriers effectively reduce the apparent resistivity of the n^- region via conductivity modulation. Essentially all of the forward current $i(t)$ is comprised of holes that diffuse across the p–n region, and then recombine with electrons from the n region.

Typical switching waveforms are illustrated in Fig. 4.25. The familiar exponential i–v character-

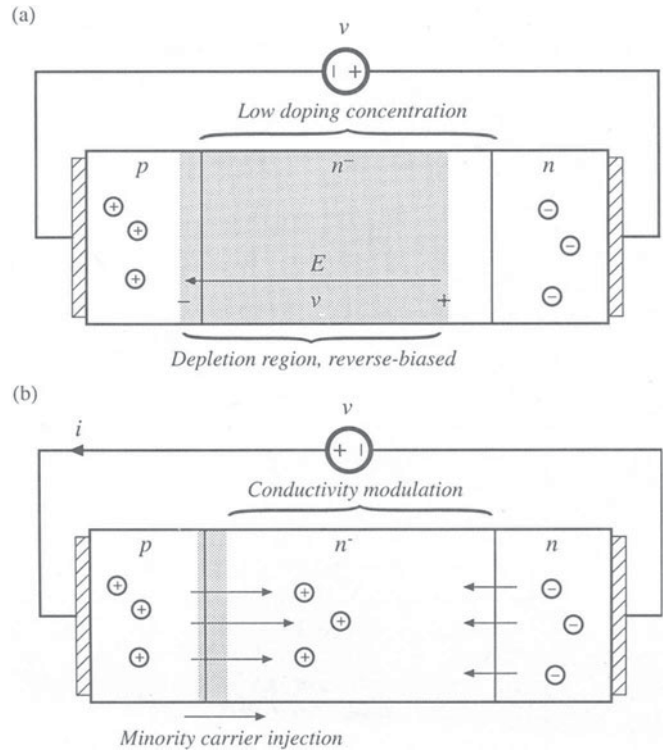


Fig. 4.24 Power diode: (a) under reverse-bias conditions, (b) under forward-bias conditions.

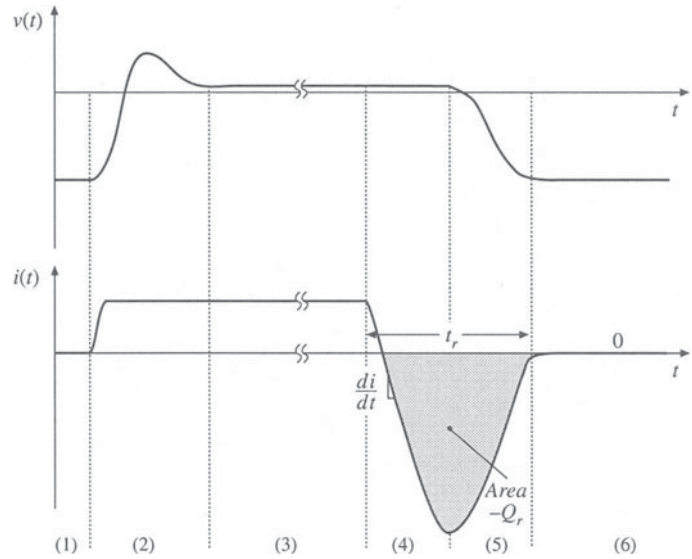


Fig. 4.25 Diode voltage and current waveforms. Interval (1): off state. Interval (2): turn-on transition. Interval (3): on state. Intervals (4) and (5): turn-off transition. Interval (6): off state.

istic of the *p–n* diode is an equilibrium relation. During transients, significant deviations from the exponential characteristic are observed; these deviations are associated with changes in the stored minority charge. As illustrated in Fig. 4.25, the diode operates in the off state during interval (1), with zero current and negative voltage. At the beginning of interval (2), the current increases to some positive value. This current charges the effective capacitance of the reverse-biased diode, supplying charge to the depletion region and increasing the voltage $v(t)$. Eventually, the voltage becomes positive, and the diode junction becomes forward-biased. The voltage may rise to a peak value of several volts, or even several tens of volts, reflecting the somewhat large resistance of the lightly doped n^- region. The forward-biased p–n^- junction continues to inject minority charge into the n^- region. As the total minority charge in the n^- region increases, conductivity modulation of the n^- region causes its effective resistance to decrease, and hence the forward voltage drop $v(t)$ also decreases. Eventually, the diode reaches equilibrium, in which the minority carrier injection rate and recombination rate are equal. During interval (3), the diode operates in the on state, with forward voltage drop given by the diode static i–v characteristic.

The turn-off transient is initiated at the beginning of interval (4). The diode remains forward-biased while minority charge is present in the vicinity of the diode p–n^- junction. Reduction of the stored minority charge can be accomplished either by active means, via negative terminal current, or by passive means, via recombination. Normally, both mechanisms occur simultaneously. The charge Q_r contained in the negative portion of the diode turn-off current waveform is called the *recovered charge*. The portion of Q_r occurring during interval (4) is actively-removed minority charge. At the end of interval (4), the stored minority charge in the vicinity of the p–n^- junction has been removed, such that the diode junction becomes reverse-biased and is able to block negative voltage. The depletion region effective capacitance is then charged during interval (5) to the negative off-state voltage. The portion of Q_r occurring during interval (5) is charge supplied to the depletion region, as well as minority charge that is actively removed from remote areas of the diode. At the end of interval (5), the diode is able to block the entire applied reverse voltage. The length of intervals (4) and (5) is called the *reverse recovery time* t_r. During interval (6), the diode operates in the off state. The diode turn-off transition, and its influence on switching loss in a PWM converter, is discussed further in Section 4.3.2.

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Table 4.1 Characteristics of several commercial power rectifier diodes

Part number	Rated maximum voltage	Rated average current	V_F (typical)	t_r (max)
Fast recovery rectifiers				
1N3913	400 V	30 A	1.1 V	400 ns
SD453N25S20PC	2500 V	400 A	2.2 V	3 μs
Ultra-fast recovery rectifiers				
MUR815	150 V	8 A	0.975 V	35 ns
MUR1560	600 V	15 A	1.2 V	60 ns
RHRU100120	1200 V	100 A	2.6 V	60 ns
Schottky rectifiers				
MBR6030L	30 V	60 A	0.48 V	
444CNQ045	45 V	440 A	0.69 V	
30CPQ150	150 V	30 A	1.19 V	

Diodes are rated according to the length of their reverse recovery time t_r. *Standard recovery* rectifiers are intended for 50 Hz or 60 Hz operation; reverse recovery times of these devices are usually not specified. *Fast recovery* rectifiers and *ultrafast recovery* rectifiers are intended for use in converter applications. The reverse recovery time t_r, and sometimes also the recovered charge Q_r, are specified by manufacturers of these devices. Ratings of several commercial devices are listed in Table 4.1.

Schottky diodes are essentially majority-carrier devices whose operation is based on the rectifying characteristic of a metal-semiconductor junction. These devices exhibit negligible minority stored charge, and their switching behavior can be adequately modeled simply by their depletion-region capacitance and equilibrium exponential *i–v* characteristic. Hence, an advantage of the Schottky diode is its fast switching speed. An even more important advantage of Schottky diodes is their low forward voltage drops, especially in devices rated 45 V or less. Schottky diodes are restricted to low breakdown voltages; very few commercial devices are rated to block 100 V or more. Their off-state reverse currents are considerably higher than those of *p–n* junction diodes. Characteristics of several commercial Schottky rectifiers are also listed in Table 4.1.

Another important characteristic of a power semiconductor device is whether its on-resistance and forward voltage drop exhibit a positive temperature coefficient. Such devices, including the MOSFET and IGBT, are advantageous because multiple chips can be easily paralleled, to obtain high-current modules. These devices also tend to be more rugged and less susceptible to hot-spot formation and second-breakdown problems. Diodes cannot be easily connected in parallel, because of their negative temperature coefficients: an imbalance in device characteristics may cause one diode to conduct more current than the others. This diode becomes hotter, which causes it to conduct even more of the total current. In consequence, the current does not divide evenly between the paralleled devices, and the current rating of one of the devices may be exceeded. Since BJTs and thyristors are controlled by a diode junction, these devices also exhibit negative temperature coefficients and have similar problems when operated in parallel. Of course, it is possible to parallel any type of semiconductor device; however, use of matched devices, a common thermal substrate, and/or external circuitry may be required to cause the on-state currents of the devices to be equal.

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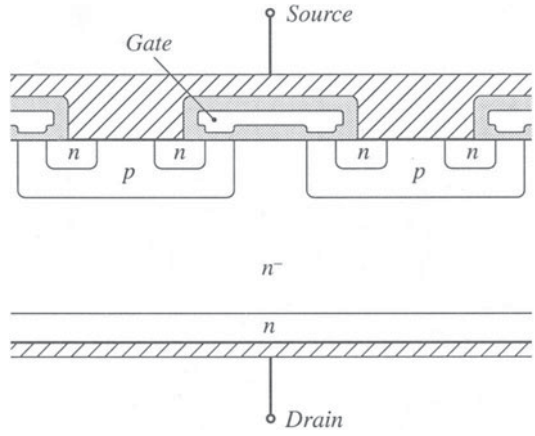


Fig. 4.26 Cross-section of DMOS *n*-channel power MOSFET structure. Crosshatched regions are metallized contacts. Shaded regions are insulating silicon dioxide layers.

4.2.2 Metal Oxide Semiconductor Field-Effect Transistor (MOSFET)

The power MOSFET is a modern power semiconductor device having gate lengths close to one micron. The power device is comprised of many small parallel-connected enhancement-mode MOSFET cells, which cover the surface of the silicon die. A cross-section of one cell is illustrated in Fig. 4.26. Current flows vertically through the silicon wafer: the metallized drain connection is made on the bottom of the chip, while the metallized source connection and polysilicon gate are on the top surface. Under normal operating conditions, in which $v_{ds} \geq 0$, both the p–n and p–n^- junctions are reverse-biased. Figure 4.27(a) illustrates operation of the device in the off state. The applied drain-to-source voltage then appears across the depletion region of the p–n^- junction. The n^- region is lightly doped, such that the desired breakdown voltage rating is attained. Figure 4.27(b) illustrates operation in the on state, with a sufficiently large positive gate-to-source voltage. A channel then forms at the surface of the p region, underneath the gate. The drain current flows through the n^- region, channel, n region, and out through the source contact. The on-resistance of the device is the sum of the resistances of the n^- region, the channel, the source and drain contacts, etc. As the breakdown voltage is increased, the on-resistance becomes dominated by the resistance of the n^- region. Since there are no minority carriers to cause conductivity modulation, the on-resistance increases rapidly as the breakdown voltage is increased to several hundred volts and beyond.

The p–n^- junction is called the *body diode*; as illustrated in Fig. 4.27(c), this junction forms an effective diode in parallel with the MOSFET channel. The body diode can become forward-biased when the drain-to-source voltage $v_{ds}(t)$ is negative. This diode is capable of conducting the full rated current of the MOSFET. However, most MOSFETs are not optimized with respect to the speed of their body diodes, and the large peak currents that flow during the reverse recovery transition of the body diode can cause device failure. Several manufacturers produce MOSFETs that contain fast recovery body diodes; these devices are rated to withstand the peak currents during the body diode reverse recovery transition.

Typical n-channel MOSFET static switch characteristics are illustrated in Fig. 4.28. The drain current is plotted as a function of the gate-to-source voltage, for various values of drain-to-source voltage. When the gate-to-source voltage is less than the threshold voltage V_{th}, the device operates in the off state. A typical value of V_{th} is 3 V. When the gate-to-source voltage is greater than 6 or 7 V, the device operates in the on state; typically, the gate is driven to 12 or 15 V to ensure minimization of the forward voltage drop. In the on state, the drain-to-source voltage V_{DS} is roughly proportional to the drain current

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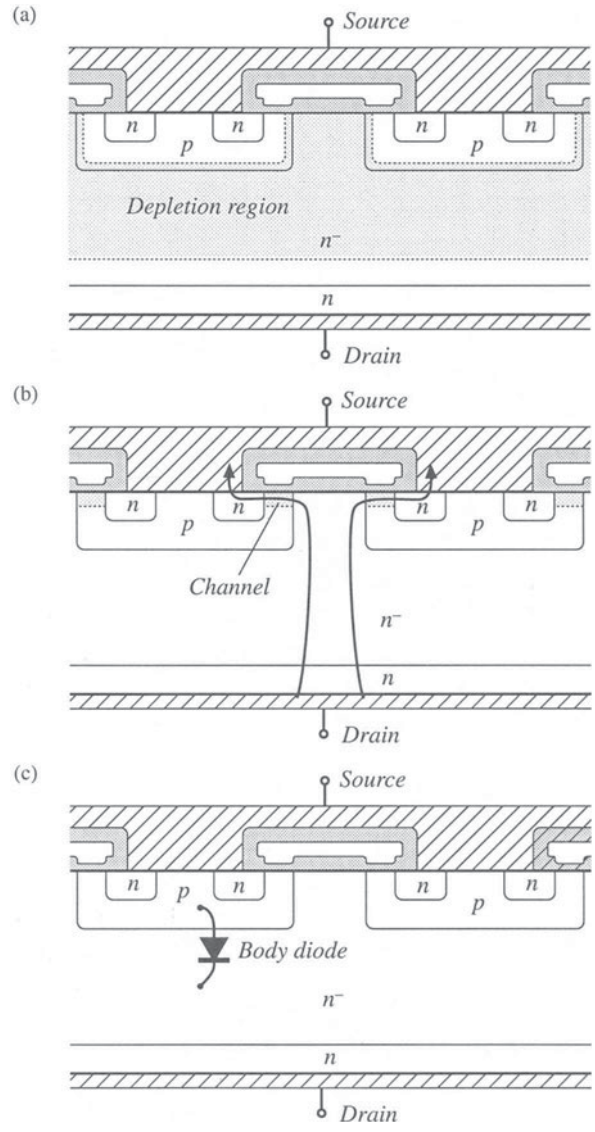


Fig. 4.27 Operation of the power MOSFET: (a) in the off state, v_{ds} appears across the depletion region in the n^- region; (b) current flow through the conducting channel in the on state; (c) body diode due to the p–n^- junction.

I_D. The MOSFET is able to conduct peak currents well in excess of its average current rating, and the nature of the static characteristics is unchanged at high current levels. Logic-level power MOSFETs are also available, which operate in the on state with a gate-to-source voltage of 5 V. A few p-channel devices can be obtained, but their properties are inferior to those of equivalent n-channel devices.

The on-resistance and forward voltage drop of the MOSFET have a positive temperature coefficient. This property makes it relatively easy to parallel devices. High current MOSFET modules are available, containing several parallel-connect chips.

The major capacitances of the MOSFET are illustrated in Fig. 4.29. This model is sufficient for

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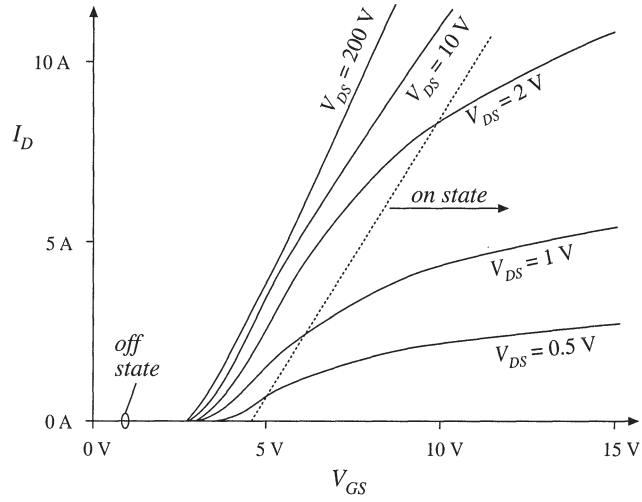


Fig. 4.28 Typical static characteristics of a power MOSFET. Drain current I_D is plotted vs. gate-to-source voltage V_{GS}, for various values of drain-to-source voltage V_{DS}.

qualitative understanding of the MOSFET switching behavior; more accurate models account for the parasitic junction field-effect transistor inherent in the DMOS geometry. Switching times of the MOSFET are determined essentially by the times required for the gate driver to charge these capacitances. Since the drain current is a function of the gate-to-source voltage, the rate at which the drain current changes is dependent on the rate at which the gate-to-source capacitance is charged by the gate drive circuit. Likewise, the rate at which the drain voltage changes is a function of the rate at which the gate-to-drain capacitance is charged. The drain-to-source capacitance leads directly to switching loss in PWM converters, since the energy stored in this capacitance is lost during the transistor turn-on transition. Switching loss is discussed in Section 4.3.

The gate-to-source capacitance is essentially linear. However, the drain-to-source and gate-to-drain capacitances are strongly nonlinear: these incremental capacitances vary as the inverse square root of the applied capacitor voltage. For example, the dependence of the incremental drain-to-source capacitance can be written in the form

$$C_{ds}(v_{ds}) = \frac{C_0}{\sqrt{1 + \frac{v_{ds}}{V_0}}} \tag{4.4}$$

where C_0 and V_0 are constants that depend on the construction of the device. These capacitances can easily vary by several orders of magnitude as v_{ds} varies over its normal operating range. For $v_{ds} \gg V_0$, Eq.

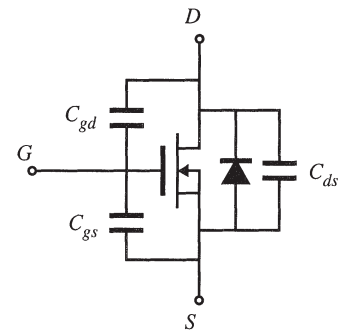


Fig. 4.29 MOSFET equivalent circuit which accounts for the body diode and effective terminal capacitances.

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Table 4.2 Characteristics of several commercial *n*-channel power MOSFETs

Part number	Rated maximum voltage	Rated average current	R_{on}	Q_g (typical)
IRFZ48	60 V	50 A	0.018 Ω	110 nC
IRF510	100 V	5.6 A	0.54 Ω	8.3 nC
IRF540	100 V	28 A	0.077 Ω	72 nC
APT10M25BNR	100 V	75 A	0.025 Ω	171 nC
IRF740	400 V	10 A	0.55 Ω	63 nC
MTM15N40E	400 V	15 A	0.3 Ω	110 nC
APT5025BN	500 V	23 A	0.25 Ω	83 nC
APT1001RBNR	1000 V	11 A	1.0 Ω	150 nC

(4.4) can be approximated as

$$C_{ds}(v_{ds}) \approx C_0 \sqrt{\frac{V_0}{v_{ds}}} = \frac{C_0'}{\sqrt{v_{ds}}} \tag{4.5}$$

These expressions are used in Section 4.3.3 to determine the switching loss due to energy stored in C_{ds}.

Characteristics of several commercially available power MOSFETs are listed in Table 4.2. The gate charge Q_g is the charge that the gate drive circuit must supply to the MOSFET to raise the gate voltage from zero to some specified value (typically 10 V), with a specified value of off state drain-to-source voltage (typically 80% of the rated V_{DS}). The total gate charge is the sum of the charges on the gate-to-drain and the gate-to-source capacitance. The total gate charge is to some extent a measure of the size and switching speed of the MOSFET.

Unlike other power devices, MOSFETs are usually not selected on the basis of their rated average current. Rather, on-resistance and its influence on conduction loss are the limiting factors, and MOSFETs typically operate at average currents somewhat less than the rated value.

MOSFETs are usually the device of choice at voltages less than or equal to approximately 400 to 500 V. At these voltages, the forward voltage drop is competitive or superior to the forward voltage drops of minority-carrier devices, and the switching speed is significantly faster. Typical switching times are in the range 50 ns to 200 ns. At voltages greater than 400 to 500 V, minority-carrier devices having lower forward voltage drops, such as the IGBT, are usually preferred. The only exception is in applications where the high switching speed overrides the increased cost of silicon required to obtain acceptably low conduction loss.

4.2.3 Bipolar Junction Transistor (BJT)

A cross-section of an NPN power BJT is illustrated in Fig. 4.30. As with other power devices, current flows vertically through the silicon wafer. A lightly doped n^- region is inserted in the collector, to obtain the desired voltage breakdown rating. The transistor operates in the off state (cutoff) when the p–n base-emitter junction and the p–n^- base-collector junction are reverse-biased; the applied collector-to-emitter voltage then appears essentially across the depletion region of the p–n^- junction. The transistor operates in the on state (saturation) when both junctions are forward-biased; substantial minority charge is then present in the p and n^- regions. This minority charge causes the n^- region to exhibit a low on-

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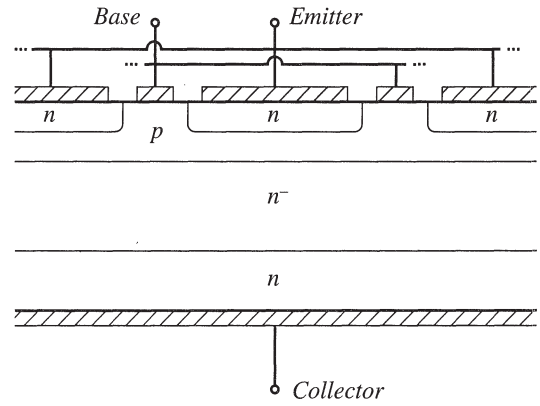


Fig. 4.30 Power BJT structure. Crosshatched regions are metallized contacts.

resistance via the conductivity modulation effect. Between the off state and the on state is the familiar active region, in which the p–n base-emitter junction is forward-biased and the p–n^- base-collector junction is reverse-biased. When the BJT operates in the active region, the collector current is proportional to the base region minority charge, which in turn is proportional (in equilibrium) to the base current. There is in addition a fourth region of operation known as *quasi-saturation*, occurring between the active and saturation regions. Quasi-saturation occurs when the base current is insufficient to fully saturate the device; hence, the minority charge present in the n^- region is insufficient to fully reduce the n^- region resistance, and high transistor on-resistance is observed.

Consider the simple switching circuit of Fig. 4.31. Figure 4.32 contains waveforms illustrating the BJT turn-on and turn-off transitions. The transistor operates in the off state during interval (1), with the base-emitter junction reverse-biased by the source voltage $v_s(t) = -V_{s1}$. The turn-on transition is initiated at the beginning of interval (2), when the source voltage changes to $v_s(t) = +V_{s2}$. Positive current is then supplied by source v_s to the base of the BJT. This current first charges the capacitances of the depletion regions of the reverse-biased base-emitter and base-collector junctions. At the end of interval (2), the base-emitter voltage exceeds zero sufficiently for the base-emitter junction to become forward-biased. The length of interval (2) is called the *turn-on delay time*. During interval (3), minority charge is injected across the base-emitter junction from the emitter into the base region; the collector current is proportional to this minority base charge. Hence during interval (3), the collector current increases. Since the transistor drives a resistive load R_L, the collector voltage also decreases during interval (3). This causes the voltage to reduce across the reverse-biased base-collector depletion region (Miller) capacitance. Increasing the base current I_{B1} (by reducing R_B or increasing V_{s2}) increases the rate of change of both the base region minority charge and the charge in the Miller capacitance. Hence, increased I_{B1} leads to a decreased turn-on switching time.

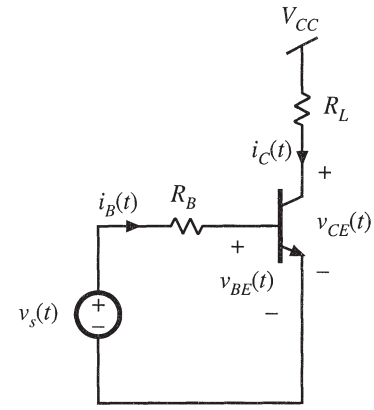


Fig. 4.31 Circuit for BJT switching time example.

Near or at the end of interval (3), the base-collector p–n^- junction becomes forward-biased. Minority carriers are then injected into the n^- region, reducing its effective resistivity. Depending on the device geometry and the magnitude of the base current, a *voltage tail* [interval (4)] may be observed as

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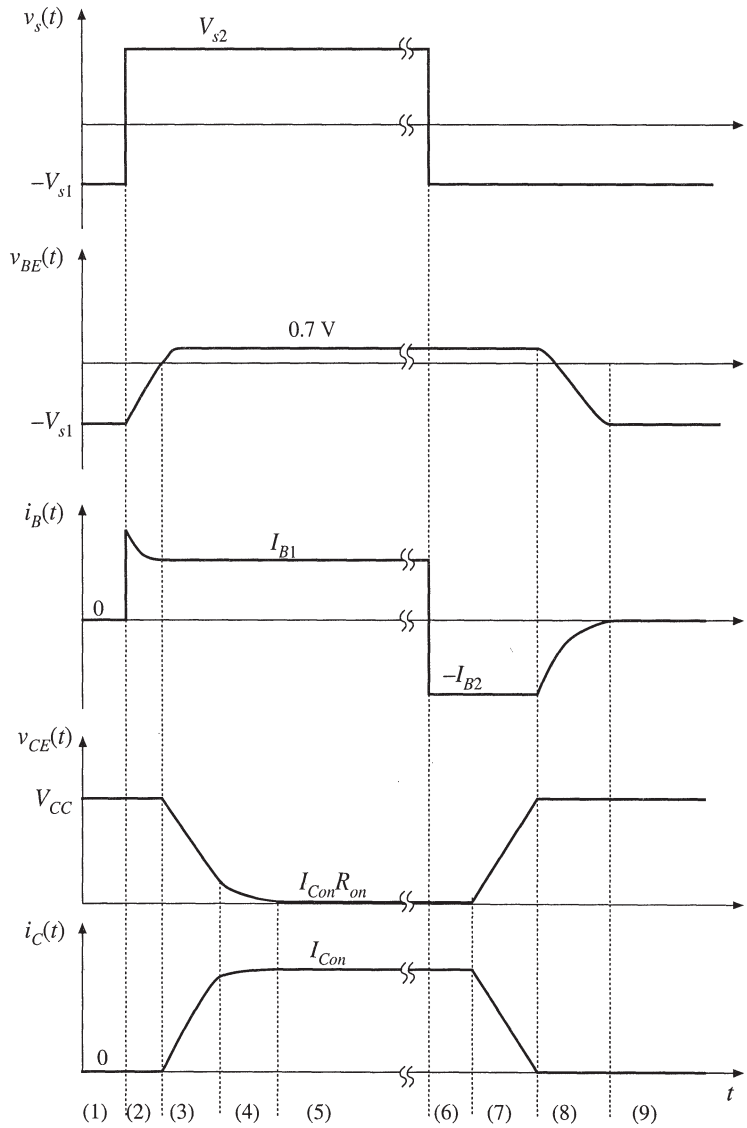


Fig. 4.32 BJT turn-on and turn-off transition waveforms.

the apparent resistance of the n^- region decreases via conductivity modulation. The BJT reaches on-state equilibrium at the beginning of interval (5), with low on-resistance and with substantial minority charge present in both the n^- and p regions. This minority charge significantly exceeds the amount necessary to support the active region conduction of the collector current I_{Con}; its magnitude is a function of $I_{B1} - I_{Con}/\beta$, where β is the active-region current gain.

The turn-off process is initiated at the beginning of interval (6), when the source voltage changes to $v_s(t) = -V_{s1}$. The base-emitter junction remains forward-biased as long as minority carriers are present in its vicinity. Also, the collector current continues to be $i_C(t) = I_{Con}$ as long as the minority

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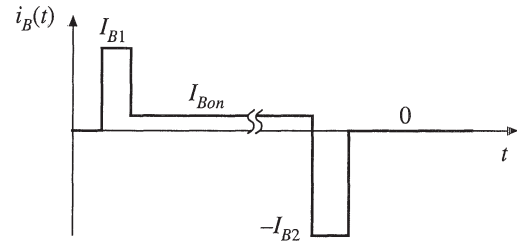


Fig. 4.33 Ideal base current waveform for minimization of switching times.

charge exceeds the amount necessary to support the active region conduction of I_{Con}, that is, as long as *excess charge* is present. So during interval (6), a negative base current flows equal to $-I_{B2} = (-V_{s1} - v_{BE}(t))/R_B$. This negative base current actively removes the total stored minority charge. Recombination further reduces the stored minority charge. Interval (6) ends when all of the excess minority charge has been removed. The length of interval (6) is called the *storage time*. During interval (7), the transistor operates in the active region. The collector current $i_C(t)$ is now proportional to the stored minority charge. Recombination and the negative base current continue to reduce the minority base charge, and hence the collector current decreases. In addition, the collector voltage increases, and hence the base current must charge the Miller capacitance. At the end of interval (7), the minority stored charge is equal to zero, and the base-emitter junction can become reverse-biased. The length of interval (7) is called the turn-off time or *fall time*. During interval (8), the reverse-biased base-emitter junction capacitance is discharged to voltage $-V_{s1}$. During interval (9), the transistor operates in equilibrium, in the off state.

It is possible to turn the transistor off using $I_{B2} = 0$; for example, we could let V_{s1} be approximately zero. However, this leads to very long storage and turn-off switching times. If $I_{B2} = 0$, then all of the stored minority charge must be removed passively, via recombination. From the standpoint of minimizing switching times, the base current waveform of Fig. 4.33 is ideal. The initial base current I_{B1} is large in magnitude, such that charge is inserted quickly into the base, and the turn-on switching times are short. A compromise value of equilibrium on state current I_{Bon} is chosen, to yield a reasonably low collector-to-emitter forward voltage drop, while maintaining moderate amounts of excess stored minority charge and hence keeping the storage time reasonably short. The current $-I_{B2}$ is large in magnitude, such that charge is removed quickly from the base and hence the storage and turn-off switching times are minimized.

Unfortunately, in most BJTs, the magnitudes of I_{B1} and I_{B2} must be limited because excessive values lead to device failure. As illustrated in Fig. 4.34, the base current flows laterally through the p

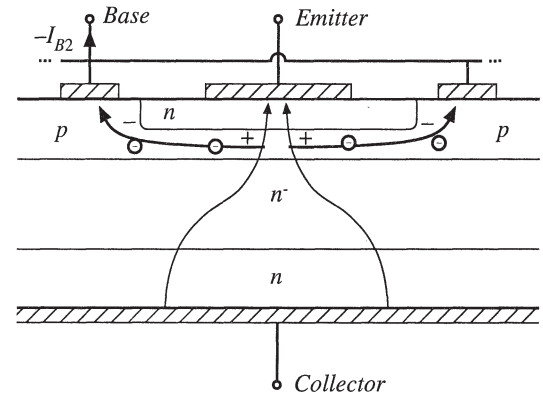


Fig. 4.34 A large I_{B2} leads to focusing of the emitter current away from the base contacts, due to the voltage induced by the lateral base region current.

region. This current leads to a voltage drop in the resistance of the p material, which influences the voltage across the base-emitter junction. During the turn-off transition, the base current $-I_{B2}$ causes the base-emitter junction voltage to be greater in the center of the base region, and smaller at the edges near the base contacts. This causes the collector current to focus near the center of the base region. In a similar fashion, a large I_{B1} causes the collector current to crowd near the edges of the base region during the turn-on transition. Since the collector-to-emitter voltage and collector current are simultaneously large during the switching transitions, substantial power loss can be associated with current focusing. Hence hot spots are induced at the center or edge of the base region. The positive temperature coefficient of the base-emitter junction current (corresponding to a negative temperature coefficient of the junction voltage) can then lead to thermal runaway and device failure. Thus, to obtain reliable operation, it may be necessary to limit the magnitudes of I_{B1} and I_{B2}. It may also be necessary to add external *snubber* networks which the reduce the instantaneous transistor power dissipation during the switching transitions.

Steady-state characteristics of the BJT are illustrated in Fig. 4.35. In Fig. 4.35(a), the collector current I_C is plotted as a function of the base current I_B, for various values of collector-to-emitter voltage V_{CE}. The cutoff, active, quasi-saturation, and saturation regions are identified. At a given collector cur-

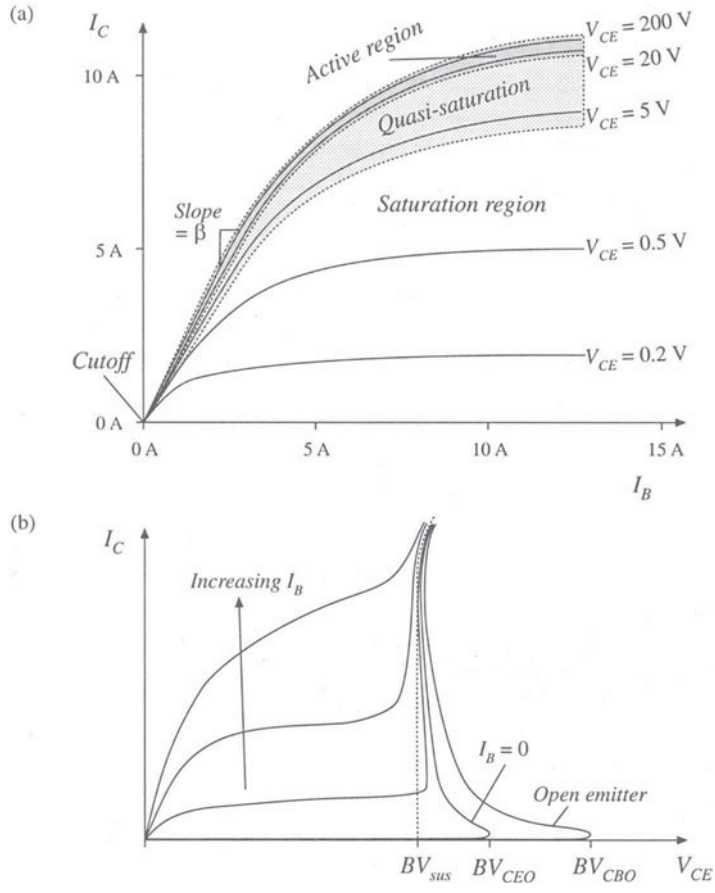


Fig. 4.35 BJT static characteristics: (a) I_C vs. I_B, illustrating the regions of operation; (b) I_C vs. V_{CE}, illustrating voltage breakdown characteristics.

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rent I_C, to operate in the saturation region with minimum forward voltage drop, the base current I_B must be sufficiently large. The slope dI_C/dI_B in the active region is the current gain β. It can be seen that β decreases at high current—near the rated current of the BJT, the current gain decreases rapidly and hence it is difficult to fully saturate the device. Collector current I_C is plotted as a function of collector-to-emitter voltage V_{CE} in Fig. 4.35(b), for various values of I_B. The breakdown voltages BV_{sus}, BV_{CEO}, and BV_{CBO} are illustrated. BV_{CBO} is the avalanche breakdown voltage of the base-collector junction, with the emitter open-circuited or with sufficiently negative base current. BV_{CEO} is the somewhat smaller collector-emitter breakdown voltage observed when the base current is zero; as avalanche breakdown is approached, free carriers are created that have the same effect as a positive base current and that cause the breakdown voltage to be reduced. BV_{sus} is the breakdown voltage observed with positive base current. Because of the high instantaneous power dissipation, breakdown usually results in destruction of the BJT. In most applications, the off state transistor voltage must not exceed BV_{CEO}.

High-voltage BJTs typically have low current gain, and hence Darlington-connected devices (Fig. 4.36) are common. If transistors Q_1 and Q_2 have current gains β_1 and β_2, respectively, then the Darlington-connected device has the substantially increased current gain $\beta_1 + \beta_2 + \beta_1\beta_2$. In a monolithic Darlington device, transistors Q_1 and Q_2 are integrated on the same silicon wafer. Diode D_1 speeds up the turn-off process, by allowing the base driver to actively remove the stored charge of both Q_1 and Q_2 during the turn-off transition.

At voltage levels below 500 V, the BJT has been almost entirely replaced by the MOSFET in power applications. It is also being displaced in higher voltage applications, where new designs utilize faster IGBTs or other devices.

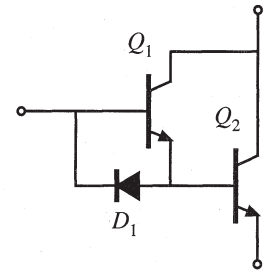


Fig. 4.36 Darlington-connected BJTs, including diode for improvement of turn-off times.

4.2.4 Insulated Gate Bipolar Transistor (IGBT)

A cross-section of the IGBT is illustrated in Fig. 4.37. Comparison with Fig. 4.26 reveals that the IGBT and power MOSFET are very similar in construction. The key difference is the *p* region connected to the collector of the IGBT. So the IGBT is a modern four-layer power semiconductor device having a MOS gate.

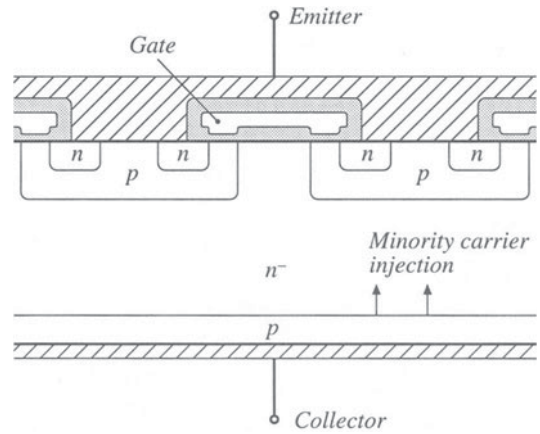


Fig. 4.37 IGBT structure. Crosshatched regions are metallized contacts. Shaded regions are insulating silicon dioxide layers.

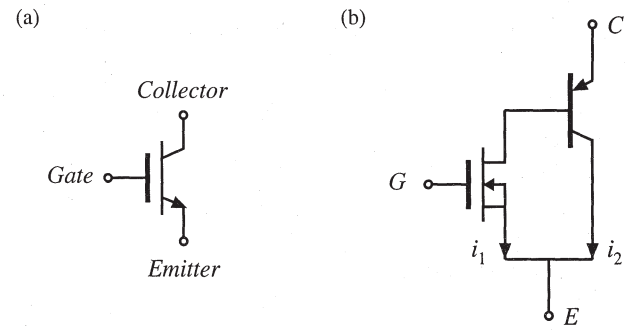


Fig. 4.38 The IGBT: (a) schematic symbol, (b) equivalent circuit.

The function of the added p region is to inject minority charges into the n^- region while the device operates in the on state, as illustrated in Fig. 4.37. When the IGBT conducts, the p–n^- junction is forward-biased, and the minority charges injected into the n^- region cause conductivity modulation. This reduces the on-resistance of the n^- region, and allows high-voltage IGBTs to be constructed which have low forward voltage drops. As of 1999, IGBTs rated as low as 600 V and as high as 3300 V are readily available. The forward voltage drops of these devices are typically 2 to 4 V, much lower than would be obtained in equivalent MOSFETs of the same silicon area.

Several schematic symbols for the IGBT are in current use; the symbol illustrated in Fig. 4.38(a) is the most popular. A two-transistor equivalent circuit for the IGBT is illustrated in Fig. 4.38(b). The IGBT functions effectively as an n-channel power MOSFET, cascaded by a PNP emitter-follower BJT. The physical locations of the two effective devices are illustrated in Fig. 4.39. It can be seen that there are two effective currents: the effective MOSFET channel current i_1, and the effective PNP collector current i_2.

The price paid for the reduced voltage drop of the IGBT is its increased switching times, especially during the turn-off transition. In particular, the IGBT turn-off transition exhibits a phenomenon known as *current tailing*. The effective MOSFET can be turned off quickly, by removing the gate charge such that the gate-to-emitter voltage is negative. This causes the channel current i_1 to quickly become zero. However, the PNP collector current i_2 continues to flow as long as minority charge is present in the n^- region. Since there is no way to actively remove the stored minority charge, it slowly decays via recombination. So i_2 slowly decays in proportion to the minority charge, and a current tail is observed. The length of the current tail can be reduced by introduction of recombination centers in the n^- region, at

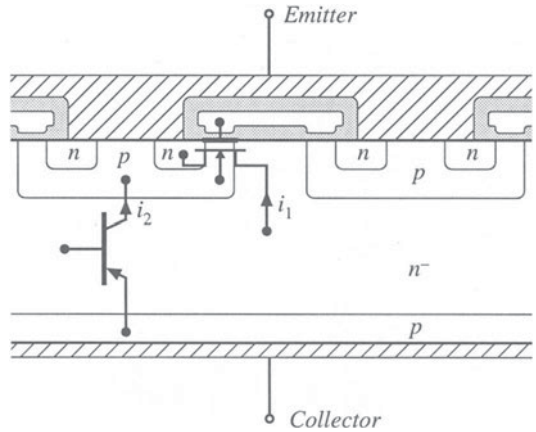


Fig. 4.39 Physical locations of the effective MOSFET and PNP components of the IGBT.

Table 4.3 Characteristics of several commercial IGBTs

Part number	Rated maximum voltage	Rated average current	V_F (typical)	t_f (typical)
Single-chip devices				
HGTP12N60A4	600 V	23 A	2.0 V	70 ns
HGTG32N60E2	600 V	32 A	2.4 V	0.62 μs
HGTG30N120D2	1200 V	30 A	3.2 V	0.58 μs
Multiple-chip modules				
CM400HA-12E	600 V	400 A	2.7 V	0.3 μs
CM300HA-24E	1200 V	300 A	2.7 V	0.3 μs
CM800HA-34H	1700 V	800 A	3.3 V	0.6 μs
High voltage modules				
CM 800HB-50H	2500 V	800 A	3.15 V	1.0 μs
CM 600HB-90H	4500 V	900 A	3.3 V	1.2 μs

the expense of a somewhat increased on-resistance. The current gain of the effective PNP transistor can also be minimized, causing i_1 to be greater than i_2. Nonetheless, the turn-off switching time of the IGBT is significantly longer than that of the MOSFET, with typical turn-off times in the range 0.5 μs to 5 μs. Switching loss induced by IGBT current tailing is discussed in Section 4.3.1. The switching frequencies of PWM converters containing IGBTs are typically in the range 1 to 30 kHz.

The added p–n^- diode junction of the IGBT is not normally designed to block significant voltage. Hence, the IGBT has negligible reverse voltage-blocking capability.

Since the IGBT is a four-layer device, there is the possibility of SCR-type latchup, in which the IGBT cannot be turned off by gate voltage control. Recent devices are not susceptible to this problem. These devices are quite robust, hot-spot and current crowding problems are nonexistent, and the need for external snubber circuits is minimal.

The on-state forward voltage drop of the IGBT can be modeled by a forward-biased diode junction, in series with an effective on-resistance. The temperature coefficient of the IGBT forward voltage drop is complicated by the fact that the diode junction voltage has a negative temperature coefficient, while the on-resistance has a positive temperature coefficient. Fortunately, near rated current the on-resistance dominates, leading to an overall positive temperature coefficient. In consequence, IGBTs can be easily connected in parallel, with a modest current derating. Large modules are commercially available, containing multiple parallel-connected chips.

Characteristics of several commercially available single-chip IGBTs and multiple-chip IGBT modules are listed in Table 4.3.

4.2.5 Thyristors (SCR, GTO, MCT)

Of all conventional semiconductor power devices, the silicon-controlled rectifier (SCR) is the oldest, has the lowest cost per rated kVA, and is capable of controlling the greatest amount of power. Devices having voltage ratings of 5000 to 7000 V and current ratings of several thousand amperes are available. In utility dc transmission line applications, series-connected light-triggered SCRs are employed in inverters and rectifiers that interface the ac utility system to dc transmission lines which carry roughly 1 kA and 1 MV. A single large SCR fills a silicon wafer that is several inches in diameter, and is mounted in a hockey-puck-style case.

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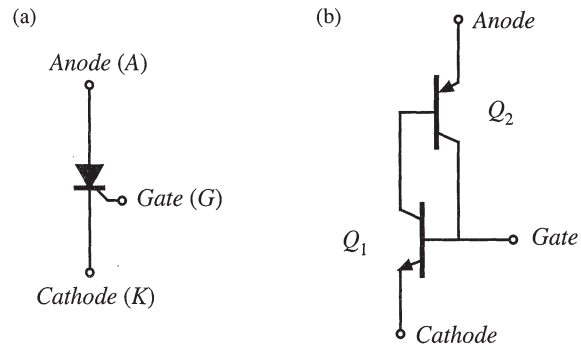


Fig. 4.40 The SCR: (a) schematic symbol, (b) equivalent circuit.

The schematic symbol of the SCR is illustrated in Fig. 4.40(a), and an equivalent circuit containing NPN and PNP BJT devices is illustrated in Fig. 4.40(b). A cross-section of the silicon chip is illustrated in Fig. 4.41. Effective transistor Q_1 is composed of the n, p, and n^- regions, while effective transistor Q_2 is composed of the p, n^-, and p regions as illustrated.

The device is capable of blocking both positive and negative anode-to-cathode voltages. Depending on the polarity of the applied voltage, one of the p–n^- junctions is reverse-biased. In either case, the depletion region extends into the lightly doped n^- region. As with other devices, the desired voltage breakdown rating is obtained by proper design of the n^- region thickness and doping concentration.

The SCR can enter the on state when the applied anode-to-cathode voltage v_{AK} is positive. Positive gate current i_G then causes effective transistor Q_1 to turn on; this in turn supplies base current to effective transistor Q_2, and causes it to turn on as well. The effective connections of the base and collector regions of transistors Q_1 and Q_2 constitute a positive feedback loop. Provided that the product of the current gains of the two transistors is greater than one, then the currents of the transistors will increase regeneratively. In the on state, the anode current is limited by the external circuit, and both effective transistors operate fully saturated. Minority carriers are injected into all four regions, and the resulting conductivity modulation leads to very low forward voltage drop. In the on state, the SCR can be modeled as a forward-biased diode junction in series with a low-value on-resistance. Regardless of the gate current, the SCR is latched in the on state: it cannot be turned off except by application of negative anode current or negative anode-to-cathode voltage. In phase controlled converters, the SCR turns off at the zero crossing of the converter ac input or output waveform. In forced commutation converters, external commuta-

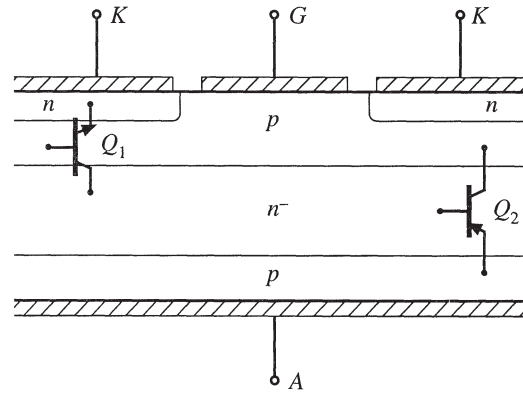


Fig. 4.41 Physical locations of the effective NPN and PNP components of the SCR.

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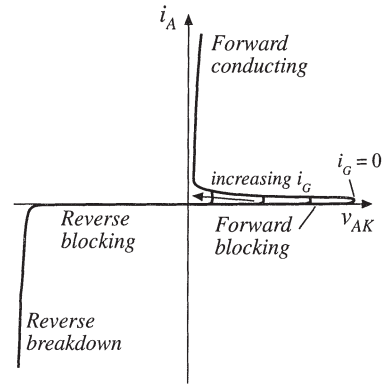


Fig. 4.42 Static i_A–v_{AK} characteristics of the SCR.

tion circuits force the controlled turn-off of the SCR, by reversing either the anode current or the anode-to-cathode voltage.

Static i_A–v_{AK} characteristics of the conventional SCR are illustrated in Fig. 4.42. It can be seen that the SCR is a voltage-bidirectional two-quadrant switch. The turn-on transition is controlled actively via the gate current. The turn-off transition is passive.

During the turn-off transition, the rate at which forward anode-to-cathode voltage is reapplied must be limited, to avoid retriggering the SCR. The turn-off time t_q is the time required for minority stored charge to be actively removed via negative anode current, and for recombination of any remaining minority charge. During the turn-off transition, negative anode current actively removes stored minority charge, with waveforms similar to diode turn-off transition waveforms of Fig. 4.25. Thus, after the first zero crossing of the anode current, it is necessary to wait for time t_q before reapplying positive anode-to-cathode voltage. It is then necessary to limit the rate at which the anode-to-cathode voltage increases, to avoid retriggering the device. Inverter-grade SCRs are optimized for faster switching times, and exhibit smaller values of t_q.

Conventional SCR wafers have large feature size, with coarse or nonexistent interdigitation of the gate and cathode contacts. The parasitic elements arising from this large feature size lead to several limitations. During the turn-on transition, the rate of increase of the anode current must be limited to a safe value. Otherwise, cathode current focusing can occur, which leads to formation of hot spots and device failure.

The coarse feature size of the gate and cathode structure is also what prevents the conventional SCR from being turned off by active gate control. One might apply a negative gate current, in an attempt to actively remove all of the minority stored charge and to reverse-bias the p–n gate-cathode junction. The reason that this attempt fails is illustrated in Fig. 4.43. The large negative gate current flows laterally through the adjoining the p region, inducing a voltage drop as shown. This causes the gate-cathode junction voltage to be smaller near the gate contact, and relatively larger away from the gate contact. The negative gate current is able to reverse-bias only the portion of the gate-cathode junction in the vicinity of the gate contact; the remainder of the gate-cathode junction continues to be forward-biased, and cathode current continues to flow. In effect, the gate contact is able to influence only the nearby portions of the cathode.

The gate turn off thyristor, or GTO, is a modern power device having small feature size. The gate and cathode contacts highly interdigitated, such that the entire gate-cathode p–n junction can be reverse-biased via negative gate current during the turn-off transition. Like the SCR, a single large GTO can fill an entire silicon wafer. Maximum voltage and current ratings of commercial GTOs are lower than those of SCRs.

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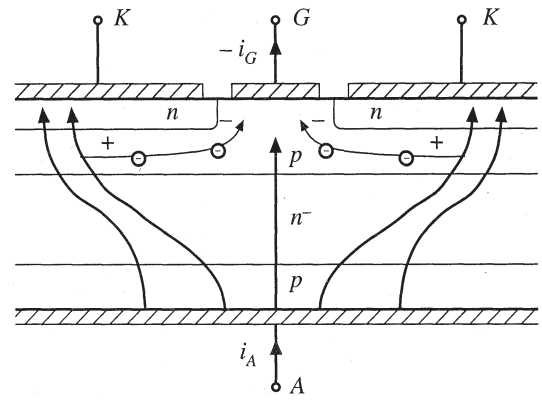


Fig. 4.43 Negative gate current is unable to completely reverse-bias the gate-cathode junction. The anode current focuses away from the gate contact.

The turn-off gain of a GTO is the ratio of on-state current to the negative gate current magnitude required to switch the device off. Typical values of this gain are 2 to 5, meaning that several hundred amperes of negative gate current may be required to turn off a GTO conducting 1000 A. Also of interest is the maximum controllable on-state current. The GTO is able to conduct peak currents significantly greater than the rated average current; however, it may not be possible to switch the device off under gate control while these high peak currents are present.

The MOS-controlled thyristor, or MCT, is a recent power device in which MOSFETs are integrated onto a highly interdigitated SCR, to control the turn-on and turn-off processes. Like the MOSFET and IGBT, the MCT is a single-quadrant device whose turn-on and turn-off transitions are controlled by a MOS gate terminal. Commercial MCTs are *p*-type devices. Voltage-bidirectional two-quadrant MCTs, and *n*-type MCTs, are also possible.

A cross-section of an MCT containing MOSFETs for control of the turn-on and turn-off transitions is illustrated in Fig. 4.44. An equivalent circuit which explains the operation of this structure is given in Fig. 4.45. To turn the device on, the gate-to-anode voltage is driven negative. This forward-biases *p*-channel MOSFET Q_3, forward-biasing the base-emitter junction of BJT Q_1. Transistors Q_1 and Q_2 then latch in the on-state. To turn the device off, the gate-to-anode voltage is driven positive. This forward-biases *n*-channel MOSFET Q_4, which in turn reverse-biases the base-emitter junction of BJT Q_2. The BJTs then turn off. It is important that the on-resistance of the *n*-channel MOSFET be small enough

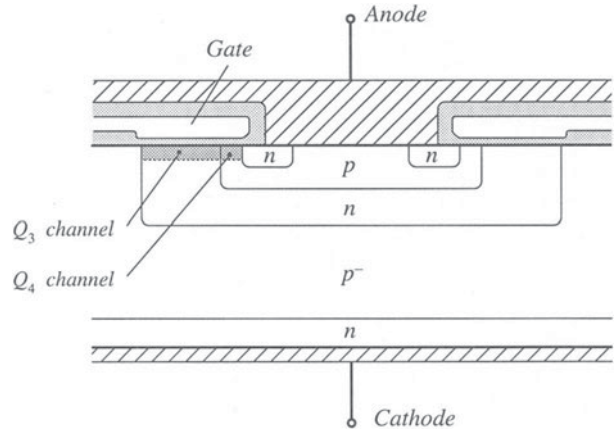


Fig. 4.44 MCT structure. Crosshatched regions are metallized contacts. Lightly shaded regions are insulating silicon dioxide layers.

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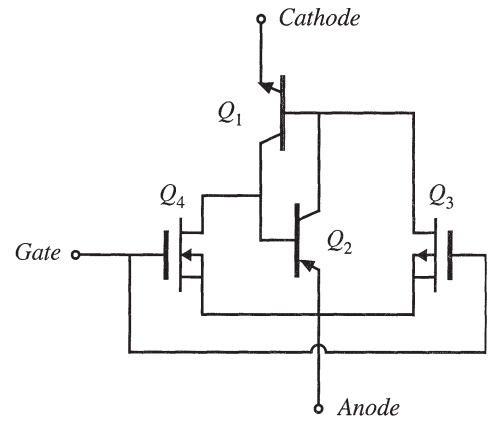


Fig. 4.45 Equivalent circuit for the MCT.

that sufficient influence on the cathode current is exerted—this limits the maximum controllable on state current (i.e., the maximum current that can be interrupted via gate control).

High-voltage MCTs exhibit lower forward voltage drops and higher current densities than IGBTs of similar voltage ratings and silicon area. However, the switching times are longer. Like the GTO, the MCT can conduct considerable surge currents; but again, the maximum current that can be interrupted via gate control is limited. To obtain a reliable turn-off transition, external snubbers are required to limit the peak anode-to-cathode voltage. A sufficiently fast gate-voltage rise time is also required. To some extent, the MCT is still an emerging device—future generations of MCTs may exhibit considerable improvements in performance and ratings.

4.3 SWITCHING LOSS

Having implemented the switches using semiconductor devices, we can now discuss another major source of loss and inefficiency in converters: switching loss. As discussed in the previous section, the turn-on and turn-off transitions of semiconductor devices require times of tens of nanoseconds to microseconds. During these switching transitions, very large instantaneous power loss can occur in the semiconductor devices. Even though the semiconductor switching times are short, the resulting average power loss can be significant.

Semiconductor devices are charge controlled. For example, the conducting state of a MOSFET is determined by the charge on its gate and in its channel, and the conducting state of a silicon diode or a BJT is determined by the presence or absence of stored minority charge in the vicinity of the semiconductor junctions inside the device. To switch a semiconductor device between the on and off states, the controlling charge must be inserted or removed; hence, the amount of controlling charge influences both the switching times and the switching loss. Charge, and energy, are also stored in the output capacitances of semiconductor devices, and energy is stored in the leakage and stray inductances in the circuit. In most converter circuits, these stored energies are also lost during the switching transitions.

In this section the major sources of switching loss are described, and a simple method for estimation of their magnitudes is given. For clarity, conduction losses and semiconductor forward voltage drops are neglected throughout this discussion.

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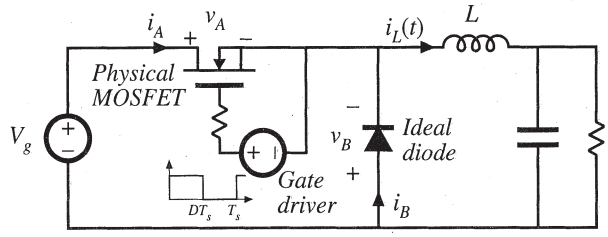


Fig. 4.46 MOSFET driving a clamped inductive load, buck converter example.

4.3.1 Transistor Switching with Clamped Inductive Load

Let's consider first the switching waveforms in the buck converter of Fig. 4.46. Let us treat the diode as ideal, and investigate only the switching loss due to the MOSFET switching times. The MOSFET drain-to-source capacitance is also neglected.

The diode and inductor present a clamped inductive load to the transistor. With such a load, the transistor voltage $v_A(t)$ and current $i_A(t)$ do not change simultaneously. For example, a magnified view of the transistor turn-off-transition waveforms is given in Fig. 4.47. For simplicity, the waveforms are

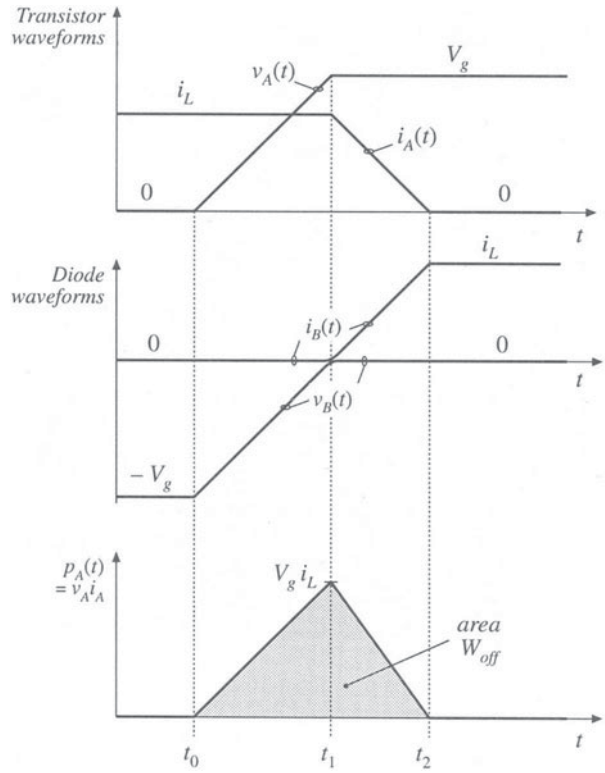


Fig. 4.47 Magnified view of transistor turn-off transition waveforms for the circuit of Fig. 4.46.

approximated as piecewise-linear. The switching times are short, such that the inductor current $i_L(t)$ is essentially constant during the entire switching transition $t_0 < t < t_2$. No current flows through the diode while the diode is reverse-biased, and the diode cannot become forward-biased while its voltage $v_B(t)$ is negative. So first, the voltage $v_A(t)$ across the transistor must rise from zero to V_g. The interval length $(t_1 - t_0)$ is essentially the time required for the gate driver to charge the MOSFET gate-to-drain capacitance. The transistor current $i_A(t)$ is constant and equal to i_L during this interval.

The diode voltage $v_B(t)$ and current $i_B(t)$ are given by

$$\begin{aligned} v_B(t) &= v_A(t) - V_g \\ i_A(t) + i_B(t) &= i_L \end{aligned} \tag{4.6}$$

At time $t = t_1$, when $v_A = V_g$, the diode becomes forward-biased. The current i_L now begins to commute from the transistor to the diode. The interval length $(t_2 - t_1)$ is the time required for the gate driver to discharge the MOSFET gate-to-source capacitance down to the threshold voltage which causes the MOSFET to be in the off state.

The instantaneous power $p_A(t)$ dissipated by the transistor is equal to $v_A(t) i_A(t)$. This quantity is also sketched in Fig. 4.47. The energy W_{off} lost during the transistor turn-off transition is the area under this waveform. With the simplifying assumption that the waveforms are piecewise-linear, then the energy lost is the area of the shaded triangle:

$$W_{off} = \tfrac{1}{2} V_g i_L (t_2 - t_0) \tag{4.7}$$

This is the energy lost during each transistor turn-off transition in the simplified circuit of Fig. 4.46.

The transistor turn-on waveforms of the simplified circuit of Fig. 4.46 are qualitatively similar to those of Fig. 4.47, with the time axis reversed. The transistor current must first rise from 0 to i_L. The diode then becomes reverse-biased, and the transistor voltage can fall from V_g to zero. The instantaneous transistor power dissipation again has peak value $V_g i_L$, and if the waveforms are piecewise linear, then the energy lost during the turn-on transition W_{on} is given by $0.5 V_g i_L$ multiplied by the transistor turn-on time.

Thus, during one complete switching period, the total energy lost during the turn-on and turn-off transitions is $(W_{on} + W_{off})$. If the switching frequency is f_s, then the average power loss incurred due to switching is

$$P_{sw} = \frac{1}{T_s} \int_{\substack{\text{switching} \\ \text{transitions}}} p_A(t)\, dt = \left(W_{on} + W_{off} \right) f_s \tag{4.8}$$

So the switching loss P_{sw} is directly proportional to the switching frequency.

An example where the loss due to transistor switching times is particularly significant is the current tailing phenomenon observed during the turn-off transition of the IGBT. As discussed in Section 4.2.4, current tailing occurs due to the slow recombination of stored minority charge in the n^- region of the IGBT. This causes the collector current to slowly decay after the gate voltage has been removed.

A buck converter circuit containing an ideal diode and nonideal (physical) IGBT is illustrated in Fig. 4.48. Turn-off transition waveforms are illustrated in Fig. 4.49; these waveforms are similar to the MOSFET waveforms of Fig. 4.47. The diode is initially reverse-biased, and the voltage $v_A(t)$ rises from approximately zero to V_g. The interval length $(t_1 - t_0)$ is the time required for the gate drive circuit to charge the IGBT gate-to-collector capacitance. At time $t = t_1$, the diode becomes forward-biased, and current begins to commute from the IGBT to the diode. The interval $(t_2 - t_1)$ is the time required for the gate drive circuit to discharge the IGBT gate-to-emitter capacitance to the threshold value which causes

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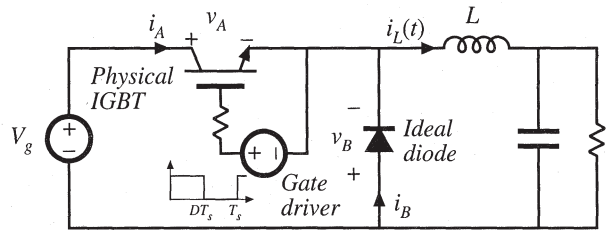


Fig. 4.48 IGBT switching loss example.

the effective MOSFET in Fig. 4.38(b) to be in the off state. This time can be minimized by use of a high-current gate drive circuit which discharges the gate capacitance quickly. However, switching off the effective MOSFET does not completely interrupt the IGBT current $i_A(t)$: current $i_2(t)$ continues to flow through the effective PNP bipolar junction transistor of Fig. 4.38(b) as long as minority carriers continue to exist within its base region. During the interval $t_2 < t < t_3$, the current is proportional to this stored minority charge, and the current tail interval length $(t_3 - t_2)$ is equal to the time required for this remaining stored minority charge to recombine.

The energy W_{off} lost during the turn-off transition of the IGBT is again the area under the instantaneous power waveform, as illustrated in Fig. 4.49. The switching loss can again be evaluated using Eq. (4.8).

The switching times of the IGBT are typically in the vicinity of 0.2 to 2 μs, or several times

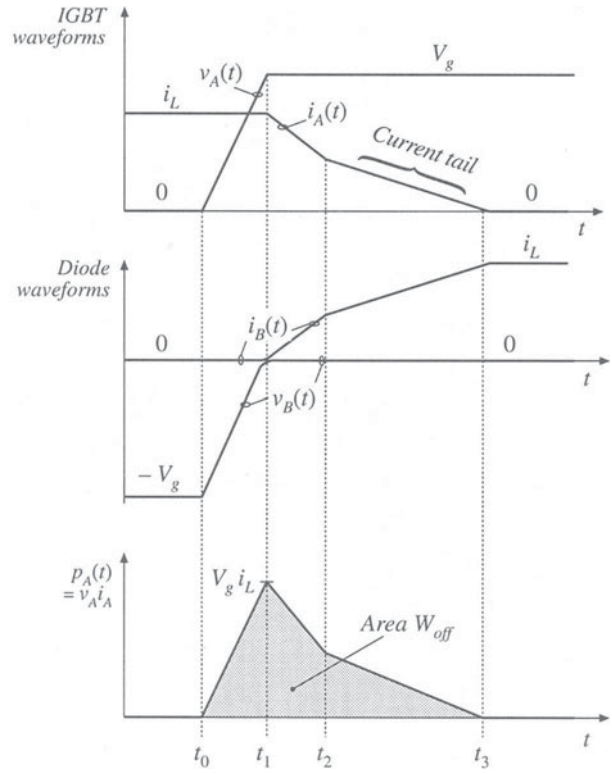


Fig. 4.49 IGBT turn-off transition waveforms for the circuit of Fig. 4.48.

longer than those of the power MOSFET. The resulting switching loss limits the maximum switching frequencies of conventional PWM converters employing IGBTs to roughly 1 to 30 kHz.

4.3.2 Diode Recovered Charge

As discussed previously, the familiar exponential i–v characteristic of the diffused-junction p–n diode is an equilibrium relationship. During switching transients, significant deviations from this characteristic are observed, which can induce transistor switching loss. In particular, during the diode turn-off transient, its stored minority charge must be removed, either actively via negative current $i_B(t)$, or passively via recombination inside the device. The diode remains forward-biased while minority charge is present in the vicinity of the diode semiconductor junction. The initial amount of minority charge is a function of the forward current, and its rate of change, under forward-biased conditions. The turn-off switching time is the time required to remove all of this charge, and to establish a new reverse-biased operating point. This process of switching the diode from the forward-biased to reverse-biased states is called *reverse recovery.*

Again, most diffused-junction power diodes are actually p–n^-–n^+ or p–i–n devices. The lightly doped or intrinsic region (of the diode and other power semiconductor devices as well) allows large breakdown voltages to be obtained. Under steady-state forward-biased conditions, a substantial amount of stored charge is present in this region, increasing its conductivity and leading to a low diode on-resistance. It takes time to insert and remove this charge, however, so there is a tradeoff between high breakdown voltage, low on-resistance, and fast switching times.

To understand how the diode stored charge induces transistor switching loss, let us consider the buck converter of Fig. 4.50. Assume for this discussion that the transistor switching times are much faster than the switching times of the diode, such that the diode reverse recovery mechanism is the only significant source of switching loss. A magnified view of the transistor-turn-on transition waveforms under these conditions is given in Fig. 4.51.

Initially, the diode conducts the inductor current, and hence some amount of stored minority charge is present in the diode. The transistor is initially in the off state. When the transistor turns on, a negative current flows through the diode; this current actively removes some or most of the diode stored minority charge, while the remainder of the minority charge recombines within the diode. The rate of change of the current is typically limited by the package inductance and other stray inductances present in the external circuit; hence, the peak magnitude of the reverse current depends on the external circuit, and can be many times larger than the forward current i_L. The area within the negative portion of the diode current waveform is the recovered stored charge Q_r, while the interval length $(t_2 - t_0)$ is the reverse recovery time t_r. The magnitude of Q_r is a function of the on state forward current i_L at the initiation of the turn-off process, as well as the circuit-limited rate-of-change of the diode current, $di_B(t)/dt$. During

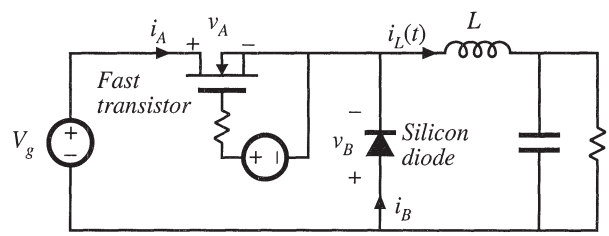


Fig. 4.50 Example, switching loss induced by diode stored charge.

the interval $t_0 < t < t_1$, the diode remains forward-biased, and hence the transistor voltage is V_g. At time $t = t_1$, the stored charge in the vicinity of the p–n^- or p–i junction is exhausted. This junction becomes reverse-biased, and begins to block voltage. During the interval $t_1 < t < t_2$, the diode voltage decreases to $-V_g$. Some negative diode current continues to flow, removing any remaining stored minority charge as well as charging the depletion layer capacitance. At time $t = t_2$, this current is essentially zero, and the diode operates in steady state under reverse-biased conditions.

Diodes in which the interval length $(t_2 - t_1)$ is short compared to $(t_1 - t_0)$ are called abrupt-recovery or "snappy" diodes. Soft recovery diodes exhibit larger values of $(t_2 - t_1)/(t_1 - t_0)$. When significant package and/or stray inductance is present in series with the diode, ringing of the depletion region capacitance with the package and stray inductances may be observed. If severe, this ringing can cause excess reverse voltage that leads to device failure. External R–C snubber circuits are sometimes necessary for reliable operation. The reverse-recovery characteristics of soft recovery diodes are intended to exhibit less ringing and voltage overshoot. Snubbing of these diodes can be reduced or eliminated.

The instantaneous power $p_A(t)$ dissipated in the transistor is also sketched in Fig. 4.51. The energy lost during the turn-on transition is

$$W_D = \int_{\substack{\text{switching}\\ \text{transition}}} v_A(t) i_A(t)\, dt \tag{4.9}$$

For an abrupt-recovery diode in which $(t_2 - t_1) \ll (t_1 - t_0)$, this integral can be evaluated in a simple manner. The transistor voltage $v_A(t)$ is then equal to V_g for essentially the entire diode recovery interval. In addition, $i_A = i_L - i_B$. Equation (4.9) then becomes

$$W_D \approx \int_{\substack{\text{switching}\\ \text{transition}}} V_g \big(i_L - i_B(t)\big)\, dt \tag{4.10}$$

$$= V_g i_L t_r + V_g Q_r$$

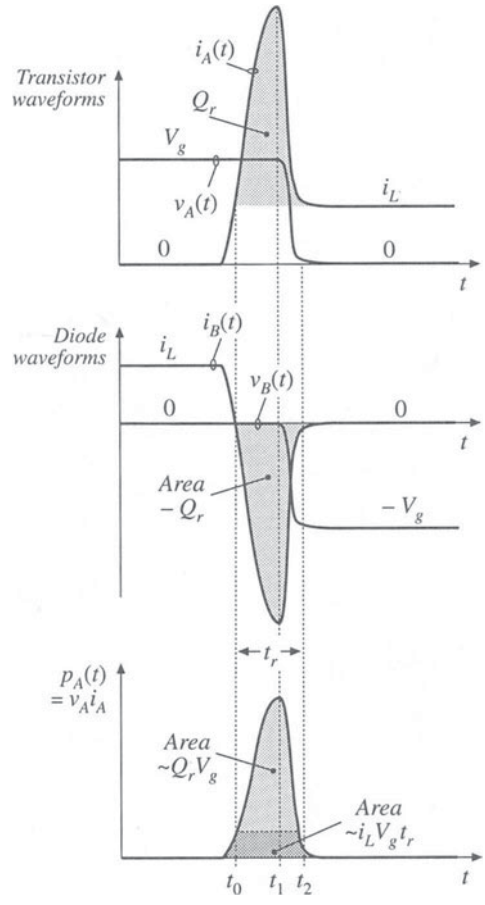


Fig. 4.51 Transistor-turn-on transition waveforms for the circuit of Fig. 4.50.

where the recovered charge Q_r is defined as the integral of the diode current $-i_B(t)$ over the interval $t_0 < t < t_2$. Hence, the diode reverse recovery process leads directly to switching loss $W_D f_s$. This is often the largest single component of switching loss in a conventional switching converter. It can be reduced by use of faster diodes, designed for minimization of stored minority charge.

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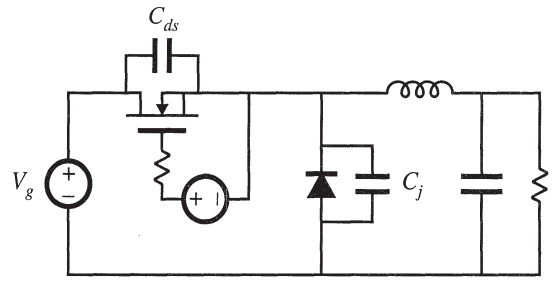


Fig. 4.52 The energy stored in the semiconductor output capacitances is lost during the transistor turn-on transition.

4.3.3 Device Capacitances, and Leakage, Package, and Stray Inductances

Reactive elements can also lead to switching loss. Capacitances that are effectively in parallel with switching elements are shorted out when the switch turns on, and any energy stored in the capacitance is lost. The capacitances are charged without energy loss when the switching elements turn off, and the transistor turn-off loss W_{off} computed in Eq. (4.7) may be reduced. Likewise, inductances that are effectively in series with a switching element lose their stored energy when the switch turns off. Hence, series inductances lead to additional switching loss at turn-off, but can reduce the transistor turn-on loss.

The stored energies of the reactive elements can be summed to find the total energy loss per switching period due to these mechanisms. For linear capacitors and inductors, the stored energy is

$$W_C = \sum_{\substack{\text{capacitive} \\ \text{elements}}} \tfrac{1}{2} C_i V_i^2$$
$$W_L = \sum_{\substack{\text{inductive} \\ \text{elements}}} \tfrac{1}{2} L_j I_j^2 \tag{4.11}$$

A common source of this type of switching loss is the output capacitances of the semiconductor switching devices. The depletion layers of reverse-biased semiconductor devices exhibit capacitance which stores energy. When the transistor turns on, this stored energy is dissipated by the transistor. For example, in the buck converter of Fig. 4.52, the MOSFET exhibits drain-to-source capacitance C_{ds}, and the reverse-biased diode exhibits junction capacitance C_j. During the switching transitions these two capacitances are effectively in parallel, since the dc source V_g is effectively a short-circuit at high frequency. To the extent that the capacitances are linear, the energy lost when the MOSFET turns on is

$$W_C = \tfrac{1}{2}\left(C_{ds} + C_j\right) V_g^2 \tag{4.12}$$

Typically, this type of switching loss is significant at voltage levels above 100 V. The MOSFET gate drive circuit, which must charge and discharge the MOSFET gate capacitances, also exhibits this type of loss.

As noted in Section 4.2.2, the incremental drain-to-source capacitance C_{ds} of the power MOSFET is a strong function of the drain-to-source voltage v_{ds}. $C_{ds}(v_{ds})$ follows an approximate inverse-square-root dependence of v_{ds}, as given by Eq. (4.5). The energy stored in C_{ds} at $v_{ds} = V_{DS}$ is

$$W_{Cds} = \int v_{ds} i_C \, dt = \int_0^{V_{DS}} v_{ds} C_{ds}(v_{ds}) \, dv_{ds} \tag{4.13}$$

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where $i_C = C_{ds}(v_{ds})\, dv_{ds}/dt$ is the current in C_{ds}. Substitution of Eq. (4.5) into (4.13) yields

$$W_{Cds} = \int_0^{V_{DS}} C_0'(v_{ds})\sqrt{v_{ds}}\, dv_{ds} = \tfrac{2}{3}\, C_{ds}(V_{DS})\, V_{DS}^2 \tag{4.14}$$

This energy is lost each time the MOSFET switches on. From the standpoint of switching loss, the drain-to-source capacitance is equivalent to a linear capacitance having the value $\frac{4}{3}C_{ds}(V_{DS})$.

The Schottky diode is essentially a majority-carrier device, which does not exhibit a reverse-recovery transient such as in Fig. 4.51. Reverse-biased Schottky diodes do exhibit significant junction capacitance, however, which can be modeled with a parallel capacitor C_j as in Fig. 4.52, and which leads to energy loss at the transistor turn-on transition.

Common sources of series inductance are transformer leakage inductances in isolated converters (discussed in Chapter 6), as well as the inductances of interconnections and of semiconductor device packages. In addition to generating switching loss, these elements can lead to excessive peak voltage stress during the transistor turn-off transition. Interconnection and package inductances can lead to significant switching loss in high-current applications, and leakage inductance is an important source of switching loss in many transformer-isolated converters.

Diode stored minority charge can induce switching loss in the (nonideal) converter reactive elements. As an example, consider the circuit of Fig. 4.53, containing an ideal voltage source $v_i(t)$, an inductor L, a capacitor C (which may represent the diode junction capacitance, or the junction capacitance in parallel with an external capacitor), and a silicon diode. The diode switching processes of many converters can be modeled by a circuit of this form. Many rectifier circuits containing SCRs exhibit similar waveforms. The voltage source produces the rectangular waveform $v_i(t)$ illustrated in Fig. 4.54. This voltage is initially positive, causing the diode to become forward-biased and the inductor current $i_L(t)$ to increase linearly with slope V_1/L. Since the current is increasing, the stored minority charge inside the diode also increases. At time $t = t_1$, the source voltage $v_i(t)$ becomes negative, and the inductor current decreases with slope $di_L/dt = -V_2/L$. The diode stored charge also decreases, but at a slower rate that depends not only on i_L but also on the minority carrier recombination lifetime of the silicon material in the diode. Hence, at time $t = t_2$, when $i_L(t)$ reaches zero, some stored minority charge remains in the diode. So the diode continues to be forward-biased, and the inductor current continues to decrease with the same slope. The negative current for $t > t_2$ constitutes a reverse diode current, which actively removes diode stored charge. At some time later, $t = t_3$, the diode stored charge in the vicinity of the diode junction becomes zero, and the diode junction becomes reverse-biased. The inductor current is now negative, and must flow through the capacitor. The inductor and capacitor then form a series resonant circuit, which rings with decaying sinusoidal waveforms as shown. This ringing is eventually damped out by the parasitic loss elements of the circuit, such as the inductor winding resistance, inductor core loss, and capacitor equivalent series resistance.

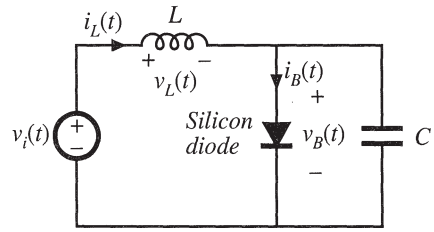


Fig. 4.53 A circuit in which the diode stored charge induces ringing, and ultimately switching loss, in (nonideal) reactive elements.

The diode recovered charge induces loss in this circuit. During the interval $t_2 < t < t_3$, the minority stored charge Q_r recovered from the diode is

$$Q_r = -\int_{t_2}^{t_3} i_L(t)\, dt \tag{4.15}$$

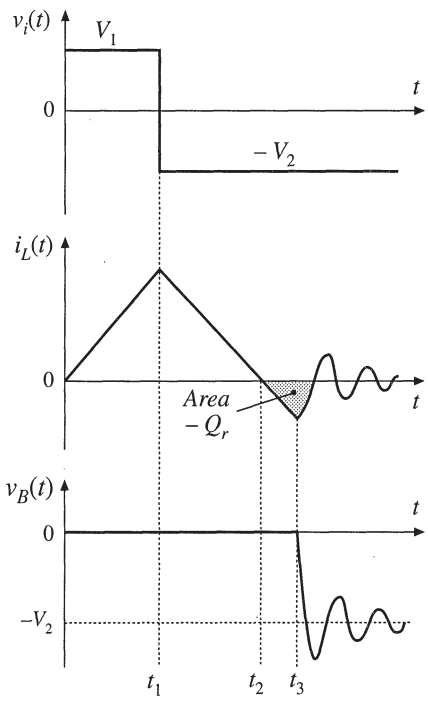


Fig. 4.54 Waveforms of the circuit of Fig. 4.53.

This charge is directly related to the energy stored in the inductor during this interval. The energy W_L stored in the inductor is the integral of the power flowing into the inductor:

$$W_L = \int_{t_2}^{t_3} v_L(t) i_L(t) dt \tag{4.16}$$

During this interval, the applied inductor voltage is

$$v_L(t) = L \frac{di_L(t)}{dt} = -V_2 \tag{4.17}$$

Substitution of Eq. (4.17) into Eq. (4.16) leads to

$$W_L = \int_{t_2}^{t_3} L \frac{di_L(t)}{dt} i_L(t) dt = \int_{t_2}^{t_3} (-V_2) i_L(t) dt \tag{4.18}$$

Evaluation of the integral on the left side yields the stored inductor energy at $t = t_3$, or $Li_L^2(t_3)/2$. The right-side integral is evaluated by noting that V_2 is constant and by substitution of Eq. (4.15), yielding $V_2 Q_r$. Hence, the energy stored in the inductor at $t = t_3$ is

$$W_L = \tfrac{1}{2} L i_L^2(t_3) = V_2 Q_r \tag{4.19}$$

or, the recovered charge multiplied by the source voltage. For $t > t_3$, the ringing of the resonant circuit formed by the inductor and capacitor causes this energy to be circulated back and forth between the inductor and capacitor. If parasitic loss elements in the circuit cause the ringing amplitude to eventually decay to zero, then the energy becomes lost as heat in the parasitic elements.

So diode stored minority charge can lead to loss in circuits that do not contain an active switching element. Also, ringing waveforms that decay before the end of the switching period indicate the presence of switching loss.

4.3.4 Efficiency vs. Switching Frequency

Suppose next that we add up all of the energies lost due to switching, as discussed above:

$$W_{tot} = W_{on} + W_{off} + W_D + W_C + W_L + \ldots \tag{4.20}$$

This is the energy lost in the switching transitions of one switching period. To obtain the average switching power loss, we must multiply by the switching frequency:

$$P_{sw} = W_{tot} f_{sw} \tag{4.21}$$

Other losses in the converter include the conduction losses P_{cond}, modeled and solved as in Chapter 3,

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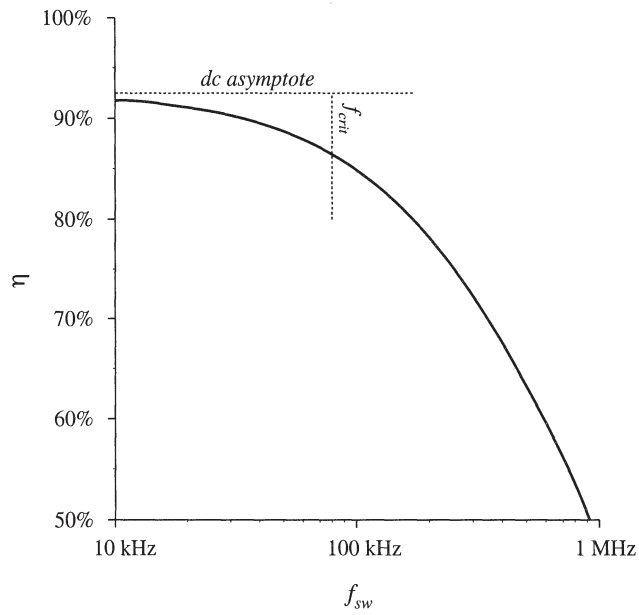


Fig. 4.55 Efficiency vs. switching frequency, based on Eq. (4.22), using arbitrary choices for the values of loss and load power. Switching loss causes the efficiency to decrease rapidly at high frequency.

and other frequency-independent fixed losses P_{fixed}, such as the power required to operate the control circuit. The total loss is therefore

$$P_{loss} = P_{cond} + P_{fixed} + W_{tot} f_{sw} \tag{4.22}$$

which increases linearly with frequency. At the critical frequency

$$f_{crit} = \frac{P_{cond} + P_{fixed}}{W_{tot}} \tag{4.23}$$

the switching losses are equal to the other converter losses. Below this critical frequency, the total loss is dominated by the conduction and fixed loss, and hence the total loss and converter efficiency are not strong functions of switching frequency. Above the critical frequency, the switching loss dominates the total loss, and the converter efficiency decreases rapidly with increasing switching frequency. Typical dependence of the full-load converter efficiency on switching frequency is plotted in Fig. 4.55, for an arbitrary choice of parameter values. The critical frequency f_{crit} can be taken as a rough upper limit on the switching frequency of a practical converter.

4.4 SUMMARY OF KEY POINTS

1. How an SPST ideal switch can be realized using semiconductor devices depends on the polarity of the voltage that the devices must block in the off state, and on the polarity of the current which the devices must conduct in the on state.
2. Single-quadrant SPST switches can be realized using a single transistor or a single diode, depending on the relative polarities of the off state voltage and on state current.

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3. Two-quadrant SPST switches can be realized using a transistor and diode, connected in series (bidirectional-voltage) or in antiparallel (bidirectional-current). Several four-quadrant schemes are also listed here.

4. A "synchronous rectifier" is a MOSFET connected to conduct reverse current, with gate drive control as necessary. This device can be used where a diode would otherwise be required. If a MOSFET with sufficiently low R_{on} is used, reduced conduction loss is obtained.

5. Majority carrier devices, including the MOSFET and Schottky diode, exhibit very fast switching times, controlled essentially by the charging of the device capacitances. However, the forward voltage drops of these devices increases quickly with increasing breakdown voltage.

6. Minority carrier devices, including the BJT, IGBT, and thyristor family, can exhibit high breakdown voltages with relatively low forward voltage drop. However, the switching times of these devices are longer, and are controlled by the times needed to insert or remove stored minority charge.

7. Energy is lost during switching transitions, owing to a variety of mechanisms. The resulting average power loss, or switching loss, is equal to this energy loss multiplied by the switching frequency. Switching loss imposes an upper limit on the switching frequencies of practical converters.

8. The diode and inductor present a "clamped inductive load" to the transistor. When a transistor drives such a load, it experiences high instantaneous power loss during the switching transitions. An example where this leads to significant switching loss is the IGBT and the "current tail" observed during its turn-off transition.

9. Other significant sources of switching loss include diode stored charge and energy stored in certain parasitic capacitances and inductances. Parasitic ringing also indicates the presence of switching loss.

REFERENCES

[1] R. D. MIDDLEBROOK, S. ĆUK, and W. BEHEN, "A New Battery Charger/Discharger Converter," *IEEE Power Electronics Specialists Conference*, 1978 Record, pp. 251-255, June 1978.

[2] H. MATSUO and F. KUROKAWA, "New Solar Cell Power Supply System Using a Boost Type Bidirectional Dc-Dc Converter," *IEEE Power Electronics Specialists Conference*, 1982 Record, pp. 14-19, June 1982.

[3] M. VENTURINI, "A New Sine-Wave-In Sine-Wave-Out Conversion Technique Eliminates Reactive Elements," *Proceedings Seventh International Solid-State Power Conversion Conference* (Powercon 7), pp. E3.1-E3.13, 1980.

[4] K. D. T. NGO, S. ĆUK, and R. D. MIDDLEBROOK, "A New Flyback Dc-to-Three-Phase Converter with Sinusoidal Outputs," *IEEE Power Electronics Specialists Conference*, 1983 Record, pp. 377–388.

[5] S. ĆUK, "Basics of Switched-Mode Power Conversion: Topologies, Magnetics, and Control," *Advances in Switched-Mode Power Conversion*, Vol. II, Irvine CA: Teslaco, pp. 279-310, 1983.

[6] L. GYUGI and B. PELLY, *Static Power Frequency Changers: Theory, Performance, and Applications*, New York: Wiley-Interscience, 1976.

[7] R. S. KAGAN and M. CHI, "Improving Power Supply Efficiency with MOSFET Synchronous Rectifiers," *Proceedings Ninth International Solid-State Power Conversion Conference* (Powercon 9), pp. D4.1-D4.9, July 1982.

[8] R. BLANCHARD and P. E. THIBODEAU, "The Design of a High Efficiency, Low Voltage Power Supply Using MOSFET Synchronous Rectification and Current Mode Control," *IEEE Power Electronics Special-*

DELTA ELECTRONICS EX. 1008
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ists Conference, 1985 Record, pp. 355-361, June 1985.

[9] N. MOHAN, T. UNDELAND, and W. ROBBINS, *Power Electronics: Converters, Applications, and Design*, 2nd edit., New York: John Wiley & Sons, 1995, Chapters 19-26.

[10] C. L. MA and P. O. LAURITZEN, "A Simple Power Diode Model with Forward and Reverse Recovery," *IEEE Power Electronics Specialists Conference*, 1991 Record, pp. 411-415, June 1991.

[11] M. SCHLECHT and L. CASEY, "A Comparison of the Square Wave and Quasi-Resonant Topologies," *IEEE Applied Power Electronics Conference*, 1987 Record, pp. 124-134, March 1987.

[12] B. J. BALIGA, *Modern Power Devices*, New York: John Wiley & Sons, 1987.

[13] P. GRAY, D. DEWITT, A. BOOTHROYD, and J. GIBBONS, *Physical Electronics and Circuit Models of Transistors*, Semiconductor Electronics Education Committee, Vol. 2, New York: John Wiley & Sons, 1964.

[14] E. OXNER, *Power FETs and Their Applications*, Englewood, New Jersey: Prentice-Hall, 1982.

[15] M. RASHID, *Power Electronics: Circuits, Devices, and Applications*, 2nd edit., Englewood, New Jersey: Prentice Hall, 1993, Chapters 3, 4, and 8.

[16] B. J. BALIGA, M. S. ADLER, R. P. LOVE, P. V. GRAY, and N. D. ZAMMER, "The Insulated Gate Transistor —A New Three Terminal MOS-Controlled Bipolar Power Device," *IEEE Transactions on Electron Devices*, Vol. 31, No. 6, pp. 821-828, June 1984.

[17] V. TEMPLE, "MOS-Controlled Thyristors—A New Class of Power Devices," *IEEE Transactions on Electron Devices*, Vol. 33, No. 10, pp. 1609-1618, October 1986.

[18] S. SUL, F. PROFUMO, G. CHO, and T. LIPO, "MCTs and IGBTs: A Comparison of Performance in Power Electronics Circuits," *IEEE Power Electronics Specialists Conference*, 1989 Record, pp. 163-169, June 1989.

[19] V. TEMPLE, S. ARTHUR, D. WATROUS, R. DE DONCKER, and H. METHA, "Megawatt MOS Controlled Thyristor for High Voltage Power Circuits," *IEEE Power Electronics Specialists Conference*, 1992 Record, pp. 1018-1025, June 1992.

PROBLEMS

In Problems 4.1 to 4.6, the input voltage V_g is dc and positive with the polarity shown. Specify how to implement the switches using a minimal number of diodes and transistors, such that the converter operates over the entire range of duty cycles $0 \le D \le 1$. The switch states should vary as shown in Fig. 4.56. You may assume that the inductor current ripples and capacitor voltage ripples are small.

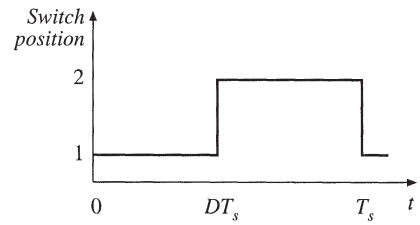


Fig. 4.56 Switch control method for Problems 4.1 to 4.6.

For each problem, do the following:

(a) Realize the switches using SPST ideal switches, and explicitly define the voltage and current of each switch.

(b) Express the on-state current and off-state voltage of each SPST switch in terms of the converter inductor currents, capacitor voltages, and/or

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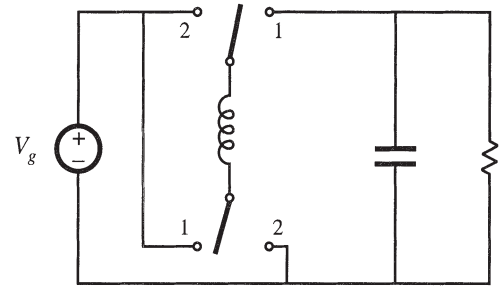
input source voltage.

(c) Solve the converter to determine the inductor currents and capacitor voltages, as in Chapter 2.

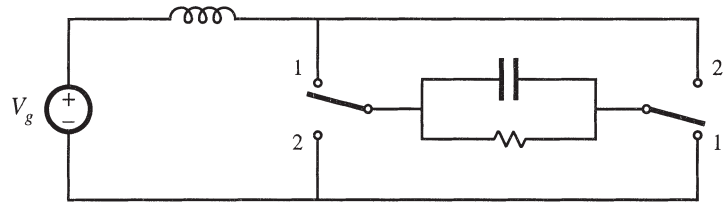
(d) Determine the polarities of the switch on-state currents and off-state voltages. Do the polarities vary with duty cycle?

(e) State how each switch can be realized using transistors and/or diodes, and whether the realization requires single-quadrant, current-bidirectional two-quadrant, voltage-bidirectional two-quadrant, or four-quadrant switches.

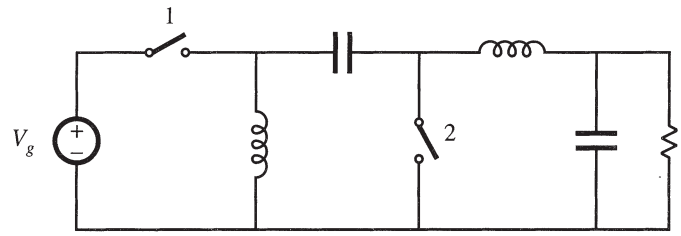
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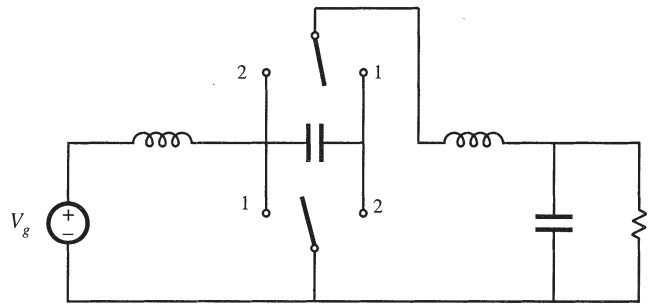
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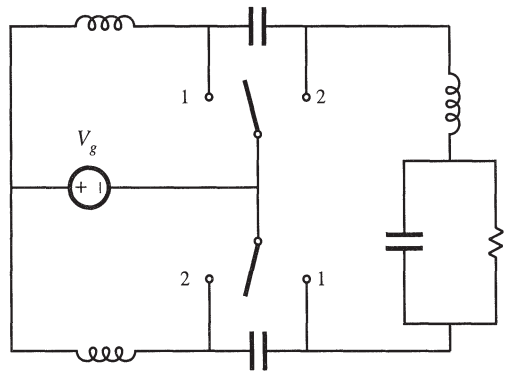
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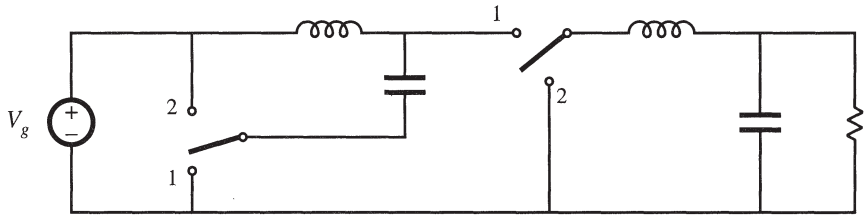
4.4



4.5



4.6



4.7 An IGBT and a silicon diode operate in a buck converter, with the IGBT waveforms illustrated in Fig. 4.57. The converter operates with input voltage $V_g = 400$ V, output voltage $V = 200$ V, and load current $I = 10$ A.

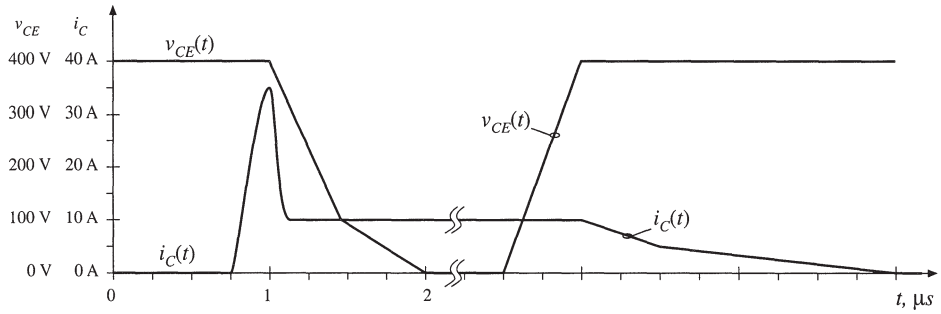


Fig. 4.57 IGBT voltage and current waveforms, Problem 4.7.

(a) Estimate the total energy lost during the switching transitions.

(b) The forward voltage drop of the IGBT is 2.5 V, and the diode has forward voltage drop 1.5 V. All other sources of conduction loss and fixed loss can be neglected. Estimate the semiconductor conduction loss.

(c) Sketch the converter efficiency over the range of switching frequencies 1 kHz $\leq f_s \leq$ 100 kHz, and label numerical values.

4.8 Two MOSFETs are employed as current-bidirectional two-quadrant switches in a bidirectional battery charger/discharger based on the dc-dc buck converter. This converter interfaces a 16 V battery to a 28 V main power bus. The maximum battery current is 40 A. The MOSFETs have on-resistances of 35 mΩ.

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Their body diodes have forward voltage drops of 1.0 V, and exhibit recovered charge Q_r of 25 μC and reverse recovery times t_r of 200 ns in the given circuit. You may assume that all diodes in this problem have "snappy" reverse recovery characteristics, and also assume that diode stored charge is the dominant cause of switching loss in this circuit. You may neglect all losses other than the semiconductor conduction losses and the switching loss induced by diode stored charge.

The current-bidirectional two-quadrant switches are realized as in Fig. 4.10(a), utilizing the MOSFET body diodes.

(a) Estimate the switching energy loss, conduction loss, and converter efficiency, when the battery is being charged at the maximum rate. The switching frequency is 100 kHz.

External diodes are now added as illustrated in Fig. 4.10(b). These diodes have forward voltage drops of 1.0 V, and exhibit recovered charge Q_r of 5 μC and reverse recovery times t_r of 40 ns in the given circuit.

(b) Repeat the analysis of Part (a), for this case.

(c) Over what range of switching frequencies does the addition of the external diodes improve the converter efficiency?

4.9 A switching converter operates with a switching frequency of 100 kHz. The converter waveforms exhibit damped sinusoidal ringing, initiated by the transistor turn-off transition, which decays slowly but eventually reaches zero before the end of the switching period. This ringing occurs in a series resonant circuit formed by parasitic inductances and capacitances in the circuit. The frequency of the ringing is 5 MHz. During the first period of sinusoidal ringing, the ac inductor current reaches a peak magnitude of 0.5 A, and the ac capacitor voltage reaches a peak magnitude of 200 V. Determine the following quantities:

(a) the value of the total parasitic inductance,

(b) the value of the total parasitic capacitance,

(c) the energy lost per switching period, associated with this ringing, and

(d) the switching loss associated with this ringing.

(e) Derive a general expression for the switching loss, as a function of the switching frequency, ringing frequency, and the ringing voltage and current peak magnitudes during the first period of ringing.

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5

The Discontinuous Conduction Mode

When the ideal switches of a dc-dc converter are implemented using current-unidirectional and/or voltage-unidirectional semiconductor switches, one or more new modes of operation known as *discontinuous conduction modes* (DCM) can occur. The discontinuous conduction mode arises when the switching ripple in an inductor current or capacitor voltage is large enough to cause the polarity of the applied switch current or voltage to reverse, such that the current- or voltage-unidirectional assumptions made in realizing the switch with semiconductor devices are violated. The DCM is commonly observed in dc–dc converters and rectifiers, and can also sometimes occur in inverters or in other converters containing two-quadrant switches.

The discontinuous conduction mode typically occurs with large inductor current ripple in a converter operating at light load and containing current-unidirectional switches. Since it is usually required that converters operate with their loads removed, DCM is frequently encountered. Indeed, some converters are purposely designed to operate in DCM for all loads.

The properties of converters change radically in the discontinuous conduction mode. The conversion ratio M becomes load-dependent, and the output impedance is increased. Control of the output may be lost when the load is removed. We will see in a later chapter that the converter dynamics are also significantly altered.

In this chapter, the origins of the discontinuous conduction mode are explained, and the mode boundary is derived. Techniques for solution of the converter waveforms and output voltage are also described. The principles of inductor volt-second balance and capacitor charge balance must always be true in steady state, regardless of the operating mode. However, application of the small ripple approximation requires some care, since the inductor current ripple (or one of the inductor current or capacitor voltage ripples) is not small.

Buck and boost converters are solved as examples. Characteristics of the basic buck, boost, and buck-boost converters are summarized in tabular form.

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5.1 ORIGIN OF THE DISCONTINUOUS CONDUCTION MODE, AND MODE BOUNDARY

Let us consider how the inductor and switch current waveforms change as the load power is reduced. Let's use the buck converter (Fig. 5.1) as a simple example. The inductor current $i_L(t)$ and diode current $i_D(t)$ waveforms are sketched in Fig. 5.2 for the continuous conduction mode. As described in Chapter 2, the inductor current waveform contains a dc component I, plus switching ripple of peak amplitude Δi_L. During the second subinterval, the diode current is identical to the inductor current. The minimum diode current during the second subinterval is equal to $(I - \Delta i_L)$; since the diode is a single-quadrant switch, operation in the continuous conduction mode requires that this current remain positive. As shown in Chapter 2, the inductor current dc component I is equal to the load current:

$$I = \frac{V}{R} \tag{5.1}$$

since no dc current flows through capacitor C. It can be seen that I depends on the load resistance R. The

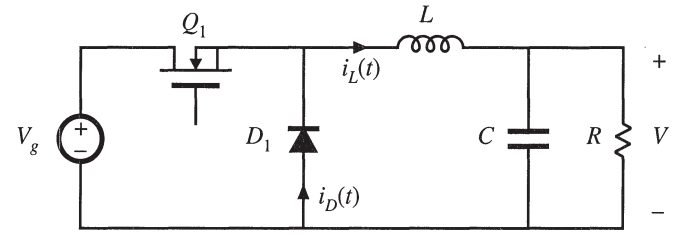


Fig. 5.1 Buck converter example.

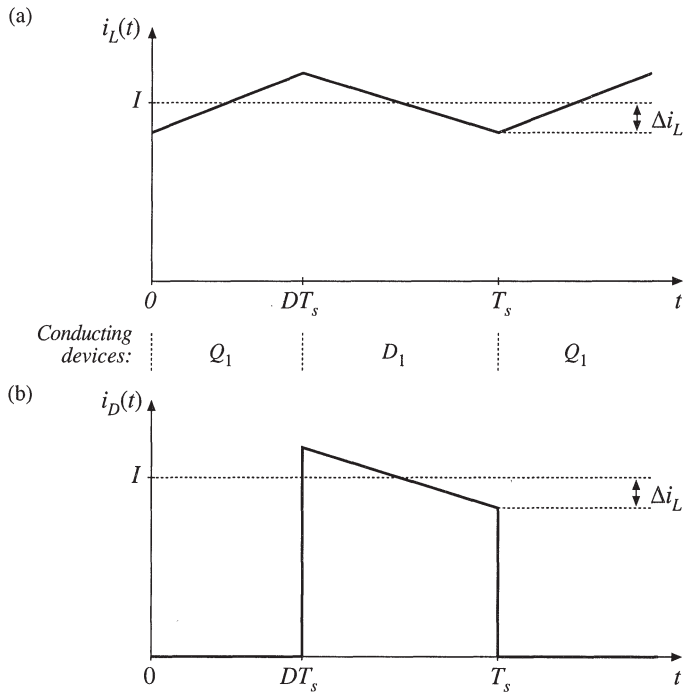


Fig. 5.2 Buck converter waveforms in the continuous conduction mode: (a) inductor current $i_L(t)$, (b) diode current $i_D(t)$.

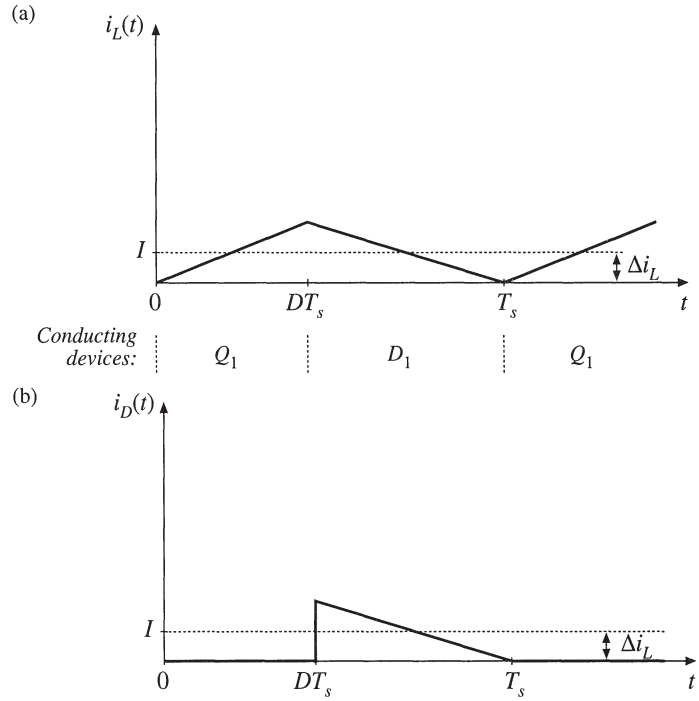


Fig. 5.3 Buck converter waveforms at the boundary between the continuous and discontinuous conduction modes: (a) inductor current $i_L(t)$, (b) diode current $i_D(t)$.

switching ripple peak amplitude is:

$$\Delta i_L = \frac{\left(V_g - V\right)}{2L} DT_s = \frac{V_g DD'T_s}{2L} \tag{5.2}$$

The ripple magnitude depends on the applied voltage $(V_g - V)$, on the inductance L, and on the transistor conduction time DT_s. But it does not depend on the load resistance R. The inductor current ripple magnitude varies with the applied voltages rather than the applied currents.

Suppose now that the load resistance R is increased, so that the dc load current is decreased. The dc component of inductor current I will then decrease, but the ripple magnitude Δi_L will remain unchanged. If we continue to increase R, eventually the point is reached where $I = \Delta i_L$, illustrated in Fig. 5.3. It can be seen that the inductor current $i_L(t)$ and the diode current $i_D(t)$ are both zero at the end of the switching period. Yet the load current is positive and nonzero.

What happens if we continue to increase the load resistance R? The diode current cannot be negative; therefore, the diode must become reverse-biased before the end of the switching period. As illustrated in Fig. 5.4, there are now three subintervals during each switching period T_s. During the first subinterval of length D_1T_s the transistor conducts, and the diode conducts during the second subinterval of length D_2T_s. At the end of the second subinterval the diode current reaches zero, and for the remainder of the switching period neither the transistor nor the diode conduct. The converter operates in the discontinuous conduction mode.

Figure 5.3 suggests a way to find the boundary between the continuous and discontinuous conduction modes. It can be seen that, for this buck converter example, the diode current is positive over the entire interval $DT_s < t < T_s$ provided that $I > \Delta i_L$. Hence, the conditions for operation in the continuous and discontinuous conduction modes are:

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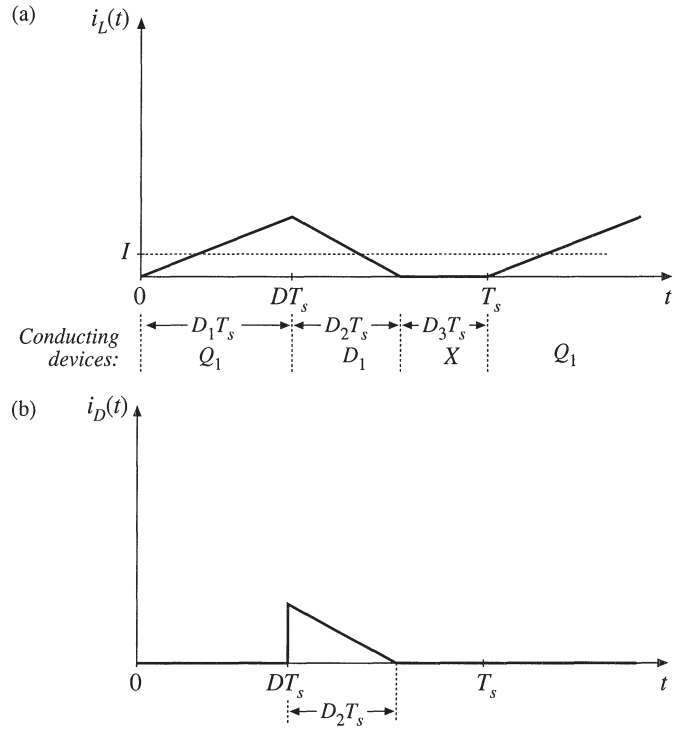


Fig. 5.4 Buck converter waveforms in the discontinuous conduction mode: (a) inductor current $i_L(t)$, (b) diode current $i_D(t)$.

$$\begin{aligned} I &> \Delta i_L \quad \text{for CCM} \\ I &< \Delta i_L \quad \text{for DCM} \end{aligned} \tag{5.3}$$

where I and Δi_L are found assuming that the converter operates in the continuous conduction mode. Insertion of Eqs. (5.1) and (5.2) into Eq. (5.3) yields the following condition for operation in the discontinuous conduction mode:

$$\frac{DV_g}{R} < \frac{DD'T_sV_g}{2L} \tag{5.4}$$

Simplification leads to

$$\frac{2L}{RT_s} < D' \tag{5.5}$$

This can also be expressed

$$K < K_{crit}(D) \quad \text{for DCM} \tag{5.6}$$

where

$$K = \frac{2L}{RT_s} \qquad \text{and} \qquad K_{crit}(D) = D'$$

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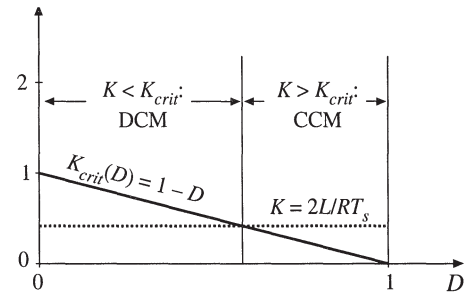


Fig. 5.5 Buck converter $K_{crit}(D)$ vs. D. The converter operates in CCM when $K > K_{crit}$, and in DCM when $K < K_{crit}$.

The dimensionless parameter K is a measure of the tendency of a converter to operate in the discontinuous conduction mode. Large values of K lead to continuous mode operation, while small values lead to the discontinuous mode for some values of duty cycle. The critical value of K at the boundary between modes, $K_{crit}(D)$, is a function of duty cycle, and is equal to D' for the buck converter.

The critical value $K_{crit}(D)$ is plotted vs. duty cycle D in Fig. 5.5. An arbitrary choice of K is also illustrated. For the values shown, it can be seen that the converter operates in DCM at low duty cycle, and in CCM at high duty cycle. Figure 5.6 illustrates what happens with heavier loading. The load resistance R is reduced in value, such that K is larger. If K is greater than one, then the converter operates in the continuous conduction mode for all duty cycles.

It is natural to express the mode boundary in terms of the load resistance R, rather than the dimensionless parameter K. Equation (5.6) can be rearranged to directly expose the dependence of the mode boundary on the load resistance:

$$\begin{aligned} R &< R_{crit}(D) \quad \text{for CCM} \\ R &> R_{crit}(D) \quad \text{for DCM} \end{aligned} \tag{5.7}$$

where

$$R_{crit}(D) = \frac{2L}{D'T_s}$$

So the converter enters the discontinuous conduction mode when the load resistance R exceeds the critical value R_{crit}. This critical value depends on the inductance, the switching period, and the duty cycle. Note that, since $D' \leq 1$, the minimum value of R_{crit} is $2L/T_s$. Therefore, if $R < 2L/T_s$, then the converter will operate in the continuous conduction mode for all duty cycles.

These results can be applied to loads that are not pure linear resistors. An effective load resis-

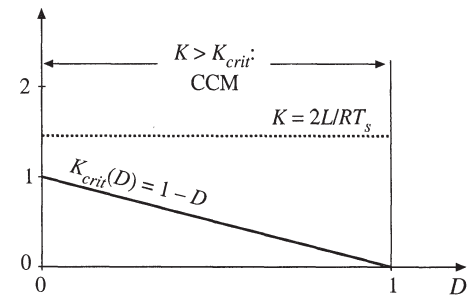


Fig. 5.6 Comparison of K with $K_{crit}(D)$, for a larger value of K. Since $K > 1$, the converter operates in CCM for all D.

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Table 5.1 CCM-DCM mode boundaries for the buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	$\max_{0 \le D \le 1} (K_{crit})$	$R_{crit}(D)$	$\min_{0 \le D \le 1} (R_{crit})$
Buck	$(1-D)$	1	$\frac{2L}{(1-D)T_s}$	$2\frac{L}{T_s}$
Boost	$D(1-D)^2$	$\frac{4}{27}$	$\frac{2L}{D(1-D)^2 T_s}$	$\frac{27}{2}\frac{L}{T_s}$
Buck–boost	$(1-D)^2$	1	$\frac{2L}{(1-D)^2 T_s}$	$2\frac{L}{T_s}$

tance R is defined as the ratio of the dc output voltage to the dc load current: $R = V/I$. This effective load resistance is then used in the above equations.

A similar mode boundary analysis can be performed for other converters. The boost converter is analyzed in Section 5.3, while analysis of the buck-boost converter is left as a homework problem. The results are listed in Table 5.1, for the three basic dc–dc converters. In each case, the dimensionless parameter K is defined as $K = 2L/RT_s$, and the mode boundary is given by

$$\begin{aligned} K &> K_{crit}(D) \quad \text{or} \quad R < R_{crit}(D) \quad \text{for CCM} \\ K &< K_{crit}(D) \quad \text{or} \quad R > R_{crit}(D) \quad \text{for DCM} \end{aligned} \tag{5.8}$$

5.2 ANALYSIS OF THE CONVERSION RATIO $M(D, K)$

With a few modifications, the same techniques and approximations developed in Chapter 2 for the steady-state analysis of the continuous conduction mode may be applied to the discontinuous conduction mode.

(a) *Inductor volt-second balance.* The dc component of the voltage applied to an inductor must be zero:

$$\langle v_L \rangle = \frac{1}{T_s}\int_0^{T_s} v_L(t)\,dt = 0 \tag{5.9}$$

(b) *Capacitor charge balance.* The dc component of current applied to a capacitor must be zero:

$$\langle i_C \rangle = \frac{1}{T_s}\int_0^{T_s} i_C(t)\,dt = 0 \tag{5.10}$$

These principles must be true for any circuit that operates in steady state, regardless of the operating mode.

(c) *The linear ripple approximation.* Care must be used when employing the linear ripple approximation in the discontinuous conduction mode.

(*i*) *Output capacitor voltage ripple.* Regardless of the operating mode, it is required that the output voltage ripple be small. Hence, for a well-designed converter operating in the discontinuous conduction mode, the peak output voltage ripple Δv should be much smaller in magnitude than the output voltage dc component V. So the linear ripple approximation applies to the output voltage waveform:

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$$v(t) \approx V \tag{5.11}$$

(*ii*) *Inductor current ripple.* By definition, the inductor current ripple is not small in the discontinuous conduction mode. Indeed, Eq. (5.3) states that the inductor current ripple Δi_L is greater in magnitude than the dc component I. So neglecting the inductor current ripple leads to inaccurate results. In other converters, several inductor currents, or a capacitor voltage, may contain large switching ripple which should not be neglected.

The equations necessary for solution of the voltage conversion ratio can be obtained by invoking volt-second balance for each inductor voltage, and charge balance for each capacitor current, in the network. The switching ripple is ignored in the output capacitor voltage, but the inductor current switching ripple must be accounted for in this buck converter example.

Let us analyze the conversion ratio $M = V/V_g$ of the buck converter of Eq. (5.1). When the transistor conducts, for $0 < t < D_1 T_s$, the converter circuit reduces to the network of Fig. 5.7(a). The inductor voltage and capacitor current are given by

$$\begin{aligned} v_L(t) &= V_g - v(t) \\ i_C(t) &= i_L(t) - \frac{v(t)}{R} \end{aligned} \tag{5.12}$$

By making the linear ripple approximation, to ignore the output capacitor voltage ripple, one obtains

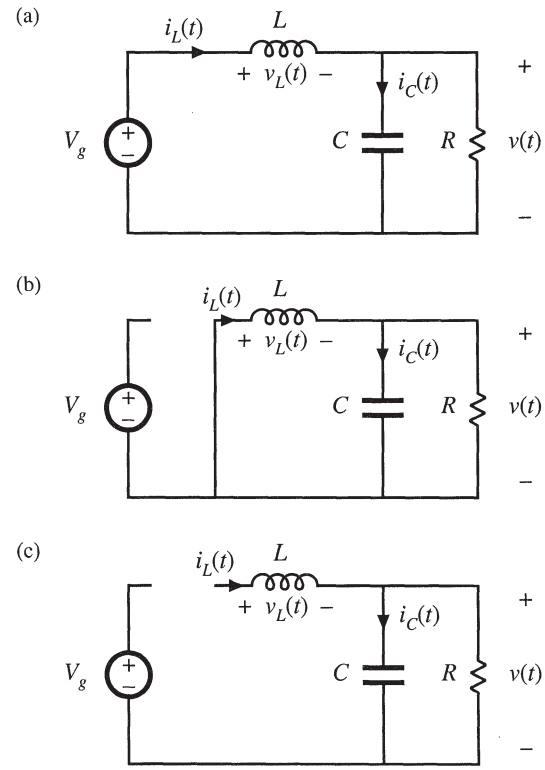


Fig. 5.7 Buck converter circuits for operation in the discontinuous conduction mode: (a) during subinterval 1, (b) during subinterval 2, (c) during subinterval 3.

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$$\begin{aligned} v_L(t) &\approx V_g - V \\ i_C(t) &\approx i_L(t) - \frac{V}{R} \end{aligned} \tag{5.13}$$

Note that the inductor current ripple has not been ignored.

The diode conducts during subinterval 2, $D_1T_s < t < (D_1 + D_2)T_s$. The circuit then reduces to Fig. 5.7(b). The inductor voltage and capacitor current are given by

$$\begin{aligned} v_L(t) &= -v(t) \\ i_C(t) &= i_L(t) - \frac{v(t)}{R} \end{aligned} \tag{5.14}$$

By neglecting the ripple in the output capacitor voltage, one obtains

$$\begin{aligned} v_L(t) &\approx -V \\ i_C(t) &\approx i_L(t) - \frac{V}{R} \end{aligned} \tag{5.15}$$

The diode becomes reverse-biased at time $t = (D_1 + D_2)T_s$. The circuit is then as shown in Fig. 5.7(c), with both transistor and diode in the off state. The inductor voltage and inductor current are both zero for the remainder of the switching period $(D_1 + D_2)T_s < t < T_s$. The network equations for the third subinterval are given by

$$\begin{aligned} v_L &= 0, \quad i_L = 0 \\ i_C(t) &= i_L(t) - \frac{v(t)}{R} \end{aligned} \tag{5.16}$$

Note that the inductor current is constant and equal to zero during the third subinterval, and therefore the inductor voltage must also be zero in accordance with the relationship $v_L(t) = L\, di_L(t)/dt$. In practice, parasitic ringing is observed during this subinterval. This ringing occurs owing to the resonant circuit formed by the inductor and the semiconductor device capacitances, and typically has little influence on the converter steady-state properties. Again ignoring the output capacitor voltage ripple, one obtains

$$\begin{aligned} v_L(t) &= 0 \\ i_C(t) &= -\frac{V}{R} \end{aligned} \tag{5.17}$$

Equations (5.13), (5.15), and (5.17) can now be used to plot the inductor voltage waveform as in Fig. 5.8. According to the principle of inductor volt-second balance, the dc component of this waveform must be zero. Since the waveform is rectangular, its dc component (or average value) is easily evaluated:

$$\langle v_L(t) \rangle = D_1\left(V_g - V\right) + D_2\left(-V\right) + D_3\left(0\right) = 0 \tag{5.18}$$

Solution for the output voltage yields

$$V = V_g \frac{D_1}{D_1 + D_2} \tag{5.19}$$

The transistor duty cycle D (which coincides with the subinterval 1 duty cycle D_1) is the control input to the converter, and can be considered known. But the subinterval 2 duty cycle D_2 is unknown, and hence

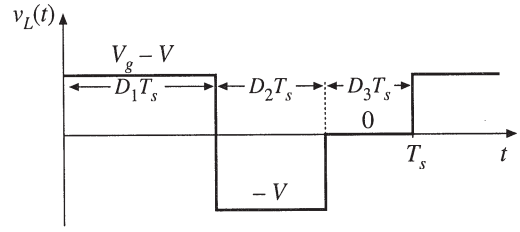


Fig. 5.8 Inductor voltage waveform $v_L(t)$, buck converter operating in discontinuous conduction mode.

another equation is needed to eliminate D_2 and solve for the output voltage V.

The second equation is obtained by use of capacitor charge balance. The connection of the capacitor to its adjacent components is detailed in Fig. 5.9. The node equation of this network is

$$i_L(t) = i_C(t) + \frac{v(t)}{R} \tag{5.20}$$

By capacitor charge balance, the dc component of capacitor current must be zero:

$$\langle i_C \rangle = 0 \tag{5.21}$$

Therefore, the dc load current must be supplied entirely by the other elements connected to the node. In particular, for the case of the buck converter, the dc component of inductor current must be equal to the dc load current:

$$\langle i_L \rangle = \frac{V}{R} \tag{5.22}$$

So we need to compute the dc component of the inductor current.

Since the inductor current ripple is not small, determination of the inductor current dc component requires that we examine the current waveform in detail. The inductor current waveform is sketched in Fig. 5.10. The current begins the switching period at zero, and increases during the first subinterval with a constant slope, given by the applied voltage divided by the inductance. The peak inductor current i_{pk} is equal to the constant slope, multiplied by the length of the first subinterval:

$$i_L(D_1T_s) = i_{pk} = \frac{V_g - V}{L} D_1T_s \tag{5.23}$$

The dc component of the inductor current is again the average value:

$$\langle i_L \rangle = \frac{1}{T_s} \int_0^{T_s} i_L(t)\,dt \tag{5.24}$$

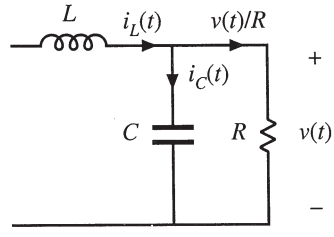


Fig. 5.9 Connection of the output capacitor to adjacent components.

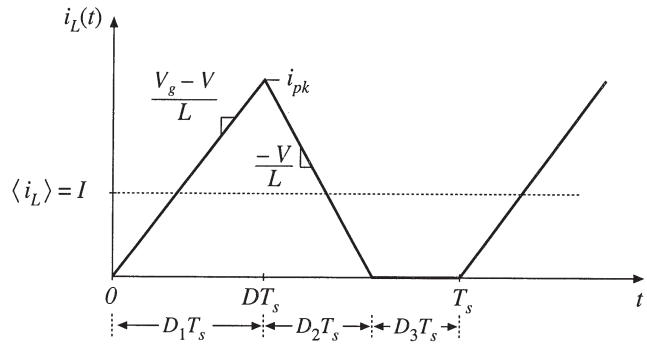


Fig. 5.10 Inductor current waveform $i_L(t)$, buck converter operating in discontinuous conduction mode.

The integral, or area under the iL(t) curve, is the area of the triangle having height i_{pk} and base dimension $(D_1 + D_2)T_s$. Use of the triangle area formula yields

$$\int_0^{T_s} i_L(t)dt = \tfrac{1}{2} i_{pk}\left(D_1 + D_2\right)T_s \tag{5.25}$$

Substitution of Eqs. (5.23) and (5.25) into Eq. (5.24) leads to

$$\langle i_L \rangle = \left(V_g - V\right)\left(\frac{D_1 T_s}{2L}\right)\left(D_1 + D_2\right) \tag{5.26}$$

Finally, by equating this result to the dc load current, according to Eq. (5.22), we obtain

$$\frac{V}{R} = \frac{D_1 T_s}{2L}\left(D_1 + D_2\right)\left(V_g - V\right) \tag{5.27}$$

Thus, we have two unknowns, V and D_2, and we have two equations. The first equation, Eq. (5.19), was obtained by inductor volt-second balance, while the second equation, Eq. (5.27), was obtained using capacitor charge balance. Elimination of D_2 from the two equations, and solution for the voltage conversion ratio $M(D_1, K) = V/V_g$, yields

$$\frac{V}{V_g} = \frac{2}{1 + \sqrt{1 + \dfrac{4K}{D_1^2}}} \tag{5.28}$$

where $K = 2L/RT_s$

valid for $K < K_{crit}$

This is the solution of the buck converter operating in discontinuous conduction mode.

The complete buck converter characteristics, including both continuous and discontinuous conduction modes, are therefore

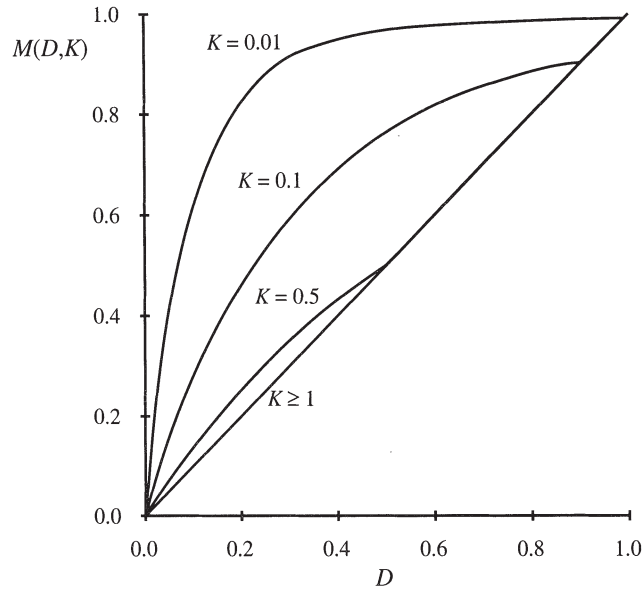


Fig. 5.11 Voltage conversion ratio $M(D, K)$, buck converter.

$$M = \begin{cases} D & \text{for } K > K_{crit} \\ \dfrac{2}{1 + \sqrt{1 + \dfrac{4K}{D^2}}} & \text{for } K < K_{crit} \end{cases} \tag{5.29}$$

where the transistor duty cycle D is identical to the subinterval 1 duty cycle D_1 of the above derivation. These characteristics are plotted in Fig. 5.11, for several values of K. It can be seen that the effect of the discontinuous conduction mode is to cause the output voltage to increase. As K tends to zero (the unloaded case), M tends to unity for all nonzero D. The characteristics are continuous, and Eq. (5.28) intersects the CCM characteristic $M = D$ at the mode boundary.

5.3 BOOST CONVERTER EXAMPLE

As a second example, consider the boost converter of Fig. 5.12. Let's determine the boundary between modes, and solve for the conversion ratio in the discontinuous conduction mode. Behavior of the boost converter operating in the continuous conduction mode was analyzed previously, in Section 2.3, and expressions for the inductor current dc component I and ripple peak magnitude Δi_L were found.

When the diode conducts, its current is identical to the inductor current $i_L(t)$. As can be seen from Fig. 2.18, the minimum value of the inductor current during the diode conduction subinterval $DT_s < t < T_s$ is $(I - \Delta i_L)$. If this minimum current is positive, then the diode is forward-biased for the entire subinterval $DT_s < t < T_s$, and the converter operates in the continuous conduction mode. So the conditions for operation of the boost converter in the continuous and discontinuous conduction modes are:

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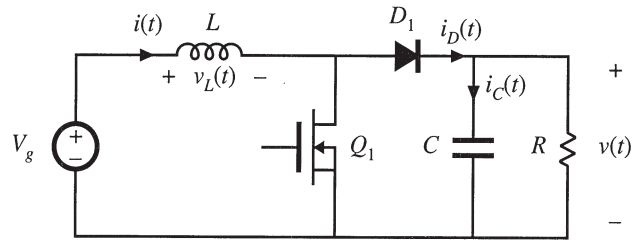


Fig. 5.12 Boost converter example.

$$\begin{aligned} I &> \Delta i_L \quad \text{for CCM} \\ I &< \Delta i_L \quad \text{for DCM} \end{aligned} \tag{5.30}$$

which is identical to the results for the buck converter. Substitution of the CCM solutions for I and Δi_L, Eqs. (2-39) and (2-43), yields

$$\frac{V_g}{D'^2 R} > \frac{DT_s V_g}{2L} \quad \text{for CCM} \tag{5.31}$$

This equation can be rearranged to obtain

$$\frac{2L}{RT_s} > DD'^2 \quad \text{for CCM} \tag{5.32}$$

which is in the standard form

$$\begin{aligned} K &> K_{crit}(D) \quad \text{for CCM} \\ K &< K_{crit}(D) \quad \text{for DCM} \end{aligned} \tag{5.33}$$

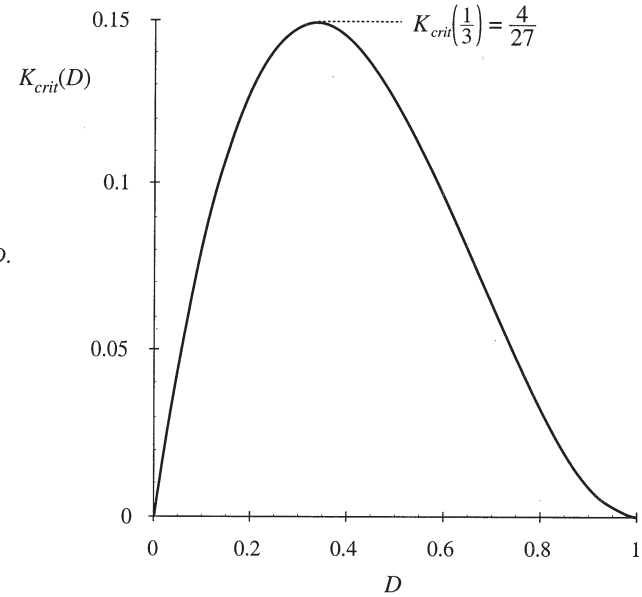


Fig. 5.13 Boost converter $K_{crit}(D)$ vs. D.

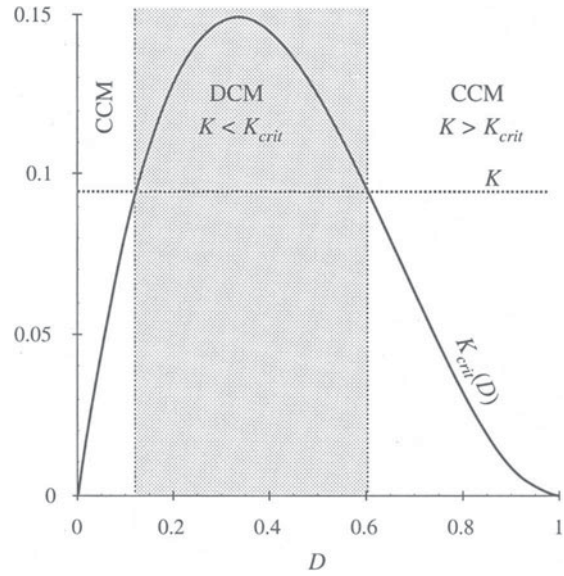


Fig. 5.14 Comparison of K with $K_{crit}(D)$.

where

$$K = \frac{2L}{RT_s} \quad \text{and} \quad K_{crit}(D) = DD'^2$$

The conditions for operation in the continuous or discontinuous conduction modes are of similar form to those for the buck converter; however, the critical value $K_{crit}(D)$ is a different function of the duty cycle D. The dependence of $K_{crit}(D)$ on the duty cycle D is plotted in Fig. 5.13. $K_{crit}(D)$ is zero at $D = 0$ and at $D = 1$, and has a maximum value of 4/27 at $D = 1/3$. Hence, if K is greater than 4/27, then the converter operates in the continuous conduction mode for all D. Figure 5.14 illustrates what happens when K is less than 4/27. The converter then operates in the discontinuous conduction mode for some intermediate range of values of D near $D = 1/3$. But the converter operates in the continuous conduction mode near $D = 0$ and $D = 1$. Unlike the buck converter, the boost converter must operate in the continuous conduction mode near $D = 0$ because the ripple magnitude approaches zero while the dc component I does not.

Next, let us analyze the conversion ratio $M = V/V_g$ of the boost converter. When the transistor conducts, for the subinterval $0 < t < D_1T_s$, the converter circuit reduces to the circuit of 5.15(a). The inductor voltage and capacitor current are given by

$$\begin{aligned} v_L(t) &= V_g \\ i_C(t) &= -\frac{v(t)}{R} \end{aligned} \tag{5.34}$$

Use of the linear ripple approximation, to ignore the output capacitor voltage ripple, leads to

$$\begin{aligned} v_L(t) &\approx V_g \\ i_C(t) &\approx -\frac{V}{R} \end{aligned} \tag{5.35}$$

During the second subinterval $D_1T_s < t < (D_1 + D_2)T_s$, the diode conducts. The circuit then reduces to

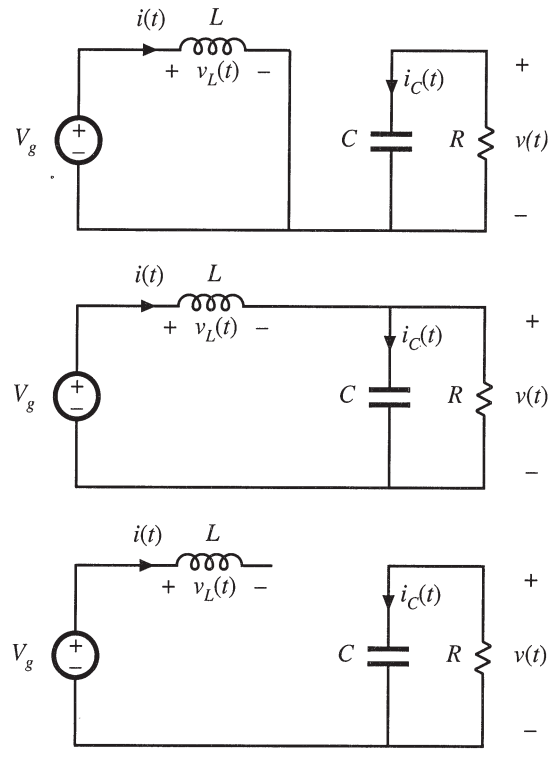


Fig. 5.15 Boost converter circuits: (a) during subinterval 1, $0 < t < D_1T_s$, (b) during subinterval 2, $D_1T_s < t < (D_1 + D_2)T_s$, (c) during subinterval 3, $(D_1 + D_2)T_s < t < T_s$.

Fig. 5.15(b). The inductor voltage and capacitor current are given by

$$\begin{aligned} v_L(t) &= V_g - v(t) \\ i_C(t) &= i(t) - \frac{v(t)}{R} \end{aligned} \tag{5.36}$$

Neglect of the output capacitor voltage ripple yields

$$\begin{aligned} v_L(t) &\approx V_g - V \\ i_C(t) &\approx i(t) - \frac{V}{R} \end{aligned} \tag{5.37}$$

The inductor current ripple has not been neglected.

During the third subinterval, $(D_1 + D_2)T_s < t < T_s$, both transistor and diode are in the off state, and Fig. 5.15(c) is obtained. The network equations are:

$$\begin{aligned} v_L &= 0, \quad i = 0 \\ i_C(t) &= -\frac{v(t)}{R} \end{aligned} \tag{5.38}$$

Use of the small-ripple approximation yields

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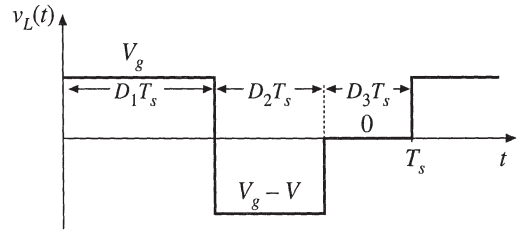


Fig. 5.16 Inductor voltage waveform $v_L(t)$, boost converter operating in discontinuous conduction mode.

$$\begin{aligned} v_L(t) &= 0 \\ i_C(t) &= -\frac{V}{R} \end{aligned} \tag{5.39}$$

Equations (5.35), (5.37), and (5.39) are now used to sketch the inductor voltage waveform as in Fig. 5.16. By volt-second balance, this waveform must have zero dc component when the converter operates in steady state. By equating the average value of this $v_L(t)$ waveform to zero, one obtains

$$D_1 V_g + D_2\left(V_g - V\right) + D_3(0) = 0 \tag{5.40}$$

Solution for the output voltage V yields

$$V = \frac{D_1 + D_2}{D_2} V_g \tag{5.41}$$

The diode duty cycle D_2 is again an unknown, and so a second equation is needed for elimination of D_2 before the output voltage V can be found.

We can again use capacitor charge balance to obtain the second equation. The connection of the output capacitor to its adjacent components is detailed in Fig. 5.17. Unlike the buck converter, the diode in the boost converter is connected to the output node. The node equation of Fig. 5.17 is

$$i_D(t) = i_C(t) + \frac{v(t)}{R} \tag{5.42}$$

where $i_D(t)$ is the diode current. By capacitor charge balance, the capacitor current $i_C(t)$ must have zero dc component in steady state. Therefore, the diode current dc component $\langle i_D \rangle$ must be equal to the dc component of the load current:

$$\langle i_D \rangle = \frac{V}{R} \tag{5.43}$$

So we need to sketch the diode current waveform, and find its dc component.

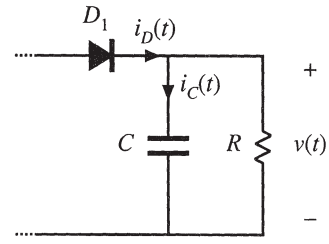


Fig. 5.17 Connection of the output capacitor to adjacent components in the boost converter.

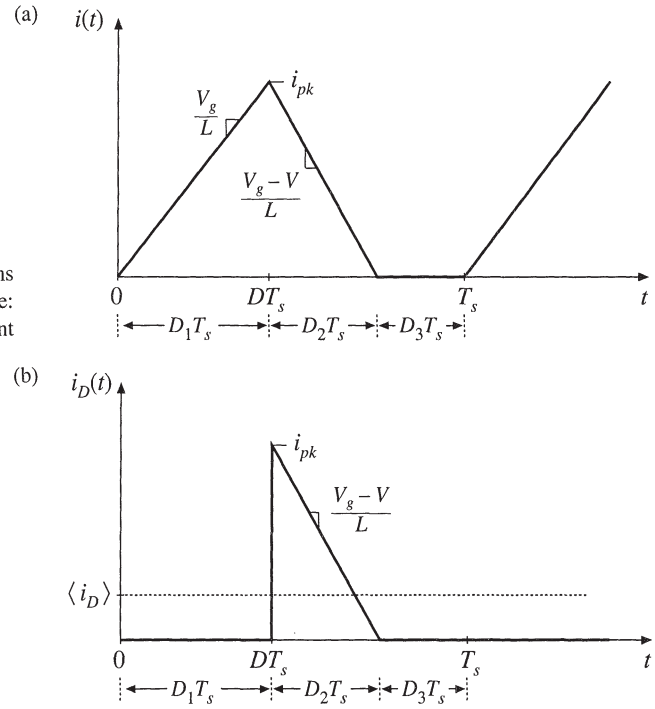


Fig. 5.18 Boost converter waveforms in the discontinuous conduction mode: (a) inductor current $i(t)$, (b) diode current $i_D(t)$.

The waveforms of the inductor current $i(t)$ and diode current $i_D(t)$ are illustrated in Fig. 5.18. The inductor current begins at zero, and rises to a peak value i_{pk} during the first subinterval. This peak value i_{pk} is equal to the slope V_g/L, multiplied by the length of the first subinterval, D_1T_s:

$$i_{pk} = \frac{V_g}{L} D_1 T_s \tag{5.44}$$

The diode conducts during the second subinterval, and the inductor current then decreases to zero, where it remains during the third subinterval. The diode current $i_D(t)$ is identical to the inductor current $i(t)$ during the second subinterval. During the first and third subintervals, the diode is reverse-biased and hence $i_D(t)$ is zero.

The dc component of the diode current, $\langle i_D \rangle$, is:

$$\langle i_D \rangle = \frac{1}{T_s} \int_0^{T_s} i_D(t) dt \tag{5.45}$$

The integral is the area under the $i_D(t)$ waveform. As illustrated in Fig. 5.18(b), this area is the area of the triangle having peak value i_{pk} and base dimension D_2T_s:

$$\int_0^{T_s} i_D(t) dt = \tfrac{1}{2} i_{pk} D_2 T_s \tag{5.46}$$

Substitution of Eqs. (5.44) and (5.46) into Eq. (5.45) leads to the following expression for the dc component of the diode current:

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$$\langle i_D \rangle = \frac{1}{T_s}\left(\frac{1}{2} i_{pk} D_2 T_s\right) = \frac{V_g D_1 D_2 T_s}{2L} \tag{5.47}$$

By equating this expression to the dc load current as in Eq. (5.43), one obtains the final result

$$\frac{V_g D_1 D_2 T_s}{2L} = \frac{V}{R} \tag{5.48}$$

So now we have two unknowns, V and D_2. We have two equations: Eq. (5.41) obtained via inductor volt-second balance, and Eq. (5.48) obtained using capacitor charge balance. Let us now eliminate D_2 from this system of equations, and solve for the output voltage V. Solution of Eq. (5.41) for D_2 yields

$$D_2 = D_1 \frac{V_g}{V - V_g} \tag{5.49}$$

By inserting this result into Eq. (5.48), and rearranging terms, one obtains the following quadratic equation:

$$V^2 - V V_g - \frac{V_g^2 D_1^2}{K} = 0 \tag{5.50}$$

Use of the quadratic formula yields

$$\frac{V}{V_g} = \frac{1 \pm \sqrt{1 + \frac{4D_1^2}{K}}}{2} \tag{5.51}$$

The quadratic equation has two roots: one of the roots of Eq. (5.51) is positive, while the other is negative. We already know that the output voltage of the boost converter should be positive, and indeed, from Eq. (5.41), it can be seen that V/V_g must be positive since the duty cycles D_1 and D_2 are positive. So we should select the positive root:

$$\frac{V}{V_g} = M(D_1, K) = \frac{1 + \sqrt{1 + \frac{4D_1^2}{K}}}{2} \tag{5.52}$$

where $K = 2L/RT_s$

valid for $K < K_{crit}(D)$

This is the solution of the boost converter operating in the discontinuous conduction mode.

The complete boost converter characteristics, including both continuous and discontinuous conduction modes, are

$$M = \begin{cases} \dfrac{1}{1-D} & \text{for } K > K_{crit} \\ \dfrac{1 + \sqrt{1 + \frac{4D^2}{K}}}{2} & \text{for } K < K_{crit} \end{cases} \tag{5.53}$$

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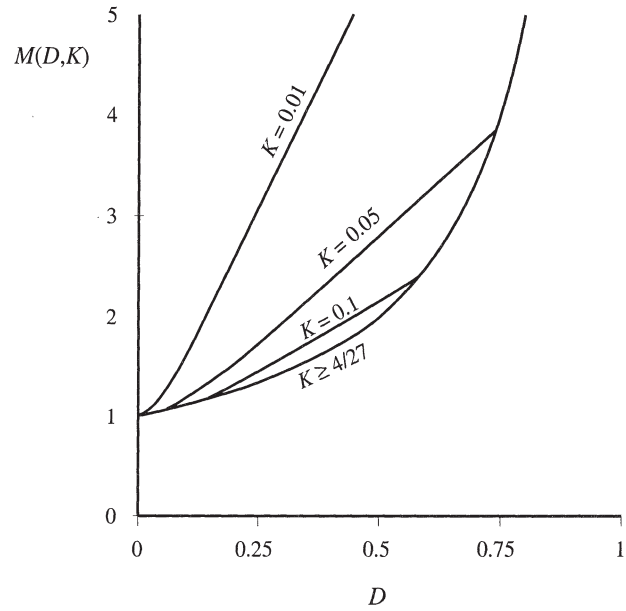


Fig. 5.19 Voltage conversion ratio $M(D, K)$ of the boost converter, including both continuous and discontinuous conduction modes

These characteristics are plotted in Fig. 5.19, for several values of K. As in the buck converter, the effect of the discontinuous conduction mode is to cause the output voltage to increase. The DCM portions of the characteristics are nearly linear, and can be approximated as

$$M \approx \frac{1}{2} + \frac{D}{\sqrt{K}} \tag{5.54}$$

5.4 SUMMARY OF RESULTS AND KEY POINTS

The characteristics of the basic buck, boost, and buck-boost are summarized in Table 5.2. Expressions for $K_{crit}(D)$, as well as for the solutions of the dc conversion ratios in CCM and DCM, and for the DCM diode conduction duty cycle D_2, are given.

The dc conversion ratios of the DCM buck, boost, and buck-boost converters are compared in

Table 5.2 Summary of CCM-DCM characteristics for the buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	DCM $M(D, K)$	DCM $D_2(D, K)$	CCM $M(D)$
Buck	$(1 - D)$	$\frac{2}{1 + \sqrt{1 + 4K/D^2}}$	$\frac{K}{D} M(D, K)$	D
Boost	$D(1 - D)^2$	$\frac{1 + \sqrt{1 + 4D^2/K}}{2}$	$\frac{K}{D} M(D, K)$	$\frac{1}{1 - D}$
Buck–boost	$(1 - D)^2$	$-\frac{D}{\sqrt{K}}$	$\sqrt{K}$	$-\frac{D}{1 - D}$

with $K = 2L/RT_s$, DCM occurs for $K < K_{crit}$.

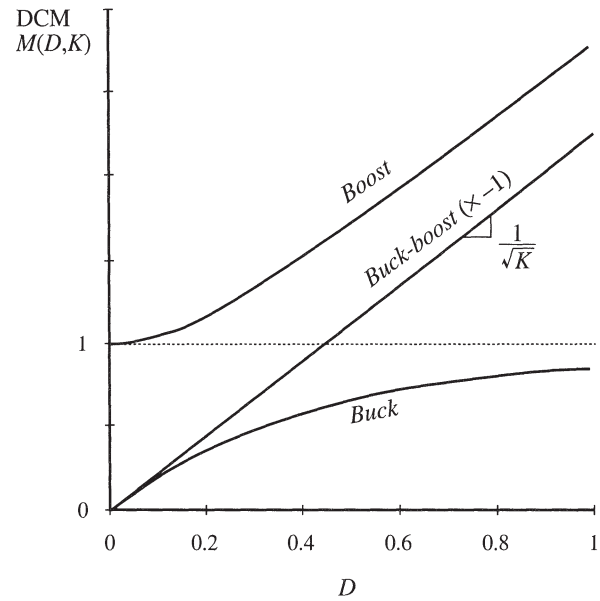


Fig. 5.20 Comparison of dc conversion ratios of the buck–boost, buck, and boost converters operated in the discontinuous conduction mode.

Fig. 5.20. The buck-boost characteristic is a line with slope $1/\sqrt{K}$. The characteristics of the buck and the boost converters are both asymptotic to this line, as well as to the line $M = 1$. Hence, when operated deeply into the discontinuous conduction mode, the boost converter characteristic becomes nearly linear with slope $1/\sqrt{K}$, especially at high duty cycle. Likewise, the buck converter characteristic becomes nearly linear with the same slope, when operated deeply into discontinuous conduction mode at low duty cycle.

The following are the key points of this chapter:

1. The discontinuous conduction mode occurs in converters containing current- or voltage-unidirectional switches, when the inductor current or capacitor voltage ripple is large enough to cause the switch current or voltage to reverse polarity.
2. Conditions for operation in the discontinuous conduction mode can be found by determining when the inductor current or capacitor voltage ripples and dc components cause the switch on state current or off state voltage to reverse polarity.
3. The dc conversion ratio M of converters operating in the discontinuous conduction mode can be found by application of the principles of inductor volt-second and capacitor charge balance.
4. Extra care is required when applying the small-ripple approximation. Some waveforms, such as the output voltage, should have small ripple which can be neglected. Other waveforms, such as one or more inductor currents, may have large ripple that cannot be ignored.
5. The characteristics of a converter changes significantly when the converter enters DCM. The output voltage becomes load-dependent, resulting in an increase in the converter output impedance.

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PROBLEMS

5.1 The elements of the buck-boost converter of Fig. 5.21 are ideal: all losses may be ignored. Your results for parts (a) and (b) should agree with Table 5.2.

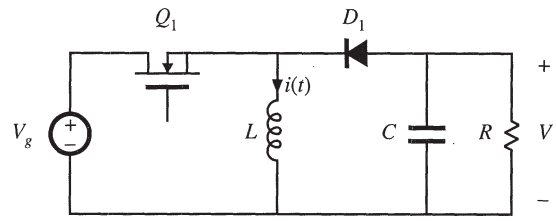


Fig. 5.21 Buck–boost converter of Problems 5.1 and 5.13.

(a) Show that the converter operates in discontinuous conduction mode when $K < K_{crit}$, and derive expressions for K and K_{crit}.

(b) Derive an expression for the dc conversion ratio V/V_g of the buck–boost converter operating in discontinuous conduction mode.

(c) For $K = 0.1$, plot V/V_g over the entire range $0 \le D \le 1$.

(d) Sketch the inductor voltage and current waveforms for $K = 0.1$ and $D = 0.3$. Label salient features.

(e) What happens to V at no load ($R \to \infty$)? Explain why, physically.

5.2 A certain buck converter contains a synchronous rectifier, as described in Section 4.1.5.

(a) Does this converter operate in the discontinuous conduction mode at light load? Explain.

(b) The load resistance is disconnected ($R \to \infty$), and the converter is operated with duty cycle 0.5. Sketch the inductor current waveform.

5.3 An unregulated dc input voltage V_g varies over the range $35\text{ V} \le V_g \le 70\text{ V}$. A buck converter reduces this voltage to 28 V; a feedback loop varies the duty cycle as necessary such that the converter output voltage is always equal to 28 V. The load power varies over the range $10\text{ W} \le P_{load} \le 1000\text{ W}$. The element values are:

$L = 22\ \mu\text{H}$ $C = 470\ \mu\text{F}$ $f_s = 75\text{ kHz}$

Losses may be ignored.

(a) Over what range of V_g and load current does the converter operate in CCM?

(b) Determine the maximum and minimum values of the steady-state transistor duty cycle.

5.4 The transistors in the converter of Fig. 5.22 are driven by the same gate drive signal, so that they turn on and off in synchronism with duty cycle D.

(a) Determine the conditions under which this converter operates in the discontinuous conduction mode, as a function of the steady-state duty ratio D

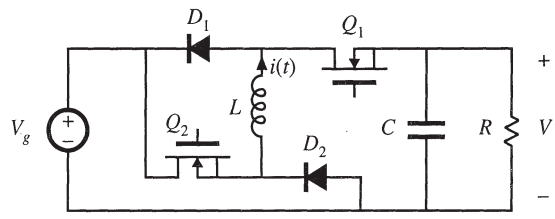


Fig. 5.22 Watkins-Johnson converter of Problem 5.4.

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and the dimensionless parameter $K = 2L/RT_s$.

(b) What happens to your answer to Part (a) for $D < 0.5$?

(c) Derive an expression for the dc conversion ratio $M(D, K)$. Sketch M vs. D for $K = 10$ and for $K = 0.1$, over the range $0 \le D \le 1$.

5.5 DCM mode boundary analysis of the Ćuk converter of Fig. 5.23. The capacitor voltage ripples are small.

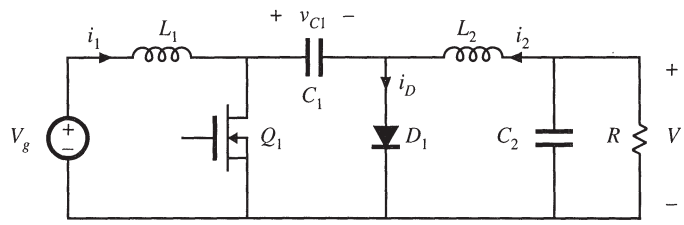


Fig. 5.23 Ćuk converter, Problems 5.5, 5.6, 5.11, and 5.12

(a) Sketch the diode current waveform for CCM operation. Find its peak value, in terms of the ripple magnitudes Δi_{L1}, Δi_{L2}, and the dc components I_1 and I_2, of the two inductor currents $i_{L1}(t)$ and $i_{L2}(t)$, respectively.

(b) Derive an expression for the conditions under which the Ćuk converter operates in the discontinuous conduction mode. Express your result in the form $K < K_{crit}(D)$, and give formulas for K and $K_{crit}(D)$.

5.6 DCM conversion ratio analysis of the Ćuk converter of Fig. 5.23.

(a) Suppose that the converter operates at the boundary between CCM and DCM, with the following element and parameter values:

$D = 0.4$	$f_s = 100$ kHz
$V_g = 120$ V	$R = 10\ \Omega$
$L_1 = 54\ \mu$H	$L_2 = 27\ \mu$H
$C_1 = 47\ \mu$F	$C_2 = 100\ \mu$F

Sketch the diode current waveform $i_D(t)$, and the inductor current waveforms $i_1(t)$ and $i_2(t)$. Label the magnitudes of the ripples and dc components of these waveforms.

(b) Suppose next that the converter operates in the discontinuous conduction mode, with a different choice of parameter and element values. Derive an analytical expression for the dc conversion ratio $M(D, K)$.

(c) Sketch the diode current waveform $i_D(t)$, and the inductor current waveforms $i_1(t)$ and $i_2(t)$, for operation in the discontinuous conduction mode.

5.7 DCM mode boundary analysis of the SEPIC of Fig. 5.24

(a) Sketch the diode current waveform for CCM operation. Find its peak value, in terms of the ripple magnitudes Δi_{L1}, Δi_{L2}, and the dc components I_1 and I_2, of the two inductor currents $i_{L1}(t)$ and $i_{L2}(t)$, respectively.

(b) Derive an expression for the conditions under which the SEPIC operates in the discontinuous conduction mode. Express your result in the form $K < K_{crit}(D)$, and give formulas for K and $K_{crit}(D)$.

5.8 DCM conversion ratio analysis of the SEPIC of Fig. 5.24.

(a) Suppose that the converter operates at the boundary between CCM and DCM, with the follow-

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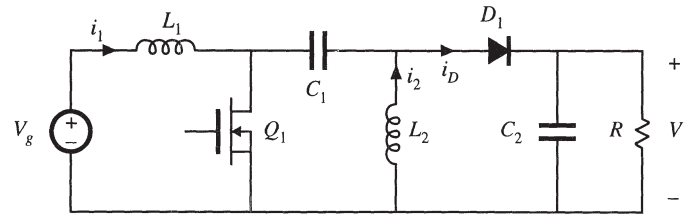


Fig. 5.24 SEPIC, Problems 5.7 and 5.8.

ing element and parameter values:

$D = 0.225$	$f_s = 100$ kHz
$V_g = 120$ V	$R = 10\ \Omega$
$L_1 = 50\ \mu$H	$L_2 = 75\ \mu$H
$C_1 = 47\ \mu$F	$C2 = 200\ \mu$F

Sketch the diode current waveform $i_D(t)$, and the inductor current waveforms $i_1(t)$ and $i_2(t)$. Label the magnitudes of the ripples and dc components of these waveforms.

(b) Suppose next that the converter operates in the discontinuous conduction mode, with a different choice of parameter and element values. Derive an analytical expression for the dc conversion ratio $M(D, K)$.

(c) Sketch the diode current waveform $i_D(t)$, and the inductor current waveforms $i_1(t)$ and $i_2(t)$, for operation in the discontinuous conduction mode.

5.9 An L–C input filter is added to a buck converter as illustrated in Fig. 5.25. Inductors L_1 and L_2 and capacitor C_2 are large in value, such that their switching ripples are small. All losses can be neglected.

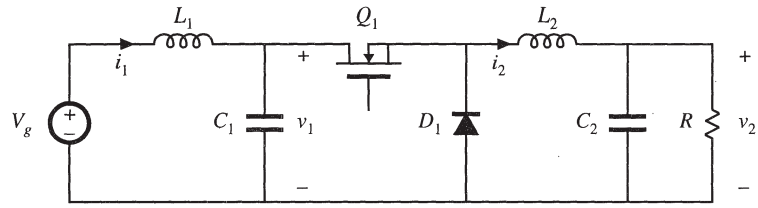


Fig. 5.25 Buck converter with input filter, Problems 5.9 and 5.10.

(a) Sketch the capacitor C_1 voltage waveform $v_1(t)$, and derive expressions for its dc component V_1 and peak ripple magnitude Δv_1.

(b) The load current is increased (R is decreased in value) such that Δv_1 is greater than V_1.

(*i*) Sketch the capacitor voltage waveform $v_1(t)$.

(*ii*) For each subinterval, determine which semiconductor devices conduct.

(*iii*) Determine the conditions under which the discontinuous conduction mode occurs. Express your result in the form $K < K_{crit}(D)$, and give formulas for K and $K_{crit}(D)$.

5.10 Derive an expression for the conversion ratio $M(D, K)$ of the DCM converter described in the previous problem. Note: D is the transistor duty cycle.

5.11 In the Cuk converter of Fig. 5.23, inductors L_1 and L_2 and capacitor C_2 are large in value, such that their switching ripples are small. All losses can be neglected.

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(a) Assuming that the converter operates in CCM, sketch the capacitor C_1 voltage waveform $v_{C1}(t)$, and derive expressions for its dc component V_1 and peak ripple magnitude Δv_{C1}.

(b) The load current is increased (R is decreased in value) such that Δv_{C1} is greater than V_1.

(i) Sketch the capacitor voltage waveform $v_{C1}(t)$.

(ii) For each subinterval, determine which semiconductor devices conduct.

(iii) Determine the conditions under which the discontinuous conduction mode occurs. Express your result in the form $K < K_{crit}(D)$, and give formulas for K and $K_{crit}(D)$.

5.12 Derive an expression for the conversion ratio $M(D, K)$ of the DCM Ćuk converter described in the previous problem. Note: D is the transistor duty cycle.

5.13 A DCM buck-boost converter as in Fig. 5.21 is to be designed to operate under the following conditions:

$$136 \text{ V} \le V_g \le 204 \text{ V}$$
$$5 \text{ W} \le P_{load} \le 100 \text{ W}$$
$$V = -150 \text{ V}$$
$$f_s = 100 \text{ kHz}$$

You may assume that a feedback loop will vary to transistor duty cycle as necessary to maintain a constant output voltage of – 150 V.

Design the converter, subject to the following considerations:

- The converter should operate in the discontinuous conduction mode at all times
- Given the above requirements, choose the element values to minimize the peak inductor current
- The output voltage peak ripple should be less than 1V.

Specify:

(a) The inductor value L

(b) The output capacitor value C

(c) The worst-case peak inductor current i_{pk}

(d) The maximum and minimum values of the transistor duty cycle D

5.14 A DCM boost converter as in Fig. 5.12 is to be designed to operate under the following conditions:

$$18 \text{ V} \le V_g \le 36 \text{ V}$$
$$5 \text{ W} \le P_{load} \le 100 \text{ W}$$
$$V = 48 \text{ V}$$
$$f_s = 150 \text{ kHz}$$

You may assume that a feedback loop will vary to transistor duty cycle as necessary to maintain a constant output voltage of 48 V.

Design the converter, subject to the following considerations:

- The converter should operate in the discontinuous conduction mode at all times. To ensure an adequate design margin, the inductance L should be chosen such that K is no greater than 75% of K_{crit} at all operating points.
- Given the above requirements, choose the element values to minimize the peak inductor current.
- The output voltage peak ripple should be less than 1V.

Specify:

(a) The inductor value L

(b) The output capacitor value C

(c) The worst-case peak inductor current i_{pk}

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(d) The maximum and minimum values of the transistor duty cycle D.

(e) The values of D, K and K_{crit} at the following operating points: (*i*) $V_g = 18$ V and $P_{load} = 5$ W; (*ii*) $V_g = 36$ V and $P_{load} = 5$ W; (*iii*) $V_g = 18$ V and $P_{load} = 100$ W; (*iv*) $V_g = 36$ V and $P_{load} = 100$ W.

5.15 In dc–dc converters used in battery-powered portable equipment, it is sometimes required that the converter continue to regulate its load voltage with high efficiency while the load is in a low-power "sleep" mode. The power required by the transistor gate drive circuitry, as well as much of the switching loss, is dependent on the switching frequency but not on the load current. So to obtain high efficiency at very low load powers, a variable-frequency control scheme is used, in which the switching frequency is reduced in proportion to the load current.

Consider the boost converter system of Fig. 5.26(a). The battery pack consists of two nickel-cadmium cells, which produce a voltage of $V_g = 2.4$ V ± 0.4 V. The converter boosts this voltage to a regulated 5 V. As illustrated in Fig. 5.26(b), the converter operates in the discontinuous conduction mode, with constant transistor on-time t_{on}. The transistor off-time t_{off} is varied by the controller to regulate the output voltage.

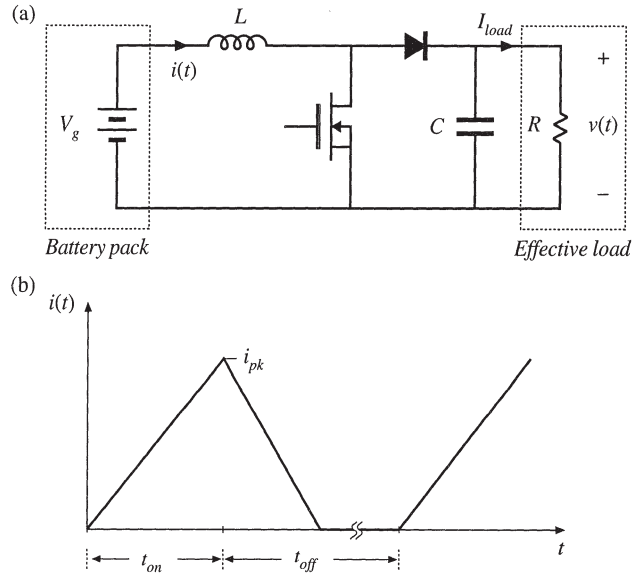


Fig. 5.26 Boost converter employed in portable battery-powered equipment with sleep mode, Problem 5.15: (a) converter circuit, (b) inductor current waveform.

(a) Write the equations for the CCM-DCM boundary and conversion ratio $M = V/V_g$, in terms of t_{on}, t_{off}, L, and the effective load resistance R.

For parts (b) and (c), the load current can vary between 100 μA and 1 A. The transistor on time is fixed: $t_{on} = 10$ μs.

(b) Select values for L and C such that:

- The output voltage peak ripple is no greater than 50 mV,
- The converter always operates in DCM, and
- The peak inductor current is as small as possible.

(c) For your design of part (b), what are the maximum and minimum values of the switching frequency?

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6
Converter Circuits

We have already analyzed the operation of a number of different types of converters: buck, boost, buck–boost, Ćuk, voltage-source inverter, etc. With these converters, a number of different functions can be performed: step-down of voltage, step-up, inversion of polarity, and conversion of dc to ac or vice-versa.

It is natural to ask, Where do these converters come from? What other converters occur, and what other functions can be obtained? What are the basic relations between converters? In this chapter, several different circuit manipulations are explored, which explain the origins of the basic converters. Inversion of source and load transforms the buck converter into the boost converter. Cascade connection of converters, and simplification of the resulting circuit, shows how the buck–boost and Ćuk converters are based on the buck and the boost converters. Differential connection of the load between the outputs of two or more converters leads to a single-phase or polyphase inverter. A short list of some of the better known converter circuits follows this discussion.

Transformer-isolated dc–dc converters are also covered in this chapter. Use of a transformer allows isolation and multiple outputs to be obtained in a dc-dc converter, and can lead to better converter optimization when a very large or very small conversion ratio is required. The transformer is modeled as a magnetizing inductance in parallel with an ideal transformer; this allows the analysis techniques of the previous chapters to be extended to cover converters containing transformers. A number of well-known isolated converters, based on the buck, boost, buck–boost, single-ended primary inductance converter (SEPIC), and Ćuk, are listed and discussed.

Finally, the evaluation, selection, and design of converters to meet given requirements are considered. Important performance-related attributes of transformer-isolated converters include: whether the transformer reset process imposes excessive voltage stress on the transistors, whether the converter can supply a high-current output without imposing excessive current stresses on the secondary-side components, and whether the converter can be well-optimized to operate with a wide range of operating points,

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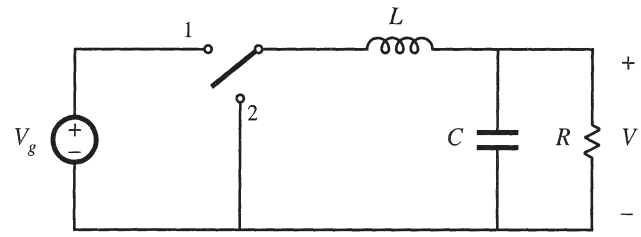


Fig. 6.1 The basic buck converter.

that is, with large tolerances in V_g and P_{load}. Switch utilization is a simplified figure-of-merit that measures the ratio of the converter output power to the total transistor voltage and current stress. As the switch utilization increases, the converter efficiency increases while its cost decreases. Isolated converters with large variations in operating point tend to utilize their power devices more poorly than nonisolated converters which function at a single operating point. Computer spreadsheets are a good tool for optimization of power stage designs and for trade studies to select a converter topology for a given application.

6.1 CIRCUIT MANIPULATIONS

The buck converter (Fig. 6.1) was developed in Chapter 1 using basic principles. The switch reduces the voltage dc component, and the low-pass filter removes the switching harmonics. In the continuous conduction mode, the buck converter has a conversion ratio of $M = D$. The buck converter is the simplest and most basic circuit, from which we will derive other converters.

6.1.1 Inversion of Source and Load

Let us consider first what happens when we interchange the power input and power output ports of a converter. In the buck converter of Fig. 6.2(a), voltage V_1 is applied at port 1, and voltage V_2 appears at port 2. We know that

$$V_2 = DV_1 \tag{6.1}$$

This equation can be derived using the principle of inductor volt-second balance, with the assumption that the converter operates in the continuous conduction mode. Provided that the switch is realized such that this assumption holds, then Eq. (6.1) is true regardless of the direction of power flow.

So let us interchange the power source and load, as in Fig. 6.2(b). The load, bypassed by the capacitor, is connected to converter port 1, while the power source is connected to converter port 2. Power now flows in the opposite direction through the converter. Equation (6.1) must still hold; by solving for the load voltage V_1, one obtains

$$V_1 = \frac{1}{D} V_2 \tag{6.2}$$

So the load voltage is greater than the source voltage. Figure 6.2(b) is a boost converter, drawn backwards. Equation 6.2 nearly coincides with the familiar boost converter result, $M(D) = 1/D'$, except that D' is replaced by D.

Since power flows in the opposite direction, the standard buck converter unidirectional switch

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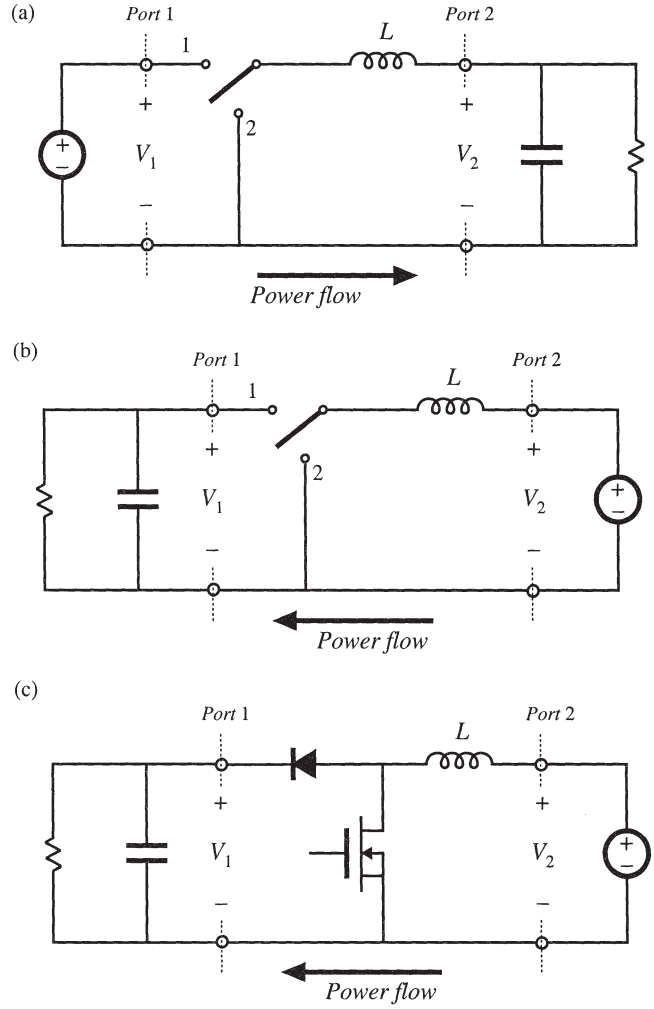


Fig. 6.2 Inversion of source and load transforms a buck converter into a boost converter: (a) buck converter, (b) inversion of source and load, (c) realization of switch.

realization cannot be used with the circuit of Fig. 6.2(b). By following the discussion of Chapter 4, one finds that the switch can be realized by connecting a transistor between the inductor and ground, and a diode from the inductor to the load, as shown in Fig. 6.2(c). In consequence, the transistor duty cycle D becomes the fraction of time which the single-pole double-throw (SPDT) switch of Fig. 6.2(b) spends in position 2, rather than in position 1. So we should interchange D with its complement D' in Eq. (6.2), and the conversion ratio of the converter of Fig. 6.2(c) is

$$V_1 = \frac{1}{D'} V_2 \tag{6.3}$$

Thus, the boost converter can be viewed as a buck converter having the source and load connections exchanged, and in which the switch is realized in a manner that allows reversal of the direction of power flow.

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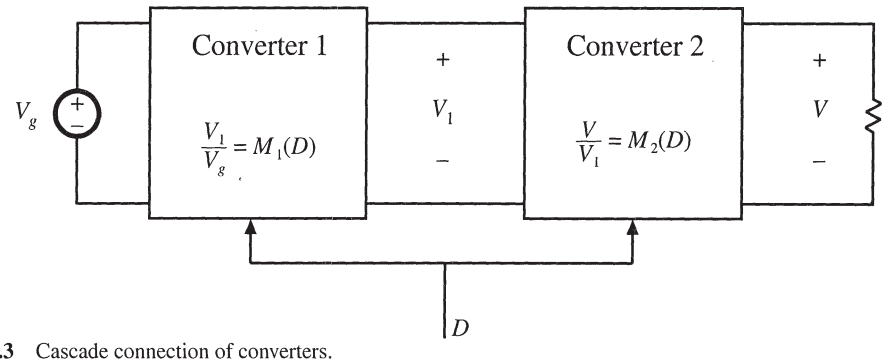


Fig. 6.3 Cascade connection of converters.

6.1.2 Cascade Connection of Converters

Converters can also be connected in cascade, as illustrated in Fig. 6.3 [1,2]. Converter 1 has conversion ratio $M_1(D)$, such that its output voltage V_1 is

$$V_1 = M_1(D)V_g \tag{6.4}$$

This voltage is applied to the input of the second converter. Let us assume that converter 2 is driven with the same duty cycle D applied to converter 1. If converter 2 has conversion ratio $M_2(D)$, then the output voltage V is

$$V = M_2(D)V_1 \tag{6.5}$$

Substitution of Eq. (6.4) into Eq. (6.5) yields

$$\frac{V}{V_g} = M(D) = M_1(D)M_2(D) \tag{6.6}$$

Hence, the conversion ratio $M(D)$ of the composite converter is the product of the individual conversion ratios $M_1(D)$ and $M_2(D)$.

Let us consider the case where converter 1 is a buck converter, and converter 2 is a boost converter. The resulting circuit is illustrated in Fig. 6.4. The buck converter has conversion ratio

$$\frac{V_1}{V_g} = D \tag{6.7}$$

The boost converter has conversion ratio

$$\frac{V}{V_1} = \frac{1}{1-D} \tag{6.8}$$

So the composite conversion ratio is

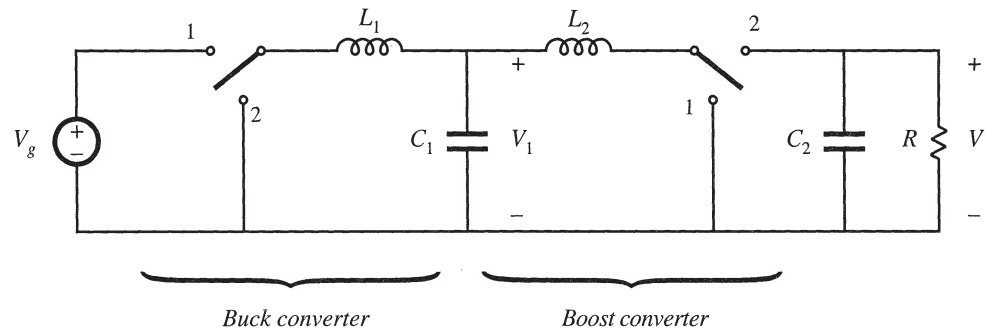


Fig. 6.4 Cascade connection of buck converter and boost converter.

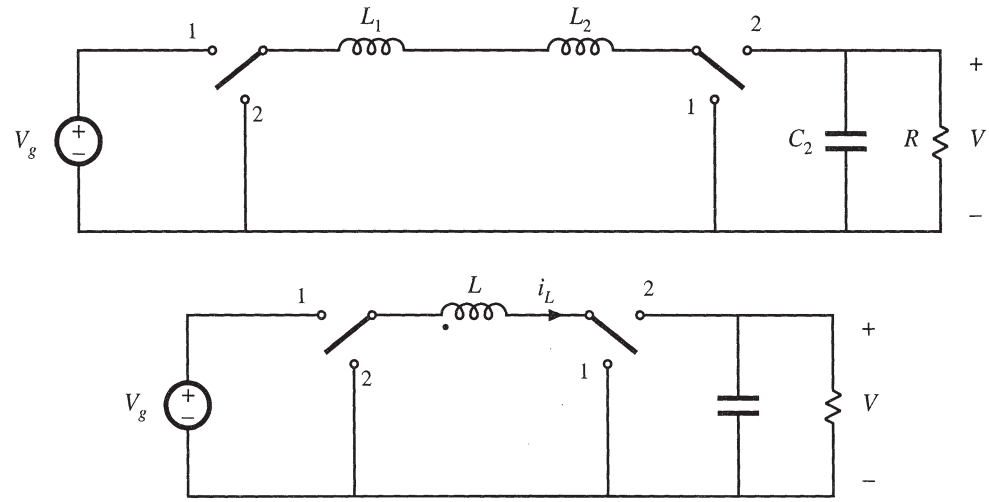


Fig. 6.5 Simplification of the cascaded buck and boost converter circuit of Fig. 6.4: (a) removal of capacitor C_1, (b) combining of inductors L_1 and L_2.

$$\frac{V}{V_g} = \frac{D}{1-D} \tag{6.9}$$

The composite converter has a noninverting buck–boost conversion ratio. The voltage is reduced when $D < 0.5$, and increased when $D > 0.5$.

The circuit of Fig. 6.4 can be simplified considerably. Note that inductors L_1 and L_2, along with capacitor C_1, form a three-pole low-pass filter. The conversion ratio does not depend on the number of poles present in the low-pass filter, and so the same steady-state output voltage should be obtained when a simpler low-pass filter is used. In Fig. 6.5(a), capacitor C_1 is removed. Inductors L_1 and L_2 are now in series, and can be combined into a single inductor as shown in Fig. 6.5(b). This converter, the noninverting buck–boost converter, continues to exhibit the conversion ratio given in Eq. (6.9).

The switches of the converter of Fig. 6.5(b) can also be simplified, leading to a negative output voltage. When the switches are in position 1, the converter reduces to Fig. 6.6(a). The inductor is connected to the input source V_g, and energy is transferred from the source to the inductor. When the

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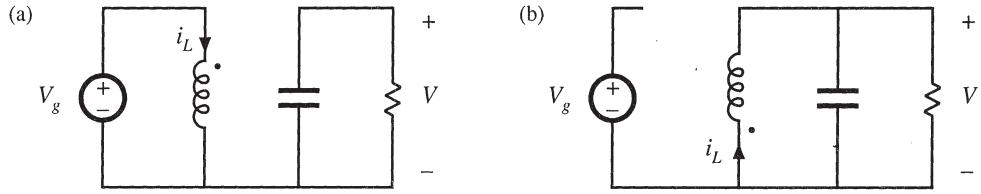


Fig. 6.6 Connections of the circuit of Fig. 6.5(b): (a) while the switches are in position 1, (b) while the switches are in position 2.

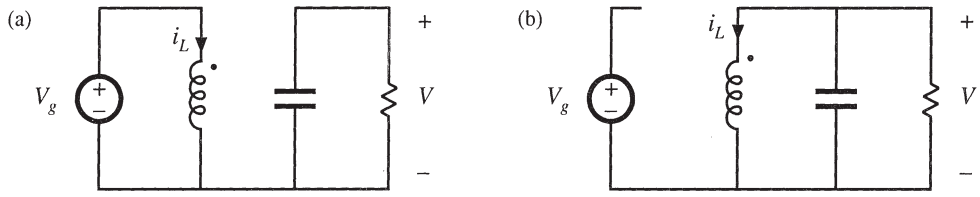


Fig. 6.7 Reversal of the output voltage polarity, by reversing the inductor connections while the switches are in position 2: (a) connections with the switches in position 1, (b) connections with the switches in position 2.

switches are in position 2, the converter reduces to Fig. 6.6(b). The inductor is then connected to the load, and energy is transferred from the inductor to the load. To obtain a negative output, we can simply reverse the polarity of the inductor during one of the subintervals (say, while the switches are in position 2). The individual circuits of Fig. 6.7 are then obtained, and the conversion ratio becomes

$$\frac{V}{V_g} = -\frac{D}{1-D} \tag{6.10}$$

Note that one side of the inductor is now always connected to ground, while the other side is switched between the input source and the load. Hence only one SPDT switch is needed, and the converter circuit of Fig. 6.8 is obtained. Figure 6.8 is recognized as the conventional buck–boost converter.

Thus, the buck–boost converter can be viewed as a cascade connection of buck and boost converters. The properties of the buck–boost converter are consistent with this viewpoint. Indeed, the equivalent circuit model of the buck-boost converter contains a 1:D (buck) dc transformer, followed by a D':1 (boost) dc transformer. The buck–boost converter inherits the pulsating input current of the buck converter, and the pulsating output current of the boost converter.

Other converters can be derived by cascade connections. The Ćuk converter (Fig. 2.20) was originally derived [1,2] by cascading a boost converter (converter 1), followed by a buck (converter 2). A negative output voltage is obtained by reversing the polarity of the internal capacitor connection during one of the subintervals; as in the buck–boost converter, this operation has the additional benefit of reducing the number of switches. The equivalent circuit model of the Ćuk converter contains a D':1 (boost)

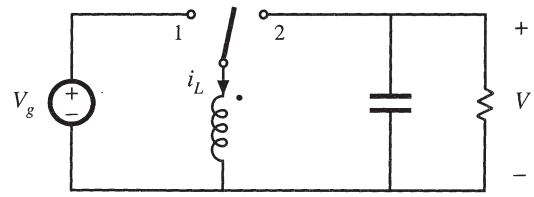


Fig. 6.8 Converter circuit obtained from the subcircuits of Fig. 6.7.

ideal dc transformer, followed by a 1:*D* (buck) ideal dc transformer. The Ćuk converter inherits the nonpulsating input current property of the boost converter, and the nonpulsating output current property of the buck converter.

6.1.3 Rotation of Three-Terminal Cell

The buck, boost, and buck–boost converters each contain an inductor that is connected to a SPDT switch. As illustrated in Fig. 6.9(a), the inductor-switch network can be viewed as a basic cell having the three terminals labeled *a*, *b*, and *c*. It was first pointed out in [1,2], and later in [3], that there are three distinct ways to connect this cell between the source and load. The connections *a–A b–B c–C* lead to the buck converter. The connections *a–C b–A c–B* amount to inversion of the source and load, and lead to the boost converter. The connections *a–A b–C c–B* lead to the buck-boost converter. So the buck, boost, and buck–boost converters could be viewed as being based on the same inductor-switch cell, with different source and load connections.

A dual three-terminal network, consisting of a capacitor-switch cell, is illustrated in Fig. 6.9(b). Filter inductors are connected in series with the source and load, such that the converter input and output currents are nonpulsating. There are again three possible ways to connect this cell between the source and load. The connections *a–A b–B c–C* lead to a buck converter with *L–C* input low-pass filter. The connections *a–B b–A c–C* coincide with inversion of source and load, and lead to a boost converter with an added output *L–C* filter section. The connections *a–A b–C c–B* lead to the Ćuk converter.

Rotation of more complicated three-terminal cells is explored in [4].

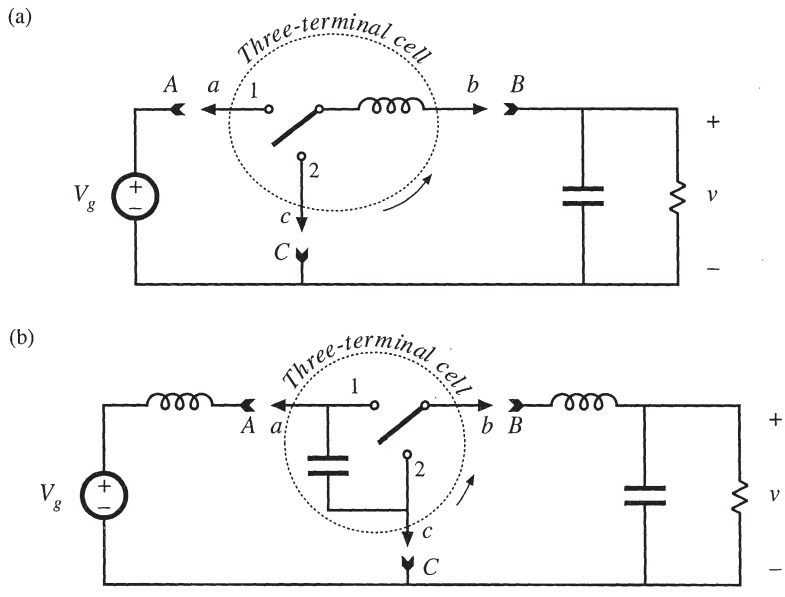


Fig. 6.9 Rotation of three-terminal switch cells: (a) switch/inductor cell, (b) switch/capacitor cell.

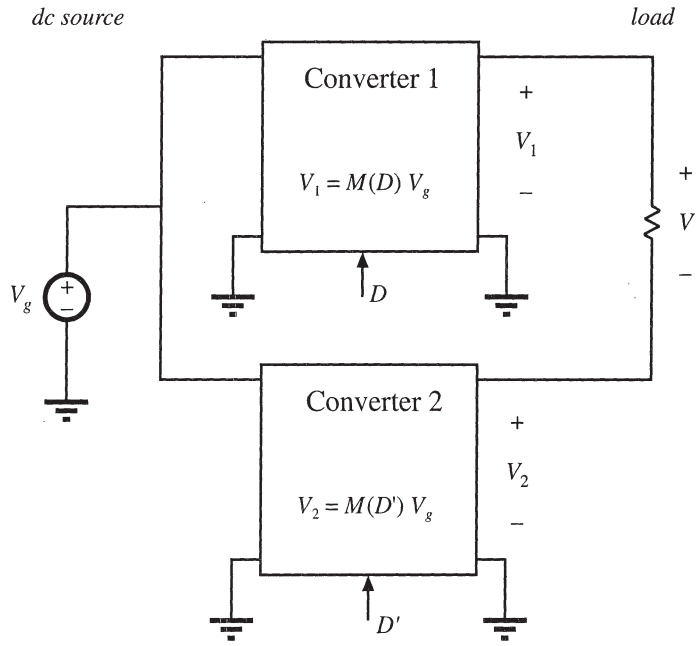


Fig. 6.10 Obtaining a bipolar output by differential connection of load.

6.1.4 Differential Connection of the Load

In inverter applications, where an ac output is required, a converter is needed that is capable of producing an output voltage of either polarity. By variation of the duty cycle in the correct manner, a sinusoidal output voltage having no dc bias can then be obtained. Of the converters studied so far in this chapter, the buck and the boost can produce only a positive unipolar output voltage, while the buck–boost and Ćuk converter produce only a negative unipolar output voltage. How can we derive converters that can produce bipolar output voltages?

A well-known technique for obtaining a bipolar output is the differential connection of the load across the outputs of two known converters, as illustrated in Fig. 6.10. If converter 1 produces voltage V_1, and converter 2 produces voltage V_2, then the load voltage V is given by

$$V = V_1 - V_2 \tag{6.11}$$

Although V_1 and V_2 may both individually be positive, the load voltage V can be either positive or negative. Typically, if converter 1 is driven with duty cycle D, then converter 2 is driven with its complement, D', so that when V_1 increases, V_2 decreases, and vice versa.

Several well-known inverter circuits can be derived using the differential connection. Let's realize converters 1 and 2 of Fig. 6.10 using buck converters. Figure 6.11(a) is obtained. Converter 1 is driven with duty cycle D, while converter 2 is driven with duty cycle D'. So when the SPDT switch of converter 1 is in the upper position, then the SPDT switch of converter 2 is in the lower position, and vice-versa. Converter 1 then produces output voltage $V_1 = DV_g$, while converter 2 produces output volt-

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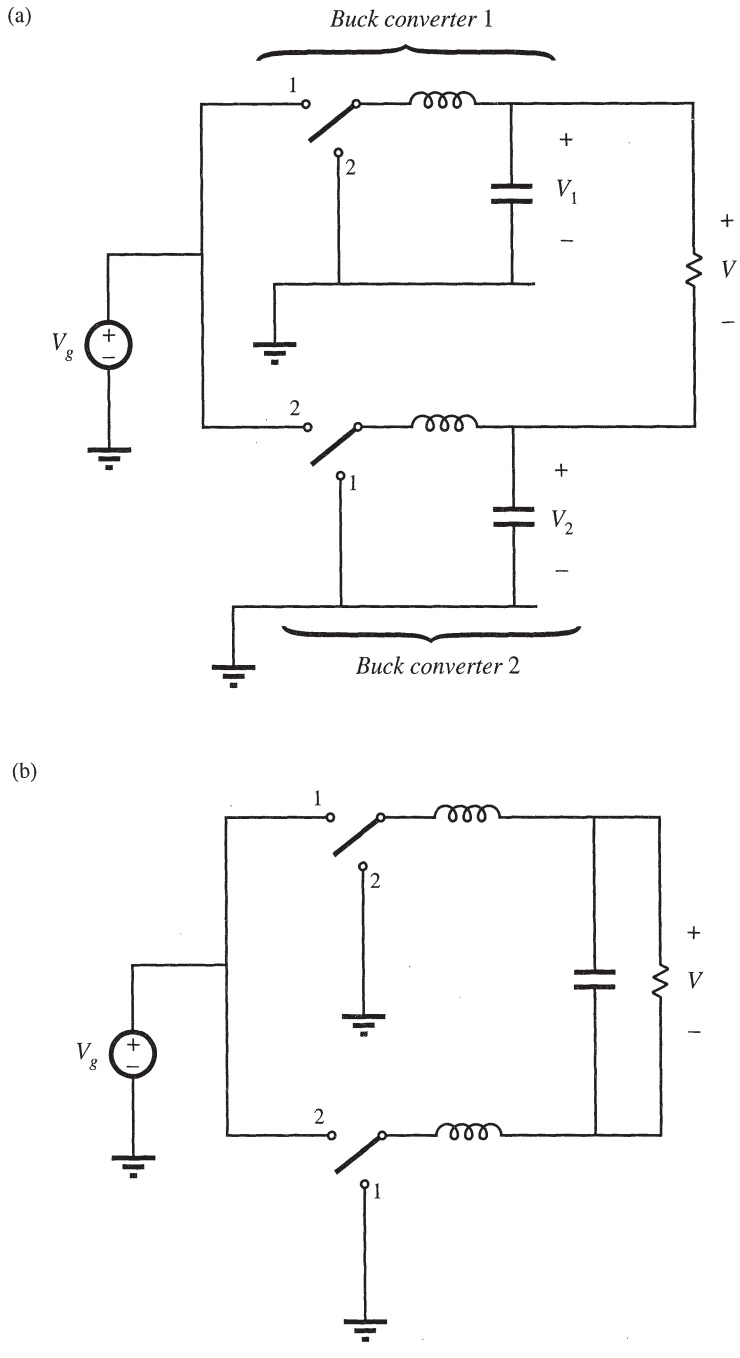


Fig. 6.11 Derivation of bridge inverter (H-bridge): (a) differential connection of load across outputs of buck converters, (b) bypassing load by capacitor, (c) combining series inductors, (d) circuit (c) redrawn in its usual form.

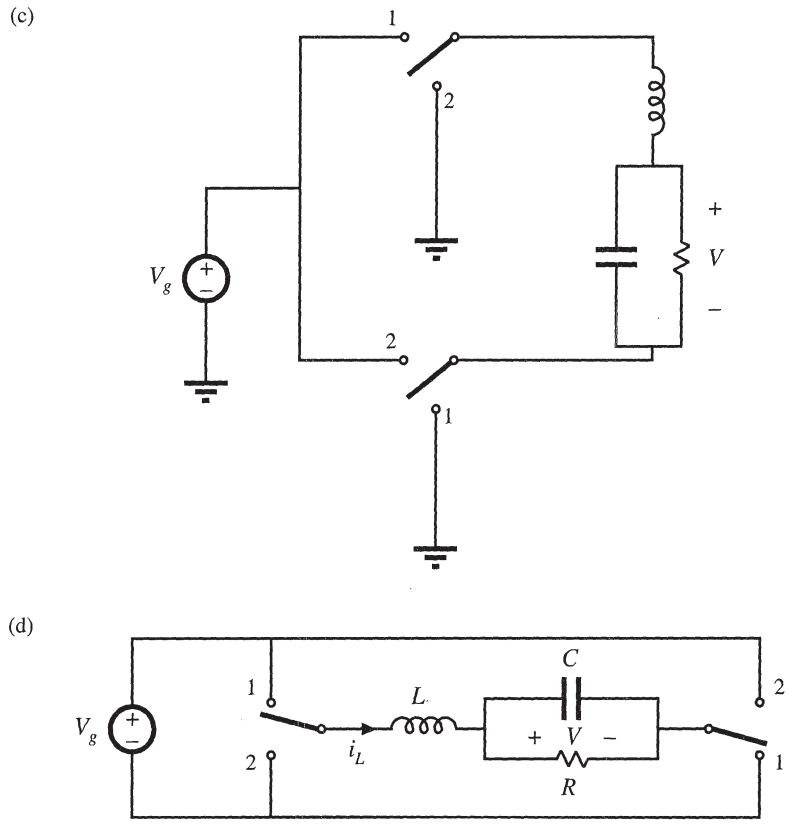


Fig. 6.11 Continued

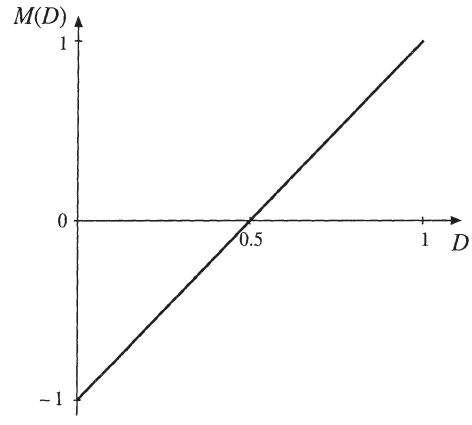


Fig. 6.12 Conversion ratio of the H-bridge inverter circuit.

age $V_2 = D'V_g$. The differential load voltage is

$$V = DV_g - D'V_g \tag{6.12}$$

Simplification leads to

$$V = (2D - 1)V_g \tag{6.13}$$

This equation is plotted in Fig. 6.12. It can be seen the output voltage is positive for $D > 0.5$, and negative for $D < 0.5$. If the duty cycle is varied sinusoidally about a quiescent operating point of 0.5, then the output voltage will be sinusoidal, with no dc bias.

The circuit of Fig. 6.11(a) can be simplified. It is usually desired to bypass the load directly with a capacitor, as in Fig. 6.11(b). The two inductors are now effectively in series, and can be combined into a single inductor as in Fig. 6.11(c). Figure 6.11(d) is identical to Fig. 6.11(c), but is redrawn for clarity. This circuit is commonly called the H-bridge, or bridge inverter circuit. Its use is widespread in servo amplifiers and single-phase inverters. Its properties are similar to those of the buck converter, from which it is derived.

Polyphase inverter circuits can be derived in a similar manner. A three-phase load can be connected differentially across the outputs of three dc–dc converters, as illustrated in Fig. 6.12. If the three-phase load is balanced, then the neutral voltage V_n will be equal to the average of the three converter output voltages:

$$V_n = \frac{1}{3}\left(V_1 + V_2 + V_3\right) \tag{6.14}$$

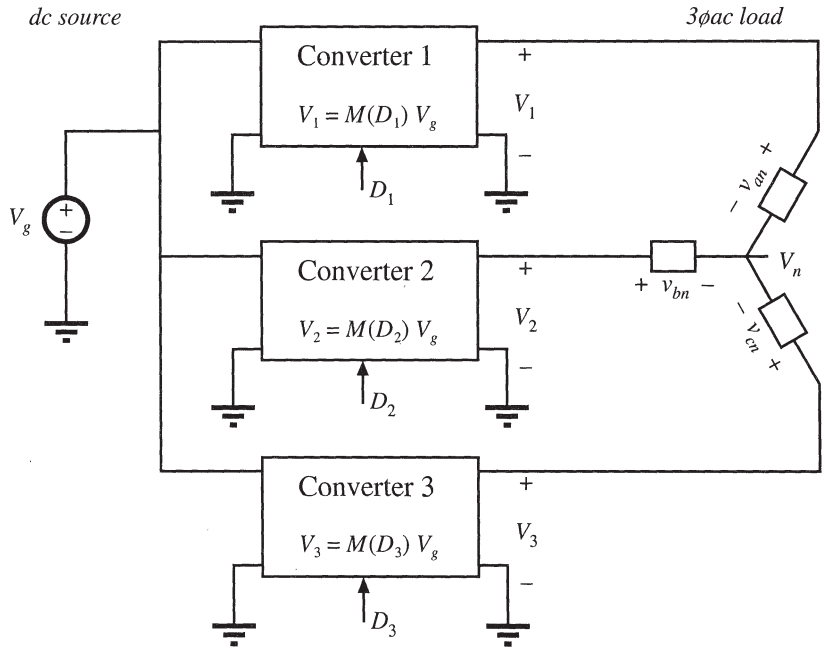


Fig. 6.12 Generation of dc–3ϕac inverter by differential connection of 3ϕ load.

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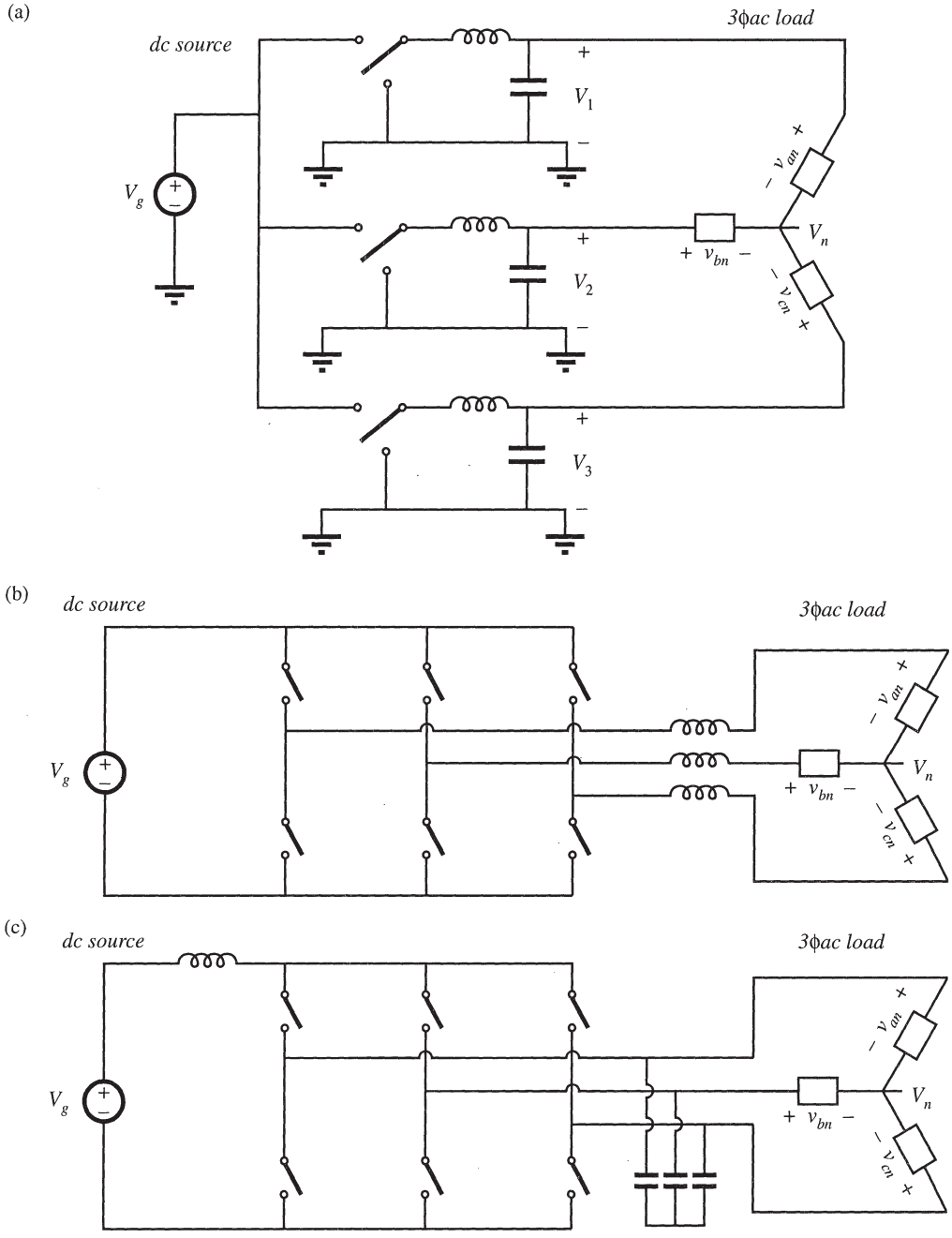


Fig. 6.13 Dc–3ϕac inverter topologies: (a) differential connection of 3ϕ load across outputs of buck converters; (b) simplification of low-pass filters to obtain the dc–3ϕac voltage-source inverter; (c) the dc–3ϕac current-source inverter.

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If the converter output voltages V_1, V_2, and V_3 contain the same dc bias, then this dc bias will also appear at the neutral point V_n. The phase voltages V_{an}, V_{bn}, and V_{cn} are given by

$$\begin{aligned} V_{an} &= V_1 - V_n \\ V_{bn} &= V_2 - V_n \\ V_{cn} &= V_3 - V_n \end{aligned} \tag{6.15}$$

It can be seen that the dc biases cancel out, and do not appear in V_{an}, V_{bn}, and V_{cn}.

Let us realize converters 1, 2, and 3 of Fig. 6.12 using buck converters. Figure 6.13(a) is then obtained. The circuit is re-drawn in Fig. 6.13(b) for clarity. This converter is known by several names, including the *voltage-source inverter* and the buck-derived three-phase bridge.

Inverter circuits based on dc–dc converters other than the buck converter can be derived in a similar manner. Figure 6.13(c) contains a three-phase current-fed bridge converter having a boost-type voltage conversion ratio, also known as the *current-source inverter*. Since most inverter applications require the capability to reduce the voltage magnitude, a dc–dc buck converter is usually cascaded at the dc input port of this inverter. Several other examples of three-phase inverters are given in [5–7], in which the converters are capable of both increasing and decreasing the voltage magnitude.

6.2 A SHORT LIST OF CONVERTERS

An infinite number of converters are possible, and hence it is not feasible to list them all. A short list is given here.

Let's consider first the class of single-input single-output converters, containing a single inductor. There are a limited number of ways in which the inductor can be connected between the source and load. If we assume that the switching period is divided into two subintervals, then the inductor should be connected to the source and load in one manner during the first subinterval, and in a different manner during the second subinterval. One can examine all of the possible combinations, to derive the complete set of converters in this class [8–10]. By elimination of redundant and degenerate circuits, one finds that there are eight converters, listed in Fig. 6.14. How the converters are counted can actually be a matter of semantics and personal preference; for example, many people in the field would not consider the noninverting buck–boost converter as distinct from the inverting buck–boost. Nonetheless, it can be said that a converter is defined by the connections between its reactive elements, switches, source, and load; by how the switches are realized; and by the numerical range of reactive element values.

The first four converters of Fig. 6.14, the buck, boost, buck-boost, and the noninverting buck-boost, have been previously discussed. These converters produce a unipolar dc output voltage. With these converters, it is possible to increase, decrease, and/or invert a dc voltage.

Converters 5 and 6 are capable of producing a bipolar output voltage. Converter 5, the H–bridge, has previously been discussed. Converter 6 is a nonisolated version of a push–pull current-fed converter [11–15]. This converter can also produce a bipolar output voltage; however, its conversion ratio $M(D)$ is a nonlinear function of duty cycle. The number of switch elements can be reduced by using a two-winding inductor as shown. The function of the inductor is similar to that of the flyback converter, discussed in the next section. When switch 1 is closed the upper winding is used, while when switch 2 is closed, current flows through the lower winding. The current flows through only one winding at any given instant, and the total ampere-turns of the two windings are a continuous function of time. Advantages of this converter are its ground-referenced load and its ability to produce a bipolar output voltage using only two SPST current-bidirectional switches. The isolated version and its variants have found

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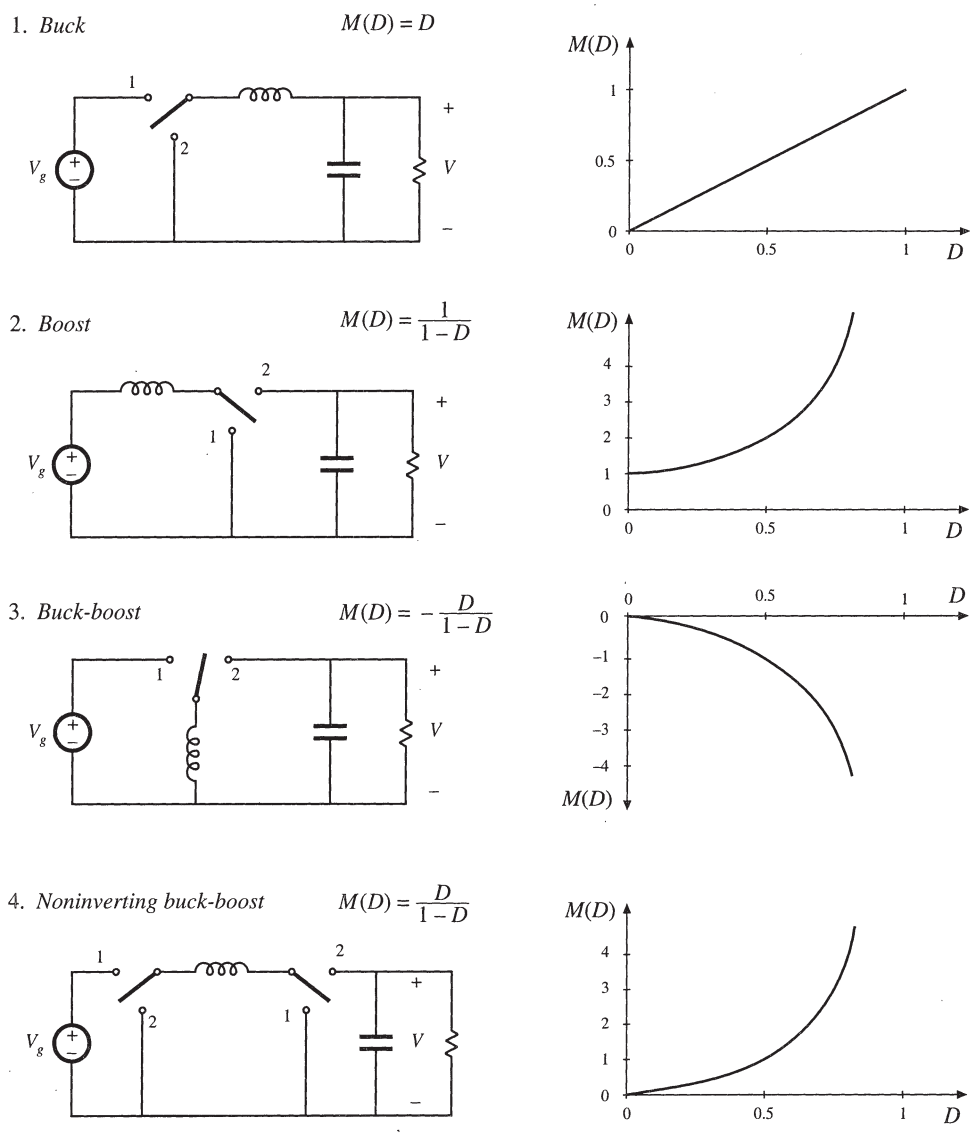


Fig. 6.14 Eight members of the basic class of single-input single-output converters containing a single inductor.

application in high-voltage dc power supplies.

Converters 7 and 8 can be derived as the inverses of converters 5 and 6. These converters are capable of interfacing an ac input to a dc output. The ac input current waveform can have arbitrary waveshape and power factor.

The class of single-input single-output converters containing two inductors is much larger. Several of its members are listed in Fig. 6.15. The Ćuk converter has been previously discussed and ana-

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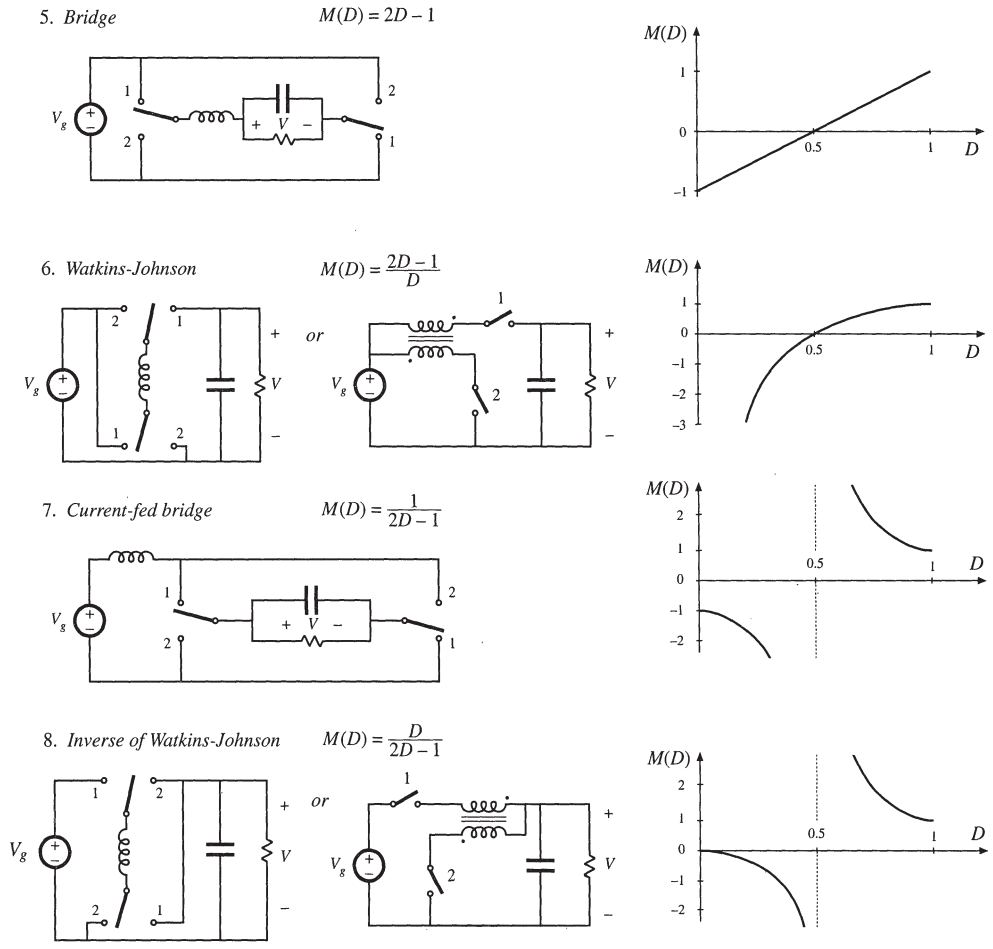


Fig. 6.14 Continued

lyzed. It has an inverting buck-boost characteristic, and exhibits nonpulsating input and output terminal currents. The SEPIC (single-ended primary inductance converter) [16], and its inverse, have noninverting buck–boost characteristics. The Ćuk and SEPIC also exhibit the desirable feature that the MOSFET source terminal is connected to ground; this simplifies the construction of the gate drive circuitry. Two-inductor converters having conversion ratios $M(D)$ that are biquadratic functions of the duty cycle D are also numerous. An example is converter 4 of Fig. 6.15 [17]. This converter can be realized using a single transistor and three diodes. Its conversion ratio is $M(D) = D^2$. This converter may find use in nonisolated applications that require a large step-down of the dc voltage, or in applications having wide variations in operating point.

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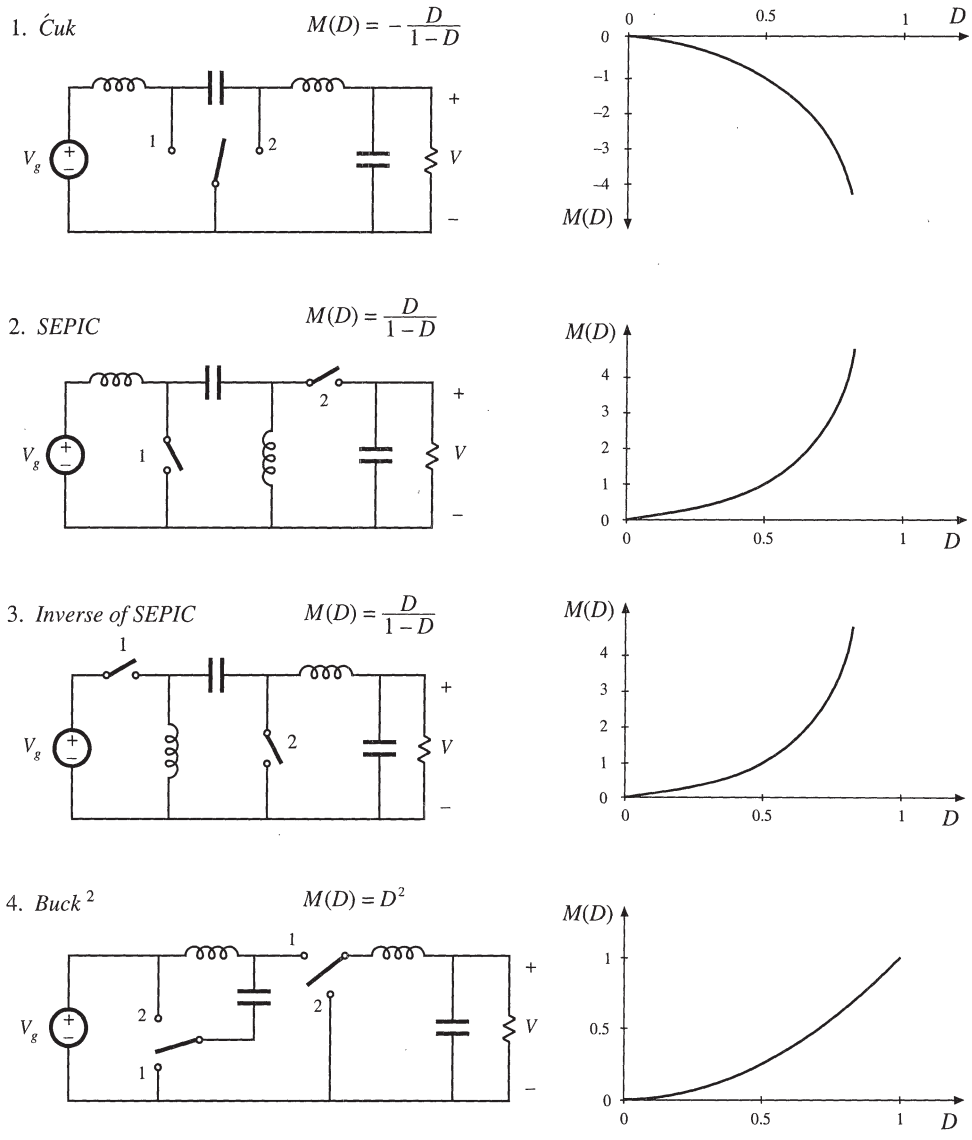


Fig. 6.15 Several members of the basic class of single-input single-output converters containing two inductors.

6.3 TRANSFORMER ISOLATION

In a large number of applications, it is desired to incorporate a transformer into a switching converter, to obtain dc isolation between the converter input and output. For example, in off-line applications (where the converter input is connected to the ac utility system), isolation is usually required by regulatory agen-

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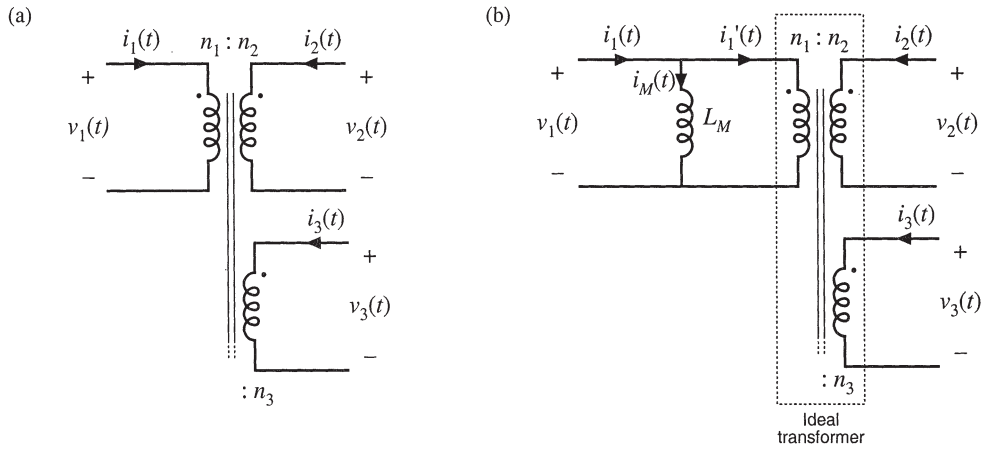


Fig. 6.16 Simplified model of a multiple-winding transformer: (a) schematic symbol, (b) equivalent circuit containing a magnetizing inductance and ideal transformer.

cies. Isolation could be obtained in these cases by simply connecting a 50 Hz or 60 Hz transformer at the converter ac input. However, since transformer size and weight vary inversely with frequency, significant improvements can be made by incorporating the transformer into the converter, so that the transformer operates at the converter switching frequency of tens or hundreds of kilohertz.

When a large step-up or step-down conversion ratio is required, the use of a transformer can allow better converter optimization. By proper choice of the transformer turns ratio, the voltage or current stresses imposed on the transistors and diodes can be minimized, leading to improved efficiency and lower cost.

Multiple dc outputs can also be obtained in an inexpensive manner, by adding multiple secondary windings and converter secondary-side circuits. The secondary turns ratios are chosen to obtain the desired output voltages. Usually only one output voltage can be regulated via control of the converter duty cycle, so wider tolerances must be allowed for the auxiliary output voltages. *Cross regulation* is a measure of the variation in an auxiliary output voltage, given that the main output voltage is perfectly regulated [18–20].

A physical multiple-winding transformer having turns ratio $n_1:n_2:n_3:...$ is illustrated in Fig. 6.16(a). A simple equivalent circuit is illustrated in Fig. 6.16(b), which is sufficient for understanding the operation of most transformer-isolated converters. The model assumes perfect coupling between windings and neglects losses; more accurate models are discussed in a later chapter. The ideal transformer obeys the relationships

$$\frac{v_1(t)}{n_1} = \frac{v_2(t)}{n_2} = \frac{v_3(t)}{n_3} = ...$$
$$0 = n_1 i_1'(t) + n_2 i_2(t) + n_3 i_3(t) + ... \tag{6.16}$$

In parallel with the ideal transformer is an inductance L_M, called the *magnetizing inductance*, referred to the transformer primary in the figure.

Physical transformers must contain a magnetizing inductance. For example, suppose we disconnect all windings except for the primary winding. We are then left with a single winding on a magnetic core—an inductor. Indeed, the equivalent circuit of Fig. 6.16(b) predicts this behavior, via the magnetizing inductance.

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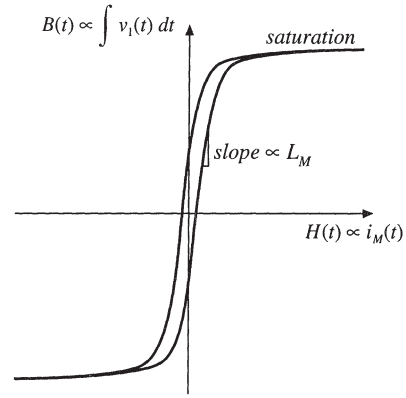


Fig. 6.17 *B–H* characteristics of transformer core.

The magnetizing current $i_M(t)$ is proportional to the magnetic field $H(t)$ inside the transformer core. The physical *B–H* characteristics of the transformer core material, illustrated in Fig. 6.17, govern the magnetizing current behavior. For example, if the magnetizing current $i_M(t)$ becomes too large, then the magnitude of the magnetic field $H(t)$ causes the core to saturate. The magnetizing inductance then becomes very small in value, effectively shorting out the transformer.

The presence of the magnetizing inductance explains why transformers do not work in dc circuits: at dc, the magnetizing inductance has zero impedance, and shorts out the windings. In a well-designed transformer, the impedance of the magnetizing inductance is large in magnitude over the intended range of operating frequencies, such that the magnetizing current $i_M(t)$ has much smaller magnitude than $i_1(t)$. Then $i_1'(t) \approx i_1(t)$, and the transformer behaves nearly as an ideal transformer. It should be emphasized that the magnetizing current $i_M(t)$ and the primary winding current $i_1(t)$ are independent quantities.

The magnetizing inductance must obey all of the usual rules for inductors. In the model of Fig. 6.16(b), the primary winding voltage $v_1(t)$ is applied across L_M, and hence

$$v_1(t) = L_M \frac{di_M(t)}{dt} \tag{6.17}$$

Integration leads to

$$i_M(t) - i_M(0) = \frac{1}{L_M} \int_0^t v_1(\tau) d\tau \tag{6.18}$$

So the magnetizing current is determined by the integral of the applied winding voltage. The principle of inductor volt-second balance also applies: when the converter operates in steady-state, the dc component of voltage applied to the magnetizing inductance must be zero:

$$0 = \frac{1}{T_s} \int_0^{T_s} v_1(t) dt \tag{6.19}$$

Since the magnetizing current is proportional to the integral of the applied winding voltage, it is important that the dc component of this voltage be zero. Otherwise, during each switching period there will be a net increase in magnetizing current, eventually leading to excessively large currents and transformer saturation.

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The operation of converters containing transformers may be understood by inserting the model of Fig. 6.16(b) in place of the transformer in the converter circuit. Analysis then proceeds as described in the previous chapters, treating the magnetizing inductance as any other inductor of the converter.

Practical transformers must also contain leakage inductance. A small part of the flux linking a winding may not link the other windings. In the two-winding transformer, this phenomenon may be modeled with small inductors in series with the windings. In most isolated converters, leakage inductance is a nonideality that leads to switching loss, increased peak transistor voltage, and that degrades cross-regulation, but otherwise has no influence on basic converter operation.

There are several ways of incorporating transformer isolation into a dc–dc converter. The full-bridge, half-bridge, forward, and push-pull converters are commonly used isolated versions of the buck converter. Similar isolated variants of the boost converter are known. The flyback converter is an isolated version of the buck–boost converter. These isolated converters, as well as isolated versions of the SEPIC and the Ćuk converter, are discussed in this section.

6.3.1 Full-Bridge and Half-Bridge Isolated Buck Converters

The full-bridge transformer-isolated buck converter is sketched in Fig. 6.18(a). A version containing a center-tapped secondary winding is shown; this circuit is commonly used in converters producing low output voltages. The two halves of the center-tapped secondary winding may be viewed as separate windings, and hence we can treat this circuit element as a three-winding transformer having turns ratio $1{:}n{:}n$. When the transformer is replaced by the equivalent circuit model of Fig. 6.16(b), the circuit of Fig.

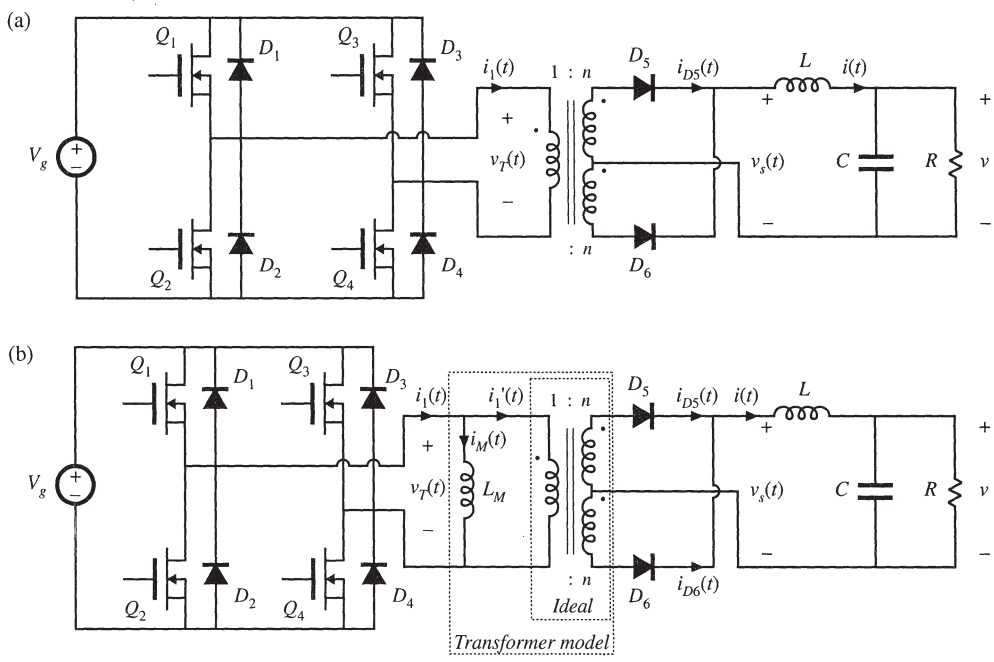


Fig. 6.18 Full-bridge transformer-isolated buck converter: (a) schematic diagram, (b) replacement of transformer with equivalent circuit model.

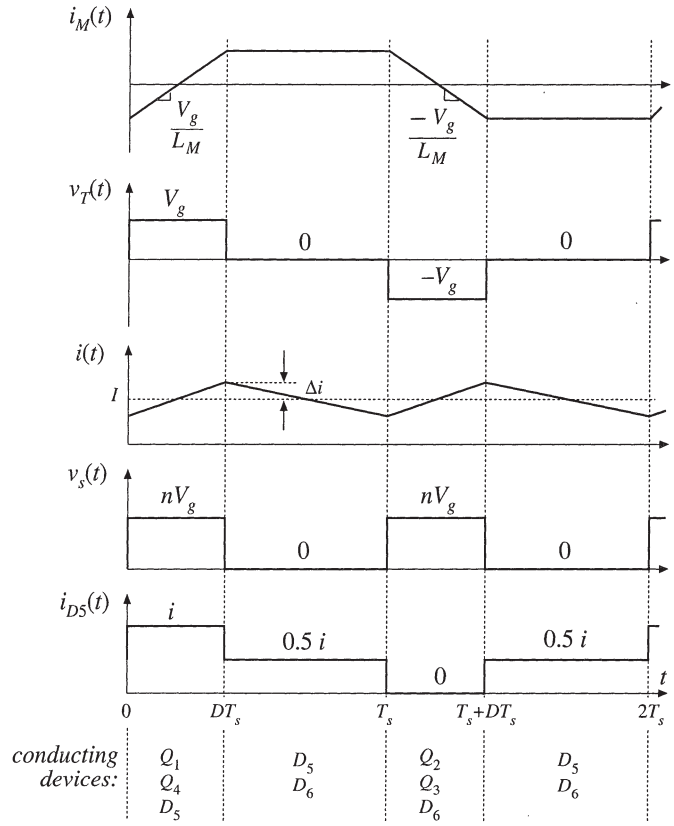


Fig. 6.19 Waveforms of the full-bridge transformer-isolated buck converter.

6.18(b) is obtained. Typical waveforms are illustrated in Fig. 6.19. The output portion of the converter is similar to the nonisolated buck converter—compare the $v_s(t)$ and $i(t)$ waveforms of Fig. 6.19 with Figs. 2.1(b) and 2.10.

During the first subinterval $0 < t < DT_s$, transistors Q_1 and Q_4 conduct, and the transformer primary voltage is $v_T = V_g$. This positive voltage causes the magnetizing current $i_M(t)$ to increase with a slope of V_g/L_M. The voltage appearing across each half of the center-tapped secondary winding is nV_g, with the polarity mark at positive potential. Diode D_5 is therefore forward-biased, and D_6 is reverse-biased. The voltage $v_s(t)$ is then equal to nV_g, and the output filter inductor current $i(t)$ flows through diode D_5.

Several transistor control schemes are possible for the second subinterval $DT_s < t < T_s$. In the most common scheme, all four transistors are switched off, and hence the transformer voltage is $v_T = 0$. Alternatively, transistors Q_2 and Q_4 could conduct, or transistors Q_1 and Q_3 could conduct. In any event, diodes D_5 and D_6 are both forward-biased during this subinterval; each diode conducts approximately one-half of the output filter inductor current.

Actually, the diode currents i_{D5} and i_{D6} during the second subinterval are functions of both the output inductor current and the transformer magnetizing current. In the ideal case (no magnetizing current), the transformer causes $i_{D5}(t)$ and $i_{D6}(t)$ to be equal in magnitude since, if $i_1'(t) = 0$, then $ni_{D5}(t) = ni_{D6}(t)$. But the sum of the two diode currents is equal to the output inductor current:

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$$i_{D5}(t) + i_{D6}(t) = i(t) \tag{6.20}$$

Therefore, it must be true that $i_{D5} = i_{D6} = 0.5i$ during the second subinterval. In practice, the diode currents differ slightly from this result, because of the nonzero magnetizing current.

The ideal transformer currents in Fig. 6.18(b) obey

$$i_1'(t) - n i_{D5}(t) + n i_{D6}(t) = 0 \tag{6.21}$$

The node equation at the primary of the ideal transformer is

$$i_1(t) = i_M(t) + i_1'(t) \tag{6.22}$$

Elimination of $i_1'(t)$ from Eqs. (6.21) and (6.22) leads to

$$i_1(t) - n i_{D5}(t) + n i_{D6}(t) = i_M(t) \tag{6.23}$$

Equations (6.23) and (6.20) describe, in the general case, the transformer winding currents during the second subinterval. According to Eq. (6.23), the magnetizing current $i_M(t)$ may flow through the primary winding, through one of the secondary windings, or it may divide between all three of these windings. How the division occurs depends on the i–v characteristics of the conducting transistors and diodes, and on the transformer leakage inductances. In the case where $i_1 = 0$, the solution to Eqs. (6.20) and (6.23) is

$$\begin{aligned} i_{D5}(t) &= \frac{1}{2} i(t) - \frac{1}{2n} i_M(t) \\ i_{D6}(t) &= \frac{1}{2} i(t) + \frac{1}{2n} i_M(t) \end{aligned} \tag{6.24}$$

Provided that $i_M \ll ni$, then i_{D5} and i_{D6} are each approximately $0.5i$.

The next switching period, $T_s < t < 2T_s$, proceeds in a similar manner, except that the transformer is excited with voltage of the opposite polarity. During $T_s < t < (T_s + DT_s)$, transistors Q_2 and Q_3 and diode D_6 conduct. The applied transformer primary voltage is $v_T = -V_g$, which causes the magnetizing current to decrease with slope $-V_g/L_M$. The voltage $v_s(t)$ is equal to nV_g, and the output inductor current $i(t)$ flows through diode D_6. Diodes D_5 and D_6 again both conduct during $(T_s + DT_s) < t < 2T_s$, with operation similar to subinterval 2 described previously. It can be seen that the switching ripple in the output filter elements has frequency $f_s = 1/T_s$. However, the transformer waveforms have frequency $0.5f_s$.

By application of the principle of inductor volt-second balance to the magnetizing inductance, the average value of the transformer voltage $v_T(t)$ must be zero when the converter operates in steady state. During the first switching period, positive volt-seconds are applied to the transformer, approximately equal to

$$\left[V_g - \left(Q_1 \text{ and } Q_4 \text{ forward voltage drops}\right)\right]\left(Q_1 \text{ and } Q_4 \text{ conduction time}\right) \tag{6.25}$$

During the next switching period, negative volt-seconds are applied to the transformer, given by

$$-\left[V_g - \left(Q_2 \text{ and } Q_3 \text{ forward voltage drops}\right)\right]\left(Q_2 \text{ and } Q_3 \text{ conduction time}\right) \tag{6.26}$$

The net volt-seconds, that is, the sum of Eqs. (6.25) and (6.26), should equal zero. While the full bridge scheme causes this to be approximately true, in practice there exist imbalances such as small differences in the transistor forward voltage drops or in the transistor switching times, so that $\langle v_T \rangle$ is small but nonzero. In consequence, during every two switching periods there is a net increase in the magnitude of the magnetizing current. This increase can cause the transistor forward voltage drops to change such that small imbalances are compensated. However, if the imbalances are too large, then the magnetizing current becomes large enough to saturate the transformer.

Transformer saturation under steady-state conditions can be avoided by placing a capacitor in series with the transformer primary. Imbalances then induce a dc voltage component across the capacitor, rather than across the transformer primary. Another solution is the use of current-programmed control, discussed in a later chapter. The series capacitor is omitted when current-programmed control is used.

By application of the principle of volt-second balance to the output filter inductor L, the dc load voltage must be equal to the dc component of $v_s(t)$:

$$V = \langle v_s \rangle \tag{6.27}$$

By inspection of the $v_s(t)$ waveform in Fig. 6.19, $\langle v_s \rangle = nDV_g$. Hence,

$$V = nDV_g \tag{6.28}$$

So as in the buck converter, the output voltage can be controlled by variation of the transistor duty cycle D. An additional increase or decrease of the voltage can be obtained via the physical transformer turns ratio n. Equation (6.28) is valid for operation in the continuous conduction mode; as in the nonisolated buck converter, the full-bridge and half-bridge converters can operate in discontinuous conduction mode at light load. The converter can operate over essentially the entire range of duty cycles $0 \le D < 1$.

Transistors Q_1 and Q_2 must not conduct simultaneously; doing so would short out the dc source V_g, causing a *shoot-through* current spike. This transistor *cross-conduction* condition can lead to low efficiency and transistor failure. Cross conduction can be prevented by introduction of delay between the turn-off of one transistor and the turn-on of the next transistor. Diodes D_1 to D_4 ensure that the peak transistor voltage is limited to the dc input voltage V_g, and also provide a conduction path for the transformer magnetizing current at light load. Details of the switching transitions of the full-bridge circuit are discussed further in a later chapter, in conjunction with zero-voltage switching phenomena.

The full-bridge configuration is typically used in switching power supplies at power levels of approximately 750 W and greater. It is usually not used at lower power levels because of its high parts count—four transistors and their associated drive circuits are required. The utilization of the transformer is good, leading to small transformer size. In particular, the utilization of the transformer core is very good, since the transformer magnetizing current can be both positive and negative. Hence, the entire core B–H loop can be used. However, in practice, the flux swing is usually limited by core loss. The transformer primary winding is effectively utilized. But the center-tapped secondary winding is not, since each half of the center-tapped winding transmits power only during alternate switching periods. Also, the secondary winding currents during subinterval 2 lead to winding power loss, but not to transmittal of energy to the load. Design of the transformer of the full-bridge configuration is discussed in detail in a later chapter.

The half-bridge transformer-isolated buck converter is illustrated in Fig. 6.20. Typical waveforms are illustrated in Fig. 6.21. This circuit is similar to the full-bridge of Fig. 6.18(a), except transistors Q_3 and Q_4, and their antiparallel diodes, have been replaced with large-value capacitors C_a and C_b. By volt-second balance of the transformer magnetizing inductance, the dc voltage across capacitor C_b is equal to the dc component of the voltage across transistor Q_2, or $0.5V_g$. The transformer primary voltage

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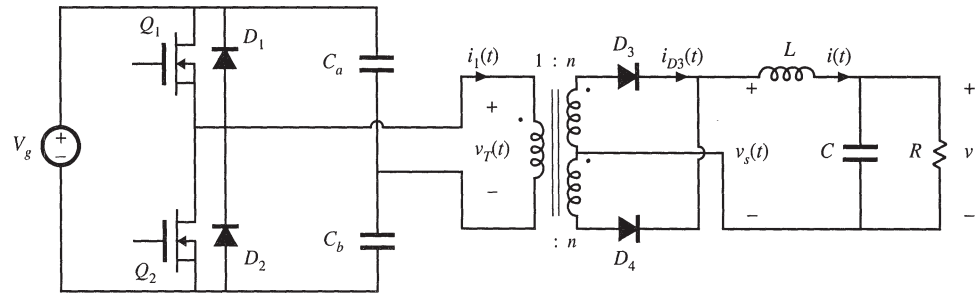


Fig. 6.20 Half-bridge transformer-isolated buck converter.

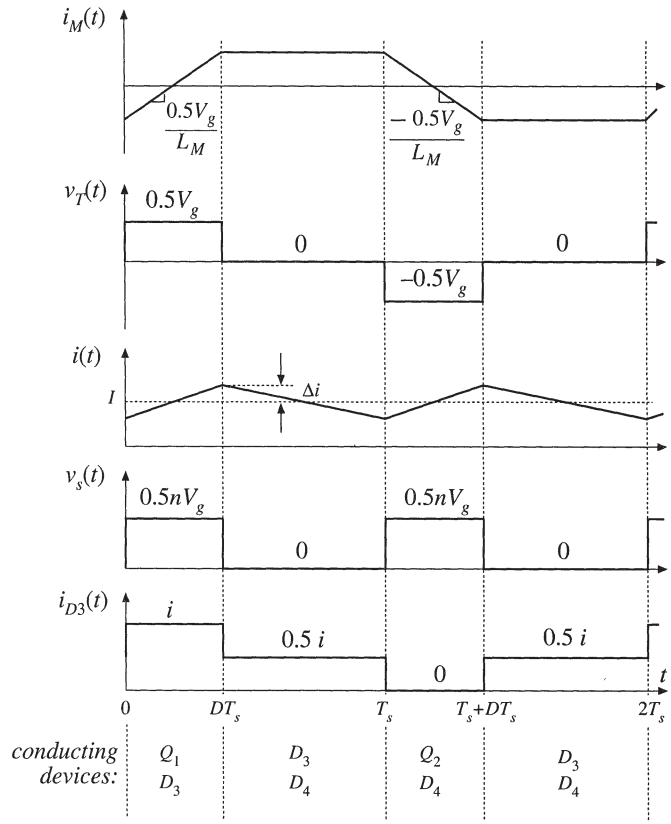


Fig. 6.21 Waveforms of the half-bridge transformer-isolated buck converter.

$v_T(t)$ is then $0.5V_g$ when transistor Q_1 conducts, and $-0.5V_g$ when transistor Q_2 conducts. The magnitude of $v_T(t)$ is half as large as in the full-bridge configuration, with the result that the output voltage is reduced by a factor of 0.5:

$$V = 0.5nDV_g \tag{6.29}$$

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The factor of 0.5 can be compensated for by doubling the transformer turns ratio n. However, this causes the transistor currents to double.

So the half-bridge configuration needs only two transistors rather than four, but these two transistors must handle currents that are twice as large as those of the full-bridge circuit. In consequence, the half-bridge configuration finds application at lower power levels, for which transistors with sufficient current rating are readily available, and where low parts count is important. Utilization of the transformer core and windings is essentially the same as in the full-bridge, and the peak transistor voltage is clamped to the dc input voltage V_g by diodes D_1 and D_2. It is possible to omit capacitor C_a if desired. The current-programmed mode generally does not work with half-bridge converters.

6.3.2 Forward Converter

The forward converter is illustrated in Fig. 6.22. This transformer-isolated converter is based on the buck converter. It requires a single transistor, and hence finds application at power levels lower than those commonly encountered in the full-bridge and half-bridge configurations. Its nonpulsating output current, shared with other buck-derived converters, makes the forward converter well suited for applications involving high output currents. The maximum transistor duty cycle is limited in value; for the common choice $n_1 = n_2$, the duty cycle is limited to the range $0 \le D < 0.5$.

The transformer magnetizing current is reset to zero while the transistor is in the off-state. How this occurs can be understood by replacing the three-winding transformer in Fig. 6.22 with the equivalent circuit of Fig. 6.16(b). The resulting circuit is illustrated in Fig. 6.23, and typical waveforms are given in Fig. 6.24. The magnetizing inductance L_M, in conjunction with diode D_1, must operate in the discontinuous conduction mode. The output inductor L, in conjunction with diode D_3, may operate in either continuous or discontinuous conduction mode. The waveforms of Fig. 6.24 are sketched for continuous mode operation of inductor L. During each switching period, three subintervals then occur as illustrated in Fig. 6.25.

During subinterval 1, transistor Q_1 conducts and the circuit of Fig. 6.25(a) is obtained. Diode D_2 becomes forward-biased, while diodes D_1 and D_3 are reverse-biased. Voltage V_g is applied to the transformer primary winding, and hence the transformer magnetizing current $i_M(t)$ increases with a slope of V_g/L_M as illustrated in Fig. 6.24. The voltage across diode D_3 is equal to V_g, multiplied by the turns ratio n_3/n_1.

The second subinterval begins when transistor Q_1 is switched off. The circuit of Fig. 6.25(b) is

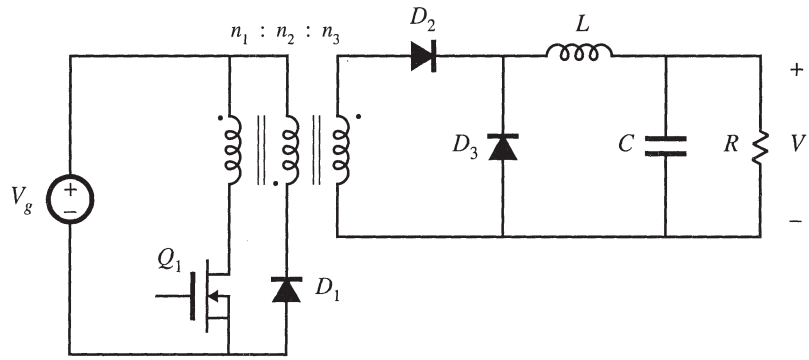


Fig. 6.22 Single-transistor forward converter.

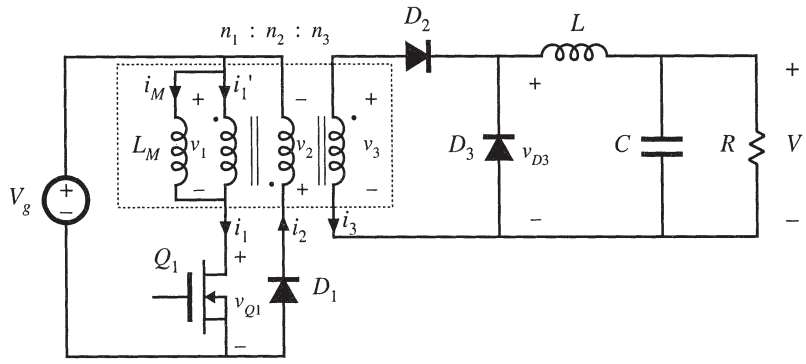


Fig. 6.23 Forward converter, with transformer equivalent circuit model.

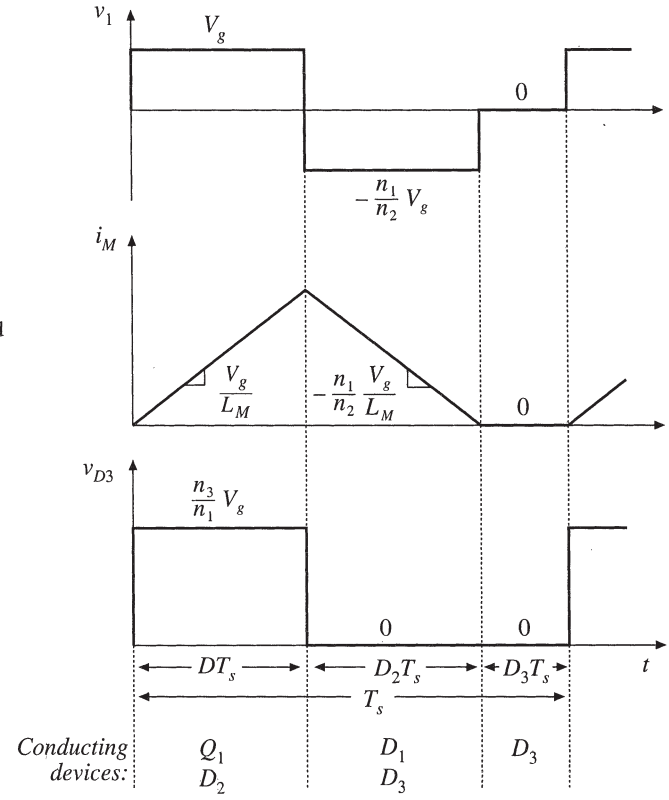


Fig. 6.24 Waveforms of the forward converter.

then obtained. The transformer magnetizing current $i_M(t)$ at this instant is positive, and must continue to flow. Since transistor Q_1 is off, the equivalent circuit model predicts that the magnetizing current must flow into the primary of the ideal transformer. It can be seen that $n_1 i_M$ ampere-turns flow out of the polarity mark of the primary winding. Hence, according to Eq. (6.16), an equal number of total ampere-turns must flow into the polarity marks of the other windings. Diode D_2 prevents current from flowing into the

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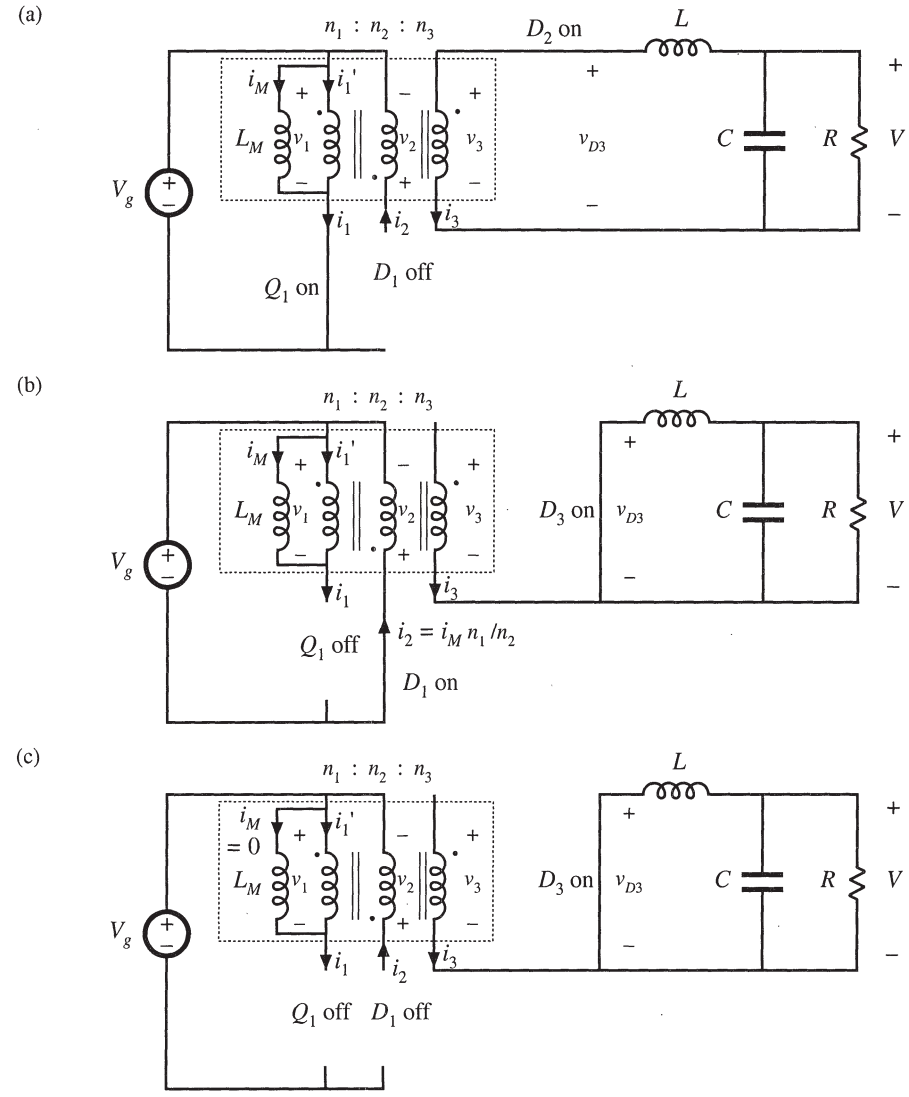


Fig. 6.25 Forward converter circuit: (a) during subinterval 1, (b) during subinterval 2, (c) during subinterval 3.

polarity mark of winding 3. Hence, the current $i_M n_1/n_2$ must flow into the polarity mark of winding 2. So diode D_1 becomes forward-biased, while diode D_2 is reverse-biased. Voltage V_g is applied to winding 2, and hence the voltage across the magnetizing inductance is $-V_g n_1/n_2$, referred to winding 1. This negative voltage causes the magnetizing current to decrease, with a slope of $-V_g n_1/n_2 L_M$. Since diode D_2 is reverse-biased, diode D_3 must turn on to conduct the output inductor current $i(t)$.

When the magnetizing current reaches zero, diode D_1 becomes reverse-biased. Subinterval 3 then begins, and the circuit of Fig. 6.25(c) is obtained. Elements Q_1, D_1, and D_2 operate in the off state, and the magnetizing current remains at zero for the balance of the switching period.

By application of the principle of inductor volt-second balance to the transformer magnetizing

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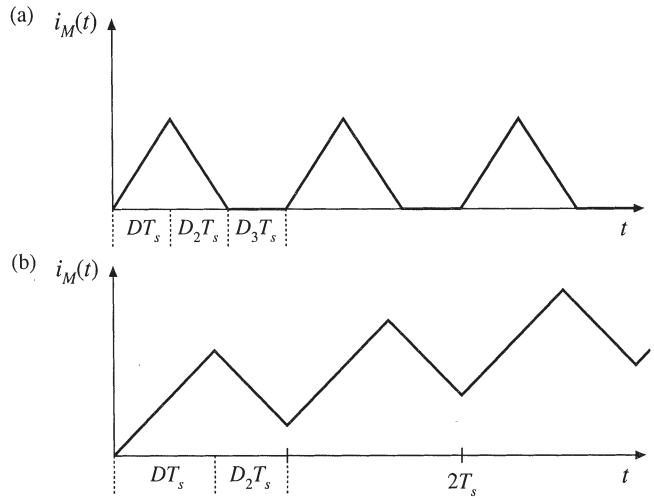


Fig. 6.26 Magnetizing current waveform, forward converter: (a) DCM, $D < 0.5$; (b) CCM, $D > 0.5$.

inductance, the primary winding voltage $v_1(t)$ must have zero average. Referring to Fig. 6.24, the average of $v_1(t)$ is given by

$$\langle v_1 \rangle = D(V_g) + D_2(-V_g n_1/n_2) + D_3(0) = 0 \tag{6.30}$$

Solution for the duty cycle D_2 yields

$$D_2 = \frac{n_2}{n_1} D \tag{6.31}$$

Note that the duty cycle D_3 cannot be negative. But since $D + D_2 + D_3 = 1$, we can write

$$D_3 = 1 - D - D_2 \geq 0 \tag{6.32}$$

Substitution of Eq. (6.31) into Eq. (6.32) leads to

$$D_3 = 1 - D\left(1 + \frac{n_2}{n_1}\right) \geq 0 \tag{6.33}$$

Solution for D then yields

$$D \leq \frac{1}{1 + \frac{n_2}{n_1}} \tag{6.34}$$

So the maximum duty cycle is limited. For the common choice $n_1 = n_2$, the limit becomes

$$D \leq \frac{1}{2} \tag{6.35}$$

If this limit is violated, then the transistor off-time is insufficient to reset the transformer magnetizing current to zero before the end of the switching period. Transformer saturation may then occur.

The transformer magnetizing current waveform $i_M(t)$ is illustrated in Fig. 6.26, for the typical

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case where $n_1 = n_2$. Figure 6.26(a) illustrates operation with $D < 0.5$. The magnetizing inductance, in conjunction with diode D_1, operates in the discontinuous conduction mode, and $i_M(t)$ is reset to zero before the end of each switching period. Figure 6.26(b) illustrates what happens when the transistor duty cycle D is greater than 0.5. There is then no third subinterval, and the magnetizing inductance operates in continuous conduction mode. Furthermore, subinterval 2 is not long enough to reset the magnetizing current to zero. Hence, there is a net increase of $i_M(t)$ over each switching period. Eventually, the magnetizing current will become large enough the saturate the transformer.

The converter output voltage can be found by application of the principle of inductor volt-second balance to inductor L. The voltage across inductor L must have zero dc component, and therefore the dc output voltage V is equal to the dc component of diode D_3 voltage $v_{D3}(t)$. The waveform $v_{D3}(t)$ is illustrated in Fig. 6.24. It has an average value of

$$\langle v_{D3} \rangle = V = \frac{n_3}{n_1} D V_g \tag{6.36}$$

This is the solution of the forward converter in the continuous conduction mode. The solution is subject to the constraint given in Eq. (6.34).

It can be seen from Eq. (6.34) that the maximum duty cycle could be increased by decreasing the turns ratio n_2/n_1. This would cause $i_M(t)$ to decrease more quickly during subinterval 2, resetting the transformer faster. Unfortunately, this also increases the voltage stress applied to transistor Q_1. The maximum voltage applied to transistor Q_1 occurs during subinterval 2; solution of the circuit of Fig. 6.25(b) for this voltage yields

$$\max\left(v_{Q1}\right) = V_g\left(1 + \frac{n_1}{n_2}\right) \tag{6.37}$$

For the common choice $n_1 = n_2$, the voltage applied to the transistor during subinterval 2 is $2V_g$. In practice, a somewhat higher voltage is observed, due to ringing associated with the transformer leakage inductance. So decreasing the turns ratio n_2/n_1 allows increase of the maximum transistor duty cycle, at the expense of increased transistor blocking voltage.

A two-transistor version of the forward converter is illustrated in Fig. 6.27. Transistors Q_1 and Q_2 are controlled by the same gate drive signal, such that they both conduct during subinterval 1, and are off during subintervals 2 and 3. The secondary side of the converter is identical to the single-transistor forward converter; diode D_3 conducts during subinterval 1, while diode D_4 conducts during subintervals 2 and 3. During subinterval 2, the magnetizing current $i_M(t)$ forward-biases diodes D_1 and D_2. The trans-

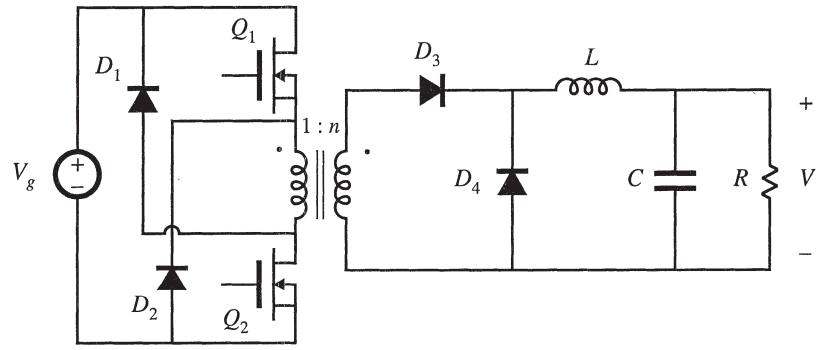


Fig. 6.27 Two-transistor forward converter.

former primary winding is then connected to V_g, with polarity opposite that of subinterval 1. The magnetizing current then decreases, with slope $-V_g/L_M$. When the magnetizing current reaches zero, diodes D_1 and D_2 become reverse-biased. The magnetizing current then remains at zero for the balance of the switching period. So operation of the two-transistor forward converter is similar to the single-transistor forward converter, in which $n_1 = n_2$. The duty cycle is limited to $D < 0.5$. This converter has the advantage that the transistor peak blocking voltage is limited to V_g, and is clamped by diodes D_1 and D_2. Typical power levels of the two-transistor forward converter are similar to those of the half-bridge configuration.

The utilization of the transformer of the forward converter is quite good. Since the transformer magnetizing current cannot be negative, only half of the core *B–H* loop can be used. This would seemingly imply that the transformer cores of forward converters should be twice as large as those of full- or half-bridge converters. However, in modern high-frequency converters, the flux swing is constrained by core loss rather than by the core material saturation flux density. In consequence, the utilization of the transformer core of the forward converter can be as good as in the full- or half-bridge configurations. Utilization of the primary and secondary windings of the transformer is better than in the full-bridge, half-bridge, or push-pull configurations, since the forward converter requires no center-tapped windings. During subinterval 1, all of the available winding copper is used to transmit power to the load. Essentially no unnecessary current flows during subintervals 2 and 3. Typically, the magnetizing current is small compared to the reflected load current, and has negligible effect on the transformer utilization. So the transformer core and windings are effectively utilized in modern forward converters.

6.3.3 Push-Pull Isolated Buck Converter

The push-pull isolated buck converter is illustrated in Fig. 6.28. The secondary-side circuit is identical with the full- and half-bridge converters, with identical waveforms. The primary-side circuit contains a center-tapped winding. Transistor Q_1 conducts for time DT_s during the first switching period. Transistor Q_2 conducts for an identical length of time during the next switching period, such that volt-second balance is maintained across the transformer primary winding. Converter waveforms are illustrated in Fig. 6.29. This converter can operate oven the entire range of duty cycles $0 \le D < 1$. Its conversion ratio is given by

$$V = nDV_g \tag{6.38}$$

This converter is sometimes used in conjunction with low input voltages. It tends to exhibit low primary-

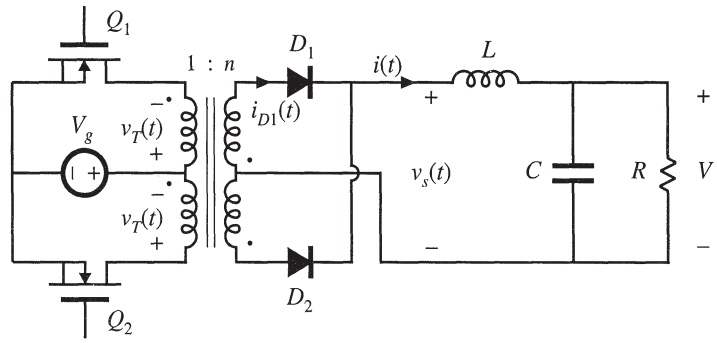


Fig. 6.28 Push-pull isolated buck converter.

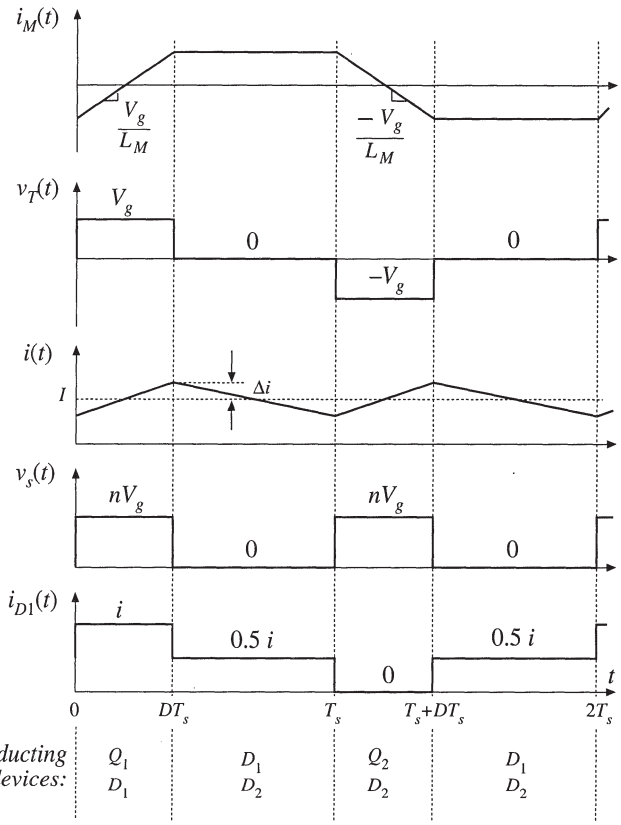


Fig. 6.29 Waveforms of the push-pull isolated buck converter.

side conduction losses, since at any given instant only one transistor is connected in series with the dc source V_g. The ability to operate with transistor duty cycles approaching unity also allows the turns ratio n to be minimized, reducing the transistor currents.

The push-pull configuration is prone to transformer saturation problems. Since it cannot be guaranteed that the forward voltage drops and conduction times of transistors Q_1 and Q_2 are exactly equal, small imbalances can cause the dc component of voltage applied to the transformer primary to be nonzero. In consequence, during every two switching periods there is a net increase in the magnitude of the magnetizing current. If this imbalance continues, then the magnetizing current can eventually become large enough to saturate the transformer.

Current-programmed control can be employed to mitigate the transformer saturation problems. Operation of the push-pull converter using only duty cycle control is not recommended.

Utilization of the transformer core material and secondary winding is similar to that for the full-bridge converter. The flux and magnetizing current can be both positive and negative, and therefore the entire B–H loop can be used, if desired. Since the primary and secondary windings are both center-tapped, their utilization is suboptimal.

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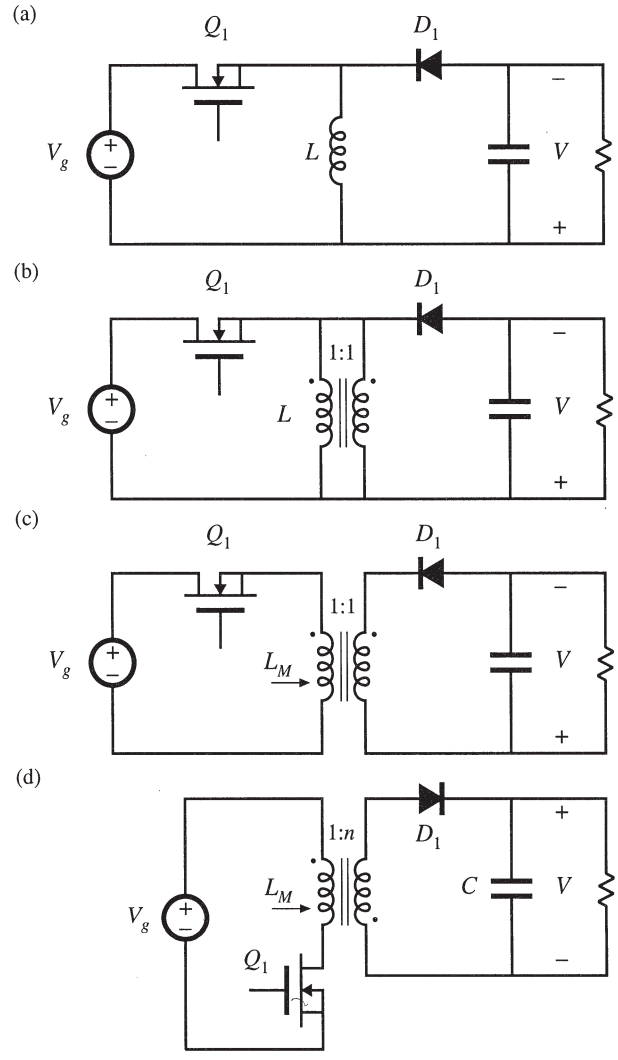


Fig. 6.30 Derivation of the flyback converter: (a) buck–boost converter; (b) inductor L is wound with two parallel wires; (c) inductor windings are isolated, leading to the flyback converter; (d) with a 1:n turns ratio and positive output.

6.3.4 Flyback Converter

The flyback converter is based on the buck–boost converter. Its derivation is illustrated in Fig. 6.30. Figure 6.30(a) depicts the basic buck-boost converter, with the switch realized using a MOSFET and diode. In Fig. 6.30(b), the inductor winding is constructed using two wires, with a 1:1 turns ratio. The basic function of the inductor is unchanged, and the parallel windings are equivalent to a single winding constructed of larger wire. In Fig. 6.30(c), the connections between the two windings are broken. One winding is used while the transistor Q_1 conducts, while the other winding is used when diode D_1 conducts. The total current in the two windings is unchanged from the circuit of Fig. 6.30(b); however, the current is now distributed between the windings differently. The magnetic fields inside the inductor in both cases

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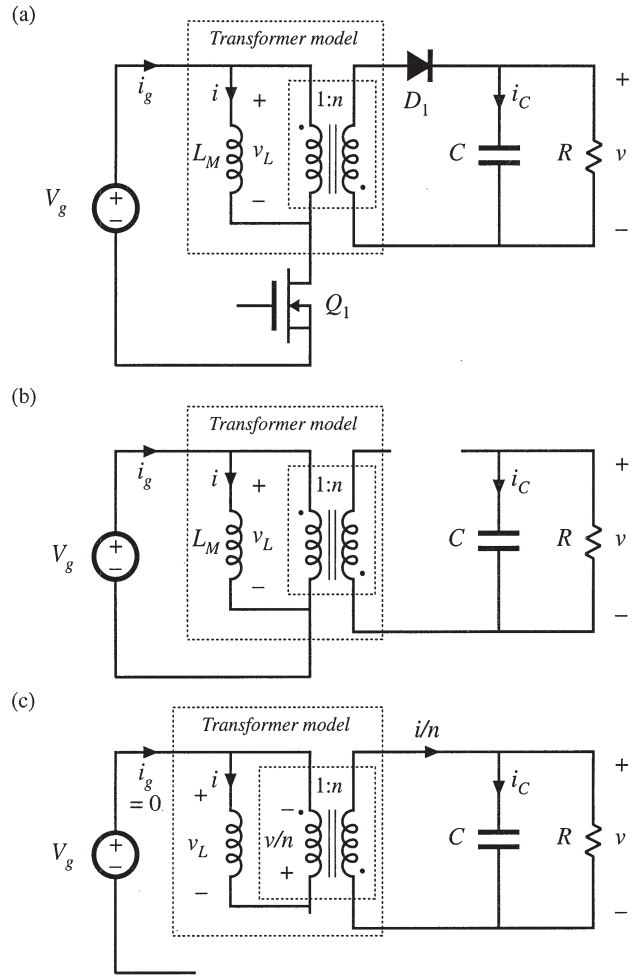


Fig. 6.31 Flyback converter circuit: (a) with transformer equivalent circuit model, (b) during subinterval 1, (c) during subinterval 2.

are identical. Although the two-winding magnetic device is represented using the same symbol as the transformer, a more descriptive name is "two-winding inductor." This device is sometimes also called a *flyback transformer*. Unlike the ideal transformer, current does not flow simultaneously in both windings of the flyback transformer. Figure 6.30(d) illustrates the usual configuration of the flyback converter. The MOSFET source is connected to the primary-side ground, simplifying the gate drive circuit. The transformer polarity marks are reversed, to obtain a positive output voltage. A 1:n turns ratio is introduced; this allows better converter optimization.

The flyback converter may be analyzed by insertion of the model of Fig. 6.16(b) in place of the flyback transformer. The circuit of Fig. 6.31(a) is then obtained. The magnetizing inductance L_M functions in the same manner as inductor L of the original buck-boost converter of Fig. 6.30(a). When transistor Q_1 conducts, energy from the dc source V_g is stored in L_M. When diode D_1 conducts, this stored energy is transferred to the load, with the inductor voltage and current scaled according to the 1:n turns ratio.

During subinterval 1, while transistor Q_1 conducts, the converter circuit model reduces to Fig.

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6.31(b). The inductor voltage v_L, capacitor current i_C, and dc source current i_g are given by

$$\begin{aligned} v_L &= V_g \\ i_C &= -\frac{v}{R} \\ i_g &= i \end{aligned} \tag{6.39}$$

With the assumption that the converter operates in the continuous conduction mode, with small inductor current ripple and small capacitor voltage ripple, the magnetizing current i and output capacitor voltage v can be approximated by their dc components, I and V, respectively. Equation (6.39) then becomes

$$\begin{aligned} v_L &= V_g \\ i_C &= -\frac{V}{R} \\ i_g &= I \end{aligned} \tag{6.40}$$

During the second subinterval, the transistor is in the off-state, and the diode conducts. The equivalent circuit of Fig. 6.31(c) is obtained. The primary-side magnetizing inductance voltage v_L, the capacitor current i_C, and the dc source current i_g for this subinterval are:

$$\begin{aligned} v_L &= -\frac{v}{n} \\ i_C &= \frac{i}{n} - \frac{v}{R} \\ i_g &= 0 \end{aligned} \tag{6.41}$$

It is important to consistently define $v_L(t)$ on the same side of the transformer for all subintervals. Upon making the small-ripple approximation, one obtains

$$\begin{aligned} v_L &= -\frac{V}{n} \\ i_C &= \frac{I}{n} - \frac{V}{R} \\ i_g &= 0 \end{aligned} \tag{6.42}$$

The $v_L(t)$, $i_C(t)$, and $i_g(t)$ waveforms are sketched in Fig. 6.32 for continuous conduction mode operation.

Application of the principle of volt-second balance to the primary-side magnetizing inductance yields

$$\langle v_L \rangle = D\left(V_g\right) + D'\left(-\frac{V}{n}\right) = 0 \tag{6.43}$$

Solution for the conversion ratio then leads to

$$M(D) = \frac{V}{V_g} = n\frac{D}{D'} \tag{6.44}$$

So the conversion ratio of the flyback converter is similar to that of the buck-boost converter, but contains an added factor of n.

Application of the principle of charge balance to the output capacitor C leads to

$$\langle i_C \rangle = D\left(-\frac{V}{R}\right) + D'\left(\frac{I}{n} - \frac{V}{R}\right) = 0 \tag{6.45}$$

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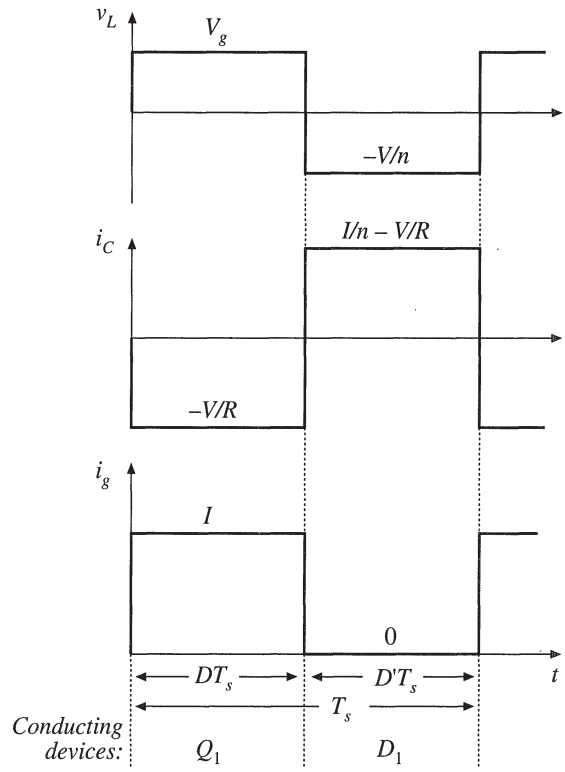


Fig. 6.32 Flyback converter waveforms, continuous conduction mode.

Solution for I yields

$$I = \frac{nV}{D'R} \tag{6.46}$$

This is the dc component of the magnetizing current, referred to the primary. The dc component of the source current i_g is

$$I_g = \langle i_g \rangle = D(I) + D'(0) \tag{6.47}$$

An equivalent circuit that models the dc components of the flyback converter waveforms can now be constructed. Circuits corresponding to the inductor loop equation (6.43) and to node equations (6.45) and (6.47) are illustrated in Fig. 6.33(a). By replacing the dependent sources with ideal dc transformers, one obtains Fig. 6.33(b). This is the dc equivalent circuit of the flyback converter. It contains a 1:D buck-type conversion ratio, followed by a D':1 boost-type conversion ratio, and an added factor of 1:n arising from the flyback transformer turns ratio. By use of the method developed in Chapter 3, the model can be refined to account for losses and to predict the converter efficiency. The flyback converter can also be operated in the discontinuous conduction mode; analysis is left as a homework problem. The results are similar to the DCM buck-boost converter results tabulated in Chapter 5, but are generalized to account for the turns ratio 1:n.

The flyback converter is commonly used at the 50 to 100 W power range, as well as in high-voltage power supplies for televisions and computer monitors. It has the advantage of very low parts

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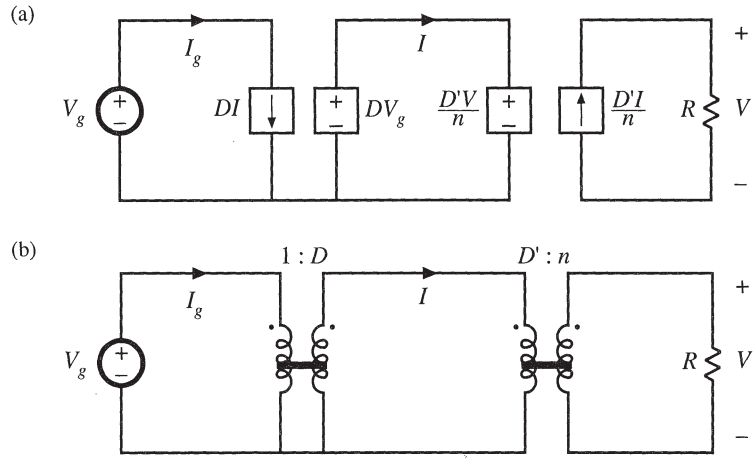


Fig. 6.33 Flyback converter equivalent circuit model, CCM: (a) circuits corresponding to Eqs. (6.43), (6.45), and (6.47); (b) equivalent circuit containing ideal dc transformers.

count. Multiple outputs can be obtained using a minimum number of parts: each additional output requires only an additional winding, diode, and capacitor. However, in comparison with the full-bridge, half-bridge, or two-transistor forward converters, the flyback converter has the disadvantages of high transistor voltage stress and poor cross-regulation. The peak transistor voltage is equal to the dc input voltage V_g plus the reflected load voltage V/n; in practice, additional voltage is observed due to ringing associated with the transformer leakage inductance. Rigorous comparison of the utilization of the flyback transformer with the transformers of buck-derived circuits is difficult because of the different functions performed by these elements. The magnetizing current of the flyback transformer is unipolar, and hence no more than half of the core material *B–H* loop can be utilized. The magnetizing current must contain a significant dc component. Yet, the size of the flyback transformer is quite small in designs intended to operate in the discontinuous conduction mode. However, DCM operation leads to increased peak currents in the transistor, diode, and filter capacitors. Continuous conduction mode designs require larger values of L_M, and hence larger flyback transformers, but the peak currents in the power stage elements are lower.

6.3.5 Boost-Derived Isolated Converters

Transformer-isolated boost converters can be derived by inversion of the source and load of buck-derived isolated converters. A number of configurations are known, and two of these are briefly discussed here. These converters find some employment in high-voltage power supplies, as well as in low-harmonic rectifier applications.

A full-bridge configuration is diagrammed in Fig. 6.34, and waveforms for the continuous conduction mode are illustrated in Fig. 6.35. The circuit topologies during the first and second subintervals are equivalent to those of the basic nonisolated boost converter, and when the turns ratio is 1:1, the inductor current $i(t)$ and output current $i_o(t)$ waveforms are identical to the inductor current and diode current waveforms of the nonisolated boost converter.

During subinterval 1, all four transistors operate in the on state. This connects the inductor L across the dc input source V_g, and causes diodes D_1 and D_2 to be reverse-biased. The inductor current $i(t)$

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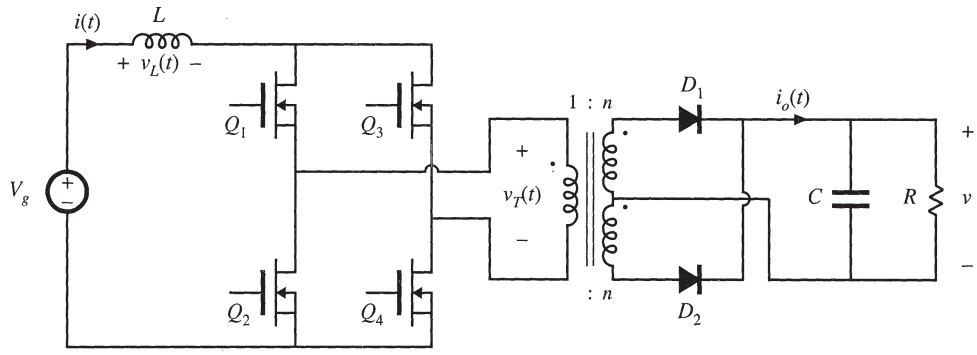


Fig. 6.34 Full-bridge transformer-isolated boost converter.

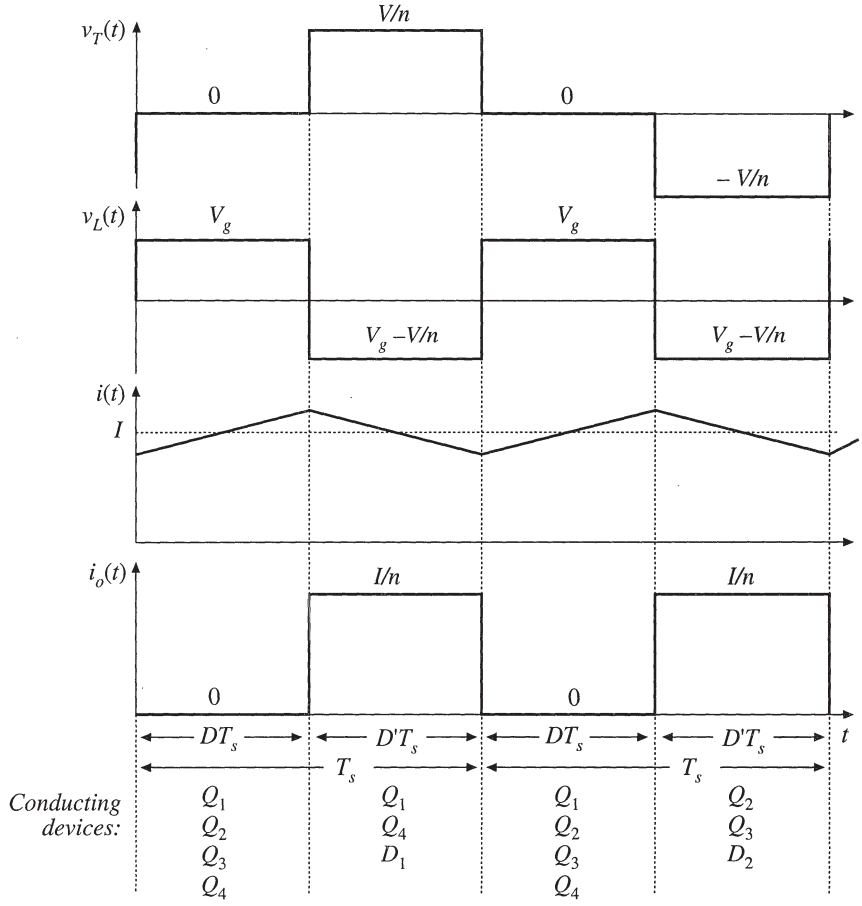


Fig. 6.35 Waveforms of the transformer-isolated full-bridge boost converter, CCM.

increases with slope V_g/L, and energy is transferred from the dc source V_g to inductor L. During the second subinterval, transistors Q_2 and Q_3 operate in the off state, so that inductor L is connected via transistors Q_1 and Q_4 through the transformer and diode D_1 to the dc output. The next switching period is similar, except that during subinterval 2, transistors Q_1 and Q_4 operate in the off state, and inductor L is connected via transistors Q_2 and Q_3 through the transformer and diode D_2 to the dc output. If the transistor off-times and the diode forward drops are identical, then the average transformer voltage is zero, and the net volt-seconds applied to the transformer magnetizing inductance over two switching periods is zero.

Application of the principle of inductor volt-second balance to the inductor voltage waveform $v_L(t)$ yields

$$\langle v_L \rangle = D\left(V_g\right) + D'\left(V_g - \frac{V}{n}\right) = 0 \tag{6.48}$$

Solution for the conversion ratio $M(D)$ then leads to

$$M(D) = \frac{V}{V_g} = \frac{n}{D'} \tag{6.49}$$

This result is similar to the boost converter $M(D)$, with an added factor of n due to the transformer turns ratio.

The transistors must block the reflected load voltage $V/n = V_g/D'$. In practice, additional voltage

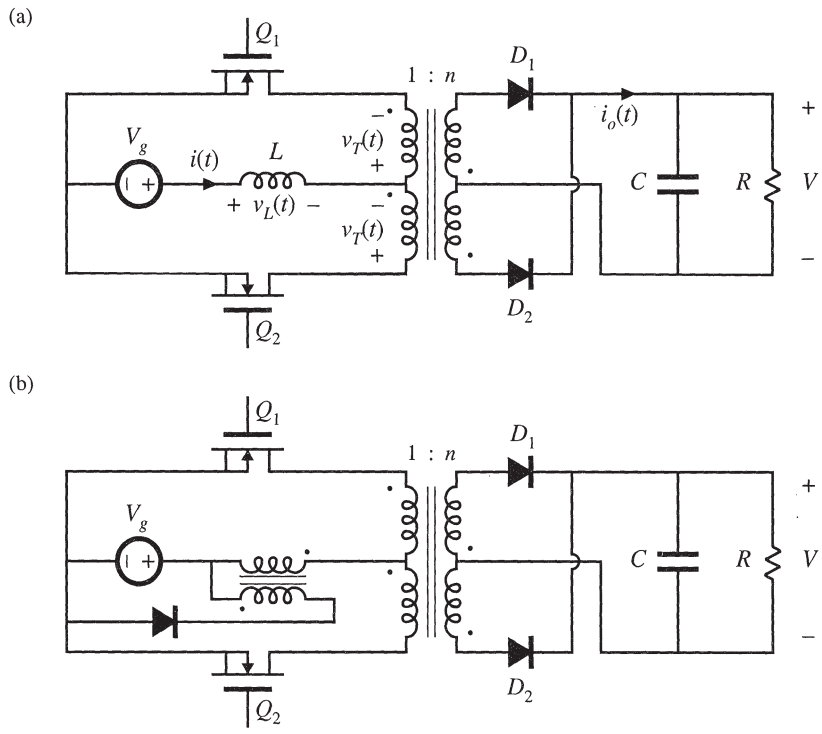


Fig. 6.36 Push-pull isolated converters: (a) based on the boost converter, (b) based on the Watkins-Johnson converter.

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is observed due to ringing associated with the transformer leakage inductance. Because the instantaneous transistor current is limited by inductor L, saturation of the transformer due to small imbalances in the semiconductor forward voltage drops or conduction times is not catastrophic. Indeed, control schemes are known in which the transformer is purposely operated in saturation during subinterval 1 [13, 15].

A push-pull configuration is depicted in Fig. 6.36(a). This configuration requires only two transistors, each of which must block voltage $2V/n$. Operation is otherwise similar to that of the full-bridge. During subinterval 1, both transistors conduct. During subinterval 2, one of the transistors operates in the off state, and energy is transferred from the inductor through the transformer and one of the diodes to the output. Transistors conduct during subinterval 2 during alternate switching periods, such that transformer volt-second balance is maintained. A similar push-pull version of the Watkins-Johnson converter, converter 6 of Fig. 6.14, is illustrated in Fig. 6.36(b).

6.3.6 Isolated Versions of the SEPIC and the Ćuk Converter

The artifice used to obtain isolation in the flyback converter can also be applied to the SEPIC and inverse-SEPIC. Referring to Fig. 6.37(a), inductor L_2 can be realized using two windings, leading to the isolated SEPIC of Fig. 6.37(b). An equivalent circuit is given in Fig. 6.37(c). It can be seen that the mag-

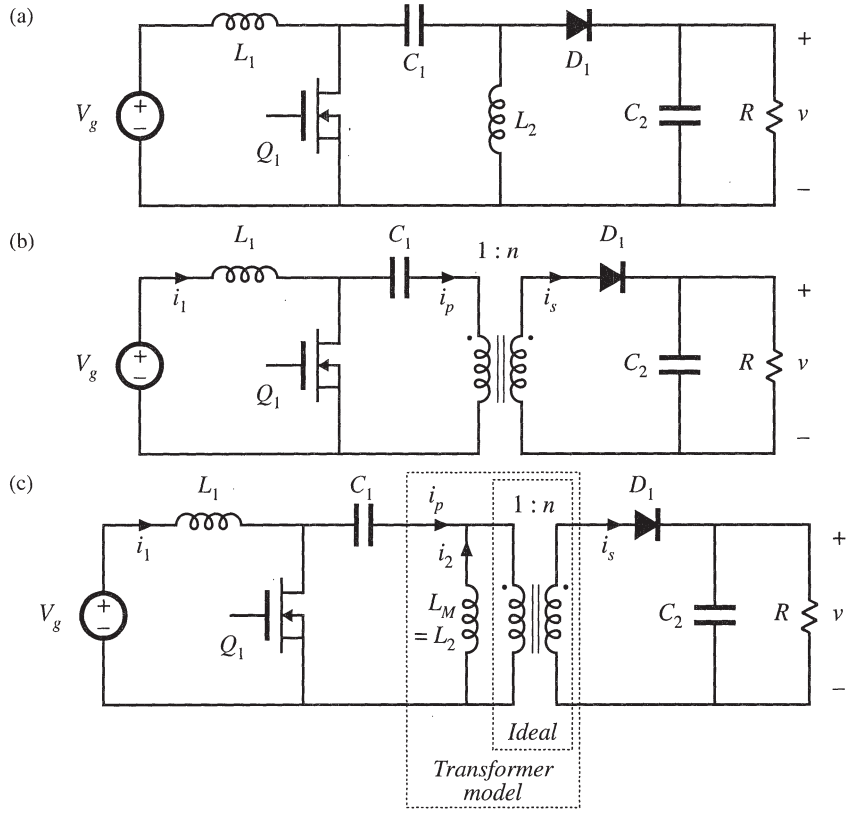


Fig. 6.37 Obtaining isolation in the SEPIC: (a) basic nonisolated converter, (b) isolated SEPIC, (c) with transformer equivalent circuit model.

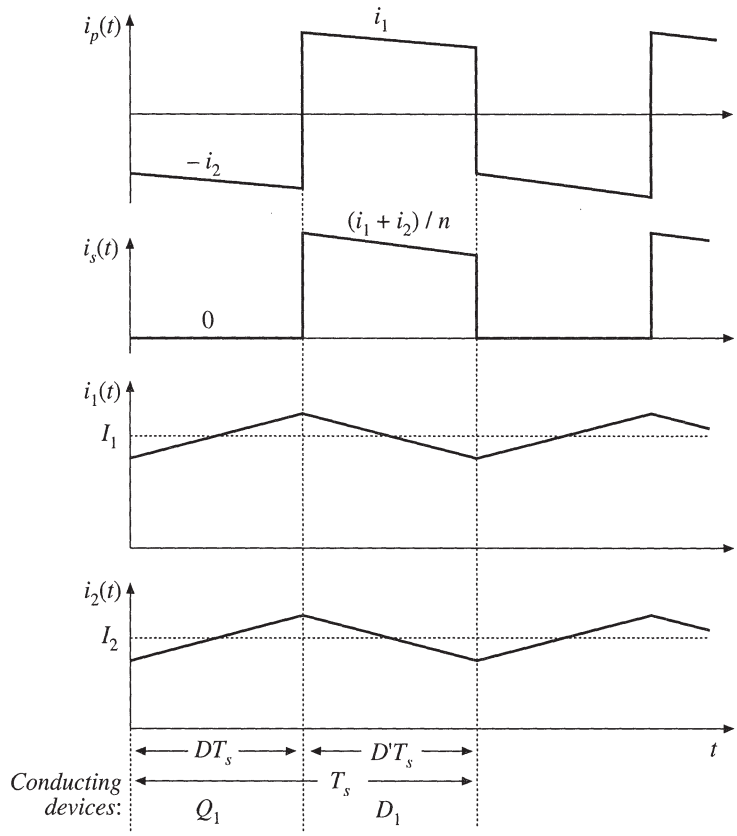


Fig. 6.38 Waveforms of the isolated SEPIC, continuous conduction mode.

netizing inductance performs the energy-storage function of the original inductor L_2. In addition, the ideal transformer provides isolation and a turns ratio.

Typical primary and secondary winding current waveforms $i_p(t)$ and $i_s(t)$ are portrayed in Fig. 6.38, for the continuous conduction mode. The magnetic device must function as both a flyback transformer and also a conventional two-winding transformer. During subinterval 1, while transistor Q_1 conducts, the magnetizing current flows through the primary winding, and the secondary winding current is zero. During subinterval 2, while diode D_1 conducts, the magnetizing current flows through the secondary winding to the load. In addition, the input inductor current i_1 flows through the primary winding. This induces an additional component of secondary current i_1/n, which also flows to the load. So design of the SEPIC transformer is somewhat unusual, and the rms winding currents are larger than those of the flyback transformer.

By application of the principle of volt-second balance to inductors L_1 and L_M, the conversion ratio can be shown to be

$$M(D) = \frac{V}{V_g} = \frac{nD}{D'} \tag{6.50}$$

Ideally, the transistor must block voltage V_g/D'. In practice, additional voltage is observed due to ringing associated with the transformer leakage inductance.

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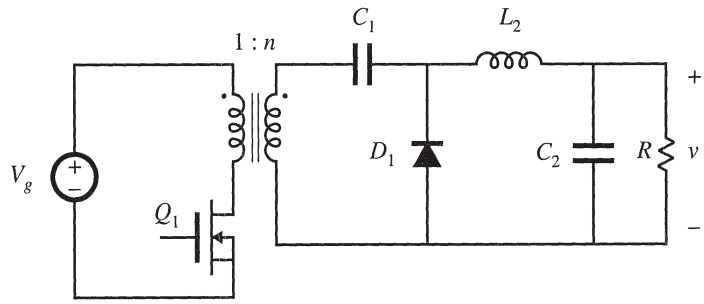


Fig. 6.39 Isolated inverse-SEPIC.

An isolated version of the inverse-SEPIC is shown in Fig. 6.39. Operation and design of the transformer is similar to that of the SEPIC.

Isolation in the Ćuk converter is obtained in a different manner [18]. The basic nonisolated Ćuk converter is illustrated in Fig. 6.40(a). In Fig. 6.40(b), capacitor C_1 is split into two series capacitors C_{1a} and C_{1b}. A transformer can now be inserted between these capacitors, as indicated in Fig. 6.40(c). The polarity marks have been reversed, so that a positive output voltage is obtained. Having capacitors in series with the transformer primary and secondary windings ensures that no dc voltage is applied to the transformer. The transformer functions in a conventional manner, with small magnetizing current and negligible energy storage within the magnetizing inductance.

Utilization of the transformer of the Ćuk converter is quite good. The magnetizing current can

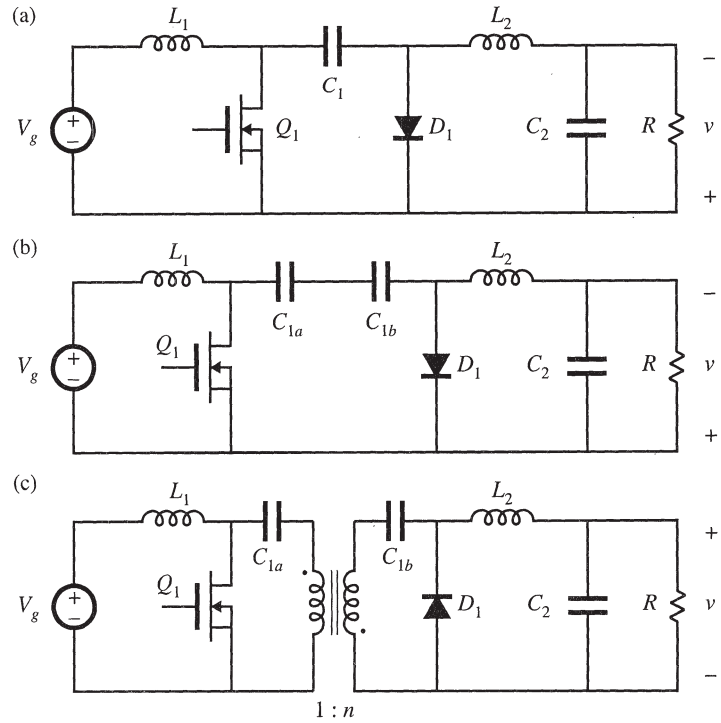


Fig. 6.40 Obtaining isolation in the Ćuk converter: (a) basic nonisolated Ćuk converter, (b) splitting capacitor C_1 into two series capacitors, (c) insertion of transformer between capacitors.

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be both positive and negative, and hence the entire core B–H loop can be utilized if desired. There are no center-tapped windings, and all of the copper is effectively utilized. The transistor must block voltage V_g/D', plus some additional voltage due to ringing associated with the transformer leakage inductance. The conversion ratio is identical to that of the isolated SEPIC, Eq. (6.50).

The isolated SEPIC and Ćuk converter find application as switching power supplies, typically at power levels of several hundred watts. They are also now finding use as ac–dc low-harmonic rectifiers.

6.4 CONVERTER EVALUATION AND DESIGN

There is no ultimate converter perfectly suited for all possible applications. For a given application, with given specifications, trade studies should be performed to select a converter topology. Several approaches that meet the specifications should be considered, and for each approach important quantities such as worst-case transistor voltage, worst-case transistor rms current, transformer size, etc., should be computed. This type of quantitative comparison can lead to selection of the best approach, while avoiding the personal biases of the engineer.

6.4.1 Switch Stress and Utilization

Often, the largest single cost in a converter is the cost of the active semiconductor devices. Also, the conduction and switching losses associated with the semiconductor devices often dominates the other converter losses. This suggests evaluating candidate converter approaches by comparing the voltage and current stresses imposed on the active semiconductor devices. Minimization of the total switch stresses leads to minimization of the total silicon area required to realize the power devices of the converter.

So it is useful to compare the *total active switch stress* and *active switch utilization* of candidate converter approaches. In a good design, the voltages and currents imposed on the semiconductor devices is minimized, while the load power is maximized. If a converter contains k active semiconductor devices, the total active switch stress S can be defined as

$$S = \sum_{j=1}^{k} V_j I_j \tag{6.51}$$

where V_j is the peak voltage applied to semiconductor switch j, and I_j is the rms current applied to switch j. Peak rather than rms current is sometimes used, with qualitatively similar results. If the converter load power is P_{load}, then the active switch utilization U can be defined as

$$U = \frac{P_{load}}{S} \tag{6.52}$$

The switch utilization is less than one in transformer-isolated converters, and is a quantity to be maximized.

For example, consider the transistor utilization in the CCM flyback converter of Fig. 6.30(d). The peak transistor voltage occurs during subinterval 2, and is equal to the dc input voltage V_g plus the reflected load voltage V/n:

$$V_{Q1,pk} = V_g + \frac{V}{n} = \frac{V_g}{D'} \tag{6.53}$$

The transistor current waveform coincides with the input current waveform $i_g(t)$, which is sketched in Fig. 6.32. The rms value of this waveform is

$$I_{Q1,rms} = I\sqrt{D} = \frac{P_{load}}{V_g\sqrt{D}} \tag{6.54}$$

So the total active switch stress is

$$S = V_{Q1,pk}\, I_{Q1,rms} = \left(V_g + \frac{V}{n}\right)\left(I\sqrt{D}\right) \tag{6.55}$$

The load power P_{load} can be expressed in terms of V and I by solution of the equivalent circuit model, Fig. 6.33(b). The result is

$$P_{load} = D' V \frac{I}{n} \tag{6.56}$$

Use of Eq. (6.44) to eliminate V_g from Eq. (6.55), and evaluation of Eq. (6.52), leads to

$$U = D'\sqrt{D} \tag{6.57}$$

The transistor utilization U tends to zero at $D = 0$ and at $D = 1$, and reaches a maximum of $U = 0.385$ at $D = 1/3$.

For given values of V_g, V, and the load power, the designer can arbitrarily choose the duty cycle D. The turns ratio is then chosen to satisfy Eq. (6.44), as follows:

$$n = \frac{V}{V_g}\frac{D'}{D} \tag{6.58}$$

At low duty cycle, the transistor rms current becomes large because the transformer turns ratio must be large. At a duty cycle approaching one, the transistor peak voltage is large. So the choice $D = 1/3$ is a good one, which minimizes the product of peak transistor voltage and rms transistor current. In practice, the converter must be optimized to meet a number of different criteria, so a somewhat different duty cycle may be chosen. Also, the converter must usually be designed to operate with some given range of load powers and input voltages; this can lead to a different choice of D, as well as to reduced switch utilization.

For a simple comparison between converters, the switch utilizations of a number of isolated and nonisolated converters are collected in Table 6.1. For simplicity, the formulas assume that the converter is designed to function at a single operating point, that is, with no variations in V_g, V, or P_{load}.

It can be seen that the nonisolated buck and boost converters operate most efficiently when their conversion ratios $M(D)$ are near one. In the case of the boost converter, the switch utilization is greater than one for $D < 0.382$, and approaches infinity as D tends to zero. The reason for this is that, at $D = 0$, the transistor is always off and hence its rms current is zero. But at $D = 0$, $V = V_g$, so the output power is nonzero. All of the load power flows through the diode rather than the transistor. Of course, if it is desired that $V = V_g$, then it would be best to eliminate the boost converter, and directly connect the load to the input voltage. But it is nonetheless true that if the output voltage V is not too much greater than V_g, then a large amount of power can be controlled by a relatively small transistor. Similar arguments apply to the buck converter: all of the load power must flow through the transistor and hence $U \leq 1$, yet converter efficiency and cost per watt are optimized when the output voltage V is not too much smaller than the input voltage.

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Table 6.1 Active switch utilizations of some common dc–dc converters, single operating point

Converter	$U(D)$	max $U(D)$	max $U(D)$ occurs at D =
Buck	$\sqrt{D}$	1	1
Boost	$\frac{D'}{\sqrt{D}}$	∞	0
Buck–boost, flyback, nonisolated SEPIC, isolated SEPIC, nonisolated Ćuk, isolated Ćuk	$D'\sqrt{D}$	$\frac{2}{3\sqrt{3}} = 0.385$	$\frac{1}{3}$
Forward, $n_1 = n_2$	$\frac{1}{2}\sqrt{D}$	$\frac{1}{2\sqrt{2}} = 0.353$	$\frac{1}{2}$
Other isolated buck-derived converters (full–bridge, half–bridge, push–pull)	$\frac{\sqrt{D}}{2\sqrt{2}}$	$\frac{1}{2\sqrt{2}} = 0.353$	1
Isolated boost-derived converters (full–bridge, push–pull)	$\frac{D'}{2\sqrt{1+D}}$	$\frac{1}{2}$	0

Incorporation of an isolation transformer leads to reduced switch utilization. In general, transformer-isolated buck-derived converters should be designed to operate at as large a duty cycle as other considerations will allow. Even so, the switch utilization is reduced to $U \leq 0.353$, meaning that the switch stress is increased by a factor of approximately 2.8 as compared with the nonisolated buck converter at $D = 1$. On the other hand, the transformer turns ratio can be chosen to match the load voltage to the input voltage and better optimize the converter. For example, in a full-bridge buck-derived converter operating with $V_g = 500$ V and $V = 5$ V, the turns ratio could be chosen to be nearly 100:1, leading to a duty cycle close to one and switch utilization of approximately 0.35. To obtain a 1 kW output power, the total transistor stress would be 1 kW/0.35 = 2.86 kVA. By comparison, the nonisolated buck converter would operate with a duty cycle of 0.01 and a switch utilization of 0.1. Its total switch stress would be 1 kW/0.1 = 10 kVA; transistors with larger rated currents and lower on-resistances would be needed. Similar arguments apply to the transformer-isolated boost-derived converters: these converters are better optimized when they operate at low duty cycles.

The nonisolated buck-boost, nonisolated SEPIC, nonisolated Ćuk converter, and the isolated SEPIC, flyback, and Ćuk converters have similar switch utilizations. In all of these converters, $U \leq 0.385$, which is approximately the same as in the isolated buck-derived converters. So the nonisolated versions of these converters tend to have lower switch utilizations than the buck or boost converters; however, isolation can be obtained with no additional penalty in switch stress. Switch utilization of a single-operating-point design is maximized when the turns ratio is chosen such that $D = 1/3$.

The cost of the active semiconductor devices of a converter approach can be estimated using the converter switch utilization, as follows:

$$\left(\begin{array}{c}\text{semiconductor cost}\\ \text{per kW output power}\end{array}\right) = \frac{\left(\begin{array}{c}\text{semiconductor device cost}\\ \text{per rated kVA}\end{array}\right)}{\left(\begin{array}{c}\text{voltage}\\ \text{derating}\\ \text{factor}\end{array}\right)\left(\begin{array}{c}\text{current}\\ \text{derating}\\ \text{factor}\end{array}\right)\left(\begin{array}{c}\text{converter}\\ \text{switch}\\ \text{utilization}\end{array}\right)} \tag{6.59}$$

The semiconductor device cost per rated kVA is equal to the cost of a semiconductor device, divided by

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the products of its maximum voltage rating and its maximum rms current capability, expressed in $/kVA. This figure depends on a variety of factors, including the device type, packaging, voltage and power levels, and market volume. A typical U.S. value in 2000 is less than $1 /kVA. Voltage and current derating is required to obtain reliable operation of the semiconductor devices. A typical *design guideline* is that the worst-case peak transistor voltage (including transients, voltage spikes due to ringing, and all other anticipated events) should not exceed 75% of the rated transistor voltage, leading to a voltage derating factor of (0.75). Hence, the cost of the active semiconductor switches in a 2000 isolated dc–dc converter is typically in the range $1 to $10 per kW of output power for medium to high-power applications.

6.4.2 Design Using Computer Spreadsheet

Computer spreadsheets are a useful tool for performing converter trade studies and designs. Given specifications regarding the desired output voltage V, the ranges of the input voltage V_g and the load power P_{load}, the desired output voltage ripple Δv, the switching frequency f_s, etc., various design options can be explored. The transformer turns ratio and the inductor current ripple Δi can be taken as design variables, chosen by the engineer. The range of duty cycle variations and the inductor and capacitor component values can then be computed. Worst-case values of the currents and voltages applied to the various power-stage elements can also be evaluated, as well as the sizes of the magnetic elements. By investigating several choices of the design variables, a good compromise between the worst-case voltage stresses and current stresses can be found.

A short spreadsheet example is given in Table 6.2. The converter operates from a dc voltage derived by rectifying a 230 V ± 20% ac source voltage. The converter dc input voltage V_g is therefore $230\sqrt{2}$ V ± 20%. The load voltage is a regulated 15 V dc, with switching ripple Δv no greater than 0.1 V. The load power can vary over the range 20 W to 200 W. It is desired to operate with a switching frequency of f_s = 100 kHz. These values are entered as specifications, at the top of the spreadsheet. The design of a forward converter, Fig. 6.22, and of a flyback converter, Fig. 6.30(d), to meet these specifications is investigated in the spreadsheet. Continuous conduction mode designs are investigated: the inductor current ripple Δi is chosen small enough that the converter operates in CCM at full load power. Depending on the choice of Δi, the converter may operate in either CCM or DCM at minimum load power.

For the single-transistor forward converter, the turns ratios n_2/n_1 and n_3/n_1, as well as the inductor current ripple Δi, can be taken as design variables. For this example, the reset-winding turns ratio n_2/n_1 is chosen to be one, and hence the duty cycle is limited to $D < 0.5$ as given by Eq. (6.35). The maximum duty cycle is computed first. The output voltage of the forward converter, in continuous conduction mode, is given by Eq. (6.36). Solution for the duty cycle D leads to

$$D = \frac{n_1}{n_3}\frac{V}{V_g} \tag{6.60}$$

The maximum value of D occurs at minimum V_g and at full load, and is given in Table 6.2. The minimum CCM value of D, occurring at maximum V_g, is also listed.

The value of the inductance L is computed next. The magnitude of the inductor current ripple Δi can be computed in a manner similar to that used for the nonisolated buck converter to obtain Eq. (2.15). The result is

$$\Delta i = \frac{D'VT_s}{2L} \tag{6.61}$$

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Table 6.2 Spreadsheet design example

Specifications			
Maximum input voltage V_g	390 V		
Minimum input voltage V_g	260 V		
Output voltage V	15 V		
Maximum load power P_{load}	200 W		
Minimum load power P_{load}	20 W		
Switching frequency f_s	100 kHz		
Maximum output ripple Δv	0.1 V		
Forward converter design, CCM		***Flyback converter design, CCM***	
Design variables		*Design variables*	
Reset winding turns ratio n_2/n_1	1	Turns ratio n_2/n_1	0.125
Turns ratio n_3/n_1	0.125	Inductor current ripple Δi	3 A ref to sec
Inductor current ripple Δi	2A ref to sec		
Results		*Results*	
Maximum duty cycle D	0.462	Maximum duty cycle D	0.316
Minimum D, at full load	0.308	Minimum D, at full load	0.235
Minimum D, at minimum load	0.251	Minimum D, at minimum load	0.179
Inductance L	26 μH	Inductance L	19 μH ref to sec
Capacitance C	25 μF	Capacitance C	210 μF
Worst-case stresses		*Worst-case stresses*	
Peak transistor voltage v_{Q1}	780 V	Peak transistor voltage v_{Q1}	510 V
Rms transistor current	1.13 A	Rms transistor current	1.38 A
Transistor utilization U	0.226	Transistor utilization U	0.284
Peak diode voltage v_{D2}	49 V	Peak diode voltage v_{D1}	64 V
Rms diode current i_{D2}	9.1 A	Rms diode current i_{D1}	16.3 A
Peak diode voltage v_{D3}	49 V	Peak diode current i_{D1}	22.2 A
Rms diode current i_{D3}	11.1 A		
Rms output capacitor current i_C	1.15 A	Rms output capacitor current i_C	9.1 A

The worst-case maximum ripple occurs in CCM at minimum duty cycle. Solution for L yields

$$L = \frac{D'VT_s}{2\Delta i} \tag{6.62}$$

This equation is used to select L such that the worst-case ripple is equal to the specified value of Δi. The required value of L is listed in Table 6.2. The required value of C that leads to the specified voltage ripple Δv is also computed, using Eq. (2.60). Since Eq. (2.60) neglects capacitor esr, a larger value of C may be required in practice.

If the converter operates in the discontinuous conduction mode at light load, then the controller must reduce the duty cycle D to maintain the required output voltage V. The conversion ratio $M(D, K)$ of the DCM forward converter can be found analytically, using the method developed in the previous chapter. Alternatively, the nonisolated buck converter solution, Eq. (5.29), can be applied directly if all element values are referred to the transformer secondary side. Hence, the output voltage in DCM is given by

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$$V = \frac{n_3}{n_1} V_g \frac{2}{1 + \sqrt{1 + \frac{4K}{D^2}}} \tag{6.63}$$

with $K = 2L/RT_s$, and $R = V^2/P_{load}$. Solution for the duty cycle D yields

$$D = \frac{2\sqrt{K}}{\sqrt{\left(\frac{2n_3 V_g}{n_1 V} - 1\right)^2 - 1}} \tag{6.64}$$

The actual duty cycle is the smaller of Eqs. (6.60) and (6.64). The minimum duty cycle occurs at minimum load power and maximum V_g, and is given in Table 6.2.

Worst-case component stresses can now be evaluated. The peak transistor voltage is given by Eq. (6.37). The rms transistor current is calculated with the help of Appendix 1. With the assumption that the transformer magnetizing current can be neglected, the transistor current is equal to the reflected inductor current $i(t)n_3/n_1$ during subinterval 1, and is equal to zero during subintervals 2 and 3. The rms transistor current is therefore

$$I_{Q1,rms} = \frac{n_3}{n_1}\sqrt{D}\sqrt{I^2 + \frac{(\Delta i)^2}{3}} \approx \frac{n_3}{n_1}\sqrt{D}\, I \tag{6.65}$$

where $I = P_{load}/V$. The worst-case value of $I_{Q1\text{-}rms}$ occurs at maximum load power and at maximum duty cycle. Expressions for the worst-case stresses in the diodes and output capacitor, as well as for the flyback converter, are found in a similar manner. Their derivation is left as an exercise for the student.

The designs of Table 6.2 are good ones which illustrate the tradeoffs inherent in selection of an isolated converter topology, although some additional design optimization is possible and is left as a homework problem. Both designs utilize a turns ratio of 8:1. The rms transistor current is 22% higher in the flyback converter. This current could be reduced, at the expense of increased transistor voltage. The flyback converter imposes only 510 V on the transistor. A transistor rated at 800 V or 1000 V could be used, with an adequate voltage derating factor and some margin for voltage ringing due to transformer leakage inductance. The 780 V imposed on the transistor of the forward converter is 53% higher than in the flyback converter. Power MOSFETs with voltage ratings greater than 1000 V are not available in 1997; hence, when voltage ringing due to transformer leakage inductance is accounted for, this design will have an inadequate voltage design margin. This problem could be overcome by changing the reset winding turns ratio n_2/n_1, or by using a two-transistor forward converter. It can be concluded that the transformer reset mechanism of the flyback converter is better than that of the conventional forward converter.

Because of the pulsating nature of the secondary-side currents in the flyback converter, the rms and peak secondary currents are significantly higher than in the forward converter. The flyback converter diode must conduct an rms current that is 47% greater than that of forward converter diode D_3, and 80% greater than the current in forward converter diode D_2. The secondary winding of the flyback transformer must also conduct this current. Furthermore, the output capacitor of the flyback converter must be rated to conduct an rms current of 9.1 A. This capacitor will be much more expensive than its counterpart in the forward converter. It can be concluded that the nonpulsating output current property of the forward converter is superior to the pulsating output current of the flyback. For these reasons, flyback converters and other converters having pulsating output currents are usually avoided when the application calls for a high-current output.

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6.5 SUMMARY OF KEY POINTS

1. The boost converter can be viewed as an inverse buck converter, while the buck-boost and Ćuk converters arise from cascade connections of buck and boost converters. The properties of these converters are consistent with their origins. Ac outputs can be obtained by differential connection of the load. An infinite number of converters are possible, and several are listed in this chapter.
2. For understanding the operation of most converters containing transformers, the transformer can be modeled as a magnetizing inductance in parallel with an ideal transformer. The magnetizing inductance must obey all of the usual rules for inductors, including the principle of volt-second balance.
3. The steady-state behavior of transformer-isolated converters may be understood by first replacing the transformer with the magnetizing-inductance-plus-ideal-transformer equivalent circuit. The techniques developed in the previous chapters can then be applied, including use of inductor volt-second balance and capacitor charge balance to find dc currents and voltages, use of equivalent circuits to model losses and efficiency, and analysis of the discontinuous conduction mode.
4. In the full–bridge, half–bridge, and push–pull isolated versions of the buck and/or boost converters, the transformer frequency is twice the output ripple frequency. The transformer is reset while it transfers energy: the applied voltage polarity alternates on successive switching periods.
5. In the conventional forward converter, the transformer is reset while the transistor is off. The transformer magnetizing inductance operates in the discontinuous conduction mode, and the maximum duty cycle is limited.
6. The flyback converter is based on the buck–boost converter. The flyback transformer is actually a two-winding inductor, which stores and transfers energy.
7. The transformer turns ratio is an extra degree-of-freedom which the designer can choose to optimize the converter design. Use of a computer spreadsheet is an effective way to determine how the choice of turns ratio affects the component voltage and current stresses.
8. Total active switch stress, and active switch utilization, are two simplified figures-of-merit which can be used to compare the various converter circuits.

REFERENCES

[1] S. ĆUK, "Modeling, Analysis, and Design of Switching Converters," Ph.D. thesis, California Institute of Technology, November 1976.

[2] S. ĆUK and R. D. MIDDLEBROOK, "A New Optimum Topology Switching Dc-to-Dc Converter," *IEEE Power Electronics Specialists Conference*, 1977 Record, pp. 160-179, June 1977.

[3] E. LANDSMAN, "A Unifying Derivation of Switching Dc-Dc Converter Topologies," *IEEE Power Electronics Specialists Conference*, 1979 Record, pp. 239-243, June 1979.

[4] R. TYMERSKI and V. VORPERIAN, "Generation, Classification, and Analysis of Switched-Mode Dc-to-Dc Converters by the Use of Converter Cells," *Proceedings International Telecommunications Energy Conference*, pp. 181-195, October 1986.

[5] S. ĆUK and R. ERICKSON, "A Conceptually New High-Frequency Switched-Mode Amplifier Technique Eliminates Current Ripple," *Proceedings Fifth National Solid-State Power Conversion Conference* (Powercon 5), pp. G3.1-G3.22, May 1978.

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[6] F. BARZEGAR and S. ĆUK, "A New Switched-Mode Amplifier Produces Clean Three-Phase Power," *Proceedings Ninth International Solid-State Power Conversion Conference* (Powercon 9), pp. E3.1-E3.15, July 1982.

[7] K. D. T. NGO, S. ĆUK, and R. D. MIDDLEBROOK, "A New Flyback Dc-to-Three-Phase Converter with Sinusoidal Outputs," *IEEE Power Electronics Specialists Conference*, 1983 Record, pp. 377-388.

[8] R. W. ERICKSON, "Synthesis of Switched-Mode Converters," *IEEE Power Electronics Specialists Conference*, 1983 Record, pp. 9-22, June 1983.

[9] D. MAKSIMOVIĆ and S. ĆUK, "General Properties and Synthesis of PWM Dc-Dc Converters," *IEEE Power Electronics Specialists Conference*, 1989 Record, pp. 515-525, June 1989.

[10] M. S. MAKOWSKI, "On Topological Assumptions on PWM Converters—A Reexamination," *IEEE Power Electronics Specialists Conference*, 1993 Record, pp. 141-147, June 1993.

[11] B. ISRAELSEN, J. MARTIN, C. REEVE, and V. SCOWN, "A 2.5 kV High Reliability TWT Power Supply: Design Techniques for High Efficiency and Low Ripple," *IEEE Power Electronics Specialists Conference*, 1977 Record, pp. 109-130, June 1977.

[12] R. SEVERNS, "A New Current-Fed Converter Topology," *IEEE Power Electronics Specialists Conference*, 1979 Record, pp. 277-283, June 1979.

[13] V. J. THOTTUVELIL, T. G. WILSON, and H. A. OWEN, "Analysis and Design of a Push-Pull Current-Fed Converter," *IEEE Power Electronics Specialists Conference*, 1981 Record, pp. 192-203, June 1981.

[14] R. REDL AND N. SOKAL, "Push–Pull Current-Fed Multiple-Output Dc–Dc Power Converter with Only One Inductor and with 0–100% Switch Duty Ratio," *IEEE Power Electronics Specialists Conference*, 1980 Record, pp. 341-345, June 1982.

[15] P. W. CLARKE, "Converter Regulation by Controlled Conduction Overlap," U. S. Patent 3,938,024, February 10, 1976.

[16] R. P. MASSEY and E. C. SNYDER, "High-Voltage Single-Ended Dc-Dc Converter," *IEEE Power Electronics Specialists Conference*, 1977 Record, pp. 156-159, June 1977.

[17] D. MAKSIMOVIĆ and S. ĆUK, "Switching Converters with Wide Dc Conversion Range," *IEEE Transactions on Power Electronics*, Vol. 6, No. 1, pp. 151-157, January 1991.

[18] R. D. MIDDLEBROOK and S. ĆUK, "Isolation and Multiple Outputs of a New Optimum Topology Switching Dc-to-Dc Converter," *IEEE Power Electronics Specialists Conference*, 1978 Record, pp. 256-264, June 13-15, 1978.

[19] T. G. WILSON, "Cross Regulation in an Energy-Storage Dc-to-Dc Converter with Two Regulated Outputs," *IEEE Power Electronics Specialists Conference*, 1977 Record, pp. 190-199, June 1977.

[20] H. MATSUO, "Comparison of Multiple-Output Dc-Dc Converters Using Cross Regulation," *IEEE Power Electronics Specialists Conference*, 1979 Record, pp. 169-185, June 1979.

[21] K. HARADA, T. NABESHIMA, and K. HISANAGA, "State-Space Analysis of the Cross-Regulation," *IEEE Power Electronics Specialists Conference*, 1979 Record, pp. 186-192, June 1979.

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[22] J. N. PARK and T. R. ZALOUM, "A Dual Mode Forward/Flyback Converter," *IEEE Power Electronics Specialists Conference*, 1982 Record, pp. 3-13, June 1982.

[23] S. ĆUK, "General Topological Properties of Switching Structures," *IEEE Power Electronics Specialists Conference*, 1979 Record, pp. 109-130, June 1979.

[24] R. SEVERNS and G. BLOOM, *Modern Dc–to–Dc Switchmode Power Converter Circuits*, New York: Van Nostrand Reinhold, 1985.

[25] N. MOHAN, T. UNDELAND, and W. ROBBINS, *Power Electronics: Converters, Applications, and Design*, 2nd edit., New York: John Wiley & Sons, 1995.

[26] J. KASSAKIAN, M. SCHLECHT, and G. VERGHESE, *Principles of Power Electronics*, Reading, MA: Addison-Wesley, 1991.

[27] D. MITCHELL, *Dc–Dc Switching Regulator Analysis*, New York: McGraw-Hill, 1988.

[28] K. KIT SUM, *Switch Mode Power Conversion: Basic Theory and Design*, New York: Marcel Dekker, 1984.

[29] R. E. TARTER, *Solid-State Power Conversion Handbook*, New York: John Wiley & Sons, 1993.

[30] Q. CHEN, F. C. LEE, and M. M. JOVANOVIĆ, "DC Analysis and Design of Multiple-Output Forward Converters with Weighted Voltage-Mode Control," *IEEE Applied Power Electronics Conference*, 1993 Record, pp. 449-455, March 1993.

PROBLEMS

6.1 Tapped-inductor boost converter. The boost converter is sometimes modified as illustrated in Fig. 6.41, to obtain a larger conversion ratio than would otherwise occur. The inductor winding contains a total of $(n_1 + n_2)$ turns. The transistor is connected to a tap placed n_1 turns from the left side of the inductor, as shown. The tapped inductor can be viewed as a two-winding $(n_1:n_2)$ transformer, in which the two windings are connected in series. The inductance of the entire $(n_1 + n_2)$ turn winding is L.

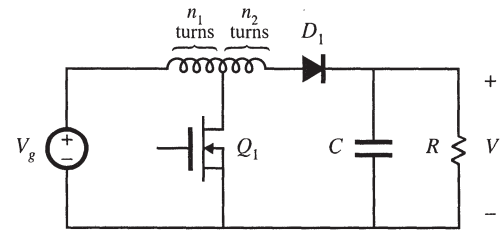


Fig. 6.41 Tapped-inductor boost converter, Problem 6.1

(a) Sketch an equivalent circuit model for the tapped inductor, which includes a magnetizing inductance and an ideal transformer. Label the values of the magnetizing inductance and turns ratio.

(b) Determine an analytical expression for the conversion ratio $M = V/V_g$. You may assume that the transistor, diode, tapped inductor, and capacitor are lossless. You may also assume that the converter operates in continuous conduction mode.

(c) Sketch $M(D)$ vs. D for $n_1 = n_2$, and compare to the nontapped ($n_2 = 0$) case.

6.2 Analysis of the DCM flyback converter. The flyback converter of Fig. 6.30(d) operates in the discontinuous conduction mode.

(a) Model the flyback transformer as a magnetizing inductance in parallel with an ideal transformer,

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and sketch the converter circuits during the three subintervals.

(b) Derive the conditions for operation in discontinuous conduction mode.

(c) Solve the converter: derive expressions for the steady-state output voltage V and subinterval 2 (diode conduction interval) duty cycle D_2.

6.3 Analysis of the isolated inverse–SEPIC of Fig. 6.39. You may assume that the converter operates in the continuous conduction mode, and that all inductor current ripples and capacitor voltage ripples are small.

(a) Derive expressions for the dc components of the magnetizing current, inductor current, and capacitor voltages.

(b) Derive analytical expressions for the rms values of the primary and secondary winding currents. Note that these quantities do not simply scale by the turns ratio.

6.4 The two–transistor flyback converter. The converter of Fig. 6.42 is sometimes used when the dc input voltage is high. Transistors Q_1 and Q_2 are driven with the same gating signal, such that they turn on and off simultaneously with the same duty cycle D. Diodes D_1 and D_2 ensure that the off state voltages of the transistors do not exceed V_g. The converter operates in discontinuous conduction mode. The magnetizing inductance, referred to the primary side, is L_M.

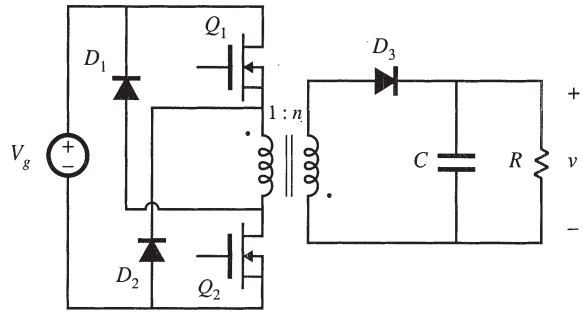


Fig. 6.42 Two-transistor flyback converter, Problem 6.4.

(a) Determine an analytical expression for the steady-state output voltage V.

(b) Over what range of duty cycles does the transformer reset properly? Explain.

6.5 A nonideal flyback converter. The flyback converter shown in Fig. 6.30(d) operates in the continuous conduction mode. The MOSFET has on-resistance R_{on}, and the diode has a constant forward voltage drop V_D. The flyback transformer has primary winding resistance R_p and secondary winding resistance R_s.

(a) Derive a complete steady-state equivalent circuit model, which is valid in the continuous conduction mode, and which correctly models the loss elements listed above as well as the converter input and output ports. Sketch your equivalent circuit.

(b) Derive an analytical expression for the converter efficiency.

6.6 A low-voltage computer power supply with synchronous rectification. The trend in digital integrated circuits is towards lower power supply voltages. It is difficult to construct a high-efficiency low-voltage power supply, because the conduction loss arising in the secondary-side diodes becomes very large. The objective of this problem is to estimate how the efficiency of a forward converter varies as the output voltage is reduced, and to investigate the use of synchronous rectifiers.

The forward converter of Fig. 6.22 operates from a dc input of $V_g = 325$ V, and supplies 20 A to its dc load. Consider three cases: (*i*) $V = 5$ V, (*ii*) $V = 3.3$ V, and (*iii*) $V = 1.5$ V. For each case, the turns ratio n_3/n_1 is chosen such that the converter produces the required output voltage at a transistor duty cycle of $D = 0.4$. The MOSFET has on-resistance $R_{on} = 5\ \Omega$. The secondary-side schottky diodes have

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forward voltage drops of $V_F = 0.5$ V. All other elements can be considered ideal.

(a) Derive an equivalent circuit for the forward converter, which models the semiconductor conduction losses described above.

(b) Solve your model for cases (*i*), (*ii*), and (*iii*) described above. For each case, determine numerical values of the turns ratio n_3/n_1 and for the efficiency η.

(c) The secondary-side Schottky diodes are replaced by MOSFETs operating as synchronous rectifiers. The MOSFETs each have an on-resistance of 4 mΩ. Determine the new numerical values of the turns ratio n_3/n_1 and the efficiency η, for cases (*i*), (*ii*), and (*iii*).

6.7 Rotation of switching cells. A network containing switches and reactive elements has terminals *a*, *b*, and *c*, as illustrated in Fig. 6.43(a). You are given that the relationship between the terminal voltages is $V_{bc}/V_{ac} = \mu(D)$.

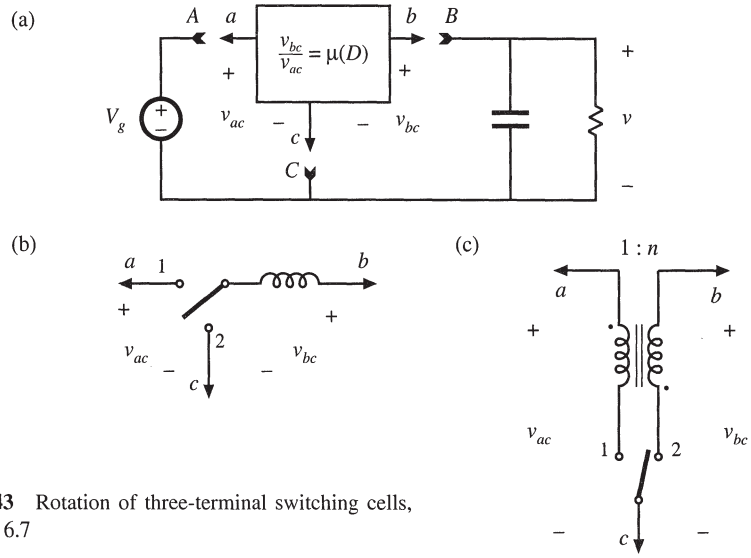


Fig. 6.43 Rotation of three-terminal switching cells, Problem 6.7

(a) Derive expressions for the source-to-load conversion ratio $V/V_g = M(D)$, in terms of $\mu(D)$, for the following three connection schemes:

(*i*) *a-A b-B c-C*

(*ii*) *a-B b-C c-A*

(*iii*) *a-C b-A c-B*

(b) Consider the three-terminal network of Fig. 6.43(b). Determine $\mu(D)$ for this network. Plug your answer into your results from part (a), to verify that the buck, boost, and buck–boost converters are generated.

(c) Consider the three-terminal network of Fig. 6.43(c). Determine $\mu(D)$ for this network. Plug your answer into your results from part (a). What converters are generated?

6.8 Transformer-isolated current-sense circuit. It is often required that the current flowing in a power transistor be sensed. A noninductive resistor *R* placed in series with the transistor will produce a voltage $v(t)$ that is proportional to the transistor drain current $i_D(t)$. Use of a transformer allows isolation between the power transistor and the control circuit. The transformer turns ratio also allows reduction of the current and power loss and increase of the voltage of the resistor. This problem is concerned with design of the transformer-isolated current-sense circuit of Fig. 6.44.

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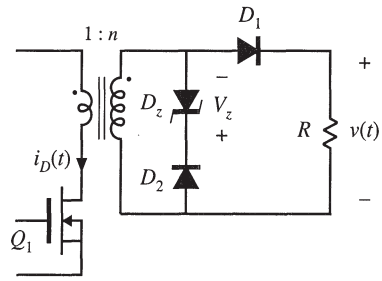


Fig. 6.44 Transformer-isolated circuit for sensing the transistor switch current, Problem 6.8

The transformer has a single-turn primary and an n-turn secondary winding. The transistor switches on and off with duty cycle D and switching frequency f_s. While the transistor conducts, its current is essentially constant and is equal to I. Diodes D_1 and D_2 are conventional silicon diodes having forward voltage drop V_D. Diode D_Z is a zener diode, which can be modeled as a voltage source of value V_Z, with the polarity indicated in the figure. For a proper design, the circuit elements should be chosen such that the transformer magnetizing current, in conjunction with diode D_2, operates in discontinuous conduction mode. In a good design, the magnetizing current is much smaller than the transistor current. Three subintervals occur during each switching period: subinterval 1, in which Q_1 and D_1 conduct; subinterval 2, in which D_2 and D_Z conduct; subinterval 3, in which Q_1, D_1 and D_2 are off.

(a) Sketch the current sense circuit, replacing the transformer and zener diode by their equivalent circuits.

(b) Sketch the waveforms of the transistor current $i_D(t)$, the transformer magnetizing current $i_M(t)$, the primary winding voltage, and the voltage $v(t)$. Label salient features.

(c) Determine the conditions on the zener voltage V_Z that ensure that the transformer magnetizing current is reset to zero before the end of the switching period.

(d) You are given the following specifications:

Switching frequency	$f_s = 100$ kHz
Transistor duty cycle	$D \leq 0.75$
Transistor peak current	max $i_D(t) \leq 25$ A

The output voltage $v(t)$ should equal 5 V when the transistor current is 25 A. To avoid saturating the transformer core, the volt-seconds applied to the single-turn primary winding while the transistor conducts should be no greater than 2 volt-μsec. The silicon diode forward voltage drops are $V_D = 0.7$ V.

Design the circuit: select values of R, n, and V_Z.

6.9 Optimal reset of the forward converter transformer. As illustrated in Fig. 6.45, it is possible to reset the transformer of the forward converter using a voltage source other than the dc input V_g; several such schemes appear in the literature. By optimally choosing the value of the reset voltage V_r, the peak voltage stresses imposed on transistor Q_1 and diode D_2 can be reduced. The maximum duty cycle can also be increased, leading to a lower transformer turns ratio and lower transistor current. The resulting improvement in converter cost and efficiency can be significant when the dc input voltage varies over a wide range.

(a) As a function of V_g, the transistor duty cycle D, and the transformer turns ratios, what is the minimum value of V_r that causes the transformer magnetizing current to be reset to zero by the end of the switching period?

(b) For your choice of V_r from part (a), what is the peak voltage imposed on transistor Q_1?

This converter is to be used in a universal-input off-line application, with the following specifications. The input voltage V_g can vary between 127 and 380 V. The load voltage is regulated by variation of the

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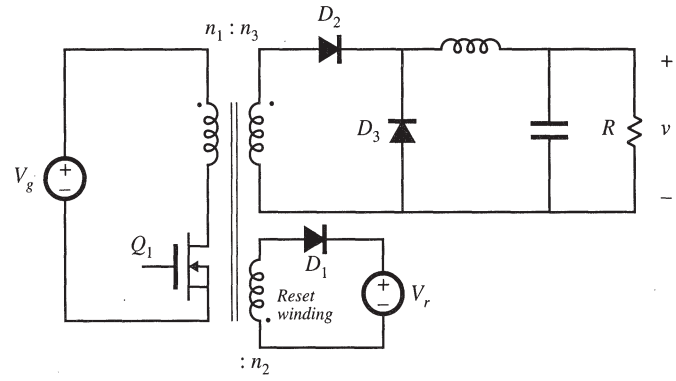


Fig. 6.45 Forward converter with auxiliary reset winding, Problem 6.9

duty cycle, and is equal to 12 V. The load power is 480 W.

(c) Choose the turns ratio n_3/n_1 such that the total active switch stress is minimized. For your choice of n_3/n_1, over what range will the duty cycle vary? What is the peak transistor current?

(d) Compare your design of Part (c) with the conventional scheme in which $n_1 = n_2$ and $V_r = V_g$. Compare the worst-case peak transistor voltage and peak transistor current.

(e) Suggest a way to implement the voltage source V_r. Give a schematic of the power-stage components of your implementation. Use a few sentences to describe the control-circuit functions required by your implementation, if any.

6.10 Design of a multiple-output dc-dc flyback converter. For this problem, you may neglect all losses and transformer leakage inductances. It is desired that the three-output flyback converter shown in Fig. 6.46 operates in the discontinuous conduction mode, with a switching frequency of $f_s = 100$ kHz. The nominal operating conditions are given in the diagram, and you may that there are no variations in the input voltage or the load currents. Select $D_3 = 0.1$ (the duty cycle of subinterval 3, in which all semiconductors are off). The objective of this problem is to find a good steady-state design, in which the semiconductor peak blocking voltages and peak currents are reasonably low.

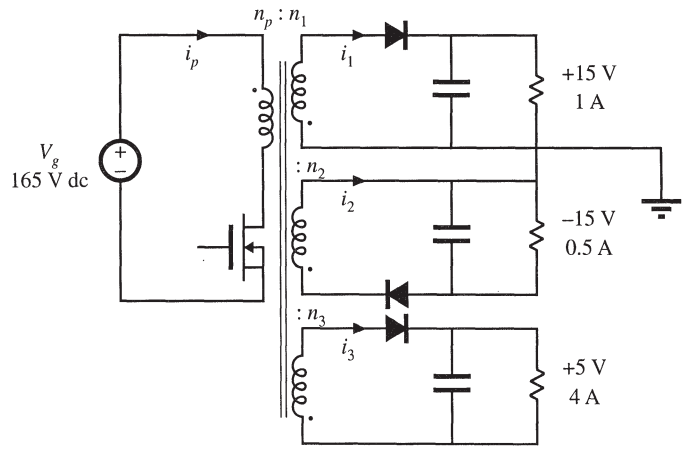


Fig. 6.46 Three-output flyback converter design, Problem 6.10.

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(a) It is possible to find a design in which the transistor peak blocking voltage is less than 300 V, and the peak diode blocking voltages are all less than 35 V, under steady-state conditions. Design the converter such that this is true. Specify: (*i*) the transistor duty cycle D, (*ii*) the magnetizing inductance L_M, referred to the primary, (*iii*) the turns ratios n_1/n_p and n_3/n_p.

(b) For your design of part (a), determine the rms currents of the four windings. Note that they don't simply scale by the turns ratios.

6.11 Spreadsheet design.

(a) Develop the analytical expressions for the "Results" and "Worst-case stresses" of the forward converter spreadsheet design example of Table 6.2.

(b) Enter the formulas you developed in part (a) into a computer spreadsheet, and verify that your computed values agree with those of Table 6.2.

(c) It is desired to reduce the forward converter peak transistor voltage to a value no greater than 650 V. Modify the design numbers to accomplish this, and briefly discuss the effect on the other component stresses.

(d) For these specifications, what is the largest possible value of the transistor utilization of the CCM forward converter? How should the spreadsheet design variables be chosen to attain the maximum transistor utilization?

6.12 Spreadsheet design of an isolated Ćuk converter. The isolated Ćuk converter of Fig. 6.40(c) is to be designed to meet the specifications listed in Table 6.2. The converter is to be designed such that it operates in continuous conduction mode at full load.

(a) Develop analytical expressions for the following quantities:

- The maximum and minimum duty cycles, for CCM operation
- The peak voltages and rms currents of both semiconductor devices
- The ripple magnitudes of the capacitor voltages and inductor currents
- The rms capacitor currents
- The transistor utilization U

(b) Enter the formulas you developed in part (a) into a computer spreadsheet. What are the design variables?

(c) For the specifications listed in Table 6.2, select the design variables to attain what you believe is the best design. Compare the performance of your design with the flyback and forward converter designs of Table 6.2.

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Part II

Converter Dynamics and Control

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7

AC Equivalent Circuit Modeling

7.1 INTRODUCTION

Converter systems invariably require feedback. For example, in a typical dc–dc converter application, the output voltage $v(t)$ must be kept constant, regardless of changes in the input voltage $v_g(t)$ or in the effective load resistance R. This is accomplished by building a circuit that varies the converter control input [i.e., the duty cycle $d(t)$] in such a way that the output voltage $v(t)$ is regulated to be equal to a desired reference value v_{ref}. In inverter systems, a feedback loop causes the output voltage to follow a sinusoidal reference voltage. In modern low-harmonic rectifier systems, a control system causes the converter input current to be proportional to the input voltage, such that the input port presents a resistive load to the ac source. So feedback is commonly employed.

A typical dc–dc system incorporating a buck converter and feedback loop block diagram is illustrated in Fig. 7.1. It is desired to design this feedback system in such a way that the output voltage is accurately regulated, and is insensitive to disturbances in $v_g(t)$ or in the load current. In addition, the feedback system should be stable, and properties such as transient overshoot, settling time, and steady-state regulation should meet specifications. The ac modeling and design of converters and their control systems such as Fig. 7.1 is the subject of Part II of this book.

To design the system of Fig. 7.1, we need a dynamic model of the switching converter. How do variations in the power input voltage, the load current, or the duty cycle affect the output voltage? What are the small-signal transfer functions? To answer these questions, we will extend the steady-state models developed in Chapters 2 and 3 to include the dynamics introduced by the inductors and capacitors of the converter. Dynamics of converters operating in the continuous conduction mode can be modeled using techniques quite similar to those of Chapters 2 and 3; the resulting ac equivalent circuits bear a strong resemblance to the dc equivalent circuits derived in Chapter 3.

Modeling is the representation of physical phenomena by mathematical means. In engineering,

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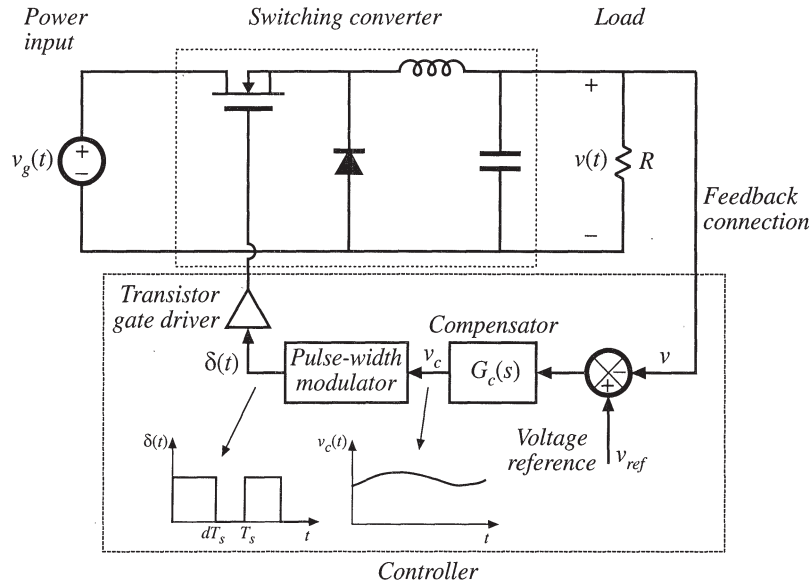


Fig. 7.1 A simple dc–dc regulator system, including a buck converter power stage and a feedback network.

it is desired to model the important dominant behavior of a system, while neglecting other insignificant phenomena. Simplified terminal equations of the component elements are used, and many aspects of the system response are neglected altogether, that is, they are "unmodeled." The resulting simplified model yields physical insight into the system behavior, which aids the engineer in designing the system to operate in a given specified manner. Thus, the modeling process involves use of approximations to neglect small but complicating phenomena, in an attempt to understand what is most important. Once this basic insight is gained, it may be desirable to carefully refine the model, by accounting for some of the previously ignored phenomena. It is a fact of life that real, physical systems are complex, and their detailed analysis can easily lead to an intractable and useless mathematical mess. Approximate models are an important tool for gaining understanding and physical insight.

As discussed in Chapter 2, the switching ripple is small in a well-designed converter operating in continuous conduction mode (CCM). Hence, we should ignore the switching ripple, and model only the underlying ac variations in the converter waveforms. For example, suppose that some ac variation is introduced into the converter duty cycle $d(t)$, such that

$$d(t) = D + D_m \cos\omega_m t \tag{7.1}$$

where D and D_m are constants, $| D_m | \ll D$, and the modulation frequency ω_m is much smaller than the converter switching frequency $\omega_s = 2\pi f_s$. The resulting transistor gate drive signal is illustrated in Fig. 7.2(a), and a typical converter output voltage waveform $v(t)$ is illustrated in Fig. 7.2(b). The spectrum of $v(t)$ is illustrated in Fig. 7.3. This spectrum contains components at the switching frequency as well as its harmonics and sidebands; these components are small in magnitude if the switching ripple is small. In addition, the spectrum contains a low-frequency component at the modulation frequency ω_m. The magnitude and phase of this component depend not only on the duty cycle variation, but also on the frequency response of the converter. If we neglect the switching ripple, then this low-frequency compo-

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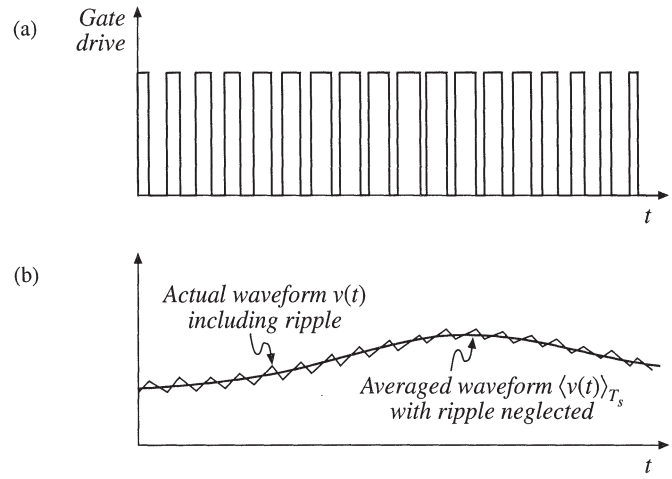


Fig. 7.2 Ac variation of the converter signals: (a) transistor gate drive signal, in which the duty cycle varies slowly, and (b) the resulting converter output voltage waveform. Both the actual waveform $v(t)$ (including high frequency switching ripple) and its averaged, low-frequency component, $\langle v(t)\rangle_{T_s}$, are illustrated.

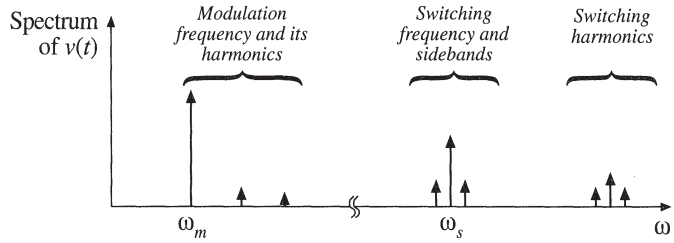


Fig. 7.3 Spectrum of the output voltage waveform $v(t)$ of Fig. 7.2.

nent remains [also illustrated in Fig. 7.2(b)]. The objective of our ac modeling efforts is to predict this low-frequency component.

A simple method for deriving the small-signal model of CCM converters is explained in Section 7.2. The switching ripples in the inductor current and capacitor voltage waveforms are removed by averaging over one switching period. Hence, the low-frequency components of the inductor and capacitor waveforms are modeled by equations of the form

$$\begin{aligned} L\frac{d\langle i_L(t)\rangle_{T_s}}{dt} &= \langle v_L(t)\rangle_{T_s} \\ C\frac{d\langle v_C(t)\rangle_{T_s}}{dt} &= \langle i_C(t)\rangle_{T_s} \end{aligned} \tag{7.2}$$

where $\langle x(t)\rangle_{T_s}$ denotes the average of $x(t)$ over an interval of length T_s:

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$$\langle x(t) \rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} x(\tau) d\tau \tag{7.3}$$

So we will employ the basic approximation of removing the high-frequency switching ripple by averaging over one switching period. Yet the average value is allowed to vary from one switching period to the next, such that low-frequency variations are modeled. In effect, the "moving average" of Eq. (7.3) constitutes low-pass filtering of the waveform. A few of the numerous references on averaged modeling of switching converters are listed at the end of this chapter [1–20].

Note that the principles of inductor volt-second balance and capacitor charge balance predict that the right-hand sides of Eqs. (7.2) are zero when the converter operates in equilibrium. Equations (7.2) describe how the inductor currents and capacitor voltages change when nonzero average inductor voltage and capacitor current are applied over a switching period.

The averaged inductor voltage and capacitor currents of Eq. (7.2) are, in general, nonlinear functions of the signals in the converter, and hence Eqs. (7.2) constitute a set of nonlinear differential equations. Indeed, the spectrum in Fig. 7.3 also contains harmonics of the modulation frequency ω_m. In most converters, these harmonics become significant in magnitude as the modulation frequency ω_m approaches the switching frequency ω_s, or as the modulation amplitude D_m approaches the quiescent duty cycle D. Nonlinear elements are not uncommon in electrical engineering; indeed, all semiconductor devices exhibit nonlinear behavior. To obtain a linear model that is easier to analyze, we usually construct a small-signal model that has been linearized about a quiescent operating point, in which the harmonics of the modulation or excitation frequency are neglected. As an example, Fig. 7.4 illustrates linearization of the familiar diode i–v characteristic shown in Fig. 7.4(b). Suppose that the diode current $i(t)$ has a quiescent (dc) value I and a signal component $\hat{i}(t)$. As a result, the voltage $v(t)$ across the diode has a quiescent value V and a signal component $\hat{v}(t)$. If the signal components are small compared to the quiescent values,

$$|\hat{v}| \ll |V|, \quad |\hat{i}| \ll |I| \tag{7.4}$$

then the relationship between $\hat{v}(t)$ and $\hat{i}(t)$ is approximately linear, $\hat{v}(t) = r_D \hat{i}(t)$. The conductance $1/r_D$

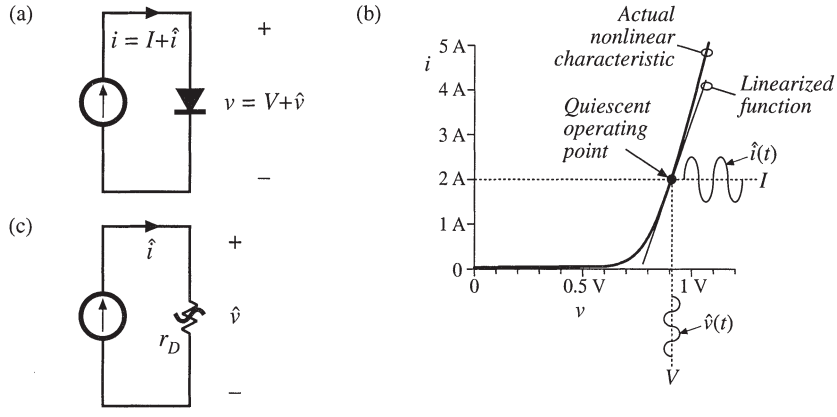


Fig. 7.4 Small-signal equivalent circuit modeling of the diode: (a) a nonlinear diode conducting current i; (b) linearization of the diode characteristic around a quiescent operating point; (c) a linearized small-signal model.

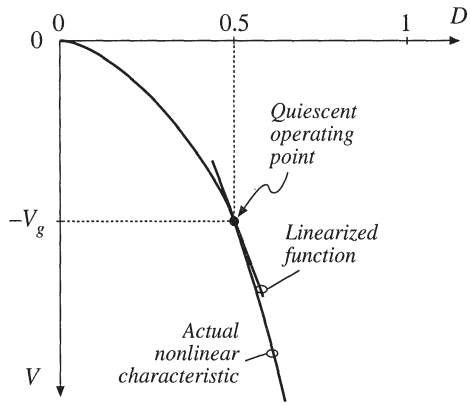


Fig. 7.5 Linearization of the static control-to-output characteristic of the buck-boost converter about the quiescent operating point $D = 0.5$.

represents the slope of the diode characteristic, evaluated at the quiescent operating point. The small-signal equivalent circuit model of Fig. 7.4(c) describes the diode behavior for small variations around the quiescent operating point.

An example of a nonlinear converter characteristic is the dependence of the steady-state output voltage V of the buck-boost converter on the duty cycle D, illustrated in Fig. 7.5. Suppose that the converter operates with some dc output voltage, say, $V = -V_g$, corresponding to a quiescent duty cycle of $D = 0.5$. Duty cycle variations $\hat{d}$ about this quiescent value will excite variations $\hat{v}$ in the output voltage. If the magnitude of the duty cycle variation is sufficiently small, then we can compute the resulting output voltage variations by linearizing the curve. The slope of the linearized characteristic in Fig. 7.5 is chosen to be equal to the slope of the actual nonlinear characteristic at the quiescent operating point; this slope is the dc control-to-output gain of the converter. The linearized and nonlinear characteristics are approximately equal in value provided that the duty cycle variations $\hat{d}$ are sufficiently small.

Although it illustrates the process of small-signal linearization, the buck-boost example of Fig. 7.5 is oversimplified. The inductors and capacitors of the converter cause the gain to exhibit a frequency response. To correctly predict the poles and zeroes of the small-signal transfer functions, we must linearize the converter averaged differential equations, Eqs. (7.2). This is done in Section 7.2. A small-signal ac equivalent circuit can then be constructed using the methods developed in Chapter 3. The resulting small-signal model of the buck-boost converter is illustrated in Fig. 7.6; this model can be solved using conventional circuit analysis techniques, to find the small-signal transfer functions, output impedance, and other frequency-dependent properties. In systems such as Fig. 7.1, the equivalent circuit model can be inserted in place of the converter. When small-signal models of the other system elements (such as the

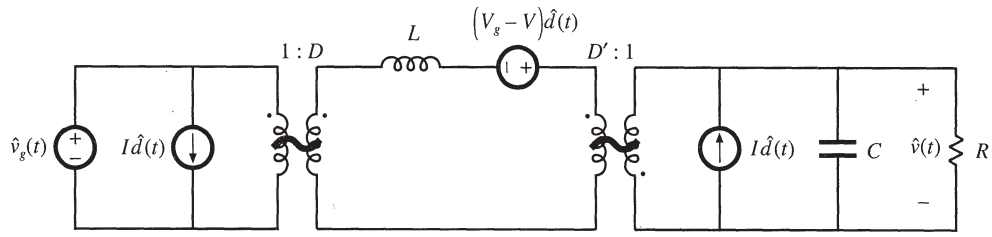


Fig. 7.6 Small-signal ac equivalent circuit model of the buck-boost converter.

pulse-width modulator) are inserted, then a complete linearized system model is obtained. This model can be analyzed using standard linear techniques, such as the Laplace transform, to gain insight into the behavior and properties of the system.

Two well-known variants of the ac modeling method, state-space averaging and circuit averaging, are explained in Sections 7.3 and 7.4. An extension of circuit averaging, known as *averaged switch modeling*, is also discussed in Section 7.4. Since the switches are the only elements that introduce switching harmonics, equivalent circuit models can be derived by averaging only the switch waveforms. The converter models suitable for analysis or simulation are obtained simply by replacing the switches with the averaged switch model. The averaged switch modeling technique can be extended to other modes of operation such as the discontinuous conduction mode, as well as to current programmed control and to resonant converters. In Section 7.5, it is shown that the small-signal model of any dc–dc pulse-width modulated CCM converter can be written in a standard form. Called the *canonical model*, this equivalent circuit describes the basic physical functions that any of these converters must perform. A simple model of the pulse-width modulator circuit is described in Section 7.6.

These models are useless if you don't know how to apply them. So in Chapter 8, the frequency response of converters is explored, in a design-oriented and detailed manner. Small-signal transfer functions of the basic converters are tabulated. Bode plots of converter transfer functions and impedances are derived in a simple, approximate manner, which allows insight to be gained into the origins of the frequency response of complex converter systems.

These results are used to design converter control systems in Chapter 9 and input filters in Chapter 10. The modeling techniques are extended in Chapters 11 and 12 to cover the discontinuous conduction mode and the current programmed mode.

7.2 THE BASIC AC MODELING APPROACH

Let us derive a small-signal ac model of the buck-boost converter of Fig. 7.7. The analysis begins as usual, by determining the voltage and current waveforms of the inductor and capacitor. When the switch is in position 1, the circuit of Fig. 7.8(a) is obtained. The inductor voltage and capacitor current are:

$$v_L(t) = L\frac{di(t)}{dt} = v_g(t) \tag{7.5}$$

$$i_C(t) = C\frac{dv(t)}{dt} = -\frac{v(t)}{R} \tag{7.6}$$

We now make the small-ripple approximation. But rather than replacing $v_g(t)$ and $v(t)$ with their dc components V_g and V as in Chapter 2, we now replace them with their low-frequency averaged values $\langle v_g(t)\rangle_{T_s}$ and $\langle v(t)\rangle_{T_s}$, defined by Eq. (7.3). Equations (7.5) and (7.6) then become

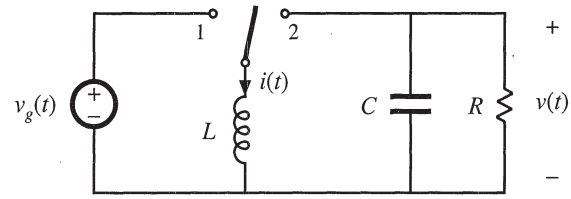


Fig. 7.7 Buck-boost converter example.

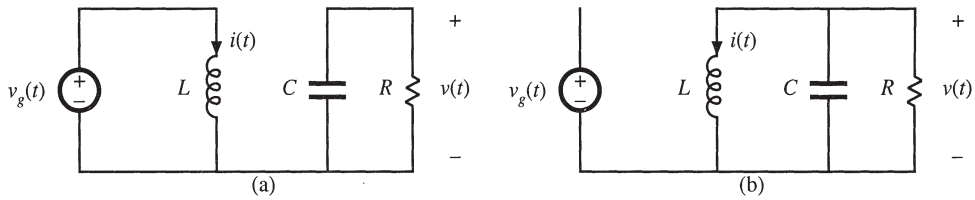


Fig. 7.8 Buck-boost converter circuit: (a) when the switch is in position 1, (b) when the switch is in position 2.

$$v_L(t) = L\frac{di(t)}{dt} \approx \langle v_g(t) \rangle_{T_s} \tag{7.7}$$

$$i_C(t) = C\frac{dv(t)}{dt} \approx -\frac{\langle v(t) \rangle_{T_s}}{R} \tag{7.8}$$

Hence, during the first subinterval, the inductor current $i(t)$ and the capacitor voltage $v(t)$ change with the essentially constant slopes given by Eqs. (7.7) and (7.8). With the switch in position 2, the circuit of Fig. 7.8(b) is obtained. Its inductor voltage and capacitor current are:

$$v_L(t) = L\frac{di(t)}{dt} = v(t) \tag{7.9}$$

$$i_C(t) = C\frac{dv(t)}{dt} = -i(t) - \frac{v(t)}{R} \tag{7.10}$$

Use of the small-ripple approximation, to replace $i(t)$ and $v(t)$ with their averaged values, yields

$$v_L(t) = L\frac{di(t)}{dt} \approx \langle v(t) \rangle_{T_s} \tag{7.11}$$

$$i_C(t) = C\frac{dv(t)}{dt} \approx -\langle i(t) \rangle_{T_s} - \frac{\langle v(t) \rangle_{T_s}}{R} \tag{7.12}$$

During the second subinterval, the inductor current and capacitor voltage change with the essentially constant slopes given by Eqs. (7.11) and (7.12).

7.2.1 Averaging the Inductor Waveforms

The inductor voltage and current waveforms are sketched in Fig. 7.9. The low-frequency average of the inductor voltage is found by evaluation of Eq. (7.3)—the inductor voltage during the first and second subintervals, given by Eqs. (7.7) and (7.11), are averaged:

$$\langle v_L(t) \rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} v_L(\tau)d\tau \approx d(t)\langle v_g(t) \rangle_{T_s} + d'(t)\langle v(t) \rangle_{T_s} \tag{7.13}$$

where $d'(t) = 1 - d(t)$. The right-hand side of Eq. (7.13) contains no switching harmonics, and models

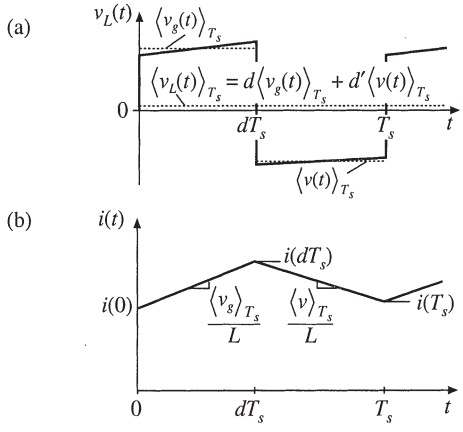


Fig. 7.9 Buck-boost converter waveforms: (a) inductor voltage, (b) inductor current.

only the low-frequency components of the inductor voltage waveform. Insertion of this equation into Eq. (7.2) leads to

$$L\frac{d\langle i(t)\rangle_{T_s}}{dt} = d(t)\langle v_g(t)\rangle_{T_s} + d'(t)\langle v(t)\rangle_{T_s} \tag{7.14}$$

This equation describes how the low-frequency components of the inductor current vary with time.

7.2.2 Discussion of the Averaging Approximation

In steady-state, the actual inductor current waveform $i(t)$ is periodic with period equal to the switching period T_s: $i(t + T_s) = i(t)$. During transients, there is a net change in $i(t)$ over one switching period. This net change in inductor current is correctly predicted by use of the average inductor voltage. We can show that this is true, based on the inductor equation

$$L\frac{di(t)}{dt} = v_L(t) \tag{7.15}$$

Divide by L, and integrate both sides from t to $t + T_s$:

$$\int_t^{t+T_s} di = \frac{1}{L}\int_t^{t+T_s} v_L(\tau)d\tau \tag{7.16}$$

The left-hand side of Eq. (7.16) is $i(t + T_s) - i(t)$, while the right-hand side can be expressed in terms of the definition of $\langle v_L(t)\rangle_{T_s}$, Eq. (7.3), by multiplying and dividing by T_s to obtain

$$i(t + T_s) - i(t) = \frac{1}{L}T_s\langle v_L(t)\rangle_{T_s} \tag{7.17}$$

The left-hand side of Eq. (7.17) is the net change in inductor current over one complete switching period. Equation (7.17) states that this change is exactly equal to the switching period T_s multiplied by the aver-

age slope $\langle v_L(t)\rangle_{T_s}/L$.

Equation (7.17) can be rearranged to obtain

$$L\frac{i(t+T_s)-i(t)}{T_s} = \langle v_L(t)\rangle_{T_s} \tag{7.18}$$

Let us now find the derivative of $\langle i(t)\rangle_{T_s}$:

$$\frac{d\langle i(t)\rangle_{T_s}}{dt} = \frac{d}{dt}\left(\frac{1}{T_s}\int_t^{t+T_s} i(\tau)d\tau\right) = \frac{i(t+T_s)-i(t)}{T_s} \tag{7.19}$$

Substitution of Eq. (7.19) into (7.18) leads to

$$L\frac{d\langle i(t)\rangle_{T_s}}{dt} = \langle v_L(t)\rangle_{T_s} \tag{7.20}$$

which coincides with Eq. (7.2).

Let us next compute how the inductor current changes over one switching period in our buck-boost example. The inductor current waveform is sketched in Fig. 7.9(b). Assume that the inductor current begins at some arbitrary value $i(0)$. During the first subinterval, the inductor current changes with the essentially constant value given by Eq. (7.7). The value at the end of the first subinterval is

$$\underbrace{i(dT_s)}_{\text{(final value)}} = \underbrace{i(0)}_{\text{(initial value)}} + \underbrace{(dT_s)}_{\text{(length of interval)}} \underbrace{\left(\frac{\langle v_g(t)\rangle_{T_s}}{L}\right)}_{\text{(average slope)}} \tag{7.21}$$

During the second subinterval, the inductor current changes with the essentially constant value given by Eq. (7.11). Hence, the value at the end of the second subinterval is

$$\underbrace{i(T_s)}_{\text{(final value)}} = \underbrace{i(dT_s)}_{\text{(initial value)}} + \underbrace{(d'T_s)}_{\text{(length of interval)}} \underbrace{\left(\frac{\langle v(t)\rangle_{T_s}}{L}\right)}_{\text{(average slope)}} \tag{7.22}$$

By substitution of Eq. (7.21) into Eq. (7.22), we can express $i(T_s)$ in terms of $i(0)$,

$$i(T_s) = i(0) + \frac{T_s}{L}\underbrace{\left(d(t)\langle v_g(t)\rangle_{T_s} + d'(t)\langle v(t)\rangle_{T_s}\right)}_{\langle v_L(t)\rangle_{T_s}} \tag{7.23}$$

Equations (7.21) to (7.23) are illustrated in Fig. 7.10. Equation (7.23) expresses the final value $i(T_s)$ directly in terms of $i(0)$, without the intermediate step of calculating $i(DT_s)$. This equation can be interpreted in the same manner as Eqs. (7.21) and (7.22): the final value $i(T_s)$ is equal to the initial value $i(0)$, plus the length of the interval T_s multiplied by the average slope $\langle v_L(t)\rangle_{T_s}/L$. But note that the interval length is chosen to coincide with the switching period, such that the switching ripple is effectively

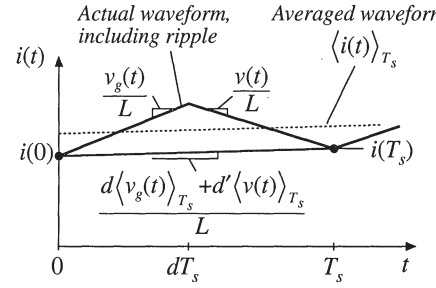


Fig. 7.10 Use of the average slope to predict how the inductor current waveform changes over one switching period. The actual waveform $i(t)$ and its low-frequency component $\langle i(t)\rangle_{T_s}$ are illustrated.

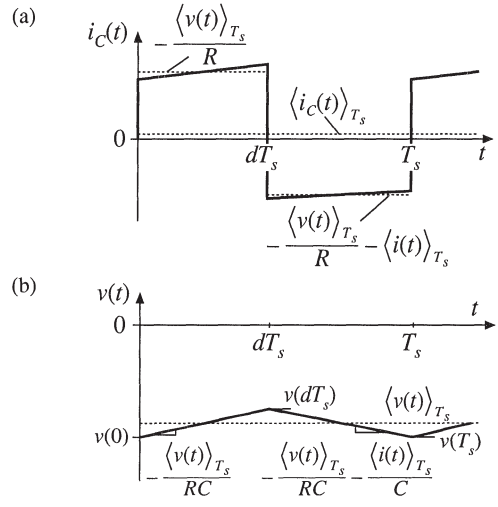


Fig. 7.11 Buck-boost converter waveforms: (a) capacitor current, (b) capacitor voltage.

removed. Also, the use of the average slope leads to correct prediction of the final value $i(T_s)$. It can be easily verified that, when Eq. (7.23) is inserted into Eq. (7.19), the previous result (7.14) is obtained.

7.2.3 Averaging the Capacitor Waveforms

A similar procedure leads to the capacitor dynamic equation. The capacitor voltage and current waveforms are sketched in Fig. 7.11. The average capacitor current can be found by averaging Eqs. (7.8) and (7.12); the result is

$$\langle i_C(t)\rangle_{T_s} = d(t)\left(-\frac{\langle v(t)\rangle_{T_s}}{R}\right) + d'(t)\left(-\langle i(t)\rangle_{T_s} - \frac{\langle v(t)\rangle_{T_s}}{R}\right) \tag{7.24}$$

Upon inserting this equation into Eq. (7.2) and collecting terms, one obtains

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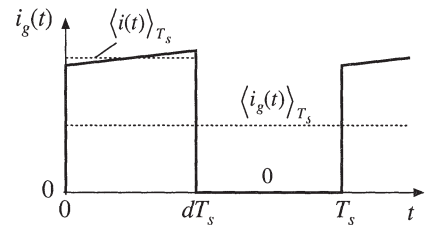


Fig. 7.12 Buck-boost converter waveforms: input source current $i_g(t)$.

$$C \frac{d\langle v(t) \rangle_{T_s}}{dt} = -d'(t) \langle i(t) \rangle_{T_s} - \frac{\langle v(t) \rangle_{T_s}}{R} \tag{7.25}$$

This is the basic averaged equation which describes dc and low-frequency ac variations in the capacitor voltage.

7.2.4 The Average Input Current

In Chapter 3, it was found to be necessary to write an additional equation that models the dc component of the converter input current. This allowed the input port of the converter to be modeled by the dc equivalent circuit. A similar procedure must be followed here, so that low-frequency variations at the converter input port are modeled by the ac equivalent circuit.

For the buck-boost converter example, the current $i_g(t)$ drawn by the converter from the input source is equal to the inductor current $i(t)$ during the first subinterval, and zero during the second subinterval. By neglecting the inductor current ripple and replacing $i(t)$ with its averaged value $\langle i(t) \rangle_{T_s}$, we can express the input current as follows:

$$i_g(t) = \begin{cases} \langle i(t) \rangle_{T_s} & \text{during subinterval 1} \\ 0 & \text{during subinterval 2} \end{cases} \tag{7.26}$$

The input current waveform is illustrated in Fig. 7.12. Upon averaging over one switching period, one obtains

$$\langle i_g(t) \rangle_{T_s} = d(t) \langle i(t) \rangle_{T_s} \tag{7.27}$$

This is the basic averaged equation which describes dc and low-frequency ac variations in the converter input current.

7.2.5 Perturbation and Linearization

The buck-boost converter averaged equations, Eqs. (7.14), (7.25), and (7.27), are collected below:

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$$
\begin{aligned}
L\frac{d\langle i(t)\rangle_{T_s}}{dt} &= d(t)\,\langle v_g(t)\rangle_{T_s} + d'(t)\,\langle v(t)\rangle_{T_s} \\
C\frac{d\langle v(t)\rangle_{T_s}}{dt} &= -d'(t)\,\langle i(t)\rangle_{T_s} - \frac{\langle v(t)\rangle_{T_s}}{R} \\
\langle i_g(t)\rangle_{T_s} &= d(t)\,\langle i(t)\rangle_{T_s}
\end{aligned}
\tag{7.28}
$$

These equations are nonlinear because they involve the multiplication of time-varying quantities. For example, the capacitor current depends on the product of the control input $d'(t)$ and the low-frequency component of the inductor current, $\langle i(t)\rangle_{T_s}$. Multiplication of time-varying signals generates harmonics, and is a nonlinear process. Most of the techniques of ac circuit analysis, such as the Laplace transform and other frequency-domain methods, are not useful for nonlinear systems. So we need to linearize Eqs. (7.28) by constructing a small-signal model.

Suppose that we drive the converter at some steady-state, or quiescent, duty ratio $d(t) = D$, with quiescent input voltage $v_g(t) = V_g$. We know from our steady-state analysis of Chapters 2 and 3 that, after any transients have subsided, the inductor current $\langle i(t)\rangle_{T_s}$, the capacitor voltage $\langle v(t)\rangle_{T_s}$, and the input current $\langle i_g(t)\rangle_{T_s}$ will reach the quiescent values I, V, and I_g, respectively, where

$$
\begin{aligned}
V &= -\frac{D}{D'}\,V_g \\
I &= -\frac{V}{D'R} \\
I_g &= DI
\end{aligned}
\tag{7.29}
$$

Equations (7.29) are derived as usual via the principles of inductor volt-second and capacitor charge balance. They could also be derived from Eqs. (7.28) by noting that, in steady state, the derivatives must equal zero.

To construct a small-signal ac model at a quiescent operating point (I, V), one assumes that the input voltage $v_g(t)$ and the duty cycle $d(t)$ are equal to some given quiescent values V_g and D, plus some superimposed small ac variations $\hat{v}_g(t)$ and $\hat{d}(t)$. Hence, we have

$$
\begin{aligned}
\langle v_g(t)\rangle_{T_s} &= V_g + \hat{v}_g(t) \\
d(t) &= D + \hat{d}(t)
\end{aligned}
\tag{7.30}
$$

In response to these inputs, and after any transients have subsided, the averaged inductor current $\langle i(t)\rangle_{T_s}$, the averaged capacitor voltage $\langle v(t)\rangle_{T_s}$, and the averaged input current $\langle i_g(t)\rangle_{T_s}$ waveforms will be equal to the corresponding quiescent values I, V, and I_g, plus some superimposed small ac variations $\hat{i}(t)$, $\hat{v}(t)$, and $\hat{i}_g(t)$:

$$
\begin{aligned}
\langle i(t)\rangle_{T_s} &= I + \hat{i}(t) \\
\langle v(t)\rangle_{T_s} &= V + \hat{v}(t) \\
\langle i_g(t)\rangle_{T_s} &= I_g + \hat{i}_g(t)
\end{aligned}
\tag{7.31}
$$

With the assumptions that the ac variations are small in magnitude compared to the dc quiescent values, or

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$$\begin{aligned} \left|\hat{v}_g(t)\right| &\ll \left|V_g\right| \\ \left|\hat{d}(t)\right| &\ll \left|D\right| \\ \left|\hat{i}(t)\right| &\ll \left|I\right| \\ \left|\hat{v}(t)\right| &\ll \left|V\right| \\ \left|\hat{i}_g(t)\right| &\ll \left|I_g\right| \end{aligned} \tag{7.32}$$

then the nonlinear equations (7.28) can be linearized. This is done by inserting Eqs. (7.30) and (7.31) into Eq. (7.28). For the inductor equation, one obtains

$$L\frac{d\left(I+\hat{i}(t)\right)}{dt} = \left(D+\hat{d}(t)\right)\left(V_g+\hat{v}_g(t)\right) + \left(D'-\hat{d}(t)\right)\left(V+\hat{v}(t)\right) \tag{7.33}$$

It should be noted that the complement of the duty cycle is given by

$$d'(t) = \left(1-d(t)\right) = 1-\left(D+\hat{d}(t)\right) = D'-\hat{d}(t) \tag{7.34}$$

where $D' = 1 - D$. The minus sign arises in the expression for $d'(t)$ because a $d(t)$ variation that causes $d(t)$ to increase will cause $d'(t)$ to decrease.

By multiplying out Eq. (7.33) and collecting terms, one obtains

$$L\left(\frac{dI}{dt}+\frac{d\hat{i}(t)}{dt}\right) = \underbrace{\left(DV_g+D'V\right)}_{\text{Dc terms}} + \underbrace{\left(D\hat{v}_g(t)+D'\hat{v}(t)+\left(V_g-V\right)\hat{d}(t)\right)}_{1^{st}\text{ order ac terms (linear)}} + \underbrace{\hat{d}(t)\left(\hat{v}_g(t)-\hat{v}(t)\right)}_{2^{nd}\text{ order ac terms (nonlinear)}} \tag{7.35}$$

The derivative of I is zero, since I is by definition a dc (constant) term. For the purposes of deriving a small-signal ac model, the dc terms can be considered known constant quantities. On the right-hand side of Eq. (7.35), three types of terms arise:

Dc terms: These terms contain dc quantities only.

First-order ac terms: Each of these terms contains a single ac quantity, usually multiplied by a constant coefficient such as a dc term. These terms are linear functions of the ac variations.

Second-order ac terms: These terms contain the products of ac quantities. Hence they are nonlinear, because they involve the multiplication of time-varying signals.

It is desired to neglect the nonlinear ac terms. Provided that the small-signal assumption, Eq. (7.32), is satisfied, then each of the second-order nonlinear terms is much smaller in magnitude that one or more of the linear first-order ac terms. For example, the second-order ac term $\hat{d}(t)\hat{v}_g(t)$ is much smaller in magnitude than the first-order ac term $D\hat{v}_g(t)$ whenever $\left|\hat{d}(t)\right| \ll D$. So we can neglect the second-order terms. Also, by definition [or by use of Eq. (7.29)], the dc terms on the right-hand side of the equation are equal to the dc terms on the left-hand side, or zero.

We are left with the first-order ac terms on both sides of the equation. Hence,

$$L\frac{d\hat{i}(t)}{dt} = D\hat{v}_g(t) + D'\hat{v}(t) + \left(V_g-V\right)\hat{d}(t) \tag{7.36}$$

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This is the desired result: the small-signal linearized equation that describes variations in the inductor current.

The capacitor equation can be linearized in a similar manner. Insertion of Eqs. (7.30) and (7.31) into the capacitor equation of Eq. (7.28) yields

$$C\frac{d\left(V+\hat{v}(t)\right)}{dt} = -\left(D'-\hat{d}(t)\right)\left(I+\hat{i}(t)\right) - \frac{\left(V+\hat{v}(t)\right)}{R} \tag{7.37}$$

Upon multiplying out Eq. (7.37) and collecting terms, one obtains

$$C\left(\frac{dV}{dt}+\frac{d\hat{v}(t)}{dt}\right) = \underbrace{\left(-D'I-\frac{V}{R}\right)}_{\text{Dc terms}} + \underbrace{\left(-D'\hat{i}(t)-\frac{\hat{v}(t)}{R}+I\hat{d}(t)\right)}_{1^{st}\text{ order ac terms (linear)}} + \underbrace{\hat{d}(t)\hat{i}(t)}_{2^{nd}\text{ order ac term (nonlinear)}} \tag{7.38}$$

By neglecting the second-order terms, and noting that the dc terms on both sides of the equation are equal, we again obtain a linearized first-order equation, containing only the first-order ac terms of Eq. (7.38):

$$C\frac{d\hat{v}(t)}{dt} = -D'\hat{i}(t) - \frac{\hat{v}(t)}{R} + I\hat{d}(t) \tag{7.39}$$

This is the desired small-signal linearized equation that describes variations in the capacitor voltage.

Finally, the equation of the average input current is also linearized. Insertion of Eqs. (7.30) and (7.31) into the input current equation of Eq. (7.28) yields

$$I_g + \hat{i}_g(t) = \left(D+\hat{d}(t)\right)\left(I+\hat{i}(t)\right) \tag{7.40}$$

By collecting terms, we obtain

$$\underbrace{I_g}_{\text{Dc term}} + \underbrace{\hat{i}_g(t)}_{1^{st}\text{ order ac term}} = \underbrace{\left(DI\right)}_{\text{Dc term}} + \underbrace{\left(D\hat{i}(t)+I\hat{d}(t)\right)}_{1^{st}\text{ order ac terms (linear)}} + \underbrace{\hat{d}(t)\hat{i}(t)}_{2^{nd}\text{ order ac term (nonlinear)}} \tag{7.41}$$

We again neglect the second-order nonlinear terms. The dc terms on both sides of the equation are equal. The remaining first-order linear ac terms are

$$\hat{i}_g(t) = D\hat{i}(t) + I\hat{d}(t) \tag{7.42}$$

This is the linearized small-signal equation that describes the low-frequency ac components of the converter input current.

In summary, the nonlinear averaged equations of a switching converter can be linearized about a quiescent operating point. The converter independent inputs are expressed as constant (dc) values, plus small ac variations. In response, the converter averaged waveforms assume similar forms. Insertion of Eqs. (7.30) and (7.31) into the converter averaged nonlinear equations yields dc terms, linear ac terms, and nonlinear terms. If the ac variations are sufficiently small in magnitude, then the nonlinear terms are

much smaller than the linear ac terms, and so can be neglected. The remaining linear ac terms comprise the small-signal ac model of the converter.

7.2.6 Construction of the Small-Signal Equivalent Circuit Model

Equations (7.36), (7.39), and (7.42) are the small-signal ac description of the ideal buck-boost converter, and are collected below:

$$\begin{aligned} L\frac{d\hat{i}(t)}{dt} &= D\hat{v}_g(t) + D'\hat{v}(t) + \left(V_g - V\right)\hat{d}(t) \\ C\frac{d\hat{v}(t)}{dt} &= -D'\hat{i}(t) - \frac{\hat{v}(t)}{R} + I\hat{d}(t) \\ \hat{i}_g(t) &= D\hat{i}(t) + I\hat{d}(t) \end{aligned} \tag{7.43}$$

In Chapter 3, we collected the averaged dc equations of a converter, and reconstructed an equivalent circuit that modeled the dc properties of the converter. We can use the same procedure here, to construct averaged small-signal ac models of converters.

The inductor equation of (7.43), or Eq. (7.36), describes the voltages around a loop containing the inductor. Indeed, this equation was derived by finding the inductor voltage via loop analysis, then averaging, perturbing, and linearizing. So the equation represents the voltages around a loop of the small-signal model, which contains the inductor. The loop current is the small-signal ac inductor current $\hat{i}(t)$. As illustrated in Fig. 7.13, the term $L\,d\hat{i}(t)/dt$ represents the voltage across the inductor L in the small-signal model. This voltage is equal to three other voltage terms. $D\hat{v}_g(t)$ and $D'\hat{v}(t)$ represent dependent sources as shown. These terms will be combined into ideal transformers. The term $(V_g - V)\hat{d}(t)$ is driven by the control input $\hat{d}(t)$, and is represented by an independent source as shown.

The capacitor equation of (7.43), or Eq. (7.39), describes the currents flowing into a node attached to the capacitor. This equation was derived by finding the capacitor current via node analysis, then averaging, perturbing, and linearizing. Hence, this equation describes the currents flowing into a node of the small-signal model, attached to the capacitor. As illustrated in Fig. 7.14, the term $C\,d\hat{v}(t)/dt$ represents the current flowing through capacitor C in the small-signal model. The capacitor voltage is $\hat{v}(t)$. According to the equation, this current is equal to three other terms. The term $-D'\hat{i}(t)$ represents a dependent source, which will eventually be combined into an ideal transformer. The term $-\hat{v}(t)/R$ is rec-

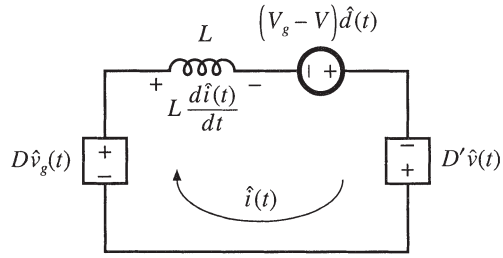


Fig. 7.13 Circuit equivalent to the small-signal ac inductor loop equation of Eq. (7.43) or (7.36).

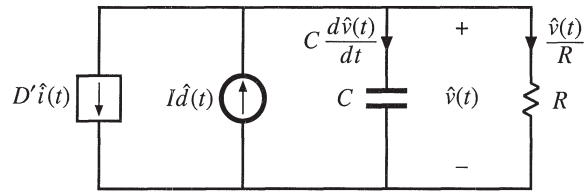


Fig. 7.14 Circuit equivalent to the small-signal ac capacitor node equation of Eq. (7.43) or (7.39).

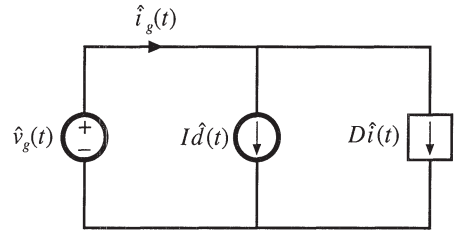


Fig. 7.15 Circuit equivalent to the small-signal ac input source current equation of Eq. (7.43) or (7.42).

ognized as the current flowing through the load resistor in the small-signal model. The resistor is connected in parallel with the capacitor, such that the ac voltage across the resistor R is $\hat{v}(t)$ as expected. The term $I\hat{d}(t)$ is driven by the control input $\hat{d}(t)$, and is represented by an independent source as shown.

Finally, the input current equation of (7.43), or Eq. (7.42), describes the small-signal ac current $\hat{i}_g(t)$ drawn by the converter out of the input voltage source $\hat{v}_g(t)$. This is a node equation which states that $\hat{i}_g(t)$ is equal to the currents in two branches, as illustrated in Fig. 7.15. The first branch, corresponding to the $D\hat{i}(t)$ term, is dependent on the ac inductor current $\hat{i}(t)$. Hence, we represent this term using a dependent current source; this source will eventually be incorporated into an ideal transformer. The second branch, corresponding to the $I\hat{d}(t)$ term, is driven by the control input $\hat{d}(t)$, and is represented by an independent source as shown.

The circuits of Figs. 7.13, 7.14, and 7.15 are collected in Fig. 7.16(a). As discussed in Chapter 3, the dependent sources can be combined into effective ideal transformers, as illustrated in Fig. 7.16(b). The sinusoid superimposed on the transformer symbol indicates that the transformer is ideal, and is part of the averaged small-signal ac model. So the effective dc transformer property of CCM dc-dc converters also influences small-signal ac variations in the converter signals.

The equivalent circuit of Fig. 7.16(b) can now be solved using techniques of conventional linear circuit analysis, to find the converter transfer functions, input and output impedances, etc. This is done in detail in the next chapter. Also, the model can be refined by inclusion of losses and other nonidealities—an example is given in Section 7.2.9.

7.2.7 Discussion of the Perturbation and Linearization Step

In the perturbation and linearization step, it is assumed that an averaged voltage or current consists of a constant (dc) component and a small-signal ac variation around the dc component. In Section 7.2.5, the

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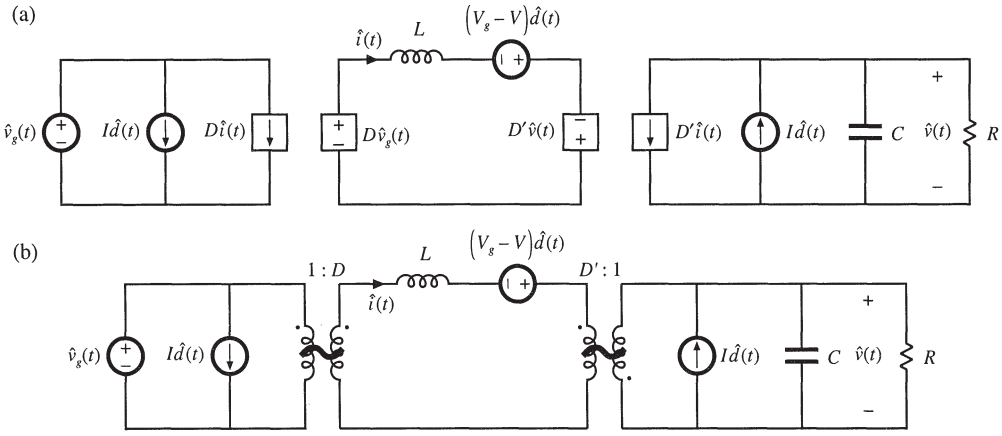


Fig. 7.16 Buck-boost converter small-signal ac equivalent circuit: (a) the circuits of Figs. 7.13 to 7.15, collected together; (b) combination of dependent sources into effective ideal transformer, leading to the final model.

linearization step was completed by neglecting nonlinear terms that correspond to products of the small-signal ac variations. In general, the linearization step amounts to taking the Taylor expansion of a nonlinear relation and retaining only the constant and linear terms. For example, the large-signal averaged equation for the inductor current in Eq. (7.28) can be written as:

$$L\frac{d\langle i(t)\rangle_{T_s}}{dt} = d(t)\langle v_g(t)\rangle_{T_s} + d'(t)\langle v(t)\rangle_{T_s} = f_1\left(\langle v_g(t)\rangle_{T_s}, \langle v(t)\rangle_{T_s}, d(t)\right) \tag{7.44}$$

Let us expand this expression in a three-dimensional Taylor series, about the quiescent operating point (V_g, V, D):

$$\begin{aligned} L\left(\frac{dI}{dt} + \frac{d\hat{i}(t)}{dt}\right) = {} & f_1\left(V_g, V, D\right) + \hat{v}_g(t)\left.\frac{\partial f_1\left(v_g, V, D\right)}{\partial v_g}\right|_{v_g = V_g} \\ & + \hat{v}(t)\left.\frac{\partial f_1\left(V_g, v, D\right)}{\partial v}\right|_{v = V} + \hat{d}(t)\left.\frac{\partial f_1\left(V_g, V, d\right)}{\partial d}\right|_{d = D} \\ & + \text{higher-order nonlinear terms} \end{aligned} \tag{7.45}$$

For simplicity of notation, the angle brackets denoting average values are dropped in the above equation. The derivative of I is zero, since I is by definition a dc (constant) term. Equating the dc terms on both sides of Eq. (7.45) gives:

$$0 = f_1\left(V_g, V, D\right) \tag{7.46}$$

which is the volt-second balance relationship for the inductor. The coefficients with the linear terms on the right-hand side of Eq. (7.45) are found as follows:

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$$\left.\frac{\partial f_1\left(v_g, V, D\right)}{\partial v_g}\right|_{v_g = V_g} = D \tag{7.47}$$

$$\left.\frac{\partial f_1\left(V_g, v, D\right)}{\partial v}\right|_{v = V} = D' \tag{7.48}$$

$$\left.\frac{\partial f_1\left(V_g, V, d\right)}{\partial d}\right|_{d = D} = V_g - V \tag{7.49}$$

Using (7.47), (7.48) and (7.49), neglecting higher-order nonlinear terms, and equating the linear ac terms on both sides of Eq. (7.45) gives:

$$L\frac{d\hat{i}(t)}{dt} = D\hat{v}_g(t) + D'\hat{v}(t) + \left(V_g - V\right)\hat{d}(t) \tag{7.50}$$

which is identical to Eq. (7.36) derived in Section 7.2.5. In conclusion, the linearization step can always be accomplished using the Taylor expansion.

7.2.8 Results for Several Basic Converters

The equivalent circuit models for the buck, boost, and buck-boost converters operating in the continuous conduction mode are summarized in Fig. 7.17. The buck and boost converter models contain ideal transformers having turns ratios equal to the converter conversion ratio. The buck-boost converter contains ideal transformers having buck and boost conversion ratios; this is consistent with the derivation of Section 6.1.2 of the buck-boost converter as a cascade connection of buck and boost converters. These models can be solved to find the converter transfer functions, input and output impedances, inductor current variations, etc. By insertion of appropriate turns ratios, the equivalent circuits of Fig. 7.17 can be adapted to model the transformer-isolated versions of the buck, boost, and buck-boost converters, including the forward, flyback, and other converters.

7.2.9 Example: A Nonideal Flyback Converter

To illustrate that the techniques of the previous section are useful for modeling a variety of converter phenomena, let us next derive a small-signal ac equivalent circuit of a converter containing transformer isolation and resistive losses. An isolated flyback converter is illustrated in Fig. 7.18. The flyback transformer has magnetizing inductance L, referred to the primary winding, and turns ratio $1{:}n$. MOSFET Q_1 has on-resistance R_{on}. Other loss elements, as well as the transformer leakage inductances and the switching losses, are negligible. The ac modeling of this converter begins in a manner similar to the dc converter analysis of Section 6.3.4. The flyback transformer is replaced by an equivalent circuit consisting of the magnetizing inductance L in parallel with an ideal transformer, as illustrated in Fig. 7.19(a).

During the first subinterval, when MOSFET Q_1 conducts, diode D_1 is off. The circuit then

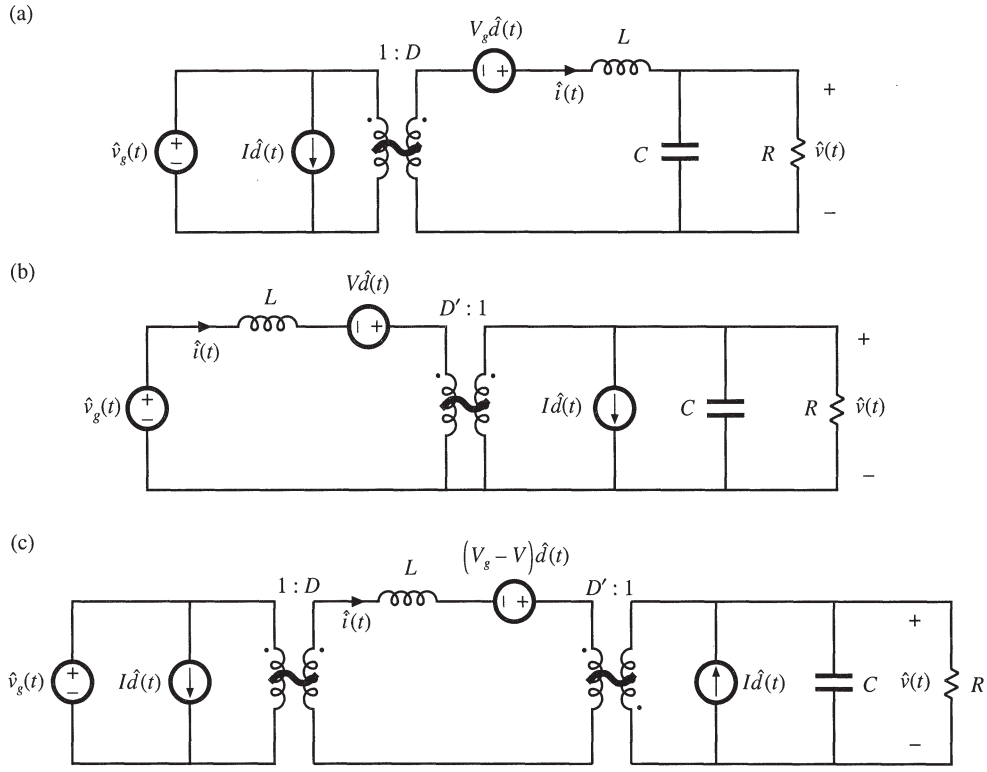


Fig. 7.17 Averaged small-signal ac models for several basic converters operating in continuous conduction mode: (a) buck, (b) boost, (c) buck-boost.

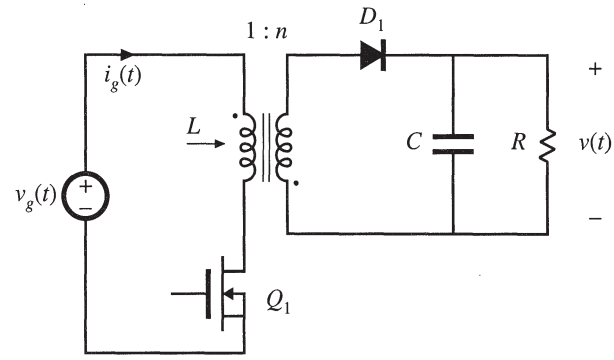


Fig. 7.18 Flyback converter example.

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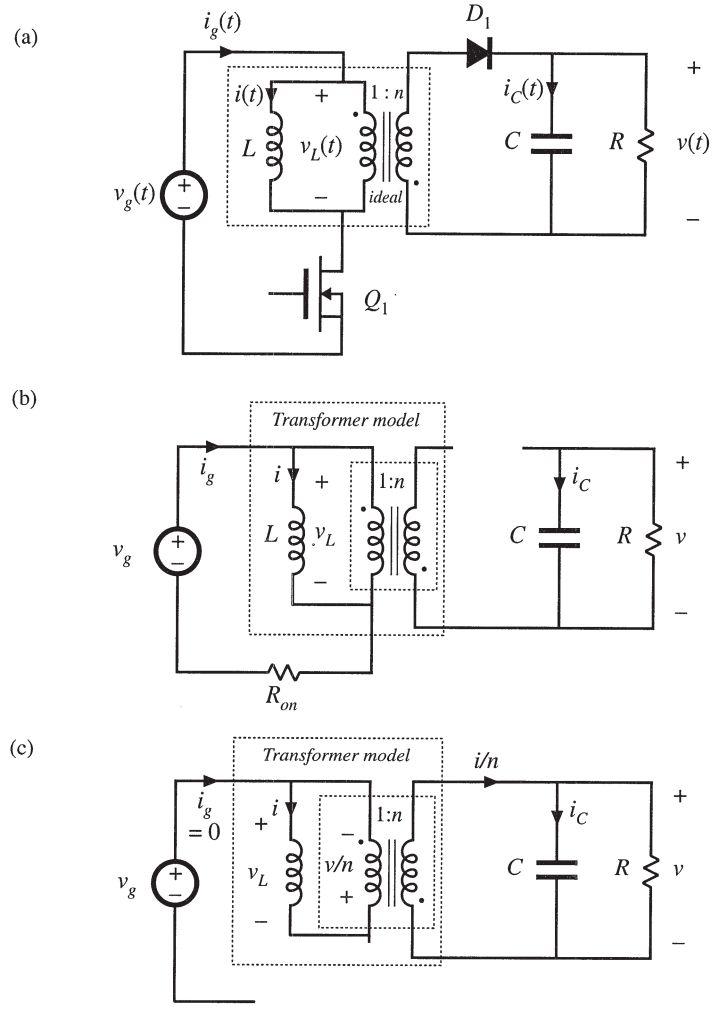


Fig. 7.19 Flyback converter example: (a) incorporation of transformer equivalent circuit, (b) circuit during subinterval 1, (c) circuit during subinterval 2.

reduces to Fig. 7.19(b). The inductor voltage $v_L(t)$, capacitor current $i_C(t)$, and converter input current $i_g(t)$ are:

$$\begin{aligned} v_L(t) &= v_g(t) - i(t)R_{on} \\ i_C(t) &= -\frac{v(t)}{R} \\ i_g(t) &= i(t) \end{aligned} \tag{7.51}$$

We next make the small ripple approximation, replacing the voltages and currents with their average val-

ues as defined by Eq. (7.3), to obtain

$$\begin{aligned} v_L(t) &= \langle v_g(t) \rangle_{T_s} - \langle i(t) \rangle_{T_s} R_{on} \\ i_C(t) &= -\frac{\langle v(t) \rangle_{T_s}}{R} \\ i_g(t) &= \langle i(t) \rangle_{T_s} \end{aligned} \tag{7.52}$$

During the second subinterval, MOSFET Q_1 is off, diode D_1 conducts, and the circuit of Fig. 7.19(c) is obtained. Analysis of this circuit shows that the inductor voltage, capacitor current, and input current are given by

$$\begin{aligned} v_L(t) &= -\frac{v(t)}{n} \\ i_C(t) &= \frac{i(t)}{n} - \frac{v(t)}{R} \\ i_g(t) &= 0 \end{aligned} \tag{7.53}$$

The small-ripple approximation leads to

$$\begin{aligned} v_L(t) &= -\frac{\langle v(t) \rangle_{T_s}}{n} \\ i_C(t) &= \frac{\langle i(t) \rangle_{T_s}}{n} - \frac{\langle v(t) \rangle_{T_s}}{R} \\ i_g(t) &= 0 \end{aligned} \tag{7.54}$$

The inductor voltage and current waveforms are sketched in Fig. 7.20. The average inductor voltage can now be found by averaging the waveform of Fig. 7.20(a) over one switching period. The result is

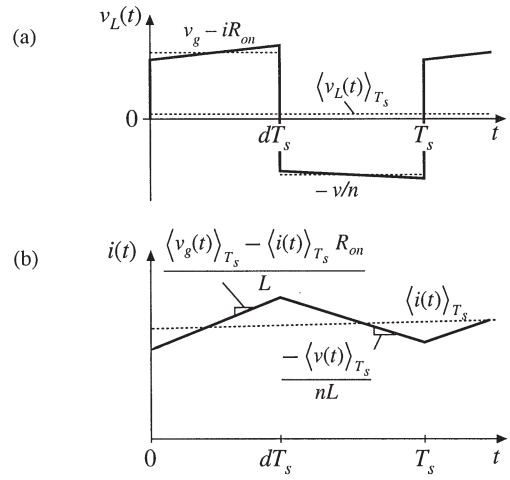


Fig. 7.20 Inductor waveforms for the flyback example: (a) inductor voltage, (b) inductor current.

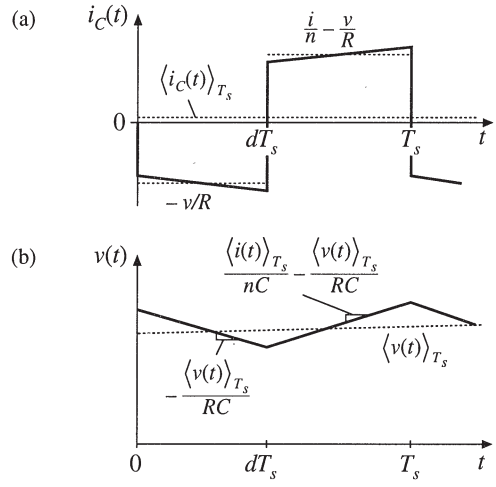


Fig. 7.21 Capacitor waveforms for the flyback example: (a) capacitor current, (b) capacitor voltage.

$$\langle v_L(t) \rangle_{T_s} = d(t) \left(\langle v_g(t) \rangle_{T_s} - \langle i(t) \rangle_{T_s} R_{on} \right) + d'(t) \left(\frac{-\langle v(t) \rangle_{T_s}}{n} \right) \tag{7.55}$$

By inserting this result into Eq. (7.20), we obtain the averaged inductor equation,

$$L \frac{d\langle i(t) \rangle_{T_s}}{dt} = d(t) \langle v_g(t) \rangle_{T_s} - d(t) \langle i(t) \rangle_{T_s} R_{on} - d'(t) \frac{\langle v(t) \rangle_{T_s}}{n} \tag{7.56}$$

The capacitor waveforms are constructed in Fig. 7.21. The average capacitor current is

$$\langle i_C(t) \rangle_{T_s} = d(t) \left(\frac{-\langle v(t) \rangle_{T_s}}{R} \right) + d'(t) \left(\frac{\langle i(t) \rangle_{T_s}}{n} - \frac{\langle v(t) \rangle_{T_s}}{R} \right) \tag{7.57}$$

This leads to the averaged capacitor equation

$$C \frac{d\langle v(t) \rangle_{T_s}}{dt} = d'(t) \frac{\langle i(t) \rangle_{T_s}}{n} - \frac{\langle v(t) \rangle_{T_s}}{R} \tag{7.58}$$

The converter input current $i_g(t)$ is sketched in Fig. 7.22. Its average is

$$\langle i_g(t) \rangle_{T_s} = d(t) \langle i(t) \rangle_{T_s} \tag{7.59}$$

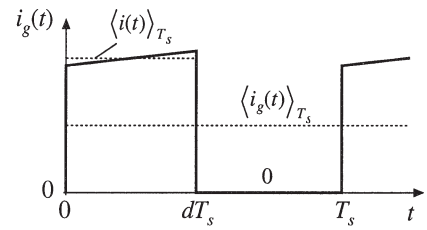


Fig. 7.22 Input source current waveform, flyback example.

The averaged converter equations (7.56), (7.58) and (7.59) are collected below:

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$$
\begin{aligned}
L\frac{d\langle i(t)\rangle_{T_s}}{dt} &= d(t)\langle v_g(t)\rangle_{T_s} - d(t)\langle i(t)\rangle_{T_s} R_{on} - d'(t)\frac{\langle v(t)\rangle_{T_s}}{n} \\
C\frac{d\langle v(t)\rangle_{T_s}}{dt} &= d'(t)\frac{\langle i(t)\rangle_{T_s}}{n} - \frac{\langle v(t)\rangle_{T_s}}{R} \\
\langle i_g(t)\rangle_{T_s} &= d(t)\langle i(t)\rangle_{T_s}
\end{aligned}
\tag{7.60}
$$

This is a nonlinear set of differential equations, and hence the next step is to perturb and linearize, to construct the converter small-signal ac equations. We assume that the converter input voltage $v_g(t)$ and duty cycle $d(t)$ can be expressed as quiescent values plus small ac variations, as follows:

$$
\begin{aligned}
\langle v_g(t)\rangle_{T_s} &= V_g + \hat{v}_g(t) \\
d(t) &= D + \hat{d}(t)
\end{aligned}
\tag{7.61}
$$

In response to these inputs, and after all transients have decayed, the average converter waveforms can also be expressed as quiescent values plus small ac variations:

$$
\begin{aligned}
\langle i(t)\rangle_{T_s} &= I + \hat{i}(t) \\
\langle v(t)\rangle_{T_s} &= V + \hat{v}(t) \\
\langle i_g(t)\rangle_{T_s} &= I_g + \hat{i}_g(t)
\end{aligned}
\tag{7.62}
$$

With these substitutions, the large-signal averaged inductor equation becomes

$$
L\frac{d\left(I + \hat{i}(t)\right)}{dt} = \left(D + \hat{d}(t)\right)\left(V_g + \hat{v}_g(t)\right) - \left(D' - \hat{d}(t)\right)\frac{\left(V + \hat{v}(t)\right)}{n} - \left(D + \hat{d}(t)\right)\left(I + \hat{i}(t)\right)R_{on}
\tag{7.63}
$$

Upon multiplying this expression out and collecting terms, we obtain

$$
\begin{aligned}
L\left(\frac{dI}{dt} + \frac{d\hat{i}(t)}{dt}\right) = &\underbrace{\left(DV_g - D'\frac{V}{n} - DR_{on}I\right)}_{\text{Dc terms}} + \underbrace{\left(D\hat{v}_g(t) - D'\frac{\hat{v}(t)}{n} + \left(V_g + \frac{V}{n} - IR_{on}\right)\hat{d}(t) - DR_{on}\hat{i}(t)\right)}_{1^{st}\text{ order ac terms (linear)}} \\
&+ \underbrace{\left(\hat{d}(t)\hat{v}_g(t) + \hat{d}(t)\frac{\hat{v}(t)}{n} - \hat{d}(t)\hat{i}(t)R_{on}\right)}_{2^{nd}\text{ order ac terms (nonlinear)}}
\end{aligned}
\tag{7.64}
$$

As usual, this equation contains three types of terms. The dc terms contain no time-varying quantities. The first-order ac terms are linear functions of the ac variations in the circuit, while the second-order ac terms are functions of the products of the ac variations. If the small-signal assumptions of Eq. (7.32) are satisfied, then the second-order terms are much smaller in magnitude that the first-order terms, and hence can be neglected. The dc terms must satisfy

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$$0 = DV_g - D'\frac{V}{n} - DR_{on}I \tag{7.65}$$

This result could also be derived by applying the principle of inductor volt-second balance to the steady-state inductor voltage waveform. The first-order ac terms must satisfy

$$L\frac{d\hat{i}(t)}{dt} = D\hat{v}_g(t) - D'\frac{\hat{v}(t)}{n} + \left(V_g + \frac{V}{n} - IR_{on}\right)\hat{d}(t) - DR_{on}\hat{i}(t) \tag{7.66}$$

This is the linearized equation that describes ac variations in the inductor current.

Upon substitution of Eqs. (7.61) and (7.62) into the averaged capacitor equation (7.60), one obtains

$$C\frac{d\left(V + \hat{v}(t)\right)}{dt} = \left(D' - \hat{d}(t)\right)\frac{\left(I + \hat{i}(t)\right)}{n} - \frac{\left(V + \hat{v}(t)\right)}{R} \tag{7.67}$$

By collecting terms, we obtain

$$C\left(\frac{dV}{dt} + \frac{d\hat{v}(t)}{dt}\right) = \underbrace{\left(\frac{D'I}{n} - \frac{V}{R}\right)}_{\text{Dc terms}} + \underbrace{\left(\frac{D'\hat{i}(t)}{n} - \frac{\hat{v}(t)}{R} - \frac{I\hat{d}(t)}{n}\right)}_{1^{st}\text{ order ac terms (linear)}} - \underbrace{\frac{\hat{d}(t)\hat{i}(t)}{n}}_{2^{nd}\text{ order ac term (nonlinear)}} \tag{7.68}$$

We neglect the second-order terms. The dc terms of Eq. (7.68) must satisfy

$$0 = \left(\frac{D'I}{n} - \frac{V}{R}\right) \tag{7.69}$$

This result could also be obtained by use of the principle of capacitor charge balance on the steady-state capacitor current waveform. The first-order ac terms of Eq. (7.68) lead to the small-signal ac capacitor equation

$$C\frac{d\hat{v}(t)}{dt} = \frac{D'\hat{i}(t)}{n} - \frac{\hat{v}(t)}{R} - \frac{I\hat{d}(t)}{n} \tag{7.70}$$

Substitution of Eqs. (7.61) and (7.62) into the averaged input current equation (7.60) leads to

$$I_g + \hat{i}_g(t) = \left(D + \hat{d}(t)\right)\left(I + \hat{i}(t)\right) \tag{7.71}$$

Upon collecting terms, we obtain

$$\underbrace{I_g}_{\text{Dc term}} + \underbrace{\hat{i}_g(t)}_{1^{st}\text{ order ac term}} = \underbrace{\left(DI\right)}_{\text{Dc term}} + \underbrace{\left(D\hat{i}(t) + I\hat{d}(t)\right)}_{1^{st}\text{ order ac terms (linear)}} + \underbrace{\hat{d}(t)\hat{i}(t)}_{2^{nd}\text{ order ac term (nonlinear)}} \tag{7.72}$$

The dc terms must satisfy

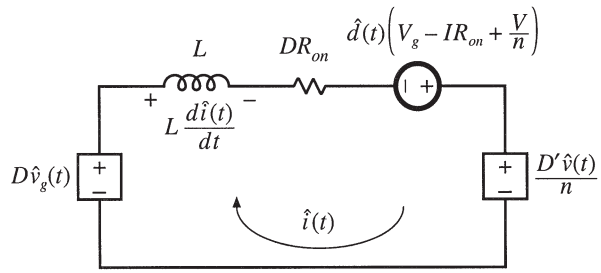


Fig. 7.23 Circuit equivalent to the small-signal ac inductor loop equation, Eq. (7.76) or (7.66).

$$I_g = DI \tag{7.73}$$

We neglect the second-order nonlinear terms of Eq. (7.72), leaving the following linearized ac equation:

$$\hat{i}_g(t) = D\hat{i}(t) + I\hat{d}(t) \tag{7.74}$$

This result models the low-frequency ac variations in the converter input current.

The equations of the quiescent values, Eqs. (7.65), (7.69), and (7.73) are collected below:

$$\begin{aligned} 0 &= DV_g - D'\frac{V}{n} - DR_{on}I \\ 0 &= \left(\frac{D'I}{n} - \frac{V}{R}\right) \\ I_g &= DI \end{aligned} \tag{7.75}$$

For given quiescent values of the input voltage V_g and duty cycle D, this system of equations can be evaluated to find the quiescent output voltage V, inductor current I, and input current dc component I_g. The results are then inserted into the small-signal ac equations.

The small-signal ac equations, Eqs. (7.66), (7.70), and (7.74), are summarized below:

$$\begin{aligned} L\frac{d\hat{i}(t)}{dt} &= D\hat{v}_g(t) - D'\frac{\hat{v}(t)}{n} + \left(V_g + \frac{V}{n} - IR_{on}\right)\hat{d}(t) - DR_{on}\hat{i}(t) \\ C\frac{d\hat{v}(t)}{dt} &= \frac{D'\hat{i}(t)}{n} - \frac{\hat{v}(t)}{R} - \frac{I\hat{d}(t)}{n} \\ \hat{i}_g(t) &= D\hat{i}(t) + I\hat{d}(t) \end{aligned} \tag{7.76}$$

The final step is to construct an equivalent circuit that corresponds to these equations.

The inductor equation was derived by first writing loop equations, to find the applied inductor voltage during each subinterval. These equations were then averaged, perturbed, and linearized, to obtain Eq. (7.66). So this equation describes the small-signal ac voltages around a loop containing the inductor. The loop current is the ac inductor current $\hat{i}(t)$. The quantity $Ld\hat{i}(t)/dt$ is the low-frequency ac voltage across the inductor. The four terms on the right-hand side of the equation are the voltages across the four other elements in the loop. The terms $D\hat{v}_g(t)$ and $-D'\hat{v}(t)/n$ are dependent on voltages elsewhere in the converter, and hence are represented as dependent sources in Fig. 7.23. The third term is driven by the duty cycle variations $\hat{d}(t)$ and hence is represented as an independent source. The fourth term, $-DR_{on}\hat{i}(t)$, is a voltage that is proportional to the loop current $\hat{i}(t)$. Hence this term obeys Ohm's law, with effective resistance DR_{on} as shown in the figure. So the influence of the MOSFET on-resistance on the converter

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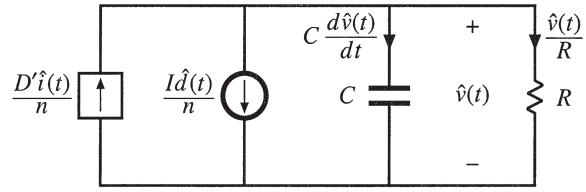


Fig. 7.24 Circuit equivalent to the small-signal ac capacitor node equation, Eq. (7.76) or (7.70).

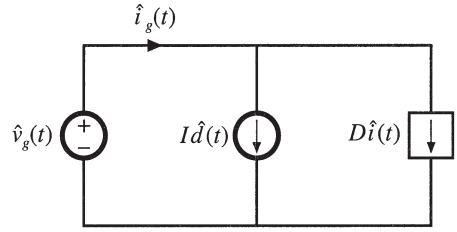


Fig. 7.25 Circuit equivalent to the small-signal ac input source current equation, Eq. (7.76) or (7.74).

small-signal transfer functions is modeled by an effective resistance of value DR_{on}.

Small-signal capacitor equation (7.70) leads to the equivalent circuit of Fig. 7.24. The equation constitutes a node equation of the equivalent circuit model. It states that the capacitor current $Cd\hat{v}(t)/dt$ is equal to three other currents. The current $D'\hat{i}(t)/n$ depends on a current elsewhere in the model, and hence is represented by a dependent current source. The term $-\hat{v}(t)/R$ is the ac component of the load current, which we model with a load resistance R connected in parallel with the capacitor. The last term is driven by the duty cycle variations $\hat{d}(t)$, and is modeled by an independent source.

The input port equation, Eq. (7.74), also constitutes a node equation. It describes the small-signal ac current $\hat{i}_g(t)$, drawn by the converter out of the input voltage source $\hat{v}_g(t)$. There are two other terms in the equation. The term $D\hat{i}(t)$ is dependent on the inductor current ac variation $\hat{i}(t)$, and is represented with a dependent source. The term $I\hat{d}(t)$ is driven by the control variations, and is modeled by an independent source. The equivalent circuit for the input port is illustrated in Fig. 7.25.

The circuits of Figs. 7.23, 7.24, and 7.25 are combined in Fig. 7.26. The dependent sources can be replaced by ideal transformers, leading to the equivalent circuit of Fig. 7.27. This is the desired result: an equivalent circuit that models the low-frequency small-signal variations in the converter waveforms. It can now be solved, using conventional linear circuit analysis techniques, to find the converter transfer functions, output impedance, and other ac quantities of interest.

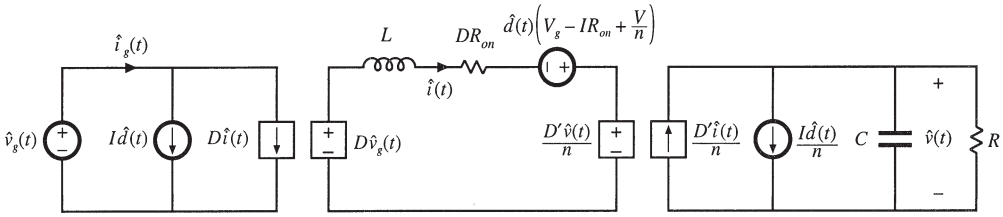


Fig. 7.26 The equivalent circuits of Figs. 7.23 to 7.25, collected together.

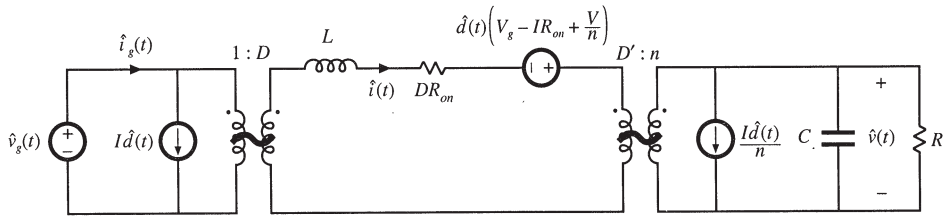


Fig. 7.27 Small-signal ac equivalent circuit model of the flyback converter.

7.3 STATE-SPACE AVERAGING

A number of ac converter modeling techniques have appeared in the literature, including the current-injected approach, circuit averaging, and the state-space averaging method. Although the proponents of a given method may prefer to express the end result in a specific form, the end results of nearly all methods are equivalent. And everybody will agree that averaging and small-signal linearization are the key steps in modeling PWM converters.

The state-space averaging approach [1, 2] is described in this section. The state-space description of dynamical systems is a mainstay of modern control theory; the state-space averaging method makes use of this description to derive the small-signal averaged equations of PWM switching converters. The state-space averaging method is otherwise identical to the procedure derived in Section 7.2. Indeed, the procedure of Section 7.2 amounts to state-space averaging, but without the formality of writing the equations in matrix form. A benefit of the state-space averaging procedure is the generality of its result: a small-signal averaged model can always be obtained, provided that the state equations of the original converter can be written.

Section 7.3.1 summarizes how to write the state equations of a network. The basic results of state-space averaging are described in Section 7.3.2, and a short derivation is given in Section 7.3.3. Section 7.3.4 contains an example, in which the state-space averaging method is used to derive the quiescent dc and small-signal ac equations of a buck-boost converter.

7.3.1 The State Equations of a Network

The state-space description is a canonical form for writing the differential equations that describe a system. For a linear network, the derivatives of the *state variables* are expressed as linear combinations of the system independent inputs and the state variables themselves. The physical state variables of a system are usually associated with the storage of energy, and for a typical converter circuit, the physical state variables are the independent inductor currents and capacitor voltages. Other typical state variables include the position and velocity of a motor shaft. At a given point in time, the values of the state variables depend on the previous history of the system, rather than on the present values of the system inputs. To solve the differential equations of the system, the initial values of the state variables must be specified. So if we know the *state* of a system, that is, the values of all of the state variables, at a given time t_0, and if we additionally know the system inputs, then we can in principle solve the system state equations to find the system waveforms at any future time.

The state equations of a system can be written in the compact matrix form of Eq. (7.77):

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$$\mathbf{K}\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t)$$
$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{E}\mathbf{u}(t) \tag{7.77}$$

Here, the state vector $\mathbf{x}(t)$ is a vector containing all of the state variables, that is, the inductor currents, capacitor voltages, etc. The input vector $\mathbf{u}(t)$ contains the independent inputs to the system, such as the input voltage source $v_g(t)$. The derivative of the state vector is a vector whose elements are equal to the derivatives of the corresponding elements of the state vector:

$$\mathbf{x}(t) = \begin{bmatrix} x_1(t) \\ x_2(t) \\ \vdots \end{bmatrix}, \qquad \frac{d\mathbf{x}(t)}{dt} = \begin{bmatrix} \frac{dx_1(t)}{dt} \\ \frac{dx_2(t)}{dt} \\ \vdots \end{bmatrix} \tag{7.78}$$

In the standard form of Eq. (7.77), $\mathbf{K}$ is a matrix containing the values of capacitance, inductance, and mutual inductance (if any), such that $\mathbf{K}d\mathbf{x}(t)/dt$ is a vector containing the inductor winding voltages and capacitor currents. In other physical systems, $\mathbf{K}$ may contain other quantities such as moment of inertia or mass. Equation (7.77) states that the inductor voltages and capacitor currents of the system can be expressed as linear combinations of the state variables and the independent inputs. The matrices $\mathbf{A}$ and $\mathbf{B}$ contain constants of proportionality.

It may also be desired to compute other circuit waveforms that do not coincide with the elements of the state vector $\mathbf{x}(t)$ or the input vector $\mathbf{u}(t)$. These other signals are, in general, dependent waveforms that can be expressed as linear combinations of the elements of the state vector and input vector. The vector $\mathbf{y}(t)$ is usually called the *output vector*. We are free to place any dependent signal in this vector, regardless of whether the signal is actually a physical output. The converter input current $i_g(t)$ is often chosen to be an element of $\mathbf{y}(t)$. In the state equations (7.77), the elements of $\mathbf{y}(t)$ are expressed as a linear combination of the elements of the $\mathbf{x}(t)$ and $\mathbf{u}(t)$ vectors. The matrices $\mathbf{C}$ and $\mathbf{E}$ contain constants of proportionality.

As an example, let us write the state equations of the circuit of Fig. 7.28. This circuit contains two capacitors and an inductor, and hence the physical state variables are the independent capacitor voltages $v_1(t)$ and $v_2(t)$, as well as the inductor current $i(t)$. So we can define the state vector as

$$\mathbf{x}(t) = \begin{bmatrix} v_1(t) \\ v_2(t) \\ i(t) \end{bmatrix} \tag{7.79}$$

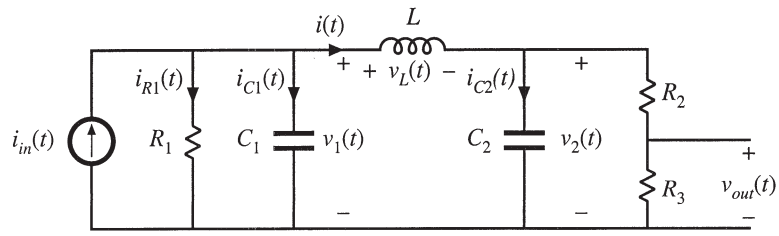


Fig. 7.28 Circuit example.

Since there are no coupled inductors, the matrix **K** is diagonal, and simply contains the values of capacitance and inductance:

$$\mathbf{K} = \begin{bmatrix} C_1 & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & L \end{bmatrix} \tag{7.80}$$

The circuit has one independent input, the current source $i_{in}(t)$. Hence we should define the input vector as

$$\mathbf{u}(t) = \begin{bmatrix} i_{in}(t) \end{bmatrix} \tag{7.81}$$

We are free to place any dependent signal in vector $\mathbf{y}(t)$. Suppose that we are interested in also computing the voltage $v_{out}(t)$ and the current $i_{R1}(t)$. We can therefore define $\mathbf{y}(t)$ as

$$\mathbf{y}(t) = \begin{bmatrix} v_{out}(t) \\ i_{R1}(t) \end{bmatrix} \tag{7.82}$$

To write the state equations in the canonical form of Eq. (7.77), we need to express the inductor voltages and capacitor currents as linear combinations of the elements of $\mathbf{x}(t)$ and $\mathbf{u}(t)$, that is, as linear combinations of $v_1(t)$, $v_2(t)$, $i(t)$, and $i_{in}(t)$.

The capacitor current $i_{C1}(t)$ is given by the node equation

$$i_{C1}(t) = C_1 \frac{dv_1(t)}{dt} = i_{in}(t) - \frac{v_1(t)}{R_1} - i(t) \tag{7.83}$$

This equation will become the top row of the matrix equation (7.77). The capacitor current $i_{C2}(t)$ is given by the node equation,

$$i_{C2}(t) = C_2 \frac{dv_2(t)}{dt} = i(t) - \frac{v_2(t)}{R_2 + R_3} \tag{7.84}$$

Note that we have been careful to express this current as a linear combination of the elements of $\mathbf{x}(t)$ and $\mathbf{u}(t)$ alone. The inductor voltage is given by the loop equation,

$$v_L(t) = L \frac{di(t)}{dt} = v_1(t) - v_2(t) \tag{7.85}$$

Equations (7.83) to (7.85) can be written in the following matrix form:

$$\underbrace{\begin{bmatrix} C_1 & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & L \end{bmatrix}}_{\mathbf{K}} \underbrace{\begin{bmatrix} \frac{dv_1(t)}{dt} \\ \frac{dv_2(t)}{dt} \\ \frac{di(t)}{dt} \end{bmatrix}}_{\frac{d\mathbf{x}(t)}{dt}} = \underbrace{\begin{bmatrix} -\frac{1}{R_1} & 0 & -1 \\ 0 & -\frac{1}{R_2 + R_3} & 1 \\ 1 & -1 & 0 \end{bmatrix}}_{\mathbf{A}} \underbrace{\begin{bmatrix} v_1(t) \\ v_2(t) \\ i(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{B}} \underbrace{\begin{bmatrix} i_{in}(t) \end{bmatrix}}_{\mathbf{u}(t)} \tag{7.86}$$

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Matrices **A** and **B** are now known.

It is also necessary to express the elements of $\mathbf{y}(t)$ as linear combinations of the elements of $\mathbf{x}(t)$ and $\mathbf{u}(t)$. By solution of the circuit of Fig. 7.28, $v_{out}(t)$ can be written in terms of $v_2(t)$ as

$$v_{out}(t) = v_2(t) \frac{R_3}{R_2 + R_3} \tag{7.87}$$

Also, $i_{R1}(t)$ can be expressed in terms of $v_1(t)$ as

$$i_{R1}(t) = \frac{v_1(t)}{R_1} \tag{7.88}$$

By collecting Eqs. (7.87) and (7.88) into the standard matrix form of Eq. (7.77), we obtain

$$\underbrace{\begin{bmatrix} v_{out}(t) \\ i_{R1}(t) \end{bmatrix}}_{\mathbf{y}(t)} = \underbrace{\begin{bmatrix} 0 & \frac{R_3}{R_2 + R_3} & 0 \\ \frac{1}{R_1} & 0 & 0 \end{bmatrix}}_{\mathbf{C}} \underbrace{\begin{bmatrix} v_1(t) \\ v_2(t) \\ i(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 0 \\ 0 \end{bmatrix}}_{\mathbf{E}} \underbrace{\left[i_{in}(t) \right]}_{\mathbf{u}(t)} \tag{7.89}$$

We can now identify the matrices **C** and **E** as shown above.

It should be recognized that, starting in Chapter 2, we have always begun the analysis of converters by writing their state equations. We are now simply writing these equations in matrix form.

7.3.2 The Basic State-Space Averaged Model

Consider now that we are given a PWM converter, operating in the continuous conduction mode. The converter circuit contains independent states that form the state vector $\mathbf{x}(t)$, and the converter is driven by independent sources that form the input vector $\mathbf{u}(t)$. During the first subinterval, when the switches are in position 1, the converter reduces to a linear circuit that can be described by the following state equations:

$$\begin{aligned} \mathbf{K} \frac{d\mathbf{x}(t)}{dt} &= \mathbf{A}_1 \mathbf{x}(t) + \mathbf{B}_1 \mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}_1 \mathbf{x}(t) + \mathbf{E}_1 \mathbf{u}(t) \end{aligned} \tag{7.90}$$

During the second subinterval, with the switches in position 2, the converter reduces to another linear circuit whose state equations are

$$\begin{aligned} \mathbf{K} \frac{d\mathbf{x}(t)}{dt} &= \mathbf{A}_2 \mathbf{x}(t) + \mathbf{B}_2 \mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}_2 \mathbf{x}(t) + \mathbf{E}_2 \mathbf{u}(t) \end{aligned} \tag{7.91}$$

During the two subintervals, the circuit elements are connected differently; therefore, the respective state equation matrices $\mathbf{A}_1$, $\mathbf{B}_1$, $\mathbf{C}_1$, $\mathbf{E}_1$ and $\mathbf{A}_2$, $\mathbf{B}_2$, $\mathbf{C}_2$, $\mathbf{E}_2$ may also differ. Given these state equations, the result of state-space averaging is the state equations of the equilibrium and small-signal ac models.

Provided that the natural frequencies of the converter, as well as the frequencies of variations of the converter inputs, are much slower than the switching frequency, then the state-space averaged model

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that describes the converter in equilibrium is

$$\begin{aligned} \mathbf{0} &= \mathbf{AX} + \mathbf{BU} \\ \mathbf{Y} &= \mathbf{CX} + \mathbf{EU} \end{aligned} \tag{7.92}$$

where the averaged matrices are

$$\begin{aligned} \mathbf{A} &= D\mathbf{A}_1 + D'\mathbf{A}_2 \\ \mathbf{B} &= D\mathbf{B}_1 + D'\mathbf{B}_2 \\ \mathbf{C} &= D\mathbf{C}_1 + D'\mathbf{C}_2 \\ \mathbf{E} &= D\mathbf{E}_1 + D'\mathbf{E}_2 \end{aligned} \tag{7.93}$$

The equilibrium dc components are

$$\begin{aligned} \mathbf{X} &= \text{equilibrium (dc) state vector} \\ \mathbf{U} &= \text{equilibrium (dc) input vector} \\ \mathbf{Y} &= \text{equilibrium (dc) output vector} \\ D &= \text{equilibrium (dc) duty cycle} \end{aligned} \tag{7.94}$$

Quantities defined in Eq. (7.94) represent the equilibrium values of the averaged vectors. Equation (7.92) can be solved to find the equilibrium state and output vectors:

$$\begin{aligned} \mathbf{X} &= -\mathbf{A}^{-1}\mathbf{BU} \\ \mathbf{Y} &= \left(-\mathbf{CA}^{-1}\mathbf{B} + \mathbf{E}\right)\mathbf{U} \end{aligned} \tag{7.95}$$

The state equations of the small-signal ac model are

$$\begin{aligned} \mathbf{K}\frac{d\hat{\mathbf{x}}(t)}{dt} &= \mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{B}\hat{\mathbf{u}}(t) + \left\{\left(\mathbf{A}_1 - \mathbf{A}_2\right)\mathbf{X} + \left(\mathbf{B}_1 - \mathbf{B}_2\right)\mathbf{U}\right\}\hat{d}(t) \\ \hat{\mathbf{y}}(t) &= \mathbf{C}\hat{\mathbf{x}}(t) + \mathbf{E}\hat{\mathbf{u}}(t) + \left\{\left(\mathbf{C}_1 - \mathbf{C}_2\right)\mathbf{X} + \left(\mathbf{E}_1 - \mathbf{E}_2\right)\mathbf{U}\right\}\hat{d}(t) \end{aligned} \tag{7.96}$$

The quantities $\hat{\mathbf{x}}(t)$, $\hat{\mathbf{u}}(t)$, $\hat{\mathbf{y}}(t)$, and $\hat{d}(t)$ in Eq. (7.96) are small ac variations about the equilibrium solution, or quiescent operating point, defined by Eqs. (7.92) to (7.95).

So if we can write the converter state equations, Eqs. (7.90) and (7.91), then we can always find the averaged dc and small-signal ac models, by evaluation of Eqs. (7.92) to (7.96).

7.3.3 Discussion of the State-Space Averaging Result

As in Sections 7.1 and 7.2, the low-frequency components of the inductor currents and capacitor voltages are modeled by averaging over an interval of length T_s. Hence, we can define the average of the state vector $\mathbf{x}(t)$ as

$$\left\langle \mathbf{x}(t) \right\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} \mathbf{x}(\tau)\,d\tau \tag{7.97}$$

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The low-frequency components of the input and output vectors are modeled in a similar manner. By averaging the inductor voltages and capacitor currents, one then obtains the following low-frequency state equation:

$$\mathbf{K}\frac{d\langle \mathbf{x}(t)\rangle_{T_s}}{dt} = \Big(d(t)\,\mathbf{A}_1 + d'(t)\,\mathbf{A}_2\Big)\langle \mathbf{x}(t)\rangle_{T_s} + \Big(d(t)\,\mathbf{B}_1 + d'(t)\,\mathbf{B}_2\Big)\langle \mathbf{u}(t)\rangle_{T_s} \tag{7.98}$$

This result is equivalent to Eq. (7.2).

For example, let us consider how the elements of the state vector $\mathbf{x}(t)$ change over one switching period. During the first subinterval, with the switches in position 1, the converter state equations are given by Eq. (7.90). Therefore, the elements of $\mathbf{x}(t)$ change with the slopes $\mathbf{K}^{-1}(\mathbf{A}_1\mathbf{x}(t) + \mathbf{B}_1\mathbf{u}(t))$. If we make the small ripple approximation, that $\mathbf{x}(t)$ and $\mathbf{u}(t)$ do not change much over one switching period, then the slopes are essentially constant and are approximately equal to

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{K}^{-1}\Big(\mathbf{A}_1\langle \mathbf{x}(t)\rangle_{T_s} + \mathbf{B}_1\langle \mathbf{u}(t)\rangle_{T_s}\Big) \tag{7.99}$$

This assumption coincides with the requirements for small switching ripple in all elements of $\mathbf{x}(t)$ and that variations in $\mathbf{u}(t)$ be slow compared to the switching frequency. If we assume that the state vector is initially equal to $\mathbf{x}(0)$, then we can write

$$\underbrace{\mathbf{x}(dT_s)}_{\substack{\text{final}\\\text{value}}} = \underbrace{\mathbf{x}(0)}_{\substack{\text{initial}\\\text{value}}} + \underbrace{(dT_s)}_{\substack{\text{interval}\\\text{length}}}\ \underbrace{\mathbf{K}^{-1}\Big(\mathbf{A}_1\langle \mathbf{x}(t)\rangle_{T_s} + \mathbf{B}_1\langle \mathbf{u}(t)\rangle_{T_s}\Big)}_{\text{slope}} \tag{7.100}$$

Similar arguments apply during the second subinterval. With the switch in position 2, the state equations are given by Eq. (7.91). With the assumption of small ripple during this subinterval, the state vector now changes with slope

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{K}^{-1}\Big(\mathbf{A}_2\langle \mathbf{x}(t)\rangle_{T_s} + \mathbf{B}_2\langle \mathbf{u}(t)\rangle_{T_s}\Big) \tag{7.101}$$

The state vector at the end of the switching period is

$$\underbrace{\mathbf{x}(T_s)}_{\substack{\text{final}\\\text{value}}} = \underbrace{\mathbf{x}(dT_s)}_{\substack{\text{initial}\\\text{value}}} + \underbrace{(d'T_s)}_{\substack{\text{interval}\\\text{length}}}\ \underbrace{\mathbf{K}^{-1}\Big(\mathbf{A}_2\langle \mathbf{x}(t)\rangle_{T_s} + \mathbf{B}_2\langle \mathbf{u}(t)\rangle_{T_s}\Big)}_{\text{slope}} \tag{7.102}$$

Substitution of Eq. (7.100) into Eq. (7.102) allows us to determine $\mathbf{x}(T_s)$ in terms of $\mathbf{x}(0)$:

$$\mathbf{x}(T_s) = \mathbf{x}(0) + dT_s\mathbf{K}^{-1}\Big(\mathbf{A}_1\langle \mathbf{x}(t)\rangle_{T_s} + \mathbf{B}_1\langle \mathbf{u}(t)\rangle_{T_s}\Big) + d'T_s\mathbf{K}^{-1}\Big(\mathbf{A}_2\langle \mathbf{x}(t)\rangle_{T_s} + \mathbf{B}_2\langle \mathbf{u}(t)\rangle_{T_s}\Big) \tag{7.103}$$

Upon collecting terms, one obtains

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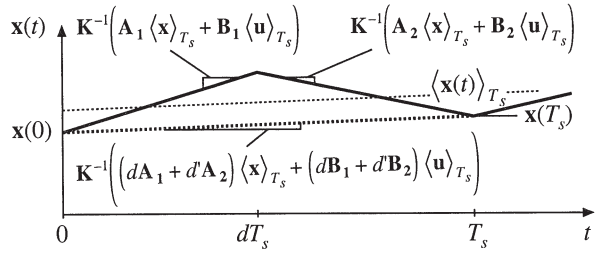


Fig. 7.29 How an element of the state vector, and its average, evolve over one switching period.

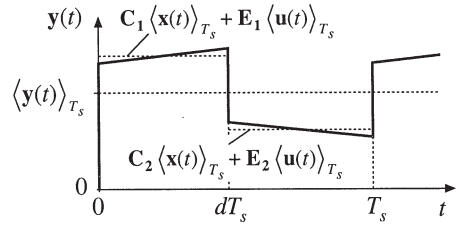


Fig. 7.30 Averaging an element of the output vector $\mathbf{y}(t)$.

$$\mathbf{x}(T_s) = \mathbf{x}(0) + T_s\mathbf{K}^{-1}\left(d(t)\mathbf{A}_1 + d'(t)\mathbf{A}_2\right)\langle\mathbf{x}(t)\rangle_{T_s} + T_s\mathbf{K}^{-1}\left(d(t)\mathbf{B}_1 + d'(t)\mathbf{B}_2\right)\langle\mathbf{u}(t)\rangle_{T_s} \tag{7.104}$$

Next, we approximate the derivative of $\langle\mathbf{x}(t)\rangle_{T_s}$ using the net change over one switching period:

$$\frac{d\langle\mathbf{x}(t)\rangle_{T_s}}{dt} \approx \frac{\mathbf{x}(T_s) - \mathbf{x}(0)}{T_s} \tag{7.105}$$

Substitution of Eq. (7.104) into (7.105) leads to

$$\mathbf{K}\frac{d\langle\mathbf{x}(t)\rangle_{T_s}}{dt} = \left(d(t)\,\mathbf{A}_1 + d'(t)\,\mathbf{A}_2\right)\langle\mathbf{x}(t)\rangle_{T_s} + \left(d(t)\,\mathbf{B}_1 + d'(t)\,\mathbf{B}_2\right)\langle\mathbf{u}(t)\rangle_{T_s} \tag{7.106}$$

which is identical to Eq. (7.99). This is the basic averaged model which describes the converter dynamics. It is nonlinear because the control input $d(t)$ is multiplied by $\langle\mathbf{x}(t)\rangle_{T_s}$ and $\langle\mathbf{u}(t)\rangle_{T_s}$. Variation of a typical element of $\mathbf{x}(t)$ and its average are illustrated in Fig. 7.29.

It is also desired to find the low-frequency components of the output vector $\mathbf{y}(t)$ by averaging. The vector $\mathbf{y}(t)$ is described by Eq. (7.90) for the first subinterval, and by Eq. (7.91) for the second subinterval. Hence, the elements of $\mathbf{y}(t)$ may be discontinuous at the switching transitions, as illustrated in Fig. 7.30. We can again remove the switching harmonics by averaging over one switching period; the

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result is

$$\langle \mathbf{y}(t) \rangle_{T_s} = d(t) \left(\mathbf{C}_1 \langle \mathbf{x}(t) \rangle_{T_s} + \mathbf{E}_1 \langle \mathbf{u}(t) \rangle_{T_s} \right) + d'(t) \left(\mathbf{C}_2 \langle \mathbf{x}(t) \rangle_{T_s} + \mathbf{E}_2 \langle \mathbf{u}(t) \rangle_{T_s} \right) \tag{7.107}$$

Rearrangement of terms yields

$$\langle \mathbf{y}(t) \rangle_{T_s} = \left(d(t)\, \mathbf{C}_1 + d'(t)\, \mathbf{C}_2 \right) \langle \mathbf{x}(t) \rangle_{T_s} + \left(d(t)\, \mathbf{E}_1 + d'(t)\, \mathbf{E}_2 \right) \langle \mathbf{u}(t) \rangle_{T_s} \tag{7.108}$$

This is again a nonlinear equation.

The averaged state equations, (7.106) and (7.108), are collected below:

$$\begin{aligned} \mathbf{K} \frac{d \langle \mathbf{x}(t) \rangle_{T_s}}{dt} &= \left(d(t)\, \mathbf{A}_1 + d'(t)\, \mathbf{A}_2 \right) \langle \mathbf{x}(t) \rangle_{T_s} + \left(d(t)\, \mathbf{B}_1 + d'(t)\, \mathbf{B}_2 \right) \langle \mathbf{u}(t) \rangle_{T_s} \\ \langle \mathbf{y}(t) \rangle_{T_s} &= \left(d(t)\, \mathbf{C}_1 + d'(t)\, \mathbf{C}_2 \right) \langle \mathbf{x}(t) \rangle_{T_s} + \left(d(t)\, \mathbf{E}_1 + d'(t)\, \mathbf{E}_2 \right) \langle \mathbf{u}(t) \rangle_{T_s} \end{aligned} \tag{7.109}$$

The next step is the linearization of these equations about a quiescent operating point, to construct a small-signal ac model. When dc inputs $d(t) = D$ and $\mathbf{u}(t) = \mathbf{U}$ are applied, converter operates in equilibrium when the derivatives of all of the elements of $\langle \mathbf{x}(t) \rangle_{T_s}$ are zero. Hence, by setting the derivative of $\langle \mathbf{x}(t) \rangle_{T_s}$ to zero in Eq. (7.109), we can define the converter quiescent operating point as the solution of

$$\begin{aligned} \mathbf{0} &= \mathbf{AX} + \mathbf{BU} \\ \mathbf{Y} &= \mathbf{CX} + \mathbf{EU} \end{aligned} \tag{7.110}$$

where definitions (7.93) and (7.94) have been used. We now perturb and linearize the converter waveforms about this quiescent operating point:

$$\begin{aligned} \langle \mathbf{x}(t) \rangle_{T_s} &= \mathbf{X} + \hat{\mathbf{x}}(t) \\ \langle \mathbf{u}(t) \rangle_{T_s} &= \mathbf{U} + \hat{\mathbf{u}}(t) \\ \langle \mathbf{y}(t) \rangle_{T_s} &= \mathbf{Y} + \hat{\mathbf{y}}(t) \\ d(t) &= D + \hat{d}(t) \quad \Rightarrow \quad d'(t) = D' - \hat{d}(t) \end{aligned} \tag{7.111}$$

Here, $\hat{\mathbf{u}}(t)$ and $\hat{d}(t)$ are small ac variations in the input vector and duty ratio. The vectors $\hat{\mathbf{x}}(t)$ and $\hat{\mathbf{y}}(t)$ are the resulting small ac variations in the state and output vectors. We must assume that these ac variations are much smaller than the quiescent values. In other words,

$$\begin{aligned} \| \mathbf{U} \| &\gg \| \hat{\mathbf{u}}(t) \| \\ D &\gg | \hat{d}(t) | \\ \| \mathbf{X} \| &\gg \| \hat{\mathbf{x}}(t) \| \\ \| \mathbf{Y} \| &\gg \| \hat{\mathbf{y}}(t) \| \end{aligned} \tag{7.112}$$

Here, $\| \mathbf{x} \|$ denotes a norm of the vector $\mathbf{x}$.

Substitution of Eq. (7.111) into Eq. (7.109) yields

$$\mathbf{K}\frac{d\left(\mathbf{X}+\hat{\mathbf{x}}(t)\right)}{dt} = \left(\left(D+\hat{d}(t)\right)\mathbf{A}_1 + \left(D'-\hat{d}(t)\right)\mathbf{A}_2\right)\left(\mathbf{X}+\hat{\mathbf{x}}(t)\right) + \left(\left(D+\hat{d}(t)\right)\mathbf{B}_1 + \left(D'-\hat{d}(t)\right)\mathbf{B}_2\right)\left(\mathbf{U}+\hat{\mathbf{u}}(t)\right)$$

$$\left(\mathbf{Y}+\hat{\mathbf{y}}(t)\right) = \left(\left(D+\hat{d}(t)\right)\mathbf{C}_1 + \left(D'-\hat{d}(t)\right)\mathbf{C}_2\right)\left(\mathbf{X}+\hat{\mathbf{x}}(t)\right) + \left(\left(D+\hat{d}(t)\right)\mathbf{E}_1 + \left(D'-\hat{d}(t)\right)\mathbf{E}_2\right)\left(\mathbf{U}+\hat{\mathbf{u}}(t)\right) \tag{7.113}$$

The derivative $d\mathbf{X}/dt$ is zero. By collecting terms, one obtains

$$\underbrace{\mathbf{K}\frac{d\hat{\mathbf{x}}(t)}{dt}}_{\text{first-order ac}} = \underbrace{\left(\mathbf{AX}+\mathbf{BU}\right)}_{\text{dc terms}} + \underbrace{\mathbf{A}\hat{\mathbf{x}}(t)+\mathbf{B}\hat{\mathbf{u}}(t)+\left\{\left(\mathbf{A}_1-\mathbf{A}_2\right)\mathbf{X}+\left(\mathbf{B}_1-\mathbf{B}_2\right)\mathbf{U}\right\}\hat{d}(t)}_{\text{first-order ac terms}} + \underbrace{\left(\mathbf{A}_1-\mathbf{A}_2\right)\hat{\mathbf{x}}(t)\hat{d}(t)+\left(\mathbf{B}_1-\mathbf{B}_2\right)\hat{\mathbf{u}}(t)\hat{d}(t)}_{\text{second-order nonlinear terms}}$$

$$\underbrace{\left(\mathbf{Y}+\hat{\mathbf{y}}(t)\right)}_{\text{dc + 1}^{st}\text{ order ac}} = \underbrace{\left(\mathbf{CX}+\mathbf{EU}\right)}_{\text{dc terms}} + \underbrace{\mathbf{C}\hat{\mathbf{x}}(t)+\mathbf{E}\hat{\mathbf{u}}(t)+\left\{\left(\mathbf{C}_1-\mathbf{C}_2\right)\mathbf{X}+\left(\mathbf{E}_1-\mathbf{E}_2\right)\mathbf{U}\right\}\hat{d}(t)}_{\text{first-order ac terms}} + \underbrace{\left(\mathbf{C}_1-\mathbf{C}_2\right)\hat{\mathbf{x}}(t)\hat{d}(t)+\left(\mathbf{E}_1-\mathbf{E}_2\right)\hat{\mathbf{u}}(t)\hat{d}(t)}_{\text{second-order nonlinear terms}} \tag{7.114}$$

Since the dc terms satisfy Eq. (7.110), they drop out of Eq. (7.114). Also, if the small-signal assumption (7.112) is satisfied, then the second-order nonlinear terms of Eq. (7.114) are small in magnitude compared to the first-order ac terms. We can therefore neglect the nonlinear terms, to obtain the following linearized ac model:

$$\mathbf{K}\frac{d\hat{\mathbf{x}}(t)}{dt} = \mathbf{A}\hat{\mathbf{x}}(t)+\mathbf{B}\hat{\mathbf{u}}(t)+\left\{\left(\mathbf{A}_1-\mathbf{A}_2\right)\mathbf{X}+\left(\mathbf{B}_1-\mathbf{B}_2\right)\mathbf{U}\right\}\hat{d}(t)$$
$$\hat{\mathbf{y}}(t) = \mathbf{C}\hat{\mathbf{x}}(t)+\mathbf{E}\hat{\mathbf{u}}(t)+\left\{\left(\mathbf{C}_1-\mathbf{C}_2\right)\mathbf{X}+\left(\mathbf{E}_1-\mathbf{E}_2\right)\mathbf{U}\right\}\hat{d}(t) \tag{7.115}$$

This is the desired result, which coincides with Eq. (7.95).

7.3.4 Example: State-Space Averaging of a Nonideal Buck-Boost Converter

Let us apply the state-space averaging method to model the buck-boost converter of Fig. 7.31. We will model the conduction loss of MOSFET Q_1 by on-resistance R_{on}, and the forward voltage drop of diode

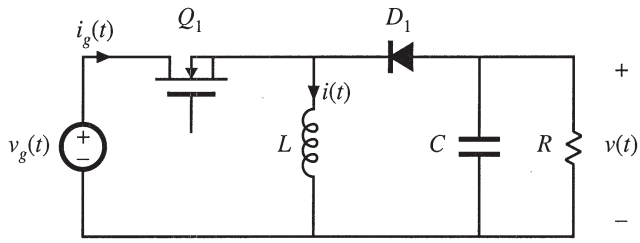


Fig. 7.31 Buck-boost converter example.

D_1 by an independent voltage source of value V_D. It is desired to obtain a complete equivalent circuit, which models both the input port and the output port of the converter.

The independent states of the converter are the inductor current $i(t)$ and the capacitor voltage $v(t)$. Therefore, we should define the state vector $\mathbf{x}(t)$ as

$$\mathbf{x}(t) = \begin{bmatrix} i(t) \\ v(t) \end{bmatrix} \tag{7.116}$$

The input voltage $v_g(t)$ is an independent source which should be placed in the input vector $\mathbf{u}(t)$. In addition, we have chosen to model the diode forward voltage drop with an independent voltage source of value V_D. So this voltage source should also be included in the input vector $\mathbf{u}(t)$. Therefore, let us define the input vector as

$$\mathbf{u}(t) = \begin{bmatrix} v_g(t) \\ V_D \end{bmatrix} \tag{7.117}$$

To model the converter input port, we need to find the converter input current $i_g(t)$. To calculate this dependent current, it should be included in the output vector $\mathbf{y}(t)$. Therefore, let us choose to define $\mathbf{y}(t)$ as

$$\mathbf{y}(t) = \begin{bmatrix} i_g(t) \end{bmatrix} \tag{7.118}$$

Note that it isn't necessary to include the output voltage $v(t)$ in the output vector $\mathbf{y}(t)$, since $v(t)$ is already included in the state vector $\mathbf{x}(t)$.

Next, let us write the state equations for each subinterval. When the switch is in position 1, the converter circuit of Fig. 7.32(a) is obtained. The inductor voltage, capacitor current, and converter input current are

$$\begin{aligned} L\frac{di(t)}{dt} &= v_g(t) - i(t)\,R_{on} \\ C\frac{dv(t)}{dt} &= -\frac{v(t)}{R} \\ i_g(t) &= i(t) \end{aligned} \tag{7.119}$$

These equations can be written in the following state-space form:

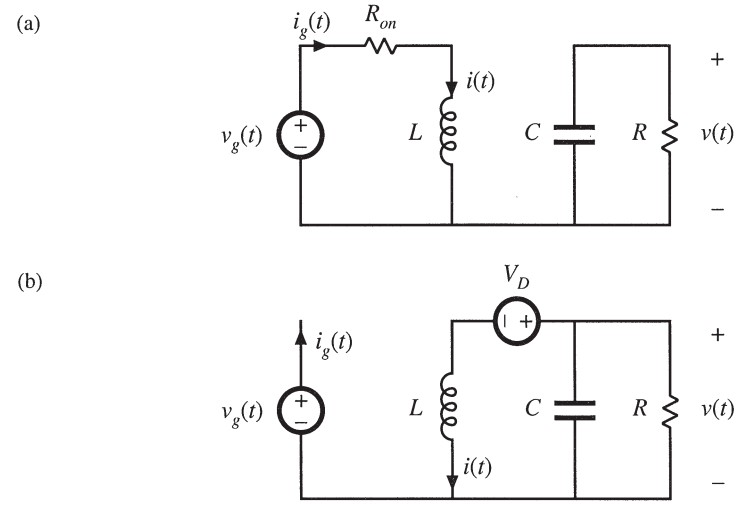


Fig. 7.32 Buck-boost converter circuit: (a) during subinterval 1, (b) during subinterval 2.

$$\underbrace{\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}}_{\mathbf{K}} \underbrace{\frac{d}{dt}\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\frac{d\mathbf{x}(t)}{dt}} = \underbrace{\begin{bmatrix} -R_{on} & 0 \\ 0 & -\frac{1}{R} \end{bmatrix}}_{\mathbf{A}_1} \underbrace{\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}}_{\mathbf{B}_1} \underbrace{\begin{bmatrix} v_g(t) \\ V_D \end{bmatrix}}_{\mathbf{u}(t)}$$

$$\underbrace{\begin{bmatrix} i_g(t) \end{bmatrix}}_{\mathbf{y}(t)} = \underbrace{\begin{bmatrix} 1 & 0 \end{bmatrix}}_{\mathbf{C}_1} \underbrace{\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 0 & 0 \end{bmatrix}}_{\mathbf{E}_1} \underbrace{\begin{bmatrix} v_g(t) \\ V_D \end{bmatrix}}_{\mathbf{u}(t)} \tag{7.120}$$

So we have identified the state equation matrices $\mathbf{A}_1$, $\mathbf{B}_1$, $\mathbf{C}_1$, and $\mathbf{E}_1$.

With the switch in position 2, the converter circuit of Fig. 7.32(b) is obtained. For this subinterval, the inductor voltage, capacitor current, and converter input current are given by

$$\begin{aligned} L\frac{di(t)}{dt} &= v(t) - V_D \\ C\frac{dv(t)}{dt} &= -\frac{v(t)}{R} - i(t) \\ i_g(t) &= 0 \end{aligned} \tag{7.121}$$

When written in state-space form, these equations become

$$\underbrace{\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}}_{\mathbf{K}} \underbrace{\frac{d}{dt}\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\frac{d\mathbf{x}(t)}{dt}} = \underbrace{\begin{bmatrix} 0 & 1 \\ -1 & -\frac{1}{R} \end{bmatrix}}_{\mathbf{A}_2} \underbrace{\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 0 & -1 \\ 0 & 0 \end{bmatrix}}_{\mathbf{B}_2} \underbrace{\begin{bmatrix} v_g(t) \\ V_D \end{bmatrix}}_{\mathbf{u}(t)}$$

$$\underbrace{\begin{bmatrix} i_g(t) \end{bmatrix}}_{\mathbf{y}(t)} = \underbrace{\begin{bmatrix} 0 & 0 \end{bmatrix}}_{\mathbf{C}_2} \underbrace{\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 0 & 0 \end{bmatrix}}_{\mathbf{E}_2} \underbrace{\begin{bmatrix} v_g(t) \\ V_D \end{bmatrix}}_{\mathbf{u}(t)} \tag{7.122}$$

So we have also identified the subinterval 2 matrices $\mathbf{A}_2$, $\mathbf{B}_2$, $\mathbf{C}_2$, and $\mathbf{E}_2$.

The next step is to evaluate the state-space averaged equilibrium equations (7.92) to (7.94). The averaged matrix $\mathbf{A}$ is

$$\mathbf{A} = D\mathbf{A}_1 + D'\mathbf{A}_2 = D\begin{bmatrix} -R_{on} & 0 \\ 0 & -\frac{1}{R} \end{bmatrix} + D'\begin{bmatrix} 0 & 1 \\ -1 & -\frac{1}{R} \end{bmatrix} = \begin{bmatrix} -DR_{on} & D' \\ -D' & -\frac{1}{R} \end{bmatrix} \tag{7.123}$$

In a similar manner, the averaged matrices $\mathbf{B}$, $\mathbf{C}$, and $\mathbf{E}$ are evaluated, with the following results:

$$\begin{aligned} \mathbf{B} &= D\mathbf{B}_1 + D'\mathbf{B}_2 = \begin{bmatrix} D & -D' \\ 0 & 0 \end{bmatrix} \\ \mathbf{C} &= D\mathbf{C}_1 + D'\mathbf{C}_2 = \begin{bmatrix} D & 0 \end{bmatrix} \\ \mathbf{E} &= D\mathbf{E}_1 + D'\mathbf{E}_2 = \begin{bmatrix} 0 & 0 \end{bmatrix} \end{aligned} \tag{7.124}$$

The dc state equations (7.92) therefore become

$$\begin{aligned} \begin{bmatrix} 0 \\ 0 \end{bmatrix} &= \begin{bmatrix} -DR_{on} & D' \\ -D' & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} I \\ V \end{bmatrix} + \begin{bmatrix} D & -D' \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_g \\ V_D \end{bmatrix} \\ \begin{bmatrix} I_g \end{bmatrix} &= \begin{bmatrix} D & 0 \end{bmatrix} \begin{bmatrix} I \\ V \end{bmatrix} + \begin{bmatrix} 0 & 0 \end{bmatrix} \begin{bmatrix} V_g \\ V_D \end{bmatrix} \end{aligned} \tag{7.125}$$

Evaluation of Eq. (7.95) leads to the following solution for the equilibrium state and output vectors:

$$\begin{aligned} \begin{bmatrix} I \\ V \end{bmatrix} &= \left(\frac{1}{1 + \frac{D}{D'^2}\frac{R_{on}}{R}} \right) \begin{bmatrix} \frac{D}{D'^2 R} & \frac{1}{D'R} \\ -\frac{D}{D'} & 1 \end{bmatrix} \begin{bmatrix} V_g \\ V_D \end{bmatrix} \\ \begin{bmatrix} I_g \end{bmatrix} &= \left(\frac{1}{1 + \frac{D}{D'^2}\frac{R_{on}}{R}} \right) \begin{bmatrix} \frac{D^2}{D'^2 R} & \frac{D}{D'R} \end{bmatrix} \begin{bmatrix} V_g \\ V_D \end{bmatrix} \end{aligned} \tag{7.126}$$

Alternatively, the steady-state equivalent circuit of Fig. 7.33 can be constructed as usual from

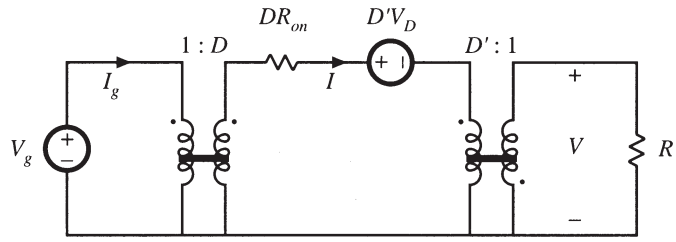


Fig. 7.33 Dc circuit model for the buck-boost converter example, equivalent to Eq. (7.125).

Eq. (7.125). The top row of Eq. (7.125) could have been obtained by application of the principle of inductor volt-second balance to the inductor voltage waveform. The second row of Eq. (7.125) could have been obtained by application of the principle of capacitor charge balance to the capacitor current waveform. The $i_g(t)$ equation expresses the dc component of the converter input current. By reconstructing circuits that are equivalent to these three equations, the dc model of Fig. 7.33 is obtained.

The small-signal model is found by evaluation of Eq. (7.95). The vector coefficients of $\hat{d}(t)$ in Eq. (7.95) are

$$\begin{aligned}\left(\mathbf{A}_1 - \mathbf{A}_2\right)\mathbf{X} + \left(\mathbf{B}_1 - \mathbf{B}_2\right)\mathbf{U} &= \begin{bmatrix} -V - IR_{on} \\ I \end{bmatrix} + \begin{bmatrix} V_g + V_D \\ 0 \end{bmatrix} = \begin{bmatrix} V_g - V - IR_{on} + V_D \\ I \end{bmatrix} \\ \left(\mathbf{C}_1 - \mathbf{C}_2\right)\mathbf{X} + \left(\mathbf{E}_1 - \mathbf{E}_2\right)\mathbf{U} &= \begin{bmatrix} I \end{bmatrix}\end{aligned} \tag{7.127}$$

The small-signal ac state equations (7.95) therefore become

$$\begin{aligned}\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \hat{i}(t) \\ \hat{v}(t) \end{bmatrix} &= \begin{bmatrix} -DR_{on} & D' \\ -D' & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} \hat{i}(t) \\ \hat{v}(t) \end{bmatrix} + \begin{bmatrix} D & -D' \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_g(t) \\ 0 \end{bmatrix} + \begin{bmatrix} V_g - V - IR_{on} + V_D \\ I \end{bmatrix} \hat{d}(t) \\ \begin{bmatrix} \hat{i}_g(t) \end{bmatrix} &= \begin{bmatrix} D & 0 \end{bmatrix} \begin{bmatrix} \hat{i}(t) \\ \hat{v}(t) \end{bmatrix} + \begin{bmatrix} 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_g(t) \\ 0 \end{bmatrix} + \begin{bmatrix} I \end{bmatrix} \hat{d}(t)\end{aligned} \tag{7.128}$$

Note that, since the diode forward voltage drop is modeled as the constant value V_D, there are no ac variations in this source, and $\hat{v}_D(t)$ equals zero. Again, a circuit model equivalent to Eq. (7.128) can be constructed, in the usual manner. When written in scalar form, Eq. (7.128) becomes

$$\begin{aligned} L\frac{d\hat{i}(t)}{dt} &= D'\,\hat{v}(t) - DR_{on}\,\hat{i}(t) + D\,\hat{v}_g(t) + \left(V_g - V - IR_{on} + V_D\right)\hat{d}(t) \\ C\frac{d\hat{v}(t)}{dt} &= -D'\,\hat{i}(t) - \frac{\hat{v}(t)}{R} + I\,\hat{d}(t) \\ \hat{i}_g(t) &= D\,\hat{i}(t) + I\,\hat{d}(t)\end{aligned} \tag{7.129}$$

Circuits corresponding to these equations are listed in Fig. 7.34. These circuits can be combined into the complete small-signal ac equivalent circuit model of Fig. 7.35.

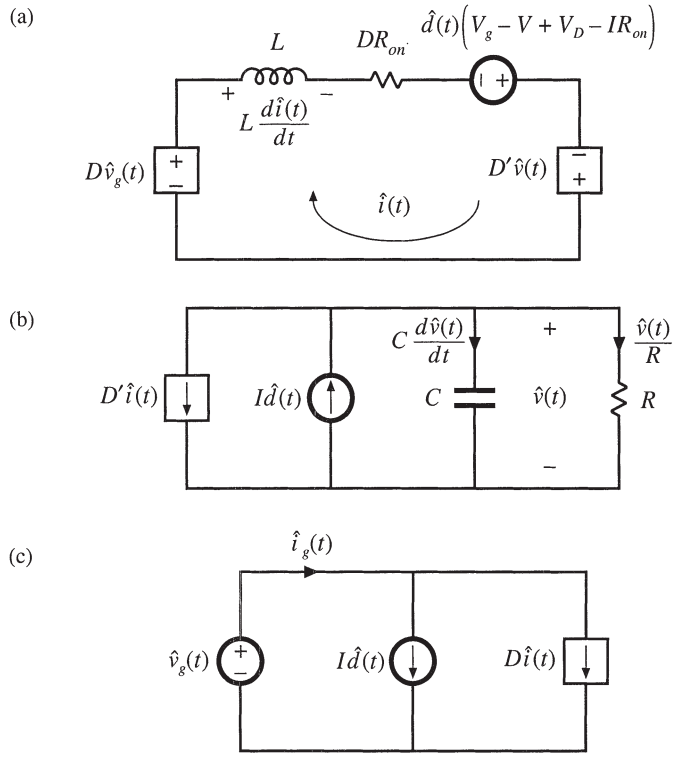


Fig. 7.34 Circuits equivalent to the small-signal converter equations: (a) inductor loop, (b) capacitor node, (c) input port.

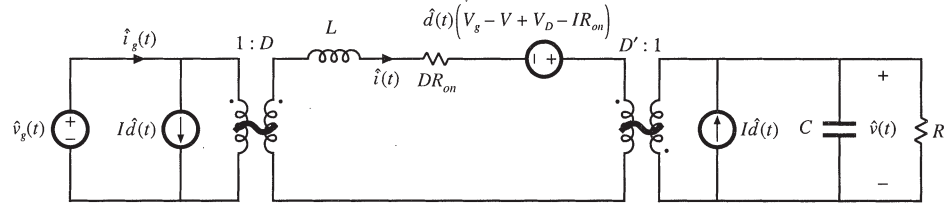


Fig. 7.35 Complete small-signal ac equivalent circuit model, nonideal buck-boost converter example.

7.4 CIRCUIT AVERAGING AND AVERAGED SWITCH MODELING

Circuit averaging is another well-known technique for derivation of converter equivalent circuits. Rather than averaging the converter state equations, with the circuit averaging technique we average the converter waveforms directly. All manipulations are performed on the circuit diagram, instead of on its equa-

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tions, and hence the circuit averaging technique gives a more physical interpretation to the model. Since circuit averaging involves averaging and small-signal linearization, it is equivalent to state-space averaging. However, in many cases circuit averaging is easier to apply, and allows the small-signal ac model to be written almost by inspection. The circuit averaging technique can also be applied directly to a number of different types of converters and switch elements, including phase-controlled rectifiers, PWM converters operated in discontinuous conduction mode or with current programming, and quasi-resonant converters—these are described in later chapters. However, in other cases it may lead to involuted models that are less easy to analyze and understand. To overcome this problem, the circuit averaging and state-space averaging approaches can be combined. Circuit averaging was developed before state-space averaging, and is described in [4]. Because of its generality, there has been a recent resurgence of interest in circuit averaging of switch networks [13–20].

The key step in circuit averaging is to replace the converter switches with voltage and current sources, to obtain a time-invariant circuit topology. The waveforms of the voltage and current generators are defined to be identical to the switch waveforms of the original converter. Once a time-invariant circuit network is obtained, then the converter waveforms can be averaged over one switching period to remove the switching harmonics. Any nonlinear elements in the averaged circuit model can then be perturbed and linearized, leading to the small-signal ac model.

In Fig. 7.36, the switching elements are separated from the remainder of the converter. The converter therefore consists of a switch network containing the converter switching elements, and a time-invariant network, containing the reactive and other remaining elements. Figure 7.36 illustrates the simple case in which there are two single-pole single-throw (SPST) switches; the switches can then be represented using a two-port network. In more complicated systems containing multiple transistors or diodes, such as in polyphase converters, the switch network may contain more than two ports.

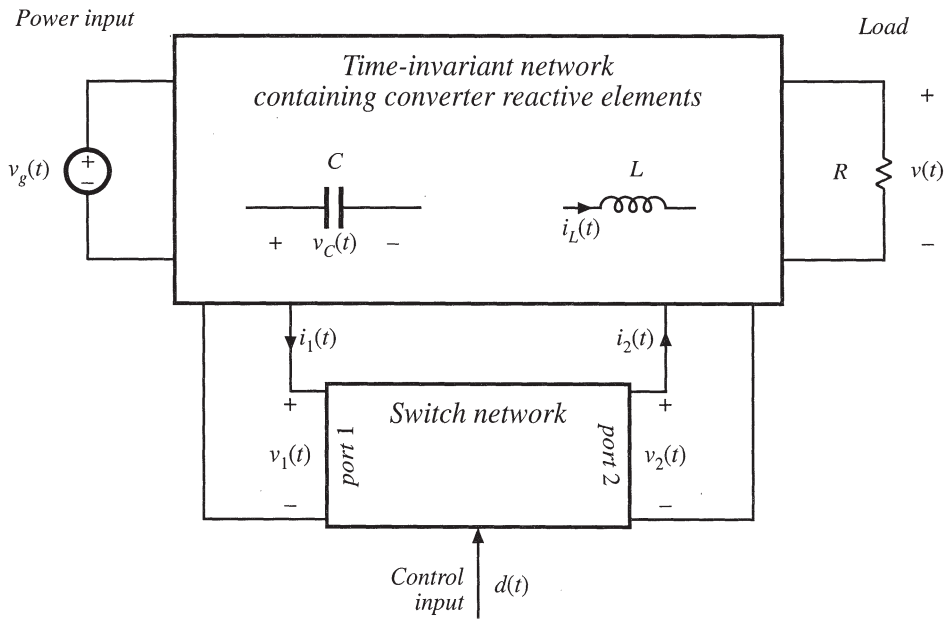


Fig. 7.36 A switching converter can be viewed as a switch network connected to a time-invariant network.

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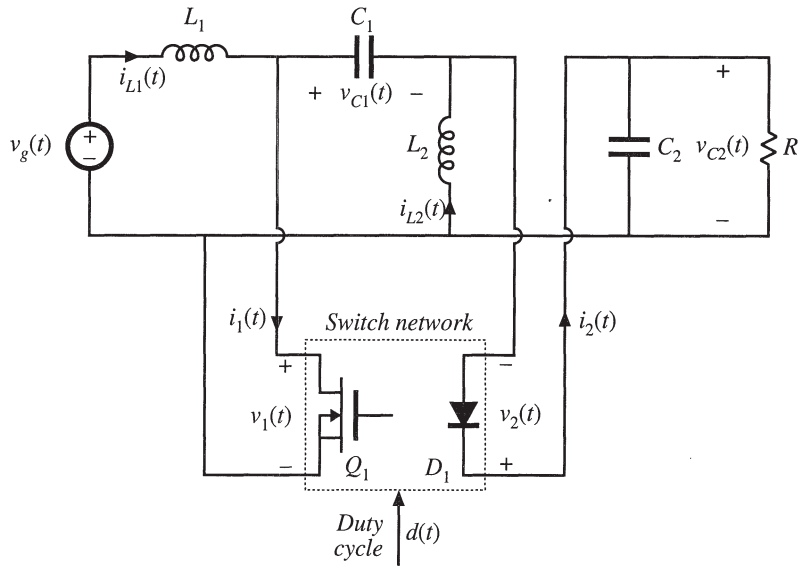


Fig. 7.37 Schematic of the SEPIC, arranged in the form of Fig. 7.36.

The central idea of the *averaged switch modeling* approach is to find an averaged circuit model for the switch network. The resulting averaged switch model can then be inserted into the converter circuit to obtain a complete averaged circuit model of the converter. An important advantage of the averaged switch modeling approach is that the same model can be used in many different converter configurations. It is not necessary to rederive an averaged circuit model for each particular converter. Furthermore, in many cases, the averaged switch model simplifies converter analysis and yields good intuitive understanding of the converter steady-state and dynamic properties.

The first step in the process of finding an averaged switch model for a switch network is to sketch the converter in the form of Fig. 7.36, in which a switch network containing only the converter switching elements is explicitly defined. The CCM SEPIC example shown in Fig. 7.37 is used to illustrate the process. There is usually more than one way to define the two ports of the switch network; a natural way to define the two-port switch network of the SEPIC is illustrated in Fig. 7.37. The switch network terminal quantities $v_1(t)$, $i_1(t)$, $v_2(t)$, and $i_2(t)$ are illustrated in Fig. 7.38 for CCM operation. Note that it is not necessary that the ports of the switch network be electrically connected within the switch network itself. Furthermore, there is no requirement that any of the terminal voltage or current waveforms of the switch network be nonpulsating.

7.4.1 Obtaining a Time-Invariant Circuit

The first step in the circuit averaging technique is to replace the switch network with voltage and current sources, such that the circuit connections do not vary in time. The switch network defined in the SEPIC is shown in Fig. 7.39(a). As with any two-port network, two of the four terminal voltages and

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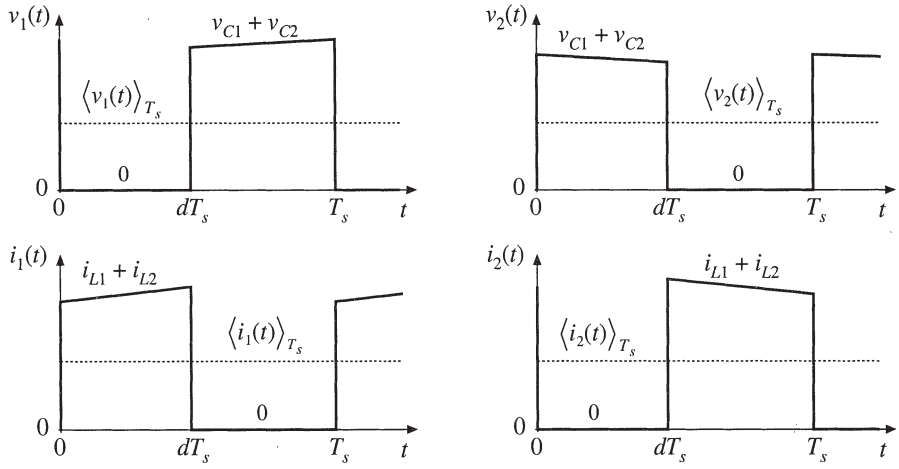


Fig. 7.38 Terminal switch network waveforms in the CCM SEPIC.

currents can be taken as independent inputs to the switch network. The remaining two voltages and/or currents are viewed as dependent outputs of the switch network. In general, the choice of independent inputs is arbitrary, as long as the inputs can indeed be independent in the given converter circuit. For CCM operation, one can choose one terminal current and one terminal voltage as the independent inputs. Let us select $i_1(t)$ and $v_2(t)$ as the switch network independent inputs. In addition, the duty cycle $d(t)$ is the independent control input.

In Fig. 7.39(b), the ports of the switch network are replaced by dependent voltage and current sources. The waveforms of these dependent sources are defined to be identical to the actual dependent outputs $v_1(t)$ and $i_2(t)$ given in Fig. 7.38. Since all waveforms in Fig. 7.39(b) match the waveforms of Figs. 7.39(a) and 7.38, the circuits are electrically equivalent. So far, no approximations have been made.

7.4.2 Circuit Averaging

The next step is determination of the average values of the switch network terminal waveforms in terms of the converter state variables (inductor currents and capacitor voltages) and the converter independent inputs (such as the input voltage and the transistor duty cycle). The basic assumption is made that the natural time constants of the converter network are much longer that the switching period T_s. This assumption coincides with the requirement for small switching ripple. One may average the waveforms over a time interval which is short compared to the system natural time constants, without significantly altering the system response. Hence, when the basic assumption is satisfied, it is a good approximation to average the converter waveforms over the switching period T_s. The resulting averaged model predicts the low-frequency behavior of the system, while neglecting the high-frequency switching harmonics. In the SEPIC example, by use of the usual small ripple approximation, the average values of the switch network terminal waveforms of Fig. 7.38 can be expressed in terms of the independent inputs and the state variables as follows:

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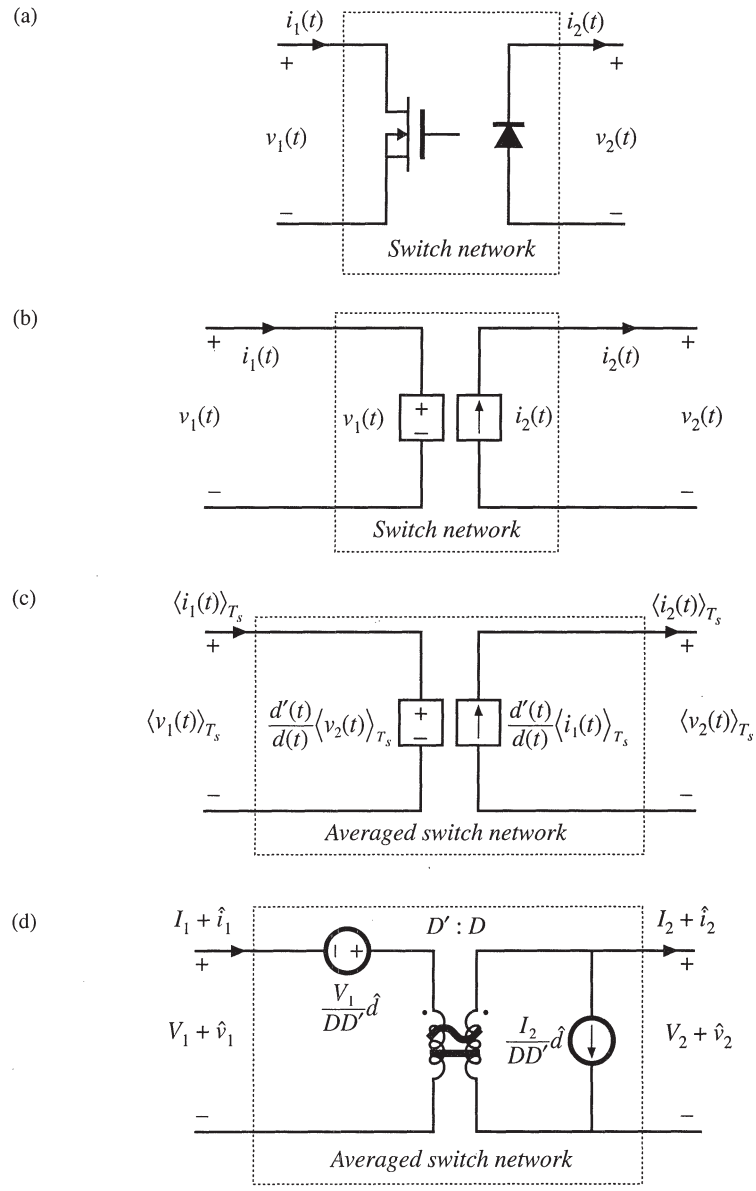


Fig. 7.39 Derivation of the averaged switch model for the CCM SEPIC: (a) switch network; (b) switch network where the switches are replaced with dependent sources whose waveforms match the switch terminal dependent waveforms; (c) large-signal, nonlinear averaged switch model obtained by averaging the switch network terminal waveforms in (b); (d) dc and ac small-signal averaged switch model.

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$$\langle v_1(t)\rangle_{T_s} = d'(t)\left(\langle v_{C1}(t)\rangle_{T_s} + \langle v_{C2}(t)\rangle_{T_s}\right) \tag{7.130}$$

$$\langle i_1(t)\rangle_{T_s} = d(t)\left(\langle i_{L1}(t)\rangle_{T_s} + \langle i_{L2}(t)\rangle_{T_s}\right) \tag{7.131}$$

$$\langle v_2(t)\rangle_{T_s} = d(t)\left(\langle v_{C1}(t)\rangle_{T_s} + \langle v_{C2}(t)\rangle_{T_s}\right) \tag{7.132}$$

$$\langle i_2(t)\rangle_{T_s} = d'(t)\left(\langle i_{L1}(t)\rangle_{T_s} + \langle i_{L2}(t)\rangle_{T_s}\right) \tag{7.133}$$

We have selected $\langle i_1(t)\rangle_{T_s}$ and $\langle v_2(t)\rangle_{T_s}$ as the switch network independent inputs. The dependent outputs of the averaged switch network are then $\langle i_2(t)\rangle_{T_s}$ and $\langle v_1(t)\rangle_{T_s}$. The next step is to express, if possible, the switch network dependent outputs $\langle i_2(t)\rangle_{T_s}$ and $\langle v_1(t)\rangle_{T_s}$ as functions *solely* of the switch network independent inputs $\langle i_1(t)\rangle_{T_s}$, $\langle v_2(t)\rangle_{T_s}$, and the control input $d(t)$. In this step, the averaged switch outputs should not be written as functions of other converter signals such as $\langle v_g(t)\rangle_{T_s}$, $\langle v_{C1}(t)\rangle_{T_s}$, $\langle v_{C2}(t)\rangle_{T_s}$, $\langle i_{L1}(t)\rangle_{T_s}$, $\langle i_{L2}(t)\rangle_{T_s}$, etc.

We can use Eqs. (7.131) and (7.132) to write

$$\langle i_{L1}(t)\rangle_{T_s} + \langle i_{L2}(t)\rangle_{T_s} = \frac{\langle i_1(t)\rangle_{T_s}}{d(t)} \tag{7.134}$$

$$\langle v_{C1}(t)\rangle_{T_s} + \langle v_{C2}(t)\rangle_{T_s} = \frac{\langle v_2(t)\rangle_{T_s}}{d(t)} \tag{7.135}$$

Substitution of these expressions into Eqs. (7.130) and (7.133) leads to

$$\langle v_1(t)\rangle_{T_s} = \frac{d'(t)}{d(t)}\langle v_2(t)\rangle_{T_s} \tag{7.136}$$

$$\langle i_2(t)\rangle_{T_s} = \frac{d'(t)}{d(t)}\langle i_1(t)\rangle_{T_s} \tag{7.137}$$

The averaged equivalent circuit for the switch network, that corresponds to Eqs. (7.136) and (7.137), is illustrated in Fig. 7.39(c). Upon completing the averaging step, the switching harmonics have been removed from all converter waveforms, leaving only the dc and low-frequency ac components. This large-signal, nonlinear, time-invariant model is valid for frequencies sufficiently less than the switching frequency. Averaging the waveforms of Fig. 7.38 modifies only the switch network; the remainder of the converter circuit is unchanged. Therefore, the averaged circuit model of the converter is obtained simply by replacing the switch network with the averaged switch model. The switch network of Fig. 7.39(a) can be identified in any two-switch converter, such as buck, boost, buck-boost, SEPIC, or Ćuk. If the converter operates in continuous conduction mode, the derivation of the averaged switch model follows the same steps, and the result shown in Fig. 7.39(c) is the same as in the SEPIC example. This means that the model of Fig. 7.39(c) can be used as a general large-signal averaged switch model for all two-switch converters operating in CCM.

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7.4.3 Perturbation and Linearization

The model of Fig. 7.39(c) is nonlinear, because the dependent generators given by Eqs. (7.136) and (7.137) are nonlinear functions of $d(t)$, $\langle i_2(t)\rangle_{T_s}$ and $\langle v_1(t)\rangle_{T_s}$. To construct a small-signal ac model, we perturb and linearize Eqs. (7.136) and (7.137) in the usual fashion. Let

$$\begin{aligned} d(t) &= D + \hat{d}(t) \\ \langle v_1(t)\rangle_{T_s} &= V_1 + \hat{v}_1(t) \\ \langle i_1(t)\rangle_{T_s} &= I_1 + \hat{i}_1(t) \\ \langle v_2(t)\rangle_{T_s} &= V_2 + \hat{v}_2(t) \\ \langle i_2(t)\rangle_{T_s} &= I_2 + \hat{i}_2(t) \end{aligned} \tag{7.138}$$

With these substitutions, Eq. (7.136) becomes

$$\left(D + \hat{d}\right)\left(V_1 + \hat{v}_1\right) = \left(D' - \hat{d}\right)\left(V_2 + \hat{v}_2\right) \tag{7.139}$$

It is desired to solve for the dependent quantity $V_1 + \hat{v}_1$. Equation (7.139) can be manipulated as follows:

$$D\left(V_1 + \hat{v}_1\right) = D'\left(V_2 + \hat{v}_2\right) - \hat{d}\left(V_1 + V_2\right) - \hat{d}\hat{v}_1 - \hat{d}\hat{v}_2 \tag{7.140}$$

The terms $\hat{d}(t)\hat{v}_1(t)$ and $\hat{d}(t)\hat{v}_2(t)$ are nonlinear, and are small in magnitude provided that the ac variations are much smaller than the quiescent values [as in Eq. (7.32)]. When the small-signal assumption is satisfied, these terms can be neglected. Upon eliminating the nonlinear terms and solving for the switch network dependent output $V_1 + \hat{v}_1$, we obtain

$$\begin{aligned} \left(V_1 + \hat{v}_1\right) &= \frac{D'}{D}\left(V_2 + \hat{v}_2\right) - \hat{d}\left(\frac{V_1 + V_2}{D}\right) \\ &= \frac{D'}{D}\left(V_2 + \hat{v}_2\right) - \hat{d}\left(\frac{V_1}{DD'}\right) \end{aligned} \tag{7.141}$$

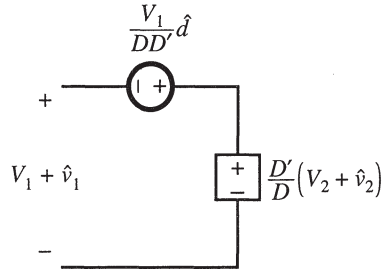


Fig. 7.40 Linearization of the dependent voltage source.

The term $(V_1/DD')\hat{d}(t)$ is driven by the control input $\hat{d}$, and hence can be represented by an independent voltage source as in Fig. 7.40. The term $(D'/D)(V_2 + \hat{v}_2(t))$ is equal to the constant value (D'/D) multiplied by the port 2 independent voltage $(V_2 + \hat{v}_2(t))$. This term is represented by a dependent voltage source in Fig. 7.40. This dependent source will become the primary winding of an ideal transformer.

In a similar manner, substitution of the relationships (7.138) into Eq. (7.137) leads to:

$$\left(D + \hat{d}\right)\left(I_2 + \hat{i}_2\right) = \left(D' - \hat{d}\right)\left(I_1 + \hat{i}_1\right) \tag{7.142}$$

The terms $\hat{i}_1(t)\hat{d}(t)$ and $\hat{i}_2(t)\hat{d}(t)$ are nonlinear, and can be neglected when the small-signal assumption is satisfied. Elimination of the nonlinear terms, and solution for $I_2 + \hat{i}_2$, yields:

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$$\begin{aligned}\left(I_2 + \hat{i}_2\right) &= \frac{D'}{D}\left(I_1 + \hat{i}_1\right) - \hat{d}\left(\frac{I_1 + I_2}{D}\right) \\ &= \frac{D'}{D}\left(I_1 + \hat{i}_1\right) - \hat{d}\left(\frac{I_2}{DD'}\right)\end{aligned} \tag{7.143}$$

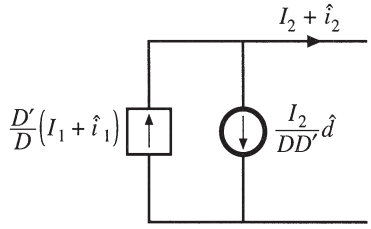


Fig. 7.41 Linearization of the dependent current source.

The term $(I_2/DD')\hat{d}(t)$ is driven by the control input $\hat{d}(t)$, and is represented by an independent current source in Fig. 7.41. The term $(D'/D)(I_1 + \hat{i}_1(t))$ is dependent on the port 1 current $(I_1 + \hat{i}_1(t))$. This term is modeled by a dependent current source in Fig. 7.41; this source will become the secondary winding of an ideal transformer. Equations (7.141) and (7.143) describe the averaged switch network model of Fig. 7.39(d). Note that the model contains both dc and small-signal ac terms: one equivalent circuit is used for both the dc and the small-signal ac models. The transformer symbol contains both a solid line (indicating that it is an ideal transformer capable of passing dc voltages and currents) and a sinusoidal line (which indicates that small-signal ac variations are modeled). The averaged switch model of Fig. 7.39(d) reveals that the switch network performs the functions of: (i) transformation of dc and small-signal ac voltage and current levels according to the D':D conversion ratio, and (ii) introduction of ac voltage and current variations into the converter circuit, driven by the control input $d(t)$. When this model is inserted into Fig. 7.37, the dc and small-signal ac SEPIC model of Fig. 7.42 is obtained. This model can now be solved to determine the steady-state voltages and currents as well as the small-signal converter transfer functions.

The switch network of Fig. 7.39(a) can be identified in all two-switch converters, including buck, boost, SEPIC, Ćuk, etc. As illustrated Fig. 7.43, a complete averaged circuit model of the converter can be constructed simply by replacing the switch network with the averaged switch model. For exam-

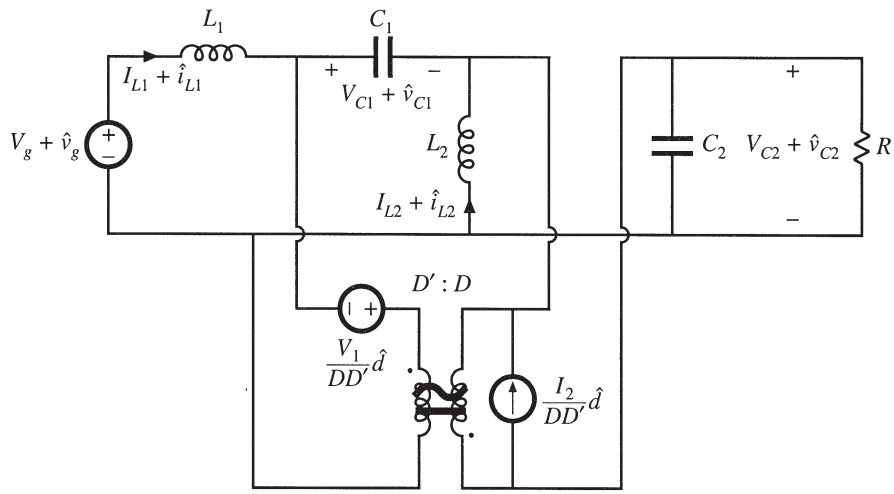


Fig. 7.42 A dc and small-signal ac averaged circuit model of the CCM SEPIC.

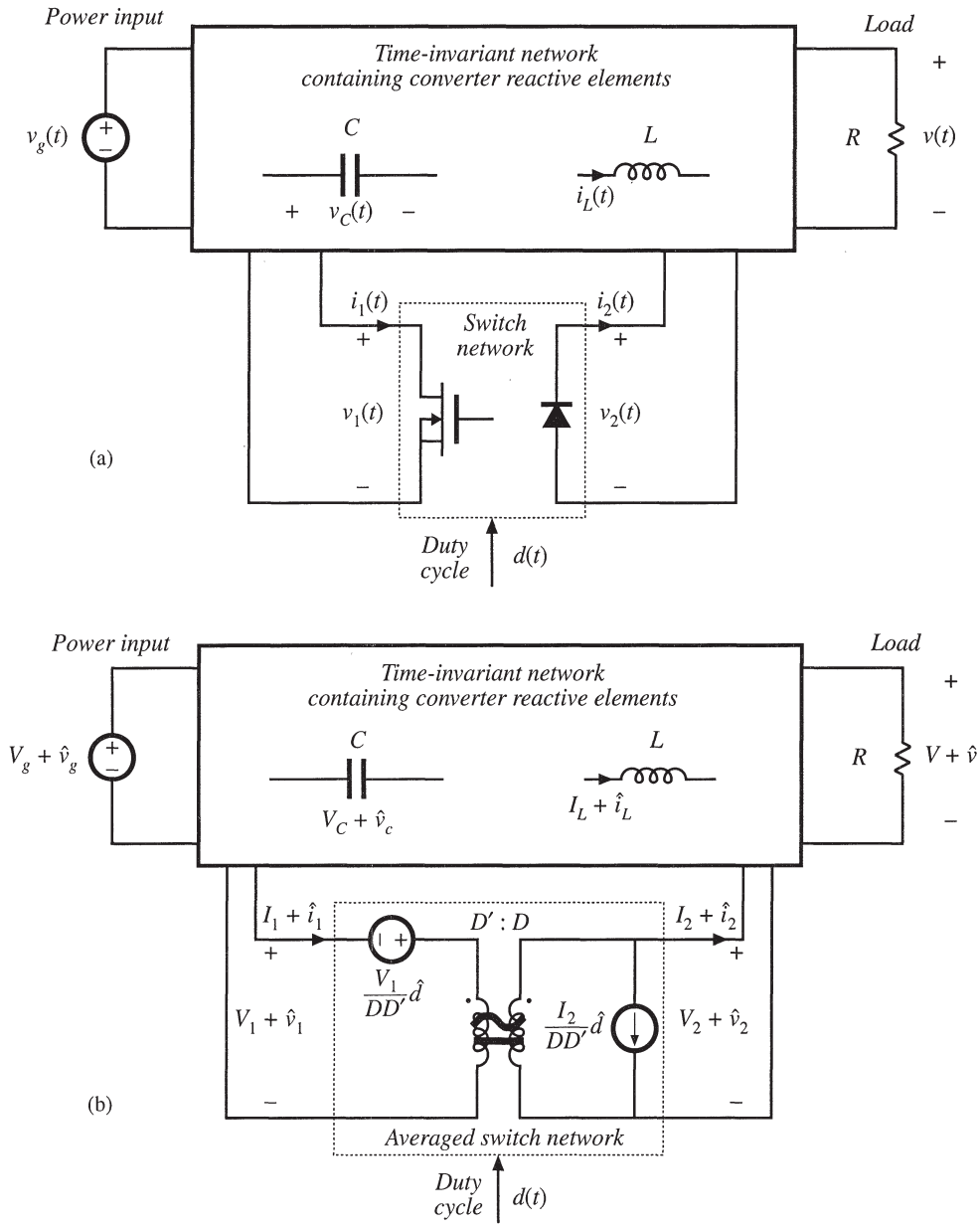


Fig. 7.43 Construction of an averaged circuit model for a two-switch converter operating in CCM: (a) the converter circuit with the general two-switch network identified; (b) dc and ac small-signal averaged circuit model obtained by replacing the switch network with the averaged model.

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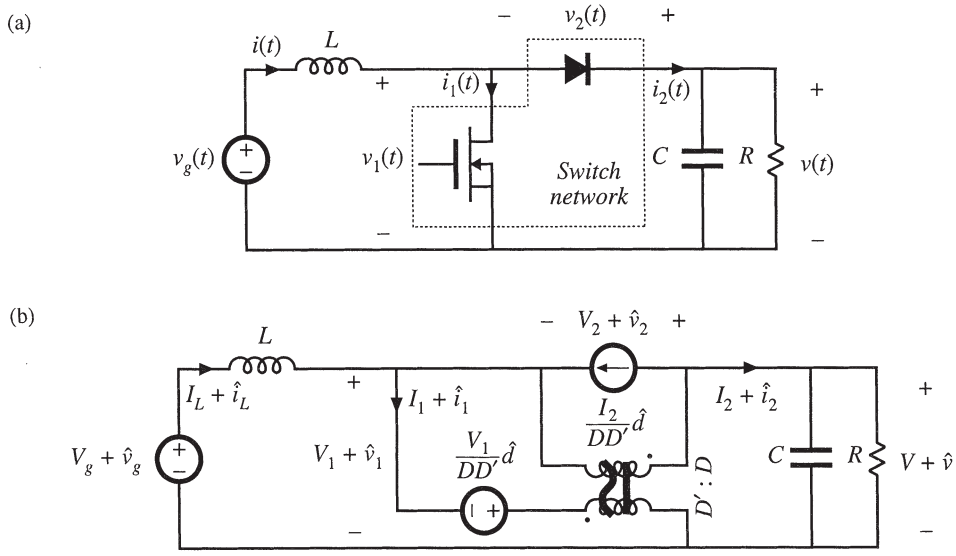


Fig. 7.44 Construction of an averaged circuit model for an ideal boost converter example: (a) converter circuit with the switch network of Fig. 7.39(a) identified; (b) a dc and small-signal ac averaged circuit model obtained by replacing the switch network with the model of Fig. 7.39(d).

ple, Fig. 7.44 shows an averaged circuit model of the boost converter obtained by identifying the switch network of Fig. 7.39(a) and replacing the switch network with the model of Fig. 7.39(d).

In summary, the circuit averaging method involves replacing the switch network with equivalent voltage and current sources, such that a time-invariant network is obtained. The converter waveforms are then averaged over one switching period to remove the switching harmonics. The large-signal model is perturbed and linearized about a quiescent operating point, to obtain a dc and a small-signal averaged switch model. Replacement of the switch network with the averaged switch model yields a complete averaged circuit model of the converter.

7.4.4 Switch Networks

So far, we have described derivation of the averaged switch model for the general two-switch network where the ports of the switch network coincide with the switch ports. No connections are assumed between the switches within the switch network itself. As a result, this switch network and its averaged model can be used to easily construct averaged circuit models of many two-switch converters, as illustrated in Fig. 7.43. It is important to note, however, that the definition of the switch network ports is not unique. Different definitions of the switch network lead to equivalent, but not identical, averaged switch models. The alternative forms of the averaged switch model may result in simpler circuit models, or models that provide better physical insight. Two alternative averaged switch models, better suited for analyses of boost and buck converters, are described in this section.

Consider the ideal boost converter of Fig. 7.45(a). The switch network contains the transistor

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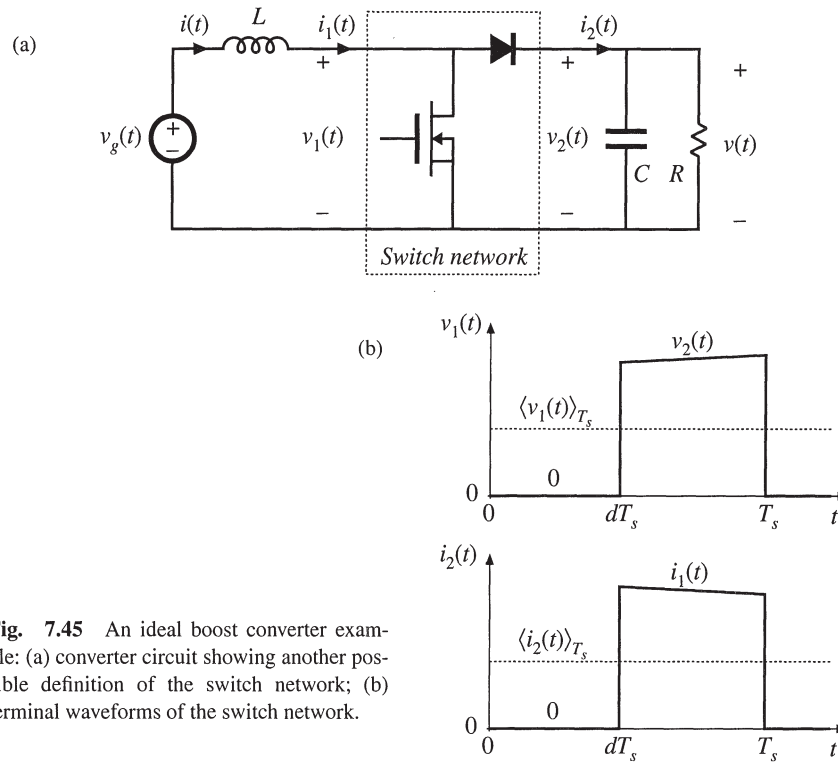


Fig. 7.45 An ideal boost converter example: (a) converter circuit showing another possible definition of the switch network; (b) terminal waveforms of the switch network.

and the diode, as in Fig. 7.44(a), but the switch network ports are defined differently. Let us proceed with the derivation of the corresponding averaged switch model. The switch network terminal waveforms are shown in Fig. 7.45(b). Since $i_1(t)$ and $v_2(t)$ coincide with the converter inductor current and capacitor voltage, it is convenient to choose these waveforms as the independent inputs to the switch network. The steps in the derivation of the averaged switch model are illustrated in Fig. 7.46.

First, we replace the switch network with dependent voltage and current generators as illustrated in Fig. 7.46(b). The voltage generator $v_1(t)$ models the dependent voltage waveform at the input port of the switch network, i.e., the transistor voltage. As illustrated in Fig. 7.45(b), $v_1(t)$ is zero when the transistor conducts, and is equal to $v_2(t)$ when the diode conducts:

$$v_1(t) = \begin{cases} 0, & 0 < t < dT_s \\ v_2(t), & dT_s < t < T_s \end{cases} \tag{7.144}$$

When $v_1(t)$ is defined in this manner, the inductor voltage waveform is unchanged. Likewise, $i_2(t)$ models the dependent current waveform at port 2 of the network, i.e., the diode current. As illustrated in Fig. 7.45(b), $i_2(t)$ is equal to zero when the transistor conducts, and is equal to $i_1(t)$ when the diode conducts:

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$$i_2(t) = \begin{cases} 0, & 0 < t < dT_s \\ i_1(t), & dT_s < t < T_s \end{cases} \tag{7.145}$$

With $i_2(t)$ defined in this manner, the capacitor current waveform is unchanged. Therefore, the original converter circuit shown in Fig. 7.45(a), and the circuit obtained by replacing the switch network of Fig. 7.46(a) with the switch network of Fig. 7.46(b), are electrically identical. So far, no approximations have been made. Next, we remove the switching harmonics by averaging all signals over one switching period, as in Eq. (7.3). The results are

$$\begin{aligned} \left\langle v_1(t) \right\rangle_{T_s} &= d'(t) \left\langle v_2(t) \right\rangle_{T_s} \\ \left\langle i_2(t) \right\rangle_{T_s} &= d'(t) \left\langle i_1(t) \right\rangle_{T_s} \end{aligned} \tag{7.146}$$

Here we have assumed that the switching ripples of the inductor current and capacitor voltage are small, or at least linear functions of time. The averaged switch model of Fig. 7.46(c) is now obtained. This is a large-signal, nonlinear model, which can replace the switch network in the original converter circuit, for construction of a large-signal nonlinear circuit model of the converter. The switching harmonics have been removed from all converter waveforms, leaving only the dc and low-frequency ac components.

The model can be linearized by perturbing and linearizing the converter waveforms about a quiescent operating point, in the usual manner. Let

$$\begin{aligned} \left\langle v_g(t) \right\rangle_{T_s} &= V_g + \hat{v}_g(t) \\ d(t) &= D + \hat{d}(t) \quad \Rightarrow d'(t) = D' - \hat{d}(t) \\ \left\langle i(t) \right\rangle_{T_s} &= \left\langle i_1(t) \right\rangle_{T_s} = I + \hat{i}(t) \\ \left\langle v(t) \right\rangle_{T_s} &= \left\langle v_2(t) \right\rangle_{T_s} = V + \hat{v}(t) \\ \left\langle v_1(t) \right\rangle_{T_s} &= V_1 + \hat{v}_1(t) \\ \left\langle i_2(t) \right\rangle_{T_s} &= I_2 + \hat{i}_2(t) \end{aligned} \tag{7.147}$$

The nonlinear voltage generator at port 1 of the averaged switch network has value

$$\left(D' - \hat{d}(t)\right)\left(V + \hat{v}(t)\right) = D'\left(V + \hat{v}(t)\right) - V\hat{d}(t) - \hat{v}(t)\hat{d}(t) \tag{7.148}$$

The term $\hat{v}(t)\hat{d}(t)$ is nonlinear, and is small in magnitude provided that the ac variations are much smaller than the quiescent values [as in Eq. (7.32)]. When the small-signal assumption is satisfied, this term can be neglected. The term $V\hat{d}(t)$ is driven by the control input, and hence can be represented by an independent voltage source. The term $D'(V + \hat{v}(t))$ is equal to the constant value D' multiplied by the output voltage $(V + \hat{v}(t))$. This term is dependent on the output capacitor voltage; it is represented by a dependent voltage source. This dependent source will become the primary winding of an ideal transformer.

The nonlinear current generator at the port 2 of the averaged switch network is treated in a similar manner. Its current is

$$\left(D' - \hat{d}(t)\right)\left(I + \hat{i}(t)\right) = D'\left(I + \hat{i}(t)\right) - I\hat{d}(t) - \hat{i}(t)\hat{d}(t) \tag{7.149}$$

The term $\hat{i}(t)\hat{d}(t)$ is nonlinear, and can be neglected provided that the small-signal assumption is satisfied.

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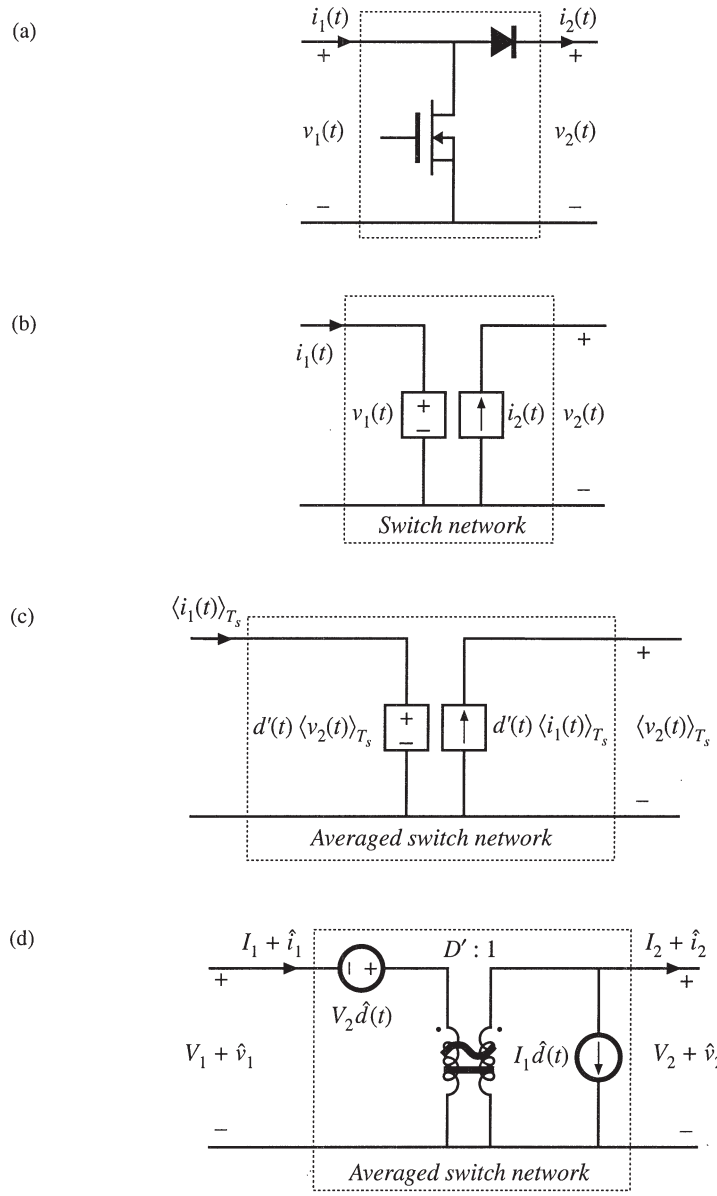


Fig. 7.46 Derivation of the averaged switch model for the CCM boost of Fig. 7.45: (a) switch network; (b) switch network where the switches are replaced by dependent sources whose waveforms match the switch terminal waveforms; (c) large-signal, nonlinear averaged switch model obtained by averaging the switch network terminal waveforms; (d) dc and ac small-signal averaged switch network model.

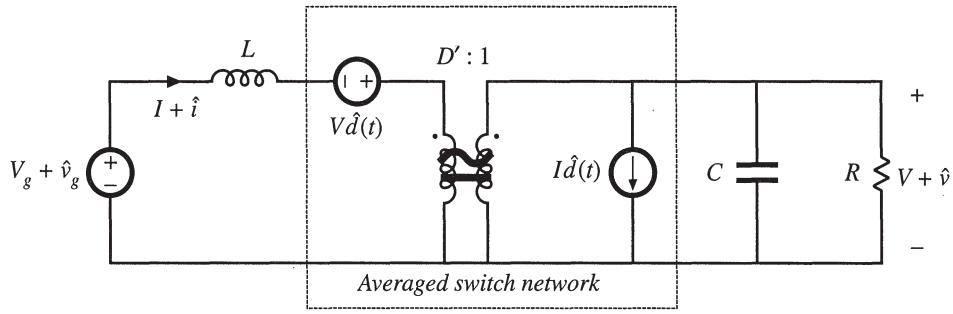


Fig. 7.47 Dc and small-signal ac averaged circuit model of the boost converter.

The term $I\hat{d}(t)$ is driven by the control input $\hat{d}(t)$, and is represented by an independent current source. The term $D'(I + \hat{i}(t))$ is dependent on the inductor current $(I + \hat{i}(t))$. This term is modeled by a dependent current source; this source will become the secondary winding of an ideal transformer.

Upon elimination of the nonlinear terms, and replacement of the dependent generators with an ideal D':1 transformer, the combined dc and small-signal ac averaged switch model of Fig. 7.46(d) is obtained. Figure 7.47 shows the complete averaged circuit model of the boost converter.

It is interesting to compare the models of Fig. 7.44(b) and Fig. 7.47. The two averaged circuit models of the boost converter are equivalent—they result in the same steady-state solution, and the same converter transfer functions. However, since both ports of the switch network in Fig. 7.45(a) share the same reference ground, the resulting averaged circuit model in Fig. 7.47 is easier to solve, and gives better physical insight into steady-state operation and dynamics of the boost converter. The circuit model of Fig. 7.47 reveals that the switch network performs the functions of: (*i*) transformation of dc and small-signal ac voltage and current levels according to the D':1 conversion ratio, and (*ii*) introduction of ac voltage and current variations into the converter circuit, driven by the control input $d(t)$. The model of Fig. 7.47 obtained using the circuit averaging approach is identical to the model of Fig. 7.17(b) obtained using the basic ac modeling technique of Section 7.2.

Next, we consider the CCM buck converter of Fig. 7.48, where the switch network ports are defined to share a common ground terminal. The derivation of the corresponding averaged switch model follows the same steps as in the SEPIC and the boost examples. Let us select $v_1(t)$ and $i_2(t)$ as the independent terminal variables of the two-port switch network, since these quantities coincide with the applied converter input voltage $v_g(t)$ and the inductor current $i(t)$, respectively. We then need to express the averaged dependent terminal waveforms $\langle i_1(t)\rangle_{T_s}$ and $\langle v_2(t)\rangle_{T_s}$ as functions of the control input $d(t)$ and of $\langle v_1(t)\rangle_{T_s}$ and $\langle i_2(t)\rangle_{T_s}$. Upon averaging the waveforms of Fig. 7.48(b), one obtains

$$\begin{aligned} \langle i_1(t)\rangle_{T_s} &= d(t)\,\langle i_2(t)\rangle_{T_s} \\ \langle v_2(t)\rangle_{T_s} &= d(t)\,\langle v_1(t)\rangle_{T_s} \end{aligned} \tag{7.150}$$

Perturbation and linearization of Eq. (7.150) then leads to

$$\begin{aligned} I_1 + \hat{i}_1(t) &= D\left(I_2 + \hat{i}_2(t)\right) + I_2\,\hat{d}(t) \\ V_2 + \hat{v}_2(t) &= D\left(V_1 + \hat{v}_1(t)\right) + V_1\,\hat{d}(t) \end{aligned} \tag{7.151}$$

An equivalent circuit corresponding to Eq. (7.151) is illustrated in Fig. 7.49(a). Replacement of the

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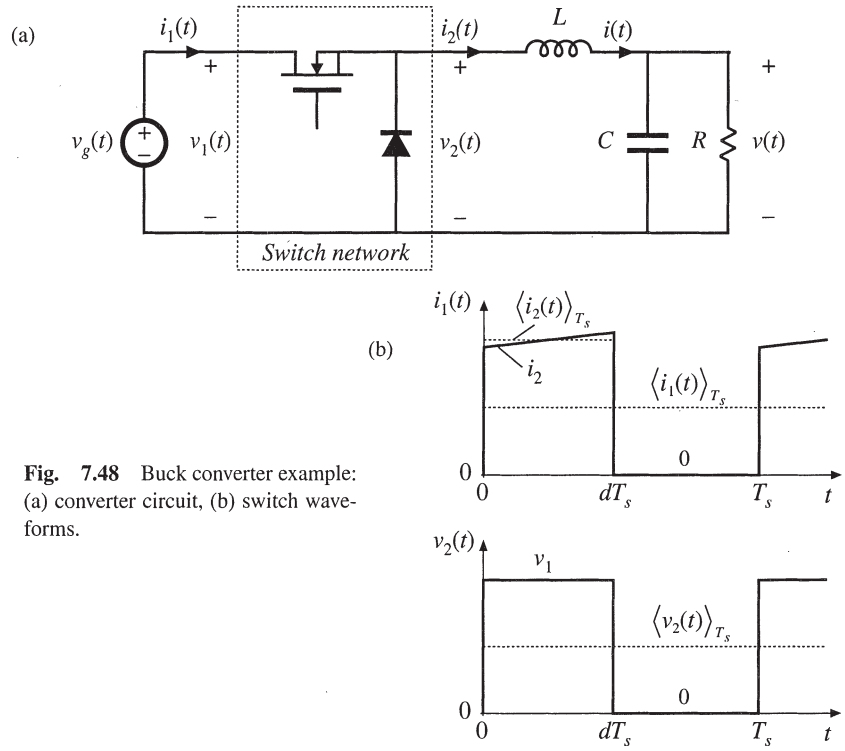


Fig. 7.48 Buck converter example: (a) converter circuit, (b) switch waveforms.

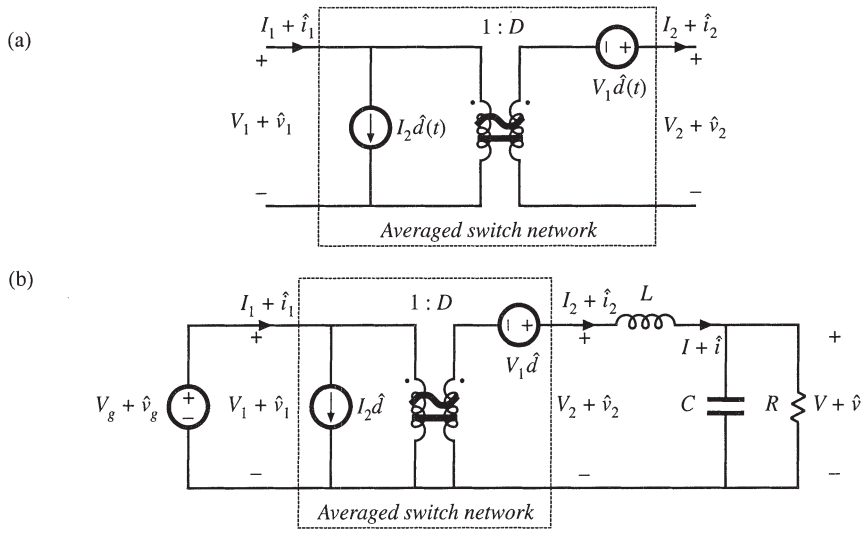


Fig. 7.49 Averaged switch modeling, buck converter example: (a) dc and small-signal ac averaged switch model; (b) Averaged circuit model of the buck converter obtained by replacement of the switch network by the averaged switch model.

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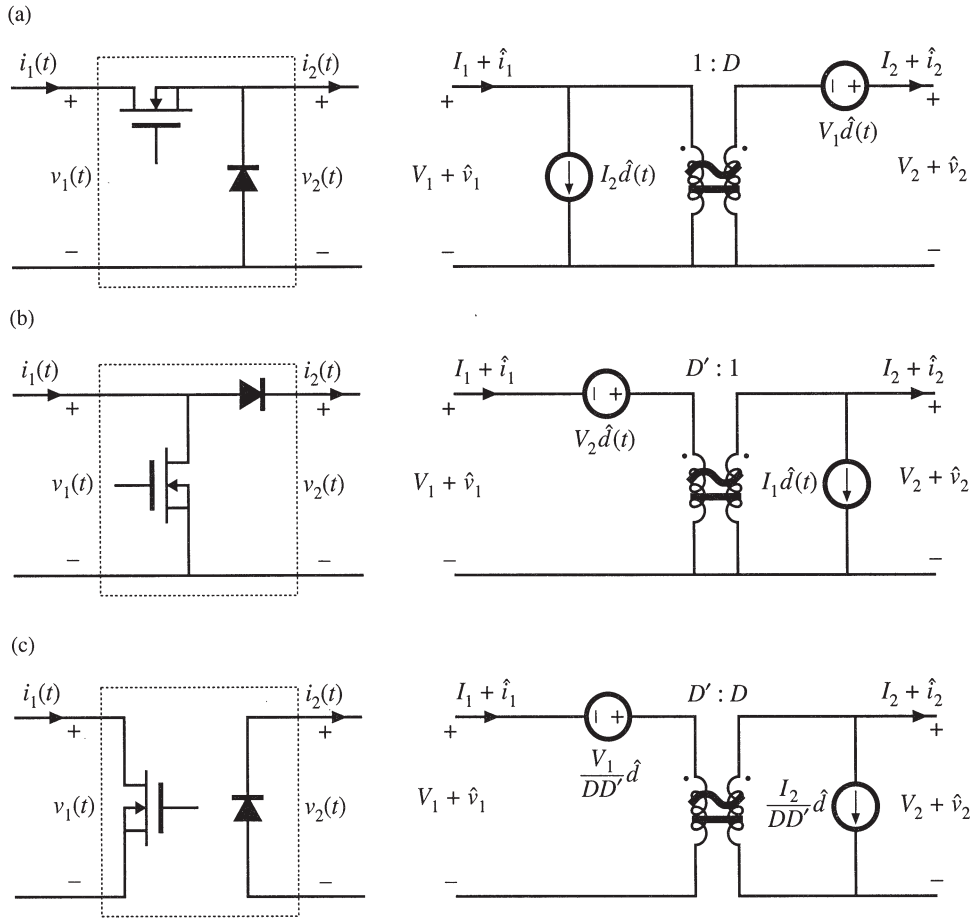


Fig. 7.50 Three basic switch networks, and their CCM dc and small-signal ac averaged switch models: (a) the buck switch network, (b) the boost switch network, and (c) the general two-switch network.

switch network in Fig. 7.48(a) with the averaged switch model of Fig. 7.49(a) leads to the converter averaged circuit model of Fig. 7.49(b). The circuit model of Fig. 7.49(b) reveals that the switch network performs the functions of: (*i*) transformation of dc and small-signal ac voltage and current levels according to the 1:D conversion ratio, and (*ii*) introduction of ac voltage and current variations into the converter circuit, driven by the control input $d(t)$. The model is easy to solve for both dc conversion ratio and small-signal frequency responses. It is identical to the model shown in Fig. 7.17(a).

The three basic switch networks—the buck switch network, the boost switch network, and the general two-switch network—together with the corresponding averaged switch models are shown in Fig. 7.50. Averaged switch models can be refined to include conduction and switching losses. These models can then be used to predict the voltages, currents, and efficiencies of nonideal converters. Two examples of averaged switch models that include losses are described in Sections 7.4.5 and 7.4.6.

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7.4.5 Example: Averaged Switch Modeling of Conduction Losses

An averaged switch model can be refined to include switch conduction losses. Consider again the SEPIC of Fig. 7.37. Suppose that the transistor on-resistance is R_{on} and the diode forward voltage drop V_D are approximately constant. In this example, all other conduction or switching losses are neglected. Our objective is to derive an averaged switch model that includes conduction losses caused by the voltage drops across R_{on} and V_D. Let us define the switch network as in Fig. 7.39(a). The waveforms of the switch network terminal currents are the same as in Fig. 7.38, but the voltage waveforms are affected by the voltage drops across R_{on} and V_D as shown in Fig. 7.51. We select $i_1(t)$ and $v_2(t)$ as the switch network independent inputs, as in Section 7.4.1. The average values of $v_1(t)$ and $v_2(t)$ can be found as follows:

$$\langle v_1(t)\rangle_{T_s} = d(t)R_{on}\left(\langle i_{L1}(t)\rangle_{T_s} + \langle i_{L2}(t)\rangle_{T_s}\right) + d'(t)\left(\langle v_{C1}(t)\rangle_{T_s} + \langle v_{C2}(t)\rangle_{T_s} + V_D\right) \tag{7.152}$$

$$\langle v_2(t)\rangle_{T_s} = d(t)\left(\langle v_{C1}(t)\rangle_{T_s} + \langle v_{C2}(t)\rangle_{T_s} - R_{on}\left(\langle i_{L1}(t)\rangle_{T_s} + \langle i_{L2}(t)\rangle_{T_s}\right)\right) + d'(t)\left(-V_D\right) \tag{7.153}$$

Next, we proceed to eliminate $\langle i_{L1}(t)\rangle_{T_s}$, $\langle i_{L2}(t)\rangle_{T_s}$, $\langle v_{C1}(t)\rangle_{T_s}$, and $\langle v_{C2}(t)\rangle_{T_s}$, to write the above equations in terms of the averaged independent terminal currents and voltages of the switch network. By combining Eqs. (7.152) and (7.153), we obtain:

$$\langle v_{C1}(t)\rangle_{T_s} + \langle v_{C2}(t)\rangle_{T_s} = \langle v_1(t)\rangle_{T_s} + \langle v_2(t)\rangle_{T_s} \tag{7.154}$$

Since the current waveforms are the same as in Fig. 7.38, Eq. (7.134) can be used here:

$$\langle i_{L1}(t)\rangle_{T_s} + \langle i_{L2}(t)\rangle_{T_s} = \frac{\langle i_1(t)\rangle_{T_s}}{d(t)} \tag{7.155}$$

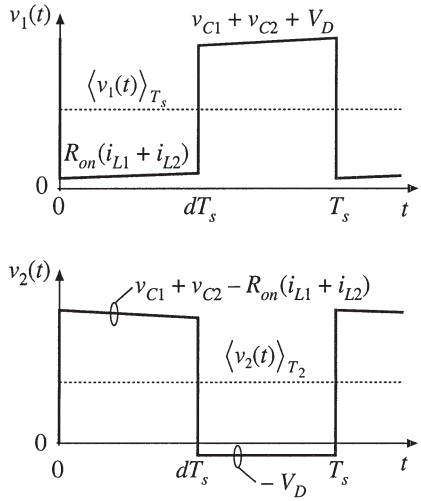


Fig. 7.51 The switch network terminal voltages $v_1(t)$ and $v_2(t)$ for the case when the transistor on-resistance is R_{on} and the diode forward voltage drop is V_D.

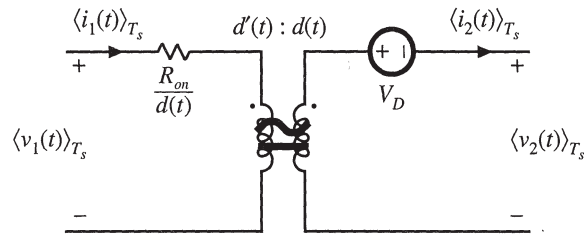


Fig. 7.52 Large-signal averaged switch model for the general two-switch network of Fig. 7.50. This model includes conduction losses due to the transistor on-resistance R_{on} and the diode forward voltage drop V_D.

Substitution of Eqs. (7.154) and (7.155) into Eq. (7.152) results in:

$$\langle v_1(t)\rangle_{T_s} = R_{on}\langle i_1(t)\rangle_{T_s} + d'(t)\left(\langle v_1(t)\rangle_{T_s} + \langle v_2(t)\rangle_{T_s} + V_D\right) \tag{7.156}$$

Equation (7.156) can be solved for the voltage $\langle v_1(t)\rangle_{T_s}$:

$$\langle v_1(t)\rangle_{T_s} = \frac{R_{on}}{d(t)}\langle i_1(t)\rangle_{T_s} + \frac{d'(t)}{d(t)}\left(\langle v_2(t)\rangle_{T_s} + V_D\right) \tag{7.157}$$

The expression for the averaged current $\langle i_2(t)\rangle_{T_s}$ is given by Eq. (7.137) derived in Section 7.4.2:

$$\langle i_2(t)\rangle_{T_s} = \frac{d'(t)}{d(t)}\langle i_1(t)\rangle_{T_s} \tag{7.158}$$

Equations (7.157) and (7.158) constitute the averaged terminal relations of the switch network. An equivalent circuit corresponding to these relationships is shown in Fig. 7.52. The generators that depend on the transistor duty cycle $d(t)$ are combined into an ideal transformer with the turns ratio $d'(t)$:$d(t)$. This part of the model is the same as in the averaged switch model derived earlier for the switch network with ideal switches. The elements R_{on}/d and V_D model the conduction losses in the switch network. This is a large-signal, nonlinear model. If desired, this model can be perturbed and linearized in the usual manner, to obtain a small-signal ac switch model.

The model of Fig. 7.52 is also well suited for computer simulations. As an example of this application, consider the buck-boost converter in Fig 7.53(a). In this converter, the transistor on-resistance is $R_{on} = 50$ mΩ, while the diode forward voltage drop is $V_D = 0.8$ V. Resistor $R_L = 100$ mΩ models the copper loss of the inductor. All other losses are neglected. Figure 7.53(b) shows the averaged circuit model of the converter obtained by replacing the switch network with the averaged switch model of Fig. 7.52.

Let's investigate how the converter output voltage reaches its steady-state value, starting from zero initial conditions. A transient simulation can be used to generate converter waveforms during the start-up transient. It is instructive to compare the responses obtained by simulation of the converter switching circuit shown in Fig. 7.53(a) against the responses obtained by simulation of the averaged circuit model shown in Fig. 7.53(b). Details of how these simulations are performed can be found in Appendix B.1. Figure 7.54 shows the start-up transient waveforms of the inductor current and the output voltage. In the waveforms obtained by simulation of the averaged circuit model, the switching ripple is removed, but other features of the converter transient responses match very closely the responses

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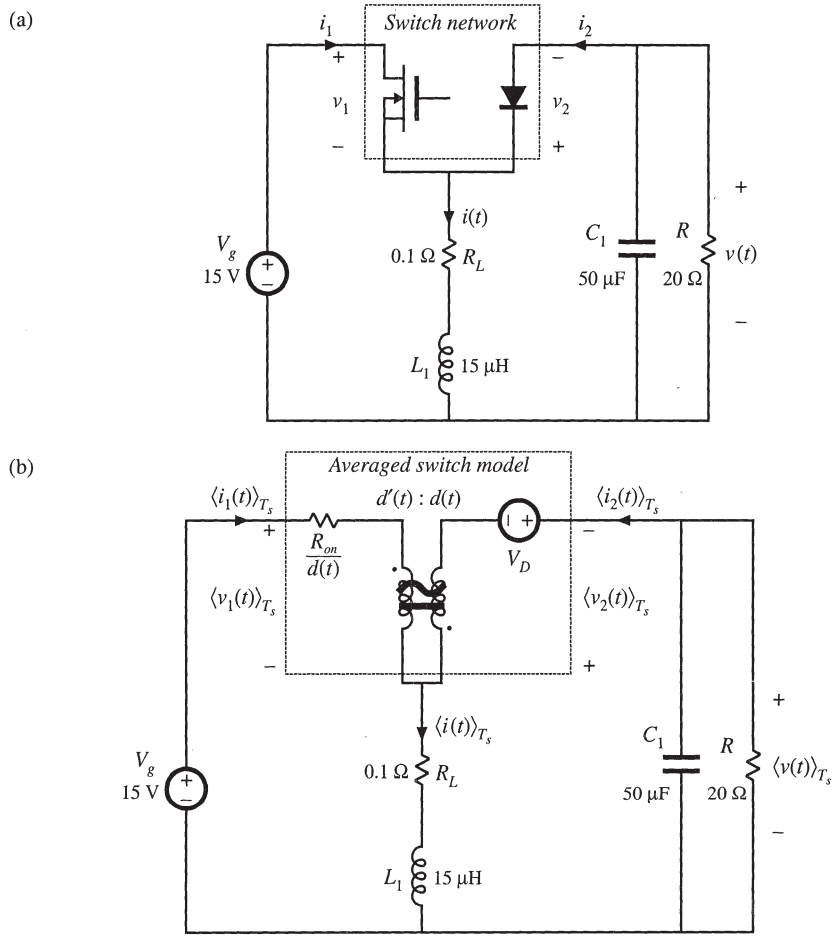


Fig. 7.53 Buck-boost converter example: (a) converter circuit; (b) averaged circuit model of the converter.

obtained from the switching circuit. Simulations of averaged circuit models can be used to predict converter steady-state and dynamic responses, as well as converter losses and efficiency.

7.4.6 Example: Averaged Switch Modeling of Switching Losses

Switching losses can also be modeled via averaged switch modeling. As an example, consider again the CCM buck converter of Fig. 7.48(a). Let us suppose that the transistor is ideal, and that the diode exhibits reverse recovery described in Section 4.3.2. The simplified switch waveforms are shown in Fig. 7.55. Initially, the diode conducts the inductor current and the transistor is in the off state. When the transistor turns on, a negative current flows through the diode so that the transistor current i_1 exceeds the inductor current. The time it takes to remove the charge Q_r stored within the diode is the reverse recovery time t_r.

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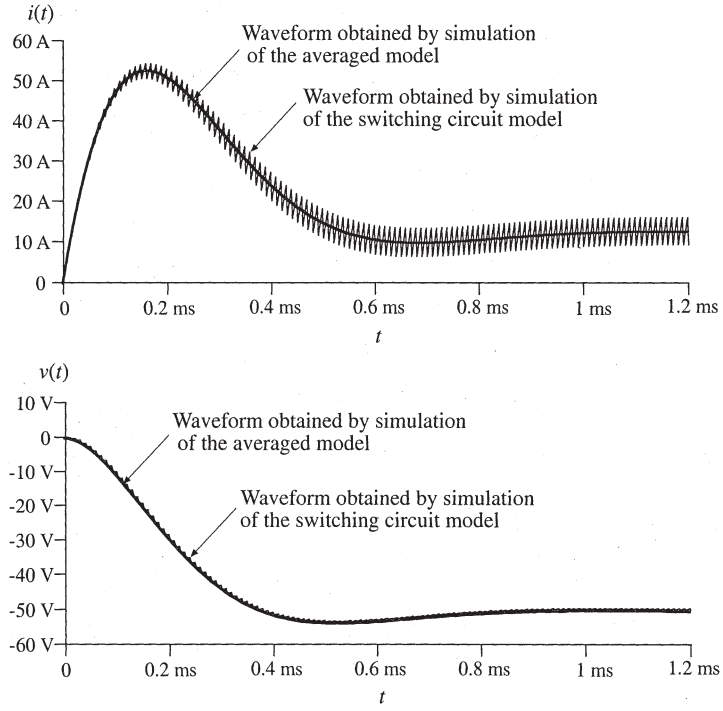


Fig. 7.54 Waveforms obtained by simulation of the switching converter circuit shown in Fig. 7.53(a) and by simulation of the averaged circuit model of Fig. 7.53(b)

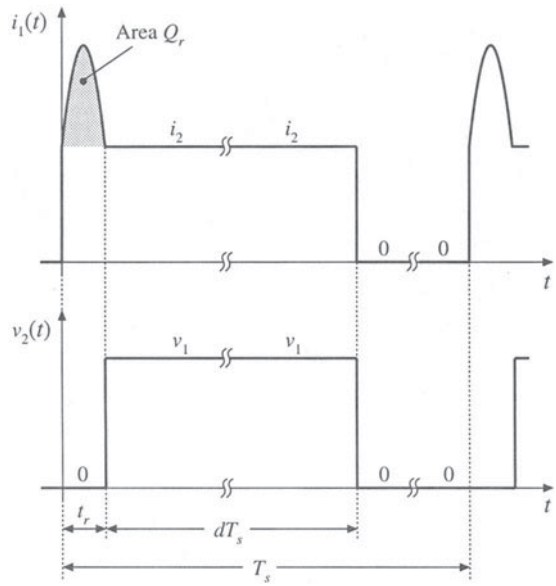


Fig. 7.55 Switch waveforms, buck converter switching loss example.

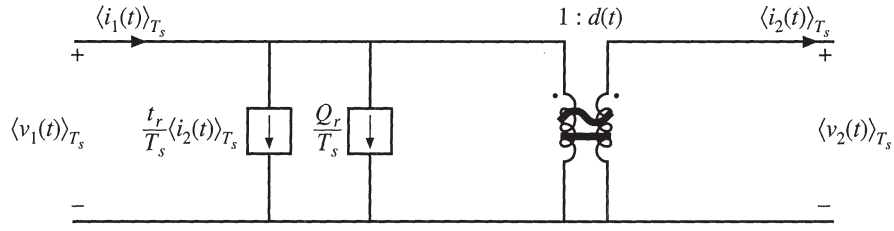


Fig. 7.56 Large-signal averaged switch model for the buck converter switching loss example.

It is assumed that the diode is "snappy," so that the voltage drop across the diode remains small during the reverse recovery time. After the diode reverse recovery is completed, the diode turns off, and the voltage v_2 across the diode quickly jumps to the input voltage $v_1 = v_g$. For this simple example, conduction losses and other switching losses are neglected.

Let us select $v_1(t)$ and $i_2(t)$ as the independent terminal variables of the two-port switch network, and derive expressions for the averaged dependent terminal waveforms $\langle i_1(t)\rangle_{T_s}$ and $\langle v_2(t)\rangle_{T_s}$. The average value of $i_1(t)$ is equal to the area under the $i_1(t)$ waveform, divided by the switching period T_s:

$$\begin{aligned}\left\langle i_1(t)\right\rangle_{T_s} &= \frac{1}{T_s}\int_0^{T_s} i_1(t)\,dt = \frac{1}{T_s}\left(Q_r + t_r\left\langle i_2(t)\right\rangle_{T_s} + dT_s\left\langle i_2(t)\right\rangle_{T_s}\right) \\ &= \frac{Q_r}{T_s} + \frac{t_r}{T_s}\left\langle i_2(t)\right\rangle_{T_s} + d\left\langle i_2(t)\right\rangle_{T_s}\end{aligned} \tag{7.159}$$

The quantity $d(t)$ is the effective transistor duty cycle, defined in Fig. 7.55 as the transistor on-time minus the reverse recovery time, divided by the switching period. The average value of $v_2(t)$ is equal to:

$$\left\langle v_2(t)\right\rangle_{T_s} = d\left\langle v_1(t)\right\rangle_{T_s} \tag{7.160}$$

Equations (7.159) and (7.160) constitute the averaged terminal relations of the switch network. An equivalent circuit corresponding to these relationships is constructed in Fig. 7.56. The generators that depend on the effective transistor duty cycle $d(t)$ are combined into an ideal transformer. To complete the model, the recovered charge Q_r and the reverse recovery time t_r can be expressed as functions of the current $\langle i_2(t)\rangle_{T_s}$ [20]. This is a large-signal averaged switch model, which accounts for the switching loss of the idealized waveforms of Fig. 7.55. If desired, this model can be perturbed and linearized in the usual manner, to obtain a small-signal ac switch model.

The model of Fig. 7.56 has the following physical interpretation. The transistor operates with the effective duty cycle $d(t)$. This is the turns ratio of the ideal dc transformer, which models the first-order switch property of lossless transfer of power from the switch input to the switch output port. The additional current generators model the switching loss. Note that both generators consume power. The total switching loss is:

$$P_{sw} = \left\langle v_1(t)\right\rangle_{T_s}\left(\frac{Q_r}{T_s} + \frac{t_r}{T_s}\left\langle i_2(t)\right\rangle_{T_s}\right) \tag{7.161}$$

These generators also correctly model how the switching loss increases the average switch input current.

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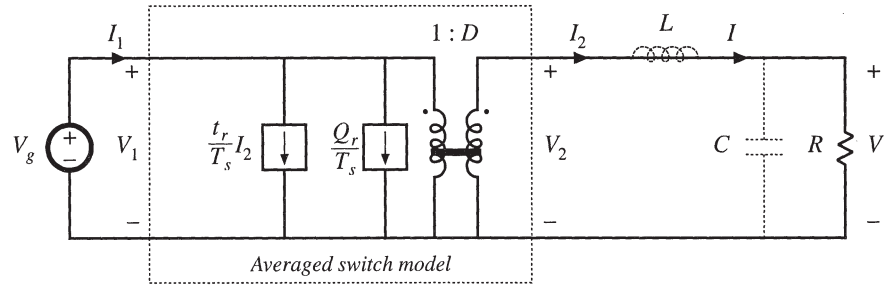


Fig. 7.57 Dc equivalent circuit model, buck converter switching loss example.

By inserting the switch model of Fig. 7.56 into the original converter circuit of Fig. 7.48(a), and by letting all waveforms be equal to their quiescent values, we obtain the steady-state model of Fig. 7.57. This model predicts that the steady-state output voltage is:

$$V = DV_g \tag{7.162}$$

To find the efficiency, we must compute the average input and output powers. The converter input power is

$$P_{in} = V_g I_1 = V_g \left(\frac{Q_r}{T_s} + \frac{t_r}{T_s} I_2 + DI_2 \right) \tag{7.163}$$

The average output power is

$$P_{out} = VI_2 = DV_g I_2 \tag{7.164}$$

Hence the converter efficiency is

$$\eta = \frac{P_{out}}{P_{in}} = \frac{1}{1 + \frac{Q_r}{DT_s I} + \frac{t_r}{DT_s}} \tag{7.165}$$

Beware, the efficiency is not simply equal to V/DV_g.

7.5 THE CANONICAL CIRCUIT MODEL

Having discussed several methods for deriving the ac equivalent circuit models of switching converters, let us now pause to interpret the results. All PWM CCM dc–dc converters perform similar basic functions. First, they transform the voltage and current levels, ideally with 100% efficiency. Second, they contain low-pass filtering of the waveforms. While necessary to remove the high-frequency switching ripple, this filtering also influences low-frequency voltage and current variations. Third, the converter waveforms can be controlled by variation of the duty cycle.

We expect that converters having similar physical properties should have qualitatively similar equivalent circuit models. Hence, we can define a *canonical circuit model* that correctly accounts for all

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of these basic properties [1-3]. The ac equivalent circuit of any CCM PWM dc–dc converter can be manipulated into this canonical form. This allows us to extract physical insight, and to compare the ac properties of converters. The canonical model is used in several later chapters, where it is desired to analyze converter phenomena in a general manner, without reference to a specific converter. So the canonical model allows us to define and discuss the physical ac properties of converters.

In this section, the canonical circuit model is developed, based on physical arguments. An example is given which illustrates how to manipulate a converter equivalent circuit into canonical form. Finally, the parameters of the canonical model are tabulated for several basic ideal converters.

7.5.1 Development of the Canonical Circuit Model

The physical elements of the canonical circuit model are collected, one at a time, in Fig. 7.58. The converter contains a power input port $v_g(t)$ and a control input port $d(t)$, as well as a power output port and load having voltage $v(t)$. As discussed in Chapter 3, the basic function of any CCM PWM dc–dc converter is the conversion of dc voltage and current levels, ideally with 100% efficiency. As illustrated in Fig. 7.58(a), we have modeled this property with an ideal dc transformer, having effective turns ratio $1{:}M(D)$ where M is the conversion ratio. This conversion ratio is a function of the quiescent duty cycle D. As discussed in Chapter 3, this model can be refined, if desired, by addition of resistors and other elements that model the converter losses.

Slow variations $v_g(t)$ in the power input induce ac variations $v(t)$ in the converter output voltage. As illustrated in Fig. 7.58(b), we expect these variations also to be transformed by the conversion ratio $M(D)$.

The converter must also contain reactive elements that filter the switching harmonics and transfer energy between the power input and power output ports. Since it is desired that the output switching ripple be small, the reactive elements should comprise a low-pass filter having a cutoff frequency well below the switching frequency. This low-pass characteristic also affects how ac line voltage variations influence the output voltage. So the model should contain an effective low-pass filter as illustrated in Fig. 7.58(c). This figure predicts that the line-to-output transfer function is

$$G_{vg}(s) = \frac{\hat{v}(s)}{\hat{v}_g(s)} = M(D)\, H_e(s) \tag{7.166}$$

where $H_e(s)$ is the transfer function of the effective low-pass filter loaded by resistance R. When the load is nonlinear, R is the incremental load resistance, evaluated at the quiescent operating point. The effective filter also influences other properties of the converter, such as the small-signal input and output impedances. It should be noted that the elemental values in the effective low-pass filter do not necessarily coincide with the physical element values in the converter. In general, the element values, transfer function, and terminal impedances of the effective low-pass filter can vary with quiescent operating point. Examples are given in the following subsections.

Control input variations, specifically, duty cycle variations $\hat{d}(t)$, also induce ac variations in the converter voltages and currents. Hence, the model should contain voltage and current sources driven by $\hat{d}(t)$. In the examples of the previous section, we have seen that both voltage sources and current sources appear, which are distributed around the circuit model. It is possible to manipulate the model such that all of the $\hat{d}(t)$ sources are pushed to the input side of the equivalent circuit. In the process, the sources may become frequency-dependent; an example is given in the next subsection. In general, the sources can be combined into a single voltage source $e(s)\hat{d}(s)$ and a single current source $j(s)\hat{d}(s)$ as shown in

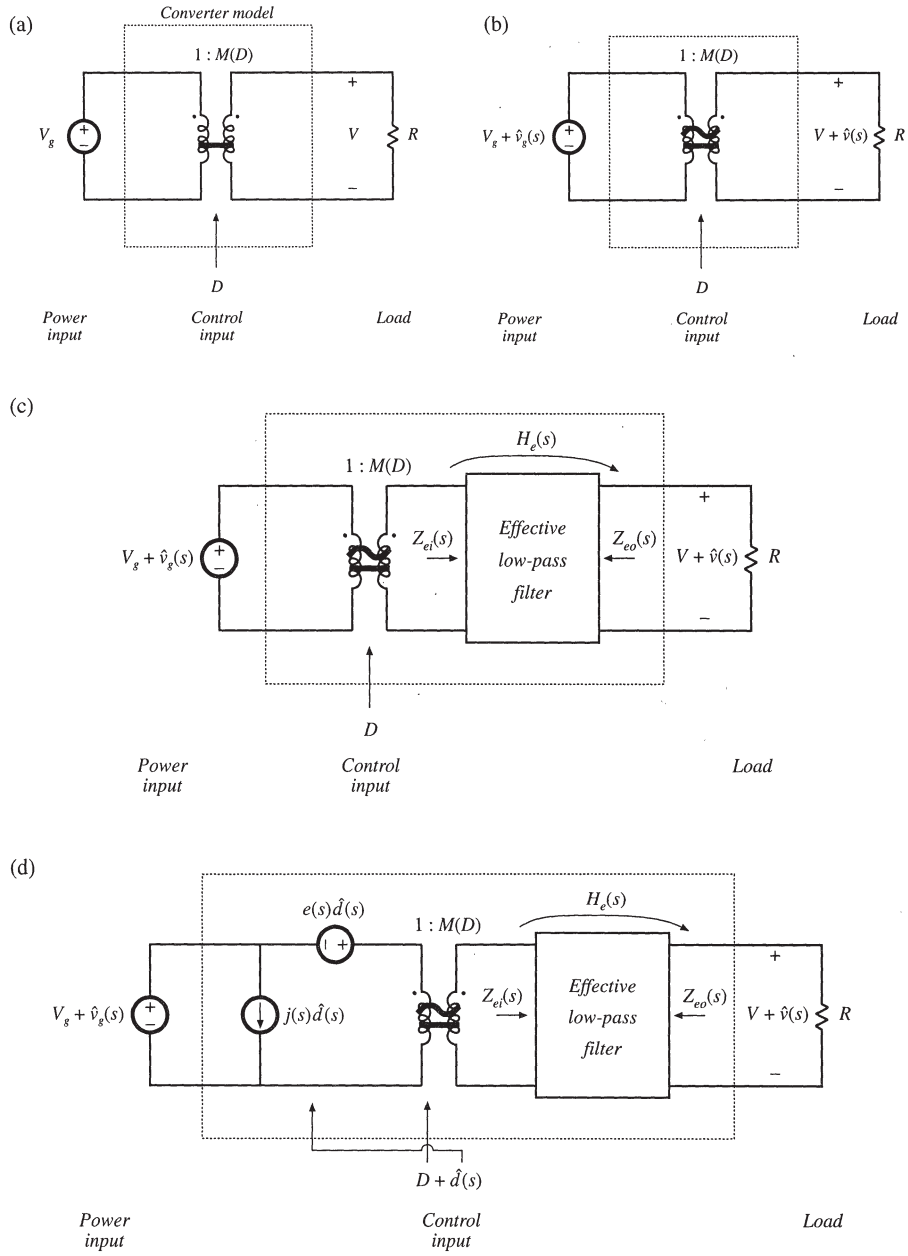


Fig. 7.58 Development of the canonical circuit model, based on physical arguments: (a) dc transformer model, (b) inclusion of ac variations, (c) reactive elements introduce effective low-pass filter, (d) inclusion of ac duty cycle variations.

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Fig. 7.58(d). This model predicts that the small-signal control-to-output transfer function is

$$G_{vd}(s) = \frac{\hat{v}(s)}{\hat{d}(s)} = e(s)\, M(D)\, H_e(s) \tag{7.167}$$

This transfer function is found by setting the $\hat{v}_g(s)$ variations to zero, and solving for the dependence of $\hat{v}(s)$ on $\hat{d}(s)$. Figure 7.58(d) is the complete canonical circuit, which can model any PWM CCM dc–dc converter.

7.5.2 Example: Manipulation of the Buck-Boost Converter Model into Canonical Form

To illustrate the steps in the derivation of the canonical circuit model, let us manipulate the equivalent circuit of the buck-boost converter into canonical form. A small-signal ac equivalent circuit for the buck-boost converter is derived in Section 7.2. The result, Fig. 7.16(b), is reproduced in Fig. 7.59. To manipulate this network into canonical form, it is necessary to push all of the independent $d(t)$ generators to the left, while pushing the inductor to the right and combining the transformers.

The $(V_g - V)\hat{d}(t)$ voltage source is in series with the inductor, and hence the positions of these two elements can be interchanged. In Fig. 7.60(a), the voltage source is placed on the primary side of the $1{:}D$ ideal transformer; this requires dividing by the effective turns ratio D. The output-side $I\hat{d}(t)$ current source has also been moved to the primary side of the $D'{:}1$ transformer. This requires multiplying by the turns ratio $1/D'$. The polarity is also reversed, in accordance with the polarities of the $D'{:}1$ transformer windings.

Next, we need to move the $I\hat{d}(t)/D$ current source to the left of the inductor. This can be done using the artifice illustrated in Fig. 7.60(b). The ground connection of the current source is broken, and the source is connected to node A instead. A second, identical, current source is connected from node A to ground. The second source causes the current flowing into node A to be unchanged, such that the node equations of Figs. 7.60(a) and 7.60(b) are identical.

In Fig. 7.60(c), the parallel combination of the inductor and current source is converted into Thevenin equivalent form. The series combination of an inductor and voltage source are obtained.

In Fig. 7.60(d), the $I\hat{d}(t)/D$ current source is pushed to the primary side of the $1{:}D$ transformer. The magnitude of the current source is multiplied by the turns ratio D. In addition, the current source is pushed through the $(V_g - V)\hat{d}(t)/D$ voltage source, using the previously described artifice. The ground connection of the source is moved to node B, and an identical source is connected from node B to ground such that the circuit node equations are unchanged.

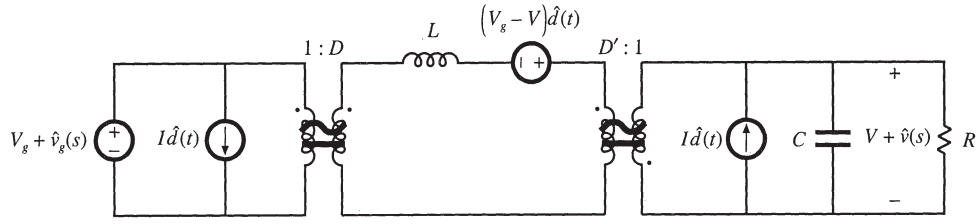


Fig. 7.59 Small-signal ac model of the buck-boost converter, before manipulation into canonical form.

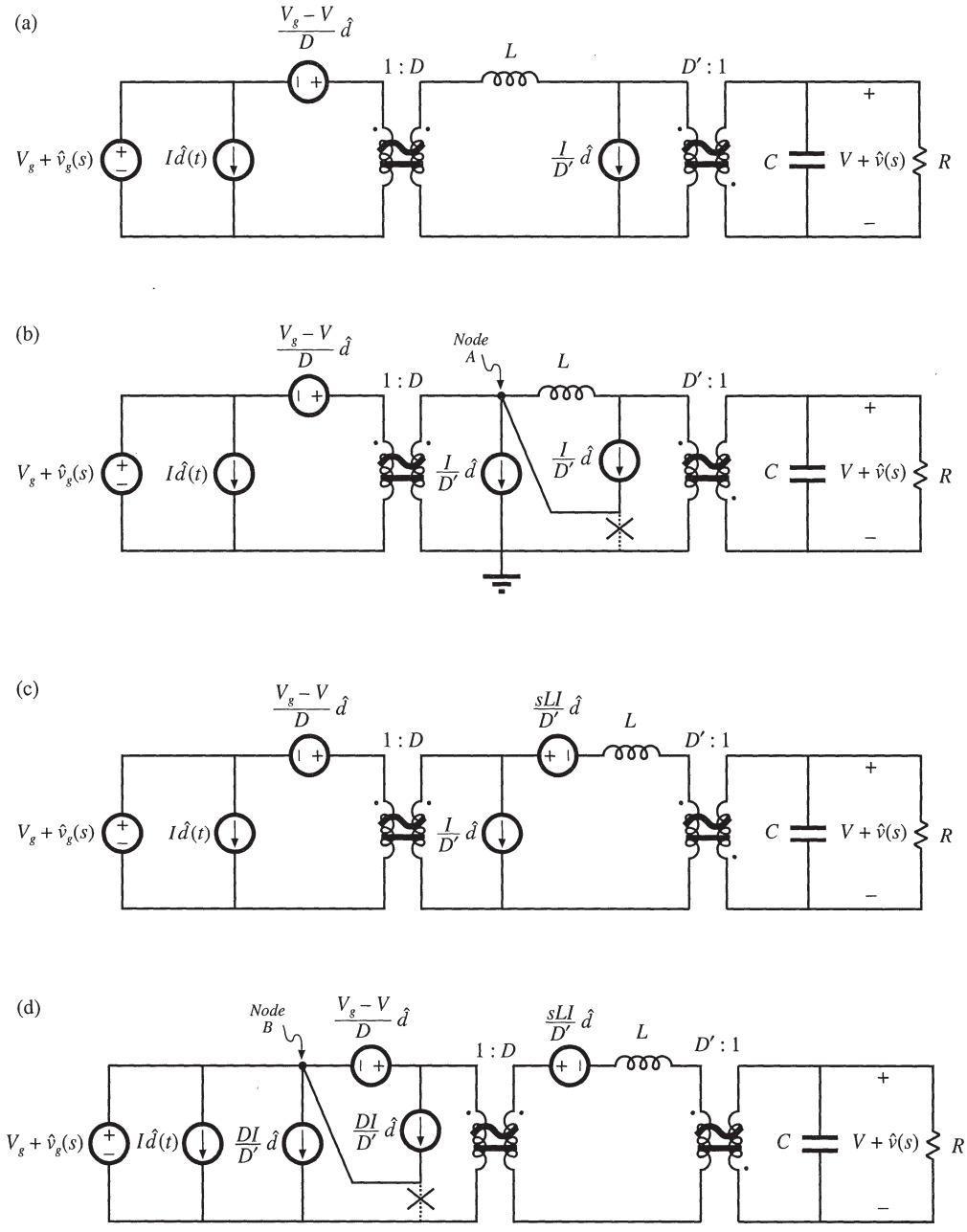


Fig. 7.60 Steps in the manipulation of the buck-boost ac model into canonical form.

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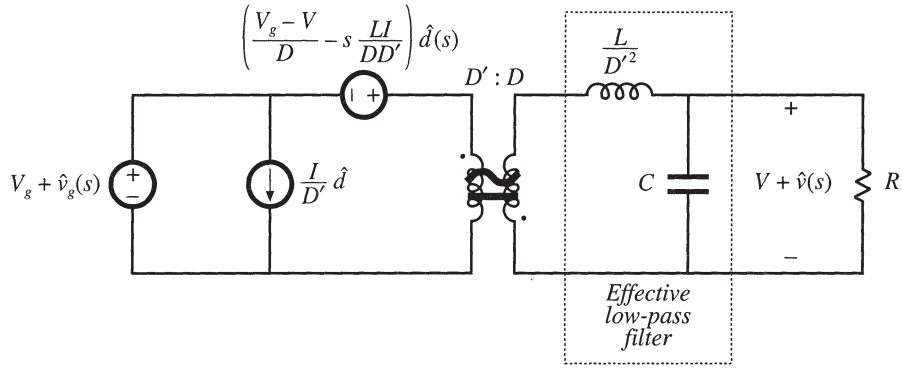


Fig. 7.61 The buck-boost converter model, in canonical form.

Figure 7.61 is the final form of the model. The inductor is moved to the secondary side of the D':1 transformer, by multiplying by the square of the turns ratio as shown. The $sLI\hat{d}(t)/D'$ voltage source is moved to the primary side of the 1:D transformer, by dividing by the turns ratio D. The voltage and current sources are combined as shown, and the two transformers are combined into a single D':D transformer. The circuit is now in canonical form.

It can be seen that the inductance of the effective low-pass filter is not simply equal to the physical inductor value L, but rather is equal to L/D'^2. At different quiescent operating points, with different values of D', the value of the effective inductance will change. In consequence, the transfer function, input impedance, and output impedance of the effective low-pass filter will also vary with quiescent operating point. The reason for this variation is the transformation of the inductance value by the effective D':1 transformer.

It can also be seen from Fig. 7.61 that the coefficient of the $\hat{d}(t)$ voltage generator is

$$e(s) = \frac{V_g - V}{D} - s\frac{LI}{DD'} \tag{7.168}$$

This expression can be simplified by substitution of the dc relationships (7.29). The result is

$$e(s) = -\frac{V}{D^2}\left(1 - s\frac{DL}{D'^2R}\right) \tag{7.169}$$

When we pushed the output-side $I\hat{d}(t)$ current source through the inductor, we obtained a voltage source having a frequency dependence. In consequence, the $e(s)\hat{d}$ voltage generator is frequency-dependent.

7.5.3 Canonical Circuit Parameter Values for Some Common Converters

For ideal CCM PWM dc–dc converters containing a single inductor and capacitor, the effective low-pass filter of the canonical model should contain a single inductor and a single capacitor. The canonical model then reduces to the circuit of Fig. 7.62. It is assumed that the capacitor is connected directly across the load. The parameter values for the basic buck, boost, and buck-boost converters are collected in Table 7.1. Again, it should be pointed out that the effective inductance L_e depends not only on the physical

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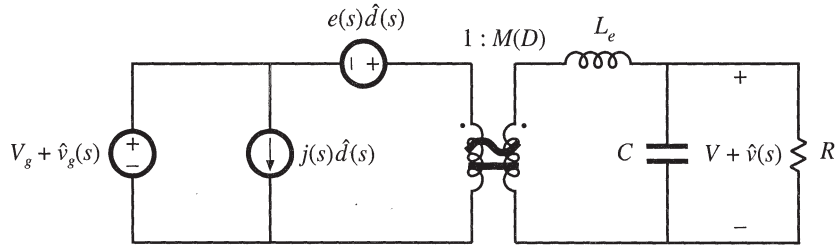


Fig. 7.62 The canonical model, for ideal CCM converters containing a single inductor and capacitor.

Table 7.1 Canonical model parameters for the ideal buck, boost and buck-boost converters

Converter	$M(D)$	L_e	$e(s)$	$j(s)$
Buck	D	L	$\frac{V}{D^2}$	$\frac{V}{R}$
Boost	$\frac{1}{D'}$	$\frac{L}{D'^2}$	$V\left(1 - \frac{sL}{D'^2R}\right)$	$\frac{V}{D'^2R}$
Buck-boost	$-\frac{D}{D'}$	$\frac{L}{D'^2}$	$-\frac{V}{D^2}\left(1 - \frac{sDL}{D'^2R}\right)$	$-\frac{V}{D'^2R}$

inductor value L, but also on the quiescent duty cycle D. Furthermore, the current flowing in the effective inductance L_e does not in general coincide with the physical inductor current $I + \hat{i}(t)$.

The model of Fig. 7.62 can be solved using conventional linear circuit analysis, to find quantities of interest such as the converter transfer functions, input impedance, and output impedance. Transformer isolated versions of the buck, boost, and buck-boost converters, such as the full bridge, forward, and flyback converters, can also be modeled using the equivalent circuit of Fig. 7.62 and the parameters of Table 7.1, provided that one correctly accounts for the transformer turns ratio.

7.6 MODELING THE PULSE-WIDTH MODULATOR

We have now achieved the goal, stated at the beginning of this chapter, of deriving a useful equivalent circuit model for the switching converter in Fig. 7.1. One detail remains: modeling the pulse-width modulator. The pulse-width modulator block shown in Fig. 7.1 produces a logic signal $\delta(t)$ that commands the converter power transistor to switch on and off. The logic signal $\delta(t)$ is periodic, with frequency f_s and duty cycle $d(t)$. The input to the pulse-width modulator is an analog control signal $v_c(t)$. The function of the pulse-width modulator is to produce a duty cycle $d(t)$ that is proportional to the analog control volt-

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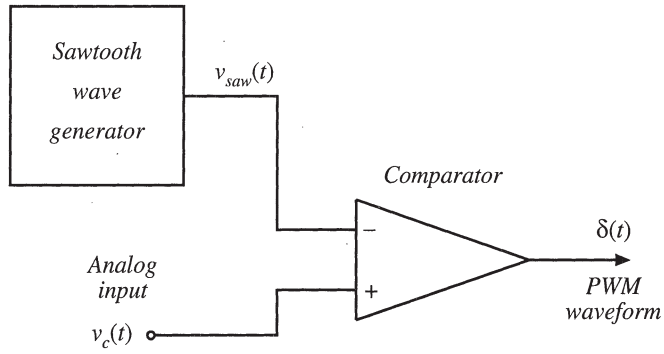


Fig. 7.63 A simple pulse-width modulator circuit.

age $v_c(t)$.

A schematic diagram of a simple pulse-width modulator circuit is given in Fig. 7.63. A sawtooth wave generator produces the voltage waveform $v_{saw}(t)$ illustrated in Fig. 7.64. The peak-to-peak amplitude of this waveform is V_M. The converter switching frequency f_s is determined by and equal to the frequency of $v_{saw}(t)$. An analog comparator compares the analog control voltage $v_c(t)$ to $v_{saw}(t)$. This comparator produces a logic-level output which is high whenever $v_c(t)$ is greater than $v_{saw}(t)$, and is otherwise low. Typical waveforms are illustrated in Fig. 7.64.

If the sawtooth waveform $v_{saw}(t)$ has minimum value zero, then the duty cycle will be zero whenever $v_c(t)$ is less than or equal to zero. The duty cycle will be $D = 1$ whenever $v_c(t)$ is greater than or equal to V_M. If, over a given switching period, $v_{saw}(t)$ varies linearly with t, then for $0 \le v_c(t) \le V_M$ the duty cycle d will be a linear function of v_c. Hence, we can write

$$d(t) = \frac{v_c(t)}{V_M} \quad \text{for } 0 \le v_c(t) \le V_M \tag{7.170}$$

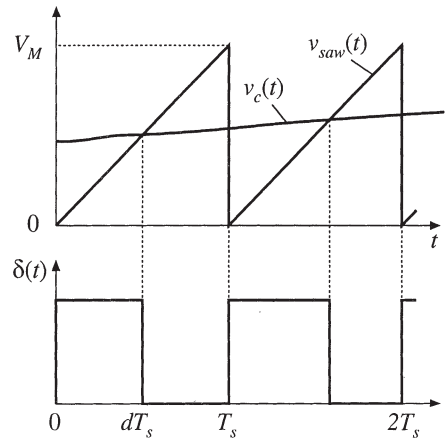


Fig. 7.64 Waveforms of the circuit of Fig. 7.63.

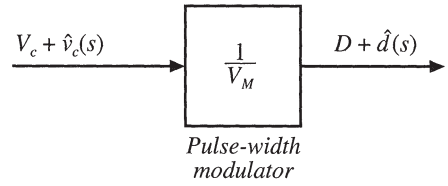


Fig. 7.65 Pulse-width modulator block diagram.

This equation is the input-output characteristic of the pulse-width modulator [2,11].

To be consistent with the perturbed-and-linearized converter models of the previous sections, we can perturb Eq. (7.170). Let

$$\begin{aligned} v_c(t) &= V_c + \hat{v}_c(t) \\ d(t) &= D + \hat{d}(t) \end{aligned} \tag{7.171}$$

Insertion of Eq. (7.171) into Eq. (7.170) leads to

$$D + \hat{d}(t) = \frac{V_c + \hat{v}_c(t)}{V_M} \tag{7.172}$$

A block diagram representing Eq. (7.172) is illustrated in Fig. 7.65. The pulse-width modulator has linear gain $1/V_M$. By equating like terms on both sides of Eq. (7.172), one obtains

$$\begin{aligned} D &= \frac{V_c}{V_M} \\ \hat{d}(t) &= \frac{\hat{v}_c(t)}{V_M} \end{aligned} \tag{7.173}$$

So the quiescent value of the duty cycle is determined in practice by V_c.

The pulse-width modulator model of Fig. 7.65 is sufficiently accurate for nearly all applications. However, it should be pointed out that pulse-width modulators also introduce sampling of the waveform. Although the analog input signal $v_c(t)$ is a continuous function of time, there can be only one discrete value of the duty cycle during every switching period. Therefore, the pulse-width modulator samples the waveform, with sampling rate equal to the switching frequency f_s. Hence, a more accurate modulator block diagram is as in Fig. 7.66 [10]. In practice, this sampling restricts the useful frequencies of the ac variations to values much less than the switching frequency. The designer must ensure that the bandwidth of the control system be sufficiently less than the Nyquist rate $f_s/2$.

Significant high-frequency variations in the control signal $v_c(t)$ can also alter the behavior of the pulse-width modulator. A common example is when $v_c(t)$ contains switching ripple, introduced by the feedback loop. This phenomenon has been analyzed by several authors [10,19], and effects of inductor current ripple on the transfer functions of current-programmed converters are investigated in Chapter 12. But it is generally best to avoid the case where $v_c(t)$ contains significant components at the switching frequency or higher, since the pulse-width modulators of such systems exhibit poor noise immunity.

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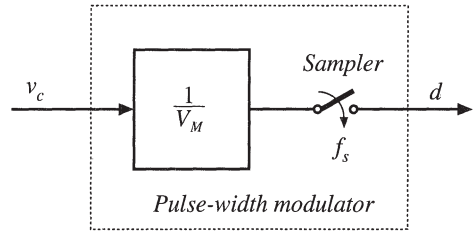


Fig. 7.66 A more accurate pulse-width modulator model, including sampling.

7.7 SUMMARY OF KEY POINTS

1. The CCM converter analytical techniques of Chapters 2 and 3 can be extended to predict converter ac behavior. The key step is to average the converter waveforms over one switching period. This removes the switching harmonics, thereby exposing directly the desired dc and low-frequency ac components of the waveforms. In particular, expressions for the averaged inductor voltages, capacitor currents, and converter input current are usually found.

2. Since switching converters are nonlinear systems, it is desirable to construct small-signal linearized models. This is accomplished by perturbing and linearizing the averaged model about a quiescent operating point.

3. Ac equivalent circuits can be constructed, in the same manner used in Chapter 3 to construct dc equivalent circuits. If desired, the ac equivalent circuits may be refined to account for the effects of converter losses and other nonidealities.

4. The state-space averaging method of Section 7.3 is essentially the same as the basic approach of Section 7.2, except that the formality of the state-space network description is used. The general results are listed in Section 7.3.2.

5. The circuit averaging technique also yields equivalent results, but the derivation involves manipulation of circuits rather than equations. Switching elements are replaced by dependent voltage and current sources, whose waveforms are defined to be identical to the switch waveforms of the actual circuit. This leads to a circuit having a time-invariant topology. The waveforms are then averaged to remove the switching ripple, and perturbed and linearized about a quiescent operating point to obtain a small-signal model.

6. When the switches are the only time-varying elements in the converter, then circuit averaging affects only the switch network. The converter model can then be derived by simply replacing the switch network with its averaged model. Dc and small-signal ac models of several common CCM switch networks are listed in Section 7.4.4. Conduction and switching losses can also be modeled using this approach.

7. The canonical circuit describes the basic properties shared by all dc–dc PWM converters operating in the continuous conduction mode. At the heart of the model is the ideal 1:$M(D)$ transformer, introduced in Chapter 3 to represent the basic dc–dc conversion function, and generalized here to include ac variations. The converter reactive elements introduce an effective low-pass filter into the network. The model also includes independent sources that represent the effect of duty cycle variations. The parameter values in the canonical models of several basic converters are tabulated for easy reference.

8. The conventional pulse-width modulator circuit has linear gain, dependent on the slope of the sawtooth waveform, or equivalently on its peak-to-peak magnitude.

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REFERENCES

[1] R. D. MIDDLEBROOK and SLOBODAN ĆUK, "A General Unified Approach to Modeling Switching-Converter Power Stages," *International Journal of Electronics*, Vol. 42, No. 6, pp. 521-550, June 1977.

[2] SLOBODAN ĆUK, "Modeling, Analysis, and Design of Switching Converters," Ph.D. thesis, California Institute of Technology, November 1976.

[3] R. D. MIDDLEBROOK AND SLOBODAN ĆUK, "Modeling and Analysis Methods for Dc-to-Dc Switching Converters," *Proceedings of the IEEE International Semiconductor Power Converter Conference*, 1977 Record, pp. 90-111, March 1977. Reprinted in *Advances in Switched-Mode Power Conversion*, Vol. 1, Irvine: Teslaco, 1983.

[4] G. W. WESTER and R. D. MIDDLEBROOK, "Low-Frequency Characterization of Switched Dc-Dc Converters," *IEEE Transactions an Aerospace and Electronic Systems*, Vol. AES-9, pp. 376-385, May 1973.

[5] DANIEL M. MITCHELL, *Dc–Dc Switching Regulator Analysis*, New York: McGraw-Hill, 1988.

[6] SETH R. SANDERS and GEORGE C. VERGESE, "Synthesis of Averaged Circuit Models for Switched Power Converters," *IEEE Transactions on Circuits and Systems*, Vol. 38, No. 8, pp. 905-915, August 1991.

[7] P. T. KREIN, J. BENTSMAN, R. M. BASS, and B. C. LESIEUTRE, "On the Use of Averaging for the Analysis of Power Electronic Systems," *IEEE Transactions on Power Electronics*, Vol. 5, No. 2, pp. 182-190, April 1990.

[8] B. LEHMAN and R. M. BASS, "Switching Frequency Dependent Averaged Models for PWM DC-DC Converters," *IEEE Transactions on Power Electronics*, Vol. 11, No. 1, pp. 89-98, January 1996.

[9] R. M. BASS and J. SUN, "Averaging Under Large-Ripple Conditions," *IEEE Power Electronics Specialists Conference*, 1998 Record, pp. 630-632, May 1998.

[10] ARTHUR R. BROWN and R. D. MIDDLEBROOK, "Sampled-Data Modeling of Switching Regulators," *IEEE Power Electronics Specialists Conference*, 1981 Record, pp. 349-369, June 1981.

[11] R. D. MIDDLEBROOK, "Predicting Modulator Phase Lag in PWM Converter Feedback Loops," *Proceedings of the Eighth National Solid-State Power Conversion Conference* (Powercon 8), April 1981.

[12] A. KISLOVSKI, R. REDL, AND N. SOKAL, *Dynamic Analysis of Switching-Mode DC/DC Converters*, New York: Van Nostrand Reinhold, 1994.

[13] R. TYMERSKI and V. VORPERIAN, "Generation, Classification and Analysis of Switched-Mode DC-to-DC Converters by the Use of Converter Cells," *Proceedings of the 1986 International Telecommunications Energy Conference* (INTELEC'86), pp. 181-195, October 1986.

[14] V. VORPERIAN, R. TYMERSKI, and F. C. LEE, "Equivalent Circuit Models for Resonant and PWM Switches," *IEEE Transactions on Power Electronics*, Vol. 4, No. 2, pp. 205-214, April 1989.

[15] V. VORPERIAN, "Simplified Analysis of PWM Converters Using the Model of the PWM Switch: Parts I and II," *IEEE Transactions on Aerospace and Electronic Systems*, Vol. AES-26, pp. 490-505, May 1990.

[16] S. FREELAND and R. D. MIDDLEBROOK, "A Unified Analysis of Converters with Resonant Switches," *IEEE Power Electronics Specialists Conference*, 1987 Record, pp. 20-30.

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[17] ARTHUR WITULSKI and ROBERT ERICKSON, "Extension of State-Space Averaging to Resonant Switches —and Beyond," *IEEE Transactions on Power Electronics*, Vol. 5, No. 1, pp. 98-109, January 1990.

[18] D. MAKSIMOVIĆ and S. ĆUK, "A Unified Analysis of PWM Converters in Discontinuous Modes," *IEEE Transactions on Power Electronics*, Vol. 6, No. 3, pp. 476-490, July 1991.

[19] D. J. SHORTT and F. C. LEE, "Extensions of the Discrete-Average Models for Converter Power Stages," *IEEE Power Electronics Specialists Conference*, 1983 Record, pp. 23-37, June 1983.

[20] O. AL-NASEEM and R.W. ERICKSON, "Prediction of Switching Loss Variations by Averaged Switch Modeling," *IEEE Applied Power Electronics Conference*, 2000 Record, pp. 242-248, February 2000.

PROBLEMS

7.1 An ideal boost converter operates in the continuous conduction mode.

(a) Determine the nonlinear averaged equations of this converter.

(b) Now construct a small-signal ac model. Let

$$\begin{aligned} \left\langle v_g(t) \right\rangle_{T_s} &= V_g + \hat{v}_g(t) \\ d(t) &= D + \hat{d}(t) \\ \left\langle i(t) \right\rangle_{T_s} &= I + \hat{i}(t) \\ \left\langle v(t) \right\rangle_{T_s} &= V + \hat{v}(t) \end{aligned}$$

where V_g, D, I, and V are steady-state dc values; $\hat{v}_g(t)$ and $\hat{d}(t)$ are small ac variations in the power and control inputs; and $\hat{i}(t)$ and $\hat{v}(t)$ are the resulting small ac variations in the inductor current and output voltage, respectively. Show that the following model results:

Large-signal dc components

$$\begin{aligned} 0 &= -D'V + V_g \\ 0 &= D'I - \frac{V}{R} \end{aligned}$$

Small-signal ac components

$$\begin{aligned} L\frac{d\hat{i}(t)}{dt} &= -D'\hat{v}(t) + V\hat{d}(t) + \hat{v}_g(t) \\ C\frac{d\hat{v}(t)}{dt} &= D'\hat{i}(t) - I\hat{d}(t) - \frac{\hat{v}(t)}{R} \end{aligned}$$

7.2 Construct an equivalent circuit that corresponds to the boost converter small-signal ac equations derived in Problem 7.1(b).

7.3 Manipulate your boost converter equivalent circuit of Problem 7.2 into canonical form. Explain each step in your derivation. Verify that the elements in your canonical model agree with Table 7.1.

7.4 The ideal current-fed bridge converter of Fig. 2.31 operates in the continuous conduction mode.

(a) Determine the nonlinear averaged equations of this converter.

(b) Perturb and linearize these equations, to determine the small-signal ac equations of the converter.

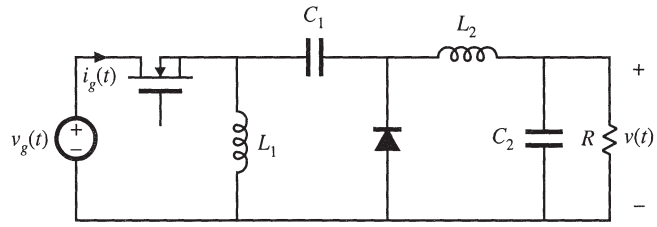


Fig. 7.67 Inverse SEPIC, Problem 7.7.

(c) Construct a small-signal ac equivalent circuit model for this converter.

7.5 Construct a complete small-signal ac equivalent circuit model for the flyback converter shown in Fig. 7.18, operating in continuous conduction mode. The transformer contains magnetizing inductance L, referred to the primary. In addition, the transformer exhibits significant core loss, which can be modeled by a resistor R_C in parallel with the primary winding. All other elements are ideal. You may use any valid method to solve this problem. Your model should correctly predict variations in $i_g(t)$.

7.6 Modeling the Ćuk converter. You may use any valid method to solve this problem.

(a) Derive the small-signal dynamic equations that model the ideal Ćuk converter.

(b) Construct a complete small-signal equivalent circuit model for the Ćuk converter.

7.7 Modeling the inverse-SEPIC. You may use any valid method to solve this problem.

(a) Derive the small-signal dynamic equations that model the converter shown in Fig. 7.67.

(b) Construct a complete small-signal equivalent circuit model for the inverse-SEPIC.

7.8 Consider the nonideal buck converter of Fig. 7.68. The input voltage source $v_g(t)$ has internal resistance R_g. Other component nonidealities may be neglected.

(a) Using the state-space averaging method, determine the small-signal ac equations that describe variations in i, v, and i_g, which occur owing to variations in the transistor duty cycle d and input voltage v_g.

(b) Construct an ac equivalent circuit model corresponding to your equations of part (a).

(c) Solve your model to determine an expression for the small-signal control-to-output transfer function.

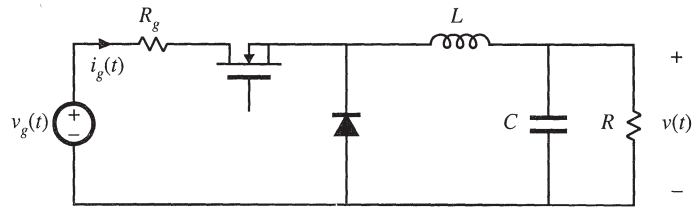


Fig. 7.68 Nonideal buck converter, Problem 7.8.

7.9 Use the circuit-averaging technique to derive the dc and small-signal ac equivalent circuit of the buck converter with input filter, illustrated in Fig. 2.32. All elements are ideal.

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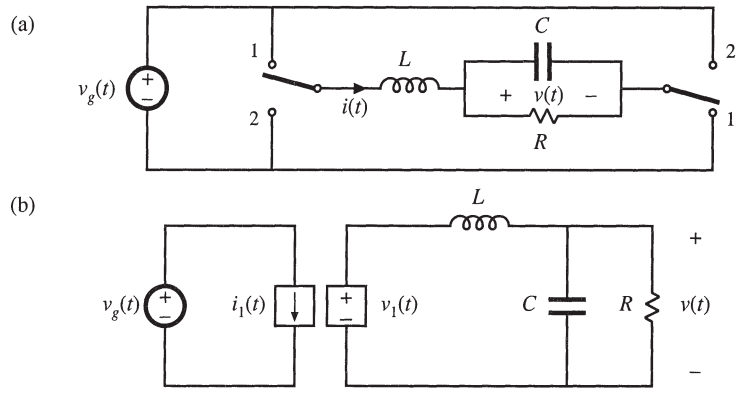


Fig. 7.69 Bridge inverter, Problem 7.11: (a) circuit, (b) large-signal averaged model.

7.10 A flyback converter operates in the continuous conduction mode. The MOSFET switch has on-resistance R_{on}, and the secondary-side diode has a constant forward voltage drop V_D. The flyback transformer has primary winding resistance R_p and secondary winding resistance R_s.

(a) Derive the small-signal ac equations for this converter.

(b) Derive a complete small-signal ac equivalent circuit model, which is valid in the continuous conduction mode and which correctly models the above losses, as well as the converter input and output ports.

7.11 Circuit averaging of the bridge inverter circuit of Fig. 7.69(a).

(a) Show that the converter of Fig. 7.69(a) can be written in the electrically identical form shown in Fig. 7.69(b). Sketch the waveforms $i_1(t)$ and $v_1(t)$.

(b) Use the circuit-averaging method to derive a large-signal averaged model for this converter.

(c) Perturb and linearize your circuit model of part (b), to obtain a single equivalent circuit that models dc and small-signal ac signals in the bridge inverter.

7.12 Use the circuit averaging method to derive an equivalent circuit that models dc and small-signal ac signals in the buck-boost converter. You may assume that the converter operates in the continuous conduction mode, and that all elements are ideal.

(a) Give a time-invariant electrically identical circuit, in which the switching elements are replaced by equivalent voltage and current sources. Define the waveforms of the sources.

(b) Derive a large-signal averaged model for this converter.

(c) Perturb and linearize your circuit model of part (b), to obtain a single equivalent circuit that models dc and small-signal ac signals in the buck-boost converter.

7.13 The two-output flyback converter of Fig. 7.70(a) operates in the continuous conduction mode. It may be assumed that the converter is lossless.

(a) Derive a small-signal ac equivalent circuit for this converter.

(b) Show that the small-signal ac equivalent circuit for this two-output converter can be written in the generalized canonical form of Fig. 7.70(b). Give analytical expressions for the generators $e(s)$ and $j(s)$.

7.14 A pulse-width modulator circuit is constructed in which the sawtooth-wave generator is replaced by a triangle-wave generator, as illustrated in Fig. 7.71(a). The triangle waveform is illustrated in Fig. 7.71(b).

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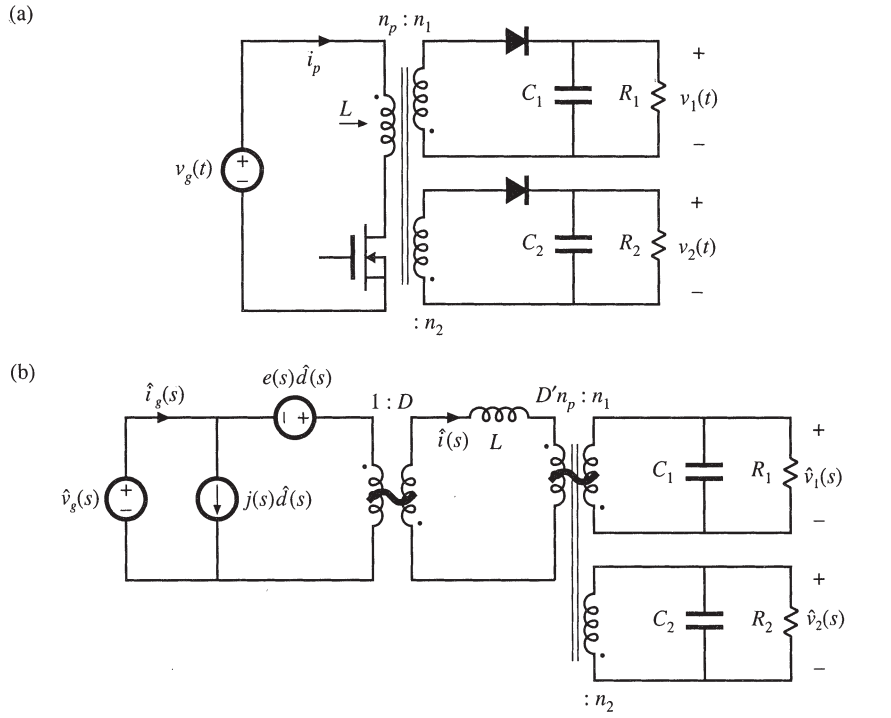


Fig. 7.70 Two-output flyback converter, Problem 7.13: (a) converter circuit, (b) small-signal ac equivalent circuit.

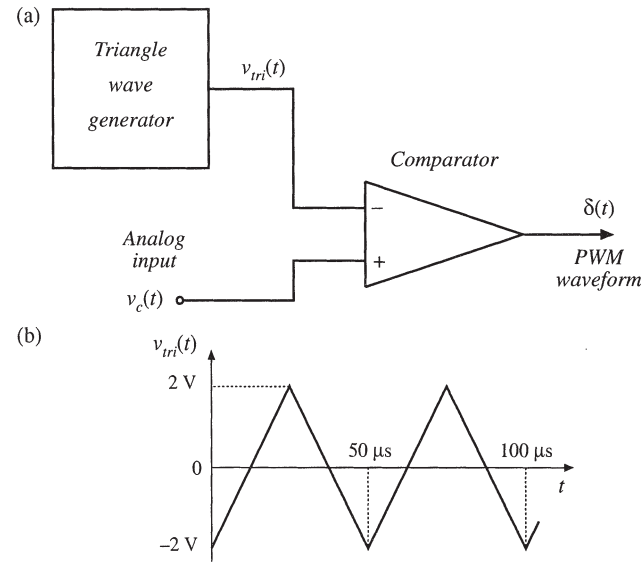


Fig. 7.71 Pulse-width modulator, Problem 7.14.

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(a) Determine the converter switching frequency, in Hz.

(b) Determine the gain $d(t)/v_c(t)$ for this circuit.

(c) Over what range of v_c is your answer to (b) valid?

7.15 Use the averaged switch modeling technique to derive an ac equivalent circuit model for the buck-boost converter of Fig. 7.31:

(a) Replace the switches in Fig. 7.31 with the averaged switch model given in Fig. 7.50(c).

(b) Compare your result with the model given in Fig. 7.16(b). Show that the two models predict the same small-signal line-to-output transfer function $G_{vg}(s) = \hat{v}/\hat{v}_g$.

7.16 Modify the CCM dc and small-signal ac averaged switch models of Fig. 7.50, to account for MOSFET on-resistance R_{on} and diode forward voltage drop V_D.

7.17 Use the averaged switch modeling technique to derive a dc and ac equivalent circuit model for the flyback converter of Fig. 7.18. You can neglect all losses and the transformer leakage inductances.

(a) Define a switch network containing the transistor Q_1 and the diode D_1 as in Fig. 7.39(a). Derive a large-signal averaged switch model of the switch network. The model should account for the transformer turns ratio n.

(b) Perturb and linearize the model you derived in part (a) to obtain the dc and ac small-signal averaged switch model. Verify that for $n = 1$ your model reduces to the model shown in Fig. 7.39(d).

(c) Using the averaged switch model you derived in part (b), sketch a complete dc and small-signal ac model of the flyback converter. Solve the model for the steady-state conversion ratio $M(D) = V/V_g$.

(d) The averaged switch models you derived in parts (a) and (b) could be used in other converters having an isolation transformer. Which ones?

7.18 In the flyback converter of Fig. 7.18, the transistor on-resistance is R_{on}, and the diode forward voltage drop is V_D. Other losses and the transformer leakage inductances can be neglected. Derive a dc and small-signal ac averaged switch model for the switch network containing the transistor Q_1 and the diode D_1. The model should account for the on-resistance R_{on}, the diode forward voltage drop V_D, and the transformer turns ratio n.

7.19 In the boost converter of Fig. 7.72(a), the $v_1(t)$ and $i_2(t)$ waveforms of Fig. 7.72(b) are observed. During the transistor turn-on transition, a reverse current flows through the diode which removes the diode stored charge. As illustrated in Fig. 7.72(b), the reverse current spike has area $-Q_r$ and duration t_r. The inductor winding has resistance R_L. You may neglect all losses other than the switching loss due to the diode stored charge and the conduction loss due to the inductor winding resistance.

(a) Derive an averaged switch model for the boost switch network in Fig. 7.72(a).

(b) Use your result of part (a) to sketch a dc equivalent circuit model for the boost converter.

(c) The diode stored charge can be expressed as a function of the current I_1 as:

$$Q_r = k_q \sqrt{I_1}$$

while the reverse recovery time t_r is approximately constant. Given $V_g = 100$ V, $D = 0.5$, $f_s = 100$ kHz, $k_q = 100$ nC/A$^{1/2}$, $t_r = 100$ ns, $R_L = 0.1\ \Omega$, use a dc sweep simulation to plot the converter efficiency as a function of the load current I_{LOAD} in the range:

$$1 \text{ A} \le I_{LOAD} \le 10 \text{ A}$$

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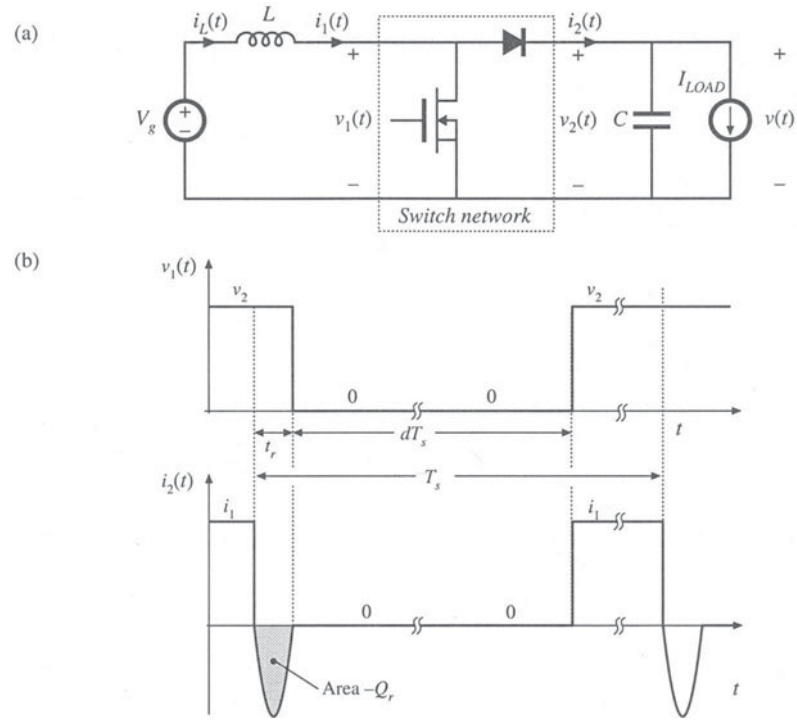


Fig. 7.72 Boost converter and waveforms illustrating reverse recovery of the diode. Averaged switch modeling in this converter is addressed in Problem 7.19.

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8

Converter Transfer Functions

The engineering design process is comprised of several major steps:

1. *Specifications and other design goals* are defined.
2. *A circuit is proposed.* This is a creative process that draws on the physical insight and experience of the engineer.
3. *The circuit is modeled.* The converter power stage is modeled as described in Chapter 7. Components and other portions of the system are modeled as appropriate, often with vendor-supplied data.
4. *Design-oriented analysis* of the circuit is performed. This involves development of equations that allow element values to be chosen such that specifications and design goals are met. In addition, it may be necessary for the engineer to gain additional understanding and physical insight into the circuit behavior, so that the design can be improved by adding elements to the circuit or by changing circuit connections.
5. *Model verification.* Predictions of the model are compared to a laboratory prototype, under nominal operating conditions. The model is refined as necessary, so that the model predictions agree with laboratory measurements.
6. *Worst-case analysis* (or other reliability and production yield analysis) of the circuit is performed. This involves quantitative evaluation of the model performance, to judge whether specifications are met under all conditions. Computer simulation is well-suited to this task.
7. *Iteration.* The above steps are repeated to improve the design until the worst-case behavior meets specifications, or until the reliability and production yield are acceptably high.

This chapter covers techniques of design-oriented analysis, measurement of experimental transfer functions, and computer simulation, as needed in steps 4, 5, and 6.

Sections 8.1 to 8.3 discuss techniques for analysis and construction of the Bode plots of the converter transfer functions, input impedance, and output impedance predicted by the equivalent circuit

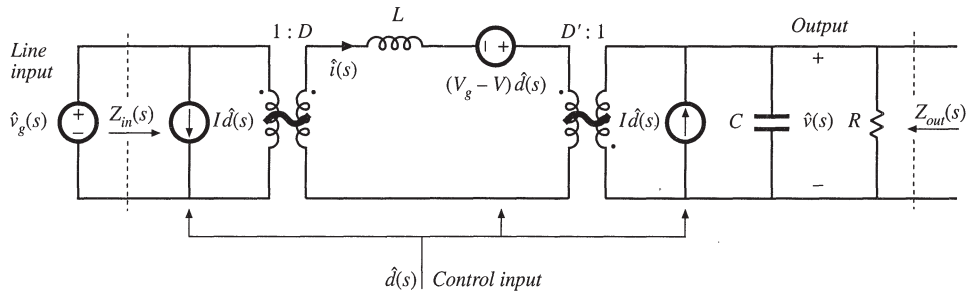


Fig. 8.1 Small-signal equivalent circuit model of the buck-boost converter, as derived in Chapter 7.

models of Chapter 7. For example, the small-signal equivalent circuit model of the buck-boost converter is illustrated in Fig. 7.17(c). This model is reproduced in Fig. 8.1, with the important inputs and terminal impedances identified. The line-to-output transfer function $G_{vg}(s)$ is found by setting duty cycle variations $\hat{d}(s)$ to zero, and then solving for the transfer function from $\hat{v}_g(s)$ to $\hat{v}(s)$:

$$G_{vg}(s) = \left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\hat{d}(s)=0} \tag{8.1}$$

This transfer function describes how variations or disturbances in the applied input voltage $v_g(t)$ lead to disturbances in the output voltage $v(t)$. It is important in design of an output voltage regulator. For example, in an off-line power supply, the converter input voltage $v_g(t)$ contains undesired even harmonics of the ac power line voltage. The transfer function $G_{vg}(s)$ is used to determine the effect of these harmonics on the converter output voltage $v(t)$.

The control-to-output transfer function $G_{vd}(s)$ is found by setting the input voltage variations $\hat{v}_g(s)$ to zero, and then solving the equivalent circuit model for $\hat{v}(s)$ as a function of $\hat{d}(s)$:

$$G_{vd}(s) = \left. \frac{\hat{v}(s)}{\hat{d}(s)} \right|_{\hat{v}_g(s)=0} \tag{8.2}$$

This transfer function describes how control input variations $\hat{d}(s)$ influence the output voltage $\hat{v}(s)$. In an output voltage regulator system, $G_{vd}(s)$ is a key component of the loop gain and has a significant effect on regulator performance.

The output impedance $Z_{out}(s)$ is found under the conditions that $\hat{v}_g(s)$ and $\hat{d}(s)$ variations are set to zero. $Z_{out}(s)$ describes how variations in the load current affect the output voltage. This quantity is also important in voltage regulator design. It may be appropriate to define $Z_{out}(s)$ either including or not including the load resistance R.

The converter input impedance $Z_{in}(s)$ plays a significant role when an electromagnetic interference (EMI) filter is added at the converter power input. The relative magnitudes of Z_{in} and the EMI filter output impedance influence whether the EMI filter disrupts the transfer function $G_{vd}(s)$. Design of input EMI filters is the subject of Chapter 10.

An objective of this chapter is the construction of Bode plots of the important transfer functions and terminal impedances of switching converters. For example, Fig. 8.2 illustrates the magnitude and phase plots of $G_{vd}(s)$ for the buck-boost converter model of Fig. 8.1. Rules for construction of magnitude and phase asymptotes are reviewed in Section 8.1, including two types of features that often appear in

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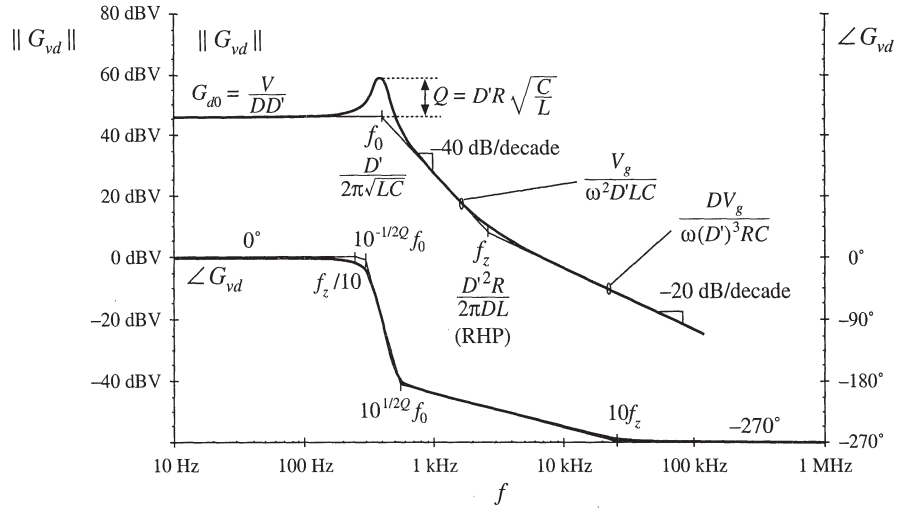


Fig. 8.2 Bode plot of control-to-output transfer function predicted by the model of Fig. 8.1, with analytical expressions for the important features.

converter transfer functions: resonances and right half-plane zeroes. Bode diagrams of the small-signal transfer functions of the buck-boost converter are derived in detail in Section 8.2, and the transfer functions of the basic buck, boost, and buck-boost converters are tabulated. The physical origins of the right half-plane zero are also described.

A difficulty usually encountered in circuit analysis (step 5 of the above list) is the complexity of the circuit model: practical circuits may contains hundreds of elements, and hence their analysis may leads to complicated derivations, intractable equations, and lots of algebra mistakes. *Design-oriented analysis*[1] is a collection of tools and techniques that can alleviate these problems. Some tools for approaching the design of a complicated converter system are described in this chapter. Writing the transfer functions in normalized form directly exposes the important features of the response. Analytical expressions for these features, as well as for the asymptotes, lead to simple equations that are useful in design. Well-separated roots of transfer function polynomials can be approximated in a simple way. Section 8.3 describes a graphical method for constructing Bode plots of transfer functions and impedances, essentially by inspection. This method can: (1) reduce the amount of algebra and associated algebra mistakes; (2) lead to greater insight into circuit behavior, which can be applied to design the circuit; and (3) lead to the insight necessary to make suitable approximations that render the equations tractable.

Experimental measurement of transfer functions and impedances (needed in step 4, model verification) is discussed in Section 8.5. Use of computer simulation to plot converter transfer functions (as needed in step 6, worst-case analysis) is covered in Appendix B.

8.1 REVIEW OF BODE PLOTS

A Bode plot is a plot of the magnitude and phase of a transfer function or other complex-valued quantity, vs. frequency. Magnitude in decibels, and phase in degrees, are plotted vs. frequency, using semilogarithmic axes. The magnitude plot is effectively a log-log plot, since the magnitude is expressed in decibels and the frequency axis is logarithmic.

The magnitude of a dimensionless quantity G can be expressed in decibels as follows:

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$$\| G \|_{\text{dB}} = 20 \log_{10}\left(\| G \| \right) \tag{8.3}$$

Decibel values of some simple magnitudes are listed in Table 8.1. Care must be used when the magnitude is not dimensionless. Since it is not proper to take the logarithm of a quantity having dimensions, the magnitude must first be normalized. For example, to express the magnitude of an impedance Z in decibels, we should normalize by dividing by a base impedance R_{base}:

Table 8.1 Expressing magnitudes in decibels

Actual magnitude	Magnitude in dB
1/2	– 6 dB
1	0 dB
2	6 dB
5 = 10/2	20 dB – 6 dB = 14 dB
10	20 dB
$1000 = 10^3$	3·20 dB = 60 dB

$$\| Z \|_{\text{dB}} = 20 \log_{10}\left(\frac{\| Z \|}{R_{base}} \right) \tag{8.4}$$

The value of R_{base} is arbitrary, but we need to tell others what value we have used. So if $\| Z \|$ is 5 Ω, and we choose R_{base} = 10 Ω, then we can say that $\| Z \|_{\text{dB}} = 20 \log_{10}(5\ \Omega/10\Omega) = -6$dB with respect to 10 Ω. A common choice is R_{base} = 1Ω; decibel impedances expressed with R_{base} = 1 Ω are said to be expressed in dBΩ. So 5 Ω is equivalent to 14 dBΩ. Current switching harmonics at the input port of a converter are often expressed in dBμA, or dB using a base current of 1 μA: 60 dBμA is equivalent to 1000 μA, or 1 mA.

The magnitude Bode plots of functions equal to powers of f are linear. For example, suppose that the magnitude of a dimensionless quantity $G(f)$ is

$$\| G \| = \left(\frac{f}{f_0} \right)^n \tag{8.5}$$

where f_0 and n are constants. The magnitude in decibels is

$$\| G \|_{\text{dB}} = 20 \log_{10}\left(\frac{f}{f_0} \right)^n = 20n \log_{10}\left(\frac{f}{f_0} \right) \tag{8.6}$$

This equation is plotted in Fig. 8.3, for several values of n. The magnitudes have value 1 ⇒ 0 dB at frequency $f = f_0$. They are linear functions of $\log_{10}(f)$. The slope is the change in $\| G \|_{\text{dB}}$ arising from a unit change in $\log_{10}(f)$; a unit increase in $\log_{10}(f)$ corresponds to a factor of 10, or decade, increase in f. From Eq. (8.6), a decade increase in f leads to an increase in $\| G \|_{\text{dB}}$ of $20n$ dB. Hence, the slope is $20n$ dB per decade. Equivalently, we can say that the slope is $20n \log_{10}(2) \approx 6n$ dB per octave, where an octave is a factor of 2 change in frequency. In practice, the magnitudes of most frequency-dependent functions can usually be approximated over a limited range of frequencies by functions of the form (8.5); over this range of frequencies, the magnitude Bode plot is approximately linear with slope $20n$ dB/decade.

A simple transfer function whose magnitude is of the form (8.5) is the *pole at the origin*:

$$G(s) = \frac{1}{\left(\frac{s}{\omega_0} \right)} \tag{8.7}$$

The magnitude is

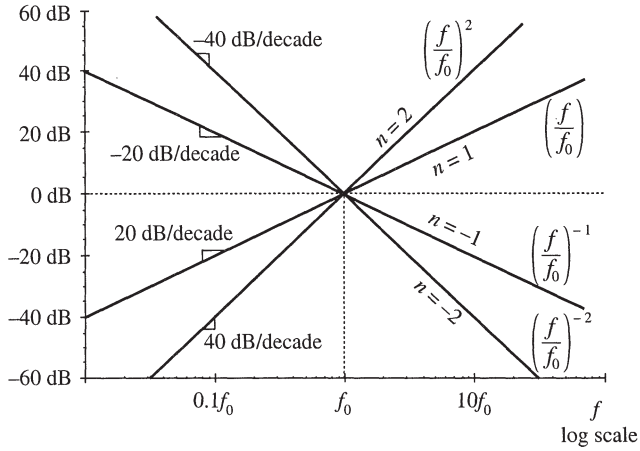


Fig. 8.3 Magnitude Bode plots of functions which vary as f^n are linear, with slope n dB per decade.

$$\left\| G(j\omega) \right\| = \frac{1}{\left\| \frac{j\omega}{\omega_0} \right\|} = \frac{1}{\left(\frac{\omega}{\omega_0}\right)} \tag{8.8}$$

If we define $f = \omega/2\pi$ and $f_0 = \omega_0/2\pi$, then Eq. (8.8) becomes

$$\left\| G \right\| = \left(\frac{f}{f_0}\right)^{-1} \tag{8.9}$$

which is of the form of Eq. (8.5) with $n = -1$. As illustrated in Fig. 8.3, the magnitude Bode plot of the pole at the origin (8.7) has a –20 dB per decade slope, and passes through 0 dB at frequency $f = f_0$.

8.1.1 Single Pole Response

Consider the simple *R-C* low-pass filter illustrated in Fig. 8.4. The transfer function is given by the voltage divider ratio

$$G(s) = \frac{v_2(s)}{v_1(s)} = \frac{\frac{1}{sC}}{\frac{1}{sC} + R} \tag{8.10}$$

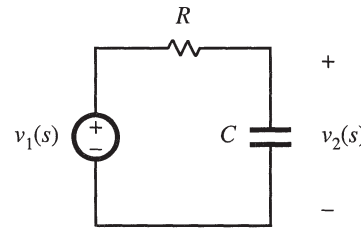


Fig. 8.4 Simple *R–C* low-pass filter example.

This transfer function is a ratio of voltages, and hence is dimensionless. By multiplying the numerator and denominator by sC, we can express the transfer function as a rational fraction:

$$G(s) = \frac{1}{1 + sRC} \tag{8.11}$$

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The transfer function now coincides with the following standard normalized form for a single pole:

$$G(s) = \frac{1}{\left(1 + \frac{s}{\omega_0}\right)} \tag{8.12}$$

The parameter $\omega_0 = 2\pi f_0$ is found by equating the coefficients of s in the denominators of Eqs. (8.11) and (8.12). The result is

$$\omega_0 = \frac{1}{RC} \tag{8.13}$$

Since R and C are real positive quantities, ω_0 is also real and positive. The denominator of Eq. (8.12) contains a root at $s = -\omega_0$, and hence $G(s)$ contains a real pole in the left half of the complex plane.

To find the magnitude and phase of the transfer function, we let $s = j\omega$, where j is the square root of -1. We then find the magnitude and phase of the resulting complex-valued function. With $s = j\omega$, Eq. (8.12) becomes

$$G(j\omega) = \frac{1}{\left(1 + j\frac{\omega}{\omega_0}\right)} = \frac{1 - j\frac{\omega}{\omega_0}}{1 + \left(\frac{\omega}{\omega_0}\right)^2} \tag{8.14}$$

The complex-valued $G(j\omega)$ is illustrated in Fig. 8.5, for one value of ω. The magnitude is

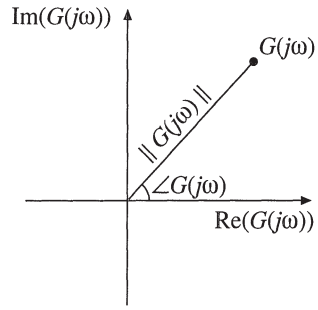


Fig. 8.5 Magnitude and phase of the complex-valued function $G(j\omega)$.

$$\left\| G(j\omega) \right\| = \sqrt{\left[\mathrm{Re}\,(G(j\omega))\right]^2 + \left[\mathrm{Im}\,(G(j\omega))\right]^2} = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2}} \tag{8.15}$$

Here, we have assumed that ω_0 is real. In decibels, the magnitude is

$$\left\| G(j\omega) \right\|_{\mathrm{dB}} = -20 \log_{10}\left(\sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2}\right) \text{ dB} \tag{8.16}$$

The easy way to sketch the magnitude Bode plot of G is to investigate the asymptotic behavior for large and small frequency.

For small frequency, $\omega \ll \omega_0$ and $f \ll f_0$, it is true that

$$\left(\frac{\omega}{\omega_0}\right) \ll 1 \tag{8.17}$$

The $(\omega/\omega_0)^2$ term of Eq. (8.15) is therefore much smaller than 1, and hence Eq. (8.15) becomes

$$\left\| G(j\omega) \right\| \approx \frac{1}{\sqrt{1}} = 1 \tag{8.18}$$

In decibels, the magnitude is approximately

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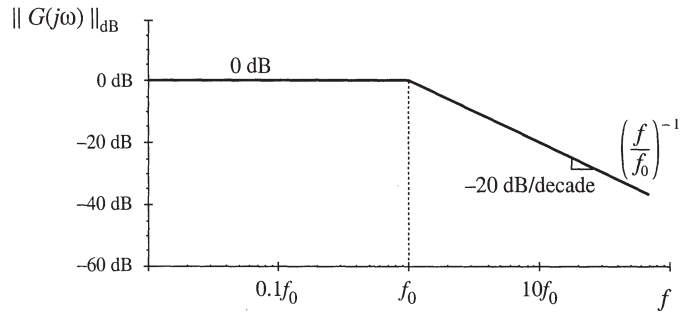


Fig. 8.6 Magnitude asymptotes for the single real pole transfer function.

$$\| G(j\omega) \|_{\text{dB}} \approx 0\text{dB} \tag{8.19}$$

Thus, as illustrated in Fig. 8.6, at low frequency $\| G(j\omega) \|_{\text{dB}}$ is asymptotic to 0 dB.

At high frequency, $\omega \gg \omega_0$ and $f \gg f_0$. In this case, it is true that

$$\left(\frac{\omega}{\omega_0}\right) \gg 1 \tag{8.20}$$

We can then say that

$$1 + \left(\frac{\omega}{\omega_0}\right)^2 \approx \left(\frac{\omega}{\omega_0}\right)^2 \tag{8.21}$$

Hence, Eq. (8.15) now becomes

$$\| G(j\omega) \| \approx \frac{1}{\sqrt{\left(\frac{\omega}{\omega_0}\right)^2}} = \left(\frac{f}{f_0}\right)^{-1} \tag{8.22}$$

This expression coincides with Eq. (8.5), with $n = -1$. So at high frequency, $\| G(j\omega) \|_{\text{dB}}$ has slope –20 dB per decade, as illustrated in Fig. 8.6. Thus, the asymptotes of $\| G(j\omega) \|$ are equal to 1 at low frequency, and $(f/f_0)^{-1}$ at high frequency. The asymptotes intersect at f_0. The actual magnitude tends toward these asymptotes at very low frequency and very high frequency. In the vicinity of the corner frequency f_0, the actual curve deviates somewhat from the asymptotes.

The deviation of the exact curve from the asymptotes can be found by simply evaluating Eq. (8.15). At the corner frequency $f = f_0$, Eq. (8.15) becomes

$$\| G(j\omega_0) \| = \frac{1}{\sqrt{1 + \left(\frac{\omega_0}{\omega_0}\right)^2}} = \frac{1}{\sqrt{2}} \tag{8.23}$$

In decibels, the magnitude is

$$\| G(j\omega_0) \|_{\text{dB}} = -20 \log_{10} \left(\sqrt{1 + \left(\frac{\omega_0}{\omega_0}\right)^2} \right) \approx -3 \text{ dB} \tag{8.24}$$

So the actual curve deviates from the asymptotes by –3 dB at the corner frequency, as illustrated in Fig. 8.7. Similar arguments show that the actual curve deviates from the asymptotes by –1 dB at $f = f_0/2$

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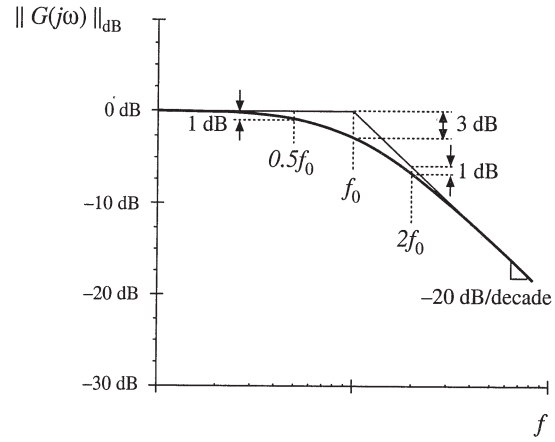


Fig. 8.7 Deviation of the actual curve from the asymptotes, real pole.

and at $f = 2f_0$.

The phase of $G(j\omega)$ is

$$\angle G(j\omega) = \tan^{-1}\left(\frac{\mathrm{Im}\left(G(j\omega)\right)}{\mathrm{Re}\left(G(j\omega)\right)}\right) \tag{8.25}$$

Insertion of the real and imaginary parts of Eq. (8.14) into Eq. (8.25) leads to

$$\angle G(j\omega) = -\tan^{-1}\left(\frac{\omega}{\omega_0}\right) \tag{8.26}$$

This function is plotted in Fig. 8.8. It tends to 0° at low frequency, and to –90° at high frequency. At the corner frequency $f = f_0$, the phase is –45°.

Since the high-frequency and low-frequency phase asymptotes do not intersect, we need a third asymptote to approximate the phase in the vicinity of the corner frequency f_0. One way to do this is illus-

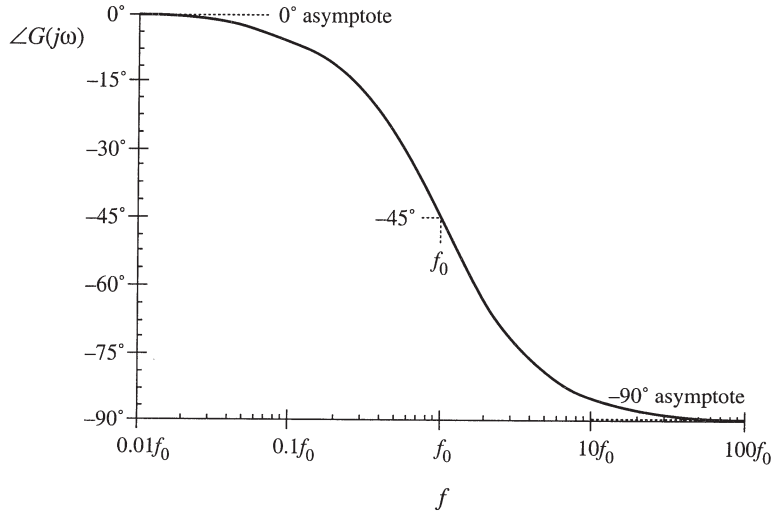


Fig. 8.8 Exact phase plot, single real pole.

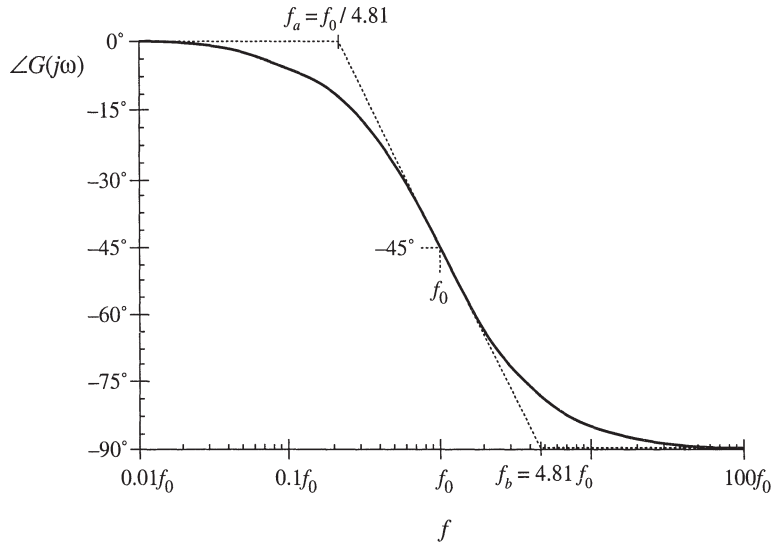


Fig. 8.9 One choice for the midfrequency phase asymptote, which correctly predicts the actual slope at $f = f_0$.

trated in Fig. 8.9, where the slope of the asymptote is chosen to be identical to the slope of the actual curve at $f = f_0$. It can be shown that, with this choice, the asymptote intersection frequencies f_a and f_b are given by

$$f_a = f_0 e^{-\pi/2} \approx \frac{f_0}{4.81}$$
$$f_b = f_0 e^{\pi/2} \approx 4.81\, f_0 \tag{8.27}$$

A simpler choice, which better approximates the actual curve, is

$$f_a = \frac{f_0}{10}$$
$$f_b = 10 f_0 \tag{8.28}$$

This asymptote is compared to the actual curve in Fig. 8.10. The pole causes the phase to change over a frequency span of approximately two decades, centered at the corner frequency. The slope of the asymptote in this frequency span is –45° per decade. At the break frequencies f_a and f_b, the actual phase deviates from the asymptotes by $\tan^{-1}(0.1) = 5.7°$.

The magnitude and phase asymptotes for the single-pole response are summarized in Fig. 8.11.

It is good practice to consistently express single-pole transfer functions in the normalized form of Eq. (8.12). Both terms in the denominator of Eq. (8.12) are dimensionless, and the coefficient of s^0 is unity. Equation (8.12) is easy to interpret, because of its normalized form. At low frequencies, where the (s/ω_0) term is small in magnitude, the transfer function is approximately equal to 1. At high frequencies, where the (s/ω_0) term has magnitude much greater than 1, the transfer function is approximately $(s/\omega_0)^{-1}$. This leads to a magnitude of $(f/f_0)^{-1}$. The corner frequency is $f_0 = \omega_0/2\pi$. So the transfer function is written directly in terms of its salient features, that is, its asymptotes and its corner frequency.

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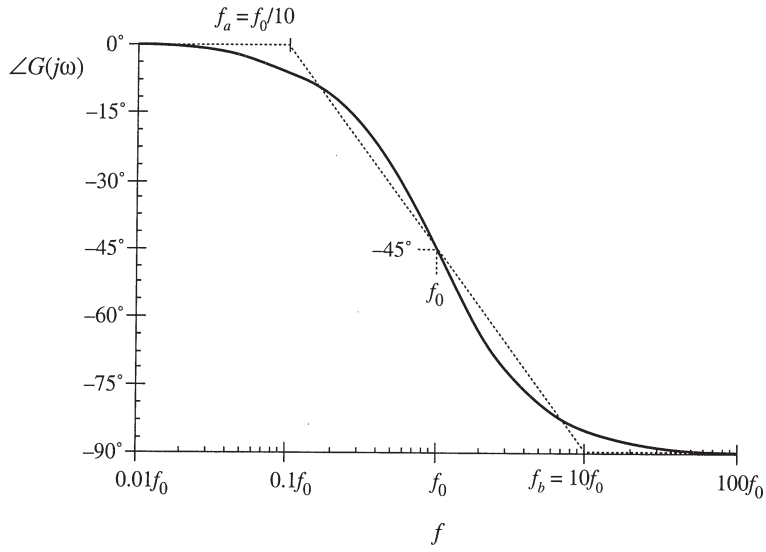


Fig. 8.10 A simpler choice for the midfrequency phase asymptote, which better approximates the curve over the entire frequency range.

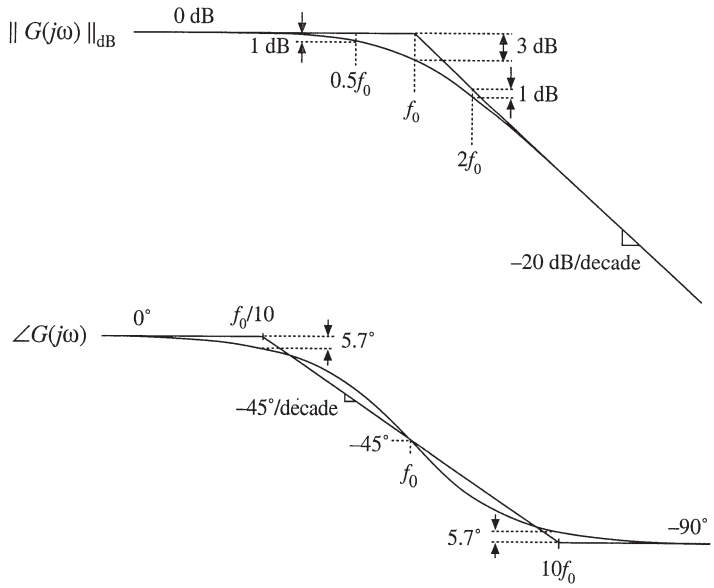


Fig. 8.11 Summary of the magnitude and phase Bode plot for the single real pole.

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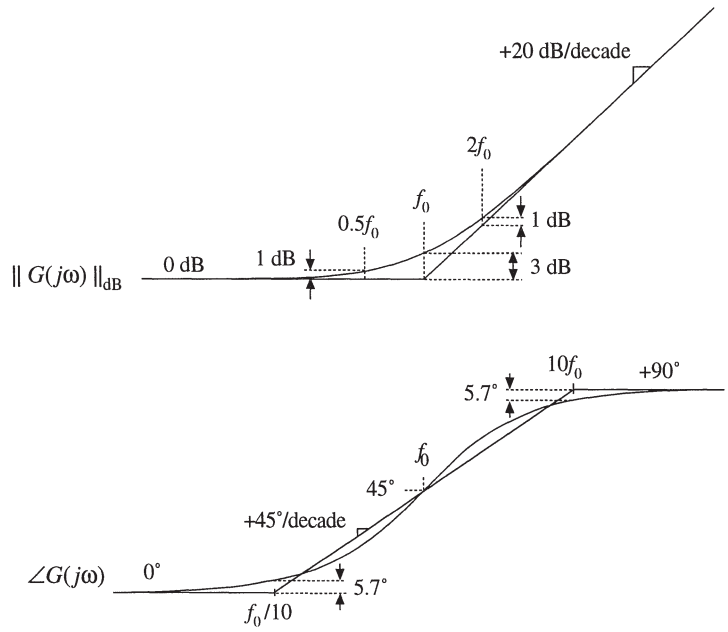


Fig. 8.12 Summary of the magnitude and phase Bode plot for the single real zero.

8.1.2 Single Zero Response

A single zero response contains a root in the numerator of the transfer function, and can be written in the following normalized form:

$$G(s) = \left(1 + \frac{s}{\omega_0}\right) \tag{8.29}$$

This transfer function has magnitude

$$\left\| G(j\omega) \right\| = \sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2} \tag{8.30}$$

At low frequency, $f \ll f_0 = \omega_0/2\pi$, the transfer function magnitude tends to $1 \Rightarrow 0$ dB. At high frequency, $f \gg f_0$, the transfer function magnitude tends to (f/f_0). As illustrated in Fig. 8.12, the high-frequency asymptote has slope +20 dB/decade.

The phase is given by

$$\angle G(j\omega) = \tan^{-1}\left(\frac{\omega}{\omega_0}\right) \tag{8.31}$$

With the exception of a minus sign, the phase is identical to Eq. (8.26). Hence, suitable asymptotes are as illustrated in Fig. 8.12. The phase tends to 0° at low frequency, and to +90° at high frequency. Over the interval $f_0/10 < f < 10f_0$, the phase asymptote has a slope of +45°/decade.

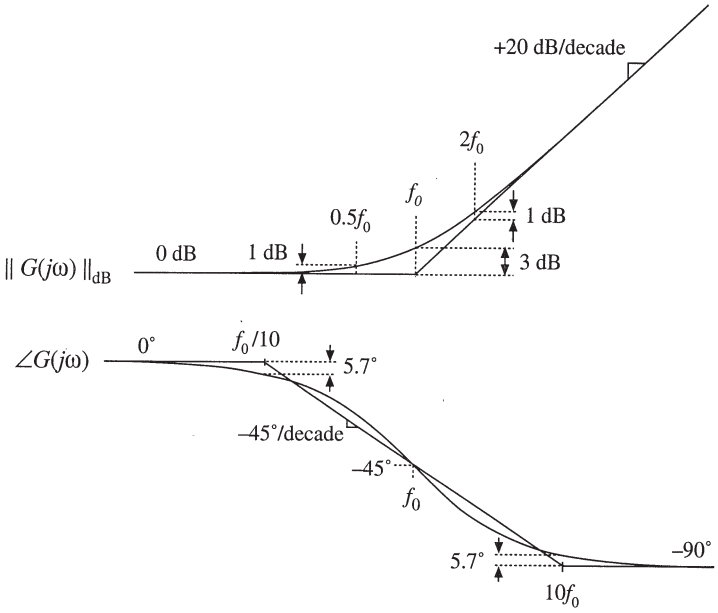


Fig. 8.13 Summary of the magnitude and phase Bode plot for the real RHP zero.

8.1.3 Right Half-Plane Zero

Right half-plane zeroes are often encountered in the small-signal transfer functions of switching converters. These terms have the following normalized form:

$$G(s) = \left(1 - \frac{s}{\omega_0}\right) \tag{8.32}$$

The root of Eq. (8.32) is positive, and hence lies in the right half of the complex s-plane. The right half-plane zero is also sometimes called a nonminimum phase zero. Its normalized form, Eq. (8.32), resembles the normalized form of the (left half-plane) zero of Eq. (8.29), with the exception of a minus sign in the coefficient of s. The minus sign causes a phase reversal at high frequency.

The transfer function has magnitude

$$\left\| G(j\omega) \right\| = \sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2} \tag{8.33}$$

This expression is identical to Eq. (8.30). Hence, it is impossible to distinguish a right half-plane zero from a left half-plane zero by the magnitude alone. The phase is given by

$$\angle G(j\omega) = -\tan^{-1}\left(\frac{\omega}{\omega_0}\right) \tag{8.34}$$

This coincides with the expression for the phase of the single pole, Eq. (8.26). So the right half-plane zero exhibits the magnitude response of the left half-plane zero, but the phase response of the pole. Magnitude and phase asymptotes are summarized in Fig. 8.13.

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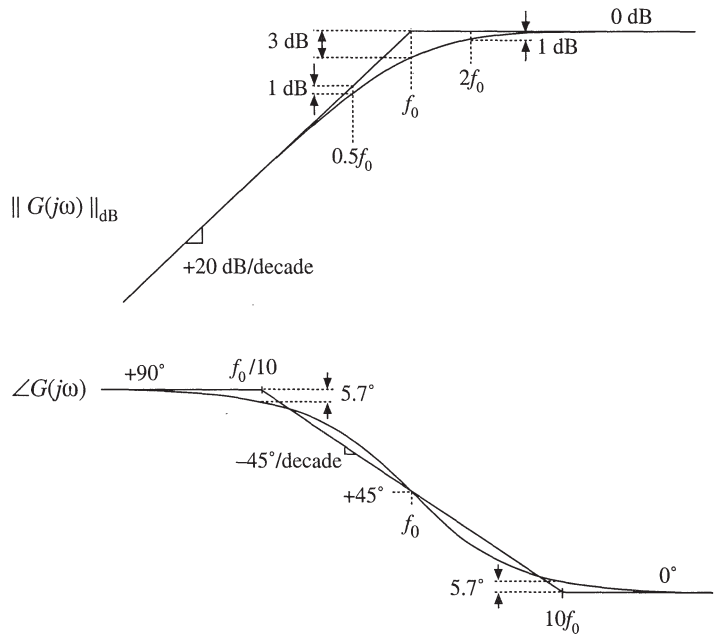


Fig. 8.14 Inversion of the frequency axis: summary of the magnitude and phase Bode plots for the inverted real pole.

8.1.4 Frequency Inversion

Two other forms arise, from inversion of the frequency axis. The inverted pole has the transfer function

$$G(s) = \frac{1}{\left(1 + \frac{\omega_0}{s}\right)} \tag{8.35}$$

As illustrated in Fig. 8.14, the inverted pole has a high-frequency gain of 1, and a low frequency asymptote having a +20 dB/decade slope. This form is useful for describing the gain of high-pass filters, and of other transfer functions where it is desired to emphasize the high frequency gain, with attenuation of low frequencies. Equation (8.35) is equivalent to

$$G(s) = \frac{\left(\frac{s}{\omega_0}\right)}{\left(1 + \frac{s}{\omega_0}\right)} \tag{8.36}$$

However, Eq. (8.35) more directly emphasizes that the high frequency gain is 1.

The inverted zero has the form

$$G(s) = \left(1 + \frac{\omega_0}{s}\right) \tag{8.37}$$

As illustrated in Fig. 8.15, the inverted zero has a high-frequency gain asymptote equal to 1, and a low-frequency asymptote having a slope equal to –20 dB/decade. An example of the use of this type of trans-

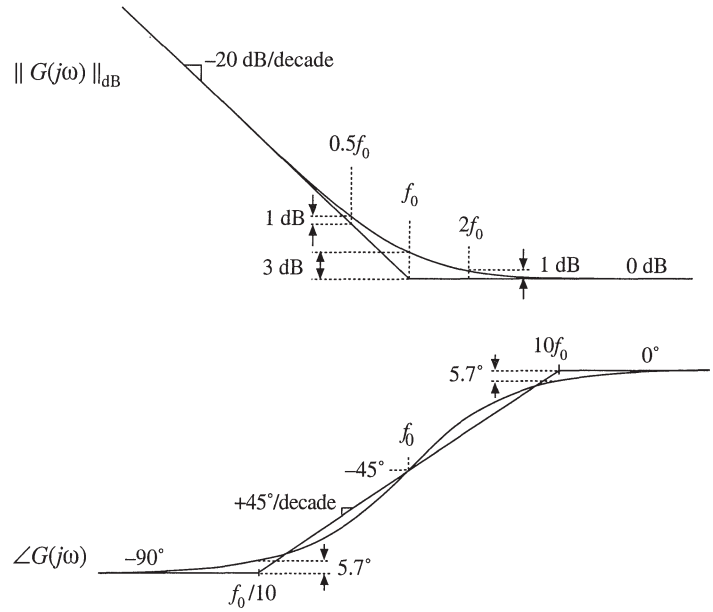


Fig. 8.15 Inversion of the frequency axis: summary of the magnitude and phase Bode plot for the inverted real zero.

fer function is the proportional-plus-integral controller, discussed in connection with feedback loop design in the next chapter. Equation (8.37) is equivalent to

$$G(s) = \frac{\left(1 + \frac{s}{\omega_0}\right)}{\left(\frac{s}{\omega_0}\right)} \tag{8.38}$$

However, Eq. (8.37) is the preferred form when it is desired to emphasize the value of the high-frequency gain asymptote.

The use of frequency inversion is illustrated by example in the next section.

8.1.5 Combinations

The Bode diagram of a transfer function containing several pole, zero, and gain terms, can be constructed by simple addition. At any given frequency, the magnitude (in decibels) of the composite transfer function is equal to the sum of the decibel magnitudes of the individual terms. Likewise, at a given frequency the phase of the composite transfer function is equal to the sum of the phases of the individual terms.

For example, suppose that we have already constructed the Bode diagrams of two complex-valued functions of ω, $G_1(\omega)$ and $G_2(\omega)$. These functions have magnitudes $R_1(\omega)$ and $R_2(\omega)$, and phases $\theta_1(\omega)$ and $\theta_2(\omega)$, respectively. It is desired to construct the Bode diagram of the product $G_3(\omega) = G_1(\omega)G_2(\omega)$. Let $G_3(\omega)$ have magnitude $R_3(\omega)$, and phase $\theta_3(\omega)$. To find this magnitude and phase, we can express $G_1(\omega)$, $G_2(\omega)$, and $G_3(\omega)$ in polar form:

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$$\begin{aligned} G_1(\omega) &= R_1(\omega)\, e^{j\theta_1(\omega)} \\ G_2(\omega) &= R_2(\omega)\, e^{j\theta_2(\omega)} \\ G_3(\omega) &= R_3(\omega)\, e^{j\theta_3(\omega)} \end{aligned} \tag{8.39}$$

The product $G_3(\omega)$ can then be expressed as

$$G_3(\omega) = G_1(\omega)G_2(\omega) = R_1(\omega)e^{j\theta_1(\omega)}\, R_2(\omega)e^{j\theta_2(\omega)} \tag{8.40}$$

Simplification leads to

$$G_3(\omega) = \left(R_1(\omega)R_2(\omega)\right) e^{j(\theta_1(\omega)+\theta_2(\omega))} \tag{8.41}$$

Hence, the composite phase is

$$\theta_3(\omega) = \theta_1(\omega) + \theta_2(\omega) \tag{8.42}$$

The total magnitude is

$$R_3(\omega) = R_1(\omega)R_2(\omega) \tag{8.43}$$

When expressed in decibels, Eq. (8.43) becomes

$$\left|R_3(\omega)\right|_{\text{dB}} = \left|R_1(\omega)\right|_{\text{dB}} + \left|R_2(\omega)\right|_{\text{dB}} \tag{8.44}$$

So the composite phase is the sum of the individual phases, and when expressed in decibels, the composite magnitude is the sum of the individual magnitudes. The composite magnitude slope, in dB per decade, is therefore also the sum of the individual slopes in dB per decade.

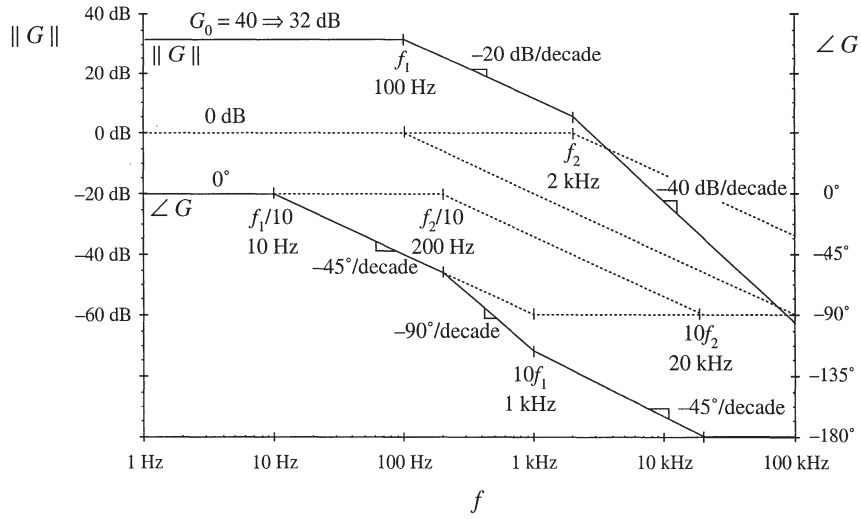


Fig. 8.16 Construction of magnitude and phase asymptotes for the transfer function of Eq.(8.45). Dashed line

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For example, consider construction of the Bode plot of the following transfer function:

$$G(s) = \frac{G_0}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)} \tag{8.45}$$

where $G_0 = 40 \Rightarrow 32$ dB, $f_1 = \omega_1/2\pi = 100$ Hz, $f_2 = \omega_2/2\pi = 2$ kHz. This transfer function contains three terms: the gain G_0, and the poles at frequencies f_1 and f_2. The asymptotes for each of these terms are illustrated in Fig. 8.16. The gain G_0 is a positive real number, and therefore contributes zero phase shift with the gain 32 dB. The poles at 100 Hz and 2 kHz each contribute asymptotes as in Fig. 8.11.

At frequencies less than 100 Hz, the G_0 term contributes a gain magnitude of 32 dB, while the two poles each contribute magnitude asymptotes of 0 dB. So the low-frequency composite magnitude asymptote is 32 dB + 0 dB + 0 dB = 32 dB. For frequencies between 100 Hz and 2 kHz, the G_0 gain again contributes 32 dB, and the pole at 2 kHz continues to contribute a 0 dB magnitude asymptote. However, the pole at 100 Hz now contributes a magnitude asymptote that decreases with a −20 dB per decade slope. The composite magnitude asymptote therefore also decreases with a −20 dB per decade slope, as illustrated in Fig. 8.16. For frequencies greater than 2 kHz, the poles at 100 Hz and 2 kHz each contribute decreasing asymptotes having slopes of −20 dB/decade. The composite asymptote therefore decreases with a slope of −20 dB/decade −20 dB/decade = −40 dB/decade, as illustrated.

The composite phase asymptote is also constructed in Fig. 8.16. Below 10 Hz, all terms contribute 0° asymptotes. For frequencies between $f_1/10 = 10$ Hz, and $f_2/10 = 200$ Hz, the pole at f_1 contributes a decreasing phase asymptote having a slope of −45°/decade. Between 200 Hz and $10f_1 = 1$ kHz, both poles contribute decreasing asymptotes with −45°/decade slopes; the composite slope is therefore −90°/decade. Between 1 kHz and $10f_2 = 20$ kHz, the pole at f_1 contributes a constant −90° phase asymptote, while the pole at f_2 contributes a decreasing asymptote with −45°/decade slope. The composite slope is then −45°/decade. For frequencies greater than 20 kHz, both poles contribute constant −90° asymptotes, leading to a composite phase asymptote of −180°.

As a second example, consider the transfer function $A(s)$ represented by the magnitude and phase asymptotes of Fig. 8.17. Let us write the transfer function that corresponds to these asymptotes. The dc asymptote is A_0. At corner frequency f_1, the asymptote slope increases from 0 dB/decade to +20 dB/decade. Hence, there must be a zero at frequency f_1. At frequency f_2, the asymptote slope decreases from +20 dB/decade to 0 dB/decade. Therefore the transfer function contains a pole at frequency f_2. So we can express the transfer function as

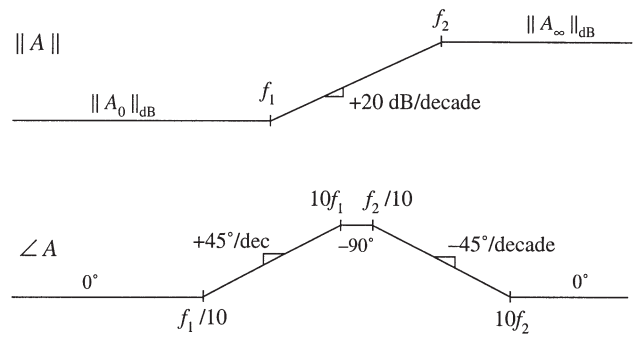


Fig. 8.17 Magnitude and phase asymptotes of example transfer function $A(s)$.

$$A(s) = A_0 \frac{\left(1 + \frac{s}{\omega_1}\right)}{\left(1 + \frac{s}{\omega_2}\right)} \tag{8.46}$$

where ω_1 and ω_2 are equal to $2\pi f_1$ and $2\pi f_2$, respectively.

We can use Eq. (8.46) to derive analytical expressions for the asymptotes. For $f < f_1$, and letting $s = j\omega$, we can see that the (s/ω_1) and (s/ω_2) terms each have magnitude less than 1. The asymptote is derived by neglecting these terms. Hence, the low-frequency magnitude asymptote is

$$\left| A_0 \frac{\left(1 + \frac{s}{\omega_1}\right)}{\left(1 + \frac{s}{\omega_2}\right)} \right|_{s = j\omega} = A_0 \frac{1}{1} = A_0 \tag{8.47}$$

For $f_1 < f < f_2$, the numerator term (s/ω_1) has magnitude greater than 1, while the denominator term (s/ω_2) has magnitude less than 1. The asymptote is derived by neglecting the smaller terms:

$$\left| A_0 \frac{\left(\not{1} + \frac{s}{\omega_1}\right)}{\left(1 + \frac{s}{\not{\omega}_2}\right)} \right|_{s = j\omega} = A_0 \frac{\left|\frac{s}{\omega_1}\right|_{s = j\omega}}{1} = A_0 \frac{\omega}{\omega_1} = A_0 \frac{f}{f_1} \tag{8.48}$$

This is the expression for the midfrequency magnitude asymptote of $A(s)$. For $f > f_2$, the (s/ω_1) and (s/ω_2) terms each have magnitude greater than 1. The expression for the high-frequency asymptote is therefore:

$$\left| A_0 \frac{\left(\not{1} + \frac{s}{\omega_1}\right)}{\left(\not{1} + \frac{s}{\omega_2}\right)} \right|_{s = j\omega} = A_0 \frac{\left|\frac{s}{\omega_1}\right|_{s = j\omega}}{\left|\frac{s}{\omega_2}\right|_{s = j\omega}} = A_0 \frac{\omega_2}{\omega_1} = A_0 \frac{f_2}{f_1} \tag{8.49}$$

We can conclude that the high-frequency gain is

$$A_\infty = A_0 \frac{f_2}{f_1} \tag{8.50}$$

Thus, we can derive analytical expressions for the asymptotes.

The transfer function $A(s)$ can also be written in a second form, using inverted poles and zeroes. Suppose that $A(s)$ represents the transfer function of a high-frequency amplifier, whose dc gain is not important. We are then interested in expressing $A(s)$ directly in terms of the high-frequency gain A_∞. We can view the transfer function as having an inverted pole at frequency f_2, which introduces attenuation at frequencies less than f_2. In addition, there is an inverted zero at $f = f_1$. So $A(s)$ could also be written

$$A(s) = A_\infty \frac{\left(1 + \frac{\omega_1}{s}\right)}{\left(1 + \frac{\omega_2}{s}\right)} \tag{8.51}$$

It can be verified that Eqs. (8.51) and (8.46) are equivalent.

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8.1.6 Quadratic Pole Response: Resonance

Consider next the transfer function $G(s)$ of the two-pole low-pass filter of Fig. 8.18. The buck converter contains a filter of this type. When manipulated into canonical form, the models of the boost and buck-boost also contain similar filters. One can show that the transfer function of this network is

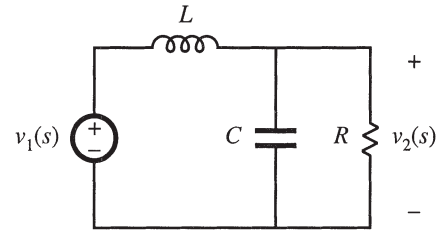


Fig. 8.18 Two-pole low-pass filter example.

$$G(s) = \frac{v_2(s)}{v_1(s)} = \frac{1}{1 + s\frac{L}{R} + s^2 LC} \tag{8.52}$$

This transfer function contains a second-order denominator polynomial, and is of the form

$$G(s) = \frac{1}{1 + a_1 s + a_2 s^2} \tag{8.53}$$

with $a_1 = L/R$ and $a_2 = LC$.

To construct the Bode plot of this transfer function, we might try to factor the denominator into its two roots:

$$G(s) = \frac{1}{\left(1 - \frac{s}{s_1}\right)\left(1 - \frac{s}{s_2}\right)} \tag{8.54}$$

Use of the quadratic formula leads to the following expressions for the roots:

$$s_1 = -\frac{a_1}{2a_2}\left[1 - \sqrt{1 - \frac{4a_2}{a_1^2}}\right] \tag{8.55}$$

$$s_2 = -\frac{a_1}{2a_2}\left[1 + \sqrt{1 - \frac{4a_2}{a_1^2}}\right] \tag{8.56}$$

If $4a_2 \leq a_1^2$, then the roots are real. Each real pole then exhibits a Bode diagram as derived in Section 8.1.1, and the composite Bode diagram can be constructed as described in Section 8.1.5 (but a better approach is described in Section 8.1.7).

If $4a_2 > a_1^2$, then the roots (8.55) and (8.56) are complex. In Section 8.1.1, the assumption was made that ω_0 is real; hence, the results of that section cannot be applied to this case. We need to do some additional work, to determine the magnitude and phase for the case when the roots are complex.

The transfer functions of Eqs. (8.52) and (8.53) can be written in the following standard normalized form:

$$G(s) = \frac{1}{1 + 2\zeta\frac{s}{\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{8.57}$$

If the coefficients a_1 and a_2 are real and positive, then the parameters ζ and ω_0 are also real and positive. The parameter ω_0 is again the angular corner frequency, and we can define $f_0 = \omega_0/2\pi$. The parameter ζ is

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called the *damping factor*: ζ controls the shape of the transfer function in the vicinity of $f = f_0$. An alternative standard normalized form is

$$G(s) = \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{8.58}$$

where

$$Q = \frac{1}{2\zeta} \tag{8.59}$$

The parameter Q is called the *quality factor* of the circuit, and is a measure of the dissipation in the system. A more general definition of Q, for sinusoidal excitation of a passive element or network, is

$$Q = 2\pi \frac{\text{(peak stored energy)}}{\text{(energy dissipated per cycle)}} \tag{8.60}$$

For a second-order passive system, Eqs. (8.59) and (8.60) are equivalent. We will see that the Q-factor has a very simple interpretation in the magnitude Bode diagrams of second-order transfer functions.

Analytical expressions for the parameters Q and ω_0 can be found by equating like powers of s in the original transfer function, Eq. (8.52), and in the normalized form, Eq. (8.58). The result is

$$\begin{aligned} f_0 &= \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{LC}} \\ Q &= R\sqrt{\frac{C}{L}} \end{aligned} \tag{8.61}$$

The roots s_1 and s_2 of Eqs. (8.55) and (8.56) are real when $Q \leq 0.5$, and are complex when $Q > 0.5$.

The magnitude of G is

$$\| G(j\omega) \| = \frac{1}{\sqrt{\left(1 - \left(\frac{\omega}{\omega_0}\right)^2\right)^2 + \frac{1}{Q^2}\left(\frac{\omega}{\omega_0}\right)^2}} \tag{8.62}$$

Asymptotes of $\| G \|$ are illustrated in Fig. 8.19. At low frequencies, $(\omega/\omega_0) \ll 1$, and hence

$$\| G \| \to 1 \quad \text{for } \omega \ll \omega_0 \tag{8.63}$$

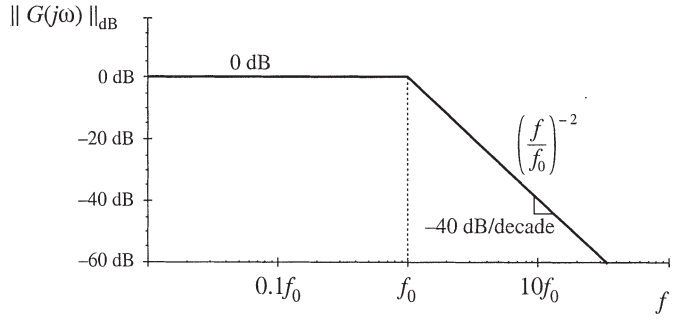


Fig. 8.19 Magnitude asymptotes for the two-pole transfer function.

At high frequencies where $(\omega/\omega_0) \gg 1$, the $(\omega/\omega_0)^4$ term dominates the expression inside the radical of Eq. (8.62). Hence, the high-frequency asymptote is

$$\| G \| \rightarrow \left(\frac{f}{f_0} \right)^{-2} \quad \text{for } \omega \gg \omega_0 \tag{8.64}$$

This expression coincides with Eq. (8.5), with $n = -2$. Therefore, the high-frequency asymptote has slope –40 dB/decade. The asymptotes intersect at $f = f_0$, and are independent of Q.

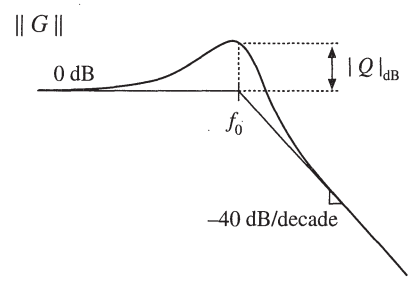


Fig. 8.20 Important features of the magnitude Bode plot, for the two-pole transfer function.

The parameter Q affects the deviation of the actual curve from the asymptotes, in the neighborhood of the corner frequency f_0. The exact magnitude at $f = f_0$ is found by substitution of $\omega = \omega_0$ into Eq. (8.62):

$$\left\| G(j\omega_0) \right\| = Q \tag{8.65}$$

So the exact transfer function has magnitude Q at the corner frequency f_0. In decibels, Eq. (8.65) is

$$\left\| G(j\omega_0) \right\|_{\text{dB}} = \left| Q \right|_{\text{dB}} \tag{8.66}$$

So if, for example, $Q = 2 \Rightarrow 6$ dB, then the actual curve deviates from the asymptotes by 6 dB at the corner frequency $f = f_0$. Salient features of the magnitude Bode plot of the second-order transfer function are summarized in Fig. 8.20.

The phase of G is

$$\angle G(j\omega) = -\tan^{-1} \left[\frac{\frac{1}{Q} \left(\frac{\omega}{\omega_0} \right)}{1 - \left(\frac{\omega}{\omega_0} \right)^2} \right] \tag{8.67}$$

The phase tends to 0° at low frequency, and to –180° at high frequency. At $f = f_0$, the phase is –90°. As illustrated in Fig. 8.21, increasing the value of Q causes a sharper phase change between the 0° and –180° asymptotes. We again need a midfrequency asymptote, to approximate the phase transition in the

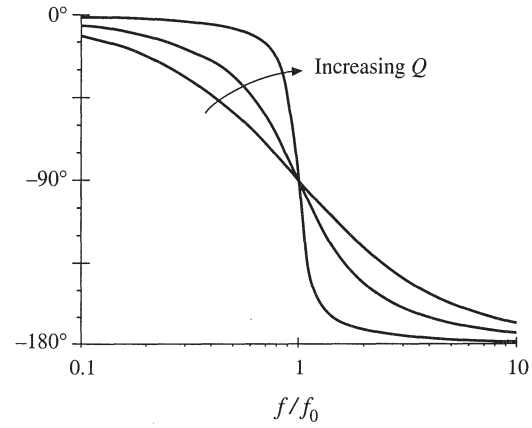


Fig. 8.21 Phase plot, second-order poles. Increasing Q causes a sharper phase change.

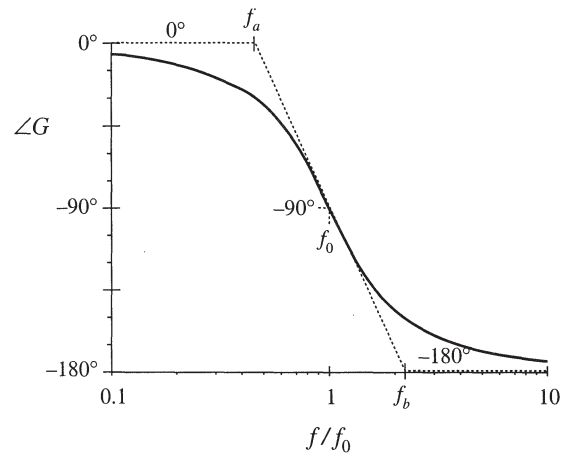


Fig. 8.22 One choice for the midfrequency phase asymptote of the two-pole response, which correctly predicts the actual slope at $f = f_0$.

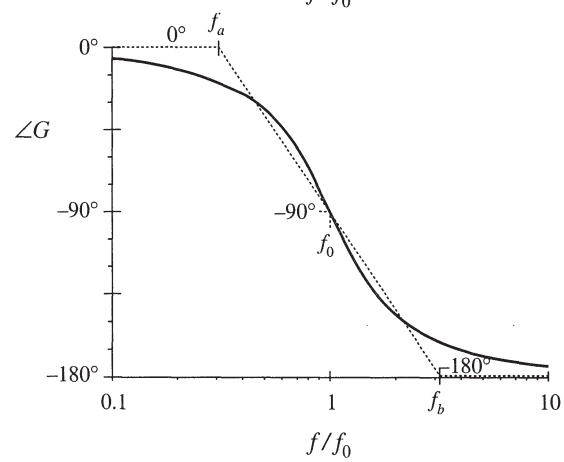


Fig. 8.23 A simpler choice for the midfrequency phase asymptote, which better approximates the curve over the entire frequency range and is consistent with the asymptote used for real poles.

vicinity of the corner frequency f_0, as illustrated in Fig. 8.22. As in the case of the real single pole, we could choose the slope of this asymptote to be identical to the slope of the actual curve at $f = f_0$. It can be shown that this choice leads to the following asymptote break frequencies:

$$\begin{aligned} f_a &= \left(e^{\pi/2}\right)^{-\frac{1}{2Q}} f_0 \\ f_b &= \left(e^{\pi/2}\right)^{\frac{1}{2Q}} f_0 \end{aligned} \tag{8.68}$$

A better choice, which is consistent with the approximation (8.28) used for the real single pole, is

$$\begin{aligned} f_a &= 10^{-1/2Q} f_0 \\ f_b &= 10^{1/2Q} f_0 \end{aligned} \tag{8.69}$$

With this choice, the midfrequency asymptote has slope $-180Q$ degrees per decade. The phase asymptotes are summarized in Fig. 8.23. With $Q = 0.5$, the phase changes from 0° to –180° over a frequency span of approximately two decades, centered at the corner frequency f_0. Increasing the Q causes this frequency span to decrease rapidly.

Second-order response magnitude and phase curves are plotted in Figs. 8.24 and 8.25.

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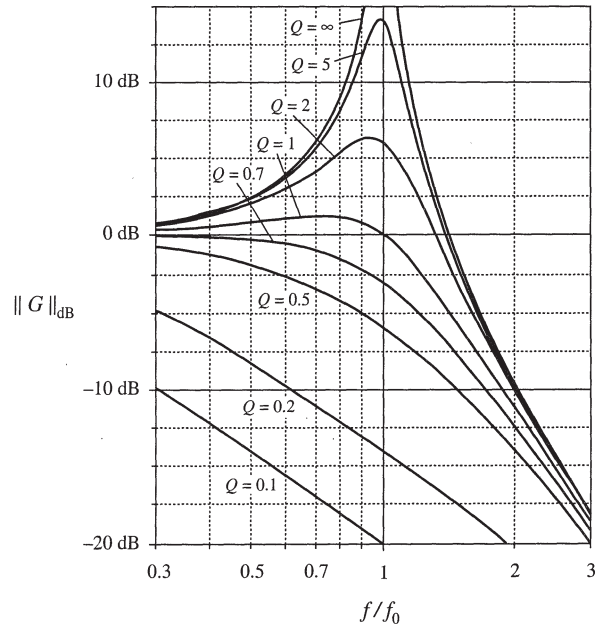


Fig. 8.24 Exact magnitude curves, two-pole response, for several values of Q.

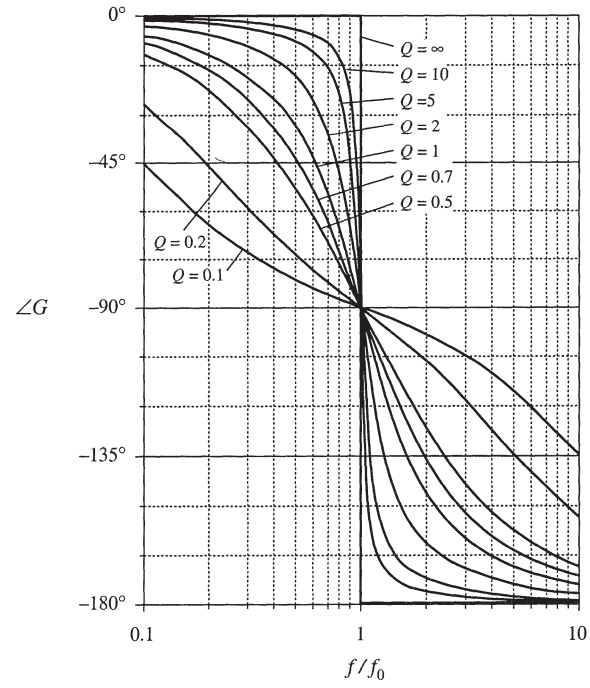


Fig. 8.25 Exact phase curves, two-pole response, for several values of Q.

8.1.7 The Low-Q Approximation

As mentioned in Section 8.1.6, when the roots of second-order denominator polynomial of Eq. (8.53) are real, then we can factor the denominator, and construct the Bode diagram using the asymptotes for real poles. We would then use the following normalized form:

$$G(s) = \frac{1}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)} \tag{8.70}$$

This is a particularly desirable approach when the corner frequencies ω_1 and ω_2 are well separated in value.

The difficulty in this procedure lies in the complexity of the quadratic formula used to find the corner frequencies. Expressing the corner frequencies ω_1 and ω_2 in terms of the circuit elements R, L, C, etc., invariably leads to complicated and unilluminating expressions, especially when the circuit contains many elements. Even in the case of the simple circuit of Fig. 8.18, whose transfer function is given by Eq. (8.52), the conventional quadratic formula leads to the following complicated formula for the corner frequencies:

$$\omega_1, \omega_2 = \frac{\frac{L}{R} \pm \sqrt{\left(\frac{L}{R}\right)^2 - 4LC}}{2LC} \tag{8.71}$$

This equation yields essentially no insight regarding how the corner frequencies depend on the element values. For example, it can be shown that when the corner frequencies are well separated in value, they can be expressed with high accuracy by the much simpler relations

$$\omega_1 \approx \frac{R}{L}, \quad \omega_2 \approx \frac{1}{RC} \tag{8.72}$$

In this case, ω_1 is essentially independent of the value of C, and ω_2 is essentially independent of L, yet Eq. (8.71) apparently predicts that both corner frequencies are dependent on all element values. The simple expressions of Eq. (8.72) are far preferable to Eq. (8.71), and can be easily derived using the low-Q approximation [2].

Let us assume that the transfer function has been expressed in the standard normalized form of Eq. (8.58), reproduced below:

$$G(s) = \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{8.73}$$

For $Q \leq 0.5$, let us use the quadratic formula to write the real roots of the denominator polynomial of Eq. (8.73) as

$$\omega_1 = \frac{\omega_0}{Q} \frac{1 - \sqrt{1 - 4Q^2}}{2} \tag{8.74}$$

$$\omega_2 = \frac{\omega_0}{Q} \frac{1 + \sqrt{1 - 4Q^2}}{2} \tag{8.75}$$

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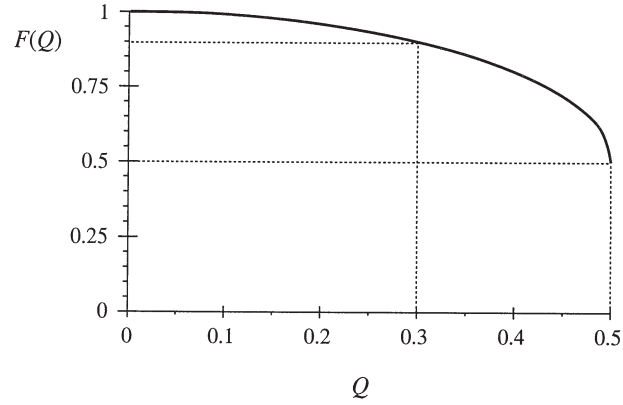


Fig. 8.26 $F(Q)$ vs. Q, as given by Eq. (8.77). The approximation $F(Q) \approx 1$ is within 10% of the exact value for $Q < 3$.

The corner frequency ω_2 can be expressed

$$\omega_2 = \frac{\omega_0}{Q} F(Q) \tag{8.76}$$

where $F(Q)$ is defined as [2]:

$$F(Q) = \frac{1}{2}\left(1 + \sqrt{1 - 4Q^2}\right) \tag{8.77}$$

Note that, when $Q \ll 0.5$, then $4Q^2 \ll 1$ and $F(Q)$ is approximately equal to 1. We then obtain

$$\omega_2 \approx \frac{\omega_0}{Q} \quad \text{for } Q \ll \frac{1}{2} \tag{8.78}$$

The function $F(Q)$ is plotted in Fig. 8.26. It can be seen that $F(Q)$ approaches 1 very rapidly as Q decreases below 0.5.

To derive a similar approximation for ω_1, we can multiply and divide Eq. (8.74) by $F(Q)$, Eq. (8.77). Upon simplification of the numerator, we obtain

$$\omega_1 = \frac{Q\omega_0}{F(Q)} \tag{8.79}$$

Again, $F(Q)$ tends to 1 for small Q. Hence, ω_1 can be approximated as

$$\omega_1 \approx Q\omega_0 \quad \text{for } Q \ll \frac{1}{2} \tag{8.80}$$

Magnitude asymptotes for the low-Q case are summarized in Fig. 8.27. For $Q < 0.5$, the two poles at ω_0 split into real poles. One real pole occurs at corner frequency $\omega_1 < \omega_0$, while the other occurs at corner frequency $\omega_2 > \omega_0$. The corner frequencies are easily approximated, using Eqs. (8.78) and (8.80).

For the filter circuit of Fig. 8.18, the parameters Q and ω_0 are given by Eq. (8.61). For the case when $Q \ll 0.5$, we can derive the following analytical expressions for the corner frequencies, using Eqs. (8.78) and (8.80):

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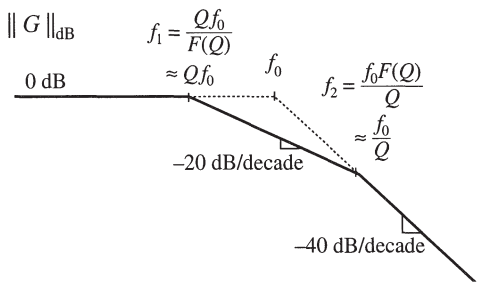


Fig. 8.27 Magnitude asymptotes predicted by the low-Q approximation. Real poles occur at frequencies Qf_0 and f_0/Q.

$$\omega_1 \approx Q\omega_0 = R\sqrt{\frac{C}{L}}\,\frac{1}{\sqrt{LC}} = \frac{R}{L}$$
$$\omega_2 \approx \frac{\omega_0}{Q} = \frac{1}{\sqrt{LC}}\,\frac{1}{R\sqrt{\frac{C}{L}}} = \frac{1}{RC} \tag{8.81}$$

So the low-Q approximation allows us to derive simple design-oriented analytical expressions for the corner frequencies.

8.1.8 Approximate Roots of an Arbitrary-Degree Polynomial

The low-Q approximation can be generalized, to find approximate analytical expressions for the roots of the nth-order polynomial

$$P(s) = 1 + a_1 s + a_2 s^2 + \cdots + a_n s^n \tag{8.82}$$

It is desired to factor the polynomial $P(s)$ into the form

$$P(s) = \left(1 + \tau_1 s\right)\left(1 + \tau_2 s\right)\cdots\left(1 + \tau_n s\right) \tag{8.83}$$

In a real circuit, the coefficients a_1, ..., a_n are real, while the time constants τ_1, ..., τ_n may be either real or complex. Very often, some or all of the time constants are well separated in value, and depend in a very simple way on the circuit element values. In such cases, simple approximate analytical expressions for the time constants can be derived.

The time constants τ_1, ..., τ_n can be related to the original coefficients a_1, ..., a_n by multiplying out Eq. (8.83). The result is

$$\begin{aligned}
a_1 &= \tau_1 + \tau_2 + \cdots + \tau_n \\
a_2 &= \tau_1\left(\tau_2 + \cdots + \tau_n\right) + \tau_2\left(\tau_3 + \cdots + \tau_n\right) + \cdots \\
a_3 &= \tau_1\tau_2\left(\tau_3 + \cdots + \tau_n\right) + \tau_2\tau_3\left(\tau_4 + \cdots + \tau_n\right) + \cdots \\
&\vdots \\
a_n &= \tau_1\tau_2\tau_3\cdots\tau_n
\end{aligned} \tag{8.84}$$

General solution of this system of equations amounts to exact factoring of the arbitrary degree polynomial, a hopeless task. Nonetheless, Eq. (8.84) does suggest a way to approximate the roots.

Suppose that all of the time constants τ_1, ..., τ_n are real and well separated in value. We can further assume, without loss of generality, that the time constants are arranged in decreasing order of magni-

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tude:

$$|\tau_1| \gg |\tau_2| \gg \cdots \gg |\tau_n| \tag{8.85}$$

When the inequalities of Eq. (8.85) are satisfied, then the expressions for a_1, ..., a_n of Eq. (8.84) are each dominated by their first terms:

$$\begin{aligned} a_1 &\approx \tau_1 \\ a_2 &\approx \tau_1\tau_2 \\ a_3 &\approx \tau_1\tau_2\tau_3 \\ &\vdots \\ a_n &= \tau_1\tau_2\tau_3\cdots\tau_n \end{aligned} \tag{8.86}$$

These expressions can now be solved for the time constants, with the result

$$\begin{aligned} \tau_1 &\approx a_1 \\ \tau_2 &\approx \frac{a_2}{a_1} \\ \tau_3 &\approx \frac{a_3}{a_2} \\ &\vdots \\ \tau_n &\approx \frac{a_n}{a_{n-1}} \end{aligned} \tag{8.87}$$

Hence, if

$$|a_1| \gg \left|\frac{a_2}{a_1}\right| \gg \left|\frac{a_3}{a_2}\right| \gg \cdots \gg \left|\frac{a_n}{a_{n-1}}\right| \tag{8.88}$$

then the polynomial $P(s)$ given by Eq. (8.82) has the approximate factorization

$$P(s) \approx (1 + a_1 s)\left(1 + \frac{a_2}{a_1} s\right)\left(1 + \frac{a_3}{a_2} s\right)\cdots\left(1 + \frac{a_n}{a_{n-1}} s\right) \tag{8.89}$$

Note that if the original coefficients in Eq. (8.82) are simple functions of the circuit elements, then the approximate roots given by Eq. (8.89) are similar simple functions of the circuit elements. So approximate analytical expressions for the roots can be obtained. Numerical values are substituted into Eq. (8.88) to justify the approximation.

In the case where two of the roots are not well separated, then one of the inequalities of Eq. (8.88) is violated. We can then leave the corresponding terms in quadratic form. For example, suppose that inequality k is not satisfied:

$$|a_1| \gg \left|\frac{a_2}{a_1}\right| \gg \cdots \gg \left|\frac{a_k}{a_{k-1}}\right| \not\gg \left|\frac{a_{k+1}}{a_k}\right| \gg \cdots \gg \left|\frac{a_n}{a_{n-1}}\right| \tag{8.90}$$

Then an approximate factorization is

$$P(s) \approx \left(1 + a_1 s\right)\left(1 + \frac{a_2}{a_1} s\right) \cdots \left(1 + \frac{a_k}{a_{k-1}} s + \frac{a_{k+1}}{a_{k-1}} s^2\right) \cdots \left(1 + \frac{a_n}{a_{n-1}} s\right) \tag{8.91}$$

The conditions for accuracy of this approximation are

$$|a_1| \gg \left|\frac{a_2}{a_1}\right| \gg \cdots \gg \left|\frac{a_k}{a_{k-1}}\right| \gg \left|\frac{a_{k-2}\, a_{k+1}}{a_{k-1}^2}\right| \gg \left|\frac{a_{k+2}}{a_{k+1}}\right| \gg \cdots \gg \left|\frac{a_n}{a_{n-1}}\right| \tag{8.92}$$

Complex conjugate roots can be approximated in this manner.

When the first inequality of Eq. (8.88) is violated, that is,

$$|a_1| \not\gg \left|\frac{a_2}{a_1}\right| \gg \left|\frac{a_3}{a_2}\right| \gg \cdots \gg \left|\frac{a_n}{a_{n-1}}\right| \tag{8.93}$$

then the first two roots should be left in quadratic form:

$$P(s) \approx \left(1 + a_1 s + a_2 s^2\right)\left(1 + \frac{a_3}{a_2} s\right) \cdots \left(1 + \frac{a_n}{a_{n-1}} s\right) \tag{8.94}$$

This approximation is justified provided that

$$\left|\frac{a_2^2}{a_3}\right| \gg |a_1| \gg \left|\frac{a_3}{a_2}\right| \gg \left|\frac{a_4}{a_3}\right| \gg \cdots \gg \left|\frac{a_n}{a_{n-1}}\right| \tag{8.95}$$

If none of the above approximations is justified, then there are three or more roots that are close in magnitude. One must then resort to cubic or higher-order forms.

As an example, consider the damped EMI filter illustrated in Fig. 8.28. Filters such as this are typically placed at the power input of a converter, to attenuate the switching harmonics present in the converter input current. By circuit analysis, on can show that this filter exhibits the following transfer function:

$$G(s) = \frac{i_g(s)}{i_c(s)} = \frac{1 + s\dfrac{L_1 + L_2}{R}}{1 + s\dfrac{L_1 + L_2}{R} + s^2 L_1 C + s^3 \dfrac{L_1 L_2 C}{R}} \tag{8.96}$$

This transfer function contains a third-order denominator, with the following coefficients:

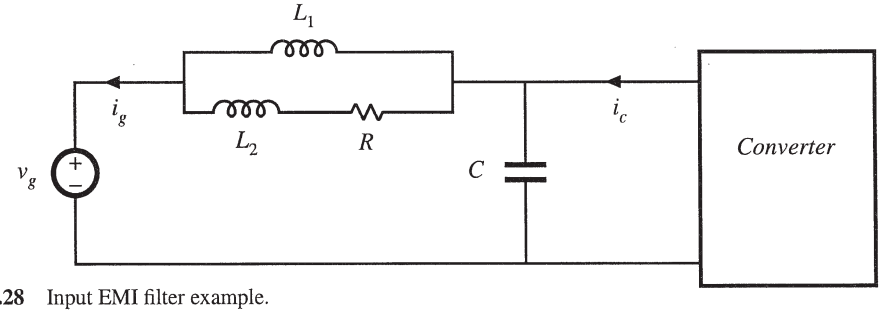


Fig. 8.28 Input EMI filter example.

$$a_1 = \frac{L_1 + L_2}{R}$$
$$a_2 = L_1 C \tag{8.97}$$
$$a_3 = \frac{L_1 L_2 C}{R}$$

It is desired to factor the denominator, to obtain analytical expressions for the poles. The correct way to do this depends on the numerical values of R, L_1, L_2, and C. When the roots are real and well separated, then Eq. (8.89) predicts that the denominator can be factored as follows:

$$\left(1 + s\frac{L_1 + L_2}{R}\right)\left(1 + sRC\frac{L_1}{L_1 + L_2}\right)\left(1 + s\frac{L_2}{R}\right) \tag{8.98}$$

According to Eq. (8.88), this approximation is justified provided that

$$\frac{L_1 + L_2}{R} \gg RC\frac{L_1}{L_1 + L_2} \gg \frac{L_2}{R} \tag{8.99}$$

These inequalities cannot be satisfied unless $L_1 \gg L_2$. When $L_1 \gg L_2$, then Eq. (8.99) can be further simplified to

$$\frac{L_1}{R} \gg RC \gg \frac{L_2}{R} \tag{8.100}$$

The approximate factorization, Eq. (8.98), can then be further simplified to

$$\left(1 + s\frac{L_1}{R}\right)\left(1 + sRC\right)\left(1 + s\frac{L_2}{R}\right) \tag{8.101}$$

Thus, in this case the transfer function contains three well separated real poles. Equations (8.98) and (8.101) represent approximate analytical factorizations of the denominator of Eq. (8.96). Although numerical values must be substituted into Eqs. (8.99) or (8.100) to justify the approximation, we can nonetheless express Eqs. (8.98) and (8.101) as analytical functions of L_1, L_2, R, and C. Equations (8.98) and (8.101) are design-oriented, because they yield insight into how the element values can be chosen such that given specified pole frequencies are obtained.

When the second inequality of Eq. (8.99) is violated,

$$\frac{L_1 + L_2}{R} \gg RC\frac{L_1}{L_1 + L_2} \not\gg \frac{L_2}{R} \tag{8.102}$$

then the second and third roots should be left in quadratic form:

$$\left(1 + s\frac{L_1 + L_2}{R}\right)\left(1 + sRC\frac{L_1}{L_1 + L_2} + s^2 L_1 \| L_2 C\right) \tag{8.103}$$

This expression follows from Eq. (8.91), with $k = 2$. Equation (8.92) predicts that this approximation is justified provided that

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$$\frac{L_1 + L_2}{R} \gg RC \frac{L_1}{L_1 + L_2} \gg \frac{L_1 \| L_2}{L_1 + L_2} RC \tag{8.104}$$

In application of Eq. (8.92), we take a_0 to be equal to 1. The inequalities of Eq. (8.104) can be simplified to obtain

$$L_1 \gg L_2, \quad \text{and} \quad \frac{L_1}{R} \gg RC \tag{8.105}$$

Note that it is no longer required that $RC \gg L_2/R$. Equation (8.105) implies that factorization (8.103) can be further simplified to

$$\left(1 + s\frac{L_1}{R}\right)\left(1 + sRC + s^2 L_2 C\right) \tag{8.106}$$

Thus, for this case, the transfer function contains a low-frequency pole that is well separated from a high-frequency quadratic pole pair. Again, the factored result (8.106) is expressed as an analytical function of the element values, and consequently is design-oriented.

In the case where the first inequality of Eq. (8.99) is violated:

$$\frac{L_1 + L_2}{R} \not\gg RC \frac{L_1}{L_1 + L_2} \gg \frac{L_2}{R} \tag{8.107}$$

then the first and second roots should be left in quadratic form:

$$\left(1 + s\frac{L_1 + L_2}{R} + s^2 L_1 C\right)\left(1 + s\frac{L_2}{R}\right) \tag{8.108}$$

This expression follows directly from Eq. (8.94). Equation (8.95) predicts that this approximation is justified provided that

$$\frac{L_1 RC}{L_2} \gg \frac{L_1 + L_2}{R} \gg \frac{L_2}{R} \tag{8.109}$$

that is,

$$L_1 \gg L_2, \quad \text{and} \quad RC \gg \frac{L_2}{R} \tag{8.110}$$

For this case, the transfer function contains a low-frequency quadratic pole pair that is well separated from a high-frequency real pole. If none of the above approximations are justified, then all three of the roots are similar in magnitude. We must then find other means of dealing with the original cubic polynomial. Design of input filters, including the filter of Fig. 8.28, is covered in Chapter 10.

8.2 ANALYSIS OF CONVERTER TRANSFER FUNCTIONS

Let us next derive analytical expressions for the poles, zeroes, and asymptote gains in the transfer functions of the basic converters.

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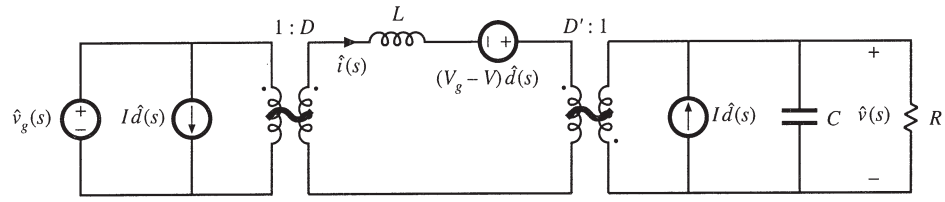


Fig. 8.29 Buck-boost converter equivalent circuit derived in Section 7.2.

8.2.1 Example: Transfer Functions of the Buck-Boost Converter

The small-signal equivalent circuit model of the buck-boost converter is derived in Section 7.2, with the result [Fig. 7.16(b)] repeated in Fig. 8.29. Let us derive and plot the control-to-output and line-to-output transfer functions for this circuit.

The converter contains two independent ac inputs: the control input $\hat{d}(s)$ and the line input $\hat{v}_g(s)$. The ac output voltage variations $\hat{v}(s)$ can be expressed as the superposition of terms arising from these two inputs:

$$\hat{v}(s) = G_{vd}(s)\hat{d}(s) + G_{vg}(s)\,\hat{v}_g(s) \tag{8.111}$$

Hence, the transfer functions $G_{vd}(s)$ and $G_{vg}(s)$ can be defined as

$$G_{vd}(s) = \left.\frac{\hat{v}(s)}{\hat{d}(s)}\right|_{\hat{v}_g(s)=0} \quad \text{and} \quad G_{vg}(s) = \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\hat{d}(s)=0} \tag{8.112}$$

To find the line-to-output transfer function $G_{vg}(s)$, we set the $\hat{d}$ sources to zero as in Fig. 8.30(a). We can then push the $v_g(s)$ source and the inductor through the transformers, to obtain the circuit of Fig. 8.30(b). The transfer function $G_{vg}(s)$ is found using the voltage divider formula:

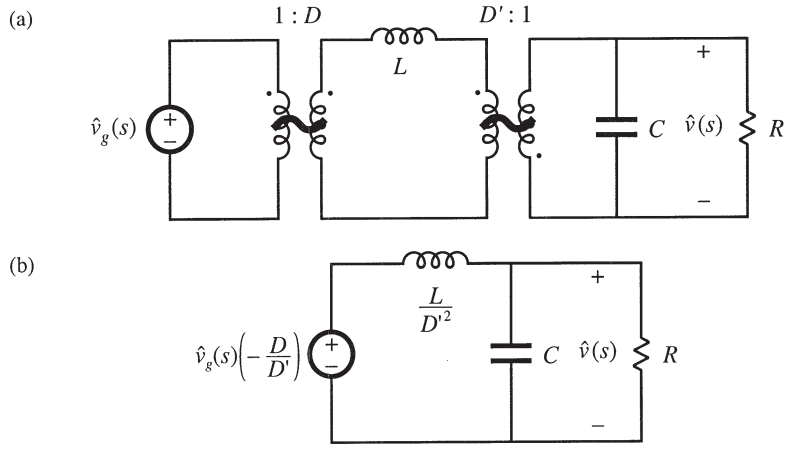


Fig. 8.30 Manipulation of buck-boost equivalent circuit to find the line-to-output transfer function $G_{vg}(s)$: (a) set $\hat{d}$ sources to zero; (b) push inductor and $\hat{v}_g$ source through transformers.

$$G_{vg}(s) = \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\hat{d}(s)=0} = -\frac{D}{D'}\frac{\left(R \parallel \frac{1}{sC}\right)}{\frac{sL}{D'^2} + \left(R \parallel \frac{1}{sC}\right)} \tag{8.113}$$

We next expand the parallel combination, and express as a rational fraction:

$$\begin{aligned} G_{vg}(s) &= \left(-\frac{D}{D'}\right)\frac{\left(\frac{R}{1+sRC}\right)}{\frac{sL}{D'^2} + \left(\frac{R}{1+sRC}\right)} \\ &= \left(-\frac{D}{D'}\right)\frac{R}{R + \frac{sL}{D'^2} + \frac{s^2RLC}{D'^2}} \end{aligned} \tag{8.114}$$

We aren't done yet—the next step is to manipulate the expression into normalized form, such that the coefficients of s^0 in the numerator and denominator polynomials are equal to one. This can be accomplished by dividing the numerator and denominator by R:

$$G_{vg}(s) = \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\hat{d}(s)=0} = \left(-\frac{D}{D'}\right)\frac{1}{1 + s\frac{L}{D'^2R} + s^2\frac{LC}{D'^2}} \tag{8.115}$$

Thus, the line-to-output transfer function contains a dc gain G_{g0} and a quadratic pole pair:

$$G_{vg}(s) = G_{g0}\frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{8.116}$$

Analytical expressions for the salient features of the line-to-output transfer function are found by equating like terms in Eqs. (8.115) and (8.116). The dc gain is

$$G_{g0} = -\frac{D}{D'} \tag{8.117}$$

By equating the coefficients of s^2 in the denominators of Eqs. (8.115) and (8.116), we obtain

$$\frac{1}{\omega_0^2} = \frac{LC}{D'^2} \tag{8.118}$$

Hence, the angular corner frequency is

$$\omega_0 = \frac{D'}{\sqrt{LC}} \tag{8.119}$$

By equating coefficients of s in the denominators of Eqs. (8.115) and (8.116), we obtain

$$\frac{1}{Q\omega_0} = \frac{L}{D'^2R} \tag{8.120}$$

Elimination of ω_0 using Eq. (8.119) and solution for Q leads to

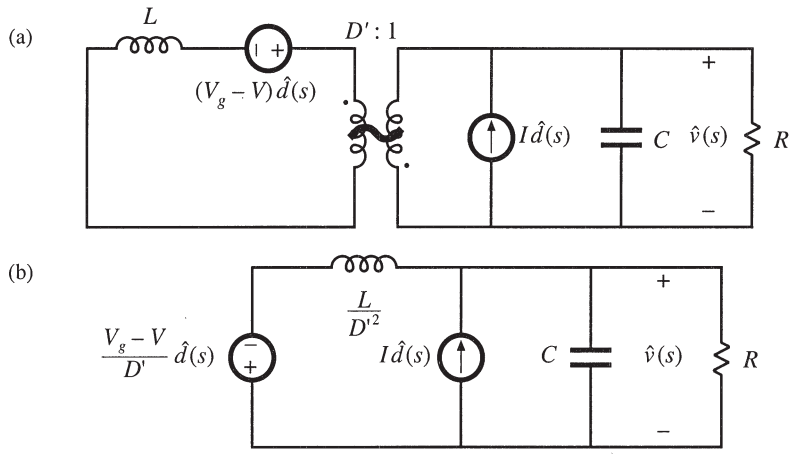


Fig. 8.31 Manipulation of buck-boost equivalent circuit to find the control-to-output transfer function $G_{vd}(s)$: (a) set $\hat{v}_g$ source to zero; (b) push inductor and voltage source through transformer.

$$Q = D'R\sqrt{\frac{C}{L}} \tag{8.121}$$

Equations (8.117), (8.119), and (8.121) are the desired results in the analysis of the line-to-output transfer function. These expressions are useful not only in analysis situations, where it is desired to find numerical values of the salient features G_{g0}, ω_0, and Q, but also in design situations, where it is desired to select numerical values for R, L, and C such that given values of the salient features are obtained.

Derivation of the control-to-output transfer function $G_{vd}(s)$ is complicated by the presence in Fig. 8.29 of three generators that depend on $\hat{d}(s)$. One good way to find $G_{vd}(s)$ is to manipulate the circuit model as in the derivation of the canonical model, Fig. 7.60. Another approach, used here, employs the principle of superposition. First, we set the $\hat{v}_g$ source to zero. This shorts the input to the 1:D transformer, and we are left with the circuit illustrated in Fig. 8.31(a). Next, we push the inductor and $\hat{d}$ voltage source through the D':1 transformer, as in Fig. 8.31(b).

Figure 8.31(b) contains a $\hat{d}$-dependent voltage source and a $\hat{d}$-dependent current source. The transfer function $G_{vd}(s)$ can therefore be expressed as a superposition of terms arising from these two sources. When the current source is set to zero (i.e., open-circuited), the circuit of Fig. 8.32(a) is obtained. The output $\hat{v}(s)$ can then be expressed as

$$\frac{\hat{v}(s)}{\hat{d}(s)} = \left(-\frac{V_g - V}{D'}\right)\frac{\left(R \parallel \frac{1}{sC}\right)}{\frac{sL}{D'^2} + \left(R \parallel \frac{1}{sC}\right)} \tag{8.122}$$

When the voltage source is set to zero (i.e., short-circuited), Fig. 8.31(b) reduces to the circuit illustrated in Fig. 8.32(b). The output $\hat{v}(s)$ can then be expressed as

$$\frac{\hat{v}(s)}{\hat{d}(s)} = I\left(\frac{sL}{D'^2} \parallel R \parallel \frac{1}{sC}\right) \tag{8.123}$$

The transfer function $G_{vd}(s)$ is the sum of Eqs. (8.122) and (8.123):

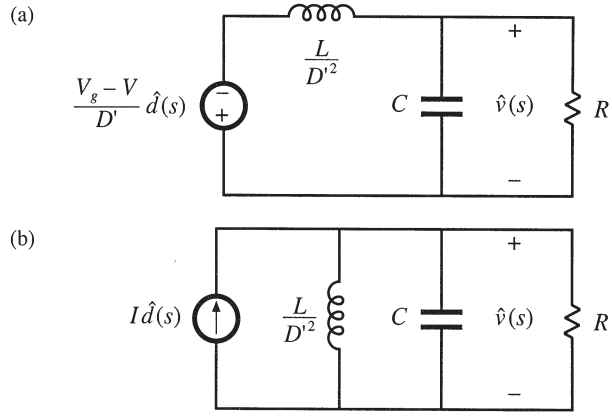


Fig. 8.32 Solution of the model of Fig. 8.32(b) by superposition: (a) current source set to zero; (b) voltage source set to zero.

$$G_{vd}(s) = \left(-\frac{V_g - V}{D'}\right)\frac{\left(R \parallel \frac{1}{sC}\right)}{\frac{sL}{D'^2} + \left(R \parallel \frac{1}{sC}\right)} + I\left(\frac{sL}{D'^2} \parallel R \parallel \frac{1}{sC}\right) \tag{8.124}$$

By algebraic manipulation, one can reduce this expression to

$$G_{vd}(s) = \left.\frac{\hat{v}(s)}{\hat{d}(s)}\right|_{\hat{v}_g(s)=0} = \left(-\frac{V_g - V}{D'}\right)\frac{\left(1 - s\frac{LI}{D'(V_g - V)}\right)}{\left(1 + s\frac{L}{D'^2R} + s^2\frac{LC}{D'^2}\right)} \tag{8.125}$$

This equation is of the form

$$G_{vd}(s) = G_{d0}\frac{\left(1 - \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)} \tag{8.126}$$

The denominators of Eq. (8.125) and (8.115) are identical, and hence $G_{vd}(s)$ and $G_{vg}(s)$ share the same ω_0 and Q, given by Eqs. (8.119) and (8.121). The dc gain is

$$G_{d0} = -\frac{V_g - V}{D'} = -\frac{V_g}{D'^2} = \frac{V}{DD'} \tag{8.127}$$

The angular frequency of the zero is found by equating coefficients of s in the numerators of Eqs. (8.125) and (8.126). One obtains

$$\omega_z = \frac{D'(V_g - V)}{LI} = \frac{D'^2R}{DL} \qquad \text{(RHP)} \tag{8.128}$$

This zero lies in the right half-plane. Equations (8.127) and (8.128) have been simplified by use of the dc relationships

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$$V = -\frac{D}{D'} V_g$$
$$I = -\frac{V}{D'R} \tag{8.129}$$

Equations (8.119), (8.121), (8.127), and (8.128) constitute the results of the analysis of the control-to-output transfer function: analytical expressions for the salient features ω_0, Q, G_{d0}, and ω_z. These expressions can be used to choose the element values such that given desired values of the salient features are obtained.

Having found analytical expressions for the salient features of the transfer functions, we can now plug in numerical values and construct the Bode plot. Suppose that we are given the following values:

$$\begin{aligned} D &= 0.6 \\ R &= 10\ \Omega \\ V_g &= 30\ \text{V} \\ L &= 160\ \mu\text{H} \\ C &= 160\ \mu\text{F} \end{aligned} \tag{8.130}$$

We can evaluate Eqs. (8.117), (8.119), (8.121), (8.127), and (8.128), to determine numerical values of the salient features of the transfer functions. The results are:

$$\begin{aligned} \left|G_{g0}\right| &= \frac{D}{D'} = 1.5 \Rightarrow 3.5\ \text{dB} \\ \left|G_{d0}\right| &= \frac{\left|V\right|}{DD'} = 187.5\ \text{V} \Rightarrow 45.5\ \text{dBV} \\ f_0 &= \frac{\omega_0}{2\pi} = \frac{D'}{2\pi\sqrt{LC}} = 400\ \text{Hz} \\ Q &= D'R\sqrt{\frac{C}{L}} = 4 \Rightarrow 12\ \text{dB} \\ f_z &= \frac{\omega_z}{2\pi} = \frac{D'^2 R}{2\pi DL} = 2.65\ \text{kHz} \end{aligned} \tag{8.131}$$

The Bode plot of the magnitude and phase of G_{vd} is constructed in Fig. 8.33. The transfer function contains a dc gain of 45.5 dBV, resonant poles at 400 Hz having a Q of $4 \Rightarrow 12$ dB, and a right half-plane zero at 2.65 kHz. The resonant poles contribute -180° to the high-frequency phase asymptote, while the right half-plane zero contributes -90°. In addition, the inverting characteristic of the buck-boost converter leads to a 180° phase reversal, not included in Fig. 8.33.

The Bode plot of the magnitude and phase of the line-to-output transfer function G_{vg} is constructed in Fig. 8.34. This transfer function contains the same resonant poles at 400 Hz, but is missing the right half-plane zero. The dc gain G_{g0} is equal to the conversion ratio $M(D)$ of the converter. Again, the 180° phase reversal, caused by the inverting characteristic of the buck-boost converter, is not included in Fig. 8.34.

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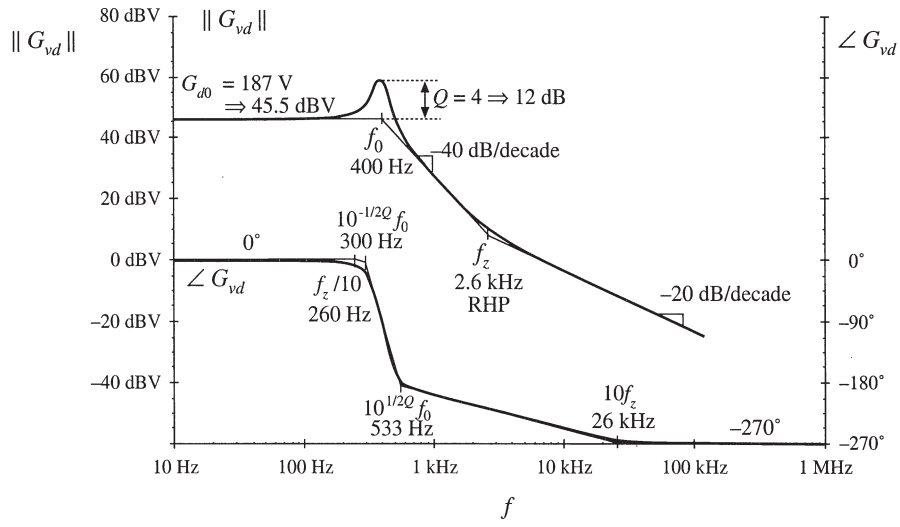


Fig. 8.33 Bode plot of the control-to-output transfer function G_{vd}, buck-boost converter example. Phase reversal owing to output voltage inversion is not included.

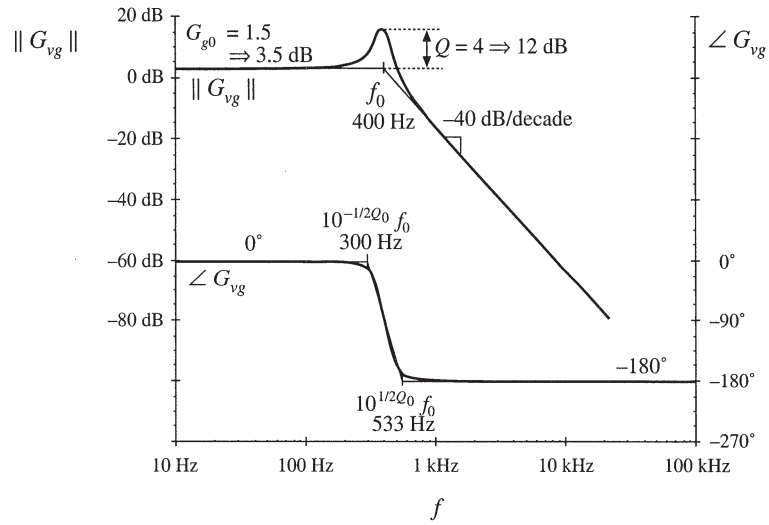


Fig. 8.34 Bode plot of the line-to-output transfer function G_{vg}, buck-boost converter example. Phase reversal owing to output voltage reversal is not included.

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Table 8.2 Salient features of the small-signal CCM transfer functions of some basic dc–dc converters

Converter	G_{g0}	G_{d0}	ω_0	Q	ω_z
Buck	D	$\frac{V}{D}$	$\frac{1}{\sqrt{LC}}$	$R\sqrt{\frac{C}{L}}$	∞
Boost	$\frac{1}{D'}$	$\frac{V}{D'}$	$\frac{D'}{\sqrt{LC}}$	$D'R\sqrt{\frac{C}{L}}$	$\frac{D'^2R}{L}$
Buck-boost	$-\frac{D}{D'}$	$\frac{V}{DD'}$	$\frac{D'}{\sqrt{LC}}$	$D'R\sqrt{\frac{C}{L}}$	$\frac{D'^2R}{DL}$

8.2.2 Transfer Functions of Some Basic CCM Converters

The salient features of the line-to-output and control-to-output transfer functions of the basic buck, boost, and buck-boost converters are summarized in Table 8.2. In each case, the control-to-output transfer function is of the form

$$G_{vd}(s) = G_{d0}\frac{\left(1-\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2\right)} \tag{8.132}$$

and the line-to-output transfer function is of the form

$$G_{vg}(s) = G_{g0}\frac{1}{1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2} \tag{8.133}$$

The boost and buck-boost converters exhibit control-to-output transfer functions containing two poles and a right half-plane zero. The buck converter $G_{vg}(s)$ exhibits two poles but no zero. The line-to-output transfer functions of all three ideal converters contain two poles and no zeroes.

These results can be easily adapted to transformer-isolated versions of the buck, boost, and buck-boost converters. The transformer has negligible effect on the transfer functions $G_{vg}(s)$ and $G_{vd}(s)$, other than introduction of a turns ratio. For example, when the transformer of the bridge topology is driven symmetrically, its magnetizing inductance does not contribute dynamics to the converter small-signal transfer functions. Likewise, when the transformer magnetizing inductance of the forward converter is reset by the input voltage v_g, as in Fig. 6.23 or 6.28, then it also contributes negligible dynamics. In all transformer-isolated converters based on the buck, boost, and buck-boost converters, the line-to-output transfer function $G_{vg}(s)$ should be multiplied by the transformer turns ratio; the transfer functions (8.132) and (8.133) and the parameters listed in Table 8.2 can otherwise be directly applied.

8.2.3 Physical Origins of the Right Half-Plane Zero in Converters

Figure 8.35 contains a block diagram that illustrates the behavior of the right half-plane zero. At low frequencies, the gain (s/ω_z) has negligible magnitude, and hence $u_{out} \approx u_{in}$. At high frequencies, where the

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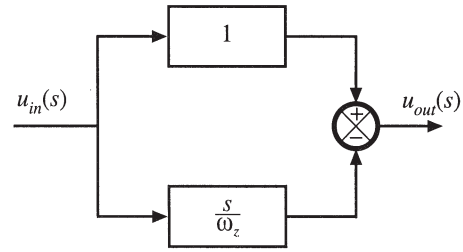


Fig. 8.35 Block diagram having a right half-plane zero transfer function, as in Eq. (8.32), with $\omega_0 = \omega_z$.

magnitude of the gain (s/ω_z) is much greater than 1, $u_{out} \approx -(s/\omega_z)u_{in}$. The negative sign causes a phase reversal at high frequency. The implication for the transient response is that the output initially tends in the opposite direction of the final value.

We have seen that the control-to-output transfer functions of the boost and buck-boost converters, Fig. 8.36, exhibit RHP zeroes. Typical transient response waveforms for a step change in duty cycle are illustrated in Fig. 8.37. For this example, the converter initially operates in equilibrium, at $d = 0.4$ and $d' = 0.6$. Equilibrium inductor current $i_L(t)$, diode current $i_D(t)$, and output voltage $v(t)$ waveforms are illustrated. The average diode current is

$$\langle i_D \rangle_{T_s} = d' \langle i_L \rangle_{T_s} \tag{8.134}$$

By capacitor charge balance, this average diode current is equal to the dc load current when the converter operates in equilibrium. At time $t = t_1$, the duty cycle is increased to 0.6. In consequence, d' decreases to 0.4. The average diode current, given by Eq. (8.134), therefore decreases, and the output capacitor begins to discharge. The output voltage magnitude initially decreases as illustrated.

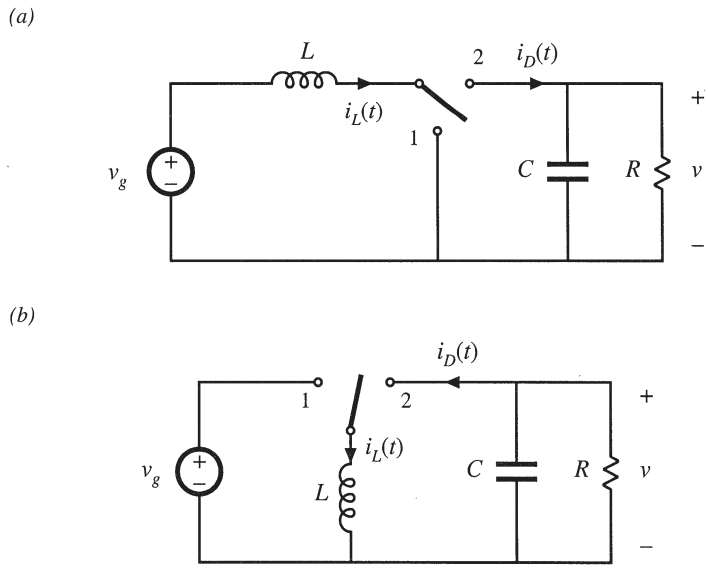


Fig. 8.36 Two basic converters whose CCM control-to-output transfer functions exhibit RHP zeroes: (a) boost, (b) buck-boost.

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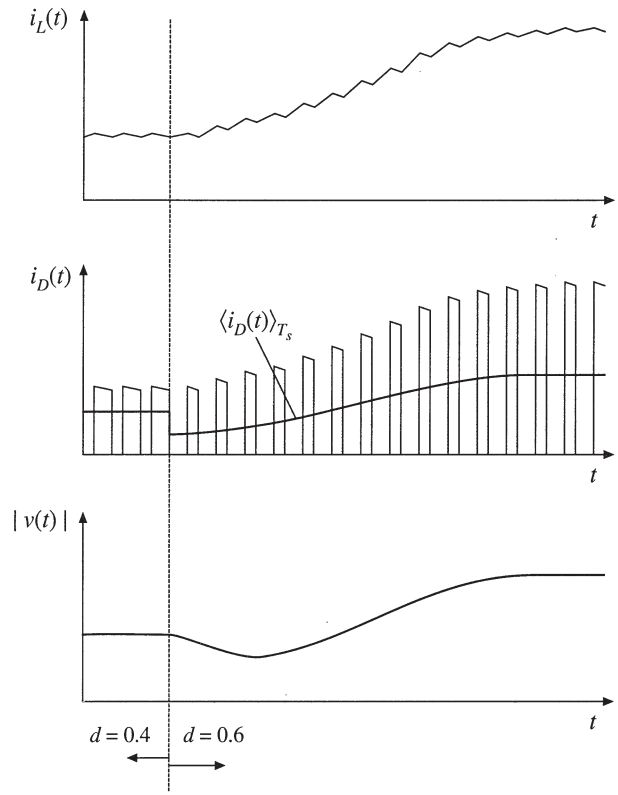


Fig. 8.37 Waveforms of the converters of Fig. 8.36, for a step response in duty cycle. The average diode current and output voltage initially decrease, as predicted by the RHP zero. Eventually, the inductor current increases, causing the average diode current and the output voltage to increase.

The increased duty cycle causes the inductor current to slowly increase, and hence the average diode current eventually exceeds its original $d = 0.4$ equilibrium value. The output voltage eventually increases in magnitude, to the new equilibrium value corresponding to $d = 0.6$.

The presence of a right half-plane zero tends to destabilize wide-bandwidth feedback loops, because during a transient the output initially changes in the wrong direction. The phase margin test for feedback loop stability is discussed in the next chapter; when a RHP zero is present, it is difficult to obtain an adequate phase margin in conventional single-loop feedback systems having wide bandwidth. Prediction of the right half-plane zero, and the consequent explanation of why the feedback loops controlling CCM boost and buck-boost converters tend to oscillate, was one of the early successes of averaged converter modeling.

8.3 GRAPHICAL CONSTRUCTION OF IMPEDANCES AND TRANSFER FUNCTIONS

Often, we can draw approximate Bode diagrams by inspection, without large amounts of messy algebra and the inevitable associated algebra mistakes. A great deal of insight can be gained into the operation of the circuit using this method. It becomes clear which components dominate the circuit response at various frequencies, and so suitable approximations become obvious. Analytical expressions for the approximate corner frequencies and asymptotes can be obtained directly. Impedances and transfer functions of quite complicated networks can be constructed. Thus insight can be gained, so that the design engineer

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can modify the circuit to obtain a desired frequency response.

The graphical construction method, also known as "doing algebra on the graph," involves use of a few simple rules for combining the magnitude Bode plots of impedances and transfer functions.

8.3.1 Series Impedances: Addition of Asymptotes

A series connection represents the addition of impedances. If the Bode diagrams of the individual impedance magnitudes are known, then the asymptotes of the series combination are found by simply taking the largest of the individual impedance asymptotes. In many cases, the result is exact. In other cases, such as when the individual asymptotes have the same slope, then the result is an approximation; nonetheless, the accuracy of the approximation can be quite good.

Consider the series-connected R–C network of Fig. 8.38. It is desired to construct the magnitude asymptotes of the total series impedance $Z(s)$, where

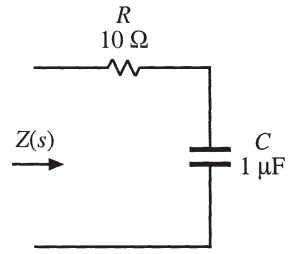


Fig. 8.38 Series R–C network example.

$$Z(s) = R + \frac{1}{sC} \tag{8.135}$$

Let us first sketch the magnitudes of the individual impedances. The 10 Ω resistor has an impedance magnitude of 10 Ω ⇒ 20 dBΩ. This value is independent of frequency, and is given in Fig. 8.39. The capacitor has an impedance magnitude of $1/\omega C$. This quantity varies inversely with ω, and hence its magnitude Bode plot is a line with slope –20 dB/decade. The line passes through 1 Ω ⇒ 0 dBΩ at the angular frequency ω where

$$\frac{1}{\omega C} = 1\ \Omega \tag{8.136}$$

that is, at

$$\omega = \frac{1}{(1\ \Omega)C} = \frac{1}{(1\ \Omega)(10^{-6}\ \text{F})} = 10^6\ \text{rad/sec} \tag{8.137}$$

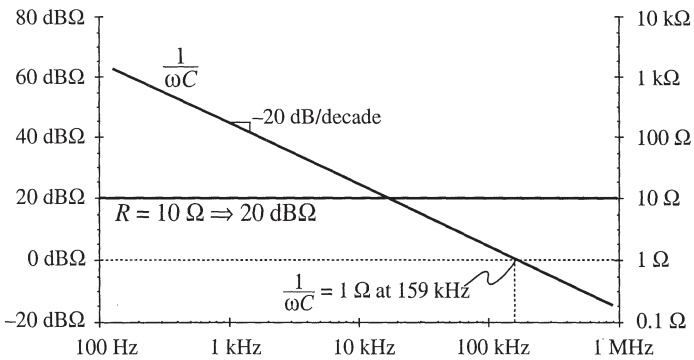


Fig. 8.39 Impedance magnitudes of the individual elements in the network of Fig. 8.38.

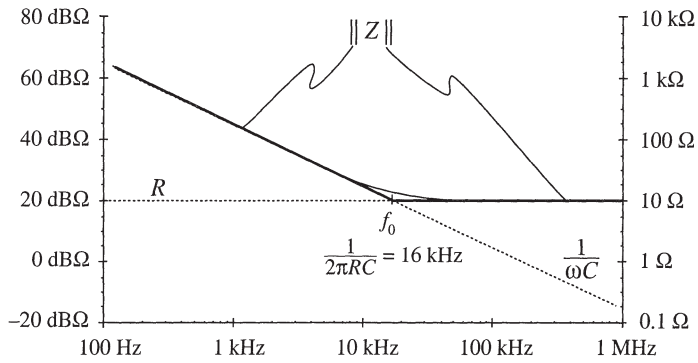


Fig. 8.40 Construction of the composite asymptotes of || *Z* ||. The asymptotes of the series combination can be approximated by simply selecting the larger of the individual resistor and capacitor asymptotes.

In terms of frequency *f*, this occurs at

$$f = \frac{\omega}{2\pi} = \frac{10^6}{2\pi} = 159 \text{ kHz} \tag{8.138}$$

So the capacitor impedance magnitude is a line with slope –20 dB/dec, and which passes through 0 dBΩ at 159 kHz, as shown in Fig. 8.39. It should be noted that, for simplicity, the asymptotes in Fig. 8.39 have been labeled *R* and $1/\omega C$. But to draw the Bode plot, we must actually plot dBΩ; for example, $20 \log_{10} (R/1\ \Omega)$ and $20 \log_{10} ((1/\omega C)/1\ \Omega)$.

Let us now construct the magnitude of $Z(s)$, given by Eq. (8.135). The magnitude of *Z* can be approximated as follows:

$$\left\| Z(j\omega) \right\| = \left\| R + \frac{1}{j\omega C} \right\| \approx \begin{cases} R & \text{for } R \gg 1/\omega C \\ \dfrac{1}{\omega C} & \text{for } R \ll 1/\omega C \end{cases} \tag{8.139}$$

The asymptotes of the series combination are simply the larger of the individual resistor and capacitor asymptotes, as illustrated by the heavy lines in Fig. 8.40. For this example, these are in fact the exact asymptotes of || *Z* ||. In the limiting case of zero frequency (dc), then the capacitor tends to an open circuit. The series combination is then dominated by the capacitor, and the exact function tends asymptotically to the capacitor impedance magnitude. In the limiting case of infinite frequency, then the capacitor tends to a short circuit, and the total impedance becomes simply *R*. So the *R* and $1/\omega C$ lines are the exact asymptotes for this example.

The corner frequency f_0, where the asymptotes intersect, can now be easily deduced. At angular frequency $\omega_0 = 2\pi f_0$, the two asymptotes are equal in value:

$$\frac{1}{\omega_0 C} = R \tag{8.140}$$

Solution for ω_0 and f_0 leads to:

$$\omega_0 = \frac{1}{RC} = \frac{1}{(10\ \Omega)(10^{-6}\ \text{F})} = 10^5\ \text{rad/sec}$$
$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi RC} = 16\ \text{kHz} \tag{8.141}$$

So if we can write analytical expressions for the asymptotes, then we can equate the expressions to find analytical expressions for the corner frequencies where the asymptotes intersect.

The deviation of the exact curve from the asymptotes follows all of the usual rules. The slope of the asymptotes changes by +20 dB/decade at the corner frequency f_0 (i.e., from −20 dBΩ/decade to 0 dBΩ/decade), and hence there is a zero at $f = f_0$. So the exact curve deviates from the asymptotes by +3 dBΩ at $f = f_0$, and by +1 dBΩ at $f = 2f_0$ and at $f = f_0/2$.

8.3.2 Series Resonant Circuit Example

As a second example, let us construct the magnitude asymptotes for the series *R–L–C* circuit of Fig. 8.41. The series impedance $Z(s)$ is

$$Z(s) = R + sL + \frac{1}{sC} \tag{8.142}$$

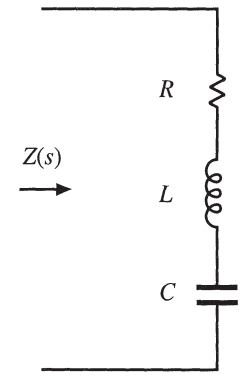


Fig. 8.41 Series *R–L–C* network example.

The magnitudes of the individual resistor, inductor, and capacitor asymptotes are plotted in Fig. 8.42, for the values

$$R = 1\ \text{k}\Omega$$
$$L = 1\ \text{mH} \tag{8.143}$$
$$C = 0.1\ \mu\text{F}$$

The series impedance $Z(s)$ is dominated by the capacitor at low frequency, by the resistor at mid frequencies, and by the inductor at high frequencies, as illustrated by the bold line in Fig. 8.42. The impedance $Z(s)$ contains a zero at angular frequency ω_1, where the capacitor and resistor asymptotes intersect. By equating the expressions for the resistor and capacitor asymptotes, we can find ω_1:

$$R = \frac{1}{\omega_1 C} \Rightarrow \omega_1 = \frac{1}{RC} \tag{8.144}$$

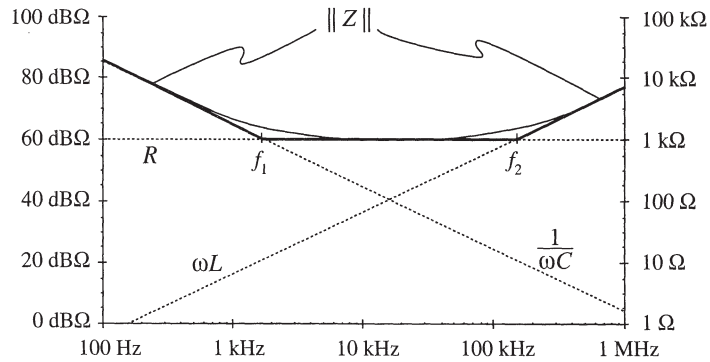


Fig. 8.42 Graphical construction of $\| Z \|$ of the series *R–L–C* network of Fig. 8.41, for the element values specified by Eq. (8.143).

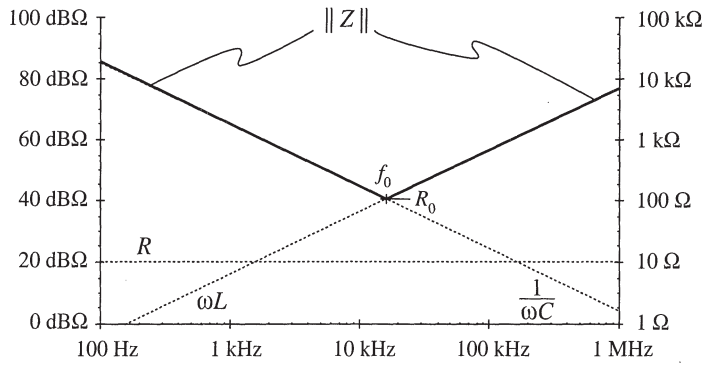


Fig. 8.43 Graphical construction of impedance asymptotes for the series R–L–C network example, with R decreased to 10 Ω.

A second zero occurs at angular frequency ω_2, where the inductor and resistor asymptotes intersect. Upon equating the expressions for the resistor and inductor asymptotes at ω_2, we obtain the following:

$$R = \omega_2 L \;\Rightarrow\; \omega_2 = \frac{R}{L} \tag{8.145}$$

So simple expressions for all important features of the magnitude Bode plot of $Z(s)$ can be obtained directly. It should be noted that Eqs. (8.144) and (8.145) are approximate, rather than exact, expressions for the corner frequencies ω_1 and ω_2. Equations (8.144) and (8.145) coincide with the results obtained via the low-Q approximation of Section 8.1.7.

Next, suppose that the value of R is decreased to 10 Ω. As R is reduced in value, the approximate corner frequencies ω_1 and ω_2 move closer together until, at R = 100 Ω, they are both 100 krad/sec. Reducing R further in value causes the asymptotes to become independent of the value of R, as illustrated in Fig. 8.43 for R = 10 Ω. The $\| Z \|$ asymptotes now switch directly from ωL to $1/\omega C$.

So now there are two zeroes at $\omega = \omega_0$. At corner frequency ω_0, the inductor and capacitor asymptotes are equal in value. Hence,

$$\omega_0 L = \frac{1}{\omega_0 C} = R_0 \tag{8.146}$$

Solution for the angular corner frequency ω_0 leads to

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{8.147}$$

At $\omega = \omega_0$, the inductor and capacitor impedances both have magnitude R_0, called the characteristic impedance.

Since there are two zeroes at $\omega = \omega_0$, there is a possibility that the two poles could be complex conjugates, and that peaking could occur in the vicinity of $\omega = \omega_0$. So let us investigate what the actual curve does at $\omega = \omega_0$. The actual value of the series impedance $Z(j\omega_0)$ is

$$Z(j\omega_0) = R + j\omega_0 L + \frac{1}{j\omega_0 C} \tag{8.148}$$

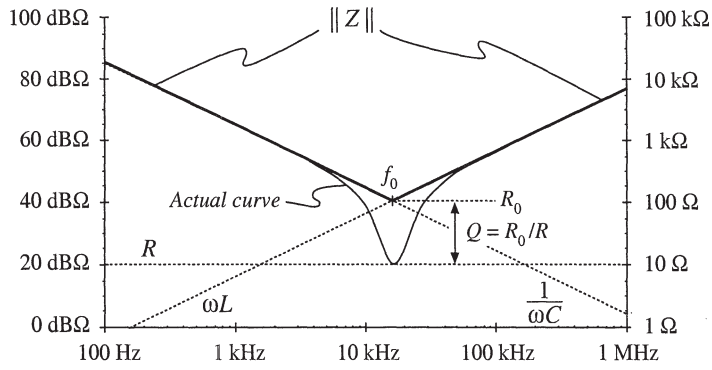


Fig. 8.44 Actual impedance magnitude (solid line) for the series resonant *R–L–C* example. The inductor and capacitor impedances cancel out at $f = f_0$, and hence $Z(j\omega_0) = R$.

Substitution of Eq. (8.146) into Eq. (8.148) leads to

$$Z(j\omega_0) = R + jR_0 + \frac{R_0}{j} = R + jR_0 - jR_0 = R \tag{8.149}$$

At $\omega = \omega_0$, the inductor and capacitor impedances are equal in magnitude but opposite in phase. Hence, they exactly cancel out in the series impedance, and we are left with $Z(j\omega_0) = R$, as illustrated in Fig. 8.44. The actual curve in the vicinity of the resonance at $\omega = \omega_0$ can deviate significantly from the asymptotes, because its value is determined by R rather than ωL or $1/\omega C$.

We know from Section 8.1.6 that the deviation of the actual curve from the asymptotes at $\omega = \omega_0$ is equal to Q. From Fig. 8.44, one can see that

$$|Q|_{\text{dB}} = |R_0|_{\text{dB}\Omega} - |R|_{\text{dB}\Omega} \tag{8.150}$$

or,

$$Q = \frac{R_0}{R} \tag{8.151}$$

Equations (8.146) to (8.151) are exact results for the series resonant circuit.

The practice of adding asymptotes by simply selecting the larger asymptote can be applied to transfer functions as well as impedances. For example, suppose that we have already constructed the magnitude asymptotes of two transfer functions, G_1 and G_2, and we wish to find the asymptotes of $G = G_1 + G_2$. At each frequency, the asymptote for G can be approximated by simply selecting the larger of the asymptotes for G_1 and G_2:

$$G = G_1 + G_2 \approx \begin{cases} G_1, & \|G_1\| \gg \|G_2\| \\ G_2, & \|G_2\| \gg \|G_1\| \end{cases} \tag{8.152}$$

Corner frequencies can be found by equating expressions for asymptotes as illustrated in the preceding examples. In the next chapter, we will see that this approach yields a simple and powerful method for determining the closed-loop transfer functions of feedback systems.

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8.3.3 Parallel Impedances: Inverse Addition of Asymptotes

A parallel combination represents inverse addition of impedances:

$$Z_{par} = \frac{1}{\frac{1}{Z_1} + \frac{1}{Z_2} + \cdots} \tag{8.153}$$

If the asymptotes of the individual impedances Z_1, Z_2, ..., are known, then the asymptotes of the parallel combination Z_{par} can be found by simply selecting the smallest individual impedance asymptote. This is true because the smallest impedance will have the largest inverse, and will dominate the inverse sum. As in the case of the series impedances, this procedure will often yield the exact asymptotes of Z_{par}.

Let us construct the magnitude asymptotes for the parallel *R–L–C* network of Fig. 8.45, using the following element values:

$$\begin{aligned} R &= 10\ \Omega \\ L &= 1\ \text{mH} \\ C &= 0.1\ \mu\text{F} \end{aligned} \tag{8.154}$$

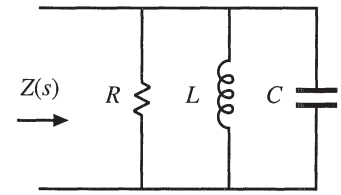


Fig. 8.45 Parallel *R–L–C* network example.

Impedance magnitudes of the individual elements are illustrated in Fig. 8.46. The asymptotes for the total parallel impedance Z are approximated by simply selecting the smallest individual element impedance, as shown by the heavy line in Fig. 8.46. So the parallel impedance is dominated by the inductor at low frequency, by the resistor at mid frequencies, and by the capacitor at high frequency. Approximate expressions for the angular corner frequencies are again found by equating asymptotes:

$$\begin{aligned} &\text{at } \omega = \omega_1, \quad R = \omega_1 L \ \Rightarrow\ \omega_1 = \frac{R}{L} \\ &\text{at } \omega = \omega_2, \quad R = \frac{1}{\omega_2 C} \ \Rightarrow\ \omega_2 = \frac{1}{RC} \end{aligned} \tag{8.155}$$

These expressions could have been obtained by conventional analysis, combined with the low-Q approximation of Section 8.1.7.

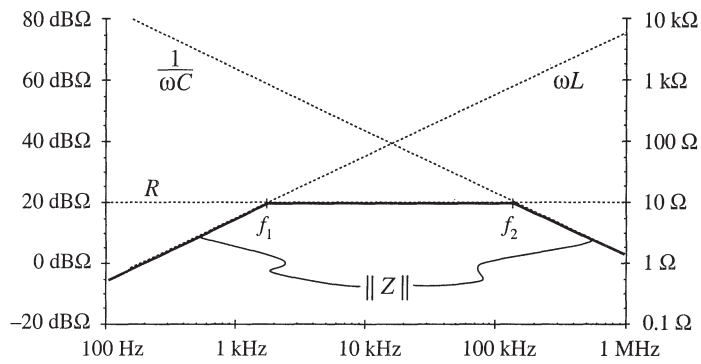


Fig. 8.46 Construction of the composite asymptotes of $\| Z \|$, for the parallel *R–L–C* example. The asymptotes of the parallel combination can be approximated by simply selecting the smallest of the individual resistor, inductor, and capacitor asymptotes.

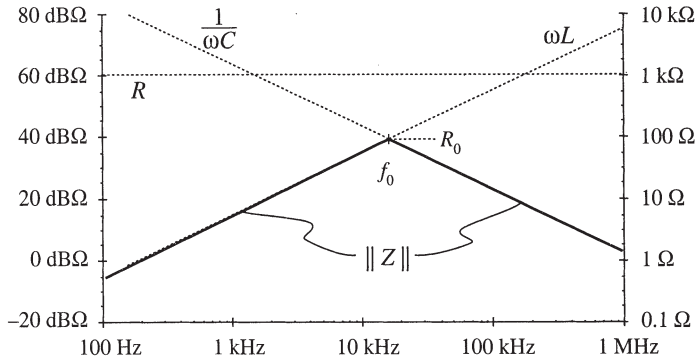


Fig. 8.47 Graphical construction of impedance asymptotes for the parallel *R–L–C* example, with *R* increased to 1 kΩ.

8.3.4 Parallel Resonant Circuit Example

Figure 8.47 illustrates what happens when the value of R in the parallel R–L–C network is increased to 1 kΩ. The asymptotes for $\| Z \|$ then become independent of R, and change directly from ωL to $1/\omega C$ at angular frequency ω_0. The corner frequency ω_0 is now the frequency where the inductor and capacitor asymptotes have equal value:

$$\omega_0 L = \frac{1}{\omega_0 C} = R_0 \tag{8.156}$$

which implies that

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{8.157}$$

At $\omega = \omega_0$, the slope of the asymptotes of $\| Z \|$ changes from +20 dB/decade to –20 dB/decade, and hence there are two poles. We should investigate whether peaking occurs, by determining the exact value of $\| Z \|$ at $\omega = \omega_0$, as follows:

$$Z(j\omega_0) = R \,\|\, j\omega_0 L \,\|\, \frac{1}{j\omega_0 C} = \frac{1}{\frac{1}{R} + \frac{1}{j\omega_0 L} + j\omega_0 C} \tag{8.158}$$

Substitution of Eq. (8.156) into (8.158) yields

$$Z(j\omega_0) = \frac{1}{\frac{1}{R} + \frac{1}{jR_0} + \frac{j}{R_0}} = \frac{1}{\frac{1}{R} - \frac{j}{R_0} + \frac{j}{R_0}} = R \tag{8.159}$$

So at $\omega = \omega_0$, the impedances of the inductor and capacitor again cancel out, and we are left with $Z(j\omega_0) = R$. The values of L and C determine the values of the asymptotes, but R determines the value of the actual curve at $\omega = \omega_0$.

The actual curve is illustrated in 8.48. The deviation of the actual curve from the asymptotes at $\omega = \omega_0$ is

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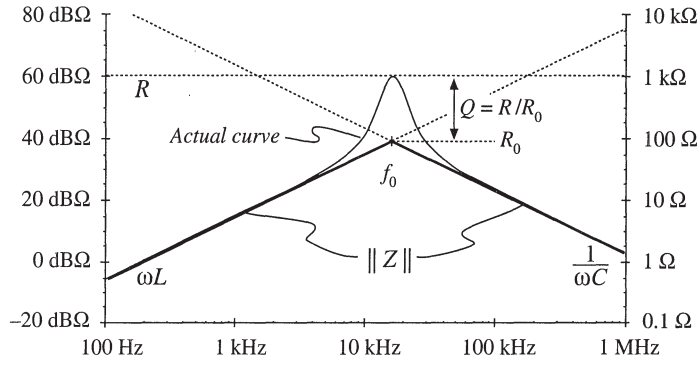


Fig. 8.48 Actual impedance magnitude (solid line) for the parallel *R–L–C* example. The inductor and capacitor impedances cancel out at $f = f_0$, and hence $Z(j\omega_0) = R$.

$$|Q|_{dB} = |R|_{dB\Omega} - |R_0|_{dB\Omega} \tag{8.160}$$

or,

$$Q = \frac{R}{R_0} \tag{8.161}$$

Equations (8.156) to (8.161) are exact results for the parallel resonant circuit.

The graphical construction method for impedance magnitudes is well known, and *reactance paper* can be purchased commercially. As illustrated in Fig. 8.49, the magnitudes of the impedances of various inductances, capacitances, and resistances are plotted on semilogarithmic axes. Asymptotes for the impedances of *R–L–C* networks can be sketched directly on these axes, and numerical values of corner frequencies can then be graphically determined.

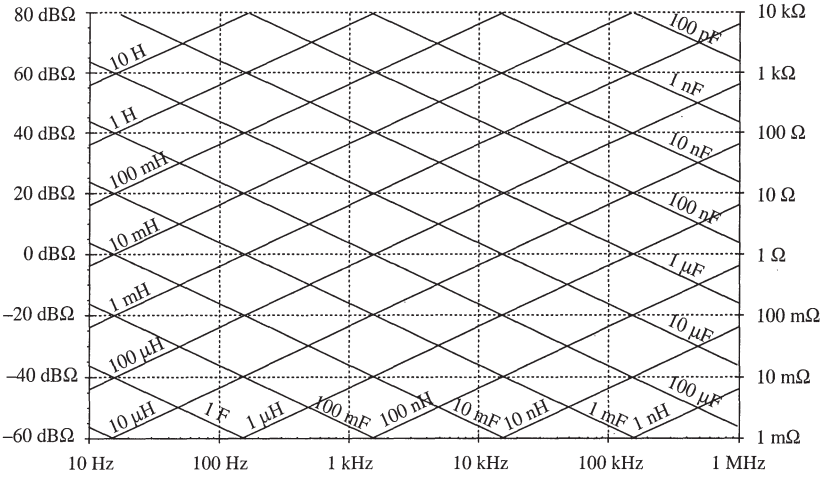


Fig. 8.49 "Reactance paper": an aid for graphical construction of impedances, with the magnitudes of various inductive, capacitive, and resistive impedances preplotted.

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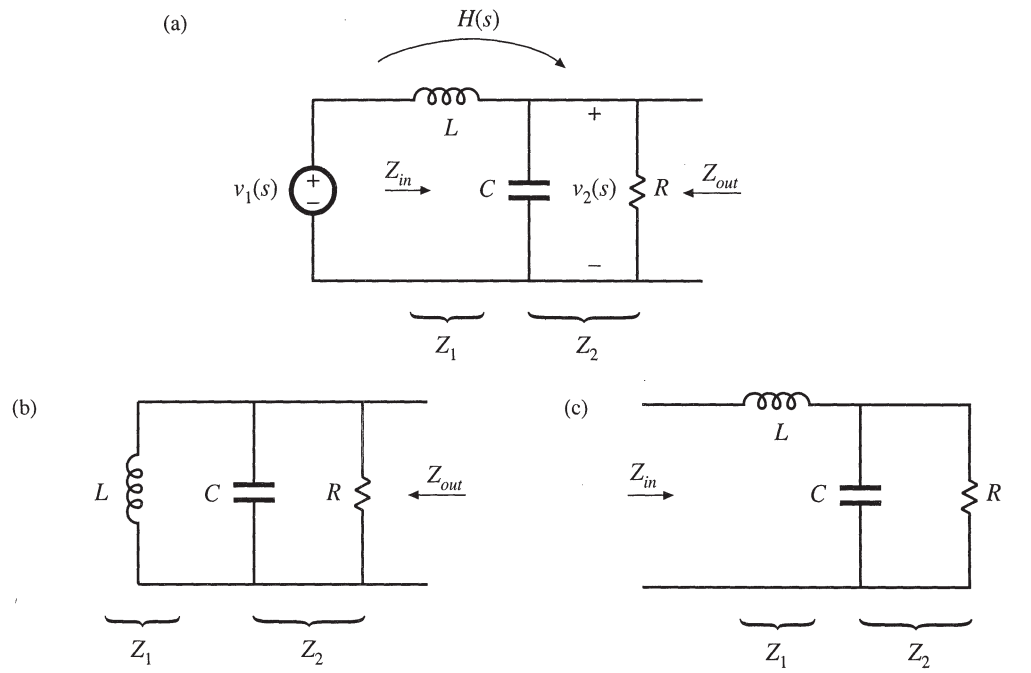


Fig. 8.50 Two-pole low-pass filter based on voltage divider circuit: (a) transfer function $H(s)$, (b) determination of Z_{out}, by setting independent sources to zero, (c) determination of $Z_{in}(s)$.

8.3.5 Voltage Divider Transfer Functions: Division of Asymptotes

Usually, we can express transfer functions in terms of impedances—for example, as the ratio of two impedances. If we can construct these impedances as described in the previous sections, then we can divide to construct the transfer function. In this section, construction of the transfer function $H(s)$ of the two-pole *R–L–C* low-pass filter (Fig. 8.50) is discussed in detail. A filter of this form appears in the canonical model for two-pole converters, and the results of this section are applied in the converter examples of the next section.

The familiar voltage divider formula shows that the transfer function of this circuit can be expressed as the ratio of impedances Z_2/Z_{in}, where $Z_{in} = Z_1 + Z_2$ is the network input impedance:

$$\frac{\hat{v}_2(s)}{\hat{v}_1(s)} = \frac{Z_2}{Z_1 + Z_2} = \frac{Z_2}{Z_{in}} \tag{8.162}$$

For this example, $Z_1(s) = sL$, and $Z_2(s)$ is the parallel combination of R and $1/sC$. Hence, we can find the transfer function asymptotes by constructing the asymptotes of Z_2 and of the series combination represented by Z_{in}, and then dividing. Another approach, which is easier to apply in this example, is to multiply the numerator and denominator of Eq. (8.162) by Z_1:

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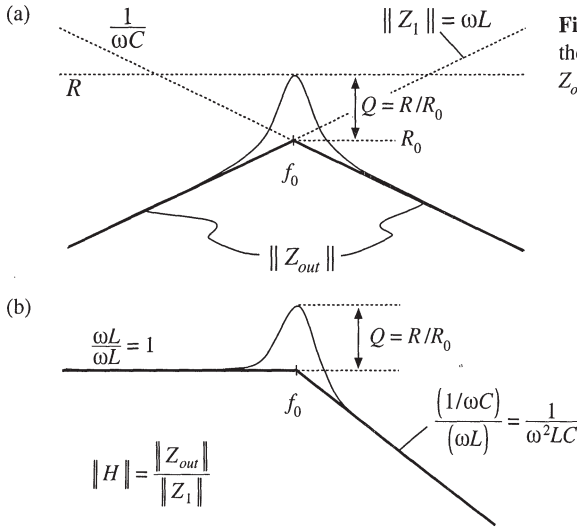


Fig. 8.51 Graphical construction of H and Z_{out} of the voltage divider circuit: (a) output impedance Z_{out}; (b) transfer function H.

$$\frac{\hat{v}_2(s)}{\hat{v}_1(s)} = \frac{Z_2 Z_1}{Z_1 + Z_2} \frac{1}{Z_1} = \frac{Z_{out}}{Z_1} \tag{8.163}$$

where $Z_{out} = Z_1 \| Z_2$ is the output impedance of the voltage divider. So another way to construct the voltage divider transfer function is to first construct the asymptotes for Z_1 and for the parallel combination represented by Z_{out}, and then divide. This method is useful when the parallel combination $Z_1 \| Z_2$ is easier to construct than the series combination $Z_1 + Z_2$. It often gives a different approximate result, which may be more (or sometimes less) accurate than the result obtained using Z_{in}.

The output impedance Z_{out} in Fig. 8.50(b) is

$$Z_{out}(s) = R \| \frac{1}{sC} \| sL \tag{8.164}$$

The impedance of the parallel *R–L–C* network is constructed in Section 8.3.3, and is illustrated in Fig. 8.51(a) for the high-Q case.

According to Eq. (8.163), the voltage divider transfer function magnitude is $\| H \| = \| Z_{out} \| / \| Z_1 \|$. This quantity is constructed in Fig. 8.51(b). For $\omega < \omega_0$, the asymptote of $\| Z_{out} \|$ coincides with $\| Z_1 \|$: both are equal to ωL. Hence, the ratio is $\| Z_{out} \| / \| Z_1 \| = 1$. For $\omega > \omega_0$, the asymptote of $\| Z_{out} \|$ is $1/\omega C$, while $\| Z_1 \|$ is equal to ωL. The ratio then becomes $\| Z_{out} \| / \| Z_1 \| = 1/\omega^2 LC$, and hence the high-

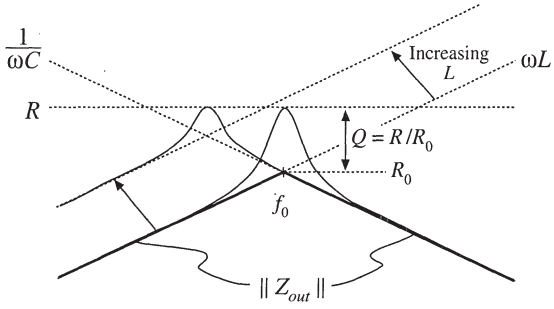


Fig. 8.52 Effect of increasing L on the output impedance asymptotes, corner frequency, and Q-factor.

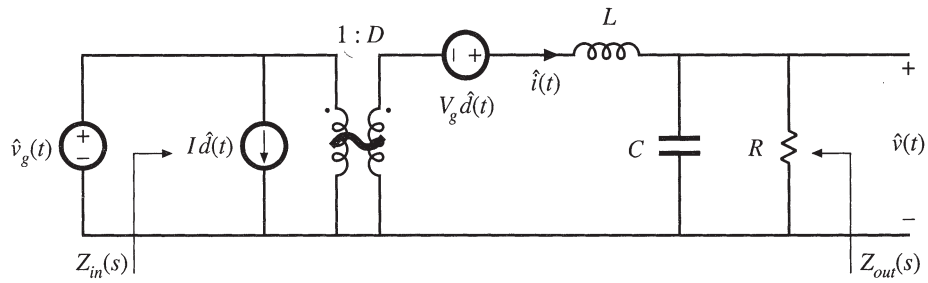


Fig. 8.53 Small-signal model of the buck converter, with input impedance $Z_{in}(s)$ and output impedance $Z_{out}(s)$ explicitly defined.

frequency asymptote has a –40 dB/decade slope. At $\omega = \omega_0$, $\| Z_{out} \|$ has exact value R, while $\| Z_1 \|$ has exact value R_0. The ratio is then $\| H(j\omega_0) \| = \| Z_{out}(j\omega_0) \| / \| Z_1(j\omega_0) \| = R/R_0 = Q$. So the filter transfer function H has the same ω_0 and Q as the impedance Z_{out}.

It now becomes obvious how variations in element values affect the salient features of the transfer function and output impedance. For example, the effect of increasing L is illustrated in Fig. 8.52. This causes the angular resonant frequency ω_0 to be reduced, and also reduces the Q-factor.

8.4 GRAPHICAL CONSTRUCTION OF CONVERTER TRANSFER FUNCTIONS

The small-signal equivalent circuit model of the buck converter, derived in Chapter 7, is reproduced in Fig. 8.53. Let us construct the transfer functions and terminal impedances of this converter, using the graphical approach of the previous section.

The output impedance $Z_{out}(s)$ is found with the $\hat{d}(s)$ and $\hat{v}_g(s)$ sources set to zero; the circuit of Fig. 8.54(a) is then obtained. This model coincides with the parallel R–L–C circuit analyzed in Sections 8.3.3 and 8.3.4. As illustrated in Fig. 8.54(b), the output impedance is dominated by the inductor at low frequency, and by the capacitor at high frequency. At the resonant frequency f_0, given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{8.165}$$

the output impedance is equal to the load resistance R. The Q-factor of the circuit is equal to

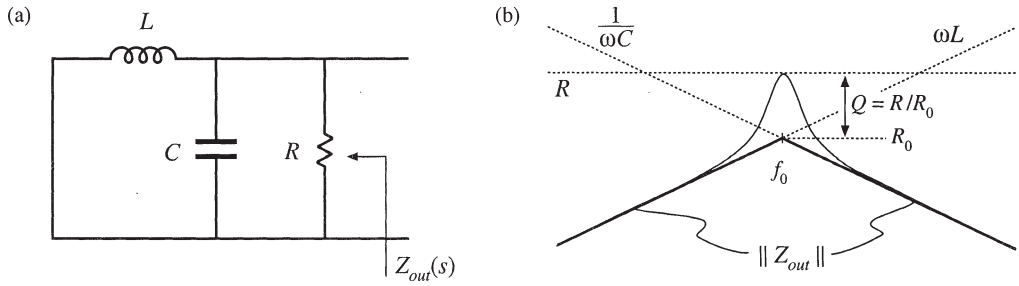


Fig. 8.54 Construction of buck converter output impedance $Z_{out}(s)$: (a) circuit model; (b) impedance asymptotes.

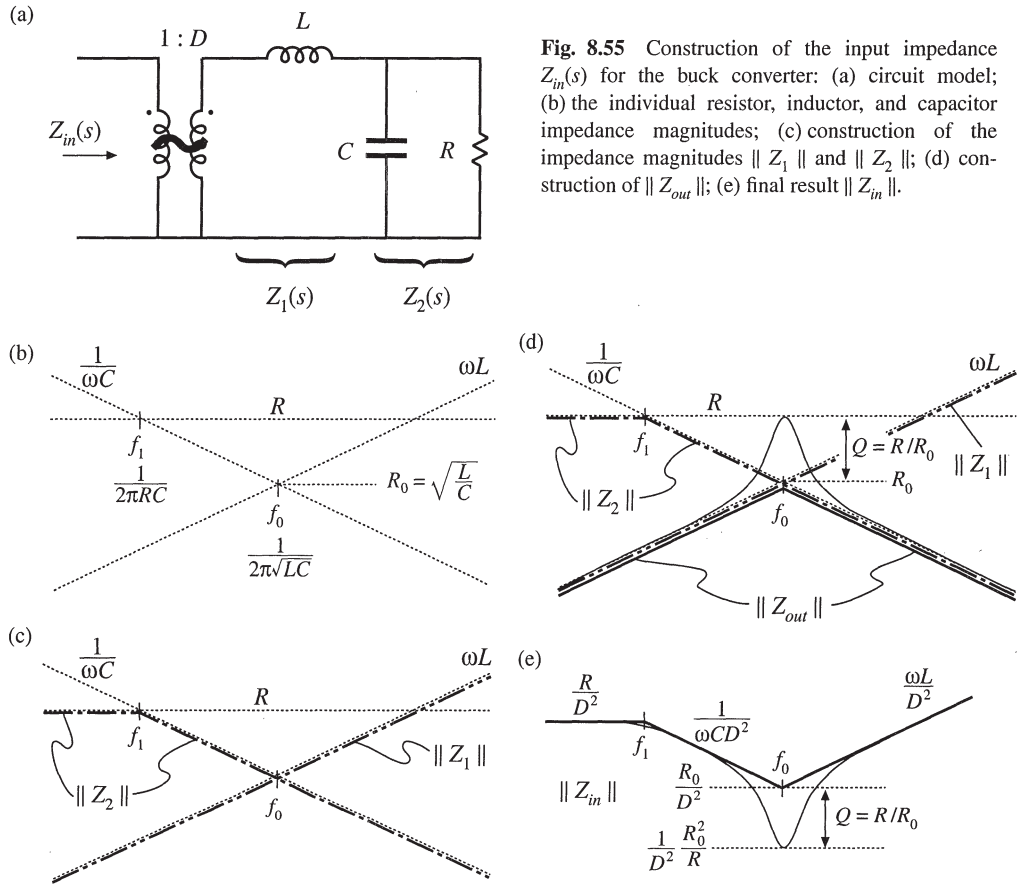


Fig. 8.55 Construction of the input impedance $Z_{in}(s)$ for the buck converter: (a) circuit model; (b) the individual resistor, inductor, and capacitor impedance magnitudes; (c) construction of the impedance magnitudes $\| Z_1 \|$ and $\| Z_2 \|$; (d) construction of $\| Z_{out} \|$; (e) final result $\| Z_{in} \|$.

$$Q = \frac{R}{R_0} \tag{8.166}$$

where

$$R_0 = \omega_0 L = \frac{1}{\omega_0 C} = \sqrt{\frac{L}{C}} \tag{8.167}$$

Thus, the circuit is lightly damped (high Q) at light load, where the value of R is large.

The converter input impedance $Z_{in}(s)$ is also found with the $\hat{d}(s)$ and $\hat{v}_g(s)$ sources set to zero, as illustrated in Fig. 8.55(a). The input impedance is referred to the primary side of the 1:D transformer, and is equal to

$$Z_{in}(s) = \frac{1}{D^2}\left[Z_1(s) + Z_2(s)\right] \tag{8.168}$$

where

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$$Z_1(s) = sL \tag{8.169}$$

and

$$Z_2(s) = R \parallel \frac{1}{sC} \tag{8.170}$$

We begin construction of the impedance asymptotes corresponding to Eqs. (8.168) to (8.170) by constructing the individual resistor, capacitor, and inductor impedances as in Fig. 8.55(b). The impedances in Fig. 8.55 are constructed for the case $R > R_0$. As illustrated in Fig. 8.55(c), $\| Z_1 \|$ coincides with the inductor reactance ωL. The impedance $\| Z_2 \|$ is asymptotic to resistance R at low frequencies, and to the capacitor reactance $1/\omega C$ at high frequency. The resistor and capacitor asymptotes intersect at corner frequency f_1, given by

$$f_1 = \frac{1}{2\pi RC} \tag{8.171}$$

According to Eq. (8.168), the input impedance $Z_{in}(s)$ is equal to the series combination of $Z_1(s)$ and $Z_2(s)$, divided by the square of the turns ratio D. The asymptotes for the series combination $[Z_1(s) + Z_2(s)]$ are found by selecting the larger of the $\| Z_1 \|$ and $\| Z_2 \|$ asymptotes. The $\| Z_1 \|$ and $\| Z_2 \|$ asymptotes intersect at frequency f_0, given by Eq. (8.165). It can be seen from Fig. 8.55(c) that the series combination is dominated by Z_2 for $f < f_0$, and by Z_1 for $f > f_0$. Upon scaling the $[Z_1(s) + Z_2(s)]$ asymptotes by the factor $1/D^2$, the input impedance asymptotes of Fig. 8.55(e) are obtained.

The zeroes of $Z_{in}(s)$, at frequency f_0, have the same Q-factor as the poles of $Z_{out}(s)$ [Eq. (8.166)]. One way to see that this is true is to note that the output impedance can be expressed as

$$Z_{out}(s) = \frac{Z_1(s)Z_2(s)}{Z_1(s) + Z_2(s)} = \frac{Z_1(s)Z_2(s)}{D^2 Z_{in}(s)} \tag{8.172}$$

Hence, we can relate $Z_{out}(s)$ to $Z_{in}(s)$ as follows:

$$Z_{in}(s) = \frac{1}{D^2} \frac{Z_1(s)Z_2(s)}{Z_{out}(s)} \tag{8.173}$$

The impedances $\| Z_1 \|$, $\| Z_2 \|$, and $\| Z_{out} \|$ are illustrated in Fig. 8.55(d). At the resonant frequency $f = f_0$, impedance Z_1 has magnitude R_0 and impedance Z_2 has magnitude approximately equal to R_0. The output impedance Z_{out} has magnitude R. Hence, Eq. (8.173) predicts that the input impedance has the magnitude

$$\| Z_{in} \| \approx \frac{1}{D^2} \frac{R_0 R_0}{R} \quad \text{at } f = f_0 \tag{8.174}$$

At $f = f_0$, the asymptotes of the input impedance have magnitude R_0/D^2. The deviation from the asymptotes is therefore equal to $Q = R/R_0$, as illustrated in Fig. 8.55(e).

The control-to-output transfer function $G_{vd}(s)$ is found with the $\hat{v}_g(s)$ source set to zero, as in Fig. 8.56(a). This circuit coincides with the voltage divider analyzed in Section 8.3.5. Hence, $G_{vd}(s)$ can be expressed as

$$G_{vd}(s) = V_g \frac{Z_{out}(s)}{Z_1(s)} \tag{8.175}$$

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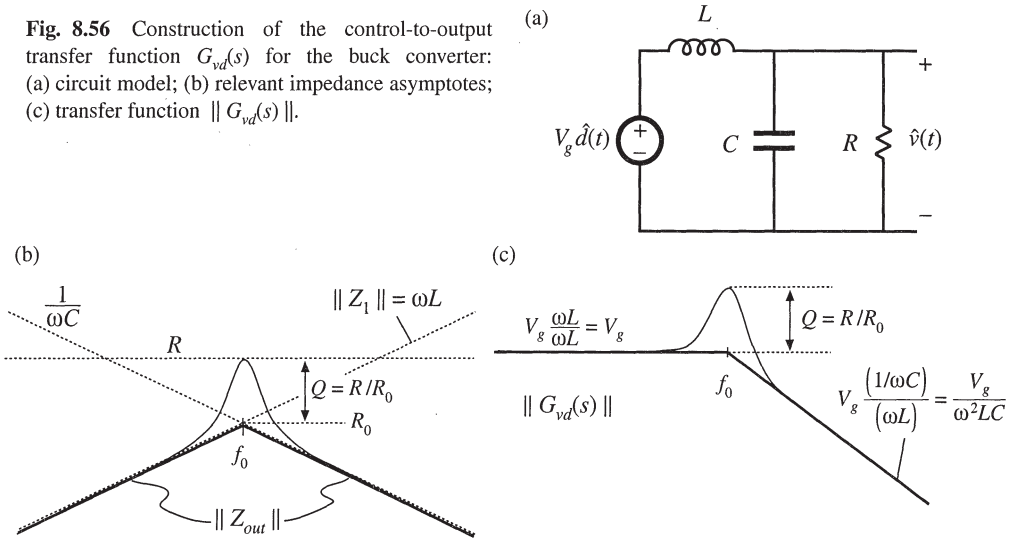


Fig. 8.56 Construction of the control-to-output transfer function $G_{vd}(s)$ for the buck converter: (a) circuit model; (b) relevant impedance asymptotes; (c) transfer function $\| G_{vd}(s) \|$.

The quantities $\| Z_{out} \|$ and $\| Z_1 \|$ are constructed in Fig. 8.56(b). According to Eq. (8.175), we can construct $\| G_{vd}(s) \|$ by finding the ratio of $\| Z_{out} \|$ and $\| Z_1 \|$, and then scaling the result by V_g. For $f < f_0$, $\| Z_{out} \|$ and $\| Z_1 \|$ are both equal to ωL and hence $\| Z_{out} \| / \| Z_1 \|$ is equal to 1. As illustrated in Fig. 8.56(c), the low-frequency asymptote of $\| G_{vd}(s) \|$ has value V_g. For $f > f_0$, $\| Z_{out} \|$ has asymptote $1/\omega C$, and $\| Z_1 \|$ is equal to ωL. Hence, $\| Z_{out} \| / \| Z_1 \|$ has asymptote $1/\omega^2 LC$, and the high-frequency asymptote of $\| G_{vd}(s) \|$ is equal to $V_g/\omega^2 LC$. The Q-factor of the two poles at $f = f_0$ is again equal to R/R_0.

The line-to-output transfer function $G_{vg}(s)$ is found with the $\hat{d}(s)$ sources set to zero, as in Fig. 8.57(a). This circuit contains the same voltage divider as in Fig. 8.56, and additionally contains the $1{:}D$ transformer. The transfer function $G_{vg}(s)$ can be expressed as

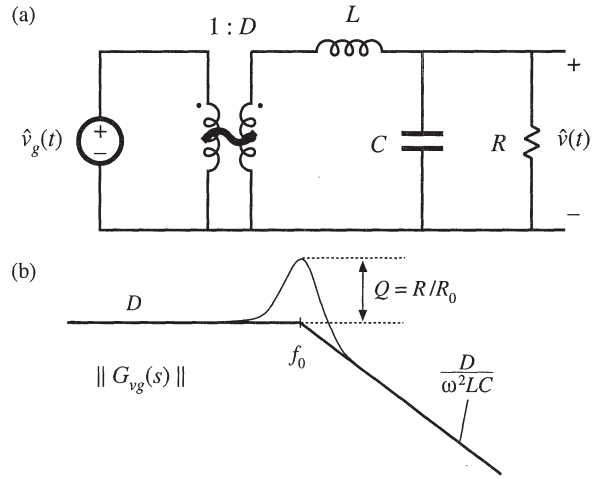


Fig. 8.57 The line-to-output transfer function $G_{vg}(s)$ for the buck converter: (a) circuit model; (b) magnitude asymptotes.

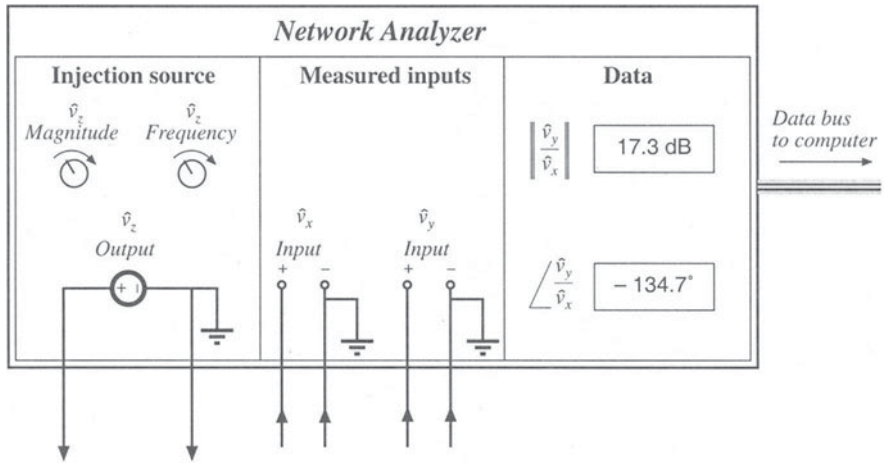


Fig. 8.58 Key features and functions of a network analyzer: sinusoidal source of controllable amplitude and frequency, two inputs, and determination of relative magnitude and phase of the input components at the injection frequency.

$$G_{vg}(s) = D\frac{Z_{out}(s)}{Z_1(s)} \tag{8.176}$$

This expression is similar to Eq. (8.175), except for the scaling factor of D. Therefore, the line-to-output transfer function of Fig. 8.57(b) has the same shape as the control-to-output transfer function $G_{vd}(s)$.

8.5 MEASUREMENT OF AC TRANSFER FUNCTIONS AND IMPEDANCES

It is good engineering practice to measure the transfer functions of prototype converters and converter systems. Such an exercise can verify that the system has been correctly modeled and designed. Also, it is often useful to characterize individual circuit elements through measurement of their terminal impedances.

Small-signal ac magnitude and phase measurements can be made using an instrument known as a network analyzer, or frequency response analyzer. The key inputs and outputs of a basic network analyzer are illustrated in Fig. 8.58. The network analyzer provides a sinusoidal output voltage $\hat{v}_z$ of controllable amplitude and frequency. This signal can be injected into the system to be measured, at any desired location. The network analyzer also has two (or more) inputs, $\hat{v}_x$ and $\hat{v}_y$. The return electrodes of $\hat{v}_z$, $\hat{v}_y$, and $\hat{v}_x$ are internally connected to earth ground. The network analyzer performs the function of a narrowband tracking voltmeter: it measures the components of $\hat{v}_x$ and $\hat{v}_y$ at the injection frequency, and displays the magnitude and phase of the quantity $\hat{v}_y/\hat{v}_x$. The narrowband tracking voltmeter feature is essential for switching converter measurements; otherwise, switching ripple and noise corrupt the desired sinusoidal signals and make accurate measurements impossible [3]. Modern network analyzers can automatically sweep the frequency of the injection source $\hat{v}_z$ to generate magnitude and phase Bode plots of the transfer function $\hat{v}_y/\hat{v}_x$.

A typical test setup for measuring the transfer function of an amplifier is illustrated in Fig. 8.59. A potentiometer, connected between a dc supply voltage V_{CC} and ground, is used to bias the

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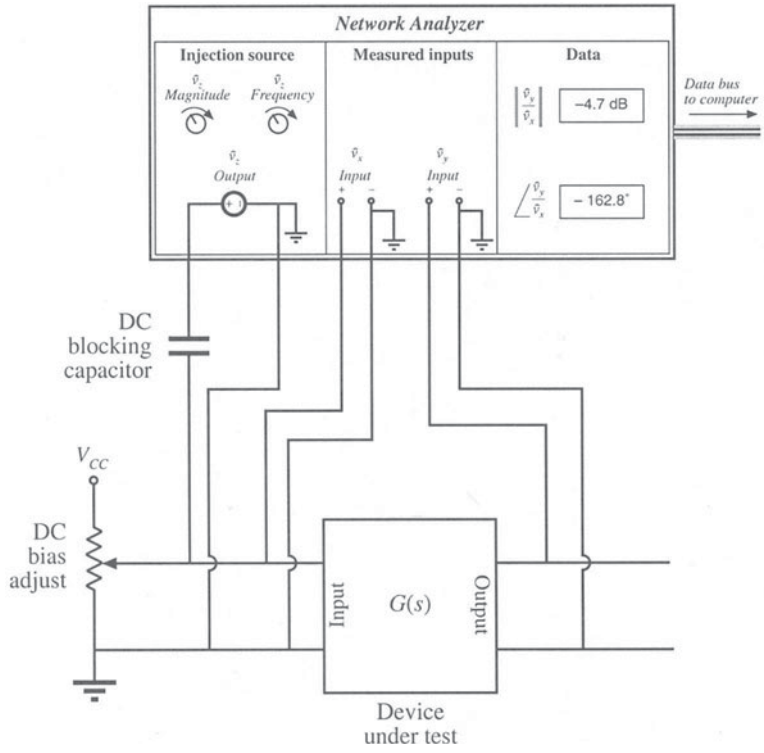


Fig. 8.59 Measurement of a transfer function.

amplifier input to attain the correct quiescent operating point. The injection source voltage $\hat{v}_z$ is coupled to the amplifier input terminals via a dc blocking capacitor. This blocking capacitor prevents the injection voltage source from upsetting the dc bias. The network analyzer inputs $\hat{v}_x$ and $\hat{v}_y$ are connected to the input and output terminals of the amplifier. Hence, the measured transfer function is

$$\frac{\hat{v}_y(s)}{\hat{v}_x(s)} = G(s) \tag{8.177}$$

Note that the blocking capacitance, bias potentiometer, and $\hat{v}_z$ amplitude have no effect on the measured transfer function

An impedance

$$Z(s) = \frac{\hat{v}(s)}{\hat{i}(s)} \tag{8.178}$$

can be measured by treating the impedance as a transfer function from current to voltage. For example, measurement of the output impedance of an amplifier is illustrated in Fig. 8.60. The quiescent operating condition is again established by a potentiometer which biases the amplifier input. The injection source $\hat{v}_z$ is coupled to the amplifier output through a dc blocking capacitor. The injection source voltage $\hat{v}_z$ excites a current $\hat{i}_{out}$ in impedance Z_s. This current flows into the output of the amplifier, and excites a

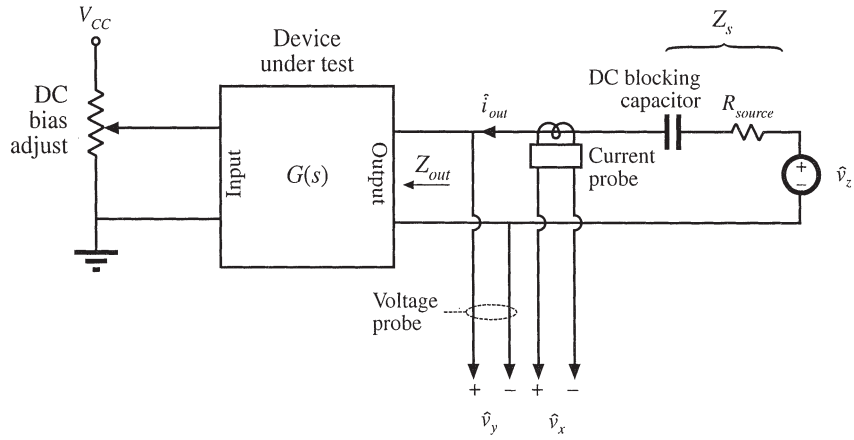


Fig. 8.60 Measurement of the output impedance of a circuit.

voltage across the amplifier output impedance:

$$Z_{out}(s) = \left.\frac{\hat{v}_y(s)}{\hat{i}_{out}(s)}\right|_{\substack{amplifier\\ ac\ input = 0}} \tag{8.179}$$

A current probe is used to measure $\hat{i}_{out}$. The current probe produces a voltage proportional to $\hat{i}_{out}$; this voltage is connected to the network analyzer input $\hat{v}_x$. A voltage probe is used to measure the amplifier output voltage $\hat{v}_y$. The network analyzer displays the transfer function $\hat{v}_y/\hat{v}_x$, which is proportional to Z_{out}. Note that the value of Z_s and the amplitude of $\hat{v}_z$ do not affect the measurement of Z_{out}.

In power applications, it is sometimes necessary to measure impedances that are very small in magnitude. Grounding problems[4] cause the test setup of Fig. 8.60 to fail in such cases. The reason is illustrated in Fig. 8.61(a). Since the return connections of the injection source $\hat{v}_z$ and the analyzer input $\hat{v}_y$ are both connected to earth ground, the injected current $\hat{i}_{out}$ can return to the source through the return connections of either the injection source or the voltage probe. In practice, $\hat{i}_{out}$ divides between the two paths according to their relative impedances. Hence, a significant current $(1 - k)\,\hat{i}_{out}$ flows through the return connection of the voltage probe. If the voltage probe return connection has some total contact and wiring impedance Z_{probe}, then the current induces a voltage drop $(1 - k)\hat{i}_{out}Z_{probe}$ in the voltage probe wiring, as illustrated in Fig. 8.61(a). Hence, the network analyzer does not correctly measure the voltage drop across the impedance Z. If the internal ground connections of the network analyzer have negligible impedance, then the network analyzer will display the following impedance:

$$Z + (1 - k)Z_{probe} = Z + Z_{probe} \| Z_{rz} \tag{8.180}$$

Here, Z_{rz} is the impedance of the injection source return connection. So to obtain an accurate measurement, the following condition must be satisfied:

$$\|Z\| \gg \left\| \left(Z_{probe} \| Z_{rz} \right) \right\| \tag{8.181}$$

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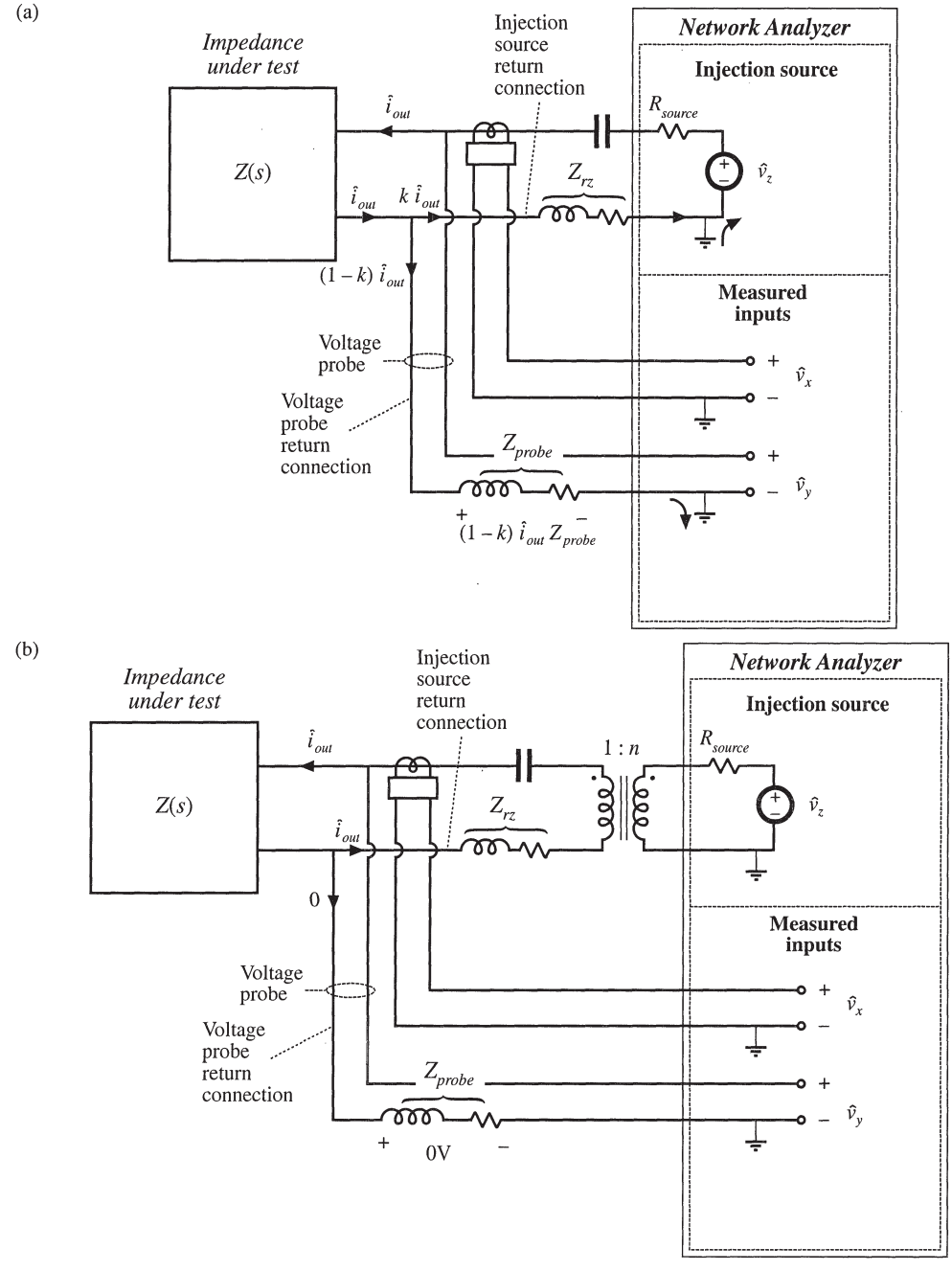


Fig. 8.61 Measurement of a small impedance $Z(s)$: (a) current flowing in the return connection of the voltage probe induces a voltage drop that corrupts the measurement; (b) an improved experiment, incorporating isolation of the injection source.

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