A typical lower limit on $\| Z \|$ is a few tens or hundreds of milliohms.

An improved test setup for measurement of small impedances is illustrated in Fig. 8.61(b). An isolation transformer is inserted between the injection source and the dc blocking capacitor. The return connections of the voltage probe and injection source are no longer in parallel, and the injected current $\hat{i}_{out}$ must now return entirely through the injection source return connection. An added benefit is that the transformer turns ratio n can be increased, to better match the injection source impedance to the impedance under test. Note that the impedances of the transformer, of the blocking capacitor, and of the probe and injection source return connections, do not affect the measurement. Much smaller impedances can therefore be measured using this improved approach.

8.6 SUMMARY OF KEY POINTS

1. The magnitude Bode diagrams of functions which vary as $(f/f_0)^n$ have slopes equal to $20n$ dB per decade, and pass through 0 dB at $f = f_0$.
2. It is good practice to express transfer functions in normalized pole-zero form; this form directly exposes expressions for the salient features of the response, that is, the corner frequencies, reference gain, etc.
3. The right half-plane zero exhibits the magnitude response of the left half-plane zero, but the phase response of the pole.
4. Poles and zeroes can be expressed in frequency-inverted form, when it is desirable to refer the gain to a high-frequency asymptote.
5. A two-pole response can be written in the standard normalized form of Eq. (8.58). When $Q > 0.5$, the poles are complex conjugates. The magnitude response then exhibits peaking in the vicinity of the corner frequency, with an exact value of Q at $f = f_0$. High Q also causes the phase to change sharply near the corner frequency.
6. When Q is less than 0.5, the two pole response can be plotted as two real poles. The low-Q approximation predicts that the two poles occur at frequencies f_0/Q and Qf_0. These frequencies are within 10% of the exact values for $Q \leq 0.3$.
7. The low-Q approximation can be extended to find approximate roots of an arbitrary degree polynomial. Approximate analytical expressions for the salient features can be derived. Numerical values are used to justify the approximations.
8. Salient features of the transfer functions of the buck, boost, and buck-boost converters are tabulated in Section 8.2.2. The line-to-output transfer functions of these converters contain two poles. Their control-to-output transfer functions contain two poles, and may additionally contain a right half-plane zero.
9. Approximate magnitude asymptotes of impedances and transfer functions can be easily derived by graphical construction. This approach is a useful supplement to conventional analysis, because it yields physical insight into the circuit behavior, and because it exposes suitable approximations. Several examples, including the impedances of basic series and parallel resonant circuits and the transfer function $H(s)$ of the voltage divider circuit, are worked in Section 8.3. The input impedance, output impedance, and transfer functions of the buck converter are constructed in Section 8.4, and physical origins of the asymptotes, corner frequencies, and Q-factor are found.
10. Measurement of transfer functions and impedances using a network analyzer is discussed in Section 8.5. Careful attention to ground connections is important when measuring small impedances.

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[2] R. D. MIDDLEBROOK, "Methods of Design-Oriented Analysis: The Quadratic Equation Revisited," *IEEE Frontiers in Education Conference*, 1992 Proceedings, pp. 95-102, Nov. 1991.

[3] F. BARZEGAR, S. ĆUK, and R. D. MIDDLEBROOK, "Using Small Computers to Model and Measure Magnitude and Phase of Regulator Transfer Functions and Loop Gain," *Proceedings of Powercon 8*, April 1981. Also in *Advances in Switched-Mode Power Conversion*, Irvine: Teslaco, Vol. 1, pp. 251-278, 1981.

[4] H. W. OTT, *Noise Reduction Techniques in Electronic Systems*, 2nd edit., New York: John Wiley & Sons, 1988, Chapter 3.

PROBLEMS

8.1 Express the gains represented by the asymptotes of Figs. 8.62(a) to (c) in factored pole-zero form. You may assume that all poles and zeroes have negative real parts.

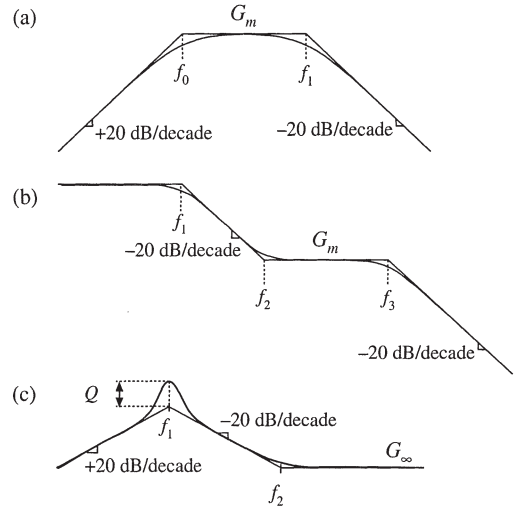


Fig. 8.62 Gain asymptotes for Problem 8.1.

8.2 Express the gains represented by the asymptotes of Figs. 8.63(a) to (c) in factored pole-zero form. You may assume that all poles and zeroes have negative real parts.

8.3 Derive analytical expressions for the low-frequency asymptotes of the magnitude Bode plots shown in Fig. 8.63(a) to (c).

8.4 Derive analytical expressions for the three magnitude asymptotes of Fig. 8.16.

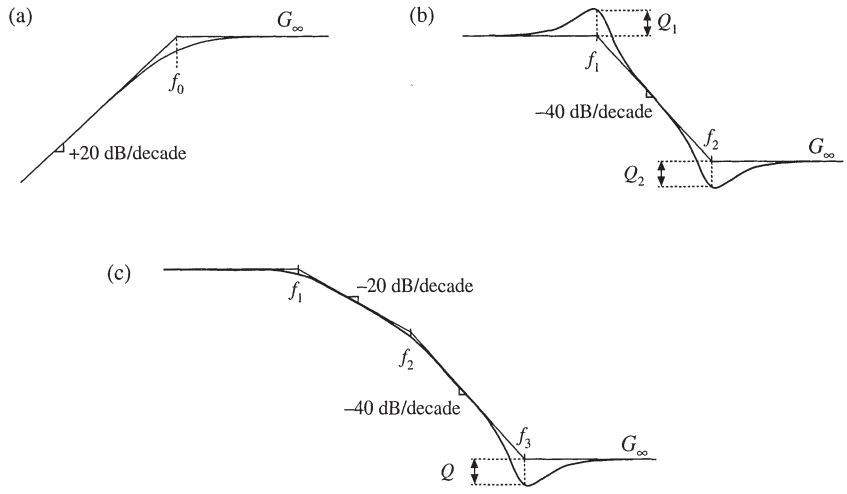


Fig. 8.63 Gain asymptotes for Problems 8.2 and 8.3.

8.5 An experimentally measured transfer function. Figure 8.64 contains experimentally measured magnitude and phase data for the gain function $A(s)$ of a certain amplifier. The object of this problem is to find an expression for $A(s)$. Overlay asymptotes as appropriate on the magnitude and phase data, and hence deduce numerical values for the gain asymptotes and corner frequencies of $A(s)$. Your magnitude and

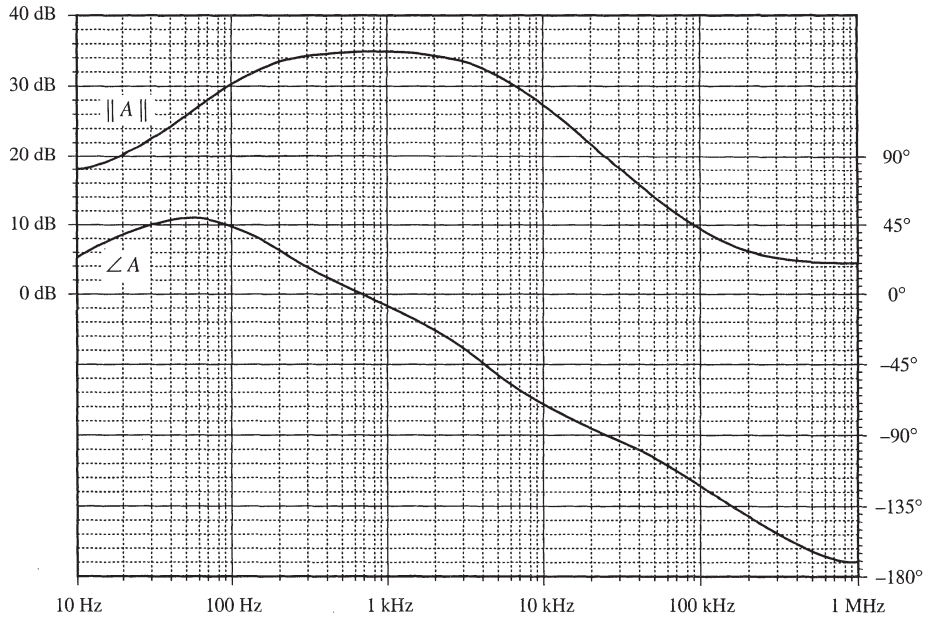


Fig. 8.64 Experimentally-measured magnitude and phase data, Problem 8.5.

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phase asymptotes must, of course, follow all of the rules: magnitude slopes must be multiples of ±20 dB per decade, phase slopes for real poles must be multiples of ±45° per decade, etc. The phase and magnitude asymptotes must be consistent with each other.

It is suggested that you start by guessing $A(s)$ based on the magnitude data. Then construct the phase asymptotes for your guess, and compare them with the given data. If there are discrepancies, then modify your guess accordingly and redo your magnitude and phase asymptotes. You should turn in: (1) your analytical expression for $A(s)$, with numerical values given, and (2) a copy of Fig. 8.64, with your magnitude and phase asymptotes superimposed and with all break frequencies and slopes clearly labeled.

8.6 An experimentally-measured impedance. Figure 8.65 contains experimentally measured magnitude and phase data for the driving-point impedance $Z(s)$ of a passive network. The object of this problem is the find an expression for $Z(s)$. Overlay asymptotes as appropriate on the magnitude and phase data, and hence deduce numerical values for the salient features of the impedance function. You should turn in: (1) your analytical expression for $Z(s)$, with numerical values given, and (2) a copy of Fig. 8.65, with your magnitude and phase asymptotes superimposed and with all salient features and asymptote slopes clearly labeled.

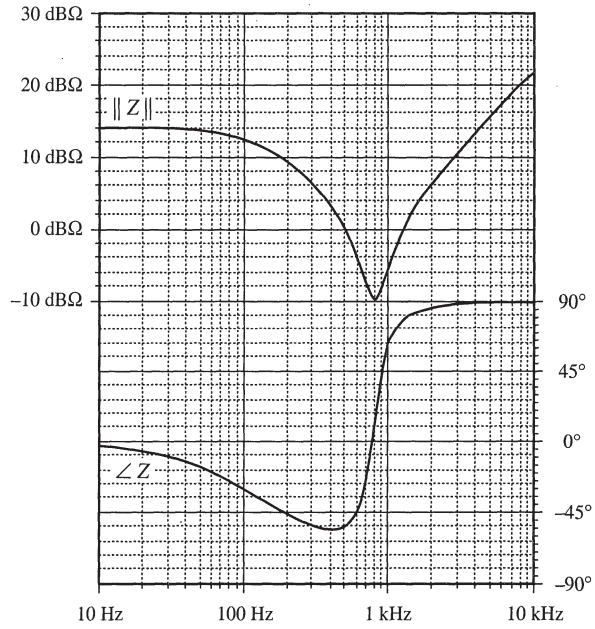


Fig. 8.65 Impedance magnitude and phase data, Problem 8.6.

8.7 In Section 7.2.9, the small-signal ac model of a nonideal flyback converter is derived, with the result illustrated in Fig. 7.27. Construct a Bode plot of the magnitude and phase of the converter output impedance $Z_{out}(s)$. Give both analytical expressions and numerical values for all important features in your plot. Note: $Z_{out}(s)$ includes the load resistance R. The element values are: $D = 0.4$, $n = 0.2$, $R = 6\ \Omega$, $L = 600\ \mu$H, $C = 100\ \mu$F, $R_{on} = 5\ \Omega$.

8.8 For the nonideal flyback converter modeled in Section 7.2.9:

(a) Derive analytical expressions for the control-to-output and line-to-output transfer functions $G_{vd}(s)$ and $G_{vg}(s)$. Express your results in standard normalized form.

(b) Derive analytical expressions for the salient features of these transfer functions.

(c) Construct the magnitude and phase Bode plots of the control-to-output transfer function, using

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the following values: $n = 2$, $V_g = 48$ V, $D = 0.3$, $R = 5\ \Omega$, $L = 250\ \mu$H, $C = 100\ \mu$F, $R_{on} = 1.2\ \Omega$. Label the numerical values of the constant asymptotes, all corner frequencies, the Q-factor, and asymptote slopes.

8.9 Magnitude Bode diagram of an *R–L–C* filter circuit. For the filter circuit of Fig. 8.66, construct the Bode plots for the magnitudes of the Thevenin-equivalent output impedance Z_{out} and the transfer function $H(s) = v_2/v_1$. Plot your results on semilog graph paper. Give approximate analytical expressions and numerical values for the important corner frequencies and asymptotes. Do all of the elements significantly affect Z_{out} and H?

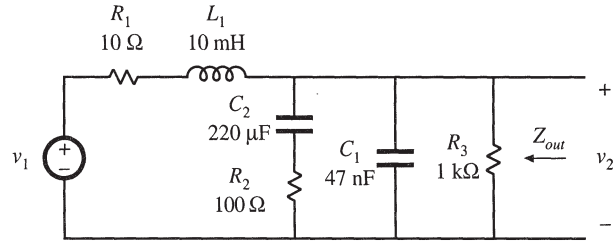


Fig. 8.66 Filter circuit of Problem 8.9.

8.10 Operational amplifier filter circuit. The op amp circuit shown in Fig. 8.67 is a practical realization of what is known as a *PID controller*, and is sometimes used to modify the loop gain of feedback circuits to improve their performance. Using semilog graph paper, sketch the Bode diagram of the magnitude of the transfer function $v_2(s)/v_1(s)$ of the circuit shown. Label all corner frequencies, flat asymptote gains, and asymptote slopes, as appropriate, giving both analytical expressions and numerical values. You may assume that the op amp is ideal.

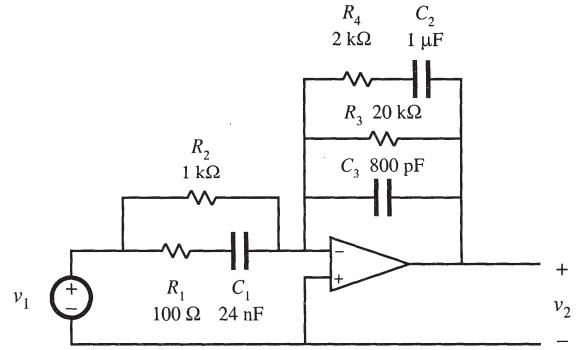


Fig. 8.67 Op-amp PID controller circuit, Problem 8.10.

8.11 Phase asymptotes. Construct the phase asymptotes for the transfer function $v_2(s)/v_1(s)$ of Problem 8.10. Label all break frequencies, flat asymptotes, and asymptote slopes.

8.12 Construct the Bode diagram for the magnitude of the output impedance Z_{out} of the network shown in Fig. 8.68. Give suitable analytical expressions for each asymptote, corner frequency, and Q-factor, as appropriate. Justify any approximations that you use.
The component values are:

$L_1 = 100\ \mu$H $L_2 = 16$ mH
$C_1 = 1000\ \mu$F $C_2 = 10\ \mu$F
$R_1 = 5\ \Omega$ $R_2 = 50\ \Omega$

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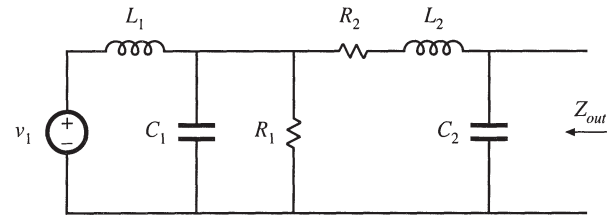


Fig. 8.68 Filter network of Problem 8.12.

8.13 The two section input filter in the circuit of Fig. 8.69 should be designed such that its output impedance $Z_{out}|_{v_g = 0}$ meets certain input filter design criteria, and hence it is desirable to construct the Bode plot for the magnitude of Z_s. Although this filter contains six reactive elements, $\| Z_s \|$ can nonetheless be constructed in a relatively straightforward manner using graphical construction techniques. The element values are:

$L_1 = 32$ mH $\quad C_1 = 32\ \mu$F
$L_2 = 400\ \mu$H $\quad C_2 = 6.8\ \mu$F
$L_3 = 800\ \mu$H $\quad R_1 = 10\ \Omega$
$L_4 = 1\ \mu$H $\quad R_2 = 1\ \Omega$

(a) Construct $\| Z_s \|$ using the "algebra on the graph" method. Give simple approximate analytical expressions for all asymptotes and corner frequencies.

(b) It is desired that $\| Z_s \|$ be approximately equal to 5 Ω at 500 Hz and 2.5 Ω at 1 kHz. Suggest a simple way to accomplish this by changing the value of one component.

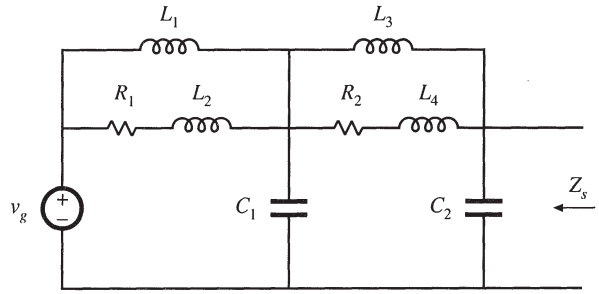


Fig. 8.69 Input filter circuit of Problem 8.13.

8.14 Construct the Bode plot of the magnitude of the output impedance of the filter illustrated in Fig. Fig. 8.70. Give approximate analytical expressions for each corner frequency. No credit will be given for computer-generated plots.

8.15 A certain open-loop buck-boost converter contains an input filter. Its small-signal ac model is shown in Fig. 8.71, and the element values are specified below. Construct the Bode plot for the magnitude of the converter output impedance $\| Z_{out}(s) \|$. Label the values of all important corner frequencies and asymptotes.

$D = 0.6$ $\quad L_f = 150\ \mu$H
$R = 6\ \Omega$ $\quad C_f = 16\ \mu$F
$C = 0.33\ \mu$F $\quad C_b = 2200\ \mu$F
$L = 25\ \mu$H $\quad R_f = 1\ \Omega$

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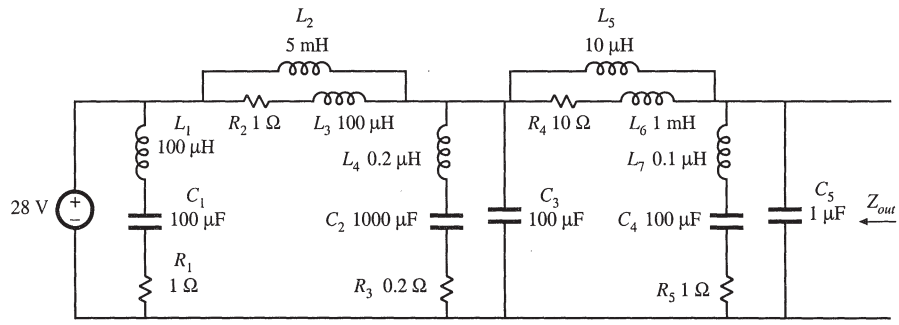


Fig. 8.70 Input filter circuit of Problem 8.14.

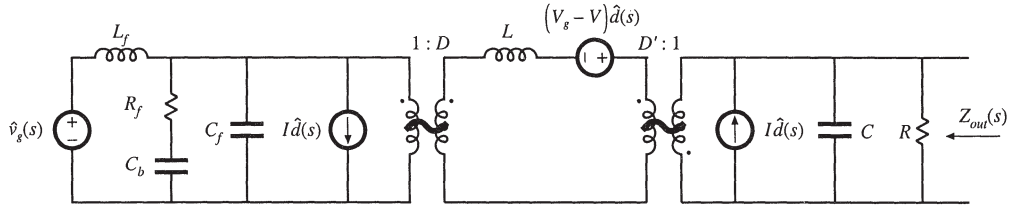


Fig. 8.71 Small-signal model of a buck-boost converter with input filter, Problem 8.15.

8.16 The small-signal equations of the Watkins-Johnson converter operating in continuous conduction mode are:

$$L\frac{d\hat{i}(t)}{dt} = -D\hat{v}(t) + (2V_g - V)\hat{d}(t) + (D - D')\hat{v}_g(t)$$
$$C\frac{d\hat{v}(t)}{dt} = D\hat{i}(t) - \frac{\hat{v}(t)}{R}$$
$$\hat{i}_g(t) = (D - D')\hat{i}(t) + 2I\hat{d}(t)$$

(a) Derive analytical expressions for the line-to-output transfer function $G_{vg}(s)$ and the control-to-output transfer function $G_{vd}(s)$.

(b) Derive analytical expressions for the salient features (dc gains, corner frequencies, and Q-factors) of the transfer functions $G_{vg}(s)$ and $G_{vd}(s)$. Express your results as functions of V_g, D, R, L, and C.

(c) The converter operates at $V_g = 28$ V, $D = 0.25$, $R = 28\ \Omega$, $C = 100\ \mu$F, $L = 400\ \mu$F. Sketch the Bode diagram of the magnitude and phase of $G_{vd}(s)$. Label salient features.

8.17 The element values in the buck converter of Fig. 7.68 are:

$V_g = 120$ V $\qquad D = 0.6$
$R = 10\ \Omega \qquad R_g = 2\ \Omega$
$L = 550\ \mu$H $\qquad C = 100\ \mu$F

(a) Determine an analytical expression for the control-to-output transfer function $G_{vg}(s)$ of this converter.

(b) Find analytical expressions for the salient features of $G_{vg}(s)$.

(c) Construct magnitude and phase asymptotes for G_{vg}. Label the numerical values of all slopes and

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other important features.

8.18 Loss mechanisms in capacitors, such as dielectric loss and contact and foil resistance, can be modeled electrically using an *equivalent series resistance* (esr). Capacitors whose dielectric materials exhibit a high dielectric constant, such as electrolytic capacitors, tantalum capacitors, and some types of multilayer ceramic capacitors, typically exhibit relatively high esr.

A buck converter contains a 1.6 mH inductor, and operates with a quiescent duty cycle of 0.5. Its output capacitor can be modeled as a 16 μF capacitor in series with a 0.2 Ω esr. The load resistance is 10 Ω. The converter operates in continuous conduction mode. The quiescent input voltage is $V_g = 120$ V.

(a) Determine an analytical expression for the control-to-output transfer function $G_{vg}(s)$ of this converter.

(b) Find analytical expressions for the salient features of $G_{vg}(s)$.

(c) Construct magnitude and phase asymptotes for G_{vg}. Label the numerical values of all slopes and other important features.

8.19 The *LCC* resonant inverter circuit contains the following transfer function:

$$H(s) = \frac{sC_1R}{1 + sR(C_1 + C_2) + s^2LC_1 + s^3LC_1C_2R}$$

(a) When C_1 is sufficiently large, this transfer function can be expressed as an inverted pole and a quadratic pole pair. Derive analytical expressions for the corner frequencies and Q-factor in this case, and sketch typical magnitude asymptotes. Determine analytical conditions for validity of your approximation.

(b) When C_2 is sufficiently large, the transfer function can be also expressed as an inverted pole and a quadratic pole pair. Derive analytical expressions for the corner frequencies and Q-factor in this case, and sketch typical magnitude asymptotes. Determine analytical conditions for validity of your approximation in this case.

(c) When $C_1 = C_2$ and when the quadratic poles have sufficiently high Q, then the transfer function can again be expressed as an inverted pole and a quadratic pole pair. Derive analytical expressions for the corner frequencies and Q-factor in this case, and sketch typical magnitude asymptotes. Determine analytical conditions for validity of your approximation in this case.

8.20 A two-section *L–C* filter has the following transfer function:

$$G(s) = \frac{1}{1 + s\left(\frac{L_1 + L_2}{R}\right) + s^2\left(L_1\left(C_1 + C_2\right) + L_2C_2\right) + s^3\left(\frac{L_1L_2C_1}{R}\right) + s^4\left(L_1L_2C_1C_2\right)}$$

The element values are:

$R = 50$ mΩ

$C_1 = 680$ μF $\qquad$ $C_2 = 4.7$ μF

$L_1 = 500$ μH $\qquad$ $L_2 = 50$ μH

(a) Factor $G(s)$ into approximate real and quadratic poles, as appropriate. Give analytical expressions for the salient features. Justify your approximation using the numerical element values.

(b) Construct the magnitude and phase asymptotes of $G(s)$.

(c) It is desired to reduce the Q to 2, without significantly changing the corner frequencies or other features of the response. It is possible to do this by changing only two element values. Specify how to accomplish this.

8.21 The boost converter of Fig. 8.72 operates in the continuous conduction mode, with quiescent duty cycle

$D = 0.6$. On semi-log axes, construct the magnitude and phase Bode plots of

(a) the control-to-output transfer function $G_{vd}(s)$,

(b) the line-to-output transfer function $G_{vg}(s)$,

(c) the output impedance $Z_{out}(s)$, and

(d) the input impedance $Z_{in}(s)$.

On each plot, label the corner frequencies and asymptotes.

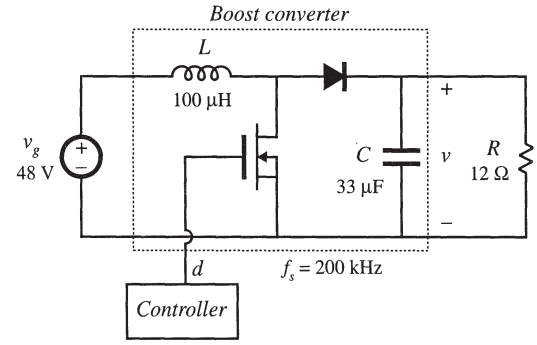


Fig. 8.72 Boost converter of Problem 8.21.

8.22 The forward converter of Fig. 8.73 operates in the continuous conduction mode, with the quiescent values $V_g = 380$ V and $V = 28$ V. The transformer turns ratio is $n_1/n_3 = 4.5$. On semi-log axes, construct the magnitude and phase Bode plots of

(a) the control-to-output transfer function $G_{vd}(s)$, and

(b) the line-to-output transfer function $G_{vg}(s)$.

On each plot, label the corner frequencies and asymptotes. *Hint:* other than introduction of the turns ratio n_1/n_3, the transformer does not significantly affect the small-signal behavior of the forward converter.

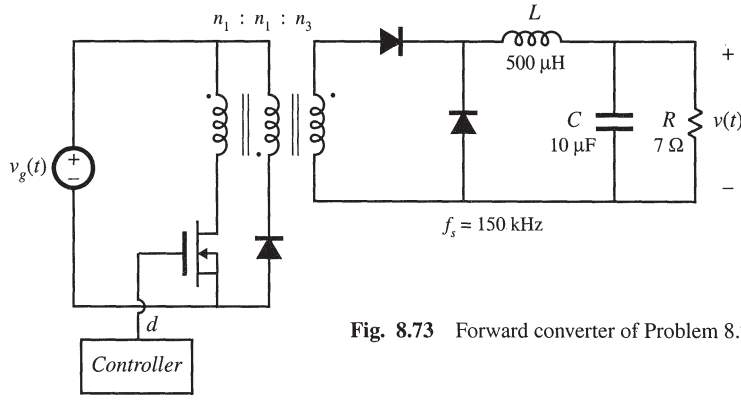


Fig. 8.73 Forward converter of Problem 8.22.

8.23 The boost converter of Fig. 8.74 operates in the continuous conduction mode, with the following quiescent values: $V_g = 120$ V, $V = 300$ V. It is desired to control the converter input current waveform, and hence it is necessary to determine the small-signal transfer function

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$$G_{id}(s) = \left. \frac{\hat{i}_g(s)}{\hat{d}(s)} \right|_{\hat{v}_g(s)=0}$$

(a) Derive an analytical expression for $G_{id}(s)$. Express all poles and zeroes in normalized standard form, and give analytical expressions for the corner frequencies, Q-factor, and dc gain.

(b) On semi-log axes, construct the Bode plot for the magnitude and phase of $G_{id}(s)$.

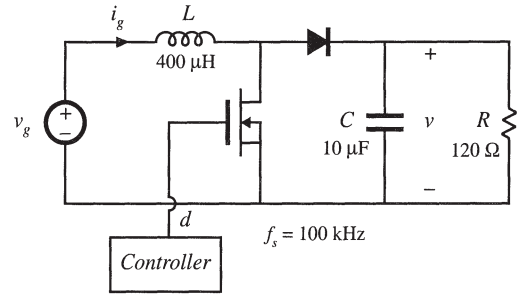


Fig. 8.74 Boost converter of Problem 8.23.

8.24 The buck-boost converter of Fig. 8.75 operates in the continuous conduction mode, with the following quiescent values: $V_g = 48$ V, $V = -24$ V. On semi-log axes, construct the magnitude and phase Bode plots of:

(a) the control-to-output transfer function $G_{vd}(s)$, and

(b) the output impedance $Z_{out}(s)$.

On each plot, label the corner frequencies and asymptotes as appropriate.

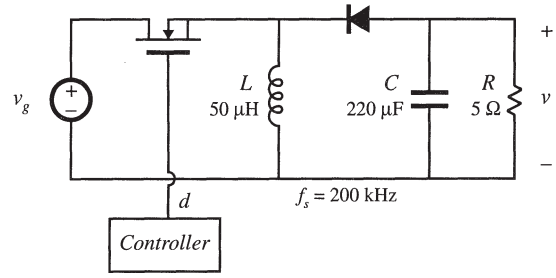


Fig. 8.75 Buck-boost converter of Problem 8.24.

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9
Controller Design

9.1 INTRODUCTION

In all switching converters, the output voltage $v(t)$ is a function of the input line voltage $v_g(t)$, the duty cycle $d(t)$, and the load current $i_{load}(t)$, as well as the converter circuit element values. In a dc–dc converter application, it is desired to obtain a constant output voltage $v(t) = V$, in spite of disturbances in $v_g(t)$ and $i_{load}(t)$, and in spite of variations in the converter circuit element values. The sources of these disturbances and variations are many, and a typical situation is illustrated in Fig. 9.1. The input voltage $v_g(t)$ of an off-line power supply may typically contain periodic variations at the second harmonic of the ac power system frequency (100 Hz or 120 Hz), produced by a rectifier circuit. The magnitude of $v_g(t)$ may also vary when neighboring power system loads are switched on or off. The load current $i_{load}(t)$ may contain variations of significant amplitude, and a typical power supply specification is that the output voltage must remain within a specified range (for example, 3.3 V ± 0.05 V) when the load current takes a step change from, for example, full rated load current to 50% of the rated current, and vice versa. The values of the circuit elements are constructed to a certain tolerance, and so in high-volume manufacturing of a converter, converters are constructed whose output voltages lie in some distribution. It is desired that essentially all of this distribution fall within the specified range; however, this is not practical to achieve without the use of negative feedback. Similar considerations apply to inverter applications, except that the output voltage is ac.

So we cannot expect to simply set the dc–dc converter duty cycle to a single value, and obtain a given constant output voltage under all conditions. The idea behind the use of negative feedback is to build a circuit that automatically adjusts the duty cycle as necessary, to obtain the desired output voltage with high accuracy, regardless of disturbances in $v_g(t)$ or $i_{load}(t)$ or variations in component values. This is

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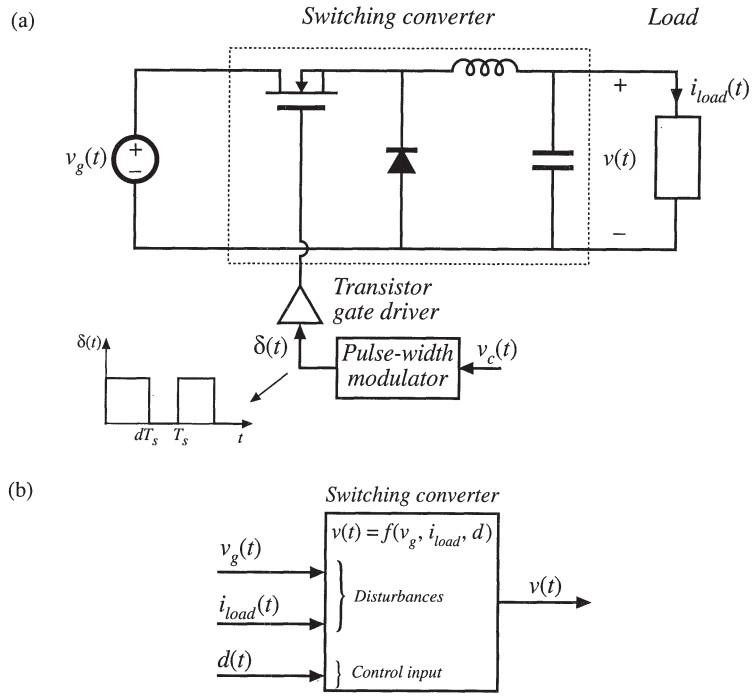


Fig. 9.1 The output voltage of a typical switching converter is a function of the line input voltage v_g, the duty cycle d, and the load current i_{load}: (a) open-loop buck converter; (b) functional diagram illustrating dependence of v on the independent quantities v_g, d, and i_{load}.

a useful thing to do whenever there are variations and unknowns that otherwise prevent the system from attaining the desired performance.

A block diagram of a feedback system is shown in Fig. 9.2. The output voltage $v(t)$ is measured, using a "sensor" with gain $H(s)$. In a dc voltage regulator or dc–ac inverter, the sensor circuit is usually a voltage divider, comprised of precision resistors. The sensor output signal $H(s)v(s)$ is compared with a reference input voltage $v_{ref}(s)$. The objective is to make $H(s)v(s)$ equal to $v_{ref}(s)$, so that $v(s)$ accurately follows $v_{ref}(s)$ regardless of disturbances or component variations in the compensator, pulse-width modulator, gate driver, or converter power stage.

The difference between the reference input $v_{ref}(s)$ and the sensor output $H(s)v(s)$ is called the error signal $v_e(s)$. If the feedback system works perfectly, then $v_{ref}(s) = H(s)v(s)$, and hence the error signal is zero. In practice, the error signal is usually nonzero but nonetheless small. Obtaining a small error is one of the objectives in adding a compensator network $G_c(s)$ as shown in Fig. 9.2. Note that the output voltage $v(s)$ is equal to the error signal $v_e(s)$, multiplied by the gains of the compensator, pulse-width modulator, and converter power stage. If the compensator gain $G_c(s)$ is large enough in magnitude, then a small error signal can produce the required output voltage $v(t) = V$ for a dc regulator (Q: how should H and v_{ref} then be chosen?). So a large compensator gain leads to a small error, and therefore the output follows the reference input with good accuracy. This is the key idea behind feedback systems.

The averaged small-signal converter models derived in Chapter 7 are used in the following sections to find the effects of feedback on the small-signal transfer functions of the regulator. The loop gain $T(s)$ is defined as the product of the small-signal gains in the forward and feedback paths of the feedback

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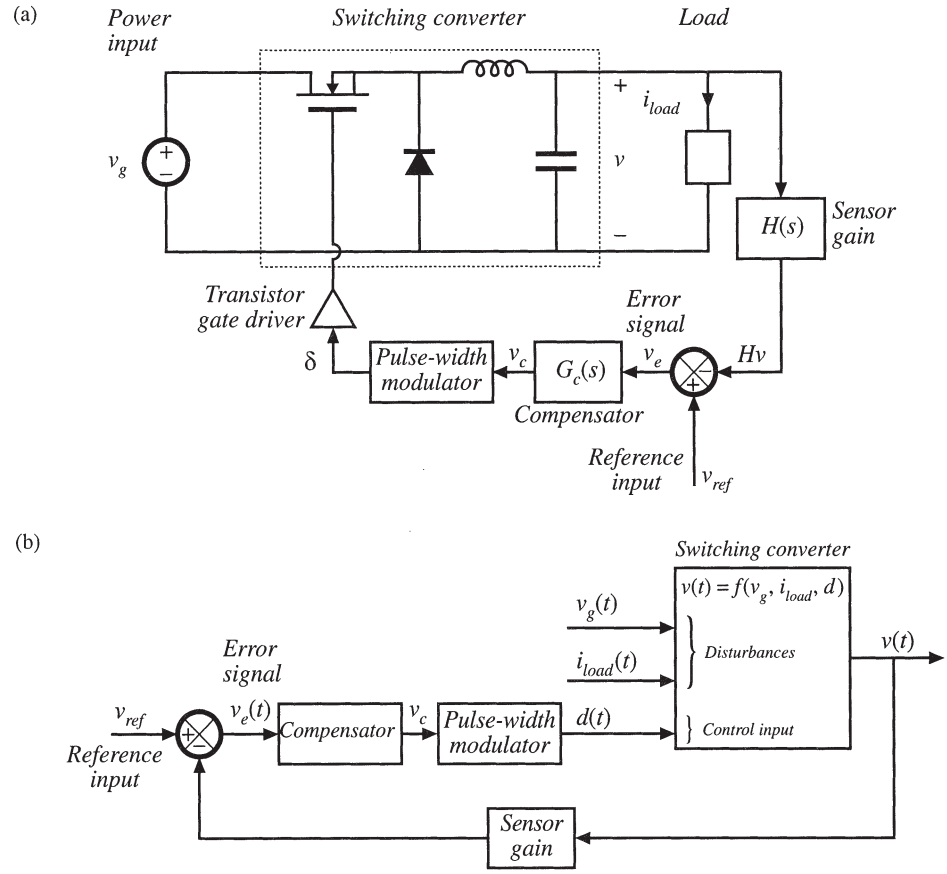


Fig. 9.2 Feedback loop for regulation of the output voltage: (a) buck converter, with feedback loop block diagram; (b) functional block diagram of the feedback system.

loop. It is found that the transfer function from a disturbance to the output is multiplied by the factor $1/(1 + T(s))$. Hence, when the loop gain T is large in magnitude, then the influence of disturbances on the output voltage is small. A large loop gain also causes the output voltage $v(s)$ to be nearly equal to $v_{ref}(s)/H(s)$, with very little dependence on the gains in the forward path of the feedback loop. So the loop gain magnitude $\| T \|$ is a measure of how well the feedback system works. All of these gains can be easily constructed using the algebra-on-the-graph method; this allows easy evaluation of important closed-loop performance measures, such as the output voltage ripple resulting from 120 Hz rectification ripple in $v_g(t)$ or the closed-loop output impedance.

Stability is another important issue in feedback systems. Adding a feedback loop can cause an otherwise well-behaved circuit to exhibit oscillations, ringing and overshoot, and other undesirable behavior. An in-depth treatment of stability is beyond the scope of this book; however, the simple phase margin criterion for assessing stability is used here. When the phase margin of the loop gain T is positive, then the feedback system is stable. Moreover, increasing the phase margin causes the system transient response to be better behaved, with less overshoot and ringing. The relation between phase margin and closed-loop response is quantified in Section 9.4.

An example is given in Section 9.5, in which a compensator network is designed for a dc regu-

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lator system. The compensator network is designed to attain adequate phase margin and good rejection of expected disturbances. Lead compensators and *P–D* controllers are used to improve the phase margin and extend the bandwidth of the feedback loop. This leads to better rejection of high-frequency disturbances. Lag compensators and *P–I* controllers are used to increase the low-frequency loop gain. This leads to better rejection of low-frequency disturbances and very small steady-state error. More complicated compensators can achieve the advantages of both approaches.

Injection methods for experimental measurement of loop gain are introduced in Section 9.6. The use of voltage or current injection solves the problem of establishing the correct quiescent operating point in high-gain systems. Conditions for obtaining an accurate measurement are exposed. The injection method also allows measurement of the loop gains of unstable systems.

9.2 EFFECT OF NEGATIVE FEEDBACK ON THE NETWORK TRANSFER FUNCTIONS

We have seen how to derive the small-signal ac transfer functions of a switching converter. For example, the equivalent circuit model of the buck converter can be written as in Fig. 9.3. This equivalent circuit contains three independent inputs: the control input variations $\hat{d}$, the power input voltage variations $\hat{v}_g$, and the load current variations $\hat{i}_{load}$. The output voltage variation $\hat{v}$ can therefore be expressed as a linear combination of the three independent inputs, as follows:

$$\hat{v}(s) = G_{vd}(s)\hat{d}(s) + G_{vg}(s)\hat{v}_g(s) - Z_{out}(s)\hat{i}_{load}(s) \tag{9.1}$$

where

$$G_{vd}(s) = \left.\frac{\hat{v}(s)}{\hat{d}(s)}\right|_{\substack{\hat{v}_g = 0 \\ \hat{i}_{load} = 0}} \qquad \text{converter control-to-output transfer function} \tag{9.1a}$$

$$G_{vg}(s) = \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\substack{\hat{d} = 0 \\ \hat{i}_{load} = 0}} \qquad \text{converter line-to-output transfer function} \tag{9.1b}$$

$$Z_{out}(s) = -\left.\frac{\hat{v}(s)}{\hat{i}_{load}(s)}\right|_{\substack{\hat{d} = 0 \\ \hat{v}_g = 0}} \qquad \text{converter output impedance} \tag{9.1c}$$

The Bode diagrams of these quantities are constructed in Chapter 8. Equation (9.1) describes how distur-

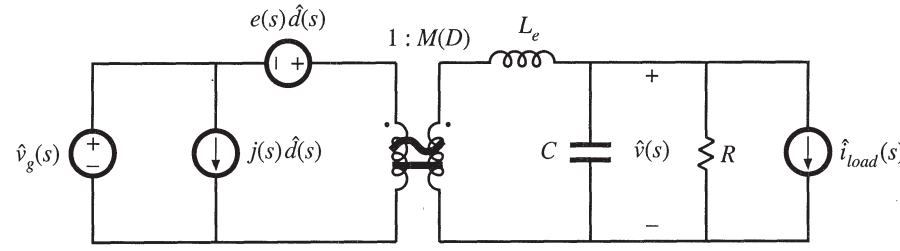


Fig. 9.3 Small-signal converter model, which represents variations in v_g, d, and i_{load}.

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bances v_g and i_{load} propagate to the output v, through the transfer function $G_{vg}(s)$ and the output impedance $Z_{out}(s)$. If the disturbances v_g and i_{load} are known to have some maximum worst-case amplitude, then Eq. (9.1) can be used to compute the resulting worst-case open-loop variation in v.

As described previously, the feedback loop of Fig. 9.2 can be used to reduce the influences of v_g and i_{load} on the output v. To analyze this system, let us perturb and linearize its averaged signals about their quiescent operating points. Both the power stage and the control block diagram are perturbed and linearized:

$$\begin{aligned} v_{ref}(t) &= V_{ref} + \hat{v}_{ref}(t) \\ v_e(t) &= V_e + \hat{v}_e(t) \end{aligned} \tag{9.2}$$

etc.

In a dc regulator system, the reference input is constant, so $v_{ref}(t) = 0$. In a switching amplifier or dc–ac inverter, the reference input may contain an ac variation. In Fig. 9.4(a), the converter model of Fig. 9.3 is combined with the perturbed and linearized control circuit block diagram. This is equivalent to the reduced block diagram of Fig. 9.4(b), in which the converter model has been replaced by blocks representing Eq. (9.1).

Solution of Fig. 9.4(b) for the output voltage variation v yields

$$\hat{v} = \hat{v}_{ref} \frac{G_c G_{vd}/V_M}{1 + HG_c G_{vd}/V_M} + \hat{v}_g \frac{G_{vg}}{1 + HG_c G_{vd}/V_M} - \hat{i}_{load} \frac{Z_{out}}{1 + HG_c G_{vd}/V_M} \tag{9.3}$$

which can be written in the form

$$\hat{v} = \hat{v}_{ref} \frac{1}{H} \frac{T}{1+T} + \hat{v}_g \frac{G_{vg}}{1+T} - \hat{i}_{load} \frac{Z_{out}}{1+T} \tag{9.4}$$

with

$$T(s) = H(s)G_c(s)G_{vd}(s)/V_M = \text{“loop gain”}$$

Equation (9.4) is a general result. The loop gain $T(s)$ is defined in general as the product of the gains around the forward and feedback paths of the loop. This equation shows how the addition of a feedback loop modifies the transfer functions and performance of the system, as described in detail below.

9.2.1 Feedback Reduces the Transfer Functions from Disturbances to the Output

The transfer function from v_g to v in the open-loop buck converter of Fig. 9.3 is $G_{vg}(s)$, as given in Eq. (9.1). When feedback is added, this transfer function becomes

$$\left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\substack{\hat{v}_{ref}=0 \\ \hat{i}_{load}=0}} = \frac{G_{vg}(s)}{1 + T(s)} \tag{9.5}$$

from Eq. (9.4). So this transfer function is reduced via feedback by the factor $1/(1 + T(s))$. If the loop gain $T(s)$ is large in magnitude, then the reduction can be substantial. Hence, the output voltage variation v resulting from a given v_g variation is attenuated by the feedback loop.

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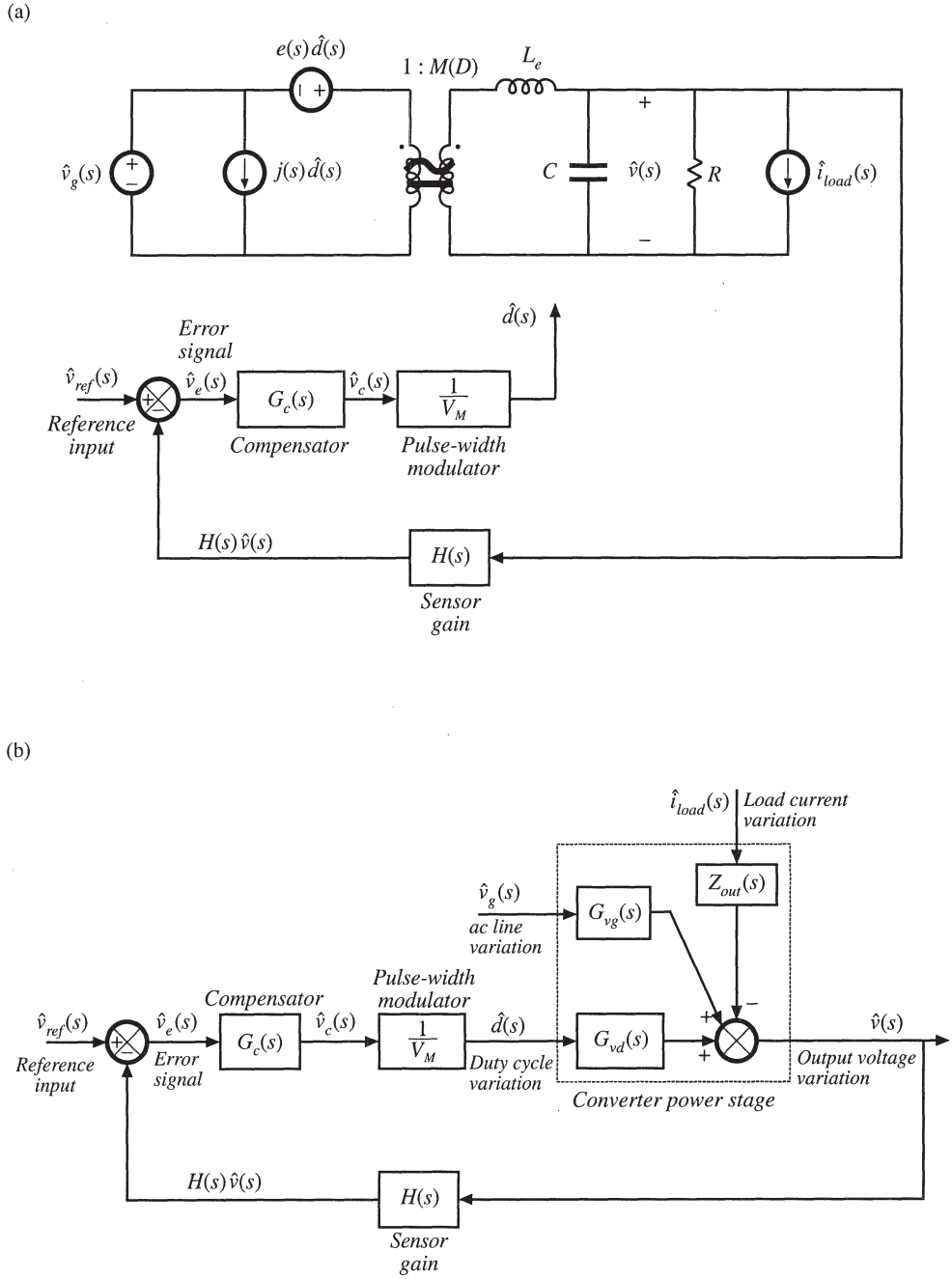


Fig. 9.4 Voltage regulator system small-signal model: (a) with converter equivalent circuit; (b) complete block diagram.

Equation (9.4) also predicts that the converter output impedance is reduced, from $Z_{out}(s)$ to

$$\left.\frac{\hat{v}(s)}{-\hat{i}_{load}(s)}\right|_{\substack{\hat{v}_{ref}=0\\ \hat{v}_g=0}} = \frac{Z_{out}(s)}{1+T(s)} \tag{9.6}$$

So the feedback loop also reduces the converter output impedance by a factor of $1/(1 + T(s))$, and the influence of load current variations on the output voltage is reduced.

9.2.2 Feedback Causes the Transfer Function from the Reference Input to the Output to be Insensitive to Variations in the Gains in the Forward Path of the Loop

According to Eq. (9.4), the closed-loop transfer function from v_{ref} to v is

$$\left.\frac{\hat{v}(s)}{\hat{v}_{ref}(s)}\right|_{\substack{\hat{v}_g=0\\ \hat{i}_{load}=0}} = \frac{1}{H(s)}\,\frac{T(s)}{1+T(s)} \tag{9.7}$$

If the loop gain is large in magnitude, that is, $\| T \| \gg 1$, then $(1 + T) \approx T$ and $T/(1 + T) \approx T/T = 1$. The transfer function then becomes

$$\frac{\hat{v}(s)}{\hat{v}_{ref}(s)} \approx \frac{1}{H(s)} \tag{9.8}$$

which is independent of $G_c(s)$, V_M, and $G_{vd}(s)$. So provided that the loop gain is large in magnitude, then variations in $G_c(s)$, V_M, and $G_{vd}(s)$ have negligible effect on the output voltage. Of course, in the dc regulator application, v_{ref} is constant and $\hat{v}_{ref} = 0$. But Eq. (9.8) applies equally well to the dc values. For example, if the system is linear, then we can write

$$\frac{V}{V_{ref}} = \frac{1}{H(0)}\,\frac{T(0)}{1+T(0)} \approx \frac{1}{H(0)} \tag{9.9}$$

So to make the dc output voltage V accurately follow the dc reference V_{ref}, we need only ensure that the dc sensor gain $H(0)$ and dc reference V_{ref} are well-known and accurate, and that $T(0)$ is large. Precision resistors are normally used to realize H, but components with tightly-controlled values need not be used in G_c, the pulse-width modulator, or the power stage. The sensitivity of the output voltage to the gains in the forward path is reduced, while the sensitivity of v to the feedback gain H and the reference input v_{ref} is increased.

9.3 CONSTRUCTION OF THE IMPORTANT QUANTITIES 1/(1 + T) AND T/(1 + T) AND THE CLOSED-LOOP TRANSFER FUNCTIONS

The transfer functions in Eqs. (9.4) to (9.9) can be easily constructed using the algebra-on-the-graph method [4]. Let us assume that we have analyzed the blocks in our feedback system, and have plotted the Bode diagram of $\| T(s) \|$. To use a concrete example, suppose that the result is given in Fig. 9.5, for which $T(s)$ is

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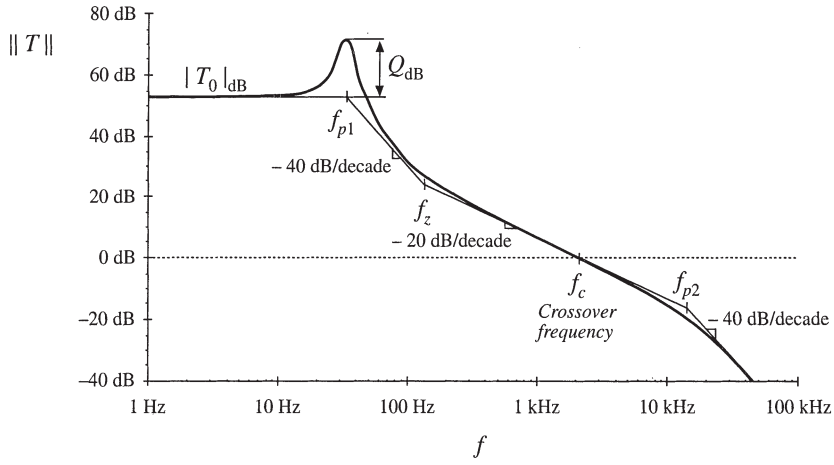


Fig. 9.5 Magnitude of the loop gain example, Eq. (9.10).

$$T(s) = T_0 \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{Q\omega_{p1}} + \left(\frac{s}{\omega_{p1}}\right)^2\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \tag{9.10}$$

This example appears somewhat complicated. But the loop gains of practical voltage regulators are often even more complex, and may contain four, five, or more poles. Evaluation of Eqs. (9.5) to (9.7), to determine the closed-loop transfer functions, requires quite a bit of work. The loop gain T must be added to 1, and the resulting numerator and denominator must be refactored. Using this approach, it is difficult to obtain physical insight into the relationship between the closed-loop transfer functions and the loop gain. In consequence, design of the feedback loop to meet specifications is difficult.

Using the algebra-on-the-graph method, the closed-loop transfer functions can be constructed by inspection, and hence the relation between these transfer functions and the loop gain becomes obvious. Let us first investigate how to plot $\| T/(1 + T) \|$. It can be seen from Fig. 9.5 that there is a frequency f_c, called the "crossover frequency," where $\| T \| = 1$. At frequencies less than f_c, $\| T \| > 1$; indeed, $\| T \| \gg 1$ for $f \ll f_c$. Hence, at low frequency, $(1 + T) \approx T$, and $T/(1 + T) \approx T/T = 1$. At frequencies greater than f_c, $\| T \| < 1$, and $\| T \| \ll 1$ for $f \gg f_c$. So at high frequency, $(1 + T) \approx 1$ and $T/(1 + T) \approx T/1 = T$. So we have

$$\frac{T}{1+T} \approx \begin{cases} 1 & \text{for } \| T \| \gg 1 \\ T & \text{for } \| T \| \ll 1 \end{cases} \tag{9.11}$$

The asymptotes corresponding to Eq. (9.11) are relatively easy to construct. The low-frequency asymptote, for $f < f_c$, is 1 or 0 dB. The high-frequency asymptotes, for $f > f_c$, follow T. The result is shown in Fig. 9.6.

So at low frequency, where $\| T \|$ is large, the reference-to-output transfer function is

$$\frac{\hat{v}(s)}{\hat{v}_{ref}(s)} = \frac{1}{H(s)} \frac{T(s)}{1 + T(s)} \approx \frac{1}{H(s)} \tag{9.12}$$

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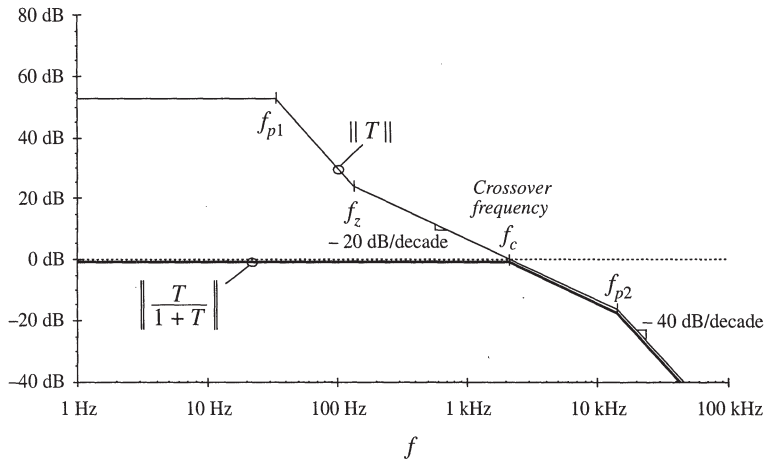


Fig. 9.6 Graphical construction of the asymptotes of $\| T/(1+T) \|$. Exact curves are omitted.

This is the desired behavior, and the feedback loop works well at frequencies where $\| T \|$ is large. At high frequency ($f \gg f_c$) where $\| T \|$ is small, the reference-to-output transfer function is

$$\frac{\hat{v}(s)}{\hat{v}_{ref}(s)} = \frac{1}{H(s)} \frac{T(s)}{1+T(s)} \approx \frac{T(s)}{H(s)} = \frac{G_c(s)G_{vd}(s)}{V_M} \tag{9.13}$$

This is not the desired behavior; in fact, this is the gain with the feedback connection removed ($H \rightarrow 0$). At high frequencies, the feedback loop is unable to reject the disturbance because the bandwidth of T is limited. The reference-to-output transfer function can be constructed on the graph by multiplying the $T/(1+T)$ asymptotes of Fig. 9.6 by $1/H$.

We can plot the asymptotes of $\| 1/(1+T) \|$ using similar arguments. At low frequencies where $\| T \| \gg 1$, then $(1+T) \approx T$, and hence $1/(1+T) \approx 1/T$. At high frequencies where $\| T \| \ll 1$, then $(1+T) \approx 1$ and $1/(1+T) \approx 1$. So we have

$$\frac{1}{1+T(s)} \approx \begin{cases} \dfrac{1}{T(s)} & \text{for } \left\| T \right\| \gg 1 \\ 1 & \text{for } \left\| T \right\| \ll 1 \end{cases} \tag{9.14}$$

The asymptotes for the $T(s)$ example of Fig. 9.5 are plotted in Fig. 9.7.

At low frequencies where $\| T \|$ is large, the disturbance transfer function from v_g to v is

$$\frac{\hat{v}(s)}{\hat{v}_g(s)} = \frac{G_{vg}(s)}{1+T(s)} \approx \frac{G_{vg}(s)}{T(s)} \tag{9.15}$$

Again, $G_{vg}(s)$ is the original transfer function, with no feedback. The closed-loop transfer function has magnitude reduced by the factor $1/\| T \|$. So if, for example, we want to reduce this transfer function by a factor of 20 at 120 Hz, then we need a loop gain $\| T \|$ of at least $20 \Rightarrow 26$ dB at 120 Hz. The disturbance transfer function from v_g to v can be constructed on the graph, by multiplying the asymptotes of Fig. 9.7 by the asymptotes for $G_{vg}(s)$.

Similar arguments apply to the output impedance. The closed-loop output impedance at low fre-

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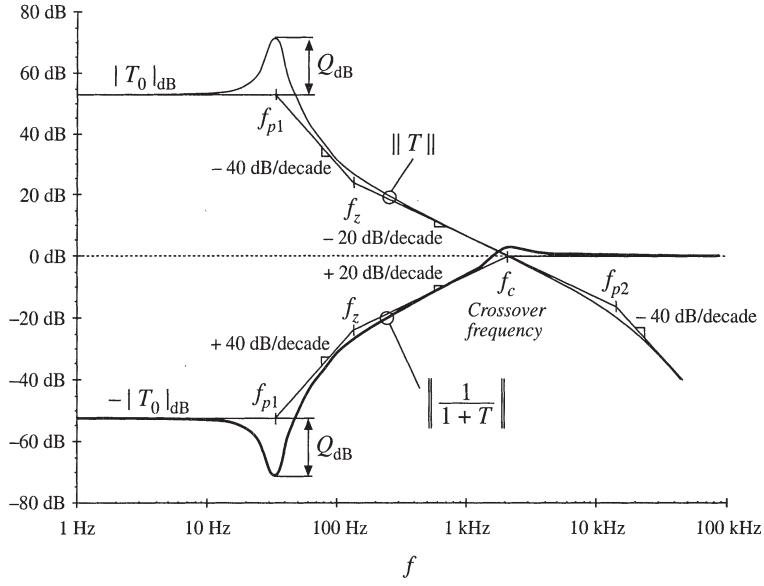


Fig. 9.7 Graphical construction of $\| 1/(1+T) \|$.

quencies is

$$\frac{\hat{v}(s)}{-\hat{i}_{load}(s)} = \frac{Z_{out}(s)}{1+T(s)} \approx \frac{Z_{out}(s)}{T(s)} \tag{9.16}$$

The output impedance is also reduced in magnitude by a factor of $1/\| T \|$ at frequencies below the crossover frequency.

At high frequencies ($f > f_c$) where $\| T \|$ is small, then $1/(1+T) \approx 1$, and

$$\begin{aligned} \frac{\hat{v}(s)}{\hat{v}_g(s)} &= \frac{G_{vg}(s)}{1+T(s)} \approx G_{vg}(s) \\ \frac{\hat{v}(s)}{-\hat{i}_{load}(s)} &= \frac{Z_{out}(s)}{1+T(s)} \approx Z_{out}(s) \end{aligned} \tag{9.17}$$

This is the same as the original disturbance transfer function and output impedance. So the feedback loop has essentially no effect on the disturbance transfer functions at frequencies above the crossover frequency.

9.4 STABILITY

It is well known that adding a feedback loop can cause an otherwise stable system to become unstable. Even though the transfer functions of the original converter, Eq. (9.1), as well as of the loop gain $T(s)$, contain no right half-plane poles, it is possible for the closed-loop transfer functions of Eq. (9.4) to contain right half-plane poles. The feedback loop then fails to regulate the system at the desired quiescent operating point, and oscillations are usually observed. It is important to avoid this situation. And even when the feedback system is stable, it is possible for the transient response to exhibit undesirable ringing

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and overshoot. The stability problem is discussed in this section, and a method for ensuring that the feedback system is stable and well-behaved is explained.

When feedback destabilizes the system, the denominator $(1 + T(s))$ terms in Eq. (9.4) contain roots in the right half-plane (i.e., with positive real parts). If $T(s)$ is a rational fraction, that is, the ratio $N(s)/D(s)$ of two polynomial functions $N(s)$ and $D(s)$, then we can write

$$\frac{T(s)}{1+T(s)} = \frac{\dfrac{N(s)}{D(s)}}{1+\dfrac{N(s)}{D(s)}} = \frac{N(s)}{N(s)+D(s)}$$
$$\frac{1}{1+T(s)} = \frac{1}{1+\dfrac{N(s)}{D(s)}} = \frac{D(s)}{N(s)+D(s)} \tag{9.18}$$

So $T(s)/(1 + T(s))$ and $1/(1+T(s))$ contain the same poles, given by the roots of the polynomial $(N(s) + D(s))$. A brute-force test for stability is to evaluate $(N(s) + D(s))$, and factor the result to see whether any of the roots have positive real parts. However, for all but very simple loop gains, this involves a great deal of work. A simpler method is given by the Nyquist stability theorem, in which the number of right half-plane roots of $(N(s) + D(s))$ can be determined by testing $T(s)$ [1,2]. This theorem is not discussed here. However, a special case of the theorem known as the phase margin test is sufficient for designing most voltage regulators, and is discussed in this section.

9.4.1 The Phase Margin Test

The crossover frequency f_c is defined as the frequency where the magnitude of the loop gain is unity:

$$\left\| T\left(j2\pi f_c\right) \right\| = 1 \Rightarrow 0 \text{ dB} \tag{9.19}$$

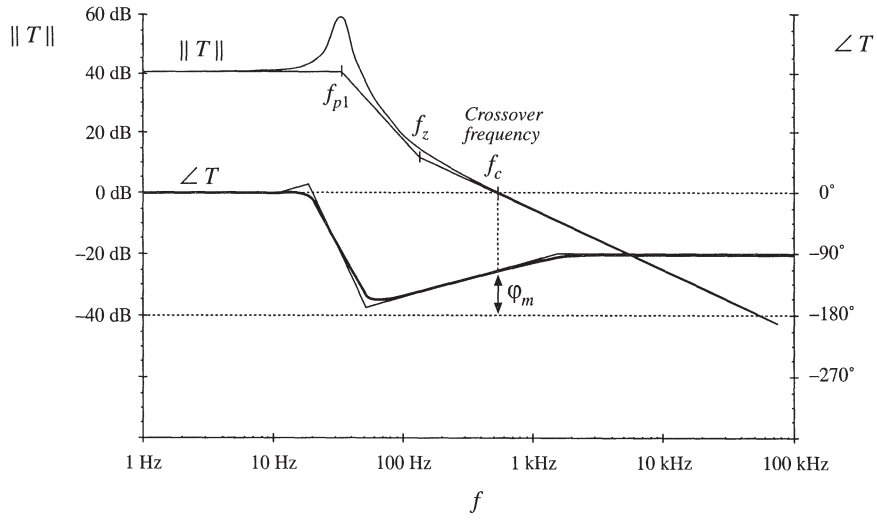


Fig. 9.8 Magnitude and phase of the loop gain of a stable system. The phase margin φ_m is positive.

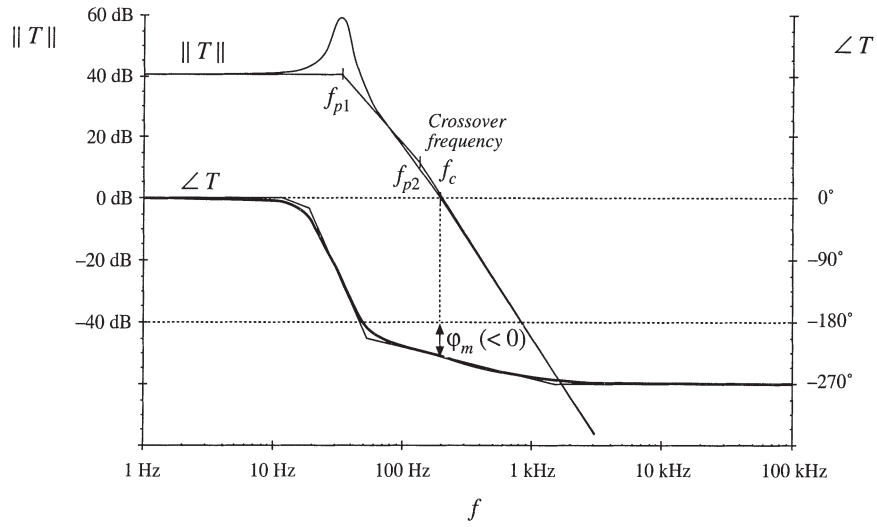


Fig. 9.9 Magnitude and phase of the loop gain of an unstable system. The phase margin φ_m is negative.

To compute the phase margin φ_m, the phase of the loop gain T is evaluated at the crossover frequency, and 180° is added. Hence,

$$\varphi_m = 180^\circ + \angle T\left(j2\pi f_c\right) \tag{9.20}$$

If there is exactly one crossover frequency, and if the loop gain $T(s)$ contains no right half-plane poles, then the quantities $1/(1 + T)$ and $T/(1 + T)$ contain no right half-plane poles when the phase margin defined in Eq. (9.20) is positive. Thus, using a simple test on $T(s)$, we can determine the stability of $T/(1 + T)$ and $1/(1 + T)$. This is an easy-to-use design tool—we simple ensure that the phase of T is greater than –180° at the crossover frequency.

When there are multiple crossover frequencies, the phase margin test may be ambiguous. Also, when T contains right half-plane poles (i.e., the original open-loop system is unstable), then the phase margin test cannot be used. In either case, the more general Nyquist stability theorem must be employed.

The loop gain of a typical stable system is shown in Fig. 9.8. It can be seen that $\angle T(j2\pi f_c) = -112^\circ$. Hence, $\varphi_m = 180^\circ - 112^\circ = +68^\circ$. Since the phase margin is positive, $T/(1 + T)$ and $1/(1 + T)$ contain no right half-plane poles, and the feedback system is stable.

The loop gain of an unstable system is sketched in Fig. 9.9. For this example, $\angle T(j2\pi f_c) = -230^\circ$. The phase margin is $\varphi_m = 180^\circ - 230^\circ = -50^\circ$. The negative phase margin implies that $T/(1 + T)$ and $1/(1 + T)$ each contain at least one right half-plane pole.

9.4.2 The Relationship Between Phase Margin and Closed-Loop Damping Factor

How much phase margin is necessary? Is a worst-case phase margin of 1° satisfactory? Of course, good designs should have adequate design margins, but there is another important reason why additional phase margin is needed. A small phase margin (in T) causes the closed-loop transfer functions $T/(1 + T)$ and $1/(1 + T)$ to exhibit resonant poles with high Q in the vicinity of the crossover frequency. The system transient response exhibits overshoot and ringing. As the phase margin is reduced these characteristics

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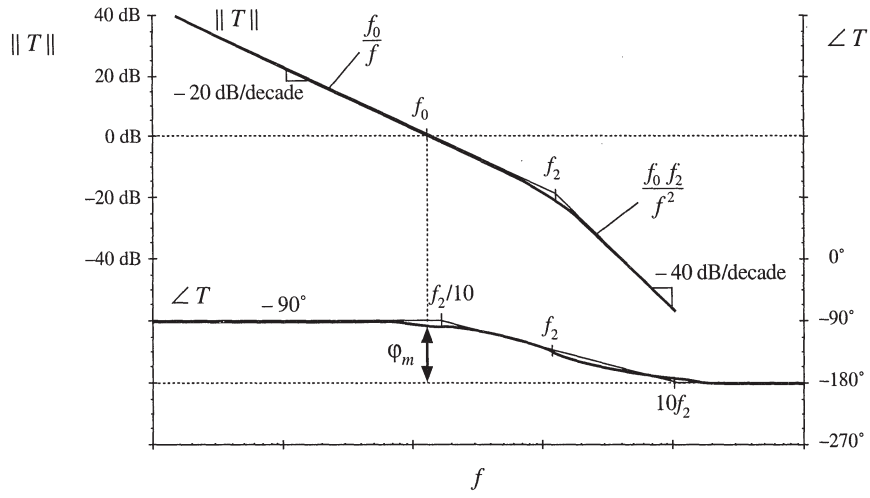


Fig. 9.10 Magnitude and phase asymptotes for the loop gain T of Eq. (9.21).

become worse (higher Q, longer ringing) until, for $\varphi_m \leq 0°$, the system becomes unstable.

Let us consider a loop gain $T(s)$ which is well-approximated, in the vicinity of the crossover frequency, by the following function:

$$T(s) = \frac{1}{\left(\frac{s}{\omega_0}\right)\left(1 + \frac{s}{\omega_2}\right)} \tag{9.21}$$

Magnitude and phase asymptotes are plotted in Fig. 9.10. This function is a good approximation near the crossover frequency for many common loop gains, in which $\| T \|$ approaches unity gain with a –20 dB/decade slope, with an additional pole at frequency $f_2 = \omega_2/2\pi$. Any additional poles and zeroes are assumed to be sufficiently far above or below the crossover frequency, such that they have negligible effect on the system transfer functions near the crossover frequency.

Note that, as $f_2 \to \infty$, the phase margin φ_m approaches 90°. As $f_2 \to 0$, $\varphi_m \to 0°$. So as f_2 is reduced, the phase margin is also reduced. Let's investigate how this affects the closed-loop response via $T/(1 + T)$. We can write

$$\frac{T(s)}{1 + T(s)} = \frac{1}{1 + \frac{1}{T(s)}} = \frac{1}{1 + \frac{s}{\omega_0} + \frac{s^2}{\omega_0 \omega_2}} \tag{9.22}$$

using Eq. (9.21). By putting this into the standard normalized quadratic form, one obtains

$$\frac{T(s)}{1 + T(s)} = \frac{1}{1 + \frac{s}{Q\omega_c} + \left(\frac{s}{\omega_c}\right)^2} \tag{9.23}$$

where

$$\omega_c = \sqrt{\omega_0 \omega_2} = 2\pi f_c$$

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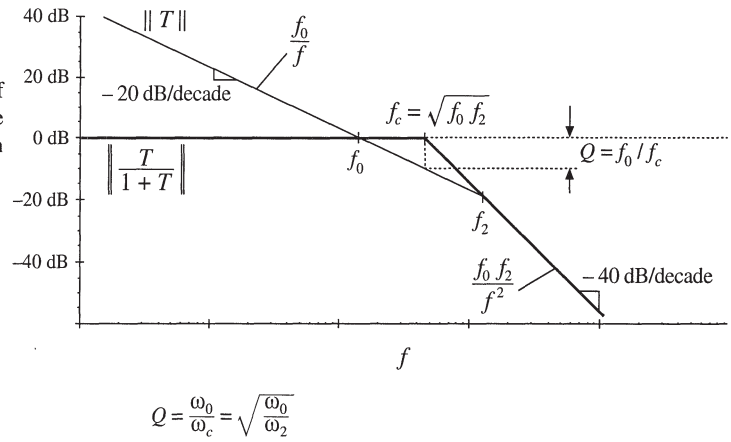


Fig. 9.11 Construction of magnitude asymptotes of the closed-loop transfer function $T/(1 + T)$, for the low-Q case.

$$Q = \frac{\omega_0}{\omega_c} = \sqrt{\frac{\omega_0}{\omega_2}}$$

So the closed-loop response contains quadratic poles at f_c, the geometric mean of f_0 and f_2. These poles have a low Q-factor when $f_0 \ll f_2$. In this case, we can use the low-Q approximation to estimate their frequencies:

$$\begin{aligned} Q\omega_c &= \omega_0 \\ \frac{\omega_c}{Q} &= \omega_2 \end{aligned} \tag{9.24}$$

Magnitude asymptotes are plotted in Fig. 9.11 for this case. It can be seen that these asymptotes conform to the rules of Section 9.3 for constructing $T/(1 + T)$ by the algebra-on-the-graph method.

Next consider the high-Q case. When the pole frequency f_2 is reduced, reducing the phase margin, then the Q-factor given by Eq. (9.23) is increased. For $Q > 0.5$, resonant poles occur at frequency f_c. The magnitude Bode plot for the case $f_2 < f_0$ is given in Fig. 9.12. The frequency f_c continues to be the geometric mean of f_2 and f_0, and f_c now coincides with the crossover (unity-gain) frequency of the $\| T \|$ asymptotes. The exact value of the closed-loop gain $T/(1 + T)$ at frequency f_c is equal to $Q = f_0/f_c$. As shown in Fig. 9.12, this is identical to the value of the low-frequency –20 dB/decade asymptote (f_0/f), evaluated at frequency f_c. It can be seen that the Q-factor becomes very large as the pole frequency f_2 is reduced.

The asymptotes of Fig. 9.12 also follow the algebra-on-the-graph rules of Section 9.3, but the deviation of the exact curve from the asymptotes is not predicted by the algebra-on-the-graph method.

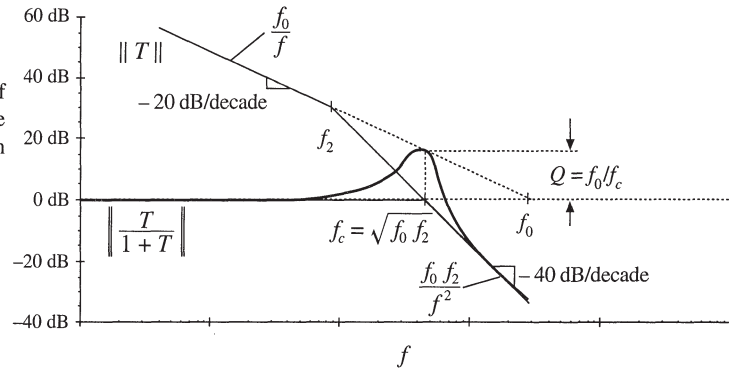


Fig. 9.12 Construction of magnitude asymptotes of the closed-loop transfer function $T/(1 + T)$, for the high-Q case.

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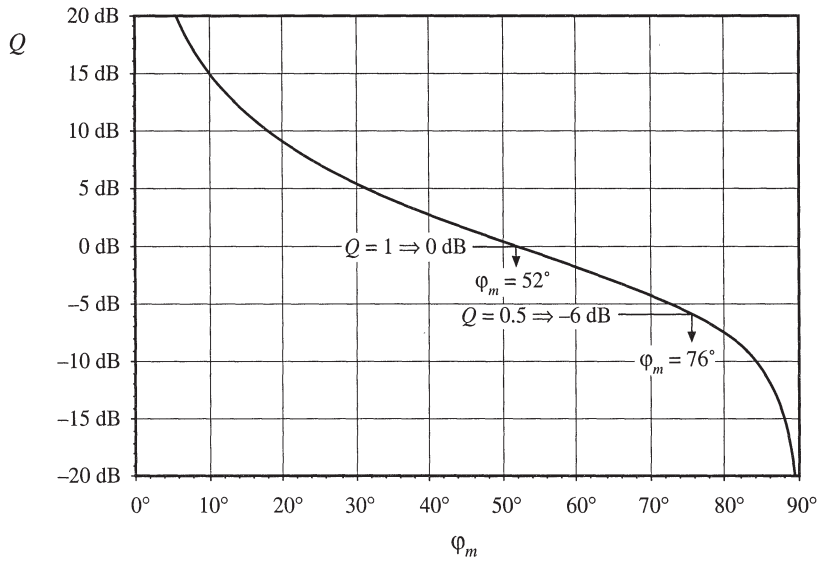


Fig. 9.13 Relationship between loop-gain phase margin φ_m and closed-loop peaking factor Q.

These two poles with Q-factor appear in both $T/(1 + T)$ and $1/(1 + T)$. We need an easy way to predict the Q-factor. We can obtain such a relationship by finding the frequency at which the magnitude of T is exactly equal to unity. We then evaluate the exact phase of T at this frequency, and compute the phase margin. This phase margin is a function of the ratio f_0/f_2, or Q^2. We can then solve to find Q as a function of the phase margin. The result is

$$Q = \frac{\sqrt{\cos \varphi_m}}{\sin \varphi_m}$$
$$\varphi_m = \tan^{-1} \sqrt{\frac{1 + \sqrt{1 + 4Q^4}}{2Q^4}} \tag{9.25}$$

This function is plotted in Fig. 9.13, with Q expressed in dB. It can be seen that obtaining real poles ($Q < 0.5$) requires a phase margin of at least 76°. To obtain $Q = 1$, a phase margin of 52° is needed. The system with a phase margin of 1° exhibits a closed-loop response with very high Q! With a small phase margin, $T(j\omega)$ is very nearly equal to –1 in the vicinity of the crossover frequency. The denominator $(1 + T)$ then becomes very small, causing the closed-loop transfer functions to exhibit a peaked response at frequencies near the crossover frequency f_c.

Figure 9.13 is the result for the simple loop gain defined by Eq. (9.21). However, this loop gain is a good approximation for many other loop gains that are encountered in practice, in which $\| T \|$ approaches unity gain with a –20 dB/decade slope, with an additional pole at frequency f_2. If all other poles and zeroes of $T(s)$ are sufficiently far above or below the crossover frequency, then they have negligible effect on the system transfer functions near the crossover frequency, and Fig. 9.13 gives a good approximation for the relationship between φ_m and Q.

Another common case is the one in which $\| T \|$ approaches unity gain with a –40 dB/decade slope, with an additional zero at frequency f_2. As f_2 is increased, the phase margin is decreased and Q is increased. It can be shown that the relation between φ_m and Q is exactly the same, Eq. (9.25).

A case where Fig. 9.13 fails is when the loop gain $T(s)$ three or more poles at or near the cross-

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over frequency. The closed-loop response then also contains three or more poles near the crossover frequency, and these poles cannot be completely characterized by a single Q-factor. Additional work is required to find the behavior of the exact $T/(1 + T)$ and $1/(1 + T)$ near the crossover frequency, but nonetheless it can be said that a small phase margin leads to a peaked closed-loop response.

9.4.3 Transient Response vs. Damping Factor

One can solve for the unit-step response of the $T/(1 + T)$ transfer function, by multiplying Eq. (9.23) by $1/s$ and then taking the inverse Laplace transform. The result for $Q > 0.5$ is

$$\hat{v}(t) = 1 + \frac{2Qe^{-\omega_c t/2Q}}{\sqrt{4Q^2 - 1}} \sin\left[\frac{\sqrt{4Q^2 - 1}}{2Q}\,\omega_c t + \tan^{-1}\left(\sqrt{4Q^2 - 1}\right)\right] \tag{9.26}$$

For $Q < 0.5$, the result is

$$\hat{v}(t) = 1 - \frac{\omega_2}{\omega_2 - \omega_1} e^{-\omega_1 t} - \frac{\omega_1}{\omega_1 - \omega_2} e^{-\omega_2 t} \tag{9.27}$$

with

$$\omega_1, \omega_2 = \frac{\omega_c}{2Q}\left(1 \pm \sqrt{1 - 4Q^2}\right)$$

These equations are plotted in Fig. 9.14 for various values of Q.

According to Eq. (9.23), when $f_2 > 4f_0$, the Q-factor is less than 0.5, and the closed-loop

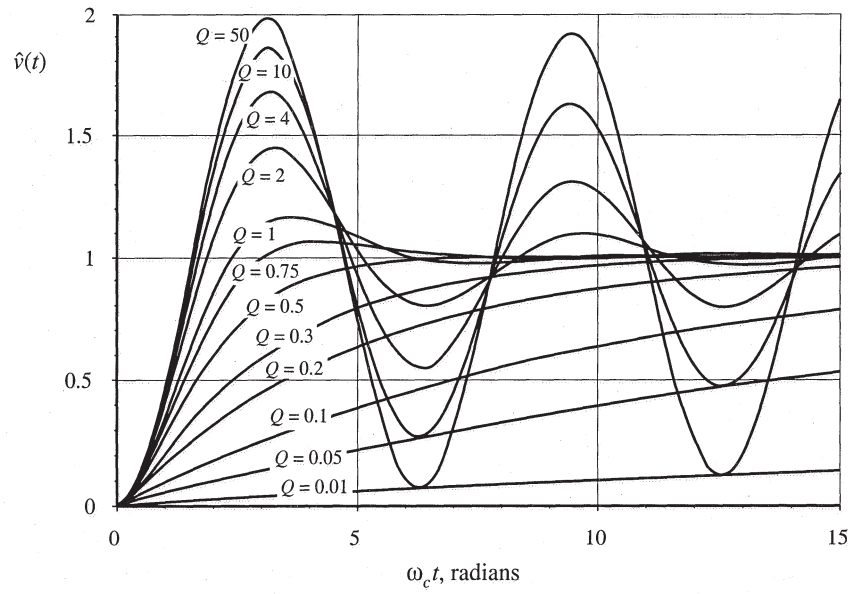


Fig. 9.14 Unit-step response of the second-order system, Eqs. (9.26) and (9.27), for various values of Q.

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response contains a low-frequency and a high-frequency real pole. The transient response in this case, Eq. (9.27), contains decaying-exponential functions of time, of the form

$$Ae^{(pole)t} \tag{9.28}$$

This is called the "overdamped" case. With very low Q, the low-frequency pole leads to a slow step response.

For $f_2 = 4f_0$, the Q-factor is equal to 0.5. The closed-loop response contains two real poles at frequency $2f_0$. This is called the "critically damped" case. The transient response is faster than in the overdamped case, because the lowest-frequency pole is at a higher frequency. This is the fastest response that does not exhibit overshoot. At $\omega_c t = \pi$ radians ($t = 1/2f_c$), the voltage has reached 82% of its final value. At $\omega_c t = 2\pi$ radians ($t = 1/f_c$), the voltage has reached 98.6% of its final value.

For $f_2 < 4f_0$, the Q-factor is greater than 0.5. The closed-loop response contains complex poles, and the transient response exhibits sinusoidal-type waveforms with decaying amplitude, Eq. (9.26). The rise time of the step response is faster than in the critically-damped case, but the waveforms exhibit overshoot. The peak value of $v(t)$ is

$$\text{peak } \hat{v}(t) = 1 + e^{-\pi/\sqrt{4Q^2 - 1}} \tag{9.29}$$

This is called the "underdamped" case. A Q-factor of 1 leads to an overshoot of 16.3%, while a Q-factor of 2 leads to a 44.4% overshoot. Large Q-factors lead to overshoots approaching 100%.

The exact transient response of the feedback loop may differ from the plots of Fig. 9.14, because of additional poles and zeroes in T, and because of differences in initial conditions. Nonetheless, Fig. 9.14 illustrates how high-Q poles lead to overshoot and ringing. In most power applications, overshoot is unacceptable. For example, in a 3.3 V computer power supply, the voltage must not be allowed to overshoot to 5 or 6 volts when the supply is turned on—this would likely destroy all of the integrated circuits in the computer! So the Q-factor must be sufficiently low, often 0.5 or less, corresponding to a phase margin of at least 76°.

9.5 REGULATOR DESIGN

Let's now consider how to design a regulator system, to meet specifications or design goals regarding rejection of disturbances, transient response, and stability. Typical dc regulator designs are defined using specifications such as the following:

1. *Effect of load current variations on the output voltage regulation.* The output voltage must remain within a specified range when the load current varies in a prescribed way. This amounts to a limit on the maximum magnitude of the closed-loop output impedance of Eq. (9.6), repeated below

$$\left.\frac{\hat{v}(s)}{-\hat{i}_{load}(s)}\right|_{\substack{\hat{v}_{ref}=0 \\ \hat{v}_g=0}} = \frac{Z_{out}(s)}{1 + T(s)} \tag{9.30}$$

   If, over some frequency range, the open-loop output impedance Z_{out} has magnitude that exceeds the limit, then the loop gain T must be sufficiently large in magnitude over the same frequency range, such that the magnitude of the closed-loop output impedance given in Eq. (9.30) is less than the given limit.

2. *Effect of input voltage variations (for example, at the second harmonic of the ac line frequency) on the output voltage regulation.* Specific maximum limits are usually placed on the amplitude of variations in the

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output voltage at the second harmonic of the ac line frequency (120 Hz or 100 Hz). If we know the magnitude of the rectification voltage ripple which appears at the converter input (as $\hat{v}_g$), then we can calculate the resulting output voltage ripple (in $\hat{v}$) using the closed loop line-to-output transfer function of Eq. (9.5), repeated below

$$\left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\substack{\hat{v}_{ref}=0 \\ \hat{i}_{load}=0}} = \frac{G_{vg}(s)}{1+T(s)} \tag{9.31}$$

The output voltage ripple can be reduced by increasing the magnitude of the loop gain at the ripple frequency. In a typical good design, $\| T \|$ is 20 dB or more at 120 Hz, so that the transfer function of Eq. (9.31) is at least an order of magnitude smaller than the open-loop line-to-output transfer function $\| G_{vg} \|$.

3. *Transient response time.* When a specified large disturbance occurs, such as a large step change in load current or input voltage, the output voltage may undergo a transient. During this transient, the output voltage typically deviates from its specified allowable range. Eventually, the feedback loop operates to return the output voltage within tolerance. The time required to do so is the transient response time; typically, the response time can be shortened by increasing the feedback loop crossover frequency.

4. *Overshoot and ringing.* As discussed in Section 9.4.3, the amount of overshoot and ringing allowed in the transient response may be limited. Such a specification implies that the phase margin must be sufficiently large.

Each of these requirements imposes constraints on the loop gain $T(s)$. Therefore, the design of the control system involves modifying the loop gain. As illustrated in Fig. 9.2, a compensator network is added for this purpose. Several well-known strategies for design of the compensator transfer function $G_c(s)$ are discussed below.

9.5.1 Lead (*PD*) compensator

This type of compensator transfer function is used to improve the phase margin. A zero is added to the loop gain, at a frequency f_z sufficiently far below the crossover frequency f_c, such that the phase margin of $T(s)$ is increased by the desired amount. The lead compensator is also called a *proportional-plus-derivative*, or *PD*, controller—at high frequencies, the zero causes the compensator to differentiate the error signal. It often finds application in systems originally containing a two-pole response. By use of this type of compensator, the bandwidth of the feedback loop (i.e., the crossover frequency f_c) can be

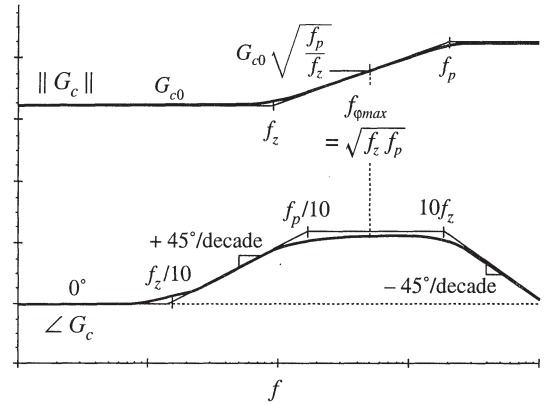


Fig. 9.15 Magnitude and phase asymptotes of the *PD* compensator transfer function G_c of Eq. (9.32).

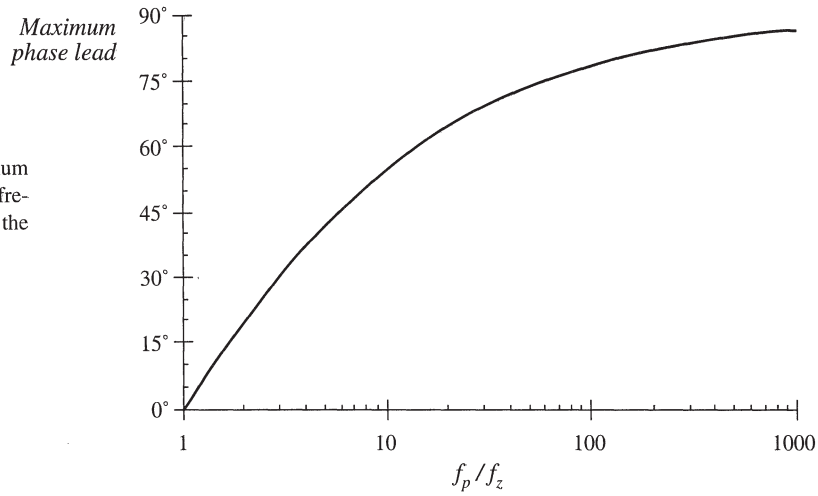


Fig. 9.16 Maximum phase lead θ vs. frequency ratio f_p/f_z for the lead compensator.

extended while maintaining an acceptable phase margin.

A side effect of the zero is that it causes the compensator gain to increase with frequency, with a +20 dB/decade slope. So steps must be taken to ensure that $\| T \|$ remains equal to unity at the desired crossover frequency. Also, since the gain of any practical amplifier must tend to zero at high frequency, the compensator transfer function $G_c(s)$ must contain high frequency poles. These poles also have the beneficial effect of attenuating high-frequency noise. Of particular concern are the switching frequency harmonics present in the output voltage and feedback signals. If the compensator gain at the switching frequency is too great, then these switching harmonics are amplified by the compensator, and can disrupt the operation of the pulse-width modulator (see Section 7.6). So the compensator network should contain poles at a frequency less than the switching frequency. These considerations typically restrict the crossover frequency f_c to be less than approximately 10% of the converter switching frequency f_s. In addition, the circuit designer must take care not to exceed the gain-bandwidth limits of available operational amplifiers.

The transfer function of the lead compensator therefore contains a low-frequency zero and several high-frequency poles. A simplified example containing a single high-frequency pole is given in Eq. (9.32) and illustrated in Fig. 9.15.

$$G_c(s) = G_{c0} \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \tag{9.32}$$

The maximum phase occurs at a frequency $f_{\varphi max}$ given by the geometrical mean of the pole and zero frequencies:

$$f_{\varphi \max} = \sqrt{f_z f_p} \tag{9.33}$$

To obtain the maximum improvement in phase margin, we should design our compensator so that the frequency $f_{\varphi max}$ coincides with the loop gain crossover frequency f_c. The value of the phase at this frequency can be shown to be

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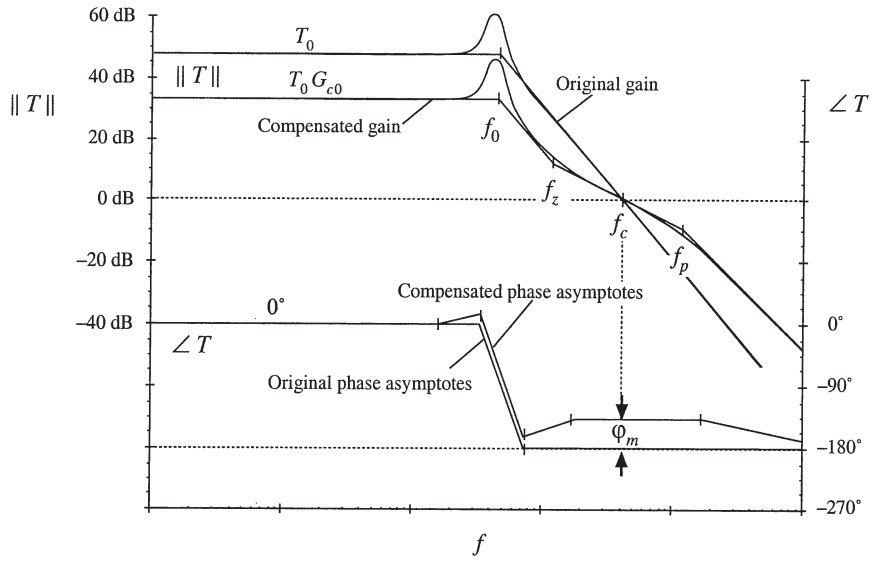


Fig. 9.17 Compensation of a loop gain containing two poles, using a lead (*PD*) compensator. The phase margin φ_m is improved.

$$\angle G_c\left(f_{\varphi\max}\right) = \tan^{-1}\left(\frac{\sqrt{\frac{f_p}{f_z}} - \sqrt{\frac{f_z}{f_p}}}{2}\right) \tag{9.34}$$

This equation is plotted in Fig. 9.16. Equation (9.34) can be inverted to obtain

$$\frac{f_p}{f_z} = \frac{1+\sin(\theta)}{1-\sin(\theta)} \tag{9.35}$$

where $\theta = \angle G_c(f_{\varphi max})$. Equations (9.34) and (9.32) imply that, to optimally obtain a compensator phase lead of θ at frequency f_c, the pole and zero frequencies should be chosen as follows:

$$\begin{aligned} f_z &= f_c \sqrt{\frac{1-\sin(\theta)}{1+\sin(\theta)}} \\ f_p &= f_c \sqrt{\frac{1+\sin(\theta)}{1-\sin(\theta)}} \end{aligned} \tag{9.36}$$

When it is desired to avoid changing the crossover frequency, the magnitude of the compensator gain is chosen to be unity at the loop gain crossover frequency f_c. This requires that G_{c0} be chosen according to the following formula:

$$G_{c0} = \sqrt{\frac{f_z}{f_p}} \tag{9.37}$$

It can be seen that G_{c0} is less than unity, and therefore the lead compensator reduces the dc gain of the

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feedback loop. Other choices of G_{c0} can be selected when it is desired to shift the crossover frequency f_c; for example, increasing the value of G_{c0} causes the crossover frequency to increase. If the frequencies f_p and f_z are chosen as in Eq. (9.36), then $f_{\varphi max}$ of Eq. (9.32) will coincide with the new crossover frequency f_c.

The Bode diagram of a typical loop gain $T(s)$ containing two poles is illustrated in Fig. 9.17. The phase margin of the original $T(s)$ is small, since the crossover frequency f_c is substantially greater than the pole frequency f_0. The result of adding a lead compensator is also illustrated. The lead compensator of this example is designed to maintain the same crossover frequency but improve the phase margin.

9.5.2 Lag (*PI*) Compensator

This type of compensator is used to increase the low-frequency loop gain, such that the output is better regulated at dc and at frequencies well below the loop crossover frequency. As given in Eq. (9.38) and illustrated in Fig. 9.18, an inverted zero is added to the loop gain, at frequency f_L.

$$G_c(s) = G_{c\infty}\left(1 + \frac{\omega_L}{s}\right) \tag{9.38}$$

If f_L is sufficiently lower than the loop crossover frequency f_c, then the phase margin is unchanged. This type of compensator is also called a *proportional-plus-integral*, or *PI*, controller—at low frequencies, the inverted zero causes the compensator to integrate the error signal.

To the extent that the compensator gain can be made arbitrarily large at dc, the dc loop gain $T(0)$ becomes arbitrarily large. This causes the dc component of the error signal to approach zero. In consequence, the steady-state output voltage is perfectly regulated, and the disturbance-to-output transfer functions approach zero at dc. Such behavior is easily obtained in practice, with the compensator of Eq. (9.38) realized using a conventional operational amplifier.

Although the *PI* compensator is useful in nearly all types of feedback systems, it is an especially simple and effective approach for systems originally containing a single pole. For the example of Fig. 9.19, the original uncompensated loop gain is of the form

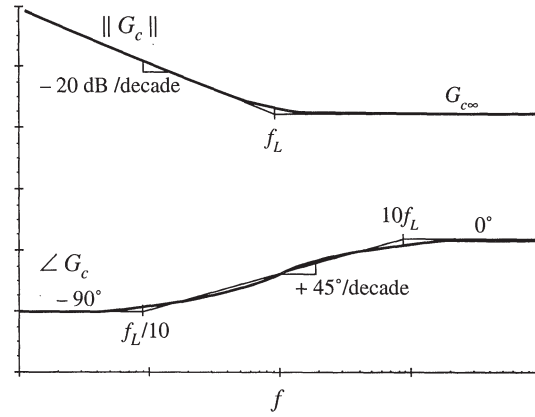


Fig. 9.18 Magnitude and phase asymptotes of the *PI* compensator transfer function G_c of Eq. (9.38).

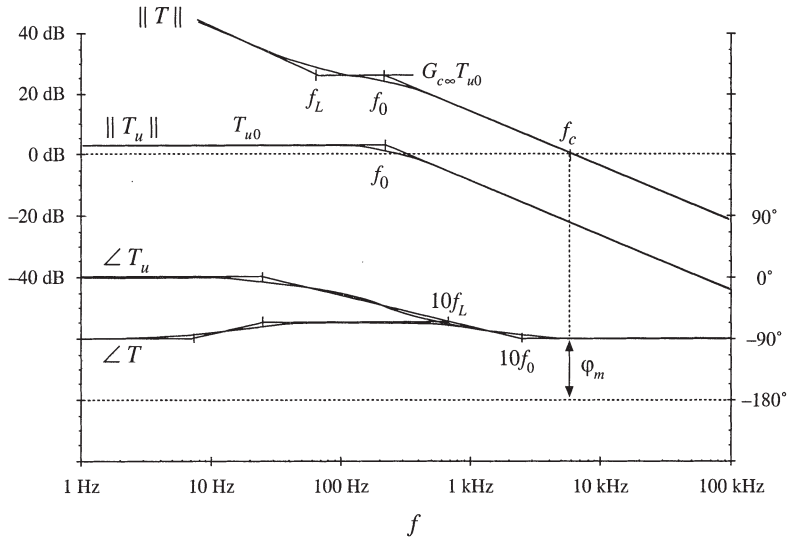


Fig. 9.19 Compensation of a loop gain containing a single pole, using a lag (*PI*) compensator. The loop gain magnitude is increased.

$$T_u(s) = \frac{T_{u0}}{\left(1 + \frac{s}{\omega_0}\right)} \tag{9.39}$$

The compensator transfer function of Eq. (9.38) is used, so that the compensated loop gain is $T(s) = T_u(s)G_c(s)$. Magnitude and phase asymptotes of $T(s)$ are also illustrated in Fig. 9.19. The compensator high-frequency gain $G_{c\infty}$ is chosen to obtain the desired crossover frequency f_c. If we approximate the compensated loop gain by its high-frequency asymptote, then at high frequencies we can write

$$\| T \| \approx \frac{T_{u0} G_{c\infty}}{\left(\frac{f}{f_0}\right)} \tag{9.40}$$

At the crossover frequency $f = f_c$, the loop gain has unity magnitude. Equation (9.40) predicts that the crossover frequency is

$$f_c \approx T_{u0} G_{c\infty} f_0 \tag{9.41}$$

Hence, to obtain a desired crossover frequency f_c, we should choose the compensator gain $G_{c\infty}$ as follows:

$$G_{c\infty} = \frac{f_c}{T_{u0} f_0} \tag{9.42}$$

The corner frequency f_L is then chosen to be sufficiently less than f_c, such that an adequate phase margin is maintained.

Magnitude asymptotes of the quantity $1/(1 + T(s))$ are constructed in Fig. 9.20. At frequencies

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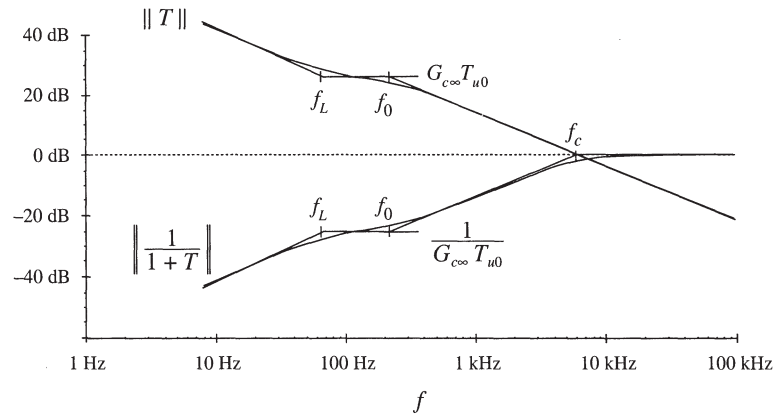


Fig. 9.20 Construction of || 1/(1 + *T*) || for the *PI*-compensated example of Fig. 9.19.

less than f_L, the *PI* compensator improves the rejection of disturbances. At dc, where the magnitude of G_c approaches infinity, the magnitude of 1/(1 + *T*) tends to zero. Hence, the closed-loop disturbance-to-output transfer functions, such as Eqs. (9.30) and (9.31), tend to zero at dc.

9.5.3 Combined (*PID*) Compensator

The advantages of the lead and lag compensators can be combined, to obtain both wide bandwidth and zero steady-state error. At low frequencies, the compensator integrates the error signal, leading to large low-frequency loop gain and accurate regulation of the low-frequency components of the output voltage. At high frequency (in the vicinity of the crossover frequency), the compensator introduces phase lead into the loop gain, improving the phase margin. Such a compensator is sometimes called a *PID* controller.

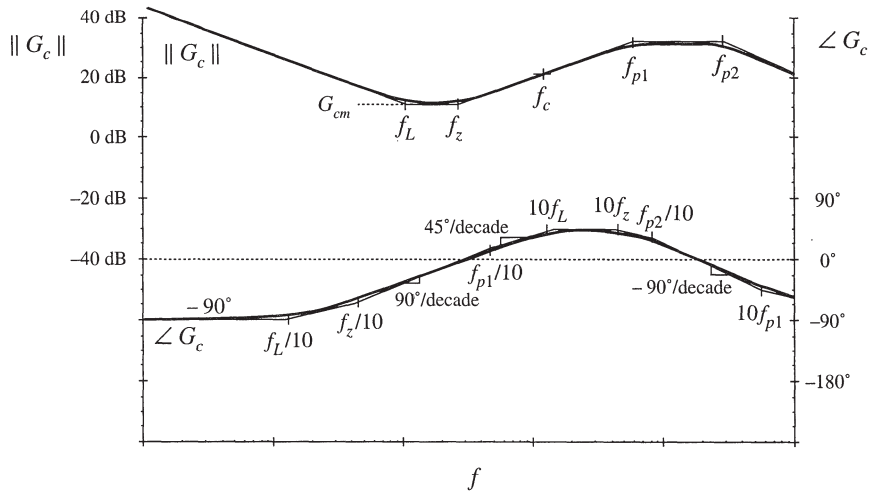


Fig. 9.21 Magnitude and phase asymptotes of the combined (*PID*) compensator transfer function G_c of Eq. (9.43).

A typical Bode diagram of a practical version of this compensator is illustrated in Fig. 9.21. The compensator has transfer function

$$G_c(s) = G_{cm} \frac{\left(1 + \frac{\omega_L}{s}\right)\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \tag{9.43}$$

The inverted zero at frequency f_L functions in the same manner as the *PI* compensator. The zero at frequency f_z adds phase lead in the vicinity of the crossover frequency, as in the *PD* compensator. The high-frequency poles at frequencies f_{p1} and f_{p2} must be present in practical compensators, to cause the gain to roll off at high frequencies and to prevent the switching ripple from disrupting the operation of the pulse-width modulator. The loop gain crossover frequency f_c is chosen to be greater than f_L and f_z, but less than f_{p1} and f_{p2}.

9.5.4 Design Example

To illustrate the design of *PI* and *PD* compensators, let us consider the design of a combined *PID* compensator for the dc–dc buck converter system of Fig. 9.22. The input voltage $v_g(t)$ for this system has nominal value 28 V. It is desired to supply a regulated 15 V to a 5 A load. The load is modeled here with a 3 Ω resistor. An accurate 5 V reference is available.

The first step is to select the feedback gain $H(s)$. The gain H is chosen such that the regulator produces a regulated 15 V dc output. Let us assume that we will succeed in designing a good feedback system, which causes the output voltage to accurately follow the reference voltage. This is accomplished via a large loop gain T, which leads to a small error voltage: $v_e \approx 0$. Hence, $Hv \approx v_{ref}$. So we should choose

$$H = \frac{V_{ref}}{V} = \frac{5}{15} = \frac{1}{3} \tag{9.44}$$

The quiescent duty cycle is given by the steady-state solution of the converter:

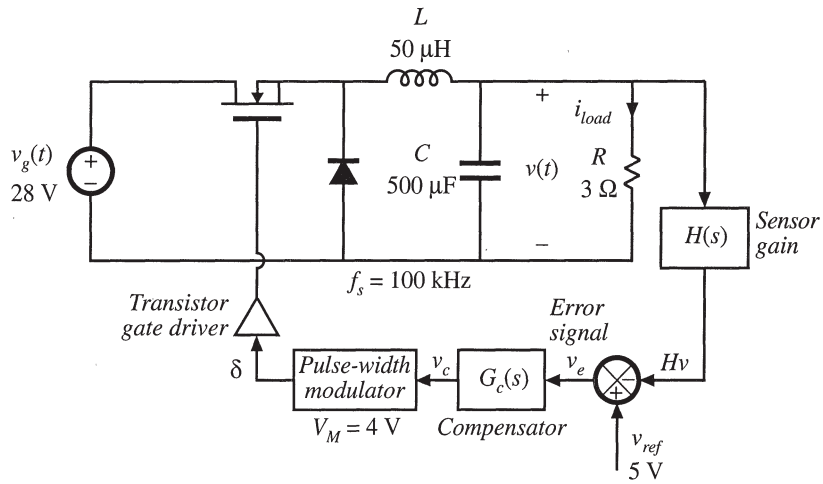


Fig. 9.22 Design example.

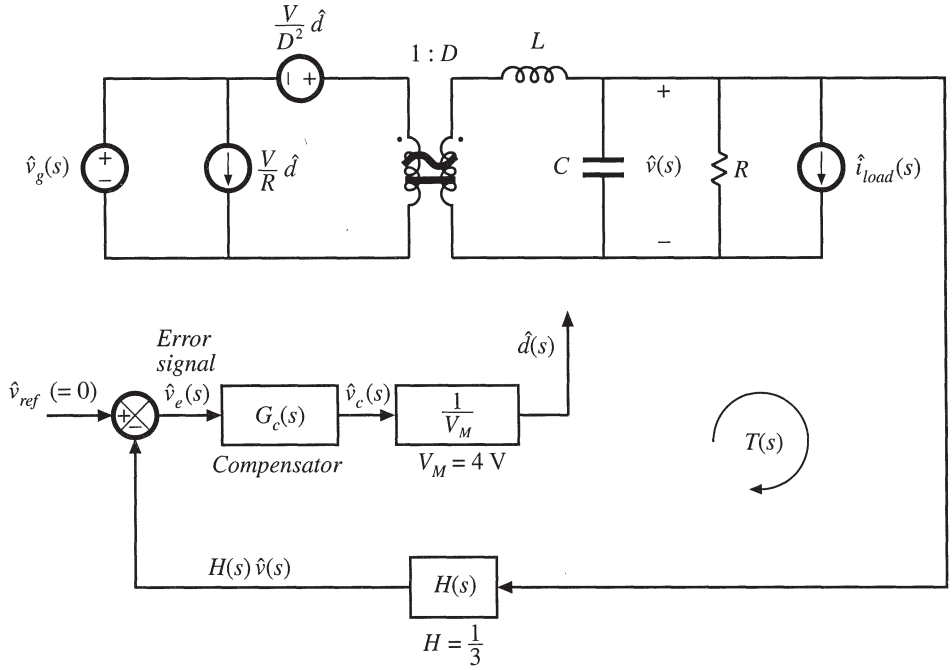


Fig. 9.23 System small-signal ac model, design example.

$$D = \frac{V}{V_g} = \frac{15}{28} = 0.536 \tag{9.45}$$

The quiescent value of the control voltage, V_c, must satisfy Eq. (7.173). Hence,

$$V_c = DV_M = 2.14 \text{ V} \tag{9.46}$$

Thus, the quiescent conditions of the system are known. It remains to design the compensator gain $G_c(s)$.

A small-signal ac model of the regulator system is illustrated in Fig. 9.23. The buck converter ac model is represented in canonical form. Disturbances in the input voltage and in the load current are modeled. For generality, reference voltage variations $\hat{v}_{ref}$ are included in the diagram; in a dc voltage regulator, these variations are normally zero.

The open-loop converter transfer functions are discussed in the previous chapters. The open-loop control-to-output transfer function is

$$G_{vd}(s) = \frac{V}{D} \frac{1}{1 + s\frac{L}{R} + s^2LC} \tag{9.47}$$

The open-loop control-to-output transfer function contains two poles, and can be written in the following normalized form:

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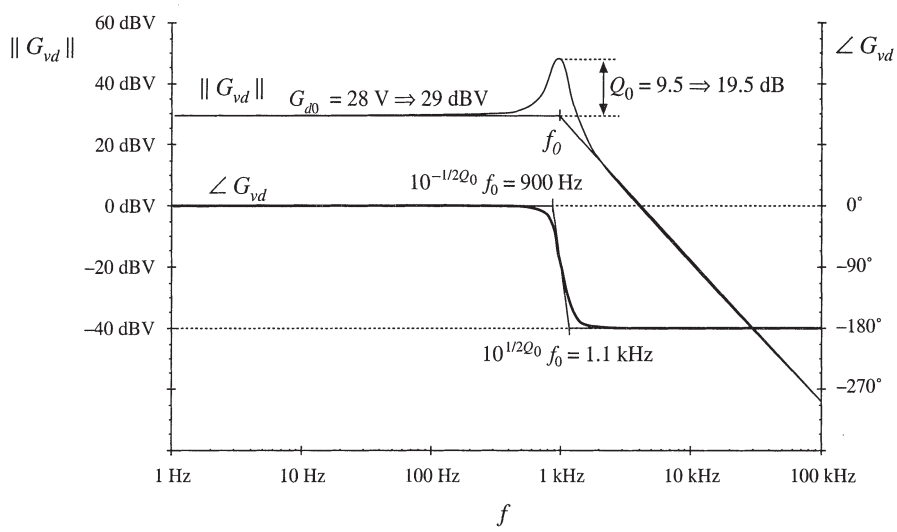


Fig. 9.24 Converter small-signal control-to-output transfer function G_{vd}, design example.

$$G_{vd}(s) = G_{d0} \frac{1}{1 + \frac{s}{Q_0\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{9.48}$$

By equating like coefficients in Eqs. (9.47) and (9.48), one finds that the dc gain, corner frequency, and Q-factor are given by

$$\begin{aligned} G_{d0} &= \frac{V}{D} = 28 \text{ V} \\ f_0 &= \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{LC}} = 1 \text{ kHz} \\ Q_0 &= R\sqrt{\frac{C}{L}} = 9.5 \Rightarrow 19.5 \text{ dB} \end{aligned} \tag{9.49}$$

In practice, parasitic loss elements, such as the capacitor equivalent series resistance (*esr*), would cause a lower Q-factor to be observed. Figure 9.24 contains a Bode diagram of $G_{vd}(s)$.

The open-loop line-to-output transfer function is

$$G_{vg}(s) = D \frac{1}{1 + s\frac{L}{R} + s^2LC} \tag{9.50}$$

This transfer function contains the same poles as in $G_{vd}(s)$, and can be written in the normalized form

$$G_{vg}(s) = G_{g0} \frac{1}{1 + \frac{s}{Q_0\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{9.51}$$

with $G_{g0} = D$. The open-loop output impedance of the buck converter is

$$Z_{out}(s) = R \parallel \frac{1}{sC} \parallel sL = \frac{sL}{1 + s\frac{L}{R} + s^2LC} \tag{9.52}$$

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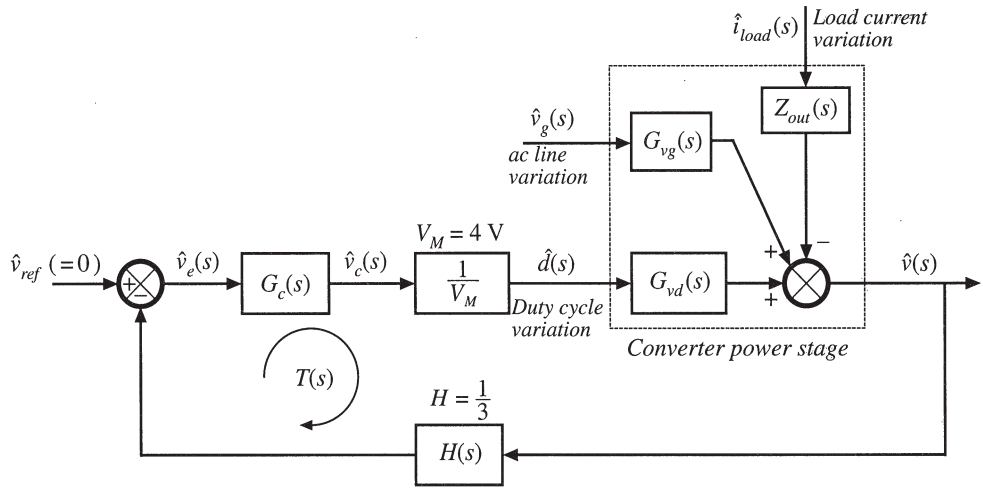


Fig. 9.25 System block diagram, design example.

Use of these equations to represent the converter in block-diagram form leads to the complete system block diagram of Fig. 9.25. The loop gain of the system is

$$T(s) = G_c(s)\left(\frac{1}{V_M}\right)G_{vd}(s)H(s) \tag{9.53}$$

Substitution of Eq. (9.48) into (9.53) leads to

$$T(s) = \frac{G_c(s)H(s)}{V_M}\frac{V}{D}\frac{1}{\left(1 + \frac{s}{Q_0\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)} \tag{9.54}$$

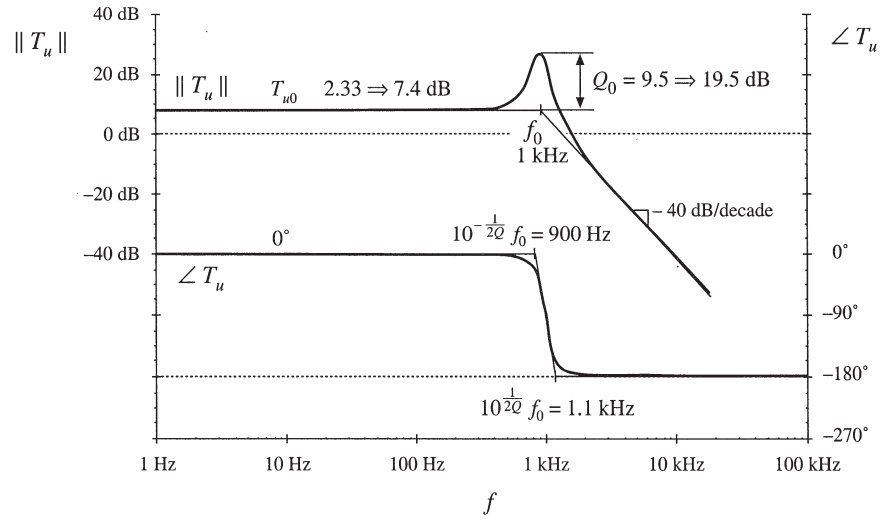


Fig. 9.26 Uncompensated loop gain T_u, design example.

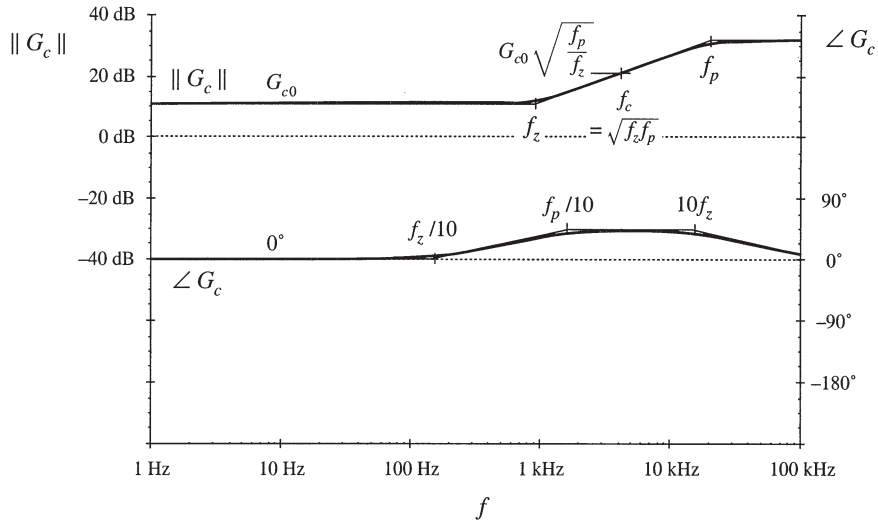


Fig. 9.27 *PD* compensator transfer function G_c, design example.

The closed-loop disturbance-to-output transfer functions are given by Eqs. (9.5) and (9.6).

The uncompensated loop gain $T_u(s)$, with unity compensator gain, is sketched in Fig. 9.26. With $G_c(s) = 1$, Eq. (9.54) can be written

$$T_u(s) = T_{u0} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{9.55}$$

where the dc gain is

$$T_{u0} = \frac{HV}{DV_M} = 2.33 \Rightarrow 7.4 \text{ dB} \tag{9.56}$$

The uncompensated loop gain has a crossover frequency of approximately 1.8 kHz, with a phase margin of less than five degrees.

Let us design a compensator, to attain a crossover frequency of $f_c = 5$ kHz, or one twentieth of the switching frequency. From Fig. 9.26, the uncompensated loop gain has a magnitude at 5 kHz of approximately $T_{u0}\,(f_0/f_c)^2 = 0.093 \Rightarrow -20.6$ dB. So to obtain unity loop gain at 5 kHz, our compensator should have a 5 kHz gain of +20.6 dB. In addition, the compensator should improve the phase margin, since the phase of the uncompensated loop gain is nearly –180° at 5 kHz. So a lead (*PD*) compensator is needed. Let us (somewhat arbitrarily) choose to design for a phase margin of 52°. According to Fig. 9.13, this choice leads to closed-loop poles having a Q-factor of 1. The unit step response, Fig. 9.14, then exhibits a peak overshoot of 16%. Evaluation of Eq. (9.36), with $f_c = 5$ kHz and $\theta = 52°$, leads to the following compensator pole and zero frequencies:

$$\begin{aligned} f_z &= (5 \text{ kHz}) \sqrt{\frac{1 - \sin(52°)}{1 + \sin(52°)}} = 1.7 \text{ kHz} \\ f_p &= (5 \text{ kHz}) \sqrt{\frac{1 + \sin(52°)}{1 - \sin(52°)}} = 14.5 \text{ kHz} \end{aligned} \tag{9.57}$$

To obtain a compensator gain of 20.6 dB $\Rightarrow$ 10.7 at 5 kHz, the low-frequency compensator gain must be

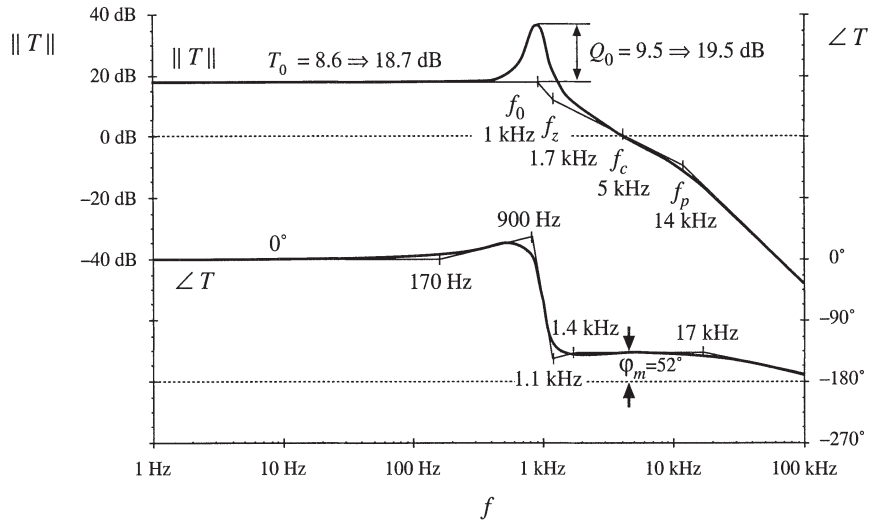


Fig. 9.28 The compensated loop gain of Eq. (9.59).

$$G_{c0} = \left(\frac{f_c}{f_0}\right)^2 \frac{1}{T_{u0}} \sqrt{\frac{f_z}{f_p}} = 3.7 \Rightarrow 11.3 \text{ dB} \tag{9.58}$$

A Bode diagram of the *PD* compensator magnitude and phase is sketched in Fig. 9.27.

With this *PD* controller, the loop gain becomes

$$T(s) = T_{u0} G_{c0} \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)\left(1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)} \tag{9.59}$$

The compensated loop gain is sketched in Fig. 9.28. It can be seen that the phase of $T(s)$ is approximately equal to 52° over the frequency range of 1.4 kHz to 17 kHz. Hence variations in component values, which cause the crossover frequency to deviate somewhat from 5 kHz, should have little impact on the phase margin. In addition, it can be seen from Fig. 9.28 that the loop gain has a dc magnitude of $T_{u0}G_{c0}$ $\Rightarrow$ 18.7 dB.

Asymptotes of the quantity $1/(1 + T)$ are constructed in Fig. 9.29. This quantity has a dc asymptote of –18.7 dB. Therefore, at frequencies less than 1 kHz, the feedback loop attenuates output voltage disturbances by 18.7 dB. For example, suppose that the input voltage $v_g(t)$ contains a 100 Hz variation of amplitude 1 V. With no feedback loop, this disturbance would propagate to the output according to the open-loop transfer function $G_{vg}(s)$, given in Eq. (9.51). At 100 Hz, this transfer function has a gain essentially equal to the dc asymptote $D = 0.536$. Therefore, with no feedback loop, a 100 Hz variation of amplitude 0.536 V would be observed at the output. In the presence of feedback, the closed-loop line-to-output transfer function of Eq. (9.5) is obtained; for our example, this attenuates the 100 Hz variation by an additional factor of 18.7 dB $\Rightarrow$ 8.6. The 100 Hz output voltage variation now has magnitude 0.536/8.6 = 0.062 V.

The low-frequency regulation can be further improved by addition of an inverted zero, as discussed in Section 9.5.2. A *PID* controller, as in Section 9.5.3, is then obtained. The compensator transfer

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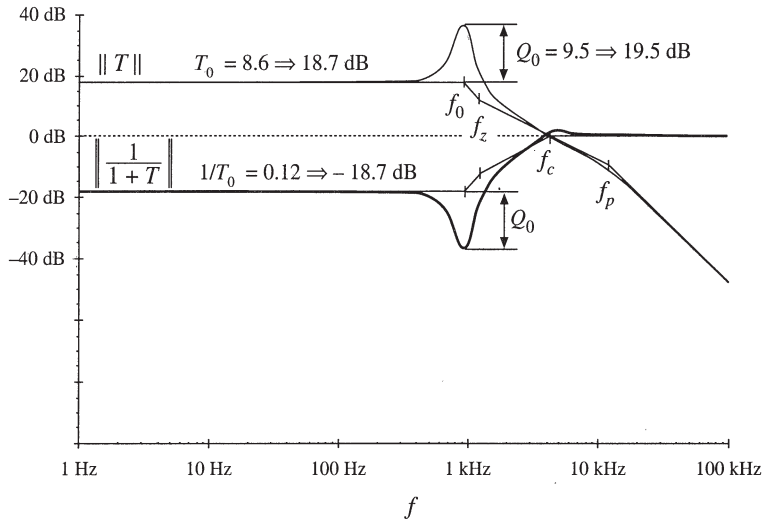


Fig. 9.29 Construction of || 1/(1 + *T*) || for the *PD*-compensated design example of Fig. 9.28.

function becomes

$$G_c(s) = G_{cm}\frac{\left(1+\frac{s}{\omega_z}\right)\left(1+\frac{\omega_L}{s}\right)}{\left(1+\frac{s}{\omega_p}\right)} \tag{9.60}$$

The Bode diagram of this compensator gain is illustrated in Fig. 9.30. The pole and zero frequencies f_z and f_p are unchanged, and are given by Eq. (9.57). The midband gain G_{cm} is chosen to be the same as the previous G_{c0}, Eq. (9.58). Hence, for frequencies greater than f_L, the magnitude of the loop gain is

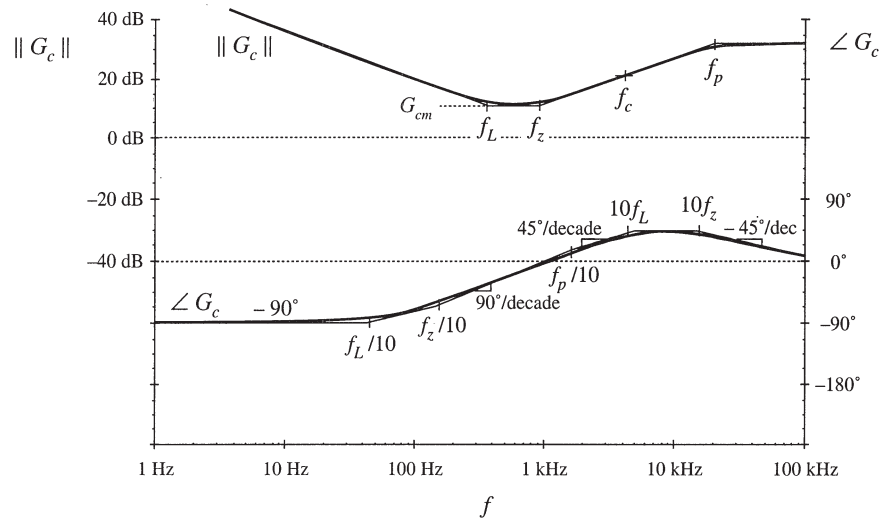


Fig. 9.30 *PID* compensator transfer function, Eq. (9.60).

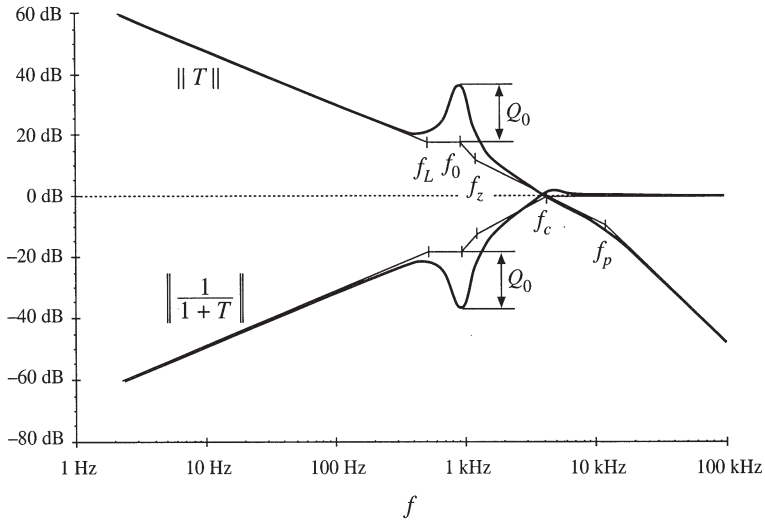


Fig. 9.31 Construction of $\| T \|$ and $\| 1/(1 + T) \|$ with the *PID*-compensator of Fig. 9.30.

unchanged by the inverted zero. The loop continues to exhibit a crossover frequency of 5 kHz.

So that the inverted zero does not significantly degrade the phase margin, let us (somewhat arbitrarily) choose f_L to be one-tenth of the crossover frequency, or 500 Hz. The inverted zero will then increase the loop gain at frequencies below 500 Hz, improving the low-frequency regulation of the output voltage. The loop gain of Fig. 9.31 is obtained. The magnitude of the quantity $1/(1 + T)$ is also constructed. It can be seen that the inverted zero at 500 Hz causes the magnitude of $1/(1 + T)$ at 100 Hz to be reduced by a factor of approximately (100 Hz)/(500 Hz) = 1/5. The total attenuation of $1/(1 + T)$ at 100 Hz is –32.7dB. A 1 V, 100 Hz variation in $v_g(t)$ would now induce a 12 mV variation in $v(t)$. Further improvements could be obtained by increasing f_L; however, this would require redesign of the *PD* portion of the compensator to maintain an adequate phase margin.

The line-to-output transfer function is constructed in Fig. 9.32. Both the open-loop transfer function $G_{vg}(s)$, Eq. (9.51), and the closed-loop transfer function $G_{vg}(s)/(1 + T(s))$, are constructed using the algebra-on-the-graph method. The two transfer functions coincide at frequencies greater than the crossover frequency. At frequencies less than the crossover frequency f_c, the closed-loop transfer function is reduced by a factor of $T(s)$. It can be seen that the poles of $G_{vg}(s)$ are cancelled by zeroes of $1/(1 + T)$. Hence the closed-loop line-to-output transfer function is approximately

$$\frac{G_{vg}(s)}{\left(1 + T(s)\right)} \approx \frac{D}{T_{u0} G_{cm}} \frac{1}{\left(1 + \frac{\omega_L}{s}\right)\left(1 + \frac{s}{\omega_z}\right)\left(1 + \frac{s}{\omega_c}\right)} \tag{9.61}$$

So the algebra-on-the-graph method allows simple approximate disturbance-to-output closed-loop transfer functions to be written. Armed with such an analytical expression, the system designer can easily compute the output disturbances, and can gain the insight required to shape the loop gain $T(s)$ such that system specifications are met. Computer simulations can then be used to judge whether the specifications are met under all operating conditions, and over expected ranges of component parameter values. Results of computer simulations of the design example described in this section can be found in Appendix B, Section B.2.2.

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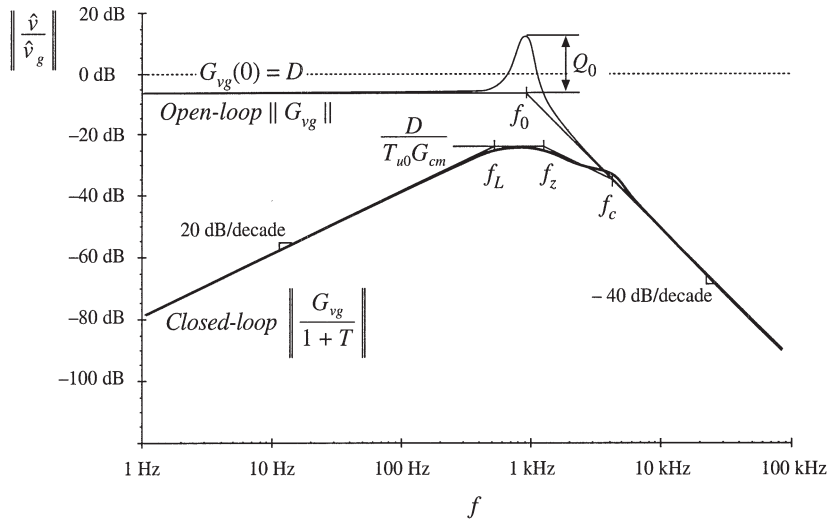


Fig. 9.32 Comparison of open-loop line-to-output transfer function G_{vg} and closed-loop line-to-output transfer function of Eq. (9.61).

9.6 MEASUREMENT OF LOOP GAINS

It is good engineering practice to measure the loop gains of prototype feedback systems. The objective of such an exercise is to verify that the system has been correctly modeled. If so, then provided that a good controller design has been implemented, then the system behavior will meet expectations regarding transient overshoot (and phase margin), rejection of disturbances, dc output voltage regulation, etc. Unfortunately, there are reasons why practical system prototypes are likely to differ from theoretical models. Phenomena may occur that were not accounted for in the original model, and that significantly influence the system behavior. Noise and electromagnetic interference (EMI) can be present, which cause the system transfer functions to deviate in unexpected ways.

So let us consider the measurement of the loop gain $T(s)$ of the feedback system of Fig. 9.33.

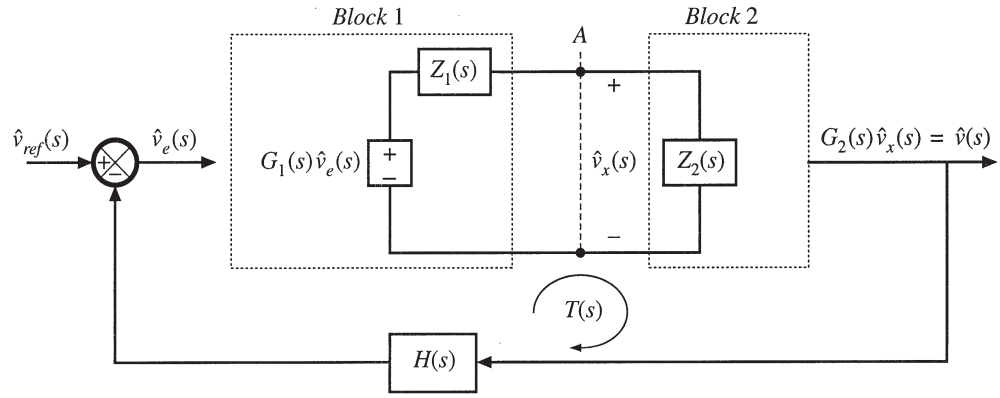


Fig. 9.33 It is desired to determine the loop gain $T(s)$ experimentally, by making measurements at point A.

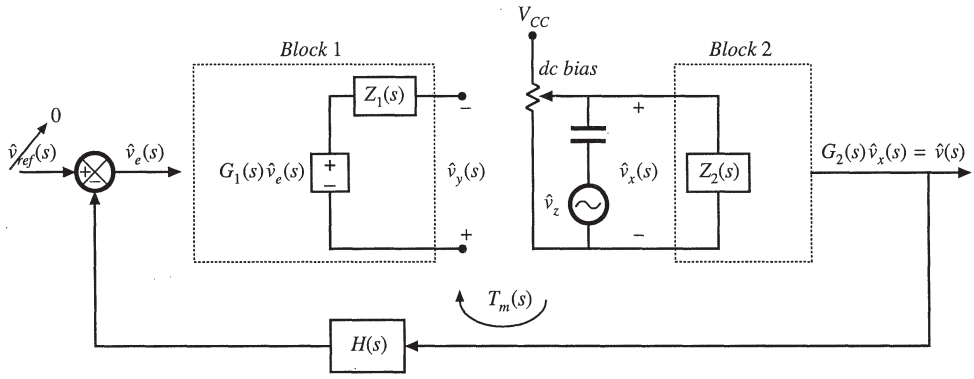


Fig. 9.34 Measurement of loop gain by breaking the loop.

We will make measurements at some point A, where two blocks of the network are connected electrically. In Fig. 9.33, the output port of block 1 is represented by a Thevenin-equivalent network, composed of the dependent voltage source $G_1\hat{v}_e$ and output impedance Z_1. Block 1 is loaded by the input impedance Z_2 of block 2. The remainder of the feedback system is represented by a block diagram as shown. The loop gain of the system is

$$T(s) = G_1(s)\left(\frac{Z_2(s)}{Z_1(s) + Z_2(s)}\right)G_2(s)H(s) \tag{9.62}$$

Measurement of this loop gain presents several challenges not present in other frequency response measurements.

In principle, one could break the loop at point A, and attempt to measure $T(s)$ using the transfer function measurement method of the previous chapter. As illustrated in Fig. 9.34, a dc supply voltage V_{CC} and potentiometer would be used, to establish a dc bias in the voltage v_x, such that all of the elements of the network operate at the correct quiescent point. Ac voltage variations in $v_z(t)$ are coupled into the injection point via a dc blocking capacitor. Any other independent ac inputs to the system are disabled. A network analyzer is used to measure the relative magnitudes and phases of the ac components of the voltages $v_y(t)$ and $v_x(t)$:

$$T_m(s) = \left.\frac{\hat{v}_y(s)}{\hat{v}_x(s)}\right|_{\substack{\hat{v}_{ref}=0 \\ \hat{v}_g=0}} \tag{9.63}$$

The measured gain $T_m(s)$ differs from the actual gain $T(s)$ because, by breaking the connection between blocks 1 and 2 at the measurement point, we have removed the loading of block 2 on block 1. Solution of Fig. 9.34 for the measured gain $T_m(s)$ leads to

$$T_m(s) = G_1(s)G_2(s)H(s) \tag{9.64}$$

Equations (9.62) and (9.64) can be combined to express $T_m(s)$ in terms of $T(s)$:

$$T_m(s) = T(s)\left(1 + \frac{Z_1(s)}{Z_2(s)}\right) \tag{9.65}$$

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Hence,

$$T_m(s) \approx T(s) \quad \text{provided that} \quad \|Z_2\| \gg \|Z_1\| \tag{9.66}$$

So to obtain an accurate measurement, we need to find an injection point where loading is negligible over the range of frequencies to be measured.

Other difficulties are encountered when using the method of Fig. 9.34. The most serious problem is adjustment of the dc bias using a potentiometer. The dc loop gain is typically very large, especially when a *PI* controller is used. A small change in the dc component of $v_x(t)$ can therefore lead to very large changes in the dc biases of some elements in the system. So it is difficult to establish the correct dc conditions in the circuit. The dc gains may drift during the experiment, making the problem even worse, and saturation of the error amplifier is a common complaint. Also, we have seen that the gains of the converter can be a function of the quiescent operating point; significant deviation from the correct operating point can cause the measured gain to differ from the loop gain of actual operating conditions.

9.6.1 Voltage Injection

An approach that avoids the dc biasing problem [3] is illustrated in Fig. 9.35. The voltage source $v_z(t)$ is injected between blocks 1 and 2, without breaking the feedback loop. Ac variations in $v_z(t)$ again excite variations in the feedback system, but dc bias conditions are determined by the circuit. Indeed, if $v_z(t)$ contains no dc component, then the biasing circuits of the system itself establish the quiescent operating point. Hence, the loop gain measurement is made at the actual system operating point.

The injection source is modeled in Fig. 9.35 by a Thevenin equivalent network, containing an independent voltage source with source impedance $Z_s(s)$. The magnitudes of v_z and Z_s are irrelevant in the determination of the loop gain. However, the injection of v_z does disrupt the loading of block 2 on block 1. Hence, a suitable injection point must be found, where the loading effect is negligible.

To measure the loop gain by voltage injection, we connect a network analyzer to measure the transfer function from $\hat{v}_x$ to $\hat{v}_y$. The system independent ac inputs are set to zero, and the network analyzer sweeps the injection voltage $\hat{v}_z(t)$ over the intended frequency range. The measured gain is

$$T_v(s) = \left.\frac{\hat{v}_y(s)}{\hat{v}_x(s)}\right|_{\substack{\hat{v}_{ref}=0 \\ \hat{v}_g=0}} \tag{9.67}$$

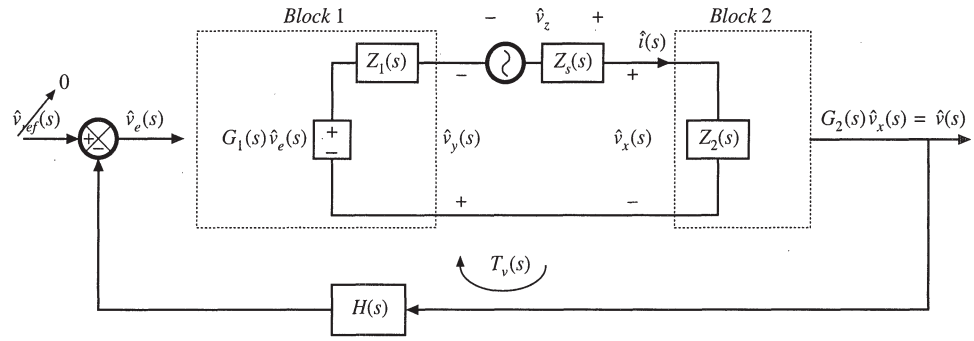


Fig. 9.35 Measurement of loop gain by voltage injection.

Let us solve Fig. 9.35, to compare the measured gain $T_v(s)$ with the actual loop gain $T(s)$ given by (9.62). The error signal is

$$\hat{v}_e(s) = -H(s)G_2(s)\hat{v}_x(s) \tag{9.68}$$

The voltage $\hat{v}_y$ can be written

$$-\hat{v}_y(s) = G_1(s)\hat{v}_e(s) - \hat{i}(s)Z_1(s) \tag{9.69}$$

where $\hat{i}(s)Z_1(s)$ is the voltage drop across the source impedance Z_1. Substitution of Eq. (9.68) into (9.69) leads to

$$-\hat{v}_y(s) = -\hat{v}_x(s)G_2(s)H(s)G_1(s) - \hat{i}(s)Z_1(s) \tag{9.70}$$

But $\hat{i}(s)$ is

$$\hat{i}(s) = \frac{\hat{v}_x(s)}{Z_2(s)} \tag{9.71}$$

Therefore, Eq. (9.70) becomes

$$\hat{v}_y(s) = \hat{v}_x(s)\left(G_1(s)G_2(s)H(s) + \frac{Z_1(s)}{Z_2(s)}\right) \tag{9.72}$$

Substitution of Eq. (9.72) into (9.67) leads to the following expression for the measured gain $T_v(s)$:

$$T_v(s) = G_1(s)G_2(s)H(s) + \frac{Z_1(s)}{Z_2(s)} \tag{9.73}$$

Equations (9.62) and (9.73) can be combined to determine the measured gain $T_v(s)$ in terms of the actual loop gain $T(s)$:

$$T_v(s) = T(s)\left(1 + \frac{Z_1(s)}{Z_2(s)}\right) + \frac{Z_1(s)}{Z_2(s)} \tag{9.74}$$

Thus, $T_v(s)$ can be expressed as the sum of two terms. The first term is proportional to the actual loop gain $T(s)$, and is approximately equal to $T(s)$ whenever $\| Z_1 \| \ll \| Z_2 \|$. The second term is not proportional to $T(s)$, and limits the minimum $T(s)$ that can be measured with the voltage injection technique. If Z_1/Z_2 is much smaller in magnitude than $T(s)$, then the second term can be ignored, and $T_v(s) \approx T(s)$. At frequencies where $T(s)$ is smaller in magnitude than Z_1/Z_2, the measured data must be discarded. Thus,

$$T_v(s) \approx T(s) \tag{9.75}$$

provided

$$(i) \quad \left\| Z_1(s) \right\| \ll \left\| Z_2(s) \right\|$$

and

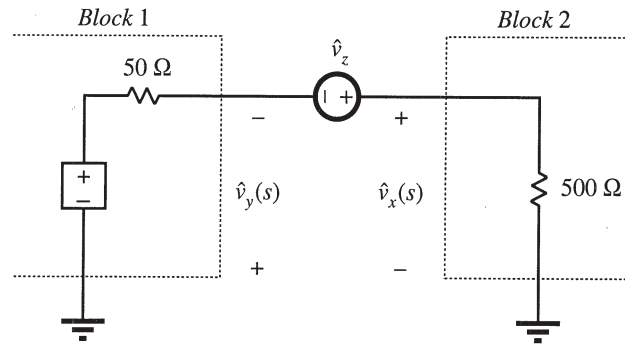


Fig. 9.36 Voltage injection example.

$$(ii)\ \|T(s)\| \gg \left\|\frac{Z_1(s)}{Z_2(s)}\right\|$$

Again, note that the value of the injection source impedance Z_s is irrelevant.

As an example, consider voltage injection at the output of an operational amplifier, having a 50 Ω output impedance, which drives a 500 Ω effective load. The system in the vicinity of the injection point is illustrated in Fig. 9.36. So $Z_1(s) = 50\ \Omega$ and $Z_2(s) = 500\ \Omega$. The ratio Z_1/Z_2 is 0.1, or –20 dB. Let us further suppose that the actual loop gain $T(s)$ contains poles at 10 Hz and 100 kHz, with a dc gain of 80 dB. The actual loop gain magnitude is illustrated in Fig. 9.37.

Voltage injection would result in measurement of $T_v(s)$ given in Eq. (9.74). Note that

$$\left(1 + \frac{Z_1(s)}{Z_2(s)}\right) = 1.1 \Rightarrow 0.83\ \text{dB} \tag{9.76}$$

Hence, for large $\| T \|$, the measured $\| T_v \|$ deviates from the actual loop gain by less than 1 dB. However, at high frequency where $\| T \|$ is less than –20 dB, the measured gain differs significantly. Apparently,

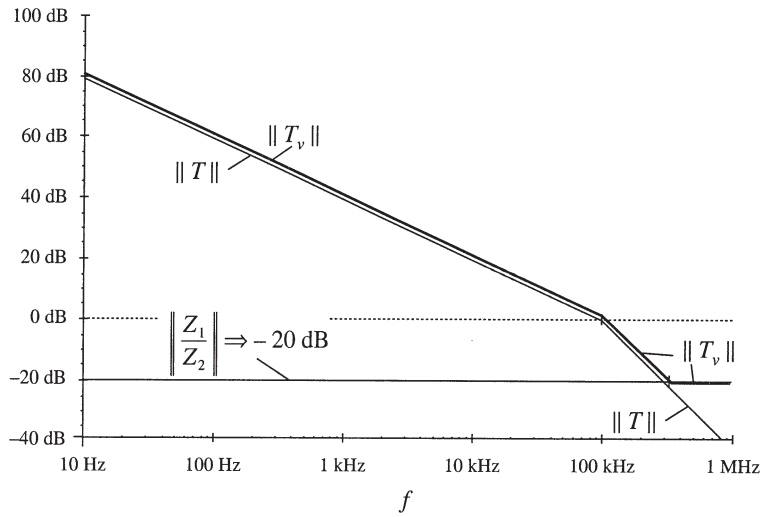


Fig. 9.37 Comparison of measured loop gain T_v and actual loop gain T, voltage injection example. The measured gain deviates at high frequency.

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$T_v(s)$ contains two high-frequency zeroes that are not present in $T(s)$. Depending on the Q-factor of these zeroes, the phase of T_v at the crossover frequency could be influenced. To ensure that the phase margin is correctly measured, it is important that Z_1/Z_2 be sufficiently small in magnitude.

9.6.2 Current Injection

The results of the preceding paragraphs can also be obtained in dual form, where the loop gain is measured by current injection [3]. As illustrated in Fig. 9.38, we can model block 1 and the analyzer injection source by their Norton equivalents, and use current probes to measure $\hat{i}_x$ and $\hat{i}_y$. The gain measured by current injection is

$$T_i(s) = \left.\frac{\hat{i}_y(s)}{\hat{i}_x(s)}\right|_{\substack{\hat{v}_{ref}=0 \\ \hat{v}_g=0}} \tag{9.77}$$

It can be shown that

$$T_i(s) = T(s)\left(1 + \frac{Z_2(s)}{Z_1(s)}\right) + \frac{Z_2(s)}{Z_1(s)} \tag{9.78}$$

Hence,

$$T_i(s) \approx T(s) \text{ provided}$$

$$(i)\ \left\|Z_2(s)\right\| \ll \left\|Z_1(s)\right\|, \text{ and} \tag{9.79}$$

$$(ii)\ \left\|T(s)\right\| \gg \left\|\frac{Z_2(s)}{Z_1(s)}\right\|$$

So to obtain an accurate measurement of the loop gain by current injection, we must find a point in the network where block 2 has sufficiently small input impedance. Again, note that the injection source impedance Z_s does not affect the measurement. In fact, we can realize i_z by use of a Thevenin-equivalent source, as illustrated in Fig. 9.39. The network analyzer injection source is represented by voltage source

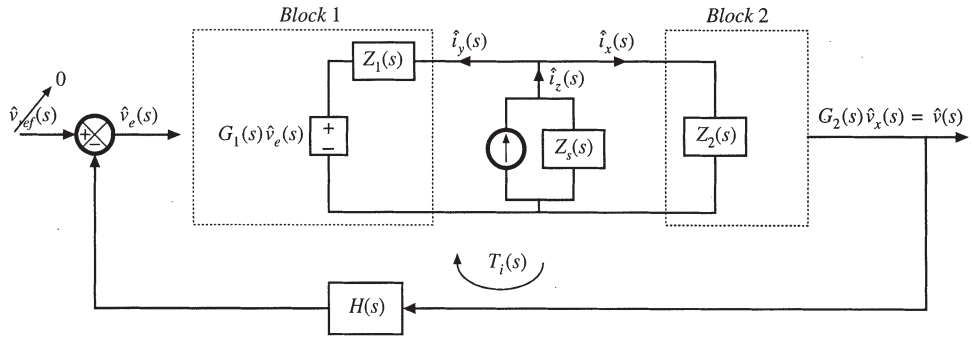


Fig. 9.38 Measurement of loop gain by current injection.

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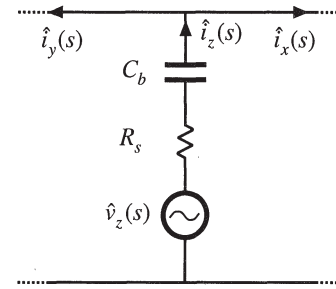


Fig. 9.39 Current injection using Thevenin-equivalent source.

$\hat{v}_z$ and output resistance R_s. A series capacitor, C_b, is inserted to avoid disrupting the dc bias at the injection point.

9.6.3 Measurement of Unstable Systems

When the prototype feedback system is unstable, we are even more eager to measure the loop gain—to find out what went wrong. But measurements cannot be made while the system oscillates. We need to stabilize the system, yet measure the original unstable loop gain. It is possible to do this by recognizing that the injection source impedance Z_s does not influence the measured loop gain [3]. As illustrated in Fig. 9.40, we can even add additional resistance R_{ext}, effectively increasing the source impedance Z_s. The measured loop gain $T_v(s)$ is unaffected.

Adding series impedance generally lowers the loop gain of a system, leading to a lower crossover frequency and a more positive phase margin. Hence, it is usually possible to add a resistor R_{ext} that is sufficiently large to stabilize the system. The gain $T_v(s)$, Eq. (9.67), continues to be approximately equal to the original unstable loop gain, according to Eq. (9.75). To avoid disturbing the dc bias conditions, it may be necessary to bypass R_{ext} with inductor L_{ext}. If the inductance value is sufficiently large, then it will not influence the stability of the modified system.

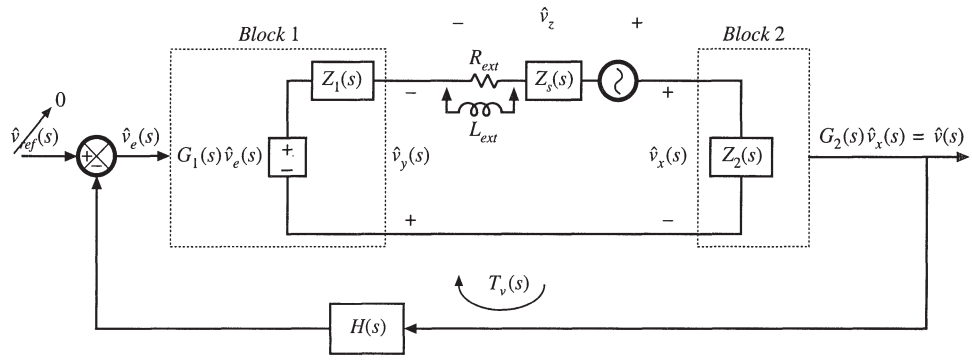


Fig. 9.40 Measurement of an unstable loop gain by voltage injection.

9.7 SUMMARY OF KEY POINTS

1. Negative feedback causes the system output to closely follow the reference input, according to the gain $1/H(s)$. The influence on the output of disturbances and variation of gains in the forward path is reduced.

2. The loop gain $T(s)$ is equal to the products of the gains in the forward and feedback paths. The loop gain is a measure of how well the feedback system works: a large loop gain leads to better regulation of the output. The crossover frequency f_c is the frequency at which the loop gain T has unity magnitude, and is a measure of the bandwidth of the control system.

3. The introduction of feedback causes the transfer functions from disturbances to the output to be multiplied by the factor $1/(1 + T(s))$. At frequencies where T is large in magnitude (i.e., below the crossover frequency), this factor is approximately equal to $1/T(s)$. Hence, the influence of low-frequency disturbances on the output is reduced by a factor of $1/T(s)$. At frequencies where T is small in magnitude (i.e., above the crossover frequency), the factor is approximately equal to 1. The feedback loop then has no effect. Closed-loop disturbance-to-output transfer functions, such as the line-to-output transfer function or the output impedance, can easily be constructed using the algebra-on-the-graph method.

4. Stability can be assessed using the phase margin test. The phase of T is evaluated at the crossover frequency, and the stability of the important closed-loop quantities $T/(1 + T)$ and $1/(1 + T)$ is then deduced. Inadequate phase margin leads to ringing and overshoot in the system transient response, and peaking in the closed-loop transfer functions.

5. Compensators are added in the forward paths of feedback loops to shape the loop gain, such that desired performance is obtained. Lead compensators, or *PD* controllers, are added to improve the phase margin and extend the control system bandwidth. *PI* controllers are used to increase the low-frequency loop gain, to improve the rejection of low-frequency disturbances and reduce the steady-state error.

6. Loop gains can be experimentally measured by use of voltage or current injection. This approach avoids the problem of establishing the correct quiescent operating conditions in the system, a common difficulty in systems having a large dc loop gain. An injection point must be found where interstage loading is not significant. Unstable loop gains can also be measured.

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PROBLEMS

9.1 Derive both forms of Eq. (9.25).

9.2 The flyback converter system of Fig. 9.41 contains a feedback loop for regulation of the main output voltage v_1. An auxiliary output produces voltage v_2. The dc input voltage v_g lies in the range $280\ \text{V} \le v_g \le 380\ \text{V}$. The compensator network has transfer function

$$G_c(s) = G_{c\infty}\left(1 + \frac{\omega_1}{s}\right)$$

where $G_{c\infty} = 0.05$, and $f_1 = \omega_1/2\pi = 400$ Hz.

(a) What is the steady-state value of the error voltage $v_e(t)$? Explain your reasoning.

(b) Determine the steady-state value of the main output voltage v_1.

(c) Estimate the steady-state value of the auxiliary output voltage v_2.

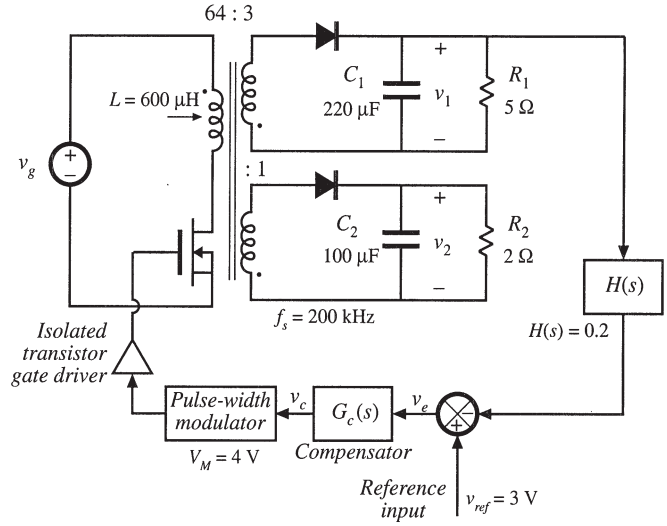


Fig. 9.41 Flyback converter system of Problem 9.2.

9.3 In the boost converter system of Fig. 9.42, all elements are ideal. The compensator has gain $G_c(s) = 250/s$.

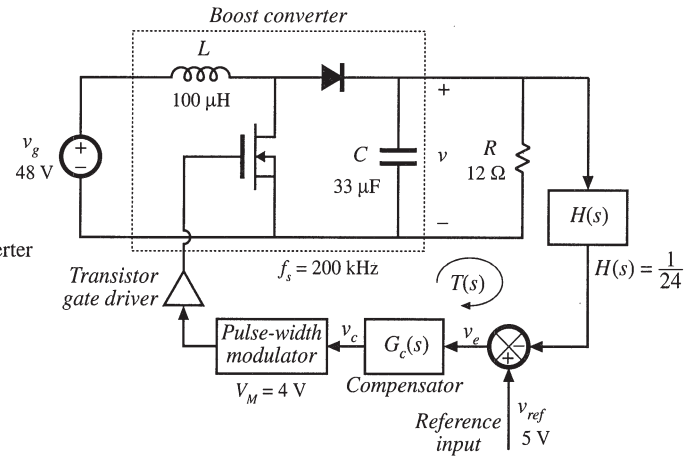


Fig. 9.42 Boost converter system of Problem 9.3.

(a) Construct the Bode plot of the loop gain $T(s)$ magnitude and phase. Label values of all corner frequencies and Q-factors, as appropriate.

(b) Determine the crossover frequency and phase margin.

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(c) Construct the Bode diagram of the magnitude of $1/(1 + T)$, using the algebra-on-the-graph method. Label values of all corner frequencies and Q-factors, as appropriate.

(d) Construct the Bode diagram of the magnitude of the closed-loop line-to-output transfer function. Label values of all corner frequencies and Q-factors, as appropriate.

9.4 A certain inverter system has the following loop gain

$$T(s) = T_0 \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)\left(1 + \frac{s}{\omega_3}\right)}$$

and the following open-loop line-to-output transfer function

$$G_{vg}(s) = G_{g0} \frac{1}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_3}\right)}$$

where

$T_0 = 100$ $\omega_1 = 500$ rad/sec

$\omega_2 = 1000$ rad/sec $\omega_3 = 24000$ rad/sec

$\omega_z = 4000$ rad/sec $G_{g0} = 0.5$

The gain of the feedback connection is $H(s) = 0.1$.

(a) Sketch the magnitude and phase asymptotes of the loop gain $T(s)$. Determine numerical values of the crossover frequency in Hz and phase margin in degrees.

(b) Construct the magnitude asymptotes of the closed-loop line-to-output transfer function. Label important features.

(c) Construct the magnitude asymptotes of the closed-loop transfer function from the reference voltage to the output voltage. Label important features.

9.5 The forward converter system of Fig. 9.43(a) is constructed with the element values shown. The quiescent value of the input voltage is $V_g = 380$ V. The transformer has turns ratio $n_1/n_3 = 4.5$. The duty cycle produced by the pulse-width modulator is restricted to the range $0 \le d(t) \le 0.5$. Within this range, $d(t)$ follows the control voltage $v_c(t)$ according to

$$d(t) = \frac{1}{2} \frac{v_c(t)}{V_M}$$

with $V_M = 3$ V.

(a) Determine the quiescent values of: the duty cycle D, the output voltage V, and the control voltage V_c.

(b) The op-amp circuit and feedback connection can be modeled using the block diagram illustrated in Fig. 9.43(b), with $H(s) = R_2/(R_1 + R_2)$. Determine the transfer functions $G_c(s)$ and $G_r(s)$.

(c) Sketch a block diagram which models the small-signal ac variations of the complete system, and determine the transfer function of each block. *Hint*: the transformer magnetizing inductance has negligible influence on the converter dynamics, and can be ignored. The small-signal models of the forward and buck converters are similar.

(d) Construct a Bode plot of the loop gain magnitude and phase. What is the crossover frequency? What is the phase margin?

(e) Construct the Bode plot of the closed-loop line-to-output transfer function magnitude

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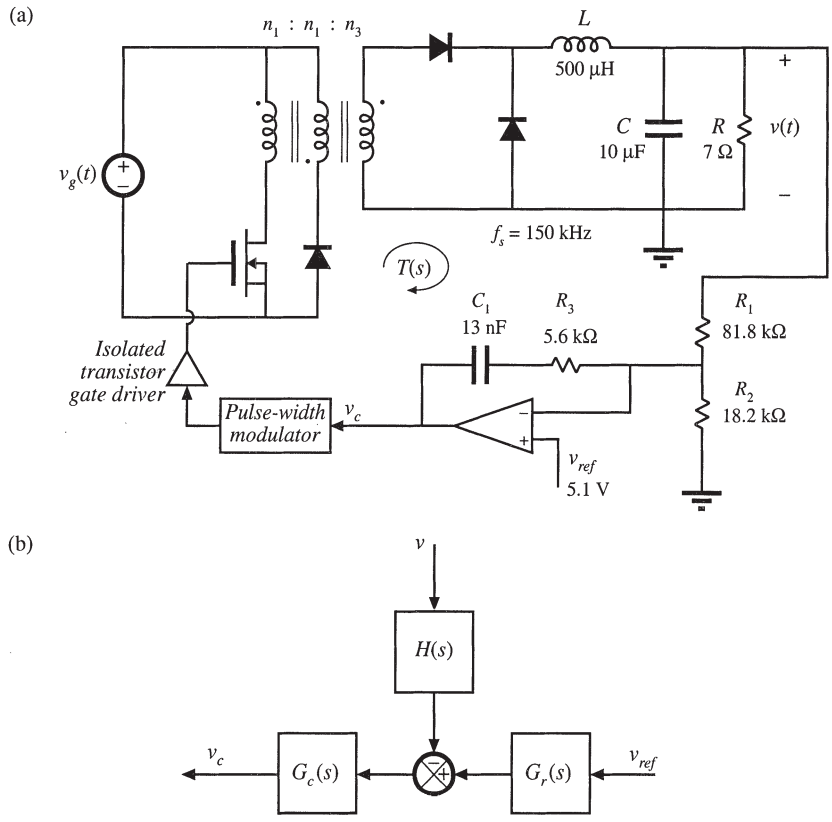


Fig. 9.43 Forward converter system of Problem 9.5: (a) system diagram, (b) modeling the op amp circuit using a block diagram.

$$\left\| \frac{\hat{v}}{\hat{v}_g} \right\|$$

Label important features. What is the gain at 120 Hz? At what frequency do disturbances in v_g have the greatest influence on the output voltage?

9.6 In the voltage regulator system of Fig. 9.43, described in Problem 9.5, the input voltage $v_g(t)$ contains a 120 Hz variation of peak amplitude 10 V.

(a) What is the amplitude of the resulting 120 Hz variation in $v(t)$?

(b) Modify the compensator network such that the 120 Hz output voltage variation has peak amplitude less than 25 mV. Your modification should leave the dc output voltage unchanged, and should result in a crossover frequency no greater than 10 kHz.

9.7 Design of a boost converter with current feedback and a *PI* compensator. In some applications, it is desired to control the converter input terminal current waveform. The boost converter system of Fig. 9.44 contains a feedback loop which causes the converter input current $i_g(t)$ to be proportional to a reference voltage $v_{ref}(t)$. The feedback connection is a current sense circuit having gain $H(s) = 0.2$ volts per ampere. A conventional pulse width modulator circuit (Fig. 7.63) is employed, having a sawtooth wave-

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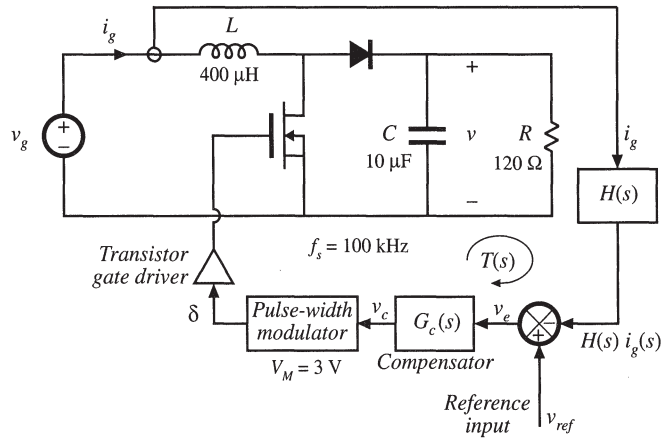


Fig. 9.44 Boost converter system with current feedback, Problem 9.7.

form with peak-peak amplitude of V_M = 3 V. The quiescent values of the inputs are: V_g = 120 V, V_{ref} = 2 V. All elements are ideal.

(a) Determine the quiescent values D, V, and I_g.

(b) Determine the small-signal transfer function

$$G_{id}(s) = \frac{\hat{i}_g(s)}{\hat{d}(s)}$$

(c) Sketch the magnitude and phase asymptotes of the uncompensated ($G_c(s) = 1$) loop gain.

(d) It is desired to obtain a loop gain magnitude of at least 35 dB at 120 Hz, while maintaining a phase margin of at least 72°. The crossover frequency should be no greater than $f_s/10$ = 10 kHz. Design a *PI* compensator that accomplishes this. Sketch the magnitude and phase asymptotes of the resulting loop gain, and label important features.

(e) For your design of part (d), sketch the magnitude of the closed-loop transfer function

$$\frac{\hat{i}_g(s)}{\hat{v}_{ref}(s)}$$

Label important features.

9.8 Design of a buck regulator to meet closed-loop output impedance specifications. The buck converter with control system illustrated inFig. 9.45 is to be designed to meet the following specifications. The closed-loop output impedance should be less than 0.2 Ω over the entire frequency range 0 to 20 kHz. To ensure that the transient response is well-behaved, the poles of the closed-loop transfer functions, in the vicinity of the crossover frequency, should have Q-factors no greater than unity. The quiescent load current I_{LOAD} can vary from 5 A to 50 A, and the above specifications must be met for every value of I_{LOAD} in this range. For simplicity, you may assume that the input voltage vg does not vary. The loop gain crossover frequency f_c may be chosen to be no greater than $f_s/10$, or 10 kHz. You may also assume that all elements are ideal. The pulse-width modulator circuit obeys Eq. (7.173).

(a) What is the intended dc output voltage V? Over what range does the effective load resistance R_{LOAD} vary?

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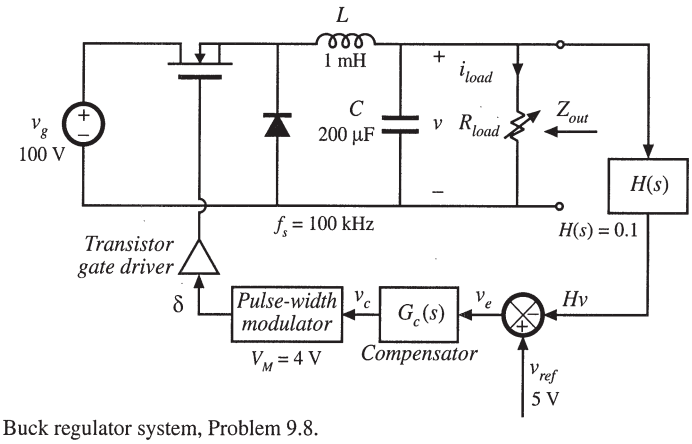


Fig. 9.45 Buck regulator system, Problem 9.8.

(b) Construct the magnitude asymptotes of the open-loop output impedance $Z_{out}(s)$. Over what range of frequencies is the output impedance specification not met? Hence, deduce how large the minimum loop gain $T(s)$ must be in magnitude, such that the closed-loop output impedance meets the specification. Choose a suitable crossover frequency f_c.

(c) Design a compensator network $G_c(s)$ such that all specifications are met. Additionally, the dc loop gain $T(s)$ should be at least 20 dB. Specify the following:

(i) Your choice for the transfer function $G_c(s)$

(ii) The worst-case closed-loop Q

(iii) Bode plots of the loop gain $T(s)$ and the closed-loop output impedance, for load currents of 5 A and 50 A. What effect does variation of R_{LOAD} have on the closed-loop behavior of your design?

(d) Design a circuit using resistors, capacitors, and an op amp to realize your compensator transfer function $G_c(s)$.

9.9 Design of a buck-boost voltage regulator. The buck-boost converter of Fig. 9.46 operates in the continuous conduction mode, with the element values shown. The nominal input voltage is V_g = 48 V, and it is desired to regulate the output voltage at –15 V. Design the best compensator that you can, which has high crossover frequency (but no greater than 10% of the switching frequency), large loop gain over the bandwidth of the feedback loop, and phase margin of at least 52°.

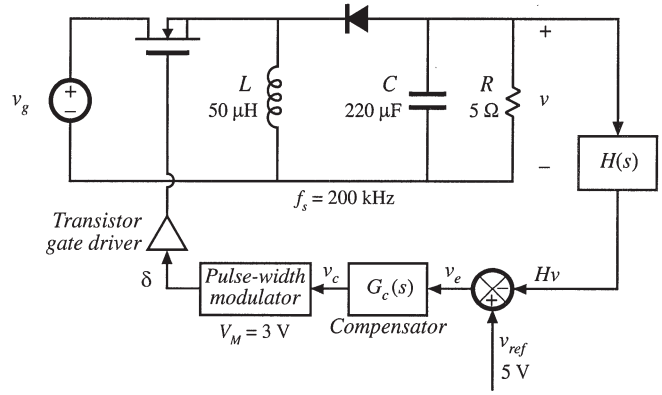


Fig. 9.46 Buck–boost voltage regulator system, Problem 9.9.

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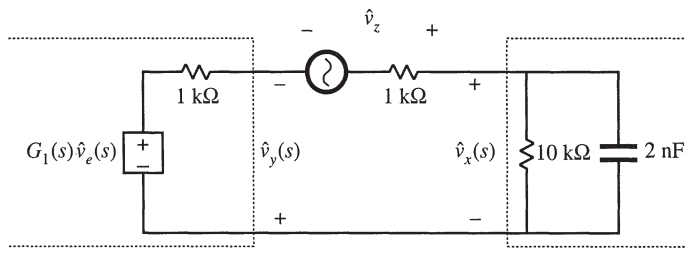
(a) Specify the required value of H. Sketch Bode plots of the uncompensated loop gain magnitude and phase, as well as the magnitude and phase of your proposed compensator transfer function $G_c(s)$. Label the important features of your plots.

(b) Construct Bode diagrams of the magnitude and phase of your compensated loop gain $T(s)$, and also of the magnitude of the quantities $T/(1+T)$ and $1/(1+T)$.

(c) Discuss your design. What prevents you from further increasing the crossover frequency? How large is the loop gain at 120 Hz? Can you obtain more loop gain at 120 Hz?

9.10 The loop gain of a certain feedback system is measured, using voltage injection at a point in the forward path of the loop as illustrated in Fig. 9.47(a). The data in Fig. 9.47(b) is obtained. What is $T(s)$? Specify $T(s)$ in factored pole-zero form, and give numerical values for all important features. Over what range of frequencies does the measurement give valid results?

(a)



(b)

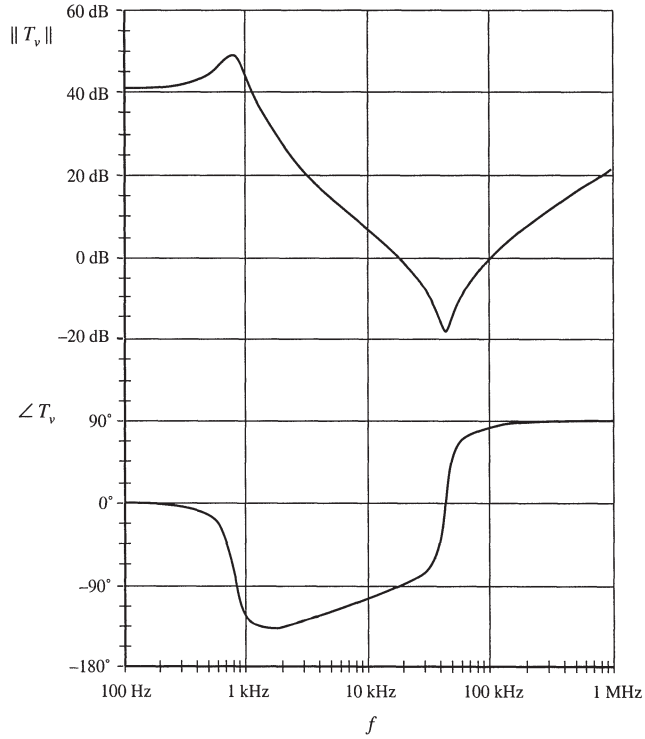


Fig. 9.47 Experimental measurement of loop gain, Problem 9.10: (a) measurement via voltage injection, (b) measured data.

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10
Input Filter Design

10.1 INTRODUCTION

10.1.1 Conducted EMI

It is nearly always required that a filter be added at the power input of a switching converter. By attenuating the switching harmonics that are present in the converter input current waveform, the input filter allows compliance with regulations that limit *conducted electromagnetic interference* (EMI). The input filter can also protect the converter and its load from transients that appear in the input voltage $v_g(t)$, thereby improving the system reliability.

A simple buck converter example is illustrated in Fig. 10.1. The converter injects the pulsating current $i_g(t)$ of Fig. 10.1(b) into the power source $v_g(t)$. The Fourier series of $i_g(t)$ contains harmonics at multiples of the switching frequency f_s, as follows:

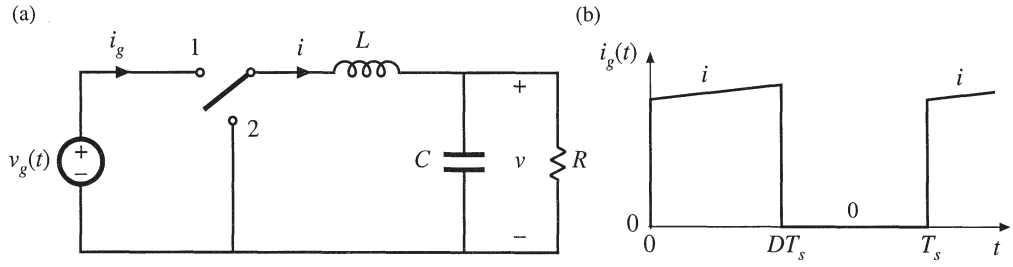


Fig. 10.1 Buck converter example: (a) circuit of power stage, (b) pulsating input current waveform.

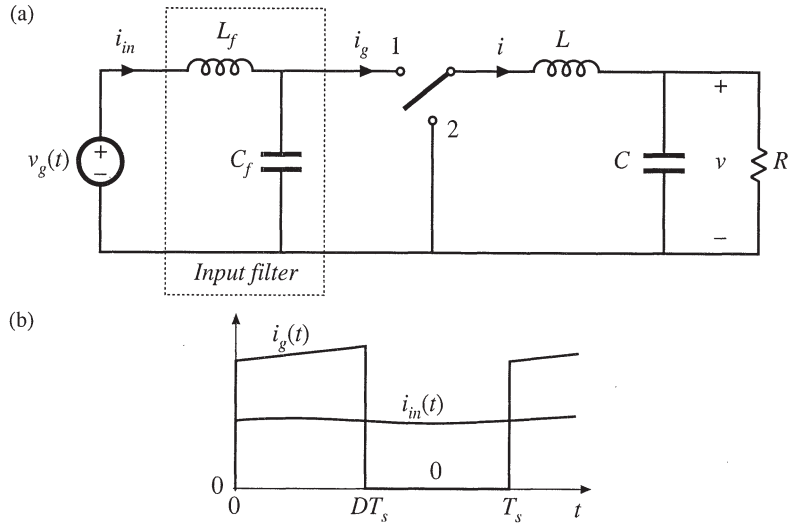


Fig. 10.2 Addition of a simple *L-C* low-pass filter to the power input terminals of the buck converter: (a) circuit, (b) input current waveforms.

$$i_g(t) = DI + \sum_{k=1}^{\infty} \frac{2I}{k\pi} \sin\left(k\pi D\right) \cos\left(k\omega t\right) \tag{10.1}$$

In practice, the magnitudes of the higher-order harmonics can also be significantly affected by the current spike caused by diode reverse recovery, and also by the finite slopes of the switching transitions. The large high-frequency current harmonics of $i_g(t)$ can interfere with television and radio reception, and can disrupt the operation of nearby electronic equipment. In consequence, regulations and standards exist that limit the amplitudes of the harmonic currents injected by a switching converter into its power source [1-8]. As an example, if the dc inductor current i of Fig. 10.2 has a magnitude of several Amperes, then the fundamental component ($n = 1$) has an rms amplitude in the vicinity of one Ampere. Regulations may require attenuation of this current to a value typically in the range 10 μA to 100 μA.

To meet limits on conducted EMI, it is necessary to add an input filter to the converter. Figure 10.2 illustrates a simple single-section *L-C* low-pass filter, added to the input of the converter of Fig. 10.1. This filter attenuates the current harmonics produced by the switching converter, and thereby smooths the current waveform drawn from the power source. If the filter has transfer function $H(s) = i_{in}/i_g$, then the input current Fourier series becomes

$$i_{in}(t) = H(0)DI + \sum_{k=1}^{\infty} \left\| H(kj\omega) \right\| \frac{2I}{k\pi} \sin\left(k\pi D\right) \cos\left(k\omega t + \angle H(kj\omega)\right) \tag{10.2}$$

In other words, the amplitude of each current harmonic at angular frequency $k\omega$ is attenuated by the filter transfer function at the harmonic frequency, $\| H(kj\omega) \|$. Typical requirements effectively limit the current harmonics to have amplitudes less than 100 μA, and hence input filters are often required to attenuate the current amplitudes by 80 dB or more.

To improve the reliability of the system, input filters are sometimes required to operate normally when transients or periodic disturbances are applied to the power input. Such *conducted susceptibility* specifications force the designer to damp the input filter resonances, so that input disturbances do not excite excessive currents or voltages within the filter or converter.

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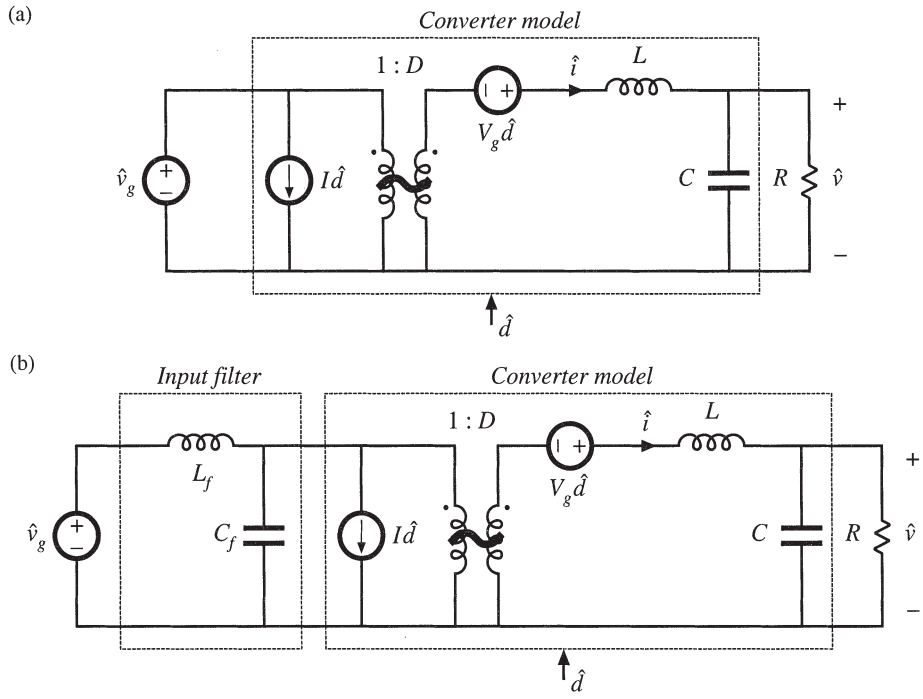


Fig. 10.3 Small-signal equivalent circuit models of the buck converter: (a) basic converter model, (b) with addition of input filter.

10.1.2 The Input Filter Design Problem

The situation faced by the design engineer is typically as follows. A switching regulator has been designed, which meets performance specifications. The regulator was properly designed as discussed in Chapter 9, using a small-signal model of the converter power stage such as the equivalent circuit of Fig. 10.3(a). In consequence, the transient response is well damped and sufficiently fast, with adequate phase margin at all expected operating points. The output impedance is sufficiently small over a wide frequency range. The line-to-output transfer function $G_{vg}(s)$, or *audiosusceptibility*, is sufficiently small, so that the output voltage remains regulated in spite of variations in $\hat{v}_g(t)$.

Having developed a good design that meets the above goals regarding dynamic response, the problem of conducted EMI is then addressed. A low-pass filter having attenuation sufficient to meet conducted EMI specifications is constructed and added to the converter input. A new problem then arises: the input filter changes the dynamics of the converter. The transient response is modified, and the control system may even become unstable. The output impedance may become large over some frequency range, possibly exhibiting resonances. The audiosusceptibility may be degraded.

The problem is that the input filter affects the dynamics of the converter, often in a manner that degrades regulator performance. For example, when a single-section *L-C* input filter is added to a buck converter as in Fig. 10.2(a), the small-signal equivalent circuit model is modified as shown in Fig. 10.3(b). The input filter elements affect all transfer functions of the converter, including the control-to-

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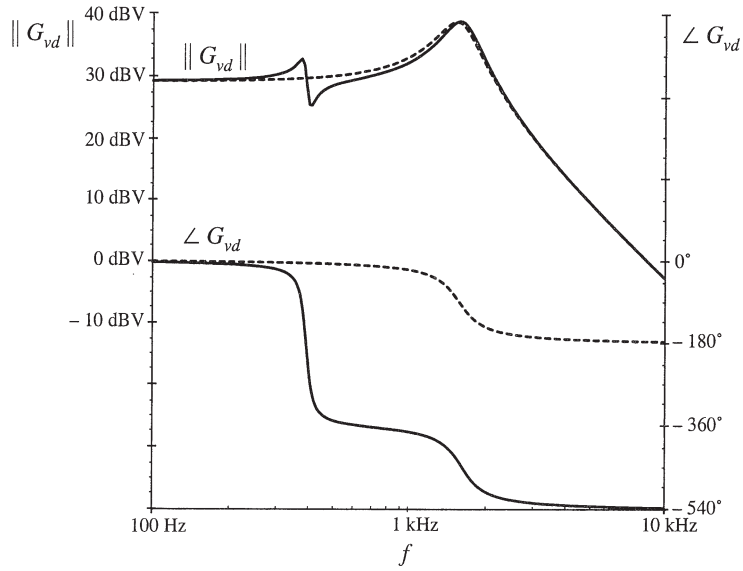


Fig. 10.4 Control-to-output transfer functions predicted by the equivalent circuit models of Fig. 10.3. *Dashed lines:* without input filter [Fig. 10.3(a)]. *Solid lines:* with input filter [Fig. 10.3(b)].

output transfer function $G_{vd}(s)$, the line-to-output transfer function $G_{vg}(s)$, and the converter output impedance $Z_{out}(s)$. Moreover, the influence of the input filter on these transfer functions can be quite severe.

As an illustration, let's examine how the control-to-output transfer function $G_{vd}(s)$ of the buck converter of Fig. 10.1 is altered when a simple *L-C* input filter is added as in Fig. 10.2. For this example, the element values are chosen to be: $D = 0.5, L = 100\ \mu\text{H}, C = 100\ \mu\text{F}, R = 3\ \Omega, L_f = 330\ \mu\text{H}, C_f = 470\ \mu\text{F}$. Figure 10.4 contains the Bode plot of the magnitude and phase of the control-to-output transfer function $G_{vd}(s)$. The dashed lines are the magnitude and phase before the input filter was added, generated by solution of the model of Fig. 10.3(a). The complex poles of the converter output filter cause the phase to approach – 180° at high frequency. Usually, this is the model used to design the regulator feedback loop and to evaluate the phase margin (*see* Chapter 9). The solid lines of Fig. 10.4 show the magnitude and phase after addition of the input filter, generated by solution of the model of Fig. 10.3(b). The magnitude exhibits a "glitch" at the resonant frequency of the input filter, and an additional – 360° of phase shift is introduced into the phase. It can be shown that $G_{vd}(s)$ now contains an additional complex pole pair and a complex right half-plane zero pair, associated with the input filter dynamics. If the crossover frequency of the regulator feedback loop is near to or greater than the resonant frequency of the input filter, then the loop phase margin will become negative and instability will result. Such behavior is typical; consequently, input filters are notorious for destabilizing switching regulator systems.

This chapter shows how to mitigate the stability problem, by introducing damping into the input filter and by designing the input filter such that its output impedance is sufficiently small [9-21]. The result of these measures is that the effect of the input filter on the control-to-output transfer function becomes negligible, and hence the converter dynamics are much better behaved. Although analysis of the fourth-order system of Fig. 10.3(b) is potentially quite complex, the approach used here simplifies the problem through use of impedance inequalities involving the converter input impedance and the filter output impedance [9,10]. These inequalities are based on Middlebrook's extra element theorem of Appendix C. This approach allows the engineer to gain the insight needed to effectively design the input filter. Optimization of the damping networks of input filters, and design of multiple-section filters, is also discussed.

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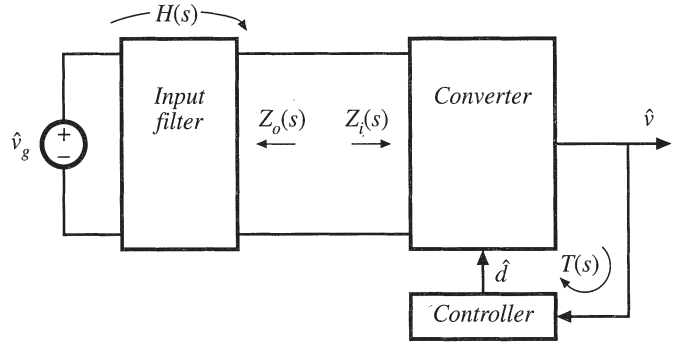


Fig. 10.5 Addition of an input filter to a switching voltage regulator system.

10.2 EFFECT OF AN INPUT FILTER ON CONVERTER TRANSFER FUNCTIONS

The control-to-output transfer function $G_{vd}(s)$ is defined as follows:

$$G_{vd}(s) = \left.\frac{\hat{v}(s)}{\hat{d}(s)}\right|_{\hat{v}_g(s)=0} \tag{10.3}$$

The control-to-output transfer functions of basic CCM converters with no input filters are listed in Section 8.2.2.

Addition of an input filter to a switching regulator leads to the system illustrated in Fig. 10.5. To determine the control-to-output transfer function in the presence of the input filter, we set $\hat{v}_g(s)$ to zero and solve for $\hat{v}(s)/\hat{d}(s)$ according to Eq. (10.3). The input filter can then be represented simply by its output impedance $Z_o(s)$ as illustrated in Fig. 10.6. Thus, the input filter can be treated as an extra element having impedance $Z_o(s)$. In Appendix C, Section C.4.3, Middlebrook's extra element theorem is employed to determine how addition of the input filter modifies the control-to-output transfer function. It is found that the modified control-to-output transfer function can be expressed as follows [9]:

$$G_{vd}(s) = \left(G_{vd}(s)\Big|_{Z_o(s)=0} \right) \frac{\left(1 + \frac{Z_o(s)}{Z_N(s)}\right)}{\left(1 + \frac{Z_o(s)}{Z_D(s)}\right)} \tag{10.4}$$

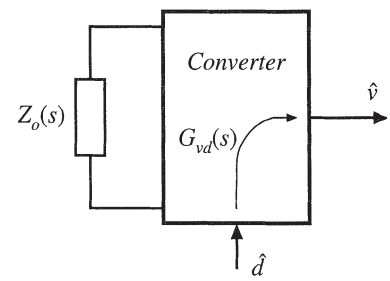


Fig. 10.6 Determination of the control-to-output transfer function $G_{vd}(s)$ for the system of Fig. 10.5.

Table 10.1 Input filter design criteria for basic converters

Converter	$Z_N(s)$	$Z_D(s)$	$Z_e(s)$
Buck	$-\frac{R}{D^2}$	$\frac{R}{D^2}\frac{\left(1+s\frac{L}{R}+s^2LC\right)}{\left(1+sRC\right)}$	$\frac{sL}{D^2}$
Boost	$-D'^2R\left(1-\frac{sL}{D'^2R}\right)$	$D'^2R\frac{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}{\left(1+sRC\right)}$	sL
Buck–boost	$-\frac{D'^2R}{D^2}\left(1-\frac{sDL}{D'^2R}\right)$	$\frac{D'^2R}{D^2}\frac{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}{\left(1+sRC\right)}$	$\frac{sL}{D^2}$

where

$$G_{vd}(s)\Big|_{Z_o(s)=0} \tag{10.5}$$

is the original control-to-output transfer function with no input filter. The quantity $Z_D(s)$ is equal to the converter input impedance $Z_i(s)$ under the condition that $\hat{d}(s)$ is equal to zero:

$$Z_D(s) = Z_i(s)\Big|_{\hat{d}(s)=0} \tag{10.6}$$

The quantity $Z_N(s)$ is equal to the converter input impedance $Z_i(s)$ under the condition that the feedback controller of Fig. 10.5 operates ideally; in other words, the controller varies $\hat{d}(s)$ as necessary to maintain $\hat{v}(s)$ equal to zero:

$$Z_N(s) = Z_i(s)\Big|_{\hat{v}(s)\xrightarrow[\text{null}]{}0} \tag{10.7}$$

In terms of the canonical circuit model parameters described in Section 7.5, $Z_N(s)$ can be shown to be

$$Z_N(s) = -\frac{e(s)}{j(s)} \tag{10.8}$$

Expressions for $Z_N(s)$ and $Z_D(s)$ for the basic buck, boost, and buck-boost converters are listed in Table 10.1.

10.2.1 Discussion

Equation (10.4) relates the power stage control-to-output transfer function $G_{vd}(s)$ to the output impedance $Z_o(s)$ of the input filter, and also to the quantities $Z_N(s)$ and $Z_D(s)$ measured at the power input port of the converter. The quantity $Z_D(s)$ coincides with the open-loop input impedance of the converter.

As described above, the quantity $Z_N(s)$ is equal to the input port impedance of the converter

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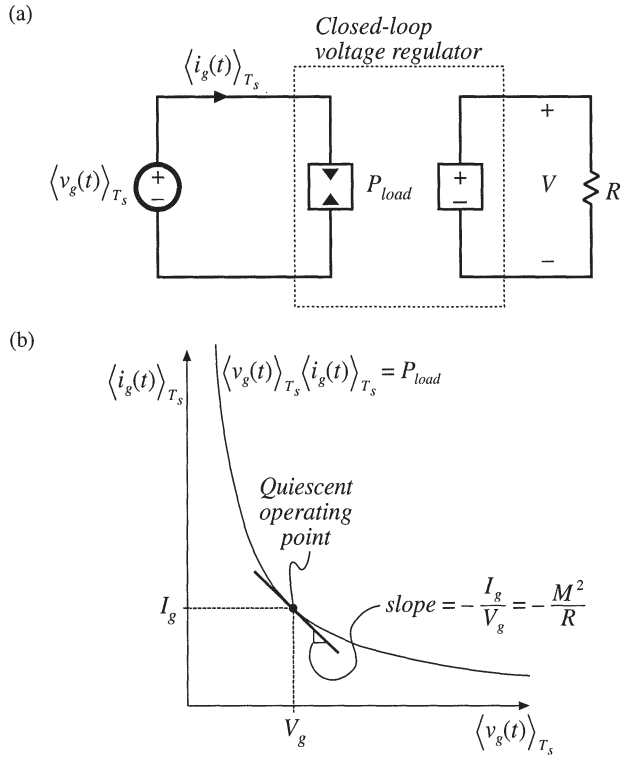


Fig. 10.7 Power input port characteristics of an ideal switching voltage regulator: (a) equivalent circuit model, including dependent power sink, (b) constant power characteristic of input port.

power stage, under the conditions that $\hat{d}(s)$ is varied as necessary to null $\hat{v}(s)$ to zero. This is, in fact, the function performed by an ideal controller: it varies the duty cycle as necessary to maintain zero error of the output voltage. Therefore, $Z_N(s)$ coincides with the impedance that would be measured at the converter power input terminals, if an ideal feedback loop perfectly regulated the converter output voltage. Of course, Eq. (10.4) is valid in general, regardless of whether a control system is present.

Figure 10.7 illustrates the large-signal behavior of a feedback loop that perfectly regulates the converter output voltage. Regardless of the applied input voltage $v_g(t)$, the output voltage is maintained equal to the desired value V. The load power is therefore constant, and equal to $P_{load} = V^2/R$. In the idealized case of a lossless converter, the power flowing into the converter input terminals will also be equal to P_{load}, regardless of the value of $v_g(t)$. Hence, the power input terminal of the converter obeys the equation

$$\langle v_g(t) \rangle_{T_s} \langle i_g(t) \rangle_{T_s} = P_{load} \tag{10.9}$$

This characteristic is illustrated in Fig. 10.7(b), and is represented in Fig. 10.7(a) by the dependent power sink symbol. The properties of power sources and power sinks are discussed in detail in Chapter 11.

Figure 10.7(b) also illustrates linearization of the constant input power characteristic, about a quiescent operating point. The resulting line has negative slope; therefore, the incremental (small signal) input resistance of the ideal voltage regulator is negative. For example, increasing the voltage $\langle v_g(t) \rangle_{T_s}$

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causes the current $\langle i_g(t) \rangle_{T_s}$ to decrease, such that the power remains constant. This incremental resistance has the value [9,14]:

$$-\frac{R}{M^2} \tag{10.10}$$

where R is the output load resistance, and M is the conversion ratio V/V_g. For each of the converters listed in Table 10.1, the dc asymptote of $Z_N(s)$ coincides with the negative incremental resistance given by the equation above.

Practical control systems exhibit a limited bandwidth, determined by the crossover frequency f_c of the feedback loop. Therefore, we would expect the closed-loop regulator input impedance to be approximately equal to $Z_N(s)$ at low frequency ($f \ll f_c$) where the loop gain is large and the regulator works well. At frequencies above the bandwidth of the regulator ($f \gg f_c$), we expect the converter input impedance to follow the open-loop value $Z_D(s)$. For closed-loop conditions, it can be shown that the regulator input impedance $Z_i(s)$ is, in fact, described by the following equation:

$$\frac{1}{Z_i(s)} = \frac{1}{Z_N(s)} \frac{T(s)}{1+T(s)} + \frac{1}{Z_D(s)} \frac{1}{1+T(s)} \tag{10.11}$$

where $T(s)$ is the controller loop gain. Thus, the regulator input impedance follows the negative resistance of $Z_N(s)$ at low frequency where the magnitude of the loop gain is large [and hence $T/(1+T) \approx 1$, $1/(1+T) \approx 0$], and reverts to the (positive) open-loop impedance $Z_D(s)$ at high frequency where $\| T \|$ is small [i.e., where $T/(1+T) \approx 0$, $1/(1+T) \approx 1$].

When an undamped or lightly damped input filter is connected to the regulator input port, the input filter can interact with the negative resistance characteristic of Z_N to form a *negative resistance oscillator*. This further explains why addition of an input filter tends to lead to instabilities.

10.2.2 Impedance Inequalities

Equation (10.4) reveals that addition of the input filter causes the control-to-output transfer function to be modified by the factor

$$\frac{\left(1 + \dfrac{Z_o(s)}{Z_N(s)}\right)}{\left(1 + \dfrac{Z_o(s)}{Z_D(s)}\right)} \tag{10.12}$$

called the *correction factor*. When the following inequalities are satisfied,

$$\begin{aligned} \| Z_o \| &\ll \| Z_N \|, \text{ and} \\ \| Z_o \| &\ll \| Z_D \| \end{aligned} \tag{10.13}$$

then the correction factor has a magnitude of approximately unity, and the input filter does not substantially alter the control-to-output transfer function [9,10]. These inequalities limit the maximum allowable output impedance of the input filter, and constitute useful filter design criteria. One can sketch the Bode plots of $\| Z_N(j\omega) \|$ and $\| Z_D(j\omega) \|$, and compare with the Bode plot of $\| Z_o(j\omega) \|$. This allows the engineer to gain the insight necessary to design an input filter that satisfies Eq. (10.13).

A similar analysis shows that the converter output impedance is not substantially affected by the input filter when the following inequalities are satisfied:

$$\begin{aligned} \| Z_o \| &\ll \| Z_e \|, \text{ and} \\ \| Z_o \| &\ll \| Z_D \| \end{aligned} \tag{10.14}$$

where $Z_D(s)$ is again as given in Table 10.1. The quantity $Z_e(s)$ is equal to the converter input impedance $Z_i(s)$ under the conditions that the converter output is shorted:

$$Z_e = Z_i \Big|_{\hat{v}=0} \tag{10.15}$$

Expressions for $Z_e(s)$ for basic converters are also listed in Table 10.1.

Similar impedance inequalities can be derived for the case of current-programmed converters [12,13], or converters operating in the discontinuous conduction mode. In [12], impedance inequalities nearly identical to the above equations were shown to guarantee that the input filter does not degrade transient response and stability in the current-programmed case. Feedforward of the converter input voltage was suggested in [16].

10.3 BUCK CONVERTER EXAMPLE

Let us again consider the example of a simple buck converter with *L-C* input filter, as illustrated in Fig. 10.8(a). Upon replacing the converter with its small-signal model, we obtain the equivalent circuit of Fig. 10.8(b). Let's evaluate Eq. (10.4) for this example, to find how the input filter modifies the control-to-output transfer function of the converter.

10.3.1 Effect of Undamped Input Filter

The quantities $Z_N(s)$ and $Z_D(s)$ can be read from Table 10.1, or can be derived using Eqs. (10.6) and (10.7) as further described in Appendix C. The quantity $Z_D(s)$ is given by Eq. (10.6). Upon setting $\hat{d}(s)$ to zero, the converter small signal model reduces to the circuit of Fig. 10.9(a). It can be seen that $Z_D(s)$ is equal to the input impedance of the *R-L-C* filter, divided by the square of the turns ratio:

$$Z_D(s) = \frac{1}{D^2}\left(sL + R \| \frac{1}{sC}\right) \tag{10.16}$$

Construction of asymptotes for this impedance is treated in Section 8.4, with the results for the numerical values of this example given in Fig. 10.10. The load resistance dominates the impedance at low frequency, leading to a dc asymptote of $R/D^2 = 12\ \Omega$. For the high-Q case shown, $\| Z_D(j\omega) \|$ follows the output capacitor asymptote, reflected through the square of the effective turns ratio, at intermediate frequencies. A series resonance occurs at the output filter resonant frequency f_0, given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{10.17}$$

For the element values listed in Fig. 10.8(a), the resonant frequency is $f_0 = 1.6$ kHz. The values of the asymptotes at the resonant frequency f_0 are given by the characteristic impedance R_0, referred to the

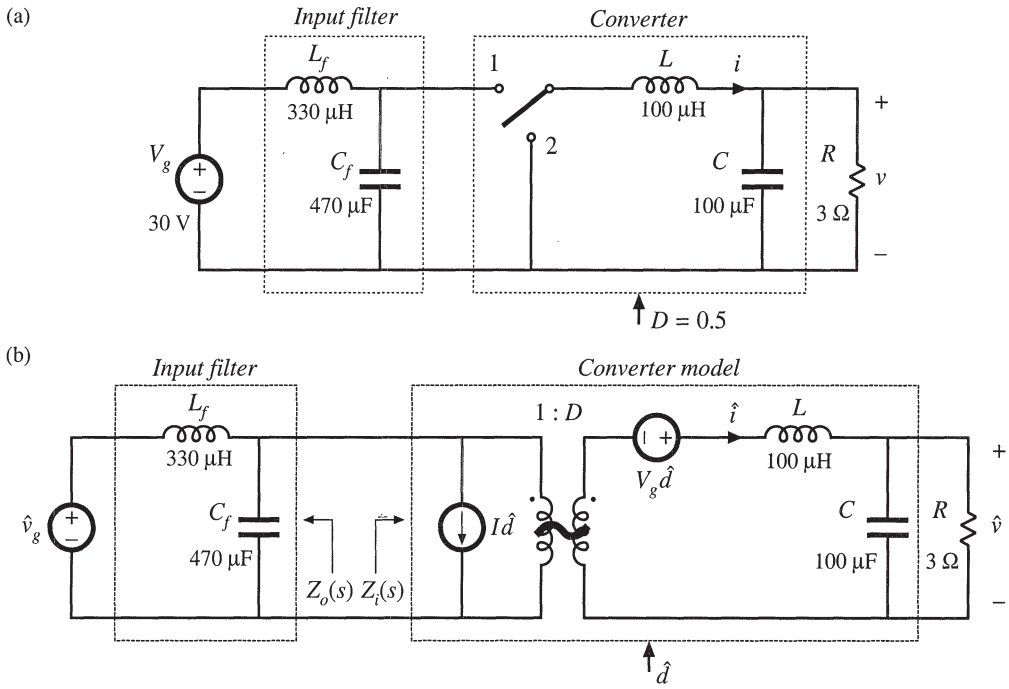


Fig. 10.8 Buck converter example: (a) converter circuit, (b) small-signal model.

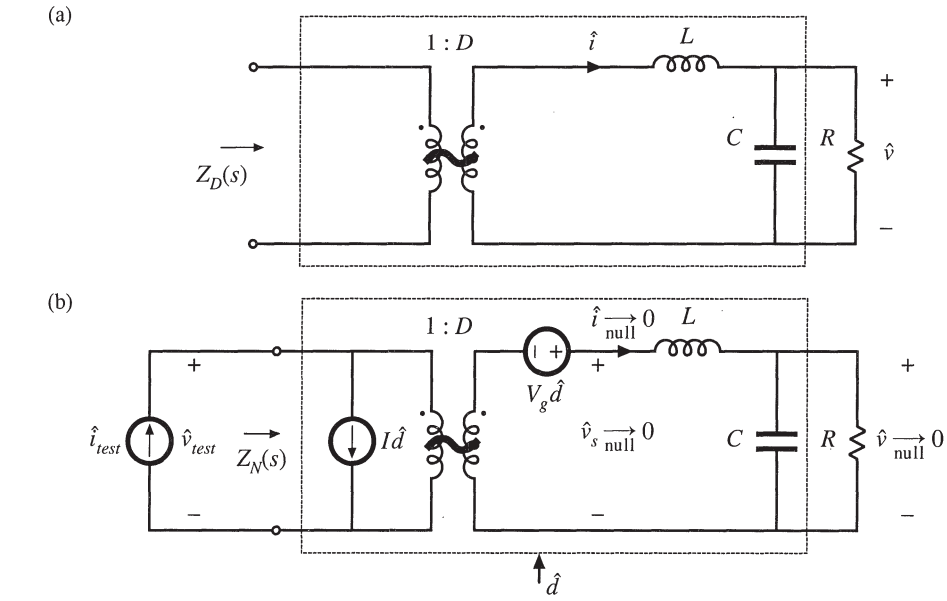


Fig. 10.9 Determination of the quantities $Z_N(s)$ and $Z_D(s)$ for the circuit of Fig. 10.8(b): (a) determination of $Z_D(s)$, (b) determination of $Z_N(s)$.

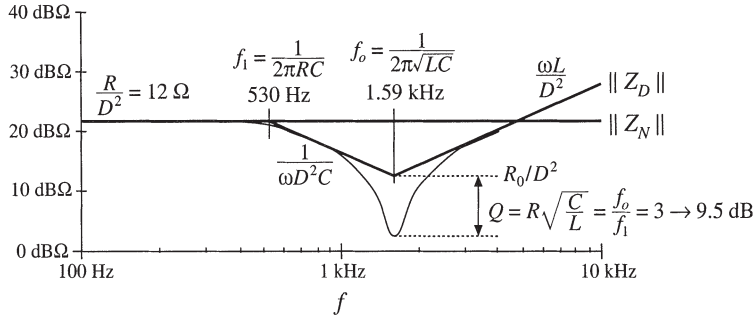


Fig. 10.10 Construction of $\| Z_N(j\omega) \|$ and $\| Z_D(j\omega) \|$, buck converter example.

transformer primary:

$$\frac{R_0}{D^2} = \frac{1}{D^2}\sqrt{\frac{L}{C}} \tag{10.18}$$

For the element values given in Fig. 10.8(a), this expression is equal to 4 Ω. The Q-factor is given by

$$Q = \frac{R}{R_0} = R\sqrt{\frac{C}{L}} \tag{10.19}$$

This expression yields a numerical value of $Q = 3$. The value of $\| Z_D(j\omega) \|$ at the resonant frequency 1.6 kHz is therefore equal to (4 Ω)/(3) = 1.33 Ω. At high frequency, $\| Z_D(j\omega) \|$ follows the reflected inductor asymptote.

The quantity $Z_N(s)$ is given by Eq. (10.7). This impedance is equal to the converter input impedance $Z_i(s)$, under the conditions that $\hat{d}(s)$ is varied to maintain the output voltage $\hat{v}(s)$ at zero. Figure 10.9(b) illustrates the derivation of an expression for $Z_N(s)$. A test current source $\hat{i}_{test}(s)$ is injected at the converter input port. The impedance $Z_N(s)$ can be viewed as the transfer function from $\hat{i}_{test}(s)$ to $\hat{v}_{test}(s)$:

$$Z_N(s) = \left.\frac{\hat{v}_{test}(s)}{\hat{i}_{test}(s)}\right|_{\hat{v} \xrightarrow[\text{null}]{} 0} \tag{10.20}$$

The null condition $\hat{v}(s) \xrightarrow[\text{null}]{} 0$ greatly simplifies analysis of the circuit of Fig. 10.9(b). Since the voltage $\hat{v}(s)$ is zero, the currents through the capacitor and load impedances are also zero. This further implies that the inductor current $\hat{i}(s)$ and transformer winding currents are zero, and hence the voltage across the inductor is also zero. Finally, the voltage $\hat{v}_s(s)$, equal to the output voltage plus the inductor voltage, is zero.

Since the currents in the windings of the transformer model are zero, the current $i_{test}(s)$ is equal to the independent source current $I\hat{d}(s)$:

$$\hat{i}_{test}(s) = I\hat{d}(s) \tag{10.21}$$

Because $\hat{v}_s(s)$ is equal to zero, the voltage applied to the secondary of the transformer model is equal to the independent source voltage $-V_g\hat{d}(s)$. Upon dividing by the turns ratio D, we obtain $\hat{v}_{test}(s)$:

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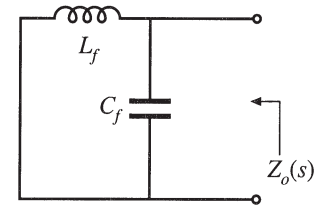


Fig. 10.11 Determination of the filter output impedance $Z_o(s)$.

$$\hat{v}_{test}(s) = -\frac{V_g \hat{d}(s)}{D} \tag{10.22}$$

Insertion of Eqs. (10.21) and (10.22) into Eq. (10.20) leads to the following result:

$$Z_N(s) = \frac{\left(-\frac{V_g \hat{d}(s)}{D}\right)}{\left(I\hat{d}(s)\right)} = -\frac{R}{D^2} \tag{10.23}$$

The steady-state relationship $I = DV_g/R$ has been used to simplify the above result. This equation coincides with the expression listed in Table 10.1. The Bode diagram of $\| Z_N(j\omega) \|$ is constructed in Fig. 10.10; this plot coincides with the dc asymptote of $\| Z_D(j\omega) \|$.

Next, let us construct the Bode diagram of the filter output impedance $Z_o(s)$. When the independent source $\hat{v}_g(s)$ is set to zero, the input filter network reduces to the circuit of Fig. 10.11. It can be seen that $Z_o(s)$ is given by the parallel combination of the inductor L_f and the capacitor C_f:

$$Z_o(s) = sL_f \| \frac{1}{sC_f} \tag{10.24}$$

Construction of the Bode diagram of this parallel resonant circuit is discussed in Section 8.3.4. As illustrated in Fig. 10.12, the magnitude $\| Z_o(j\omega) \|$ is dominated by the inductor impedance at low frequency, and by the capacitor impedance at high frequency. The inductor and capacitor asymptotes intersect at the filter resonant frequency:

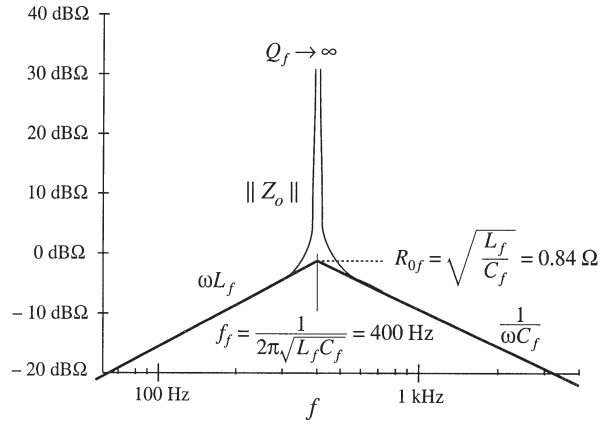


Fig. 10.12 Magnitude plot of the output impedance of the input filter of Fig. 10.11. Since the filter is not damped, the Q-factor is very large.

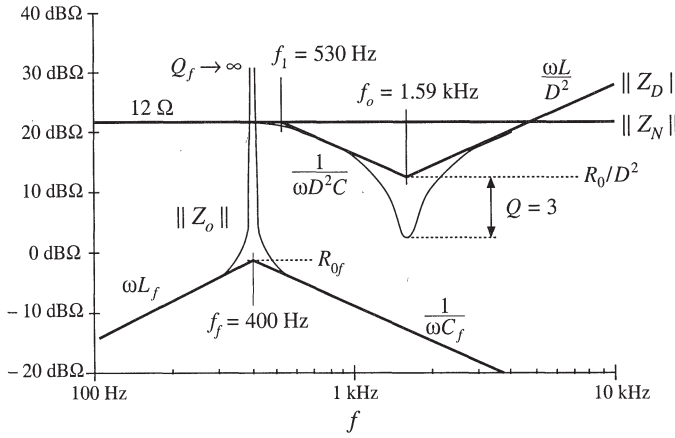


Fig. 10.13 Impedance design criteria $\| Z_N(j\omega) \|$ and $\| Z_D(j\omega) \|$ from Fig. 10.10, with the filter output impedance $\| Z_o(j\omega) \|$ of Fig. 10.12 superimposed. The design criteria of Eq. (10.13) are not satisfied at the input filter resonance.

$$f_f = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{10.25}$$

For the given values, the input filter resonant frequency is f_f = 400 Hz. This filter has characteristic impedance

$$R_{0f} = \sqrt{\frac{L_f}{C_f}} \tag{10.26}$$

equal to 0.84 Ω. Since the input filter is undamped, its Q-factor is ideally infinite. In practice, parasitic elements such as inductor loss and capacitor equivalent series resistance limit the value of Q_f. Nonetheless, the impedance $\| Z_o(j\omega) \|$ is very large in the vicinity of the filter resonant frequency f_f.

The Bode plot of the filter output impedance $\| Z_o(j\omega) \|$ is overlaid on the $\| Z_N(j\omega) \|$ and $\| Z_D(j\omega) \|$ plots in Fig. 10.13, for the element values listed in Fig. 10.8(a). We can now determine whether the impedance inequalities (10.13) are satisfied. Note the design-oriented nature of Fig. 10.13: since analytical expressions are given for each impedance asymptote, the designer can easily adjust the component values to satisfy Eq. (10.13). For example, the values of L_f and C_f should be chosen to ensure that the asymptotes of $\| Z_o(j\omega) \|$ lie below the worst-case value of R/D^2, as well as the other asymptotes of $\| Z_D(j\omega) \|$.

It should also be apparent that it is a bad idea to choose the input and output filter resonant frequencies f_0 and f_f to be equal, because it would then be more difficult to satisfy the inequalities of Eq. (10.13). Instead, the resonant frequencies f_0 and f_f should be well separated in value.

Since the input filter is undamped, it is impossible to satisfy the impedance inequalities (10.13) in the vicinity of the input filter resonant frequency f_f. Regardless of the choice of element values, the input filter changes the control-to-output transfer function $G_{vd}(s)$ in the vicinity of frequency f_f. Figures 10.14 and 10.15 illustrate the resulting correction factor [Eq. (10.12)] and the modified control-to-output transfer function [Eq. (10.4)], respectively. At frequencies well below the input filter resonant frequency, impedance inequalities (10.13) are well satisfied. The correction factor tends to the value $1\angle 0°$, and the

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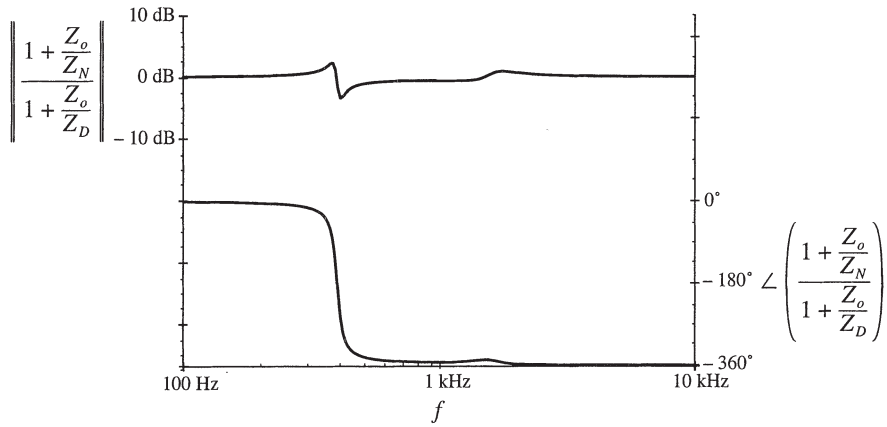


Fig. 10.14 Magnitude of the correction factor, Eq. (10.12), for the buck converter example of Fig. 10.8.

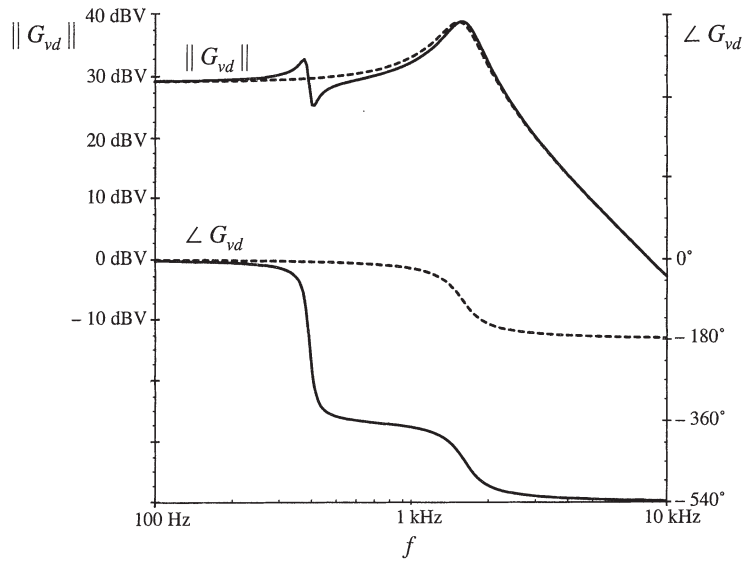


Fig. 10.15 Effect of the undamped input filter on the control-to-output transfer function of the buck converter example. *Dashed lines:* without input filter. *Solid lines:* with undamped input filter.

control-to-output transfer function $G_{vd}(s)$ is essentially unchanged. In the vicinity of the resonant frequency f_f, the correction factor contains a pair of complex poles, and also a pair of right half-plane complex zeroes. These cause a "glitch" in the magnitude plot of the correction factor, and they contribute 360° of lag to the phase of the correction factor. The glitch and its phase lag can be seen in the Bode plot of $G_{vd}(s)$. At high frequency, the correction factor tends to a value of approximately $1\angle -360°$; consequently, the high-frequency magnitude of G_{vd} is unchanged. However, when the – 360° contributed by the correction factor is added to the – 180° contributed at high frequency by the two poles of the original $G_{vd}(s)$, a high-frequency phase asymptote of – 540° is obtained. If the crossover frequency of the converter feedback loop is placed near to or greater than the input filter resonant frequency f_f, then a negative

phase margin is inevitable. This explains why addition of an input filter often leads to instabilities and oscillations in switching regulators.

10.3.2 Damping the Input Filter

Let's damp the resonance of the input filter, so that impedance inequalities (10.13) are satisfied at all frequencies.

One approach to damping the filter is to add resistor R_f in parallel with capacitor C_f as illustrated in Fig. 10.16(a). The output impedance of this network is identical to the parallel resonant impedance analyzed in Section 8.3.4. The maximum value of the output impedance occurs at the resonant frequency f_f, and is equal in value to the resistance R_f. Hence, to satisfy impedance inequalities (10.13), we should choose R_f to be much less than the $\| Z_N(j\omega) \|$ and $\| Z_D(j\omega) \|$ asymptotes. The condition $R_f \ll \| Z_N(j\omega) \|$ can be expressed as:

$$R_f \ll \frac{R}{D^2} \tag{10.27}$$

Unfortunately, this raises a new problem: the power dissipation in R_f. The dc input voltage V_g is applied across resistor R_f, and therefore R_f dissipates power equal to V_g^2/R_f. Equation (10.27) implies that this power loss is greater than the load power! Therefore, the circuit of Fig. 10.16(a) is not a practical solution.

One solution to the power loss problem is to place R_f in parallel with L_f as illustrated in Fig. 10.16(b). The value of R_f in Fig. 10.16(b) is also chosen according to Eq. (10.27). Since the dc voltage across inductor L_f is zero, there is now no dc power loss in resistor R_f. The problem with this circuit is that its transfer function contains a high-frequency zero. Addition of R_f degrades the slope of the high-frequency asymptote, from – 40 dB/decade to – 20 dB/decade. The circuit of Fig. 10.16(b) is effectively a single-pole R-C low-pass filter, with no attenuation provided by inductor L_f.

One practical solution is illustrated in Fig. 10.17 [10]. Dc blocking capacitor C_b is added in series with resistor R_f. Since no dc current can flow through resistor R_f, its dc power loss is eliminated. The value of C_b is chosen to be very large such that, at the filter resonant frequency f_f, the impedance of the R_f-C_b branch is dominated by resistor R_f. When C_b is sufficiently large, then the output impedance of this network reduces to the output impedances of the filters of Fig. 10.16. The impedance asymptotes for the case of large C_b are illustrated in Fig. 10.17(b).

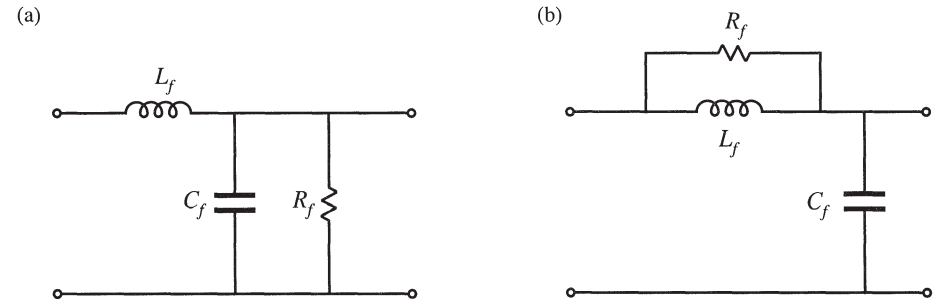


Fig. 10.16 Two attempts to damp the input filter: (a) addition of damping resistance R_f across C_f, (b) addition of damping resistance R_f in parallel with L_f.

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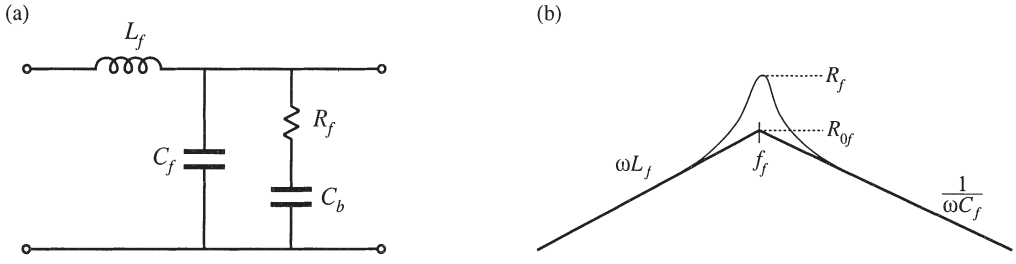


Fig. 10.17 A practical method to damping the input filter, including damping resistance R_f and dc blocking capacitor C_b: (a) circuit, (b) output impedance asymptotes.

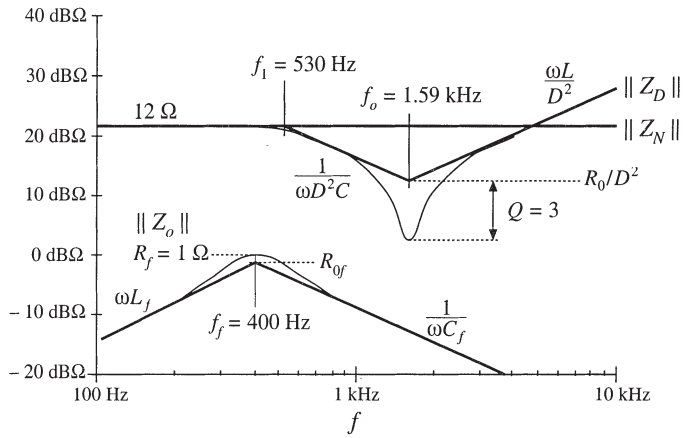


Fig. 10.18 Impedance design criteria $\| Z_N(j\omega) \|$ and $\| Z_D(j\omega) \|$ from Fig. 10.10, with the filter output impedance $\| Z_o(j\omega) \|$ of Fig. 10.17(b) superimposed. The design criteria of Eq. (10.13) are well satisfied.

The low-frequency asymptotes of $\| Z_N(j\omega) \|$ and $\| Z_D(j\omega) \|$ in Fig. 10.10 are equal to $R/D^2 = 12\ \Omega$. The choice $R_f = 1\ \Omega$ therefore satisfies impedance inequalities (10.13) very well. The choice $C_b = 4700\ \mu$F leads to $1/2\pi f_f C_b = 0.084\ \Omega$, which is much smaller than R_f. The resulting magnitude $\| Z_o(j\omega) \|$ is compared with $\| Z_N(j\omega) \|$ and $\| Z_D(j\omega) \|$ in Fig. 10.18. It can be seen that the chosen values of R_f and C_b lead to adequate damping, and impedance inequalities (10.13) are now well satisfied.

Figure 10.19 illustrates how addition of the damped input filter modifies the magnitude and phase of the control-to-output transfer function. There is now very little change in $G_{vd}(s)$, and we would expect that the performance of the converter feedback loop is unaffected by the input filter.

10.4 DESIGN OF A DAMPED INPUT FILTER

As illustrated by the example of the previous section, design of an input filter requires not only that the filter impedance asymptotes satisfy impedance inequalities, but also that the filter be adequately damped. Damping of the input filter is also necessary to prevent transients and disturbances in $v_g(t)$ from exciting filter resonances. Other design constraints include attaining the desired filter attenuation, and minimizing

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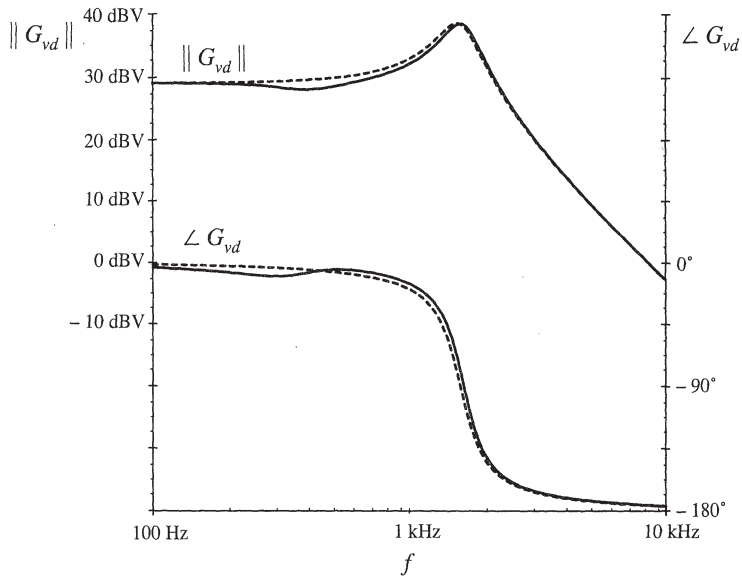


Fig. 10.19 Effect of the damped input filter on the control-to-output transfer function of the buck converter example. *Dashed lines:* without input filter. *Solid lines:* with damped input filter.

the size of the reactive elements. Although a large number of classical filter design techniques are well known, these techniques do not address the problems of limiting the maximum output impedance and damping filter resonances.

The value of the blocking capacitor C_b used to damp the input filter in Section 10.3.2 is ten times larger than the value of C_f, and hence its size and cost are of practical concern. Optimization of an input filter design therefore includes minimization of the size of the elements used in the damping networks.

Several practical approaches to damping the single-section L-C low-pass filter are illustrated in Fig. 10.20 [10,11,17]. Figure 10.20(a) contains the R_f-C_b damping branch considered in the previous section. In Fig. 10.20(b), the damping resistor R_f is placed in parallel with the filter inductor L_f, and a high-frequency blocking inductor L_b is placed in series with R_f. Inductor L_b causes the filter transfer function to roll off with a high-frequency slope of – 40 dB/decade. In Fig. 10.20(c), the damping resistor R_f is placed in series with the filter inductor L_f, and the dc current is bypassed by inductor L_b. In each case, it is desired to obtain a given amount of damping [i.e., to cause the peak value of the filter output impedance to be no greater than a given value that satisfies the impedance inequalities (10.13)], while minimizing the value of C_b or L_b. This problem can be formulated in an alternate but equivalent form: for a given choice of C_b or L_b, find the value of R_f that minimizes the peak output impedance [10]. The solutions to this optimization problem, for the three filter networks of Fig. 21, are summarized in this section. In each case, the quantities R_{0f} and f_f are defined by Eqs. (10.25) and (10.26).

Consider the filter of Fig. 10.20(b), with fixed values of L_f, C_f, and L_b. Figure 10.21 contains Bode plots of the filter output impedance $\| Z_o(j\omega) \|$ for several values of damping resistance R_f. For the limiting case $R_f = \infty$, the circuit reduces to the original undamped filter with infinite Q_f. In the limiting case $R_f = 0$, the filter is also undamped, but the resonant frequency is increased because L_b becomes connected in parallel with L_f. Between these two extremes, there must exist an optimum value of R_f that causes the peak filter output impedance to be minimized. It can be shown [10,17] that all magnitude plots must pass through a common point, and therefore the optimum attains its peak at this point. This fact has been used to derive the design equations of optimally-damped L-C filter sections.

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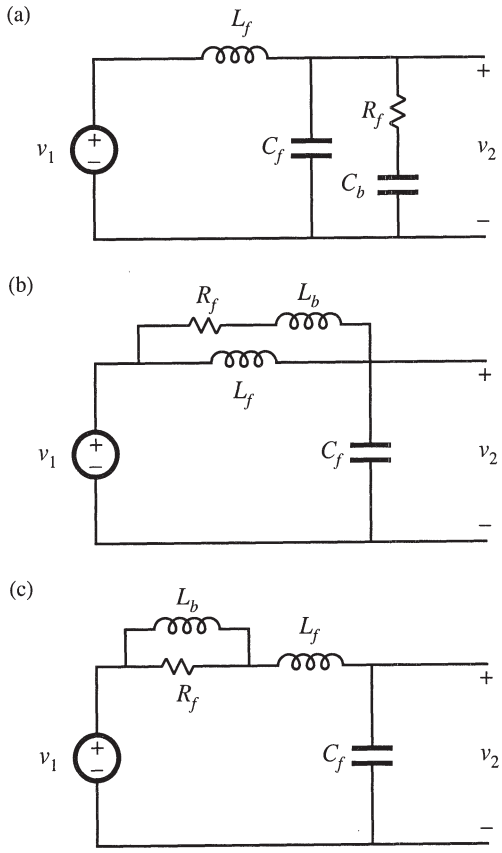


Fig. 10.20 Several practical approaches to damping the single-section input filter: (a) R_f-C_b parallel damping, (b) R_f-L_b parallel damping, (c) R_f-L_b series damping.

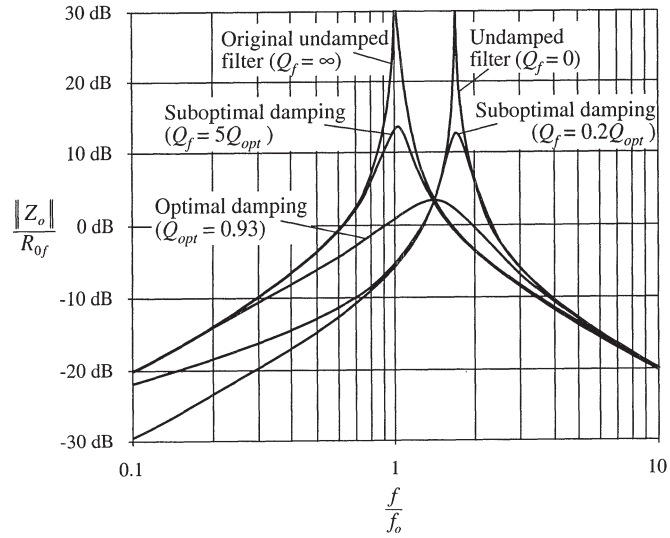


Fig. 10.21 Comparison of output impedance curves for optimal parallel R_f-L_b damping with undamped and several suboptimal designs. For this example, $n = L_b/L = 0.516$

10.4.1 R_f-C_b Parallel Damping

Optimization of the filter network of Fig. 10.20(a) and Section 10.3.2 was described in [10]. The high-frequency attenuation of this filter is not affected by the choice of C_b, and the high-frequency asymptote is identical to that of the original undamped filter. The sole tradeoff in design of the damping elements for this filter is in the size of the blocking capacitor C_b vs. the damping achieved.

For this filter, let us define the quantity n as the ratio of the blocking capacitance C_b to the filter capacitance C_f:

$$n = \frac{C_b}{C_f} \tag{10.28}$$

For the optimum design, the peak filter output impedance occurs at the frequency

$$f_m = f_f \sqrt{\frac{2}{2+n}} \tag{10.29}$$

The value of the peak output impedance for the optimum design is

$$\| Z_o \|_{\text{mm}} = R_{0f} \frac{\sqrt{2(2+n)}}{n} \tag{10.30}$$

The value of damping resistance that leads to optimum damping is described by

$$Q_{opt} = \frac{R_f}{R_{0f}} = \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}} \tag{10.31}$$

The above equations allow choice of the damping values R_f and C_b.

For example, let's redesign the damping network of Section 10.3.2, to achieve the same peak output impedance $\| Z_o(j\omega) \|_{\text{mm}} = 1\ \Omega$, while minimizing the value of the blocking capacitance C_b. From Section 10.3.2, the other parameter values are $R_{0f} = 0.84\ \Omega$, $C_f = 470\ \mu$F, and $L_f = 330\ \mu$H. First, we solve Eq. (10.30) to find the required value of n:

$$n = \frac{R_{0f}^2}{\| Z_o \|_{\text{mm}}^2} \left(1 + \sqrt{1 + 4 \frac{\| Z_o \|_{\text{mm}}^2}{R_{0f}^2}} \right) \tag{10.32}$$

Evaluation of this expression with the given numerical values leads to $n = 2.5$. The blocking capacitor is therefore required to have a value of $nC_f = 1200\ \mu$F. This is one-quarter of the value employed in Section 10.3.2. The value of R_f is then found by evaluation of Eq. (10.31), leading to

$$R_f = R_{0f} \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}} = 0.67\ \Omega \tag{10.33}$$

The output impedance of this filter design is compared with the output impedances of the original undamped filter of Section 10.3.1, and of the suboptimal design of Section 10.3.2, in Fig. 10.22. It can be

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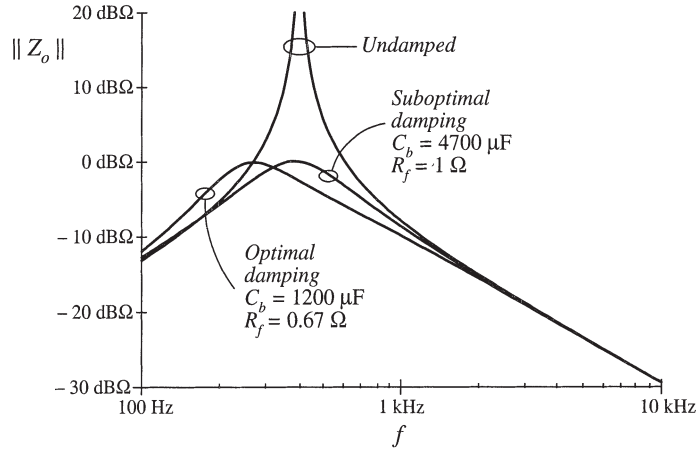


Fig. 10.22 Comparison of the output impedances of the design with optimal parallel R_f-C_b damping, the suboptimal design of Section 10.3.2, and the original undamped filter.

seen that the optimally damped filter does indeed achieve the desired peak output impedance of 1 Ω, at the slightly lower peak frequency given by Eq. (10.29)

The R_f-C_b parallel damping approach finds significant application in dc–dc converters. Since a series resistor is placed in series with C_b, C_b can be realized using capacitor types having substantial equivalent series resistance, such as electrolytic and tantalum types. However, in some applications, the R_f-L_b approaches of the next subsections can lead to smaller designs. Also, the large blocking capacitor value may be undesirable in applications having an ac input.

10.4.2 R_f-L_b Parallel Damping

Figure 10.20(b) illustrates the placement of damping resistor R_f in parallel with inductor L_f. Inductor L_b causes the filter to exhibit a two-pole attenuation characteristic at high frequency. To allow R_f to damp the filter, inductor L_b should have an impedance magnitude that is sufficiently smaller than R_f at the filter resonant frequency f_f. Optimization of this damping network is described in [17].

With this approach, inductor L_b can be physically much smaller than L_f. Since R_f is typically much greater than the dc resistance of L_f, essentially none of the dc current flows through L_b. Furthermore, R_f could be realized as the equivalent series resistance of L_b at the filter resonant frequency f_f. Hence, this is a very simple, low-cost approach to damping the input filter.

The disadvantage of this approach is the fact that the high-frequency attenuation of the filter is degraded: the high-frequency asymptote of the filter transfer function is increased from $1/\omega^2 L_f C_f$ to $1/\omega^2(L_f \| L_b)C_f$. Furthermore, since the need for damping limits the maximum value of L_b, significant loss of high-frequency attenuation is unavoidable. To compensate, the value of L_f must be increased. Therefore, a tradeoff occurs between damping and degradation of high-frequency attenuation, as illustrated in Fig. 10.23. For example, limiting the degradation of high-frequency attenuation to 6 dB leads to an optimum peak filter output impedance $\| Z_o \|_{\text{mm}}$ of $\sqrt{6}$ times the original characteristic impedance R_{0f}. Additional damping leads to further degradation of the high-frequency attenuation.

The optimally damped design (i.e., the choice of R_f that minimizes the peak output impedance

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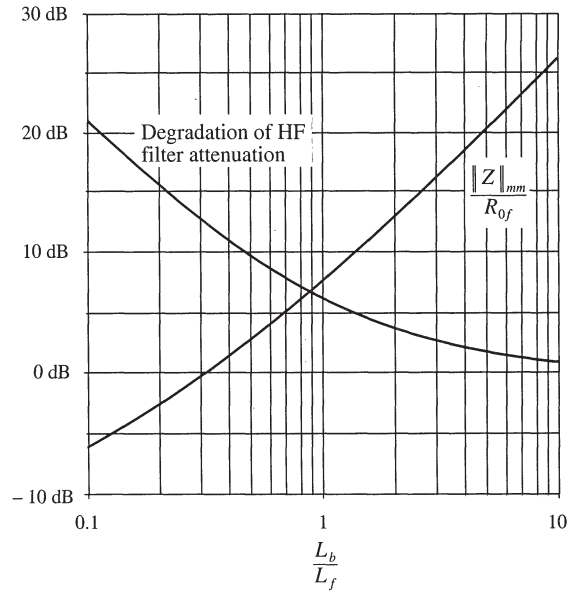


Fig. 10.23 Performance attained via optimal design procedure, parallel R_f-L_b circuit of 10.20(b). Optimum peak filter output impedance $\| Z_o \|_{\text{mm}}$ and increase of filter high-frequency gain, vs. $n = L_b/L$.

$\| Z_o \|$ for a given choice of L_b) is described by the following equations:

$$Q_{opt} = \frac{R_f}{R_{0f}} = \sqrt{\frac{n(3+4n)(1+2n)}{2(1+4n)}} \tag{10.34}$$

where

$$n = \frac{L_b}{L_f} \tag{10.35}$$

The peak filter output impedance occurs at frequency

$$f_m = f_f \sqrt{\frac{1+2n}{2n}} \tag{10.36}$$

and has the value

$$\| Z_o \|_{mm} = R_{0f} \sqrt{2n(1+2n)} \tag{10.37}$$

The attenuation of the filter high-frequency asymptote is degraded by the factor

$$\frac{L_f}{L_f \| L_b} = 1 + \frac{1}{n} \tag{10.38}$$

So, given an undamped L_f-C_f filter having corner frequency f_f, and characteristic impedance R_{0f}, and given a requirement for the maximum allowable output impedance $\| Z_o \|_{\text{mm}}$, one can solve Eq. (10.37) for the required value of n. One can then determine the required numerical values of L_b and R_f.

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10.4.3 R_f-L_b Series Damping

Figure 10.20(c) illustrates the placement of damping resistor R_f in series with inductor L_f. Inductor L_b provides a dc bypass to avoid significant power dissipation in R_f. To allow R_f to damp the filter, inductor L_b should have an impedance magnitude that is sufficiently greater than R_f at the filter resonant frequency.

Although this circuit is theoretically equivalent to the parallel damping R_f-L_b case of Section 10.4.2, several differences are observed in practical designs. Both inductors must carry the full dc current, and hence both have significant size. The filter high-frequency attenuation is not affected by the choice of L_b, and the high-frequency asymptote is identical to that of the original undamped filter. The tradeoff in design of this filter does not involve high-frequency attenuation; rather, the issue is damping vs. bypass inductor size.

Design equations similar to those of the previous sections can be derived for this case. The optimum peak filter output impedance occurs at frequency

$$f_m = f_f \sqrt{\frac{2+n}{2(1+n)}} \tag{10.39}$$

and has the value

$$\|Z_o\|_{mm} = R_{0f} \frac{\sqrt{2(1+n)(2+n)}}{n} \tag{10.40}$$

The value of damping resistance that leads to optimum damping is described by

$$Q_{opt} = \frac{R_{0f}}{R_f} = \left(\frac{1+n}{n}\right) \sqrt{\frac{2(1+n)(4+n)}{(2+n)(4+3n)}} \tag{10.41}$$

For this case, the peak output impedance cannot be reduced below $\sqrt{2}\,R_{0f}$ via damping. Nonetheless, it is possible to further reduce the filter output impedance by redesign of L_f and C_f, to reduce the value of R_{0f}.

10.4.4 Cascading Filter Sections

A cascade connection of multiple *L-C* filter sections can achieve a given high-frequency attenuation with less volume and weight than a single-section *L-C* filter. The increased cutoff frequency of the multiple-section filter allows use of smaller inductance and capacitance values. Damping of each *L-C* section is usually required, which implies that damping of each section should be optimized. Unfortunately, the results of the previous sections are restricted to single-section filters. Interactions between cascaded *L-C* sections can lead to additional resonances and increased filter output impedance.

It is nonetheless possible to design cascaded filter sections such that interaction between *L-C* sections is negligible. In the approach described below, the filter output impedance is approximately equal to the output impedance of the last section, and resonances caused by interactions between stages are avoided. Although the resulting filter may not be "optimal" in any sense, insight can be gained that allows intelligent design of multiple-section filters with economical damping of each section.

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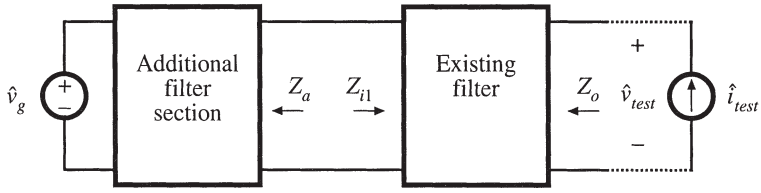


Fig. 10.24 Addition of a filter section at the input of an existing filter.

Consider the addition of a filter section to the input of an existing filter, as in Fig. 10.24. Let us assume that the existing filter has been correctly designed to meet the output impedance design criteria of Eq. (10.13): under the conditions $Z_a(s) = 0$ and $\hat{v}_g(s) = 0$, $\| Z_o \|$ is sufficiently small. It is desired to add a damped filter section that does not significantly increase $\| Z_o \|$.

Middlebrook's extra element theorem of Appendix C can again be invoked, to express how addition of the filter section modifies $Z_o(s)$:

$$\text{modified } Z_o(s) = \left[Z_o(s)\right]_{Z_a(s)=0} \frac{\left(1 + \dfrac{Z_a(s)}{Z_{N1}(s)}\right)}{\left(1 + \dfrac{Z_a(s)}{Z_{D1}(s)}\right)} \tag{10.42}$$

where

$$Z_{N1}(s) = Z_{i1}(s)\Big|_{\hat{v}_{test}(s) \xrightarrow[\text{null}]{} 0} \tag{10.43}$$

is the impedance at the input port of the existing filter, with its output port short-circuited. Note that, in this particular case, nulling $\hat{v}_{test}(s)$ is the same as shorting the filter output port because the short-circuit current flows through the $\hat{i}_{test}$ source. The quantity

$$Z_{D1}(s) = Z_{i1}(s)\Big|_{\hat{i}_{test}(s)=0} \tag{10.44}$$

is the impedance at the input port of the existing filter, with its output port open-circuited. Hence, the additional filter section does not significantly alter Z_o provided that

$$\begin{aligned} \| Z_a \| &\ll \| Z_{N1} \| \quad \text{and} \\ \| Z_a \| &\ll \| Z_{D1} \| \end{aligned} \tag{10.45}$$

Bode plots of the quantities Z_{N1} and Z_{D1} can be constructed either analytically or by computer simulation, to obtain limits of Z_a. When $\| Z_a \|$ satisfies Eq. (10.45), then the "correction factor" $(1 + Z_a/Z_{N1})/(1 + Z_a/Z_{D1})$ is approximately equal to 1, and the modified Z_o is approximately equal to the original Z_o.

To satisfy the design criteria (10.45), it is advantageous to select the resonant frequencies of Z_a to differ from the resonant frequencies of Z_{D1}. In other words, we should stagger-tune the filter sections. This minimizes the interactions between filter sections, and can allow use of smaller reactive element values.

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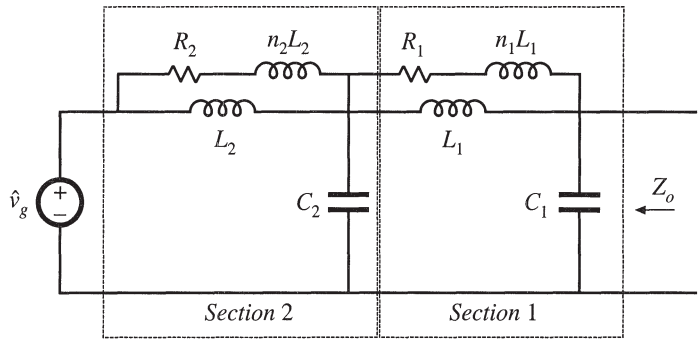


Fig. 10.25 Two-section input filter example, employing R_f-L_b parallel damping in each section.

10.4.5 Example: Two Stage Input Filter

As an example, let us consider the design of a two-stage filter using R_f-L_b parallel damping in each section as illustrated in Fig. 10.25 [17]. It is desired to achieve the same attenuation as the single-section filters designed in Sections 10.3.2 and 10.4.1, and to filter the input current of the same buck converter example of Fig. 10.8. These filters exhibit an attenuation of 80 dB at 250 kHz, and satisfy the design inequalities of Eq. (10.13) with the $\| Z_N \|$ and $\| Z_D \|$ impedances of Fig. 10.10. Hence, let's design the filter of Fig. 10.25 to attain 80 dB of attenuation at 250 kHz.

As described in the previous section and below, it is advantageous to stagger-tune the filter sections so that interaction between filter sections is reduced. We will find that the cutoff frequency of filter section 1 should be chosen to be smaller than the cutoff frequency of section 2. In consequence, the attenuation of section 1 will be greater than that of section 2. Let us (somewhat arbitrarily) design to obtain 45 dB of attenuation from section 1, and 35 dB of attenuation from section 2 (so that the total is the specified 80 dB). Let us also select $n_1 = n_2 = n = L_b/L_f = 0.5$ for each section; as illustrated in Fig. 10.23, this choice leads to a good compromise between damping of the filter resonance and degradation of high frequency filter attenuation. Equation (10.38) and Fig. 10.23 predict that the R_f-L_b damping network will degrade the high frequency attenuation by a factor of $(1 + 1/n) = 3$, or 9.5 dB. Hence, the section 1 undamped resonant frequency f_{f1} should be chosen to yield 45 dB + 9.5 dB = 54.5 dB $\Rightarrow$ 533 of attenuation at 250 kHz. Since section 1 exhibits a two-pole (– 40 dB/decade) roll-off at high frequencies, f_{f1} should be chosen as follows:

$$f_{f1} = \frac{(250\text{ kHz})}{\sqrt{533}} = 10.8\text{ kHz} \tag{10.46}$$

Note that this frequency is well above the 1.6 kHz resonant frequency f_0 of the buck converter output filter. Consequently, the output impedance $\| Z_o \|$ can be as large as 3 Ω, and still be well below the $\| Z_N(j\omega) \|$ and $\| Z_D(j\omega) \|$ plots of Fig. 10.10.

Solution of Eq. (10.37) for the required section 1 characteristic impedance that leads to a peak output impedance of 3 Ω with $n = 0.5$ leads to

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$$R_{0f1} = \frac{\| Z_o \|_{mm}}{\sqrt{2n(1+2n)}} = \frac{3\ \Omega}{\sqrt{2(0.5)(1+2(0.5))}} = 2.12\ \Omega \tag{10.47}$$

The filter inductance and capacitance values are therefore

$$\begin{aligned} L_1 &= \frac{R_{0f1}}{2\pi f_{f1}} = 31.2\ \mu\text{H} \\ C_1 &= \frac{1}{2\pi f_{f1} R_{0f1}} = 6.9\ \mu\text{F} \end{aligned} \tag{10.48}$$

The section 1 damping network inductance is

$$n_1 L_1 = 15.6\ \mu\text{H} \tag{10.49}$$

The section 1 damping resistance is found from Eq. (10.34):

$$R_1 = Q_{opt} R_{0f1} = R_{0f1} \sqrt{\frac{n(3+4n)(1+2n)}{2(1+4n)}} = 1.9\ \Omega \tag{10.50}$$

The peak output impedance will occur at the frequency given by Eq. (10.36), 15.3 kHz. The quantities $\| Z_{N1}(j\omega) \|$ and $\| Z_{D1}(j\omega) \|$ for filter section 1 can now be constructed analytically or plotted by computer simulation. $\| Z_{N1}(j\omega) \|$ is the section 1 input impedance Z_{i1} with the output of section 1 shorted, and is given by the parallel combination of the sL_1 and the $(R_1 + sn_1L_1)$ branches. $\| Z_{D1}(j\omega) \|$ is the section 1 input impedance Z_{i1} with the output of section 1 open-circuited, and is given by the series combination of $Z_{N1}(s)$ with the capacitor impedance $1/sC_1$. Figure 10.26 contains plots of $\| Z_{N1}(j\omega) \|$ and $\| Z_{D1}(j\omega) \|$ for filter section 1, generated using Spice.

One way to approach design of filter section 2 is as follows. To avoid significantly modifying the overall filter output impedance Z_o, the section 2 output impedance $\| Z_a(j\omega) \|$ must be sufficiently less than $\| Z_{N1}(j\omega) \|$ and $\| Z_{D1}(j\omega) \|$. It can be seen from Fig. 10.26 that, with respect to $\| Z_{D1}(j\omega) \|$, this is most difficult to accomplish when the peak frequencies of sections 1 and 2 coincide. It is most difficult to satisfy the $\| Z_{N1}(j\omega) \|$ design criterion when the peak frequency of sections 2 is lower than the peak frequency of section 1. Therefore, the best choice is to stagger-tune the filter sections, with the resonant frequency of section 1 being lower than the peak frequency of section 2. This implies that section 1 will produce more high-frequency attenuation than section 2. For this reason, we have chosen to achieve 45 dB of attenuation with section 1, and 35 dB of attenuation from section 2.

The section 2 undamped resonant frequency f_{f2} should be chosen in the same manner used in Eq. (10.46) for section 1. We have chosen to select $n_2 = n = L_b/L_f = 0.5$ for section 2; this again means that the R_f-L_b damping network will degrade the high frequency attenuation by a factor of $(1 + 1/n) = 3$, or 9.5 dB. Hence, the section 2 undamped resonant frequency f_{f2} should be chosen to yield 35 dB + 9.5 dB = 44.5 dB $\Rightarrow$ 169 of attenuation at 250 kHz. Since section 2 exhibits a two-pole (– 40 dB/decade) roll-off at high frequencies, f_{f2} should be chosen as follows:

$$f_{f2} = \frac{(250\ \text{kHz})}{\sqrt{169}} = 19.25\ \text{kHz} \tag{10.51}$$

The output impedance of section 2 will peak at the frequency 27.2 kHz, as given by Eq. (10.36). Hence, the peak frequencies of sections 1 and 2 differ by almost a factor of 2.

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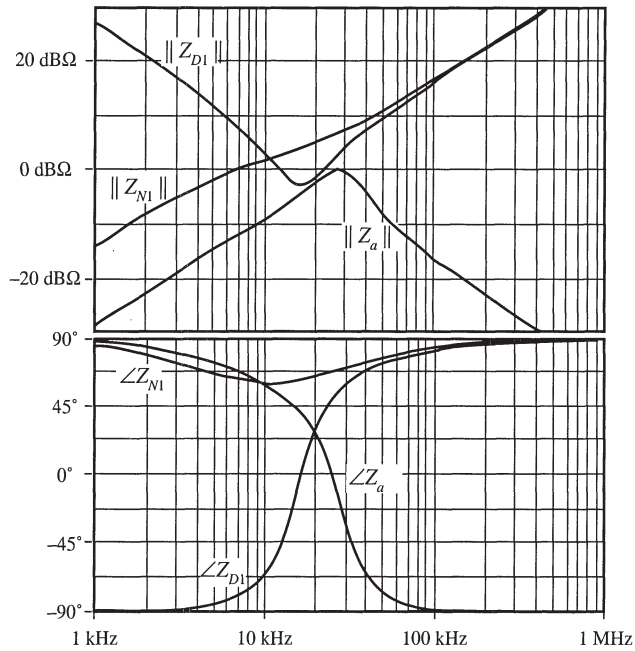


Fig. 10.26 Bode plot of Z_{N1} and Z_{D1} for filter section 1. Also shown is the Bode plot for the output impedance Z_a of filter section 2.

Figure 10.26 shows that, at 27.2 kHz, $\| Z_{D1}(j\omega) \|$ has a magnitude of roughly 3 dBΩ, and that $\| Z_{N1}(j\omega) \|$ is approximately 7 dBΩ. Hence, let us design section 2 to have a peak output impedance of 0 dBΩ $\Rightarrow$ 1 Ω. Solution of Eq. (10.37) for the required section 2 characteristic impedance leads to

$$R_{0f2} = \frac{\| Z_a \|_{\text{mm}}}{\sqrt{2n(1+2n)}} = \frac{1\ \Omega}{\sqrt{2(0.5)(1+2(0.5))}} = 0.71\ \Omega \tag{10.52}$$

The section 2 element values are therefore

$$\begin{aligned} L_2 &= \frac{R_{0f2}}{2\pi f_{f2}} = 5.8\ \mu\text{H} \\ C_2 &= \frac{1}{2\pi f_{f2} R_{0f2}} = 11.7\ \mu\text{F} \\ n_2 L_2 &= 2.9\ \mu\text{H} \\ R_2 &= Q_{opt} R_{0f2} = R_{0f2} \sqrt{\frac{n(3+4n)(1+2n)}{2(1+4n)}} = 0.65\ \Omega \end{aligned} \tag{10.53}$$

A Bode plot of the resulting Z_a is overlaid on Fig. 10.26. It can be seen that $\| Z_a(j\omega) \|$ is less than, but very close to, $\| Z_{D1}(j\omega) \|$ between the peak frequencies of 15 kHz and 27 kHz. The impedance inequalities (10.45) are satisfied somewhat better below 15 kHz, and are satisfied very well at high frequency.

The resulting filter output impedance $\| Z_o(j\omega) \|$ is plotted in Fig. 10.27, for section 1 alone and for the complete cascaded two-section filter. It can be seen that the peak output impedance is approxi-

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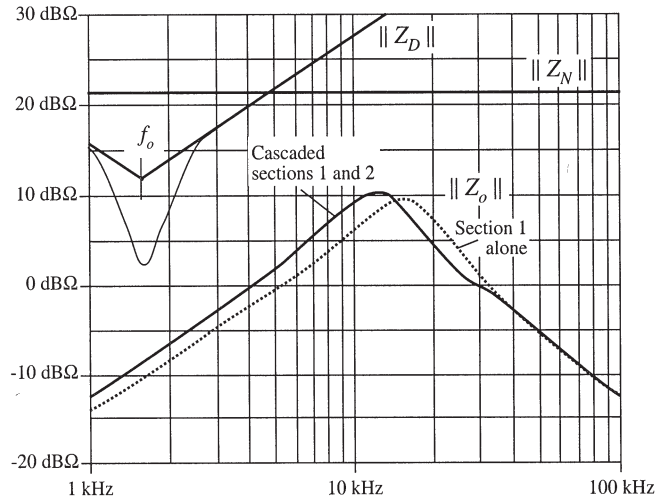


Fig. 10.27 Comparison of the impedance design criteria $\| Z_N(j\omega) \|$ and $\| Z_D(j\omega) \|$, Eq. (10.13), with the filter output impedance $\| Z_o(j\omega) \|$. *Solid line:* $\| Z_o(j\omega) \|$ of cascaded design. *Dashed line:* $\| Z_o(j\omega) \|$ of section 1 alone.

mately 10 dBΩ, or roughly 3 Ω. The impedance design criteria (10.13) are also shown, and it can be seen that the filter meets these design criteria. Note the absence of resonances in $\| Z_o(j\omega) \|$.

The effect of stage 2 on $\| Z_o(j\omega) \|$ is very small above 40 kHz [where inequalities (10.45) are very well satisfied], and has moderate-to-small effect at lower frequencies. It is interesting that, above approximately 12 kHz, the addition of stage 2 actually *decreases* $\| Z_o(j\omega) \|$. The reason for this can be seen from Fig. C.8 of Appendix C: when the phase difference between $\angle Z_a(j\omega)$ and $\angle Z_{D1}(j\omega)$ is not too large ($\leq 90^\circ$), then the $1/(1 + Z_a/Z_{D1})$ term decreases the magnitude of the resulting $\| Z_o(j\omega) \|$. As can be seen from the phase plot of Fig. 10.26, this is indeed what happens. So allowing $\| Z_a(j\omega) \|$ to be similar in magnitude to $\| Z_{D1}(j\omega) \|$ above 12 kHz was an acceptable design choice.

The resulting filter transfer function is illustrated in Fig. 10.28. It can be seen that it does indeed attain the goal of 80 dB attenuation at 250 kHz.

Figure 10.29 compares the single stage design of Section 10.4.1 to the two-stage design of this section. Both designs attain 80 dB attenuation at 250 kHz, and both designs meet the impedance design criteria of Eq. (10.13). However, the single-stage approach requires much larger filter elements.

10.5 SUMMARY OF KEY POINTS

1. Switching converters usually require input filters, to reduce conducted electromagnetic interference and possibly also to meet requirements concerning conducted susceptibility.
2. Addition of an input filter to a converter alters the control-to-output and other transfer functions of the converter. Design of the converter control system must account for the effects of the input filter.
3. If the input filter is not damped, then it typically introduces complex poles and RHP zeroes into the converter control-to-output transfer function, at the resonant frequencies of the input filter. If these resonant frequencies are lower than the crossover frequency of the controller loop gain, then the phase margin will become negative and the regulator will be unstable.

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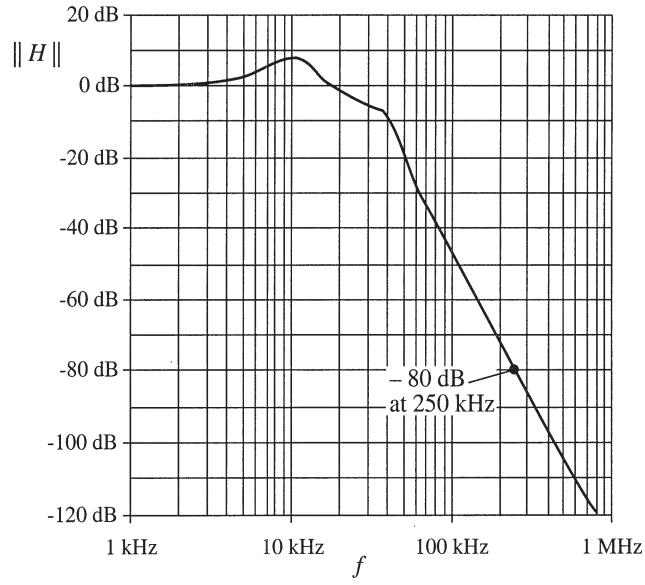


Fig. 10.28 Input filter transfer function, cascaded two-section design.

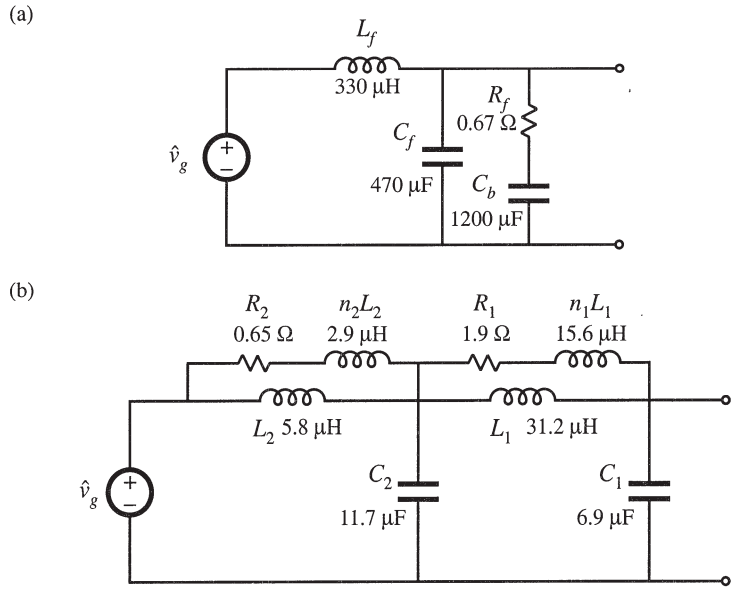


Fig. 10.29 Comparison of single-section (a) and two section (b) input filter designs. Both designs meet the design criteria (10.13), and both exhibit 80 dB of attenuation at 250 kHz.

4. The input filter can be designed so that it does not significantly change the converter control-to-output and other transfer functions. Impedance inequalities (10.13) give simple design criteria that guarantee this. To meet these design criteria, the resonances of the input filter must be sufficiently damped.

5. Optimization of the damping networks of single-section filters can yield significant savings in filter element size. Equations for optimizing three different filter sections are listed.

6. Substantial savings in filter element size can be realized via cascading filter sections. The design of noninteracting cascaded filter sections can be achieved by an approach similar to the original input filter design method. Impedance inequalities (10.45) give design criteria that guarantee that interactions are not substantial.

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PROBLEMS

10.1 It is required to design an input filter for the flyback converter of Fig. 10.30. The maximum allowed amplitude of switching harmonics of $i_{in}(t)$ is 10 μA rms. Calculate the required attenuation of the filter at the switching frequency.

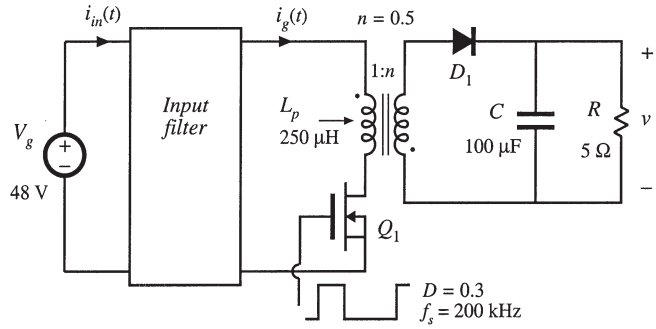


Fig. 10.30 Flyback converter, Problems 10.1, 10.4, 10.6, 10.8, and 10.10.

10.2 In the boost converter of Fig. 10.31, the input filter is designed so that the maximum amplitude of switching harmonics of $i_{in}(t)$ is not greater than 10 μA rms. Find the required attenuation of the filter at the switching frequency.

10.3 Derive the expressions for Z_N and Z_D in Table 10.1.

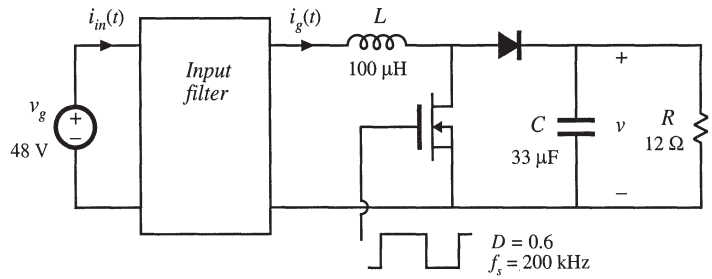


Fig. 10.31 Boost converter, Problems 10.2, 10.5, 10.7, and 10.9.

10.4 The input filter for the flyback converter of Fig. 10.30 is designed using a single L_f-C_f section. The filter is damped using a resistor R_f in series with a very large blocking capacitor C_b.

(a) Sketch a small-signal model of the flyback converter. Derive expressions for $Z_N(s)$ and $Z_D(s)$ using your model. Sketch the magnitude Bode plots of Z_N and Z_D, and label all salient features.

(b) Design the input filter, i.e., select the values of L_f, C_f, and R_f, so that: (*i*) the filter attenuation at the switching frequency is at least 100 dB, and (*ii*) the magnitude of the filter output impedance $Z_o(s)$ satisfies the conditions $\| Z_o(j\omega) \| < 0.3 \| Z_D(j\omega) \|$, $\| Z_o(j\omega) \| < 0.3 \| Z_N(j\omega) \|$, for all frequencies.

(c) Use Spice simulations to verify that the filter designed in part (b) meets the specifications.

(d) Using Spice simulations, plot the converter control-to-output magnitude and phase responses without the input filter, and with the filter designed in part (b). Comment on the changes introduced by the filter.

10.5 It is required to design the input filter for the boost converter of Fig. 10.31 using a single L_f-C_f section. The filter is damped using a resistor R_f in series with a very large blocking capacitor C_b.

(a) Sketch the magnitude Bode plots of $Z_N(s)$ and $Z_D(s)$ for the boost converter, and label all salient features.

(b) Design the input filter, i.e., select the values of L_f, C_f, and R_f, so that: (*i*) the filter attenuation at the switching frequency is at least 80 dB, and (*ii*) the magnitude of the filter output impedance $Z_o(s)$ satisfies the conditions $\| Z_o(j\omega) \| < 0.2 \| Z_D(j\omega) \|$, $\| Z_o(j\omega) \| < 0.2 \| Z_N(j\omega) \|$, for all frequencies.

(c) Use Spice simulations to verify that the filter designed in part (b) meets the specifications.

(d) Using Spice simulations, plot the converter control-to-output magnitude and phase responses without the input filter, and with the filter designed in part (b). Comment on the changes in the control-to-output responses introduced by the filter.

10.6 Repeat the filter design of Problem 10.4 using the optimum filter damping approach described in Section 10.4.1. Find the values of L_f, C_f, R_f, and C_b.

10.7 Repeat the filter design of Problem 10.5 using the optimum filter damping approach of Section 10.4.1. Find the values of L_f, C_f, R_f, and C_b.

10.8 Repeat the filter design of Problem 10.4 using the optimum R_f-L_b parallel damping approach described in Section 10.4.2. Find the values of L_f, C_f, R_f, and L_b.

10.9 Repeat the filter design of Problem 10.5 using the optimum R_f-L_b parallel damping approach described in Section 10.4.2. Find the values of L_f, C_f, R_f, and L_b.

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10.10 It is required to design the input filter for the flyback converter of Fig. 10.30 using two filter sections. Each filter section is damped using a resistor in series with a blocking capacitor.

(a) Design the input filter, i.e., select values of all circuit parameters, so that (*i*) the filter attenuation at the switching frequency is at least 100 dB, and (*ii*) the magnitude of the filter output impedance $Z_o(s)$ satisfies the conditions $\| Z_o(j\omega) \| < 0.3 \| Z_D(j\omega) \|$, $\| Z_o(j\omega) \| < 0.3 \| Z_N(j\omega) \|$, for all frequencies.

(b) Use Spice simulations to verify that the filter designed in part (a) meets the specifications.

(c) Using Spice simulations, plot the converter control-to-output magnitude and phase responses without the input filter, and with the filter designed in part (b). Comment on the changes introduced by the filter.

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11

AC and DC Equivalent Circuit Modeling of the Discontinuous Conduction Mode

So far, we have derived equivalent circuit models for dc–dc pulse-width modulation (PWM) converters operating in the continuous conduction mode. As illustrated in Fig. 11.1, the basic dc conversion property is modeled by an effective dc transformer, having a turns ratio equal to the conversion ratio $M(D)$. This model predicts that the converter has a voltage-source output characteristic, such that the output voltage is essentially independent of the load current or load resistance R. We have also seen how to refine this model, to predict losses and efficiency, converter dynamics, and small-signal ac transfer functions. We found that the transfer functions of the buck converter contain two low-frequency poles, owing to the converter filter inductor and capacitor. The control-to-output transfer functions of the boost and buck-boost converters additionally contain a right half-plane zero. Finally, we have seen how to utilize these results in the design of converter control systems.

What are the basic dc and small-signal ac equivalent circuits of converters operating in the discontinuous conduction mode (DCM)? It was found in Chapter 5 that, in DCM, the output voltage becomes load-dependent: the conversion ratio $M(D, K)$ is a function of the dimensionless parameter $K = 2L/RT_s$, which in turn is a function of the load resistance R. So the converter no longer has a voltage-source output characteristic, and hence the dc transformer model is less appropriate. In this chapter, the averaged switch modeling [1-8] approach is employed, to derive equivalent circuits of the DCM switch network.

In Section 11.1, it is shown that the *loss-free resistor* model [9-11] is the averaged switch model of the DCM switch network. This equivalent circuit represents the steady-state and large-signal dynamic characteristics of the DCM switch network, in a clear and simple manner. In the discontinuous conduction mode, the average transistor voltage and current obey Ohm's law, and hence the transistor is modeled by an effective resistor R_e. The average diode voltage and current obey a power source characteristic, with power equal to the power effectively dissipated in R_e. Therefore, the diode is modeled with a *dependent power source*.

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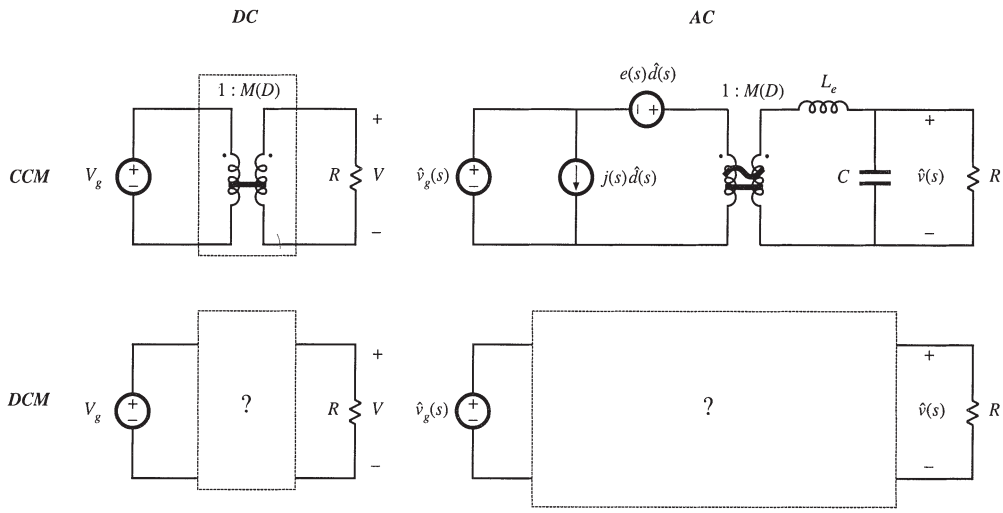


Fig. 11.1 The objective of this chapter is the derivation of large-signal dc and small-signal ac equivalent circuit models for converters operating in the discontinuous conduction mode.

Since most converters operate in discontinuous conduction mode at some operating points, small-signal ac DCM models are needed, to prove that the control systems of such converters are correctly designed. In Section 11.2, a small-signal model of the DCM switch network is derived by linearization of the loss-free resistor model. The transfer functions of DCM converters are quite different from their respective CCM transfer functions. The basic DCM buck, boost, and buck-boost converters essentially exhibit simple single-pole transfer functions [12, 13], in which the second pole and the RHP zero (in the case of boost and buck-boost converters) are at high frequencies. So the basic converters operating in DCM are easy to control; for this reason, converters are sometimes purposely operated in DCM for all loads. The transfer functions of higher order converters such as the DCM Ćuk or SEPIC are considerably more complicated; but again, one pole is shifted to high frequency, where it has negligible practical effect. This chapter concludes, in Section 11.3, with a discussion of a more detailed analysis used to predict high-frequency dynamics of DCM converters. The more detailed analysis predicts that the high-frequency pole of DCM converters occurs at frequencies near or exceeding the switching frequency [2-6]. The RHP zero, in the case of DCM buck-boost and boost converters, also occurs at high frequencies. This is why, in practice, the high-frequency dynamics can usually be neglected in DCM.

11.1 DCM AVERAGED SWITCH MODEL

Consider the buck-boost converter of Fig. 11.2. Let us follow the averaged switch modeling approach of Section 7.4, to derive an equivalent circuit that models the averaged terminal waveforms of the switch network. The general two-switch network and its terminal quantities $v_1(t)$, $i_1(t)$, $v_2(t)$, and $i_2(t)$ are defined as illustrated in Fig. 11.2, consistent with Fig. 7.39(a). The inductor and switch network voltage and current waveforms are illustrated in Fig. 11.3, for DCM operation.

The inductor current is equal to zero at the beginning of each switching period. During the first subinterval, while the transistor conducts, the inductor current increases with a slope of $v_g(t)/L$. At the

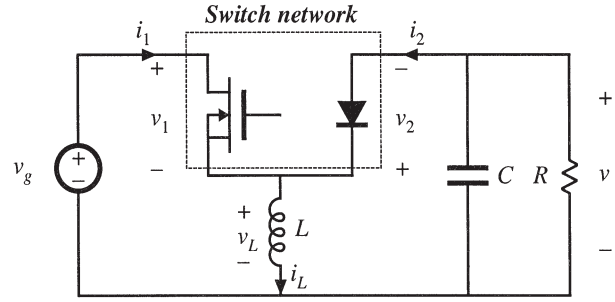


Fig. 11.2 Buck-boost converter example, with switch network terminal quantities identified.

end of the first subinterval, the inductor current $i_L(t)$ attains the peak value given by

$$i_{pk} = \frac{v_g}{L} d_1 T_s \tag{11.1}$$

During the second subinterval, while the diode conducts, the inductor current decreases with a slope equal to $v(t)/L$. The second subinterval ends when the diode becomes reverse-biased, at time $t = (d_1 + d_2)T_s$. The inductor current then remains at zero for the balance of the switching period. The inductor voltage is zero during the third subinterval.

A DCM averaged switch model can be derived with reference to the waveforms of Fig. 11.3. Following the approach of Section 7.4.2, let us find the average values of the switch network terminal waveforms $v_1(t)$, $v_2(t)$, $i_1(t)$, and $i_2(t)$ in terms of the converter state variables (inductor currents and capacitor voltages), the input voltage $v_g(t)$, and the subinterval lengths d_1 and d_2.

The average switch network input voltage $\langle v_1(t) \rangle_{T_s}$, or the average transistor voltage, is found by averaging the $v_1(t)$ waveform of Fig. 11.3:

$$\left\langle v_1(t) \right\rangle_{T_s} = d_1(t) \cdot 0 + d_2(t) \left(\left\langle v_g(t) \right\rangle_{T_s} - \left\langle v(t) \right\rangle_{T_s} \right) + d_3(t) \left\langle v_g(t) \right\rangle_{T_s} \tag{11.2}$$

Use of the identity $d_3(t) = 1 - d_1(t) - d_2(t)$ yields

$$\left\langle v_1(t) \right\rangle_{T_s} = \left(1 - d_1(t)\right) \left\langle v_g(t) \right\rangle_{T_s} - d_2(t) \left\langle v(t) \right\rangle_{T_s} \tag{11.3}$$

Similar analysis leads to the following expression for the average diode voltage:

$$\begin{aligned} \left\langle v_2(t) \right\rangle_{T_s} &= d_1(t) \left(\left\langle v_g(t) \right\rangle_{T_s} - \left\langle v(t) \right\rangle_{T_s} \right) + d_2(t) \cdot 0 + d_3(t) \left(- \left\langle v(t) \right\rangle_{T_s} \right) \\ &= d_1(t) \left\langle v_g(t) \right\rangle_{T_s} - \left(1 - d_2(t)\right) \left\langle v(t) \right\rangle_{T_s} \end{aligned} \tag{11.4}$$

The average switch network input current $\langle i_1(t) \rangle_{T_s}$ is found by integrating the $i_1(t)$ waveform of Fig. 11.3 over one switching period:

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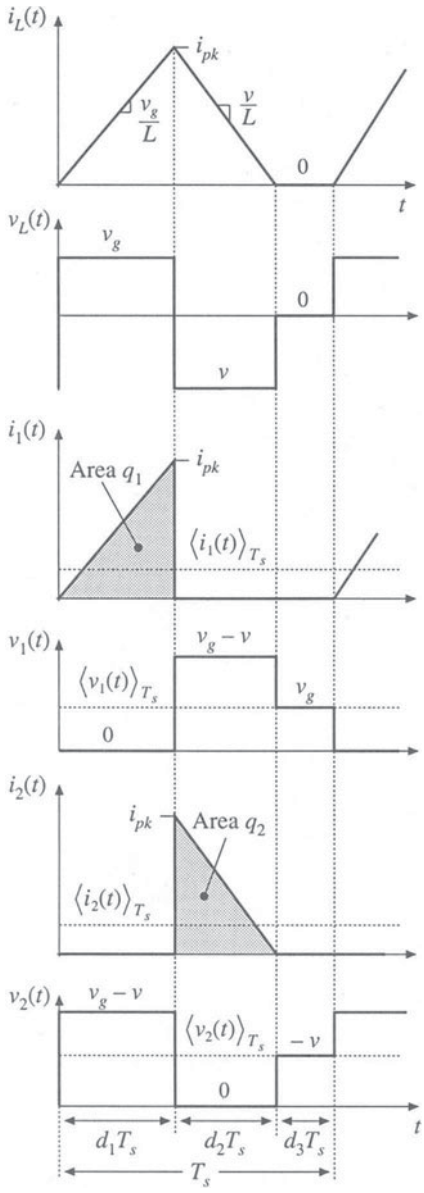


Fig. 11.3 Inductor and switch network voltage and current waveforms.

$$\langle i_1(t)\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} i_1(t)dt = \frac{q_1}{T_s} \tag{11.5}$$

The integral q_1 is equal to the area under the $i_1(t)$ waveform during the first subinterval. This area is easily evaluated using the triangle area formula:

$$q_1 = \int_t^{t+T_s} i_1(t)dt = \frac{1}{2}\left(d_1T_s\right)\left(i_{pk}\right) \tag{11.6}$$

Substitution of Eqs. (11.1) and (11.6) into Eq. (11.5) gives:

$$\langle i_1(t)\rangle_{T_s} = \frac{d_1^2(t)T_s}{2L}\langle v_g(t)\rangle_{T_s} \tag{11.7}$$

Note that $\langle i_1(t)\rangle_{T_s}$ is not equal to $d_1\langle i_L(t)\rangle_{T_s}$. Since the inductor current ripple is not small, it is necessary to sketch the actual input current waveform, including the large switching ripple, and then correctly compute the average as in Eqs. (11.5) to (11.7).

The average diode current $\langle i_2(t)\rangle_{T_s}$ is found in a manner similar to that used above for $\langle i_1(t)\rangle_{T_s}$:

$$\langle i_2(t)\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} i_2(t)dt = \frac{q_2}{T_s} \tag{11.8}$$

The integral q_2 is equal to the area under the $i_2(t)$ waveform during the second subinterval. This area is evaluated using the triangle area formula:

$$q_2 = \int_t^{t+T_s} i_2(t)dt = \frac{1}{2}\left(d_2T_s\right)\left(i_{pk}\right) \tag{11.9}$$

Substitution of Eqs. (11.1) and (11.9) into Eq. (11.8) leads to:

$$\langle i_2(t)\rangle_{T_s} = \frac{d_1(t)d_2(t)T_s}{2L}\langle v_g(t)\rangle_{T_s} \tag{11.10}$$

Equations (11.3), (11.4), (11.7) and (11.10) constitute the averaged terminal equations of the switch network in the DCM buck-boost converter. In these equations, it remains to express the subinterval length d_2 in terms of the switch duty cycle $d_1 = d$, and the converter averaged waveforms. One approach to finding the subinterval length d_2 is by solving the inductor current waveform. In the buck-boost converter, the diode switches off when the inductor current reaches zero, at the end of the sec-

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ond subinterval. As a result, $i_L(T_s) = i_L(0) = 0$. There is no net change in inductor current over one complete switching period, and no net volt-seconds are applied to the inductor over any complete switching period that starts at the time when the transistor is turned on. Therefore, the average inductor voltage computed over this period is zero,

$$\left\langle v_L(t)\right\rangle_{T_s} = d_1\left\langle v_g(t)\right\rangle_{T_s} + d_2\left\langle v(t)\right\rangle_{T_s} + d_3 \cdot 0 = 0 \tag{11.11}$$

even when the converter is not in equilibrium. This equation can be used to find the length of the second subinterval:

$$d_2(t) = -d_1(t)\frac{\left\langle v_g(t)\right\rangle_{T_s}}{\left\langle v(t)\right\rangle_{T_s}} \tag{11.12}$$

Substitution of Eq. (11.12) into Eqs. (11.3), (11.4), (11.7) and (11.10), allows us to obtain simple expressions for the averaged terminal waveforms of the switch network in the discontinuous conduction mode:

$$\left\langle v_1(t)\right\rangle_{T_s} = \left\langle v_g(t)\right\rangle_{T_s} \tag{11.13}$$

$$\left\langle v_2(t)\right\rangle_{T_s} = -\left\langle v(t)\right\rangle_{T_s} \tag{11.14}$$

$$\left\langle i_1(t)\right\rangle_{T_s} = \frac{d_1^2(t)T_s}{2L}\left\langle v_1(t)\right\rangle_{T_s} \tag{11.15}$$

$$\left\langle i_2(t)\right\rangle_{T_s} = \frac{d_1^2(t)T_s}{2L}\frac{\left\langle v_1(t)\right\rangle_{T_s}^2}{\left\langle v_2(t)\right\rangle_{T_s}} \tag{11.16}$$

Let us next construct an equivalent circuit corresponding to the averaged switch network equations (11.15) and (11.16). The switch network input port is modeled by Eq. (11.15). This equation states that the average input current $\langle i_1(t)\rangle_{T_s}$ is proportional to the applied input voltage $\langle v_1(t)\rangle_{T_s}$. In other words, the low-frequency components of the switch network input port obey Ohm's law:

$$\left\langle i_1(t)\right\rangle_{T_s} = \frac{\left\langle v_1(t)\right\rangle_{T_s}}{R_e(d_1)} \tag{11.17}$$

where the effective resistance R_e is

$$R_e(d_1) = \frac{2L}{d_1^2 T_s} \tag{11.18}$$

An equivalent circuit is illustrated in Fig. 11.4. During the first subinterval, the slope of the input current waveform $i_1(t)$ is proportional to the input voltage $\langle v_g(t)\rangle_{T_s} = \langle v_1(t)\rangle_{T_s}$, as illustrated in Fig. 11.3. As a result, the peak current i_{pk}, the total charge q_1, and the average input current $\langle i_1(t)\rangle_{T_s}$, are also proportional to $\langle v_1(t)\rangle_{T_s}$. Of course, there is no physical resistor inside the converter. Indeed, if the converter elements are ideal, then no heat is generated inside the converter. Rather, the power apparently consumed by R_e is transferred to the switch network output port.

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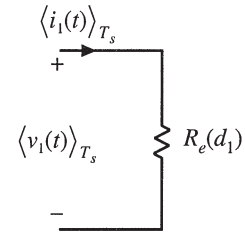


Fig. 11.4 Equivalent circuit that models the average waveforms of the switch input (transistor) port.

The switch network output (diode) port is modeled by Eq. (11.16), or

$$\langle i_2(t)\rangle_{T_s}\langle v_2(t)\rangle_{T_s} = \frac{\langle v_1(t)\rangle_{T_s}^2}{R_e(d_1)} = \langle p(t)\rangle_{T_s} \tag{11.19}$$

Note that $\langle v_1(t)\rangle_{T_s}^2/R_e$ is the average power $\langle p(t)\rangle_{T_s}$ apparently consumed by the effective resistor $R_e(d_1)$. Equation (11.19) states that this power flows out of the switch network output port. So the switch network consumes no net power—its average input and output powers are equal.

Equation (11.19) can also be derived by consideration of the inductor stored energy. During the first subinterval, the inductor current increases from 0 to i_{pk}. In the process, the inductor stores the following energy:

$$\frac{1}{2}Li_{pk}^2 = \frac{\langle v_1\rangle_{T_s}^2 d_1^2 T_s^2}{2L} = \frac{\langle v_1\rangle_{T_s}^2}{R_e(d_1)}T_s \tag{11.20}$$

Here, i_{pk} has been expressed in terms of $\langle v_1(t)\rangle_{T_s}$ using Eqs. (11.1) and (11.13). This energy is transferred from the source v_g, through the switch network input terminals (i.e., through the transistor), to the inductor. During the second subinterval, the inductor releases all of its stored energy through the switch network output terminals (i.e., through the diode), to the output. The average output power can therefore be expressed as the energy transferred per cycle, divided by the switching period:

$$\langle p(t)\rangle_{T_s} = \left(\frac{\langle v_1\rangle_{T_s}^2}{R_e(d_1)}T_s\right)\left(\frac{1}{T_s}\right) = \frac{\langle v_1\rangle_{T_s}^2}{R_e(d_1)} \tag{11.21}$$

This power is transferred to the load, and hence

$$\langle v\rangle_{T_s}\langle i_2\rangle_{T_s} = \langle v_2\rangle_{T_s}\langle i_2\rangle_{T_s} = \langle p(t)\rangle_{T_s} = \frac{\langle v_1\rangle_{T_s}^2}{R_e(d_1)} \tag{11.22}$$

This result coincides with Eq. (11.19).

The average power $\langle p(t)\rangle_{T_s}$ is independent of the load characteristics, and is determined solely by the effective resistance R_e and the applied switch network input terminal voltage or current. In other words, the switch network output port behaves as a source of power, equal to the power apparently consumed by the effective resistance R_e. This behavior is represented schematically by the dependent power source symbol illustrated in Fig. 11.5. In any lossless two-port network, when the voltage and current at one port are independent of the characteristics of the external network connected to the second port, then the second port must exhibit a dependent power source characteristic [10]. This situation arises in a num-

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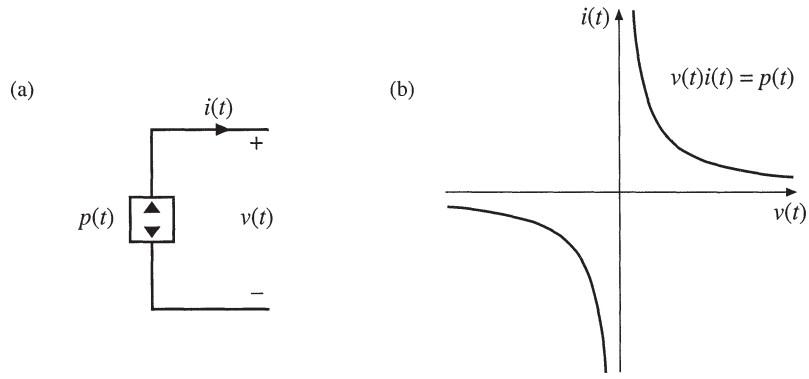


Fig. 11.5 The dependent power source: (a) schematic symbol, (b) i–v characteristic.

ber of common power-processing applications, including switch networks operating in the discontinuous conduction mode.

The power source characteristic illustrated in Fig. 11.5(b) is symmetrical with respect to voltage and current; in consequence, the power source exhibits several unique properties. Similar to the voltage source, the ideal power source must not be short-circuited; otherwise, infinite current occurs. And similar to the current source, the ideal power source must not be open-circuited, to avoid infinite terminal voltage. The power source must be connected to a load capable of absorbing the power $p(t)$, and the operating point is defined by the intersection of the load and power source i–v characteristics.

As illustrated in Fig. 11.6(a), series- and parallel-connected power sources can be combined

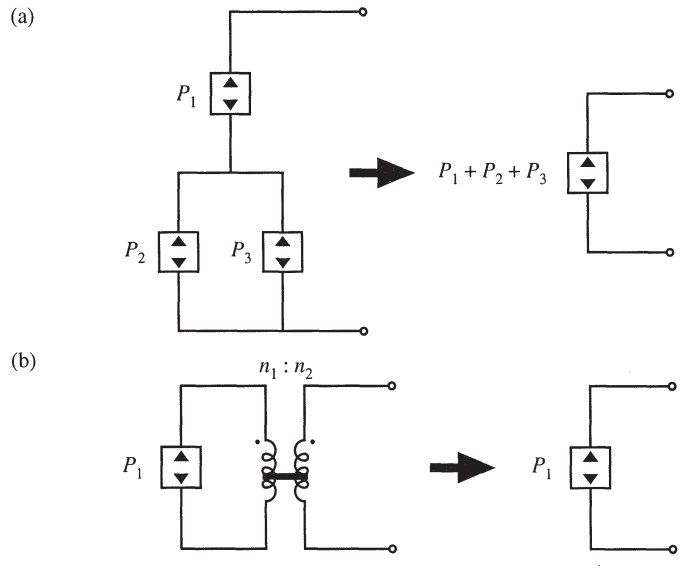


Fig. 11.6 Circuit manipulations of power source elements: (a) combination of series- and parallel- connected power sources into a single equivalent power source, (b) invariance of the power source to reflection through an ideal transformer of arbitrary turns ratio.

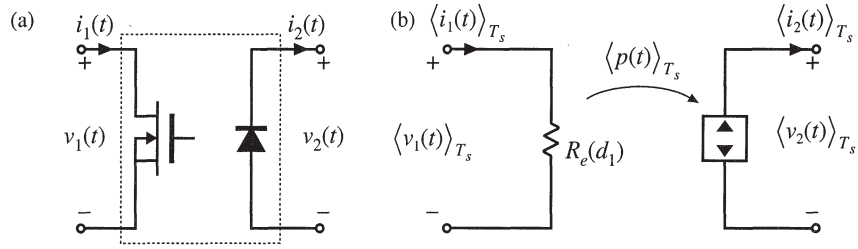


Fig. 11.7 (a) the general two-switch network, and (b) the corresponding averaged switch model in the discontinuous conduction mode: the average transistor waveforms obey Ohm's law, while the average diode waveforms behave as a dependent power source.

into a single power source, equal to the sum of the powers of the individual sources. Fig. 11.6(b) illustrates how reflection of a power source through a transformer, having an arbitrary turns ratio, leaves the power source unchanged. Power sources are also invariant to duality transformations.

The averaged large-signal model of the general two-switch network in DCM is illustrated in Fig. 11.7(b). The input port behaves effectively as resistance R_e. The instantaneous power apparently consumed by R_e is transferred to the output port, and the output port behaves as a dependent power source. This lossless two-port network is called the *loss-free resistor* model (LFR) [9]. The loss-free resistor represents the basic power conversion properties of DCM switch networks [11]. It can be shown that the loss-free resistor models the averaged properties of DCM switch networks not only in the buck-boost converter, but also in other PWM converters.

When the switch network of the DCM buck-boost converter is replaced by the averaged model of Fig. 11.7(b), the converter equivalent circuit of Fig. 11.8 is obtained. Upon setting all averaged waveforms to their quiescent values, and letting the inductor and capacitor become a short-circuit and an open-circuit, respectively, we obtain the dc model of Fig. 11.9.

Systems containing power sources or loss-free resistors can usually be easily solved, by equating average source and load powers. For example, in the dc network of Fig. 11.9, the power flowing into the converter input terminals is

$$P = \frac{V_g^2}{R_e} \tag{11.23}$$

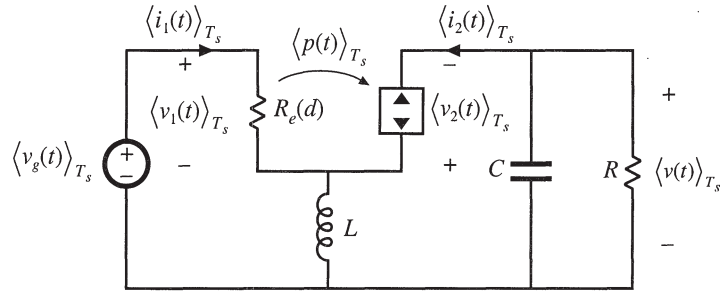


Fig. 11.8 Replacement of the switch network of the DCM buck-boost converter with the loss-free resistor model.

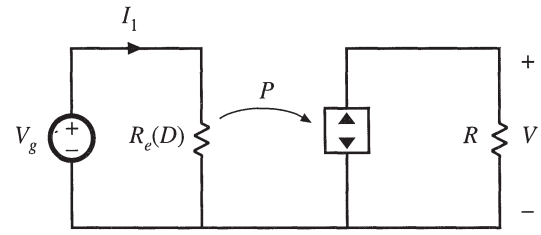


Fig. 11.9 Dc network example containing a loss-free resistor model.

The power flowing into the load resistor is

$$P = \frac{V^2}{R} \tag{11.24}$$

The loss-free resistor model states that these two powers must be equal:

$$P = \frac{V_g^2}{R_e} = \frac{V^2}{R} \tag{11.25}$$

Solution for the voltage conversion ratio $M = V/V_g$ yields

$$\frac{V}{V_g} = \pm\sqrt{\frac{R}{R_e}} \tag{11.26}$$

Equation (11.26) is a general result, valid for any converter that can be modeled by a loss-free resistor and that drives a resistive load. Other arguments must be used to determine the polarity of V/V_g. In the buck-boost converter shown in Fig. 11.2, the diode polarity indicates that V/V_g must be negative. The steady-state value of R_e is

$$R_e(D) = \frac{2L}{D^2 T_s} \tag{11.27}$$

where D is the quiescent transistor duty cycle. Substitution of Eq. (11.27) into (11.26) leads to

$$\frac{V}{V_g} = -\sqrt{\frac{D^2 T_s R}{2L}} = -\frac{D}{\sqrt{K}} \tag{11.28}$$

with $K = 2L/RT_s$. This equation coincides with the previous steady-state result given in Table 5.2.

Similar arguments apply when the waveforms contain ac components. For example, consider the network of Fig. 11.10, in which the voltages and currents are periodic functions of time. The rms val-

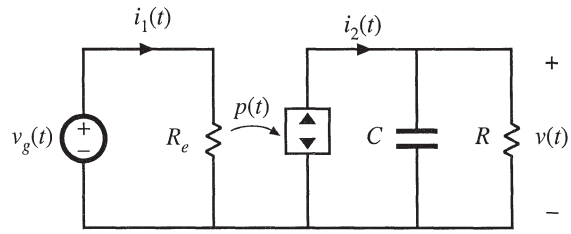


Fig. 11.10 Ac network example containing a loss-free resistor model.

ues of the waveforms can be determined by simply equating the average source and load powers. The average power flowing into the converter input port is

$$P_{av} = \frac{V_{g,rms}^2}{R_e} \tag{11.29}$$

where P_{av} is the average power consumed by the effective resistance R_e. No average power is consumed by capacitor C, and hence the average power P_{av} must flow entirely into the load resistor R:

$$P_{av} = \frac{V_{rms}^2}{R} \tag{11.30}$$

Upon equating Eqs. (11.29) and (11.30), we obtain

$$\frac{V_{rms}}{V_{g,rms}} = \sqrt{\frac{R}{R_e}} \tag{11.31}$$

Thus, the rms terminal voltages obey the same relationship as in the dc case.

Averaged equivalent circuits of the DCM buck, boost, and buck-boost converters, as well as the DCM Ćuk and SEPIC converters, are listed in Fig. 11.11. In each case, the averaged transistor waveforms obey Ohm's law, and are modeled by an effective resistance R_e. The averaged diode waveforms follow a power source characteristic, equal to the power effectively dissipated in R_e. For the buck, boost, and buck-boost converters, R_e is given by

$$R_e = \frac{2L}{d^2 T_s} \tag{11.32}$$

For the Ćuk and SEPIC converters, R_e is given by

$$R_e = \frac{2\left(L_1 \| L_2\right)}{d^2 T_s} \tag{11.33}$$

Here, d is the transistor duty cycle.

Steady-state conditions in the converters of Fig. 11.11 are found by letting the inductors and capacitors become short-circuits and open-circuits, respectively, and then solving the resulting dc circuits with $d(t) = D$. The buck-boost, Ćuk, and SEPIC then reduce to the circuit of Fig. 11.9. The buck and boost converters reduce to the circuits of Fig. 11.12. Equilibrium conversion ratios $M = V/V_g$ of these converters are summarized in Table 11.1, as functions of $R_e(D)$. It can be shown that these converters operate in the discontinuous conduction mode whenever the load current I is less than the critical current I_{crit}:

$$\begin{aligned} I &> I_{crit} \quad \text{for CCM} \\ I &< I_{crit} \quad \text{for DCM} \end{aligned} \tag{11.34}$$

For all of these converters, I_{crit} is given by

$$I_{crit} = \frac{1-D}{D} \frac{V_g}{R_e(D)} \tag{11.35}$$

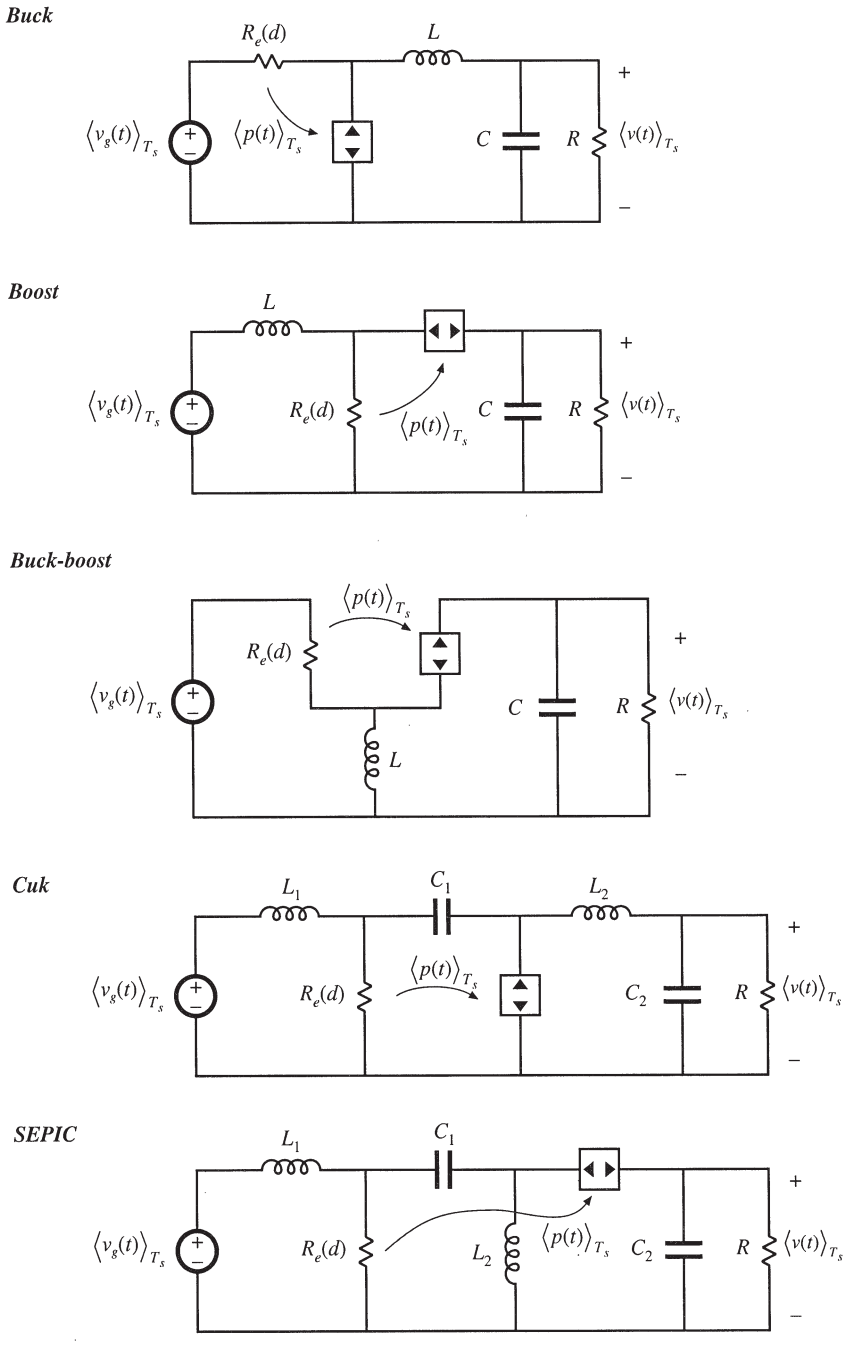


Fig. 11.11 Averaged large-signal equivalent circuits of five basic converters operating in the discontinuous conduction mode.

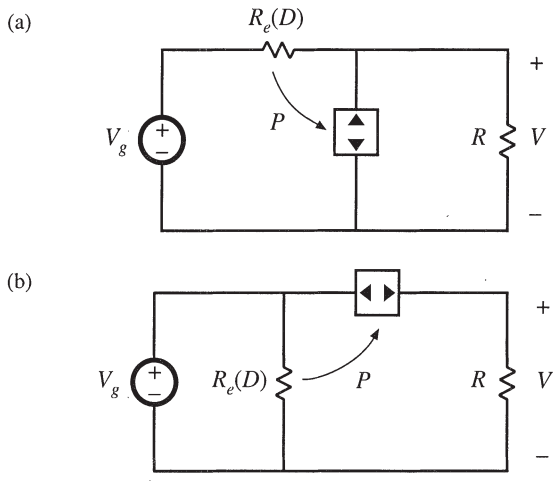


Fig. 11.12 Dc equivalent circuits representing the buck (a) and boost (b) converters operating in DCM.

Table 11.1 CCM and DCM conversion ratios of basic converters

Converter	*M*, CCM	*M*, DCM
Buck	D	$\frac{2}{1+\sqrt{1+4R_e/R}}$
Boost	$\frac{1}{1-D}$	$\frac{1+\sqrt{1+4R/R_e}}{2}$
Buck-boost, Ćuk	$\frac{-D}{1-D}$	$-\sqrt{\frac{R}{R_e}}$
SEPIC	$\frac{D}{1-D}$	$\sqrt{\frac{R}{R_e}}$

11.2 SMALL-SIGNAL AC MODELING OF THE DCM SWITCH NETWORK

The next step is construction of a small-signal equivalent circuit model for converters operating in the discontinuous conduction mode. In the large-signal ac equivalent circuits of Fig. 11.11, the averaged switch networks are nonlinear. Hence, construction of a small-signal ac model involves perturbation and linearization of the loss-free resistor network. The signals in the large-signal averaged DCM switch network model of Fig. 11.13(a) are perturbed about a quiescent operating point, as follows:

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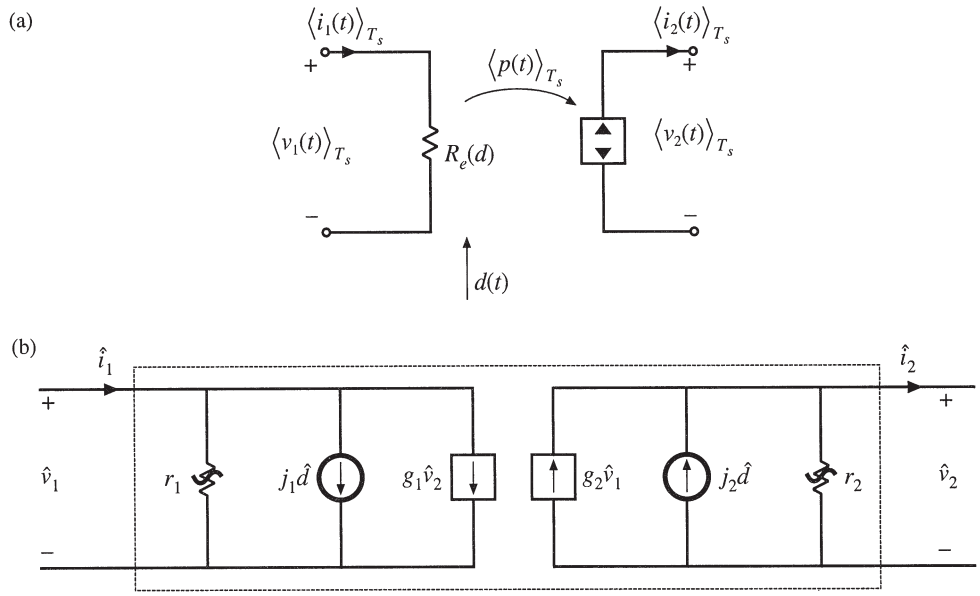


Fig. 11.13 Averaged models of the general two-switch network in a converter operating in DCM: (a) large-signal model, (b) small-signal model.

$$\begin{aligned} d(t) &= D + \hat{d}(t) \\ \langle v_1(t)\rangle_{T_s} &= V_1 + \hat{v}_1(t) \\ \langle i_1(t)\rangle_{T_s} &= I_1 + \hat{i}_1(t) \\ \langle v_2(t)\rangle_{T_s} &= V_2 + \hat{v}_2(t) \\ \langle i_2(t)\rangle_{T_s} &= I_2 + \hat{i}_2(t) \end{aligned} \tag{11.36}$$

Here, D is the quiescent value of the transistor duty cycle, V_1 is the quiescent value of the applied average transistor voltage $\langle v_1(t)\rangle_{T_s}$, etc. The quantities $\hat{d}(t)$, $\hat{v}_1(t)$, etc., are small ac variations about the respective quiescent values. It is desired to linearize the average switch network terminal equations (11.15) and (11.16).

Equations (11.15) and (11.16) express the average terminal currents $\langle i_1(t)\rangle_{T_s}$ and $\langle i_2(t)\rangle_{T_s}$ as functions of the transistor duty cycle $d(t) = d_1(t)$ and the average terminal voltages $\langle v_1(t)\rangle_{T_s}$ and $\langle v_2(t)\rangle_{T_s}$. Upon perturbation and linearization of these equations, we will therefore find that $\hat{i}_1(t)$ and $\hat{i}_2(t)$ are expressed as linear functions of $\hat{d}(t)$, $\hat{v}_1(t)$, and $\hat{v}_2(t)$. So the small-signal switch network equations can be written in the following form:

$$\begin{aligned} \hat{i}_1 &= \frac{\hat{v}_1}{r_1} + j_1\hat{d} + g_1\hat{v}_2 \\ \hat{i}_2 &= -\frac{\hat{v}_2}{r_2} + j_2\hat{d} + g_2\hat{v}_1 \end{aligned} \tag{11.37}$$

These equations describe the two-port equivalent circuit of Fig. 11.13(b).

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The parameters r_1, j_1, and g_1 can be found by Taylor expansion of Eq. (11.15), as described in Section 7.2.7. The average transistor current $\langle i_1(t)\rangle_{T_s}$, Eq. (11.15), can be expressed in the following form:

$$\langle i_1(t)\rangle_{T_s} = \frac{\langle v_1(t)\rangle_{T_s}}{R_e\big(d(t)\big)} = f_1\Big(\langle v_1(t)\rangle_{T_s}, \langle v_2(t)\rangle_{T_s}, d(t)\Big) \tag{11.38}$$

Let us expand this expression in a three-dimensional Taylor series, about the quiescent operating point (V_1, V_2, D):

$$\begin{aligned} I_1 + \hat{i}_1(t) = f_1\big(V_1, V_2, D\big) + \hat{v}_1(t)\left.\frac{\partial f_1\big(v_1, V_2, D\big)}{\partial v_1}\right|_{v_1 = V_1} \\ + \hat{v}_2(t)\left.\frac{\partial f_1\big(V_1, v_2, D\big)}{\partial v_2}\right|_{v_2 = V_2} + \hat{d}(t)\left.\frac{\partial f_1\big(V_1, V_2, d\big)}{\partial d}\right|_{d = D} \\ + \text{higher–order nonlinear terms} \end{aligned} \tag{11.39}$$

For simplicity of notation, the angle brackets denoting average values are dropped in the above equation. The dc terms on both sides of Eq. (11.39) must be equal:

$$I_1 = f_1\big(V_1, V_2, D\big) = \frac{V_1}{R_e(D)} \tag{11.40}$$

As usual, we linearize the equation by discarding the higher-order nonlinear terms. The remaining first-order linear ac terms on both sides of Eq. (11.39) are equated:

$$\hat{i}_1(t) = \hat{v}_1(t)\frac{1}{r_1} + \hat{v}_2(t)g_1 + \hat{d}(t)j_1 \tag{11.41}$$

where

$$\frac{1}{r_1} = \left.\frac{\partial f_1\big(v_1, V_2, D\big)}{\partial v_1}\right|_{v_1 = V_1} = \frac{1}{R_e(D)} \tag{11.42}$$

$$g_1 = \left.\frac{\partial f_1\big(V_1, v_2, D\big)}{\partial v_2}\right|_{v_2 = V_2} = 0 \tag{11.43}$$

$$\begin{aligned} j_1 &= \left.\frac{\partial f_1\big(V_1, V_2, d\big)}{\partial d}\right|_{d = D} = -\frac{V_1}{R_e^2(D)}\left.\frac{\partial R_e(d)}{\partial d}\right|_{d = D} \\ &= \frac{2V_1}{DR_e(D)} \end{aligned} \tag{11.44}$$

Thus, the small-signal input resistance r_1 is equal to the effective resistance R_e, evaluated at the quiescent operating point. This term describes how variations in $\langle v_1(t)\rangle_{T_s}$ affect $\langle i_1(t)\rangle_{T_s}$, via $R_e(D)$. The small-signal

parameter g_1 is equal to zero, since the average transistor current $\langle i_1(t)\rangle_{T_s}$ is independent of the average diode voltage $\langle v_2(t)\rangle_{T_s}$. The small-signal gain j_1 describes how duty cycle variations, which affect the value of $R_e(d)$, lead to variations in $\langle i_1(t)\rangle_{T_s}$.

In a similar manner, $\langle i_2(t)\rangle_{T_s}$ from Eq. (11.16) can be expressed as

$$\langle i_2(t)\rangle_{T_s} = \frac{\langle v_1(t)\rangle_{T_s}^2}{R_e(d(t))\langle v_2(t)\rangle_{T_s}} = f_2\left(\langle v_1(t)\rangle_{T_s}, \langle v_2(t)\rangle_{T_s}, d(t)\right) \tag{11.45}$$

Expansion of the function $f_2(v_1, v_2, d)$ in a three-dimensional Taylor series about the quiescent operating point leads to

$$\begin{aligned} I_2 + \hat{i}_2(t) = {} & f_2(V_1, V_2, D) + \hat{v}_1(t)\left.\frac{\partial f_2(v_1, V_2, D)}{\partial v_1}\right|_{v_1 = V_1} \\ & + \hat{v}_2(t)\left.\frac{\partial f_2(V_1, v_2, D)}{\partial v_2}\right|_{v_2 = V_2} + \hat{d}(t)\left.\frac{\partial f_2(V_1, V_2, d)}{\partial d}\right|_{d = D} \\ & + \text{higher–order nonlinear terms} \end{aligned} \tag{11.46}$$

By equating the dc terms on both sides of Eq. (11.46), we obtain

$$I_2 = f_2(V_1, V_2, D) = \frac{V_1^2}{R_e(D)V_2} \tag{11.47}$$

The higher-order nonlinear terms are discarded, leaving the following first-order linear ac terms:

$$\hat{i}_2(t) = \hat{v}_2(t)\left(-\frac{1}{r_2}\right) + \hat{v}_1(t)g_2 + \hat{d}(t)j_2 \tag{11.48}$$

with

$$\frac{1}{r_2} = -\left.\frac{\partial f_2(V_1, v_2, D)}{\partial v_2}\right|_{v_2 = V_2} = \frac{1}{R} = \frac{1}{M^2 R_e(D)} \tag{11.49}$$

$$g_2 = \left.\frac{\partial f_2(v_1, V_2, D)}{\partial v_1}\right|_{v_1 = V_1} = \frac{2}{MR_e(D)} \tag{11.50}$$

$$\begin{aligned} j_2 = {} & \left.\frac{\partial f_2(V_1, V_2, d)}{\partial d}\right|_{d = D} = -\frac{V_1^2}{R_e^2(D)V_2}\left.\frac{\partial R_e(d)}{\partial d}\right|_{d = D} \\ = {} & \frac{2V_1}{DMR_e(D)} \end{aligned} \tag{11.51}$$

The output resistance r_2 describes how variations in $\langle v_2(t)\rangle_{T_s}$ influence $\langle i_2(t)\rangle_{T_s}$. As illustrated in Fig. 11.14,

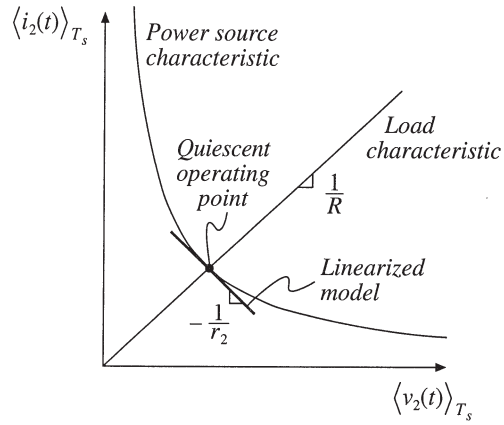


Fig. 11.14 The small-signal output resistance r_2 is determined by the slope of the power source characteristic at the quiescent operating point.

Table 11.2 Small-signal DCM switch model parameters

Switch network	g_1	j_1	r_1	g_2	j_2	r_2
General two-switch, Fig. 11.7(a)	0	$\frac{2V_1}{DR_e}$	R_e	$\frac{2}{MR_e}$	$\frac{2V_1}{DMR_e}$	M^2R_e
Buck, Fig. 11.16(a)	$\frac{1}{R_e}$	$\frac{2(1-M)V_1}{DR_e}$	R_e	$\frac{2-M}{MR_e}$	$\frac{2(1-M)V_1}{DMR_e}$	M^2R_e
Boost, Fig. 11.16(b)	$\frac{1}{(M-1)^2R_e}$	$\frac{2MV_1}{D(M-1)R_e}$	$\frac{(M-1)^2}{M^2}R_e$	$\frac{2M-1}{(M-1)^2R_e}$	$\frac{2V_1}{D(M-1)R_e}$	$(M-1)^2R_e$

r_2 is determined by the slope of the power source characteristic, evaluated at the quiescent operating point. For a linear resistive load, $r_2 = R$. For any type of load, it is true that $r_2 = M^2R_e(D)$. The parameters j_2 and g_2 describe how variations in the duty cycle $d(t)$ and in the average transistor voltage $\langle v_1(t) \rangle_{T_s}$ (which influence the average power $\langle p(t) \rangle_{T_s}$) lead to variations in the average diode current $\langle i_2(t) \rangle_{T_s}$. Values of the small-signal parameters in the DCM switch model of Fig. 11.13(b) are summarized in the top row of Table 11.2.

A small-signal model of the DCM buck-boost converter is obtained by replacing the transistor and diode of the converter with the switch model of Fig. 11.13(b). The result is illustrated in Fig. 11.15. This equivalent circuit can now be solved using conventional linear circuit analysis techniques, to determine the transfer functions and other small-signal quantities of interest.

The same small-signal switch model can be employed to model other DCM converters, by simply replacing the transistor and diode with ports 1 and 2, respectively, of the two-port model of Fig. 11.13(b). An alternative approach, which yields more convenient results in the analysis of the buck and boost converters, is to define the switch network as illustrated in Figs. 11.16(a) and 11.16(b), respectively. These switch networks can also be modeled using the two-port small-signal equivalent circuit of Fig. 11.16(c); however, new expressions for the parameters r_1, j_1, g_1, etc., must be derived. These expressions are again found by linearizing the equations of the averaged switch network terminal currents.

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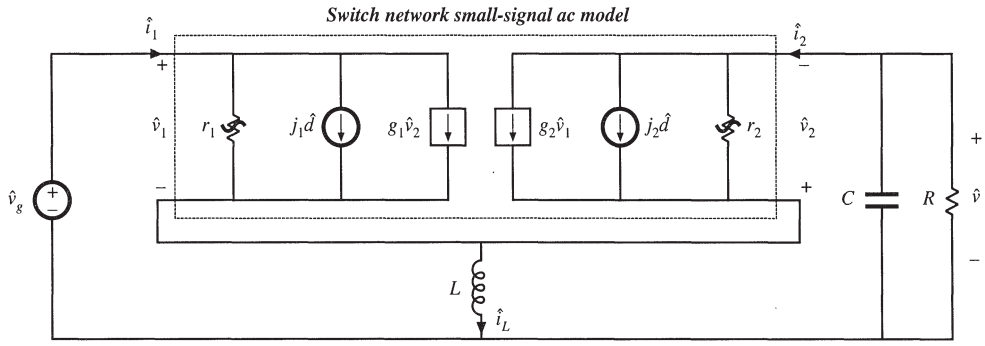


Fig. 11.15 Small-signal ac model of the DCM buck-boost converter obtained by insertion of the switch network two-port small-signal model into the original converter circuit.

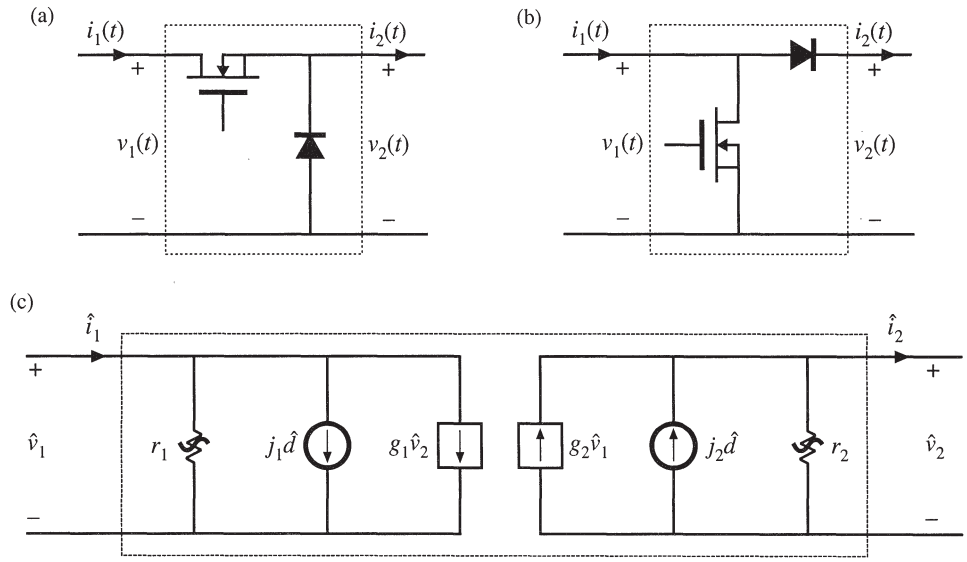


Fig. 11.16 A convenient way to model the switch networks of DCM buck and boost converters: (a) defined terminal quantities of the DCM buck switch network, (b) defined terminal quantities of the boost switch network, (c) two-port small-signal ac model. The model parameters are given in Table 11.2.

Table 11.2 lists the small-signal parameters for the buck switch network of Fig. 11.16(a) (middle row) and for the boost switch network of Fig. 11.16(b) (bottom row). Insertion of the small-signal two-port model into the DCM buck and boost converters leads to the equivalent circuits of Fig. 11.17.

The small-signal equivalent circuit models of Fig. 11.15 and Fig. 11.17 contain two dynamic elements: capacitor C and inductor L. Control-to-output transfer functions obtained by solving these equivalent circuit models have two poles. It has been shown [2-6] that one of the poles, due to the capacitor C, appears at a low frequency, while the other pole (and a RHP zero in the case of boost and buck-

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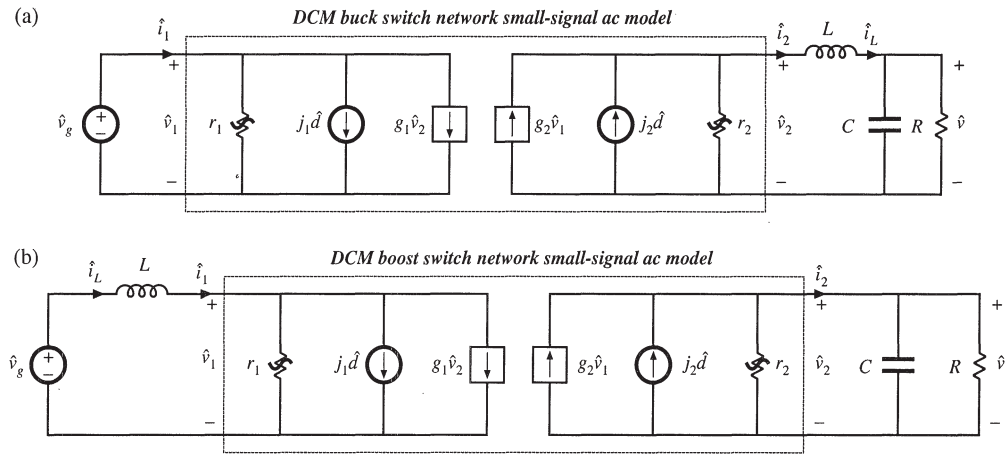


Fig. 11.17 Small-signal ac models of (a) the DCM buck converter, and (b) the DCM boost converter, obtained by replacing the switch networks defined in Fig. 11.16(a) and (b) with the small-signal switch model of Fig. 11.16(c).

boost converters) due to the inductor L, occurs at much higher frequency, close to the converter switching frequency. Therefore, in practice, the DCM buck, boost, and buck-boost converters exhibit essentially single-pole transfer functions, which are negligibly influenced by the inductor dynamics.

The small-signal equivalent circuit models have been derived in this section from the large-signal averaged switch network equations (11.15) and (11.16). These equations are based on Eq. (11.11), which states that the average inductor voltage, and therefore its small-signal ac voltage, is zero. This contradicts predictions of the resulting small-signal models in Figs. 11.15 and 11.17. As a result, we expect that the models derived in this section can be used to predict low-frequency dynamics, while predictions of the high-frequency dynamics due to the inductor L are of questionable validity. Equivalent circuit models that give more accurate predictions of high-frequency dynamics of DCM converters are discussed in Section 11.3.

A simple approximate way to determine the low-frequency small-signal transfer functions of the buck, boost, and buck-boost converters is to let the inductance L tend to zero. If L is shorted in the equivalent circuits of Figs. 11.15 and 11.17, the model in all three cases reduces to Fig. 11.18. This cir-

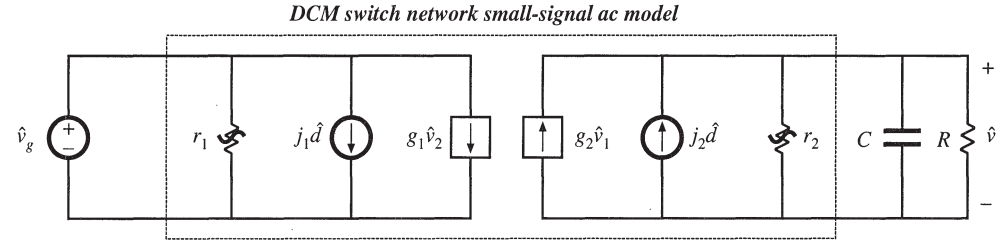


Fig. 11.18 Low-frequency ac model obtained by letting L approach zero. The buck, boost, or buck-boost converters can be modeled, by employing the appropriate parameters from Table 11.2.

cuit is relatively easy to solve.

The control-to-output transfer function $G_{vd}(s)$ is found by letting $\hat{v}_g = 0$ in Fig. 11.18. Solution for $\hat{v}$ then leads to

$$G_{vd}(s) = \left.\frac{\hat{v}}{\hat{d}}\right|_{\hat{v}_g = 0} = \frac{G_{d0}}{1 + \frac{s}{\omega_p}} \tag{11.52}$$

with

$$\begin{aligned} G_{d0} &= j_2\left(R \| r_2\right) \\ \omega_p &= \frac{1}{\left(R \| r_2\right) C} \end{aligned} \tag{11.53}$$

The line-to-output transfer function $G_{vg}(s)$ is found by letting $\hat{d} = 0$ in Fig. 11.18. One then obtains

$$G_{vg}(s) = \left.\frac{\hat{v}}{\hat{v}_g}\right|_{\hat{d} = 0} = \frac{G_{g0}}{1 + \frac{s}{\omega_p}} \tag{11.54}$$

with

$$G_{g0} = g_2\left(R \| r_2\right) = M \tag{11.55}$$

Expressions for G_{d0}, G_{g0}, and ω_p are listed in Table 11.3, for the DCM buck, boost, and buck-boost converters with resistive loads [12,13].

The ac modeling approach described in this section is both general and useful. The transistor and diode of a DCM converter can be simply replaced by the two-port network of Fig. 11.13(b), leading to the small-signal ac model. Alternatively, the switch network can be defined as in Fig. 11.16(a) or 11.16(b), and then modeled by the same two-port network, Fig. 11.16(c). The small-signal converter model can then be solved via conventional circuit analysis techniques, to obtain the small-signal transfer functions of the converter.

Table 11.3 Salient features of DCM converter small-signal transfer functions

Converter	G_{d0}	G_{g0}	ω_p
Buck	$\frac{2V}{D}\frac{1-M}{2-M}$	M	$\frac{2-M}{(1-M)RC}$
Boost	$\frac{2V}{D}\frac{M-1}{2M-1}$	M	$\frac{2M-1}{(M-1)RC}$
Buck–boost	$\frac{V}{D}$	M	$\frac{2}{RC}$

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11.2.1 Example: Control-to-Output Frequency Response of a DCM Boost Converter

As a simple numerical example, let us find the small-signal control-to-output transfer function of a DCM boost converter having the following element and parameter values:

$$\begin{aligned} R &= 12\ \Omega \\ L &= 5\ \mu\text{H} \\ C &= 470\ \mu\text{F} \\ f_s &= 100\ \text{kHz} \end{aligned} \tag{11.56}$$

The output voltage is regulated to be $V = 36$ V. It is desired to determine $G_{vd}(s)$ at the operating point where the load current is $I = 3$ A and the dc input voltage is $V_g = 24$ V.

The effective resistance $R_e(D)$ is found by solution of the dc equivalent circuit of Fig. 11.12(b). Since the load current I and the input and output voltages V and V_g are known, the power source value P is

$$P = I\left(V - V_g\right) = \left(3\ \text{A}\right)\left(36\ \text{V} - 24\ \text{V}\right) = 36\ \text{W} \tag{11.57}$$

The effective resistance is therefore

$$R_e = \frac{V_g^2}{P} = \frac{(24\ \text{V})^2}{36\ \text{W}} = 16\ \Omega \tag{11.58}$$

The steady-state duty cycle D can now be found using Eq. (11.32):

$$D = \sqrt{\frac{2L}{R_e T_s}} = \sqrt{\frac{2(5\ \mu\text{H})}{(16\ \Omega)(10\ \mu\text{s})}} = 0.25 \tag{11.59}$$

The expressions given in Table 11.3 for G_{d0} and ω_p of the boost converter can now be evaluated:

$$\begin{aligned} G_{d0} &= \frac{2V}{D}\,\frac{M-1}{2M-1} = \frac{2(36\ \text{V})}{(0.25)}\,\frac{\left(\dfrac{(36\ \text{V})}{(24\ \text{V})} - 1\right)}{\left(2\dfrac{(36\ \text{V})}{(24\ \text{V})} - 1\right)} = 72\ \text{V} \Rightarrow 37\ \text{dBV} \\ f_p &= \frac{\omega_p}{2\pi} = \frac{2M-1}{2\pi(M-1)RC} = \frac{\left(2\dfrac{(36\ \text{V})}{(24\ \text{V})} - 1\right)}{2\pi\left(\dfrac{(36\ \text{V})}{(24\ \text{V})} - 1\right)(12\ \Omega)(470\ \mu\text{F})} = 112\ \text{Hz} \end{aligned} \tag{11.60}$$

A Bode diagram of the control-to-output transfer function is constructed in Fig. 11.19. The solid lines illustrate the magnitude and phase predicted by the approximate single-pole model of Fig. 11.18. The dashed lines are the predictions of the more accurate model discussed in Section 11.3, which include a second pole at $f_2 = 64$ kHz and a RHP zero at $f_z = 127$ kHz, arising from the inductor dynamics. Since the switching frequency is 100 kHz, the accuracy of the model at these frequencies cannot be guaranteed. Nonetheless, in practice, the lagging phase asymptotes arising from the inductor dynamics can be

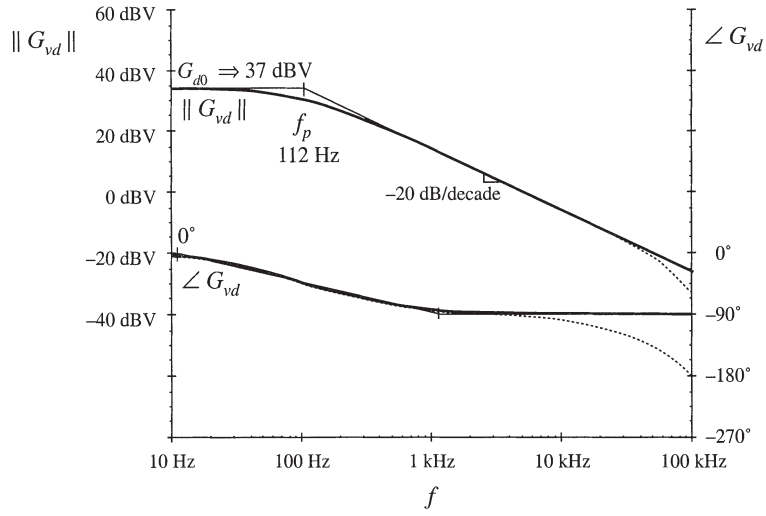


Fig. 11.19 Magnitude and phase of the control-to-output transfer function, DCM boost example. Solid lines: function and its asymptotes, approximate single-pole response predicted by the model of Fig. 11.18. Dashed lines: more accurate response that includes high-frequency inductor dynamics.

observed beginning at $f_2/10 = 6.4$ kHz.

11.2.2 Example: Control-to-Output Frequency Responses of a CCM/DCM SEPIC

As another example, consider the SEPIC of Fig. 11.20. According to Eq. (11.34), this converter operates in CCM if

$$\frac{V}{R} > \frac{1-D}{D}\frac{V_g}{R_e(D)} \tag{11.61}$$

where $R_e(D)$ is given by Eq. (11.33). Upon neglecting losses in the converter, one finds that the CCM conversion ratio is

$$\frac{V}{V_g} \approx \frac{D}{1-D} \tag{11.62}$$

When Eqs. (11.33) and (11.62) are substituted into Eq. (11.61), the condition for operation in CCM becomes:

$$R < \frac{2\left(L_1 \| L_2\right)}{(1-D)^2 T_s} = 46\ \Omega \tag{11.63}$$

The converter control-to-output frequency responses are generated using Spice ac simulations. Details of

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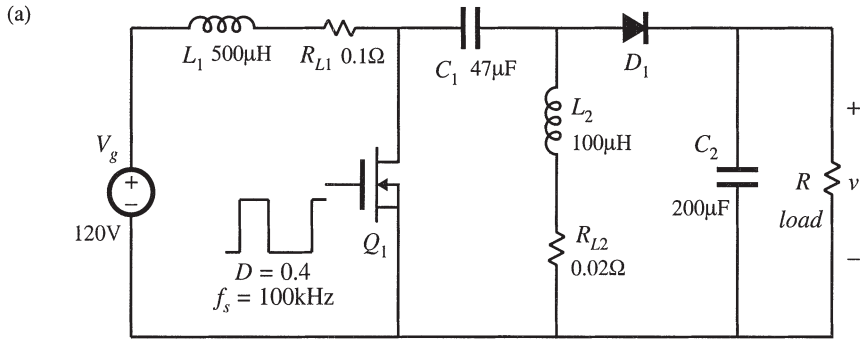


Fig. 11.20 SEPIC example.

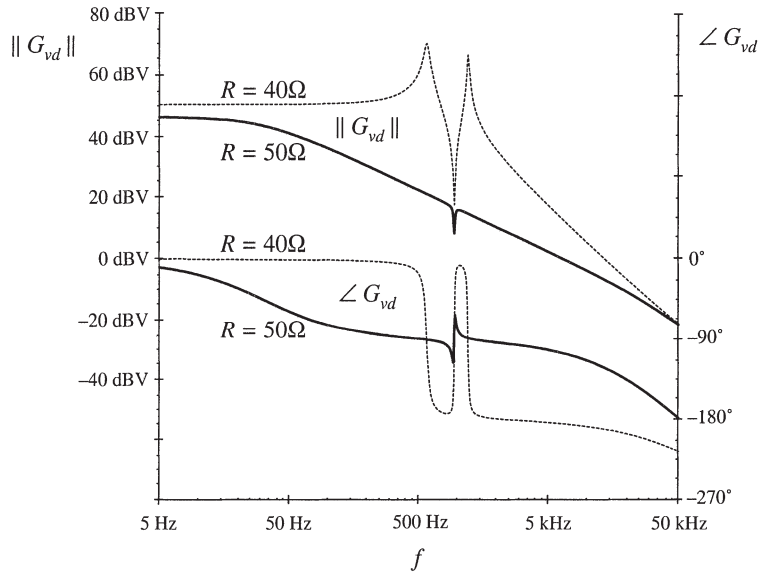


Fig. 11.21 Magnitude and phase of the control-to-output transfer function obtained by simulation of the SEPIC example shown in Fig. 11.20, for two values of the load resistance: $R = 50\Omega$ when the converter operates in DCM (solid lines), and $R = 40\Omega$ for which the converter operates in CCM (dashed lines).

the simulation setup are described in Appendix B, Section B.2.1. Figure 11.21 shows magnitude and phase responses of the control-to-output transfer function obtained for two different values of the load resistance: $R = 40\ \Omega$, for which the converter operates in CCM, and $R = 50\ \Omega$, for which the converter operates in DCM. For these two operating points, the quiescent (dc) voltages and currents in the circuit are nearly the same. Nevertheless, the frequency responses are qualitatively very different in the two operating modes. In CCM, the converter exhibits a fourth-order response with two pairs of high-Q complex-conjugate poles and a pair of complex-conjugate zeros. Another RHP (right-half plane) zero can be observed at frequencies approaching 50 kHz. In DCM, there is a dominant low-frequency pole followed

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by a pair of complex-conjugate poles and a pair of complex-conjugate zeros. The frequencies of the complex poles and zeros are very close in value. A high-frequency pole and a RHP zero contribute additional phase lag at higher frequencies.

11.3 HIGH-FREQUENCY DYNAMICS OF CONVERTERS IN DCM

As discussed in Section 11.2, transfer functions of converters operating in discontinuous conduction mode exhibit a dominant low-frequency pole. A pole and possibly a zero caused by inductor dynamics, are pushed to high frequencies. To correctly model the high-frequency dynamics of DCM converters, one must account for the fact that the ac voltage across the inductor is not zero. Equation (11.12) is employed in Section 11.1 to greatly simplify the equations of the DCM averaged switch model. Although this model gives good results at low frequencies, it cannot accurately predict high frequency inductor dynamics because it implies that the ac inductor voltage is zero.

A more accurate approach is employed in this section. The subinterval length d_2 is found by averaging the inductor current waveform $i_L(t)$ of Fig. 11.3 [4-6]:

$$\left\langle i_L(t)\right\rangle_{T_s} = \frac{1}{2} i_{pk}\Big(d(t) + d_2(t)\Big) = \frac{d(t)\Big(d(t) + d_2(t)\Big)T_s}{2L}\left\langle v_g(t)\right\rangle_{T_s} \tag{11.64}$$

Solution for $d_2(t)$ yields:

$$d_2(t) = \frac{2L\left\langle i_L(t)\right\rangle_{T_s}}{d(t)T_s\left\langle v_g(t)\right\rangle_{T_s}} - d(t) = \left(\frac{R_e(d)\left\langle i_L(t)\right\rangle_{T_s}}{\left\langle v_g(t)\right\rangle_{T_s}} - 1\right) d(t) \tag{11.65}$$

Equation (11.65), together with Eqs. (11.3), (11.4), (11.7), and (11.10), constitutes a large-signal averaged model in DCM that can be used to investigate steady-state behavior, as well as low-frequency and high-frequency dynamics. Unfortunately, the model equations are more involved, and do not allow elimination of all converter voltages and currents in terms of the switch network average terminal waveforms.

Let us use this model to find predictions for the high-frequency pole caused by the inductor dynamics of DCM converters. Consider the buck-boost converter of Fig. 11.2 having the DCM waveforms shown in Fig. 11.3. The average transistor voltage $\langle v_1(t)\rangle_{T_s}$ and the average diode current $\langle i_2(t)\rangle_{T_s}$ are selected as the switch network dependent variables. Substitution of Eq. (11.65) into Eq. (11.3) yields

$$\left\langle v_1(t)\right\rangle_{T_s} = \Big(1 - d(t)\Big)\left\langle v_g(t)\right\rangle_{T_s} + d(t)\left\langle v(t)\right\rangle_{T_s} - \frac{R_e(d)\left\langle i_L(t)\right\rangle_{T_s}\left\langle v(t)\right\rangle_{T_s} d(t)}{\left\langle v_g(t)\right\rangle_{T_s}} \tag{11.66}$$

The averaged switch voltage $\langle v_1(t)\rangle_{T_s}$ in Eq. (11.66) is a nonlinear function of the switch duty cycle, the average inductor current, and the average input and output voltages:

$$\left\langle v_1(t)\right\rangle_{T_s} = \gamma_1\left(\left\langle v_g(t)\right\rangle_{T_s}, \left\langle v(t)\right\rangle_{T_s}, \left\langle i_L(t)\right\rangle_{T_s}, d(t)\right) \tag{11.67}$$

A small-signal ac model can be obtained by Taylor expansion of Eq. (11.67). The small-signal ac component $\hat{v}_1$ of the average switch voltage can be found as:

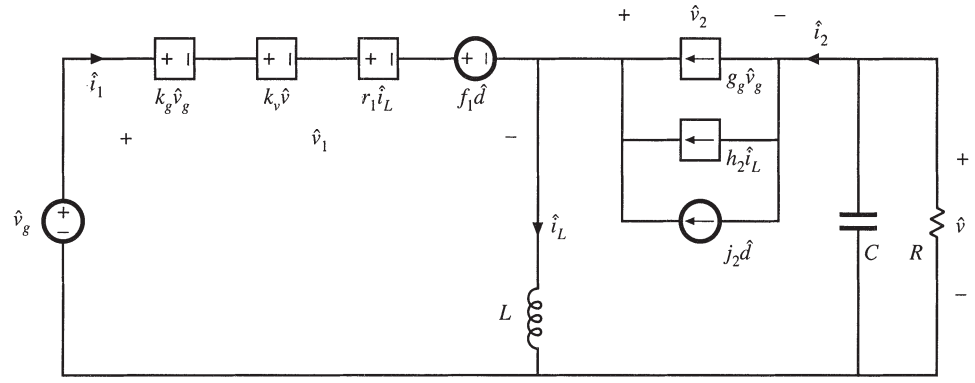


Fig. 11.22 A small-signal ac model of the DCM buck-boost converter.

$$\hat{v}_1(t) = \hat{v}_g(t)k_g + \hat{v}(t)k_v + \hat{i}_L r_1 + \hat{d}(t)f_1 \tag{11.68}$$

where the small-signal model parameters k_g, k_v, r_1, and f_1 are computed as partial derivatives of γ_1 evaluated at the quiescent operating point. In particular,

$$r_1 = \left.\frac{\partial \gamma_1\left(V_g, V, i_L, D\right)}{\partial i_L}\right|_{i_L = I_L} = -\frac{V}{V_g}R_e D \tag{11.69}$$

Substitution of Eq. (11.65) into Eq. (11.10) yields

$$\left\langle i_2(t)\right\rangle_{T_s} = \left\langle i_L(t)\right\rangle_{T_s} - \frac{\left\langle v_g(t)\right\rangle_{T_s}}{R_e} = \gamma_2\left(\left\langle v_g(t)\right\rangle_{T_s}, \left\langle i_L(t)\right\rangle_{T_s}, d(t)\right) \tag{11.70}$$

The small-signal ac component $\hat{i}_2$ of the average diode current can be found as:

$$\hat{i}_2(t) = \hat{v}_g(t)g_g + \hat{i}_L h_2 + \hat{d}(t)j_2 \tag{11.71}$$

where the small-signal model parameters g_g, h_2, and j_2 are computed as partial derivatives of γ_2 evaluated at the quiescent operating point. Figure 11.22 shows the small-signal ac model of the buck-boost converter, where the transistor and the diode switch are replaced by the sources specified by Eqs. (11.68) and (11.71), respectively. It can be shown that this model predicts essentially the same low-frequency dynamics as the model derived in Section 11.2.

To find the control-to-output transfer function, we set $\hat{v}_g = 0$. At high frequencies, the small-signal ac component of the capacitor voltage is very small, $\hat{v} \approx 0$. Therefore, the contribution of the dependent source $k_v\hat{v}$ can be neglected at high frequencies. Then, from the equivalent circuit model of Fig. 11.22, we have

$$sL\hat{i}_L + r_1\hat{i}_L + f_1\hat{d} = 0 \tag{11.72}$$

Equation (11.72) can be solved for the control-to-inductor current transfer function at high frequencies:

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$$\frac{\hat{i}_L}{\hat{d}} = -\frac{f_1}{r_1}\frac{1}{1+\frac{s}{\omega_2}} \tag{11.73}$$

where the pole frequency f_2 is given by

$$f_2 = \frac{\omega_2}{2\pi} = \frac{r_1}{2\pi L} \tag{11.74}$$

To simplify the expression for the pole frequency f_2, we use the steady-state relationship that follows from Eq. (11.12):

$$-\frac{V}{V_g} = \frac{D}{D_2} \tag{11.75}$$

Also, recall that the steady-state equivalent resistance $R_e(D)$ can be written as

$$R_e = \frac{2Lf_s}{D^2} \tag{11.76}$$

where f_s is the switching frequency. Upon substitution of Eqs. (11.69), (11.75) and (11.76) into Eq. (11.74) we get:

$$f_2 = \frac{f_s}{\pi D_2} \tag{11.77}$$

This is an expression for the frequency f_2 of the high-frequency pole that is caused by the inductor dynamics of the DCM buck-boost converter. It can be shown that Eq. (11.77) is a general result for the high-frequency pole, valid for all basic converters operating in DCM. Since $0 < D_2 < 1$, Eq. (11.77) implies that the high-frequency pole is always greater than approximately one third of the switching frequency.

Table 11.4 summarizes the expressions for the high-frequency pole ω_2 and the RHP zero ω_z caused by the inductor dynamics in control-to-output transfer functions $G_{vd}(s)$ of basic DCM converters [6]. The high-frequency pole and the RHP zero occur at frequencies close to or exceeding the switching frequency f_s. This is why, in practice, the high-frequency inductor dynamics can usually be neglected.

Table 11.4 High-frequency pole and RHP zero of the DCM converter control-to-output transfer function $G_{vd}(s)$

Converter	High-frequency pole ω_2	RHP zero ω_z
Buck	$\frac{2Mf_s}{D(1-M)}$	none
Boost	$\frac{2(M-1)f_s}{D}$	$\frac{2f_s}{D}$
Buck–boost	$\frac{2\lvert M\rvert f_s}{D}$	$\frac{2f_s}{D}$

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11.4 SUMMARY OF KEY POINTS

1. In the discontinuous conduction mode, the average transistor voltage and current are proportional, and hence obey Ohm's law. An averaged equivalent circuit can be obtained by replacing the transistor with an effective resistor $R_e(d)$. The average diode voltage and current obey a power source characteristic, with power equal to the power effectively dissipated by R_e. In the averaged equivalent circuit, the diode is replaced with a dependent power source.
2. The two-port lossless network consisting of an effective resistor and power source, which results from averaging the transistor and diode waveforms of DCM converters, is called a loss-free resistor. This network models the basic power-processing functions of DCM converters, much in the same way that the ideal dc transformer models the basic functions of CCM converters.
3. The large-signal averaged model can be solved under equilibrium conditions to determine the quiescent values of the converter currents and voltages. Average power arguments can often be used.
4. A small-signal ac model for the DCM switch network can be derived by perturbing and linearizing the loss-free resistor network. The result has the form of a two-port *y*-parameter model. The model describes the small-signal variations in the transistor and diode currents, as functions of variations in the duty cycle and in the transistor and diode ac voltage variations.
5. To simplify the ac analysis of the DCM buck and boost converters, it is convenient to define two other forms of the small-signal switch model, corresponding to the switch networks of Figs. 11.16(a) and 11.16(b). These models are also *y*-parameter two-port models, but have different parameter values.
6. The inductor dynamics of the DCM buck, boost, and buck-boost converters occur at high frequency, above or just below the switching frequency. Hence, in most cases the high frequency inductor dynamics can be ignored. In the small-signal ac model, the inductance L is set to zero, and the remaining model is solved relatively easily for the low-frequency converter dynamics. The DCM buck, boost, and buck-boost converters exhibit transfer functions containing essentially a single low-frequency dominant pole.
7. To obtain a more accurate model of the inductor dynamics in DCM, it is necessary to write the equations of the averaged inductor waveforms in a way that does not assume that the average inductor voltage is zero.

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PROBLEMS

11.1 Averaged switch modeling of a flyback converter. The converter of Fig. 11.23 operates in the discontinuous conduction mode. The two-winding inductor has a 1:n turns ratio and negligible leakage inductance, and can be modeled as an ideal transformer in parallel with primary-side magnetizing inductance L_p.

(a) Sketch the transistor and diode voltage and current waveforms, and derive expressions for their average values.

(b) Sketch an averaged model for the converter that includes a loss-free resistor network, and give an expression for $R_e(d)$.

(c) Solve your model to determine the voltage ratio V/V_g in the discontinuous conduction mode.

(d) Over what range of load current I is your answer of part (c) valid? Express the DCM boundary in the form $I < I_{crit}(D, R_e, V_g, n)$.

(e) Derive an expression for the small-signal control-to-output transfer function $G_{vd}(s)$. You may neglect inductor dynamics.

11.2 Averaged switch modeling of a nonisolated Watkins-Johnson converter. The converter of Fig. 11.24 operates in the discontinuous conduction mode. The two-winding inductor has a 1:1 turns ratio and negligible leakage inductance, and can be modeled as an ideal transformer in parallel with magnetizing inductance L.

(a) Sketch the transistor and diode voltage and current waveforms, and derive expressions for their average values.

(b) Sketch an averaged model for the converter that includes a loss-free resistor network, and give an expression for $R_e(d)$.

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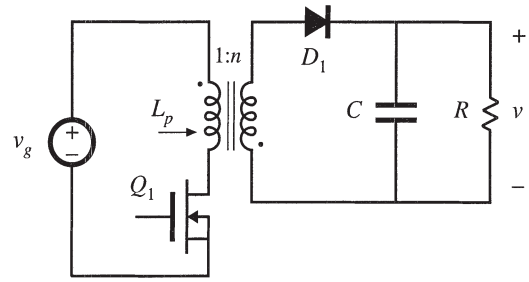


Fig. 11.23 Flyback converter, Problem 11.1.

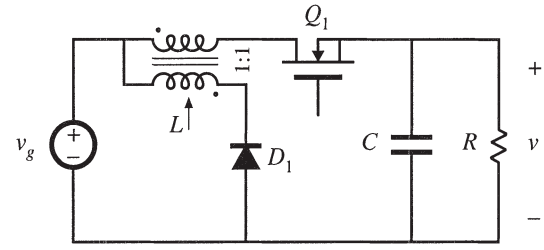


Fig. 11.24 Watkins-Johnson converter, Problem 11.2.

(c) Solve your model to determine the converter conversion ratio $M(D) = V/V_g$ in the discontinuous conduction mode. Over what range of load currents is your expression valid?

11.3 Sketch the steady-state output characteristics of the buck-boost converter: plot the output voltage V vs. the load current I, for several values of duty cycle D. Include both CCM and DCM operation, and clearly label the boundary between modes.

11.4 In the network of Fig. 11.25, the power source waveform $p(t)$ is given by

$$p(t) = 1000 \cos^2 377t$$

The circuit operates in steady state. Determine the rms resistor voltage $V_{R,rms}$.

11.5 Verify the expressions for G_{d0} and ω_p given in Table 11.3.

11.6 A certain buck converter operates with an input voltage of $V_g = 28$ V and an output voltage of $V = 15$ V. The load resistance is $R = 10\Omega$. Other element and parameter values are: $L = 8\mu H$, $C = 220\mu F$, $f_s = 150$kHz.

(a) Determine the value of R_e.

(b) Determine the quiescent duty cycle D.

(c) Sketch a Bode plot of the control-to-output transfer function $G_{vd}(s)$. Label the values of all salient features. You may neglect inductor dynamics.

11.7 Using the approach of Section 11.3, determine the control-to-output transfer function $G_{vd}(s)$ of a boost converter. Do not make the approximation $L \approx 0$.

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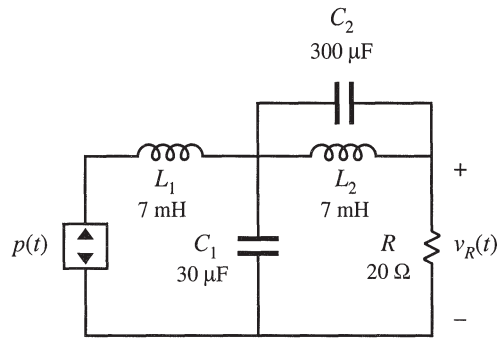


Fig. 11.25 Network with a power source, Problem 11.4.

(a) Derive analytical expressions for the dc gain G_{d0} and the RHP zero frequency ω_z, as functions of M, R_e, D, V_g, L, C, and R.

(b) With the assumption that C is sufficiently large and that L is sufficiently small, the poles of $G_{vd}(s)$ can be factored using the low-Q approximation. Do so, and express the two poles as functions of M, D, L, C, and R. Show that the low-frequency pole matches the expression in Table 11.3, and that the high-frequency pole is given by the expression in Table 11.4.

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12

Current Programmed Control

So far, we have discussed duty ratio control of PWM converters, in which the converter output is controlled by direct choice of the duty ratio $d(t)$. We have therefore developed expressions and small-signal transfer functions that relate the converter waveforms and output voltage to the duty ratio.

Another control scheme, which finds wide application, is current programmed control [1–13], in which the converter output is controlled by choice of the peak transistor switch current peak($i_s(t)$). The control input signal is a current $i_c(t)$, and a simple control network switches the transistor on and off, such that the peak transistor current follows $i_c(t)$. The transistor duty cycle $d(t)$ is not directly controlled, but depends on $i_c(t)$ as well as on the converter inductor currents, capacitor voltages, and power input voltage. Converters controlled via current programming are said to operate in the *current programmed mode* (CPM).

The block diagram of a simple current programmed controller is illustrated in Fig. 12.1. Control signal $i_c(t)$ and switch current $i_s(t)$ waveforms are given in Fig. 12.2. A clock pulse at the Set input of a latch initiates the switching period, causing the latch output Q to be high and turning on the transistor. While the transistor conducts, its current $i_s(t)$ is equal to the inductor current $i_L(t)$; this current increases with some positive slope m_1 that depends on the value of inductance and the converter voltages. In more complicated converters, $i_s(t)$ may follow the sum of several inductor currents. Eventually, the switch current $i_s(t)$ becomes equal to the control signal $i_c(t)$. At this point, the controller turns the transistor switch off, and the inductor current decreases for the remainder of the switching period. The controller must measure the switch current $i_s(t)$ with some current sensor circuit, and compare $i_s(t)$ to $i_c(t)$ using an analog comparator. In practice, voltages proportional to $i_s(t)$ and $i_c(t)$ are compared, with constant of proportionality R_f. When $i_s(t) \geq i_c(t)$, the comparator resets the latch, turning the transistor off for the remainder of the switching period.

As usual, a feedback loop can be constructed for regulation of the output voltage. The output voltage $v(t)$ is compared to a reference voltage v_{ref}, to generate an error signal. This error signal is applied

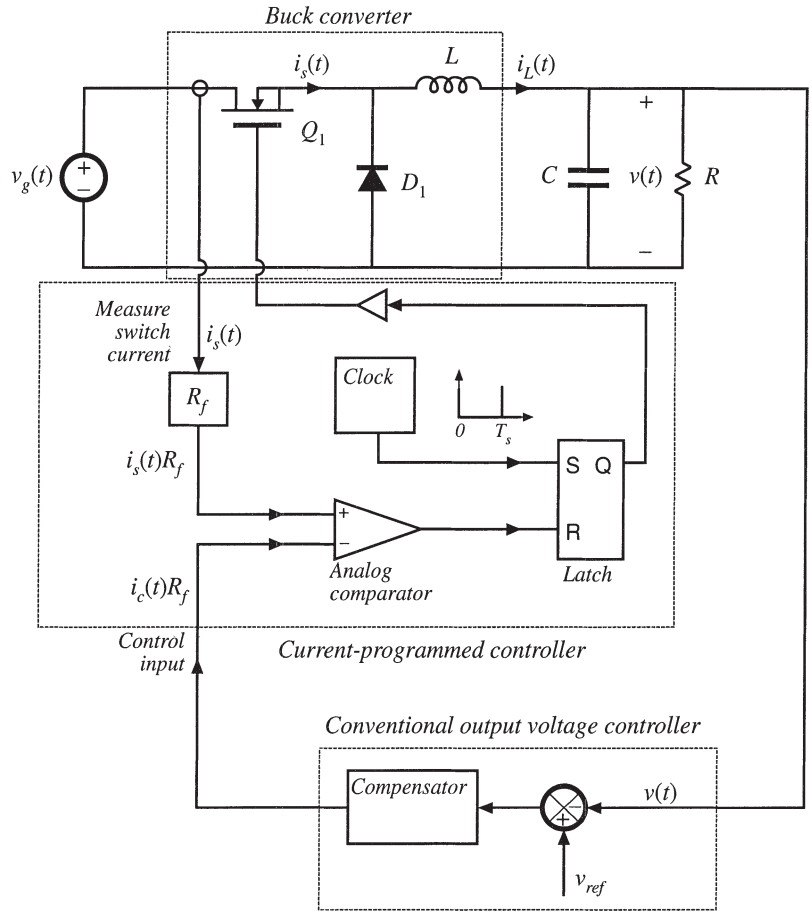


Fig. 12.1 Current-programmed control of a buck converter. The peak transistor current replaces the duty cycle as the control input.

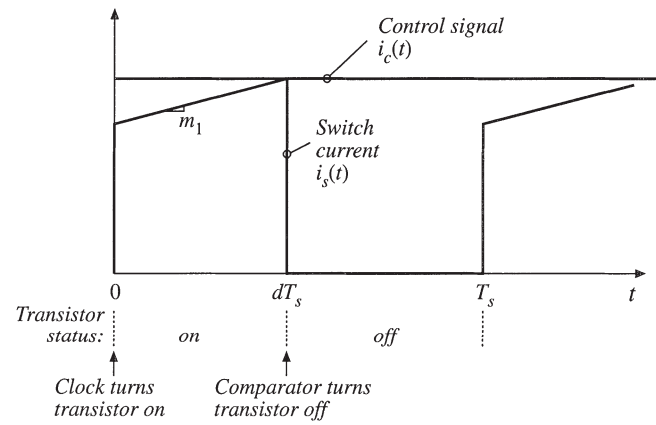


Fig. 12.2 Switch current $i_s(t)$ and control input $i_c(t)$ waveforms, for the current-programmed system ofFig. 12.1.

to the input of a compensation network, and the output of the compensator drives the control signal $i_c(t)R_f$. To design such a feedback system, we need to model how variations in the control signal $i_c(t)$ and in the line input voltage $v_g(t)$ affect the output voltage $v(t)$.

The chief advantage of the current programmed mode is its simpler dynamics. To first order, the small-signal control-to-output transfer function $\hat{v}(s)/\hat{i}_c(s)$ contains one less pole than $\hat{v}(s)/\hat{d}(s)$. Actually, this pole is moved to a high frequency, near the converter switching frequency. Nonetheless, simple robust wide-bandwidth output voltage control can usually be obtained, without the use of compensator lead networks. It is true that the current programmed controller requires a circuit for measurement of the switch current $i_s(t)$; however, in practice such a circuit is also required in duty ratio controlled systems, for protection of the transistor against excessive currents during transients and fault conditions. Current programmed control makes use of the available current sensor information during normal operation of the converter, to obtain simpler system dynamics. Transistor failures due to excessive switch current can then be prevented simply by limiting the maximum value of $i_c(t)$. This ensures that the transistor will turn off whenever the switch current becomes too large, on a cycle-by-cycle basis.

An added benefit is the reduction or elimination of transformer saturation problems in full-bridge or push–pull isolated converters. In these converters, small voltage imbalances induce a dc bias in the transformer magnetizing current; if sufficiently large, this dc bias can saturate the transformer. The dc current bias increases or decreases the transistor switch currents. In response, the current programmed controller alters the transistor duty cycles, such that transformer volt-second balance tends to be maintained. Current-programmed full-bridge isolated buck converters should be operated without a capacitor in series with the transformer primary winding; this capacitor tends to destabilize the system. For the same reason, current-programmed control of half-bridge isolated buck converters is generally avoided.

A disadvantage of current programmed control is its susceptibility to noise in the $i_s(t)$ or $i_c(t)$ signals. This noise can prematurely reset the latch, disrupting the operation of the controller. In particular, a small amount of filtering of the sensed switch current waveform is necessary, to remove the turn-on current spike caused by the diode stored charge. Addition of an artificial ramp to the current-programmed controller, as discussed in Section 12.1, can also improve the noise immunity of the circuit.

Commercial integrated circuits that implement current programmed control are widely available, and operation of converters in the current programmed mode is quite popular. In this chapter, converters operating in the current programmed mode are modeled. In Section 12.1, the stability of the current programmed controller and its inner switch-current-sensing loop is examined. It is found that this controller is unstable whenever converter steady-state duty cycle D is greater than 0.5. The current programmed controller can be stabilized by addition of an artificial ramp signal to the sensed switch current waveform. In Section 12.2, the system small-signal transfer functions are described, using a simple first-order model. The averaged terminal waveforms of the switch network can be described by a simple current source, in conjunction with a power source element. Perturbation and linearization leads to a simple small-signal model. Although this first-order model yields a great deal of insight into the control-to-output transfer function and converter output impedance, it does not predict the line-to-output transfer function $G_{vg}(s)$ of current-programmed buck converters. Hence, the model is refined in Section 12.3. Section 12.4 extends the modeling of current programmed converters to the discontinuous conduction mode.

12.1 OSCILLATION FOR $D > 0.5$

The current programmed controller of Fig. 12.1 is unstable whenever the steady-state duty cycle is greater than 0.5. To avoid this stability problem, the control scheme is usually modified, by addition of an artificial ramp to the sensed switch current waveform. In this section, the stability of the current programmed controller, with its inner switch-current-sensing loop, is analyzed. The effects of the addition of

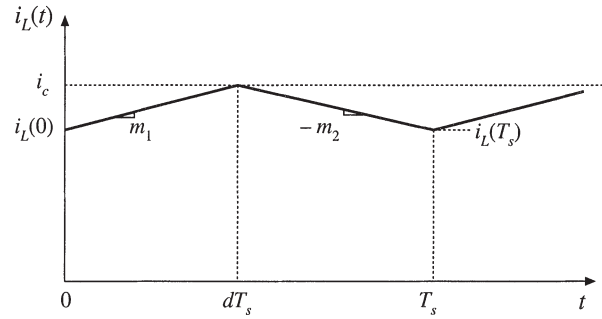


Fig. 12.3 Inductor current waveform of a current-programmed converter operating in the continuous conduction mode.

the artificial ramp are explained, using a simple first-order discrete-time analysis. Effects of the artificial ramp on controller noise susceptibility is also discussed.

Figure 12.3 illustrates a generic inductor current waveform of a switching converter operating in the continuous conduction mode. The inductor current changes with a slope m_1 during the first subinterval, and a slope $-m_2$ during the second subinterval. For the basic nonisolated converters, the slopes m_1 and $-m_2$ are given by

Buck converter

$$m_1 = \frac{v_g - v}{L} \qquad -m_2 = -\frac{v}{L}$$

Boost converter

$$m_1 = \frac{v_g}{L} \qquad -m_2 = \frac{v_g - v}{L} \tag{12.1}$$

Buck–boost converter

$$m_1 = \frac{v_g}{L} \qquad -m_2 = \frac{v}{L}$$

With knowledge of the slopes m_1 and $-m_2$, we can determine the general relationships between $i_L(0)$, i_c, $i_L(T_s)$, and dT_s.

During the first subinterval, the inductor current $i_L(t)$ increases with slope m_1, until $i_L(t)$ reaches the control signal i_c. Hence,

$$i_L(dT_s) = i_c = i_L(0) + m_1 dT_s \tag{12.2}$$

Solution for the duty cycle d leads to

$$d = \frac{i_c - i_L(0)}{m_1 T_s} \tag{12.3}$$

In a similar manner, for the second subinterval we can write

$$\begin{aligned} i_L(T_s) &= i_L(dT_s) - m_2 d'T_s \\ &= i_L(0) + m_1 dT_s - m_2 d'T_s \end{aligned} \tag{12.4}$$

In steady-state, $i_L(0) = i_L(T_s)$, $d = D$, $m_1 = M_1$, and $m_2 = M_2$. Insertion of these relationships into Eq. (12.4) yields

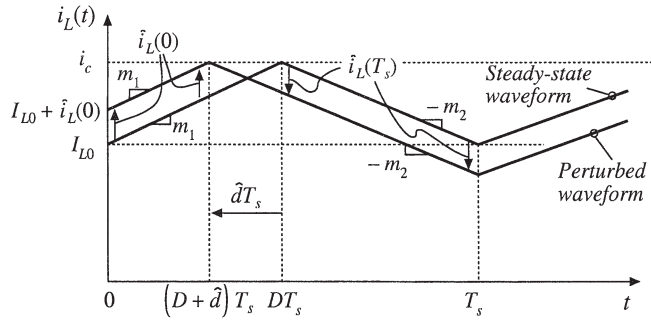


Fig. 12.4 Effect of initial perturbation $\hat{i}_L(0)$ on inductor current waveform.

$$0 = M_1 DT_s - M_2 D'T_s \tag{12.5}$$

Or,

$$\frac{M_2}{M_1} = \frac{D}{D'} \tag{12.6}$$

Steady-state Eq. (12.6) coincides with the requirement for steady-state volt-second balance on the inductor.

Consider now a small perturbation in $i_L(0)$:

$$i_L(0) = I_{L0} + \hat{i}_L(0) \tag{12.7}$$

I_{L0} is a steady-state value of $i_L(0)$, which satisfies Eqs. (12.4) and (12.5), while $\hat{i}_L(0)$ is a small perturbation such that

$$\left|\hat{i}_L(0)\right| \ll \left|I_{L0}\right| \tag{12.8}$$

It is desired to assess the stability of the current-programmed controller, by determining whether this small perturbation eventually decays to zero. To do so, let us solve for the perturbation after n switching periods, $\hat{i}_L(nT_s)$, and determine whether $\hat{i}_L(nT_s)$ tends to zero for large n.

The steady-state and perturbed inductor current waveforms are illustrated in Fig. 12.4. For clarity, the size of the inductor current perturbation $\hat{i}_L(0)$ is exaggerated. It is assumed that the converter operates near steady-state, such that the slopes m_1 and m_2 are essentially unchanged. Figure 12.4 is drawn for a positive $\hat{i}_L(0)$; the quantity $\hat{d}T_s$ is then negative. Since the slopes of the steady-state and perturbed waveforms are essentially equal over the interval $0 < t < (D + \hat{d})T_s$, the difference between the waveforms is equal to $\hat{i}_L(0)$ for this entire interval. Likewise, the difference between the two waveforms is a constant $\hat{i}_L(T_s)$ over the interval $DT_s < t < T_s$, since both waveforms then have the slope $-m_2$. Note that $\hat{i}_L(T_s)$ is a negative quantity, as sketched in Fig. 12.4. Hence, we can solve for $\hat{i}_L(T_s)$ in terms of $\hat{i}_L(0)$, by considering only the interval $(D + \hat{d})T_s < t < DT_s$ as illustrated in Fig. 12.5.

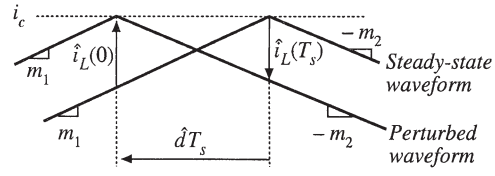


Fig. 12.5 Expanded view of the steady-state and perturbed inductor current waveforms, near the peak of $i_L(t)$.

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From Fig. 12.5, we can use the steady-state waveform to express $\hat{i}_L(0)$ as the slope m_1, multiplied by the interval length $-\hat{d}T_s$. Hence,

$$\hat{i}_L(0) = -m_1 \hat{d} T_s \tag{12.9}$$

Likewise, we can use the perturbed waveform to express $\hat{i}_L(T_s)$ as the slope $-m_2$, multiplied by the interval length $-\hat{d}T_s$:

$$\hat{i}_L(T_s) = m_2 \hat{d} T_s \tag{12.10}$$

Elimination of the intermediate variable $\hat{d}$ from Eqs. (12.9) and (12.10) leads to

$$\hat{i}_L(T_s) = \hat{i}_L(0) \left(-\frac{m_2}{m_1} \right) \tag{12.11}$$

If the converter operating point is sufficiently close to the quiescent operating point, then m_2/m_1 is given approximately by Eq. (12.6). Equation (12.11) then becomes

$$\hat{i}_L(T_s) = \hat{i}_L(0) \left(-\frac{D}{D'} \right) \tag{12.12}$$

A similar analysis can be performed during the next switching period, to show that

$$\hat{i}_L(2T_s) = \hat{i}_L(T_s) \left(-\frac{D}{D'} \right) = \hat{i}_L(0) \left(-\frac{D}{D'} \right)^2 \tag{12.13}$$

After n switching periods, the perturbation becomes

$$\hat{i}_L(nT_s) = \hat{i}_L((n-1)T_s) \left(-\frac{D}{D'} \right) = \hat{i}_L(0) \left(-\frac{D}{D'} \right)^n \tag{12.14}$$

Note that, as n tends to infinity, the perturbation $\hat{i}_L(nT_s)$ tends to zero provided that the characteristic value $-D/D'$ has magnitude less than one. Conversely, the perturbation $\hat{i}_L(nT_s)$ becomes large in magnitude when the characteristic value $\alpha = -D/D'$ has magnitude greater than one:

$$\left| \hat{i}_L(nT_s) \right| \rightarrow \begin{cases} 0 & \text{when } \left| -\frac{D}{D'} \right| < 1 \\ \infty & \text{when } \left| -\frac{D}{D'} \right| > 1 \end{cases} \tag{12.15}$$

Therefore, for stable operation of the current programmed controller, we need $|\alpha| = D/D' < 1$, or

$$D < 0.5 \tag{12.16}$$

As an example, consider the operation of the boost converter with the steady-state terminal voltages $V_g = 20$ V, $V = 50$ V. Since $V/V_g = 1/D'$, the boost converter should operate with $D = 0.6$. We therefore expect the current programmed controller to be unstable. The characteristic value will be

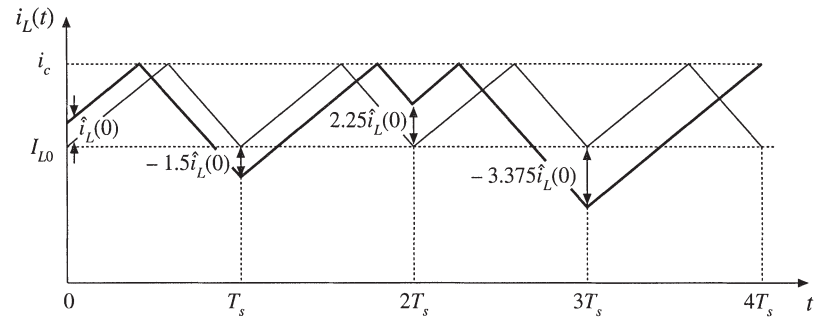


Fig. 12.6 Unstable oscillation for $D = 0.6$.

$$\alpha = -\frac{D}{D'} = \left(-\frac{0.6}{0.4}\right) = -1.5 \tag{12.17}$$

As given by Eq. (12.14), a perturbation in the inductor current will increase by a factor of – 1.5 over every switching period. As illustrated in Fig. 12.6, the perturbation grows to $-1.5\hat{i}_L(0)$ after one switching period, to $+2.25\hat{i}_L(0)$ after two switching periods, and to $-3.375\hat{i}_L(0)$ after three switching periods. For the particular initial conditions illustrated in Fig. 12.6, this growing oscillation saturates the current programmed controller after three switching periods. The transistor remains on for the entire duration of the fourth switching period. The inductor current and controller waveforms may eventually become oscillatory and periodic in nature, with period equal to an integral number of switching periods. Alternatively, the waveforms may become chaotic. In either event, the controller does not operate as intended.

Figure 12.7 illustrates the inductor current waveforms when the output voltage is decreased to $V = 30$ V. The boost converter then operates with $D = 1/3$, and the characteristic value becomes

$$\alpha = -\frac{D}{D'} = \left(-\frac{1/3}{2/3}\right) = -0.5 \tag{12.18}$$

Perturbations now decrease in magnitude by a factor of 0.5 over each switching period. A disturbance in the inductor current becomes small in magnitude after a few switching periods.

The instability for $D > 0.5$ is a well-known problem of current programmed control, which is not dependent on the converter topology. The controller can be rendered stable for all duty cycles by addition of an artificial ramp to the sensed switch current waveform, as illustrated in Fig. 12.8. This arti-

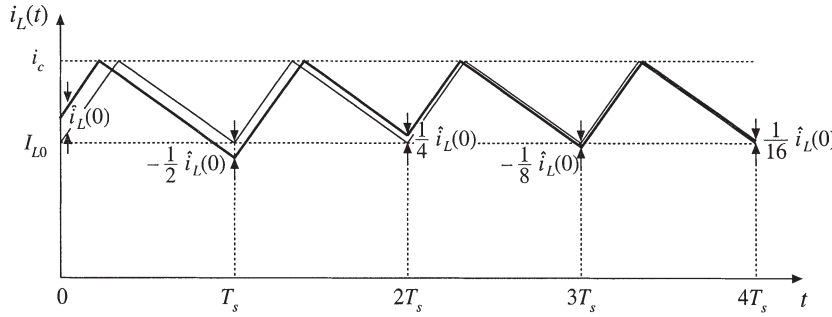


Fig. 12.7 A stable transient with $D = 1/3$.

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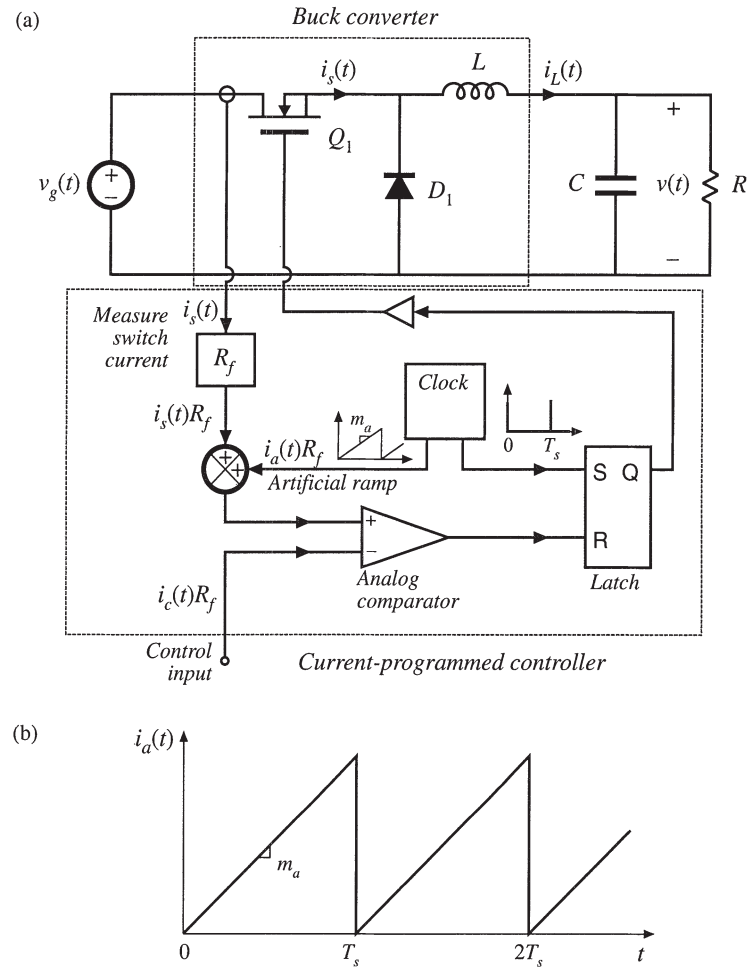


Fig. 12.8 Stabilization of the current programmed controller by addition of an artificial ramp to the measured switch current waveform: (a) block diagram, (b) artificial ramp waveform.

ficial ramp has the qualitative effect of reducing the gain of the inner switch-current-sensing discrete feedback loop. The artificial ramp has slope m_a as shown. The controller now switches the transistor off when

$$i_a(dT_s) + i_L(dT_s) = i_c \tag{12.19}$$

where $i_a(t)$ is the artificial ramp waveform. Therefore, the transistor is switched off when the inductor current $i_L(t)$ is given by

$$i_L(dT_s) = i_c - i_a(dT_s) \tag{12.20}$$

Figure 12.9 illustrates the analog comparison of the inductor current waveform $i_L(t)$ with the quantity $[i_c - i_a(t)]$.

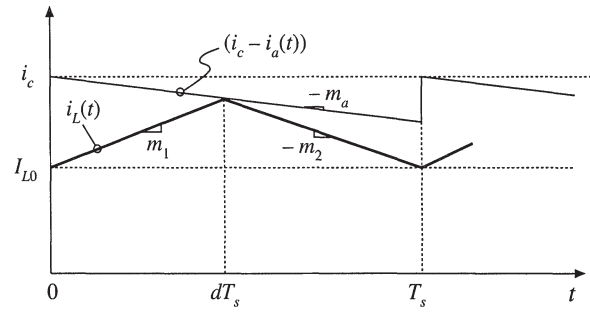


Fig. 12.9 Addition of artificial ramp: the transistor is now switched off when $i_L(t) = i_c - i_a(t)$.

We can again determine the stability of the current programmed controller by analyzing the change in a perturbation of the inductor current waveform over a complete switching period. Figure 12.10 illustrates steady-state and perturbed inductor current waveforms, in the presence of the artificial ramp. Again, the magnitude of the perturbation $\hat{i}_L(0)$ is exaggerated. The perturbed waveform is sketched for a positive value of $\hat{i}_L(0)$; this causes $\hat{d}$, and usually also $\hat{i}_L(T_s)$, to be negative. If the perturbed waveforms are sufficiently close to the quiescent operating point, then the slopes m_1 and m_2 are essentially unchanged, and the relationship between $\hat{i}_L(0)$ and $\hat{i}_L(T_s)$ can be determined solely by consideration of the interval $(D + \hat{d})T_s < t < DT_s$. The perturbations $\hat{i}_L(0)$ and $\hat{i}_L(T_s)$ are expressed in terms of the slopes m_1, m_2, and m_a, and the interval length $-\hat{d}T_s$, as follows:

$$\hat{i}_L(0) = -\hat{d}T_s\left(m_1 + m_a\right) \tag{12.21}$$

$$\hat{i}_L(T_s) = -\hat{d}T_s\left(m_a - m_2\right) \tag{12.22}$$

Elimination of $\hat{d}$ yields

$$\hat{i}_L(T_s) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right) \tag{12.23}$$

A similar analysis can be applied to the n^{th} switching period, leading to

$$\hat{i}_L(nT_s) = \hat{i}_L((n-1)T_s)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right)^n = \hat{i}_L(0)\,\alpha^n \tag{12.24}$$

The evolution of inductor current perturbations are now determined by the characteristic value

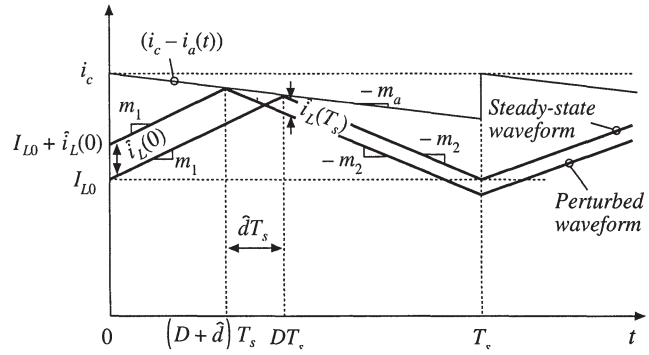


Fig. 12.10 Steady-state and perturbed inductor current waveforms, in the presence of an artificial ramp.

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$$\alpha = -\frac{m_2 - m_a}{m_1 + m_a} \tag{12.25}$$

For large n, the perturbation magnitude tends to

$$\left| \hat{i}_L(nT_s) \right| \rightarrow \begin{cases} 0 & \text{when } |\alpha| < 1 \\ \infty & \text{when } |\alpha| > 1 \end{cases} \tag{12.26}$$

Therefore, for stability of the current programmed controller, we need to choose the slope of the artificial ramp m_a such that the characteristic value α has magnitude less than one. The artificial ramp gives us an additional degree of freedom, which we can use to stabilize the system for duty cycles greater than 0.5. Note that increasing the value of m_a causes the numerator of Eq. (12.25) to decrease, while the denominator increases. Therefore, the characteristic value α attains magnitude less than one for sufficiently large m_a.

In the conventional voltage regulator application, the output voltage $v(t)$ is well regulated by the converter control system, while the input voltage $v_g(t)$ is unknown. Equation (12.1) then predicts that the value of the slope m_2 is constant and known with a high degree of accuracy, for the buck and buck-boost converters. Therefore, let us use Eq. (12.6) to eliminate the slope m_1 from Eq. (12.25), and thereby express the characteristic value α as a function of the known slope m_2 and the steady-state duty cycle D:

$$\alpha = -\frac{1 - \frac{m_a}{m_2}}{\frac{D'}{D} + \frac{m_a}{m_2}} \tag{12.27}$$

One common choice of artificial ramp slope is

$$m_a = \tfrac{1}{2} m_2 \tag{12.28}$$

It can be verified, by substitution of Eq. (12.28) into (12.27), that this choice leads to $\alpha = -1$ at $D = 1$, and to $|\alpha| < 1$ for $0 \leq D < 1$. This is the minimum value of m_a that leads to stability for all duty cycles. We will see in Section 12.3 that this choice of m_a has the added benefit of causing the ideal line-to-output transfer function $G_{vg}(s)$ of the buck converter to become zero.

Another common choice of m_a is

$$m_a = m_2 \tag{12.29}$$

This causes the characteristic value α to become zero for all D. As a result, $\hat{i}_L(T_s)$ is zero for any $\hat{i}_L(0)$ that does not saturate the controller. The system removes any error after one switching period T_s. This behavior is known as *deadbeat control*, or *finite settling time*.

It should be noted that the above stability analysis employs a quasi-static approximation, in which the slopes m_1 and m_2 of the perturbed inductor current waveforms are assumed to be identical to the steady-state case. In the most general case, the stability and transient response of a complete system employing current programmed control must be assessed using a system-wide discrete time or sampled-data analysis. Nonetheless, in practice the above arguments are found to be sufficient for selection of the artificial ramp slope m_a.

Current-programmed controller circuits exhibit significant sensitivity to noise. The reason for this is illustrated in Fig. 12.11(a), in which the control signal $i_c(t)$ is perturbed by a small amount of noise

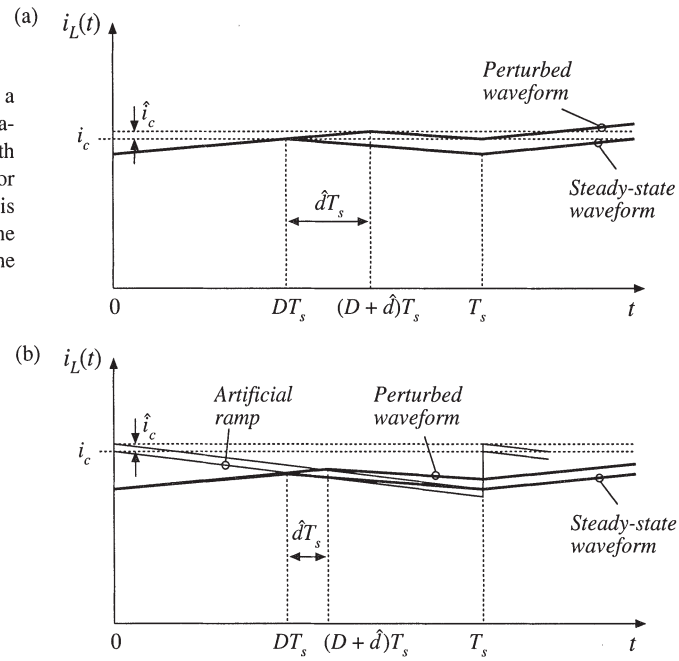


Fig. 12.11 When noise perturbs a controller signal such as i_c, a perturbation in the duty cycle results: (a) with no artificial ramp and small inductor current ripple, the perturbation $\hat{d}$ is large; (b) an artificial ramp reduces the controller gain, thereby reducing the perturbation $\hat{d}$.

represented by $\hat{i}_c$. It can be seen that, when there is no artificial ramp and when the inductor current ripple is small, then a small perturbation in i_c leads to a large perturbation in the duty cycle: the controller has high gain. When noise is present in the controller circuit, then significant jitter in the duty cycle waveforms may be observed. A solution is to reduce the gain of the controller by introduction of an artificial ramp. As illustrated in Fig. 12.11(b), the same perturbation in i_c now leads to a reduced variation in the duty cycle. When the layout and grounding of the controller circuit introduce significant noise into the duty cycle waveform, it may be necessary to add an artificial ramp whose amplitude is substantially greater than the inductor current ripple.

12.2 A SIMPLE FIRST-ORDER MODEL

Once the current programmed controller has been constructed, and stabilized using an artificial ramp, then it is desired to design a feedback loop for regulation of the output voltage. As usual, this voltage feedback loop must be designed to meet specifications regarding line disturbance rejection, transient response, output impedance, etc. A block diagram of a typical system is illustrated in Fig. 12.12, containing an inner current programmed controller, with an outer voltage feedback loop.

To design the outer voltage feedback loop, an ac equivalent circuit model of the switching converter operating in the current programmed mode is needed. In Chapter 7, averaging was employed to develop small-signal ac equivalent circuit models for converters operating with duty ratio control. These models predict the circuit behavior in terms of variations d in the duty cycle. If we could find the relationship between the control signal $i_c(t)$ and the duty cycle $d(t)$ for the current programmed controller, then we could adapt the models of Chapter 7, to apply to the current programmed mode as well. In general, the duty cycle depends not only on $i_c(t)$, but also on the converter voltages and currents; hence, the current programmed controller incorporates multiple effective feedback loops as indicated in Fig. 12.12.

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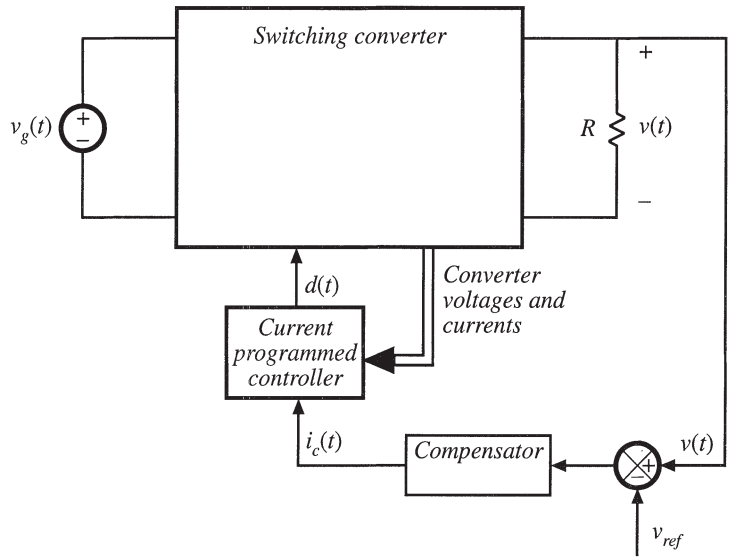


Fig. 12.12 Block diagram of a converter system incorporating current programmed control.

In this section, the averaging approach is extended, as described above, to treat current programmed converters. A simple first-order approximation is employed, in which it is assumed that the current programmed controller operates ideally, and hence causes the average inductor current $\langle i_L(t) \rangle_{T_s}$ to be identical to the control $i_c(t)$. This approximation is justified whenever the inductor current ripple and artificial ramp have negligible magnitudes. The inductor current then is no longer an independent state of the system, and no longer contributes a pole to the converter small-signal transfer functions.

This first-order model is derived in Section 12.2.1, using a simple algebraic approach. In Section 12.2.2, a simple physical interpretation is obtained via the averaged switch modeling technique. A more accurate, but more complicated, model is described in Section 12.3.

12.2.1 Simple Model via Algebraic Approach: Buck-Boost Example

The power stage of a simple buck-boost converter operating in the continuous conduction mode is illustrated in Fig. 12.13(a), and its inductor current waveform is given in Fig. 12.13(b). The small-signal averaged equations for this converter, under duty cycle control, were derived in Section 7.2. The result, Eq. (7.43), is reproduced below:

$$\begin{aligned} L\frac{d\hat{i}_L(t)}{dt} &= D\hat{v}_g(t) + D'\hat{v}(t) + \left(V_g - V\right)\hat{d}(t) \\ C\frac{d\hat{v}(t)}{dt} &= -D'\hat{i}_L - \frac{\hat{v}(t)}{R} + I_L\hat{d}(t) \\ \hat{i}_g(t) &= D\hat{i}_L + I_L\hat{d}(t) \end{aligned} \tag{12.30}$$

The Laplace transforms of these equations, with initial conditions set to zero, are

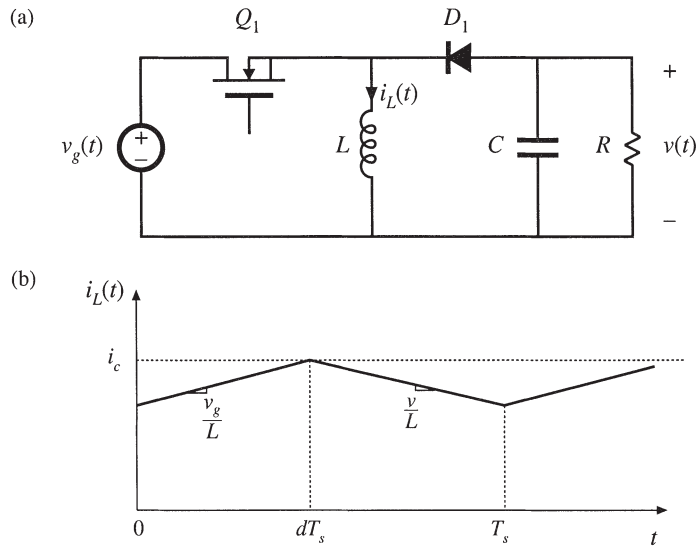


Fig. 12.13 Buck-boost converter example: (a) power stage, (b) inductor current waveform.

$$\begin{aligned} sL\hat{i}_L(s) &= D\hat{v}_g(s) + D'\hat{v}(s) + \left(V_g - V\right)\hat{d}(s) \\ sC\hat{v}(s) &= -D'\hat{i}_L(s) - \frac{\hat{v}(s)}{R} + I_L\hat{d}(s) \\ \hat{i}_g(s) &= D\hat{i}_L(s) + I_L\hat{d}(s) \end{aligned} \tag{12.31}$$

We now make the assumption that the inductor current $\hat{i}_L(s)$ is identical to the programmed control current $\hat{i}_c(s)$. This is valid to the extent that the controller is stable, and that the magnitudes of the inductor current ripple and artificial ramp waveform are sufficiently small:

$$\hat{i}_L(s) \approx \hat{i}_c(s) \tag{12.32}$$

This approximation, in conjunction with the inductor current equation of (12.31), can now be used to find the relationship between the control current $\hat{i}_c(s)$ and the duty cycle $\hat{d}(s)$, as follows:

$$sL\hat{i}_c(s) \approx D\hat{v}_g(s) + D'\hat{v}(s) + \left(V_g - V\right)\hat{d}(s) \tag{12.33}$$

Solution for $\hat{d}(s)$ yields

$$\hat{d}(s) = \frac{sL\hat{i}_c(s) - D\hat{v}_g(s) - D'\hat{v}(s)}{\left(V_g - V\right)} \tag{12.34}$$

This small-signal expression describes how the current programmed controller varies the duty cycle, in response to a given control input variation $\hat{i}_c(s)$. It can be seen that $\hat{d}(s)$ depends not only on $\hat{i}_c(s)$, but also on the converter output voltage and input voltage variations. Equation (12.34) can now be substituted into the second and third lines of Eq. (12.31), thereby eliminating $\hat{d}(s)$. One obtains

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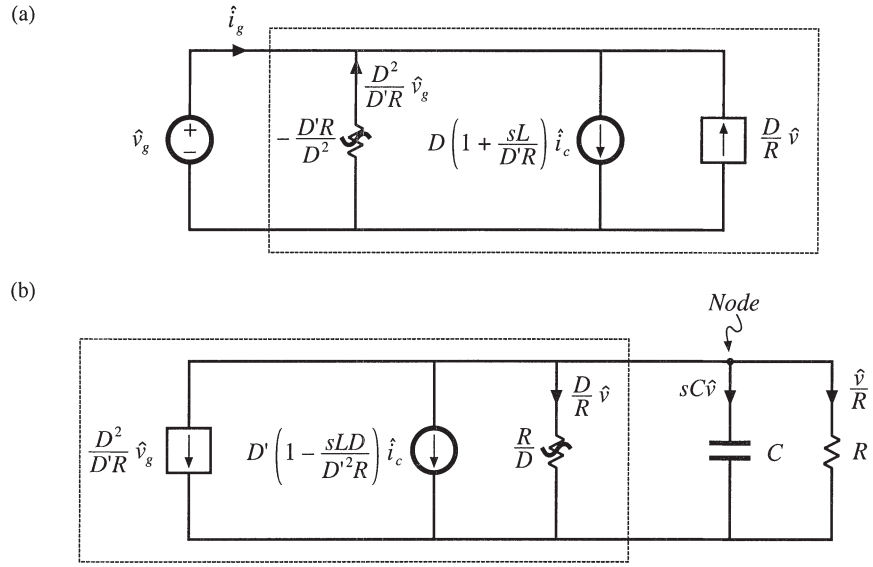


Fig. 12.14 Construction of CPM CCM buck–boost converter equivalent circuit: (a) input port model, corresponding to Eq. (12.38); (b) output port model, corresponding to Eq. (12.37).

$$\begin{aligned} sC\hat{v}(s) &= -D'\hat{i}_c(s) - \frac{\hat{v}(s)}{R} + I_L \frac{sL\hat{i}_c(s) - D\hat{v}_g(s) - D'\hat{v}(s)}{\left(V_g - V\right)} \\ \hat{i}_g(s) &= D\hat{i}_c(s) + I_L \frac{sL\hat{i}_c(s) - D\hat{v}_g(s) - D'\hat{v}(s)}{\left(V_g - V\right)} \end{aligned} \tag{12.35}$$

These equations can be simplified by collecting terms, and by use of the steady-state relationships

$$\begin{aligned} V &= -\frac{D}{D'} V_g \\ I_L &= -\frac{V}{D'R} = \frac{D}{D'^2R} V_g \end{aligned} \tag{12.36}$$

Equation (12.35) then becomes

$$sC\hat{v}(s) = \left(\frac{sLD}{D'R} - D'\right)\hat{i}_c(s) - \left(\frac{D}{R} + \frac{1}{R}\right)\hat{v}(s) - \left(\frac{D^2}{D'R}\right)\hat{v}_g(s) \tag{12.37}$$

$$\hat{i}_g(s) = \left(\frac{sLD}{D'R} + D\right)\hat{i}_c(s) - \left(\frac{D}{R}\right)\hat{v}(s) - \left(\frac{D^2}{D'R}\right)\hat{v}_g(s) \tag{12.38}$$

These are the basic ac small-signal equations for the simplified first-order model of the current-programmed buck-boost converter. These equations can now be used to construct small-signal ac circuit models that represent the behavior of the converter input and output ports. In Eq. (12.37), the quantity $sC\hat{v}(s)$ is the output capacitor current. The $\hat{i}_c(s)$ term is represented in Fig. 12.14(b) by an independent

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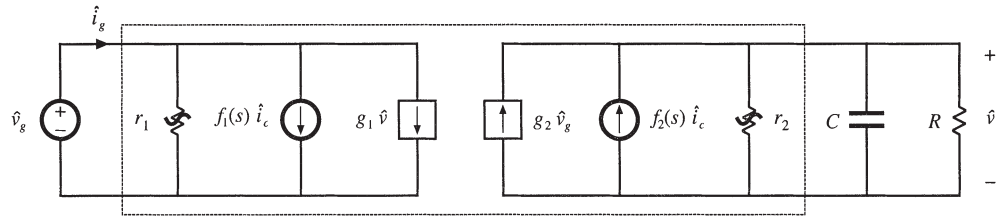


Fig. 12.15 Two-port equivalent circuit used to model the current-programmed CCM buck, boost, and buck–boost converters.

current source, while the $\hat{v}_g(s)$ term is represented by a dependent current source. $\hat{v}(s)/R$ is the current through the load resistor, and $\hat{v}(s)D/R$ is the current through an effective ac resistor of value R/D.

Equation (12.38) describes the current $\hat{i}_g(s)$ drawn by the converter input port, out of the source $\hat{v}_g(s)$. The $\hat{i}_c(s)$ term is again represented in Fig. 12.14(a) by an independent current source, and the $\hat{v}(s)$ term is represented by a dependent current source. The quantity $-\hat{v}_g(s)D^2/D'R$ is modeled by an effective ac resistor having the negative value $-D'R/D^2$.

Figures 12.14(a) and (b) can now be combined into the small-signal two-port model of Fig. 12.15. The current programmed buck and boost converters can also be modeled by a two-port equivalent circuit, of the same form. Table 12.1 lists the model parameters for the basic buck, boost, and buck-boost converters.

The two-port equivalent circuit can now be solved, to find the converter transfer functions and output impedance. The control-to-output transfer function is found by setting v_g to zero. Solution for the output voltage then leads to the transfer function $G_{vc}(s)$:

$$G_{vc}(s) = \left.\frac{\hat{v}(s)}{\hat{i}_c(s)}\right|_{\hat{v}_g = 0} = f_2\left(r_2 \,\|\, R \,\|\, \frac{1}{sC}\right) \tag{12.39}$$

Substitution of the model parameters for the buck-boost converter yields

$$G_{vc}(s) = -R\,\frac{D'}{1+D}\,\frac{\left(1 - s\,\frac{DL}{D'^2R}\right)}{\left(1 + s\,\frac{RC}{1+D}\right)} \tag{12.40}$$

Table 12.1 Current programmed mode small-signal equivalent circuit parameters, simple model

Converter	g_1	f_1	r_1	g_2	f_2	r_2
Buck	$\frac{D}{R}$	$D\left(1 + \frac{sL}{R}\right)$	$-\frac{R}{D^2}$	0	1	∞
Boost	0	1	∞	$\frac{1}{D'R}$	$D'\left(1 - \frac{sL}{D'^2R}\right)$	R
Buck–boost	$-\frac{D}{R}$	$D\left(1 + \frac{sL}{D'R}\right)$	$-\frac{D'R}{D^2}$	$-\frac{D^2}{D'R}$	$-D'\left(1 - \frac{sDL}{D'^2R}\right)$	$\frac{R}{D}$

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It can be seen that this transfer function contains only one pole; the pole due to the inductor has been lost. The dc gain is now directly dependent on the load resistance R. In addition, the transfer function contains a right half-plane zero whose corner frequency is unchanged from the duty-cycle-controlled case. In general, introduction of current programming alters the transfer function poles and dc gain, but not the zeroes.

The line-to-output transfer function $G_{vg}(s)$ is found by setting the control input i_c to zero, and then solving for the output voltage. The result is

$$G_{vg}(s) = \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{i_c=0} = g_2\left(r_2 \,\|\, R \,\|\, \frac{1}{sC}\right) \tag{12.41}$$

Substitution of the parameters for the buck-boost converter leads to

$$G_{vg}(s) = -\frac{D^2}{1-D^2}\frac{1}{\left(1+s\frac{RC}{1+D}\right)} \tag{12.42}$$

Again, the inductor pole is lost. The output impedance is

$$Z_{out}(s) = r_2 \,\|\, R \,\|\, \frac{1}{sC} \tag{12.43}$$

For the buck-boost converter, one obtains

$$Z_{out}(s) = \frac{R}{1+D}\frac{1}{\left(1+s\frac{RC}{1+D}\right)} \tag{12.44}$$

12.2.2 Averaged Switch Modeling

Additional physical insight into the properties of current programmed converters can be obtained by use of the averaged switch modeling approach developed in Section 7.4. Consider the buck converter of Fig. 12.16. We can define the terminal voltages and currents of the switch network as shown. When the buck converter operates in the continuous conduction mode, the switch network average terminal waveforms are related as follows:

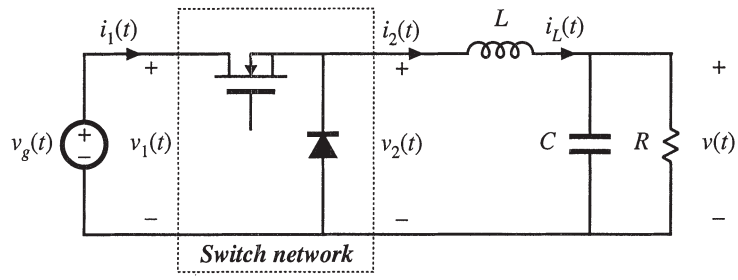


Fig. 12.16 Averaged switch modeling of a current-programmed converter: CCM buck example.

$$\begin{aligned} \langle v_2(t)\rangle_{T_s} &= d(t)\,\langle v_1(t)\rangle_{T_s} \\ \langle i_1(t)\rangle_{T_s} &= d(t)\,\langle i_2(t)\rangle_{T_s} \end{aligned} \tag{12.45}$$

We again invoke the approximation in which the inductor current exactly follows the control current. In terms of the switch network terminal current i_2, we can therefore write

$$\langle i_2(t)\rangle_{T_s} \approx \langle i_c(t)\rangle_{T_s} \tag{12.46}$$

The duty cycle $d(t)$ can now be eliminated from Eq. (12.45), as follows:

$$\langle i_1(t)\rangle_{T_s} = d(t)\,\langle i_c(t)\rangle_{T_s} = \frac{\langle v_2(t)\rangle_{T_s}}{\langle v_1(t)\rangle_{T_s}}\,\langle i_c(t)\rangle_{T_s} \tag{12.47}$$

This equation can be written in the alternative form

$$\langle i_1(t)\rangle_{T_s}\,\langle v_1(t)\rangle_{T_s} = \langle i_c(t)\rangle_{T_s}\,\langle v_2(t)\rangle_{T_s} = \langle p(t)\rangle_{T_s} \tag{12.48}$$

Equations (12.46) and (12.48) are the desired result, which describes the average terminal relations of the CCM current-programmed buck switch network. Equation (12.46) states that the average terminal current $\langle i_2(t)\rangle_{T_s}$ is equal to the control current $\langle i_c(t)\rangle_{T_s}$. Equation (12.48) states that the input port of the switch network consumes average power $\langle p(t)\rangle_{T_s}$ equal to the average power flowing out of the switch output port. The averaged equivalent circuit of Fig. 12.17 is obtained.

Figure 12.17 describes the behavior of the current programmed buck converter switch network, in a simple and straightforward manner. The switch network output port behaves as a current source of value $\langle i_c(t)\rangle_{T_s}$. The input port follows a power sink characteristic, drawing power from the source v_g equal to the power supplied by the i_c current source. Properties of the power source and power sink elements are described in Chapters 11 and 18.

Similar arguments lead to the averaged switch models of the current programmed boost and buck-boost converters, illustrated in Fig. 12.18. In both cases, the switch network averaged terminal waveforms can be represented by a current source of value $\langle i_c(t)\rangle_{T_s}$, in conjunction with a dependent power source or power sink.

A small-signal ac model of the current-programmed buck converter can now be constructed by perturbation and linearization of the switch network averaged terminal waveforms. Let

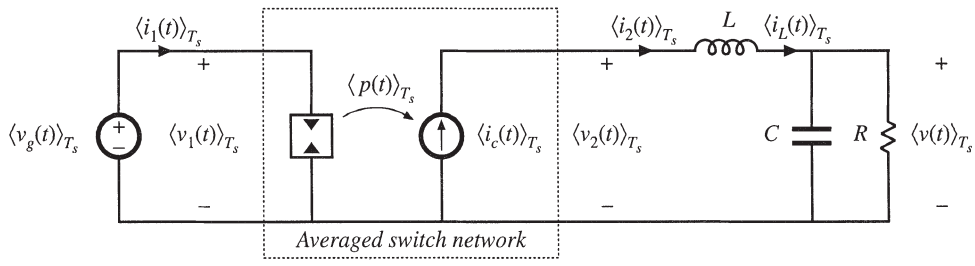


Fig. 12.17 Averaged model of CPM buck converter.

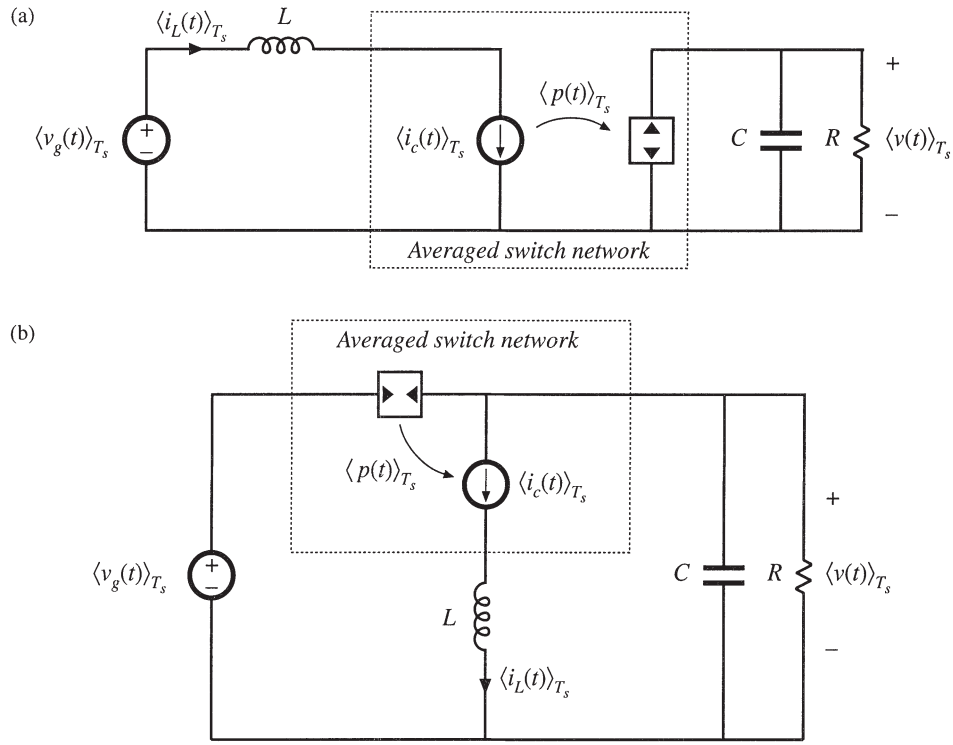


Fig. 12.18 Averaged models of CPM boost (a) and CPM buck–boost (b) converters, derived via averaged switch modeling.

$$\begin{aligned}
\langle v_1(t)\rangle_{T_s} &= V_1 + \hat{v}_1(t) \\
\langle i_1(t)\rangle_{T_s} &= I_1 + \hat{i}_1(t) \\
\langle v_2(t)\rangle_{T_s} &= V_2 + \hat{v}_2(t) \\
\langle i_2(t)\rangle_{T_s} &= I_2 + \hat{i}_2(t) \\
\langle i_c(t)\rangle_{T_s} &= I_c + \hat{i}_c(t)
\end{aligned} \tag{12.49}$$

Perturbation and linearization of the $\langle i_c(t)\rangle_{T_s}$ current source of Fig. 12.17 simply leads to a current source of value $\hat{i}_c(t)$. Perturbation of the power source characteristic, Eq. (12.48), leads to

$$\left(V_1 + \hat{v}_1(t)\right)\left(I_1 + \hat{i}_1(t)\right) = \left(I_c + \hat{i}_c(t)\right)\left(V_2 + \hat{v}_2(t)\right) \tag{12.50}$$

Upon equating the dc terms on both sides of this equation, we obtain

$$V_1 I_1 = I_c V_2 \quad \Rightarrow \quad I_1 = D I_c \tag{12.51}$$

The linear small-signal ac terms of Eq. (12.50) are

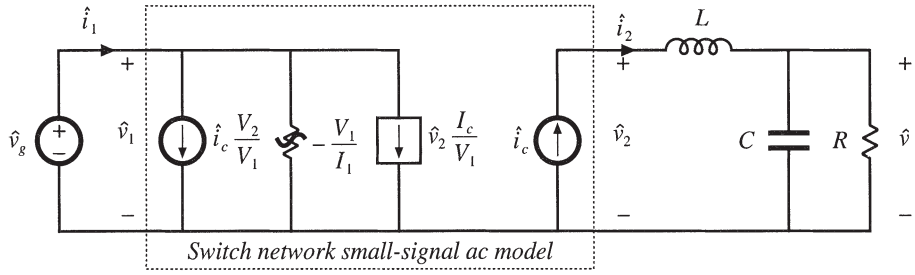


Fig. 12.19 Small-signal model of the CCM CPM buck converter, derived by perturbation and linearization of the switch network in Fig. 12.17.

$$\hat{v}_1(t)I_1 + V_1\hat{i}_1(t) = \hat{i}_c(t)V_2 + I_c\hat{v}_2(t) \tag{12.52}$$

Solution for the small-signal switch network input current $\hat{i}_1(t)$ yields

$$\hat{i}_1(t) = \hat{i}_c(t)\frac{V_2}{V_1} + \hat{v}_2(t)\frac{I_c}{V_1} - \hat{v}_1(t)\frac{I_1}{V_1} \tag{12.53}$$

The small-signal ac model of Fig. 12.19 can now be constructed. The switch network output port is again a current source, of value $\hat{i}_c(t)$. The switch network input port model is obtained by linearization of the power sink characteristic, as given by Eq. (12.53). The input port current $\hat{i}_1(t)$ is composed of three terms. The $\hat{i}_c(t)$ term is modeled by an independent current source, the $\hat{v}_2(t)$ term is modeled by a dependent current source, and the $\hat{v}_1(t)$ term is modeled by an effective ac resistor having the negative value $-V_1/I_1$. As illustrated in Fig. 12.20, this incremental resistance is determined by the slope of the power sink input port characteristic, evaluated at the quiescent operating point. The power sink leads to a negative incremental resistance because an increase in $\langle v_1(t)\rangle_{T_s}$ causes a decrease in $\langle i_1(t)\rangle_{T_s}$, such that constant $\langle p(t)\rangle_{T_s}$ is maintained.

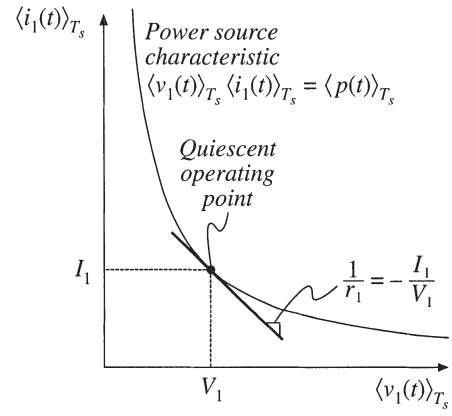


Fig. 12.20 Origin of the input port negative incremental resistance r_1: the slope of the power sink characteristic, evaluated at the quiescent operating point.

The equivalent circuit of Fig. 12.19 can now be simplified by use of the dc relations $V_2 = DV_1$, $I_2 = V_2/R$, $I_1 = DI_2$, $I_2 = I_c$. Equation (12.53) then becomes

$$\hat{i}_1(t) = D\hat{i}_c(t) + \frac{D}{R}\hat{v}_2(t) - \frac{D^2}{R}\hat{v}_1(t) \tag{12.54}$$

Finally, we can eliminate the quantities $\hat{v}_1$ and $\hat{v}_2$ in favor of the converter terminal voltages $\hat{v}_g$ and $\hat{v}$, as follows. The quantity $\hat{v}_1$ is simply equal to $\hat{v}_g$. The quantity $\hat{v}_2$ is equal to the output voltage $\hat{v}$ plus the voltage across the inductor, $sL\hat{i}_c(s)$. Hence,

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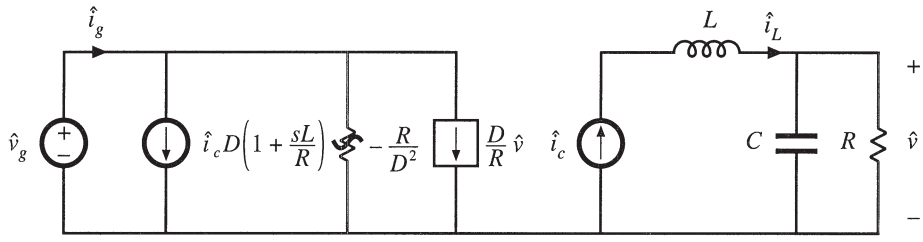


Fig. 12.21 Simplification of the CPM buck converter model of Fig. 12.19, with dependent source expressed in terms of the output voltage variations.

$$\hat{v}_2(s) = \hat{v}(s) + sL\hat{i}_c(s) \tag{12.55}$$

With these substitutions, Eq. (12.54) becomes

$$\hat{i}_1(s) = D\left(1 + s\frac{L}{R}\right)\hat{i}_c(s) + \frac{D}{R}\hat{v}(s) - \frac{D^2}{R}\hat{v}_g(s) \tag{12.56}$$

The equivalent circuit of Fig. 12.21 is now obtained. It can be verified that this equivalent circuit coincides with the model of Fig. 12.15 and the buck converter parameters of Table 12.1.

The approximate small-signal properties of the current programmed buck converter can now be explained. Since the inductor is in series with the current source $\hat{i}_c$, the inductor does not contribute to the control-to-output transfer function. The control-to-output transfer function is determined simply by the relation

$$G_{vc}(s) = \left.\frac{\hat{v}(s)}{\hat{i}_c(s)}\right|_{\hat{v}_g = 0} = \left(R \parallel \frac{1}{sC}\right) \tag{12.57}$$

So current programming transforms the output characteristic of the buck converter into a current source. The power sink input characteristic of the current programmed buck converter leads to a negative incremental input resistance, as described above. Finally, Fig. 12.21 predicts that the buck converter line-to-output transfer function is zero:

$$G_{vg}(s) = \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\hat{i}_c = 0} = 0 \tag{12.58}$$

Disturbances in v_g do not influence the output voltage, since the inductor current depends only on i_c. The current programmed controller adjusts the duty cycle as necessary to maintain constant inductor current, regardless of variations in v_g. The more accurate models of Section 12.3 predict that $G_{vg}(s)$ is not zero, but is nonetheless small in magnitude.

Similar arguments lead to the boost converter small-signal equivalent circuit of Fig. 12.22. Derivation of this equivalent circuit is left as a homework problem. In the case of the boost converter, the switch network input port behaves as a current source, of value i_c, while the output port is a dependent power source, equal to the power apparently consumed by the current source i_c. In the small-signal model, the current source $\hat{i}_c$ appears in series with the inductor L, and hence the converter transfer functions cannot contain poles arising from the inductor. The switch network power source output characteristic leads to an ac resistance of value $r_2 = R$. The line-to-output transfer function $G_{vg}(s)$ is nonzero in the

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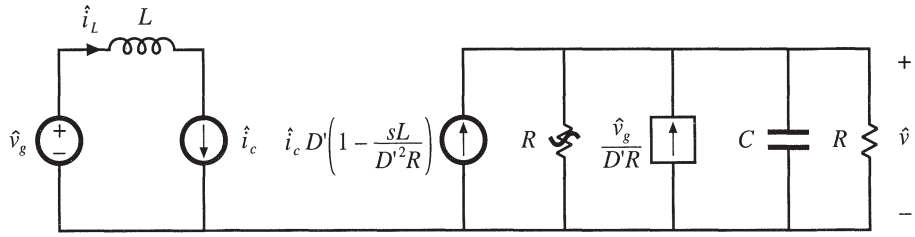


Fig. 12.22 Small-signal model of the CCM CPM boost converter, derived via averaged switch modeling and the approximation $i_L \approx i_c$.

boost converter, since the magnitude of the power source depends directly on the value of v_g. The control-to-output transfer function $G_{vc}(s)$ contains a right half-plane zero, identical to the right half-plane zero of the duty-cycle-controlled boost converter.

12.3 A MORE ACCURATE MODEL

The simple models discussed in the previous section yield much insight into the low-frequency behavior of current-programmed converters. Unfortunately, they do not always describe everything that we need to know. For example, the simple model of the buck converter predicts that the line-to-output transfer function $G_{vg}(s)$ is zero. While it is true that this transfer function is usually small in magnitude, the transfer function is not equal to zero. To predict the effect of input voltage disturbances on the output voltage, we need to compute the actual $G_{vg}(s)$.

In this section, a more accurate analysis is performed which does not rely on the approximation $\langle i_L(t) \rangle_{T_s} \approx i_C(t)$. The analytical approach of [5,6] is combined with the controller model of [7]. A functional block diagram of the current programmed controller is constructed, which accounts for the presence of the artificial ramp and for the inductor current ripple. This block diagram is appended to the averaged converter models derived in Chapter 7, leading to a complete converter CPM model. Models for the CPM buck, boost, and buck–boost converters are listed, and the buck converter model is analyzed in detail.

12.3.1 Current Programmed Controller Model

Rather than using the approximation $\langle i_L(t) \rangle_{T_s} = \langle i_c(t) \rangle_{T_s}$, let us derive a more accurate expression relating the average inductor current $\langle i_L(t) \rangle_{T_s}$ to the control input $i_c(t)$. The inductor current waveform is illustrated in Fig. 12.23. It can be seen that the peak value of $i_L(t)$ differs from $i_c(t)$, by the magnitude of the artificial ramp waveform at time $t = dT_s$, that is, by $m_a dT_s$. The peak and average values of the inductor current waveform differ by the average value of the inductor current ripple. Under transient conditions, in which $i_L(0)$ is not equal to $i_L(T_s)$, the magnitudes of the inductor current ripples during the dT_s and $d'T_s$ subintervals are $m_1 dT_s/2$ and $m_2 d'T_s/2$, respectively. Hence, the average value of the inductor current ripple is $d(m_1 dT_s/2) + d'(m_2 d'T_s/2)$. We can express the average inductor current as

$$\begin{aligned} \langle i_L(t) \rangle_{T_s} &= \langle i_c(t) \rangle_{T_s} - m_a dT_s - d\frac{m_1 dT_s}{2} - d'\frac{m_2 d'T_s}{2} \\ &= \langle i_c(t) \rangle_{T_s} - m_a dT_s - m_1 \frac{d^2 T_s}{2} - m_2 \frac{d'^2 T_s}{2} \end{aligned} \tag{12.59}$$

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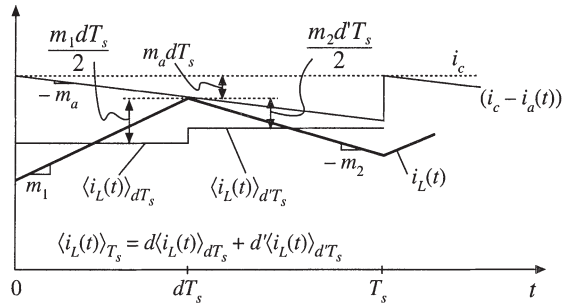


Fig. 12.23 Accurate determination of the relationship between the average inductor current $\langle i_L(t)\rangle_{T_s}$ and i_c.

This is the more accurate relationship which is employed in this section.

A small-signal current programmed controller model is found by perturbation and linearization of Eq. (12.59). Let

$$\begin{aligned}
\langle i_L(t)\rangle_{T_s} &= I_L + \hat{i}_L(t) \\
\langle i_c(t)\rangle_{T_s} &= I_c + \hat{i}_c(t) \\
d(t) &= D + \hat{d}(t) \\
m_1(t) &= M_1 + \hat{m}_1(t) \\
m_2(t) &= M_2 + \hat{m}_2(t)
\end{aligned} \tag{12.60}$$

Note that it is necessary to perturb the slopes m_1 and m_2, since the inductor current slope depends on the converter voltages according to Eq. (12.1). For the basic buck, boost, and buck–boost converters, the slope variations are given by

Buck converter

$$\hat{m}_1 = \frac{\hat{v}_g - \hat{v}}{L} \qquad \hat{m}_2 = \frac{\hat{v}}{L}$$

Boost converter

$$\hat{m}_1 = \frac{\hat{v}_g}{L} \qquad \hat{m}_2 = \frac{\hat{v} - \hat{v}_g}{L} \tag{12.61}$$

Buck–boost converter

$$\hat{m}_1 = \frac{\hat{v}_g}{L} \qquad \hat{m}_2 = -\frac{\hat{v}}{L}$$

It is assumed that m_a does not vary: $\hat{m}_a = M_a$. Substitution of Eq. (12.60) into Eq. (12.59) leads to

$$\left(I_L + \hat{i}_L(t)\right) = \left(I_c + \hat{i}_c(t)\right) - M_a T_s\left(D + \hat{d}(t)\right) - \frac{T_s}{2}\left(M_1 + \hat{m}_1(t)\right)\left(D + \hat{d}(t)\right)^2 - \frac{T_s}{2}\left(M_2 + \hat{m}_2(t)\right)\left(D' - \hat{d}(t)\right)^2 \tag{12.62}$$

The first-order ac terms are

$$\hat{i}_L(t) = \hat{i}_c(t) - \left(M_a T_s + DM_1 T_s - D'M_2 T_s\right)\hat{d}(t) - \frac{D^2 T_s}{2}\hat{m}_1(t) - \frac{D'^2 T_s}{2}\hat{m}_2(t) \tag{12.63}$$

With use of the equilibrium relationship $DM_1 = D'M_2$, Eq. (12.63) can be further simplified:

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Table 12.2 Current programmed controller gains for basic converters

Converter	F_g	F_v
Buck	$\frac{D^2T_s}{2L}$	$\frac{(1-2D)T_s}{2L}$
Boost	$\frac{(2D-1)T_s}{2L}$	$\frac{D'^2T_s}{2L}$
Buck–boost	$\frac{D^2T_s}{2L}$	$-\frac{D'^2T_s}{2L}$

$$\hat{i}_L(t) = \hat{i}_c(t) - M_a T_s \hat{d}(t) - \frac{D^2 T_s}{2}\hat{m}_1(t) - \frac{D'^2 T_s}{2}\hat{m}_2(t) \tag{12.64}$$

Finally, solution for $\hat{d}(t)$ yields

$$\hat{d}(t) = \frac{1}{M_a T_s}\left[\hat{i}_c(t) - \hat{i}_L(t) - \frac{D^2 T_s}{2}\hat{m}_1(t) - \frac{D'^2 T_s}{2}\hat{m}_2(t)\right] \tag{12.65}$$

This is the actual relationship that the current programmed controller follows, to determine $\hat{d}(t)$ as a function of $\hat{i}_c(t)$, $\hat{i}_L(t)$, $\hat{m}_1(t)$, and $\hat{m}_2(t)$. Since the quantities $\hat{m}_1(t)$, and $\hat{m}_2(t)$ depend on $\hat{v}_g(t)$ and $\hat{v}(t)$, according to Eq. (12.61), we can express Eq. (12.65) in the following form:

$$\hat{d}(t) = F_m\left[\hat{i}_c(t) - \hat{i}_L(t) - F_g\hat{v}_g(t) - F_v\hat{v}(t)\right] \tag{12.66}$$

where $F_m = 1/M_a T_s$. Expressions for the gains F_g and F_v, for the basic buck, boost, and buck–boost converters, are listed in Table 12.2. A functional block diagram of the current programmed controller, corresponding to Eq. (12.66), is constructed in Fig. 12.24.

Current programmed converter models can now be obtained, by combining the controller block

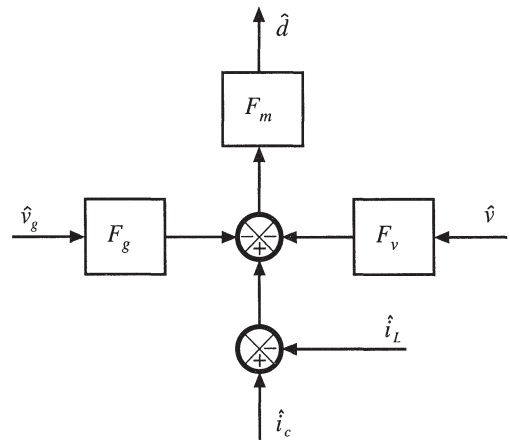


Fig. 12.24 Functional block diagram of the current programmed controller.

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diagram of Fig. 12.24 with the averaged converter models derived in Chapter 7. Figure 12.25 illustrates the CPM converter models obtained by combination of Fig. 12.24 with the buck, boost, and buck-boost models of Fig. 7.17. For each converter, the current programmed controller contains effective feedback of the inductor current $\hat{i}_L(t)$ and the output voltage $\hat{v}(t)$, as well as effective feedforward of the input voltage $\hat{v}_g(t)$.

12.3.2 Solution of the CPM Transfer Functions

Next, let us solve the models of Fig. 12.25, to determine more accurate expressions for the control-to-output and line-to-output transfer functions of current-programmed buck, boost, and buck–boost converters. As discussed in Chapter 8, the converter output voltage $\hat{v}$ can be expressed as a function of the duty-cycle $\hat{d}$ and input voltage $\hat{v}_g$ variations, using the transfer functions $G_{vd}(s)$ and $G_{vg}(s)$:

$$\hat{v}(s) = G_{vd}(s)\hat{d}(s) + G_{vg}(s)\hat{v}_g(s) \tag{12.67}$$

In a similar manner, the inductor current variation $\hat{i}$ can be expressed as a function of the duty-cycle $\hat{d}$ and input voltage $\hat{v}_g$ variations, by defining the transfer functions $G_{id}(s)$ and $G_{ig}(s)$:

$$\hat{i}_L(s) = G_{id}(s)\hat{d}(s) + G_{ig}(s)\hat{v}_g(s) \tag{12.68}$$

where the transfer functions $G_{id}(s)$ and $G_{ig}(s)$ are given by:

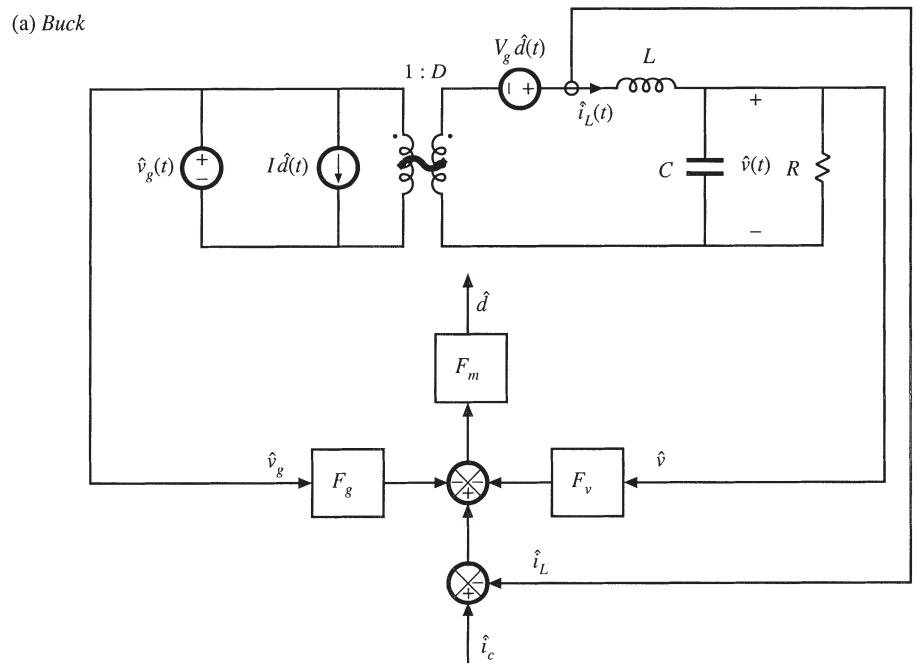
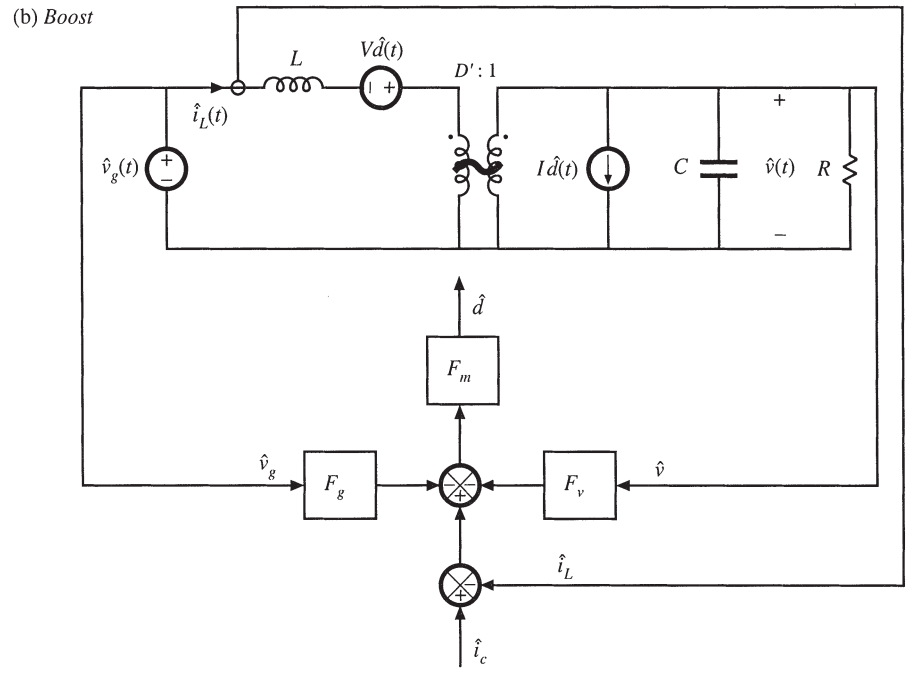


Fig. 12.25 More accurate models of current-programmed converters: (a) buck, (b) boost, (c) buck–boost.

(b) *Boost*



(c) *Buck–boost*

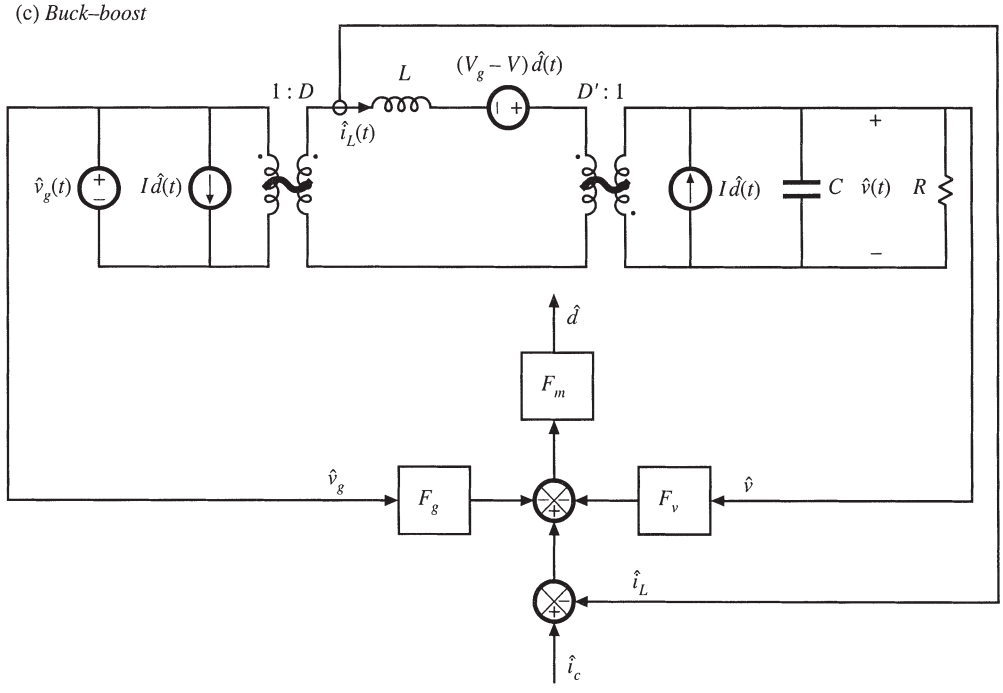


Fig. 12.25 Continued.

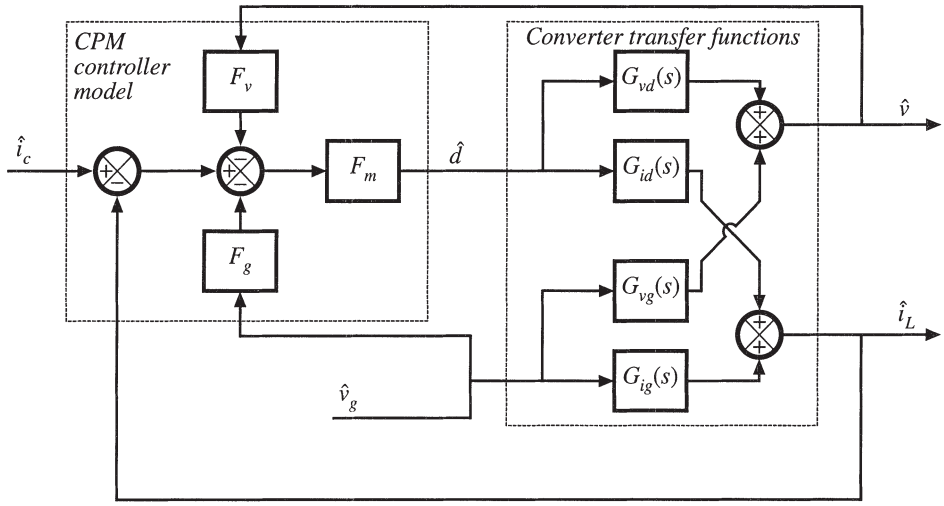


Fig. 12.26 Block diagram that models the current-programmed converters of Fig. 12.25.

$$G_{id}(s) = \left.\frac{\hat{i}_L(s)}{\hat{d}(s)}\right|_{\hat{v}_g(s)=0}$$
$$G_{ig}(s) = \left.\frac{\hat{i}_L(s)}{\hat{v}_g(s)}\right|_{\hat{d}(s)=0} \tag{12.69}$$

Figure 12.26 illustrates replacement of the converter circuit models of Fig. 12.25 with block diagrams that correspond to Eqs. (12.67) and (12.68).

The control-to-output and line-to-output transfer functions can now be found, by manipulation of the block diagram of Fig. 12.26, or by algebraic elimination of $\hat{d}$ and $\hat{i}_L$ from Eqs. (12.66), (12.67), and (12.68), and solution for $\hat{v}$. Substitution of Eq. (12.68) into Eq. (12.66) and solution for $\hat{d}$ leads to

$$\hat{d} = \frac{F_m}{\left(1 + F_m G_{id}\right)}\left[\hat{i}_c - \left(G_{ig} + F_g\right)\hat{v}_g - F_v\hat{v}\right] \tag{12.70}$$

By substituting this expression into Eq. (12.67), one obtains

$$\hat{v} = \frac{F_m G_{vd}}{\left(1 + F_m G_{id}\right)}\left[\hat{i}_c - \left(G_{ig} + F_g\right)\hat{v}_g - F_v\hat{v}\right] + G_{vg}\hat{v}_g \tag{12.71}$$

Solution of this equation for $\hat{v}$ leads to the desired result:

$$\hat{v} = \frac{F_m G_{vd}}{1 + F_m\left(G_{id} + F_v G_{vd}\right)}\hat{i}_c + \frac{G_{vg} - F_m F_g G_{vd} + F_m\left(G_{vg}G_{id} - G_{ig}G_{vd}\right)}{1 + F_m\left(G_{id} + F_v G_{vd}\right)}\hat{v}_g \tag{12.72}$$

Therefore, the current-programmed control-to-output transfer function is

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$$G_{vc}(s) = \left.\frac{\hat{v}(s)}{\hat{i}_c(s)}\right|_{\hat{v}_g(s)=0} = \frac{F_m G_{vd}}{1 + F_m\left(G_{id} + F_v G_{vd}\right)} \tag{12.73}$$

The current-programmed line-to-output transfer function is

$$G_{vg\text{-}cpm}(s) = \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\hat{i}_c(s)=0} = \frac{G_{vg} - F_m F_g G_{vd} + F_m\left(G_{vg}G_{id} - G_{ig}G_{vd}\right)}{1 + F_m\left(G_{id} + F_v G_{vd}\right)} \tag{12.74}$$

Equations (12.73) and (12.74) are general expressions for the important transfer functions of single-inductor current-programmed converters operating in the continuous conduction mode.

12.3.3 Discussion

The controller model of Eq. (12.66) and Fig. 12.24 accounts for the differences between i_L and i_c that arise by two mechanisms: the inductor current ripple and the artificial ramp. The inductor current ripple causes the peak and average values of the inductor current to differ; this leads to a deviation between the average inductor current and i_c. Since the magnitude of the inductor current ripple is a function of the converter input and capacitor voltages, this mechanism introduces $\hat{v}_g$ and $\hat{v}$ dependencies into the controller small-signal block diagram. Thus, the F_g and F_v gain blocks of Fig. 12.24 model the small-signal effects of the inductor current ripple. For operation deep in continuous conduction mode ($2L/RT_s \gg 1$), the inductor current ripple is small. The F_g and F_v gain blocks can then be ignored, and the inductor current ripple has negligible effect on the current programmed controller gain.

The artificial ramp also causes the average inductor current to differ from i_c. This is modeled by the gain block F_m, which depends inversely on the artificial ramp slope M_a. With no artificial ramp, $M_a = 0$ and F_m tends to infinity. The current-programmed control systems of Fig. 12.25 then effectively have infinite loop gain. Since the duty cycle $\hat{d}$ is finite, the signal at the input to the F_m block ($\hat{d}/F_m$) must tend to zero. The block diagram then predicts that

$$\frac{\hat{d}}{F_m} = 0 = \hat{i}_c - \hat{i}_L - F_g\hat{v}_g - F_v\hat{v} \tag{12.75}$$

In the case of negligible inductor current ripple ($F_g \to 0$ and $F_v \to 0$), this equation further reduces to

$$0 = \hat{i}_c - \hat{i}_L \tag{12.76}$$

This coincides with the simple approximation employed in Section 12.2. Hence, the transfer functions predicted in this section reduce to the results of Section 12.2 when there is no artificial ramp and negligible inductor current ripple. In the limit when $F_m \to \infty$, $F_g \to 0$, and $F_v \to 0$, the control-to-output transfer function (12.73) reduces to

$$\lim_{\substack{F_m \to \infty \\ F_g \to 0 \\ F_v \to 0}} G_{vc}(s) = \frac{G_{vd}}{G_{id}} \tag{12.77}$$

and the line-to-output transfer function reduces to

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$$\lim_{\substack{F_m \to \infty \\ F_g \to 0 \\ F_v \to 0}} G_{vg\text{-}cpm}(s) = \frac{G_{vg}G_{id} - G_{ig}G_{vd}}{G_{id}} \tag{12.78}$$

It can be verified that Eqs. (12.77) and (12.78) are equivalent to the transfer functions derived in Section 12.2.

When an artificial ramp is present, then the gain F_m is reduced to a finite value. The current-programmed controller no longer perfectly regulates the inductor current i_L, and the terms on the right-hand side of Eq. (12.75) do not add to zero. In the extreme case of a very large artificial ramp (large M_a and hence small F_m), the current-programmed controller degenerates to duty-cycle control. The artificial ramp and analog comparator of Fig. 12.8 then function as a pulse-width modulator similar to Fig. 7.63, with small-signal gain F_m. For small F_m and for $F_g \to 0$, $F_v \to 0$, the control-to-output transfer function (12.73) reduces to

$$\lim_{\substack{\text{small } F_m \\ F_v \to 0 \\ F_g \to 0}} G_{vc}(s) = F_m G_{vd}(s) \tag{12.79}$$

which coincides with conventional duty cycle control. Likewise, Eq. (12.74) reduces to

$$\lim_{\substack{F_m \to \infty \\ F_g \to 0 \\ F_v \to 0}} G_{vg\text{-}cpm}(s) = G_{vg} \tag{12.80}$$

which is the line-to-output transfer function for conventional duty cycle control.

12.3.4 Current-Programmed Transfer Functions of the CCM Buck Converter

The control-to-output transfer function $G_{vd}(s)$ and line-to-output transfer function $G_{vg}(s)$ of the CCM buck converter with duty cycle control are tabulated in Chapter 8, by analysis of the equivalent circuit model in Fig. 7.17(a). The results are:

$$G_{vd}(s) = \frac{V}{D} \frac{1}{den(s)} \tag{12.81}$$

$$G_{vg}(s) = D \frac{1}{den(s)} \tag{12.82}$$

where the denominator polynomial is

$$den(s) = 1 + s\frac{L}{R} + s^2 LC \tag{12.83}$$

The inductor current transfer functions $G_{id}(s)$ and $G_{ig}(s)$ defined by Eqs. (12.68) and (12.69) are also found by solution of the equivalent circuit model in Fig. 7.17(a), with the following results:

$$G_{id}(s) = \frac{V}{DR} \frac{\left(1 + sRC\right)}{den(s)} \tag{12.84}$$

$$G_{ig}(s) = \frac{D}{R}\frac{\left(1 + sRC\right)}{den(s)} \tag{12.85}$$

where $den(s)$ is again given by Eq. (12.83).

With no artificial ramp and negligible ripple, the control-to-output transfer function reduces to the ideal expression (12.77). Substitution of Eqs. (12.81) and (12.84) yields

$$\lim_{\substack{F_m \to \infty \\ F_g \to 0 \\ F_v \to 0}} G_{vc}(s) = \frac{G_{vd}(s)}{G_{id}(s)} = \frac{R}{1 + sRC} \tag{12.86}$$

Under the same conditions, the line-to-output transfer function reduces to the ideal expression (12.78). Substitution of Eqs. (12.81) to (12.85) leads to

$$\lim_{\substack{F_m \to \infty \\ F_g \to 0 \\ F_v \to 0}} G_{vg\text{-}cpm}(s) = \frac{G_{vg}(s)G_{id}(s) - G_{vd}(s)G_{ig}(s)}{G_{id}(s)} = 0 \tag{12.87}$$

Equations (12.86) and (12.87) coincide with the expressions derived in Section 12.2 for the CCM buck converter.

For arbitrary F_m, F_v, and F_g, the control-to-output transfer function is given by Eq. (12.73). Substitution of Eqs. (12.81) to (12.85) into Eq. (12.73) yields

$$G_{vc}(s) = \frac{F_m G_{vd}}{1 + F_m\left[G_{id} + F_v G_{vd}\right]} = \frac{F_m\left(\frac{V}{D}\frac{1}{den(s)}\right)}{1 + F_m\left[\left(\frac{V}{DR}\frac{1 + sRC}{den(s)}\right) + F_v\left(\frac{V}{D}\frac{1}{den(s)}\right)\right]} \tag{12.88}$$

Simplification leads to

$$G_{vc}(s) = \frac{F_m\frac{V}{D}}{den(s) + \frac{F_m V}{DR}\left(1 + sRC\right) + F_m F_v\frac{V}{D}} \tag{12.89}$$

Finally, the control-to-output transfer function can be written in the following normalized form:

$$G_{vc}(s) = \frac{G_{c0}}{1 + \frac{s}{Q_c\omega_c} + \left(\frac{s}{\omega_c}\right)^2} \tag{12.90}$$

where

$$G_{c0} = \frac{V}{D}\frac{F_m}{1 + \frac{F_m V}{DR} + \frac{F_m F_v V}{D}} \tag{12.91}$$

$$\omega_c = \frac{1}{\sqrt{LC}}\sqrt{1 + \frac{F_m V}{DR} + \frac{F_m F_v V}{D}} \tag{12.92}$$

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$$Q_c = R\sqrt{\frac{C}{L}}\,\frac{\sqrt{1+\dfrac{F_m V}{DR}+\dfrac{F_m F_v V}{D}}}{\left(1+\dfrac{RCF_m V}{DL}\right)} \tag{12.93}$$

In the above equations, the salient features G_{c0}, ω_c, and Q_c are expressed as the duty-ratio-control value, multiplied by a factor that accounts for the effects of current-programmed control.

It can be seen from Eq. (12.93) that current programming tends to reduce the Q-factor of the poles. For large F_m, Q_c varies as $F_m^{-1/2}$; consequently, the poles become real and well-separated in magnitude. The low-Q approximation of Section 8.1.7 then predicts that the low-frequency pole becomes

$$Q_c\omega_c = \frac{R}{L}\,\frac{\left(1+\dfrac{F_m V}{DR}+\dfrac{F_m F_v V}{D}\right)}{\left(1+\dfrac{RCF_m V}{DL}\right)} \tag{12.94}$$

For large F_m and small F_v, this expression can be further approximated as

$$Q_c\omega_c \approx \frac{1}{RC} \tag{12.95}$$

which coincides with the low-frequency pole predicted by the simple model of Section 12.2. The low-Q approximation also predicts that the high-frequency pole becomes

$$\frac{\omega_c}{Q_c} = \frac{1}{RC}\left(1+\frac{RCF_m V}{DL}\right) \tag{12.96}$$

For large F_m, this expression can be further approximated as

$$\frac{\omega_c}{Q_c} \approx \frac{F_m V}{DL} = f_s\frac{M_2}{DM_a} \tag{12.97}$$

The high-frequency pole is typically predicted to lie near to or greater than the switching frequency f_s. It should be pointed out that the converter switching and modulator sampling processes lead to discrete-time phenomena that affect the high-frequency behavior of the converter, and that are not predicted by the continuous-time averaged analysis employed here. Hence, the averaged model is valid only at frequencies sufficiently less than one-half of the switching frequency.

For arbitrary F_m, F_v, and F_g, the current-programmed line-to-output transfer function $G_{vg\text{-}cpm}(s)$ is given by Eq. (12.74). This equation is most easily evaluated by first finding the ideal transfer function, Eq. (12.78), and then using the result to simplify Eq. (12.74). In the case of the buck converter, Eq. (12.87) shows that the quantity $(G_{vg}G_{id} - G_{vd}G_{ig})$ is equal to zero. Hence, Eq. (12.74) becomes

$$G_{vg\text{-}cpm}(s) = \frac{G_{vg} - F_m F_g G_{vd} + F_m(0)}{1 + F_m\left(G_{id} + F_v G_{vd}\right)} \tag{12.98}$$

Substitution of Eqs. (12.81) to (12.85) into Eq. (12.98) yields

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$$G_{vg\text{-}cpm}(s) = \frac{\frac{D}{den(s)} - F_m F_g \frac{V}{D}\frac{1}{den(s)}}{1 + F_m\left(\frac{V}{DR}\frac{1+sRC}{den(s)} + F_v \frac{V}{D}\frac{1}{den(s)}\right)} \tag{12.99}$$

Simplification leads to

$$G_{vg\text{-}cpm}(s) = \frac{\left(D - F_m F_g \frac{V}{D}\right)}{den(s) + \frac{F_m V}{DR}\left(1 + sRC\right) + F_m F_v \frac{V}{D}} \tag{12.100}$$

Finally, the current-programmed line-to-output transfer function can be written in the following normalized form:

$$G_{vg\text{-}cpm}(s) = \frac{G_{g0}}{1 + \frac{s}{Q_c \omega_c} + \left(\frac{s}{\omega_c}\right)^2} \tag{12.101}$$

where

$$G_{g0} = D\frac{\left(1 - \frac{F_m F_g V}{D^2}\right)}{\left(1 + \frac{F_m V}{DR} + \frac{F_m F_v V}{D}\right)} = D\frac{\left(1 - \frac{M_2}{2M_a}\right)}{\left(1 + \frac{F_m V}{DR} + \frac{F_m F_v V}{D}\right)} \tag{12.102}$$

The quantities Q_c and ω_c are given by Eqs. (12.92) and (12.93).

Equation (12.102) shows how current programming reduces the dc gain of the buck converter line-to-output transfer function. For duty cycle control ($F_m \to 0$), G_{g0} is equal to D. Nonzero values of F_m reduce the numerator and increase the denominator of Eq. (12.102), which tends to reduce G_{g0}. We have already seen that, in the ideal case ($F_m \to \infty$, $F_g \to 0$, $F_v \to 0$), G_{g0} becomes zero. Equation (12.102) reveals that nonideal current-programmed buck converters can also exhibit zero G_{g0}, if the artificial ramp slope M_a is chosen equal to $0.5M_2$. The current programmed controller then prevents input line voltage variations from reaching the output. The mechanism that leads to this result is the effective feedforward of v_g, inherent in the current programmed controller via the $F_g \hat{v}_g$ term in Eq. (12.66). It can be seen from Fig. 12.26 that, when $F_g F_m G_{vd}(s) = G_{vg}(s)$, then the feedforward path from $\hat{v}_g$ through F_g induces variations in the output $\hat{v}$ that exactly cancel the $\hat{v}_g$-induced variations in the direct forward path of the converter through $G_{vg}(s)$. This cancellation occurs in the buck converter when $M_a = 0.5M_2$.

12.3.5 Results for Basic Converters

The transfer functions of the basic buck, boost, and buck-boost converters with current-programmed control are summarized in Tables 12.3 to 12.5. Control-to-output and line-to-output transfer functions for both the simple model of Section 12.2 and the more accurate model derived in this section are listed. For completeness, the transfer functions for duty cycle control are included. In each case, the salient features are expressed as the corresponding quantity with duty cycle control, multiplied by a factor that accounts for current-programmed control.

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Table 12.3 Summary of results for the CPM buck converter

Simple model

$$\frac{\hat{v}}{\hat{i}_c} = \frac{R}{1 + sRC}$$

$$\frac{\hat{v}}{\hat{v}_g} = 0$$

Duty cycle controlled gains

$$G_{vd}(s) = \frac{V}{D}\frac{1}{den(s)} \qquad G_{id}(s) = \frac{V}{DR}\frac{1 + sRC}{den(s)}$$

$$G_{vg}(s) = D\frac{1}{den(s)} \qquad G_{ig}(s) = \frac{D}{R}\frac{1 + sRC}{den(s)}$$

$$den(s) = 1 + s\frac{L}{R} + s^2LC$$

More accurate model

$$\frac{\hat{v}}{\hat{i}_c} = G_{vc}(s) = G_{c0}\frac{1}{1 + \frac{s}{Q_c\omega_c} + \left(\frac{s}{\omega_c}\right)^2}$$

$$G_{c0} = \frac{V}{D}\frac{F_m}{\left(1 + \frac{F_mV}{DR} + \frac{F_mF_vV}{D}\right)}$$

$$\omega_c = \frac{1}{\sqrt{LC}}\sqrt{1 + \frac{F_mV}{DR} + \frac{F_mF_vV}{D}}$$

$$Q_c = R\sqrt{\frac{C}{L}}\frac{\sqrt{1 + \frac{F_mV}{DR} + \frac{F_mF_vV}{D}}}{\left(1 + \frac{RCF_mV}{DL}\right)}$$

$$\frac{\hat{v}}{\hat{v}_g} = G_{vg\text{-}cpm}(s) = G_{g0}\frac{1}{1 + \frac{s}{Q_c\omega_c} + \left(\frac{s}{\omega_c}\right)^2}$$

$$G_{g0} = D\frac{\left(1 - \frac{F_mF_gV}{D^2}\right)}{\left(1 + \frac{F_mV}{DR} + \frac{F_mF_vV}{D}\right)}$$

Table 12.4 Summary of results for the CPM boost converter

Simple model

$$\frac{\hat{v}}{\hat{i}_c} = \frac{D'R}{2}\frac{\left(1 - s\frac{L}{D'^2R}\right)}{\left(1 + s\frac{RC}{2}\right)}$$

$$\frac{\hat{v}}{\hat{v}_g} = \frac{1}{2D'}\frac{1}{\left(1 + s\frac{RC}{2}\right)}$$

Duty cycle controlled gains

$$G_{vd}(s) = \frac{V}{D'}\frac{\left(1 - s\frac{L}{D'^2R}\right)}{den(s)} \qquad G_{id}(s) = \frac{2V}{D'^2R}\frac{\left(1 + s\frac{RC}{2}\right)}{den(s)}$$

$$G_{vg}(s) = \frac{1}{D'}\frac{1}{den(s)} \qquad G_{ig}(s) = \frac{1}{D'^2R}\frac{\left(1 + sRC\right)}{den(s)}$$

$$den(s) = 1 + s\frac{L}{D'^2R} + s^2\frac{LC}{D'^2}$$

More accurate model

$$\frac{\hat{v}}{\hat{i}_c} = G_{vc}(s) = G_{c0}\frac{\left(1 - s\frac{L}{D'^2R}\right)}{1 + \frac{s}{Q_c\omega_c} + \left(\frac{s}{\omega_c}\right)^2}$$

$$G_{c0} = \frac{V}{D'}\frac{F_m}{\left(1 + \frac{2F_mV}{D'^2R} + \frac{F_mF_vV}{D'}\right)}$$

$$\omega_c = \frac{D'}{\sqrt{LC}}\sqrt{1 + \frac{2F_mV}{D'^2R} + \frac{F_mF_vV}{D'}}$$

$$Q_c = D'R\sqrt{\frac{C}{L}}\frac{\sqrt{1 + \frac{2F_mV}{D'^2R} + \frac{F_mF_vV}{D'}}}{\left(1 + RC\frac{F_mV}{L} - \frac{F_mF_vV}{D'}\right)}$$

$$\frac{\hat{v}}{\hat{v}_g} = G_{vg\text{-}cpm}(s) = G_{g0}\frac{\left(1 + \frac{s}{\omega_{gz}}\right)}{1 + \frac{s}{Q_c\omega_c} + \left(\frac{s}{\omega_c}\right)^2}$$

$$G_{g0} = \frac{1}{D'}\frac{\left(1 - F_mF_gV + \frac{F_mV}{D'^2R}\right)}{\left(1 + \frac{2F_mV}{D'^2R} + \frac{F_mF_vV}{D'}\right)}$$

$$\omega_{gz} = \frac{D'^3R}{L}\frac{\left(1 - F_mF_gV + \frac{F_mV}{D'^2R}\right)}{F_mF_gV}$$

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Table 12.5 Summary of results for the CPM buck–boost converter

Simple model

$$\frac{\hat{v}}{\hat{i}_c} = -\frac{D'R}{(1+D)} \frac{\left(1 - s\frac{DL}{D'^2R}\right)}{\left(1 + s\frac{RC}{1+D}\right)}$$

$$\frac{\hat{v}}{\hat{v}_g} = -\frac{D^2}{1-D^2} \frac{1}{\left(1 + s\frac{RC}{1+D}\right)}$$

Duty cycle controlled gains

$$G_{vd}(s) = -\frac{|V|}{DD'} \frac{\left(1 - s\frac{DL}{D'^2R}\right)}{den(s)}$$

$$G_{vg}(s) = -\frac{D}{D'} \frac{1}{den(s)}$$

$$G_{id}(s) = -\frac{|V|(1+D)}{DD'^2R} \frac{\left(1 + s\frac{RC}{(1+D)}\right)}{den(s)}$$

$$G_{ig}(s) = \frac{D}{D'^2R} \frac{(1+sRC)}{den(s)}$$

$$den(s) = 1 + s\frac{L}{D'^2R} + s^2\frac{LC}{D'^2}$$

More accurate model

$$\frac{\hat{v}}{\hat{i}_c} = G_{vc}(s) = G_{c0} \frac{\left(1 - s\frac{DL}{D'^2R}\right)}{1 + \frac{s}{Q_c\omega_c} + \left(\frac{s}{\omega_c}\right)^2}$$

$$\omega_c = \frac{D'}{\sqrt{LC}} \sqrt{1 + \frac{F_m|V|(1+D)}{DD'^2R} - \frac{F_mF_v|V|}{DD'}}$$

$$\frac{\hat{v}}{\hat{v}_g} = G_{vg\text{-}cpm}(s) = G_{g0} \frac{\left(1 + \frac{s}{\omega_{gz}}\right)}{1 + \frac{s}{Q_c\omega_c} + \left(\frac{s}{\omega_c}\right)^2}$$

$$G_{c0} = -\frac{|V|}{DD'} \frac{F_m}{\left(1 + \frac{F_m|V|(1+D)}{DD'^2R} - \frac{F_mF_v|V|}{DD'}\right)}$$

$$Q_c = D'R\sqrt{\frac{C}{L}} \frac{\sqrt{1 + \frac{F_m|V|(1+D)}{DD'^2R} - \frac{F_mF_v|V|}{DD'}}}{\left(1 + \frac{F_m|V|RC}{DL} + \frac{F_mF_v|V|}{D'}\right)}$$

$$G_{g0} = -\frac{D}{D'}\left(1 + \frac{F_m|V|}{D'^2R} - \frac{F_mF_g|V|}{D^2}\right)$$

$$\omega_{gz} = \frac{DD'^2R}{|V|LF_mF_g}\left(1 + \frac{F_m|V|}{D'^2R} - \frac{F_mF_g|V|}{D^2}\right)$$

The two poles of the line-to-output transfer functions $G_{vg\text{-}cpm}$ and control-to-output transfer functions G_{vc} of all three converters typically exhibit low Q-factors in CPM. The low-Q approximation can be applied, as in Eqs. (12.94) to (12.97), to find the low-frequency pole. The line-to-output transfer functions of the boost and buck–boost converters exhibit two poles and one zero, with substantial dc gain.

12.3.6 Quantitative Effects of Current-Programmed Control on the Converter Transfer Functions

The frequency responses of a CCM buck converter, operating with current-programmed control and with duty cycle control, are compared in Appendix B, Section B.3.2. The buck converter of Fig. B.25 was simulated as described in Appendix B, and the resulting plots are reproduced here.

The magnitude and phase of the control-to-output transfer functions are illustrated in Fig. 12.27. It can be seen that, for duty cycle control, the transfer function $G_{vd}(s)$ exhibits a resonant two-pole response. The substantial damping introduced by current-programmed control leads to essentially a single-pole response in the current-programmed control-to-output transfer function $G_{vc}(s)$. A second pole appears in the vicinity of 100 kHz, which is near the 200 kHz switching frequency. Because of this effective single-pole response, it is relatively easy to design a controller that exhibits a well-behaved response,

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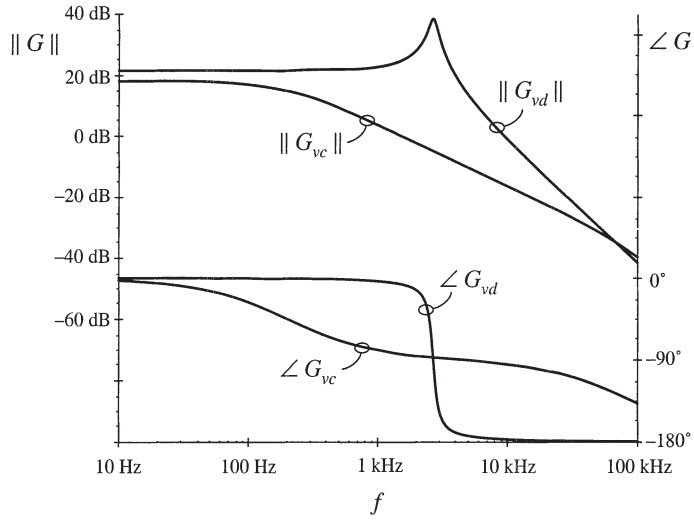


Fig. 12.27 Comparison of CPM control with duty-cycle control, for the control-to-output frequency response of the buck converter example.

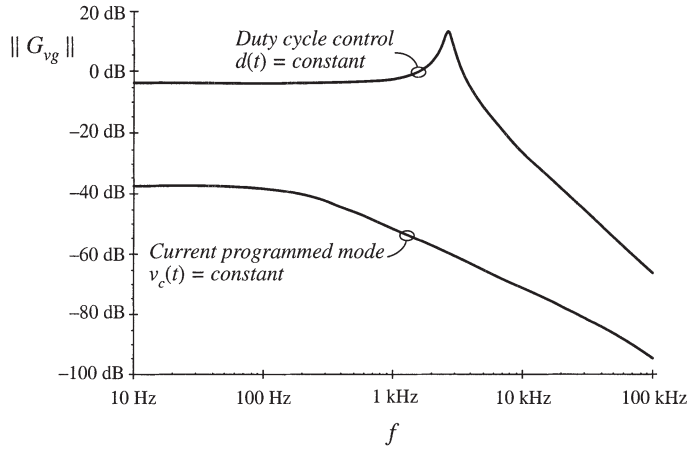


Fig. 12.28 Comparison of CPM control with duty-cycle control, for the line-to-output frequency response of the buck converter example.

having ample phase margin over a wide range of operating points. Proportional-plus-integral (*PI*) controllers are commonly used in current-programmed regulators.

The line-to-output transfer functions of the same example are compared in Fig. 12.28. The line-to-output transfer function $G_{vg}(s)$ for duty-cycle control is characterized by a dc asymptote approximately equal to the duty cycle $D = 0.676$. Resonant poles occur at the corner frequency of the *L–C* filter. The line-to-output transfer function $G_{vg\text{-}cpm}(s)$ with current-programmed control is significantly reduced, and exhibits more than 30 dB of additional attenuation over the frequencies of interest. It should again be

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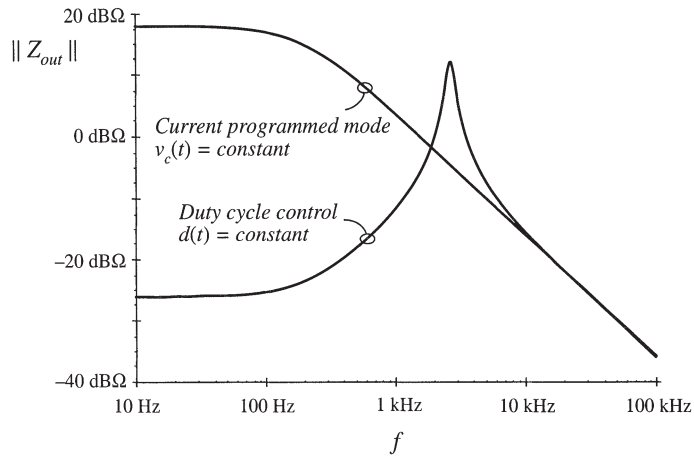


Fig. 12.29 Comparison of CPM control with duty-cycle control, for the output impedance of the buck converter example.

noted that the transfer function $G_{vg\text{-}cpm}(s)$ in Fig. 12.28 cannot be predicted by the simple models of Section 12.2; the more accurate model of Section 12.3 must be employed.

The effect of current-programmed control on the converter output impedance is illustrated in Fig. 12.29. The output impedance plotted in the figure includes the load resistance of 10 Ω. For duty-cycle control, the dc asymptote of the output impedance is dominated by the inductor winding resistance of 0.05 Ω. The inductor becomes significant in the vicinity of 200 Hz. Above the resonant frequency of the output filter, the output impedance is dominated by the output filter capacitor. For current-programmed control, the simple model of Section 12.2 predicts that the inductor branch of the circuit is driven by a current source; this effectively removes the influence of the inductor on the output impedance. The plot of Fig. 12.29 was generated using the more accurate model of this section; nonetheless, the output impedance is accurately predicted by the simple model. The dc asymptote is dominated by the load resistance, and the high-frequency asymptote follows the impedance of the output filter capacitor. It can be seen that current programming substantially increases the converter output impedance.

12.4 DISCONTINUOUS CONDUCTION MODE

Current-programmed converters operating in the discontinuous conduction mode can be described using the averaged switch modeling approaches of Sections 12.3 and 11.1. It is found in this section that the average transistor voltage and current follow a power sink characteristic, while the average diode voltage and current obey a power source characteristic. Perturbation and linearization of these characteristics leads to a small-signal equivalent circuit that models CPM DCM converters. The basic DCM CPM buck, boost, and buck–boost converters essentially exhibit single-pole transfer functions: the second pole and the right half-plane zero appear at frequencies near to or greater than the switching frequency, owing to the small value of L in DCM.

A DCM CPM buck–boost converter example is analyzed here. However, Eqs. (12.103) to (12.120) are written in general form, and apply equally well to DCM CPM buck and boost converters. The schematic of a buck-boost converter is illustrated in Fig. 12.30. The terminal waveforms of the switch network are defined as shown: $v_1(t)$ and $i_1(t)$ are the transistor waveforms, while $v_2(t)$ and $i_2(t)$ are

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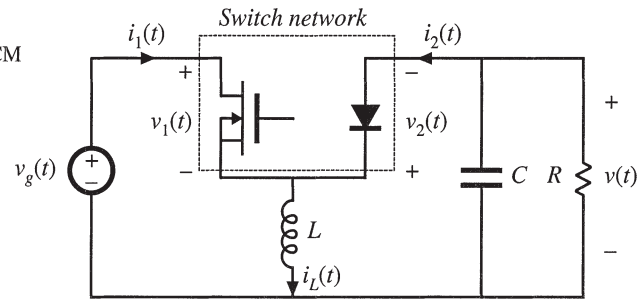


Fig. 12.30 Current-programmed DCM buck–boost converter example.

the diode waveforms. Figure 12.31 illustrates typical DCM waveforms, for current-programmed control with an artificial ramp having slope $-m_a$. The inductor current is zero at the beginning of each switching period. By solution of the transistor conduction subinterval, the programmed current i_{pk} can be related to the transistor duty cycle d_1 by:

$$\begin{aligned} i_c &= i_{pk} + m_a d_1 T_s \\ &= \left(m_1 + m_a\right) d_1 T_s \end{aligned} \tag{12.103}$$

Solution for d_1 leads to

$$d_1(t) = \frac{i_c(t)}{\left(m_1 + m_a\right) T_s} \tag{12.104}$$

The average transistor current is found by integrating the $i_1(t)$ waveform of Fig. 12.31 over one switching period:

$$\left\langle i_1(t) \right\rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} i_1(\tau) d\tau = \frac{q_1}{T_s} \tag{12.105}$$

The total area q_1 is equal to one-half of the peak current i_{pk}, multiplied by the subinterval length $d_1 T_s$. Hence,

$$\left\langle i_1(t) \right\rangle_{T_s} = \tfrac{1}{2} i_{pk}(t) d_1(t) \tag{12.106}$$

Elimination of i_{pk} and d_1, to express the average transistor current as a function of i_c, leads to

$$\left\langle i_1(t) \right\rangle_{T_s} = \frac{\tfrac{1}{2} L i_c^2 f_s}{\left\langle v_1(t) \right\rangle_{T_s} \left(1 + \dfrac{m_a}{m_1}\right)^2} \tag{12.107}$$

Finally, Eq. (12.107) can be rearranged to obtain the averaged switch network input port relationship:

$$\left\langle i_1(t) \right\rangle_{T_s} \left\langle v_1(t) \right\rangle_{T_s} = \frac{\tfrac{1}{2} L i_c^2 f_s}{\left(1 + \dfrac{m_a}{m_1}\right)^2} = \left\langle p(t) \right\rangle_{T_s} \tag{12.108}$$

Thus, the average transistor waveforms obey a power sink characteristic. When $m_a = 0$, then the average power $\langle p(t) \rangle_{T_s}$ is a function only of L, i_c, and f_s. The presence of the artificial ramp causes $\langle p(t) \rangle_{T_s}$ to additionally depend on the converter voltages, via m_1.

The power sink characteristic can also be explained via inductor energy arguments. During the first subinterval, the inductor current increases from 0 to i_{pk}. In the process, the inductor stores the following energy:

$$W = \tfrac{1}{2} L i_{pk}^2 \tag{12.109}$$

The energy W is transferred from the power input v_g, through the switch network input port, to the inductor, once per switching period. This energy transfer process accounts for the power flow

$$\langle p(t) \rangle_{T_s} = W f_s = \tfrac{1}{2} L i_{pk}^2 f_s \tag{12.110}$$

The switch network input port, that is, the transistor terminals, can therefore be modeled by a power sink element, as in Fig. 12.32.

The average switch network output port current, that is, the average diode current, is

$$\langle i_2(t) \rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} i_2(\tau) d\tau = \frac{q_2}{T_s} \tag{12.111}$$

By inspection of Fig. 12.31, the area q_2 is given by

$$q_2 = \tfrac{1}{2} i_{pk} d_2 T_s \tag{12.112}$$

The duty cycle d_2 is determined by the time required for the inductor current to return to zero, during the second subinterval. By arguments similar to those used to derive Eq. (11.12), the duty cycle d_2 can be found as follows:

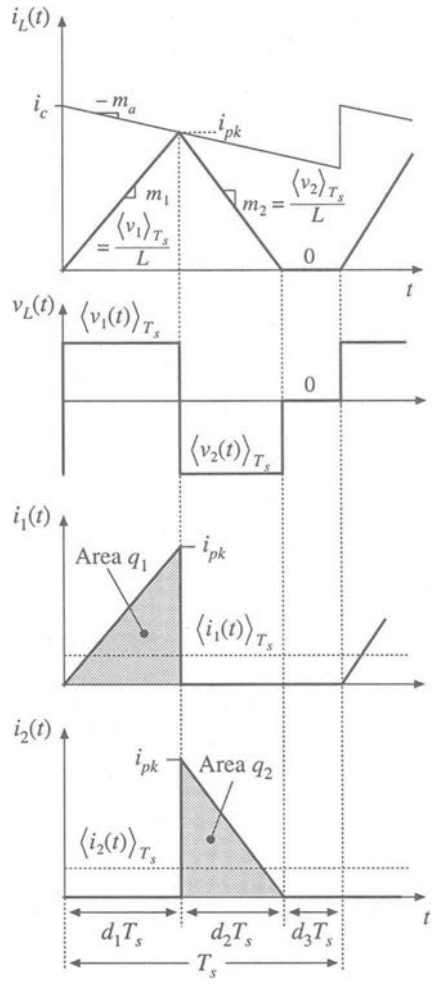


Fig. 12.31 Waveforms, CPM DCM buck–boost example.

$$d_2(t) = d_1(t) \frac{\langle v_1(t) \rangle_{T_s}}{\langle v_2(t) \rangle_{T_s}} \tag{12.113}$$

Substitution of Eqs. (12.113), (12.112), and (12.110) into Eq. (12.111) yields

$$\langle i_2(t) \rangle_{T_s} = \frac{\langle p(t) \rangle_{T_s}}{\langle v_2(t) \rangle_{T_s}} \tag{12.114}$$

The output port of the averaged switch network is therefore described by the relationship

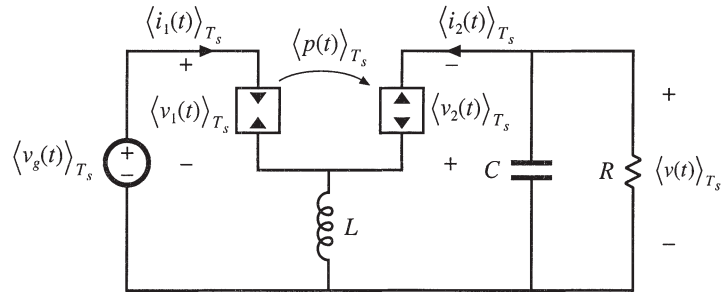


Fig. 12.32 CPM DCM buck–boost converter model, derived via averaged switch modeling.

$$\langle i_2(t)\rangle_{T_s}\langle v_2(t)\rangle_{T_s} = \frac{\frac{1}{2}Li_c^2(t)f_s}{\left(1+\frac{m_a}{m_1}\right)^2} = \langle p(t)\rangle_{T_s} \tag{12.115}$$

In the averaged model, the diode can be replaced by a power source of value $\langle p(t)\rangle_{T_s}$, equal to the power apparently consumed at the switch network input port. During the second subinterval, the inductor releases all of its stored energy through the diode, to the converter output. This results in an average power flow of value $\langle p(t)\rangle_{T_s}$.

A CPM DCM buck-boost averaged model is therefore as given in Fig. 12.32. In this model, the transistor is simply replaced by a power sink of value $\langle p(t)\rangle_{T_s}$, while the diode is replaced by a power source also of value $\langle p(t)\rangle_{T_s}$.

The steady-state equivalent circuit model of the CPM DCM buck-boost converter is obtained by letting the inductor and capacitor tend to short- and open-circuits, respectively. The model of Fig. 12.33 is obtained. The steady-state output voltage V can now be determined by equating the dc load power to the converter average power $\langle p(t)\rangle_{T_s}$. For a resistive load, one obtains

$$\frac{V^2}{R} = P \tag{12.116}$$

where the steady state value of $\langle p(t)\rangle_{T_s}$ is given by

$$P = \frac{\frac{1}{2}LI_c^2(t)f_s}{\left(1+\frac{M_a}{M_1}\right)^2} \tag{12.117}$$

and where I_c is the steady-state value of the control input $i_c(t)$. Solution for V yields the following result

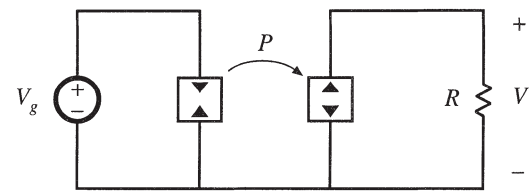
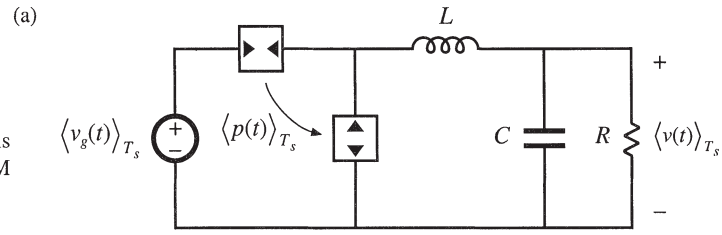


Fig. 12.33 Steady-state model of the CPM DCM buck–boost converter.

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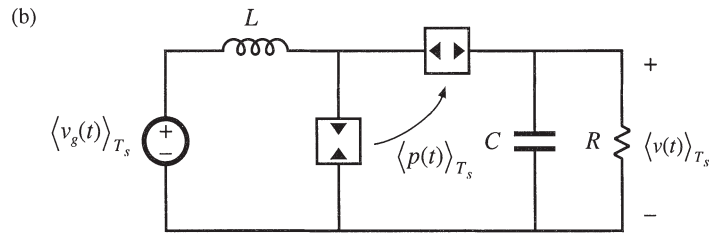


Fig. 12.34 Averaged models of current-programmed DCM converters: (a) buck, (b) boost.

$$V = \sqrt{PR} = I_c \sqrt{\frac{RLf_s}{2\left(1 + \frac{M_a}{M_1}\right)^2}} \tag{12.118}$$

for the case of a resistive load.

Averaged models of the DCM CPM buck, boost, and other converters can be found in a similar manner. In each case, the average transistor waveforms are shown to follow a power sink characteristic, while the average diode waveforms follow a power source characteristic. The resulting equivalent circuits of the CPM DCM buck and boost converters are illustrated in Fig. 12.34. In each case, the average power is given by

Table 12.6 Steady-state DCM current-programmed characteristics of basic converters

Converter	M	I_{crit}	Stability range when $m_a = 0$
Buck	$\frac{P_{load} - P}{P_{load}}$	$\frac{1}{2}\left(I_c - M m_a T_s\right)$	$0 \le M < \frac{2}{3}$
Boost	$\frac{P_{load}}{P_{load} - P}$	$\frac{\left(I_c - \frac{M-1}{M} m_a T_s\right)}{2M}$	$0 \le D \le 1$
Buck–boost	Depends on load characteristic: $P_{load} = P$	$\frac{\left(I_c - \frac{M}{M-1} m_a T_s\right)}{2(M-1)}$	$0 \le D \le 1$

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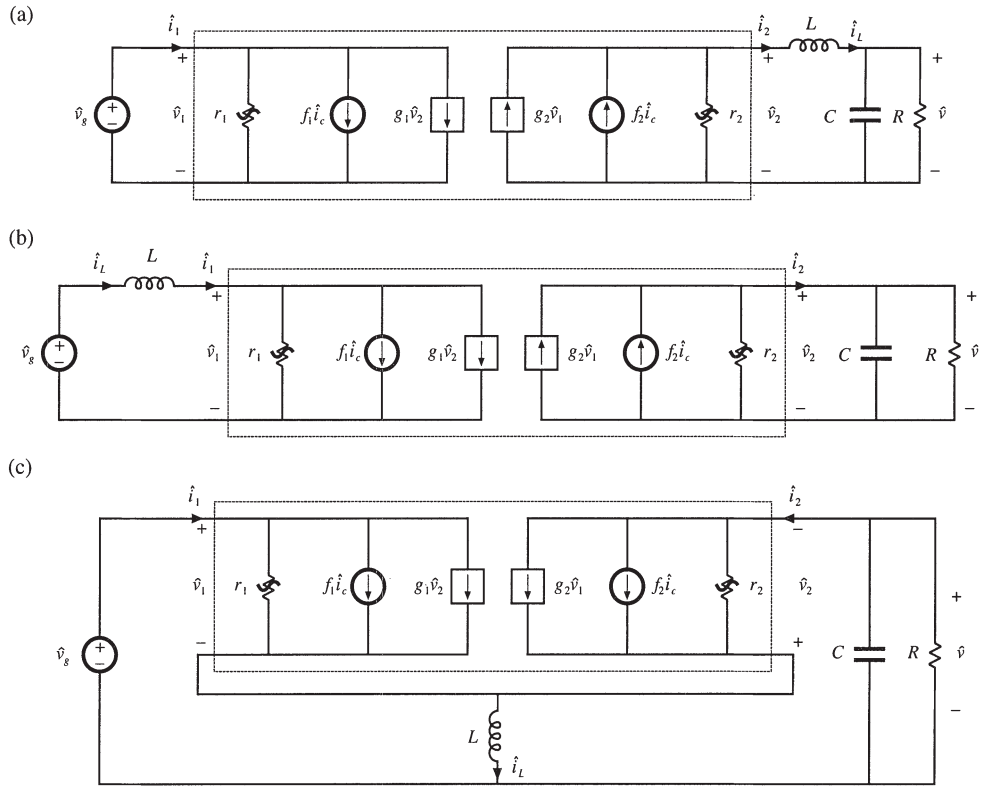


Fig. 12.35 Small-signal models of DCM CPM converters, derived by perturbation and linearization of Figs. 12.32 and 12.34: (a) buck, (b) boost, (c) buck–boost.

$$\langle p(t)\rangle_{T_s} = \frac{\frac{1}{2}Li_c^2(t)f_s}{\left(1+\frac{m_a}{m_1}\right)^2} \tag{12.119}$$

with m_1 defined as in Eq. (12.1).

Steady-state characteristics of the DCM CPM buck, boost, and buck–boost converters are summarized in Table 12.6. In each case, the dc load power is $P_{load} = VI$ and P is given by Eq. (12.117). The conditions for operation of a current programmed converter in the discontinuous conduction mode can be expressed as follows:

$$\begin{aligned} |I| &> |I_{crit}| \quad \text{for CCM} \\ |I| &< |I_{crit}| \quad \text{for DCM} \end{aligned} \tag{12.120}$$

where I is the dc load current. The critical load current at the CCM–DCM boundary, I_{crit}, is expressed as a function of I_c and the voltage conversion ratio $M = V/V_g$ in Table 12.6.

In the discontinuous conduction mode, the inductor current is zero at the beginning and end of

Table 12.7 Current programmed DCM small-signal equivalent circuit parameters: input port

Converter	g_1	f_1	r_1
Buck	$\frac{1}{R}\left(\frac{M^2}{1-M}\right)\frac{\left(1-\frac{m_a}{m_1}\right)}{\left(1+\frac{m_a}{m_1}\right)}$	$2\frac{I_1}{I_c}$	$-R\left(\frac{1-M}{M^2}\right)\frac{\left(1+\frac{m_a}{m_1}\right)}{\left(1-\frac{m_a}{m_1}\right)}$
Boost	$-\frac{1}{R}\left(\frac{M}{M-1}\right)$	$2\frac{I}{I_c}$	$\frac{R}{M^2\left(\frac{2-M}{M-1}+\frac{2m_a/m_1}{1+\frac{m_a}{m_1}}\right)}$
Buck–boost	0	$2\frac{I_1}{I_c}$	$\frac{-R}{M^2}\frac{\left(1+\frac{m_a}{m_1}\right)}{\left(1-\frac{m_a}{m_1}\right)}$

Table 12.8 Current programmed DCM small-signal equivalent circuit parameters: output port

Converter	g_2	f_2	r_2
Buck	$\frac{1}{R}\left(\frac{M}{1-M}\right)\frac{\left(\frac{m_a}{m_1}(2-M)-M\right)}{\left(1+\frac{m_a}{m_1}\right)}$	$2\frac{I}{I_c}$	$R\frac{(1-M)\left(1+\frac{m_a}{m_1}\right)}{\left(1-2M+\frac{m_a}{m_1}\right)}$
Boost	$\frac{1}{R}\left(\frac{M}{M-1}\right)$	$2\frac{I_2}{I_c}$	$R\left(\frac{M-1}{M}\right)$
Buck–boost	$\frac{2M}{R}\frac{\left(\frac{m_a}{m_1}\right)}{\left(1+\frac{m_a}{m_1}\right)}$	$2\frac{I_2}{I_c}$	R

each switching period. As a result, the current programmed controller does not exhibit the type of instability described in Section 12.1. The current programmed controllers of DCM boost and buck–boost converters are stable for all duty cycles with no artificial ramp. However, the CPM DCM buck converter exhibits a different type of low-frequency instability when $M > 2/3$ and $m_a = 0$, that arises because the dc output characteristic is nonlinear and can exhibit two equilibrium points when the converter drives a resistive load. The stability range can be extended to $0 \le D \le 1$ by addition of an artificial ramp having slope $m_a > 0.086\, m_2$, or by addition of output voltage feedback.

Small-signal models of DCM CPM converters can be derived by perturbation and linearization of the averaged models of Figs. 12.32 and 12.34. The results are given in Fig. 12.35. Parameters of the small-signal models are listed in Tables 12.7 and 12.8.

The CPM DCM small-signal models of Fig. 12.35 are quite similar to the respective small-signal models of DCM duty-ratio controlled converters illustrated in Figs. 11.15 and 11.17. The sole differences are the parameter expressions of Tables 12.7 and 12.8. Transfer functions can be determined in a

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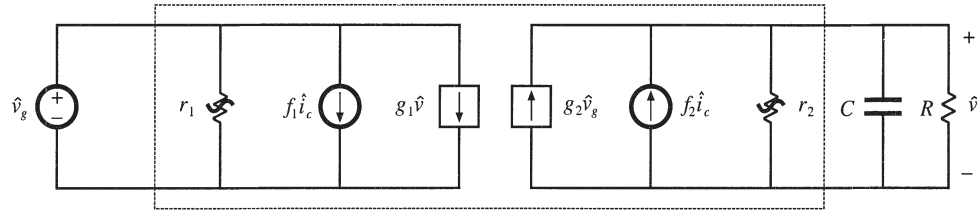


Fig. 12.36 Simplified small-signal model obtained by letting L become zero in Fig. 12.35 (a), (b), or (c).

similar manner. In particular, a simple approximate way to determine the low-frequency small-signal transfer functions of the CPM DCM buck, boost, and buck-boost converters is to simply let the inductance L tend to zero in the equivalent circuits of Fig. 12.35. This approximation is justified for frequencies sufficiently less than the converter switching frequency, because in the discontinuous conduction mode the value of L is small, and hence the pole and any RHP zero associated with L occur at frequencies near to or greater than the switching frequency. For all three converters, the equivalent circuit of Fig. 12.36 is obtained.

Figure 12.36 predicts that the control-to-output transfer function $G_{vc}(s)$ is

$$G_{vc}(s) = \left.\frac{\hat{v}}{\hat{i}_c}\right|_{\hat{v}_g = 0} = \frac{G_{c0}}{1 + \frac{s}{\omega_p}} \tag{12.121}$$

with

$$G_{c0} = f_2\left(R \| r_2\right)$$
$$\omega_p = \frac{1}{\left(R \| r_2\right) C}$$

The line-to-output transfer function is predicted to be

$$G_{vg}(s) = \left.\frac{\hat{v}}{\hat{v}_g}\right|_{\hat{i}_c = 0} = \frac{G_{g0}}{1 + \frac{s}{\omega_p}} \tag{12.122}$$

with

$$G_{g0} = g_2\left(R \| r_2\right)$$

If desired, more accurate expressions which account for inductor dynamics can be derived by solution of the models of Fig. 12.35.

12.5 SUMMARY OF KEY POINTS

1. In current-programmed control, the peak switch current $i_s(t)$ follows the control input $i_c(t)$. This widely used control scheme has the advantage of a simpler control-to-output transfer function. The line-to-output transfer functions of current-programmed buck converters are also reduced.

2. The basic current-programmed controller is unstable when $D > 0.5$, regardless of the converter topology. The controller can be stabilized by addition of an artificial ramp having slope m_a. When $m_a > 0.5m_2$, then the controller is stable for all duty cycles.

3. The behavior of current-programmed converters can be modeled in a simple and intuitive manner by the first-order approximation $\langle i_L(t) \rangle_{T_s} \approx i_c(t)$. The averaged terminal waveforms of the switch network can then be modeled simply by a current source of value i_c, in conjunction with a power sink or power source element. Perturbation and linearization of these elements leads to the small-signal model. Alternatively, the small-signal converter equations derived in Chapter 7 can be adapted to cover the current programmed mode, using the simple approximation $i_L(t) \approx i_c(t)$.

4. The simple model predicts that one pole is eliminated from the converter line-to-output and control-to-output transfer functions. Current programming does not alter the transfer function zeroes. The dc gains become load-dependent.

5. The more accurate model of Section 12.3 correctly accounts for the difference between the average inductor current $\langle i_L(t) \rangle_{T_s}$ and the control input $i_c(t)$. This model predicts the nonzero line-to-output transfer function $G_{vg}(s)$ of the buck converter. The current-programmed controller behavior is modeled by a block diagram, which is appended to the small-signal converter models derived in Chapter 7. Analysis of the resulting multiloop feedback system then leads to the relevant transfer functions.

6. The more accurate model predicts that the inductor pole occurs at the crossover frequency f_c of the effective current feedback loop gain $T_i(s)$. The frequency f_c typically occurs in the vicinity of the converter switching frequency f_s. The more accurate model also predicts that the line-to-output transfer function $G_{vg}(s)$ of the buck converter is nulled when $m_a = 0.5m_2$.

7. Current programmed converters operating in the discontinuous conduction mode are modeled in Section 12.4. The averaged transistor waveforms can be modeled by a power sink, while the averaged diode waveforms are modeled by a power source. The power is controlled by $i_c(t)$. Perturbation and linearization of these averaged models, as usual, leads to small-signal equivalent circuits.

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PROBLEMS

12.1 A nonideal buck converter operates in the continuous conduction mode, with the values $V_g = 10$ V, $f_2 = 100$ kHz, $L = 4$ μH, $C = 75$ μF, and $R = 0.25$ Ω. The desired full-load output is 5 V at 20 A. The power stage contains the following loss elements: MOSFET on-resistance $R_{on} = 0.1$ Ω, Schottky diode forward voltage drop $V_D = 0.5$ V, inductor winding resistance $R_L = 0.03$ Ω.

(a) Steady-state analysis: determine the converter steady-state duty cycle D, the inductor current ripple slopes m_1 and m_2, and the dimensionless parameter $K = 2L/RT_s$.

(b) Determine the small-signal equations for this converter, for duty cycle control.

A current-programmed controller is now implemented for this converter. An artificial ramp is used, having a fixed slope $M_a = 0.5M_2$, where M_2 is the steady-state slope m_2 obtained with an output of 5 V at 20 A.

(c) Over what range of D is the current programmed controller stable? Is it stable at rated output? Note that the nonidealities affect the stability boundary.

(d) Determine the control-to-output transfer function $G_{vc}(s)$, using the simple approximation $\langle i_L(t) \rangle_{T_s} \approx i_c(t)$. Give analytical expressions for the corner frequency and dc gain. Sketch the Bode plot of $G_{vc}(s)$.

12.2 Use the averaged switch modeling approach to model the CCM boost converter with current-programmed control:

(a) Define the switch network terminal quantities as in Fig. 7.46(a). With the assumption that $\langle i_L(t) \rangle_{T_s} \approx i_c(t)$, determine expressions for the average values of the switch network terminal waveforms, and hence derive the equivalent circuit of Fig. 12.18(a).

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(b) Perturb and linearize your model of part (a), to obtain the equivalent circuit of Fig. 12.22.

(c) Solve your model of part (b), to derive expressions for the control-to-output transfer function $G_{vc}(s)$ and the line-to-output transfer function $G_{vg}(s)$. Express your results in standard normalized form, and give analytical expressions for the corner frequencies and dc gains.

12.3 Use the averaged switch modeling approach to model the CCM Ćuk converter with current-programmed control. A Ćuk converter is diagrammed in Fig. 2.20.

(a) It is desired to model the switch network with an i_c current source and a dependent power source or sink, using the approach of Section 12.2.2. How should the switch network terminal voltages and currents be defined?

(b) Sketch the switch network terminal voltage and current waveforms. With the assumption that $\langle i_1(t)\rangle_{T_s} - \langle i_2(t)\rangle_{T_s} \approx i_c(t)$ (where i_1 and i_2 are the inductor currents defined in Fig. 2.20), determine expressions for the average values of the switch network terminal waveforms, and hence derive an equivalent circuit similar to the equivalent circuits of Fig. 12.18.

(c) Perturb and linearize your model of part (b), to obtain a small signal equivalent circuit similar to the model of Fig. 12.19. It is not necessary to solve your model.

12.4 The full-bridge converter of Fig. 6.19(a) operates with $V_g = 320$ V, and supplies 1000 W to a 42 V resistive load. Losses can be neglected, the duty cycle is 0.7, and the switching period T_s defined in Fig. 6.20 is 10 μsec. $L = 50$ μH and $C = 100$ μF. A current-programmed controller is employed, whose waveforms are referred to the secondary side of the transformer. In the following calculations, you may neglect the transformer magnetizing current.

(a) What is the minimum artificial ramp slope m_a that will stabilize the controller at the given operating point? Express your result in terms of m_2.

(b) An artificial ramp having the slope $m_a = m_2$ is employed. Sketch the Bode plot of the current loop gain $T_i(s)$, and label numerical values of the corner frequencies and dc gains. It is not necessary to re-derive the analytical expression for T_i. Determine the crossover frequency f_c.

(c) For $m_a = m_2$, sketch the Bode plots of the control-to-output transfer function $G_{vc}(s)$ and line-to-output transfer function $G_{vg}(s)$, and label numerical values of the corner frequencies and dc gains. It is not necessary to re-derive analytical expressions for these transfer functions.

12.5 In a CCM current-programmed buck converter, it is desired to minimize the line-to-output transfer function $G_{vg}(s)$ via the choice $m_a = 0.5m_2$. However, because of component tolerances, the value of inductance L can vary by ±10% from its nominal value of 100 μH. Hence, m_a is fixed in value while m_2 varies, and $m_a = 0.5m_2$ is obtained only at the nominal value of L. The switching frequency is 100 kHz, the output voltage is 15 V, the load current varies over the range 2 to 4 A, and the input voltage varies over the range 22 to 32 V. You may neglect losses. Determine the worst-case (maximum) value of the line-to-output dc gain $G_{vg}(0)$.

12.6 The nonideal flyback converter of Fig. 7.18 employs current-programmed control, with artificial ramp having slope m_a. MOSFET Q_1 exhibits on-resistance R_{on}. All current programmed controller waveforms are referred to the transformer primary side.

(a) Derive a block diagram which models the current-programmed controller, of form similar to Fig. 12.24. Give analytical expressions for the gains in your block diagram.

(b) Combine your result of part (a) with the converter small-signal model. Derive a new expression for the control-to-output transfer function $G_{vc}(s)$.

12.7 A buck converter operates with current-programmed control. The element values are:

$V_g = 120$ V	$D = 0.6$
$R = 10$ Ω	$f_s = 100$ kHz
$L = 550$ μH	$C = 100$ μF

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An artificial ramp is employed, having slope 0.15 A/μsec.

(a) Construct the magnitude and phase asymptotes of the control-to-output transfer function $G_{vd}(s)$ for duty-cycle control. On the same plot, construct the magnitude and phase asymptotes of the control-to-output transfer function $G_{vc}(s)$ for current-programmed control. Compare.

(b) Construct the magnitude asymptotes of the line-to-output transfer function $G_{vg}(s)$ for duty-cycle control. On the same plot, construct the magnitude asymptotes of the line-to-output transfer function $G_{vg\text{-}cpm}(s)$ for current-programmed control. Compare.

12.8 A buck-boost converter operates in the discontinuous conduction mode. Its current-programmed controller has no compensating artificial ramp: $m_a = 0$.

(a) Derive an expression for the control-to-output transfer function $G_{vc}(s)$, using the approximation $L \approx 0$. Give analytical expressions for the corner frequency and dc gain.

(b) Repeat part (a), with the inductor included. Show that, provided the inductor is sufficiently small, then the inductor merely adds a high-frequency pole and zero to $G_{vc}(s)$, and the low-frequency pole derived in part (a) is essentially unchanged.

(c) At the CCM-DCM boundary, what is the minimum value of the RHP zero frequency?

12.9 A current-programmed boost converter interfaces a 3 V battery to a small portable 5 V load. The converter operates in the discontinuous conduction mode, with constant transistor on-time t_{on} and variable off-time; the switching frequency can therefore vary and is used as the control variable. There is no artificial ramp, and the peak transistor current i_c is equal to a fixed value I_c; in practice, I_c is chosen to minimize the total loss.

(a) Sketch the transistor and diode voltage and current waveforms. Determine expressions for the waveform average values, and hence derive a large-signal averaged equivalent circuit for this converter.

(b) Perturb and linearize your model of part (a), to obtain a small-signal equivalent circuit. Note that the switching frequency f_s should be perturbed.

(c) Solve your model of part (b), to derive an expression for the low-frequency control-to-output transfer function $G_{vf}(s) = \hat{v}(s)/\hat{f}_s(s)$. Express your results in standard normalized form, and give analytical expressions for the corner frequencies and dc gains. You may assume that L is small.

12.10 A current-programmed boost converter is employed in a low-harmonic rectifier system, in which the input voltage is a rectified sinusoid: $v_g(t) = V_M \mid \sin(\omega t) \mid$. The dc output voltage is $v(t) = V > V_M$. The capacitance C is large, such that the output voltage contains negligible ac variations. It is desired to control the converter such that the input current $i_g(t)$ is proportional to $v_g(t)$: $i_g(t) = v_g(t)/R_e$, where R_e is a constant, called the "emulated resistance." The averaged boost converter model of Fig. 12.18(a) suggests that this can be accomplished by simply letting $i_c(t)$ be proportional to $v_g(t)$, according to $i_c(t) = v_g(t)/R_e$. You may make the simplifying assumption that the converter always operates in the continuous conduction mode.

(a) Solve the model of Fig. 12.18(a), subject to the assumptions listed above, to determine the power $\langle p(t) \rangle_{T_s}$. Find the average value of $\langle p(t) \rangle_{T_s}$, averaged over one cycle of the ac input $v_g(t)$.

(b) An artificial ramp is necessary to stabilize the current-programmed controller at some operating points. What is the minimum value of m_a that ensures stability at all operating points along the input rectified sinusoid? Express your result as a function of V and L. Show your work.

(c) The artificial ramp and inductor current ripple cause the average input current to differ from $i_c(t)$. Derive an algebraic expression for $\langle i_g(t) \rangle_{T_s}$, as a function of $i_c(t)$ and other quantities such as m_a, $v_g(t)$, V, L, and T_s. For this part, you may assume that the inductor dynamics are negligible. Show your work.

(d) Substitute $v_g(t) = V_M \mid \sin(\omega t) \mid$ and $i_c(t) = v_g(t)/R_e$, into your result of part (c), to determine an expression for $i_g(t)$. How does $i_g(t)$ differ from a rectified sinusoid?

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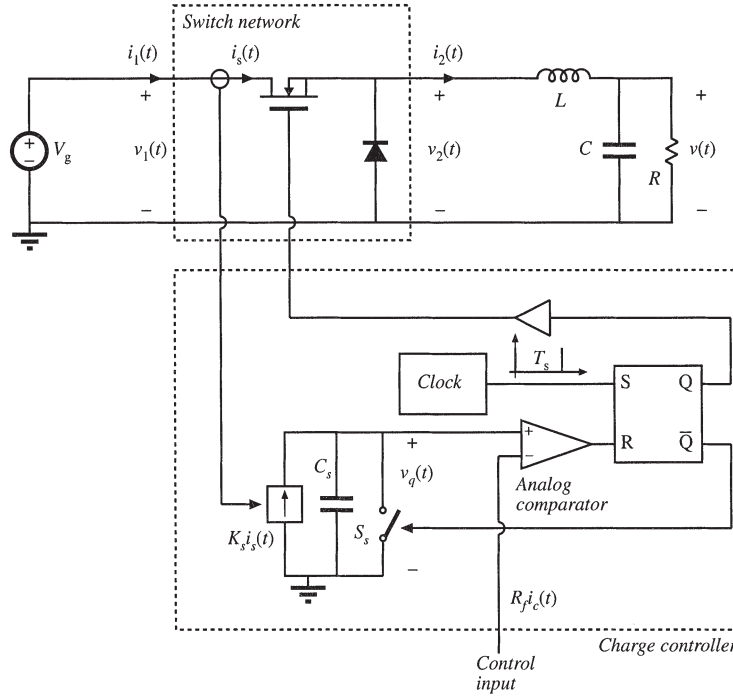


Fig. 12.37 Buck converter with charge controller, Problem 12.11.

12.11 Figure 12.37 shows a buck converter with a charge controller [14]. Operation of the charge controller is similar to operation of the current-programmed controller. At the beginning of each switching period, at time $t = 0$, a short clock pulse sets the SR latch. The logic high signal at the Q output of the latch turns the power MOSFET on. At the same time, the logic low signal at the $\overline{Q}$ output of the latch turns the switch S_s off. Current $K_s i_s$ proportional to the power MOSFET current charges the capacitor C_s. At $t = dT_s$, the capacitor voltage $v_q(t)$ reaches the control input voltage $R_f i_c$, the comparator output goes high and resets the latch. The logic low signal at the Q output of the latch turns the power MOSFET off. At the same time, the logic high signal at the $\overline{Q}$ output of the latch turns the switch S_s on, which quickly discharges the capacitor C_s to zero.

In this problem, the converter and controller parameters are: $V_g = 24$ V, $f_s = 1/T_s = 100$ kHz, $L = 60$ μH, $C = 100$ μF, $R = 3\ \Omega$, $K_s T_s / C_s = R_f = 1\ \Omega$. You can assume that the converter operates in continuous conduction mode.

(a) Find expressions for the average values of the switch network terminal waveforms, and hence derive a large-signal averaged switch model of the buck switch network with charge control. The control input to the model is the control current i_c. The averaged switch model should consist of a current source and a power source. The switch duty cycle d should not appear in the model.

(b) Using the averaged switch model derived in part (a), find an expression for the quiescent output voltage V as a function of V_g, I_c, and R. Given $I_c = 2$ A, find numerical values for V, I_1, I_2, and the duty cycle D. For this quiescent operating point, sketch the waveforms $i_1(t)$, $i_2(t)$, and $v_q(t)$ during one switching period.

(c) Perturb and linearize the averaged switch model from part (a) to derive a small-signal averaged switch model for the buck switch network with charge control. Find analytical expressions for

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all parameter values in terms of the converter parameters and the quiescent operating conditions. Sketch the complete small-signal model of the buck converter with the charge controller.

(d) Solve the model obtained in part (c) to find the control-to-output transfer function $G_{vc}(s) = \hat{v}/\hat{t}_c$. At the quiescent operating point found in part (b), construct the Bode plot for the magnitude of G_{vc} and label all salient features of the magnitude response.

(e) Comment on advantages charge control may have compared to duty-cycle control or current-programmed control.

12.12 Figure 12.38 shows a buck converter with a one-cycle controller [15]. Operation of the one-cycle controller is similar to operation of the current-programmed controller. At the beginning of each switching period, at time $t = 0$, a short clock pulse sets the SR latch. The logic high signal at the Q output of the latch turns the power MOSFET on. At the same time, the logic low signal at the $\overline{Q}$ output of the latch turns the switch S_s off. Current $G_s v_2(t)$ proportional to the voltage $v_2(t)$ charges the capacitor C_s. At $t = dT_s$, the capacitor voltage $v_s(t)$ reaches the control input voltage v_c, the comparator output goes high and resets the latch. The logic low signal at the Q output of the latch turns the power MOSFET off. At the same time, the logic high signal at the $\overline{Q}$ output of the latch turns the switch S_s on, which quickly discharges the capacitor C_s to zero.

In this problem, the converter and controller parameters are: $V_g = 24$ V, $f_s = 1/T_s = 100$ kHz, $L = 60$ μH, $C = 100$ μF, $R = 3\ \Omega$, $G_s T_s / C_s = 1$. You can assume that the converter operates in the continuous conduction mode.

(a) Find expressions for the average values of the switch network terminal waveforms, and hence derive a large-signal averaged switch model of the buck switch network with one-cycle control. The control input to the model is the control voltage v_c. The switch duty cycle d should not appear in the model.

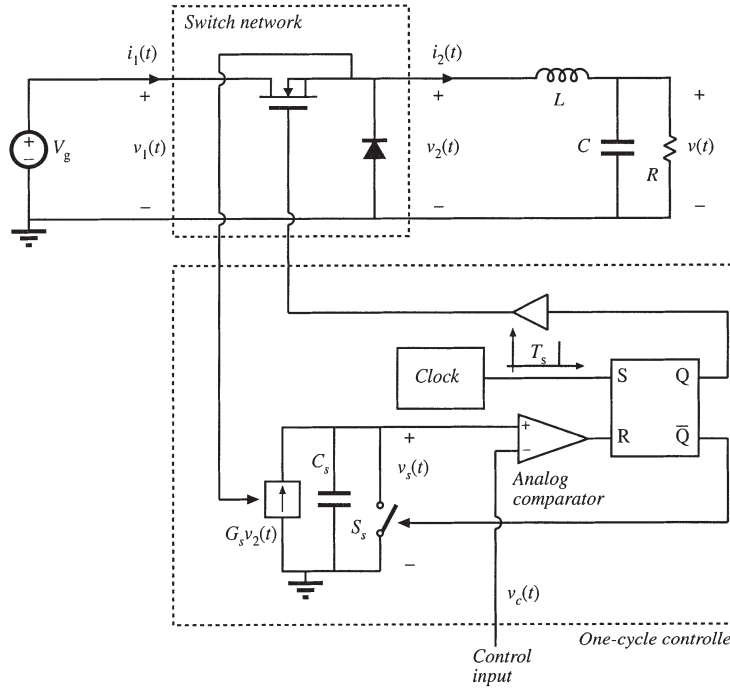


Fig. 12.38 Buck converter with one-cycle controller, Problem 12.12.

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(b) Using the averaged switch model derived in part (a), find an expression for the quiescent output voltage V as a function of V_c. Given $V_c = 10$ V, find the numerical values for V, I_1, I_2, and the duty cycle D. For this quiescent operating point, sketch the waveforms $i_1(t)$, $i_2(t)$, and $v_s(t)$ during one switching period.

(c) Perturb and linearize the averaged switch model from part (a) to derive a small-signal averaged switch model for the buck switch network with one-cycle control. Find analytical expressions for all parameter values in terms of the converter parameters and the quiescent operating conditions. Sketch the complete small-signal model of the buck converter with the one-cycle controller.

(d) Solve the model obtained in part (c) to find the control-to-output transfer function $G_{vc}(s) = \hat{v}/\hat{v}_c$, and the line-to-output transfer function $G_{vg}(s) = \hat{v}/\hat{v}_g$. For the quiescent operating point found in part (b), sketch the magnitude Bode plots of these transfer functions, and label all salient features.

(e) Comment on advantages one-cycle control may have compared to duty-cycle control.

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Part III

Magnetics

13

Basic Magnetics Theory

Magnetics are an integral part of every switching converter. Often, the design of the magnetic devices cannot be isolated from the converter design. The power electronics engineer must not only model and design the converter, but must model and design the magnetics as well. Modeling and design of magnetics for switching converters is the topic of Part III of this book.

In this chapter, basic magnetics theory is reviewed, including magnetic circuits, inductor modeling, and transformer modeling [1-5]. Loss mechanisms in magnetic devices are described. Winding eddy currents and the proximity effect, a significant loss mechanism in high-current high-frequency windings, are explained in detail [6-11]. Inductor design is introduced in Chapter 14, and transformer design is covered in Chapter 15.

13.1 REVIEW OF BASIC MAGNETICS

13.1.1 Basic Relationships

The basic magnetic quantities are illustrated in Fig. 13.1. Also illustrated are the analogous, and perhaps more familiar, electrical quantities. The *magnetomotive force* $\mathcal{F}$, or scalar potential, between two points x_1 and x_2 is given by the integral of the magnetic field $\boldsymbol{H}$ along a path connecting the points:

$$\mathcal{F} = \int_{x_1}^{x_2} \boldsymbol{H} \cdot d\boldsymbol{\ell} \tag{13.1}$$

where $d\boldsymbol{\ell}$ is a vector length element pointing in the direction of the path. The dot product yields the com-

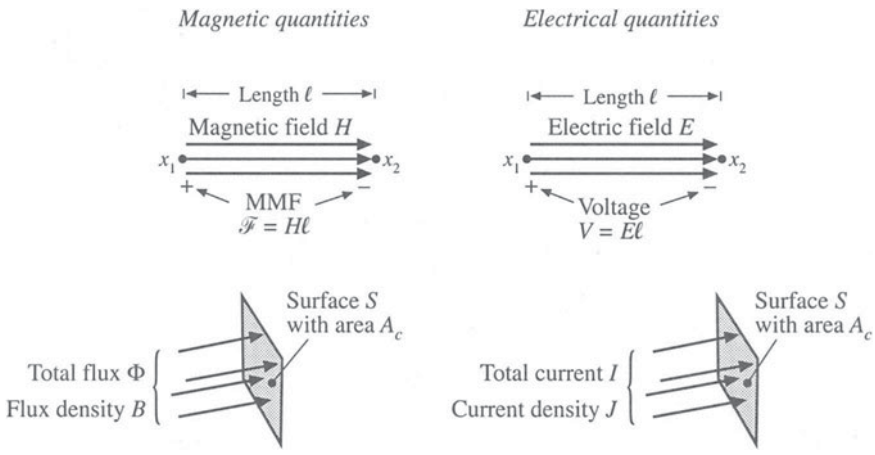


Fig. 13.1 Comparison of magnetic field H, MMF Φ, flux $\mathscr{F}$, and flux density B, with the analogous electrical quantities E, V, I, and J.

ponent of $\boldsymbol{H}$ in the direction of the path. If the magnetic field is of uniform strength H passing through an element of length ℓ as illustrated, then Eq. (13.1) reduces to

$$\mathscr{F} = H\ell \tag{13.2}$$

This is analogous to the electric field of uniform strength E, which induces a voltage $V = E\ell$ between two points separated by distance ℓ.

Figure 13.1 also illustrates a total magnetic flux Φ passing through a surface S having area A_c. The total flux Φ is equal to the integral of the normal component of the flux density B over the surface

$$\Phi = \int_{\text{surface } S} \boldsymbol{B} \cdot d\boldsymbol{A} \tag{13.3}$$

where $d\boldsymbol{A}$ is a vector area element having direction normal to the surface. For a uniform flux density of magnitude B as illustrated, the integral reduces to

$$\Phi = BA_c \tag{13.4}$$

Flux density $\boldsymbol{B}$ is analogous to the electrical current density $\boldsymbol{J}$, and flux Φ is analogous to the electric current I. If a uniform current density of magnitude J passes through a surface of area A_c, then the total current is $I = JA_c$.

Faraday's law relates the voltage induced in a winding to the total flux passing through the interior of the winding. Figure 13.2 illustrates flux $\Phi(t)$ passing through the interior of a loop of wire. The loop encloses cross-sectional area A_c. According to Faraday's law, the flux induces a voltage $v(t)$ in the wire, given by

$$v(t) = \frac{d\Phi(t)}{dt} \tag{13.5}$$

where the polarities of $v(t)$ and $\Phi(t)$ are defined according to the right-hand rule, as in Fig. 13.2. For a

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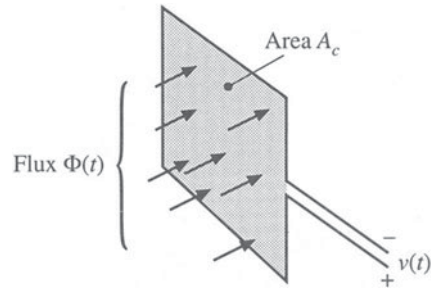


Fig. 13.2 The voltage $v(t)$ induced in a loop of wire is related by Faraday's law to the derivative of the total flux $\Phi(t)$ passing through the interior of the loop.

uniform flux distribution, we can express $v(t)$ in terms of the flux density $B(t)$ by substitution of Eq. (13.4):

$$v(t) = A_c \frac{dB(t)}{dt} \tag{13.6}$$

Thus, the voltage induced in a winding is related to the flux Φ and flux density B passing through the interior of the winding.

Lenz's law states that the voltage $v(t)$ induced by the changing flux $\Phi(t)$ in Fig. 13.2 is of the polarity that tends to drive a current through the loop to counteract the flux change. For example, consider the shorted loop of Fig. 13.3. The changing flux $\Phi(t)$ passing through the interior of the loop induces a voltage $v(t)$ around the loop. This voltage, divided by the impedance of the loop conductor, leads to a current $i(t)$ as illustrated. The current $i(t)$ induces a flux $\Phi'(t)$, which tends to oppose the changes in $\Phi(t)$. Lenz's law is invoked later in this chapter, to provide a qualitative understanding of eddy current phenomena.

Ampere's law relates the current in a winding to the magnetomotive force $\mathcal{F}$ and magnetic field $\boldsymbol{H}$. The net MMF around a closed path of length ℓ_m is equal to the total current passing through the interior of the path. For example, Fig. 13.4 illustrates a magnetic core, in which a wire carrying current $i(t)$ passes through the window in the center of the core. Let us consider the closed path illustrated, which follows the magnetic field lines around the interior of the core. Ampere's law states that

$$\oint_{\text{closed path}} \boldsymbol{H} \cdot d\boldsymbol{\ell} = \text{total current passing through interior of path} \tag{13.7}$$

The total current passing through the interior of the path is equal to the total current passing through the

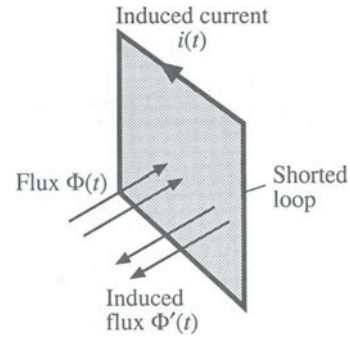


Fig. 13.3 Illustration of Lenz's law in a shorted loop of wire. The flux $\Phi(t)$ induces current $i(t)$, which in turn generates flux $\Phi'(t)$ that tends to oppose changes in $\Phi(t)$.

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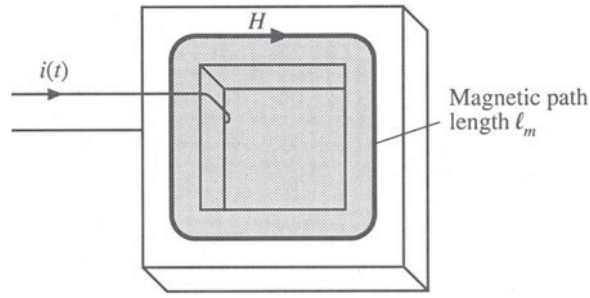


Fig. 13.4 The net MMF around a closed path is related by Ampere's law to the total current passing through the interior of the path.

window in the center of the core, or $i(t)$. If the magnetic field is uniform and of magnitude $H(t)$, then the integral is $H(t)\ell_m$. So for the example of Fig. 13.4, Eq. (13.7) reduces to

$$\mathcal{F}(t) = H(t)\ell_m = i(t) \tag{13.8}$$

Thus, the magnetic field strength $H(t)$ is related to the winding current $i(t)$. We can view winding currents as sources of MMF. Equation (13.8) states that the MMF around the core, $\mathcal{F}(t) = H(t)\ell_m$, is equal to the winding current MMF $i(t)$. The total MMF around the closed loop, accounting for both MMFs, is zero.

The relationship between $\boldsymbol{B}$ and $\boldsymbol{H}$, or equivalently between Φ and $\mathcal{F}$, is determined by the core material characteristics. Figure 13.5(a) illustrates the characteristics of free space, or air:

$$\boldsymbol{B} = \mu_0 \boldsymbol{H} \tag{13.9}$$

The quantity μ_0 is the permeability of free space, and is equal to $4\pi \cdot 10^{-7}$ Henries per meter in MKS units. Figure 13.5(b) illustrates the *B–H* characteristic of a typical iron alloy under high-level sinusoidal steady-state excitation. The characteristic is highly nonlinear, and exhibits both *hysteresis* and *saturation*. The exact shape of the characteristic is dependent on the excitation, and is difficult to predict for arbitrary waveforms.

For purposes of analysis, the core material characteristic of Fig. 13.5(b) is usually modeled by the linear or piecewise-linear characteristics of Fig. 13.6. In Fig. 13.6(a), hysteresis and saturation are ignored. The *B–H* characteristic is then given by

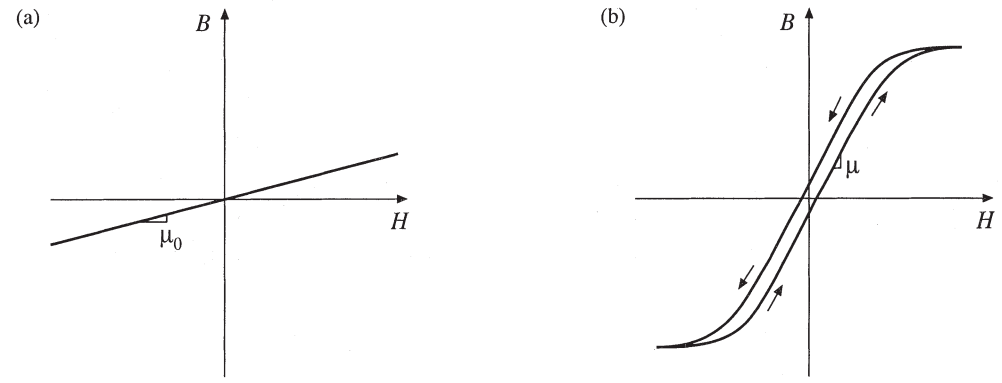


Fig. 13.5 *B–H* characteristics: (a) of free space or air, (b) of a typical magnetic core material.

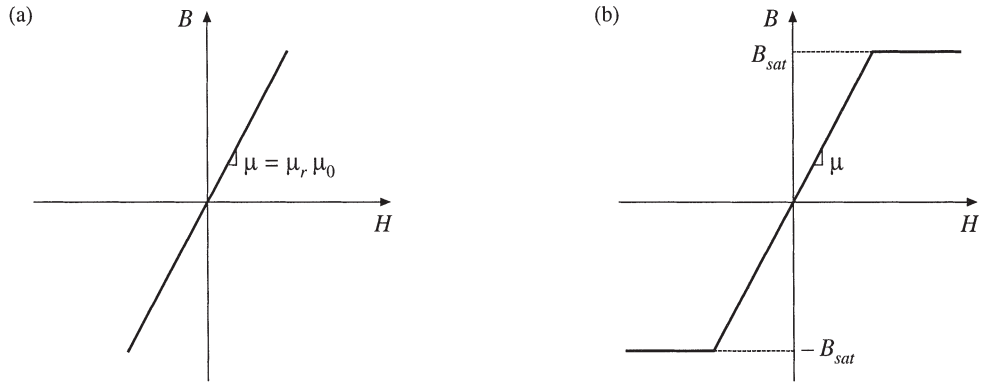


Fig. 13.6 Approximation of the *B–H* characteristics of a magnetic core material: (a) by neglecting both hysteresis and saturation, (b) by neglecting hysteresis.

$$\begin{aligned} \boldsymbol{B} &= \mu \boldsymbol{H} \\ \mu &= \mu_r \mu_0 \end{aligned} \tag{13.10}$$

The core material permeability μ can be expressed as the product of the relative permeability μ_r and of μ_0. Typical values of μ_r lie in the range 10^3 to 10^5.

The piecewise-linear model of Fig. 13.6(b) accounts for saturation but not hysteresis. The core material saturates when the magnitude of the flux density B exceeds the saturation flux density B_{sat}. For $|B| < B_{sat}$, the characteristic follows Eq. (13.10). When $|B| > B_{sat}$, the model predicts that the core reverts to free space, with a characteristic having a much smaller slope approximately equal to μ_0. Square-loop materials exhibit this type of abrupt-saturation characteristic, and additionally have a very large relative permeability μ_r. Soft materials exhibit a less abrupt saturation characteristic, in which μ gradually decreases as H is increased. Typical values of B_{sat} are 1 to 2 Tesla for iron laminations and silicon steel, 0.5 to 1 Tesla for powdered iron and molypermalloy materials, and 0.25 to 0.5 Tesla for ferrite materials.

Unit systems for magnetic quantities are summarized in Table 13.1. The MKS system is used throughout this book. The unrationalized cgs system also continues to find some use. Conversions between these systems are listed.

Figure 13.7 summarizes the relationships between the basic electrical and magnetic quantities of a magnetic device. The winding voltage $v(t)$ is related to the core flux and flux density via Faraday's

Table 13.1 Units for magnetic quantities

Quantity	MKS	Unrationalized cgs	Conversions
Core material equation	$B = \mu_0 \mu_r H$	$B = \mu_r H$	
B	Tesla	Gauss	$1\ \text{T} = 10^4\ \text{G}$
H	Ampere/meter	Oersted	$1\ \text{A/m} = 4\pi \cdot 10^{-3}\ \text{Oe}$
Φ	Weber	Maxwell	$1\ \text{Wb} = 10^8\ \text{Mx}$ $1\ \text{T} = 1\ \text{Wb/m}^2$

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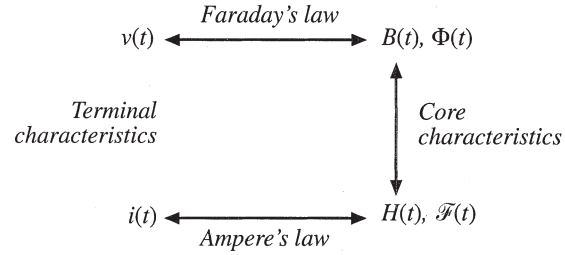


Fig. 13.7 Summary of the steps in determination of the terminal electrical *i–v* characteristics of a magnetic element.

law. The winding current $i(t)$ is related to the magnetic field strength via Ampere's law. The core material characteristics relate B and H.

We can now determine the electrical terminal characteristics of the simple inductor of Fig. 13.8(a). A winding of n turns is placed on a core having permeability μ. Faraday's law states that the flux $\Phi(t)$ inside the core induces a voltage $v_{turn}(t)$ in each turn of the winding, given by

$$v_{turn}(t) = \frac{d\Phi(t)}{dt} \tag{13.11}$$

Since the same flux $\Phi(t)$ passes through each turn of the winding, the total winding voltage is

$$v(t) = nv_{turn}(t) = n\frac{d\Phi(t)}{dt} \tag{13.12}$$

Equation (13.12) can be expressed in terms of the average flux density $B(t)$ by substitution of Eq. (13.4):

$$v(t) = nA_c\frac{dB(t)}{dt} \tag{13.13}$$

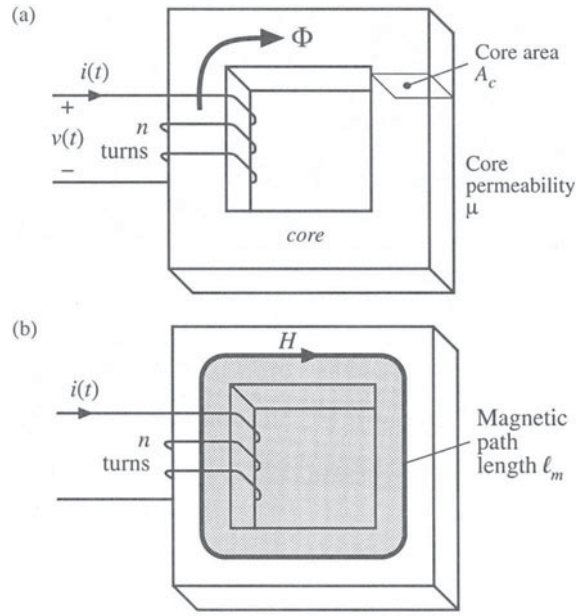


Fig. 13.8 Inductor example: (a) inductor geometry, (b) application of Ampere's law.

where the average flux density $B(t)$ is $\Phi(t)/A_c$.

The use of Ampere's law is illustrated in Fig. 13.8(b). A closed path is chosen which follows an average magnetic field line around the interior of the core. The length of this path is called the *mean magnetic path length* ℓ_m. If the magnetic field strength $H(t)$ is uniform, then Ampere's law states that $H\ell_m$ is equal to the total current passing through the interior of the path, that is, the net current passing through the window in the center of the core. Since there are n turns of wire passing through the window, each carrying current $i(t)$, the net current passing through the window is $ni(t)$. Hence, Ampere's law states that

$$H(t)\ell_m = ni(t) \tag{13.14}$$

Let us model the core material characteristics by neglecting hysteresis but accounting for saturation, as follows:

$$B = \begin{cases} B_{sat} & \text{for } H \geq B_{sat}/\mu \\ \mu H & \text{for } |H| < B_{sat}/\mu \\ -B_{sat} & \text{for } H \leq -B_{sat}/\mu \end{cases} \tag{13.15}$$

The B–H characteristic saturated slope μ_0 is much smaller than μ, and is ignored here. A characteristic similar to Fig. 13.6(b) is obtained. The current magnitude I_{sat} at the onset of saturation can be found by substitution of $H = B_{sat}/\mu$ into Eq. (13.14). The result is

$$I_{sat} = \frac{B_{sat}\ell_m}{\mu n} \tag{13.16}$$

We can now eliminate B and H from Eqs. (13.13) to (13.15), and solve for the electrical terminal characteristics. For $|I| < I_{sat}$, $B = \mu H$. Equation (13.13) then becomes

$$v(t) = \mu n A_c \frac{dH(t)}{dt} \tag{13.17}$$

Substitution of Eq. (13.14) into Eq. (13.17) to eliminate $H(t)$ then leads to

$$v(t) = \frac{\mu n^2 A_c}{\ell_m} \frac{di(t)}{dt} \tag{13.18}$$

which is of the form

$$v(t) = L \frac{di(t)}{dt} \tag{13.19}$$

with

$$L = \frac{\mu n^2 A_c}{\ell_m} \tag{13.20}$$

So the device behaves as an inductor for $|I| < I_{sat}$. When $|I| > I_{sat}$, then the flux density $B(t) = B_{sat}$ is constant. Faraday's law states that the terminal voltage is then

$$v(t) = nA_c \frac{dB_{sat}}{dt} = 0 \tag{13.21}$$

When the core saturates, the magnetic device behavior approaches a short circuit. The device behaves as an inductor only when the winding current magnitude is less than I_{sat}. Practical inductors exhibit some small residual inductance due to their nonzero saturated permeabilities; nonetheless, in saturation the inductor impedance is greatly reduced, and large inductor currents may result.

13.1.2 Magnetic Circuits

Figure 13.9(a) illustrates uniform flux and magnetic field inside a element having permeability μ, length ℓ, and cross-sectional area A_c. The MMF between the two ends of the element is

$$\mathcal{F} = H\ell \tag{13.22}$$

Since $H = B/\mu$ and $B = \Phi/A_c$, we can express $\mathcal{F}$ as

$$\mathcal{F} = \frac{\ell}{\mu A_c}\Phi \tag{13.23}$$

This equation is of the form

$$\mathcal{F} = \Phi\mathcal{R} \tag{13.24}$$

with

$$\mathcal{R} = \frac{\ell}{\mu A_c} \tag{13.25}$$

Equation (13.24) resembles Ohm's law. This equation states that the magnetic flux through an element is proportional to the MMF across the element. The constant of proportionality, or the reluctance $\mathcal{R}$, is analogous to the resistance R of an electrical conductor. Indeed, we can construct a lumped-element magnetic circuit model that corresponds to Eq. (13.24), as in Fig. 13.9(b). In this magnetic circuit model, voltage and current are replaced by MMF and flux, while the element characteristic, Eq. (13.24), is represented by the analog of a resistor, having reluctance $\mathcal{R}$.

Complicated magnetic structures, composed of multiple windings and multiple heterogeneous

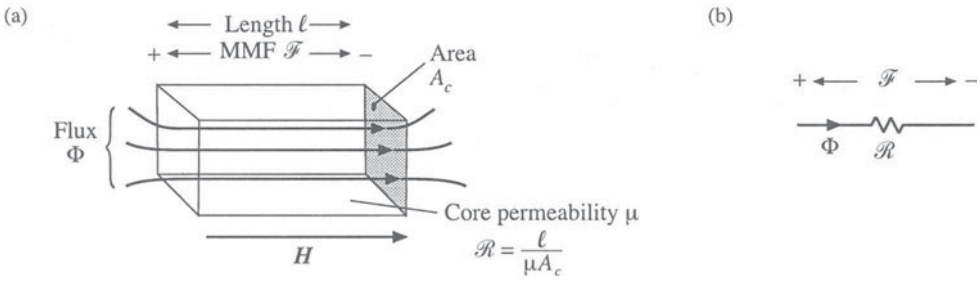


Fig. 13.9 An element containing magnetic flux (a), and its equivalent magnetic circuit (b).

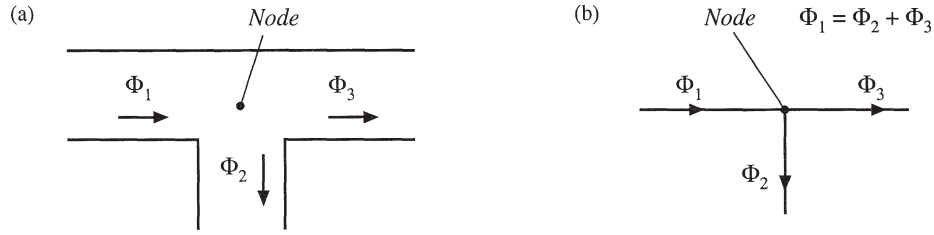


Fig. 13.10 Kirchoff's current law, applied to magnetic circuits: the net flux entering a node must be zero: (a) physical element, in which three legs of a core meet at a node; (b) magnetic circuit model.

elements such as cores and air gaps, can be represented using equivalent magnetic circuits. These magnetic circuits can then be solved using conventional circuit analysis, to determine the various fluxes, MMFs, and terminal voltages and currents. Kirchoff's laws apply to magnetic circuits, and follow directly from Maxwell's equations. The analog of Kirchoff's current law holds because the divergence of $\boldsymbol{B}$ is zero, and hence magnetic flux lines are continuous and cannot end. Therefore, any flux line that enters a node must leave the node. As illustrated in Fig. 13.10, the total flux entering a node must be zero. The analog of Kirchoff's voltage law follows from Ampere's law, Eq. (13.7). The left-hand-side integral in Eq. (13.7) is the sum of the MMFs across the reluctances around the closed path. The right-hand-side of Eq. (13.7) states that currents in windings are sources of MMF. An n-turn winding carrying current $i(t)$ can be modeled as an MMF source, analogous to a voltage source, of value $ni(t)$. When these MMF sources are included, the total MMF around a closed path is zero.

Consider the inductor with air gap of Fig. 13.11(a). A closed path following the magnetic field lines is illustrated. This path passes through the core, of permeability μ and length ℓ_c, and across the air gap, of permeability μ_0 and length ℓ_g. The cross-sectional areas of the core and air gap are approximately equal. Application of Ampere's law for this path leads to

$$\mathscr{F}_c + \mathscr{F}_g = ni \tag{13.26}$$

where $\mathscr{F}_c$ and $\mathscr{F}_g$ are the MMFs across the core and air gap, respectively. The core and air gap characteristics can be modeled by reluctances as in Fig. 13.9 and Eq. (13.25); the core reluctance $\mathscr{R}_c$ and air gap reluctance $\mathscr{R}_g$ are given by

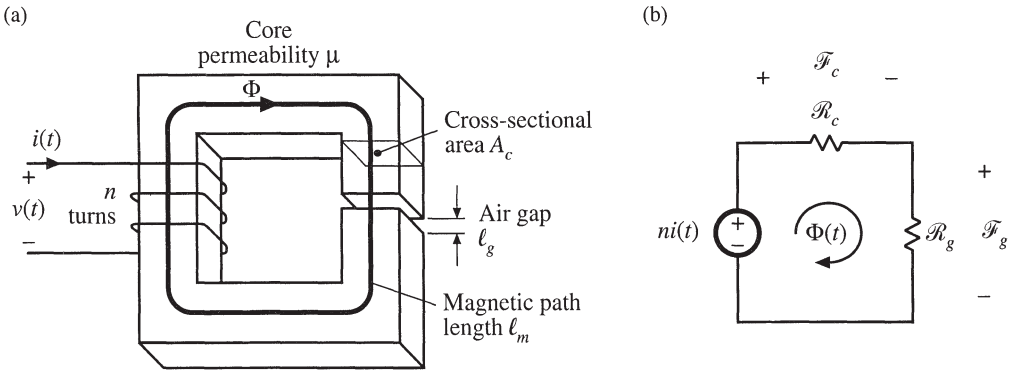


Fig. 13.11 Inductor with air gap example: (a) physical geometry, (b) magnetic circuit model.

$$\mathcal{R}_c = \frac{\ell_c}{\mu A_c}$$
$$\mathcal{R}_g = \frac{\ell_g}{\mu_0 A_c} \tag{13.27}$$

A magnetic circuit corresponding to Eqs. (13.26) and (13.27) is given in Fig. 13.11(b). The winding is a source of MMF, of value ni. The core and air gap reluctances are effectively in series. The solution of the magnetic circuit is

$$ni = \Phi\left(\mathcal{R}_c + \mathcal{R}_g\right) \tag{13.28}$$

The flux $\Phi(t)$ passes through the winding, and so we can use Faraday's law to write

$$v(t) = n\frac{d\Phi(t)}{dt} \tag{13.29}$$

Use of Eq. (13.28) to eliminate $\Phi(t)$ yields

$$v(t) = \frac{n^2}{\mathcal{R}_c + \mathcal{R}_g}\frac{di(t)}{dt} \tag{13.30}$$

Therefore, the inductance L is

$$L = \frac{n^2}{\mathcal{R}_c + \mathcal{R}_g} \tag{13.31}$$

The air gap increases the total reluctance of the magnetic circuit, and decreases the inductance.

Air gaps are employed in practical inductors for two reasons. With no air gap ($\mathcal{R}_g = 0$), the inductance is directly proportional to the core permeability μ. This quantity is dependent on temperature and operating point, and is difficult to control. Hence, it may be difficult to construct an inductor having a well-controlled value of L. Addition of an air gap having a reluctance $\mathcal{R}_g$ greater than $\mathcal{R}_c$ causes the value of L in Eq. (13.31) to be insensitive to variations in μ.

Addition of an air gap also allows the inductor to operate at higher values of winding current $i(t)$ without saturation. The total flux Φ is plotted vs. the winding MMF ni in Fig. 13.12. Since Φ is proportional to B, and when the core is not saturated ni is proportional to the magnetic field strength H in the

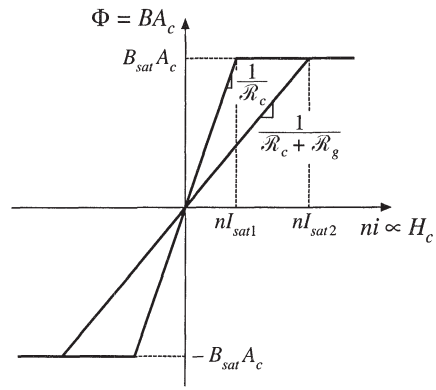


Fig. 13.12 Effect of air gap on the magnetic circuit Φ vs. ni characteristics. The air gap increases the current I_{sat} at the onset of core saturation.

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core, Fig. 13.12 has the same shape as the core *B–H* characteristic. When the core is not saturated, Φ is related to *ni* according to the linear relationship of Eq. (13.28). When the core saturates, Φ is equal to

$$\Phi_{sat} = B_{sat} A_c \tag{13.32}$$

The winding current I_{sat} at the onset of saturation is found by substitution of Eq. (13.32) into (13.28):

$$I_{sat} = \frac{B_{sat} A_c}{n} \left(\mathcal{R}_c + \mathcal{R}_g \right) \tag{13.33}$$

The Φ–*ni* characteristics are plotted in Fig. 13.12 for two cases: (a) air gap present, and (b) no air gap ($\mathcal{R}_g = 0$). It can be seen that I_{sat} is increased by addition of an air gap. Thus, the air gap allows increase of the saturation current, at the expense of decreased inductance.

13.2 TRANSFORMER MODELING

Consider next the two-winding transformer of Fig. 13.13. The core has cross-sectional area A_c, mean magnetic path length ℓ_m, and permeability μ. An equivalent magnetic circuit is given in Fig. 13.14. The core reluctance is

$$\mathcal{R} = \frac{\ell_m}{\mu A_c} \tag{13.34}$$

Since there are two windings in this example, it is necessary to determine the relative polarities of the MMF generators. Ampere's law states that

$$\mathcal{F}_c = n_1 i_1 + n_2 i_2 \tag{13.35}$$

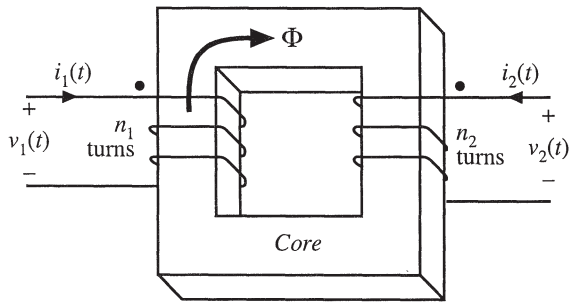


Fig. 13.13 A two-winding transformer.

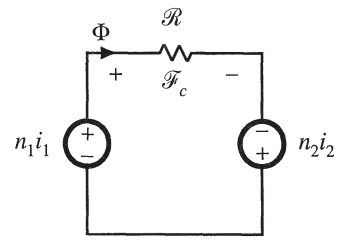


Fig. 13.14 Magnetic circuit that models the two-winding transformer of Fig. 13.13.

The MMF generators are additive, because the currents i_1 and i_2 pass in the same direction through the core window. Solution of Fig. 13.14 yields

$$\Phi\mathcal{R} = n_1 i_1 + n_2 i_2 \tag{13.36}$$

This expression could also be obtained by substitution of $\mathcal{F}_c = \Phi\mathcal{R}$ into Eq. (13.35).

13.2.1 The Ideal Transformer

In the ideal transformer, the core reluctance $\mathcal{R}$ approaches zero. The causes the core MMF $\mathcal{F}_c = \Phi\mathcal{R}$ to also approach zero. Equation (13.35) then becomes

$$0 = n_1 i_1 + n_2 i_2 \tag{13.37}$$

Also, by Faraday's law, we have

$$\begin{aligned} v_1 &= n_1 \frac{d\Phi}{dt} \\ v_2 &= n_2 \frac{d\Phi}{dt} \end{aligned} \tag{13.38}$$

Note that Φ is the same in both equations above: the same total flux links both windings. Elimination of Φ leads to

$$\frac{d\Phi}{dt} = \frac{v_1}{n_1} = \frac{v_2}{n_2} \tag{13.39}$$

Equations (13.37) and (13.39) are the equations of the ideal transformer:

$$\frac{v_1}{n_1} = \frac{v_2}{n_2} \quad \text{and} \quad n_1 i_1 + n_2 i_2 = 0 \tag{13.40}$$

The ideal transformer symbol of Fig. 13.15 is defined by Eq. (13.40).

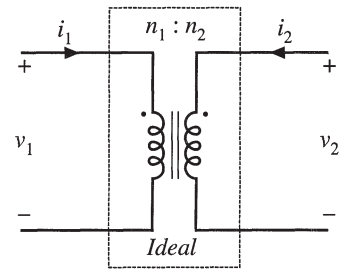


Fig. 13.15 Ideal transformer symbol.

13.2.2 The Magnetizing Inductance

For the actual case in which the core reluctance $\mathcal{R}$ is nonzero, we have

$$\Phi\mathcal{R} = n_1 i_1 + n_2 i_2 \quad \text{with} \quad v_1 = n_1 \frac{d\Phi}{dt} \tag{13.41}$$

Elimination of Φ yields

$$v_1 = \frac{n_1^2}{\mathcal{R}} \frac{d}{dt}\left[i_1 + \frac{n_2}{n_1} i_2 \right] \tag{13.42}$$

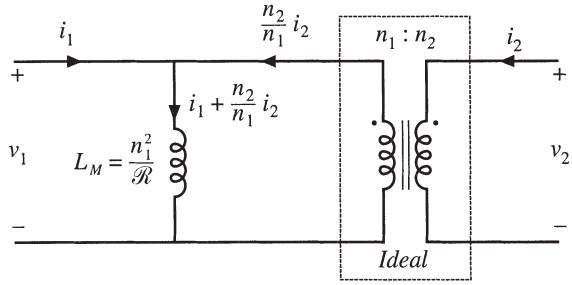


Fig. 13.16 Transformer model including magnetizing inductance.

This equation is of the form

$$v_1 = L_M \frac{di_M}{dt} \tag{13.43}$$

where

$$\begin{aligned} L_M &= \frac{n_1^2}{\mathcal{R}} \\ i_M &= i_1 + \frac{n_2}{n_1} i_2 \end{aligned} \tag{13.44}$$

are the *magnetizing inductance* and *magnetizing current*, referred to the primary winding. An equivalent circuit is illustrated in Fig. 13.16.

Figure 13.16 coincides with the transformer model introduced in Chapter 6. The magnetizing inductance models the magnetization of the core material. It is a real, physical inductor, which exhibits saturation and hysteresis. All physical transformers must contain a magnetizing inductance. For example, suppose that we disconnect the secondary winding. We are then left with a single winding on a magnetic core—an inductor. Indeed, the equivalent circuit of Fig. 13.16 predicts this behavior, via the magnetizing inductance. The magnetizing current causes the ratio of the winding currents to differ from the turns ratio.

The transformer saturates when the core flux density $B(t)$ exceeds the saturation flux density B_{sat}. When the transformer saturates, the magnetizing current $i_M(t)$ becomes large, the impedance of the magnetizing inductance becomes small, and the transformer windings become short circuits. It should be noted that large winding currents $i_1(t)$ and $i_2(t)$ do not necessarily cause saturation: if these currents obey Eq. (13.37), then the magnetizing current is zero and there is no net magnetization of the core. Rather, saturation of a transformer is a function of the applied volt-seconds. The magnetizing current is given by

$$i_M(t) = \frac{1}{L_M} \int v_1(t) dt \tag{13.45}$$

Alternatively, Eq. (13.45) can be expressed in terms of the core flux density $B(t)$ as

$$B(t) = \frac{1}{n_1 A_c} \int v_1(t) dt \tag{13.46}$$

The flux density and magnetizing current will become large enough to saturate the core when the applied volt-seconds λ_1 is too large, where λ_1 is defined for a periodic ac voltage waveform as

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$$\lambda_1 = \int_{t_1}^{t_2} v_1(t)dt \tag{13.47}$$

The limits are chosen such that the integral is taken over the positive portion of the applied periodic voltage waveform.

To fix a saturating transformer, the flux density should be decreased by increasing the number of turns, or by increasing the core cross-sectional area A_c. Adding an air gap has no effect on saturation of conventional transformers, since it does not modify Eq. (13.46). An air gap simply makes the transformer less ideal, by decreasing L_M and increasing $i_M(t)$ without changing $B(t)$. Saturation mechanisms in transformers differ from those of inductors, because transformer saturation is determined by the applied winding voltage waveforms, rather than the applied winding currents.

13.2.3 Leakage Inductances

In practice, there is some flux which links one winding but not the other, by "leaking" into the air or by some other mechanism. As illustrated in Fig. 13.17, this flux leads to *leakage inductance*, i.e., additional effective inductances that are in series with the windings. A topologically equivalent structure is illustrated in Fig. 13.17(b), in which the leakage fluxes $\Phi_{\ell 1}$ and $\Phi_{\ell 2}$ are shown explicitly as separate inductors.

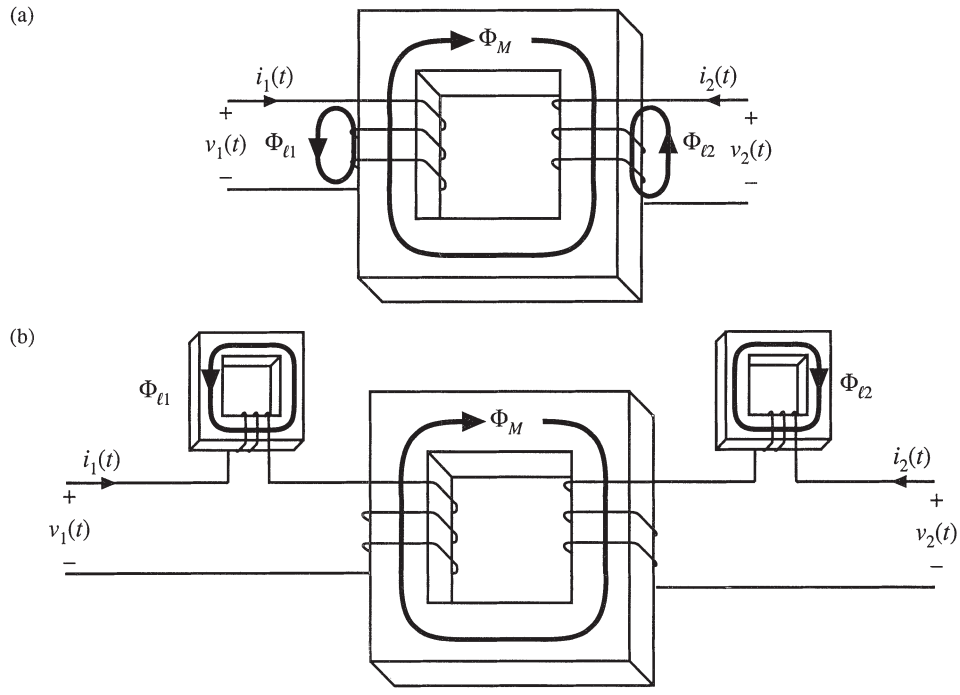


Fig. 13.17 Leakage flux in a two-winding transformer: (a) transformer geometry, (b) an equivalent system.

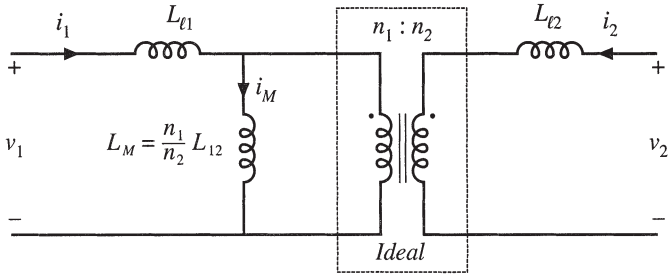


Fig. 13.18 Two-winding transformer equivalent circuit, including magnetizing inductance referred to primary, and primary and secondary leakage inductances.

Figure 13.18 illustrates a transformer electrical equivalent circuit model, including series inductors $L_{\ell 1}$ and $L_{\ell 2}$ which model the leakage inductances. These leakage inductances cause the terminal voltage ratio $v_2(t)/v_1(t)$ to differ from the ideal turns ratio n_2/n_1. In general, the terminal equations of a two-winding transformer can be written

$$\begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{22} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1(t) \\ i_2(t) \end{bmatrix} \tag{13.48}$$

The quantity L_{12} is called the *mutual inductance*, and is given by

$$L_{12} = \frac{n_1 n_2}{\mathcal{R}} = \frac{n_2}{n_1} L_M \tag{13.49}$$

The quantities L_{11} and L_{22} are called the primary and secondary *self-inductances*, given by

$$\begin{aligned} L_{11} &= L_{\ell 1} + \frac{n_1}{n_2} L_{12} \\ L_{22} &= L_{\ell 2} + \frac{n_2}{n_1} L_{12} \end{aligned} \tag{13.50}$$

Note that Eq. (13.48) does not explicitly identify the physical turns ratio n_2/n_1. Rather, Eq. (13.48) expresses the transformer behavior as a function of electrical quantities alone. Equation (13.48) can be used, however, to define the *effective turns ratio*

$$n_e = \sqrt{\frac{L_{22}}{L_{11}}} \tag{13.51}$$

and the *coupling coefficient*

$$k = \frac{L_{12}}{\sqrt{L_{11} L_{22}}} \tag{13.52}$$

The coupling coefficient k lies in the range $0 \le k \le 1$, and is a measure of the degree of magnetic coupling between the primary and secondary windings. In a transformer with perfect coupling, the leakage inductances $L_{\ell 1}$ and $L_{\ell 2}$ are zero. The coupling coefficient k is then equal to 1. Construction of low-voltage transformers having coupling coefficients in excess of 0.99 is quite feasible. When the coupling coefficient is close to 1, then the effective turns ratio n_e is approximately equal to the physical turns ratio n_2/n_1.

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13.3 LOSS MECHANISMS IN MAGNETIC DEVICES

13.3.1 Core Loss

Energy is required to effect a change in the magnetization of a core material. Not all of this energy is recoverable in electrical form; a fraction is lost as heat. This power loss can be observed electrically as hysteresis of the *B–H* loop.

Consider an *n*–turn inductor excited by periodic waveforms $v(t)$ and $i(t)$ having frequency f. The net energy that flows into the inductor over one cycle is

$$W = \int_{\text{one cycle}} v(t)i(t)\,dt \tag{13.53}$$

We can relate this expression to the core *B–H* characteristic: substitute $B(t)$ for $v(t)$ using Faraday's law, Eq. (13.13), and substitute $H(t)$ for $i(t)$ using Ampere's law, i.e. Eq. (13.14):

$$\begin{aligned} W &= \int_{\text{one cycle}} \left(nA_c \frac{dB(t)}{dt}\right)\left(\frac{H(t)\ell_m}{n}\right)dt \\ &= \left(A_c\ell_m\right)\int_{\text{one cycle}} H\,dB \end{aligned} \tag{13.54}$$

The term $A_c\ell_m$ is the volume of the core, while the integral is the area of the *B–H* loop:

$$\text{(energy lost per cycle)} = \text{(core volume)(area of } B\text{–}H \text{ loop)} \tag{13.55}$$

The *hysteresis power loss* P_H is equal to the energy lost per cycle, multiplied by the excitation frequency f:

$$P_H = \left(f\right)\left(A_c\ell_m\right)\int_{\text{one cycle}} H\,dB \tag{13.56}$$

To the extent that the size of the hysteresis loop is independent of frequency, hysteresis loss increases directly with operating frequency.

Magnetic core materials are iron alloys that, unfortunately, are also good electrical conductors. As a result, ac magnetic fields can cause electrical *eddy currents* to flow within the core material itself. An example is illustrated in Fig. 13.19. The ac flux $\Phi(t)$ passes through the core. This induces eddy currents $i(t)$ which, according to Lenz's law, flow in paths that oppose the time-varying flux $\Phi(t)$. These eddy currents cause i^2R losses in the resistance of the core material. The eddy current losses are especially significant in high-frequency applications.

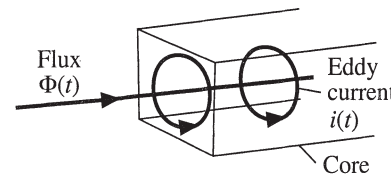


Fig. 13.19 Eddy currents in an iron core.

According to Faraday's law, the ac flux $\Phi(t)$ induces voltage in the core, which drives the current around the paths illustrated in Fig. 13.19. Since the induced voltage is proportional to the derivative of the flux, the voltage magnitude increases directly with the excitation frequency f. If the impedance of

the core material is purely resistive and independent of frequency, then the magnitude of the induced eddy currents also increases directly with f. This implies that the i^2R eddy current losses should increase as f^2. In power ferrite materials, the core material impedance magnitude actually decreases with increasing f. Over the useful frequency range, the eddy current losses typically increase faster than f^2.

There is a basic tradeoff between saturation flux density and core loss. Use of a high operating flux density leads to reduced size, weight, and cost. Silicon steel and similar materials exhibit saturation flux densities of 1.5 to 2 T. Unfortunately, these core materials exhibit high core loss. In particular, the low resistivity of these materials leads to high eddy current loss. Hence, these materials are suitable for filter inductor and low-frequency transformer applications. The core material is produced in laminations or thin ribbons, to reduce the eddy current magnitude. Other ferrous alloys may contain molybdenum, cobalt, or other elements, and exhibit somewhat lower core loss as well as somewhat lower saturation flux densities.

Iron alloys are also employed in powdered cores, containing ferromagnetic particles of sufficiently small diameter such that eddy currents are small. These particles are bound together using an insulating medium. Powdered iron and molybdenum permalloy powder cores exhibit typical saturation flux densities of 0.6 to 0.8 T, with core losses significantly lower than laminated ferrous alloy materials. The insulating medium behaves effectively as a distributed air gap, and hence these cores have relatively low permeability. Powder cores find application as transformers at frequencies of several kHz, and as filter inductors in high frequency (100 kHz) switching converters.

Amorphous alloys exhibit low hysteresis loss. Core conductivity and eddy current losses are somewhat lower than ferrous alloys, but higher than ferrites. Saturation flux densities in the range 0.6 to 1.5 T are obtained.

Ferrite cores are ceramic materials having low saturation flux density, 0.25 to 0.5 T. Their resistivities are much higher than other materials, and hence eddy current losses are much smaller. Manganese-zinc ferrite cores find widespread use as inductors and transformers in converters having switching frequencies of 10 kHz to 1 MHz. Nickel-zinc ferrite materials can be employed at yet higher frequencies.

Figure 13.20 contains typical total core loss data, for a certain ferrite material. Power loss density, in Watts per cubic centimeter of core material, is plotted as a function of sinusoidal excitation frequency f and peak ac flux density ΔB. At a given frequency, the core loss P_{fe} can be approximated by an empirical function of the form

$$P_{fe} = K_{fe}(\Delta B)^{\beta} A_c \ell_m \qquad (13.57)$$

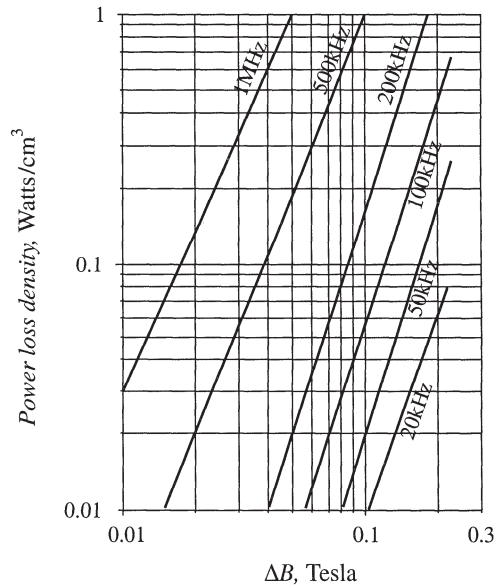


Fig. 13.20 Typical core loss data for a high-frequency power ferrite material. Power loss density is plotted vs. peak ac flux density ΔB, for sinusoidal excitation.

The parameters K_{fe} and β are determined by fitting Eq. (13.57) to the manufacturer's published data. Typical values of β for ferrite materials operating in their intended range of ΔB and f lie in the range 2.6 to 2.8. The constant of proportionality K_{fe} increases rapidly with excitation frequency f. The dependence of K_{fe} on f can also be approximated by empirical formulae that are fitted to the manu-

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facturer's published data; a fourth-order polynomial or a function of the form $K_{fe0} f^{\xi}$ are sometimes employed for this purpose.

13.3.2 Low-Frequency Copper Loss

Significant loss also occurs in the resistance of the copper windings. This is also a major determinant of the size of a magnetic device: if copper loss and winding resistance were irrelevant, then inductor and transformer elements could be made arbitrarily small by use of many small turns of small wire.

Figure 13.21 contains an equivalent circuit of a winding, in which element R models the winding resistance. The copper loss of the winding is

$$P_{cu} = I_{rms}^2 R \tag{13.58}$$

where I_{rms} is the rms value of $i(t)$. The dc resistance of the winding conductor can be expressed as

$$R = \rho \frac{\ell_b}{A_w} \tag{13.59}$$

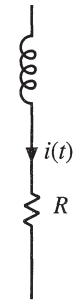


Fig. 13.21 Winding equivalent circuit that models copper loss.

where A_w is the wire bare cross-sectional area, and ℓ_b is the length of the wire. The resistivity ρ is equal to $1.724 \cdot 10^{-6}$ Ω–cm for soft-annealed copper at room temperature. This resistivity increases to $2.3 \cdot 10^{-6}$ Ω–cm at 100°C.

13.4 EDDY CURRENTS IN WINDING CONDUCTORS

Eddy currents also cause power losses in winding conductors. This can lead to copper losses significantly in excess of the value predicted by Eqs. (13.58) and (13.59). The specific conductor eddy current mechanisms are called the *skin effect* and the *proximity effect*. These mechanisms are most pronounced in high-current conductors of multi-layer windings, particularly in high-frequency converters.

13.4.1 Introduction to the Skin and Proximity Effects

Figure 13.22(a) illustrates a current $i(t)$ flowing through a solitary conductor. This current induces magnetic flux $\Phi(t)$, whose flux lines follow circular paths around the current as shown. According to Lenz's law, the ac flux in the conductor induces eddy currents, which flow in a manner that tends to oppose the ac flux $\Phi(t)$. Figure 13.22(b) illustrates the paths of the eddy currents. It can be seen that the eddy currents tend to reduce the net current density in the center of the conductor, and increase the net current density near the surface of the conductor.

The current distribution within the conductor can be found by solution of Maxwell's equations. For a sinusoidal current $i(t)$ of frequency f, the result is that the current density is greatest at the surface of the conductor. The current density is an exponentially decaying function of distance into the conductor, with characteristic length δ known as the *penetration depth* or *skin depth*. The penetration depth is given by

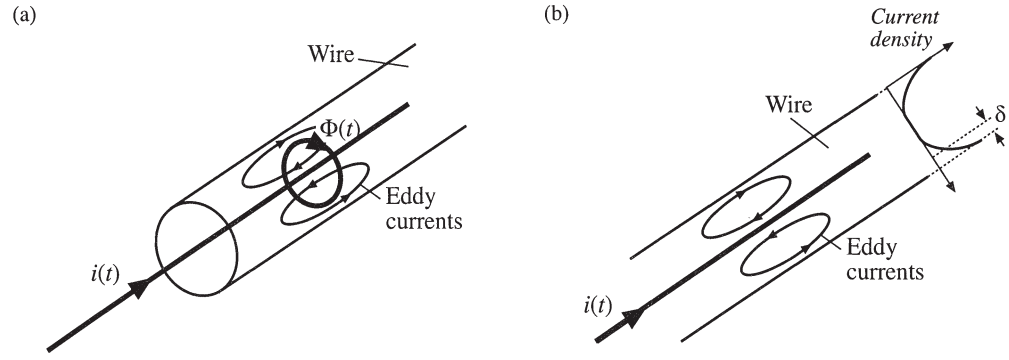


Fig. 13.22 The skin effect: (a) current $i(t)$ induces flux $\Phi(t)$, which in turn induces eddy currents in conductor; (b) the eddy currents tend to oppose the current $i(t)$ in the center of the wire, and increase the current on the surface of the wire.

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{13.60}$$

For a copper conductor, the permeability μ is equal to μ_0, and the resistivity ρ is given in Section 13.3.2. At 100°C, the penetration depth of a copper conductor is

$$\delta = \frac{7.5}{\sqrt{f}} \text{ cm} \tag{13.61}$$

with f expressed in Hz. The penetration depth of copper conductors is plotted in Fig. 13.23, as a function of frequency f. For comparison, the wire diameters d of standard American Wire Gauge (AWG) conductors are also listed. It can be seen that $d/\delta = 1$ for AWG #40 at approximately 500 kHz, while $d/\delta = 1$ for

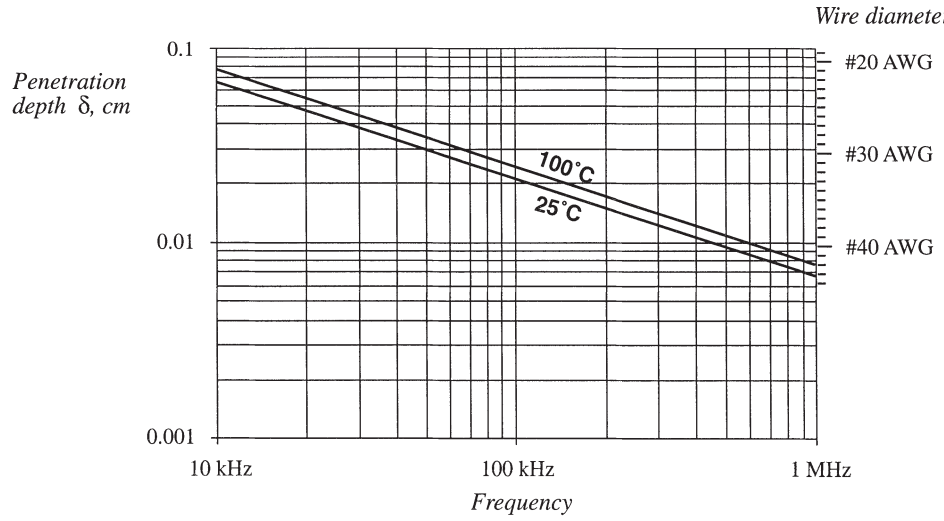


Fig. 13.23 Penetration depth δ, as a function of frequency f, for copper wire.

AWG #22 at approximately 10 kHz.

The skin effect causes the resistance and copper loss of solitary large-diameter wires to increase at high frequency. High-frequency currents do not penetrate to the center of the conductor. The current crowds at the surface of the wire, the inside of the wire is not utilized, and the effective wire cross-sectional area is reduced. However, the skin effect alone is not sufficient to explain the increased high-frequency copper losses observed in multiple-layer transformer windings.

A conductor that carries a high-frequency current $i(t)$ induces copper loss in a adjacent conductor by a phenomenon known as the *proximity effect*. Figure 13.24 illustrates two copper foil conductors that are placed in close proximity to each other. Conductor 1 carries a high-frequency sinusoidal current $i(t)$, whose penetration depth δ is much smaller than the thickness h of conductors 1 or 2. Conductor 2 is open-circuited, so that it carries a net current of zero. However, it is possible for eddy currents to be induced in conductor 2 by the current $i(t)$ flowing in conductor 1.

The current $i(t)$ flowing in conductor 1 generates a flux $\Phi(t)$ in the space between conductors 1 and 2; this flux attempts to penetrate conductor 2. By Lenz's law, a current is induced on the adjacent (left) side of conductor 2, which tends to oppose the flux $\Phi(t)$. If the conductors are closely spaced, and if $h \gg \delta$, then the induced current will be equal and opposite to the current $i(t)$, as illustrated in Fig. 13.24.

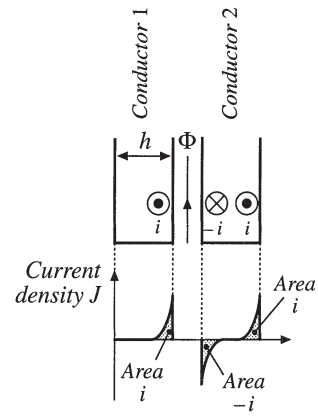


Fig. 13.24 The proximity effect in adjacent copper foil conductors. Conductor 1 carries current $i(t)$. Conductor 2 is open-circuited.

Since conductor 2 is open-circuited, the net current in conductor 2 must be zero. Therefore, a current + $i(t)$ flows on the right-side surface of conductor 2. So the current flowing in conductor 1 induces a current that circulates on the surfaces of conductor 2.

Figure 13.25 illustrates the proximity effect in a simple transformer winding. The primary winding consists of three series-connected turns of copper foil, having thickness $h \gg \delta$, and carrying net current $i(t)$. The secondary winding is identical; to the extent that the magnetizing current is small, the secondary turns carry net current $-i(t)$. The windings are surrounded by a magnetic core material that encloses the mutual flux of the transformer.

The high-frequency sinusoidal current $i(t)$ flows on the right surface of primary layer 1, adjacent to layer 2. This induces a copper loss in layer 1, which can be calculated as follows. Let R_{dc} be the dc resistance of layer 1, given by Eq. (13.59), and let I be the rms value of $i(t)$. The skin effect causes the copper loss in layer 1 to be equal to the loss in a conductor of thickness δ with uniform current density. This reduction of the conductor thickness from h to δ effectively increases the resistance by the same factor. Hence, layer 1 can be viewed as having an "ac resistance" given by

$$R_{ac} = \frac{h}{\delta} R_{dc} \tag{13.62}$$

The copper loss in layer 1 is

$$P_1 = I^2 R_{ac} \tag{13.63}$$

The proximity effect causes a current to be induced in the adjacent (left-side) surface of primary layer 2, which tends to oppose the flux generated by the current of layer 1. If the conductors are closely spaced, and if $h \gg \delta$, then the induced current will be equal and opposite to the current $i(t)$, as illustrated

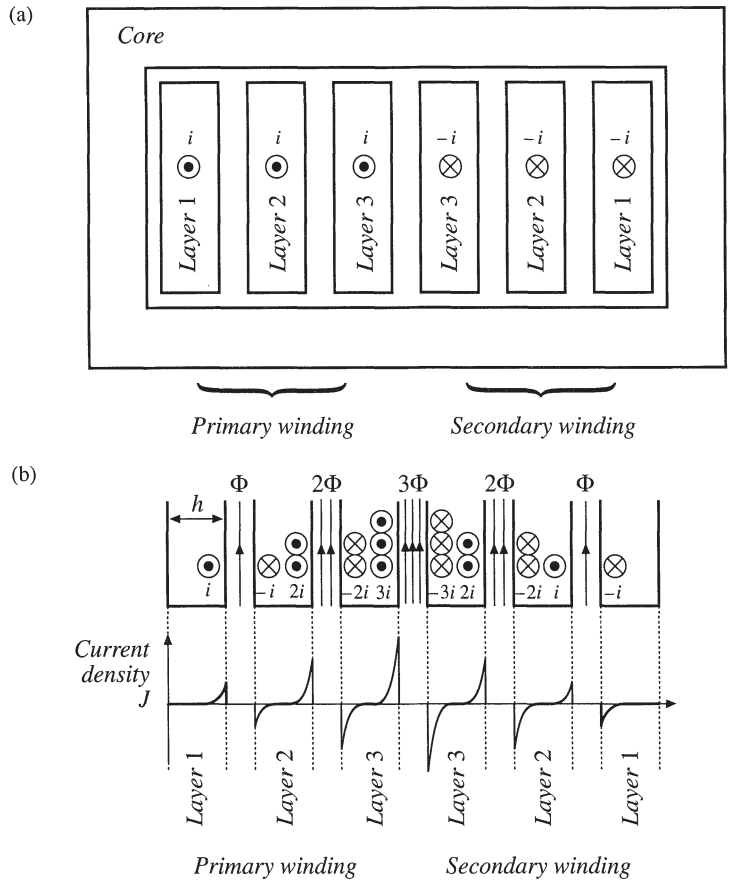


Fig. 13.25 A simple transformer example illustrating the proximity effect: (a) core and winding geometry, (b) distribution of currents on surfaces of conductors.

in Fig. 13.25. Hence, current $-i(t)$ flows on the left surface of the second layer. Since layers 1 and 2 are connected in series, they must both conduct the same net current $i(t)$. As a result, a current $+2i(t)$ must flow on the right-side surface of layer 2.

The current flowing on the left surface of layer 2 has the same magnitude as the current of layer 1, and hence the copper loss is the same: P_1. The current flowing on the right surface of layer 2 has rms magnitude $2I$; hence, it induces copper loss $(2I)^2R_{ac} = 4P_1$. The total copper loss in primary layer 2 is therefore

$$P_2 = P_1 + 4P_1 = 5P_1 \tag{13.64}$$

The copper loss in the second layer is five times as large as the copper loss in the first layer!

The current $2i(t)$ flowing on the right surface of layer 2 induces a flux $2\Phi(t)$ as illustrated in Fig. 13.25. This causes an opposing current $-2i(t)$ to flow on the adjacent (left) surface of primary layer 3. Since layer 3 must also conduct net current $i(t)$, a current $+3i(t)$ flows on the right surface of layer 3. The total copper loss in layer 3 is

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$$P_3 = \left(2^2 + 3^2\right)P_1 = 13P_1 \tag{13.65}$$

Likewise, the copper loss in layer m of a multiple-layer winding can be written

$$P_m = I^2\left[(m-1)^2 + m^2\right]\left(\frac{h}{\delta} R_{dc}\right) \tag{13.66}$$

It can be seen that the copper loss compounds very quickly in a multiple-layer winding.

The total copper loss in the three-layer primary winding is $P_1 + 5P_1 + 13P_1$, or $19P_1$. More generally, if the winding contains a total of M layers, then the total copper loss is

$$\begin{aligned} P &= I^2\left(\frac{h}{\delta} R_{dc}\right)\sum_{m=1}^{M}\left[(m-1)^2 + m^2\right] \\ &= I^2\left(\frac{h}{\delta} R_{dc}\right)\frac{M}{3}\left(2M^2 + 1\right) \end{aligned} \tag{13.67}$$

If a dc or low-frequency ac current of rms amplitude I were applied to the M-layer winding, its copper loss would be $P_{dc} = I^2 M R_{dc}$. Hence, the proximity effect increases the copper loss by the factor

$$F_R = \frac{P}{P_{dc}} = \frac{1}{3}\left(\frac{h}{\delta}\right)\left(2M^2 + 1\right) \tag{13.68}$$

This expression is valid for a foil winding having $h \gg \delta$.

As illustrated in Fig. 13.25, the currents in the secondary winding are symmetrical, and hence the secondary winding has the same conduction loss.

The example above, and the associated equations, are limited to $h \gg \delta$ and to the winding geometry shown. The equations do not quantify the behavior for $h \sim \delta$, nor for round conductors, nor are the equations sufficiently general to cover the more complicated winding geometries often encountered in the magnetic devices of switching converters. Optimum designs may, in fact, occur with conductor thicknesses in the vicinity of one penetration depth. The discussions of the following sections allow computation of proximity losses in more general circumstances.

13.4.2 Leakage Flux in Windings

As described above, an externally-applied magnetic field will induce eddy currents to flow in a conductor, and thereby induce copper loss. To understand how magnetic fields are oriented in windings, let us consider the simple two-winding transformer illustrated in Fig. 13.26. In this example, the core has large permeability $\mu \gg \mu_0$. The primary winding consists of eight turns of wire arranged in two layers, and each turn carries current $i(t)$ in the direction indicated. The secondary winding is identical to the primary winding, except that the current polarity is reversed.

Flux lines for typical operation of this transformer are sketched in Fig. 13.26(b). As described in Section 13.2, a relatively large mutual flux is present, which magnetizes the core. In addition, leakage flux is present, which does not completely link both windings. Because of the symmetry of the winding geometry in Fig. 13.26, the leakage flux runs approximately vertically through the windings.

To determine the magnitude of the leakage flux, we can apply Ampere's Law. Consider the closed path taken by one of the leakage flux lines, as illustrated in Fig. 13.27. Since the core has large permeability, we can assume that the MMF induced in the core by this flux is negligible, and that the

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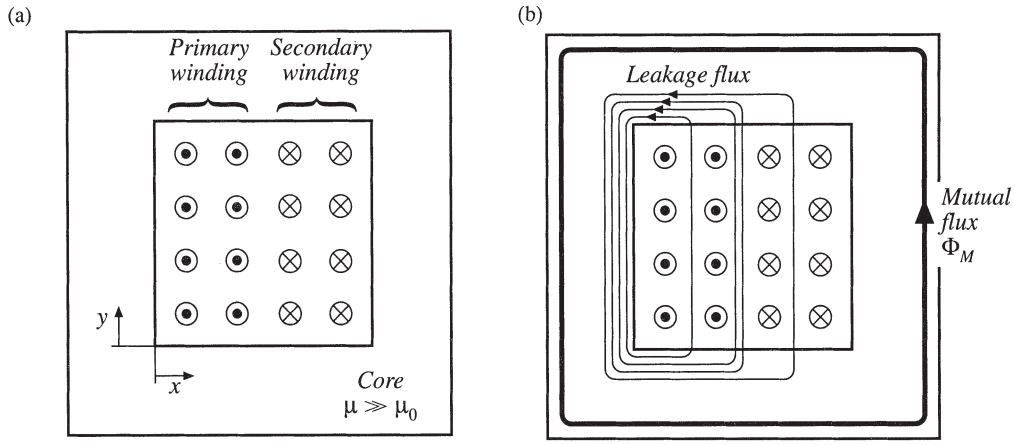


Fig. 13.26 Two-winding transformer example: (a) core and winding geometry, (b) typical flux distribution.

total MMF around the path is dominated by the MMF $\mathcal{F}(x)$ across the core window. Hence, Ampere's Law states that the net current enclosed by the path is equal to the MMF across the air gap:

$$\textit{Enclosed current} = \mathcal{F}(x) = H(x)\ell_w \tag{13.69}$$

where ℓ_w is the height of the window as shown in Fig. 13.27. The net current enclosed by the path depends on the number of primary and secondary conductors enclosed by the path, and is therefore a function of the horizontal position x. The first layer of the primary winding consists of 4 turns, each carrying current $i(t)$. So when the path encloses only the first layer of the primary winding, then the enclosed current is $4i(t)$ as shown in Fig. 13.28. Likewise, when the path encloses both layers of the primary winding, then the enclosed current is $8i(t)$. When the path encloses the entire primary, plus layer 2 of the secondary winding, then the net enclosed current is $8i(t) - 4i(t) = 4i(t)$. The MMF $\mathcal{F}(x)$ across the core window is zero outside the winding, and rises to a maximum of $8i(t)$ at the interface between the primary and secondary windings. Since $H(x) = \mathcal{F}(x)/\ell_w$, the magnetic field intensity $H(x)$ is proportional to the sketch of Fig. 13.28.

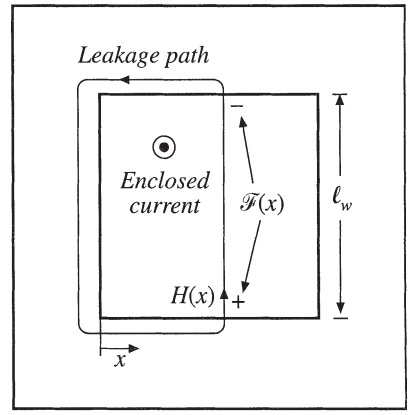


Fig. 13.27 Analysis of leakage flux using Ampere's Law, for the transformer of Fig. 13.26.

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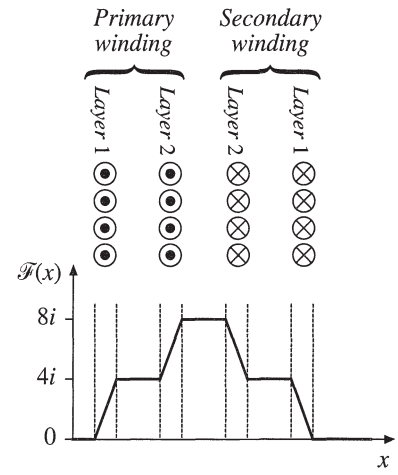


Fig. 13.28 MMF diagram for the transformer winding example of Figs. 13.26 and 13.27.

It should be noted that the shape of the $\mathcal{F}(x)$ curve in the vicinity of the winding conductors depends on the distribution of the current within the conductors. Since this distribution is not yet known, the $\mathcal{F}(x)$ curve of Fig. 13.28 is arbitrarily drawn as straight line segments.

In general, the magnetic fields that surround conductors and lead to eddy currents must be determined using finite element analysis or other similar methods. However, in a large class of coaxial solenoidal winding geometries, the magnetic field lines are nearly parallel to the winding layers. As shown below, we can then obtain an analytical solution for the proximity losses.

13.4.3 Foil Windings and Layers

The winding symmetry described in the previous section allows simplification of the analysis. For the purposes of determining leakage inductance and winding eddy currents, a layer consisting of n_ℓ turns of round wire carrying current $i(t)$ can be approximately modeled as an effective single turn of foil, which carries current $n_\ell i(t)$. The steps in the transformation of a layer of round conductors into a foil conductor are formalized in Fig. 13.29 [6, 8–11]. The round conductors are replaced by square conductors having the same copper cross-sectional area, Fig. 13.29(b). The thickness h of the square conductors is therefore

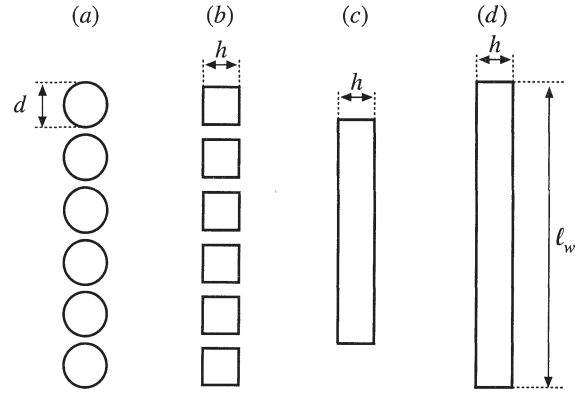


Fig. 13.29 Approximating a layer of round conductors as an effective foil conductor.

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equal to the bare copper wire diameter, multiplied by the factor $\sqrt{\pi/4}$:

$$h = \sqrt{\frac{\pi}{4}}\, d \tag{13.70}$$

These square conductors are then joined together, into a foil layer [Fig. 13.29(c)]. Finally, the width of the foil is increased, such that it spans the width of the core window [Fig. 13.29(d)]. Since this stretching process increases the conductor cross-sectional area, a compensating factor η must be introduced such that the correct dc conductor resistance is predicted. This factor, sometimes called the *conductor spacing factor* or the winding *porosity*, is defined as the ratio of the actual layer copper area [Fig. 13.29(a)] to the area of the effective foil conductor of Fig. 13.29(d). The porosity effectively increases the resistivity ρ of the conductor, and thereby increases its skin depth:

$$\delta' = \frac{\delta}{\sqrt{\eta}} \tag{13.71}$$

If a layer of width ℓ_w contains n_ℓ turns of round wire having diameter d, then the winding porosity η is given by

$$\eta = \sqrt{\frac{\pi}{4}}\, d\, \frac{n_\ell}{\ell_w} \tag{13.72}$$

A typical value of η for round conductors that span the width of the winding bobbin is 0.8. In the following analysis, the factor φ is given by h/δ for foil conductors, and by the ratio of the effective foil conductor thickness h to the effective skin depth δ' for round conductors as follows:

$$\varphi = \frac{h}{\delta'} = \sqrt{\eta}\, \sqrt{\frac{\pi}{4}}\, \frac{d}{\delta} \tag{13.73}$$

13.4.4 Power Loss in a Layer

In this section, the average power loss P in a uniform layer of thickness h is determined. As illustrated in Fig. 13.30, the magnetic field strengths on the left and right sides of the conductor are denoted $H(0)$ and $H(d)$, respectively. It is assumed that the component of magnetic field normal to the conductor surface is zero. These magnetic fields are driven by the magnetomotive forces $\mathscr{F}(0)$ and $\mathscr{F}(h)$, respectively. Sinusoidal waveforms are assumed, and rms magnitudes are employed. It is further assumed here that $H(0)$ and $H(h)$ are in phase; the effect of a phase shift is treated in [10].

With these assumptions, Maxwell's equations are solved to find the current density distribution in the layer. The power loss density is then computed, and is integrated over the volume of the layer to find the total copper loss in the layer [10]. The result is

$$P = R_{dc}\, \frac{\varphi}{n_\ell^2} \left[\Big(\mathscr{F}^2(h) + \mathscr{F}^2(0) \Big) G_1(\varphi) - 4\, \mathscr{F}(h) \mathscr{F}(0) G_2(\varphi) \right] \tag{13.74}$$

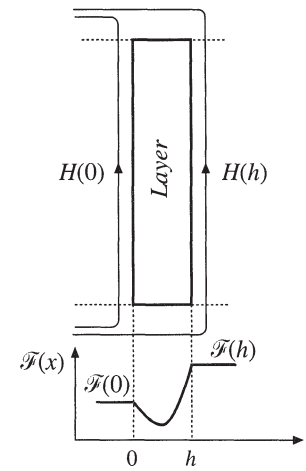


Fig. 13.30 The power loss is determined for a uniform layer. Uniform tangential magnetic fields $H(0)$ and $H(h)$ are applied to the layer surfaces.

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where n_ℓ is the number of turns in the layer, and R_{dc} is the dc resistance of the layer. The functions $G_1(\varphi)$ and $G_2(\varphi)$ are

$$G_1(\varphi) = \frac{\sinh(2\varphi) + \sin(2\varphi)}{\cosh(2\varphi) - \cos(2\varphi)}$$
$$G_2(\varphi) = \frac{\sinh(\varphi)\cos(\varphi) + \cosh(\varphi)\sin(\varphi)}{\cosh(2\varphi) - \cos(2\varphi)} \tag{13.75}$$

If the winding carries current of rms magnitude I, then we can write

$$\mathscr{F}(h) - \mathscr{F}(0) = n_\ell I \tag{13.76}$$

Let us further express $\mathscr{F}(h)$ in terms of the winding current I, as

$$\mathscr{F}(h) = m n_\ell I \tag{13.77}$$

The quantity m is therefore the ratio of the MMF $\mathscr{F}(h)$ to the layer ampere-turns $n_\ell I$. Then,

$$\frac{\mathscr{F}(0)}{\mathscr{F}(h)} = \frac{m-1}{m} \tag{13.78}$$

The power dissipated in the layer, Eq. (13.74), can then be written

$$P = I^2 R_{dc} \varphi Q'(\varphi, m) \tag{13.79}$$

where

$$Q'(\varphi, m) = \left(2m^2 - 2m + 1\right) G_1(\varphi) - 4m\left(m - 1\right) G_2(\varphi) \tag{13.80}$$

We can conclude that the proximity effect increases the copper loss in the layer by the factor

$$\frac{P}{I^2 R_{dc}} = \varphi Q'(\varphi, m) \tag{13.81}$$

Equation (13.81), in conjunction with the definitions (13.80), (13.77), (13.75), and (13.73), can be plotted using a computer spreadsheet or small computer program. The result is illustrated in Fig. 13.31, for several values of m.

It is illuminating to express the layer copper loss P in terms of the dc power loss $P_{dc}|_{\varphi = 1}$ that would be obtained in a foil conductor having a thickness $\varphi = 1$. This loss is found by dividing Eq. (13.81) by the effective thickness ratio φ:

$$\frac{P}{P_{dc}\big|_{\varphi = 1}} = Q'(\varphi, m) \tag{13.82}$$

Equation (13.82) is plotted in Fig. 13.32. Large copper loss is obtained for small φ simply because the layer is thin and hence the dc resistance of the layer is large. For large m and large φ, the proximity effect leads to large power loss; Eq. (13.66) predicts that $Q'(\varphi, m)$ is asymptotic to $m^2 + (m-1)^2$ for large φ. Between these extremes, there is a value of φ which minimizes the layer copper loss.

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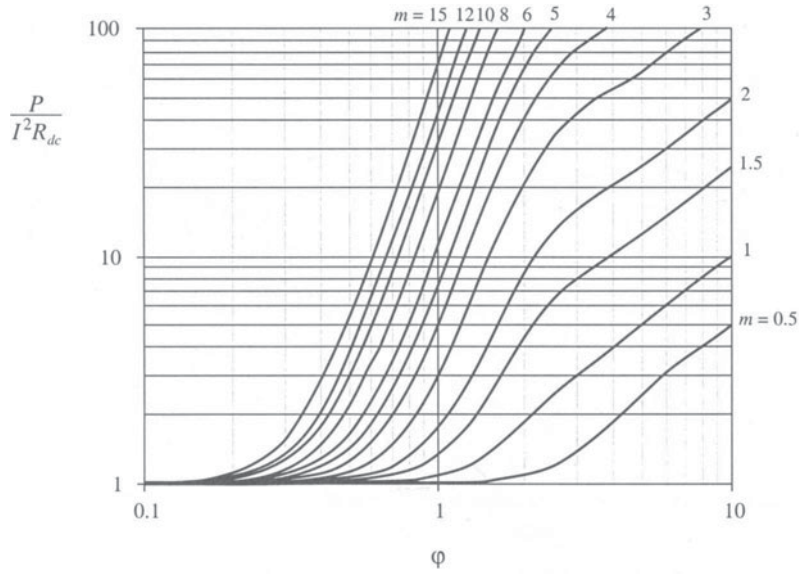


Fig. 13.31 Increase of layer copper loss due to the proximity effect, as a function of φ and MMF ratio m, for sinusoidal excitation.

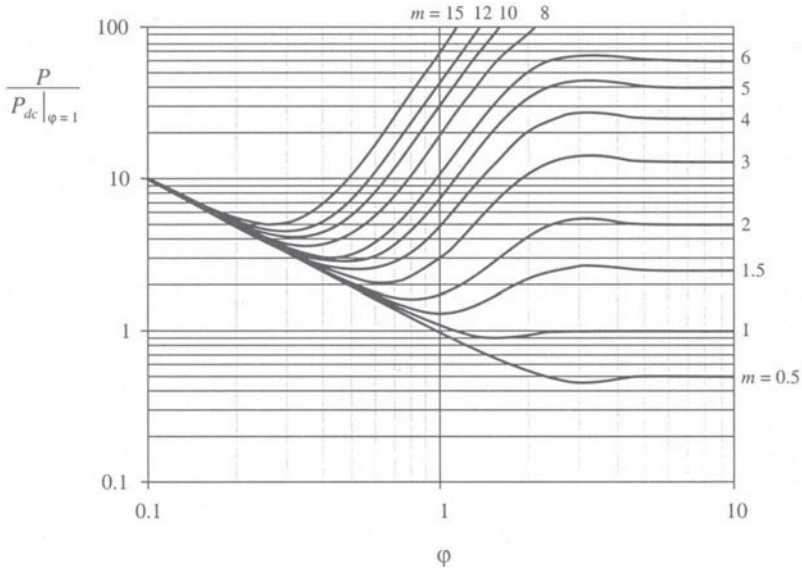


Fig. 13.32 Layer copper loss, relative to the dc loss in a layer having effective thickness of one penetration depth.

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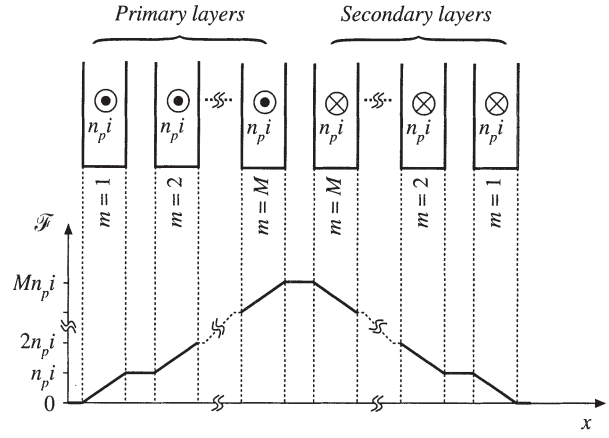


Fig. 13.33 Conventional two-winding transformer example. Each winding consists of M layers.

13.4.5 Example: Power Loss in a Transformer Winding

Let us again consider the proximity loss in a conventional transformer, in which the primary and secondary windings each consist of M layers. The normalized MMF diagram is illustrated in Fig. 13.33. As given by Eq. (13.81), the proximity effect increases the copper loss in each layer by the factor $\varphi Q'(\varphi, m)$. The total increase in primary winding copper loss P_{pri} is found by summation over all of the primary layers:

$$F_R = \frac{P_{pri}}{P_{pri,dc}} = \frac{1}{M} \sum_{m=1}^{M} \varphi Q'(\varphi, m) \tag{13.83}$$

Owing to the symmetry of the windings in this example, the secondary winding copper loss is increased by the same factor. Upon substituting Eq. (13.80) and collecting terms, we obtain

$$F_R = \frac{\varphi}{M} \sum_{m=1}^{M} \left[m^2 \left(2G_1(\varphi) - 4G_2(\varphi) \right) - m \left(2G_1(\varphi) - 4G_2(\varphi) \right) + G_1(\varphi) \right] \tag{13.84}$$

The summation can be expressed in closed form with the help of the identities

$$\begin{aligned} \sum_{m=1}^{M} m &= \frac{M(M+1)}{2} \\ \sum_{m=1}^{M} m^2 &= \frac{M(M+1)(2M+1)}{6} \end{aligned} \tag{13.85}$$

Use of these identities to simplify Eq. (13.84) leads to

$$F_R = \varphi \left[G_1(\varphi) + \frac{2}{3} \left(M^2 - 1 \right) \left(G_1(\varphi) - 2G_2(\varphi) \right) \right] \tag{13.86}$$

This expression is plotted in Fig. 13.34, for several values of M. For large φ, $G_1(\varphi)$ tends to 1, while

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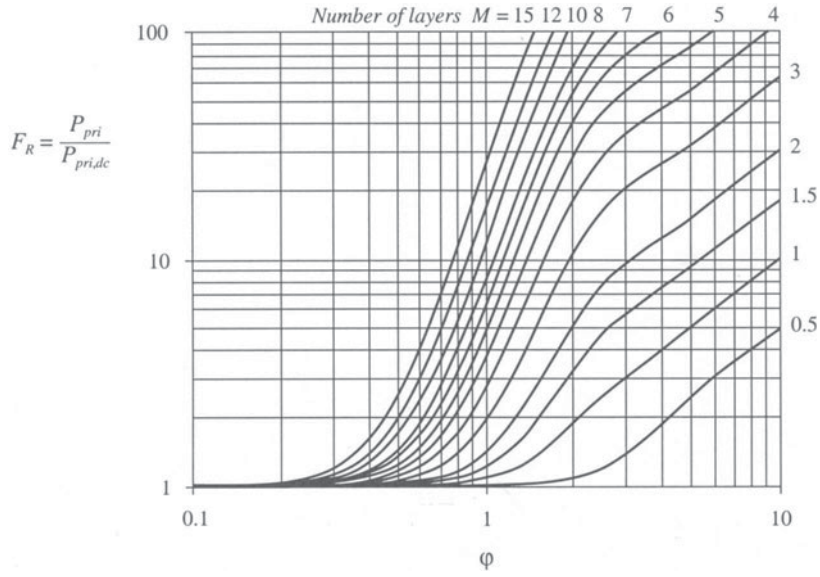


Fig. 13.34 Increased total winding copper loss in the two-winding transformer example, as a function of φ and number of layers M, for sinusoidal excitation.

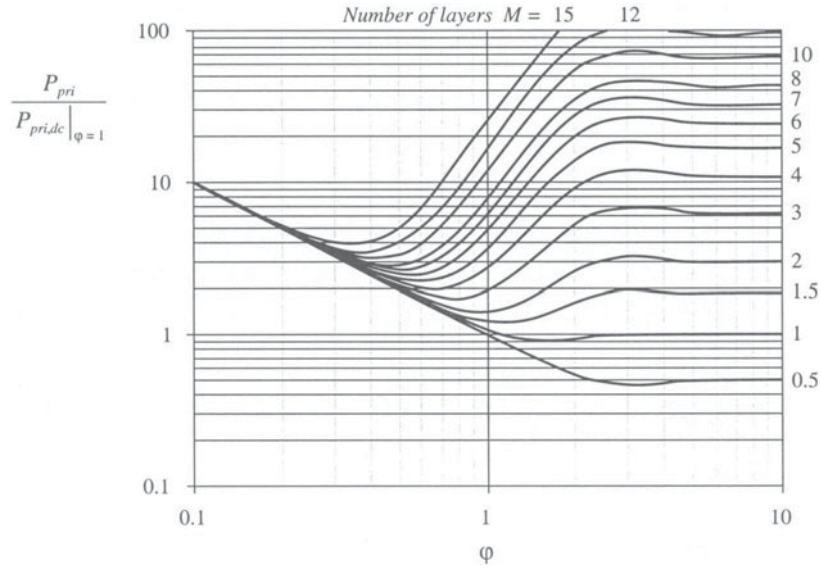


Fig. 13.35 Transformer example winding total copper loss, relative to the winding dc loss for layers having effective thicknesses of one penetration depth.

$G_2(\varphi)$ tends to 0. It can be verified that F_R then tends to the value predicted by Eq. (13.68).

We can again express the total primary power loss in terms of the dc power loss that would be obtained using a conductor in which $\varphi = 1$. This loss is found by dividing Eq. (13.86) by φ:

$$\frac{P_{pri}}{P_{pri,dc}\Big|_{\varphi=1}} = G_1(\varphi) + \frac{2}{3}\left(M^2 - 1\right)\Big(G_1(\varphi) - 2G_2(\varphi)\Big) \tag{13.87}$$

This expression is plotted in Fig. 13.35, for several values of M. Depending on the number of layers, the minimum copper loss for sinusoidal excitation is obtained for φ near to, or somewhat less than, unity.

13.4.6 Interleaving the Windings

One way to reduce the copper losses due to the proximity effect is to interleave the windings. Figure 13.36 illustrates the MMF diagram for a simple transformer in which the primary and secondary layers are alternated, with net layer current of magnitude i. It can be seen that each layer operates with $\mathscr{F} = 0$ on one side, and $\mathscr{F} = i$ on the other. Hence, each layer operates effectively with $m = 1$. Note that Eq. (13.74) is symmetric with respect to $\mathscr{F}(0)$ and $\mathscr{F}(h)$; hence, the copper losses of the interleaved secondary and primary layers are identical. The proximity losses of the entire winding can therefore be determined directly from Fig. 13.34 and 13.35, with $M = 1$. It can be shown that the minimum copper loss for this case (with sinusoidal currents) occurs with $\varphi = \pi/2$, although the copper loss is nearly constant for any $\varphi \geq 1$, and is approximately equal to the dc copper loss obtained when $\varphi = 1$. It should be apparent that interleaving can lead to significant improvements in copper loss when the winding contains several layers.

Partial interleaving can lead to a partial improvement in proximity loss. Figure 13.37 illustrates a transformer having three primary layers and four secondary layers. If the total current carried by each primary layer is $i(t)$, then each secondary layer should carry current $0.75i(t)$. The maximum MMF again occurs in the spaces between the primary and secondary windings, but has value $1.5i(t)$.

To determine the value for m in a given layer, we can solve Eq. (13.78) for m:

$$m = \frac{\mathscr{F}(h)}{\mathscr{F}(h) - \mathscr{F}(0)} \tag{13.88}$$

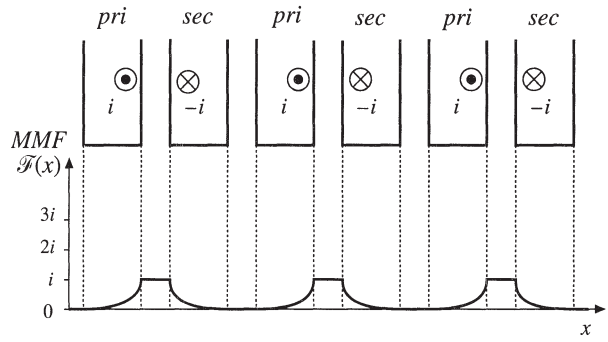


Fig. 13.36 MMF diagram for a simple transformer with interleaved windings. Each layer operates with $m = 1$.

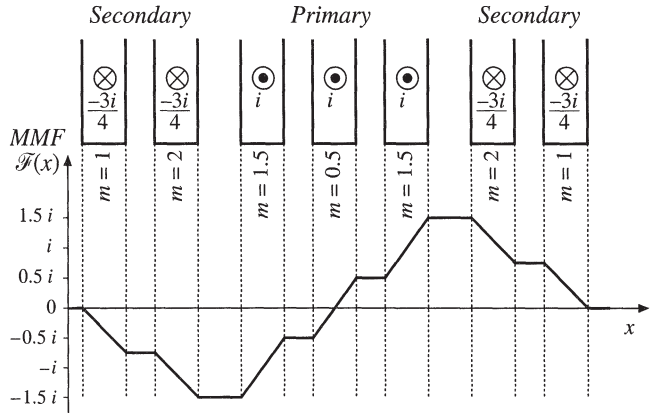


Fig. 13.37 A partially interleaved two-winding transformer, illustrating fractional values of m. The MMF diagram is constructed for the low-frequency limit.

The above expression is valid in general, and Eq. (13.74) is symmetrical in $\mathcal{F}(0)$ and $\mathcal{F}(h)$. However, when $F(0)$ is greater in magnitude than $\mathcal{F}(h)$, it is convenient to interchange the roles of $\mathcal{F}(0)$ and $\mathcal{F}(h)$, so that the plots of Figs. 13.31 and 13.32 can be employed.

In the leftmost secondary layer of Fig. 13.37, the layer carries current $-0.75i$. The MMF changes from 0 to $-0.75i$. The value of m for this layer is found by evaluation of Eq. (13.88):

$$m = \frac{\mathcal{F}(h)}{\mathcal{F}(h) - \mathcal{F}(0)} = \frac{-0.75i}{-0.75i - 0} = 1 \tag{13.89}$$

The loss in this layer, relative to the dc loss of this secondary layer, can be determined using the plots of Figs. 13.31 and 13.32 with $m = 1$. For the next secondary layer, we obtain

$$m = \frac{\mathcal{F}(h)}{\mathcal{F}(h) - \mathcal{F}(0)} = \frac{-1.5i}{-1.5i - (-0.75i)} = 2 \tag{13.90}$$

Hence the loss in this layer can be determined using the plots of Figs. 13.31 and 13.32 with $m = 2$.The next layer is a primary-winding layer. Its value of m can be expressed as

$$m = \frac{\mathcal{F}(0)}{\mathcal{F}(0) - \mathcal{F}(h)} = \frac{-1.5i}{-1.5i - (-0.5i)} = 1.5 \tag{13.91}$$

The loss in this layer, relative to the dc loss of this primary layer, can be determined using the plots of Figs. 13.31 and 13.32 with $m = 1.5$. The center layer has an m of

$$m = \frac{\mathcal{F}(h)}{\mathcal{F}(h) - \mathcal{F}(0)} = \frac{0.5i}{0.5i - (-0.5i)} = 0.5 \tag{13.92}$$

The loss in this layer, relative to the dc loss of this primary layer, can be determined using the plots of Figs. 13.31 and 13.32 with $m = 0.5$. The remaining layers are symmetrical to the corresponding layers described above, and have identical copper losses. The total loss in the winding is found by summing the losses described above for each layer.

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Interleaving windings can significantly reduce the proximity loss when the primary and secondary currents are in phase. However, in some cases such as the transformers of the flyback and SEPIC converters, the winding currents are out of phase. Interleaving then does little to reduce the MMFs and magnetic fields in the vicinity of the windings, and hence the proximity loss is essentially unchanged. It should also be noted that Eqs. (13.74) to (13.82) assume that the winding currents are in phase. General expressions for out-of-phase currents, as well as analysis of a flyback example, are given in [10].

The above procedure can be used to determine the high-frequency copper losses of more complicated multiple-winding magnetic devices. The MMF diagrams are constructed, and then the power loss in each layer is evaluated using Eq. (13.81). These losses are summed, to find the total copper loss. The losses induced in electrostatic shields can also be determined. Several additional examples are given in [10].

It can be concluded that, for sinusoidal currents, there is an optimal conductor thickness in the vicinity of $\varphi = 1$ that leads to minimum copper loss. It is highly advantageous to minimize the number of layers, and to interleave the windings. The amount of copper in the vicinity of the high-MMF portions of windings should be kept to a minimum. Core geometries that maximize the width ℓ_w of the layers, while minimizing the overall number of layers, lead to reduced proximity loss.

Use of *Litz* wire is another means of increasing the conductor area while maintaining low proximity losses. Tens, hundreds, or more strands of small-gauge insulated copper wire are bundled together, and are externally connected in parallel. These strands are twisted, or transposed, such that each strand passes equally through each position inside and on the surface of the bundle. This prevents the circulation of high-frequency currents between strands. To be effective, the diameter of the strands should be sufficiently less than one skin depth. Also, it should be pointed out that the Litz wire bundle itself is composed of multiple layers. The disadvantages of Litz wire are its increased cost, and its reduced fill factor.

13.4.7 PWM Waveform Harmonics

The pulse-width-modulated waveforms encountered in switching converters contain significant harmonics, which can lead to increased proximity losses. The effect of harmonics on the losses in a layer can be determined via field harmonic analysis [10], in which the MMF waveforms $\mathscr{F}(0,t)$ and $\mathscr{F}(d,t)$ of Eq. (13.74) are expressed in Fourier series. The power loss of each individual harmonic is computed as in Section 13.4.4, and the losses are summed to find the total loss in a layer. For example, the PWM waveform of Fig. 13.38 can be represented by the following Fourier series:

$$i(t) = I_0 + \sum_{j=1}^{\infty} \sqrt{2}\, I_j \cos(j\omega t) \tag{13.93}$$

where

$$I_j = \frac{\sqrt{2}\, I_{pk}}{j\pi} \sin(j\pi D)$$

with $\omega = 2\pi/T_s$. This waveform contains a dc component $I_0 = DI_{pk}$, plus harmonics of rms magnitude I_j proportional to $1/j$. The transformer winding current waveforms of most switching converters follow this Fourier series, or a similar series.

Effects of waveforms harmonics on proximity losses are discussed in [8–10]. The dc component of the winding currents does not lead to proximity loss, and should not be included in proximity loss calculations. Failure to remove the dc component can lead to significantly pessimistic estimates of copper

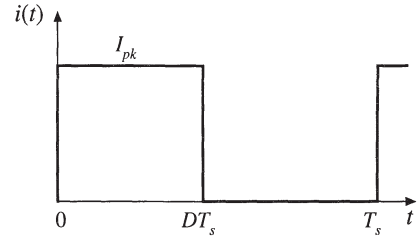


Fig. 13.38 Pulse-width modulated winding current waveform.

loss. The skin depth δ is smaller for high frequency harmonics than for the fundamental, and hence the waveform harmonics exhibit an increased effective φ. Let φ_1 be given by Eq. (13.73), in which δ is found by evaluation of Eq. (13.60) at the fundamental frequency. Since the penetration depth δ varies as the inverse square-root of frequency, the effective value of φ for harmonic j is

$$\varphi_j = \sqrt{j}\,\varphi_1 \tag{13.94}$$

In a multiple-layer winding excited by a current waveform whose fundamental component has $\varphi = \varphi_1$ close to 1, harmonics can significantly increase the total copper loss. This occurs because, for $m > 1$, $Q'(\varphi, m)$ is a rapidly increasing function of φ in the vicinity of 1. When φ_1 is sufficiently greater than 1, then $Q'(\varphi, m)$ is nearly constant, and harmonics have less influence on the total copper loss.

For example, suppose that the two-winding transformer of Fig. 13.33 is employed in a converter such as the forward converter, in which a winding current waveform $i(t)$ can be well approximated by the Fourier series of Eq. (13.93). The winding contains M layers, and has dc resistance R_{dc}. The copper loss induced by the dc component is

$$P_{dc} = I_0^2 R_{dc} \tag{13.95}$$

The copper loss P_j ascribable to harmonic j is found by evaluation of Eq. (13.86) with $\varphi = \varphi_j$:

$$P_j = I_j^2 R_{dc} \sqrt{j}\,\varphi_1 \left[G_1(\sqrt{j}\,\varphi_1) + \frac{2}{3}\left(M^2 - 1\right)\left(G_1(\sqrt{j}\,\varphi_1) - 2G_2(\sqrt{j}\,\varphi_1)\right)\right] \tag{13.96}$$

The total copper loss in the winding is the sum of losses arising from all components of the harmonic series:

$$\frac{P_{cu}}{DI_{pk}^2 R_{dc}} = D + \frac{2\varphi_1}{D\pi^2} \sum_{j=1}^{\infty} \frac{\sin^2(j\pi D)}{j\sqrt{j}} \left[G_1(\sqrt{j}\,\varphi_1) + \frac{2}{3}\left(M^2 - 1\right)\left(G_1(\sqrt{j}\,\varphi_1) - 2G_2(\sqrt{j}\,\varphi_1)\right)\right] \tag{13.97}$$

In Eq. (13.97), the copper loss is expressed relative to the loss $DI_{pk}^2 R_{dc}$ predicted by a low-frequency analysis. This expression can be evaluated by use of a computer program or computer spreadsheet.

To explicitly quantify the effects of harmonics, we can define the harmonic loss factor F_H as

$$F_H = \frac{\sum_{j=1}^{\infty} P_j}{P_1} \tag{13.98}$$

with P_j given by Eq. (13.96). The total winding copper loss is then given by

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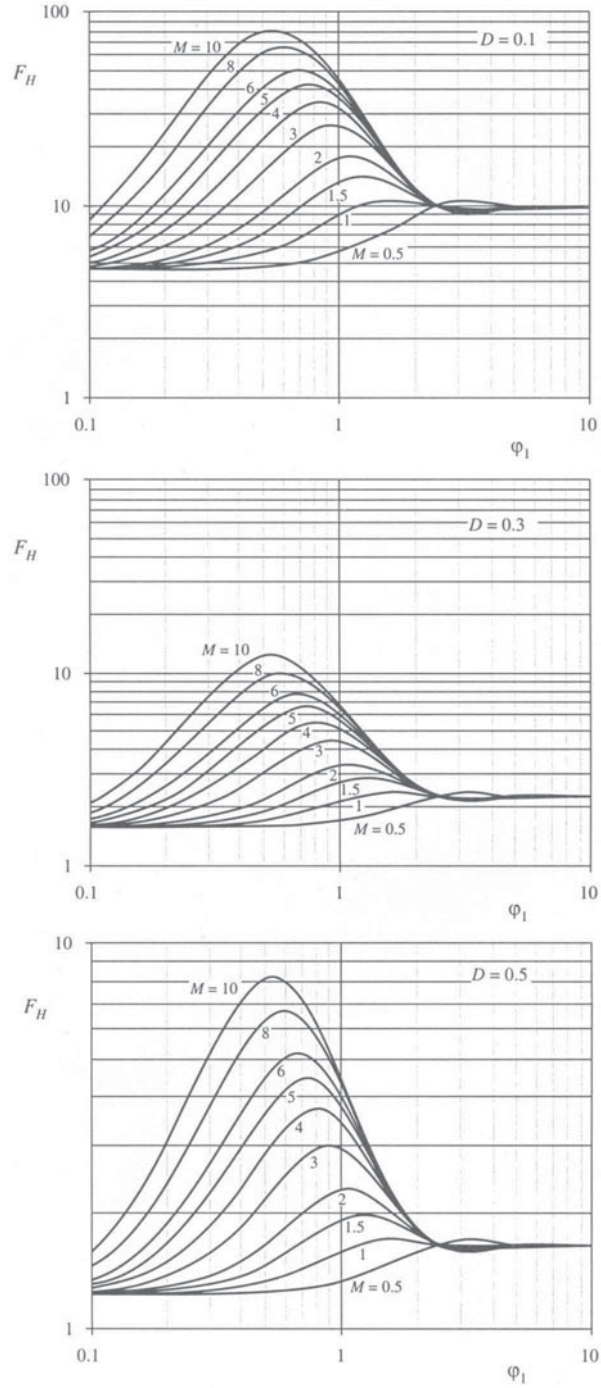


Fig. 13.39 Increased proximity losses induced by PWM waveform harmonics, forward converter example: (a) at $D = 0.1$, (b) at $D = 0.3$, (c) at $D = 0.5$.

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$$P_{cu} = I_0^2 R_{dc} + F_H F_R I_1^2 R_{dc} \tag{13.99}$$

with F_R given by Eq. (13.86). The harmonic factor F_H is a function not only of the winding geometry, but also of the harmonic spectrum of the winding current waveform. The harmonic factor F_H is plotted in Fig. 13.39 for several values of D, for the simple transformer example. The total harmonic distortion (THD) of the example current waveforms are: 48% for $D = 0.5$, 76% for $D = 0.3$, and 191% for $D = 0.1$. The waveform THD is defined as

$$\text{THD} = \frac{\sqrt{\sum_{j=2}^{\infty} I_j^2}}{I_1} \tag{13.100}$$

It can be seen that harmonics significantly increase the proximity loss of a multilayer winding when φ_1 is close to 1. For sufficiently small φ_1, the proximity effect can be neglected, and F_H tends to the value $1 + (\text{THD})^2$. For large φ_1, the harmonics also increase the proximity loss; however, the increase is less dramatic than for φ_1 near 1 because the fundamental component proximity loss is large. It can be concluded that, when the current waveform contains high THD and when the winding contains several layers or more, then proximity losses can be kept low only by choosing φ_1 much less than 1. Interleaving the windings allows a larger value of φ_1 to be employed.

13.5 SEVERAL TYPES OF MAGNETIC DEVICES, THEIR *B–H* LOOPS, AND CORE VS. COPPER LOSS

A variety of magnetic elements are commonly used in power applications, which employ the properties of magnetic core materials and windings in different ways. As a result, quite a few factors constrain the design of a magnetic device. The maximum flux density must not saturate the core. The peak ac flux density should also be sufficiently small, such that core losses are acceptably low. The wire size should be sufficiently small, to fit the required number of turns in the core window. Subject to this constraint, the wire cross-sectional area should be as large as possible, to minimize the winding dc resistance and copper loss. But if the wire is too thick, then unacceptable copper losses occur owing to the proximity effect. An air gap is needed when the device stores significant energy. But an air gap is undesirable in transformer applications. It should be apparent that, for a given magnetic device, some of these constraints are active while others are not significant.

Thus, design of a magnetic element involves not only obtaining the desired inductance or turns ratio, but also ensuring that the core material does not saturate and that the total power loss is not too large. Several common power applications of magnetics are discussed in this section, which illustrate the factors governing the choice of core material, maximum flux density, and design approach.

13.5.1 Filter Inductor

A filter inductor employed in a CCM buck converter is illustrated in Fig. 13.40(a). In this application, the value of inductance L is usually chosen such that the inductor current ripple peak magnitude Δi is a small fraction of the full-load inductor current dc component I, as illustrated in Fig. 13.40(b). As illustrated in Fig. 13.41, an air gap is employed that is sufficiently large to prevent saturation of the core by the peak current $I + \Delta i$.

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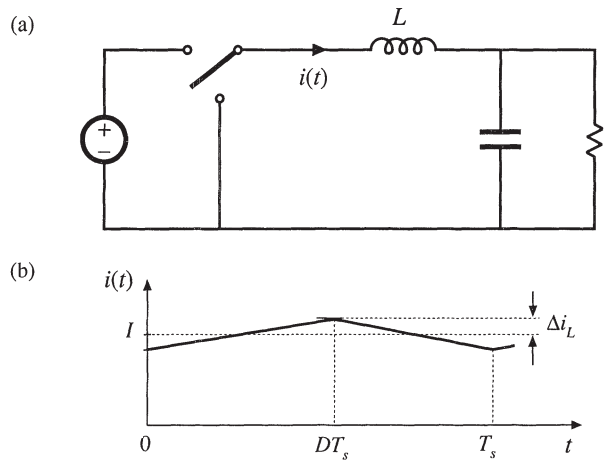


Fig. 13.40 Filter inductor employed in a CCM buck converter: (a) circuit schematic, (b) inductor current waveform.

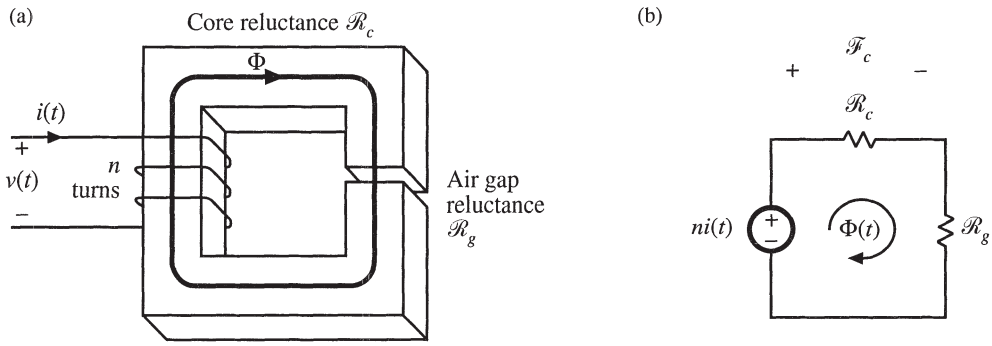


Fig. 13.41 Filter inductor: (a) structure, (b) magnetic circuit model.

The core magnetic field strength $H_c(t)$ is related to the winding current $i(t)$ according to

$$H_c(t) = \frac{ni(t)}{\ell_c} \frac{\mathcal{R}_c}{\mathcal{R}_c + \mathcal{R}_g} \tag{13.101}$$

where ℓ_c is the magnetic path length of the core. Since $H_c(t)$ is proportional to $i(t)$, $H_c(t)$ can be expressed as a large dc component H_{c0} and a small superimposed ac ripple ΔH_c, where

$$\begin{aligned} H_{c0} &= \frac{nI}{\ell_c} \frac{\mathcal{R}_c}{\mathcal{R}_c + \mathcal{R}_g} \\ \Delta H_c &= \frac{n\Delta i}{\ell_c} \frac{\mathcal{R}_c}{\mathcal{R}_c + \mathcal{R}_g} \end{aligned} \tag{13.102}$$

A sketch of $B(t)$ vs. $H_c(t)$ for this application is given in Fig. 13.42. This device operates with the minor B–H loop illustrated. The size of the minor loop, and hence the core loss, depends on the magnitude of the inductor current ripple Δi. The copper loss depends on the rms inductor current ripple, essentially

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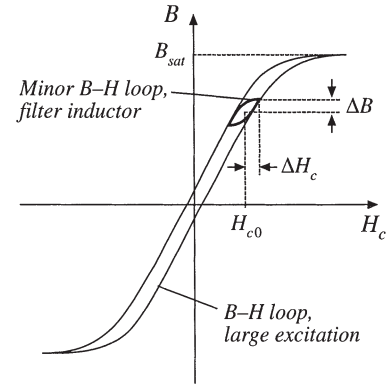


Fig. 13.42 Filter inductor minor *B–H* loop.

equal to the dc component *I*. Typically, the core loss can be ignored, and the design is driven by the copper loss. The maximum flux density is limited by saturation of the core. Proximity losses are negligible. Although a high-frequency ferrite material can be employed in this application, other materials having higher core losses and greater saturation flux density lead to a physically smaller device. Design of a filter inductor in which the maximum flux density is a specified value is considered in the next chapter.

13.5.2 AC Inductor

An ac inductor employed in a resonant converter is illustrated in Fig. 13.43. In this application, the high-frequency current variations are large. In consequence, the $B(t)$–$H(t)$ loop illustrated in Fig. 13.44 is large. Core loss and proximity loss are usually significant in this application. The maximum flux density

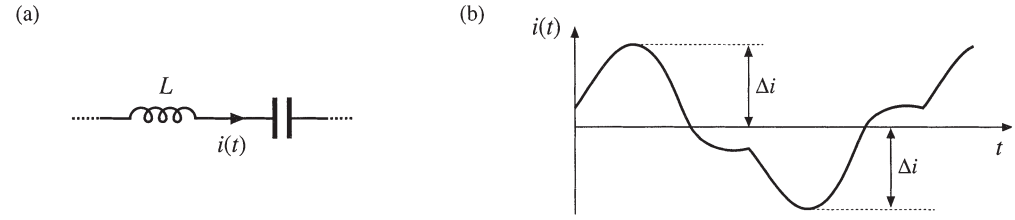


Fig. 13.43 Ac inductor, resonant converter example: (a) resonant tank circuit, (b) inductor current waveform.

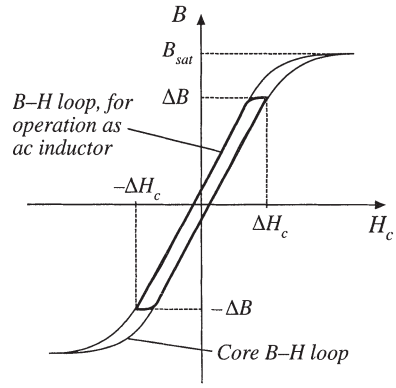


Fig. 13.44 Operational *B–H* loop of an ac inductor.

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is limited by core loss rather than saturation. Both core loss and copper loss must be accounted for in the design of this element, and the peak ac flux density ΔB is a design variable that is typically chosen to minimize the total loss. A high-frequency material having low core loss, such as ferrite, is normally employed. Design of magnetics such as this, in which the ac flux density is a design variable that is chosen in a optimal manner, is considered in Chapter 15.

13.5.3 Transformer

Figure 13.45 illustrates a conventional transformer employed in a switching converter. Magnetization of the core is modeled by the magnetizing inductance L_M. The magnetizing current $i_M(t)$ is related to the core magnetic field $H(t)$ according to Ampere's law

$$H(t) = \frac{n i_M(t)}{\ell_m} \tag{13.103}$$

However, $i_M(t)$ is not a direct function of the winding currents $i_1(t)$ or $i_2(t)$. Rather, the magnetizing current is dependent on the applied winding voltage waveform $v_1(t)$. Specifically, the maximum ac flux density is directly proportional to the applied volt-seconds λ_1. A typical B–H loop for this application is illustrated in Fig. 13.46.

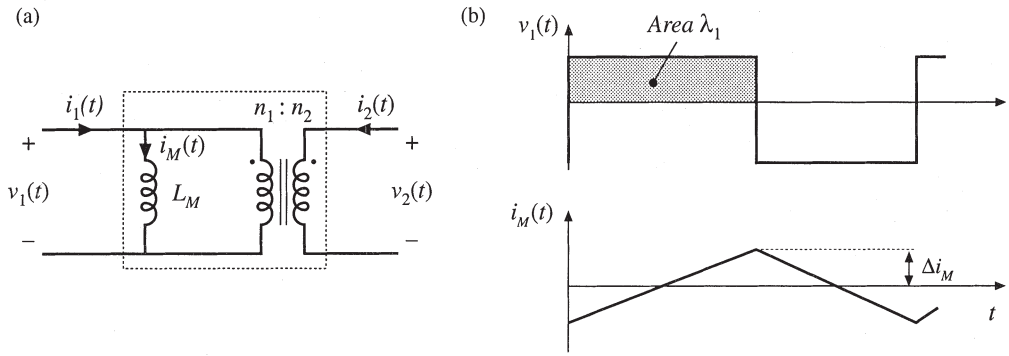


Fig. 13.45 Conventional transformer: (a) equivalent circuit, (b) typical primary voltage and magnetizing current waveforms.

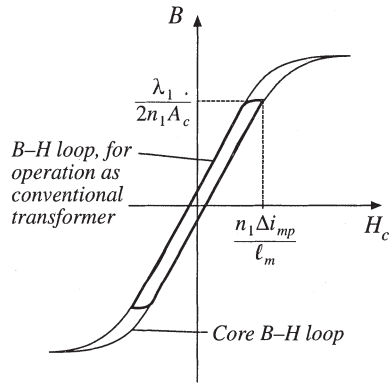


Fig. 13.46 Operational B–H loop of a conventional transformer.

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In the transformer application, core loss and proximity losses are usually significant. Typically the maximum flux density is limited by core loss rather than by saturation. A high-frequency material having low core loss is employed. Both core and copper losses must be accounted for in the design of the transformer. The design must also incorporate multiple windings. Transformer design with flux density optimized for minimum total loss is described in Chapter 15.

13.5.4 Coupled Inductor

A coupled inductor is a filter inductor having multiple windings. Figure 13.47(a) illustrates coupled inductors in a two-output forward converter. The inductors can be wound on the same core, because the winding voltage waveforms are proportional. The inductors of the SEPIC and Ćuk converters, as well as of multiple-output buck-derived converters and some other converters, can be coupled. The inductor current ripples can be controlled by control of the winding leakage inductances [12,13]. Dc currents flow in each winding as illustrated in Fig. 13.47(b), and the net magnetization of the core is proportional to the sum of the winding ampere-turns:

$$H_c(t) = \frac{n_1 i_1(t) + n_2 i_2(t)}{\ell_c} \frac{\mathcal{R}_c}{\mathcal{R}_c + \mathcal{R}_g} \tag{13.104}$$

As in the case of the single-winding filter inductor, the size of the minor *B–H* loop is proportional to the total current ripple (Fig. 13.48). Small ripple implies small core loss, as well as small proximity loss. An air gap is employed, and the maximum flux density is typically limited by saturation.

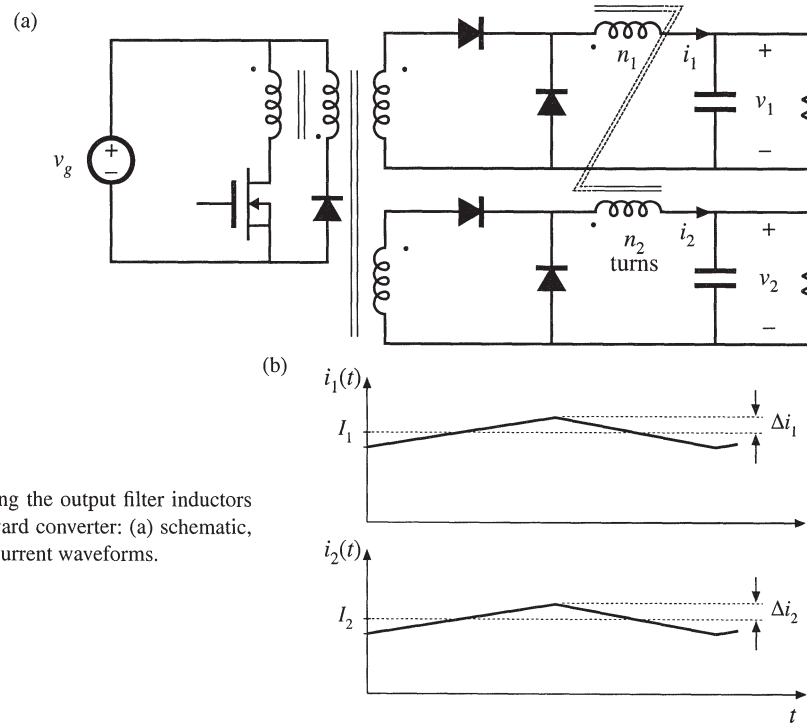


Fig. 13.47 Coupling the output filter inductors of a two-output forward converter: (a) schematic, (b) typical inductor current waveforms.

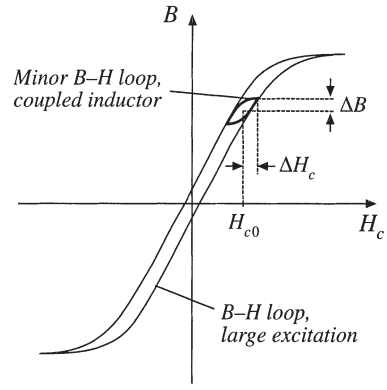


Fig. 13.48 Coupled inductor minor *B–H* loop.

13.5.5 Flyback Transformer

As discussed in Chapter 6, the flyback transformer functions as an inductor with two windings. The primary winding is used during the transistor conduction interval, and the secondary is used during the diode conduction interval. A flyback converter is illustrated in Fig. 13.49(a), with the flyback transformer modeled as a magnetizing inductance in parallel with an ideal transformer. The magnetizing current $i_M(t)$ is proportional to the core magnetic field strength $H_c(t)$. Typical DCM waveforms are given in Fig. 13.49(b).

Since the flyback transformer stores energy, an air gap is needed. Core loss depends on the magnitude of the ac component of the magnetizing current. The *B–H* loop for discontinuous conduction mode operation is illustrated in Fig. 13.50. When the converter is designed to operate in DCM, the core loss is significant. The peak ac flux density ΔB is then chosen to maintain an acceptably low core loss. For CCM operation, core loss is less significant, and the maximum flux density may be limited only by saturation of the core. In either case, winding proximity losses are typically quite significant. Unfortunately, interleaving the windings has little impact on the proximity loss because the primary and secondary winding currents are out of phase.

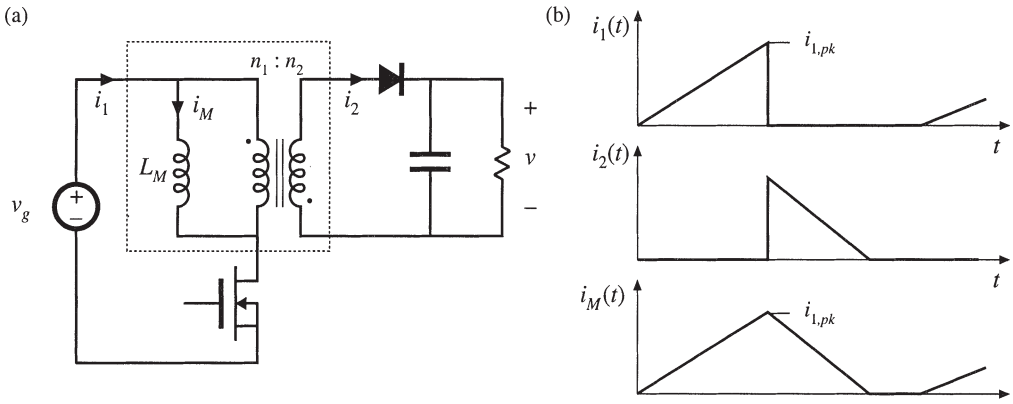


Fig. 13.49 Flyback transformer: (a) converter schematic, with transformer equivalent circuit, (b) DCM current waveforms.

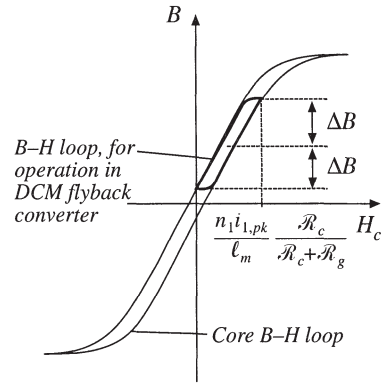


Fig. 13.50 Operational *B–H* loop of a DCM flyback transformer.

13.6 SUMMARY OF KEY POINTS

1. Magnetic devices can be modeled using lumped-element magnetic circuits, in a manner similar to that commonly used to model electrical circuits. The magnetic analogs of electrical voltage V, current I, and resistance R, are magnetomotive force (MMF) $\mathscr{F}$, flux Φ, and reluctance $\mathscr{R}$ respectively.
2. Faraday's law relates the voltage induced in a loop of wire to the derivative of flux passing through the interior of the loop.
3. Ampere's law relates the total MMF around a loop to the total current passing through the center of the loop. Ampere's law implies that winding currents are sources of MMF, and that when these sources are included, then the net MMF around a closed path is equal to zero.
4. Magnetic core materials exhibit hysteresis and saturation. A core material saturates when the flux density B reaches the saturation flux density B_{sat}.
5. Air gaps are employed in inductors to prevent saturation when a given maximum current flows in the winding, and to stabilize the value of inductance. The inductor with air gap can be analyzed using a simple magnetic equivalent circuit, containing core and air gap reluctances and a source representing the winding MMF.
6. Conventional transformers can be modeled using sources representing the MMFs of each winding, and the core MMF. The core reluctance approaches zero in an ideal transformer. Nonzero core reluctance leads to an electrical transformer model containing a magnetizing inductance, effectively in parallel with the ideal transformer. Flux that does not link both windings, or "leakage flux," can be modeled using series inductors.
7. The conventional transformer saturates when the applied winding volt-seconds are too large. Addition of an air gap has no effect on saturation. Saturation can be prevented by increasing the core cross-sectional area, or by increasing the number of primary turns.
8. Magnetic materials exhibit core loss, due to hysteresis of the *B–H* loop and to induced eddy currents flowing in the core material. In available core materials, there is a tradeoff between high saturation flux density B_{sat} and high core loss P_{fe}. Laminated iron alloy cores exhibit the highest B_{sat} but also the highest P_{fe}, while ferrite cores exhibit the lowest P_{fe} but also the lowest B_{sat}. Between these two extremes are powdered iron alloy and amorphous alloy materials.
9. The skin and proximity effects lead to eddy currents in winding conductors, which increase the copper loss P_{cu} in high-current high-frequency magnetic devices. When a conductor has thickness approaching or

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larger than the penetration depth δ, magnetic fields in the vicinity of the conductor induce eddy currents in the conductor. According to Lenz's law, these eddy currents flow in paths that tend to oppose the applied magnetic fields.

10. The magnetic field strengths in the vicinity of the winding conductors can be determined by use of MMF diagrams. These diagrams are constructed by application of Ampere's law, following the closed paths of the magnetic field lines which pass near the winding conductors. Multiple-layer noninterleaved windings can exhibit high maximum MMFs, with resulting high eddy currents and high copper loss.

11. An expression for the copper loss in a layer, as a function of the magnetic field strengths or MMFs surrounding the layer, is given in Section 13.4.4. This expression can be used in conjunction with the MMF diagram, to compute the copper loss in each layer of a winding. The results can then be summed, yielding the total winding copper loss. When the effective layer thickness is near to or greater than one skin depth, the copper losses of multiple-layer noninterleaved windings are greatly increased.

12. Pulse-width-modulated winding currents contain significant total harmonic distortion, which can lead to a further increase of copper loss. The increase in proximity loss caused by current harmonics is most pronounced in multiple-layer non-interleaved windings, with an effective layer thickness near one skin depth.

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PROBLEMS

13.1 The core illustrated in Fig. 13.51(a) is 1 cm thick. All legs are 1 cm wide, except for the right-hand side vertical leg, which is 0.5 cm wide. You may neglect nonuniformities in the flux distribution caused by turning corners.

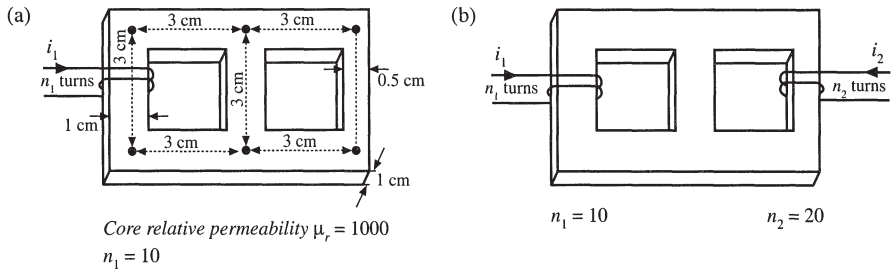


Fig. 13.51 Problem 13.1

(a) Determine the magnetic circuit model of this device, and label the values of all reluctances in your model.

(b) Determine the inductance of the winding.

A second winding is added to the same core, as shown in Fig. 13.51(b).

(c) Modify your model of part (a) to include this winding.

(d) The electrical equations for this circuit may be written in the form

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{22} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$

Use superposition to determine analytical expressions and numerical values for L_{11}, L_{12}, and L_{22}.

13.2 Two windings are placed as illustrated in Fig. 13.52(a) on a core of uniform cross-sectional area $A_c = 1$ cm^2. Each winding has 50 turns. The relative permeability of the core is $\mu_r = 10^4$.

(a) Sketch an equivalent magnetic circuit, and determine numerical values for each reluctance.

(b) Determine the self-inductance of each winding.

(c) Determine the inductance L^+ obtained when the windings are connected in series as in Fig. 13.52(b).

(d) Determine the inductance L^- obtained when the windings are connected in anti-series as in Fig. 13.52(c).

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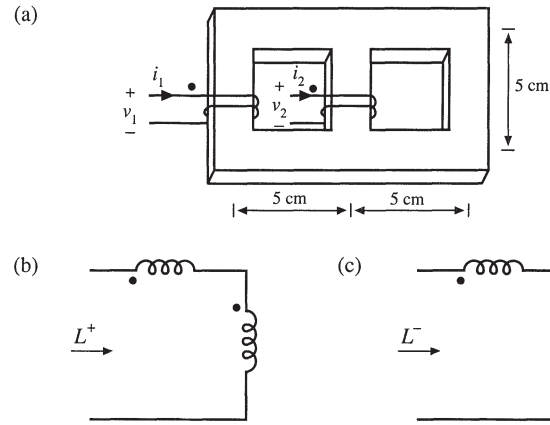


Fig. 13.52 Problem 13.2.

13.3 All three legs of the magnetic device illustrated in Fig. 13.53 are of uniform cross-sectional area A_C. Legs 1 and 2 each have magnetic path length 3ℓ, while leg 3 has magnetic path length ℓ. Both windings have n turns. The core has permeability $\mu \gg \mu_0$.

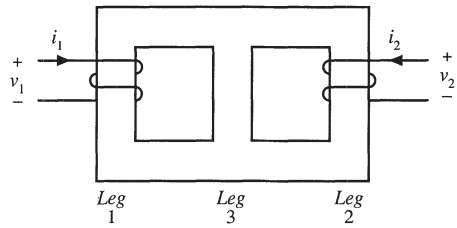


Fig. 13.53 Magnetic core for Problem 13.3.

(a) Sketch a magnetic equivalent circuit, and give analytical expressions for all element values.

A voltage source is connected to winding 1, such that $v_1(t)$ is a square wave of peak value V_{max} and period T_s. Winding 2 is open-circuited.

(b) Sketch $i_1(t)$ and label its peak value.

(c) Find the flux $\varphi_2(t)$ in leg 2. Sketch $\varphi_2(t)$ and label its peak value.

(d) Sketch $v_2(t)$ and label its peak value.

13.4 The magnetic device illustrated in Fig. 13.54(a) consists of two windings, which can replace the two inductors in a Ćuk, SEPIC, or other similar converter. For this problem, all three legs have the same uniform cross-sectional area A_c. The legs have gaps of lengths g_1, g_2, and g_3, respectively. The core permeability μ is very large. You may neglect fringing flux. Legs 1 and 2 have windings containing n_1 and n_2 turns, respectively.

(a) Derive a magnetic circuit model for this device, and give analytical expressions for each reluctance in your model. Label the polarities of the MMF generators.

(b) Write the electrical terminal equations of this device in the matrix form

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{22} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$

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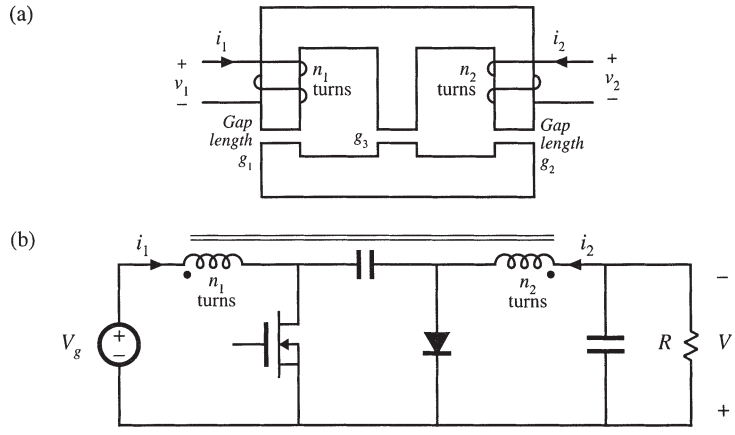


Fig. 13.54 Magnetic core and converter for Problem 13.4.

and derive analytical expressions for L_{11}, L_{12}, and L_{22}.

(c) Derive an electrical circuit model for this device, and give analytical expressions for the turns ratio and each inductance in your model, in terms of the turns and reluctances of part (a).

This single magnetic device is to be used to realize the two inductors of the Ćuk converter, as in Fig. 13.54(b).

(d) Sketch the voltage waveforms $v_1(t)$ and $v_2(t)$, making the linear ripple approximation as appropriate. You may assume that the converter operates in the continuous conduction mode.

(e) The voltage waveforms of part (d) are applied to your model of parts (b) and (c). Solve your model to determine the slopes of the inductor current ripples during intervals DT_s and $D'T_s$. Sketch the steady-state inductor current waveforms $i_1(t)$ and $i_2(t)$, and label all slopes.

(f) By skillful choice of n_1/n_2 and the air gap lengths, it is possible to make the inductor current ripple Δi in either $i_1(t)$ or $i_2(t)$ go to zero. Determine the conditions on n_1/n_2, g_1, g_2, and g_3 that cause the current ripple in $i_2(t)$ to become zero. Sketch the resulting $i_1(t)$ and $i_2(t)$, and label all slopes.

It is possible to couple the inductors in this manner, and cause one of the inductor current ripples to go to zero, in any converter in which the inductor voltage waveforms are proportional.

13.5 Over its usable operating range, a certain permanent magnet material has the *B–H* characteristics illustrated by the solid line in Fig. 13.55. The magnet has length $\ell_m = 0.5$ cm, and cross-sectional area 4 cm^2. $B_m = 1$ T. Derive an equivalent magnetic circuit model for the magnet, and label the numerical values of the elements.

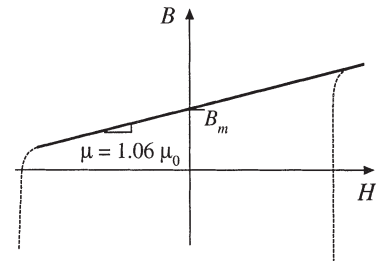


Fig. 13.55 *B–H* characteristic of the permanent magnet material for Problem 13.5.

13.6 The two-transistor forward converter of Fig. 6.27 operates with V_g = 300 V, V = 28 V, switching frequency f_s = 100 kHz, and turns ratio n = 0.25. The dc load power is 250 W. The transformer uses an EC41 ferrite core; relevant data for this core is listed in Appendix D. The core loss is given by Fig. 13.20. The primary winding consists of 44 turns of #21 AWG wire, and the secondary winding is composed of 11 turns of #15 AWG wire. Data regarding the American wire gauge is also listed in Appendix D.

(a) Estimate the core loss of this transformer

(b) Determine the copper loss of this transformer. You may neglect proximity losses.

13.7 The two-transistor forward converter of Fig. 6.27 operates in CCM with V_g = 300 V, V = 28 V, switching frequency f_s = 100 kHz, and turns ratio n = 0.25. The dc load power is 250 W. The transformer uses an EC41 ferrite core; relevant data for this core is listed in Appendix D. This core has window height ℓ_w = 2.78 cm. The primary winding consists of 44 turns of #24 AWG wire, and the secondary winding is composed of 11 turns of #14 AWG wire. Each winding comprises one layer. Data regarding the American wire gauge is also listed in Appendix D. The winding operates at room temperature.

(a) Determine the primary and secondary copper losses induced by the dc components of the winding currents.

(b) Determine the primary and secondary copper losses induced by the fundamental components of the winding currents.

(c) Determine the primary and secondary copper losses induced by the second harmonic components of the winding currents.

13.8 The winding currents of the transformer in a high-voltage inverter are essentially sinusoidal, with negligible harmonics and no dc components. The primary winding consists of one layer containing 10 turns of round copper wire. The secondary winding consists of 250 turns of round copper wire, arranged in ten layers. The operating frequency is f = 50 kHz, and the winding porosity is 0.8. Determine the primary and secondary wire diameters and wire gauges that minimize the total copper loss.

13.9 A certain three-winding transformer contains one primary and two secondaries. The operating frequency is 40 kHz. The primary winding contains a total of 60 turns of #26AWG, arranged in three layers. The secondary windings each consist of five turns of copper foil, one turn per layer. The foil thickness is 0.25 mm. The primary layers have porosity 0.8, while the secondary layer porosity is 1. The primary winding carries a sinusoidal current having rms value I, while each secondary carries rms current $6I$. The windings are not interleaved: the primary winding is closest to the center leg of the core, followed by secondary winding #1, followed by secondary winding #2.

(a) Sketch an MMF diagram illustrating the magnetic fields in the vicinity of each winding layer.

(b) Determine the increased copper loss, due to the proximity effect, in each layer.

(c) Determine the ratio of copper loss to dc copper loss, F_R, for the entire transformer windings.

(d) In this application, it is not feasible to interleave the primary winding with the other windings. However, changing the conductor size is permissible. Discuss how the windings could be better optimized.

13.10 A transformer winding contains a four-layer primary winding, and two two-layer secondary windings. Each layer of the primary winding carries total current I. Each layer of secondary winding #1 carries total current $1.5I$. Each layer of secondary winding #2 carries total current $0.5I$. All currents are sinusoidal. The effective relative conductor thickness is $\varphi = 2$. The windings are partially interleaved, in the following order: two primary layers, followed by both layers of secondary #1, followed by both layers of secondary #2, and finally the two remaining primary layers.

(a) Sketch an MMF diagram for this winding arrangement.

(b) Determine the increased copper loss, due to the proximity effect, for each layer.

(c) Determine the increase in total transformer copper loss, due to the proximity effect.

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13.11 A single-output forward converter contains a transformer having a noninterleaved secondary winding with four layers. The converter operates at $D = 0.3$ in CCM, with a secondary winding current waveform similar to Fig. 13.38.

(a) Estimate the value of φ_1 that minimizes the secondary winding copper losses.

(b) Determine the resulting secondary copper loss, relative to $I_{rms}^2 R_{dc}$.

13.12 A schematic diagram and waveforms of the isolated SEPIC, operating in CCM, are given in Figs. 6.37 and 6.38.

(a) Do you expect the SEPIC transformer to contain an air gap? Why or why not?

(b) Sketch the SEPIC transformer *B–H* loop, for CCM operation.

(c) For CCM operation, do you expect core loss to be significant? Explain your reasoning.

(d) For CCM operation, do you expect winding proximity losses to be significant? Explain your reasoning.

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14
Inductor Design

This chapter treats the design of magnetic elements such as filter inductors, using the K_g method. With this method, the maximum flux density B_{max} is specified in advance, and the element is designed to attain a given copper loss.

The design of a basic filter inductor is discussed in Sections 14.1 and 14.1.5. In the filter inductor application, it is necessary to obtain the required inductance, avoid saturation, and obtain an acceptable low dc winding resistance and copper loss. The geometrical constant K_g is a measure of the effective magnetic size of a core, when dc copper loss and winding resistance are the dominant constraints [1,2]. Design of a filter inductor involves selection of a core having a K_g sufficiently large for the application, then computing the required air gap, turns, and wire size. A simple step-by-step filter inductor design procedure is given. Values of K_g for common ferrite core shapes are tabulated in Appendix D.

Extension of the K_g method to multiple-winding elements is covered in Section 14.3. In applications requiring multiple windings, it is necessary to optimize the wire sizes of the windings so that the overall copper loss is minimized. It is also necessary to write an equation that relates the peak flux density to the applied waveforms or to the desired winding inductance. Again, a simple step-by-step transformer design approach is given.

The goal of the K_g approach of this chapter is the design of a magnetic device having a given copper loss. Core loss is not specifically addressed in the K_g approach, and B_{max} is a given fixed value. In the next chapter, the flux density is treated as a design variable to be optimized. This allows the overall loss (i.e., core loss plus copper loss) to be minimized.

14.1 FILTER INDUCTOR DESIGN CONSTRAINTS

A filter inductor employed in a CCM buck converter is illustrated in Fig. 14.1(a). In this application, the value of inductance L is usually chosen such that the inductor current ripple peak magnitude Δi is a small fraction of the full-load inductor current dc component I, as illustrated in Fig. 14.1(b). As illustrated in Fig. 14.2, an air gap is employed that is sufficiently large to prevent saturation of the core by the peak

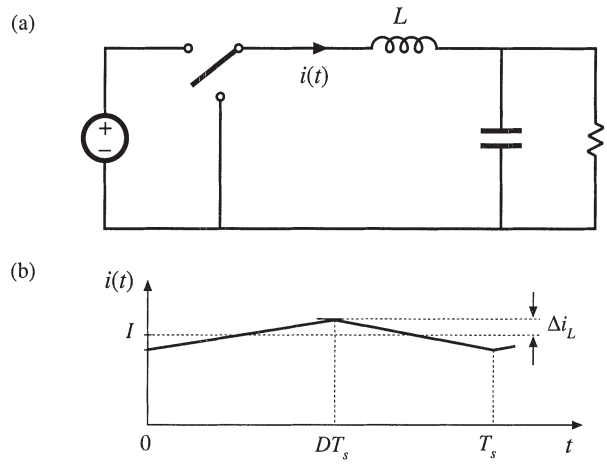


Fig. 14.1 Filter inductor employed in a CCM buck converter: (a) circuit schematic, (b) inductor current waveform.

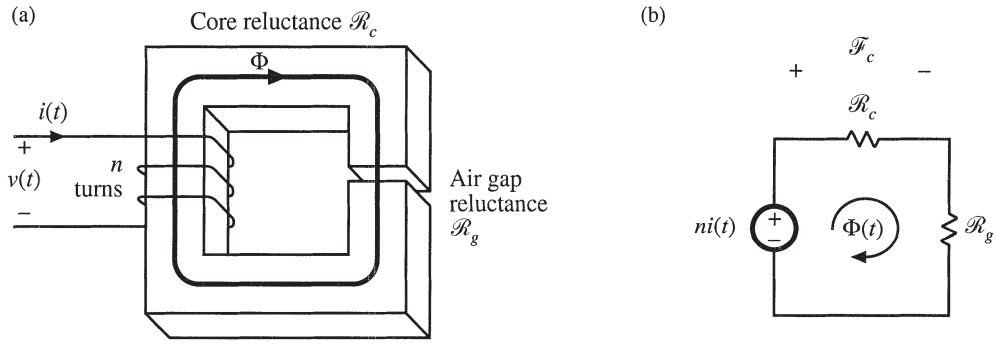


Fig. 14.2 Filter inductor: (a) structure, (b) magnetic circuit model.

current $I + \Delta i$.

Let us consider the design of the filter inductor illustrated in Figs. 14.1 and 14.2. It is assumed that the core and proximity losses are negligible, so that the inductor losses are dominated by the low-frequency copper losses. The inductor can therefore be modeled by the equivalent circuit of Fig. 14.3, in which R represents the dc resistance of the winding. It is desired to obtain a given inductance L and given winding resistance R. The inductor should not saturate when a given worst-case peak current I_{max} is applied. Note that specification of R is equivalent to specification of the copper loss P_{cu}, since

$$P_{cu} = I_{rms}^2 R \tag{14.1}$$

The influence of inductor winding resistance on converter efficiency and output voltage is modeled in Chapter 3.

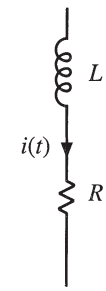


Fig. 14.3 Filter inductor equivalent circuit.

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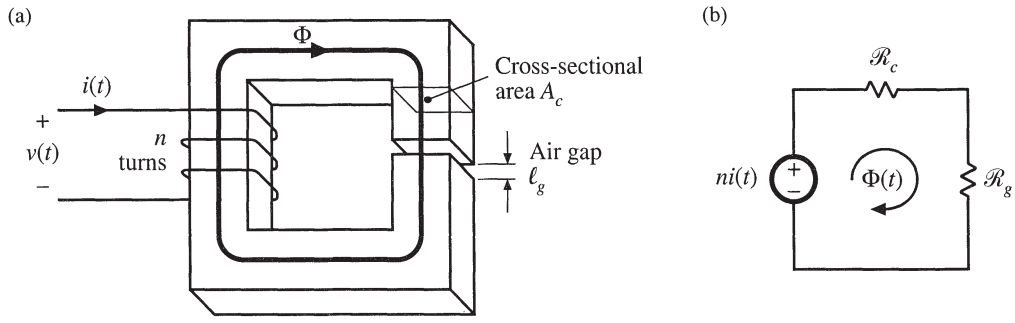


Fig. 14.4 Filter inductor: (a) assumed geometry, (b) magnetic circuit.

It is assumed that the inductor geometry is topologically equivalent to Fig. 14.4(a). An equivalent magnetic circuit is illustrated in Fig. 14.4(b). The core reluctance $\mathcal{R}_c$ and air gap reluctance $\mathcal{R}_g$ are

$$\mathcal{R}_c = \frac{\ell_c}{\mu_c A_c} \qquad \mathcal{R}_g = \frac{\ell_g}{\mu_0 A_c} \tag{14.2}$$

where ℓ_c is the core magnetic path length, A_c is the core cross-sectional area, μ_c is the core permeability, and ℓ_g is the air gap length. It is assumed that the core and air gap have the same cross-sectional areas. Solution of Fig. 14.4(b) yields

$$ni = \Phi\left(\mathcal{R}_c + \mathcal{R}_g\right) \tag{14.3}$$

Usually, $\mathcal{R}_c \ll \mathcal{R}_g$, and hence Eq. (14.3) can be approximated as

$$ni \approx \Phi \mathcal{R}_g \tag{14.4}$$

The air gap dominates the inductor properties. Four design constraints now can be identified.

14.1.1 Maximum Flux Density

Given a peak winding current I_{max}, it is desired to operate the core flux density at a maximum value B_{max}. The value of B_{max} is chosen to be less than the worst-case saturation flux density B_{sat} of the core material.

Substitution of $\Phi = BA_c$ into Eq. (14.4) leads to

$$ni = BA_c \mathcal{R}_g \tag{14.5}$$

Upon letting $I = I_{max}$ and $B = B_{max}$, we obtain

$$nI_{max} = B_{max} A_c \mathcal{R}_g = B_{max} \frac{\ell_g}{\mu_0} \tag{14.6}$$

This is the first design constraint. The turns ratio n and the air gap length ℓ_g are unknowns.

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14.1.2 Inductance

The given inductance value L must be obtained. The inductance is equal to

$$L = \frac{n^2}{\mathcal{R}_g} = \frac{\mu_0 A_c n^2}{\ell_g} \tag{14.7}$$

This is the second design constraint. The turns ratio n, core area A_c, and gap length ℓ_g are unknown.

14.1.3 Winding Area

As illustrated in Fig. 14.5, the winding must fit through the window, i.e., the hole in the center of the core. The cross-sectional area of the conductor, or bare area, is A_W If the winding has n turns, then the area of copper conductor in the window is

$$nA_W \tag{14.8}$$

If the core has window area W_A, then we can express the area available for the winding conductors as

$$K_u W_A \tag{14.9}$$

where K_u is the *window utilization factor*, or *fill factor*. Hence, the third design constraint can be expressed as

$$K_u W_A \geq nA_W \tag{14.10}$$

The fill factor K_u is the fraction of the core window area that is filled with copper. K_u must lie between zero and one. As discussed in [1], there are several mechanism that cause K_u to be less than unity. Round wire does not pack perfectly; this reduces K_u by a factor of 0.7 to 0.55, depending on the winding technique. The wire has insulation; the ratio of wire conductor area to total wire area varies from approximately 0.95 to 0.65, depending on the wire size and type of insulation. The bobbin uses some of the window area. Insulation may be required between windings and/or winding layers. Typical values of K_u for cores with winding bobbins are: 0.5 for a simple low-voltage inductor, 0.25 to 0.3 for an off-line transformer, 0.05 to 0.2 for a high-voltage transformer supplying several kV, and 0.65 for a low-voltage foil transformer or inductor.

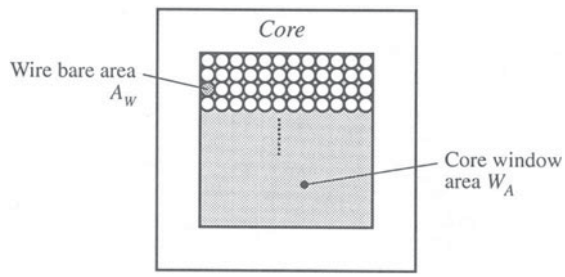


Fig. 14.5 The winding must fit in the core window area.

14.1.4 Winding Resistance

The resistance of the winding is

$$R = \rho \frac{\ell_b}{A_W} \tag{14.11}$$

where ρ is the resistivity of the conductor material, ℓ_b is the length of the wire, and A_W is the wire bare area. The resistivity of copper at room temperature is $1.724 \cdot 10^{-6}$ Ω–cm. The length of the wire comprising an n-turn winding can be expressed as

$$\ell_b = n(MLT) \tag{14.12}$$

where (MLT) is the mean-length-per-turn of the winding. The mean-length-per-turn is a function of the core geometry. Substitution of Eq. (14.12) into (14.11) leads to

$$R = \rho \frac{n(MLT)}{A_W} \tag{14.13}$$

This is the fourth constraint.

14.1.5 The Core Geometrical Constant K_g

The four constraints, Eqs. (14.6), (14.7), (14.10), and (14.13), involve the quantities A_c, W_A, and MLT, which are functions of the core geometry, the quantities I_{max}, B_{max}, μ_0, L, K_u, R, and ρ, which are given specifications or other known quantities, and n, ℓ_g, and A_W, which are unknowns. Elimination of the unknowns n, ℓ_g, and A_W leads to the following equation:

$$\frac{A_c^2 W_A}{(MLT)} \geq \frac{\rho L^2 I_{max}^2}{B_{max}^2 R K_u} \tag{14.14}$$

The quantities on the right side of this equation are specifications or other known quantities. The left side of the equation is a function of the core geometry alone. It is necessary to choose a core whose geometry satisfies Eq. (14.14).

The quantity

$$K_g = \frac{A_c^2 W_A}{(MLT)} \tag{14.15}$$

is called the core geometrical constant. It is a figure-of-merit that describes the effective electrical size of magnetic cores, in applications where copper loss and maximum flux density are specified. Tables are included in Appendix D that list the values of K_g for several standard families of ferrite cores. K_g has dimensions of length to the fifth power.

Equation (14.14) reveals how the specifications affect the core size. Increasing the inductance or peak current requires an increase in core size. Increasing the peak flux density allows a decrease in core size, and hence it is advantageous to use a core material that exhibits a high saturation flux density. Allowing a larger winding resistance R, and hence larger copper loss, leads to a smaller core. Of course,

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the increased copper loss and smaller core size will lead to a higher temperature rise, which may be unacceptable. The fill factor K_u also influences the core size.

Equation (14.15) reveals how core geometry affects the core capabilities. An inductor capable of meeting increased electrical requirements can be obtained by increasing either the core area A_c, or the window area W_A. Increase of the core area requires additional iron core material. Increase of the window area implies that additional copper winding material is employed. We can trade iron for copper, or vice versa, by changing the core geometry in a way that maintains the K_g of Eq. (14.15).

14.2 A STEP-BY-STEP PROCEDURE

The procedure developed in Section 14.1 is summarized below. This simple filter inductor design procedure should be regarded as a first-pass approach. Numerous issues have been neglected, including detailed insulation requirements, conductor eddy current losses, temperature rise, roundoff of number of turns, etc.

The following quantities are specified, using the units noted:

Wire resistivity	ρ	(Ω–cm)
Peak winding current	I_{max}	(A)
Inductance	L	(H)
Winding resistance	R	(Ω)
Winding fill factor	K_u	
Maximum operating flux density	B_{max}	(T)

The core dimensions are expressed in cm:

Core cross-sectional area	A_c	(cm^2)
Core window area	W_A	(cm^2)
Mean length per turn	MLT	(cm)

The use of centimeters rather than meters requires that appropriate factors be added to the design equations.

1. *Determine core size*

$$K_g \geq \frac{\rho L^2 I_{max}^2}{B_{max}^2 R K_u} 10^8 \quad (cm^5) \tag{14.16}$$

Choose a core which is large enough to satisfy this inequality. Note the values of A_c, W_A, and MLT for this core. The resistivity ρ of copper wire is $1.724 \cdot 10^{-6}$ Ω–cm at room temperature, and $2.3 \cdot 10^{-6}$ Ω–cm at 100°C.

2. *Determine air gap length*

$$\ell_g = \frac{\mu_0 L I_{max}^2}{B_{max}^2 A_c} 10^4 \quad (m) \tag{14.17}$$

with A_c expressed in cm^2. $\mu_0 = 4\pi \cdot 10^{-7}$ H/m. The air gap length is given in meters. The value expressed in Eq. (14.17) is approximate, and neglects fringing flux and other nonidealities.

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Core manufacturers sell gapped cores. Rather than specifying the air gap length, the equivalent quantity A_L is used. A_L is equal to the inductance, in mH, obtained with a winding of 1000 turns. When A_L is specified, it is the core manufacturer's responsibility to obtain the correct gap length. Equation (14.17) can be modified to yield the required A_L, as follows:

$$A_L = \frac{10 B_{max}^2 A_c^2}{L I_{max}^2} \quad \text{(mH/1000 turns)} \tag{14.18}$$

where A_c is given in cm^2, L is given in Henries, and B_{max} is given in Tesla.

3. *Determine number of turns*

$$n = \frac{L I_{max}}{B_{max} A_c} \, 10^4 \tag{14.19}$$

4. *Evaluate wire size*

$$A_W \le \frac{K_u W_A}{n} \quad (\text{cm}^2) \tag{14.20}$$

Select wire with bare copper area less than or equal to this value. An American Wire Gauge table is included in Appendix D.

As a check, the winding resistance can be computed:

$$R = \frac{\rho n (MLT)}{A_w} \quad (\Omega) \tag{14.21}$$

14.3 MULTIPLE-WINDING MAGNETICS DESIGN VIA THE K_g METHOD

The K_g method can be extended to the case of multiple-winding magnetics, such as the transformers and coupled inductors described in Sections 13.5.3 to 13.5.5. The desired turns ratios, as well as the desired winding voltage and current waveforms, are specified. In the case of a coupled inductor or flyback transformer, the magnetizing inductance is also specified. It is desired to select a core size, number of turns for each winding, and wire sizes. It is also assumed that the maximum flux density B_{max} is given.

With the K_g method, a desired copper loss is attained. In the multiple-winding case, each winding contributes some copper loss, and it is necessary to allocate the available window area among the various windings. In Section 14.3.1 below, it is found that total copper loss is minimized if the window area is divided between the windings according to their apparent powers. This result is employed in the following sections, in which an optimized K_g method for coupled inductor design is developed.

14.3.1 Window Area Allocation

The first issue to settle in design of a multiple-winding magnetic device is the allocation of the window area A_W among the various windings. It is desired to design a device having k windings with turns ratios $n_1 : n_2 : ... : n_k$. These windings must conduct rms currents $I_1, I_2, ..., I_k$ respectively. It should be noted that the windings are effectively in parallel: the winding voltages are ideally related by the turns ratios

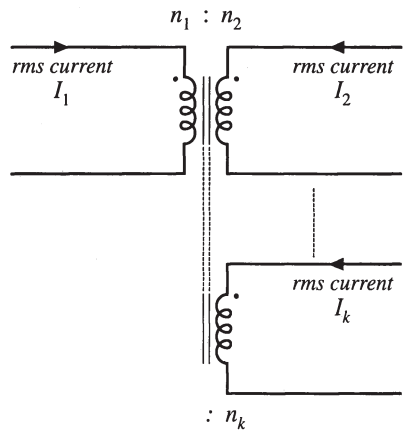


Fig. 14.6 It is desired to optimally allocate the window area of a k–winding magnetic element to minimize low-frequency copper losses, with given rms winding currents and turns ratios.

$$\frac{v_1(t)}{n_1} = \frac{v_2(t)}{n_2} = \cdots = \frac{v_k(t)}{n_k} \tag{14.22}$$

However, the winding rms currents are determined by the loads, and in general are not related to the turns ratios. The device is represented schematically in Fig. 14.6.

The relevant geometrical parameters are summarized in Fig. 14.7(a). It is necessary to allocate a portion of the total window area W_A to each winding, as illustrated in Fig. 14.7(b). Let α_j be the fraction of the window area allocated to winding j, where

$$\begin{aligned} &0 < \alpha_j < 1 \\ &\alpha_1 + \alpha_2 + \cdots + \alpha_k = 1 \end{aligned} \tag{14.23}$$

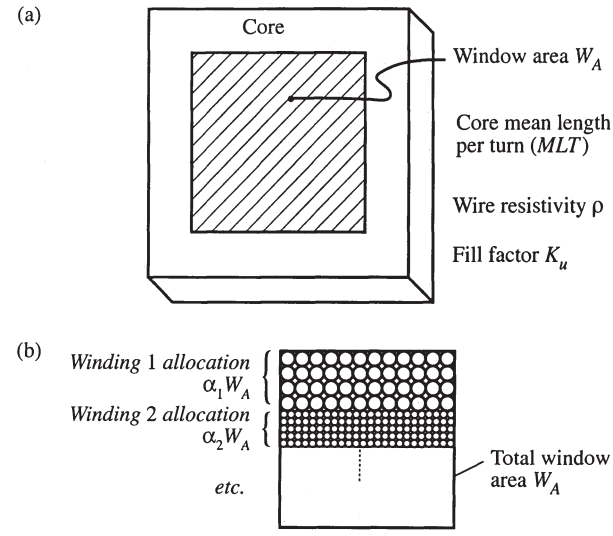


Fig. 14.7 Basic core topology, including window area W_A enclosed by core (a). The window is allocated to the various windings to minimize low-frequency copper loss (b).

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The low-frequency copper loss $P_{cu,j}$ in winding j depends on the dc resistance R_j of winding j, as follows:

$$P_{cu,j} = I_j^2 R_j \tag{14.24}$$

The resistance of winding j is

$$R_j = \rho \frac{\ell_j}{A_{W,j}} \tag{14.25}$$

where ρ is the wire resistivity, ℓ_j is the length of the wire used for winding j, and $A_{W,j}$ is the cross-sectional area of the wire used for winding j. These quantities can be expressed as

$$\ell_j = n_j (MLT) \tag{14.26}$$

$$A_{W,j} = \frac{W_A K_u \alpha_j}{n_j} \tag{14.27}$$

where (MLT) is the winding mean-length-per-turn, and K_u is the winding fill factor. Substitution of these expressions into Eq. (14.25) leads to

$$R_j = \rho \frac{n_j^2 (MLT)}{W_A K_u \alpha_j} \tag{14.28}$$

The copper loss of winding j is therefore

$$P_{cu,j} = \frac{n_j^2 i_j^2 \rho (MLT)}{W_A K_u \alpha_j} \tag{14.29}$$

The total copper loss of the k windings is

$$P_{cu,tot} = P_{cu,1} + P_{cu,2} + \cdots + P_{cu,k} = \frac{\rho (MLT)}{W_A K_u} \sum_{j=1}^{k} \left(\frac{n_j^2 I_j^2}{\alpha_j} \right) \tag{14.30}$$

It is desired to choose the α_js such that the total copper loss $P_{cu,tot}$ is minimized. Let us consider what happens when we vary one of the αs, say α_1, between 0 and 1.

When $\alpha_1 = 0$, then we allocate zero area to winding 1. In consequence, the resistance of winding 1 tends to infinity. The copper loss of winding 1 also tends to infinity. On the other hand, the other windings are given maximum area, and hence their copper losses can be reduced. Nonetheless, the total copper loss tends to infinity.

When $\alpha_1 = 1$, then we allocate all of the window area to winding 1, and none to the other windings. Hence, the resistance of winding 1, as well as its low-frequency copper loss, are minimized. But the copper losses of the remaining windings tend to infinity.

As illustrated in Fig. 14.8, there must be an optimum value of α_1 that lies between these two extremes, where the total copper loss is minimized. Let us compute the optimum values of α_1, α_2, ..., α_k using the method of Lagrange multipliers. It is desired to minimize Eq. (14.30), subject to the constraint of Eq. (14.23). Hence, we define the function

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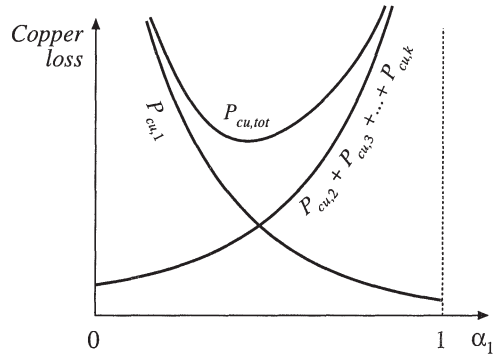


Fig. 14.8 Variation of copper losses with α_1.

$$f(\alpha_1, \alpha_2, \cdots, \alpha_k, \xi) = P_{cu,tot}(\alpha_1, \alpha_2, \cdots, \alpha_k) + \xi\, g(\alpha_1, \alpha_2, \cdots, \alpha_k) \tag{14.31}$$

where

$$g(\alpha_1, \alpha_2, \cdots, \alpha_k) = 1 - \sum_{j=1}^{k} \alpha_j \tag{14.32}$$

is the constraint that must equal zero, and ξ is the Lagrange multiplier. The optimum point is the solution of the system of equations

$$\begin{aligned}
&\frac{\partial f(\alpha_1, \alpha_2, \cdots, \alpha_k, \xi)}{\partial \alpha_1} = 0 \\
&\frac{\partial f(\alpha_1, \alpha_2, \cdots, \alpha_k, \xi)}{\partial \alpha_2} = 0 \\
&\qquad\vdots \\
&\frac{\partial f(\alpha_1, \alpha_2, \cdots, \alpha_k, \xi)}{\partial \alpha_k} = 0 \\
&\frac{\partial f(\alpha_1, \alpha_2, \cdots, \alpha_k, \xi)}{\partial \xi} = 0
\end{aligned} \tag{14.33}$$

The solution is

$$\xi = \frac{\rho(MLT)}{W_A K_u}\left(\sum_{j=1}^{k} n_j I_j\right)^2 = P_{cu,tot} \tag{14.34}$$

$$\alpha_m = \frac{n_m I_m}{\sum_{j=1}^{k} n_j I_j} \tag{14.35}$$

This is the optimal choice for the αs, and the resulting minimum value of $P_{cu,tot}$.

According to Eq. (14.22), the winding voltages are proportional to the turns ratios. Hence, we can express the α_ms in the alternate form

$$\alpha_m = \frac{V_m I_m}{\sum_{j=1}^{k} V_j I_j} \tag{14.36}$$

by multiplying and dividing Eq. (14.35) by the quantity V_m/n_m. It is irrelevant whether rms or peak voltages are used. Equation (14.36) is the desired result. It states that the window area should be allocated to the various windings in proportion to their apparent powers. The numerator of Eq. (14.36) is the apparent power of winding m, equal to the product of the rms current and the voltage. The denominator is the sum of the apparent powers of all windings.

As an example, consider the PWM full-bridge transformer having a center-tapped secondary, as illustrated in Fig. 14.9. This can be viewed as a three-winding transformer, having a single primary-side winding of n_1 turns, and two secondary-side windings, each of n_2 turns. The winding current waveforms $i_1(t)$, $i_2(t)$, and $i_3(t)$ are illustrated in Fig. 14.10. Their rms values are

$$I_1 = \sqrt{\frac{1}{2T_s}\int_0^{2T_s} i_1^2(t)dt} = \frac{n_2}{n_1} I\sqrt{D} \tag{14.37}$$

$$I_2 = I_3 = \sqrt{\frac{1}{2T_s}\int_0^{2T_s} i_2^2(t)dt} = \frac{1}{2} I\sqrt{1+D} \tag{14.38}$$

Substitution of these expressions into Eq. (14.35) yields

$$\alpha_1 = \frac{1}{\left(1+\sqrt{\frac{1+D}{D}}\right)} \tag{14.39}$$

$$\alpha_2 = \alpha_3 = \frac{1}{2}\frac{1}{\left(1+\sqrt{\frac{D}{1+D}}\right)} \tag{14.40}$$

If the design is to be optimized at the operating point $D = 0.75$, then one obtains

$$\begin{aligned} \alpha_1 &= 0.396 \\ \alpha_2 &= 0.302 \\ \alpha_3 &= 0.302 \end{aligned} \tag{14.41}$$

So approximately 40% of the window area should be allocated to the primary winding, and 30% should

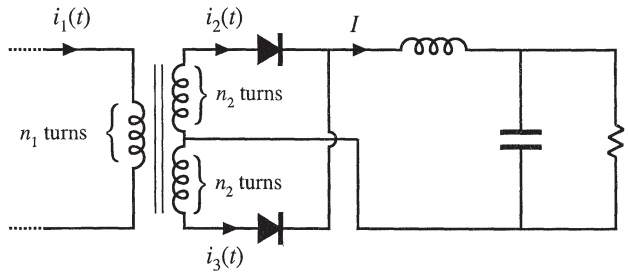


Fig. 14.9 PWM full-bridge transformer example.

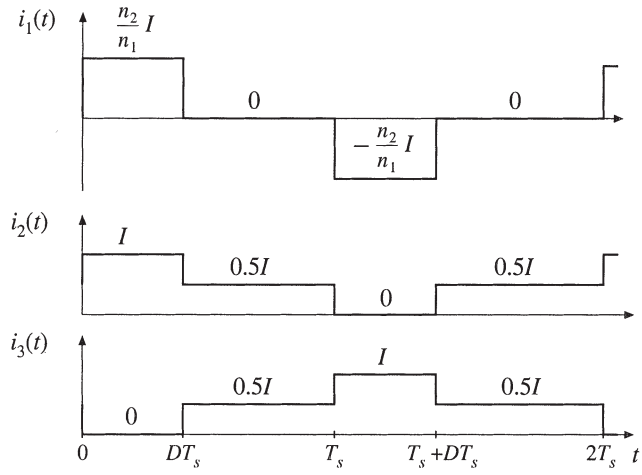


Fig. 14.10 Transformer waveforms, PWM full-bridge converter example.

be allocated to each half of the center-tapped secondary. The total copper loss at this optimal design point is found from evaluation of Eq. (14.34):

$$\begin{aligned} P_{cu,tot} &= \frac{\rho(MLT)}{W_A K_u}\left(\sum_{j=1}^{3} n_j I_j\right)^2 \\ &= \frac{\rho(MLT) n_2^2 I^2}{W_A K_u}\left(1 + 2D + 2\sqrt{D(1+D)}\right) \end{aligned} \tag{14.42}$$

14.3.2 Coupled Inductor Design Constraints

Let us now consider how to design a k-winding coupled inductor, as discussed in Section 13.5.4 and illustrated in Fig. 14.11. It is desired that the magnetizing inductance be a specified value L_M, referred to winding 1. It is also desired that the numbers of turns for the other windings be chosen according to desired turns ratios. When the magnetizing current $i_M(t)$ reaches its maximum value $I_{M,max}$, the coupled inductor should operate with a given maximum flux density B_{max}. With rms currents $I_1, I_2, \ldots, I_k$ applied to the respective windings, the total copper loss should be a desired value P_{cu} given by Eq. (14.34). Hence, the design procedure involves selecting the core size and number of primary turns so that the desired magnetizing inductance, the desired flux density, and the desired total copper loss are achieved. Other quantities, such as air gap length, secondary turns, and wire sizes, can then be selected. The derivation follows the derivation for the single winding case (Section 14.1), and incorporates the window area optimization of Section 14.3.1.

The magnetizing current $i_M(t)$ can be expressed in terms of the winding currents $i_1(t)$, $i_2(t)$,..., $i_k(t)$ by solution of Fig. 14.11(a) (or by use of Ampere's Law), as follows:

$$i_M(t) = i_1(t) + \frac{n_2}{n_1} i_2(t) + \cdots + \frac{n_k}{n_1} i_k(t) \tag{14.43}$$

By solution of the magnetic circuit model of Fig. 14.11(b), we can write

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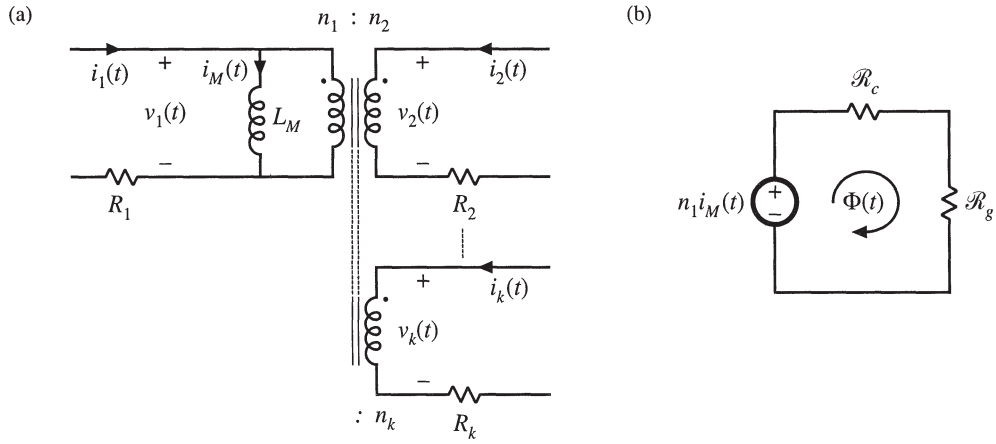


Fig. 14.11 A k-winding magnetic device, with specified turns ratios and waveforms: (a) electrical circuit model, (b) a magnetic circuit model.

$$n_1 i_M(t) = B(t) A_c \mathcal{R}_g \tag{14.44}$$

This equation is analogous to Eq. (14.4), and assumes that the reluctance $\mathcal{R}_g$ of the air gap is much larger than the reluctance $\mathcal{R}_c$ of the core. As usual, the total flux $\Phi(t)$ is equal to $B(t)A_c$. Leakage inductances are ignored.

To avoid saturation of the core, the instantaneous flux density $B(t)$ must be less than the saturation flux density of the core material, B_{sat}. Let us define $I_{M,max}$ as the maximum value of the magnetizing current $i_M(t)$. According to Eq. (14.44), this will lead to a maximum flux density B_{max} given by

$$n_1 I_{M,max} = B_{max} A_c \mathcal{R}_g = B_{max} \frac{\ell_g}{\mu_0} \tag{14.45}$$

For a value of $I_{M,max}$ given by the circuit application, we should use Eq. (14.45) to choose the turns n_1 and gap length ℓ_g such that the maximum flux density B_{max} is less than the saturation density B_{sat}. Equation (14.45) is similar to Eq. (14.6), but accounts for the magnetizations produced by multiple winding currents.

The magnetizing inductance L_M, referred to winding 1, is equal to

$$L_M = \frac{n_1^2}{\mathcal{R}_g} = n_1^2 \frac{\mu_0 A_c}{\ell_g} \tag{14.46}$$

This equation is analogous to Eq. (14.7).

As shown in Section 14.3.1, the total copper loss is minimized when the core window area W_A is allocated to the various windings according to Eq. (14.35) or (14.36). The total copper loss is then given by Eq. (14.34). Equation (14.34) can be expressed in the form

$$P_{cu} = \frac{\rho (MLT) n_1^2 I_{tot}^2}{W_A K_u} \tag{14.47}$$

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where

$$I_{tot} = \sum_{j=1}^{k} \frac{n_j}{n_1} I_j \tag{14.48}$$

is the sum of the rms winding currents, referred to winding 1.

We can now eliminate the unknown quantities ℓ_g and n_1 from Eqs. (14.45), (14.46), and (14.47). Equation (14.47) then becomes

$$P_{cu} = \frac{\rho (MLT) L_M^2 I_{tot}^2 I_{M,max}^2}{B_{max}^2 A_c^2 W_A K_u} \tag{14.49}$$

We can now rearrange this equation, by grouping terms that involve the core geometry on the left-hand side, and specifications on the right-hand side:

$$\frac{A_c^2 W_A}{(MLT)} = \frac{\rho L_M^2 I_{tot}^2 I_{M,max}^2}{B_{max}^2 K_u P_{cu}} \tag{14.50}$$

The left-hand side of the equation can be recognized as the same K_g term defined in Eq. (14.15). Therefore, to design a coupled inductor that meets the requirements of operating with a given maximum flux density B_{max}, given primary magnetizing inductance L_M, and with a given total copper loss P_{cu}, we must select a core that satisfies

$$K_g \geq \frac{\rho L_M^2 I_{tot}^2 I_{M,max}^2}{B_{max}^2 K_u P_{cu}} \tag{14.51}$$

Once such a core is found, then the winding 1 turns and gap length can be selected to satisfy Eqs. (14.45) and (14.46). The turns of windings 2 through k are selected according to the desired turns ratios. The window area is allocated among the windings according to Eq. (14.35), and the wire gauges are chosen using Eq. (14.27).

The procedure above is applicable to design of coupled inductors. The results are applicable to design of flyback and SEPIC transformers as well, although it should be noted that the procedure does not account for the effects of core or proximity loss. It also can be extended to design of other devices, such as conventional transformers—doing so is left as a homework problem.

14.3.3 Design Procedure

The following quantities are specified, using the units noted:

Wire effective resistivity	ρ	(Ω–cm)
Total rms winding currents, referred to winding 1	$I_{tot} = \sum_{j=1}^{k} \frac{n_j}{n_i} I_j$	(A)
Peak magnetizing current, referred to winding 1	$I_{M,max}$	(A)
Desired turns ratios	n_2/n_1, n_3/n_1, etc.	

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Magnetizing inductance, referred to winding 1	L_M	(H)
Allowed total copper loss	P_{cu}	(W)
Winding fill factor	K_u	
Maximum operating flux density	B_{max}	(T)

The core dimensions are expressed in cm:

Core cross-sectional area	A_c	(cm^2)
Core window area	W_A	(cm^2)
Mean length per turn	MLT	(cm)

The use of centimeters rather than meters requires that appropriate factors be added to the design equations.

1. *Determine core size*

$$K_g \geq \frac{\rho L_M^2 I_{tot}^2 I_{M,max}^2}{B_{max}^2 P_{cu} K_u} 10^8 \qquad (cm^5) \tag{14.52}$$

Choose a core which is large enough to satisfy this inequality. Note the values of A_c, W_A, and MLT for this core. The resistivity ρ of copper wire is $1.724 \cdot 10^{-6}$ Ω–cm at room temperature, and $2.3 \cdot 10^{-6}$ Ω–cm at 100°C.

2. *Determine air gap length*

$$\ell_g = \frac{\mu_0 L_M I_{M,max}^2}{B_{max}^2 A_c} 10^4 \qquad (m) \tag{14.53}$$

Here, B_{max} is expressed in Tesla, A_c is expressed in cm^2, and ℓ_g is expressed in meters. The permeability of free space is $\mu_0 = 4\pi \cdot 10^{-7}$ H/m. This value is approximate, and neglects fringing flux and other non-idealities.

3. *Determine number of winding 1 turns*

$$n_1 = \frac{L_M I_{M,max}}{B_{max} A_c} 10^4 \tag{14.54}$$

Here, B_{max} is expressed in Tesla and A_c is expressed in cm^2.

4. *Determine number of secondary turns*

   Use the desired turns ratios:

$$\begin{aligned} n_2 &= \left(\frac{n_2}{n_1}\right) n_1 \\ n_3 &= \left(\frac{n_3}{n_1}\right) n_1 \\ &\vdots \end{aligned} \tag{14.55}$$

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5. *Evaluate fraction of window area allocated to each winding*

$$\begin{aligned} \alpha_1 &= \frac{n_1 I_1}{n_1 I_{tot}} \\ \alpha_2 &= \frac{n_2 I_2}{n_1 I_{tot}} \\ &\vdots \\ \alpha_k &= \frac{n_k I_k}{n_1 I_{tot}} \end{aligned} \tag{14.56}$$

6. *Evaluate wire sizes*

$$\begin{aligned} A_{w1} &\le \frac{\alpha_1 K_u W_A}{n_1} \\ A_{w2} &\le \frac{\alpha_2 K_u W_A}{n_2} \\ &\vdots \end{aligned} \tag{14.57}$$

Select wire with bare copper area less than or equal to these values. An American Wire Gauge table is included in Appendix D.

14.4 EXAMPLES

14.4.1 Coupled Inductor for a Two-Output Forward Converter

As a first example, let us consider the design of coupled inductors for the two-output forward converter illustrated in Fig. 14.12. This element can be viewed as two filter inductors that are wound on the same core. The turns ratio is chosen to be the same as the ratio of the output voltages. The magnetizing inductance performs the function of filtering the switching harmonics for both outputs, and the magnetizing current is equal to the sum of the reflected winding currents.

At the nominal full-load operating point, the converter operates in the continuous conduction mode with a duty cycle of $D = 0.35$. The switching frequency is 200 kHz. At this operating point, it is desired that the ripple in the magnetizing current have a peak magnitude equal to 20% of the dc component of magnetizing current.

The dc component of the magnetizing current I_M is

$$\begin{aligned} I_M &= I_1 + \frac{n_2}{n_1} I_2 \\ &= (4\text{ A}) + \frac{12}{28}(2\text{ A}) \\ &= 4.86\text{ A} \end{aligned} \tag{14.58}$$

The magnetizing current ripple Δi_M can be expressed as

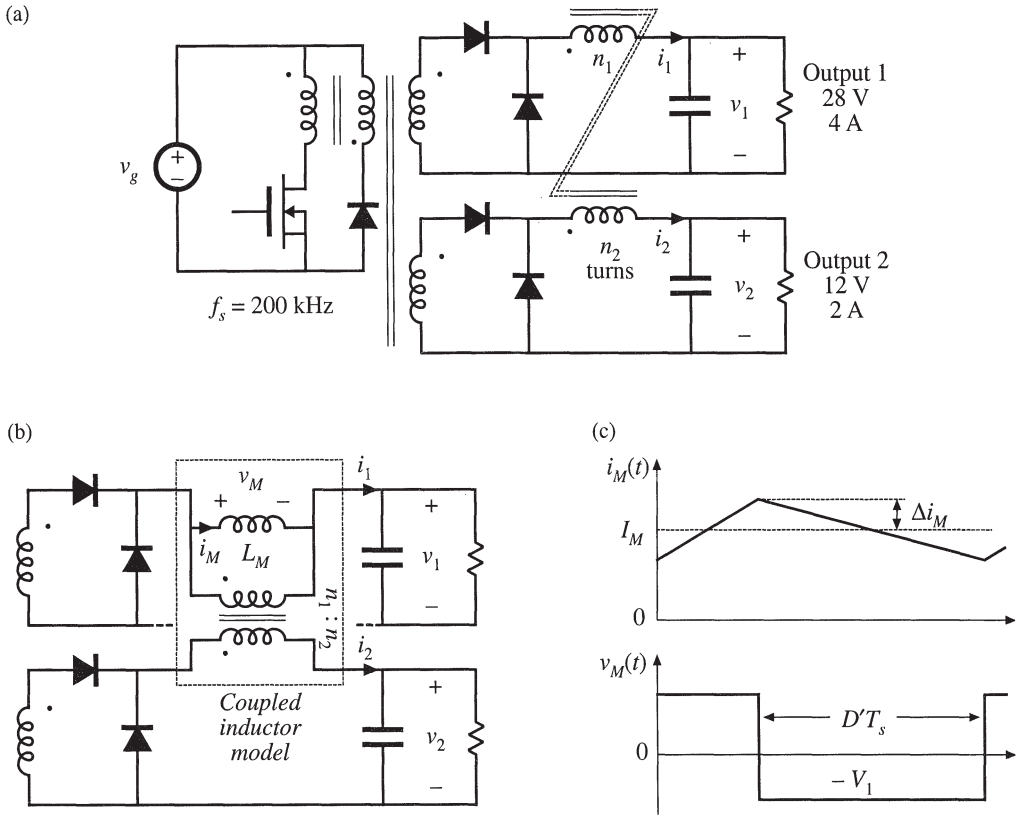


Fig. 14.12 Two-output forward converter example: (a) circuit schematic, (b) coupled inductor model inserted into converter secondary-side circuit, (c) magnetizing current and voltage waveforms of coupled inductor, referred to winding 1.

$$\Delta i_M = \frac{V_1 D' T_s}{2L_M} \tag{14.59}$$

Since we want Δi_M to be equal to 20% of I_M, we should choose L_M as follows:

$$\begin{aligned} L_M &= \frac{V_1 D' T_s}{2\Delta i_M} \\ &= \frac{(28\text{ V})(1 - 0.35)(5\ \mu\text{s})}{2(4.86\text{ A})(20\%)} \\ &= 47\ \mu\text{H} \end{aligned} \tag{14.60}$$

The peak magnetizing current, referred to winding 1, is therefore

$$I_{M,max} = I_M + \Delta i_M = 5.83\text{ A} \tag{14.61}$$

Since the current ripples of the winding currents are small compared to the respective dc components, the

rms values of the winding currents are approximately equal to the dc components: $I_1 = 4$ A, $I_2 = 2$ A. Therefore, the sum of the rms winding currents, referred to winding 1, is

$$I_{tot} = I_1 + \frac{n_2}{n_1} I_2 = 4.86 \text{ A} \tag{14.62}$$

For this design, it is decided to allow 0.75 W of copper loss, and to operate the core at a maximum flux density of 0.25 Tesla. A fill factor of 0.4 is assumed. The required K_g is found by evaluation of Eq. (14.52), as follows:

$$\begin{aligned} K_g &\geq \frac{(1.724 \cdot 10^{-6}\ \Omega - \text{cm})(47\ \mu\text{H})^2(4.86\text{ A})^2(5.83\text{ A})^2}{(0.25\text{ T})^2(0.75\text{ W})(0.4)}\, 10^8 \\ &= 16 \cdot 10^{-3}\ \text{cm}^5 \end{aligned} \tag{14.63}$$

A ferrite PQ 20/16 core is selected, which has a K_g of $22.4 \cdot 10^{-3}$ cm^5. From Appendix D, the geometrical parameters for this core are: $A_c = 0.62$ cm^2, $W_A = 0.256$ cm^2, and $MLT = 4.4$ cm.

The air gap is found by evaluation of Eq. (14.53) as follows:

$$\begin{aligned} \ell_g &= \frac{\mu_0 L_M I_{M,max}^2}{B_{max}^2 A_c}\, 10^4 \\ &= \frac{(4\pi \cdot 10^{-7}\text{H/m})(47\ \mu\text{H})(5.83\text{ A})^2}{(0.25\text{ T})^2(0.62\text{ cm}^2)}\, 10^4 \\ &= 0.52\text{ mm} \end{aligned} \tag{14.64}$$

In practice, a slightly longer air gap would be necessary, to allow for the effects of fringing flux and other nonidealities. The winding 1 turns are found by evaluation of Eq. (14.54):

$$\begin{aligned} n_1 &= \frac{L_M I_{M,max}}{B_{max} A_c}\, 10^4 \\ &= \frac{(47\ \mu\text{H})(5.83\text{ A})}{(0.25\text{ T})(0.62\text{ cm}^2)}\, 10^4 \\ &= 17.6\text{ turns} \end{aligned} \tag{14.65}$$

The winding 2 turns are chosen according to the desired turns ratio:

$$\begin{aligned} n_2 &= \left(\frac{n_2}{n_1}\right) n_1 \\ &= \left(\frac{12}{28}\right)(17.6) \\ &= 7.54\text{ turns} \end{aligned} \tag{14.66}$$

The numbers of turns are rounded off to $n_1 = 17$ turns, $n_2 = 7$ turns (18:8 would be another possible choice). The window area W_A is allocated to the windings according to the fractions from Eq. (14.56):

$$\begin{aligned} \alpha_1 &= \frac{n_1 I_1}{n_1 I_{tot}} = \frac{(17)(4\text{ A})}{(17)(4.86\text{ A})} = 0.8235 \\ \alpha_2 &= \frac{n_2 I_2}{n_1 I_{tot}} = \frac{(7)(2\text{ A})}{(17)(4.86\text{ A})} = 0.1695 \end{aligned} \tag{14.67}$$

The wire sizes can therefore be chosen as follows:

$$A_{w1} \le \frac{\alpha_1 K_u W_A}{n_1} = \frac{(0.8235)(0.4)(0.256\,\text{cm}^2)}{(17)} = 4.96 \cdot 10^{-3}\,\text{cm}^2$$
$$\text{use AWG \#21}$$
$$A_{w2} \le \frac{\alpha_2 K_u W_A}{n_2} = \frac{(0.1695)(0.4)(0.256\,\text{cm}^2)}{(7)} = 2.48 \cdot 10^{-3}\,\text{cm}^2 \tag{14.68}$$
$$\text{use AWG \#24}$$

14.4.2 CCM Flyback Transformer

As a second example, let us design the flyback transformer for the converter illustrated in Fig. 14.13. This converter operates with an input voltage of 200 V, and produces an full-load output of 20 V at 5A. The switching frequency is 150 kHz. Under these operating conditions, it is desired that the converter operate in the continuous conduction mode, with a magnetizing current ripple equal to 20% of the dc component of magnetizing current. The duty cycle is chosen to be $D = 0.4$, and the turns ratio is $n_2/n_1 = 0.15$. A copper loss of 1.5 W is allowed, not including proximity effect losses. To allow room for isolation between the primary and secondary windings, a fill factor of $K_u = 0.3$ is assumed. A maximum flux density of $B_{max} = 0.25$ T is used; this value is less than the worst-case saturation flux density B_{sat} of the ferrite core material.

By solution of the converter using capacitor charge balance, the dc component of the magnetizing current can be found to be

$$I_M = \left(\frac{n_2}{n_1}\right)\frac{1}{D'}\frac{V}{R} = 1.25\text{ A} \tag{14.69}$$

Hence, the magnetizing current ripple should be

$$\Delta i_M = (20\%) I_M = 0.25\text{ A} \tag{14.70}$$

and the maximum value of the magnetizing current is

$$I_{M,max} = I_M + \Delta i_M = 1.5\text{ A} \tag{14.71}$$

To obtain this ripple, the magnetizing inductance should be

$$L_M = \frac{V_g D T_s}{2\Delta i_M} = 1.07\text{ mH} \tag{14.72}$$

The rms value of the primary winding current is found using Eq. (A.6) of Appendix A, as follows:

$$I_1 = I_M \sqrt{D}\sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_M}{I_M}\right)^2} = 0.796\text{ A} \tag{14.73}$$

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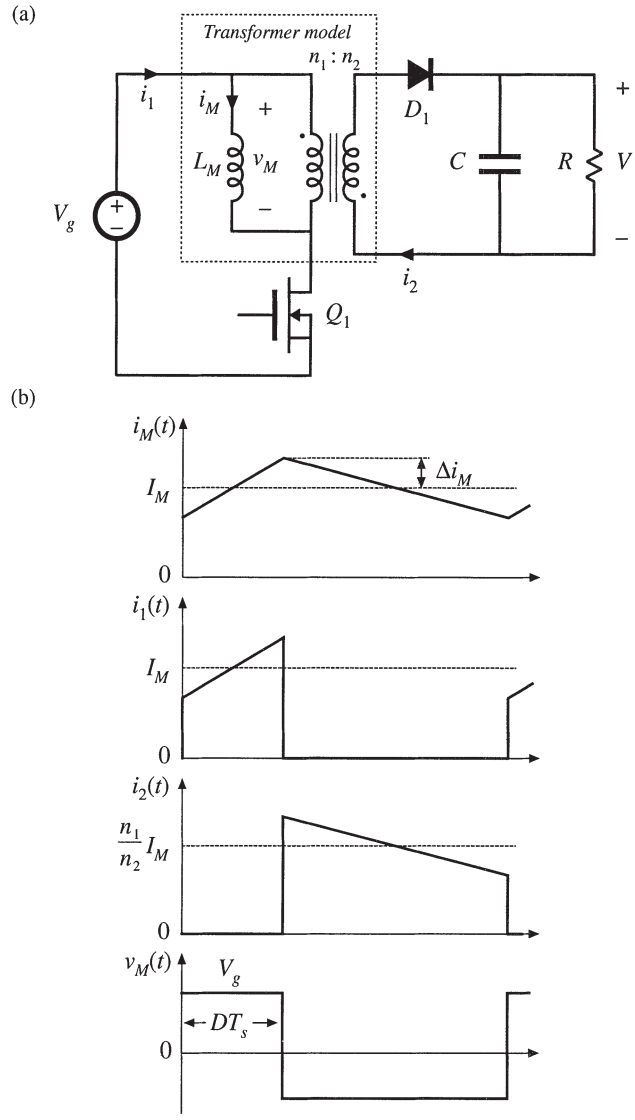


Fig. 14.13 Flyback transformer design example: (a) converter schematic, (b) typical waveforms.

The rms value of the secondary winding current is found in a similar manner:

$$I_2 = \frac{n_1}{n_2} I_M \sqrt{D'} \sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_M}{I_M}\right)^2} = 6.50 \text{ A} \tag{14.74}$$

Note that I_2 is not simply equal to the turns ratio multiplied by I_1. The total rms winding current is equal to:

$$I_{tot} = I_1 + \frac{n_2}{n_1} I_2 = 1.77 \text{ A} \tag{14.75}$$

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We can now determine the necessary core size. Evaluation of Eq. (14.52) yields

$$\begin{aligned} K_g &\geq \frac{\rho L_M^2 I_{tot}^2 I_{M,max}^2}{B_{max}^2 P_{cu} K_u} 10^8 \\ &= \frac{\left(1.724 \cdot 10^{-6}\Omega\text{-cm}\right)\left(1.07 \cdot 10^{-3}\text{ H}\right)^2\left(1.77\text{ A}\right)^2\left(1.5\text{ A}\right)^2}{\left(0.25\text{ T}\right)^2\left(1.5\text{ W}\right)\left(0.3\right)} 10^8 \\ &= 0.049\text{ cm}^5 \end{aligned} \tag{14.76}$$

The smallest EE core listed in Appendix D that satisfies this inequality is the EE30, which has $K_g = 0.0857\text{ cm}^5$. The dimensions of this core are

$$\begin{array}{ll} A_c & 1.09\text{ cm}^2 \\ W_A & 0.476\text{ cm}^2 \\ MLT & 6.6\text{ cm} \\ \ell_m & 5.77\text{ cm} \end{array} \tag{14.77}$$

The air gap length ℓ_g is chosen according to Eq. (14.53):

$$\begin{aligned} \ell_g &= \frac{\mu_0 L_M I_{M,max}^2}{B_{max}^2 A_c} 10^4 \\ &= \frac{\left(4\pi \cdot 10^{-7}\text{H/m}\right)\left(1.07 \cdot 10^{-3}\text{ H}\right)\left(1.5\text{ A}\right)^2}{\left(0.25\text{ T}\right)^2\left(1.09\text{ cm}^2\right)} 10^4 \\ &= 0.44\text{ mm} \end{aligned} \tag{14.78}$$

The number of winding 1 turns is chosen according to Eq. (14.54), as follows:

$$\begin{aligned} n_1 &= \frac{L_M I_{M,max}}{B_{max} A_c} 10^4 \\ &= \frac{\left(1.07 \cdot 10^{-3}\text{ H}\right)\left(1.5\text{ A}\right)}{\left(0.25\text{ T}\right)\left(1.09\text{ cm}^2\right)} 10^4 \\ &= 58.7\text{ turns} \end{aligned} \tag{14.79}$$

Since an integral number of turns is required, we round off this value to

$$n_1 = 59 \tag{14.80}$$

To obtain the desired turns ratio, n_2 should be chosen as follows:

$$\begin{aligned} n_2 &= \left(\frac{n_2}{n_1}\right) n_1 \\ &= \left(0.15\right) 59 \\ &= 8.81 \end{aligned} \tag{14.81}$$

We again round this value off, to

$$n_2 = 9 \tag{14.82}$$

The fractions of the window area allocated to windings 1 and 2 are selected in accordance with Eq. (14.56):

$$\begin{aligned} \alpha_1 &= \frac{I_1}{I_{tot}} = \frac{(0.796\ \text{A})}{(1.77\ \text{A})} = 0.45 \\ \alpha_2 &= \frac{n_2 I_2}{n_1 I_{tot}} = \frac{(9)(6.5\ \text{A})}{(59)(1.77\ \text{A})} = 0.55 \end{aligned} \tag{14.83}$$

The wire gauges should therefore be

$$\begin{aligned} A_{W1} &\le \frac{\alpha_1 K_u W_A}{n_1} = 1.09 \cdot 10^{-3}\ \text{cm}^2 \quad \text{— use \#28 AWG} \\ A_{W2} &\le \frac{\alpha_2 K_u W_A}{n_2} = 8.88 \cdot 10^{-3}\ \text{cm}^2 \quad \text{— use \#19 AWG} \end{aligned} \tag{14.84}$$

The above American Wire Gauges are selected using the wire gauge table given at the end of Appendix D.

The above design does not account for core loss or copper loss caused by the proximity effect. Let us compute the core loss for this design. Figure Fig. 14.14 contains a sketch of the *B–H* loop for this design. The flux density $B(t)$ can be expressed as a dc component (determined by the dc value of the magnetizing current I_M), plus an ac variation of peak amplitude ΔB that is determined by the current ripple Δi_M. The maximum value of $B(t)$ is labeled B_{max}; this value is determined by the sum of the dc component and the ac ripple component. The core material saturates when the applied $B(t)$ exceeds B_{sat}; hence, to avoid saturation, B_{max} should be less than B_{sat}. The core loss is determined by the amplitude of the ac variations in $B(t)$, i.e., by ΔB.

The ac component ΔB is determined using Faraday's law, as follows. Solution of Faraday's law for the derivative of $B(t)$ leads to

$$\frac{dB(t)}{dt} = \frac{v_M(t)}{n_1 A_c} \tag{14.85}$$

As illustrated in Fig. 14.15, the voltage applied during the first subinterval is $v_M(t) = V_g$. This causes the

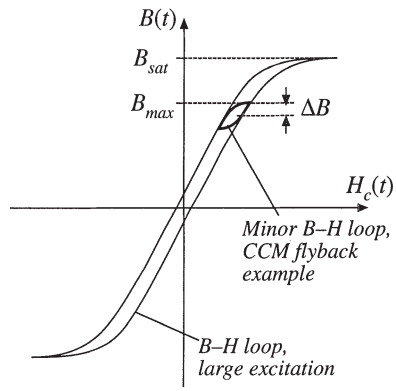


Fig. 14.14 *B–H* loop for the flyback transformer design example.

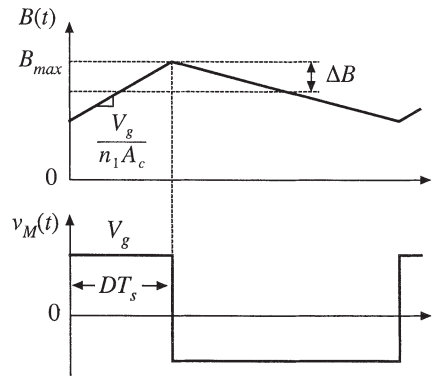


Fig. 14.15 Variation of flux density $B(t)$, flyback transformer example.

flux density to increase with slope

$$\frac{dB(t)}{dt} = \frac{V_g}{n_1 A_c} \tag{14.86}$$

Over the first subinterval $0 < t < DT_s$, the flux density $B(t)$ changes by the net amount $2\Delta B$. This net change is equal to the slope given by Eq. (14.86), multiplied by the interval length DT_s:

$$\Delta B = \left(\frac{V_g}{2n_1 A_c}\right)(DT_s) \tag{14.87}$$

Upon solving for ΔB and expressing A_c in cm^2, we obtain

$$\Delta B = \frac{V_g DT_s}{2n_1 A_c} 10^4 \tag{14.88}$$

For the flyback transformer example, the peak ac flux density is found to be

$$\begin{aligned} \Delta B &= \frac{(200\text{ V})(0.4)(6.67\ \mu\text{s})}{2(59)(1.09\text{ cm}^2)} 10^4 \\ &= 0.041\text{ T} \end{aligned} \tag{14.89}$$

To determine the core loss, we next examine the data provided by the manufacturer for the given core material. A typical plot of core loss is illustrated in Fig. 14.16. For the values of ΔB and switching frequency of the flyback transformer design, this plot indicates that 0.078 W will be lost in every cm^3 of the core material. Of course, this value neglects the effects of harmonics on core loss. The total core loss P_{fe} will therefore be equal to this loss density, multiplied by the volume of the core:

$$\begin{aligned} P_{fe} &= (0.078\text{ W/cm}^3)(A_c \ell_m) \\ &= (0.078\text{ W/cm}^3)(1.09\text{ cm}^2)(5.77\text{ cm}) \\ &= 0.49\text{ W} \end{aligned} \tag{14.90}$$

This core loss is somewhat less than the copper loss of 1.5 W, and neglecting the core loss is often warranted in designs that operate in the continuous conduction mode and that employ ferrite core materials.

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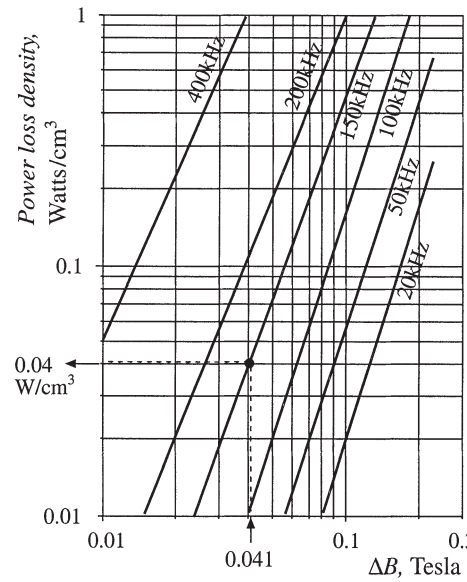


Fig. 14.16 Determination of core loss density for the flyback transformer design example.

14.5 SUMMARY OF KEY POINTS

1. A variety of magnetic devices are commonly used in switching converters. These devices differ in their core flux density variations, as well as in the magnitudes of the ac winding currents. When the flux density variations are small, core loss can be neglected. Alternatively, a low-frequency material can be used, having higher saturation flux density.
2. The core geometrical constant K_g is a measure of the magnetic size of a core, for applications in which copper loss is dominant. In the K_g design method, flux density and total copper loss are specified. Design procedures for single-winding filter inductors and for conventional multiple-winding transformers are derived.

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[3] T. G. WILSON JR., T. G. WILSON, and H. A. OWEN, "Coupling of Magnetic Design Choices to DC–to–DC Converter Electrical Performance," *IEEE Applied Power Electronics Conference*, 1994 Record, pp. 340-347.

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PROBLEMS

14.1 A simple buck converter operates with a 50 kHz switching frequency and a dc input voltage of $V_g = 40$ V. The output voltage is $V = 20$ V. The load resistance is $R \geq 4\ \Omega$.

(a) Determine the value of the output filter inductance L such that the peak-to-average inductor current ripple Δi is 10% of the dc component I.

(b) Determine the peak steady-state inductor current I_{max}.

(c) Design an inductor which has the values of L and I_{max} from parts (a) and (b). Use a ferrite EE core, with $B_{max} = 0.25$ T. Choose a value of winding resistance such that the inductor copper loss is less than or equal to 1 W at room temperature. Assume $K_u = 0.5$. Specify: core size, gap length, wire size (AWG), and number of turns.

14.2 A boost converter operates at the following quiescent point: $V_g = 28$ V, $V = 48$ V, $P_{load} = 150$ W, $f_s = 100$ kHz. Design the inductor for this converter. Choose the inductance value such that the peak current ripple is 10% of the dc inductor current. Use a peak flux density of 0.225 T, and assume a fill factor of 0.5. Allow copper loss equal to 0.5% of the load power, at room temperature. Use a ferrite PQ core. Specify: core size, air gap length, wire gauge, and number of turns.

14.3 Extension of the K_g approach to design of two-winding transformers. It is desired to design a transformer having a turns ratio of 1:n. The transformer stores negligible energy, no air gap is required, and the ratio of the winding currents $i_2(t)/i_1(t)$ is essentially equal to the turns ratio n. The applied primary volt-seconds λ_1 are defined for a typical PWM voltage waveform $v_1(t)$ in Fig. 13.45(b); these volt-seconds should cause the maximum flux density to be equal to a specified value $B_{max} = \Delta B$. You may assume that the flux density $B(t)$ contains no dc bias, as in Fig. 13.46. You should allocate half of the core window area to each winding. The total copper loss P_{cu} is also specified. You may neglect proximity losses.

(a) Derive a transformer design procedure, in which the following quantities are specified: total copper loss P_{cu}, maximum flux density B_{max}, fill factor K_u, wire resistivity ρ, rms primary current I_1, applied primary volt-seconds λ_1, and turns ratio 1:n. Your procedure should yield the following data: required core geometrical constant K_g, primary and secondary turns n_1 and n_2, and primary and secondary wire areas A_{w1} and A_{w2}.

(b) The voltage waveform applied to the transformer primary winding of the Ćuk converter [Fig. 6.41(c)] is equal to the converter input voltage V_g while the transistor conducts, and is equal to $-V_g D/(1 - D)$ while the diode conducts. This converter operates with a switching frequency of 100 kHz, and a transistor duty cycle D equal to 0.4. The dc input voltage is $V_g = 120$ V, the dc output voltage is $V = 24$ V, and the load power is 200 W. You may assume a fill factor of $K_u = 0.3$. Use your procedure of part (a) to design a transformer for this application, in which $B_{max} = 0.15$ T, and $P_{cu} = 0.25$ W at 100°C. Use a ferrite PQ core. Specify: core size, primary and secondary turns, and wire gauges.

14.4 Coupled inductor design. The two-output forward converter of Fig. 13.47(a) employs secondary-side coupled inductors. An air gap is employed.

Design a coupled inductor for the following application: $V_1 = 5$ V, $V_2 = 15$ V, $I_1 = 20$ A, $I_2 = 4$ A, $D = 0.4$. The magnetizing inductance should be equal to 8 μH, referred to the 5 V winding. You may assume a fill factor K_u of 0.5. Allow a total of 1 W of copper loss at 100°C, and use a peak flux density of

B_{max} = 0.2 T. Use a ferrite EE core. Specify: core size, air gap length, number of turns and wire gauge for each winding.

14.5 Flyback transformer design. A flyback converter operates with a 160 Vdc input, and produces a 28 Vdc output. The maximum load current is 2 A. The transfomer turns ratio is 8:1. The switching frequency is 100 kHz. The converter should be designed to operate in the discontinuous conduction mode at all load currents. The total copper loss should be less than 0.75 W.

(a) Choose the value of transformer magnetizing inductance L_M such that, at maximum load current, D_3 = 0.1 (the duty cycle of subinterval 3, in which all semiconductors are off). Please indicate whether your value of L_M is referred to the primary or secondary winding. What is the peak transistor current? The peak diode current?

(b) Design a flyback transformer for this application. Use a ferrite pot core with B_{max} = 0.25 Tesla, and with fill factor K_u = 0.4. Specify: core size, primary and secondary turns and wire sizes, and air gap length.

(c) For your design of part (b), compute the copper losses in the primary and secondary windings. You may neglect proximity loss.

(d) For your design of part (b), compute the core loss. Loss data for the core material is given by Fig. 13.20. Is the core loss less than the copper loss computed in Part (c)?

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15
Transformer Design

In the design methods of the previous chapter, copper loss P_{cu} and maximum flux density B_{max} are specified, while core loss P_{fe} is not specifically addressed. This approach is appropriate for a number of applications, such as the filter inductor in which the dominant design constraints are copper loss and saturation flux density. However, in a substantial class of applications, the operating flux density is limited by core loss rather than saturation. For example, in a conventional high-frequency transformer, it is usually necessary to limit the core loss by operating at a reduced value of the peak ac flux density ΔB.

This chapter covers the general transformer design problem. It is desired to design a k–winding transformer as illustrated in Fig. 15.1. Both copper loss P_{cu} and core loss P_{fe} are modeled. As the operating flux density is increased (by decreasing the number of turns), the copper loss is decreased but the core loss is increased. We will determine the operating flux density that minimizes the total power loss $P_{tot} = P_{fe} + P_{cu}$.

It is possible to generalize the core geometrical constant K_g design method, derived in the previous chapter, to treat the design of magnetic devices when both copper loss and core loss are significant. This leads to the geometrical constant K_{gfe}, a measure of the effective magnetic size of core in a transformer design application. Several examples of transformer designs via the K_{gfe} method are given in this chapter. A similar procedure is also derived, for design of single-winding inductors in which core loss is significant.

15.1 TRANSFORMER DESIGN: BASIC CONSTRAINTS

As in the case of the filter inductor design, we can write several basic constraining equations. These equations can then be combined into a single equation for selection of the core size. In the case of transformer design, the basic constraints describe the core loss, flux density, copper loss, and total power loss

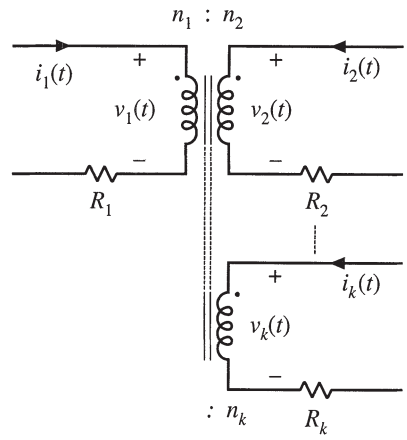


Fig. 15.1 A *k*-winding transformer, in which both core loss and copper loss are significant.

vs. flux density. The flux density is then chosen to optimize the total power loss.

15.1.1 Core Loss

As described in Chapter 13, the total core loss P_{fe} depends on the peak ac flux density ΔB, the operating frequency f, and the volume of the core. At a given frequency, we can approximate the core loss by a function of the form

$$P_{fe} = K_{fe}(\Delta B)^{\beta} A_c \ell_m \tag{15.1}$$

Again, A_c is the core cross-sectional area, ℓ_m is the core mean magnetic path length, and hence $A_c \ell_m$ is the volume of the core. K_{fe} is a constant of proportionality which depends on the operating frequency. The exponent β is determined from the core manufacturer's published data. Typically, the value of β for ferrite power materials is approximately 2.6; for other core materials, this exponent lies in the range 2 to 3. Equation (15.1) generally assumes that the applied waveforms are sinusoidal; effects of waveform harmonic content are ignored here.

15.1.2 Flux Density

An arbitrary periodic primary voltage waveform $v_1(t)$ is illustrated in Fig. 15.2. The volt-seconds applied during the positive portion of the waveform is denoted λ_1:

$$\lambda_1 = \int_{t_1}^{t_2} v_1(t)\,dt \tag{15.2}$$

These volt-seconds, or flux-linkages, cause the flux density to change from its negative peak to its positive peak value. Hence, from Faraday's law, the peak value of the ac component of the flux density is

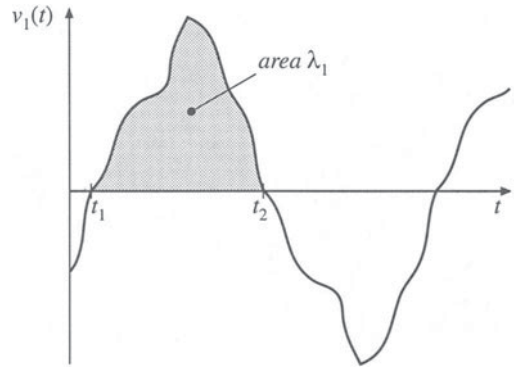


Fig. 15.2 An arbitrary transformer primary voltage waveforms, illustrating the volt-seconds applied during the positive portion of the cycle.

$$\Delta B = \frac{\lambda_1}{2n_1 A_c} \tag{15.3}$$

Note that, for a given applied voltage waveform and λ_1, we can reduce ΔB by increasing the primary turns n_1. This has the effect of decreasing the core loss according to Eq. (15.1). However, it also causes the copper loss to increase, since the new windings will be comprised of more turns of smaller wire. As a result, there is an optimal choice for ΔB, in which the total loss is minimized. In the next sections, we will determine the optimal ΔB. Having done so, we can then use Eq. (15.3) to determine the primary turns n_1, as follows:

$$n_1 = \frac{\lambda_1}{2\Delta B A_c} \tag{15.4}$$

It should also be noted that, in some converter topologies such as the forward converter with conventional reset winding, the flux density $B(t)$ and the magnetizing current $i_M(t)$ are not allowed to be negative. In consequence, the instantaneous flux density $B(t)$ contains a dc bias. Provided that the core does not approach saturation, this dc bias does not significantly affect the core loss: core loss is determined by the ac component of $B(t)$. Equations (15.2) to (15.4) continue to apply to this case, since ΔB is the peak value of the ac component of $B(t)$.

15.1.3 Copper Loss

As shown in Section 14.3.1, the total copper loss is minimized when the core window area W_A is allocated to the various windings according to their relative apparent powers. The total copper loss is then given by Eq. (14.34). This equation can be expressed in the form

$$P_{cu} = \frac{\rho(MLT) n_1^2 I_{tot}^2}{W_A K_u} \tag{15.5}$$

where

$$I_{tot} = \sum_{j=1}^{k} \frac{n_j}{n_1} I_j \tag{15.6}$$

is the sum of the rms winding currents, referred to winding 1. Use of Eq. (15.4) to eliminate n_1 from Eq. (15.5) leads to

$$P_{cu} = \left(\frac{\rho \lambda_1^2 I_{tot}^2}{4K_u}\right)\left(\frac{(MLT)}{W_A A_c^2}\right)\left(\frac{1}{\Delta B}\right)^2 \tag{15.7}$$

The right-hand side of Eq. (15.7) is grouped into three terms. The first group contains specifications, while the second group is a function of the core geometry. The last term is a function of ΔB, to be chosen to optimize the design. It can be seen that copper loss varies as the inverse square of ΔB; increasing ΔB reduces P_{cu}.

The increased copper loss due to the proximity effect is not explicitly accounted for in this design procedure. In practice, the proximity loss must be estimated after the core and winding geometries are known. However, the increased ac resistance due to proximity loss can be accounted for in the design procedure. The effective value of the wire resistivity ρ is increased by a factor equal to the estimated ratio R_{ac}/R_{dc}. When the core geometry is known, the engineer can attempt to implement the windings such that the estimated R_{ac}/R_{dc} is obtained. Several design iterations may be needed.

15.1.4 Total power loss vs. ΔB

The total power loss P_{tot} is found by adding Eqs. (15.1) and (15.7):

$$P_{tot} = P_{fe} + P_{cu} \tag{15.8}$$

The dependence of P_{fe}, P_{cu}, and P_{tot} on ΔB is sketched in Fig. 15.3.

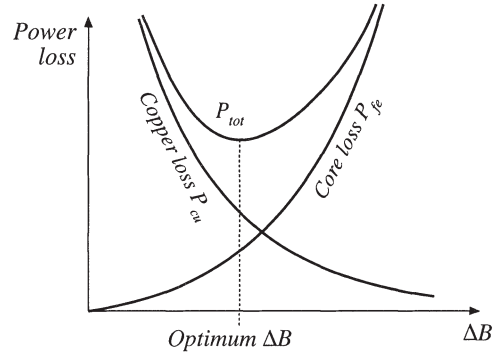


Fig. 15.3 Dependence of copper loss, core loss, and total loss on peak ac flux density.

15.1.5 Optimum Flux Density

Let us now choose the value of ΔB that minimizes Eq. (15.8). At the optimum ΔB, we can write

$$\frac{dP_{tot}}{d(\Delta B)} = \frac{dP_{fe}}{d(\Delta B)} + \frac{dP_{cu}}{d(\Delta B)} = 0 \tag{15.9}$$

Note that the optimum does not necessarily occur where $P_{fe} = P_{cu}$. Rather, it occurs where

$$\frac{dP_{fe}}{d(\Delta B)} = -\frac{dP_{cu}}{d(\Delta B)} \tag{15.10}$$

The derivatives of the core and copper losses with respect to ΔB are given by

$$\frac{dP_{fe}}{d(\Delta B)} = \beta K_{fe} (\Delta B)^{(\beta - 1)} A_c \ell_m \tag{15.11}$$

$$\frac{dP_{cu}}{d(\Delta B)} = -2 \left(\frac{\rho \lambda_1^2 I_{tot}^2}{4 K_u} \right) \left(\frac{(MLT)}{W_A A_c^2} \right) (\Delta B)^{-3} \tag{15.12}$$

Substitution of Eqs. (15.11) and (15.12) into Eq. (15.10), and solution for ΔB, leads to the optimum flux density

$$\Delta B = \left[\frac{\rho \lambda_1^2 I_{tot}^2}{2 K_u} \frac{(MLT)}{W_A A_c^3 \ell_m} \frac{1}{\beta K_{fe}} \right]^{\left(\frac{1}{\beta + 2}\right)} \tag{15.13}$$

The resulting total power loss is found by substitution of Eq. (15.13) into (15.1), (15.8), and (15.9). Simplification of the resulting expression leads to

$$P_{tot} = \left[A_c \ell_m K_{fe} \right]^{\left(\frac{2}{\beta + 2}\right)} \left[\frac{\rho \lambda_1^2 I_{tot}^2}{4 K_u} \frac{(MLT)}{W_A A_c^2} \right]^{\left(\frac{\beta}{\beta + 2}\right)} \left[\left(\frac{\beta}{2}\right)^{-\left(\frac{\beta}{\beta + 2}\right)} + \left(\frac{\beta}{2}\right)^{\left(\frac{2}{\beta + 2}\right)} \right] \tag{15.14}$$

This expression can be regrouped, as follows:

$$\frac{W_A \left(A_c\right)^{(2(\beta - 1)/\beta)}}{(MLT) \ell_m^{(2/\beta)}} \left[\left(\frac{\beta}{2}\right)^{-\left(\frac{\beta}{\beta + 2}\right)} + \left(\frac{\beta}{2}\right)^{\left(\frac{2}{\beta + 2}\right)} \right]^{-\left(\frac{\beta + 2}{\beta}\right)} = \frac{\rho \lambda_1^2 I_{tot}^2 K_{fe}^{(2/\beta)}}{4 K_u \left(P_{tot}\right)^{\left((\beta + 2)/\beta\right)}} \tag{15.15}$$

The terms on the left side of Eq. (15.15) depend on the core geometry, while the terms on the right side depend on specifications regarding the application (ρ, I_{tot}, λ_1, K_u, P_{tot}) and the desired core material (K_{fe}, β). The left side of Eq. (15.15) can be defined as the core geometrical constant K_{gfe}:

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$$K_{gfe} = \frac{W_A \left(A_c\right)^{\left(2(\beta-1)/\beta\right)}}{(MLT)\ell_m^{(2/\beta)}} \left[\left(\frac{\beta}{2}\right)^{-\left(\frac{\beta}{\beta+2}\right)} + \left(\frac{\beta}{2}\right)^{\left(\frac{2}{\beta+2}\right)} \right]^{-\left(\frac{\beta+2}{\beta}\right)} \tag{15.16}$$

Hence, to design a transformer, the right side of Eq. (15.15) is evaluated. A core is selected whose K_{gfe} exceeds this value:

$$K_{gfe} \geq \frac{\rho \lambda_1^2 I_{tot}^2 K_{fe}^{(2/\beta)}}{4K_u \left(P_{tot}\right)^{\left((\beta+2)/\beta\right)}} \tag{15.17}$$

The quantity K_{gfe} is similar to the geometrical constant K_g used in the previous chapter to design magnetics when core loss is negligible. K_{gfe} is a measure of the magnetic size of a core, for applications in which core loss is significant. Unfortunately, K_{gfe} depends on β, and hence the choice of core material affects the value of K_{gfe}. However, the β of most high-frequency ferrite materials lies in the narrow range 2.6 to 2.8, and K_{gfe} varies by no more than ± 5% over this range. Appendix D lists the values of K_{gfe} for various standard ferrite cores, for the value $\beta = 2.7$.

Once a core has been selected, then the values of A_c, W_A, ℓ_m, and MLT are known. The peak ac flux density ΔB can then be evaluated using Eq. (15.13), and the primary turns n_1 can be found using Eq. (15.4). The number of turns for the remaining windings can be computed using the desired turns ratios. The various window area allocations are found using Eq. (14.35). The wire sizes for the various windings can then be computed as discussed in the previous chapter,

$$A_{w,j} = \frac{K_u W_A \alpha_j}{n_j} \tag{15.18}$$

where $A_{w,j}$ is the wire area for winding j.

15.2 A STEP-BY-STEP TRANSFORMER DESIGN PROCEDURE

The procedure developed in the previous sections is summarized below. As in the filter inductor design procedure of the previous chapter, this simple transformer design procedure should be regarded as a first-pass approach. Numerous issues have been neglected, including detailed insulation requirements, conductor eddy current losses, temperature rise, roundoff of number of turns, etc.

The following quantities are specified, using the units noted:

Wire effective resistivity	ρ	(Ω-cm)
Total rms winding currents, referred to primary	$I_{tot} = \sum_{j=1}^{k} \frac{n_j}{n_i} I_j$	(A)
Desired turns ratios	n_2/n_1, n_3/n_1, etc.	
Applied primary volt-seconds	$\lambda_1 = \int_{\substack{positive \\ portion \\ of\ cycle}} v_1(t)\,dt$	(V-sec)

Allowed total power dissipation	P_{tot}	(W)
Winding fill factor	K_u	
Core loss exponent	β	
Core loss coefficient	K_{fe}	(W/cm^{3}T$^\beta$)

The core dimensions are expressed in cm:

Core cross-sectional area	A_c	(cm^2)
Core window area	W_A	(cm^2)
Mean length per turn	MLT	(cm)
Magnetic path length	ℓ_m	(cm)
Peak ac flux density	ΔB	(Tesla)
Wire areas	$A_{w1}, A_{w2}, \ldots$	(cm^2)

The use of centimeters rather than meters requires that appropriate factors be added to the design equations.

15.2.1 Procedure

1. *Determine core size.*

$$K_{gfe} \geq \frac{\rho \lambda_1^2 I_{tot}^2 K_{fe}^{(2/\beta)}}{4 K_u \left(P_{tot}\right)^{\left((\beta+2)/\beta\right)}} 10^8 \tag{15.19}$$

Choose a core that is large enough to satisfy this inequality. If necessary, it may be possible to use a smaller core by choosing a core material having lower loss, i.e., smaller K_{fe}.

2. *Evaluate peak ac flux density.*

$$\Delta B = \left[10^8 \frac{\rho \lambda_1^2 I_{tot}^2}{2 K_u} \frac{(MLT)}{W_A A_c^3 \ell_m} \frac{1}{\beta K_{fe}} \right]^{\left(\frac{1}{\beta+2}\right)} \tag{15.20}$$

Check whether ΔB is greater than the core material saturation flux density. If the core operates with a flux dc bias, then the dc bias plus ΔB should not exceed the saturation flux density. Proceed to the next step if adequate margins exist to prevent saturation. Otherwise, (1) repeat the procedure using a core material having greater core loss, or (2) use the K_g design method, in which the maximum flux density is specified.

3. *Evaluate primary turns.*

$$n_1 = \frac{\lambda_1}{2 \Delta B A_c} 10^4 \tag{15.21}$$

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4. *Choose numbers of turns for other windings*

   According to the desired turns ratios:

$$\begin{aligned} n_2 &= n_1\left(\frac{n_2}{n_1}\right) \\ n_3 &= n_1\left(\frac{n_3}{n_1}\right) \\ &\vdots \end{aligned} \tag{15.22}$$

5. *Evaluate fraction of window area allocated to each winding.*

$$\begin{aligned} \alpha_1 &= \frac{n_1 I_1}{n_1 I_{tot}} \\ \alpha_2 &= \frac{n_2 I_2}{n_1 I_{tot}} \\ &\vdots \\ \alpha_k &= \frac{n_k I_k}{n_1 I_{tot}} \end{aligned} \tag{15.23}$$

6. *Evaluate wire sizes.*

$$\begin{aligned} A_{w1} &\le \frac{\alpha_1 K_u W_A}{n_1} \\ A_{w2} &\le \frac{\alpha_2 K_u W_A}{n_2} \\ &\vdots \end{aligned} \tag{15.24}$$

Choose wire gauges to satisfy these criteria

A winding geometry can now be determined, and copper losses due to the proximity effect can be evaluated. If these losses are significant, it may be desirable to further optimize the design by reiterating the above steps, accounting for proximity losses by increasing the effective wire resistivity to the value $\rho_{eff} = \rho_{cu} P_{cu}/P_{dc}$, where P_{cu} is the actual copper loss including proximity effects, and P_{dc} is the copper loss obtained when the proximity effect is negligible.

If desired, the power losses and transformer model parameters can now be checked. For the simple model of Fig. 15.4, the following parameters are estimated:

Magnetizing inductance, referred to winding 1: $L_M = \dfrac{\mu n_1^2 A_c}{\ell_m}$

Peak ac magnetizing current, referred to winding 1: $i_{M,pk} = \dfrac{\lambda_1}{2L_M}$

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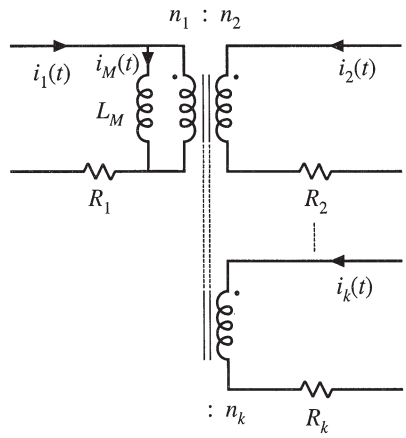


Fig. 15.4 Computed elements of simple transformer model.

Winding resistances:

$$R_1 = \frac{\rho n_1 (MLT)}{A_{w1}}$$
$$R_2 = \frac{\rho n_2 (MLT)}{A_{w2}}$$
$$\vdots$$

The core loss, copper loss, and total power loss can be determined using Eqs. (15.1), (15.7), and (15.8), respectively.

15.3 EXAMPLES

15.3.1 Example 1: Single-Output Isolated Ćuk Converter

As an example, let us consider the design of a simple two-winding transformer for the Ćuk converter of Fig. 15.5. This transformer is to be optimized at the operating point shown, corresponding to $D = 0.5$. The steady-state converter solution is $V_{c1} = V_g$, $V_{c2} = V$. The desired transformer turns ratio is

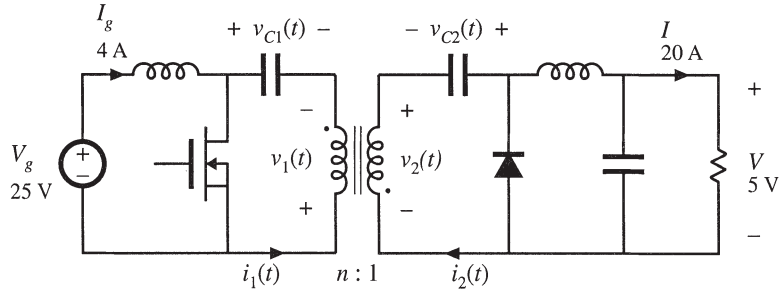


Fig. 15.5 Isolated Ćuk converter example.

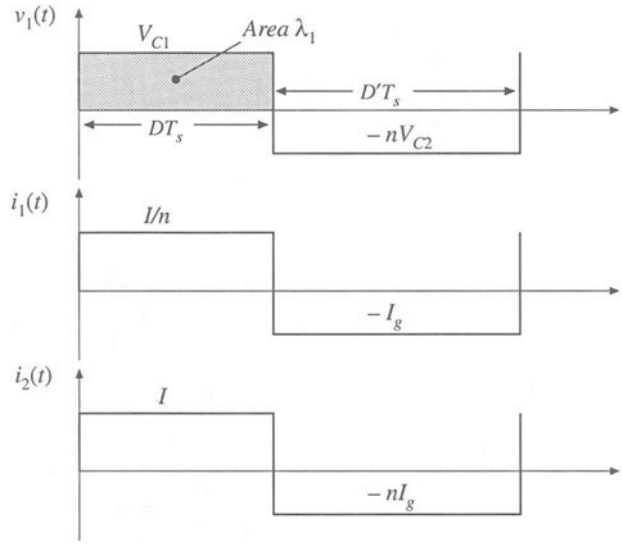


Fig. 15.6 Waveforms, Ćuk converter transformer design example.

$n = n_1/n_2 = 5$. The switching frequency is $f_s = 200$ kHz, corresponding to $T_s = 5$ μs. A ferrite pot core consisting of Magnetics, Inc. P-material is to be used; at 200 kHz, this material is described by the following parameters: $K_{fe} = 24.7$ W/T$^{\beta}$cm^3, $\beta = 2.6$. A fill factor of $K_u = 0.5$ is assumed. Total power loss of $P_{tot} = 0.25$ W is allowed. Copper wire, having a resistivity of $\rho = 1.724 \cdot 10^{-6}$ Ω–cm, is to be used.

Transformer waveforms are illustrated in Fig. 15.6. The applied primary volt-seconds are

$$\begin{aligned}\lambda_1 &= DT_s V_{c1} = (0.5)(5\ \mu\text{sec})(25\ \text{V}) \\ &= 62.5\ \text{V–}\mu\text{sec}\end{aligned} \tag{15.25}$$

The primary rms current is

$$I_1 = \sqrt{D\left(\frac{I}{n}\right)^2 + D'\left(I_g\right)^2} = 4\ \text{A} \tag{15.26}$$

It is assumed that the rms magnetizing current is much smaller than the rms winding currents. Since the transformer contains only two windings, the secondary rms current is equal to

$$I_2 = nI_1 = 20\ \text{A} \tag{15.27}$$

The total rms winding current, referred to the primary, is

$$I_{tot} = I_1 + \frac{1}{n} I_2 = 8\ \text{A} \tag{15.28}$$

The core size is evaluated using Eq. (15.19):

$$\begin{aligned}K_{gfe} &\geq \frac{(1.724 \cdot 10^{-6})(62.5 \cdot 10^{-6})^2 (8)^2 (24.7)^{(2/2.6)}}{4\,(0.5)(0.25)^{(4.6/2.6)}}\, 10^8 \\ &= 0.00295\end{aligned} \tag{15.29}$$

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The pot core data of Appendix D lists the 2213 pot core with $K_{gfe} = 0.0049$ for $\beta = 2.7$. Evaluation of Eq. (15.16) shows that $K_{gfe} = 0.0047$ for this core, when $\beta = 2.6$. In any event, 2213 is the smallest standard pot core size having $K_{gfe} \leq 0.00295$. The increased value of K_{gfe} should lead to lower total power loss. The peak ac flux density is found by evaluation of Eq. (15.20), using the geometrical data for the 2213 pot core:

$$\Delta B = \left[10^8 \frac{(1.724 \cdot 10^{-6})(62.5 \cdot 10^{-6})^2 (8)^2}{2\,(0.5)} \frac{(4.42)}{(0.297)(0.635)^3 (3.15)} \frac{1}{(2.6)(24.7)} \right]^{(1/4.6)} \tag{15.30}$$
$$= 0.0858 \text{ Tesla}$$

This flux density is considerably less than the saturation flux density of approximately 0.35 Tesla. The primary turns are determined by evaluation of Eq. (15.21):

$$n_1 = 10^4 \frac{(62.5 \cdot 10^{-6})}{2(0.0858)(0.635)} \tag{15.31}$$
$$= 5.74 \text{ turns}$$

The secondary turns are found by evaluation of Eq. (15.22). It is desired that the transformer have a 5:1 turns ratio, and hence

$$n_2 = \frac{n_1}{n} = 1.15 \text{ turns} \tag{15.32}$$

In practice, we might select $n_1 = 5$ and $n_2 = 1$. This would lead to a slightly higher ΔB and slightly higher loss.

The fraction of the window area allocated to windings 1 and 2 are determined using Eq. (15.23):

$$\alpha_1 = \frac{(4 \text{ A})}{(8 \text{ A})} = 0.5$$
$$\alpha_2 = \frac{\left(\frac{1}{5}\right)(20 \text{ A})}{(8 \text{ A})} = 0.5 \tag{15.33}$$

For this example, the window area is divided equally between the primary and secondary windings, since the ratio of their rms currents is equal to the turns ratio. We can now evaluate the primary and secondary wire areas, via Eq. (15.24):

$$A_{w1} = \frac{(0.5)(0.5)(0.297)}{(5)} = 14.8 \cdot 10^{-3} \text{ cm}^2$$
$$A_{w2} = \frac{(0.5)(0.5)(0.297)}{(1)} = 74.2 \cdot 10^{-3} \text{ cm}^2 \tag{15.34}$$

The wire gauge is selected using the wire table of Appendix D. AWG #16 has area $13.07 \cdot 10^{-3}$ cm^2, and is suitable for the primary winding. AWG #9 is suitable for the secondary winding, with area $66.3 \cdot 10^{-3}$ cm^2. These are very large conductors, and one turn of AWG #9 is not a practical solution! We can also expect significant proximity losses, and significant leakage inductance. In practice, interleaved foil windings might be used. Alternatively, Litz wire or several parallel strands of smaller wire could be employed.

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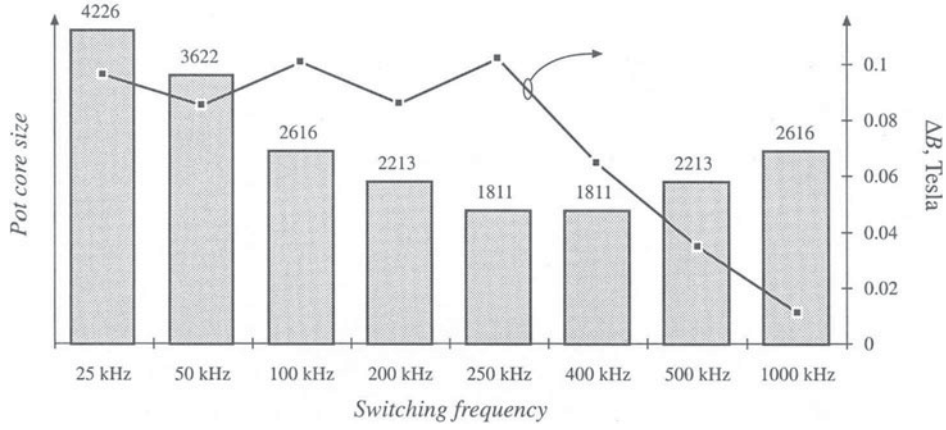


Fig. 15.7 Variation of transformer size (bar chart) with switching frequency, Ćuk converter example. Optimum peak ac flux density (data points) is also plotted.

It is a worthwhile exercise to repeat the above design at several different switching frequencies, to determine how transformer size varies with switching frequency. As the switching frequency is increased, the core loss coefficient K_{fe} increases. Figure 15.7 illustrates the transformer pot core size, for various switching frequencies over the range 25 kHz to 1 MHz, for this Ćuk converter example using P material with $P_{tot} < 0.25$ W. Peak flux densities in Tesla are also plotted. For switching frequencies below 250 kHz, increasing the frequency causes the core size to decrease. This occurs because of the decreased applied volt-seconds λ_1. Over this range, the optimal ΔB is essentially independent of switching frequency; the ΔB variations shown occur owing to quantization of core sizes.

For switching frequencies greater than 250 kHz, increasing frequency causes greatly increased core loss. Maintaining $P_{tot} \leq 0.25$ W then requires that ΔB be reduced, and hence the core size is increased. The minimum transformer size for this example is apparently obtained at 250 kHz.

In practice, several matters complicate the dependence of transformer size on switching frequency. Figure 15.7 ignores the winding geometry and copper losses due to winding eddy currents. Greater power losses can be allowed in larger cores. Use of a different core material may allow higher or lower switching frequencies. The same core material, used in a different application with different specifications, may lead to a different optimal frequency. Nonetheless, examples have been reported in the literature [1–4] in which ferrite transformer size is minimized at frequencies ranging from several hundred kilohertz to several megahertz. More detailed design optimizations can be performed using computer optimization programs [5, 6].

15.3.2 Example 2: Multiple-Output Full-Bridge Buck Converter

As a second example, let us consider the design of transformer T_1 for the multiple-output full-bridge buck converter of Fig. 15.8. This converter has a 5 V and a 15 V output, with maximum loads as shown. The transformer is to be optimized at the full-load operating point shown, corresponding to $D = 0.75$. Waveforms are illustrated in Fig. 15.9. The converter switching frequency is $f_s = 150$ kHz. In the full-bridge configuration, the transformer waveforms have fundamental frequency equal to one-half of the switching frequency, so the effective transformer frequency is 75 kHz. Upon accounting for losses

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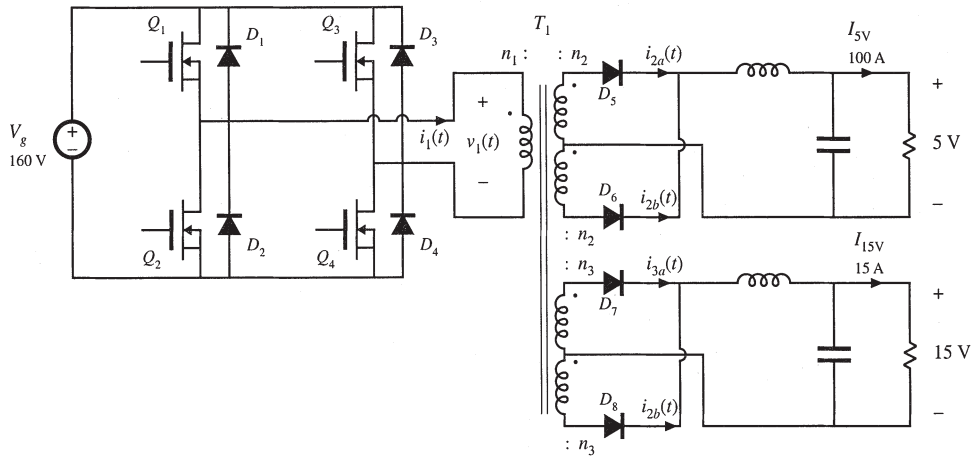


Fig. 15.8 Multiple-output full-bridge isolated buck converter example.

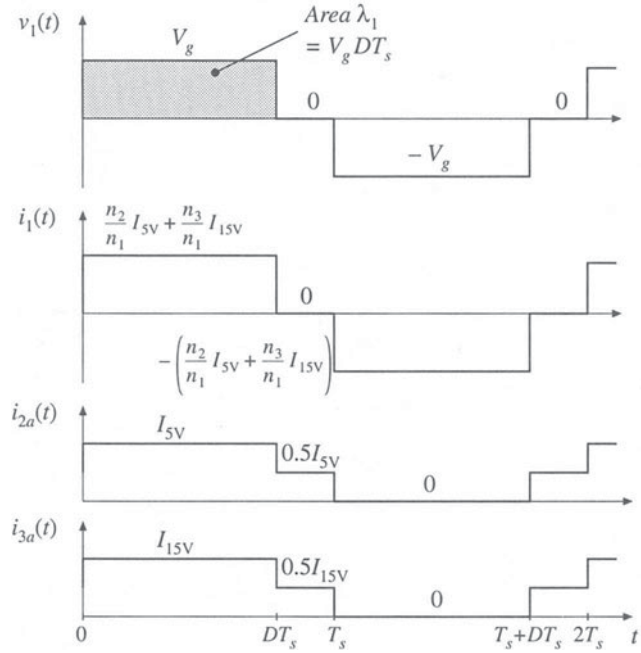


Fig. 15.9 Transformer waveforms, full-bridge converter example.

caused by diode forward voltage drops, one finds that the desired transformer turns ratios $n_1{:}n_2{:}n_3$ are 110:5:15. A ferrite EE consisting of Magnetics, Inc. P-material is to be used in this example; at 75 kHz, this material is described by the following parameters: K_{fe} = 7.6 W/T$^{\beta}$cm^3, β = 2.6. A fill factor of K_u = 0.25 is assumed in this isolated multiple-output application. Total power loss of P_{tot} = 4 W, or approximately 0.5% of the load power, is allowed. Copper wire, having a resistivity of $\rho = 1.724 \cdot 10^{-6}$ Ω–cm, is to be used.

The applied primary volt-seconds are

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$$\lambda_1 = DT_s V_g = (0.75)(6.67\ \mu\text{sec})(160\ \text{V}) = 800\ \text{V–}\mu\text{sec} \tag{15.35}$$

The primary rms current is

$$I_1 = \left(\frac{n_2}{n_1} I_{5\text{V}} + \frac{n_3}{n_1} I_{15\text{V}}\right)\sqrt{D} = 5.7\ \text{A} \tag{15.36}$$

The 5 V secondary windings carry rms current

$$I_2 = \tfrac{1}{2} I_{5\text{V}} \sqrt{1 + D} = 66.1\ \text{A} \tag{15.37}$$

The 15 V secondary windings carry rms current

$$I_3 = \tfrac{1}{2} I_{15\text{V}} \sqrt{1 + D} = 9.9\ \text{A} \tag{15.38}$$

The total rms winding current, referred to the primary, is

$$\begin{aligned} I_{tot} &= \sum_{\substack{all\,5 \\ windings}} \frac{n_j}{n_1} I_j = I_1 + 2\frac{n_2}{n_1} I_2 + 2\frac{n_3}{n_1} I_3 \\ &= 14.4\ \text{A} \end{aligned} \tag{15.39}$$

The core size is evaluated using Eq. (15.19):

$$\begin{aligned} K_{gfe} &\geq \frac{(1.724 \cdot 10^{-6})(800 \cdot 10^{-6})^2 (14.4)^2 (7.6)^{(2/2.6)}}{4(0.25)(4)^{(4.6/2.6)}} 10^8 \\ &= 0.00937 \end{aligned} \tag{15.40}$$

The EE core data of Appendix D lists the EE40 core with $K_{gfe} = 0.0118$ for $\beta = 2.7$. Evaluation of Eq. (15.16) shows that $K_{gfe} = 0.0108$ for this core, when $\beta = 2.6$. In any event, EE40 is the smallest standard EE core size having $K_{gfe} \leq 0.00937$. The peak ac flux density is found by evaluation of Eq. (15.20), using the geometrical data for the EE40 core:

$$\begin{aligned} \Delta B &= \left[10^8 \frac{(1.724 \cdot 10^{-6})(800 \cdot 10^{-6})^2 (14.4)^2}{2(0.25)} \frac{(8.5)}{(1.1)(1.27)^3 (7.7)} \frac{1}{(2.6)(7.6)}\right]^{(1/4.6)} \\ &= 0.23\ \text{Tesla} \end{aligned} \tag{15.41}$$

This flux density is less than the saturation flux density of approximately 0.35 Tesla. The primary turns are determined by evaluation of Eq. (15.21):

$$\begin{aligned} n_1 &= 10^4 \frac{(800 \cdot 10^{-6})}{2(0.23)(1.27)} \\ &= 13.7\ \text{turns} \end{aligned} \tag{15.42}$$

The secondary turns are found by evaluation of Eq. (15.22). It is desired that the transformer have a 110:5:15 turns ratio, and hence

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$$n_2 = \frac{5}{110} n_1 = 0.62 \text{ turns} \tag{15.43}$$

$$n_3 = \frac{15}{110} n_1 = 1.87 \text{ turns} \tag{15.44}$$

In practice, we might select $n_1 = 22$, $n_2 = 1$, and $n_3 = 3$. This would lead to a reduced ΔB with reduced core loss and increased copper loss. Since the resulting ΔB is suboptimal, the total power loss will be increased. According to Eq. (15.3), the peak ac flux density for the EE40 core will be

$$\Delta B = \frac{(800 \cdot 10^{-6})}{2(22)(1.27)} 10^4 = 0.143 \text{ Tesla} \tag{15.45}$$

The resulting core and copper loss can be computed using Eqs. (15.1) and (15.7):

$$P_{fe} = (7.6)(0.143)^{2.6}(1.27)(7.7) = 0.47 \text{ W} \tag{15.46}$$

$$P_{cu} = \frac{(1.724 \cdot 10^{-6})(800 \cdot 10^{-6})^2 (14.4)^2}{4\,(0.25)} \frac{(8.5)}{(1.1)(1.27)^2} \frac{1}{(0.143)^2} 10^8 = 5.4 \text{ W} \tag{15.47}$$

Hence, the total power loss would be

$$P_{tot} = P_{fe} + P_{cu} = 5.9 \text{ W} \tag{15.48}$$

Since this is 50% greater than the design goal of 4 W, it is necessary to increase the core size. The next larger EE core is the EE50 core, having K_{gfe} of 0.0284. The optimum ac flux density for this core, given by Eq. (15.3), is $\Delta B = 0.14$ T; operation at this flux density would require $n_1 = 12$ and would lead to a total power loss of 2.3 W. With $n_1 = 22$, calculations similar to Eqs. (15.45) to (15.48) lead to a peak flux density of $\Delta B = 0.08$ T. The resulting power losses would then be $P_{fe} = 0.23$ W, $P_{cu} = 3.89$ W, $P_{tot} = 4.12$ W.

With the EE50 core and $n_1 = 22$, the fraction of the available window area allocated to the primary winding is given by Eq. (15.23) as

$$\alpha_1 = \frac{I_1}{I_{tot}} = \frac{5.7}{14.4} = 0.396 \tag{15.49}$$

The fraction of the available window area allocated to each half of the 5 V secondary winding should be

$$\alpha_2 = \frac{n_2 I_2}{n_1 I_{tot}} = \frac{5}{110} \frac{66.1}{14.4} = 0.209 \tag{15.50}$$

The fraction of the available window area allocated to each half of the 15 V secondary winding should be

$$\alpha_3 = \frac{n_3 I_3}{n_1 I_{tot}} = \frac{15}{110} \frac{9.9}{14.4} = 0.094 \tag{15.51}$$

The primary wire area A_{w1}, 5 V secondary wire area A_{w2}, and 15 V secondary wire area A_{w3} are then given

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by Eq. (15.24) as

$$\begin{aligned} A_{w1} &= \frac{\alpha_1 K_u W_A}{n_1} = \frac{(0.396)(0.25)(1.78)}{(22)} = 8.0 \cdot 10^{-3}\ \text{cm}^2 \\ &\Rightarrow \text{AWG \#19} \\ A_{w2} &= \frac{\alpha_2 K_u W_A}{n_2} = \frac{(0.209)(0.25)(1.78)}{(1)} = 93.0 \cdot 10^{-3}\ \text{cm}^2 \\ &\Rightarrow \text{AWG \#8} \\ A_{w3} &= \frac{\alpha_3 K_u W_A}{n_3} = \frac{(0.094)(0.25)(1.78)}{(3)} = 13.9 \cdot 10^{-3}\ \text{cm}^2 \\ &\Rightarrow \text{AWG \#16} \end{aligned} \tag{15.52}$$

It may be preferable to wind the 15 V outputs using two #19 wires in parallel; this would lead to the same area A_{w3} but would be easier to wind. The 5 V windings could be wound using many turns of smaller paralleled wires, but it would probably be easier to use a flat copper foil winding. If insulation requirements allow, proximity losses could be minimized by interleaving several thin layers of foil with the primary winding.

15.4 AC INDUCTOR DESIGN

The transformer design procedure of the previous sections can be adapted to handle the design of other magnetic devices in which both core loss and copper loss are significant. A procedure is outlined here for design of single-winding inductors whose waveforms contain significant high-frequency ac components (Fig. 15.10). An optimal value of ΔB is found, which leads to minimum total core-plus-copper loss. The major difference is that we must design to obtain a given inductance, using a core with an air gap. The constraints and a step-by-step procedure are briefly outlined below.

15.4.1 Outline of Derivation

As in the filter inductor design procedure of the previous chapter, the desired inductance L must be obtained, given by

$$L = \frac{\mu_0 A_c n^2}{\ell_g} \tag{15.53}$$

The applied voltage waveform and the peak ac component of the flux density ΔB are related according to

$$\Delta B = \frac{\lambda}{2nA_c} \tag{15.54}$$

The copper loss is given by

$$P_{cu} = \frac{\rho n^2 (MLT)}{K_u W_A} I^2 \tag{15.55}$$

where I is the rms value of $i(t)$. The core loss P_{fe} is given by Eq. (15.1).

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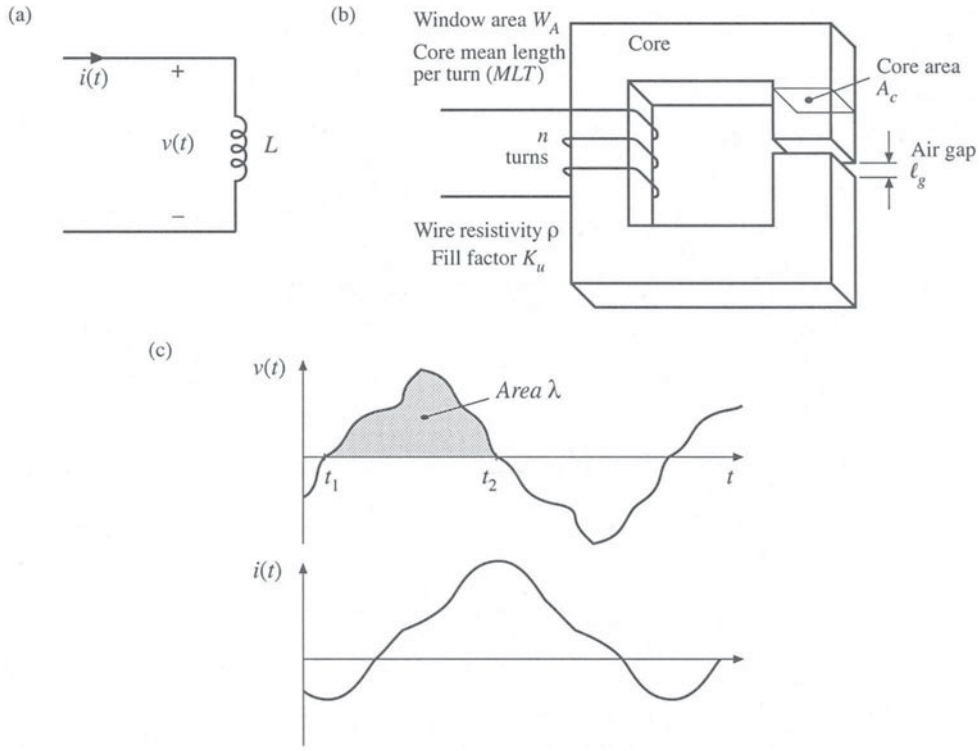


Fig. 15.10 Ac inductor, in which copper loss and core loss are significant: (a) definition of terminal quantities, (b) core geometry, (c) arbitrary terminal waveforms.

The value of ΔB that minimizes the total power loss $P_{tot} = P_{cu} + P_{fe}$ is found in a manner similar to the transformer design derivation. Equation (15.54) is used to eliminate n from the expression for P_{cu}. The optimal ΔB is then computed by setting the derivative of P_{tot} to zero. The result is

$$\Delta B = \left[\frac{\rho \lambda^2 I^2}{2K_u} \frac{(MLT)}{W_A A_c^2 \ell_m} \frac{1}{\beta K_{fe}} \right]^{\left(\frac{1}{\beta+2}\right)} \tag{15.56}$$

which is essentially the same as Eq. (15.13). The total power loss P_{tot} is evaluated at this value of ΔB, and the resulting expression is manipulated to find K_{gfe}. The result is

$$K_{gfe} \geq \frac{\rho \lambda^2 I^2 K_{fe}^{(2/\beta)}}{2K_u \left(P_{tot}\right)^{\left((\beta+2)/\beta\right)}} \tag{15.57}$$

where K_{gfe} is defined as in Eq. (15.16). A core that satisfies this inequality is selected.

15.4.2 Step-by-step AC Inductor Design Procedure

The units of Section 15.2 are employed here.

1. *Determine core size.*

$$K_{gfe} \geq \frac{\rho \lambda^2 I^2 K_{fe}^{(2/\beta)}}{2K_u \left(P_{tot}\right)^{\left((\beta+2)/\beta\right)}} 10^8 \tag{15.58}$$

Choose a core that is large enough to satisfy this inequality. If necessary, it may be possible to use a smaller core by choosing a core material having lower loss, that is, smaller K_{fe}.

2. *Evaluate peak ac flux density.*

$$\Delta B = \left[10^8 \frac{\rho \lambda^2 I^2}{2K_u} \frac{(MLT)}{W_A A_c^3 \ell_m} \frac{1}{\beta K_{fe}} \right]^{\left(\frac{1}{\beta+2}\right)} \tag{15.59}$$

3. *Number of turns.*

$$n = \frac{\lambda}{2\Delta B A_c} 10^4 \tag{15.60}$$

4. *Air gap length.*

$$\ell_g = \frac{\mu_0 A_c n^2}{L} 10^{-4} \tag{15.61}$$

with A_c specified in cm^2 and ℓ_g expressed in meters. Alternatively, the air gap can be indirectly expressed via A_L (mH/1000 turns):

$$A_L = \frac{L}{n^2} 10^9 \tag{15.62}$$

5. *Check for saturation.*

If the inductor current contains a dc component I_{dc}, then the maximum total flux density B_{max} is greater than the peak ac flux density ΔB. The maximum total flux density, in Tesla, is given by

$$B_{max} = \Delta B + \frac{LI_{dc}}{nA_c} 10^4 \tag{15.63}$$

If B_{max} is close to or greater than the saturation flux density B_{sat}, then the core may saturate. The filter inductor design procedure of the previous chapter should then be used, to operate at a lower flux density.

6. *Evaluate wire size.*

$$A_w \leq \frac{K_u W_A}{n} \tag{15.64}$$

A winding geometry can now be determined, and copper losses due to the proximity effect can be evaluated. If these losses are significant, it may be desirable to further optimize the design by reiterating the above steps, accounting for proximity losses by increasing the effective wire resistivity to the value $\rho_{eff} = \rho_{cu} P_{cu} / P_{dc}$, where P_{cu} is the actual copper loss including proximity effects, and P_{dc} is the copper loss predicted when the proximity effect is ignored.

7. *Check power loss.*

$$\begin{aligned} P_{cu} &= \frac{\rho n (MLT)}{A_w} I^2 \\ P_{fe} &= K_{fe} (\Delta B)^{\beta} A_c \ell_m \\ P_{tot} &= P_{cu} + P_{fe} \end{aligned} \tag{15.65}$$

15.5 SUMMARY

1. In a multiple-winding transformer, the low-frequency copper losses are minimized when the available window area is allocated to the windings according to their apparent powers, or ampere-turns.
2. As peak ac flux density is increased, core loss increases while copper losses decrease. There is an optimum flux density that leads to minimum total power loss. Provided that the core material is operated near its intended frequency, then the optimum flux density is less than the saturation flux density. Minimization of total loss then determines the choice of peak ac flux density.
3. The core geometrical constant K_{gfe} is a measure of the magnetic size of a core, for applications in which core loss is significant. In the K_{gfe} design method, the peak flux density is optimized to yield minimum total loss, as opposed to the K_g design method where peak flux density is a given specification.

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PROBLEMS

15.1 Forward converter inductor and transformer design. The objective of this problem set is to design the magnetics (two inductors and one transformer) of the two-transistor, two-output forward converter shown in Fig. 15.11. The ferrite core material to be used for all three devices has a saturation flux density of approximately 0.3 T at 120°C. To provide a safety margin for your designs, you should use a maximum flux density B_{max} that is no greater than 75% of this value. The core loss at 100 kHz is described by Eq. (15.1), with the parameter values $\beta = 2.6$ and $K_{fe} = 50$ W/T$^{\beta}$ cm^3. Calculate copper loss at 100°C.

Steady-state converter analysis and design. You may assume 100% efficiency and ideal lossless components for this section.

(a) Select the transformer turns ratios so that the desired output voltages are obtained when the duty cycle is $D = 0.4$.

(b) Specify values of L_1 and L_2 such that their current ripples Δi_1 and Δi_2 are 10% of their respective full-load current dc components I_1 and I_2.

(c) Determine the peak and rms currents in each inductor and transformer winding.

Inductor design. Allow copper loss of 1 W in L_1 and 0.4 W in L_2. Assume a fill factor of $K_u = 0.5$. Use ferrite EE cores—tables of geometrical data for standard EE core sizes are given in Appendix D. Design the output filter inductors L_1 and L_2. For each inductor, specify:

(*i*) EE core size

(*ii*) Air gap length

(*iii*) Number of turns

(*iv*) AWG wire size

Transformer design. Allow a total power loss of 1 W. Assume a fill factor of $K_u = 0.35$ (lower than for the filter inductors, to allow space for insulation between the windings). Use a ferrite EE core. You may neglect losses due to the skin and proximity effects, but you should include core and copper losses. Design the transformer, and specify the following:

(*i*) EE core size

(*ii*) Turns n_1, n_2, and n_3

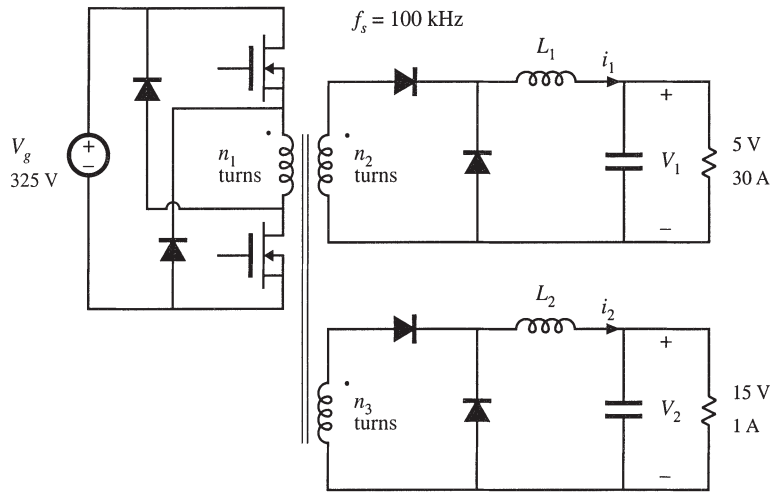


Fig. 15.11 Two-output forward converter of Problem 15.1.

(*iii*) AWG wire size for the three windings

Check your transformer design:

(*iv*) Compute the maximum flux density. Will the core saturate?

(*v*) Compute the core loss, the copper loss of each winding, and the total power loss

15.2 A single-transistor forward converter operates with an input voltage V_g = 160 V, and supplies two outputs: 24 V at 2 A, and 15 V at 6 A. The duty cycle is D = 0.4. The turns ratio between the primary winding and the reset winding is 1:1. The switching frequency is 100 kHz. The core material loss equation parameters are β = 2.7, K_{fe} = 50. You may assume a fill factor of 0.25. Do not allow the core maximum flux density to exceed 0.3 T.

Design a transformer for this application, having a total power loss no greater than 1.5 W at 100°C. Neglect proximity losses. You may neglect the reset winding. Use a ferrite PQ core. Specify: core size, peak ac flux density, wire sizes, and number of turns for each winding. Compute the core and copper losses for your design.

15.3 Flyback/SEPIC transformer design. The "transformer" of the flyback and SEPIC converters is an energy storage device, which might be more accurately described as a multiple-winding inductor. The magnetizing inductance L_p functions as an energy-transferring inductor of the converter, and therefore the "transformer" normally contains an air gap. The converter may be designed to operate in either the continuous or discontinuous conduction mode. Core loss may be significant. It is also important to ensure that the peak current in the magnetizing inductance does not cause saturation.

A flyback transformer is to be designed for the following two-output flyback converter application:

Input:	160 Vdc
Output 1:	5 Vdc at 10 A
Output 2:	15 Vdc at 1 A
Switching frequency:	100 kHz
Magnetizing inductance L_p:	1.33 mH, referred to primary
Turns ratio:	160:5:15
Transformer power loss:	Allow 1 W total

(a) Does the converter operate in CCM or DCM? Referred to the primary winding, how large are (*i*) the magnetizing current ripple Δi, (*ii*) the magnetizing current dc component I, and (*iii*) the peak magnetizing current I_{pk}?

(b) Determine (*i*) the rms winding currents, and (*ii*) the applied primary volt-seconds λ_1. Is λ_1 proportional to I_{pk}?

(c) Modify the transformer and ac inductor design procedures of this chapter, to derive a general procedure for designing flyback transformers that explicitly accounts for both core and copper loss, and that employs the optimum ac flux density that minimizes the total loss.

(d) Give a general step-by-step design procedure, with all specifications and units clearly stated.

(e) Design the flyback transformer for the converter of part (a), using your step-by-step procedure of part (d). Use a ferrite EE core, with β = 2.7 and K_{fe} = 50 W/T$^{\beta}$cm^3. Specify: core size, air gap length, turns, and wire sizes for all windings.

(f) For your final design of part (e), what are (*i*) the core loss, (*ii*) the total copper loss, and (*iii*) the peak flux density?

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15.4 Over the intended range of operating frequencies, the frequency dependence of the core-loss coefficient K_{fe} of a certain ferrite core material can be approximated using a monotonically increasing fourth-order polynomial of the form

$$K_{fe}(f) = K_{fe0}\left(1 + a_1\left(\frac{f}{f_0}\right) + a_2\left(\frac{f}{f_0}\right)^2 + a_3\left(\frac{f}{f_0}\right)^3 + a_4\left(\frac{f}{f_0}\right)^4\right)$$

where K_{fe0}, a_1, a_2, a_3, a_4, and f_0 are constants. In a typical converter transformer application, the applied primary volt-seconds λ_1 varies directly with the switching period $T_s = 1/f$. It is desired to choose the optimum switching frequency such that K_{gfe}, and therefore the transformer size, are minimized.

(a) Show that the optimum switching frequency is a root of the polynomial

$$1 + a_1\left(\frac{\beta-1}{\beta}\right)\left(\frac{f}{f_0}\right) + a_2\left(\frac{\beta-2}{\beta}\right)\left(\frac{f}{f_0}\right)^2 + a_3\left(\frac{\beta-3}{\beta}\right)\left(\frac{f}{f_0}\right)^3 + a_4\left(\frac{\beta-4}{\beta}\right)\left(\frac{f}{f_0}\right)^4$$

Next, a core material is chosen whose core loss parameters are

$\beta = 2.7$	$K_{fe0} = 7.6$
$f_0 = 100$ kHz	
$a_1 = -1.3$	$a_2 = 5.3$
$a_3 = -0.5$	$a_4 = 0.075$

The polynomial fits the manufacturer's published data over the range 10 kHz $< f <$ 1 MHz.

(b) Sketch K_{fe} vs. f.

(c) Determine the value of f that minimizes K_{gfe}.

(d) Sketch $K_{gfe}(f)/K_{gfe}(100\text{ kHz})$, over the range 100 kHz $\le f \le$ 1 MHz. How sensitive is the transformer size to the choice of switching frequency?

15.5 Transformer design to attain a given temperature rise. The temperature rise ΔT of the center leg of a ferrite core is directly proportional to the total power loss P_{tot} of a transformer: $\Delta T = R_{th} P_{tot}$, where R_{th} is the thermal resistance of the transformer under given environmental conditions. You may assume that this temperature rise has minimal dependence on the distribution of losses within the transformer. It is desired to modify the K_{gfe} transformer design method, such that temperature rise ΔT replaces total power loss P_{tot} as a specification. You may neglect the dependence of the wire resistivity ρ on temperature.

(a) Modify the n-winding transformer K_{gfe} design method, as necessary. Define a new core geometrical constant K_{th} that includes R_{th}.

(b) Thermal resistances of ferrite EC cores are listed in Section D.3 of Appendix D. Tabulate K_{th} for these cores, using $\beta = 2.7$.

(c) A 750 W single-output full-bridge isolated buck dc-dc converter operates with converter switching frequency f_s = 200 kHz, dc input voltage V_g = 400 V, and dc output voltage V = 48 V. The turns ratio is 6:1. The core loss equation parameters at 100 kHz are K_{fe} = 10 W/T$^{\beta}$cm^3 and $\beta = 2.7$. Assume a fill factor of $K_u = 0.3$. You may neglect proximity losses. Use your design procedure of parts (a) and (b) to design a transformer for this application, in which the temperature rise is limited to 20°C. Specify: EC core size, primary and secondary turns, wire sizes, and peak ac flux density.

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Part IV

Modern Rectifiers
and Power System Harmonics

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16

Power and Harmonics in Nonsinusoidal Systems

Rectification used to be a much simpler topic. A textbook could cover the topic simply by discussing the various circuits, such as the peak-detection and inductor-input rectifiers, the phase-controlled bridge, polyphase transformer connections, and perhaps multiplier circuits. But recently, rectifiers have become much more sophisticated, and are now systems rather than mere circuits. They often include pulse-width modulated converters such as the boost converter, with control systems that regulate the ac input current waveform. So modern rectifier technology now incorporates many of the dc–dc converter fundamentals.

The reason for this is the undesirable ac line current harmonics, and low power factors, of conventional peak-detection and phase-controlled rectifiers. The adverse effects of power system harmonics are well recognized. These effects include: unsafe neutral current magnitudes in three-phase systems, heating and reduction of life in transformers and induction motors, degradation of system voltage waveforms, unsafe currents in power-factor-correction capacitors, and malfunctioning of certain power system protection elements. In a real sense, conventional rectifiers are harmonic polluters of the ac power distribution system. With the widespread deployment of electronic equipment in our society, rectifier harmonics have become a significant and measurable problem. Thus there is a need for *high-quality rectifiers*, which operate with high power factor, high efficiency, and reduced generation of harmonics. Several international standards now exist that specifically limit the magnitudes of harmonic currents, for both high-power equipment such as industrial motor drives, and low-power equipment such as electronic ballasts for fluorescent lamps and power supplies for office equipment.

This chapter treats the flow of energy in power systems containing nonsinusoidal waveforms. Average power, rms values, and power factor are expressed in terms of the Fourier series of the voltage and current waveforms. Harmonic currents in three-phase systems are discussed, and present-day standards are listed. The following chapters treat harmonics and harmonic mitigation in conventional line-commutated rectifiers, high-quality rectifier circuits and their models, and control of high-quality rectifiers.

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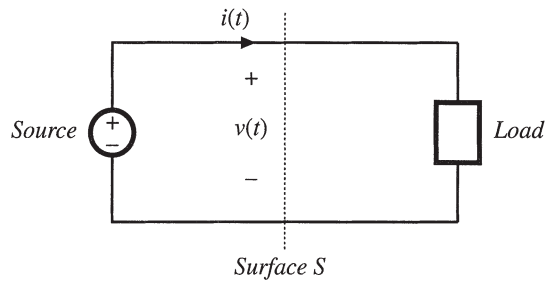


Fig. 16.1 Observe the transmission of energy through surface *S*.

16.1 AVERAGE POWER

Let us consider the transmission of energy from a source to a load, through a given surface as in Fig. 16.1. In the network of Fig. 16.1, the voltage waveform $v(t)$ (not necessarily sinusoidal) is given by the source, and the current waveform is determined by the response of the load. In the more general case in which the source output impedance is significant, then $v(t)$ and $i(t)$ both depend on the characteristics of the source and load. Balanced three-phase systems may be treated in the same manner, on a per-phase basis, using a line current and line-to-neutral voltage.

If $v(t)$ and $i(t)$ are periodic, then they may be expressed as Fourier series:

$$\begin{aligned} v(t) &= V_0 + \sum_{n=1}^{\infty} V_n \cos\left(n\omega t - \varphi_n\right) \\ i(t) &= I_0 + \sum_{n=1}^{\infty} I_n \cos\left(n\omega t - \theta_n\right) \end{aligned} \tag{16.1}$$

where the period of the ac line voltage waveform is defined as $T = 2\pi/\omega$. In general, the instantaneous power $p(t) = v(t)i(t)$ can assume both positive and negative values at various points during the ac line cycle. Energy then flows in both directions between the source and load. It is of interest to determine the net energy transmitted to the load over one cycle, or

$$W_{cycle} = \int_0^T v(t)i(t)dt \tag{16.2}$$

This is directly related to the average power as follows:

$$P_{av} = \frac{W_{cycle}}{T} = \frac{1}{T}\int_0^T v(t)i(t)dt \tag{16.3}$$

Let us investigate the relationship between the harmonic content of the voltage and current waveforms, and the average power. Substitution of the Fourier series, Eq. (16.1), into Eq. (16.3) yields

$$P_{av} = \frac{1}{T}\int_0^T \left(V_0 + \sum_{n=1}^{\infty} V_n \cos\left(n\omega t - \varphi_n\right)\right)\left(I_0 + \sum_{n=1}^{\infty} I_n \cos\left(n\omega t - \theta_n\right)\right)dt \tag{16.4}$$

To evaluate this integral, we must multiply out the infinite series. It can be shown that the integrals of

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cross-product terms are zero, and the only contributions to the integral comes from the products of voltage and current harmonics of the same frequency:

$$\int_0^T \Big(V_n \cos\big(n\omega t - \varphi_n\big)\Big)\Big(I_m \cos\big(m\omega t - \theta_m\big)\Big)dt = \begin{cases} 0 & \text{if } n \neq m \\ \dfrac{V_n I_n}{2} \cos\big(\varphi_n - \theta_n\big) & \text{if } n = m \end{cases} \tag{16.5}$$

The average power is therefore

$$P_{av} = V_0 I_0 + \sum_{n=1}^{\infty} \frac{V_n I_n}{2} \cos\big(\varphi_n - \theta_n\big) \tag{16.6}$$

So net energy is transmitted to the load only when the Fourier series of $v(t)$ and $i(t)$ contain terms at the same frequency. For example, if $v(t)$ and $i(t)$ both contain third harmonic, then net energy is transmitted at the third harmonic frequency, with average power equal to

$$\frac{V_3 I_3}{2} \cos\big(\varphi_3 - \theta_3\big) \tag{16.7}$$

Here, $V_3 I_3/2$ is equal to the rms volt-amperes of the third harmonic current and voltage. The cos $(\phi_3 - \theta_3)$ term is a displacement term which accounts for the phase difference between the third harmonic voltage and current.

Some examples of power flow in systems containing harmonics are illustrated in Figs. 16.2 to 16.4. In example 1, Fig. 16.2, the voltage contains fundamental only, while the current contains third har-

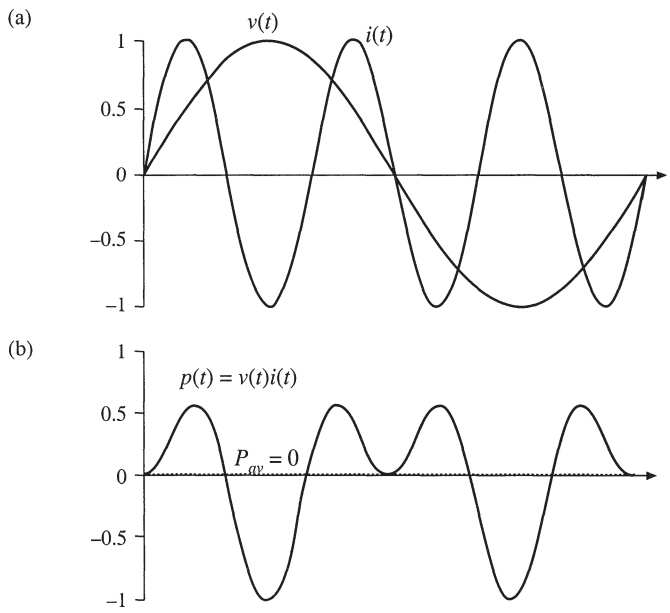


Fig. 16.2 Voltage, current, and instantaneous power waveforms, example 1. The voltage contains only fundamental, and the current contains only third harmonic. The average power is zero.

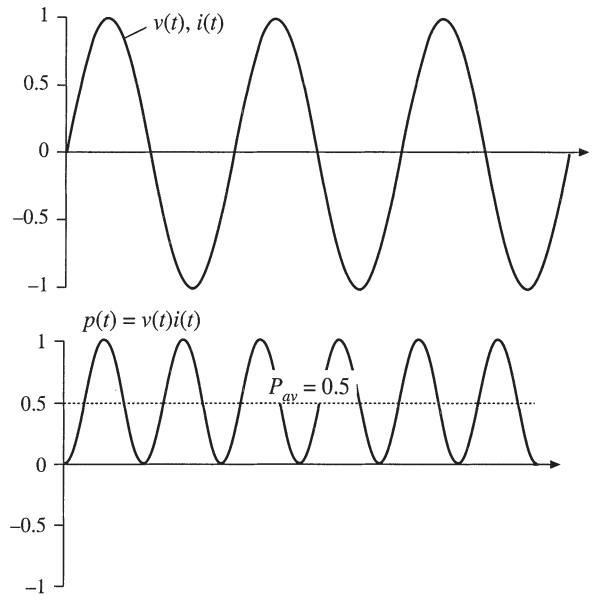


Fig. 16.3 Voltage, current, and instantaneous power waveforms, example 2. The voltage and current each contain only third harmonic, and are in phase. Net energy is transmitted at the third harmonic frequency.

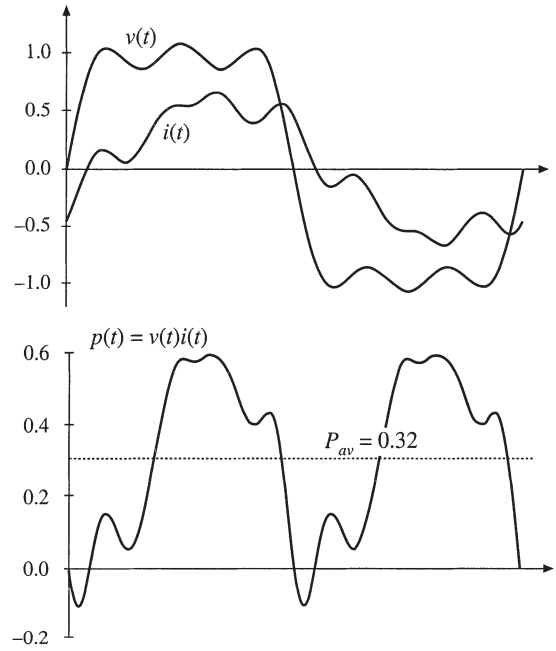


Fig. 16.4 Voltage, current, and instantaneous power waveforms, example 3. The voltage contains fundamental, third, and fifth harmonics. The current contains fundamental, fifth, and seventh harmonics. Net energy is transmitted at the fundamental and fifth harmonic frequencies.

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monic only. It can be seen that the instantaneous power waveform $p(t)$ has a zero average value, and hence P_{av} is zero. Energy circulates between the source and load, but over one cycle the net energy transferred to the load is zero. In example 2, Fig. 16.3, the voltage and current each contain only third harmonic. The average power is given by Eq. (16.7) in this case.

In example 3, Fig. 16.4, the voltage waveform contains fundamental, third harmonic, and fifth harmonic, while the current contains fundamental, fifth harmonic, and seventh harmonic, as follows:

$$\begin{aligned} v(t) &= 1.2\cos(\omega t) + 0.33\cos(3\omega t) + 0.2\cos(5\omega t) \\ i(t) &= 0.6\cos(\omega t + 30°) + 0.1\cos(5\omega t + 45°) + 0.1\cos(7\omega t + 60°) \end{aligned} \tag{16.8}$$

Average power is transmitted at the fundamental and fifth harmonic frequencies, since only these frequencies are present in both waveforms. The average power is found by evaluation of Eq. (16.6); all terms are zero except for the fundamental and fifth harmonic terms, as follows:

$$P_{av} = \frac{(1.2)(0.6)}{2}\cos(30°) + \frac{(0.2)(0.1)}{2}\cos(45°) = 0.32 \tag{16.9}$$

The instantaneous power and its average are illustrated in Fig. 16.4(b).

16.2 ROOT-MEAN-SQUARE (RMS) VALUE OF A WAVEFORM

The rms value of a periodic waveform $v(t)$ with period T is defined as

$$(\text{rms value}) = \sqrt{\frac{1}{T}\int_0^T v^2(t)\,dt} \tag{16.10}$$

The rms value can also be expressed in terms of the Fourier components. Insertion of Eq. (16.1) into Eq. (16.10), and simplification using Eq. (16.5), yields

$$(\text{rms value}) = \sqrt{V_0^2 + \sum_{n=1}^{\infty}\frac{V_n^2}{2}} \tag{16.11}$$

Again, the integrals of the cross-product terms are zero. This expression holds when the waveform is a current:

$$(\text{rms current}) = \sqrt{I_0^2 + \sum_{n=1}^{\infty}\frac{I_n^2}{2}} \tag{16.12}$$

Thus, the presence of harmonics in a waveform always increases its rms value. In particular, in the case where the voltage $v(t)$ contains only fundamental while the current $i(t)$ contains harmonics, then the harmonics increase the rms value of the current while leaving the average power unchanged. This is undesirable, because the harmonics do not lead to net delivery of energy to the load, yet they increase the $I_{rms}{}^2R$ losses in the system.

In a practical system, series resistances always exist in the source, load, and/or transmission wires, which lead to unwanted power losses obeying the expression

$$(\text{rms current})^2 R_{series} \tag{16.13}$$

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Examples of such loss elements are the resistance of ac generator windings, the resistance of the wire connecting the source and load, the resistance of transformer windings, and the resistance of semiconductor devices and magnetics windings in switching converters. Thus, it is desired to make the rms current as small as possible, while transferring the required amount of energy and average power to the load.

Shunt resistances usually also exist, which cause power loss according to the relation

$$\frac{(\text{rms voltage})^2}{R_{shunt}} \tag{16.14}$$

Examples include the core losses in transformers and ac generators, and switching converter transistor switching loss. Therefore, it is desired to also make the rms voltage as small as possible while transferring the required average power to the load.

16.3 POWER FACTOR

Power factor is a figure of merit that measures how effectively energy is transmitted between a source and load network. It is measured at a given surface as in Fig. 16.1, and is defined as

$$\text{power factor} = \frac{(\text{average power})}{(\text{rms voltage})\,(\text{rms current})} \tag{16.15}$$

The power factor always has a value between zero and one. The ideal case, unity power factor, occurs for a load that obeys Ohm's Law. In this case, the voltage and current waveforms have the same shape, contain the same harmonic spectrum, and are in phase. For a given average power throughput, the rms current and voltage are minimized at maximum (unity) power factor, that is, with a linear resistive load. In the case where the voltage contains no harmonics but the load is nonlinear and contains dynamics, then the power factor can be expressed as a product of two terms, one resulting from the phase shift of the fundamental component of the current, and the other resulting from the current harmonics.

16.3.1 Linear Resistive Load, Nonsinusoidal Voltage

In this case, the current harmonics are in phase with, and proportional to, the voltage harmonics. As a result, all harmonics result in the net transfer of energy to the load. The current harmonic magnitudes and phases are

$$I_n = \frac{V_n}{R} \tag{16.16}$$

$$\theta_n = \varphi_n \qquad \text{so} \quad \cos(\theta_n - \varphi_n) = 1 \tag{16.17}$$

The rms voltage is again

$$(\text{rms voltage}) = \sqrt{V_0^2 + \sum_{n=1}^{\infty} \frac{V_n^2}{2}} \tag{16.18}$$

and the rms current is

$$\begin{aligned}(\text{rms current}) &= \sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}} = \sqrt{\frac{V_0^2}{R^2} + \sum_{n=1}^{\infty} \frac{V_n^2}{2R^2}} \\ &= \frac{1}{R}(\text{rms voltage})\end{aligned} \tag{16.19}$$

By use of Eq. (16.6), the average power is

$$\begin{aligned}P_{av} &= V_0 I_0 + \sum_{n=1}^{\infty} \frac{V_n I_n}{2} \cos(\varphi_n - \theta_n) \\ &= \frac{V_0^2}{R} + \sum_{n=1}^{\infty} \frac{V_n^2}{2R} \\ &= \frac{1}{R}(\text{rms voltage})^2\end{aligned} \tag{16.20}$$

Insertion of Eqs. (16.19) and (16.20) into Eq. (16.15) then shows that the power factor is unity. Thus, if the load is linear and purely resistive, then the power factor is unity regardless of the harmonic content of $v(t)$. The harmonic content of the load current waveform $i(t)$ is identical to that of $v(t)$, and all harmonics result in the transfer of energy to the load. This raises the possibility that one could construct a power distribution system based on nonsinusoidal waveforms in which the energy is efficiently transferred to the load.

16.3.2 Nonlinear Dynamical Load, Sinusoidal Voltage

If the voltage $v(t)$ contains a fundamental component but no dc component or harmonics, so that $V_0 = V_2 = V_3 = \ldots = 0$, then harmonics in $i(t)$ do not result in transmission of net energy to the load. The average power expression, Eq. (16.6), becomes

$$P_{av} = \frac{V_1 I_1}{2} \cos(\varphi_1 - \theta_1) \tag{16.21}$$

However, the harmonics in $i(t)$ do affect the value of the rms current:

$$(\text{rms current}) = \sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}} \tag{16.22}$$

Hence, as in example 1 (Fig. 16.2), harmonics cause the load to draw more rms current from the source, but not more average power. Increasing the current harmonics does not cause more energy to be transferred to the load, but does cause additional losses in series resistive elements R_{series}.

Also, the presence of load dynamics and reactive elements, which causes the phase of the fundamental components of the voltage and current to differ $(\theta_1 - \varphi_1)$, also reduces the power factor. The $\cos(\varphi_1 - \theta_1)$ term in the average power Eq. (16.21) becomes less than unity. However, the rms value of the current, Eq. (16.22), does not depend on the phase. So shifting the phase of $i(t)$ with respect to $v(t)$ reduces the average power without changing the rms voltage or current, and hence the power factor is reduced.

By substituting Eqs. (16.21) and (16.22) into (16.15), we can express the power factor for the sinusoidal voltage in the following form:

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$$\text{(power factor)} = \left(\frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}}} \right) \left(\cos\left(\varphi_1 - \theta_1\right) \right) \tag{16.23}$$

$$= \text{(distortion factor) (displacement factor)}$$

So when the voltage contains no harmonics, then the power factor can be written as the product of two terms. The first, called the *distortion factor*, is the ratio of the rms fundamental component of the current to the total rms value of the current

$$\text{(distortion factor)} = \left(\frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}}} \right) = \frac{\text{(rms fundamental current)}}{\text{(rms current)}} \tag{16.24}$$

The second term of Eq. (16.23) is called the *displacement factor*, and is the cosine of the angle between the fundamental components of the voltage and current waveforms.

The *Total Harmonic Distortion* (THD) is defined as the ratio of the rms value of the waveform not including the fundamental, to the rms fundamental magnitude. When no dc is present, this can be written:

$$\text{(THD)} = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \tag{16.25}$$

The total harmonic distortion and the distortion factor are closely related. Comparison of Eqs. (16.24) and (16.25), with $I_0 = 0$, leads to

$$\text{(distortion factor)} = \frac{1}{\sqrt{1 + (\text{THD})^2}} \tag{16.26}$$

This equation is plotted in Fig. 16.5. The distortion factor of a waveform with a moderate amount of distortion is quite close to unity. For example, if the waveform contains third harmonic whose magnitude is

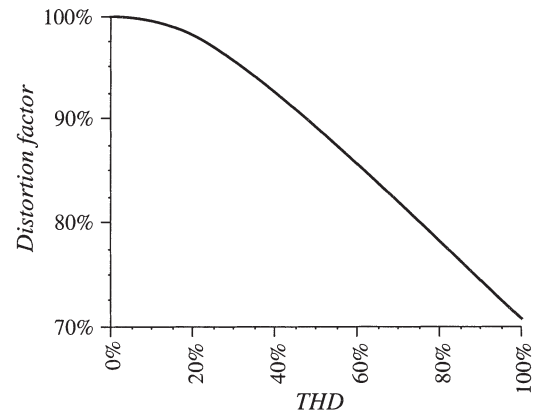


Fig. 16.5 Distortion factor vs. total harmonic distortion.

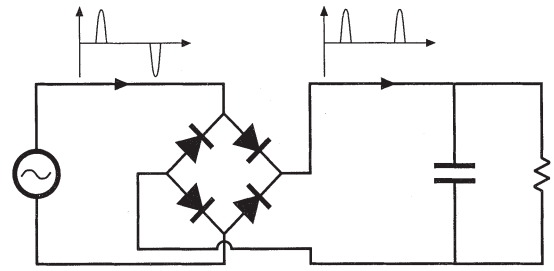


Fig. 16.6 Conventional peak detection rectifier.

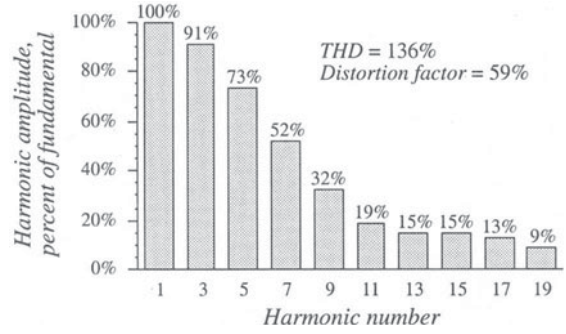


Fig. 16.7 Typical ac line current spectrum of a peak detection rectifier. Harmonics 1 to 19 are shown.

10% of the fundamental, the distortion factor is 99.5%. Increasing the third harmonic to 20% decreases the distortion factor to 98%, and a 33% harmonic magnitude yields a distortion factor of 95%. So the power factor is not significantly degraded by the presence of harmonics unless the harmonics are quite large in magnitude.

An example of a case in which the distortion factor is much less than unity is the conventional peak detection rectifier of Fig. 16.6. In this circuit, the ac line current consists of short-duration current pulses occurring at the peak of the voltage waveform. The fundamental component of the line current is essentially in phase with the voltage, and the displacement factor is close to unity. However, the low-order current harmonics are quite large, close in magnitude to that of the fundamental—a typical current spectrum is given in Fig. 16.7. The distortion factor of peak detection rectifiers is usually in the range 55% to 65%. The resulting power factor is similar in value.

In North America, the standard 120 V power outlet is protected by a 15 A circuit breaker. In consequence, the available load power quite limited. Derating the circuit breaker current by 20%, assuming typical efficiencies for the dc–dc converter and peak detection rectifier, and with a power factor of 55%, one obtains the following estimate for the maximum available dc load power:

$$\begin{aligned}&\text{(ac voltage) (derated breaker current) (power factor) (rectifier efficiency)}\\ &= (120\text{ V}) \quad (80\%\text{ of }15\text{ A}) \quad (0.55) \quad (0.98)\\ &= 776\text{ W}\end{aligned} \tag{16.27}$$

The less-than-unity efficiency of a dc–dc converter would further reduce the available dc load power. Using a peak detection rectifier to supply a load power greater than this requires that the user install higher amperage and/or higher voltage service, which is inconvenient and costly. The use of a rectifier

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circuit having nearly unity power factor would allow a significant increase in available dc load power:

$$\begin{aligned}&\text{(ac voltage) (derated breaker current) (power factor) (rectifier efficiency)}\\&= (120\text{ V}) \quad (80\%\text{ of }15\text{ A}) \quad (0.99) \quad (0.93)\\&= 1325\text{ W}\end{aligned} \tag{16.28}$$

or almost twice the available power of the peak detection rectifier. This alone can be a compelling reason to employ high quality rectifiers in commercial systems.

16.4 POWER PHASORS IN SINUSOIDAL SYSTEMS

The apparent power is defined as the product of the rms voltage and rms current. Apparent power is easily measured—it is simply the product of the readings of a voltmeter and ammeter placed in the circuit at the given surface. Many power system elements, such as transformers, must be rated according to the apparent power that they are able to supply. The unit of apparent power is the volt-ampere, or VA. The power factor, defined in Eq. (16.15), is the ratio of average power to apparent power.

In the case of sinusoidal voltage and current waveforms, we can additionally define the *complex power* $\boldsymbol{S}$ and the *reactive power* $\boldsymbol{Q}$. If the sinusoidal voltage $v(t)$ and current $i(t)$ can be represented by the phasors $\boldsymbol{V}$ and $\boldsymbol{I}$, then the complex power is a phasor defined as

$$\boldsymbol{S} = \boldsymbol{V}\boldsymbol{I}^* = P + jQ \tag{16.29}$$

Here, $\boldsymbol{I}^*$ is the complex conjugate of $\boldsymbol{I}$, and j is the square root of -1. The magnitude of $\boldsymbol{S}$, or $\| \boldsymbol{S} \|$, is equal to the apparent power, measured in VA. The real part of $\boldsymbol{S}$ is the average power P, having units of watts. The imaginary part of $\boldsymbol{S}$ is the reactive power Q, having units of reactive volt-amperes, or VARs.

A phasor diagram illustrating $\boldsymbol{S}$, P, and Q, is given in Fig. 16.8. The angle $(\varphi_1 - \theta_1)$ is the angle between the voltage phasor $\boldsymbol{V}$ and the current phasor $\boldsymbol{I}$. $(\varphi_1 - \theta_1)$ is additionally the phase of the complex power $\boldsymbol{S}$. The power factor in the purely sinusoidal case is therefore

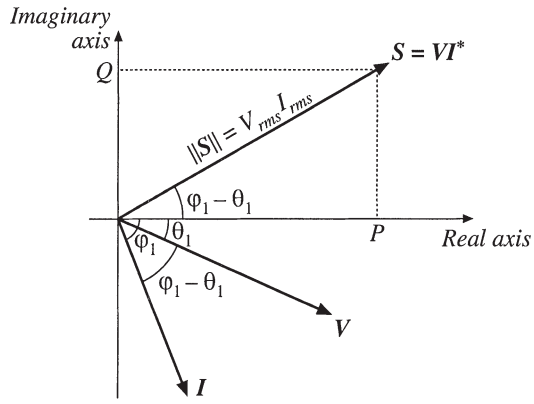


Fig. 16.8 Power phasor diagram, for a sinusoidal system, illustrating the voltage, current, and complex power phasors.

$$\text{power factor} = \frac{P}{\|S\|} = \cos\left(\varphi_1 - \theta_1\right) \tag{16.30}$$

It should be emphasized that this equation is valid only for systems in which the voltage and current are purely sinusoidal. The distortion factor of Eq. (16.24) then becomes unity, and the power factor is equal to the displacement factor as in Eq. (16.30).

The reactive power Q does not lead to net transmission of energy between the source and load. When reactive power is present, the rms current and apparent power are greater than the minimum amount necessary to transmit the average power P. In an inductor, the current lags the voltage by 90°, causing the displacement factor to be zero. The alternate storing and releasing of energy in an inductor leads to current flow and nonzero apparent power, but the average power P is zero. Just as resistors consume real (average) power P, inductors can be viewed as consumers of reactive power Q. In a capacitor, the current leads to voltage by 90°, again causing the displacement factor to be zero. Capacitors supply reactive power Q, and are commonly placed in the utility power distribution system near inductive loads. If the reactive power supplied by the capacitor is equal to the reactive power consumed by the inductor, then the net current (flowing from the source into the capacitor-inductive-load combination) will be in phase with the voltage, leading unity power factor and minimum rms current magnitude.

It will be seen in the next chapter that phase-controlled rectifiers produce a nonsinusoidal current waveform whose fundamental component lags the voltage. This lagging current does not arise from energy storage, but it does nonetheless lead to a reduced displacement factor, and to rms current and apparent power that are greater than the minimum amount necessary to transmit the average power.

16.5 HARMONIC CURRENTS IN THREE PHASE SYSTEMS

The presence of harmonic currents can also lead to some special problems in three-phase systems. In a four-wire three-phase system, harmonic currents can lead to large currents in the neutral conductors, which may easily exceed the conductor rms current rating. Power factor correction capacitors may experience significantly increased rms currents, causing them to fail. In this section, these problems are examined, and the properties of harmonic current flow in three-phase systems are derived.

16.5.1 Harmonic Currents in Three-Phase Four-Wire Networks

Let us consider the three-phase four-wire network of Fig. 16.9. In general, we can express the Fourier series of the line currents and line-neutral voltages as follows:

$$\begin{aligned} i_a(t) &= I_{a0} + \sum_{k=1}^{\infty} I_{ak} \cos\left(k\omega t - \theta_{ak}\right) \\ i_b(t) &= I_{b0} + \sum_{k=1}^{\infty} I_{bk} \cos\left(k(\omega t - 120°) - \theta_{bk}\right) \\ i_c(t) &= I_{c0} + \sum_{k=1}^{\infty} I_{ck} \cos\left(k(\omega t + 120°) - \theta_{ck}\right) \end{aligned} \tag{16.31}$$

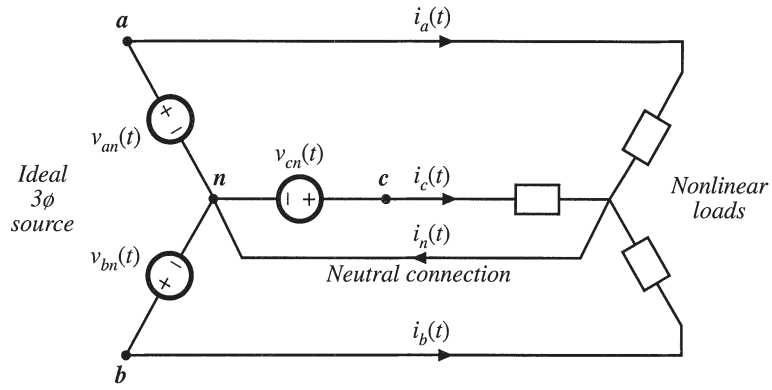


Fig. 16.9 Current flow in a three-phase four-wire network.

$$\begin{aligned} v_{an}(t) &= V_m \cos(\omega t) \\ v_{bn}(t) &= V_m \cos(\omega t - 120^\circ) \\ v_{cn}(t) &= V_m \cos(\omega t + 120^\circ) \end{aligned} \tag{16.32}$$

The neutral current is therefore $i_n = i_a + i_b + i_c$, or

$$\begin{aligned} i_n(t) &= I_{a0} + I_{b0} + I_{c0} + \\ &\sum_{k=1}^{\infty} \left[I_{ak} \cos(k\omega t - \theta_{ak}) + I_{bk} \cos(k(\omega t - 120^\circ) - \theta_{bk}) + I_{ck} \cos(k(\omega t + 120^\circ) - \theta_{ck}) \right] \end{aligned} \tag{16.33}$$

When the load is unbalanced (even though the voltages are balanced and undistorted), we can say little else about the neutral and line currents. If the load is unbalanced and nonlinear, then the line and neutral currents may contain harmonics of any order, including even and triplen harmonics.

Equation (16.33) is considerably simplified in the case where the loads are balanced. A balanced nonlinear load is one in which $I_{ak} = I_{bk} = I_{ck} = I_k$ and $\theta_{ak} = \theta_{bk} = \theta_{ck} = \theta_k$, for all k; that is, the harmonics of the three phases all have equal amplitudes and phase shifts. In this case, Eq. (16.33) reduces to

$$i_n(t) = 3I_0 + \sum_{k=3,6,9,\cdots}^{\infty} 3I_k \cos(k\omega t - \theta_k) \tag{16.34}$$

Hence, the fundamental and most of the harmonics cancel out, and do not appear in the neutral conductor. Thus, it is in the interests of the utility to balance their nonlinear loads as well as their harmonics.

But not all of the harmonics cancel out of Eq. (16.34): the dc and *triplen* (triple-*n*, or 3,6,9,...) harmonics add rather than cancel. The rms neutral current is

$$i_{n,\,rms} = 3\sqrt{I_0^2 + \sum_{k=3,6,9,\cdots}^{\infty} \frac{I_k^2}{2}} \tag{16.35}$$

Example

A balanced nonlinear load produces line currents containing fundamental and 20% third harmonic: $i_{an}(t) = I_1 \cos(\omega t - \theta_1) + 0.2I_1 \cos(3\omega t - \theta_3)$. Find the rms neutral current, and compare its amplitude to the rms line current amplitude.

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Solution:

$$i_{n,\,rms} = 3\sqrt{\frac{(0.2I_1)^2}{2}} = \frac{0.6\,I_1}{\sqrt{2}}$$
$$i_{1,\,rms} = \sqrt{\frac{I_1^2 + (0.2I_1)^2}{2}} = \frac{I_1}{\sqrt{2}}\sqrt{1 + 0.04} \approx \frac{I_1}{\sqrt{2}} \tag{16.36}$$

So the neutral current magnitude is 60% of the line current magnitude! The triplen harmonics in the three phases add, such that 20% third harmonic leads to 60% third harmonic neutral current. Yet the presence of the third harmonic has very little effect on the rms value of the line current. Significant unexpected neutral current flows.

16.5.2 Harmonic Currents in Three-Phase Three-Wire Networks

If there is no neutral connection to the wye-connected load, as in Fig. 16.10, then $i_n(t)$ must be zero. If the load is balanced, then Eq. (16.34) still applies, and therefore the dc and triplen harmonics of the load currents must be zero. Therefore, the line currents i_a, i_b, and i_c cannot contain triplen or dc harmonics. What happens is that a voltage is induced at the load neutral point n', containing dc and triplen harmonics, which eliminates the triplen and dc load current harmonics.

This result is true only when the load is balanced. With an unbalanced load, all harmonics can appear in the line currents, including triplen and dc. In practice, the load is never exactly balanced, and some small amounts of third harmonic line currents are measured.

With a delta-connected load as in Fig. 16.11, there is also no neutral connection, so the line currents cannot contain triplen or dc components. But the loads are connected line-to-line, and are excited by undistorted sinusoidal voltages. Hence triplen harmonic and dc currents do, in general, flow through the nonlinear loads. Therefore, these currents simply circulate around the delta. If the load is balanced, then again no triplen harmonics appear in the line currents.

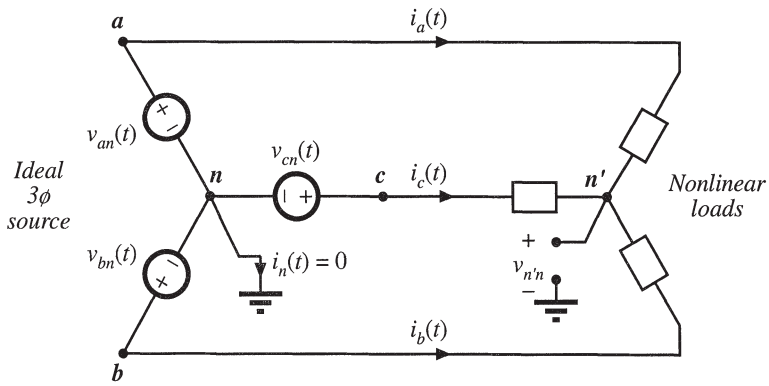


Fig. 16.10 Current flow in a three-phase three-wire wye-connected network.

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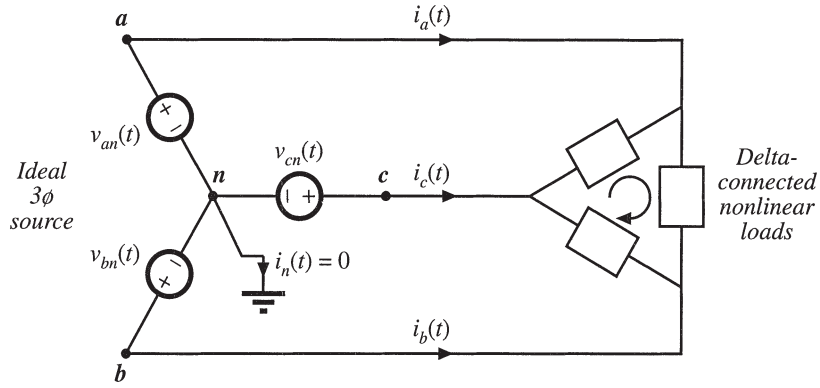


Fig. 16.11 A balanced nonlinear delta-connected load may generate triplen current harmonics. These harmonics circulate around the delta, but do not flow through the lines if the load is balanced.

16.5.3 Harmonic Current Flow in Power Factor Correction Capacitors

Harmonic currents tend to flow through shunt-connected power factor correction capacitors. To some extent, this is a good thing because the capacitors tend to low-pass filter the power system currents, and prevent nonlinear loads from polluting the entire power system. The flow of harmonic currents is then confined to the nonlinear load and local power factor correction capacitors, and voltage waveform distortion is reduced. High-frequency harmonic currents tend to flow through shunt capacitors because the capacitor impedance decreases with frequency, while the inductive impedance of transmission lines increases with frequency. In this sense, power factor correction capacitors mitigate the effects of harmonic currents arising from nonlinear loads in much the same way that they mitigate the effects of reactive currents that arise from inductive loads.

But the problem is that the power factor correction capacitors may not be rated to handle these harmonic currents, and hence there is a danger that the capacitors may overheat and fail when they are exposed to significant harmonic currents. The loss in capacitors is modeled using an *equivalent series resistance* (esr) as shown in Fig. 16.12. The esr models dielectric loss (hysteresis of the dielectric *D–E* loop), contact resistance, and foil and lead resistances. Power loss occurs, equal to $i_{rms}^2(esr)$. Dielectric materials are typically poor conductors of heat, so a moderate amount of power loss can cause a large temperature rise in the center of the capacitor. In consequence, the rms current must be limited to a safe value.

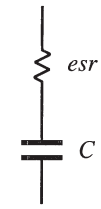


Fig. 16.12 Capacitor equivalent circuit. Losses are modeled by an equivalent series resistance (esr).

Typical power factor correction capacitors are rated by voltage *V*, frequency *f*, and reactive power in kVARs. These ratings are computed from the capacitance *C* and safe rms current I_{rms}, assuming undistorted sinusoidal waveforms, as follows:

$$\text{rated rms voltage } V_{rms} = \frac{I_{rms}}{2\pi f C} \tag{16.37}$$

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$$\text{rated reactive power} = \frac{I_{rms}^2}{2\pi f C} \tag{16.38}$$

In an undistorted system, the rms current, and hence also the capacitor esr loss, cannot increase unless the rms voltage is also increased. But high-frequency harmonics can lead to larger rms currents without an increased voltage. Any harmonics that flow result in increased rms current beyond the expected value predicted by Eq. (16.37). If the capacitor is not rated to handle additional power loss, then failure or premature aging can occur.

16.6 AC LINE CURRENT HARMONIC STANDARDS

Besides the increased currents and reduced power factors of peak detection rectifiers, the harmonics themselves can be detrimental: if large enough in magnitude, they can pollute the power system. Harmonic currents cause distortion of the voltage waveform via the power system series impedance. These voltage harmonics can interfere with the operation of nearby loads. As noted previously, increased currents in shunt capacitors, and increased losses in distribution transformers and ac machines, can lead to premature aging and failure of these devices. Odd triplen harmonics (triple-*n*: 3rd, 9th, 15th, etc.) lead to unexpectedly large neutral currents in three-phase systems. Harmonic currents can also excite system resonances some distance from their source, with results that are difficult to predict. For these reasons, a number of organizations have adopted standards that limit the magnitudes of the harmonic currents that a load is allowed to inject into the ac line. The US military was one of the early organizations to recognize these problems; the very strict 3% limit was initially adopted. The standards adopted by the IEC and IEEE are more recent, and are intended for conventional utility systems. A fourth example, not discussed here, is the telephone interference factor, which limits power distribution system harmonics in cases when telephone lines and power lines share the same poles.

16.6.1 International Electrotechnical Commission Standard 1000

This international agency adopted a first draft of their IEC 555 standard in 1982. It has since undergone a number of revisions, and has been superceded by IEC 1000 [7]. This standard is now enforced in Europe, making it a de facto standard for commercial equipment intended to be sold worldwide.

The IEC 1000-3-2 standard covers a number of different types of low power equipment, with differing harmonic limits. It specifically limits harmonics for equipment having an input current of up to 16 A, connected to 50 or 60 Hz, 220 V to 240 V single phase circuits (two or three wire), as well as 380 V to 415 V three phase (three or four wire) circuits. In a city environment such as a large building, a large fraction of the total power system load can be nonlinear. For example, a major portion of the electrical load in a building is comprised of fluorescent lights, which present a very nonlinear characteristic to the utility system. A modern office may also contain a large number of personal computers, printers, copiers, etc., each of which may employ peak detection rectifiers. Although each individual load is a negligible fraction of the total local load, these loads can collectively become significant.

The IEC 1000-3-2 standard defines several categories of equipment, each of which is covered by a different set of harmonic limits. As an example, Table 16.1 shows the harmonic limits for *Class A* equipment, which includes low harmonic rectifiers for computer and other office equipment.

The European norm EN 61000-3-2 defines similar limits.

Table 16.1 IEC 1000-3-2 Harmonic current limits, class A

Odd harmonics		Even harmonics	
Harmonic number	Maximum current	Harmonic number	Maximum current
3	2.30 A	2	1.08 A
5	1.14 A	4	0.43 A
7	0.77 A	6	0.30 A
9	0.40 A	$8 \le n \le 40$	$0.23\ \text{A} \cdot (8/n)$
11	0.33 A		
13	0.21 A		
$15 \le n \le 39$	$0.15\ \text{A} \cdot (15/n)$		

16.6.2 IEEE/ANSI Standard 519

In 1993, the IEEE published a revised draft standard limiting the amplitudes of current harmonics, *IEEE Guide for Harmonic Control and Reactive Compensation of Static Power Converters*. The harmonic limits are based on the ratio of the fundamental component of the load current I_L to the short circuit current at the point of common coupling (PCC) at the utility I_{sc}. Stricter limits are imposed on large loads than on small loads. The limits are similar in magnitude to IEC 1000, and cover high voltage loads (of much higher power) not addressed by IEC 1000. Enforcement of this standard is presently up to the local utility company.

The odd harmonic limits for general distribution systems at voltages of 120 V to 69 kV are listed in Table 16.2. The limits for even harmonics are 25% of the odd harmonic limits. Limits for general distribution systems at 69.001 kV to 161 kV are 50% of the values listed in Table 16.2. Dc current components and half-wave rectifiers are not allowed.

It is the responsibility of the power consumer to meet these current harmonic standards. Standard IEEE-519 also specifies maximum allowable voltage harmonics, listed in Table 16.3. It is the responsibility of the utility, or power supplier, to meet these limits. Both total harmonic distortion and maximum individual harmonic magnitudes are limited.

Table 16.2 IEEE-519 Maximum odd harmonic current limits for general distribution systems, 120 V to 69 kV

I_{sc}/I_L	$n < 11$	$11 \le n < 17$	$17 \le n < 23$	$23 \le n < 35$	$35 \le n$	THD
< 20	4.0%	2.0%	1.5%	0.6%	0.3%	5.0%
20-50	7.0%	3.5%	2.5%	1.0%	0.5%	8.0%
50-100	10.0%	4.5%	4.0%	1.5%	0.7%	12.0%
100-1000	12.0%	5.5%	5.0%	2.0%	1.0%	15.0%
> 1000	15.0%	7.0%	6.0%	2.5%	1.4%	20.0%

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Table 16.3 IEEE-519 Voltage distortion limits

Bus voltage at PCC	Individual harmonics	THD
69 kV and lower	3.0%	5.0%
69.001 kV to 161 kV	1.5%	2.5%
Above 161 kV	1.0%	1.5%

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PROBLEMS

16.1 Passive rectifier circuit. In the passive rectifier circuit of Fig. 16.13, L is very large, such that the inductor current $i(t)$ is essentially dc. All components are ideal.

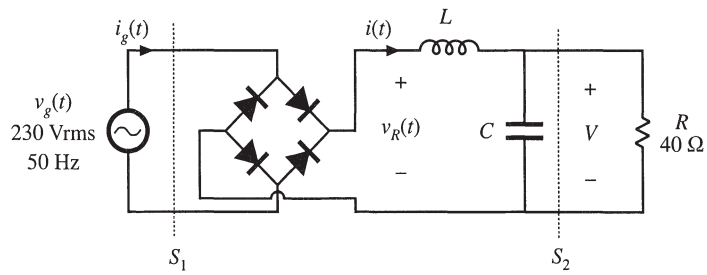


Fig. 16.13 Passive rectifier circuit of Problem 16.1

(a) Determine the dc output voltage, current, and power.

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(b) Sketch the ac line current waveform $i_g(t)$ and the rectifier output voltage waveform $v_R(t)$.

(c) Determine the ac line current rms magnitude, fundamental rms magnitude, and third harmonic rms magnitude. Does this rectifier network conform to the IEC-1000 harmonic current limits?

(d) Determine the power factor, measured at surfaces S_1 and S_2.

16.2 The three-phase rectifier of Fig. 16.14 is connected to a balanced 60 Hz 3øac 480 V (rms, line-line) sinusoidal source as shown. All elements are ideal. The inductance L is large, such that the current $i(t)$ is essentially constant, with negligible 360 Hz ripple.

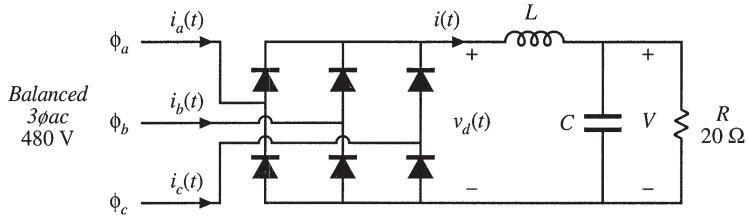


Fig. 16.14 Three-phase rectifier circuit of Problem 16.2

(a) Sketch the waveform $v_d(t)$.

(b) Determine the dc output voltage V.

(c) Sketch the line current waveforms $i_a(t)$, $i_b(t)$, and $i_c(t)$.

(d) Find the Fourier series of $i_a(t)$.

(e) Find the distortion factor, displacement factor, power factor, and line current THD.

16.3 Harmonic pollution police. In the network of Fig. 16.15, voltage harmonics are observed at the indicated surface. The object of this problem is to decide whether to blame the source or the load for the observed harmonic pollution. Either the source element or the load element contains a nonlinearity that generates harmonics, while the other element is linear.

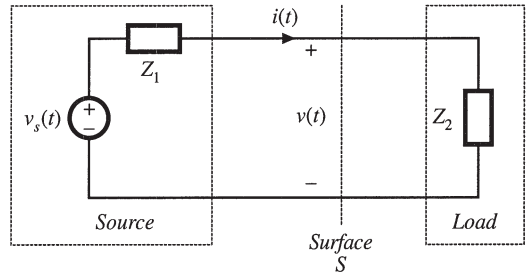


Fig. 16.15 Single-phase power system of Problems 16.3 to 16.5

(a) Consider first the case where the load is a passive linear impedance $Z_2(s)$, and hence its phase lies in the range $-90^\circ \le \angle Z_2(j\omega) \le +90^\circ$ for all positive ω. The source generates harmonics. Express the average power P in the form

$$P = \sum_{n=0}^{\infty} P_n$$

where P_n is the average power transmitted to the load by harmonic number n. What can you say about the polarities of the P_ns?

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(b) Consider next the case where the load is nonlinear, while the source is linear and can be modeled by a Thevenin-equivalent sinusoidal voltage source and linear impedance $Z_1(s)$. Again express the average power P as a sum of average powers, as in part (a). What can you say about the polarities of the P_ns in this case?

(c) The following Fourier series are measured:

Harmonic number	$v(t)$		$i(t)$	
	Magnitude	Phase	Magnitude	Phase
1	230 V	0°	6 A	– 20°
3	20 V	180°	4 A	20°
5	8 V	60°	1 A	– 110°

Who do you accuse? Explain your reasoning.

16.4 For the network and waveforms of Problem 16.3, determine the power factor at the indicated surface, and the average power flowing to the load. Harmonics higher in frequency than the fifth harmonic are negligible in magnitude.

16.5 Repeat Problem 16.3(c), using the following Fourier series:

Harmonic number	$v(t)$		$i(t)$	
	Magnitude	Phase	Magnitude	Phase
1	120 V	0°	5 A	25°
3	4 V	60°	0.5 A	40°
5	2 V	– 160°	0.2 A	– 100°

16.6 A balanced three-phase wye-connected load is constructed using a 20 Ω resistor in each phase. This load is connected to a balanced three-phase wye-connected voltage source, whose fundamental voltage component is 380 Vrms line-to-line. In addition, each (line-to-neutral) voltage source produces third and fifth harmonics. Each harmonic has amplitude 20 Vrms, and is in phase with the (line-to-neutral) fundamental.

(a) The source and load neutral points are connected, such that a four-wire system is obtained. Find the Fourier series of the line currents and the neutral current.

(b) The neutral connection is broken, such that a three-wire system is obtained. Find the Fourier series of the line currents. Also find the Fourier series of the voltage between the source and load neutral points.

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17

Line-Commutated Rectifiers

Conventional diode peak-detection rectifiers are inexpensive, reliable, and in widespread use. Their shortcomings are the high harmonic content of their ac line currents, and their low power factors. In this chapter, the basic operation and ac line current waveforms of several of the most common single-phase and three-phase diode rectifiers are summarized. Also introduced are phase-controlled three-phase rectifiers and inverters, and passive harmonic mitigation techniques. Several of the many references in this area are listed at the end of this chapter [1–15].

Rigorous analytical design of line-commutated rectifier and filter circuits is unfeasible for all but the simplest of circuits. Typical peak-detection rectifiers are numerically ill-conditioned, because small changes in the dc-side ripple voltage lead to large changes in the ac line current waveforms. Therefore, the discussions of this chapter are confined to mostly qualitative arguments, with the objective of giving the reader some insight into the physical operation of rectifier/filter circuits. Waveforms, harmonic magnitudes, and power factors are best determined by measurement or computer simulation.

17.1 THE SINGLE-PHASE FULL-WAVE RECTIFIER

A single-phase full-wave rectifier, with uncontrolled diode rectifiers, is shown in Fig. 17.1. The circuit includes a dc-side *L–C* filter. There are two conventional uses for this circuit. In the traditional full-wave rectifier, the output capacitor is large in value, and the dc output voltage $v(t)$ has negligible ripple at the second harmonic of the ac line frequency. Inductor L is most often small or absent. Additional small inductance may be in series with the ac source $v_g(t)$. A second conventional use of this circuit is in the low-harmonic rectifiers discussed in the next chapter. In this case, the resistive load is replaced by a dc-dc converter that is controlled such that its power input port obeys Ohm's law. For the purposes of understanding the rectifier waveforms, the converter can be modeled by an effective resistance R, as in the cir-

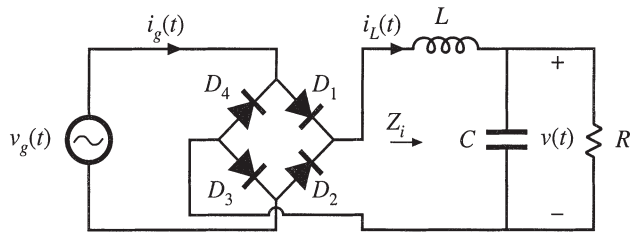


Fig. 17.1 Conventional single-phase full-wave rectifier, with dc-side *L–C* filter.

cuit of Fig. 17.1. In this application, the *L–C* filter is required to filter the conducted electromagnetic interference (EMI) generated by the converter. The inductor and capacitor element values are typically small in value, and $v(t)$ is approximately a rectified sinusoid. More generally, there may be several sections of *L–C* filter networks, connected to both the dc and ac sides of the diode rectifier, which filter EMI, smooth the dc output voltage, and reduce the ac line current harmonics.

The presence of any filter degrades the ac current waveform of the rectifier. With no reactive elements ($L = 0$ and $C = 0$), the rectifier presents a purely resistive load to the ac input. The output voltage $v(t)$ is then a rectified sinusoid, there are no ac line current harmonics, and the power factor is unity. Addition of reactive elements between the rectifier diodes and the load leads in general to ac line current harmonics. Given that such a filter is necessary, one might ask what can be done to keep these harmonics as small as possible. In this section, the dependence of the ac line current total harmonic distortion on the filter parameters is described.

The circuit of Fig. 17.1 generates odd harmonics of the ac line voltage in the ac line current. The dc output voltage contains dc and even harmonics of the ac line voltage. The circuit exhibits several modes of operation, depending on the relative values of L, C, and R. It is easiest to understand these modes by considering the limiting cases, as follows.

17.1.1 Continuous Conduction Mode

When the inductor L is very large, then the inductor current $i_L(t)$ is essentially constant. This follows from the inductor definition $v_L(t) = L di_L(t)/dt$. For a given applied inductor voltage waveform $v_L(t)$, the slope $di_L(t)/dt$ can be made arbitrarily small by making L sufficiently large. In the limiting case where L is infinite, the slope $di_L(t)/dt$ becomes zero, and the inductor current is constant dc. To provide a path for the constant inductor to flow, at least two of the rectifier diodes must conduct at any given instant in time. For the circuit of Fig. 17.1, diodes D_1 and D_3 conduct when the ac line voltage $v_g(t)$ is positive, and D_2 and D_4 conduct when $v_g(t)$ is negative. The ac line current waveform is therefore a square wave, with $i_g(t) = i_L(t)$ when $v_g(t)$ is positive, and $i_g(t) = -i_L(t)$ when $v_g(t)$ is negative. The diode conduction angle β, defined as the angle through which one of the diodes conducts, is equal to 180° in CCM.

The rms value of a square wave is equal to its peak value I_{pk}, in this case the dc load current. The fundamental component of a square wave is equal to $4I_{pk}/\pi$. The square-wave contains odd harmonics which vary as $1/n$. The distortion factor is therefore

$$\text{distortion factor} = \frac{I_{1,rms}}{I_{rms}} = \frac{4}{\pi\sqrt{2}} = 90.0\% \tag{17.1}$$

The total harmonic distortion is

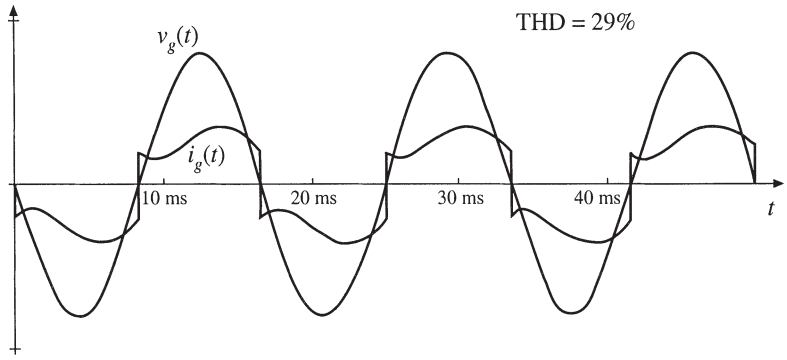


Fig. 17.2 Typical ac line current and voltage waveforms, continuous conduction mode. $f_0/f_L = 5$, $Q = 0.25$.

$$\text{THD} = \sqrt{\left(\frac{1}{\text{distortion factor}}\right)^2 - 1} = 48.3\% \tag{17.2}$$

So the limiting case of the large inductor leads to some significant harmonic distortion, although it is not as bad as the peak detection rectifier case. Since the square wave is in phase with the ac input voltage, the displacement factor is unity, and hence the power factor is equal to the distortion factor.

Whenever the inductor is sufficiently large, the rectifier diodes conduct continuously (i.e., there is no time interval in which all four diodes are reverse-biased). This is called the continuous conduction mode (CCM). A typical ac line current waveform is plotted in Fig. 17.2 for a finite but large value of L. It can be seen that the ac line current is discontinuous at the ac line voltage zero crossing, as in the square-wave limiting case. Some ringing is also present. This waveform contains a total harmonic distortion of approximately 29%.

17.1.2 Discontinuous Conduction Mode

The opposite case occurs when the inductor is very small and the capacitor C is very large. This is the peak detector circuit. In the limit as L goes to zero and C goes to infinity, the ac line current approaches a string of delta (impulse) functions that coincide with the peaks of the sinusoidal input voltage waveform. It can be shown that, in this limiting case, the THD becomes infinite while the distortion factor and power factor become zero. Of course, in the practical case the current is not infinite; nonetheless, large THD with low power factor is quite possible. The diodes conduct for less than one-half of the ac line period, and hence $\beta < 180^\circ$ in DCM.

Whenever the capacitor is large and the inductor is small, the rectifier tends to "peak detect," and the rectifier operates in the discontinuous conduction mode (DCM). There exist time intervals of nonzero length where all four rectifier diodes are reverse-biased. A typical set of waveforms is plotted in Fig. 17.3, where the capacitor is large but finite, and the inductor is small but nonzero. The ac line voltage and the value of the load resistance are the same as in Fig. 17.2, yet the peak current is substantially larger. The THD for this waveform is 145%, and the distortion factor is 57%.

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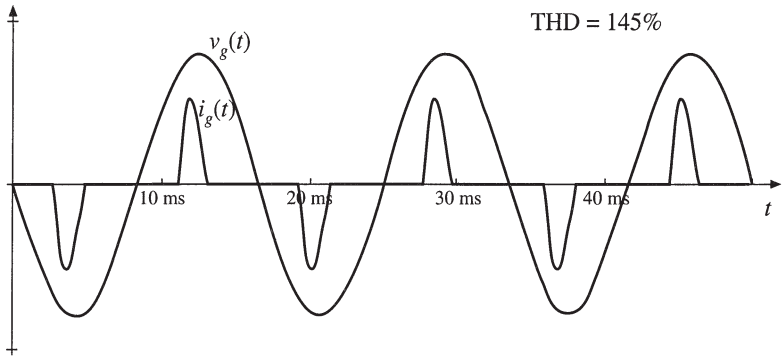


Fig. 17.3 Typical ac line current and voltage waveforms, discontinuous conduction mode. $f_0/f_L = 8.4$, $Q = 121$.

17.1.3 Behavior When *C* is Large

A variety of authors have discussed the solution of passive rectifier circuits; several works are listed in the references [8–15]. Analysis of even the simple circuit of Fig. 17.1 is surprisingly complex. For the case when C is infinite, it was shown in [8] that the rectifier waveshapes can be expressed as a function of a single dimensionless parameter K_L, defined as

$$K_L = \frac{2L}{RT_L} \tag{17.3}$$

where $T_L = 1/f_L$ is the ac line period. Equation (17.3) is of the same form as Eq. (5.6), used to define the dimensionless parameter K which governs the DCM behavior of PWM converters. Figure 17.4 illustrates the behavior of the single-phase rectifier circuit of Fig. 17.1, as a function of K_L and for infinite C [8]. When K_L is greater than approximately 0.1, the rectifier operates in CCM, with waveforms similar to those in Fig. 17.2.

The voltage conversion ratio M is defined as

$$M = \frac{V}{V_m} \tag{17.4}$$

where V_m is the peak value of the sinusoidal ac input voltage. In CCM, the output voltage is ideally independent of load, with $M = 2/\pi$. Addition of ac-side inductance can cause the output voltage to exhibit a dependence on load current. The total harmonic distortion in CCM is nearly constant and equal to the value given by Eq. (17.2).

Near the boundary between CCM and DCM, the fundamental component of the line current significantly lags the line voltage. The displacement factor reaches a minimum value slightly less than 80%, and power factors between 70% and 80% are observed.

For $K_L \ll 0.1$, the rectifier operates heavily in DCM, as a peak-detection rectifier. As K_L is decreased, the displacement factor approaches unity, while the THD increases rapidly. The power factor is dominated by the distortion factor. The output voltage becomes dependent on the load, and hence the rectifier exhibits a small but nonzero output impedance.

For K_L less than approximately 0.05, the waveforms are unchanged when some or all of the inductance is shifted to the ac side of the diode bridge. Figure 17.4 therefore applies to rectifiers contain-

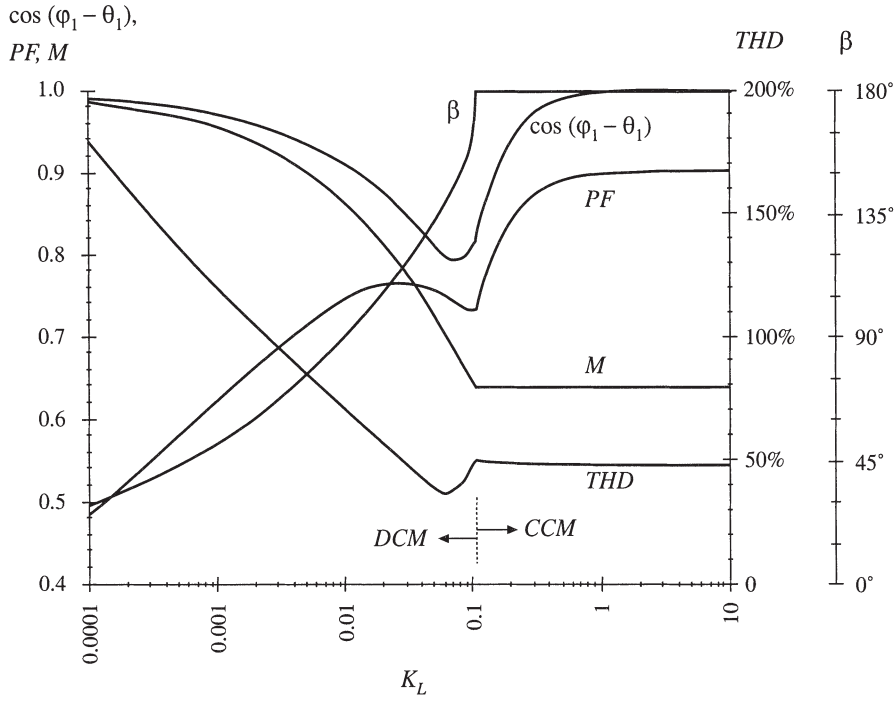


Fig. 17.4 Diode conduction angle β, displacement factor, power factor, conversion ratio, and total harmonic distortion of the rectifier circuit of Fig. 17.1, with infinite capacitance.

ing both ac-side and dc-side inductance, provided that the circuit operates sufficiently deeply in DCM. The parameter K_L is computed according to Eq. (17.3), with L taken to be the total ac-side plus dc-side inductance. A common example is the case where the circuit contains no physical discrete inductor; the performance is then determined by parasitic elements such as the capacitor equivalent series inductance, the inductance of the utility distribution wiring, and transformer leakage inductances.

17.1.4 Minimizing THD When *C* is Small

Let us now consider the performance of the second case, in which the inductor and capacitor are small and are intended solely to prevent load-generated EMI from reaching the ac line. In this case, dc-side filtering of the low-frequency even voltage harmonics of the ac line frequency is not necessary. The filter can be characterized by a corner frequency f_0, characteristic impedance R_0, and Q-factor, where

$$\begin{aligned} f_0 &= \frac{1}{2\pi\sqrt{LC}} \\ R_0 &= \sqrt{\frac{L}{C}} \\ Q &= \frac{R}{R_0} \\ f_p &= \frac{1}{2\pi RC} = \frac{f_0}{Q} \end{aligned} \tag{17.5}$$

To obtain good filtering of the EMI, the corner frequency f_0 should be selected to be sufficiently low. However, as can be seen from Eq. (17.5), reducing the value of f_0 requires increasing the values of L and/or C. As described above, it is undesirable to choose either element value too large, because large distortion results. So f_0 should not be too low, and there is a limit to the amount of filtering that can be obtained without significantly distorting the ac line current waveform.

How low can f_0 be? Once f_0 is chosen, how should L and C be chosen such that THD is minimized? We might expect that THD is increased when the phase of the filter input impedance $-Z_i(j\omega)$, evaluated at the second harmonic of the line frequency or $2fL$, differs significantly from 0°. When the zero crossings of the voltage and current waveforms do not coincide, then diode switching distorts the current waveform. To a lesser extent, input impedance phase shift at the higher-order even harmonic frequencies of the ac line frequency should also affect the THD. The input impedance $Z_i(s)$ contains two zeroes at frequency f_0, and a pole at frequency $f_p = f_0/Q$. To obtain small phase shift at low frequency, f_0 must be sufficiently large. In addition, Q must be neither too small nor too large: small Q causes the zeroes at f_0 to introduce low-frequency phase shift, while large Q causes the pole at f_p to occur at low frequency.

An approximate plot of THD vs. the choice of f_0 and Q is given in Fig. 17.5. It can be seen that there is an optimum choice for Q: minimum THD occurs when Q lies in the range 0.5 to 1. A typical waveform is plotted for the choice $f_0/f_L = 10$, $Q = 1$, in Fig. 17.6. The THD for this waveform is 3.6%, and the distortion factor is 99.97%.

Small Q corresponds to CCM operation, with large L and small C. In the extreme case as $Q \rightarrow 0$, the ac line current tends to a square wave with THD = 48%. Large Q corresponds to DCM operation, with small L and large C. In the extreme case as $Q \rightarrow \infty$, the ac line current tends to a string of delta functions with THD $\rightarrow \infty$. The optimum choice of Q leads to operation near the CCM-DCM boundary, such that the ac line current waveform contains neither step changes nor subintervals of zero current.

In the case when the load resistance R varies over a wide range of values, it may be difficult to optimize the circuit such that low THD is always obtained. It can be seen that increasing f_0/f_L leads to low THD for a wider range of load resistance. For example, when $f_0 = 5f_L$, THD ≤ 10% can be obtained only for Q between approximately 0.6 and 1.5, which is a 2.5:1 range of load resistance variations. If the

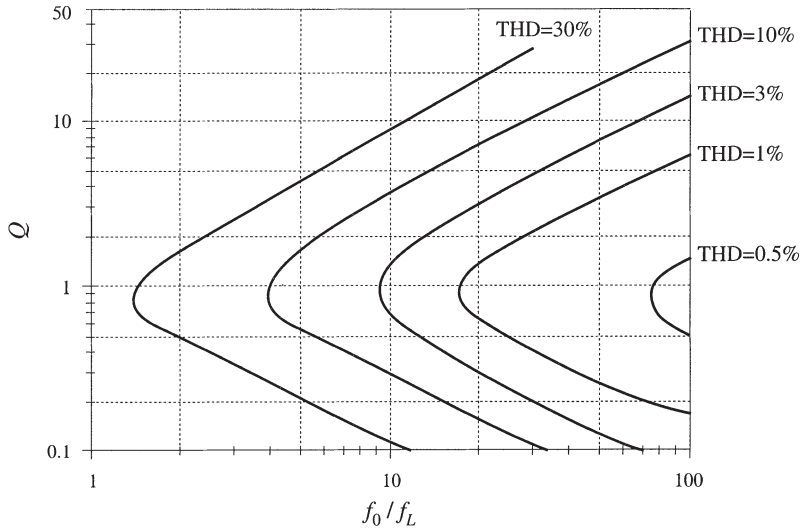


Fig. 17.5 Approximate total harmonic distortion of the single-phase diode rectifier with dc-side *L–C* filter.

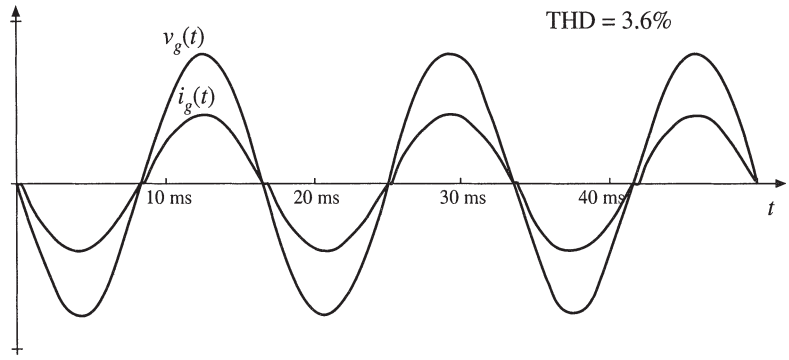


Fig. 17.6 Typical ac line current and voltage waveforms, near the boundary between continuous and discontinuous modes and with small dc filter capacitor. $f_0/f_L = 10$, $Q = 1$.

filter cutoff frequency f_0 is increased to $20f_L$, then THD $\leq 10\%$ is obtained for Q between approximately 0.15 and 7, or nearly a 50:1 range of resistance variations. In most cases, maximum harmonic limits are enforced only at full load, and hence it is possible to design with relatively low values of f_0/f_L if desired.

17.2 THE THREE-PHASE BRIDGE RECTIFIER

A basic full-wave three-phase uncontrolled rectifier with LC output filter is shown in Fig. 17.7. Its behavior is similar to the single-phase case, in that it exhibits both continuous and discontinuous conduction modes, depending on the values of L and C. The rectifier generates odd non-triplen harmonics in the ac line current. So the ac line current may contain 1st, 5th, 7th, 11th, 13th, etc. harmonics. The dc output may contain dc and even triplen harmonics: 0, 6, 12, 18, etc.

In the basic circuit of Fig. 17.7, no more than two of the six diodes can conduct during each interval, and hence the line current waveforms must contain intervals of nonzero length during which the current is zero. Unlike the single-phase case, the ac line current waveform must contain distortion even when the filter elements are removed.

17.2.1 Continuous Conduction Mode

In the continuous conduction mode, each ac line current is nonzero for 120 degrees out of each line half-cycle. For the remaining 60 degrees, the current is zero. This mode occurs when the inductance L is suf-

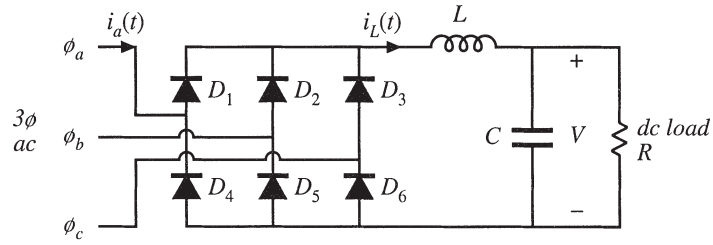


Fig. 17.7 Basic uncontrolled 3ø bridge rectifier circuit, with dc-side *L–C* filter.

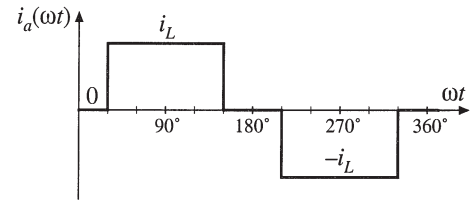


Fig. 17.8 Ac line current waveform $i_a(t)$, for the case when inductor L is large. The phase is drawn with respect to the zero crossing of the line-to-neutral voltage $v_{an}(t)$.

ficiently large, as well as when the filter elements L and C are removed entirely.

In the limit, when L is very large, then the current $i_L(t)$ is essentially constant. The current in phase a, $i_a(t)$, is then as shown in Fig. 17.8. It can be shown that the Fourier series for this waveform is

$$i_a(t) = \sum_{n=1,5,7,11,\ldots}^{\infty} \frac{4}{n\pi} I_L \sin\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\pi}{3}\right) \sin\left(n\omega t\right) \tag{17.6}$$

which is similar to the spectrum of the square wave of the single-phase case, but with the triplen harmonics missing. The THD of this waveform is 31%, and the distortion factor is $3/\pi = 95.5\%$. As in the case of the square wave, the amplitude of the odd nontriplen n^{th} harmonic is $(1/n)$ times the fundamental amplitude. So this waveform contains 20% fifth harmonic, 14% seventh harmonic, 9% eleventh harmonic, etc. It is interesting that, in comparison with the square-wave single-phase case, the missing 60° in the three-phase case improves the THD and power factor, by removing the triplen harmonics.

With a less-than-infinite value of inductance, the output ripple causes the ac line currents to be rounded, as in the typical waveform of Fig. 17.9. This waveform has a 31.9% THD, with a distortion factor that is not much different from the waveform of Fig. 17.8.

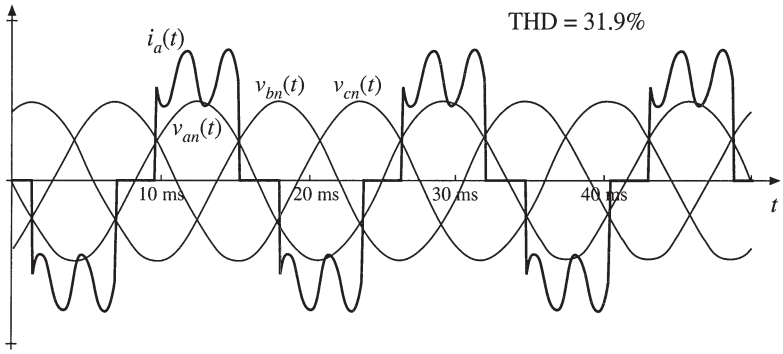


Fig. 17.9 Continuous conduction mode ac line-neutral voltages and phase a current, for a moderate value of inductance.

17.2.2 Discontinuous Conduction Mode

If the inductance is further reduced, then the three-phase rectifier enters the discontinuous conduction mode. The rectifier then begins to peak-detect, and the current waveforms become narrow pulses of high amplitude, occurring near the peaks of the line-line voltages. The phase a line current $i_a(t)$ contains two positive and two negative pulses, at the positive and negative peaks of the line-line voltages $v_{ab}(t)$ and $v_{ac}(t)$. As in the single-phase case, the total harmonic distortion becomes quite large in this case, and the

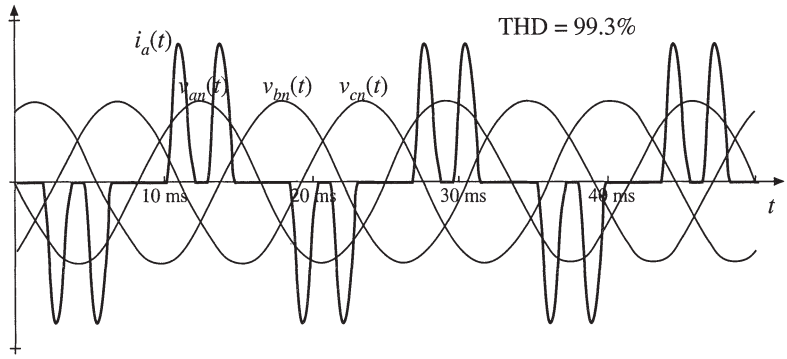


Fig. 17.10 Discontinuous conduction mode ac line-neutral voltages and phase *a* current.

power factor can be significantly degraded.

A typical waveform is given in Fig. 17.10. This waveform has a THD of 99.3%, and a distortion factor of 71%. This would be considered unacceptable in high-power applications, except perhaps at light load.

17.3 PHASE CONTROL

There are a wide variety of schemes for controlling the dc output of a 3ø rectifier using thyristors [1,2]. The most common one is shown in Fig. 17.11, in which the six diodes of Fig. 17.7 are replaced by silicon controlled rectifiers (SCRs). Typical waveforms are given in Fig. 17.12, for large dc-side filter inductance.

If Q_1 were an uncontrolled diode, it would conduct whenever the line-to-line voltage v_{ab} or v_{ac} is the largest in magnitude of the six line–line voltages v_{ab}, v_{bc}, v_{ca}, v_{ba}, v_{cb}, and v_{ca}. This occurs for 120° of each cycle, beginning at the point where $v_{ab} = v_{cb}$. In Fig. 17.12, this occurs at $\omega t = 60°$. The output voltage of the controlled rectifier is controlled by delaying the firing of Q_1 by an angle α, such that Q_1 begins conducting at $\omega t = 60° + \alpha$. This has the effect of reducing the dc output voltage.

There can be no dc component of voltage across inductor *L*. Hence, in steady-state, the dc component of the rectifier output voltage $v_R(t)$ must equal the dc load voltage *V*. But $v_R(t)$ is periodic, with period equal to six times the ac line period (or 60°). So the dc component of $v_R(t)$ can be found by Fourier analysis, and is equal to the average value of $v_R(t)$. Over one 60° interval, for example $(60° + \alpha) \le \omega t \le (120° + \alpha)$, $v_R(t)$ follows the line-line voltage $v_{ab}(t) = 3V_m \sin(\omega t + 30°)$. The average is therefore

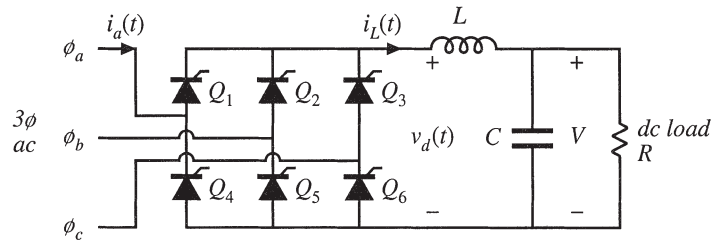


Fig. 17.11 Basic controlled 3ø bridge rectifier circuit, with dc-side *L–C* filter.

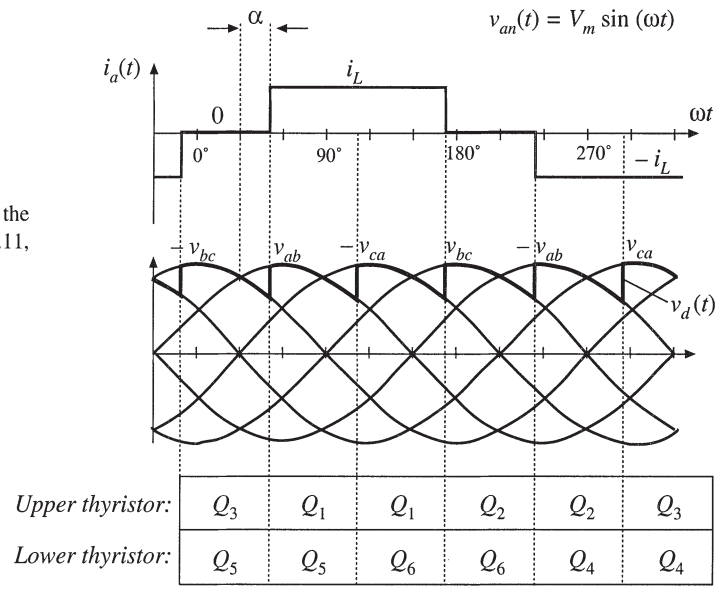


Fig. 17.12 Waveforms for the controlled rectifier of Fig. 17.11, with large dc filter inductance.

$$V = \frac{3}{\pi}\int_{30^\circ+\alpha}^{90^\circ+\alpha} \sqrt{3}\, V_m \sin\left(\theta + 30^\circ\right) d\theta$$
$$= \frac{3\sqrt{2}}{\pi} V_{L\text{-}L,\,rms} \cos\alpha \qquad (17.7)$$

where $V_{L\text{-}L,\,rms}$ is the rms line-to-line voltage. This equation is plotted in Fig. 17.13. It can be seen that, if it is necessary to reduce the dc output voltage to values close to zero, then the delay angle α must be

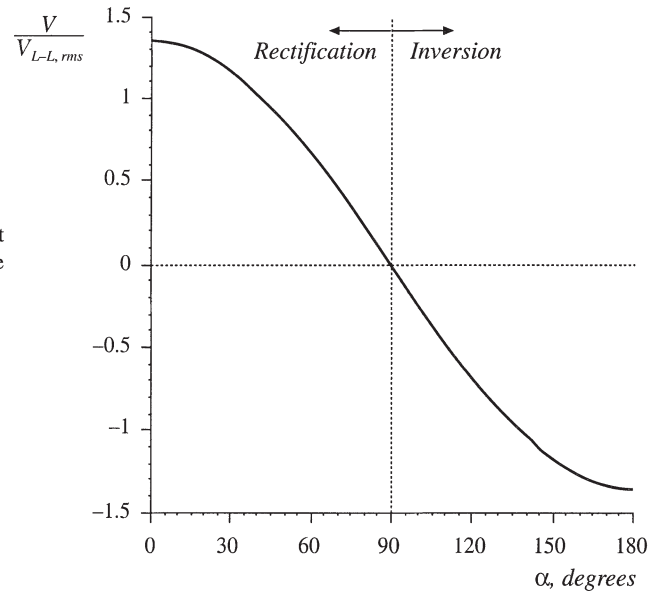


Fig. 17.13 Variation of the dc output voltage V with delay angle α, for the phase-controlled circuit of Fig. 17.11.

increased to close to 90°. With a small inductance, the controlled rectifier can also operate in discontinuous conduction mode, with modified output voltage characteristics.

17.3.1 Inverter Mode

If the dc load is capable of supplying power, then it is possible for the direction of power flow to reverse. For example, consider the three-phase controlled rectifier circuit of Fig. 17.14. The resistive load is replaced by a voltage source and thevenin-equivalent resistance, capable of either supplying or consuming power. The dc load power is equal to VI_L, which is positive (rectifier mode) when both V and I_L are positive. The thyristor is a unidirectional-current switch, which cannot conduct negative current, and hence I_L must always be positive. However, it is possible to cause the output voltage V to be negative, by increasing the delay angle α. The dc load power VI_L then becomes a negative quantity (inverter mode), meaning that power flows from the dc load into the 3øac system.

Provided that the dc-side filter inductance L is sufficiently large, then Eq. (17.7) is valid even when the delay angle α is greater than 90°. It can be seen in Fig. 17.13 that the dc output voltage V becomes negative for $\alpha > 90°$, and hence the power flow indeed reverses. Delay angles approaching 180° are possible, with the maximum angle limited by commutation of the thyristor devices.

17.3.2 Harmonics and Power Factor

Let us next consider the harmonic content and power factor of the phase-controlled rectifier with large inductance. Comparison of the line current waveform of Fig. 17.12 with that of the uncontrolled rectifier (Fig. 17.8) reveals that the waveshapes are identical. The only difference is the phase lag α present in the phase-controlled rectifier. This has the effect of shifting the fundamental component of current (and the harmonics as well) by angle α. The Fourier series is therefore

$$i_a(t) = \sum_{n=1,5,7,11,\ldots}^{\infty} \frac{4}{n\pi} I_L \sin\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\pi}{3}\right) \sin\left(n\omega t - n\alpha\right) \tag{17.8}$$

Hence the harmonic amplitudes are the same (the fifth harmonic amplitude is 20% of the fundamental, etc.), the THD is again 31%, and the distortion factor is again 95.5%. But there is phase lag in the fundamental component of current, which leads to a displacement factor of $\cos(\alpha)$. The power factor is therefore

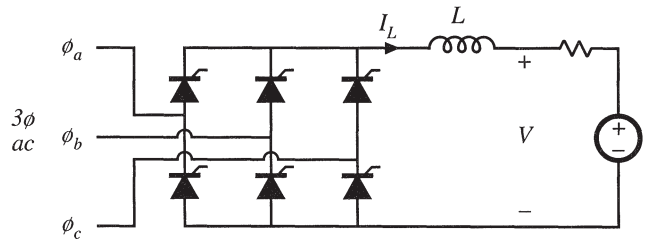


Fig. 17.14 If the load is capable of supplying power, then the 3ø bridge circuit functions as an inverter for $V < 0$ and $\alpha > 90°$.

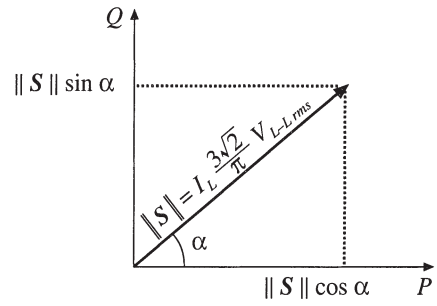


Fig. 17.15 Fundamental component complex power diagram for the 3ø bridge circuit operating in rectifier mode.

$$\text{power factor} = 0.955 \left| \cos(\alpha) \right| \tag{17.9}$$

which can be quite low when the dc output voltage V is low.

It is at first somewhat puzzling that the introduction of phase control can cause the fundamental current to lag the voltage. Apparently, the rectifier consumes reactive power equal to

$$Q = \sqrt{3}\, I_{a,\,rms} V_{L\text{-}L,\,rms} \sin\alpha = I_L \frac{3\sqrt{2}}{\pi} V_{L\text{-}L,\,rms} \sin\alpha \tag{17.10}$$

We normally associate lagging current and the consumption of reactive power with inductive energy storage. But this is not what is happening in the rectifier; indeed, the inductor and capacitor can be removed entirely from the rectifier circuit, and a lagging fundamental current is still obtained by phase control. It is simply the delay of the switching of the rectifiers that causes the current to lag, and no energy storage is involved. So two mechanisms cause the phase-controlled rectifier to operate with low power factor: the lagging fundamental component of current, and the generation of current harmonics.

Equation (17.10) can be further interpreted. Note that the dc output power P is equal to the dc inductor current I_L times the dc output voltage V. By use of Eq. (17.7), this can be written

$$P = I_L \frac{3\sqrt{2}}{\pi} V_{L\text{-}L,\,rms} \cos\alpha \tag{17.11}$$

Comparison of Eqs. (17.10) and (17.11) reveals that the rectifier fundamental volt-amperes can be expressed using the conventional concepts of complex power $\boldsymbol{S} = P + jQ$, where P is the real (average) power consumed and Q is the fundamental reactive power consumed. The complex power phasor diagram, treating the fundamental components only, is illustrated in Fig. 17.15.

17.3.3 Commutation

Let's consider next what happens during the switching transitions. In the phase-controlled rectifier circuit of Fig. 17.16, the dc-side inductor L_d is large in value, such that its current ripple is negligible. Inductors L_a, L_b, and L_c are also present in the ac lines; these may be physical inductors of the rectifier circuit, or they may represent the source impedance of the power system, typically the leakage inductances of a nearby transformer. These inductors are relatively small in value.

Consider the switching transition illustrated in Fig. 17.17. Thyristors Q_3 and Q_5 initially conduct. At time t_{c1}, thyristor Q_1 is gated on, and the dc current i_L begins to shift from Q_3 to Q_1. The ac line currents $i_a(t)$ and $i_c(t)$ cannot be discontinuous, since inductors L_a and L_c are present in the lines. So dur-

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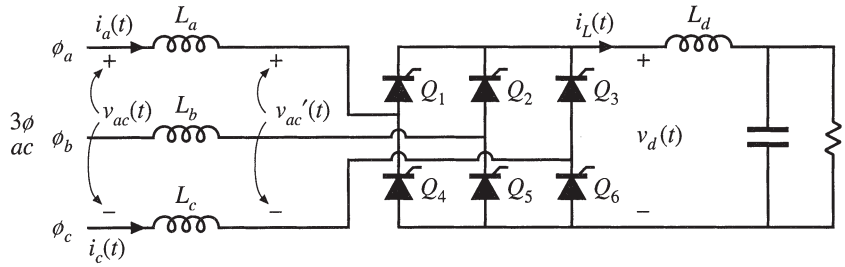


Fig. 17.16 Controlled 3ø rectifier circuit, with small ac-side inductances.

ing the interval $t_{c1} < t < t_{c2}$, thyristors Q_1 and Q_3 both conduct, and the voltage v_{ac}' is zero. Voltage is applied across inductors L_a and L_c, causing their currents to change; for successful commutation, sufficient volt-seconds must be applied to cause the currents to change from i_L to zero, and vice versa. Any stored charge that remains in thyristor Q_3 when current $i_c(t)$ reaches zero must also be removed, and hence $i_c(t)$ actually continues negative as discussed in Chapter 4. When the reverse recovery process of Q_3 is complete, then Q_3 is finally in the off-state, and the next subinterval begins with the conduction of thyristors Q_1 and Q_5.

The commutation process described above has several effects on the converter behavior. First, it can be seen that the thyristor bridge dc-side voltage $v_d(t)$ is reduced in value during the commutation interval. Hence, its average value $\langle v_d \rangle$ and the dc output voltage V are reduced. The amount of reduction is dependent on the dc load current: a larger dc load current leads to a longer commutation interval, and hence to a greater reduction in $\langle v_d \rangle$. So the rectifier has an effective output resistance. Second, the maximum value of the delay angle α is limited to some value less than 180°. If α exceeds this limit, then insufficient volt-seconds are available to change inductor current $i_c(t)$ from i_L to zero, leading to *commutation failure*. Third, when the rectifier ac-side inductors are small or zero, so that L_a, L_b, and L_c represent

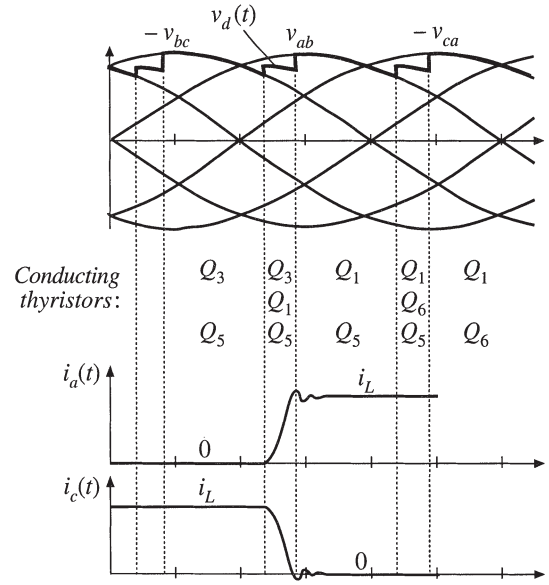


Fig. 17.17 Switching transition waveforms, for the rectifier of Fig. 17.16.

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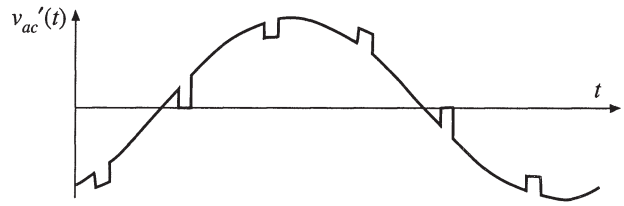


Fig. 17.18 Notching of the ac line-line voltage waveforms during the commutation intervals.

essentially only the power system source impedance, then commutation causes significant notching of the ac voltage waveforms (Fig. 17.18) at the point of common coupling of the rectifier to the power system. Other elements connected locally to the power system will experience voltage distortion. Limits for the areas of these notches are suggested in IEEE/ANSI standard 519.

17.4 HARMONIC TRAP FILTERS

Passive filters are often employed to reduce the current harmonics generated by rectifiers, such that harmonic limits are met. The filter network is designed to pass the fundamental and to attenuate the significant harmonics such as the fifth, seventh, and perhaps several higher-order odd nontriplen harmonics. Such filters are constructed using resonant tank circuits tuned to the harmonic frequencies. These networks are most commonly employed in balanced three-phase systems. A schematic diagram of one phase of the filter is given in Fig. 17.19.

The ac power system is modeled by the thevenin-equivalent network containing voltage source v_s and impedance Z_s'. Impedance Z_s' is usually inductive in nature, although resonances may occur due to nearby power-factor-correction capacitors. In most filter networks, a series inductor L_s' is employed; the filter is then called a harmonic trap filter. For purposes of analysis, the series inductor L_s' can be lumped into Z_s', as follows:

$$Z_s(s) = Z_s'(s) + sL_s' \tag{17.12}$$

The rectifier and its current harmonics are modeled by current source i_r. Shunt impedances Z_1, Z_2,... are

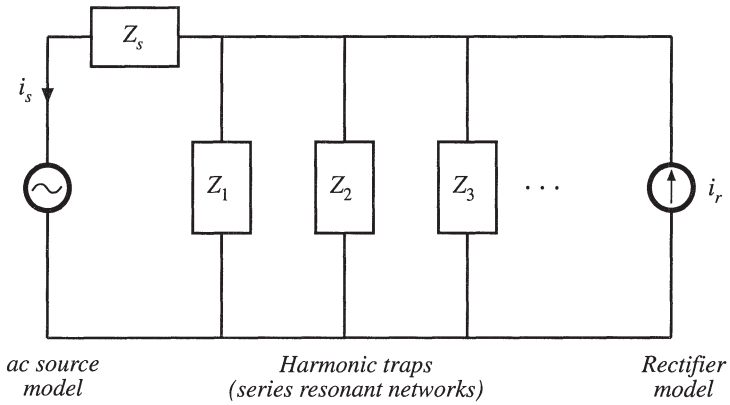


Fig. 17.19 A harmonic trap filter. One phase is illustrated, on a line-to-neutral basis.

tuned such that they have low impedance at the harmonic frequencies, and hence the harmonic currents tend to flow through the shunt impedances rather than into the ac power system.

The approximate algebra-on-the-graph method described in Chapter 8 is used here to construct the filter transfer function, in terms of impedance Z_s and the shunt impedances Z_1, Z_2,.... This approach yields a simple intuitive understanding of how the filter operates. Since the harmonic frequencies are close in value, the pole and zero frequencies of the filter are never well separated in value. So the approximate algebra-on-the-graph method is, in general, not sufficiently accurate for the complete design of these filters, and the pole frequencies must be found by numerical methods. A typical design approach might involve estimating element values using the algebra-on-the-graph method, then refining the values using a computer simulation package.

The filter transfer function $H(s)$ is given by the current divider ratio

$$H(s) = \frac{i_s(s)}{i_r(s)} = \frac{Z_1 \parallel Z_2 \parallel \cdots}{Z_s + Z_1 \parallel Z_2 \parallel \cdots} \tag{17.13}$$

As discussed in Chapter 8, another way to write this transfer function is

$$H(s) = \frac{i_s(s)}{i_r(s)} = \frac{Z_s \parallel Z_1 \parallel Z_2 \parallel \cdots}{Z_s} \tag{17.14}$$

So we can construct $H(s)$ by first constructing the parallel combination $Z_s \parallel Z_1 \parallel Z_2 \parallel$ ..., then dividing by the total line impedance Z_s. It can be shown that, if $Z_s(s)$ contains no poles, then the numerator of $H(s)$ is the product of the zeroes of the shunt impedances Z_1, Z_2,.... So this graphical method yields the exact zeroes of $H(s)$, which coincide with the series resonances of the shunt impedances. But the poles of $H(s)$, which arise from parallel resonances in the filter, require more work to compute.

Let us first consider the simple case illustrated in Fig. 17.20, where Z_1 consists of a series resonant circuit tuned to eliminate the fifth harmonic, and Z_s is composed of a single inductor L_s. Construction of the impedance of a series resonant network is described in Chapter 8. The $\parallel Z_1 \parallel$ asymptotes follow the capacitor impedance magnitude $1/\omega C_1$ at low frequency, and the inductor impedance magnitude ωL_1 at high frequency. At the resonant frequency, $\parallel Z_1 \parallel$ is equal to R_1. The asymptotes for $\parallel Z_1 \parallel$ are constructed in Fig. 17.21(a).

Figure 17.21(a) also illustrates the impedance magnitude $\parallel Z_s \parallel = \omega L_s$, as well as construction of

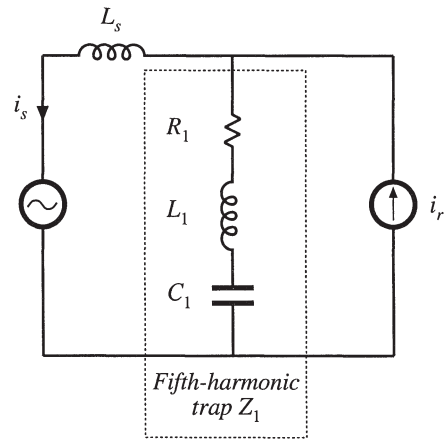


Fig. 17.20 Simple harmonic trap filter example, containing a series resonant trap tuned to the fifth harmonic, and inductive line impedance.

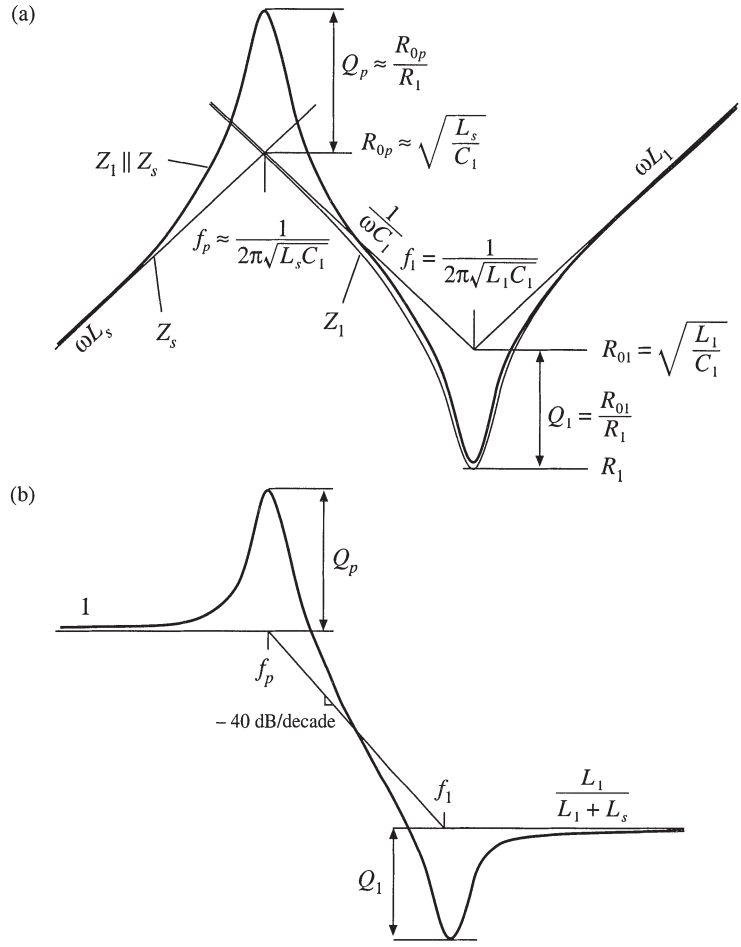


Fig. 17.21 Construction of approximate frequency response using the algebra-on-the-graph method: (a) impedance asymptotes, (b) transfer function asymptotes $\| H \|$.

the approximate asymptotes for the parallel combination ($Z_s \| Z_1$). Recall that, to construct the approximate asymptotes for the parallel combination, we simply select the smaller of the Z_s and Z_1 asymptotes. The result is the shaded set of asymptotes shown in the figure: the parallel combination follows ωL_s at low frequency, and $\| Z_1 \|$ at high frequency. Note that, in addition to the intended series resonance at frequency f_1, a parallel resonance occurs at frequency f_p.

The filter transfer function $\| H(s) \|$ is now constructed using Eq. (17.14). As illustrated in Fig. 17.21(b), $\| H(s) \| = 1$ at low frequencies where both the numerator and the denominator of Eq. (17.14) are equal to ωL_s. The parallel resonance at frequency f_p leads to resonant poles and peaking in $\| H(s) \|$. The resonance at frequency f_1 leads to resonant zeroes and attenuation in $\| H(s) \|$. At high frequency, the gain is $L_1/(L_1 + L_s)$.

So if we want to attenuate fifth harmonic currents, we should choose the element values such that the series resonant frequency f_1 coincides with the fifth harmonic frequency. This frequency is sim-

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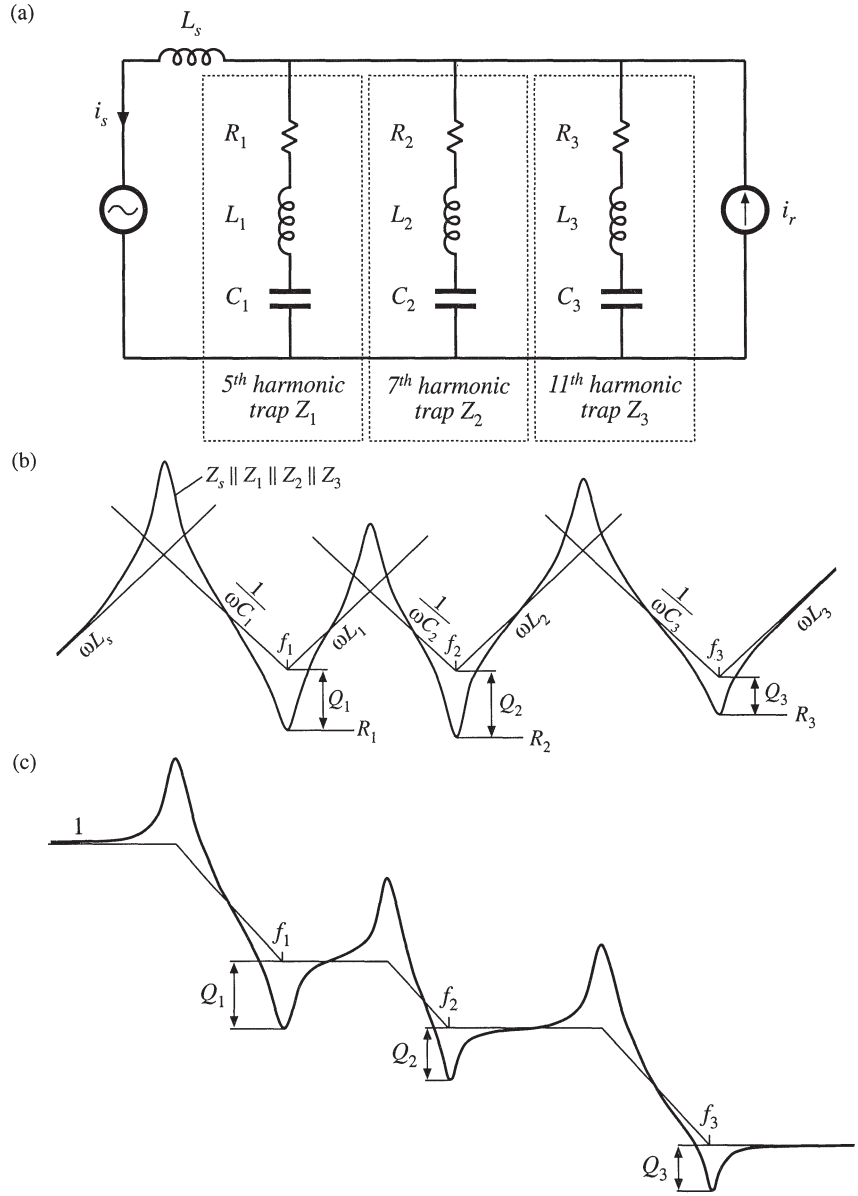


Fig. 17.22 Construction of approximate frequency response for a harmonic trap filter that attenuates the fifth, seventh, and eleventh harmonics: (a) impedance asymptotes, (b) transfer function asymptotes.

ply the resonant frequency of the shunt impedance Z_1, or

$$f_1 = \frac{\omega_1}{2\pi} = \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{17.15}$$

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In addition, care must be exercised regarding the parallel resonance. Since no three-phase system is exactly balanced, small amounts of third harmonic currents always occur. These currents usually have negligible effect; however, the parallel resonance of the harmonic trap filter can increase their magnitudes significantly. Even worse, the Q-factor of the parallel resonance, Q_p, is greater than the series-resonance Q-factor Q_1.

The filter circuit of Fig. 17.20 is simple enough that an exact analysis can be performed easily. The exact transfer function is

$$H(s) = \frac{\left(1 + \frac{s}{\omega_1 Q_1} + \left(\frac{s}{\omega_1}\right)^2\right)}{\left(1 + \frac{s}{\omega_p Q_p} + \left(\frac{s}{\omega_p}\right)^2\right)} \tag{17.16}$$

where

$$f_1 = \frac{\omega_1}{2\pi} = \frac{1}{2\pi\sqrt{L_1 C_1}} \qquad f_p = \frac{\omega_p}{2\pi} = \frac{1}{2\pi\sqrt{(L_1 + L_s)C_1}}$$

$$Q_1 = \frac{1}{R_1}\sqrt{\frac{L_1}{C_1}} \qquad Q_p = \frac{1}{R_1}\sqrt{\frac{(L_1 + L_s)}{C_1}}$$

The resonant zeroes do indeed appear at the series resonant frequency, while the parallel resonance and its associated resonant poles appear at frequency f_p determined by the series combination of L_1 and L_p.

To attenuate several harmonics—for example, the fifth, seventh, and eleventh—series resonant networks can be tuned to provide resonant zeroes at each. A circuit is given in Fig. 17.22(a), with the impedance asymptotes of Fig. 17.22(b). The resulting approximate $\| H(s) \|$ is given in Fig. 17.22(c). It can be seen that, associated with each series resonance is a parallel resonance. Each parallel resonant frequency should be chosen such that it is not significantly excited by harmonics present in the network.

The filter transfer function can be given high-frequency single-pole rolloff by addition of a bypass resistor R_{bp}, as illustrated in Fig. 17.23(a). Typical impedance and transfer function asymptotes for this network are constructed in Fig. 17.24. The bypass resistor allows some additional attenuation of the higher-order harmonics, without need for series resonant traps tuned to each harmonic. The network of Fig. 17.23(a) is sometimes called a "high pass" network, because it allows high-frequency currents to flow through the shunt branch. But it causes the overall filter transfer function $H(s)$ to reject high frequencies. A simple harmonic trap filter that contains series resonances that can be tuned to the fifth and

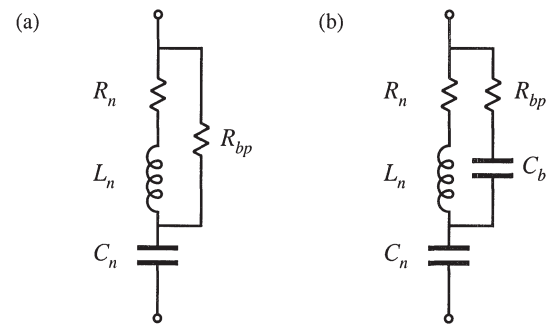


Fig. 17.23 Addition of bypass resistor R_{bp} to a series resonant network, to obtain a high-frequency rolloff characteristic: (a) basic circuit, (b) addition of blocking capacitor C_b to reduce power consumption at the fundamental frequency.

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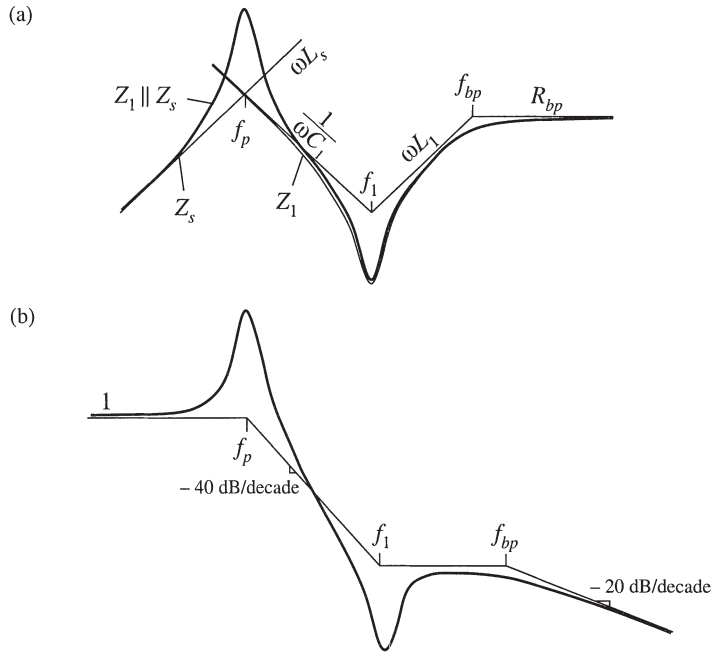


Fig. 17.24 Construction of approximate frequency response for a harmonic trap filter containing bypass resistor: (a) impedance asymptotes, (b) transfer function asymptotes.

seventh harmonics, with a single-pole rolloff to attenuate higher-order harmonics such as the eleventh and thirteenth, is illustrated in Fig. 17.25.

Power loss in the bypass resistor can be an issue: since R_{bp} is not part of the resonant network, significant fundamental (50 Hz or 60 Hz) currents can flow through R_{bp}. The power loss can be reduced by addition of blocking capacitor C_b as illustrated in Fig. 17.23(b). This capacitor is chosen to increase the impedance of the R_{bp}–C_b leg at the fundamental frequency, but have negligible effect at the higher-

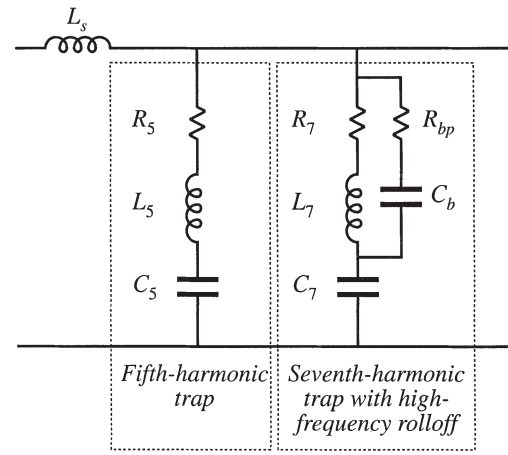


Fig. 17.25 A harmonic trap filter containing series resonances tuned to the fifth and seventh harmonics, and high-frequency rolloff characteristic.

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order harmonic frequencies.

The harmonic trap filter network can also supply significant reactive power to the rectifier and power system. As given by Eq. (17.10), the rectifier fundamental current lags the voltage, and the rectifier consumes reactive power. As seen in Fig. 17.22(a), the impedances of the series resonant tank networks are dominated by their capacitor asymptotes at low frequency. Hence, at the fundamental frequency, the filter impedance reduces to an equivalent capacitor, equal to the parallel combination of the tank capacitors. The current through this capacitance leads the ac line voltage, and hence as mentioned in the previous chapter, the capacitor is a source of reactive power.

17.5 TRANSFORMER CONNECTIONS

A final conventional approach to reducing the input harmonics of three-phase rectifiers is the use of phase-shifting transformer circuits. With these schemes, the low-order harmonics, such as the fifth and seventh, can be eliminated. The remaining harmonics are smaller in magnitude, and also are easier to filter.

The rectifier circuit of Fig. 17.7 is known as a *six-pulse* rectifier because the diode output voltage waveform contains six pulses per ac line period. The output voltage ripple has a fundamental frequency that is six times the ac line frequency. As illustrated in Fig. 17.8, the ac line current waveforms contain three steps: at any given instant, $i_a(t)$ is equal to either i_L, 0, or $-i_L$. The spectrum of the current waveform contains fundamental and odd nontriplen harmonics (1, 5, 7, 11, 13,...), whose amplitudes vary as $1/n$.

It is possible to shift the phase of the ac line voltage using three-phase transformer circuits. For example, in the delta-wye transformer circuit of Fig. 17.26, the transformer primary windings are driven by the primary-side line-to-line voltages, while the transformer secondaries supply the secondary-side line-to-neutral voltages. In an ideal transformer, the secondary voltage is equal to the primary voltage multiplied by the turns ratio; hence, the phasor representing the secondary voltage is in phase with the

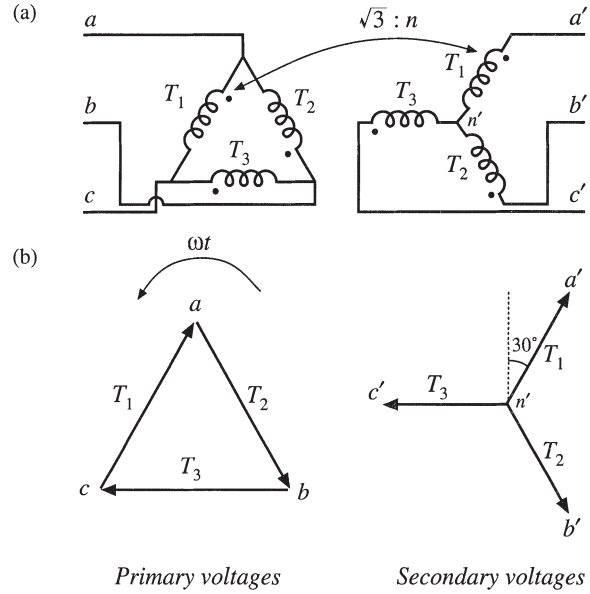


Fig. 17.26 Three-phase delta-wye transformer connection: (a) circuit, (b) voltage phasor diagram.

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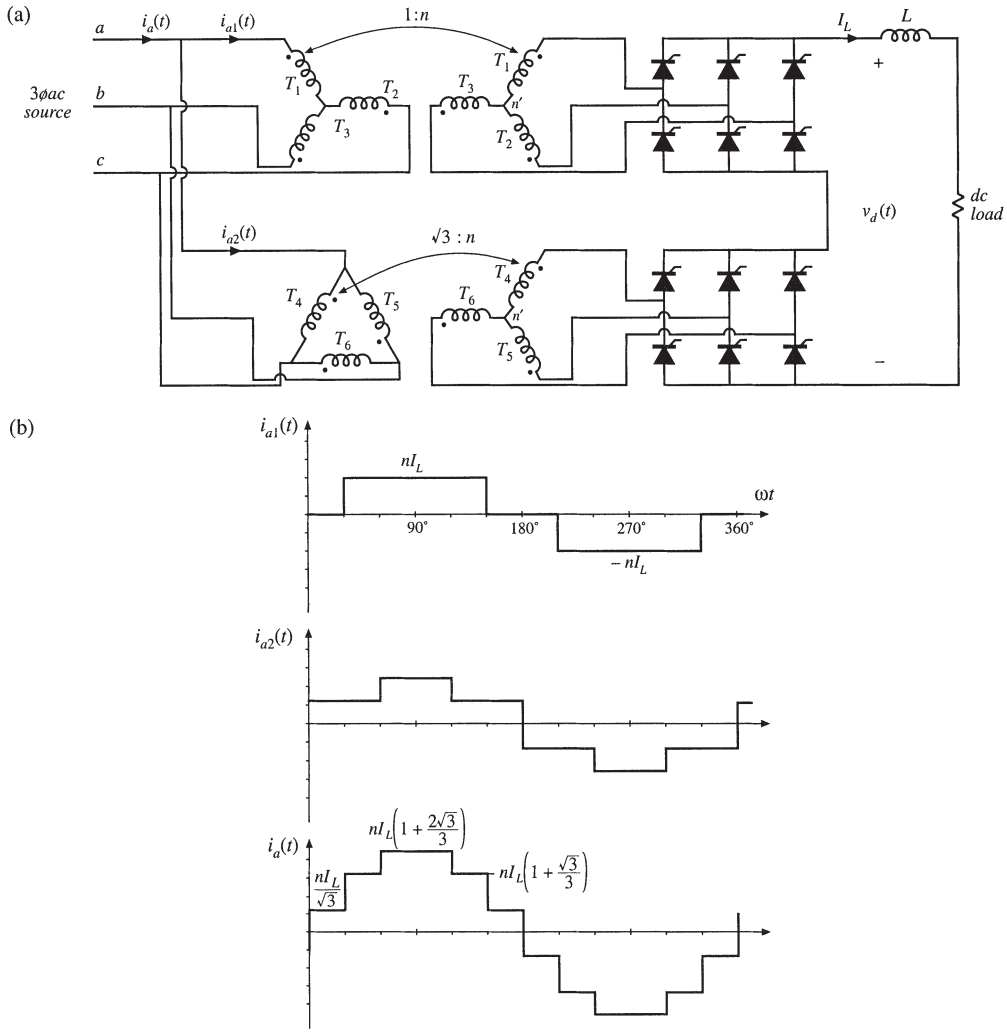


Fig. 17.27 Twelve-pulse rectifier: (a) circuit, (b) input phase *a* current waveforms.

primary voltage phasor, and is scaled in magnitude by the turns ratio. So in the delta-wye transformer connection, the secondary line-to-neutral voltages are in phase with the primary line-to-line voltages. In a balanced three-phase system, the line-to-line voltages are shifted in phase by 30° with respect to the line-to-neutral voltages, and are increased in magnitude by a factor of $\sqrt{3}$. Hence the secondary line-to-neutral voltages lag the primary line-to-neutral voltages by 30°. The wye-delta connection is also commonly used; this circuit causes the secondary voltages to lead the primary voltages by 30°. Many other more complicated transformer circuits are known, such as the zig-zag, forked-wye, and extended-delta connections, which can lead to phase shifts of any desired amount.

The 30° phase shift of the delta-wye transformer circuit is used to advantage in the twelve-pulse rectifier circuit of Fig. 17.27(a). This circuit consists of two bridge rectifier circuits driven by 3ø voltages

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that differ in phase by 30°. The bridge rectifier outputs are connected in series to the dc filter inductor and load. The total rectifier output voltage $v_d(t)$ has a fundamental frequency that is twelve times the ac line frequency. The input phase a ac line current $i_a(t)$ is the sum of currents in three windings, and has the stepped waveshape illustrated in Fig. 17.27(b). It can be shown that this waveform contains Fourier components at the fundamental frequency and at the 11^{th}, 13^{th}, 23^{rd}, 25^{th},... harmonic frequencies, whose amplitudes vary as $1/n$. Doing so is left as a homework problem. Thus, the twelve-pulse rectifier eliminates the 5^{th}, 7^{th}, 17^{th}, 19^{th},... harmonics.

An eighteen-pulse rectifier can be constructed using three six-pulse bridge rectifiers, with transformer circuits that shift the applied voltages by 0°, + 20°, and – 20°. A twenty-four pulse rectifier requires four six-pulse bridge rectifiers, fed by voltages shifted by 0°, + 15°, – 15°, and 30°. If p is the pulse number, then the rectifier produces line current harmonics of number $n = pk \pm 1$, where $k = 0, 1, 2, 3,...$. If the dc current ripple can be neglected, then the magnitudes of the remaining current harmonics vary as $1/n$. The dc-side harmonics are of number pk.

So by use of polyphase transformer connections and rectifier circuits having high pulse number, quite good ac line current waveforms can be obtained. As the pulse number is increased, the current waveforms approaches a sinusoid, and contains a greater number of steps having smaller amplitude. The low-order harmonics can be eliminated, and the remaining high-frequency harmonics are easily filtered.

17.6 SUMMARY

1. With a large dc filter inductor, the single-phase full-wave rectifier produces a square-wave line current waveform, attaining a power factor of 90% and 48% THD. With smaller values of inductance, these figures are degraded. In the discontinuous conduction mode, THD greater than 100%, with power factors of 55% to 65% are typical. When the capacitance is large, the power factor, THD, displacement factor, and conversion ratio can be expressed as a function of only the dimensionless parameter K_L.

2. In the three-phase case, the bridge rectifier with large dc filter inductor produces a stepped waveform similar to the square wave, but missing the triplen harmonics. This waveform has 31% THD, and leads to a power factor of 95.5%. Reduced dc inductor values again lead to increased THD and reduced power factor, and as L tends to zero, the THD tends to infinity while the power factor tends to zero. In practice, the minimum effective series inductance is limited by the power system source inductance.

3. With a large dc inductor, phase control does not influence the distortion factor or THD, but does lead to a lagging fundamental current and decreased displacement factor. Phase-controlled rectifiers and inverters are consumers of reactive power.

4. If the load is capable of supplying power, then the phase-controlled rectifier can become an inverter. The delay angle a is greater than 90°, and the output voltage polarity is reversed with respect to rectifier operation. The maximum delay angle is limited by commutation failure to a value less than 180°.

5. Harmonic trap filters and multipulse-rectifier/polyphase transformer circuits find application in high-power applications where their large size and weight are less of a consideration than their low cost. In the harmonic trap filter, series resonant tank circuits are tuned to the offending harmonic frequencies, and shunt the harmonic currents away from the utility power network. Parallel resonances may cause unwanted peaks in the filter transfer function. Operation of these filters may be understood using the algebra-on-the-graph method, and computer simulations can be used to refine the accuracy of the analysis or design. Rectifiers of higher pulse number can also yield improved current waveforms, whose harmonics are of high frequency and small amplitude, and are easily filtered.

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PROBLEMS

17.1 The half-controlled single-phase rectifier circuit of Fig. 17.28 contains a large inductor L, whose current $i_L(t)$ contains negligible ripple. The thyristor delay angle is α.

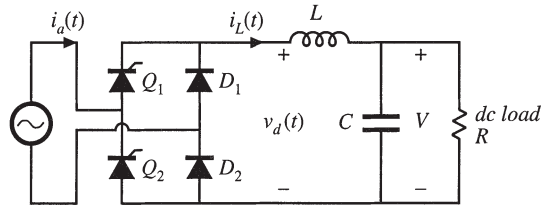


Fig. 17.28 Half-controlled rectifier circuit of Problem 17.1.

(a) Sketch the waveforms $v_d(t)$ and $i_a(t)$. Label the conduction intervals of each thyristor and diode.

(b) Derive an expression for the dc output voltage V, as a function of the rms line-line voltage and the delay angle.

(c) Derive an expression for the power factor.

(d) Over what range of α are your expressions of parts (b) and (c) valid?

17.2 The half-controlled rectifier circuit of Fig. 17.29 contains a large inductor L, whose current $i_L(t)$ contains negligible ripple. The thyristor delay angle is α.

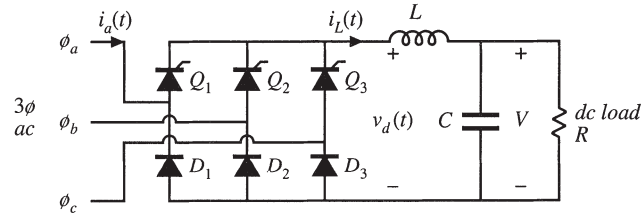


Fig. 17.29 Three-phase half-controlled rectifier circuit of Problem 17.2.

(a) Sketch the waveforms $v_d(t)$ and $i_a(t)$. Label the conduction intervals of each thyristor and diode.

(b) Derive an expression for the dc output voltage V, as a function of the rms line-line voltage and the delay angle.

(c) Derive an expression for the power factor.

(d) Over what range of α are your expressions of parts (b) and (c) valid?

17.3 A 3ø SCR bridge is connected directly to a resistive load, as illustrated in Fig. 17.30. This circuit operates in the continuous conduction mode for small delay angle α, and in the discontinuous conduction mode for sufficiently large α.

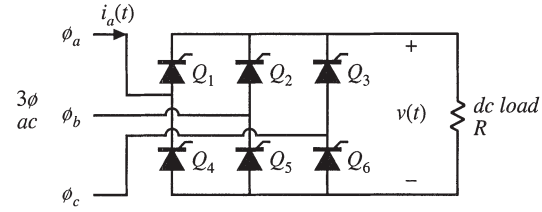


Fig. 17.30 Three-phase controlled rectifier circuit of Problem 17.3.

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(a) Sketch the output voltage waveform $v(t)$, for CCM operation and for DCM operation. Clearly label the conduction intervals of each SCR.

(b) Under what conditions does the rectifier operate in CCM? in DCM?

(c) Derive an expression for the dc component of the output voltage in CCM.

(d) Repeat part (c), for DCM operation.

17.4 A rectifier is connected to the 60 Hz utility system. It is desired to design a harmonic trap filter that has negligible attenuation or amplification of 60 Hz currents, but which attenuates both the fifth- and seventh-harmonic currents by a factor of 10 (– 20 dB). The ac line inductance L_s is 500 μH.

(a) Select L_5, the inductance of the fifth harmonic trap, equal to 500 μH, and L_7, the inductance of the seventh harmonic trap, equal to 250 μH. Compute first-pass values for the resistor and capacitor values of the fifth and seventh harmonic trap circuits, neglecting the effects of parallel resonance.

(b) Plot the frequency response of your filter. It is suggested that you do this using SPICE or a similar computer program. Does your filter meet the attenuation specifications? Are there significant parallel resonances? What is the gain or attenuation at the third harmonic frequency?

(c) Modify your element values, to obtain the best design you can. You must choose L_s = 500 μH, but you may change all other element values. Plot the frequency response of your improved filter. "Best" means that the 20 dB attenuations are obtained at the fifth and seventh harmonic frequencies, that the gain at 60 Hz is essentially 0 dB, and that the Q-factors of parallel resonances are minimized.

17.5 A rectifier is connected to the 50 Hz utility system. It is desired to design a harmonic trap filter that has negligible attenuation or amplification of 50 Hz currents, but that attenuates the fifth-, seventh-, and eleventh-harmonic currents by a factor of 5 (– 14 dB). In addition, the filter must contain a single-pole response that attenuates the thirteenth and higher harmonics by a factor of $5n/13$, where n is the harmonic number. The ac line inductance L_s is 100 μH.

Design a harmonic trap filter that meets these specifications. Design the best filter you can, which meets the attenuation specifications, that has nearly unity (0 dB ± 1 dB) gain at 50 Hz, and that has minimum gains at the third and ninth harmonics. Plot the frequency response of your filter, and specify your circuit element values.

17.6 A single-phase rectifier operates from a 230 Vrms 50 Hz European single-phase source. The rectifier must supply a 1000 W dc load, and must meet the IEC-1000 class A or class D harmonic current limits. The circuit of Fig. 17.1 is to be used. The dc load voltage may have 100 Hz ripple whose peak-to-peak amplitude is no greater than 5% of the dc voltage component.

(a) Estimate the minimum value of inductance that will meet these requirements.

(b) Specify values of L and C that meet these requirements, and prove (by simulation) that your design is correct.

17.7 Figure 17.31 illustrates a twelve-pulse rectifier, containing six controlled (SCR) devices and six uncontrolled (diode) devices. The dc filter inductance L is large, such that its current ripple is negligible. The SCRs operate with delay angle α. The SCR bridge is driven by a wye-wye connected three-phase transformer circuit, while the diode bridge is driven by a wye-delta connected three-phase transformer circuit. Since both transformer circuits have wye-connected primaries, they can be combined to realize the circuit with a single wye-connected primary.

(a) Determine the rms magnitudes and phases of the line-to-line output voltages of the transformer secondaries $v_{a1'b1'}$ and $v_{a2'b2'}$, as a function of the applied line-line primary voltage v_{ab}.

(b) Sketch the waveforms of the voltages $v_{d1}(t)$ and $v_{d2}(t)$. Label the conduction intervals of each thyristor and diode.

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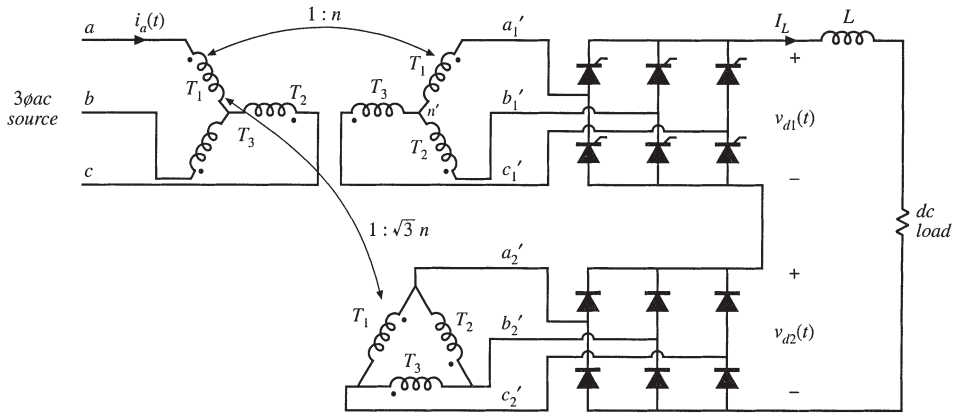


Fig. 17.31 Twelve-pulse rectifier circuit, with one controlled and one uncontrolled bridge, Problem 17.7.

(c) Derive an expression for the dc component of the output voltage, as a function of the rms line-line input voltage, the delay angle α, and the turns ratio n.

(d) Over what range of α is your expression of part (c) valid? What output voltages can be produced by this rectifier?

17.8 For the twelve-pulse rectifier circuit of Fig. 17.27(a), determine the Fourier coefficients, for the fundamental through the thirteenth harmonic, of the primary-side currents $i_{a1}(t)$ and $i_{a2}(t)$, as well as for the ac line current $i_a(t)$. Express your results in terms of the turns ratio n and the dc load current I_L. You may assume that the dc filter inductance L is large and that the transformers are ideal.

17.9 The single-phase controlled-bridge rectifier of Fig. 17.32 operates in the continuous conduction mode. It is desired to regulate the load voltage $v(t)$ in the presence of slow variations in the amplitude of the sinusoidal input voltage $v_g(t)$. Hence, a controller must be designed that varies the delay angle α such that $v(t)$ is kept constant, and it is of interest to derive a small-signal ac model for the dc side of the rectifier circuit.

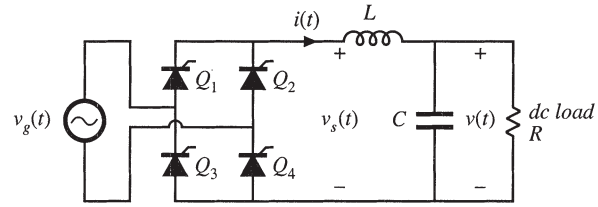


Fig. 17.32 Single-phase controlled rectifier, Problem 17.9.

(a) Sketch $v_s(t)$ and $v_g(t)$, and label the delay angle α.

(b) Use the circuit averaging method to determine the small-signal transfer functions

$$\frac{\hat{v}(s)}{\hat{\alpha}(s)} \quad \text{control-to-output transfer function}$$

and

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$\frac{\hat{v}(s)}{\hat{v}_g(s)}$ line-to-output transfer function

as well as the steady-state relationship

$$V = f(V_g, A)$$

where

$$\alpha(t) = A + \hat{\alpha}(t)$$
$$v(t) = V + \hat{v}(t)$$
$$v_g(t) = \left(V_g + \hat{v}_g(t)\right) \sin(\omega t)$$

You may assume that the frequencies of the variations in α, v, and v_g are much slower that the ac line frequency ω, and that the inductor current ripple is small.

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18

Pulse-Width Modulated Rectifiers

To obtain low ac line current THD, the passive techniques described in the previous chapter rely on low-frequency transformers and/or reactive elements. The large size and weight of these elements are objectionable in many applications. This chapter covers active techniques that employ converters having switching frequencies much greater than the ac line frequency. The reactive elements and transformers of these converters are small, because their sizes depend on the converter switching frequency rather than the ac line frequency.

Instead of making do with conventional diode rectifier circuits, and dealing after-the-fact with the resulting low-frequency harmonics, let us consider now how to build a rectifier that behaves as ideally as possible, without generation of line current harmonics. In this chapter, the properties of the *ideal rectifier* are explored, and a model is described. The ideal rectifier presents an effective resistive load to the ac power line; hence, if the supplied ac voltage is sinusoidal, then the current drawn by the rectifier is also sinusoidal and is in phase with the voltage. Converters that approximate the properties of the ideal rectifier are sometimes called *power factor corrected*, because their input power factor is essentially unity [1].

The boost converter, as well as a variety of other converters, can be controlled such that a near-ideal rectifier system is obtained. This is accomplished by control of a high-frequency switching converter, such that the ac line current waveform follows the applied ac line voltage. Both single-phase and three-phase rectifiers can be constructed using PWM techniques. A typical dc power supply system that is powered by the single-phase ac utility contains three major power-processing elements. First, a high-frequency converter with a wide-bandwidth input-current controller functions as a near-ideal rectifier. Second, an energy-storage capacitor smooths the pulsating power at the rectifier output, and a low-bandwidth controller causes the average input power to follow the power drawn by the load. Finally, a dc–dc converter provides a well-regulated dc voltage to the load. In this chapter, single-phase rectifier systems are discussed, expressions for rms currents are derived, and various converter approaches are compared.

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The techniques developed in earlier chapters for modeling and analysis of dc-dc converters are extended in this chapter to treat the analysis, modeling, and control of low-harmonic rectifiers. The CCM models of Chapter 3 are used to compute the average losses and efficiency of CCM PWM converters operating as rectifiers. The results yield insight that is useful in power stage design. Several converter control schemes are known, including peak current programming, average current control, critical conduction mode control, and nonlinear carrier control. Ac modeling of the rectifier control system is also covered.

18.1 PROPERTIES OF THE IDEAL RECTIFIER

It is desired that the ideal single-phase rectifier present a resistive load to the ac system. The ac line current and voltage will then have the same waveshape and will be in phase. Unity power factor rectification is the result. Thus, the rectifier input current $i_{ac}(t)$ should be proportional to the applied input voltage $v_{ac}(t)$:

$$i_{ac}(t) = \frac{v_{ac}(t)}{R_e} \tag{18.1}$$

where R_e is the constant of proportionality. An equivalent circuit for the ac port of an ideal rectifier is therefore an effective resistance R_e, as shown in Fig. 18.1(a). R_e is also known as the *emulated resistance*. It should be noted that the presence of R_e does not imply the generation of heat: the power apparently

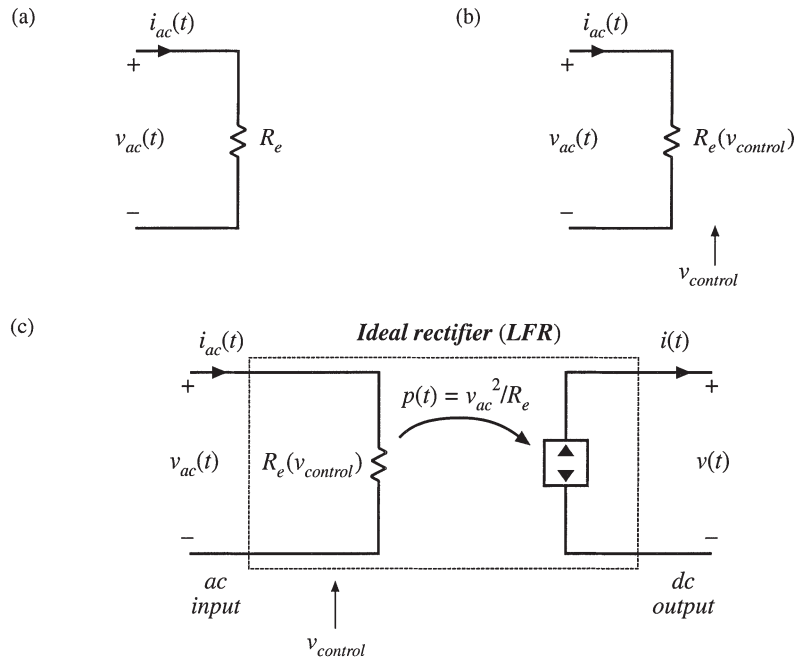


Fig. 18.1 Development of the ideal rectifier equivalent circuit model: (a) input port resistor emulation; (b) the value of the emulated resistance, and hence the power throughput, is controllable; (c) output port power source characteristic, and complete model.

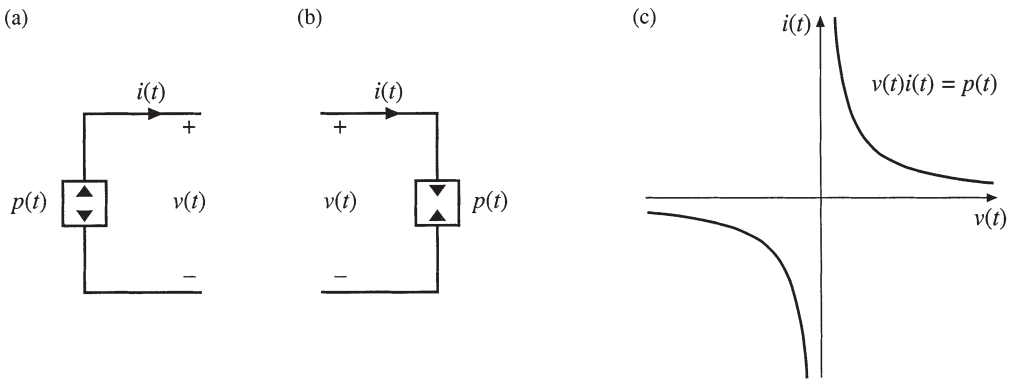


Fig. 18.2 The dependent power source: (a) power source schematic symbol, (b) power sink schematic symbol, (c) *i–v* characteristic.

"consumed" by R_e is actually transferred to the rectifier dc output port. R_e simply models how the ideal rectifier loads the ac power system.

Output regulation is accomplished by variation of the effective resistance R_e, and hence the value of R_e must depend on a control signal $v_{control}(t)$ as in Fig. 18.1(b). This allows variation of the rectifier power throughput, since the average power consumed by R_e is

$$P_{av} = \frac{V_{ac,rms}^2}{R_e(v_{control})} \tag{18.2}$$

Note that changing R_e results in a time-varying system, with generation of harmonics. To avoid generation of significant amounts of harmonics and degradation of the power factor, variations in R_e and in the control input must be slow with respect to the ac line frequency.

To the extent that the rectifier is lossless and contains negligible internal energy storage, the instantaneous power flowing into R_e must appear at the rectifier output port. Note that the instantaneous power throughput

$$p(t) = \frac{v_{ac}^2(t)}{R_e\left(v_{control}(t)\right)} \tag{18.3}$$

is dependent only on $v_{ac}(t)$ and the control input $v_{control}(t)$, and is independent of the characteristics of the load connected to the output port. Hence, the output port must behave as a source of constant power, obeying the relationship

$$v(t)i(t) = p(t) = \frac{v_{ac}^2(t)}{R_e} \tag{18.4}$$

The *dependent power source* symbol of Fig. 18.2(a) is used to denote such an output characteristic. As illustrated in Fig. 18.1(c), the output port is modeled by a power source that is dependent on the instantaneous power flowing into R_e.

Thus, a two-port model for the ideal unity-power-factor single-phase rectifier is as shown in Fig. 18.1(c) [2–4]. The two port model is also called a *loss-free resistor* (LFR) because (1) its input port obeys Ohm's law, and (2) power entering the input port is transferred directly to the output port without loss of

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energy. The defining equations of the LFR are:

$$i_{ac}(t) = \frac{v_{ac}(t)}{R_e\left(v_{control}\right)} \tag{18.5}$$

$$v(t)i(t) = p(t) \tag{18.6}$$

$$p(t) = \frac{v_{ac}^2(t)}{R_e\left(v_{control}(t)\right)} \tag{18.7}$$

When the LFR output port is connected to a resistive load of value R, the dc output rms voltages and currents V_{rms} and I_{rms} are related to the ac input rms voltages and currents $V_{ac,rms}$ and $I_{ac,rms}$ as follows:

$$\frac{V_{rms}}{V_{ac,rms}} = \sqrt{\frac{R}{R_e}} \tag{18.8}$$

$$\frac{I_{ac,rms}}{I_{rms}} = \sqrt{\frac{R}{R_e}} \tag{18.9}$$

The properties of the power source and loss-free resistor network are discussed in Chapter 11. Regardless of the specific converter implementation, any single-phase rectifier having near-ideal properties can be modeled using the LFR two-port model.

18.2 REALIZATION OF A NEAR-IDEAL RECTIFIER

Feedback can be employed to cause a converter that exhibits controlled dc transformer characteristics to obey the LFR equations. In the single-phase case, the simplest and least expensive approach employs a full-wave diode rectifier network, cascaded by a dc–dc converter, as in Fig. 18.3. The dc–dc converter is represented by an ideal dc transformer, as discussed in Chapter 3. A control network varies the duty cycle, as necessary to cause the converter input current $i_g(t)$ to be proportional to the applied input volt-

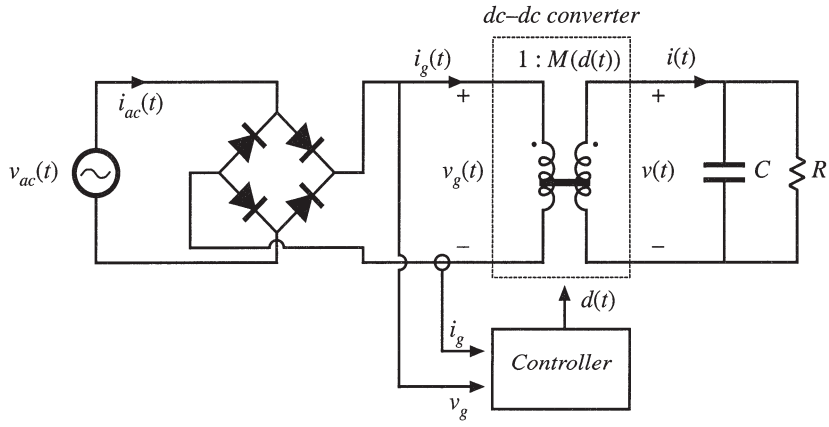


Fig. 18.3 Synthesis of an ideal rectifier by varying the duty cycle of a PWM dc–dc converter.

age $v_g(t)$ as in Eq. (18.1). The effective turns ratio of the ideal transformer then varies with time. Ideal waveforms are illustrated in Fig. 18.4. If the applied input voltage $v_{ac}(t)$ is sinusoidal,

$$v_{ac}(t) = V_M \sin(\omega t) \tag{18.10}$$

then the rectified voltage $v_g(t)$ is

$$v_g(t) = V_M \left| \sin(\omega t) \right| \tag{18.11}$$

It is desired that the converter output voltage be a constant dc value $v(t) = V$. The converter conversion ratio must therefore be

$$M\big(d(t)\big) = \frac{v(t)}{v_g(t)} = \frac{V}{V_M \left| \sin(\omega t) \right|} \tag{18.12}$$

This expression neglects the converter dynamics. As can be seen from Fig. 18.4, the controller must cause the conversion ratio to vary between infinity (at the ac line voltage zero crossings) and some minimum value M_{min} (at the peaks of the ac line voltage waveform). M_{min} is given by

$$M_{min} = \frac{V}{V_M} \tag{18.13}$$

Any converter topology whose ideal conversion ratio can be varied between these limits can be employed in this application.

To the extent that the dc–dc converter is ideal (i.e., if the losses can be neglected and there is negligible low-frequency energy storage), the instantaneous input and output powers are equal. Hence, the output current $i(t)$ in Fig. 18.3 is given by

$$i(t) = \frac{v_g(t) i_g(t)}{V} = \frac{v_g^2(t)}{V R_e} \tag{18.14}$$

Substitution of Eq. (18.11) into Eq. (18.14) then leads to

$$\begin{aligned} i(t) &= \frac{V_M^2}{V R_e} \sin^2(\omega t) \\ &= \frac{V_M^2}{2 V R_e} \big(1 - \cos(2\omega t)\big) \end{aligned} \tag{18.15}$$

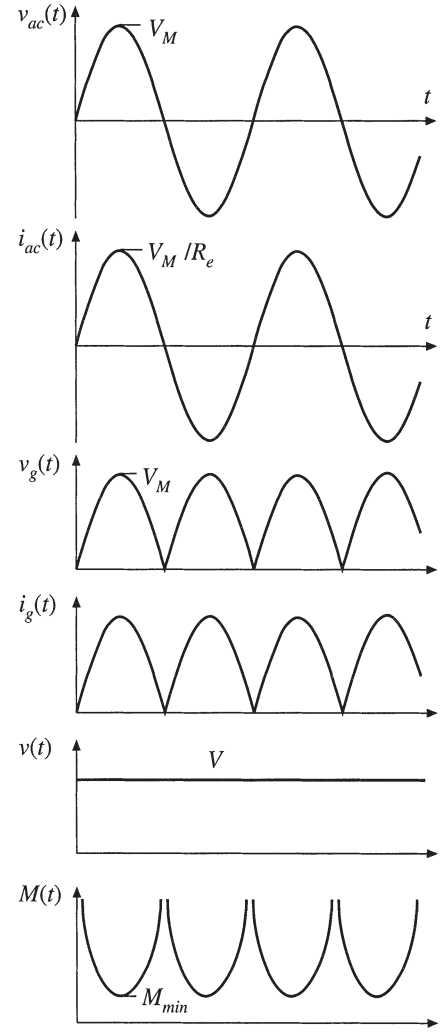


Fig. 18.4 Waveforms of the rectifier system of Fig. 18.3.

Hence, the converter output current contains a dc component and a component at the second harmonic of the ac line frequency. One of the functions of capacitor C in Fig. 18.3 is to filter out the second harmonic component of $i(t)$, so that the load current (flowing through resistor R) is essentially equal to the dc component

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$$I = \langle i(t) \rangle_{T_L} = \frac{V_M^2}{2VR_e} \tag{18.16}$$

where T_L is the period of the applied ac line voltage.

The average power is

$$P = \frac{V_M^2}{2R_e} \tag{18.17}$$

The above equations are generally valid for PWM converters used as single-phase low-harmonic rectifiers.

18.2.1 CCM Boost Converter

A system based on the CCM boost converter is illustrated in Fig. 18.5 [1,5,6]. Ideally, the boost converter can produce any conversion ratio between one and infinity. Hence, the boost converter is capable of producing the $M(d(t))$ given by Eq. (18.12), provided that $V \geq V_M$. Further, the boost converter can produce very low THD, with better transistor utilization than other approaches.

If the boost converter operates in continuous conduction mode, and if the inductor is small enough that its influence on the low-frequency components of the converter waveforms is negligible, then the duty ratio should follow $M(d(t)) = 1/(1 - d(t))$. This implies that the duty ratio should follow the function

$$d(t) = 1 - \frac{v_g(t)}{V} \tag{18.18}$$

This expression is true only in the continuous conduction mode. The boost converter operates in the continuous conduction mode provided that the inductor current ripple

$$\Delta i_g(t) = \frac{v_g(t)d(t)T_s}{2L} \tag{18.19}$$

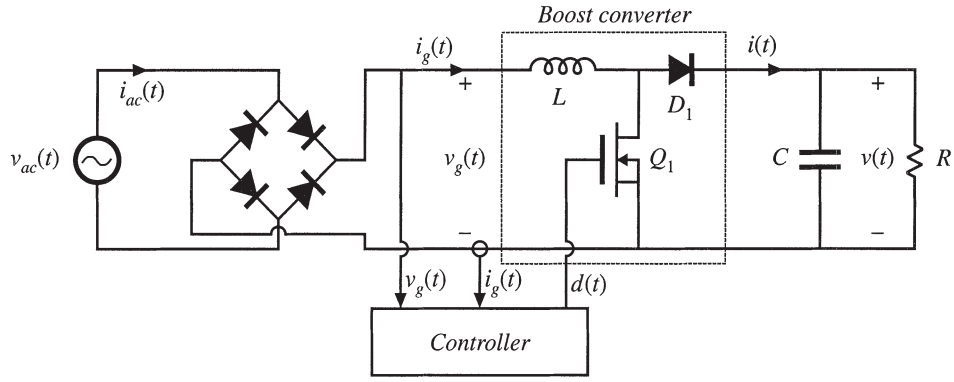


Fig. 18.5 Rectifier system based on the boost converter.

is greater than the average inductor current, or

$$\left\langle i_g(t)\right\rangle_{T_s} = \frac{v_g(t)}{R_e} \tag{18.20}$$

Hence, the converter operates in CCM when

$$\left\langle i_g(t)\right\rangle_{T_s} > \Delta i_g(t) \;\Rightarrow\; d(t) < \frac{2L}{R_e T_s} \tag{18.21}$$

Substitution of Eq. (18.18) into (18.21) and solution for R_e leads to

$$R_e < \frac{2L}{T_s\left(1 - \dfrac{v_g(t)}{V}\right)} \quad \text{for CCM} \tag{18.22}$$

Since $v_g(t)$ varies according to Eq. (18.11), Eq. (18.22) may be satisfied at some points on the ac line cycle, and not at others. Since $0 \le v_g(t) \le V_M$, we can conclude that the converter operates in CCM over the entire ac line cycle when

$$R_e < \frac{2L}{T_s} \tag{18.23}$$

Equations (18.18) and (18.22) then hold for all t. The converter always operates in DCM when

$$R_e > \frac{2L}{T_s\left(1 - \dfrac{V_M}{V}\right)} \tag{18.24}$$

For R_e between these limits, the converter operates in DCM when $v_g(t)$ is near zero, and in CCM when $v_g(t)$ approaches V_M.

The static input characteristics of the open-loop boost converter are sketched in Fig. 18.6. The input current $i_g(t)$ is plotted vs. input voltage $v_g(t)$, for various duty cycles $d(t)$. In CCM, the input characteristics of the boost converter are described by

$$\frac{v_g(t)}{V} = 1 - d(t) \qquad \text{in CCM} \tag{18.25}$$

To obtain a general plot, we can normalize the input current and input voltage as follows:

$$m_g(t) = \frac{v_g(t)}{V} \tag{18.26}$$

$$j_g(t) = \frac{2L}{VT_s}\, i_g(t) \tag{18.27}$$

Equation (18.25) then becomes

$$m_g(t) = 1 - d(t) \tag{18.28}$$

This equation is independent of the input current $i_g(t)$, and hence is represented by vertical lines in Fig.

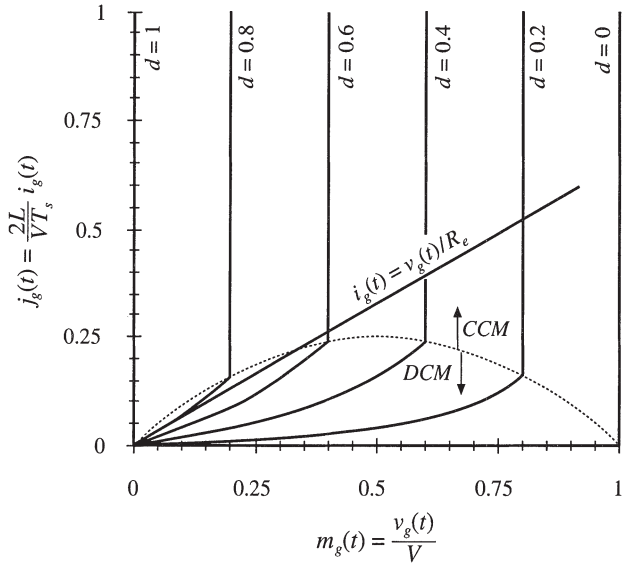


Fig. 18.6 Static input characteristics of the boost converter. A typical linear resistive input characteristic is superimposed.

18.6.

To derive the boost input characteristic for DCM operation, we can solve the steady-state equivalent circuit model of Fig. 11.12(b) (reproduced in Fig. 18.7). *Beware*: the natural DCM effective resistance of Chapter 11, $R_e = 2L/d^2T_s$, does not necessarily coincide with the emulated resistance $R_e = v_g/i_g$ of Eq. (18.1). In this chapter, the quantity R_e is defined according to Eq. (18.1). Solution of Fig. 18.7 for the input current $i_g(t)$ leads to:

$$i_g(t) = \frac{v_g(t)}{\left(\frac{2L}{d^2T_s}\right)} + \frac{p(t)}{V - v_g(t)} \tag{18.29}$$

The instantaneous power consumed by the effective resistor in the model of Fig. 18.7 is

$$p(t) = \frac{v_g^2(t)}{\left(\frac{2L}{d^2T_s}\right)} \tag{18.30}$$

Substitution of Eq. (18.30) into Eq. (18.29) and simplification leads to

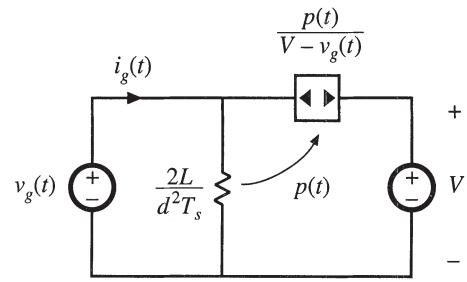


Fig. 18.7 Averaged equivalent circuit model of the boost converter operating in DCM, derived in Chapter 11.

$$\frac{2L}{VT_s} i_g(t) \left(1 - \frac{v_g(t)}{V}\right) = d^2(t) \frac{v_g(t)}{V} \qquad \text{in DCM} \qquad (18.31)$$

Normalization of this equation according to Eqs. (18.26) and (18.27) yields

$$j_g(t)\left(1 - m_g(t)\right) = d^2 m_g(t) \qquad (18.32)$$

This equation describes the curved (DCM) portions of the Fig. 18.6 input characteristics, for low $i_g(t)$.

To express the CCM/DCM mode boundary as a function of $v_g(t)$ and $i_g(t)$, Eqs. (18.1) and (18.22) can be combined, leading to

$$\frac{2L}{VT_s} i_g(t) > \left(\frac{v_g(t)}{V}\right)\left(1 - \frac{v_g(t)}{V}\right) \qquad \text{for CCM} \qquad (18.33)$$

Normalization of this equation, according to Eqs. (18.26) and (18.27), results in

$$j_g(t) > m_g(t)\left(1 - m_g(t)\right) \qquad \text{for CCM} \qquad (18.34)$$

This equation describes a parabola having roots at $m_g = 0$ and $m_g = 1$, with the maximum value $j_g = 0.25$ at $m_g = 0.5$. The mode boundary equation is plotted as a dashed line in Fig. 18.6

The complete input characteristics for the boost converter were plotted in Fig. 18.6 using Eqs. (18.28), (18.32), and (18.34). Figure 18.6 also illustrates the desired linear resistive input characteristic, Eq. (18.1). For the value of R_e illustrated, the converter operates in DCM for $v_g(t)$ near zero, and in CCM for $v_g(t)$ near V_M. The intersections of boost input characteristics with the desired linear input characteristic illustrate how the controller must choose the duty cycle at various values of $v_g(t)$.

Other converters capable of producing the $M(d(t))$ of Eq. (18.12) include the buck-boost, SEPIC, and Ćuk converters. The boost, SEPIC, and Ćuk converters share the desirable property of nonpulsating input current, and hence require minimal input EMI filtering. The SEPIC produces a non inverted output voltage. Isolated versions of these converters (see Chapter 6) are also sometimes employed [7–9]. Schemes involving the parallel resonant converter, as well as several types of quasi-resonant converters, are also documented in the literature [10–13].

The open-loop boost converter, when operated in discontinuous conduction mode, is also sometimes used as an approximation of an ideal rectifier. The DCM effective resistance $2L/d^2(t)T_s$ of Fig. 18.7 is then taken as an approximation of the desired emulated resistance of Eq. (18.1). The model differs from that of the ideal rectifier model of Fig. 18.1(c) in that the power source is connected between the input and output terminals. As a result, harmonics are present in the input current waveform. For example, if $v_g(t)$ is a rectified sinusoid, then the current through the effective resistance $2L/d^2(t)T_s$ will also be a rectified sinusoid. However, the input current $\langle i_g(t)\rangle_{T_s}$ is now equal to the sum of the current through R_e and the current flowing through the power source element. Since the power source is a nonlinear element, $\langle i_g(t)\rangle_{T_s}$ contains harmonics. For large C, the output voltage is essentially constant. The input current waveform is then given by Eq. (18.31). If V is sufficiently large, then the term $(1 - v_g(t)/V)$ is approximately equal to one, and the harmonics in $\langle i_g(t)\rangle_{T_s}$ are small. The zero crossings of $v_g(t)$, $p(t)$, and $\langle i_g(t)\rangle_{T_s}$ coincide. So although the DCM boost converter generates some current harmonics, it is nonetheless possible to construct a low harmonic rectifier that meets harmonic limits. Again, this approach has the disadvantages of the increased peak currents of DCM, and the need for additional filtering of the high-frequency pulsating input currents. Computer simulation of a DCM boost rectifier is described in Appendix B, Section B.2.3.

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A similar approach is to operate the boost converter at the boundary between the continuous and discontinuous conduction modes. This approach is known as "critical conduction mode" operation. It eliminates the distortion mechanism described above, but requires variable switching-frequency control. This approach is quite popular at low power levels, and is described further in Section 18.3.3.

Other converters not capable of producing the $M(d(t))$ of Eq. (18.12), such as the buck converter, are sometimes employed as the dc–dc converter of Fig. 18.3. Distortion of the ac line current waveform must then occur. Nonetheless, at low power levels it may be possible to meet the applicable ac line current harmonic standards using such an approach.

18.2.2 DCM Flyback Converter

In Chapter 11, the loss-free resistor network is used to model converters operating in discontinuous conduction mode. This suggests that DCM converters can also be used as near-ideal rectifiers. Indeed, the buck-boost, flyback, SEPIC, and Ćuk converters, when operated in discontinuous conduction mode without additional control, inherently behave as natural loss-free resistors. The DCM effective resistance R_e, found in Chapter 11 to be equal to $2L/D^2T_s$, then coincides with the rectifier emulated resistance of Eq. (18.1). At low power levels, this can be an effective and low-cost approach. Inrush current limiting is also inherent in this approach, and isolation and scaling via a turns ratio are provided by the transformer. Disadvantages are the increased peak currents of DCM, and the need for additional filtering of the high-frequency pulsating input currents.

A simple low-harmonic rectifier system based on the transformer-isolated flyback converter is illustrated in Fig. 18.8 [2]. The ac line voltage is connected through an input EMI filter to a bridge rectifier and a flyback converter. The flyback converter is operated at constant switching frequency f_s and constant duty cycle D. The converter is designed such that it operates in the discontinuous conduction mode under all conditions. The input EMI filter smooths the pulsating input current waveform, so that $i_{ac}(t)$ is approximately sinusoidal.

The flyback converter is replaced by its averaged equivalent circuit in Fig. 18.9. As discussed in Chapter 11, the terminal waveforms of the flyback converter have been averaged over the switching period T_s, resulting in the loss-free resistor model. This model illustrates how the DCM flyback converter presents a resistive load to the ac input. It also illustrates how the power flow can be controlled, by varia-

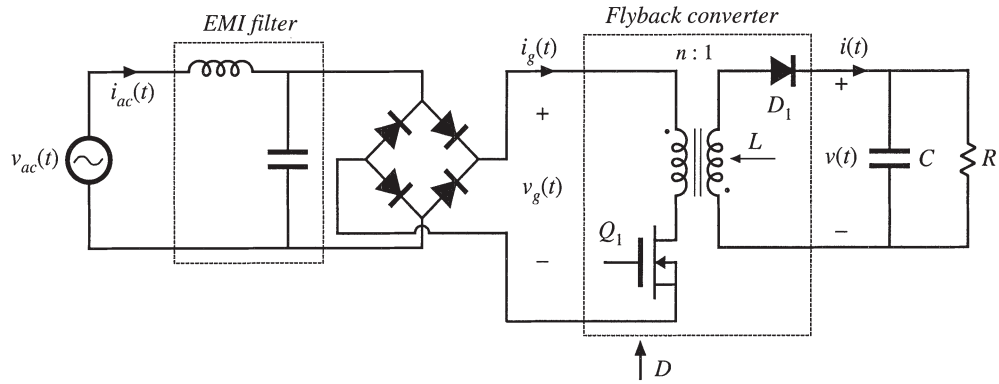


Fig. 18.8 Low-harmonic rectifier system incorporating a flyback converter that operates in the discontinuous conduction mode.

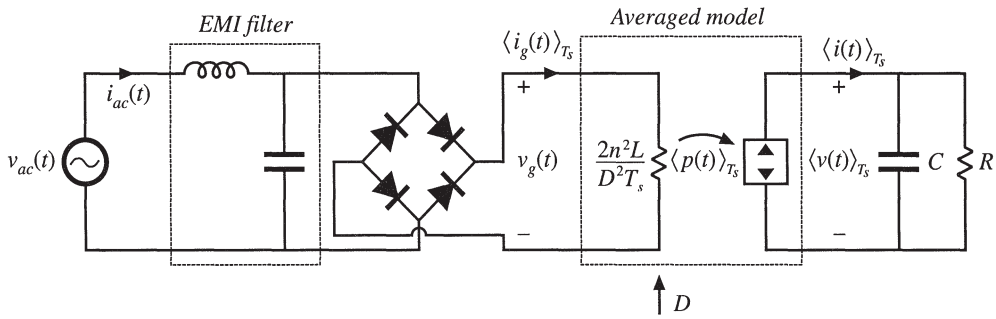


Fig. 18.9 Averaged equivalent circuit that models the system of Fig. 18.8.

tion of D to control the value of the emulated resistance R_e.

To design this converter, one must select the value of inductance to be sufficiently small, such that the converter operates in DCM at all points on the ac sine wave, at maximum load. If we denote the lengths of the transistor conduction interval, diode conduction interval, and discontinuous interval as DT_s, d_2T_s, and d_3T_s, respectively, then the converter operates in DCM provided that d_3 is greater than zero. This implies that

$$d_2(t) < 1 - D \tag{18.35}$$

By volt-second balance on the transformer magnetizing inductance, we can express $d_2(t)$ as

$$d_2(t) = D\frac{v_g(t)}{nV} \tag{18.36}$$

Substitution of Eq. (18.36) into Eq. (18.35) and solution for D yields

$$D < \frac{1}{\left(1 + \frac{v_g(t)}{nV}\right)} \tag{18.37}$$

During a given switching period, the converter will operate in DCM provided that the above inequality is satisfied. The worst case occurs when the rectified sinusoid $v_g(t)$ is equal to its peak value V_M. The inequality then becomes

$$D < \frac{1}{\left(1 + \frac{V_M}{nV}\right)} \tag{18.38}$$

If Eq. (18.38) is satisfied, then the converter operates in DCM at all points on the ac line sinusoid.

In steady state, the dc output voltage is given by Eq. (18.8). Upon substitution of the expression for R_e and solution for D, this equation becomes

$$D = \frac{2nV}{V_M}\sqrt{\frac{L}{RT_s}} \tag{18.39}$$

Insertion of this relationship into Eq. (18.38), and solution for L, yields

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$$L < L_{crit} = \frac{RT_s}{4\left(1 + \frac{nV}{V_M}\right)^2} \tag{18.40}$$

For variations in load R and peak ac input voltage V_M, the worst case will occur at minimum R (maximum power) and minimum V_M. Hence, the designer should choose L to satisfy

$$L < L_{crit\text{-}min} = \frac{R_{min}T_s}{4\left(1 + \frac{nV}{V_{M\text{-}min}}\right)^2} \tag{18.41}$$

If this equation is violated, then at maximum load power and minimum input voltage amplitude, the convert will operate in CCM near the peak of the ac sinewave. This will lead to an input current waveform having substantial distortion.

18.3 CONTROL OF THE CURRENT WAVEFORM

A wide variety of approaches are known for active control of the input current waveform to attain input resistor emulation [14–33]. Average current control [17,18], input voltage feedforward [17], current-programmed control [19–22], hysteretic control and critical conduction mode control [23–27], and nonlinear carrier control [28–30] are briefly surveyed here. Other approaches include sliding-mode control [31], charge control [32], and ASDTIC control [33].

18.3.1 Average Current Control

Average current control is a popular method of implementing control of the input current waveform in a low-harmonic rectifier. This approach works in both continuous and discontinuous conduction modes, and can produce high-quality current waveforms over a wide range of input voltages and load powers. The problems of crossover distortion, found in some competing schemes such as current programmed control, are largely avoided. Several popular integrated circuits are available that implement average current control.

Figure 18.10 illustrates average current control of the input current waveform $\langle i_g(t)\rangle_{T_s}$ in a boost converter. The input current $i_g(t)$ flows through a shunt resistor. The voltage across this shunt resistor is amplified by an op amp circuit. This op amp circuit contains a low-pass filter characteristic that attenuates the high-frequency switching harmonics. The output voltage $v_a(t)$ of the op amp circuit is proportional to the low-frequency average value of $i_g(t)$:

$$v_a(t) = R_s\left\langle i_g(t)\right\rangle_{T_s} \tag{18.42}$$

This signal is compared to the reference voltage $v_r(t)$, to produce an error signal that drives the compensator network and pulse-width modulator as illustrated. If the feedback loop is well designed, then the error signal is small:

$$v_a(t) \approx v_r(t) \tag{18.43}$$

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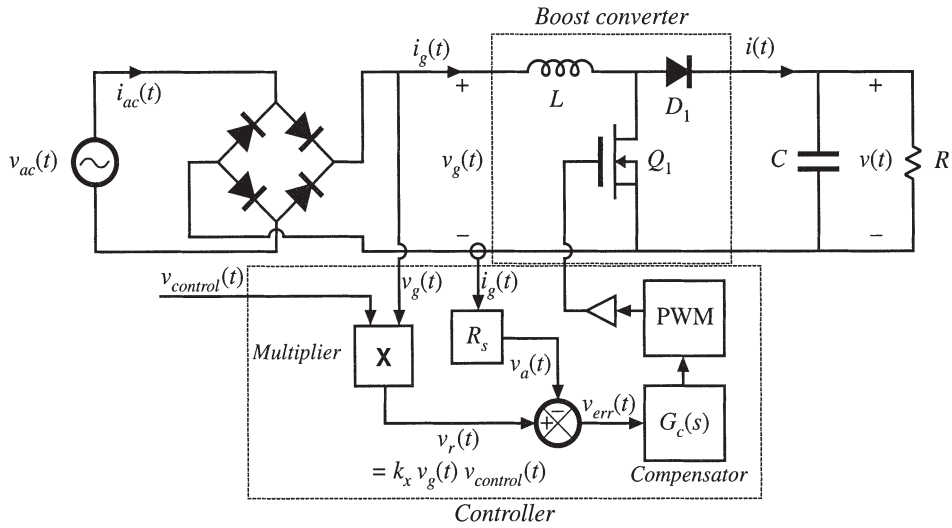


Fig. 18.11 Average current control of a boost converter, to obtain a low-harmonic rectifier.

The average current controller causes the sensed current $i_g(t)$ to follow the reference waveform $v_r(t)$.

To cause the input current to be proportional to the input voltage, the reference voltage $v_r(t)$ is derived from the sensed input voltage waveform, as in Fig. 18.11. The current reference signal $v_r(t)$ is derived from the sensed input voltage $v_g(t)$, and hence has a sinusoidal waveshape. Hence, the average current controller causes the average input current $i_g(t)$ to be proportional to the input voltage $v_g(t)$. The multiplier illustrated in Fig. 18.11 allows adjustment of the constant of proportionality, so that the magnitude of the emulated resistance can be controlled via a control signal $v_{control}(t)$. Let us assume that the multiplier terminal equations are

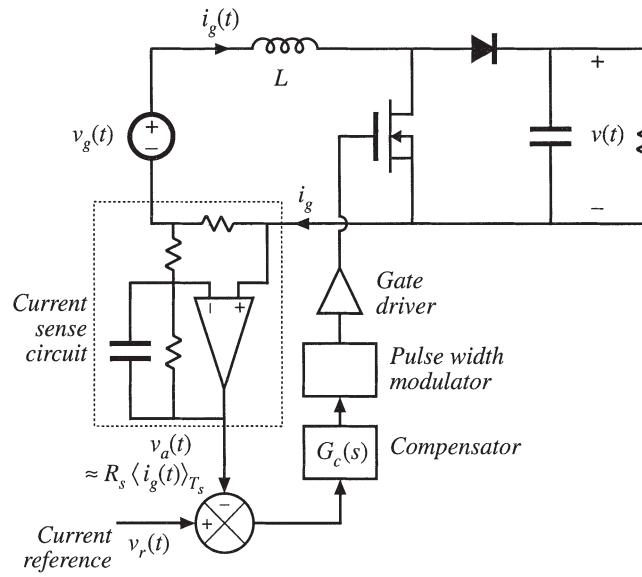


Fig. 18.10 Average current control of the input current in a boost converter.

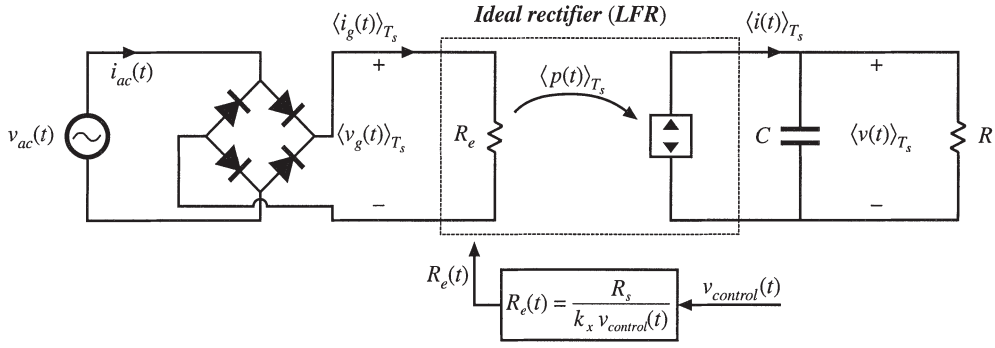


Fig. 18.12 Model of the system of Fig. 18.5, based on the loss-free resistor model of Fig. 18.1(c), which predicts the low-frequency system waveforms. This model assumes that the feedback loop of Fig. 18.5 operates ideally.

$$v_r(t) = k_x v_g(t)\, v_{control}(t) \tag{18.44}$$

Then the emulated resistance is

$$R_e = \frac{v_g(t)}{i_g(t)} = \frac{\left(\dfrac{v_r(t)}{k_x v_{control}(t)}\right)}{\left(\dfrac{v_a(t)}{R_s}\right)} \tag{18.45}$$

Here, Eqs. (18.44) and (18.42) have been used to eliminate v_g and i_g. Substitution of Eq. (18.43) leads to the result

$$R_e\left(v_{control}(t)\right) = \frac{R_s}{k_x v_{control}(t)} \tag{18.46}$$

Hence, if the feedback loop is well designed, then the system of Fig. 18.11 can be represented by the LFR model as in Fig. 18.12. The average current controller scheme of Fig. 18.11 and the model of Fig. 18.12 are independent of the dc–dc converter topology, and can be applied to systems containing CCM boost, buck-boost, Ćuk, SEPIC, and other topologies.

Average power flow and the output voltage are regulated by variation of the emulated resistance R_e, in average current control as well as in most other schemes. This is usually accomplished by use of a multiplier in the input voltage sensing path, as shown in Fig. 18.13. This control loop continually adjusts R_e to maintain balance of the average rectifier power $P_{av} = V_{g,rms}^2 / R_e$ and the load power P_{load}, such that the following relation is obeyed:

$$P_{av} = \frac{V_{g,rms}^2}{R_e} = P_{load} \tag{18.47}$$

Average current control works quite well. Its only disadvantages are the need to sense the average input current, rather than the transistor current, and the need for a multiplier in the controller circuit.

Most average current control implementations include provisions for feedforward of the input voltage amplitude. This allows disturbances in the ac input voltage amplitude to be canceled out by the

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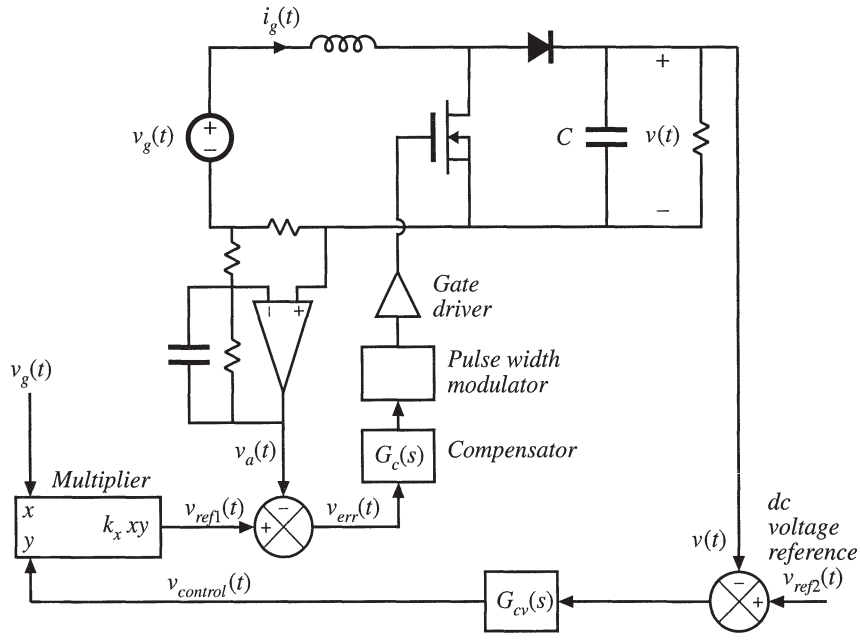


Fig. 18.13 Average current control incorporating a multiplier for regulation of the output voltage.

controller, such that the dc output voltage is unaffected.

Combination of Eqs. (18.44), (18.46), and (18.47), and solution for $v_{ref1}(t)$ leads to

$$v_{ref1}(t) = \frac{P_{av} v_g(t) R_s}{V_{g,rms}^2} \tag{18.48}$$

This equation shows how the reference voltage should be varied to maintain a given rectifier average power throughput P_{av}. Apparently, it is necessary to divide by the square of the rms input voltage amplitude. A controller that implements Eq. (18.48) is illustrated in Fig. 18.14. The multiplier block of Fig. 18.13 has been generalized to perform the function $k_v xy/z^2$. It is somewhat complicated to compute the rms value of a general ac waveform; however, the ac input voltage $v_g(t)$ normally is sinusoidal with negligible harmonics. Hence, the peak value of $v_g(t)$ is directly proportional to its rms value, and we can use the peak value V_M in place of $V_{g,rms}$. So the controller of Fig. 18.14 produces the reference voltage

$$v_{ref1}(t) = \frac{k_v v_{control}(t) v_g(t)}{V_M^2} \tag{18.49}$$

Comparison of Eqs. (18.48) and (18.49) leads to the conclusion that

$$P_{av} = \frac{k_v v_{control}(t)}{2R_s} \tag{18.50}$$

So the average power throughput is directly controlled by $v_{control}(t)$, and is independent of the input voltage $v_g(t)$.

Feedforward can cause the rectifier dc output voltage to be less sensitive to variations in the ac

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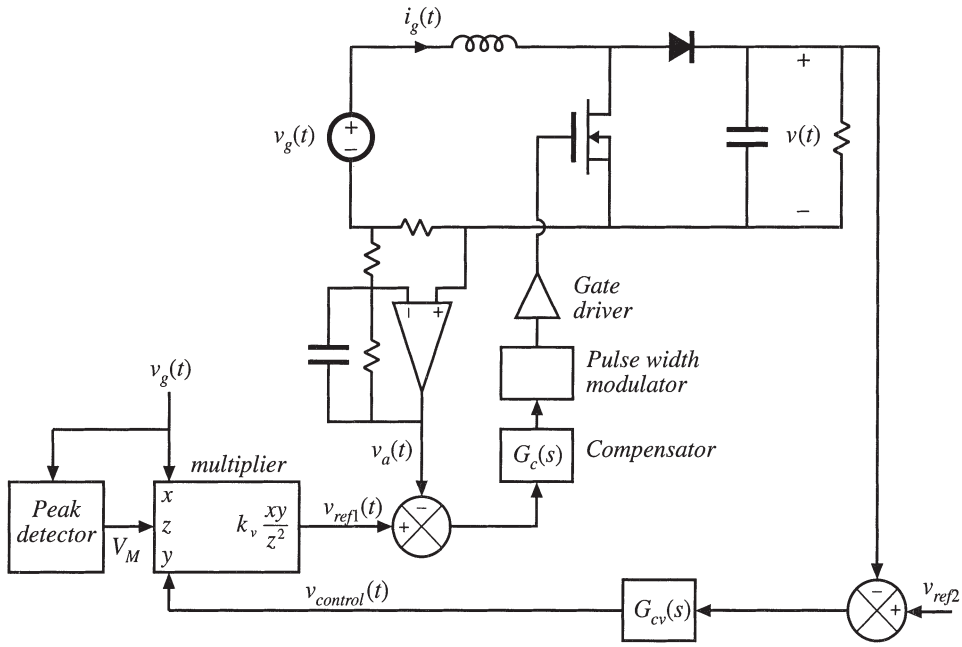


Fig. 18.14 Average current control incorporating input voltage feedforward.

line voltage. A disadvantage is the ac line current distortion introduced by variations in the voltage produced by the peak detector.

To aid in the design of the inner feedback loop that controls the ac line current waveshape, a converter model is needed that describes how the converter average input current depends on the duty cycle. We would prefer to apply the averaged small-signal modeling techniques of Chapter 7 here. The problem is that the variations in the duty cycle $d(t)$, as well as in the ac input voltage $v_g(t)$ and current $i_g(t)$, are not small. As a result, in general the small-signal assumptions are violated, and we are faced with the design of a control system that exhibits significant nonlinear time-varying behavior.

When the rectifier operates near periodic steady state, the output voltage $v(t)$ of a well-designed system exhibits small variations. So we can write

$$\langle v(t) \rangle_{T_s} = V + \hat{v}(t) \tag{18.51}$$

with

$$|\hat{v}(t)| \ll |V| \tag{18.52}$$

In other words, the small-signal assumption continues to be valid with respect to the rectifier output voltage. In the case of the boost converter, this allows us to linearize the converter input characteristics.

Following the approach of Chapter 7, we can express the average inductor voltage of the boost converter as

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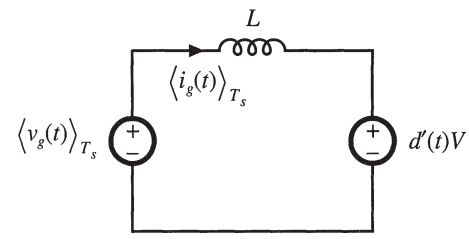


Fig. 18.15 Linearized model describing the boost converter input characteristics, corresponding to Eq. (18.55)

$$L \frac{d\langle i_g(t) \rangle_{T_s}}{dt} = \langle v_g(t) \rangle_{T_s} - d'(t) \langle v(t) \rangle_{T_s} \tag{18.53}$$

This equation contains the nonlinear term $d'(t) \langle v(t) \rangle_{T_s}$. Substitution of Eq. (18.51) into (18.53) yields

$$L \frac{d\langle i_g(t) \rangle_{T_s}}{dt} = \langle v_g(t) \rangle_{T_s} - d'(t) V - d'(t) \hat{v}(t) \tag{18.54}$$

When Eq. (18.52) is satisfied, then the nonlinear term $- d'(t)\hat{v}(t)$ is much smaller in magnitude than the linear term $- d'(t)V$. Therefore, we can discard the nonlinear term to obtain

$$L \frac{d\langle i_g(t) \rangle_{T_s}}{dt} = \langle v_g(t) \rangle_{T_s} - d'(t) V \tag{18.55}$$

This linear differential equation is valid even though $i_g(t)$, $v_g(t)$, and $d(t)$ contain large variations.

An equivalent circuit corresponding to Eq. (18.55) is given in Fig. 18.15. The averaged control-to-input-current transfer function is found by setting the independent inputs other than $d(t)$ to zero, and then solving for i_g; the model predicts that this transfer function is

$$\frac{i_g(s)}{d(s)} = \frac{V}{sL} \tag{18.56}$$

where $i_g(s)$ is the Laplace transform of $\langle i_g(t) \rangle_{T_s}$. So the input characteristics of the boost rectifier can be linearized, even though the ac input variations are not small.

Unfortunately, Eq. (18.52) is not sufficient to linearize the equations describing the input characteristics of the buck-boost, SEPIC, Ćuk, and most other single-phase rectifiers. The control system design engineer must then deal with a truly nonlinear time-varying dynamical system.

One approach that is sometimes suggested employs the *quasi-static approximation* [34,35]. It is assumed that the ac line variations are much slower than the rectifier system dynamics, such that the rectifier always operates near equilibrium. The quiescent operating point changes slowly along the input sinusoid; an equilibrium analysis can be performed to find expressions for the slowly-varying "equilibrium" duty ratio and converter voltages and currents. The small-signal dc–dc converter transfer functions derived in Chapters 7 and 8 are evaluated using this time-varying operating point. The converter poles, zeroes, and gains are found to vary along the ac input sinusoid. An average current controller is designed using these time-varying transfer functions, such that the current loop gain has a positive phase margin at all operating points.

We expect that the quasi-static approximation should be valid if the rectifier system dynamics are sufficiently fast, and it is reasonable to anticipate that high-frequency PWM converters have dynam-

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ics that are much faster than the ac line frequency. The problem is that no good condition on system parameters, which can justify the approximation, is known for the basic converter topologies. There is room for additional research in this area.

It is well-understood in the field of control systems that, when the rectifier system dynamics are not sufficiently fast, the quasi-static approximation yields neither sufficient nor necessary conditions for stability of the resulting design. Time-varying "loop gains" that always have a positive phase margin may nonetheless be unstable, and a negative phase margin does not always imply instability. Such phenomena are sometimes observed in rectifier systems. Even worse, it is difficult to justify the use of the Laplace transform on rectifiers described by time-varying differential equations, unless the quasi-static approximation can be validated.

18.3.2 Current Programmed Control

Another well-known approach to attaining input resistor emulation is the use of current-programmed control. As illustrated in Fig. 18.16, the programmed current $i_c(t)$ is made proportional to the ac input voltage. This causes the average inductor current, and hence also $\langle i_g(t) \rangle_{T_s}$, to approximately follow $v_g(t)$. As in average current control, a multiplier is used to adjust the emulated resistance and average power flow; the control signal $v_{control}(t)$ is typically used to stabilize the dc output voltage magnitude. Several rectifier control ICs are commercially available, which implement current-programmed control.

As discussed in Chapter 12, several mechanisms cause the average inductor current and hence also $\langle i_g(t) \rangle_{T_s}$ to differ from the programmed $i_c(t)$. These mechanisms introduce crossover distortion and line current harmonics. An artificial ramp having sufficiently large slope m_a is necessary to stabilize the

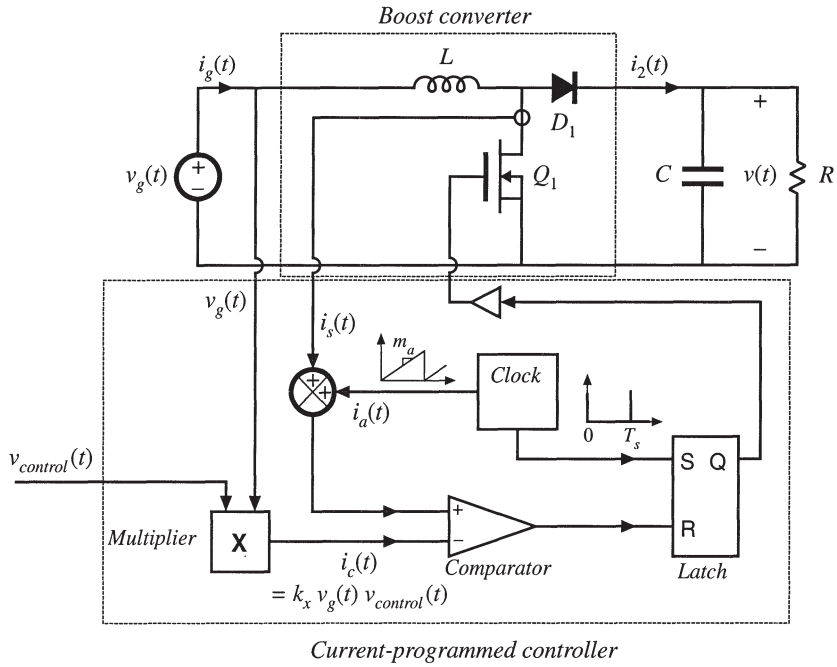


Fig. 18.16 Current-programmed control of a boost rectifier.

current-programmed boost converter when it operates in CCM with $d(t) > 0.5$. The addition of this ramp causes $\langle i_g(t) \rangle_{T_s}$ to differ from $i_c(t)$. Additional deviation is introduced by the inductor current ripple. Both mechanisms are most pronounced when the inductor current is small, near the zero-crossings of the ac line waveforms.

The static input characteristics, that is, the average input current vs. the input voltage, of the current-programmed boost converter are given by

$$\left\langle i_g(t) \right\rangle_{T_s} = \begin{cases} v_g(t) \dfrac{L i_c^2(t) f_s V}{2\left(V - v_g(t)\right)\left(v_g(t) + m_a L\right)^2} & \text{in DCM} \\ i_c(t) - \left(1 - \dfrac{v_g(t)}{V}\right)\left(m_a + \dfrac{v_g(t)}{2L}\right) T_s & \text{in CCM} \end{cases} \tag{18.57}$$

The converter operates in the continuous conduction mode when

$$\left\langle i_g(t) \right\rangle_{T_s} > \frac{T_s V}{2L} \frac{v_g(t)}{V} \left(1 - \frac{v_g(t)}{V}\right) \tag{18.58}$$

In terms of the control current $i_c(t)$, the condition for operation in CCM can be expressed

$$i_c(t) > \frac{T_s V}{L} \left(\frac{m_a L}{V} + \frac{v_g(t)}{V}\right)\left(1 - \frac{v_g(t)}{V}\right) \tag{18.59}$$

In the conventional current-programmed rectifier control scheme, the control current $i_c(t)$ is simply proportional to the ac input voltage:

$$i_c(t) = \frac{v_g(t)}{R_e} \tag{18.60}$$

where R_e is the emulated resistance that would be obtained if the average input current exactly followed the reference current $i_c(t)$. The static input characteristics given by Eqs. (18.57) to (18.60) are plotted in Fig. 18.17. The average input current $\langle i_g(t) \rangle_{T_s}$ is plotted as a function of the applied input voltage $v_g(t)$, for several values of emulated resistance R_e. The region near the CCM–DCM boundary is shown. The curves are plotted for a fixed artificial ramp having slope

$$m_a = \frac{V}{2L} \tag{18.61}$$

This is the minimum value of artificial ramp that stabilizes the boost current-programmed controller at all static operating points. Decreasing m_a below this value leads to instability at operating points in the continuous conduction mode at low $v_g(t)/V$.

To obtain resistor emulation, it is desired that the static input characteristics be linear and pass through the origin. It can be seen from Fig. 18.17 that this is not the case: the curves are reasonably linear in the continuous conduction mode, but exhibit significant curvature as the CCM–DCM boundary is approached. The resulting average current waveforms are summarized in Fig. 18.8.

To minimize the line current THD, it is apparent that the converter should be designed to operate deeply in the continuous conduction mode for most of the ac line cycle. This is accomplished with emulated resistances R_e that are much smaller than $R_{base} = 2L/T_s$. In addition, the artificial ramp slope m_a

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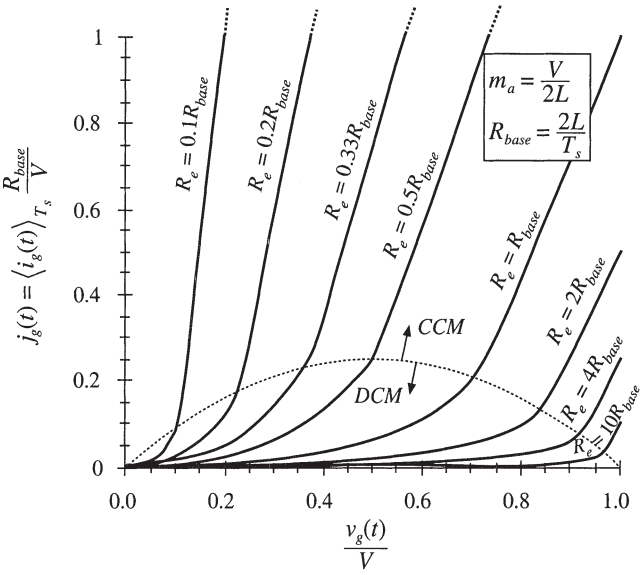


Fig. 18.17 Static input characteristics of a current-programmed boost converter, with minimum stabilizing artificial ramp of Eq. (18.61).

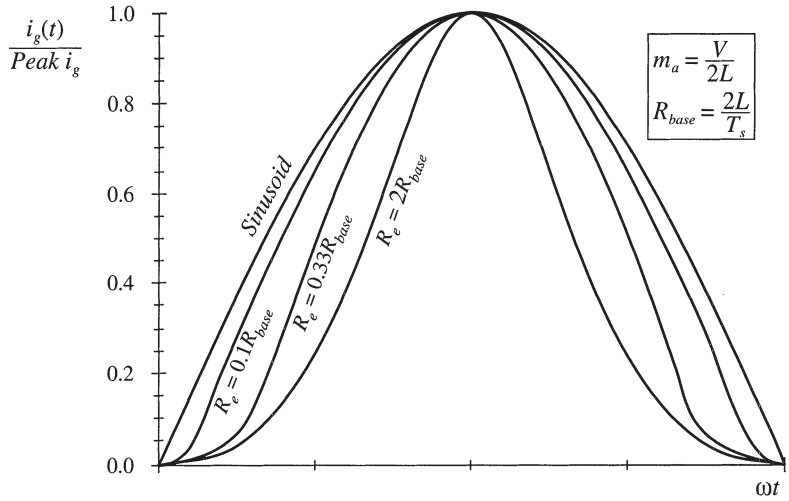


Fig. 18.18 Input current waveshapes predicted by the static input characteristics of Fig. 18.17, compared with a pure sinusoid. Curves are plotted for the case $V_M = 0.8V$, with minimum stabilizing artificial ramp.

should be no greater than otherwise necessary. In practice, THD of 5% to 10% can easily be obtained in rectifiers that function over a narrow range of rms input voltages and load currents. However, low THD cannot be obtained at all operating points in universal-input rectifiers; THD of 20% to 50% may be observed at maximum ac input voltage. This problem can be solved by biasing the current reference waveform. Design of current-programmed rectifiers is discussed in [19–22], and some strategies for solving this problem are addressed in [19].

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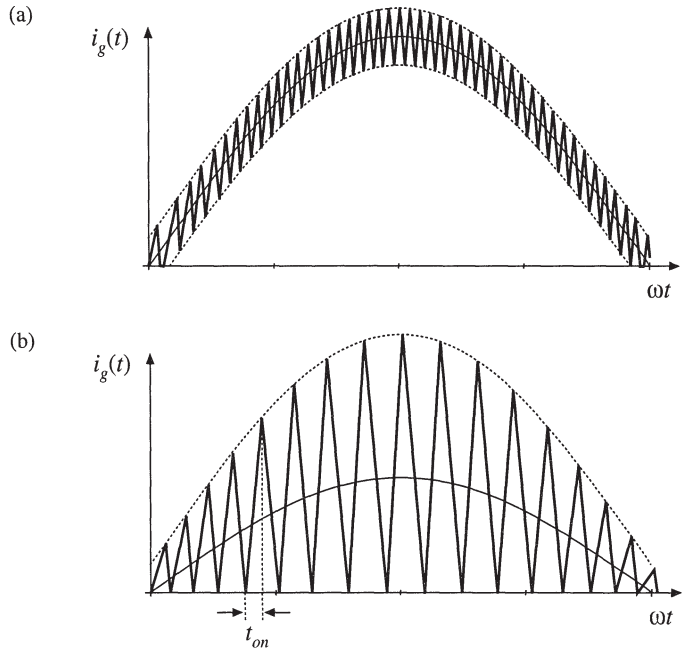


Fig. 18.19 Input current waveforms of two boost converters with hysteretic control: (a) ± 10% regulation band, (b) critical conduction mode operation (± 100% regulation band).

18.3.3 Critical Conduction Mode and Hysteretic Control

Another control scheme sometimes used in low-harmonic rectifiers, as well as in dc–dc converters and dc–ac inverters, is hysteretic control. Rather than operating at a fixed switching frequency and duty cycle, the hysteretic controller switches the transistor on and off as necessary to maintain a waveform within given limits. A special case of hysteretic control, called *critical conduction mode* control, is implemented in several commercially-available ICs, and is popular for low-harmonic rectifiers rated below several hundred Watts [23–25].

An example is the sinusoid of Fig. 18.19(a), in which the boost converter input current is controlled to follow a sinusoidal reference with a ± 10% tolerance. The inductor current increases when the transistor is on, and decreases when the transistor is off. So this hysteretic controller switches the transistor on whenever the input current falls below 90% of the reference input. The controller switches the transistor off whenever the input current exceeds 110% of the reference. Hysteretic controllers tend to have simple implementations. However, they have the disadvantages of variable switching frequency and reduced noise immunity.

Another example of hysteretic control is the waveform of Fig. 18.19(b). The lower limit is chosen to be zero, while the upper limit is twice the reference input. This controller operates the boost converter at the boundary between the continuous and discontinuous conduction modes. An alternative control scheme that generates the same waveform simply operates the transistor with constant on-time: the transistor is switched on when the inductor current reaches zero, and is switched off after a fixed

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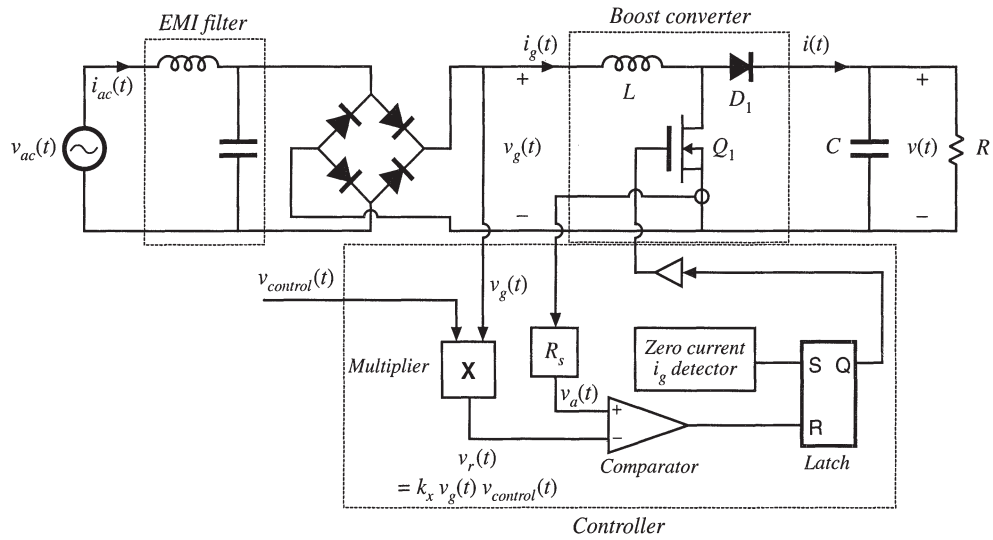


Fig. 18.20 A typical implementation of critical conduction mode control.

interval of length t_{on}. The resulting inductor current waveform will have a peak value that depends directly on the applied input voltage, and whose average value is one-half of its peak. With either control approach, the converter naturally exhibits loss-free-resistor or ideal rectifier behavior. The emulated resistance is

$$R_e = \frac{2L}{t_{on}} \tag{18.62}$$

This scheme has the advantage of small inductor size and low-cost control ICs. Disadvantages are increased peak currents, variable switching frequency, and the need for additional input EMI filtering.

A typical critical conduction mode controller is illustrated in Fig. 18.20. A zero-current detector senses when the inductor current is zero; this is typically accomplished by monitoring the voltage across the inductor. The zero-current detector sets a latch, turning on the transistor and initiating the switching period. The transistor current is also monitored, and is compared to a sinusoidal reference $v_r(t)$ that is proportional to the applied input voltage $v_g(t)$. When the sensed current is equal to the reference, the latch is reset and the transistor is turned off.

Since the switching frequency can vary, possibly over a wide range, it is important to carefully design the converter power stage. For a given power P, the required transistor on-time t_{on} can be found by combining Eqs. (18.17) and (18.62), and solving for t_{on}:

$$t_{on} = \frac{4LP}{V_M^2} \tag{18.63}$$

Application of the principle of volt-second balance to inductor L of Fig. 18.20 leads to the following equation:

$$v_g t_{on} + \left(v_g - V\right) t_{off} = 0 \tag{18.64}$$

Hence, the transistor off-time is given by

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$$t_{off} = t_{on} \frac{v_g}{\left(V - v_g\right)} \tag{18.65}$$

The switching period T_s is equal to

$$T_s = t_{off} + t_{on} \tag{18.66}$$

Substitution of Eqs. (18.63) and (18.65) into Eq. (18.66) yields

$$T_s = \frac{4LP}{V_M^2} \frac{1}{\left(1 - \frac{v_g(t)}{V}\right)} \tag{18.67}$$

The following expression for switching frequency is found by substitution of Eq. (18.11) into Eq. (18.67):

$$f_s = \frac{1}{T_s} = \frac{V_M^2}{4LP}\left(1 - \frac{V_M}{V}\left|\sin(\omega t)\right|\right) \tag{18.68}$$

The maximum switching frequency occurs when $\sin(\omega t)$ equals zero:

$$\max f_s = \frac{V_M^2}{4LP} \tag{18.69}$$

The minimum switching frequency occurs at the peak of the sine wave:

$$\min f_s = \frac{V_M^2}{4LP}\left(1 - \frac{V_M}{V}\right) \tag{18.70}$$

Equations (18.69) and (18.70) can be used to select the value of the inductance L and the output voltage V, so that the switching frequency varies over an acceptable range.

18.3.4 Nonlinear Carrier Control

The nonlinear-carrier controller (NLC) is capable of attaining input resistor emulation in boost and other converters that operate in the continuous conduction mode. Implementation of the controller is quite simple, with no need for sensing of the input voltage or input current. There is also no need for a current loop error amplifier. The boost nonlinear-carrier charge controller is inherently stable and is free from the stability problems that require addition of an artificial ramp in current programmed controllers.

A CCM boost rectifier system with nonlinear-carrier charge control is illustrated in Fig. 18.21, and waveforms are given in Fig. 18.22. The reasoning behind this approach is as follows. It is desirable to control the transistor switch current $i_s(t)$. This pulsating current is much easier to sense than the continuous converter input current—a simple current transformer can be used, as in Fig. 18.21. Further, it is desirable to control the integral of this current, or the charge, for two reasons: (1) integration of the waveform leads to improved noise immunity, and (2) the integral of the waveform is directly related to its average value,

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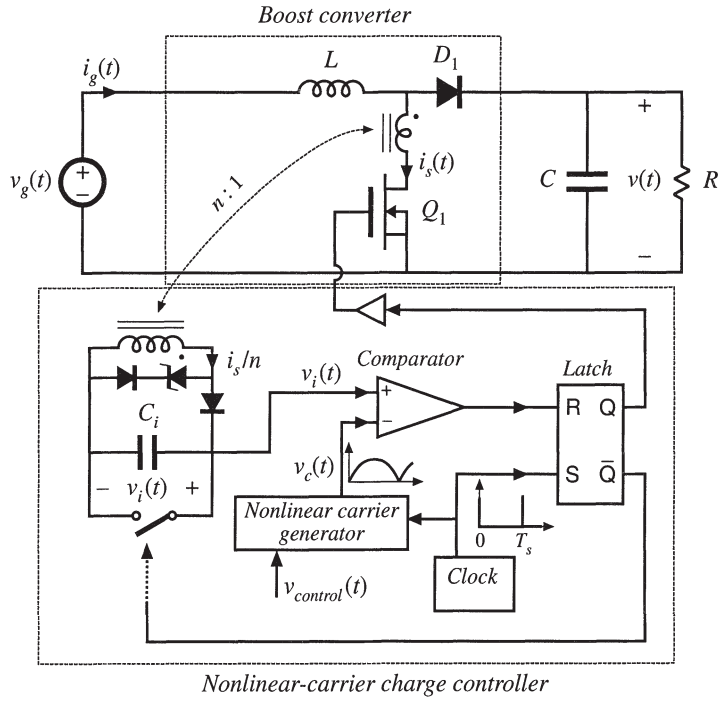


Fig. 18.21 Nonlinear-carrier charge control of a boost converter.

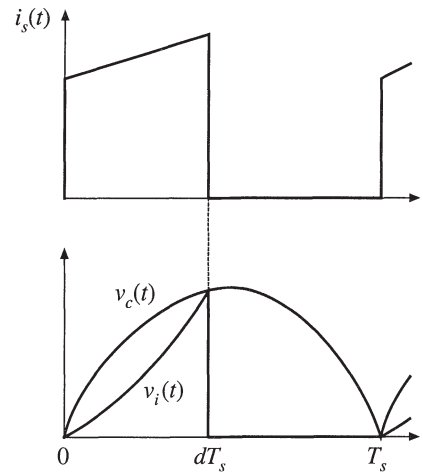


Fig. 18.22 Transistor current $i_s(t)$, parabolic carrier voltage $v_c(t)$, and integrator voltage $v_i(t)$ waveforms for the NLC-controlled boost rectifier of Fig. 18.21.

$$\left\langle i_s(t)\right\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} i_s(\tau)d\tau \tag{18.71}$$

In a fixed-frequency system, T_s is constant, and the integral over one switching period is proportional to the average value. Hence the average switch current can be controlled to be proportional to a reference signal by simply switching the transistor off when the integral of the switch current is equal to the reference. In the controller of Fig. 18.21, the switch current $i_s(t)$ is scaled by the transformer turns ratio n, and then integrated by capacitor C_i, such that

$$v_i(t) = \frac{1}{C_i}\int_0^{dT_s} \frac{i_s(\tau)}{n}\,d\tau \qquad \text{for } 0 < t < dT_s \tag{18.72}$$

The integrator voltage $v_i(t)$ is reset to zero at the end of each switching period, and the integration process begins anew at the beginning of the next switching period. So at the instant that the transistor is switched off, the voltage $v_i(dT_s)$ is proportional to the average switch current:

$$v_i(dT_s) = \frac{\left\langle i_s\right\rangle_{T_s}}{nC_i f_s} \qquad \text{for interval } 0 < t < T_s \tag{18.73}$$

How should the average switch current be controlled? To obtain input resistor emulation, it is desired that

$$\left\langle i_g(t)\right\rangle_{T_s} = \frac{\left\langle v_g(t)\right\rangle_{T_s}}{R_e(v_{control})} \tag{18.74}$$

It is further desired to avoid sensing either $i_g(t)$ or $v_g(t)$. As with other schemes, we will sense the dc output voltage $\langle v(t)\rangle_{T_s}$, to construct a low-bandwidth feedback loop that balances the average input and output powers. So let us determine the relationship between $\langle i_s(t)\rangle_{T_s}$ and $\langle v(t)\rangle_{T_s}$ implied by Eq. (18.74). If we assume that the boost converter operates in the continuous conduction mode, then we can write

$$\left\langle i_s(t)\right\rangle_{T_s} = d(t)\left\langle i_g(t)\right\rangle_{T_s} \tag{18.75}$$

and

$$\left\langle v_g(t)\right\rangle_{T_s} = d'(t)\left\langle v(t)\right\rangle_{T_s} \tag{18.76}$$

Substitution of Eqs. (18.75) and (18.76) into Eq. (18.74) leads to

$$\left\langle i_s(t)\right\rangle_{T_s} = d(t)\big(1-d(t)\big)\frac{\left\langle v(t)\right\rangle_{T_s}}{R_e(v_{control})} \tag{18.77}$$

The controller of Fig. 18.21 implements this equation.

The nonlinear carrier generator of Fig. 18.21 produces the parabolic waveform $v_c(t)$, given by

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$$v_c(t) = v_{control}\left(\frac{t}{T_s}\right)\left(1 - \frac{t}{T_s}\right) \qquad \text{for } 0 \le t \le T_s$$
$$v_c(t + T_s) = v_c(t) \tag{18.78}$$

This waveform is illustrated in Fig. 18.22. Note that Eq. (18.78) resembles Eq. (18.77), with $d(t)$ replaced by (t/T_s). The controller switches the transistor off at time $t = dT_s$ when the integrator voltage $v_i(t)$ is equal to the carrier waveform $v_c(t)$. Hence, it is true that

$$v_i(dT_s) = v_c(dT_s) = v_{control}(t)\, d(t)\left(1 - d(t)\right) \tag{18.79}$$

Substitution of Eq. (18.73) yields

$$\frac{\langle i_s(t)\rangle_{T_s}}{nC_i f_s} = v_{control}(t)\, d(t)\left(1 - d(t)\right) \tag{18.80}$$

This is of the same form as Eq. (18.77). Comparison of Eqs. (18.77) and (18.80) reveals that the emulated resistance R_e is given by

$$R_e(v_{control}) = d(t)\left(1 - d(t)\right)\frac{\langle v(t)\rangle_{T_s}}{\langle i_s(t)\rangle_{T_s}} = \frac{\langle v(t)\rangle_{T_s}}{nC_i f_s v_{control}(t)} \tag{18.81}$$

If the dc output voltage and the control voltage have negligible ac variation, then R_e is essentially constant, and the ac line current will exhibit low harmonic distortion. So neither the input voltage nor the input current need be sensed, and input resistor emulation can be obtained in CCM boost converters by sensing only the switch current.

A simple way to generate the parabolic carrier waveform uses two integrators, as illustrated in Fig. 18.23. The slowly varying control voltage $v_{control}(t)$ is integrated, to obtain a ramp waveform $v_r(t)$ whose peak amplitude is proportional to $v_{control}(t)$. The dc component of this waveform is removed, and then integrated again. The output of the second integrator is the parabolic carrier $v_c(t)$, illustrated in Fig. 18.22 and given by Eq. (18.78). Both integrators are reset to zero before the end of each switching period

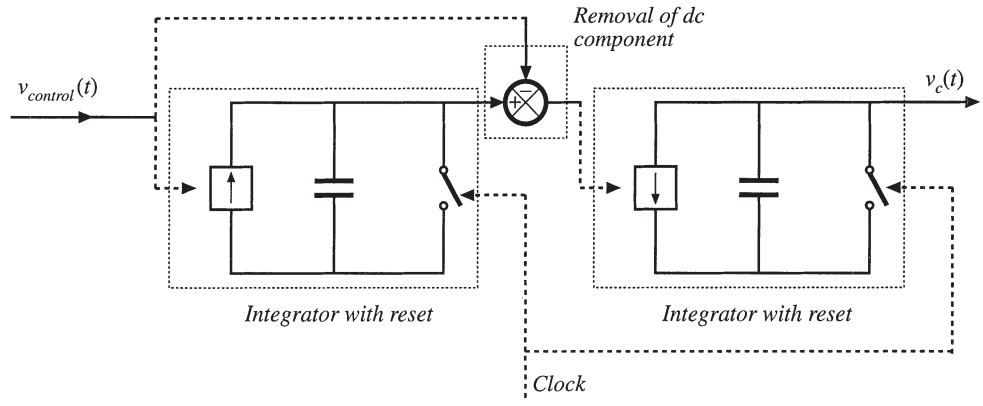


Fig. 18.23 Generation of parabolic carrier waveform by double integration.

by the clock generator. The amplitude of the parabolic carrier, and hence also the emulated resistance, can be controlled by variation of $v_{control}(t)$.

Equations (18.75) and (18.76) are valid only when the converter operates in the continuous conduction mode. In consequence, the ac line current waveform is distorted when the converter operates in DCM. Since this occurs near the zero crossings of the ac line voltage, crossover distortion is generated. Nonetheless, the harmonic distortion is less severe than in current-programmed schemes, and it is feasible to construct universal-input rectifiers that employ the NLC control approach. Total harmonic distortion is analyzed and plotted in [28].

Nonlinear carrier control can be applied to current-programmed boost rectifiers, as well as to other rectifiers based on the buck-boost, SEPIC, Ćuk, or other topologies, with either integral charge control or peak-current-programmed control [28,29]. In these cases, a different carrier waveform must be employed. A nonlinear-carrier controller in which the ac input voltage $v_g(t)$ is sensed, rather than the switch current $i_s(t)$, is described in [30].

18.4 SINGLE-PHASE CONVERTER SYSTEMS INCORPORATING IDEAL RECTIFIERS

An additional issue that arises in PWM rectifier systems is the control of power drawn from the ac line, the power delivered to the dc load, and the energy stored in a bulk energy storage capacitor.

18.4.1 Energy Storage

It is usually desired that the dc output voltage of a converter system be regulated with high accuracy. In practice, this is easily accomplished using a high-gain wide-bandwidth feedback loop. A well-regulated dc output voltage $v(t) = V$ is then obtained, which has negligible ac variations. For a given constant load characteristic, the load current I and the instantaneous load power $p_{load}(t) = P_{load}$, are also constant:

$$p_{load}(t) = v(t)i(t) = VI \tag{18.82}$$

However, the instantaneous input power $p_{ac}(t)$ of a single-phase ideal rectifier is not constant:

$$p_{ac}(t) = v_g(t)i_g(t) \tag{18.83}$$

If $v_g(t)$ is given by Eq. (18.11), and if $i_g(t)$ follows Eq. (18.1), then the instantaneous input power becomes

$$p_{ac}(t) = \frac{V_M^2}{R_e}\sin^2(\omega t) = \frac{V_M^2}{2R_e}\left(1 - \cos(2\omega t)\right) \tag{18.84}$$

which varies with time. The instantaneous input power is zero at the zero crossings of the ac input voltage. Equations (18.82) and (18.84) are illustrated in Fig. 18.24(a). Note that the desired instantaneous load power $p_{load}(t)$ is not equal to the desired instantaneous rectifier input power $p_{ac}(t)$. Some element within the rectifier system must supply or consume the difference between these two instantaneous powers.

Since the ideal rectifier does not consume or generate power, nor does it contain significant internal energy storage, it is necessary to add to the system a low-frequency energy storage element such

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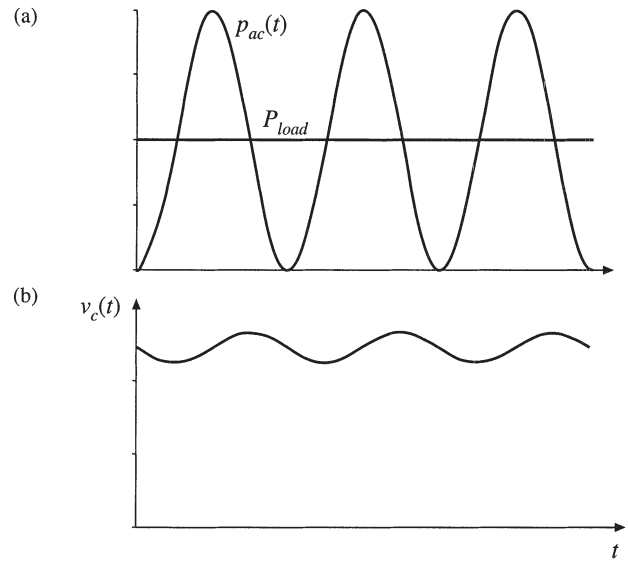


Fig. 18.24 Waveforms of a single-phase ideal rectifier system: (a) pulsating ac input power $p_{ac}(t)$, and constant dc load power P_{load}; (b) energy storage capacitor voltage $v_C(t)$.

as an electrolytic capacitor. The difference between the instantaneous input and load powers flows through this capacitor.

The waveforms of rectifier systems containing reactive elements can be determined by solution of the rectifier energy equation [36,37]. If the energy storage capacitor C is the only system element capable of significant low-frequency energy storage, then the power $p_C(t)$ flowing into the capacitor is equal to the difference between the instantaneous input and output powers:

$$p_C(t) = \frac{dE_C(t)}{dt} = \frac{d\left(\frac{1}{2} C v_C^2(t)\right)}{dt} = p_{ac}(t) - p_{load}(t) \tag{18.85}$$

where C is the capacitance, $v_C(t)$ is the capacitor voltage, and $E_C(t)$ is the energy stored in the capacitor. Hence as illustrated in Fig. 18.24(b), when $p_{ac}(t) > p_{load}(t)$ then energy flows into the capacitor, and $v_C(t)$ increases. Likewise, $v_C(t)$ decreases when $p_{ac}(t) < p_{load}(t)$. So the capacitor voltage $v_C(t)$ must be allowed to increase and decrease as necessary to store and release the required energy. In steady-state, the average values of $p_{ac}(t)$ and $p_{load}(t)$ must be equal, so that over one ac line cycle there is no net change in capacitor stored energy.

Where can the energy storage capacitor be placed? It is necessary to separate the energy storage capacitor from the regulated dc output, so that the capacitor voltage is allowed to independently vary as illustrated in Fig. 18.24(b). A conventional means of accomplishing this is illustrated in Fig. 18.25. A second dc–dc converter is inserted, between the energy storage capacitor and the regulated dc load. A wide-bandwidth feedback loop controls this converter, to attain a well-regulated dc load voltage. The capacitor voltage $v_C(t)$ is allowed to vary. Thus, this system configuration is capable of (1) wide-bandwidth control of the ac line current waveform, to attain unity power factor, (2) internal low-frequency energy storage, and (3) wide-bandwidth regulation of the dc output voltage. It is also possible to integrate these functions into a single converter, provided that the required low-frequency independence of the input, output, and capacitor voltages is maintained [38].

The energy storage capacitor also allows the system to function in other situations in which the instantaneous input and output powers differ. For example, it is commonly required that the output volt-

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