

Fig. 18.25 Elements of a single-phase-ac to dc power supply, in which the ac line current and dc load voltage are independently regulated with high bandwidth. An internal independent energy storage capacitor is required.

age remain regulated during ac line voltage failures of short duration. The *hold-up time* is the duration that the output voltage $v(t)$ remains regulated after $v_{ac}(t)$ has become zero. A typical requirement is that the system continue to supply power to the load during one complete missing ac line cycle, that is, for 20 msec in a 50 Hz system. During the hold-up time, the load power is supplied entirely by the energy storage capacitor. The value of capacitance should be chosen such that at the end of the hold-up time, the capacitor voltage $v_C(t)$ exceeds the minimum value that the dc-dc converter requires to produce the desired load voltage.

The energy storage function could be performed by an element other than a capacitor, such as an inductor. However, use of an inductor is a poor choice, because of its high weight and cost. For example, a 100 μF 100 V electrolytic capacitor and a 100 μH 100 A inductor can each store 1 Joule of energy. But the capacitor is considerably smaller, lighter, and less expensive.

A problem introduced by the energy storage capacitor is the large *inrush current* observed during the system turn-on transient. The capacitor voltage $v_C(t)$ is initially zero; substantial amounts of charge and energy are required to raise this voltage to its equilibrium value. The boost converter is not capable of limiting the magnitude of the resulting inrush current: even when $d(t) = 0$, a large current flows through the boost converter diode to the capacitor, as long as the converter output voltage is less than the input voltage. Some additional circuitry is required to limit the inrush current of the boost converter. Converters having a buck-boost type conversion ratio are inherently capable of controlling the inrush current. This advantage comes at the cost of additional switch stress.

It is also possible to design the ideal rectifier to operate correctly when connected to utility power systems anywhere in the world. *Universal input* rectifiers can operate with nominal ac rms voltage magnitudes as low as the 100 V encountered in a portion of Japan, or as high as the 260 V found in western Australia, with ac line frequencies of either 50 Hz or 60 Hz. Regardless of the ac input voltage, the universal-input rectifier produces a constant nominal dc output voltage V_C .

Let us now consider in more detail the low-frequency energy storage process of the system of Fig. 18.25. Let us assume that the dc-dc converter contains a controller having bandwidth much greater than the ac line frequency, such that the load voltage contains negligible low-frequency variations. A low-frequency model of the dc-dc converter is then as illustrated in Fig. 18.26. The dc-dc converter produces constant voltage $v(t) = V$, modeled by a voltage source as shown. This causes the load to draw constant current $i(t) = I$, leading to load power $p_{load}(t) = P_{load}$. To the extent that converter losses can be neglected, the dc-dc converter input port draws power P_{load} , regardless of the value of $v_C(t)$. So the dc-dc converter input port can be modeled as a constant power sink, of value P_{load} .

The model of Fig. 18.26 implies that the difference between the rectifier power $p_{ac}(t)$ and the load power P_{load} flows into the capacitor, as given by Eq. (18.85). The capacitor voltage increases when $p_{ac}(t)$ exceeds P_{load} , and decreases when $p_{ac}(t)$ is less than P_{load} . In steady state, the average values of $p_{ac}(t)$ and P_{load} must be equal. But note that $p_{ac}(t)$ is determined by the magnitudes of $v_{ac}(t)$ and R_e , and

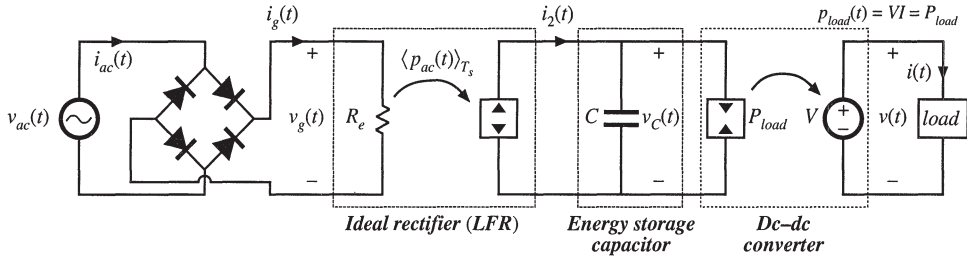


Fig. 18.26 Low-frequency equivalent circuit of the system of Fig. 18.25.

not by the load. The system of Fig. 18.26 contains no mechanism to cause the average rectifier power and load power to be equal. In consequence, it is necessary to add an additional control system that adjusts R_e as necessary, to cause the average rectifier output power and dc-dc converter input power to balance. The conventional way to accomplish this is simply to regulate the dc component of $v_C(t)$.

A complete system containing ideal rectification, energy storage, and wide-bandwidth output voltage regulation is illustrated in Fig. 18.27. This system incorporates the boost converter and controller of Fig. 18.5, as well as a generic dc-dc converter with output voltage feedback. In addition, the system contains a low-bandwidth feedback loop, which regulates the dc component of the energy-storage capacitor voltage to be equal to a reference voltage v_{ref2} . This is accomplished by slow variations of $v_{control}(t)$ and R_e . This controller should have sufficiently small loop gain at the even harmonics of the ac line frequency, so that variations in R_e are much slower than the ac line frequency.

Increasing the bandwidth of the energy storage capacitor voltage controller can lead to significant ac line current harmonics. When this controller has wide bandwidth and high gain, then it varies $R_e(t)$ quickly, distorting the ac line current waveform. In the extreme limit of perfect regulation of the

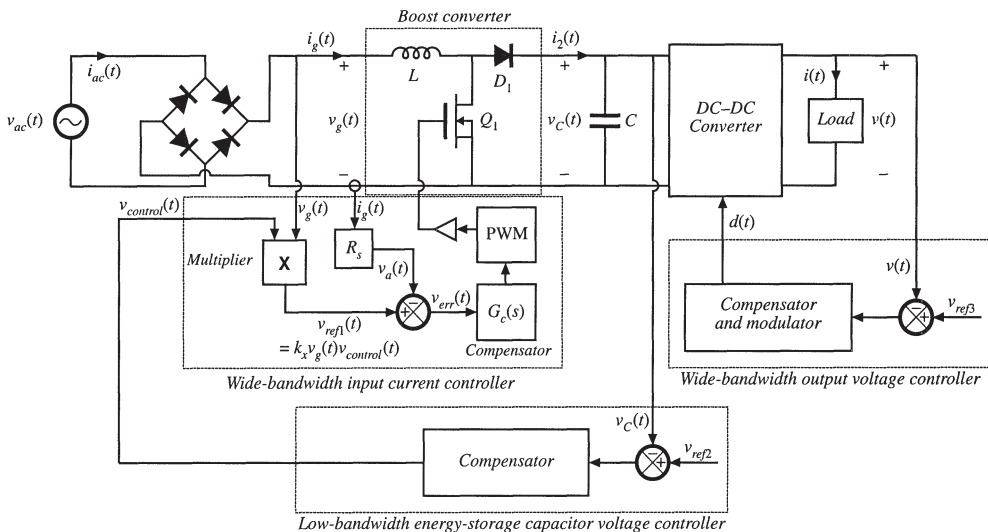


Fig. 18.27 A complete dc power supply system incorporating a near-ideal single-phase boost rectifier system, energy storage capacitor, and dc-dc converter. Wide-bandwidth feedback loops regulate the ac line current waveform and the dc load voltage, and a slow feedback loop regulates the energy storage capacitor voltage.

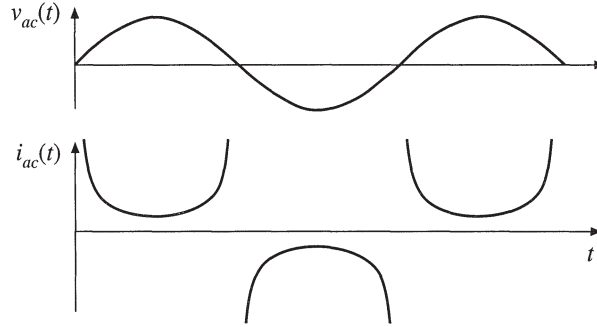


Fig. 18.28 Ac line current waveform of the single-phase ideal rectifier with output voltage feedback, when it supplies constant instantaneous power to a dc load. The THD tends to infinity, and the power factor tends to zero.

energy storage capacitor voltage $v_C(t) = V_C$, then the capacitor stored energy is constant, and the instantaneous input ac line power $p_{ac}(t)$ and load power $p_{load}(t)$ are equal. The controller prevents the energy-storage capacitor from performing its low-frequency energy storage function. The ac line current then becomes

$$i_{ac}(t) = \frac{p_{ac}(t)}{v_{ac}(t)} = \frac{p_{load}(t)}{v_{ac}(t)} = \frac{P_{load}}{V_M \sin(\omega t)} \quad (18.86)$$

This waveform is sketched in Fig. 18.28. In this idealized limiting case, the ac line current tends to infinity at the zero crossings of the ac line voltage waveform, such that the instantaneous input power is constant. It can be shown that the THD of this current waveform is infinite, and its distortion factor and power factor are zero. So the bandwidth of this controller should be limited.

The energy storage capacitor voltage ripple can be found by integration of Eq. (18.85). Under steady-state conditions, where the average value of $p_{ac}(t) = P_{load}$, integration of Eq. (18.85) yields

$$E_C(t) = \frac{1}{2} C v_C^2(t) = E_C(0) + \int_0^t (-P_{load} \cos(2\omega t)) dt \quad (18.87)$$

where ω is the ac line frequency. Evaluation of the integral leads to

$$E_C(t) = E_C(0) - \frac{P_{load} \sin(2\omega t)}{2\omega} \quad (18.88)$$

Therefore, the capacitor voltage waveform is

$$v_C(t) = \sqrt{\frac{2E_C(t)}{C}} = \sqrt{v_C^2(0) - \frac{P_{load}}{\omega C} \sin(2\omega t)} \quad (18.89)$$

It can be verified that the rms value of this waveform is $V_{C,rms} = v_C(0)$. Hence, Eq. (18.89) can be written

$$v_C(t) = V_{C,rms} \sqrt{1 - \frac{P_{load}}{\omega C V_{C,rms}^2} \sin(2\omega t)} \quad (18.90)$$

This waveform is sketched in Fig. 18.24(b). The minimum and maximum values of the capacitor voltage occur when $\sin(2\omega t)$ is equal to 1 and -1, respectively. Therefore, the peak-to-peak capacitor voltage rip-

ple is

$$2\Delta v_C = V_{C,rms} \left[\sqrt{1 + \frac{P_{load}}{\omega C V_{C,rms}^2}} - \sqrt{1 - \frac{P_{load}}{\omega C V_{C,rms}^2}} \right] \approx \frac{P_{load}}{\omega C V_{C,rms}} \quad (18.91)$$

The approximation is valid for $P_{load}/(\omega C V_{C,rms}^2)$ sufficiently less than one, a condition that is satisfied whenever the ac voltage ripple is sufficiently less than $V_{C,rms}$.

18.4.2 Modeling the Outer Low-Bandwidth Control System

As discussed above, the outer low-bandwidth controller, which varies the emulated resistance as necessary to balance the average ac input and dc load powers, is common to all near-ideal rectifier systems. For design of this controller, the rectifier can be modeled using the loss-free resistor (LFR) model. Perturbation and linearization of the LFR leads to a small-signal equivalent circuit that predicts the relevant small-signal transfer functions. Such a model is derived in this section [2,39,40].

It is desirable to stabilize the rectifier output voltage against variations in load power, ac line voltage, and component characteristics. Hence, a voltage feedback loop is necessary. As discussed in Section 18.4.1, this loop cannot attempt to remove the capacitor voltage ripple that occurs at the second harmonic of the ac line frequency, 2ω , since doing so would require that $R_e(t)$ change significantly at the second harmonic frequency. This would introduce significant distortion, phase shift, and power factor degradation into the ac line current waveform. In consequence this loop must have sufficiently small gain at frequency 2ω , and hence its bandwidth must be low. Therefore, for the purposes of designing the low-bandwidth outer control loop, it is unnecessary to model the system high-frequency behavior. It can be assumed that any inner wide-bandwidth controller operates ideally at low frequencies, such that the ideal rectifier model of Fig. 18.29(a) adequately represents the low-frequency system behavior.

A small-signal model is derived here that correctly predicts the control-to-output transfer function and output impedance of any rectifier system that can be modeled as a loss-free resistor. The model neglects the complicating effects of high-frequency switching ripple, and is valid for control variations at frequencies sufficiently less than the ac line frequency. Both resistive and dc-dc converter/regulator loads are treated.

The steps in the derivation of the small-signal ac model are summarized in Fig. 18.29. Figure 18.29(a) is the basic ideal rectifier model, in which the converter high frequency switching ripple is removed via averaging over the switching period T_s , but waveform frequency components slower than the switching frequency are correctly modeled, including the 2ω second-harmonic and dc components of output voltage. It is difficult to use this model in design of the feedback loop because it is highly nonlinear and time-varying.

If the ac input voltage $v_g(t)$ is

$$v_g(t) = \sqrt{2} v_{g,rms} \left| \sin(\omega t) \right| \quad (18.92)$$

then the model of Fig. 18.29(a) predicts that the instantaneous output power $\langle p(t) \rangle_{T_s}$ is

$$\langle p(t) \rangle_{T_s} = \frac{\langle v_g(t) \rangle_{T_s}^2}{R_e(v_{control}(t))} = \frac{v_{g,rms}^2}{R_e(v_{control}(t))} (1 - \cos(2\omega t)) \quad (18.93)$$

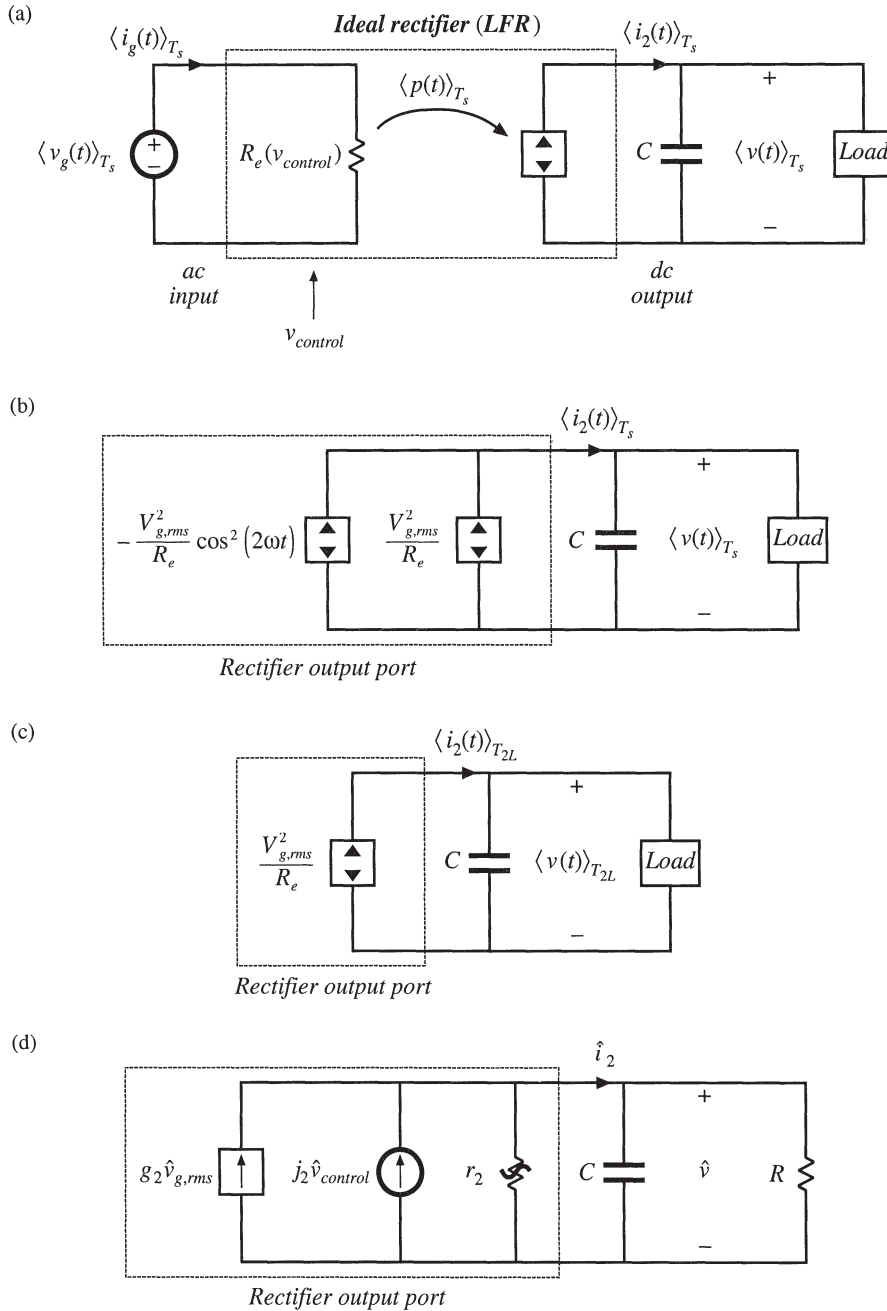


Fig. 18.29 Steps in the derivation of low-frequency small-signal rectifier model: (a) large-signal LFR model, averaged over one switching period T_s ; (b) separation of power source into its constant and time-varying components; (c) removal of second-harmonic components by averaging over one-half of the ac line period, T_{2L} ; (d) small-signal model obtained by perturbation and linearization of Fig. 18.29(c).

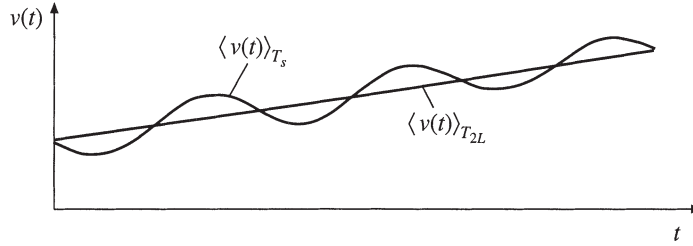


Fig. 18.30 Removal of components of $v(t)$ at the harmonics of the ac line frequency, by averaging over one-half of the ac line period, T_{2L} .

The output power is comprised of a constant term $v_{g,rms}^2/R_e$, and a term that varies at the second harmonic of the ac line frequency. These two terms are explicitly identified in Fig. 18.29(b).

The second-harmonic variation in $\langle p(t) \rangle_{T_s}$ leads to time-varying system equations, and slow variations in $v_{control}(t)$ lead to an output voltage spectrum containing components not only at the frequencies present in $v_{control}(t)$, but also at the even harmonics of the ac line frequency and their sidebands, as well as at the switching frequency and its harmonics and sidebands. It is desired to model only the low-frequency components excited by slow variations in $v_{control}(t)$, the load, and the ac line voltage amplitude $v_{g,rms}$. The even harmonics of the ac line frequency can be removed by averaging over one-half of the ac line period

$$T_{2L} = \frac{1}{2} \frac{2\pi}{\omega} = \frac{\pi}{\omega} \quad (18.94)$$

Hence, we average over the switching period T_s to remove the switching harmonics, and then average again over one-half of the ac line period T_{2L} to remove the even harmonics of the ac line frequency. The resulting model is valid for frequencies sufficiently less than the ac line frequency ω . Averaging of the rectifier output voltage is illustrated in Fig. 18.30: averaging over T_{2L} removes the ac line frequency harmonics, leaving the underlying low-frequency variations. By averaging the model of Fig. 18.29(b) over T_{2L} , we obtain the model of Fig. 18.29(c). This step removes the second-harmonic variation in the power source.

The equivalent circuit of Fig. 18.29(c) is time-invariant, but nonlinear. We can now perturb and linearize as usual, to construct a small-signal ac model that describes how slow variations in $v_{control}(t)$, $v_{g,rms}$, and the load, affect the rectifier output waveforms. Let us assume that the averaged output voltage $\langle v(t) \rangle_{T_{2L}}$, rectifier averaged output current $\langle i_2(t) \rangle_{T_{2L}}$, rms line voltage amplitude $v_{g,rms}$, and control voltage $v_{control}(t)$, can be represented as quiescent values plus small slow variations:

$$\begin{aligned} \langle v(t) \rangle_{T_{2L}} &= V + \hat{v}(t) \\ \langle i_2(t) \rangle_{T_{2L}} &= I_2 + \hat{i}_2(t) \\ v_{g,rms} &= V_{g,rms} + \hat{v}_{g,rms}(t) \\ v_{control}(t) &= V_{control} + \hat{v}_{control}(t) \end{aligned} \quad (18.95)$$

with

$$\begin{aligned}
 V &\gg |\hat{v}(t)| \\
 I_2 &\gg |\hat{i}_2(t)| \\
 V_{g,rms} &\gg |\hat{v}_{g,rms}(t)| \\
 V_{control} &\gg |\hat{v}_{control}(t)|
 \end{aligned} \tag{18.96}$$

In the averaged model of Fig. 18.29(c), $\langle i_2(t) \rangle_{T_{2L}}$ is given by

$$\begin{aligned}
 \langle i_2(t) \rangle_{T_{2L}} &= \frac{\langle p(t) \rangle_{T_{2L}}}{\langle v(t) \rangle_{T_{2L}}} = \frac{v_{g,rms}^2(t)}{R_e(v_{control}(t)) \langle v(t) \rangle_{T_{2L}}} \\
 &= f\left(v_{g,rms}(t), \langle v(t) \rangle_{T_{2L}}, v_{control}(t)\right)
 \end{aligned} \tag{18.97}$$

This equation resembles DCM buck-boost Eq. (11.45), and linearization proceeds in a similar manner. Expansion of Eq. (18.97) in a three-dimensional Taylor series about the quiescent operating point, and elimination of higher-order nonlinear terms, leads to

$$\hat{i}_2(t) = g_2 \hat{v}_{g,rms}(t) + j_2 \hat{v}_{control}(t) - \frac{\hat{v}(t)}{r_2} \tag{18.98}$$

where

$$g_2 = \left. \frac{df(v_{g,rms}, V, V_{control})}{dv_{g,rms}} \right|_{v_{g,rms} = V_{g,rms}} = \frac{2}{R_e(V_{control})} \frac{V_{g,rms}}{V} \tag{18.99}$$

$$\left(-\frac{1}{r_2} \right) = \left. \frac{df(V_{g,rms}, \langle v \rangle_{T_{2L}}, V_{control})}{d\langle v \rangle_{T_{2L}}} \right|_{\langle v \rangle_{T_{2L}} = V} = -\frac{I_2}{V} \tag{18.100}$$

$$j_2 = \left. \frac{df(V_{g,rms}, V, v_{control})}{dv_{control}} \right|_{v_{control} = V_{control}} = -\frac{V_{g,rms}^2}{VR_e^2(V_{control})} \left. \frac{dR_e(v_{control})}{dv_{control}} \right|_{v_{control} = V_{control}} \tag{18.101}$$

A small-signal equivalent circuit based on Eq. (18.98) is given in Fig. 18.29(d). Expressions for the parameters g_2 , j_2 , and r_2 for several controllers are listed in Table 18.1. This model is valid for the conditions of Eq. (18.96), with the additional assumption that the output voltage ripple is sufficiently small. Figure 18.29(d) is useful only for determining the various ac transfer functions; no information regarding dc conditions can be inferred. The ac resistance r_2 is derived from the slope of the average value of the power source output characteristic, evaluated at the quiescent operating point. The other coefficients, j_2 and g_2 , are also derived from the slopes of the same characteristic, taken with respect to $v_{control}(t)$ and $v_{g,rms}$ and evaluated at the quiescent operating point. The resistance R is the incremental resistance of the load, evaluated at the quiescent operating point. In the boost converter with hysteretic control, the transistor on-time t_{on} replaces $v_{control}$ as the control input; likewise, the transistor duty cycle d is taken as the

Table 18.1 Small-signal model parameters for several types of rectifier control schemes

Controller type	g_2	j_2	r_2
Average current control with feedforward, Fig. 18.14	0	$\frac{P_{av}}{VV_{control}}$	$\frac{V^2}{P_{av}}$
Current-programmed control, Fig. 18.16	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{P_{av}}{VV_{control}}$	$\frac{V^2}{P_{av}}$
Nonlinear-carrier charge control of boost rectifier, Fig. 18.21	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{P_{av}}{VV_{control}}$	$\frac{V^2}{2P_{av}}$
Boost with critical conduction mode control, Fig. 18.20	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{P_{av}}{VV_{control}}$	$\frac{V^2}{P_{av}}$
DCM buck-boost, flyback, SEPIC, or Ćuk converters	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{2P_{av}}{VD}$	$\frac{V^2}{P_{av}}$

control input to the DCM buck-boost, flyback, SEPIC, and Ćuk converters. Harmonics are ignored for the current-programmed and NLC controllers; the expressions given in Table 18.1 assume that the converter operates in CCM with negligible harmonics.

The control-to-output transfer function is

$$\frac{\hat{v}(s)}{\hat{v}_{control}(s)} = j_2 R \| r_2 \frac{1}{1 + sC R \| r_2} \quad (18.102)$$

The line-to-output transfer function is

$$\frac{\hat{v}(s)}{\hat{v}_{g,rms}(s)} = g_2 R \| r_2 \frac{1}{1 + sC R \| r_2} \quad (18.103)$$

Thus, the small-signal transfer functions of the high quality rectifier contain a single pole, ascribable to the output filter capacitor operating in conjunction with the incremental load resistance R and r_2 , the effective output resistance of the power source. Although this model is based on the ideal rectifier, its form is similar to that of the dc–dc DCM buck-boost converter ac model of Chapter 11. This is natural, because the DCM buck-boost converter is itself a natural loss-free resistor. The major difference is that the rms value of the ac input voltage must be used, and that the second harmonic components of r_2 , j_2 , and g_2 must additionally be removed via averaging. Nonetheless, the equivalent circuit and ac transfer functions are of similar form.

When the rectifier drives a regulated dc–dc converter as in Fig. 18.25, then the dc–dc converter presents a constant power load to the rectifier, as illustrated in Fig. 18.26. In equilibrium, the rectifier and dc–dc converter operate with the same average power P_{av} and the same dc voltage V . The incremental resistance R of the constant power load is negative, and is given by

$$R = -\frac{V^2}{P_{av}} \quad (18.104)$$

which is equal in magnitude but opposite in polarity to the rectifier incremental output resistance r_2 , for all controllers except the NLC controller. The parallel combination $r_2 \| R$ then tends to an open circuit, and the control-to-output and line-to-output transfer functions become

$$\frac{\hat{v}(s)}{\hat{v}_{control}(s)} = \frac{j_2}{sC} \quad (18.105)$$

and

$$\frac{\hat{v}(s)}{\hat{v}_{g,rms}(s)} = \frac{g_2}{sC} \quad (18.106)$$

In the case of the NLC controller, the parallel combination $r_2 \parallel R$ becomes equal to $r_2/2$, and Eqs. (18.102) and (18.103) continue to apply.

18.5 RMS VALUES OF RECTIFIER WAVEFORMS

To correctly specify the power stage elements of a near-ideal rectifier, it is necessary to compute the root-mean-square values of their currents. A typical waveform such as the transistor current of the boost converter (Fig. 18.31) is pulse-width modulated, with both the duty cycle and the peak amplitude varying with the ac input voltage. When the switching frequency is much larger than the ac line frequency, then the rms value can be well-approximated as a double integral. The square of the current is integrated first to find its average over a switching period, and the result is then integrated to find the average over the ac line period.

Computation of the rms and average values of the waveforms of a PWM rectifier can be quite tedious, and this can impede the effective design of the power stage components. In this section, several approximations are developed, which allow relatively simple analytical expressions to be written for the rms and average values of the power stage currents, and which allow comparison of converter approaches [14,41]. The transistor current in the boost rectifier is found to be quite low.

The rms value of the transistor current is defined as

$$I_{Qrms} = \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} i_Q^2(t) dt} \quad (18.107)$$

where T_{ac} is the period of the ac line waveform. The integral can be expressed as a sum of integrals over all of the switching periods contained in one ac line period:

$$I_{Qrms} = \sqrt{\frac{1}{T_{ac}} T_s \sum_{n=1}^{T_{ac}/T_s} \left(\frac{1}{T_s} \int_{(n-1)T_s}^{nT_s} i_Q^2(t) dt \right)} \quad (18.108)$$

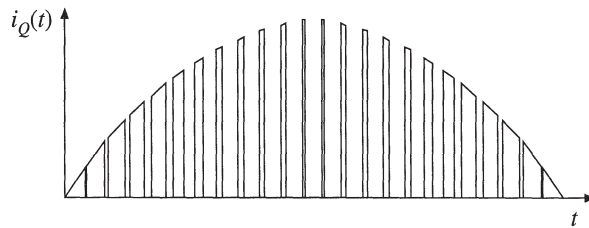


Fig. 18.31 Modulated transistor current waveform, boost rectifier.

where T_s is the switching period. The quantity inside the parentheses is the value of i_Q^2 averaged over the n^{th} switching period. The summation can be approximated by an integral in the case when T_s is much less than T_{ac} . This approximation corresponds to taking the limit as T_s tends to zero, as follows:

$$\begin{aligned}
 I_{Qrms} &\approx \sqrt{\frac{1}{T_{ac}} \lim_{T_s \rightarrow 0} \left[T_s \sum_{n=1}^{T_{ac}/T_s} \left(\frac{1}{T_s} \int_{(n-1)T_s}^{nT_s} i_Q^2(\tau) d\tau \right) \right]} \\
 &= \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \frac{1}{T_s} \int_t^{t+T_s} i_Q^2(\tau) d\tau dt} \\
 &= \sqrt{\left\langle \left\langle i_Q^2(t) \right\rangle_{T_s} \right\rangle_{T_{ac}}}
 \end{aligned} \tag{18.109}$$

So $i_Q^2(t)$ is first averaged over one switching period. The result is then averaged over the ac line period, and the square root is taken of the result.

18.5.1 Boost Rectifier Example

For the boost rectifier, the transistor current $i_Q(t)$ is equal to the input current when the transistor conducts, and is zero when the transistor is off. Therefore, the average of $i_Q^2(t)$ over one switching period is

$$\begin{aligned}
 \left\langle i_Q^2 \right\rangle_{T_s} &= \frac{1}{T_s} \int_t^{t+T_s} i_Q^2(t) dt \\
 &= d(t) i_{ac}^2(t)
 \end{aligned} \tag{18.110}$$

If the input voltage is given by

$$v_{ac}(t) = V_M |\sin \omega t| \tag{18.111}$$

then the input current will be

$$i_{ac}(t) = \frac{V_M}{R_e} |\sin \omega t| \tag{18.112}$$

where R_e is the emulated resistance. With a constant output voltage V , the transistor duty cycle must obey the relationship

$$\frac{V}{v_{ac}(t)} = \frac{1}{1-d(t)} \tag{18.113}$$

This assumes that the converter dynamics are fast compared to the ac line frequency. Substitution of Eq. (18.111) into (18.113) and solution for $d(t)$ yields

$$d(t) = 1 - \frac{V_M}{V} |\sin \omega t| \tag{18.114}$$

Substitution of Eqs. (18.112) and (18.114) into Eq. (18.110) yields the following expression

$$\langle i_Q^2 \rangle_{T_s} = \frac{V_M^2}{R_e^2} \left(1 - \frac{V_M}{V} |\sin \omega t| \right) \sin^2(\omega t) \quad (18.115)$$

One can now plug this expression into Eq. (18.109):

$$\begin{aligned} I_{Qrms} &= \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \langle i_Q^2 \rangle_{T_s} dt} \\ &= \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \frac{V_M^2}{R_e^2} \left(1 - \frac{V_M}{V} |\sin \omega t| \right) \sin^2(\omega t) dt} \end{aligned} \quad (18.116)$$

which can be further simplified to

$$I_{Qrms} = \sqrt{\frac{2}{T_{ac}} \frac{V_M^2}{R_e^2} \int_0^{T_{ac}/2} \left(\sin^2(\omega t) - \frac{V_M}{V} \sin^3(\omega t) \right) dt} \quad (18.117)$$

This involves integration of powers of $\sin(\omega t)$ over a complete half-cycle. The integral can be evaluated with the help of the following formula:

$$\frac{1}{\pi} \int_0^\pi \sin^n(\theta) d\theta = \begin{cases} \frac{2}{\pi} \frac{2 \cdot 4 \cdot 6 \cdots (n-1)}{1 \cdot 3 \cdot 5 \cdots n} & \text{if } n \text{ is odd} \\ \frac{1 \cdot 3 \cdot 5 \cdots (n-1)}{2 \cdot 4 \cdot 6 \cdots n} & \text{if } n \text{ is even} \end{cases} \quad (18.118)$$

This type of integral commonly arises in rms calculations involving PWM rectifiers. The values of the integral for several choices of n are listed in Table 18.2. Evaluation of the integral in Eq. (18.117) using Eq. (18.118) leads to the following result:

$$I_{Qrms} = \frac{V_M}{\sqrt{2} R_e} \sqrt{1 - \frac{8}{3\pi} \frac{V_M}{V}} = I_{ac rms} \sqrt{1 - \frac{8}{3\pi} \frac{V_M}{V}} \quad (18.119)$$

It can be seen that the rms transistor current is minimized by choosing the output voltage V to be as small as possible. The best that can be done is to choose $V = V_M$, which leads to

$$I_{Qrms} = 0.39 I_{ac rms} \quad (18.120)$$

Larger values of V lead to a larger rms transistor current.

A similar analysis for the rms diode current leads to the following expression

$$I_{Drms} = I_{ac rms} \sqrt{\frac{8}{3\pi} \frac{V_M}{V}} \quad (18.121)$$

The choice $V = V_M$ maximizes the rms diode current, with the result

Table 18.2 Solution of the integral of Eq. (18.118), for several values of n

n	$\frac{1}{\pi} \int_0^\pi \sin^n(\theta) d\theta$
1	$\frac{2}{\pi}$
2	$\frac{1}{2}$
3	$\frac{4}{3\pi}$
4	$\frac{3}{8}$
5	$\frac{16}{15\pi}$
6	$\frac{15}{48}$

$$I_{Drms} = 0.92 I_{ac rms} \quad (18.122)$$

Larger values of V lead to smaller rms diode current.

Average currents can be computed in a similar way. The results are

$$\begin{aligned} I_{Qav} &= I_{ac rms} \frac{2\sqrt{2}}{\pi} \left(1 - \frac{\pi}{8} \frac{V_M}{V} \right) \\ I_{Dav} &= I_{ac rms} \frac{V_M}{2\sqrt{2} V} \end{aligned} \quad (18.123)$$

Expressions for rms, average, and peak currents of the power stage components of the continuous conduction mode boost converter are summarized in Table 18.3. Expressions are also tabulated for flyback and SEPIC topologies, operating in the continuous conduction mode. In the case of the flyback converter, an L_1 – C_1 input filter is also included. In all cases, the effects of switching ripple are neglected.

18.5.2 Comparison of Single-Phase Rectifier Topologies

When isolation is not a rectifier requirement, and when it is acceptable that the dc output voltage be marginally larger than the peak ac input voltage, then the boost converter is a very effective approach. For example, consider the design of a 1 kW rectifier operating from the 240 Vrms input line voltage. If the converter efficiency and power factor are both approximately unity, then the rms input current is $I_{rms} = (1000 \text{ W})/(240 \text{ V}) = 4.2 \text{ A}$. The dc output voltage is chosen to be 380 V, or slightly larger than the peak ac input voltage. By use of Eq. (18.119), the rms transistor current is found to be 2 A. This is quite a low value—less than half of the rms input current, which demonstrates how effectively the converter utilizes the power switch. The rms diode current is 3.6 A, and the transistor and diode blocking voltages are 380 V. With a 120 V ac input voltage, the transistor and diode rms currents increase to 6.6 A and 5.1 A, respectively.

The only real drawback of the boost converter is its inability to limit inrush currents. When the dc output voltage is less than the instantaneous input voltage, the control circuit of the boost rectifier loses control of the inductor current waveform. A very large inrush current occurs when the dc output capacitor is initially charged. Additional circuitry must be employed to limit the magnitude of this current.

Buck-boost, SEPIC, and Ćuk topologies can be used to solve the inrush current problem. Since these converters have a $d/(1-d)$ conversion ratio, their waveforms can be controlled when the output voltage is any positive value. But the price paid for this capability is increased component stresses. For the same 1 kW rectifier with 240 Vrms ac input and 380 V output, the transistor rms current and peak voltage of the nonisolated SEPIC are 5.5 A and 719 V. The rms diode current is 4.85 A. The semiconductor voltage stresses can be reduced by reducing the output voltage, at the expense of increased rms currents. With a 120 V ac input voltage, the transistor and diode rms currents increase to 9.8 A and 6.1 A, respectively.

Isolation can also be obtained in the SEPIC and other topologies, as discussed in Chapter 6. The turns ratio of the isolation transformer can also be used to reduce the primary-side currents when the dc output voltage is low. But the transformer winding rms currents are higher than those of a dc–dc converter, because of the pulsating (twice-line-frequency) power flow. For the 1 kW, 240 V ac input SEPIC example, with a 42 V 23.8 A dc load, and a 4:1 transformer turns ratio, the rms transformer currents are 5.5 A (primary) and 36.4 A (secondary). The rms transistor current is 6.9 A. At 120 V ac input voltage,

Table 18.3 Summary of rectifier current stresses for several converter topologies

	rms	Average	Peak
CCM boost			
Transistor	$I_{ac\ rms} \sqrt{1 - \frac{8}{3\pi} \frac{V_M}{V}}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi} \left(1 - \frac{\pi}{8} \frac{V_M}{V}\right)$	$I_{ac\ rms} \sqrt{2}$
Diode	$I_{dc} \sqrt{\frac{16}{3\pi} \frac{V}{V_M}}$	I_{dc}	$2I_{dc} \frac{V}{V_M}$
Inductor	$I_{ac\ rms}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi}$	$I_{ac\ rms} \sqrt{2}$
CCM flyback, with $n:1$ isolation transformer and input filter			
Transistor, xfmr primary	$I_{ac\ rms} \sqrt{1 + \frac{8}{3\pi} \frac{V_M}{nV}}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi}$	$I_{ac\ rms} \sqrt{2} \left(1 + \frac{V_M}{nV}\right)$
L_1	$I_{ac\ rms}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi}$	$I_{ac\ rms} \sqrt{2}$
C_1	$I_{ac\ rms} \sqrt{\frac{8}{3\pi} \frac{V_M}{nV}}$	0	$I_{ac\ rms} \sqrt{2} \max\left(1, \frac{V_M}{nV}\right)$
Diode, xfmr secondary	$I_{dc} \sqrt{\frac{3}{2} + \frac{16}{3\pi} \frac{nV}{V_M}}$	I_{dc}	$2I_{dc} \left(1 + \frac{nV}{V_M}\right)$
CCM SEPIC, nonisolated			
Transistor	$I_{ac\ rms} \sqrt{1 + \frac{8}{3\pi} \frac{V_M}{V}}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi}$	$I_{ac\ rms} \sqrt{2} \left(1 + \frac{V_M}{V}\right)$
L_1	$I_{ac\ rms}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi}$	$I_{ac\ rms} \sqrt{2}$
C_1	$I_{ac\ rms} \sqrt{\frac{8}{3\pi} \frac{V_M}{V}}$	0	$I_{ac\ rms} \sqrt{2} \max\left(1, \frac{V_M}{V}\right)$
L_2	$I_{ac\ rms} \frac{V_M}{V} \frac{\sqrt{3}}{2}$	$\frac{I_{ac\ rms}}{\sqrt{2}} \frac{V_M}{V}$	$I_{ac\ rms} \frac{V_M}{V} \sqrt{2}$
Diode	$I_{dc} \sqrt{\frac{3}{2} + \frac{16}{3\pi} \frac{V}{V_M}}$	I_{dc}	$2I_{dc} \left(1 + \frac{V}{V_M}\right)$
CCM SEPIC, with $n:1$ isolation transformer			
Transistor	$I_{ac\ rms} \sqrt{1 + \frac{8}{3\pi} \frac{V_M}{nV}}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi}$	$I_{ac\ rms} \sqrt{2} \left(1 + \frac{V_M}{nV}\right)$
L_1	$I_{ac\ rms}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi}$	$I_{ac\ rms} \sqrt{2}$
C_1 , xfmr primary	$I_{ac\ rms} \sqrt{\frac{8}{3\pi} \frac{V_M}{nV}}$	0	$I_{ac\ rms} \sqrt{2} \max\left(1, \frac{V_M}{nV}\right)$
Diode, xfmr secondary	$I_{dc} \sqrt{\frac{3}{2} + \frac{16}{3\pi} \frac{nV}{V_M}}$	I_{dc}	$2I_{dc} \left(1 + \frac{nV}{V_M}\right)$

with, in all cases, $\frac{I_{acrms}}{I_{dc}} = \sqrt{2} \frac{V}{V_M}$, ac input voltage = $V_M \sin(\omega t)$, dc output voltage = V .

these currents increase to 7.7 A, 42.5 A, and 11.4 A, respectively.

18.6 MODELING LOSSES AND EFFICIENCY IN CCM HIGH-QUALITY RECTIFIERS

As in the case of dc–dc converters, we would like to model the converter loss elements so that we can correctly specify the power stage components. The equivalent circuit approach used in the dc–dc case can be generalized to include ac–dc low harmonic rectifiers, although the resulting equations are more complicated because of the low-frequency ac modulation of the waveforms.

A dc–dc boost converter and its steady-state equivalent circuit are illustrated in Fig. 18.32. When the converter operates in equilibrium, the model of Fig. 18.32(b) can be solved to determine the converter losses and efficiency. In the ac–dc case, the input voltage $v_g(t)$ is a rectified sinusoid, and the controller varies the duty cycle $d(t)$ to cause $i_g(t)$ to follow $v_g(t)$ according to

$$i_g(t) = \frac{v_g(t)}{R_e} \quad (18.124)$$

The emulated resistance R_e is chosen by the controller such that the desired dc output voltage is obtained. Ac variations in $d(t)$, $v_g(t)$, and several other system waveforms are not small, and hence the small-signal approximation employed in Chapters 7 to 12 is not justified. We can continue to model the low-frequency components of the converter via averaging, but the resulting equivalent circuits are, in general, time-varying and nonlinear.

For the purposes of determining the rectifier efficiency, it is assumed that (1) the inductor is sufficiently small, such that it has negligible influence on the ac-line-frequency components of the system waveforms, and (2) the capacitor is large, so that the output voltage $v(t)$ is essentially equal to its equilibrium dc value, with negligible low- or high-frequency ac variations. So in the ac–dc case, the model becomes as shown in Fig. 18.33. Low-frequency components ($\ll f_s$) of the controller waveforms are sketched in Fig. 18.34.

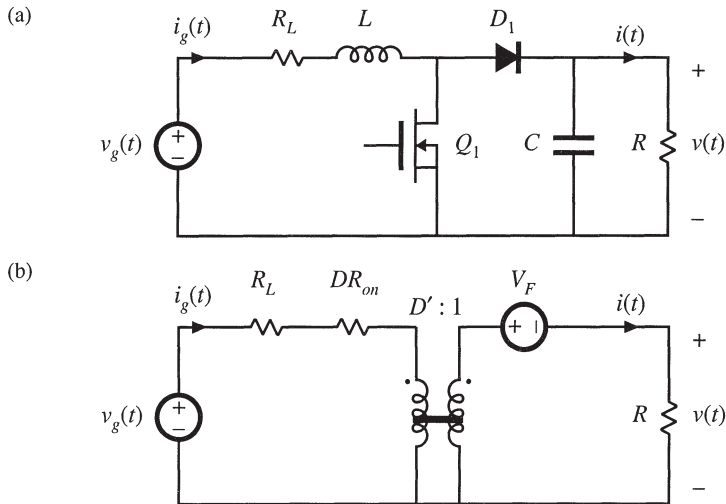


Fig. 18.32 Dc–dc boost converter, (a), and a steady-state equivalent circuit, (b), which models the inductor resistance R_L , MOSFET on-resistance R_{on} , and diode forward voltage drop V_F .

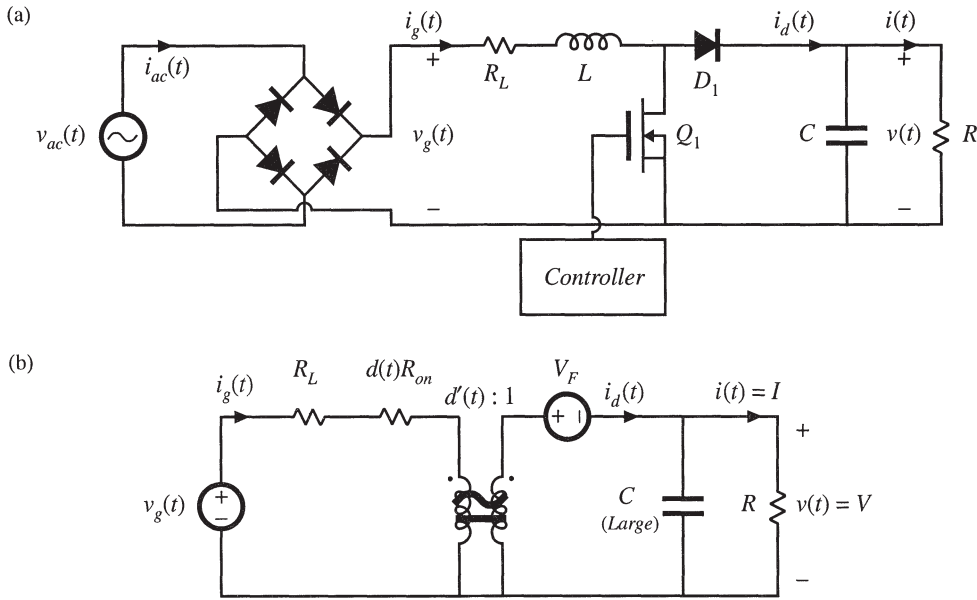


Fig. 18.33 Ac-dc boost rectifier, (a), and a low-frequency equivalent circuit, (b), that models converter losses and efficiency.

To find the rectifier waveforms, losses, and efficiency, we must solve the circuit of Fig. 18.33(b), under the conditions that the controller varies the duty cycle $d(t)$ such that Eq. (18.124) is satisfied. This leads to time-varying circuit elements $d(t)R_{on}$ and the $d'(t) : 1$ transformer. The solution that follows involves the following steps: (1) solve for the $d(t)$ waveform; (2) average $i_d(t)$ to find its dc component, equal to the load current I ; and (3) find other quantities of interest such as the rectifier efficiency.

The simplified boost converter circuit model of Fig. 18.35, in which only the MOSFET conduction loss is accounted for, is solved here. However, the results can be generalized directly to the circuit of Fig. 18.33(b); doing so is left as a homework problem. A similar procedure can also be followed to derive expressions for the losses and efficiencies of other rectifier topologies.

18.6.1 Expression for Controller Duty Cycle $d(t)$

The controller varies the duty cycle $d(t)$ such that Eq. (18.124) is satisfied. By solving the input-side loop of Fig. 18.35, we obtain

$$i_g(t)d(t)R_{on} = v_g(t) - d'(t)v \quad (18.125)$$

Substitute Eq. (18.124) into (18.125) to eliminate $i_g(t)$:

$$\frac{v_g(t)}{R_e} d(t)R_{on} = v_g(t) - d'(t)v \quad (18.126)$$

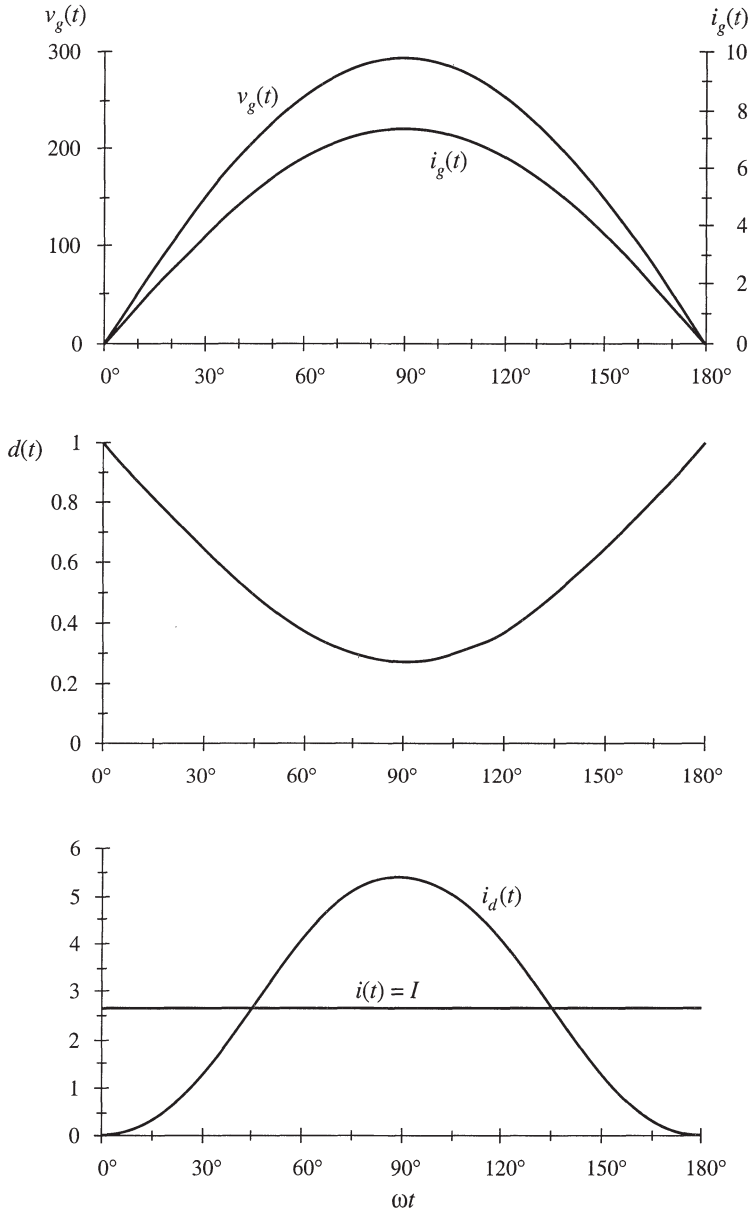


Fig. 18.34 Typical low-frequency components of the boost rectifier waveforms.

with
$$v_g(t) = V_M |\sin \omega t| \quad (18.127)$$

We can now solve for the duty cycle $d(t)$. The result is

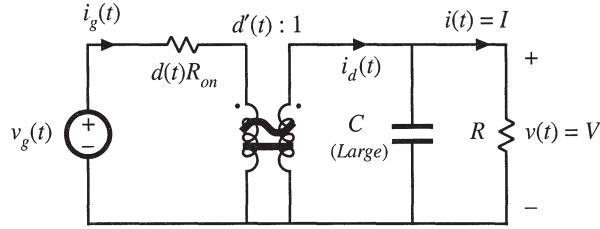


Fig. 18.35 Simplified boost power stage low-frequency equivalent circuit, in which only the MOSFET on-resistance is modeled.

$$d(t) = \frac{v - v_g(t)}{v - v_g(t) \frac{R_{on}}{R_e}} \quad (18.128)$$

This expression neglects the converter dynamics, an assumption that is justified when these dynamics are sufficiently faster than the ac line voltage variation. The expression also neglects operation in the discontinuous conduction mode near the zero-crossing of the ac line voltage waveform. This is justified when the rectifier operates in the continuous conduction mode for most of the ac line cycle, because the power loss near the zero-crossing is negligible.

18.6.2 Expression for the DC Load Current

By charge balance on output capacitor C , the dc load current I is equal to the dc component of the diode current i_d :

$$I = \langle i_d \rangle_{T_{ac}} \quad (18.129)$$

Solution of Fig. 18.35 for $i_d(t)$ yields

$$i_d(t) = d'(t)i_g(t) = d'(t) \frac{v_g(t)}{R_e} \quad (18.130)$$

From Eq. (18.128), $d'(t) = 1 - d(t)$ is given by

$$d'(t) = \frac{v_g(t) \left(1 - \frac{R_{on}}{R_e} \right)}{v - v_g(t) \frac{R_{on}}{R_e}} \quad (18.131)$$

so

$$i_d(t) = \frac{v_g^2(t)}{R_e} \frac{\left(1 - \frac{R_{on}}{R_e} \right)}{v - v_g(t) \frac{R_{on}}{R_e}} \quad (18.132)$$

Now substitute $v_g(t) = V_M \sin \omega t$, and integrate to find $\langle i_d(t) \rangle_{T_{ac}}$:

$$I = \langle i_d \rangle_{T_{ac}} = \frac{2}{T_{ac}} \int_0^{T_{ac}/2} \left(\frac{V_M^2}{R_e} \right) \frac{\left(1 - \frac{R_{on}}{R_e} \right) \sin^2(\omega t)}{\left(v - \frac{V_M R_{on}}{R_e} \sin(\omega t) \right)} dt \quad (18.133)$$

Again, $T_{ac} = 2\pi/\omega$ is the ac line period. Equation (18.133) can be rewritten as

$$I = \frac{2}{T_{ac}} \frac{V_M^2}{V R_e} \left(1 - \frac{R_{on}}{R_e} \right) \int_0^{T_{ac}/2} \frac{\sin^2(\omega t)}{1 - a \sin(\omega t)} dt \quad (18.134)$$

$$\text{where} \quad a = \left(\frac{V_M}{V} \right) \left(\frac{R_{on}}{R_e} \right) \quad (18.135)$$

By waveform symmetry, we need only integrate from 0 to $T_{ac}/4$. Also, make the substitution $\theta = \omega t$:

$$I = \frac{V_M^2}{V R_e} \left(1 - \frac{R_{on}}{R_e} \right) \frac{2}{\pi} \int_0^{\pi/2} \frac{\sin^2(\theta)}{1 - a \sin(\theta)} d\theta \quad (18.136)$$

Evaluation of this integral is tedious. It arises in not only the boost rectifier, but in a number of other high-quality rectifier topologies as well. The derivation is not given here, but involves the substitution $z = \tan(\theta/2)$, performing a partial fraction expansion of the resulting rational function of z , and integration of the results. The solution is:

$$\frac{4}{\pi} \int_0^{\pi/2} \frac{\sin^2(\theta)}{1 - a \sin(\theta)} d\theta = F(a) = \frac{2}{a^2 \pi} \left(-2a - \pi + \frac{4 \sin^{-1}(a) + 2 \cos^{-1}(a)}{\sqrt{1 - a^2}} \right) \quad (18.137)$$

This equation is somewhat complicated, but it is in closed form, and can easily be evaluated by computer spreadsheet. The quantity a , which is a measure of the loss resistance R_{on} relative to the emulated resistance R_e , is typically much smaller than 1. $F(a)$ is plotted in Fig. 18.36. The function $F(a)$ can be well-approximated as follows:

$$F(a) \approx 1 + 0.862a + 0.78a^2 \quad (18.138)$$

For $|a| \leq 0.15$, the $F(a)$ predicted by this approximate expression is within 0.1% of the exact value. If the a^2 term is omitted, then the accuracy drops to $\pm 2\%$ over the same range of a . The rectifier efficiency η calculated in the next section depends directly on $F(a)$, and hence the accuracy of $F(a)$ coincides with the accuracy of η .

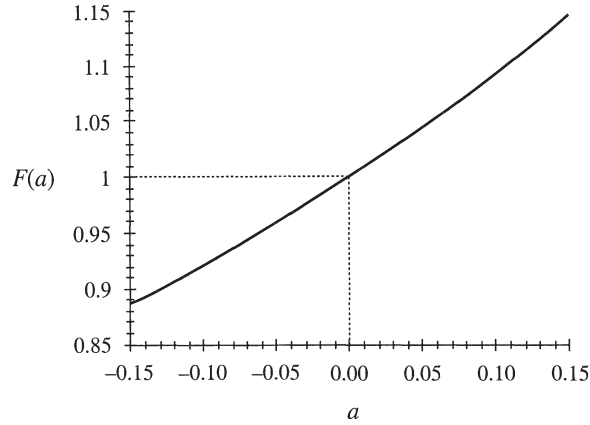


Fig. 18.36 Plot of the integral $F(a)$ vs. a .

18.6.3 Solution for Converter Efficiency η

Now that we have found the dc load current, we can calculate the converter efficiency η . The average input power is

$$P_{in} = \langle p_{in}(t) \rangle_{T_{ac}} = \frac{V_M^2}{2R_e} \quad (18.139)$$

The average load power is

$$P_{out} = VI = (V) \left(\frac{V_M^2}{VR_e} \left(1 - \frac{R_{on}}{R_e} \right) \frac{F(a)}{2} \right) \quad (18.140)$$

$$\text{where} \quad a = \left(\frac{V_M}{V} \right) \left(\frac{R_{on}}{R_e} \right) \quad (18.141)$$

Here, we have substituted Eq. (18.136) for I . The efficiency is therefore

$$\eta = \frac{P_{out}}{P_{in}} = \left(1 - \frac{R_{on}}{R_e} \right) F(a) \quad (18.142)$$

by substitution of Eqs. (18.139) and (18.140). If desired, the parabolic approximation for $F(a)$, Eq. (18.138), can be employed. This leads to

$$\eta \approx \left(1 - \frac{R_{on}}{R_e} \right) \left(1 + 0.862 \frac{V_M}{V} \frac{R_{on}}{R_e} + 0.78 \left(\frac{V_M}{V} \frac{R_{on}}{R_e} \right)^2 \right) \quad (18.143)$$

Equations (18.142) and (18.143) show how the efficiency varies with MOSFET on resistance R_{on} and

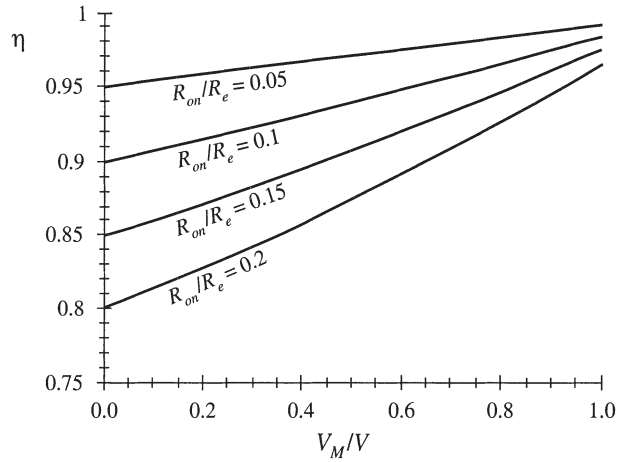


Fig. 18.37 Boost rectifier efficiency, Eq. (18.142), accounting for MOSFET on resistance.

with ac peak voltage V_M . Equation (18.142) is plotted in Fig. 18.37. It can be seen that high efficiency is obtained when the peak ac line voltage V_M is close to the dc output voltage V . Efficiencies in the range 90% to 95% can then be obtained, even with MOSFET on-resistances as high as $0.2R_e$. Of course, Fig. 18.37 is optimistic because it neglects sources of loss other than the MOSFET conduction loss.

18.6.4 Design Example

Let us utilize Fig. 18.37 to design for a given efficiency. Consider the following specifications:

Output voltage	390 V
Output power	500 W
rms input voltage	120 V
Efficiency	95%

Assume that losses other than the MOSFET conduction loss are negligible. The average input power is

$$P_{in} = \frac{P_{out}}{\eta} = \frac{500 \text{ W}}{0.95} = 526 \text{ W} \quad (18.144)$$

The emulated resistance is therefore

$$R_e = \frac{V_{g,rms}^2}{P_{in}} = \frac{(120 \text{ V})^2}{526 \text{ W}} = 27.4 \Omega \quad (18.145)$$

Also,

$$\frac{V_M}{V} = \frac{120\sqrt{2} \text{ V}}{390 \text{ V}} = 0.435 \quad (18.146)$$

From Fig. 18.37, or by evaluation of the exact equation (18.142), 95% efficiency with $V_M/V = 0.435$ occurs with $R_{on}/R_e \approx 0.077$. So we require a MOSFET having an on-resistance of

$$R_{on} \leq (0.077) R_e = (0.077) (27.4 \Omega) = 2.11 \Omega \quad (18.147)$$

Of course, other converter losses have not been accounted for, which will reduce the efficiency.

It is instructive to compare this result with that obtained using the expressions for rms current from Section 18.5. The rms transistor current of the ideal CCM boost converter is given by Eq. (18.119). The rms input current will be equal to $P_{in}/V_{g,rms} = (526 \text{ W})/(120 \text{ V}) = 4.38 \text{ A}$. Hence, Eq. (18.119) predicts an rms transistor current of

$$\begin{aligned} I_{Qrms} &= I_{ac rms} \sqrt{1 - \frac{8}{3\pi} \frac{V_M}{V}} \\ &= (4.38 \text{ A}) \sqrt{1 - \frac{8}{3\pi} \frac{(120 \text{ V}) \sqrt{2}}{(390 \text{ V})}} \\ &= 3.48 \text{ A} \end{aligned} \quad (18.148)$$

Hence, the MOSFET on-resistance should be chosen according to

$$R_{on} \leq \frac{P_{in} - P_{out}}{I_{Qrms}^2} = \frac{(526 \text{ W}) - (500 \text{ W})}{(4.38 \text{ A})^2} = 2.17 \Omega \quad (18.149)$$

This calculation is approximate because Eq. (18.119) was derived using the waveforms of the ideal (lossless) converter. Nonetheless, it gives an answer that is very close to the more exact result of Eq. (18.147). We would expect this approximate approach to exhibit good accuracy in this example, because of the high 95% efficiency.

18.7 IDEAL THREE-PHASE RECTIFIERS

The single-phase ideal rectifier concepts of the previous sections can be generalized to cover ideal three-phase rectifiers. Figure 18.38(a) illustrates the properties of an ideal three-phase rectifier, which presents a balanced resistive load to the utility system. A three-phase converter system is controlled such that resistor emulation is obtained in each input phase. The rectifier three-phase input port can then be modeled by per-phase effective resistances R_e , as illustrated in Fig. 18.38(a). The instantaneous powers apparently consumed by these resistors are transferred to the rectifier dc output port. The rectifier output port can therefore be modeled by power sources equal to the instantaneous powers flowing into the effective resistances R_e . It is irrelevant whether the three power sources are connected in series or in parallel; in either event, they can be combined into a single source equal to the total three-phase instantaneous input power as illustrated in Fig. 18.38(b).

If the three-phase ac input voltages are

$$\begin{aligned} v_{an}(t) &= V_M \sin(\omega t) \\ v_{bn}(t) &= V_M \sin(\omega t - 120^\circ) \\ v_{cn}(t) &= V_M \sin(\omega t - 240^\circ) \end{aligned} \quad (18.150)$$

then the instantaneous powers flowing into the phase a , b , and c effective resistances R_e are

$$\begin{aligned}
 p_a(t) &= \frac{v_{an}^2(t)}{R_e} = \frac{V_M^2}{2R_e} (1 - \cos(2\omega t)) \\
 p_b(t) &= \frac{v_{bn}^2(t)}{R_e} = \frac{V_M^2}{2R_e} (1 - \cos(2\omega t - 240^\circ)) \\
 p_c(t) &= \frac{v_{cn}^2(t)}{R_e} = \frac{V_M^2}{2R_e} (1 - \cos(2\omega t - 120^\circ))
 \end{aligned} \tag{18.151}$$

Each instantaneous phase power contains a dc term $V_M^2/(2R_e)$, and a second-harmonic term. The total instantaneous three-phase power is

$$p_{tot}(t) = p_a(t) + p_b(t) + p_c(t) = \frac{3}{2} \frac{V_M^2}{R_e} \tag{18.152}$$

This is the instantaneous power which flows out of the rectifier dc output port. Note that the second harmonic terms add to zero, such that the rectifier instantaneous output power is constant. This is a consequence of the fact that the instantaneous power flow in any balanced three-phase ac system is constant. So, unlike the single-phase case, the ideal three-phase rectifier can supply constant instantaneous power to a dc load, without the need for internal low-frequency energy storage.

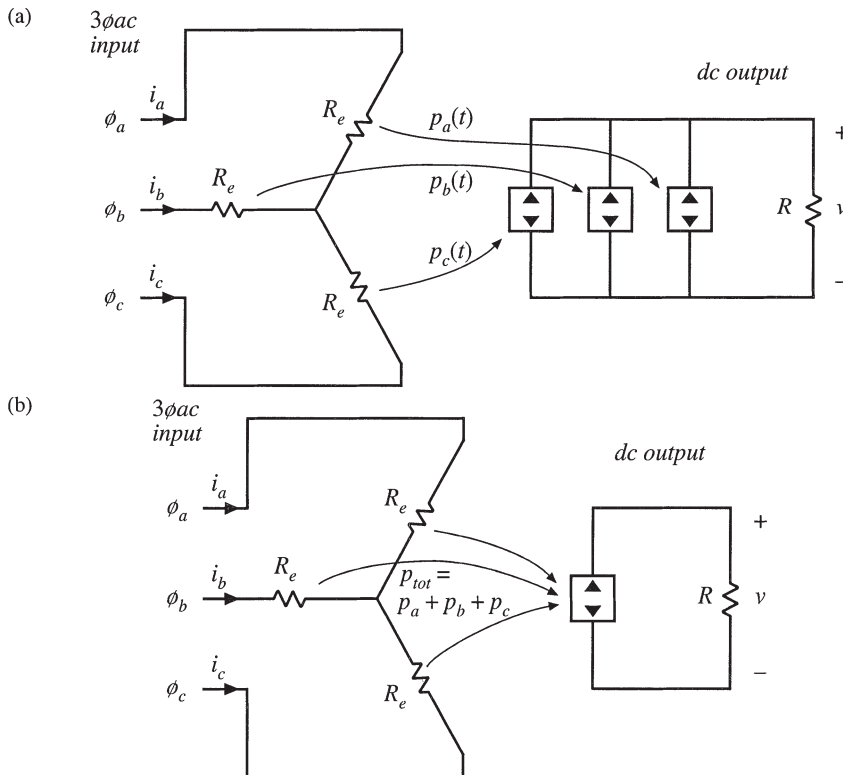


Fig. 18.38 Development of the ideal three-phase rectifier model: (a) three ideal single-phase rectifiers, (b) combination of the three power sources into an equivalent single power source.

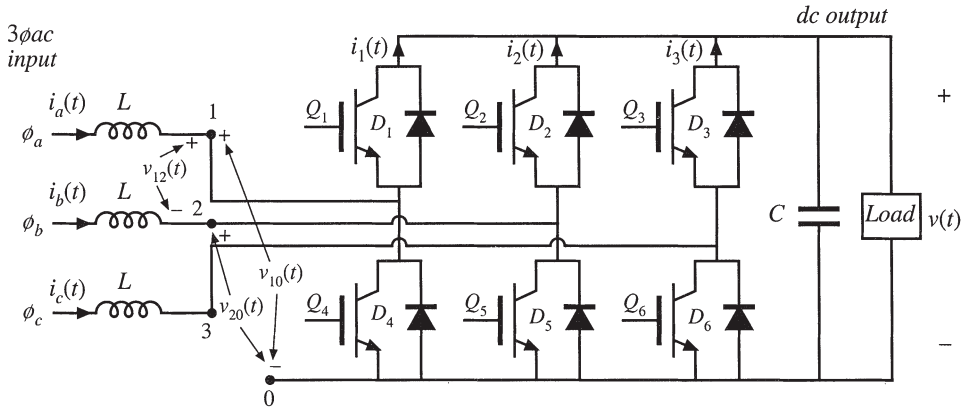


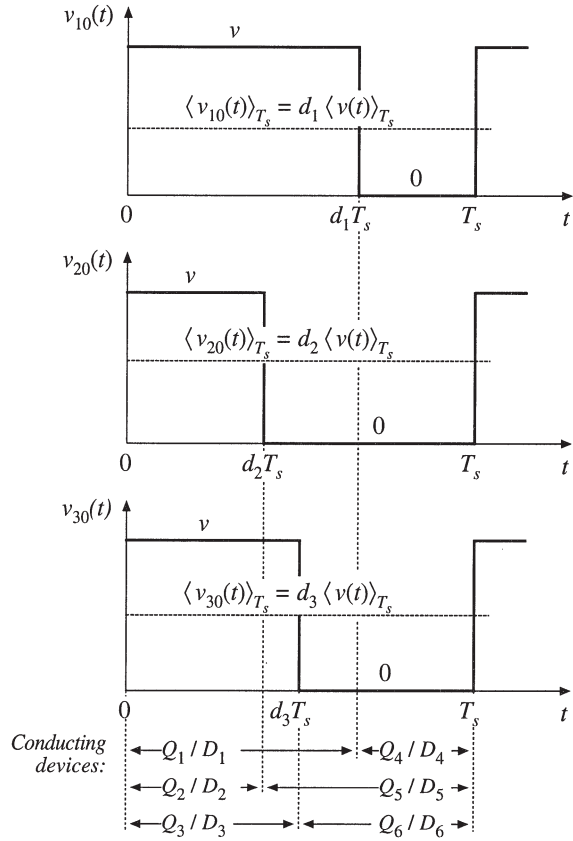
Fig. 18.39 Boost-type 3 ϕ ac–dc PWM rectifier.

A variety of 3 ϕ ac–dc PWM rectifiers are known; a few of the many references on this subject are listed in the references [42–59]. The most well-known topology is the three-phase ac–dc boost rectifier, illustrated in Fig. 18.39. This converter requires six SPST current-bidirectional two-quadrant switches. The inductors and capacitor filter the high-frequency switching harmonics, and have little influence on the low-frequency ac components of the waveforms. The switches of each phase are controlled to obtain input resistor emulation, either with a multiplying controller scheme similar to Fig. 18.5, or with some other approach. To obtain undistorted line current waveforms, the dc output voltage V must be greater than or equal to the peak line-to-line ac input voltage V_{Lpk} . In a typical realization, V is somewhat greater than V_{Lpk} . This converter resembles the voltage-source inverter, discussed briefly in Chapter 4, except that the converter is operated as a rectifier, and the converter input currents are controlled via high-frequency pulse-width modulation.

The three-phase boost rectifier of Fig. 18.39 has several attributes that make it the leading candidate for most 3 ϕ ac–dc rectifier applications. The ac input currents are nonpulsating, and hence very little additional input EMI filtering is required. As in the case of the single-phase boost rectifier, the rms transistor currents and also the conduction losses of the three-phase boost rectifier are low relative to other 3 ϕ ac–dc topologies such as the current-source inverter. The converter is capable of bidirectional power flow. A disadvantage is the requirement for six active devices; when compared with a dc–dc converter of similar ratings, the active semiconductor utilization (discussed in Chapter 6) is low. Also, since the rectifier has a boost characteristic, it is not suitable for direct replacement of traditional buck-type phase-controlled rectifiers.

The literature contains a wide variety of schemes for controlling the switches of a six-switch three-phase bridge network, which are applicable for control of the switches of Fig. 18.39. The basic operation of the converter can be most easily understood by assuming that the switches are controlled via simple sinusoidal pulse-width modulation. Transistor Q_1 is driven with duty cycle $d_1(t)$, while transistor Q_4 is driven by the complement of $d_1(t)$, or $d_1'(t) = 1 - d_1(t)$. Transistors Q_2 and Q_5 are driven with duty cycles $d_2(t)$ and $d_2'(t)$, respectively, and transistors Q_3 and Q_6 are driven with duty cycles $d_3(t)$ and $d_3'(t)$, respectively. The switch voltage waveforms of Fig. 18.40 are obtained. The average switch voltages are

Fig. 18.40 Switch waveforms, 3 ϕ ac-dc boost rectifier.



$$\begin{aligned}
 \langle v_{10}(t) \rangle_{T_s} &= d_1(t) \langle v(t) \rangle_{T_s} \\
 \langle v_{20}(t) \rangle_{T_s} &= d_2(t) \langle v(t) \rangle_{T_s} \\
 \langle v_{30}(t) \rangle_{T_s} &= d_3(t) \langle v(t) \rangle_{T_s}
 \end{aligned} \tag{18.153}$$

The averaged line-to-line switch voltages are therefore

$$\begin{aligned}
 \langle v_{12}(t) \rangle_{T_s} &= \langle v_{10}(t) \rangle_{T_s} - \langle v_{20}(t) \rangle_{T_s} = (d_1(t) - d_2(t)) \langle v(t) \rangle_{T_s} \\
 \langle v_{23}(t) \rangle_{T_s} &= \langle v_{20}(t) \rangle_{T_s} - \langle v_{30}(t) \rangle_{T_s} = (d_2(t) - d_3(t)) \langle v(t) \rangle_{T_s} \\
 \langle v_{31}(t) \rangle_{T_s} &= \langle v_{30}(t) \rangle_{T_s} - \langle v_{10}(t) \rangle_{T_s} = (d_3(t) - d_1(t)) \langle v(t) \rangle_{T_s}
 \end{aligned} \tag{18.154}$$

In a similar manner, the average switch currents can be shown to be

$$\begin{aligned}
 \langle i_1(t) \rangle_{T_s} &= d_1(t) \langle i_a(t) \rangle_{T_s} \\
 \langle i_2(t) \rangle_{T_s} &= d_2(t) \langle i_b(t) \rangle_{T_s} \\
 \langle i_3(t) \rangle_{T_s} &= d_3(t) \langle i_c(t) \rangle_{T_s}
 \end{aligned}
 \quad (18.155)$$

Equations (18.154) and (18.155) lead to the circuit-averaged model of Fig. 18.41.

With sinusoidal PWM, the duty cycles are varied sinusoidally in synchronism with the ac line, as follows:

$$\begin{aligned}
 d_1(t) &= D_0 + \frac{1}{2} D_m \sin(\omega t - \varphi) \\
 d_2(t) &= D_0 + \frac{1}{2} D_m \sin(\omega t - \varphi - 120^\circ) \\
 d_3(t) &= D_0 + \frac{1}{2} D_m \sin(\omega t - \varphi - 240^\circ)
 \end{aligned}
 \quad (18.156)$$

where ω is the ac line frequency. Since each instantaneous duty cycle must lie in the interval $[0,1]$, the dc bias D_0 is required. The factor D_m is called the *modulation index*; for $D_0 = 0.5$, D_m must be less than or equal to one. Other choices of D_0 further restrict D_m . In general, the modulation index can be defined as equal to the peak-to-peak amplitude of the fundamental component of the duty cycle variation.

If the switching frequency is sufficiently large, then filter inductors L can be small in value, such that they have negligible effect on the low-frequency ac waveforms. The averaged switch voltage $\langle v_{12}(t) \rangle_{T_s}$ then becomes approximately equal to the ac line-line voltage $v_{ab}(t)$:

$$\langle v_{12}(t) \rangle_{T_s} = (d_1(t) - d_2(t)) \langle v(t) \rangle_{T_s} \approx v_{ab}(t) \quad (18.157)$$

Substitution of Eqs. (18.150) and (18.156) leads to

$$\frac{1}{2} D_m \left[\sin(\omega t - \varphi) - \sin(\omega t - \varphi - 120^\circ) \right] \langle v(t) \rangle_{T_s} = V_M \left[\sin(\omega t) - \sin(\omega t - 120^\circ) \right] \quad (18.158)$$

For small L , the angle φ must tend to zero, and hence the sinusoidal terms in Eq. (18.158) cancel out. In steady-state, the dc output voltage is $\langle v(t) \rangle_{T_s} = V$. Equation (18.158) then becomes

$$\frac{1}{2} D_m V = V_M \quad (18.159)$$

Solution for the dc output voltage V leads to

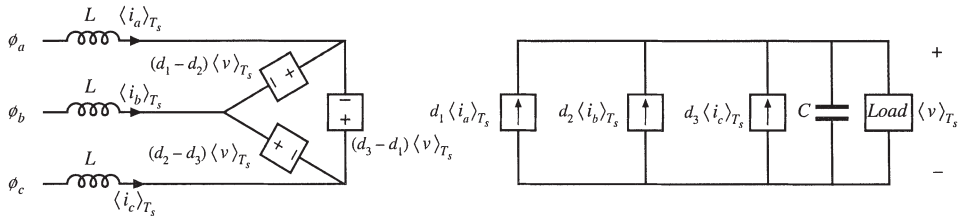


Fig. 18.41 Averaged model of the open-loop 3 ϕ ac-dc boost rectifier.

$$V = \frac{2V_M}{D_m} \quad (18.160)$$

Equation (18.160) can be written in terms of the peak line-to-line voltage $V_{L,pk}$, as

$$V = \frac{2}{\sqrt{3}} \frac{V_{L,pk}}{D_m} = 1.15 \frac{V_{L,pk}}{D_m} \quad (18.161)$$

With $D_m \leq 1$, the dc output voltage V must be greater than or equal to 1.15 times the peak line-to-line ac input voltage. Thus, the rectifier has a boost characteristic.

The sinusoidal PWM approach of Eq. (18.156) is not the only way to vary the duty cycles to obtain sinusoidal ac voltages and currents. For example, triplen harmonics can be added to the duty cycle expressions of Eq. (18.156). These triplen harmonics cancel out in Eq. (18.154), such that the average inverter input voltages $\langle v_{12}(t) \rangle_{T_s}$, $\langle v_{23}(t) \rangle_{T_s}$, and $\langle v_{31}(t) \rangle_{T_s}$ contain only fundamental. Figure 18.42 illustrates duty cycle variations that lead to a dc output voltage V equal to $V_{L,pk}$. The effective modulation index in this case is 1.15. The ac-side voltages and currents are again undistorted. Further increases in the modulation index can be attained only by introduction of distortion in the ac-side voltages and currents. Of course, in practice the duty cycle modulations are usually generated by the feedback loops that control the input current waveforms to attain resistor emulation.

Three-phase ac-to-dc rectifiers having buck, buck-boost, or other characteristics, are possible, but find much less use than the boost topology. A 3 ϕ ac-dc rectifier system can also be constructed simply using three separate single-phase rectifiers [34]; however, each single-phase rectifier must then contain transformer isolation, leading to substantially increased switch stress and loss. Other unconventional approaches to three-phase low-harmonic rectification have also been recently explored, such as the Vienna rectifier [56,59], single-switch approaches [49–55], and other circuits[44,45,46,57,58].

Yet another approach to solving the problem of three-phase rectifier harmonics is the *harmonic correction* scheme illustrated in Fig. 18.43. An active six-switch three-phase bridge removes the harmonics generated by a nonlinear three-phase load such as an uncontrolled rectifier. The harmonic corrector is controlled such that its ac line currents contain harmonics that are equal in magnitude but opposite in phase to the harmonics generated by the nonlinear load. No average power flows into the harmonic corrector. The total kVA rating of the harmonic corrector semiconductor devices depends on the magnitudes of the harmonics produced by the nonlinear load. If the THD generated by the load is not too large, then

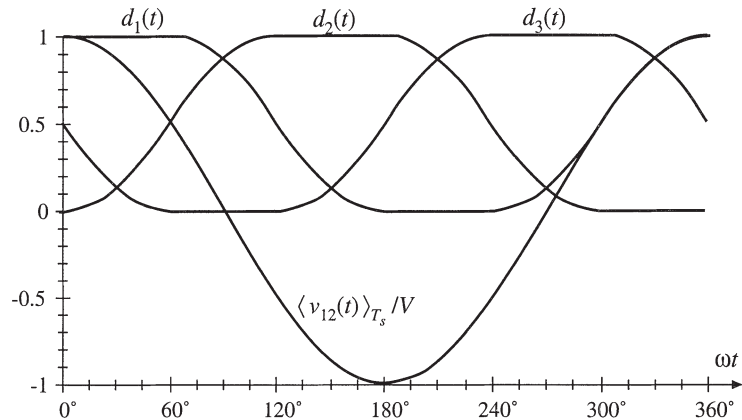


Fig. 18.42 A modulation strategy that leads to a dc output voltage equal to the peak input line-line voltage.

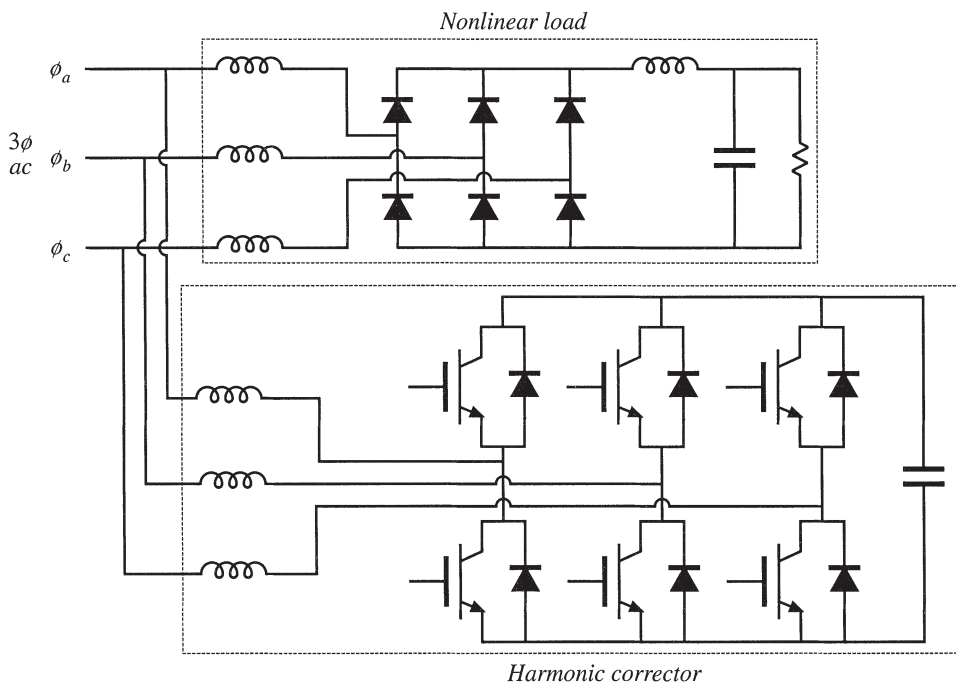


Fig. 18.43 A harmonic corrector, based on the 3 ϕ ac–dc CCM boost converter of Fig. 18.39.

the harmonic corrector scheme requires less total active silicon than the CCM boost-type rectifier of Fig. 18.39. But if the uncontrolled rectifier contains small ac line inductances, such that it operates in the discontinuous conduction mode with large THD, then it is probably better to simply replace the uncontrolled rectifier with the CCM boost-type rectifier of Fig. 18.39.

18.8 SUMMARY OF KEY POINTS

1. The ideal rectifier presents an effective resistive load, the emulated resistance R_e , to the ac power system. The power apparently “consumed” by R_e is transferred to the dc output port. In a three-phase ideal rectifier, input resistor emulation is obtained in each phase. In both the single-phase and three-phase cases, the output port follows a power source characteristic, dependent on the instantaneous ac input power. Ideal rectifiers can perform the function of low-harmonic rectification, without need for low-frequency reactive elements.
2. The dc–dc boost converter, as well as other converters capable of increasing the voltage according to Eq. (18.12), can be adapted to the ideal rectifier application. A control system causes the input current to be proportional to the input voltage. The converter may operate in CCM, DCM, or in both modes. The mode boundary can be expressed as a function of R_e , $2L/T_s$, and the instantaneous voltage ratio $v_g(t)/V$. A well-designed average current controller leads to resistor emulation regardless of the operating mode; however, other schemes may lead to distorted current waveforms when the mode boundary is crossed.
3. In a single-phase system, the instantaneous ac input power is pulsating, while the dc load power is constant. Whenever the instantaneous input and output powers are not equal, the ideal rectifier system must

contain energy storage. A large capacitor is commonly employed; the voltage of this capacitor must be allowed to vary independently, as necessary to store and release energy. A slow feedback loop regulates the dc component of the capacitor voltage, to ensure that the average ac input power and dc load power are balanced.

4. RMS values of rectifiers waveforms can be computed by double integration. In the case of the boost converter, the rms transistor current can be as low as 39% of the rms ac input current, when the dc output voltage V is close in value to the peak ac input voltage V_M . Other converter topologies such as the buck-boost, SEPIC, and Ćuk converters exhibit significantly higher rms transistor currents but are capable of limiting the converter inrush current.
5. In the three-phase case, a boost-type rectifier based on the PWM voltage-source inverter also exhibits low rms transistor currents. This approach requires six active switching elements, and its dc output voltage must be greater than the peak input line-to-line voltage. Average current control can be used to obtain input resistor emulation. An equivalent circuit can be derived by averaging the switch waveforms. The converter operation can be understood by assuming that the switch duty cycles vary sinusoidally; expressions for the average converter waveforms can then be derived.
6. Converter losses and efficiency can be modeled using the steady-state equivalent circuit models of Chapter 3, with a time-varying duty cycle. The output current is averaged over one ac line period, to determine its dc component. The converter losses and efficiency can then be computed. This approach is approximate, in that (i) it assumes that the converter dynamics are much faster than the ac line frequency, and (ii) it neglects operation in the discontinuous conduction mode.
7. Average current control involves direct regulation of the low-frequency components of the rectifier input current to follow the input voltage. Feedforward can also be added, to cancel the influence of ac line voltage variations on the dc output voltage.
8. Current programmed control can also be adapted to attain input resistor emulation in rectifiers. The programmed current reference signal $i_c(t)$ is made proportional to the ac input voltage. The difference between $i_c(t)$ and the average inductor current leads to distortion, owing to the inductor current ripple and the need for a stabilizing artificial ramp. Several approaches are known for reducing the resulting harmonic distortion of the line current waveform.
9. Hysteretic control, particularly with 100% current ripple, has a simple controller implementation. The disadvantages are variable switching frequency, and increased peak currents.
10. Nonlinear carrier control also leads to a simple controller implementation, and has the advantage of CCM operation with small peak transistor current.
11. The outer low-bandwidth control system, which regulates the dc output voltage to balance the rectifier and load powers, can be modeled by averaging the rectifier waveforms over one-half of the ac line period T_{2L} . This causes the dc-side system equations to become time-invariant. A small-signal model is then obtained by perturbation and linearization.
12. The inner high-bandwidth control system, which regulates the ac input current waveform to attain resistor emulation, is in general highly nonlinear. However, in the case of the boost rectifier, a valid small-signal model can be derived. This approach is unsuccessful in the case of other converters; one must then resort to other approaches such as the quasi-static approximation or simulation.

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PROBLEMS

- 18.1** The boost converter of Fig. 18.5 is replaced by a buck-boost converter. Inductor energy storage has negligible influence on the low-frequency components of the converter waveforms. The average load power is P_{load} . The dc output voltage is V and the sinusoidal ac input voltage has peak amplitude V_M .
- (a) Determine expressions for the duty cycle variations $d(t)$ and the inductor current variation $i(t)$, assuming that the converter operates in the continuous conduction mode.
 - (b) Derive the conditions for operation in the continuous conduction mode. Manipulate your result to show that the converter operates in CCM when R_e is less than $R_{e,crit}(L, T_s, v_g(t), V)$, and determine $R_{e,crit}$.
 - (c) For what values of R_e does the converter always operate in CCM? in DCM?
 - (d) The ac input voltage has rms amplitude in the range 108 V to 132 V. The maximum load power is 100 W, and the minimum load power is 10 W. The dc output voltage is 120 V. The switching frequency is 75 kHz. What value of L guarantees that the converter always operates in CCM? in DCM?

- 18.2** Derive expressions for the input characteristics of the buck-boost converter, similar to Eqs. (18.25) to (18.33). Sketch the converter input characteristics, and label the CCM–DCM boundary.
- 18.3** Derive expressions for the rms transistor and diode currents of rectifiers based on the single-phase CCM Čuk topology. Express your results in forms similar to those of Table 18.3.
- 18.4** To obtain an isolated dc output, the boost converter in Fig. 18.5 is replaced by the full-bridge transformer-isolated CCM boost converter of Fig. 6.35. Derive an expression for the rms transistor current. Express your result as a function of $I_{ac\ rms}$, n , V , and V_M .
- 18.5** Comparison of CCM boost and isolated SEPIC topologies as universal-input single-phase rectifiers. You are given that the dc output voltage is $V = 400$ V, the load power is $P = 500$ W, and the rms input voltage varies between 90 and 270 V, such that the peak ac input voltage V_M varies between $V_{Mmin} = 127$ V and $V_{Mmax} = 382$ V. Define the transistor stress S as the product of the worst-case peak transistor voltage and the worst-case rms transistor current. It is desired to minimize S .
- Determine S for the boost converter in this application.
 - Briefly discuss your result of part (a): if universal input operation was not required, and hence $V_M = 382$ V always, what S would result?
- In the isolated SEPIC, the transformer turns ratio $n : 1$ can be chosen to optimize the design.
- Express S for the SEPIC as a function of n , V , P , V_{Mmin} , and V_{Mmax} .
 - Choose n for the SEPIC such that S is minimized in this application. Compare with the results of parts (a) and (b).
- 18.6** In the boost-type dc–3 ϕ ac rectifier of Fig. 18.39, the ac-side inductances L are not small: they exhibit line-frequency impedances that should not be ignored. The three-phase ac voltages are given by Eq. (18.150), and the duty cycles are modulated as in Eq. (18.156). The converter operates in the continuous conduction mode.
- Determine the magnitudes and phases of the line-to-neutral average voltages at the ac inputs to the switch network. Express your result in terms of D_m , V , and ϕ .
 - Determine the real power P and reactive power Q drawn from the 3 ϕ ac source. Express your results as functions of V_M , V , D_m , ϕ , and ωL .
 - How must ϕ be chosen to obtain unity power factor?
- 18.7** In the boost-type dc–3 ϕ ac rectifier of Fig. 18.39, the switch duty ratios are modulated as illustrated in Fig. 18.42. When the inductances L are sufficiently small, a dc output voltage V equal to the peak line-to-line ac input voltage can be obtained, with undistorted ac line currents. As illustrated in Fig. 18.42, $d_1(t)$ is equal to 1 for $0^\circ \leq \omega t \leq 60^\circ$, where $\omega t = 0^\circ$ when $\langle v_{12}(t) \rangle_{T_s} = V$.
- Derive expressions for $d_2(t)$ and $d_3(t)$, over the interval $0^\circ \leq \omega t \leq 60^\circ$.
 - State how $d_1(t)$, $d_2(t)$, and $d_3(t)$ should vary over each 60° interval.
- 18.8** The buck-type 3 ϕ ac–dc rectifier of Fig. 18.44 operates in the continuous conduction mode. Transistors Q_1 to Q_6 operate with duty cycles $d_1(t)$ to $d_6(t)$, respectively.
- Determine the constraints on switch operation. Which transistors must not conduct simultaneously? Which duty cycles must total unity?
 - Average the 3 ϕ bridge switch network, to determine expressions for the average ac-side switch currents $\langle i_a(t) \rangle_{T_s}$, $\langle i_b(t) \rangle_{T_s}$, and $\langle i_c(t) \rangle_{T_s}$.
 - Show that the average dc-side switch voltage can be expressed as

$$\langle v_d(t) \rangle_{T_s} = (d_1(t) - d_4(t)) \langle v_{an}(t) \rangle_{T_s} + (d_2(t) - d_5(t)) \langle v_{bn}(t) \rangle_{T_s} + (d_3(t) - d_6(t)) \langle v_{cn}(t) \rangle_{T_s}$$

- The duty cycles are varied as follows:

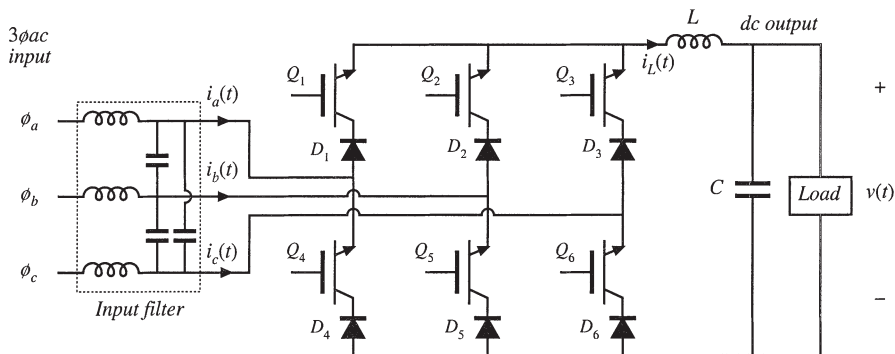


Fig. 18.44 Buck-type 3 ϕ ac–dc rectifier, Problem 18.8.

$$\begin{aligned} d_1(t) &= \frac{1}{3} + \frac{1}{2} D_m \sin(\omega t - \varphi) \\ d_2(t) &= \frac{1}{3} + \frac{1}{2} D_m \sin(\omega t - \varphi - 120^\circ) \\ d_3(t) &= \frac{1}{3} + \frac{1}{2} D_m \sin(\omega t - \varphi - 240^\circ) \\ d_4(t) &= \frac{1}{3} - \frac{1}{2} D_m \sin(\omega t - \varphi) \\ d_5(t) &= \frac{1}{3} - \frac{1}{2} D_m \sin(\omega t - \varphi - 120^\circ) \\ d_6(t) &= \frac{1}{3} - \frac{1}{2} D_m \sin(\omega t - \varphi - 240^\circ) \end{aligned}$$

with the ac input voltages given by Eq. (18.150). The input filter has negligible effect of the low-frequency components of the converter waveforms. Determine the steady-state dc output voltage V_o as a function of V_M , D_m , and φ .

- (e) Determine the power factor. You may assume that the input filter completely removes the switching harmonics from the currents $i_a(t)$, $i_b(t)$, and $i_c(t)$. However, the input filter elements consume or supply negligible line-frequency reactive power.

18.9

In the three-phase DCM flyback rectifier of Fig. 18.45, the input filter has negligible effect on the low-frequency components of the input ac waveforms. The transistor operates with switching frequency f_s and duty cycle d . Flyback transformers T_1 , T_2 , and T_3 each have magnetizing inductance L referred to the primary, turns ratio $n : 1$, and have negligible leakage inductances.

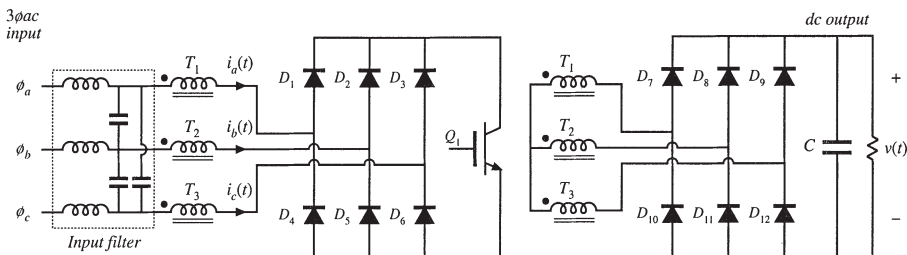


Fig. 18.45 Isolated 3 ϕ ac–dc rectifier based on the flyback converter operating in discontinuous conduction mode; Problem 18.9.

- (a) Determine expressions for the low-frequency components of the ac input and dc output currents.
 (b) Derive an averaged equivalent circuit model for the converter, and give expressions for the ele-

ment values.

- (c) Derive the conditions for operation in the discontinuous conduction mode.
- 18.10** Power stage design of a universal-input boost rectifier. The objective of this problem is to work out the power stage design of a low harmonic rectifier based on the boost converter. This converter is to be designed to operate anywhere in the world, and hence the input voltage may vary over the range 90 to 270 Vrms, 50 to 60 Hz. The converter produces a regulated 385 V dc output, at 1000 W. The switching frequency f_s is 100 kHz. You may assume that the controller operates perfectly, to produce an undistorted ac line current waveform and a well-regulated dc output voltage.
- (a) Derive an expression for how the duty cycle $d(t)$ will vary over the ac line cycle. You may neglect converter dynamics and losses. Sketch $d(t)$ under conditions of maximum and minimum ac line voltage.
- (b) Specify the inductor:
- Specify the value of L such that, at the peak of the sinusoidal input voltage, and under worst-case conditions, the inductor current ripple Δi_g is 20% of the instantaneous low frequency current $i_g(t)$.
 - Specify the worst-case values of the peak and rms inductor current, assuming 100% efficiency.
- (c) Determine the worst-case rms currents of the MOSFET and diode, assuming 100% efficiency.
- (d) Specify the value of C that leads to a worst-case low-frequency ($\ll f_s$) output voltage peak-peak ripple of 5 V.
- (e) Given the following loss elements
- | | |
|-----------------------------|---------------------------------------|
| Inductor winding resistance | 0.1 Ω |
| MOSFET on-resistance | 0.4 Ω |
| Diode forward voltage drop | 1.5 V |
| Switching loss: model as | $i_g^2(t)(0.25 \text{ } \mu\text{W})$ |
- For a constant 1000 W load, and assuming that the controller operates perfectly as described above, find the rectifier efficiency
- at an ac input voltage of 90 V rms
 - at an ac input voltage of 270 V rms

- 18.11** The flyback converter shown in Fig. 18.46 operates in the continuous conduction mode. The MOSFET

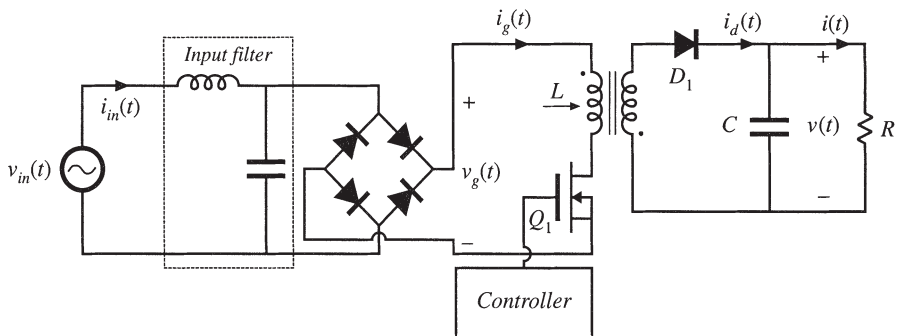


Fig. 18.46 Low-harmonic rectifier system based on the CCM flyback converter, Problem 18.11.

has on-resistance R_{on} , and diode D_1 has a constant forward voltage drop V_D . All other loss elements can

be neglected. The turns ratio of the flyback transformer is 1:1. The controller varies the duty cycle such that $\langle i_g(t) \rangle_{T_s}$ is equal to $v_g(t)/R_e$, where R_e is the emulated resistance. The input voltage is $v_{in}(t) = V_M \sin(\omega t)$. The input filter removes the switching harmonics from the input current $i_g(t)$, but has negligible effect on the low-frequency components of the converter waveforms.

- Derive an expression for the rectifier efficiency, in terms of V_M , V , V_D , R_{on} , and R_e .
- Given the following values, find the value of MOSFET on-resistance which leads to an efficiency of 96%.

rms input voltage	120 V
Dc output voltage	120 V
Diode D_1 forward voltage drop	1.5 V
Load power	200 W

18.12 Derive an expression for the emulated resistance $R_e(V_{g,rms}, R_s, k_v, v_{control})$ of the average-current-controlled boost rectifier with ac line voltage feedforward, Fig. 18.14.

18.13 Derive the CPM boost rectifier static input characteristics, Eq. (18.57).

18.14 The boost rectifier system of Fig. 18.47 employs average current control with ac line voltage feedforward.

The ac line frequency is 50 Hz. The rectifier drives a constant-power load of 500 W. The pulse-width modulator contains a ramp having a peak-to-peak amplitude of 3 V. There is no compensator in the inner wide-bandwidth average current control feedback loop. The average current sensing circuit has gain

$$\frac{v_a(s)}{i_g(s)} = \frac{R_s}{1 + \frac{s}{\omega_0}}$$

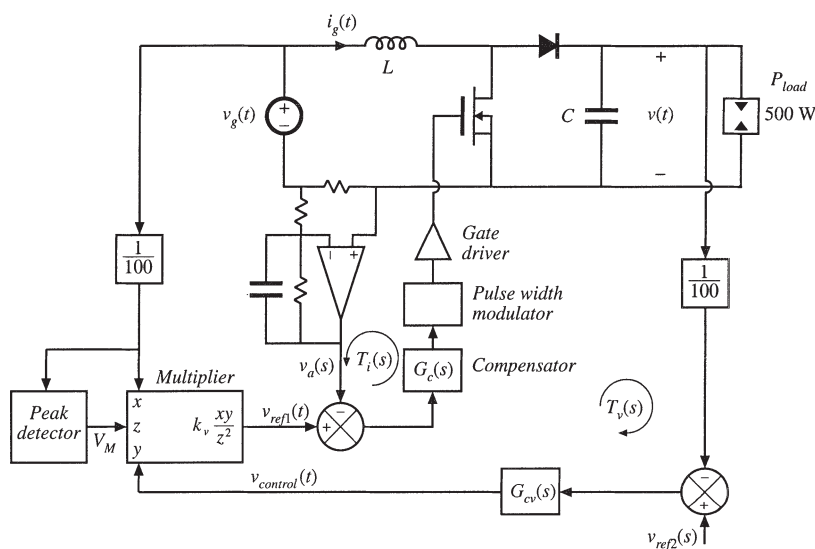


Fig. 18.47 Average current controlled boost rectifier with input voltage feedforward, Problem 18.14.

Other converter parameter values are

$$f_s = 100 \text{ kHz}$$

$$L = 2.5 \text{ mH}$$

$$f_0 = \frac{\omega_0}{2\pi} = 10 \text{ kHz}$$

$$R_s = 1 \text{ } \Omega$$

$$V = 385 \text{ V}$$

$$V_{g,rms} = 230 \text{ V}$$

- (a) Construct the magnitude and phase Bode diagrams of the loop gain $T_i(s)$ of the average-current-control loop. Label important features.
- (b) Determine numerical values of the crossover frequency and phase margin of $T_i(s)$.

The outer low-bandwidth feedback loop has loop gain $T_v(s)$. The compensator of this loop has constant gain $G_{cv}(s) = 330$. The multiplier gain is $k_v = 2$. The capacitor value is $C = 680 \text{ } \mu\text{F}$. The reference voltage $v_{ref}(t)$ is 3.85 V.

- (c) Determine the peak magnitude of the output 100 Hz voltage ripple.
- (d) Determine the quiescent control voltage $V_{control}$.
- (e) Construct the magnitude and phase Bode diagrams of the loop gain $T_v(s)$ of the outer feedback loop. Label important features.
- (f) Determine numerical values of the crossover frequency and phase margin of $T_v(s)$.

18.15

A critical conduction mode controller causes a boost rectifier to exhibit an ac input current waveform similar to Fig. 18.19(b). The ac input voltage is 120 Vrms at 60 Hz. The rectifier supplies 225 Vdc to a 120 W load. The boost converter inductance is $L = 600 \text{ } \mu\text{H}$.

- (a) Determine the emulated resistance R_e .
- (b) Write the numerical expression for the converter switching frequency f_s , as a function of t_{on} and the applied terminal voltages. Sketch f_s vs. time.
- (c) What is the maximum switching frequency? What is the minimum switching frequency?
- (d) Derive an analytical expression for the rms transistor current for this control method, as a function of the magnitude of the sinusoidal line current. Compare the rms transistor current of this approach with a CCM boost rectifier having negligible current switching ripple.

Part V

Resonant Converters

19

Resonant Conversion

Part V of this text deals with a class of converters whose operation differs significantly from the PWM converters covered in Parts I to IV. *Resonant power converters* [1–36] contain resonant L – C networks whose voltage and current waveforms vary sinusoidally during one or more subintervals of each switching period. These sinusoidal variations are large in magnitude, and hence the small ripple approximation introduced in Chapter 2 does not apply.

Dc-to-high-frequency-ac inverters are required in a variety of applications, including electronic ballasts for gas discharge lamps [3,4], induction heating, and electrosurgical generators. These applications typically require generation of a sinusoid of tens or hundreds of kHz, having moderate or low total harmonic distortion. A simple resonant inverter system is illustrated in Fig. 19.1(a). A switch network produces a square wave voltage $v_s(t)$. As illustrated in Fig. 19.2, the spectrum of $v_s(t)$ contains fundamental plus odd harmonics. This voltage is applied to the input terminals of a resonant tank network. The tank network resonant frequency f_0 is tuned to the fundamental component of $v_s(t)$, that is, to the switching frequency f_s , and the tank exhibits negligible response at the harmonics of f_s . In consequence, the tank current $i_s(t)$, as well as the load voltage $v(t)$ and load current $i(t)$, have essentially sinusoidal waveforms of frequency f_s , with negligible harmonics. By changing the switching frequency f_s (closer to or further from the resonant frequency f_0), the magnitudes of $i_s(t)$, $v(t)$, and $i(t)$ can be controlled. Other schemes for control of the output voltage, such as phase-shift control of the bridge switch network, are also possible. A variety of resonant tank networks can be employed; Fig. 19.1(b) to (d) illustrate the well-known *series*, *parallel*, and *LCC* tank networks. Inverters employing the series resonant tank network are known as the *series resonant*, or *series loaded*, inverter. In the *parallel resonant* or *parallel loaded* inverter, the load voltage is equal to the resonant tank capacitor voltage. The LCC inverter employs tank capacitors both in series and in parallel with the load.

Figure 19.3 illustrates a high-frequency inverter of an electronic ballast for a gas-discharge lamp. A half-bridge configuration of the LCC inverter drives the lamp with an approximately sinusoidal

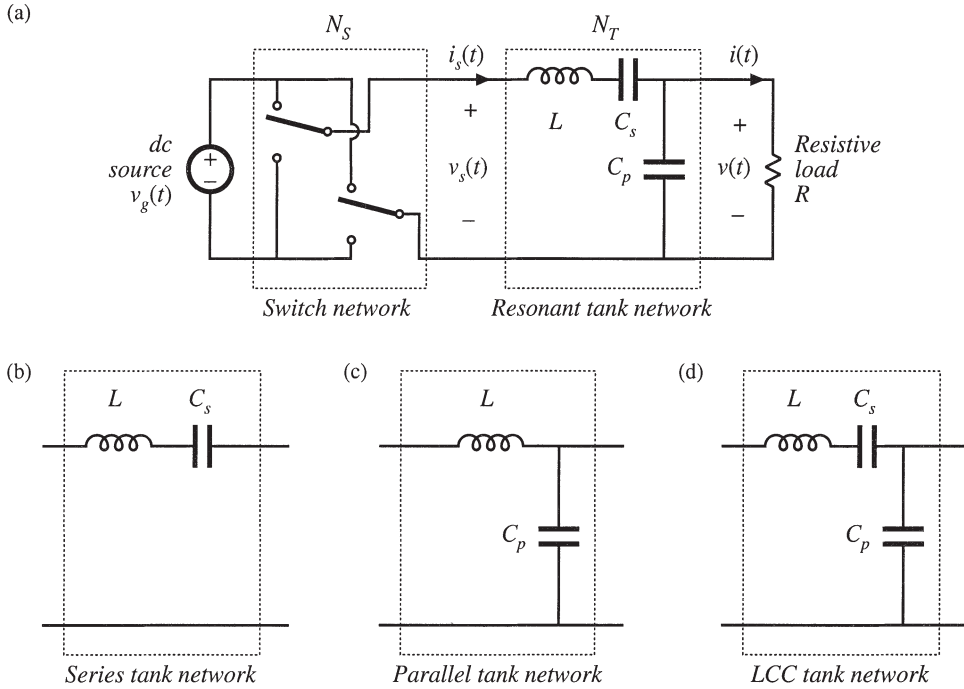
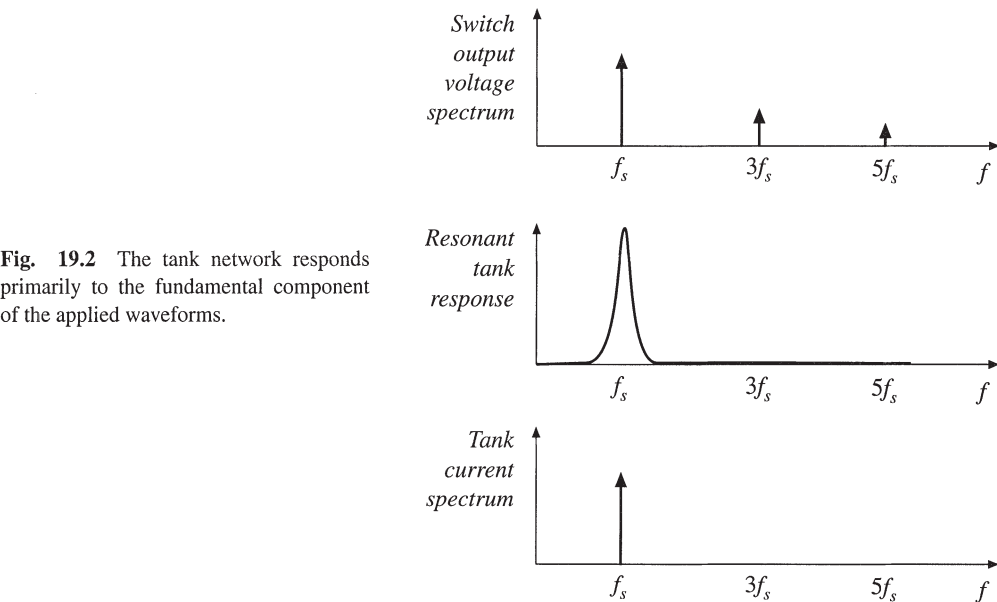


Fig. 19.1 A basic class of resonant inverters that consist of (a) a switch network N_S that drives a resonant tank network N_T near resonance. Several common tank networks: (b) series, (c) parallel, (d) LCC.



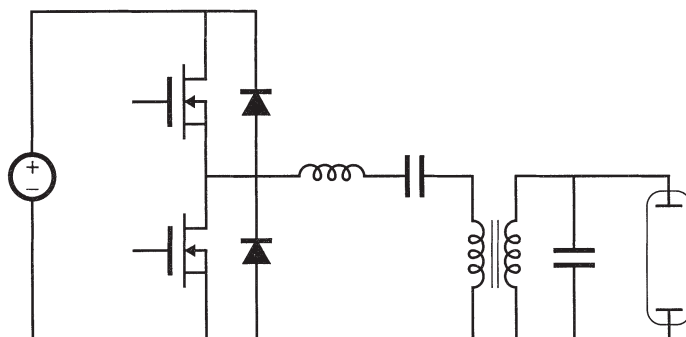


Fig. 19.3 Half-bridge LCC inverter circuit, as an electronic ballast for a gas-discharge lamp.

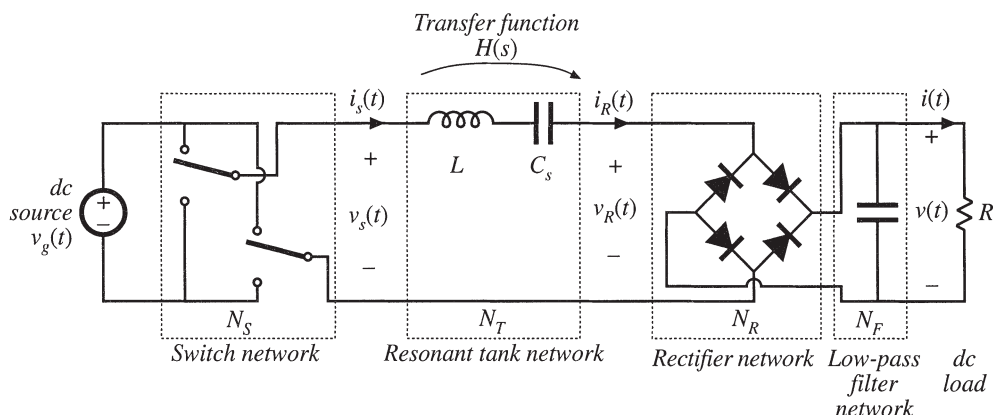


Fig. 19.4 Derivation of a resonant dc-dc converter, by rectification and filtering of the output of a resonant inverter.

high-frequency ac waveform. The converter is controlled to provide a relatively high voltage to start the lamp, and a lower voltage thereafter. When the ballast is powered by the ac utility, a low-harmonic rectifier typically provides the input dc voltage for the inverter.

A resonant dc-dc converter can be constructed by rectifying and filtering the ac output of a resonant inverter. Figure 19.4 illustrates a series-resonant dc-dc converter, in which the approximately sinusoidal resonant tank output current $i_R(t)$ is rectified by a diode bridge rectifier, and filtered by a large capacitor to supply a dc load having current I and voltage V . Again, by variation of the switching frequency f_s (closer to or further from the resonant frequency f_0), the magnitude of the tank current $i_R(t)$, and hence also the dc load current I , can be controlled. Resonant dc-dc converters based on series, parallel, LCC, and other resonant tank networks are well understood. These converters are employed when specialized application requirements justify their use. For example, they are commonly employed in high voltage dc power supplies [5,6], because the substantial leakage inductance and winding capacitance of high-voltage transformers leads unavoidably to a resonant tank network. The same principle can be employed to construct *resonant link* inverters or resonant link cycloconverters [7–9]; controllable switch networks are then employed on both sides of the resonant tank network.

Figure 19.5 illustrates another approach to resonant power conversion, in which resonant ele-

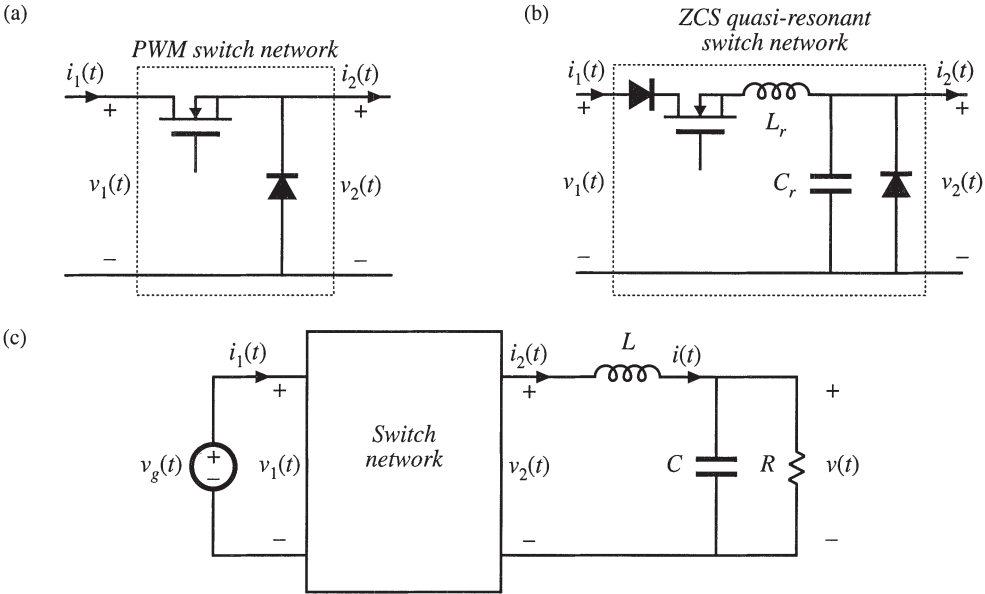


Fig. 19.5 Derivation of a quasi-resonant converter: (a) conventional PWM switch network, (b) a ZCS quasi-resonant switch network, (c) a quasi-resonant buck converter is obtained by employing a quasi-resonant switch network such as (b) in a buck converter.

ments are inserted into the switch network of an otherwise-PWM converter. A *resonant switch network*, or *quasi-resonant* converter, is then obtained. For example, in Fig. 19.5(b), resonant elements L_r and C_r are combined with the switch network transistor and diode. The resonant frequency of these elements is somewhat higher than the switching frequency. This causes the switch network waveforms $i_1(t)$ and $v_2(t)$ to become quasi-sinusoidal pulses. The resonant switch network of Fig. 19.5(b) can replace the PWM switch network of Fig. 19.5(a) in nearly any PWM converter. For example, insertion of the resonant switch network of Fig. 19.5(b) into the converter circuit of Fig. 19.5(c) leads to a quasi-resonant buck converter. Numerous resonant switch networks are known, which lead to a large number of resonant switch versions of buck, boost, buck–boost, and other converters. Quasi-resonant converters are described in Chapter 20.

The chief advantage of resonant converters is their reduced switching loss, via mechanisms known as *zero-current switching* (ZCS), and *zero-voltage switching* (ZVS). The turn-on and/or turn-off transitions of the various converter semiconductor elements can occur at zero crossings of the resonant converter quasi-sinusoidal waveforms. This eliminates some of the switching loss mechanisms described in Chapter 4. Hence, switching loss is reduced, and resonant converters can operate at switching frequencies that are higher than in comparable PWM converters. Zero-voltage switching can also eliminate some of the sources of converter-generated electromagnetic interference.

Resonant converters exhibit several disadvantages. Although the resonant element values can be chosen such that good performance with high efficiency is obtained at a single operating point, typically it is difficult to optimize the resonant elements such that good performance is obtained over a wide range of load currents and input voltages. Significant currents may circulate through the tank elements, even when the load is removed, leading to poor efficiency at light load. Also, the quasi-sinusoidal waveforms of resonant converters exhibit greater peak values than those exhibited by the rectangular waveforms of PWM converters, provided that the PWM current spikes due to diode stored charge are ignored. For

these reasons, resonant converters exhibit increased conduction losses, which can offset their reduced switching losses.

In this chapter, the properties of the series, parallel, and other resonant inverters and dc–dc converters are investigated using the *sinusoidal approximation* [3, 10–12]. Harmonics of the switching frequency are neglected, and the tank waveforms are assumed to be purely sinusoidal. This allows simple equivalent circuits to be derived for the bridge inverter, tank, rectifier, and output filter portions of the converter, whose operation can be understood and solved using standard linear ac analysis. This intuitive approach is quite accurate for operation in the continuous conduction mode with a high- Q response, but becomes less accurate when the tank is operated with a low Q -factor or for operation of dc–dc resonant converters in or near the discontinuous conduction mode.

For dc–dc resonant converters, the important result of this approach is that the dc voltage conversion ratio of a continuous conduction mode resonant converter is given approximately by the ac transfer function of the tank circuit, evaluated at the switching frequency. The tank is loaded by an effective output resistance, having a value nearly equal to the output voltage divided by the output current. It is thus quite easy to determine how the tank components and circuit connections affect the converter behavior. The influence of tank component losses, transformer nonidealities, etc., on the output voltage and converter efficiency can also be found. Several resonant network theorems are presented, which allow the load dependence of conduction loss and of the zero-voltage- or zero-current-switching properties to be explained in a simple and intuitive manner.

It is found that the series resonant converter operates with a step-down voltage conversion ratio. With a 1:1 transformer turns ratio, the dc output voltage is ideally equal to the dc input voltage when the transistor switching frequency is equal to the tank resonant frequency. The output voltage is reduced as the switching frequency is increased or decreased away from resonance. On the other hand, the parallel resonant converter is capable of both step-up and step-down of voltage levels, depending on the switching frequency and the effective tank Q -factor. The exact steady-state solutions of the ideal series and parallel resonant dc–dc converters are stated in Section 19.5.

Zero-voltage switching and zero-current switching mechanisms of the series resonant converter are described in Section 19.3. In Section 19.4, the dependence of resonant inverter properties on load is examined. A simple frequency-domain approach explains why some resonant converters, over certain ranges of operating points, exhibit large circulating tank currents and low efficiency. The boundaries of zero-voltage switching and zero-current switching are also determined.

It is also possible to modify the PWM converters of the previous chapters, so that zero-current or zero-voltage switching is obtained. A number of diverse approaches are known that lead to *soft switching* in buck, boost, forward, flyback, bridge, and other topologies. Chapter 20 summarizes some of the well-known schemes, including resonant switches, quasi-square wave switches, the full-bridge zero-voltage transition converter, and zero-voltage switching in forward and flyback converters containing active-clamp snubbers. A detailed description of soft-switching mechanisms of diodes, MOSFETs, and IGBTs is also given.

19.1 SINUSOIDAL ANALYSIS OF RESONANT CONVERTERS

Consider the class of resonant converters that contain a controlled switch network N_S that drives a linear resonant tank network N_T . In a resonant inverter, the tank network drives a resistive load as in Fig. 19.1. The reactive component of the load impedance, if any, can be effectively incorporated into the tank network. In the case of a resonant dc–dc converter, the resonant tank network is connected to an uncontrolled rectifier network N_R , filter network N_F and load R , as illustrated in Fig. 19.4. Many well-known converters can be represented in this form, including the series, parallel, and LCC topologies.

In the most common modes of operation, the controlled switch network produces a square wave voltage output $v_s(t)$ whose frequency f_s is close to the tank network resonant frequency f_0 . In response, the tank network rings with approximately sinusoidal waveforms of frequency f_s . In the case where the resonant tank responds primarily to the fundamental component f_s of the switch waveform $v_s(t)$, and has negligible response at the harmonic frequencies nf_s , $n = 3, 5, 7, \dots$, then the tank waveforms are well approximated by their fundamental components. As shown in Fig. 19.2, this is indeed the case when the tank network contains a high- Q resonance at or near the switching frequency, and a low-pass characteristic at higher frequencies. Hence, let us neglect harmonics, and compute the relationships between the fundamental components of the tank terminal waveforms $v_s(t)$, $i_s(t)$, $i_R(t)$, and $v_R(t)$.

19.1.1 Controlled Switch Network Model

If the switch network of Fig. 19.6 is controlled to produce a square wave of frequency $f_s = \omega_s/2\pi$ as in Fig. 19.7, then its output voltage waveform $v_s(t)$ can be expressed in the Fourier series

$$v_s(t) = \frac{4V_g}{\pi} \sum_{n=1,3,5,\dots} \frac{1}{n} \sin(n\omega_s t) \quad (19.1)$$

The fundamental component is

$$v_{s1}(t) = \frac{4V_g}{\pi} \sin(\omega_s t) = V_{s1} \sin(\omega_s t) \quad (19.2)$$

which has a peak amplitude of $(4/\pi)$ times the dc input voltage V_g , and is in phase with the original square wave $v_s(t)$. Hence, the switch network output terminal is modeled as a sinusoidal voltage generator, $v_{s1}(t)$.

It is also of interest to model the converter dc input port. This requires computation of the dc component I_g of the switch input current $i_g(t)$. The switch input current $i_g(t)$ is equal to the output current $i_s(t)$ when the switches are in position 1, and its inverse $-i_s(t)$ when the switches are in position 2. Under the conditions described above, the tank rings sinusoidally and $i_s(t)$ is well approximated by a sinusoid of some peak amplitude I_{s1} and phase ϕ_s :

$$i_s(t) \approx I_{s1} \sin(\omega_s t - \phi_s) \quad (19.3)$$

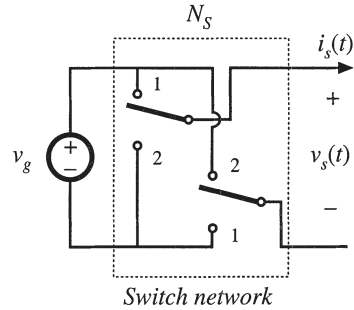


Fig. 19.6 An ideal switch network.

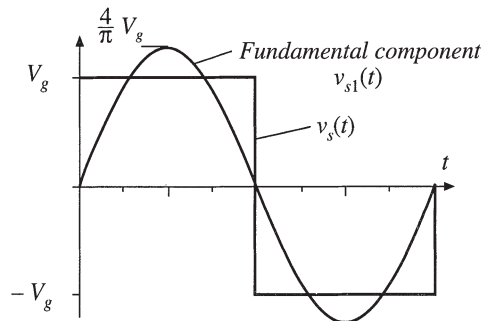


Fig. 19.7 Switch network output voltage $v_s(t)$ and its fundamental component $v_{s1}(t)$.

Fig. 19.8 Switch network waveforms $i_s(t)$ and $i_g(t)$.

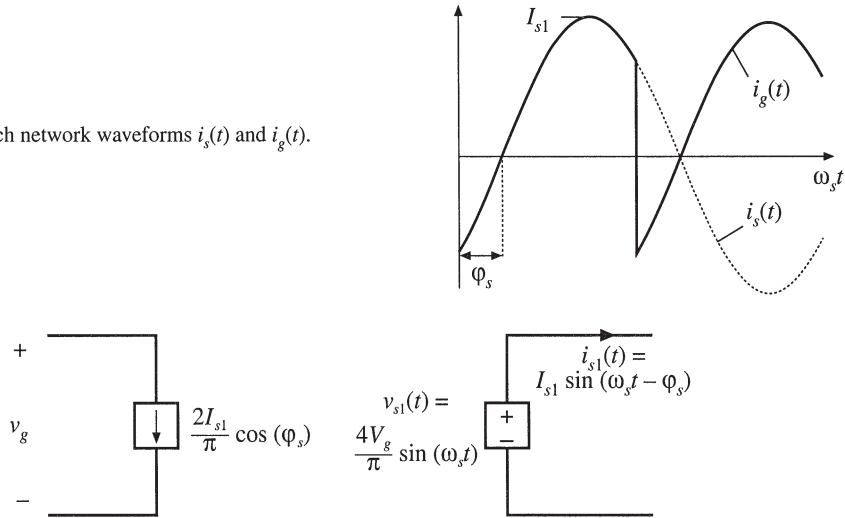


Fig. 19.9 An equivalent circuit for the switch network, which models the fundamental component of the output voltage waveform and the dc component of the input current waveform.

The input current waveform is shown in Fig. 19.8.

The dc component, or average value, of the input current can be found by averaging $i_g(t)$ over one half switching period:

$$\begin{aligned}
 \langle i_g(t) \rangle_{T_s} &= \frac{2}{T_s} \int_0^{T_s/2} i_g(\tau) d\tau \\
 &\approx \frac{2}{T_s} \int_0^{T_s/2} I_{s1} \sin(\omega_s \tau - \phi_s) d\tau \\
 &= \frac{2}{\pi} I_{s1} \cos(\phi_s)
 \end{aligned} \tag{19.4}$$

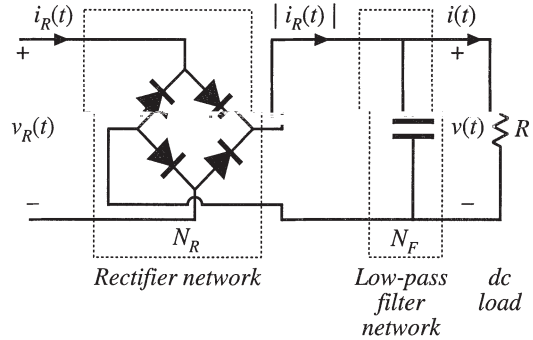
Thus, the dc component of the converter input current depends directly on the peak amplitude of the tank input current I_{s1} and on the cosine of its phase shift ϕ_s .

An equivalent circuit for the switch is given in Fig. 19.9. This circuit models the basic energy conversion properties of the switch: the dc power supplied by the voltage source V_g is converted into ac power at the switch output. Note that the dc power at the source is the product of V_g and the dc component of $i_g(t)$, and the ac power at the switch is the average of $v_s(t)i_s(t)$. Furthermore, if the harmonics of $v_s(t)$ are negligible, then the switch output voltage can be represented by its fundamental component, a sinusoid $v_{s1}(t)$ of peak amplitude $4V_g/\pi$. It can be verified that the switch network dc input power and fundamental average output power, predicted by Fig. 19.9, are equal.

19.1.2 Modeling the Rectifier and Capacitive Filter Networks

In the series resonant dc–dc converter, the output rectifier is driven by the nearly sinusoidal tank output current $i_R(t)$. A large capacitor C_F is placed at the dc output, so that the output voltage $v(t)$ contains negligible harmonics of the switching frequency f_s , as shown in Fig. 19.10. Hence, we can make the small-rip-

Fig. 19.10 Uncontrolled rectifier with capacitive filter network, as in the series resonant converter.



ple approximation as usual: $v(t) \approx V$, $i(t) \approx I$. The diode rectifiers switch when $i_R(t)$ passes through zero, as shown in Fig. 19.11. The rectifier input voltage $v_R(t)$ is essentially a square wave, equal to $+v(t)$ when $i_R(t)$ is positive and $-v(t)$ when $i_R(t)$ is negative. Note that $v_R(t)$ is in phase with $i_R(t)$.

If the tank output current $i_R(t)$ is a sinusoid with peak amplitude I_{R1} and phase shift φ_R :

$$i_R(t) = I_{R1} \sin(\omega_s t - \varphi_R) \quad (19.5)$$

then the rectifier input voltage may be expressed in the Fourier series

$$v_R(t) = \frac{4V}{\pi} \sum_{n=1,3,5,\dots}^{\infty} \frac{1}{n} \sin(n\omega_s t - \varphi_R) \quad (19.6)$$

where φ_R is the phase shift of $i_R(t)$, with respect to $v_s(t)$. This voltage waveform is impressed on the output port of the resonant tank network. Again, if the tank network responds primarily to the fundamental component (f_s) of $v_R(t)$, and has negligible response at the harmonic frequencies nf_s , $n = 3, 5, 7, \dots$, then the harmonics of $v_R(t)$ can be ignored. The voltage waveform $v_R(t)$ is then well approximated by its fundamental component $v_{R1}(t)$:

$$v_{R1}(t) = \frac{4V}{\pi} \sin(\omega_s t - \varphi_R) = V_{R1} \sin(\omega_s t - \varphi_R) \quad (19.7)$$

The fundamental voltage component $v_{R1}(t)$ has a peak value of $(4/\pi)$ times the dc output voltage V , and is in phase with the current $i_R(t)$.

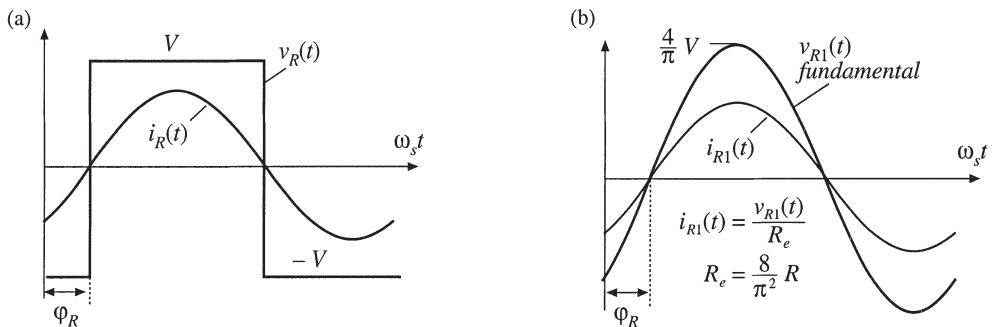
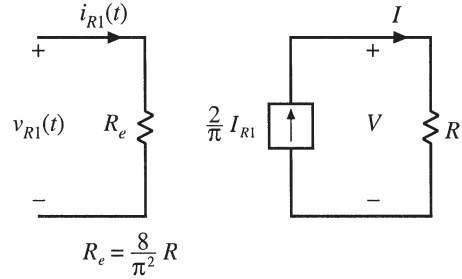


Fig. 19.11 Rectifier network input terminal waveforms: (a) actual waveforms $v_R(t)$ and $i_R(t)$, (b) fundamental components $v_{R1}(t)$ and $i_{R1}(t)$.

Fig. 19.12 An equivalent circuit for the rectifier and filter network, which models the fundamental components of the rectifier ac input waveforms and the dc components of the load waveforms. The rectifier presents an effective resistive load R_e to the tank network.



The rectified tank output current, $|i_R(t)|$, is filtered by capacitor C_F . Since no dc current can pass through C_F , the dc component of $|i_R(t)|$ must be equal to the steady-state load current I . By equating dc components we obtain:

$$\begin{aligned} I &= \frac{2}{T_S} \int_0^{T_S/2} I_{R1} |\sin(\omega_s t - \phi_R)| dt \\ &= \frac{2}{\pi} I_{R1} \end{aligned} \quad (19.8)$$

Therefore, the load current and the tank output current amplitudes are directly related in steady state.

Since $v_{R1}(t)$, the fundamental component of $v_R(t)$, is in phase with $i_R(t)$, the rectifier presents an effective resistive load R_e to the tank circuit. The value of R_e is equal to the ratio of $v_{R1}(t)$ to $i_R(t)$. Division of Eq. (19.7) by Eq. (19.5), and elimination of I_{R1} using Eq. (19.8) yields

$$R_e = \frac{v_{R1}(t)}{i_R(t)} = \frac{8}{\pi^2} \frac{V}{I} \quad (19.9)$$

With a resistive load R equal to V/I , this equation reduces to

$$R_e = \frac{8}{\pi^2} R = 0.8106R \quad (19.10)$$

Thus, the tank network is damped by an effective load resistance R_e equal to 81% of the actual load resistance R . An equivalent circuit that models the rectifier network input port fundamental components and output port dc components is given in Fig. 19.12.

19.1.3 Resonant Tank Network

We have postulated that the effects of harmonics can be neglected, and we have consequently shown that the bridge can be modeled as a fundamental voltage source $v_{s1}(t)$. In the case of a dc-dc converter, the rectifier can be modeled using an effective resistor of value R_e . We can now solve the resonant tank network by standard linear analysis.

As shown in Fig. 19.13, the tank circuit is a linear network with the following voltage transfer function:

$$\frac{v_{R1}(s)}{v_{s1}(s)} = H(s) \quad (19.11)$$

Hence, the ratio V_{R1}/V_{s1} of the peak magnitudes of $v_{R1}(t)$ and $v_{s1}(t)$ is given by:

$$\frac{V_{R1}}{V_{s1}} = \|H(s)\|_{s=j\omega_s} \quad (19.12)$$

In addition, $i_R(s)$ is given by:

$$i_R(s) = \frac{v_{R1}(s)}{R_e} = \frac{H(s)}{R_e} v_{s1}(s) \quad (19.13)$$

So the peak magnitude of $i_R(t)$ is:

$$I_{R1} = \frac{\|H(s)\|_{s=j\omega_s}}{R_e} V_{s1} \quad (19.14)$$

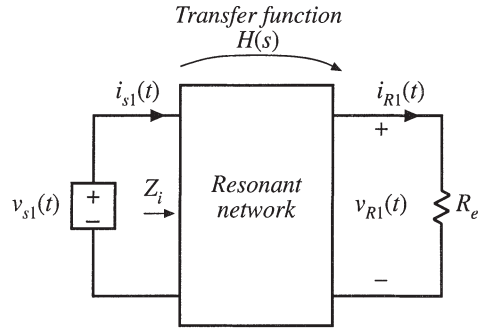


Fig. 19.13 The linear tank network, excited by an effective sinusoidal input source and driving an effective resistive load.

Thus, the magnitude of the tank transfer function is found, with an effective resistive load.

19.1.4 Solution of Converter Voltage Conversion Ratio $M = V/V_g$

An equivalent circuit of a complete dc–dc resonant converter is depicted in Fig. 19.14. The voltage conversion ratio of the resonant converter can now be found:

$$M = \frac{V}{V_g} = \underbrace{\left(R\right)}_{\left(\frac{V}{I}\right)} \underbrace{\left(\frac{2}{\pi}\right)}_{\left(\frac{I}{I_{R1}}\right)} \underbrace{\left(\frac{1}{R_e}\right)}_{\left(\frac{I_{R1}}{V_{R1}}\right)} \underbrace{\left(\|H(s)\|_{s=j\omega_s}\right)}_{\left(\frac{V_{R1}}{V_{s1}}\right)} \underbrace{\left(\frac{4}{\pi}\right)}_{\left(\frac{V_{s1}}{V_g}\right)} \quad (19.15)$$

Simplification by use of Eq. (19.10) yields:

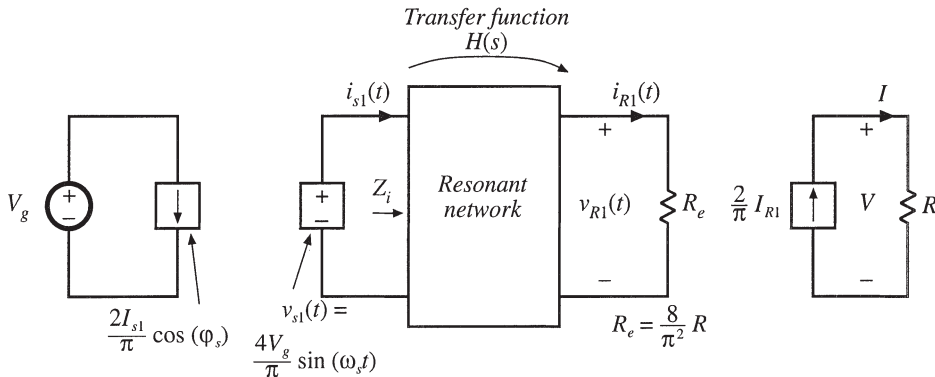


Fig. 19.14 Steady-state equivalent circuit that models the dc and fundamental components of resonant converter waveforms.

$$\frac{V}{V_g} = \left\| H(s) \right\|_{s=j\omega_s} \quad (19.16)$$

Equation (19.16) is the desired result. It states that the dc conversion ratio of the resonant converter is approximately the same as the ac transfer function of the resonant tank circuit, evaluated at the switching frequency f_s . This intuitive result can be applied to converters with many different types of tank circuits. However, it should be reemphasized that Eq. (19.16) is valid only if the response of the tank circuit to the harmonics of $v_s(t)$ is negligible compared to the fundamental response, an assumption that is not always justified. In addition, we have assumed that the switch network is controlled to produce a square wave and that the rectifier network drives a capacitive-type filter network. Finally, the transfer function $H(s)$ is evaluated using the effective load resistance R_e given by Eq. (19.9).

19.2 EXAMPLES

19.2.1 Series Resonant DC–DC Converter Example

The series resonant converter with switching frequency control is shown in Fig. 19.4. Current-bidirectional two-quadrant switches are necessary. For this circuit, the tank network consists of a series L – C circuit, and Fig. 19.14 can be redrawn as in Fig. 19.15. The transfer function $H(s)$ is therefore:

$$\begin{aligned} H(s) &= \frac{R_e}{Z_i(s)} = \frac{R_e}{R_e + sL + \frac{1}{sC}} \\ &= \frac{\left(\frac{s}{Q_e \omega_0} \right)}{1 + \left(\frac{s}{Q_e \omega_0} \right) + \left(\frac{s}{\omega_0} \right)^2} \end{aligned} \quad (19.17)$$

where

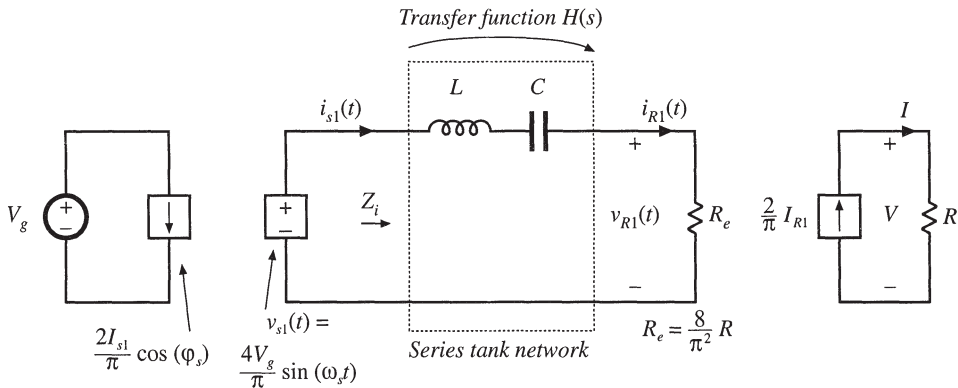


Fig. 19.15 Steady-state equivalent circuit of the series resonant converter.

$$\begin{aligned}\omega_0 &= \frac{1}{\sqrt{LC}} = 2\pi f_0 \\ R_0 &= \sqrt{\frac{L}{C}} \\ Q_e &= \frac{R_0}{R_e}\end{aligned}$$

The magnitude of $H(j\omega_s)$, which coincides with the converter dc conversion ratio $M = V/V_g$, is

$$M = \|H(j\omega_s)\| = \frac{1}{\sqrt{1 + Q_e^2 \left(\frac{1}{F} - F\right)^2}} \quad (19.18)$$

where

$$F = f_s/f_0 \quad (19.19)$$

The Bode diagrams of $Z_i(s)$ and $H(s)$ are constructed in Fig. 19.16, using the graphical construction method of Chapter 8. The series resonant impedance $Z_i(s)$ is dominated by the capacitor C at low frequency, and by the inductor L at high frequency. At the resonant frequency f_0 , the impedances of the inductor and capacitor are equal in magnitude and opposite in phase; hence, they cancel. The series resonant impedance $Z_i(s)$ is equal to R_e at $f = f_0$.

The transfer function $\|H(j\omega)\|$ is constructed graphically, by division of R_e by the $\|Z_i\|$ asymptotes of Fig. 19.16. At resonance, one obtains $\|H\| = R_e/R_e = 1$. At frequencies above or below the resonant frequency, $\|Z_i\| > R_e$ and hence $\|H\| < 1$. So the conversion ratio M is less than or equal to 1. It can also be seen that a decrease in the load resistance R , which increases the effective quality factor Q_e , causes a more peaked response in the vicinity of resonance. Exact characteristics of the series resonant converter are plotted in Fig. 19.45.

Over what range of switching frequencies is Eq. (19.18) accurate? The response of the tank to the fundamental component of $v_s(t)$ must be sufficiently greater than the response to the harmonics of $v_s(t)$. This is certainly true for operation above resonance because $H(s)$ contains a bandpass characteristic that decreases with a single pole slope for $f_s > f_0$. For the same reason, Eq. (19.18) is valid when the switching frequency is below but near resonance.

However, for switching frequencies f_s much less than the resonant frequency f_0 , the sinusoidal approximation breaks down completely because the tank responds more strongly to the harmonics of

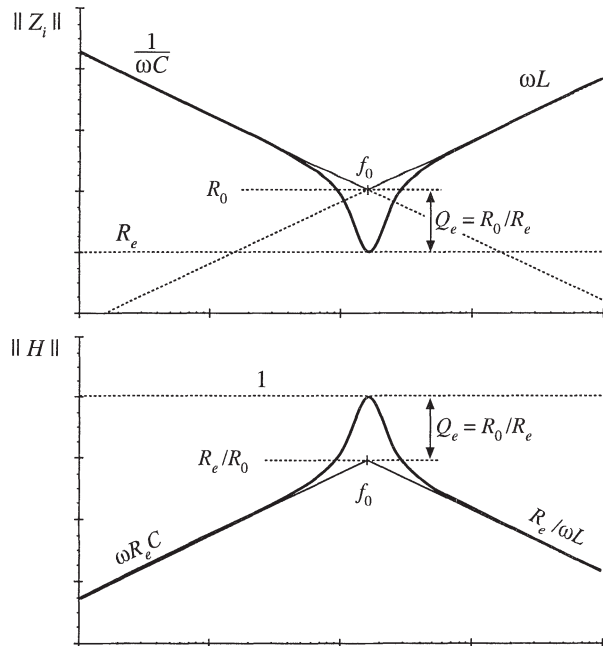
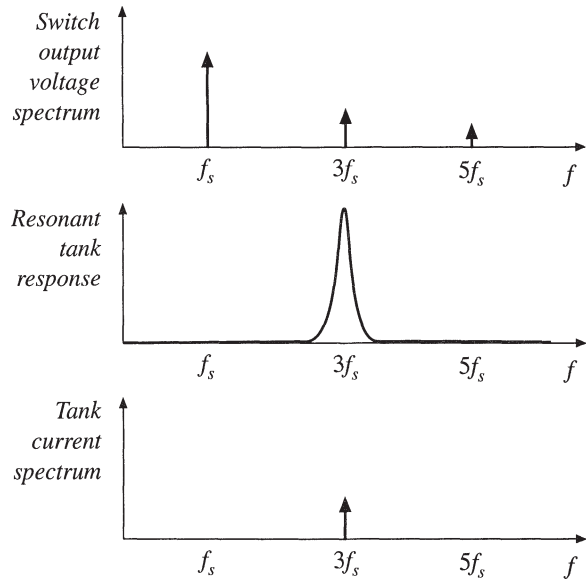


Fig. 19.16 Construction of the Bode diagrams of $Z_i(s)$ and $H(s)$ for the series resonant converter.

Fig. 19.17 Excitation of the tank network by the third harmonic of the switching frequency.



$v_s(t)$ than to its fundamental. For example, at $f_s = f_0/3$, the third harmonic of $v_s(t)$ is equal to f_0 and directly excites the tank resonance. Some other type of analysis must be used to understand what happens at these lower frequencies. Also, in the low- Q case, the approximation is less accurate because the filter response is less peaked, and hence does not favor the fundamental component as strongly. As shown in a later section, discontinuous conduction modes may then occur whose waveforms are highly nonsinusoidal.

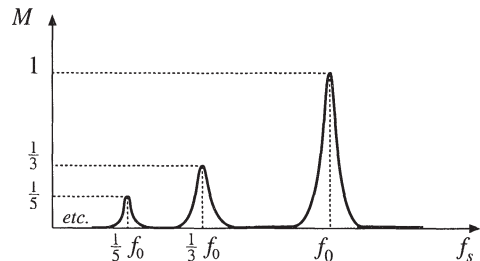
19.2.2 Subharmonic Modes of the Series Resonant Converter

If the n^{th} harmonic of the switch output waveform $v_s(t)$ is close to the resonant tank frequency, $nf_s \sim f_0$, and if the tank effective quality factor Q_e is sufficiently large, then as illustrated in Fig. 19.17, the tank responds primarily to harmonic n . All other components of the tank waveforms can then be neglected, and it is a good approximation to replace $v_s(t)$ with its n^{th} harmonic component:

$$v_s(t) \approx v_{sn}(t) = \frac{4V_g}{n\pi} \sin(n\omega_s t) \quad (19.20)$$

This expression differs from Eq. (19.2) because the amplitude is reduced by a factor of $1/n$, and the fre-

Fig. 19.18 The subharmonic modes of the series resonant converter. These modes occur when the harmonics of the switching frequency excite the tank resonance.



quency is nf_s rather than f_s .

The arguments used to model the tank and rectifier/filter networks are unchanged from Section 19.1. The rectifier presents an effective resistive load to the tank, of value $R_e = 8R/\pi^2$. In consequence, the converter dc conversion ratio is given by

$$M = \frac{V}{V_g} = \frac{\|H(jn\omega_s)\|}{n} \quad (19.21)$$

This is a good approximation provided that nf_s is close to f_0 , and that Q_e is sufficiently large. Typical characteristics are sketched in Fig. 19.18.

The series resonant converter is not generally designed to operate in a subharmonic mode, since the fundamental modes yield greater output voltage and power, and hence higher efficiency. Nonetheless, the system designer should be aware of their existence, because inadvertent operation in these modes can lead to large signal instabilities.

19.2.3 Parallel Resonant DC–DC Converter Example

The parallel resonant dc–dc converter is diagrammed in Fig. 19.19. It differs from the series resonant converter in two ways. First, the tank capacitor appears in parallel with the rectifier network rather than in series: this causes the tank transfer function $H(s)$ to have a different form. Second, the rectifier drives an inductive-input low-pass filter. In consequence, the value of the effective resistance R_e differs from that of the rectifier with a capacitive filter. Nonetheless, sinusoidal approximations can be used to understand the operation of the parallel resonant converter.

As in the series resonant converter, the switch network is controlled to produce a square wave $v_s(t)$. If the tank network responds primarily to the fundamental component of $v_s(t)$, then arguments identical to those of Section 19.1 can be used to model the output fundamental components and input dc components of the switch waveforms. The resulting equivalent circuit is identical to Fig. 19.9.

The uncontrolled rectifier with inductive filter network can be described using the dual of the arguments of Section 19.1.2. In the parallel resonant converter, the output rectifiers are driven by the nearly sinusoidal tank capacitor voltage $v_R(t)$, and the diode rectifiers switch when $v_R(t)$ passes through zero as in Fig. 19.20. If the filter inductor current ripple is small, then in steady-state the filter inductor current is essentially equal to the dc load current I . The rectifier input current $i_R(t)$ is therefore a square wave of amplitude I , and is in phase with the tank capacitor voltage $v_R(t)$:

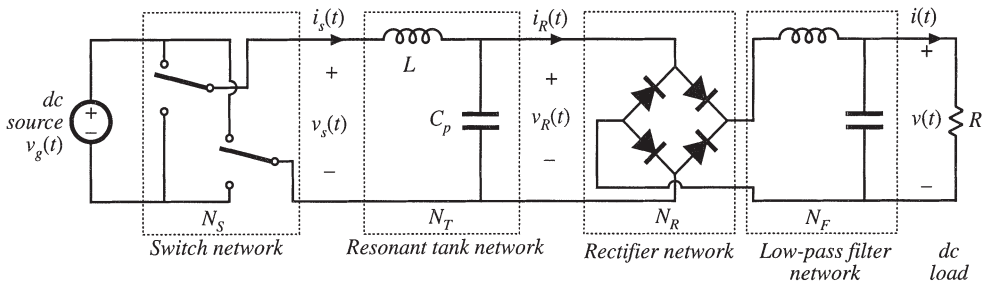


Fig. 19.19 Block diagram of the parallel resonant converter.

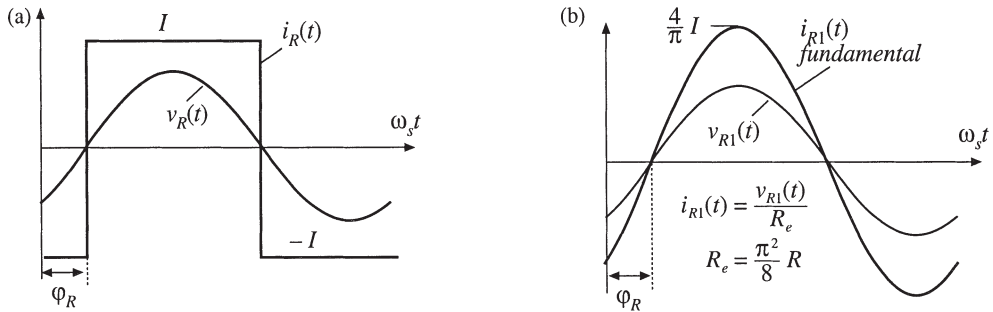


Fig. 19.20 Rectifier network input terminal waveforms, for the parallel resonant converter: (a) actual waveforms $v_R(t)$ and $i_R(t)$, (b) fundamental components $v_{R1}(t)$ and $i_{R1}(t)$.

$$i_R(t) = \frac{4I}{\pi} \sum_{n=1,3,5,\dots}^{\infty} \frac{1}{n} \sin(n\omega_s t - \phi_R) \quad (19.22)$$

where ϕ_R is the phase shift of $v_R(t)$.

The fundamental component of $i_R(t)$ is

$$i_{R1}(t) = \frac{4I}{\pi} \sin(\omega_s t - \phi_R) \quad (19.23)$$

Hence, the rectifier again presents an effective resistive load to the tank circuit, equal to

$$R_e = \frac{v_{R1}(t)}{i_{R1}(t)} = \frac{\pi V_{R1}}{4I} \quad (19.24)$$

The ac components of the rectified tank capacitor voltage $|v_R(t)|$ are removed by the output low pass filter. In steady state, the output voltage V is equal to the dc component of $|v_R(t)|$:

$$V = \frac{2}{T_S} \int_0^{T_S/2} V_{R1} |\sin(\omega_s t - \phi_R)| dt = \frac{2}{\pi} V_{R1} \quad (19.25)$$

So the load voltage V and the tank capacitor voltage amplitude are directly related in steady state. Substitution of Eq. (19.25) and resistive load characteristics $V = IR$ into Eq. (19.24) yields:

$$R_e = \frac{\pi^2}{8} R = 1.2337R \quad (19.26)$$

An equivalent circuit for the uncontrolled rectifier with inductive filter network is given in Fig. 19.21. This model is similar to the one used for the series resonant converter, Fig. 19.12, except that the roles of the rectifier input voltage $v_R(t)$ and current $i_R(t)$ are interchanged, and the effective resistance R_e has a different value. The model for the complete converter is given in Fig. 19.22.

Solution of Fig. 19.22 yields the converter dc conversion ratio:

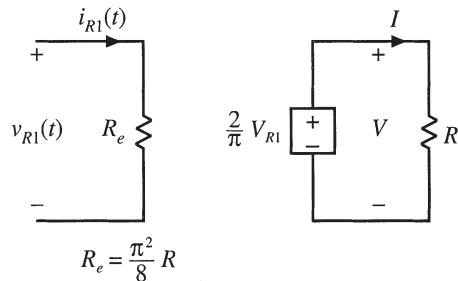


Fig. 19.21 An equivalent circuit for the rectifier and inductive filter network of the parallel resonant converter, which models the fundamental components of the rectifier ac input waveforms and the dc components of the load waveforms.

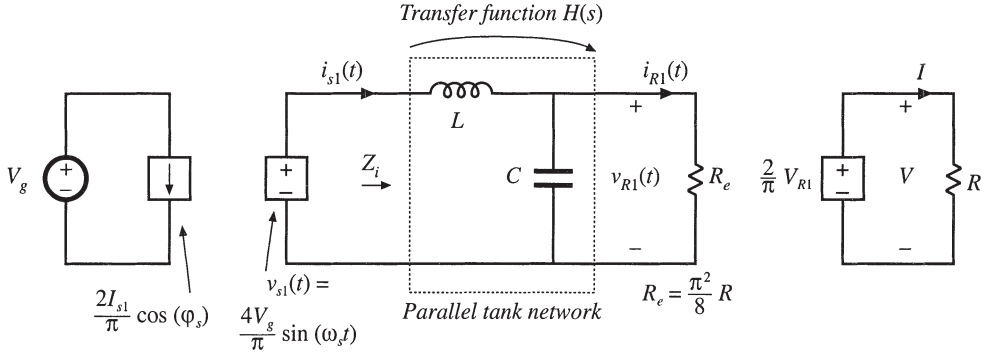


Fig. 19.22 Equivalent circuit for the parallel resonant converter, which models the fundamental components of the tank waveforms, and the dc components of the converter input current and output voltage.

$$M = \frac{V}{V_g} = \frac{8}{\pi^2} \|H(s)\|_{s=j\omega_s} \quad (19.27)$$

where $H(s)$ is the tank transfer function

$$H(s) = \frac{Z_o(s)}{sL} \quad (19.28)$$

and

$$Z_o(s) = sL \parallel \frac{1}{sC} \parallel R_e \quad (19.29)$$

The Bode magnitude diagrams of $H(s)$ and $Z_o(s)$ are constructed in Fig. 19.23, using the graphical construction method of Chapter 8. The impedance $Z_o(s)$ is the parallel combination of the impedances of the tank inductor L , capacitor C , and effective load R_e . The magnitude asymptote of the parallel combination of these components, at a given frequency, is equal to the smallest of the individual asymptotes ωL , $1/\omega C$, and R_e . Hence, at low frequency where the inductor impedance dominates the parallel combination, $\|Z_o(s)\| \approx \omega L$, while at high frequency the capacitor dominates and $\|Z_o(s)\| \approx 1/\omega C$. At resonance, the impedances of the inductor and capacitor are equal in magnitude but opposite in phase, so that their effects cancel. The impedance $\|Z_o(s)\|$ is then equal to R_e :

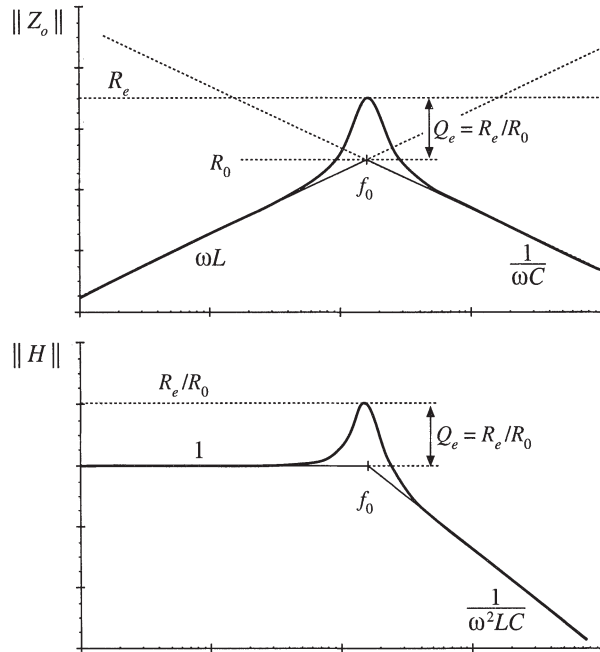
$$\|Z_o(s)\|_{s=j\omega_s} = \frac{1}{\frac{1}{j\omega_0 L} + j\omega_0 C + \frac{1}{R_e}} = R_e \quad (19.30)$$

with

$$\omega_0 L = \frac{1}{\omega_0 C} = R_0$$

The dc conversion ratio is therefore

Fig. 19.23 Construction of Bode diagrams of $Z_i(s)$ and $H(s)$ for the parallel resonant converter.



$$\begin{aligned}
 M &= \frac{8}{\pi^2} \left\| \frac{Z_o(s)}{sL} \right\|_{s=j\omega_s} = \frac{8}{\pi^2} \left\| \frac{1}{1 + \frac{s}{Q_e\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \right\|_{s=j\omega_s} \\
 &= \frac{8}{\pi^2} \frac{1}{\sqrt{(1-F^2)^2 + \left(\frac{F}{Q_e}\right)^2}}
 \end{aligned} \quad (19.31)$$

where $F = f_s/f_0$.

At resonance, the conversion ratio is

$$M = \frac{8}{\pi^2} \frac{R_e}{R_0} = \frac{R}{R_0} \quad (19.32)$$

The actual peak value of M occurs at a switching frequency slightly below the resonant frequency, with peak M slightly greater than Eq. (19.32). Provided that the load resistance R is greater than the tank characteristic impedance R_e , the parallel resonant converter can produce conversion ratios both greater than and less than one. In fact, the ideal parallel resonant converter can produce conversion ratios approaching infinity, provided that the output current is limited to values less than V_g/R_0 . Of course, losses limit the maximum output voltage that can be produced by practical converters.

19.3 SOFT SWITCHING

As mentioned previously, the soft-switching phenomena known as zero-current switching (ZCS) and zero-voltage switching (ZVS) can lead to reduced switching loss. When the turn-on and/or turn-off tran-

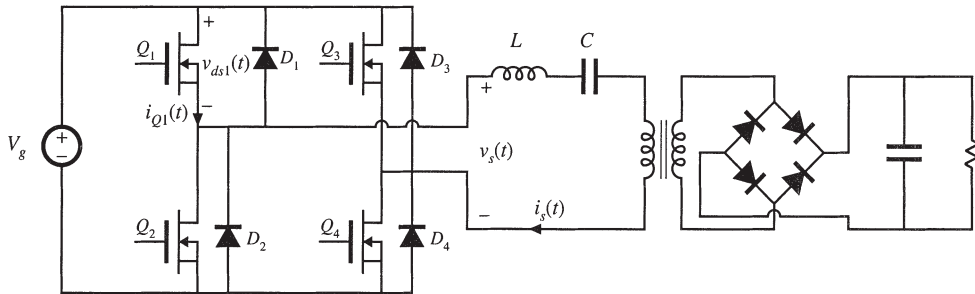


Fig. 19.24 A series resonant converter incorporating a full-bridge switch network.

sitions of a semiconductor switching device coincide with the zero crossings of the applied waveforms, some of the switching loss mechanisms discussed in Section 4.3 are eliminated. In converters containing MOSFETs and diodes, zero-voltage switching mitigates the switching loss otherwise caused by diode recovered charge and semiconductor output capacitance. Zero-current switching can mitigate the switching loss caused by current tailing in IGBTs and by stray inductances. Zero-current switching can also be used for commutation of SCRs. In the majority of applications, where diode recovered charge and semiconductor output capacitances are the dominant sources of PWM switching loss, zero-voltage switching is preferred.

19.3.1 Operation of the Full Bridge Below Resonance: Zero-Current Switching

When the series and parallel resonant inverters and dc-dc converters are operated below resonance, the zero-current switching phenomenon can occur, in which the circuit causes the transistor current to go to zero before the transistor is turned off. Let us consider the operation of the full bridge switch network of the series resonant converter in detail.

A full bridge circuit, realized using power MOSFETs and antiparallel diodes, is shown in Fig. 19.24. The switch output voltage $v_s(t)$, and its fundamental component $v_{s1}(t)$, as well as the approximately sinusoidal tank current waveform $i_s(t)$, are illustrated in Fig. 19.25. At frequencies less than the tank resonant frequency, the input impedance of the series resonant tank network $Z_i(s)$ is dominated by the tank capacitor impedance [see Fig. 19.16(a)]. Hence, the tank presents an effective capacitive load to the bridge, and switch current $i_s(t)$ leads the switch voltage fundamental component $v_{s1}(t)$, as shown in Fig. 19.25. In consequence, the zero crossing of the current waveform $i_s(t)$ occurs before the zero crossing of the voltage $v_s(t)$.

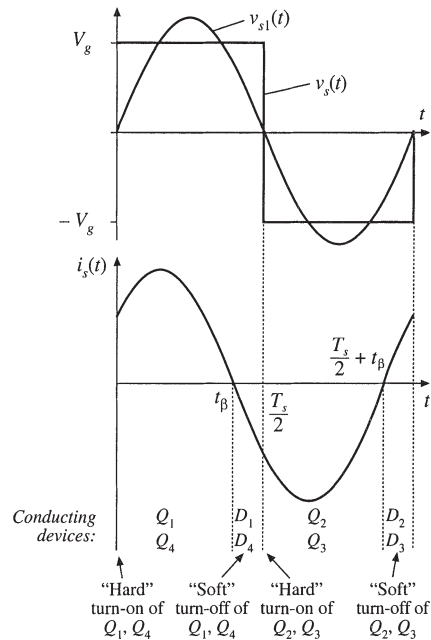
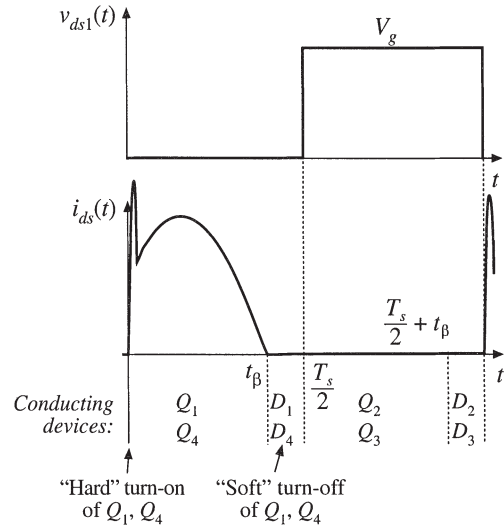


Fig. 19.25 Switch network output waveforms for the series resonant converter, operated below resonance in the $k = 1$ CCM. Zero-current switching aids the transistor turn-off process.

Fig. 19.26 Transistor Q_1 voltage and current waveforms, for operation of the series resonant converter below resonance in the $k = 1$ CCM.



For the half cycle $0 < t < T_s/2$, the switch voltage v_s is equal to $+V_g$. For $0 < t < t_\beta$, the current $i_s(t)$ is positive and transistors Q_1 and Q_4 conduct. Diodes D_1 and D_4 conduct when $i_s(t)$ is negative, over the interval $t_\beta < t < T_s/2$. The situation during $T_s/2 < t < T_s$ is symmetrical. Since $i_{s1}(t)$ leads $v_{s1}(t)$, the transistors conduct before their respective antiparallel diodes. Note that, at any given time during the D_1 conduction interval $t_\beta < t < T_s/2$, transistor Q_1 can be turned off without incurring switching loss. The circuit naturally causes the transistor turn-off transition to be lossless, and long turn-off switching times can be tolerated.

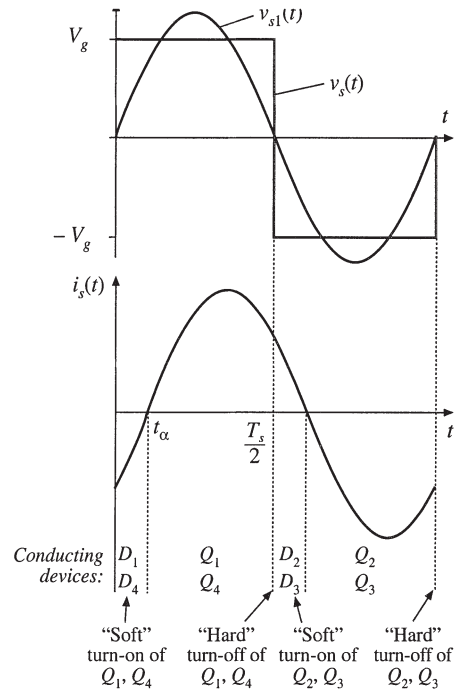
In general, zero current switching can occur when the resonant tank presents an effective capacitive load to the switches, so that the switch current zero crossings occur before the switch voltage zero crossings. In the bridge configuration, zero current switching is characterized by the half-bridge conduction sequence $Q_1-D_1-Q_2-D_2$, such that the transistors are turned off while their respective antiparallel diodes conduct. It is possible, if desired, to replace the transistors with naturally commutated thyristors whenever the zero-current-switching property occurs at the turn-off transition.

The transistor turn-on transition in Fig. 19.26 is similar to that of a PWM switch: it is hard-switched and is not lossless. During the turn-on transition of Q_1 , diode D_2 must turn off. Neither the transistor current nor the transistor voltage is zero, Q_1 passes through a period of high instantaneous power dissipation, and switching loss occurs. As in the PWM case, the reverse recovery current of diode D_2 flows through Q_1 . This current spike can be the largest component of switching loss. In addition, the energy stored in the drain-to-source capacitances of Q_1 and Q_2 and in the depletion layer capacitance of D_1 is lost when Q_1 turns on. These turn-on transition switching loss mechanisms can be a major disadvantage of zero-current-switching schemes. Since zero-current switching does not address the switching loss mechanisms that dominate in MOSFET converters, improvements in efficiency are typically not observed.

19.3.2 Operation of the Full Bridge Above Resonance: Zero-Voltage Switching

When the series resonant converter is operated above resonance, the zero-voltage switching phenomenon can occur, in which the circuit causes the transistor voltage to become zero before the controller turns the

Fig. 19.27 Switch network output waveforms for the series resonant converter, operated above resonance in the continuous conduction mode. Zero-voltage switching aids the transistor turn-on process.



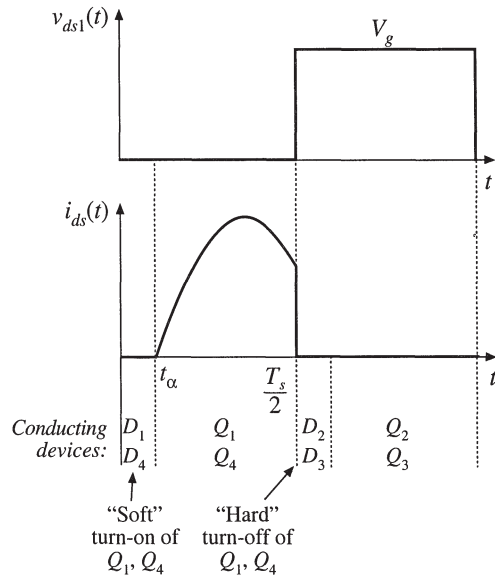
transistor on. With a minor circuit modification, the transistor turn-off transitions can also be caused to occur at zero voltage. This process can lead to significant reductions in the switching losses of converters based on MOSFETs and diodes.

For the full bridge circuit of Fig. 19.24, the switch output voltage $v_s(t)$, and its fundamental component $v_{s1}(t)$, as well as the approximately sinusoidal tank current waveform $i_s(t)$, are plotted in Fig. 19.27. At frequencies greater than the tank resonant frequency, the input impedance of the tank network $Z_i(s)$ is dominated by the tank inductor impedance. Hence, the tank presents an effective inductive load to the bridge, and the switch current $i_s(t)$ lags the switch voltage fundamental component $v_{s1}(t)$, as shown in Fig. 19.27. In consequence, the zero crossing of the voltage waveform $v_s(t)$ occurs before the current waveform $i_s(t)$.

For the half cycle $0 < t < T_s/2$, the switch voltage $v_s(t)$ is equal to $+V_g$. For $0 < t < t_\alpha$, the current $i_s(t)$ is negative and diodes D_1 and D_4 conduct. Transistors Q_1 and Q_4 conduct when $i_s(t)$ is positive, over the interval $t_\alpha < t < T_s/2$. The waveforms during $T_s/2 < t < T_s$ are symmetrical. Since the zero crossing of $v_s(t)$ leads the zero crossing of $i_s(t)$, the transistors conduct after their respective antiparallel diodes. Note that, at any given time during the D_1 conduction interval $0 < t < t_\alpha$, transistor Q_1 can be turned on without incurring switching loss. The circuit naturally causes the transistor turn-on transition to be lossless, and long turn-on switching times can be tolerated. A particularly significant implication of this is that the switching loss associated with reverse recovery of the antiparallel diodes is avoided. Relatively slow diodes, such as the MOSFET body diodes, can be employed for realization of diodes D_1 to D_4 . In addition, the output capacitances of transistors Q_1 to Q_4 and diodes D_1 to D_4 do not lead to switching loss.

In general, zero-voltage switching can occur when the resonant tank presents an effective inductive load to the switches, and hence the switch voltage zero crossings occur before the switch current zero crossings. In the bridge configuration, zero-voltage switching is characterized by the half-bridge conduction sequence D_1 – Q_1 – D_2 – Q_2 , such that the transistors are turned on while their respective antipar-

Fig. 19.28 Transistor Q_1 voltage and current waveforms, for operation of the series resonant converter above resonance in the $k = 0$ CCM.



allel diodes conduct. Since the transistor voltage is zero during the entire turn on transition, switching loss due to slow turn-on times or due to energy storage in any of the device capacitances does not occur at turn-on.

The transistor turn-off transition in Fig. 19.28 is similar to that of a PWM switch. In converters that employ IGBTs or other minority-carrier devices, significant switching loss may occur at the turn-off transitions. The current tailing phenomenon causes Q_1 to pass through a period of high instantaneous power dissipation, and switching loss occurs.

To assist the transistor turn off process, small capacitors C_{leg} may be introduced into the legs of the bridge, as demonstrated in Fig. 19.29. In a converter employing MOSFETs, the device output capacitances are sufficient for this purpose, with no need for external discrete capacitors. A delay is also introduced into the gate drive signals, so that there is a short commutation interval when all four transistors are off. During the normal Q_1 , D_1 , Q_2 , and D_2 conduction intervals, the leg capacitors appear in parallel with the semiconductor switches, and have no effect on the converter operation. However, these capacitors introduce commutation intervals at transistor turn-off. When Q_1 is turned off, the tank current $i_s(T_s/2)$ flows through the switch capacitances C_{leg} instead of Q_1 , and the voltage across Q_1 and C_{leg} increases. Eventually, the voltage across Q_1 reaches V_g ; diode D_2 then becomes forward-biased. If the MOSFET turn-off time is sufficiently fast, then the MOSFET is switched fully off before the drain voltage rises significantly above zero, and negligible turn-off switching loss is incurred. The energy stored in the device capacitances, that is, in C_{leg} , is transferred to the tank inductor. The fact that none of the semiconductor device capacitances or stored charges lead to switching loss is the major advantage of zero-voltage switching, and is the most common motivation for its use. MOSFET converters can typically be operated in this manner, using only the internal drain-to-source capacitances. However, other devices such as IGBTs typically require substantial external capacitances to reduce the losses incurred during the IGBT turn-off transitions.

An additional advantage of zero-voltage switching is the reduction of EMI associated with device capacitances. In conventional PWM converters and also, to some extent, in zero-current switching converters, significant high-frequency ringing and current spikes are generated by the rapid charging and discharging of the semiconductor device capacitances during the turn-on and/or turn-off transitions.

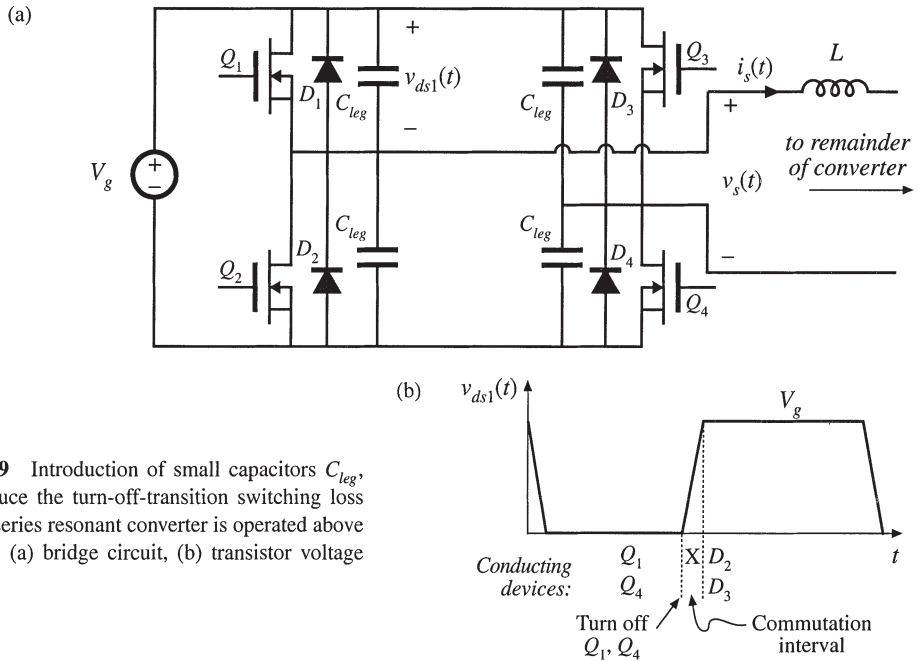


Fig. 19.29 Introduction of small capacitors C_{leg} , which reduce the turn-off-transition switching loss when the series resonant converter is operated above resonance: (a) bridge circuit, (b) transistor voltage waveform.

Ringing is conspicuously absent from the waveforms of converters in which all semiconductor devices switch at zero voltage; these converters inherently do not generate this type of EMI.

19.4 LOAD-DEPENDENT PROPERTIES OF RESONANT CONVERTERS

The properties of the CCM PWM converters studied in previous chapters are largely unaffected by the load current. In consequence, these converters exhibit several desirable properties that are often taken for granted. The transistor current is proportional to the load current; hence conduction losses become small at light load, leading to good light-load efficiency. Also, the output impedance is low, and hence the dc output voltage does not significantly depend on the load i - v characteristic (at least, in CCM). Unfortunately, these good properties are not necessarily shared by resonant converters. Of central importance in design of a resonant converter is the selection of the resonant tank topology and element values, so that the transistor conduction losses at light load are minimized, so that zero-voltage switching is obtained over a wide range of load currents (preferably, for all anticipated loads, but at least at full and intermediate load powers), and so that the converter dynamic range is compatible with the load i - v characteristic. These design issues are addressed in this section.

The conduction loss caused by circulating tank currents is well-recognized as a problem in resonant converter design. These currents are independent of, or only weakly dependent on, the load current, and lead to poor efficiency at light load. In Fig. 19.30, the switch current $i_s(s)$ is equal to $v_s(s)/Z_i(s)$. If we want the switch current to track the load current, then at the switching frequency $\|Z_i\|$ should be dominated by, or at least strongly influenced by, the load resistance R . Unfortunately, this is often not consistent with the requirement for zero-voltage switching, in which Z_i is dominated by a tank inductor.

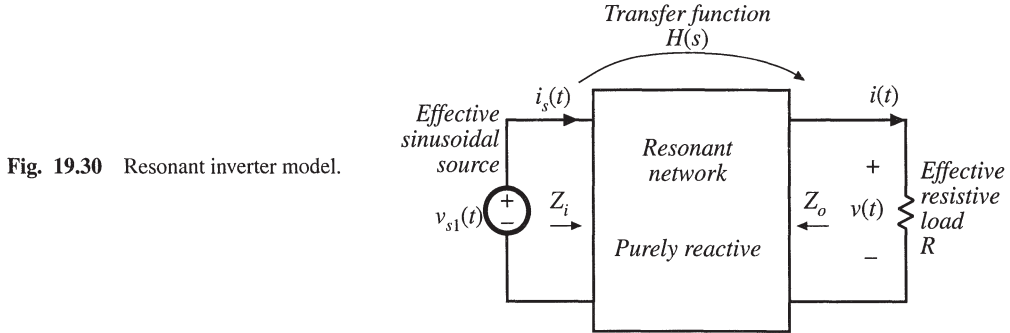


Fig. 19.30 Resonant inverter model.

To design a resonant converter that exhibits good properties, the engineer must develop physical insight into how the load resistance R affects the tank input impedance and output voltage.

In this section, the inverter output characteristics, zero-voltage switching boundary, and the dependence of transistor current on load resistance, are related to the properties of the tank network under the extreme conditions of an open-circuited or short-circuited load. The undamped tank network responses are easily plotted, and the insight needed to optimize the tank network design can be gained quickly.

19.4.1 Inverter Output Characteristics

Let us first investigate how the magnitude of the inverter output voltage $\|v\|$ depends on the load current magnitude $\|i\|$. Consider the resonant inverter system of Fig. 19.30. Let $H_\infty(s)$ be the open-circuit ($R \rightarrow \infty$) transfer function of the tank network:

$$H_\infty(s) = \left. \frac{v(s)}{v_{s1}(s)} \right|_{R \rightarrow \infty} \quad (19.33)$$

and let $Z_{o0}(s)$ be the output impedance, determined when the source $v_{s1}(s)$ is short-circuited. Then we can model the output port of the tank network using the Thevenin-equivalent circuit of Fig. 19.31. Solution of this circuit using the voltage divider formula leads to

$$v(s) = H_\infty(s) v_{s1}(s) \frac{R}{R + Z_{o0}(s)} \quad (19.34)$$

At a given angular switching frequency $\omega_s = 2\pi f_s$, the phasor representing the magnitude and phase of the ac output voltage is found by letting $s = j\omega_s$:

$$v(j\omega_s) = H_\infty(j\omega_s) v_{s1}(j\omega_s) \frac{R}{R + Z_{o0}(j\omega_s)} \quad (19.35)$$

The magnitude can be found by noting that

$$\|v(j\omega_s)\|^2 = v(j\omega_s) v^*(j\omega_s) \quad (19.36)$$

where $v^*(j\omega_s)$ is the complex conjugate of $v(j\omega_s)$. Substitution of Eq. (19.35) into Eq. (19.36) leads to

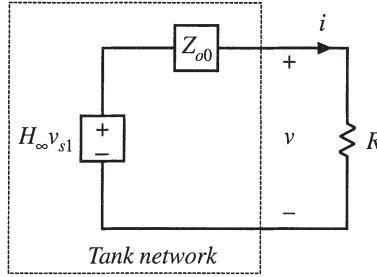


Fig. 19.31 Thevenin-equivalent circuit that models the output port of the tank network.

$$\begin{aligned}
 \|v(j\omega_s)\|^2 &= \left(H_\infty(j\omega_s) v_{s1}(j\omega_s) \frac{R}{R + Z_{o0}(j\omega_s)} \right) \left(H_\infty(j\omega_s) v_{s1}(j\omega_s) \frac{R}{R + Z_{o0}(j\omega_s)} \right)^* \\
 &= H_\infty(j\omega_s) H_\infty^*(j\omega_s) v_{s1}(j\omega_s) v_{s1}^*(j\omega_s) \frac{R^2}{(R + Z_{o0}(j\omega_s))(R + Z_{o0}(j\omega_s))^*} \\
 &= \|H_\infty(j\omega_s)\|^2 \|v_{s1}(j\omega_s)\|^2 \frac{R^2}{(R + Z_{o0}(j\omega_s))(R + Z_{o0}(j\omega_s))^*}
 \end{aligned} \tag{19.37}$$

This result can be further simplified with the assumption that the tank network contains only purely reactive elements, i.e., that any losses or other resistive elements within the tank network have negligible effect. Then the output impedance $Z_{o0}(j\omega_s)$, as well as all other driving-point impedances of the tank network, are purely imaginary quantities. This implies that the complex conjugate $Z_{o0}^*(j\omega_s)$ is given by

$$Z_{o0}^*(j\omega_s) = -Z_{o0}(j\omega_s) \tag{19.38}$$

Substitution of Eq. (19.38) into Eq. (19.37) and simplification leads to

$$\|v(j\omega_s)\|^2 = \frac{\|H_\infty(j\omega_s)\|^2 \|v_s(j\omega_s)\|^2}{\left(1 + \frac{\|Z_{o0}(j\omega_s)\|^2}{R^2}\right)} \tag{19.39}$$

with

$$R = \frac{\|v(j\omega_s)\|}{\|i(j\omega_s)\|} \tag{19.40}$$

Substitution of Eq. (19.40) into Eq. (19.39) and rearrangement of terms yields

$$\|v(j\omega_s)\|^2 + \|i(j\omega_s)\|^2 \|Z_{o0}(j\omega_s)\|^2 = \|H_\infty(j\omega_s)\|^2 \|v_s(j\omega_s)\|^2 \tag{19.41}$$

Hence, at a given frequency, the inverter output characteristic, that is, the relationship between $\|v(j\omega_s)\|$ and $\|i(j\omega_s)\|$, is elliptical. Equation (19.41) can be further rearranged, into the form

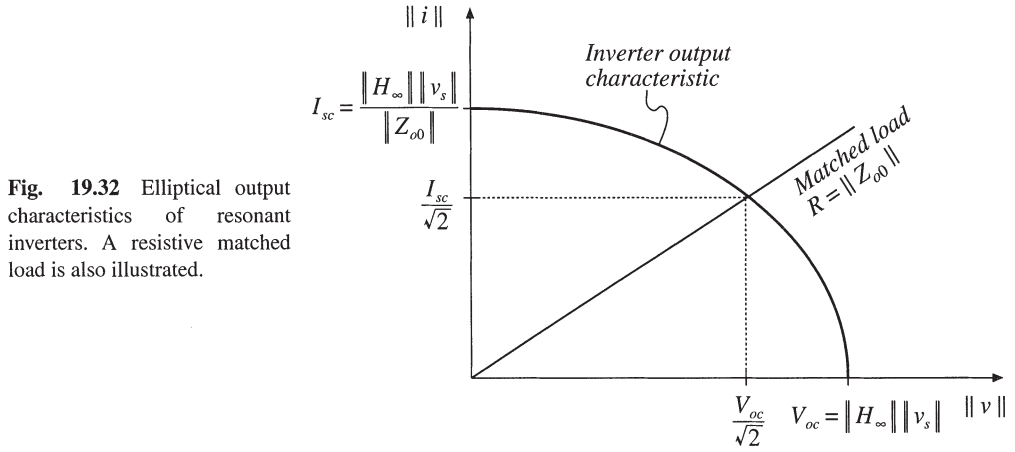


Fig. 19.32 Elliptical output characteristics of resonant inverters. A resistive matched load is also illustrated.

$$\frac{\|v(j\omega_s)\|^2}{V_{oc}^2} + \frac{\|i(j\omega_s)\|^2}{I_{sc}^2} = 1 \quad (19.42)$$

where the open-circuit voltage V_{oc} and short-circuit current I_{sc} are given by

$$\begin{aligned} V_{oc} &= \|H_{\infty}(j\omega_s)\| \|v_s(j\omega_s)\| \\ I_{sc} &= \frac{\|H_{\infty}(j\omega_s)\| \|v_s(j\omega_s)\|}{\|Z_{o0}(j\omega_s)\|} = \frac{V_{oc}}{\|Z_{o0}(j\omega_s)\|} \end{aligned} \quad (19.43)$$

These inverter output characteristics are constructed in Fig. 19.32. This characteristic describes how, at a given switching frequency, the ac output voltage magnitude varies as the circuit is loaded. The equilibrium output voltage is given by the intersection of this elliptical characteristic with the load i - v characteristic. For example, Fig. 19.32 also illustrates a superimposed resistive load line having slope $1/R$, in the special case where $R = \|Z_{o0}(j\omega_s)\|$. This value of R corresponds to matched load operation, in which the converter output power is maximized. It can be shown that the operating point is then given by

$$\begin{aligned} \|v(j\omega_s)\|^2 &= \frac{V_{oc}^2}{2} \\ \|i(j\omega_s)\|^2 &= \frac{I_{sc}^2}{2} \end{aligned} \quad (19.44)$$

Note that Fig. 19.32 can also be applied to the output i - v characteristics of resonant dc-dc converters, since the output rectifier then loads the tank with an effective resistive load R_e .

19.4.2 Dependence of Transistor Current on Load

The transistors must conduct the current appearing at the input port of the tank network, $i_s(t)$. This current is determined by the tank network input impedance $Z_i(j\omega_s)$:

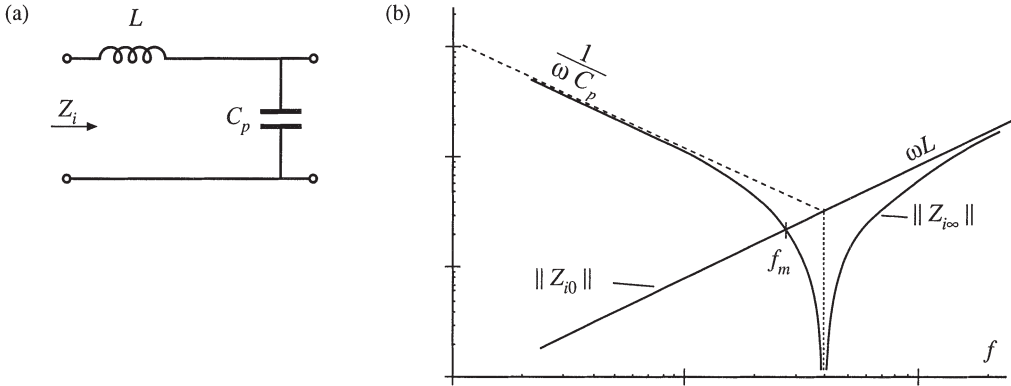


Fig. 19.33 Tank network, parallel resonant converter example: (a) tank circuit, (b) Bode plot of input impedance magnitude $\|Z_i\|$ for the limiting cases $R \rightarrow 0$ and $R \rightarrow \infty$.

$$i_{s1}(j\omega_s) = \frac{v_{s1}(j\omega_s)}{Z_i(j\omega_s)} \quad (19.45)$$

As described previously, obtaining good light-load efficiency requires that $\|Z_i(j\omega_s)\|$ increase as the load resistance R increases. To understand how $\|Z_i(j\omega_s)\|$ depends on R , let us sketch $\|Z_i(j\omega_s)\|$ in the extreme cases of an open-circuited ($R \rightarrow \infty$) and short-circuited ($R \rightarrow 0$) load:

$$\begin{aligned} Z_{i0}(j\omega_s) &= Z_i(j\omega_s) \Big|_{R \rightarrow 0} \\ Z_{i\infty}(j\omega_s) &= Z_i(j\omega_s) \Big|_{R \rightarrow \infty} \end{aligned} \quad (19.46)$$

For example, consider the parallel resonant converter of Figs. 19.19 to 19.23. The Bode diagrams of the impedances $\|Z_{i0}(j\omega_s)\|$ and $\|Z_{i\infty}(j\omega_s)\|$ are constructed in Fig. 19.33. $Z_{i0}(s)$ is found with the load R shorted, and is equal to the inductor impedance sL . $Z_{i\infty}(s)$, found with the load R open-circuited, is given by the series combination $(sL + 1/sC)$. It can be seen in Fig. 19.33 that the impedance magnitudes $\|Z_{i0}(j\omega_s)\|$ and $\|Z_{i\infty}(j\omega_s)\|$ intersect at frequency f_m . If the switching frequency is chosen such that $f_s < f_m$, then $\|Z_{i\infty}(j\omega_s)\| > \|Z_{i0}(j\omega_s)\|$. The converter then exhibits the desirable characteristic that the no-load switch current magnitude $\|v_s(j\omega_s)\| / \|Z_{i\infty}(j\omega_s)\|$ is smaller than the switch current under short-circuit conditions, $\|v_s(j\omega_s)\| / \|Z_{i0}(j\omega_s)\|$. In fact, the short-circuit switch current is limited by the impedance of the tank inductor, while the open-circuit switch current is determined primarily by the impedance of the tank capacitor.

If the switching frequency is chosen such that $f_s > f_m$, then $\|Z_{i\infty}(j\omega_s)\| < \|Z_{i0}(j\omega_s)\|$. The no-load switch current is then greater in magnitude than the switch current when the load is short-circuited! When the load current is reduced or removed, the transistors will continue to conduct large currents and generate high conduction losses. This causes the efficiency at light load to be poor. It can be concluded that, to obtain good light-load efficiency in the parallel resonant converter, one should choose f_s sufficiently less than f_m . Unfortunately, this requires operation below resonance, leading to reduced output voltage dynamic range and a tendency to lose the zero-voltage switching property.

A remaining question is how $\|Z_i(j\omega_s)\|$ behaves for intermediate values of load between the open-circuit and short-circuit conditions. The answer is given by Theorem 1 below: $\|Z_i(j\omega_s)\|$ varies monotonically with R , and therefore is bounded by $\|Z_{i0}(j\omega_s)\|$ and $\|Z_{i\infty}(j\omega_s)\|$. Hence, the Bode plots of

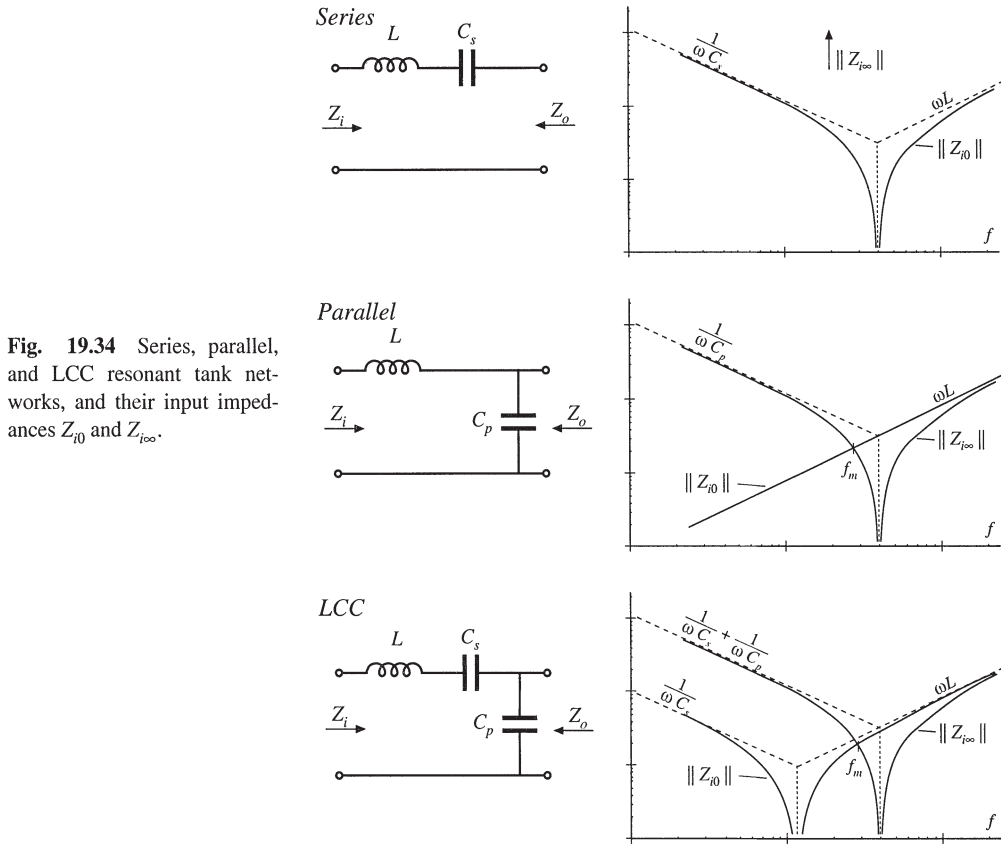


Fig. 19.34 Series, parallel, and LCC resonant tank networks, and their input impedances Z_{i0} and $Z_{i\infty}$.

the limiting cases $\|Z_{i0}(j\omega_s)\|$ and $\|Z_{i\infty}(j\omega_s)\|$ provide a correct qualitative understanding of the behavior of $\|Z_i\|$ for all R . The theorem is valid for lossless tank networks.

Theorem 1: If the tank network is purely reactive, then its input impedance $\|Z_i\|$ is a monotonic function of the load resistance R .

This theorem is proven by use of Middlebrook's Extra Element Theorem (see Appendix C). The tank network input impedance $Z_i(s)$ can be expressed as a function of the load resistance R and the tank network driving-point impedances, as follows:

$$Z_i(s) = Z_{i0}(s) \frac{\left(1 + \frac{R}{Z_{o0}(s)}\right)}{\left(1 + \frac{R}{Z_{o\infty}(s)}\right)} = Z_{i\infty}(s) \frac{\left(1 + \frac{Z_{o0}(s)}{R}\right)}{\left(1 + \frac{Z_{o\infty}(s)}{R}\right)} \quad (19.47)$$

where Z_{i0} and $Z_{i\infty}$ are the resonant network input impedances, with the load short-circuited or open-circuited, respectively, and Z_{o0} and $Z_{o\infty}$ are the resonant network output impedances, with the source input short-circuited or open-circuited, respectively. These terminal impedances are simple functions of the tank elements, and their Bode diagrams are easily constructed. The input impedances of the series reso-

nant, parallel resonant, and LCC inverters are listed in Fig. 19.34. Since these impedances do not depend on the load, they are purely reactive, ideally have zero real parts [38], and their complex conjugates are given by $Z_{o0}^* = -Z_{o0}$, $Z_{o\infty}^* = -Z_{o\infty}$, etc. Again, recall that the magnitude of a complex impedance $Z(j\omega)$ can be expressed as the square root of $Z(j\omega)Z^*(j\omega)$. Hence, the magnitude of $Z_i(s)$ is given by

$$\begin{aligned}\|Z_i\|^2 &= Z_i Z_i^* = Z_{i0}(s) Z_{i0}^*(s) \frac{\left(1 + \frac{R}{Z_{o0}(s)}\right) \left(1 + \frac{R}{Z_{o0}^*(s)}\right)}{\left(1 + \frac{R}{Z_{o\infty}(s)}\right) \left(1 + \frac{R}{Z_{o\infty}^*(s)}\right)} \\ &= \|Z_{i0}\|^2 \frac{\left(1 + \frac{R^2}{\|Z_{o0}\|^2}\right)}{\left(1 + \frac{R^2}{\|Z_{o\infty}\|^2}\right)}\end{aligned}\quad (19.48)$$

where Z_i^* is the complex conjugate of Z_i .

Next, let us differentiate Eq. (19.48) with respect to R :

$$\frac{d\|Z_i\|^2}{dR} = 2R \|Z_{i0}\|^2 \frac{\left(\frac{1}{\|Z_{o0}\|^2} - \frac{1}{\|Z_{o\infty}\|^2}\right)}{\left(1 + \frac{R^2}{\|Z_{o\infty}\|^2}\right)^2}\quad (19.49)$$

The derivative has roots at (i) $R = 0$, (ii) $R = \infty$, and in the special case (iii) where $\|Z_{i0}\| = \|Z_{i\infty}\|$. Since the derivative is otherwise nonzero, the resonant network input impedance $\|Z_i\|$ is a monotonic function of R , over the range $0 < R < \infty$. In special case (iii), $\|Z_i\|$ is independent of R . Therefore, Theorem 1 is proved.

An example is given in Figs. 19.36 and 19.35, for the LCC inverter. Figure 19.35 illustrates the impedance asymptotes of the limiting cases $\|Z_{i0}\|$ and $\|Z_{i\infty}\|$. Variation of $\|Z_i\|$ between these limits, for finite nonzero R , is illustrated in Fig. 19.36. The open-circuit resonant frequency f_∞ and the short-circuit resonant frequency f_0 are given by

$$\begin{aligned}f_0 &= \frac{1}{2\pi\sqrt{LC_s}} \\ f_\infty &= \frac{1}{2\pi\sqrt{L C_s \| C_p}}\end{aligned}\quad (19.50)$$

where $C_s \| C_p$ denotes inverse addition of C_s and C_p :

$$C_s \| C_p = \frac{1}{\frac{1}{C_s} + \frac{1}{C_p}}\quad (19.51)$$

For the LCC inverter, the impedance magnitudes $\|Z_{i0}\|$ and $\|Z_{i\infty}\|$ are equal at frequency f_m , given by

$$f_m = \frac{1}{2\pi\sqrt{L C_s \| 2C_p}}\quad (19.52)$$

Fig. 19.35 Construction of the quantities $\|Z_{i0}\|$ and $\|Z_{i\infty}\|$, for the LCC inverter.

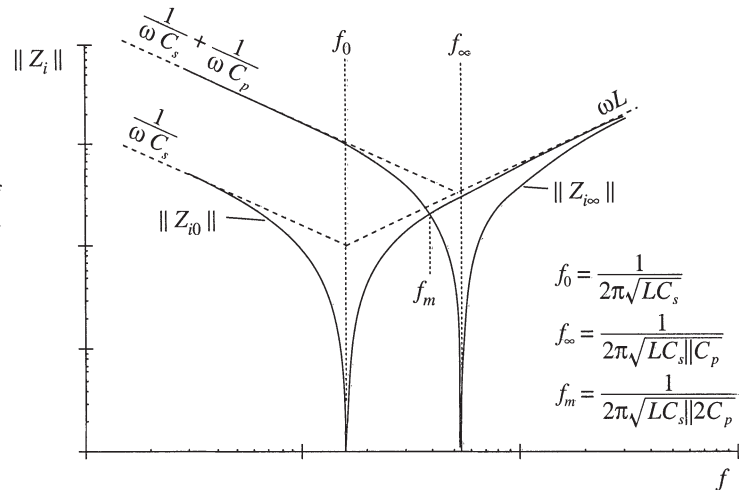
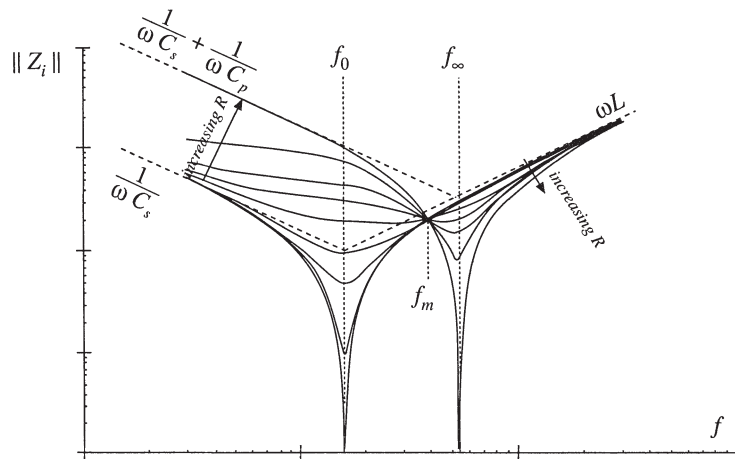


Fig. 19.36 Variation of tank network input impedance $\|Z_i\|$ with load resistance R , LCC inverter. As the load resistance is increased, $\|Z_i\|$ changes monotonically from $\|Z_{i0}\|$ to $\|Z_{i\infty}\|$.



If the switching frequency is chosen to be greater than f_m , then $\|Z_{i\infty}\|$ is less than $\|Z_{i0}\|$. This implies that, as the load current is decreased, the transistor current will increase. Such a converter will have poor efficiency at light load, and will exhibit significant circulating currents. If the switching frequency is chosen to be less than f_m , then the transistor current will increase with decrease with decreasing load current. The short-circuit current is limited by $\|Z_{i0}\|$, while the circulating currents under open-circuit conditions are determined by $\|Z_{i\infty}\|$. In general, if $f > f_m$, then the transistor current is greater than or equal to the short-circuit current for all R . The inequality is reversed when $f < f_m$.

The impedance magnitudes $\|Z_{i0}\|$ and $\|Z_{i\infty}\|$ are illustrated in Fig. 19.34 for the series, parallel, and LCC tank networks. In the case of the series tank network, $\|Z_{i\infty}\| = \infty$. In consequence, the no-load transistor current is zero, both above resonance and below resonance. Hence, the series resonant inverter exhibits the desirable property that the transistor current is proportional to the load current. In addition, when the load is short-circuited, the current magnitude is limited by the impedance of the series resonant tank. For the parallel and LCC inverters, it is desirable to operate below the frequency f_m .

Thus, the dependence of the transistor current on load can be easily determined, using an intuitive frequency-domain approach.

19.4.3 Dependence of the ZVS/ZCS Boundary on Load Resistance

It is also necessary to determine the critical load resistance $R = R_{crit}$ at the boundary between ZVS and ZCS. This boundary can also be expressed as a function of the impedances Z_{i0} and $Z_{i\infty}$.

As discussed in Section 19.3, zero-voltage switching occurs when the switch current $i_s(t)$ lags the switch voltage $v_s(t)$. Zero-current switching occurs when $i_s(t)$ leads $v_s(t)$. This definition ignores the effects of semiconductor output capacitances, and hence gives an approximate ZVS/ZCS boundary. The phase between the switch current and switch voltage is again determined by the input impedance of the tank network:

$$i_{s1}(j\omega_s) = \frac{v_{s1}(j\omega_s)}{Z_i(j\omega_s)} \quad (19.53)$$

Hence, zero-voltage switching occurs when $Z_i(j\omega_s)$ is inductive in nature, zero-current switching occurs when $Z_i(j\omega_s)$ is capacitive in nature, and the ZVS/ZCS boundary occurs where $Z_i(j\omega_s)$ has zero phase.

It is instructive to again consider the limiting cases of a short-circuited and open-circuited load. The Bode plots of $Z_{i0}(j\omega_s)$ and $Z_{i\infty}(j\omega_s)$ for an LCC inverter example are sketched in Fig. 19.37. Since, in these limiting cases, the input impedance Z_i is composed only of the reactive tank elements, $Z_{i0}(j\omega_s)$ and $Z_{i\infty}(j\omega_s)$ are purely imaginary quantities having phase of either -90° or $+90^\circ$. For $f_s < f_0$, both $Z_{i0}(j\omega_s)$ and $Z_{i\infty}(j\omega_s)$ are dominated by the tank capacitor or capacitors; the phase of $Z_i(j\omega_s)$ is therefore -90° . Hence, zero-current switching is obtained under both short-circuit and open-circuit conditions. For $f_s > f_\infty$, both $Z_{i0}(j\omega_s)$ and $Z_{i\infty}(j\omega_s)$ are dominated by the tank inductor; hence the phase of $Z_i(j\omega_s)$ is $+90^\circ$. Zero-voltage switching is obtained for both a short-circuited and an open-circuited load. For $f_0 < f_s < f_\infty$, $Z_{i0}(j\omega_s)$ is dominated by the tank inductor while $Z_{i\infty}(j\omega_s)$ is dominated by the tank capacitors. This implies that zero-voltage switching is obtained under short-circuit conditions, and zero-voltage switching is obtained under open-circuit conditions. For this case, there must be some critical value of load resistance $R = R_{crit}$ that represents the boundary between ZVS and ZCS, and that causes the phase of $Z_i(j\omega_s)$ to be equal to 0° .

The behavior of $Z_i(j\omega_s)$ for nonzero finite R is easily extrapolated from the limiting cases dis-

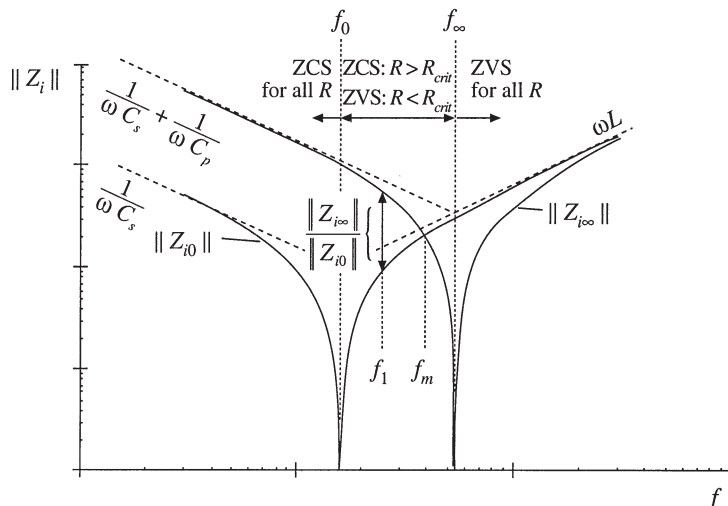


Fig. 19.37 Use of the input impedance quantities Z_{i0} and $Z_{i\infty}$ to determine the ZCS/ZVS boundaries, LCC example.

cussed above. Theorem 2 below shows that:

1. If zero-current switching occurs for both an open-circuited load and a short-circuited load [i.e., $Z_{i0}(j\omega_s)$ and $Z_{i\infty}(j\omega_s)$ both have phase $+90^\circ$], then zero-current switching occurs for all loads.
2. If zero-voltage switching occurs for both an open-circuited load and a short-circuited load [i.e., $Z_{i0}(j\omega_s)$ and $Z_{i\infty}(j\omega_s)$ both have phase -90°], then zero-voltage switching occurs for all loads.
3. If zero-voltage switching occurs for an open-circuited load and zero-current switching occurs for a short-circuited load [i.e., $Z_{i0}(j\omega_s)$ has phase -90° and $Z_{i\infty}(j\omega_s)$ has phase $+90^\circ$], then zero-voltage switching occurs for $R > R_{crit}$, and zero-current switching occurs for $R < R_{crit}$, with R_{crit} given by Eq. (19.54) below.
4. If zero-current switching occurs for an open-circuited load and zero-voltage switching occurs for a short-circuited load [i.e., $Z_{i0}(j\omega_s)$ has phase $+90^\circ$ and $Z_{i\infty}(j\omega_s)$ has phase -90°], then zero-current switching occurs for $R > R_{crit}$, and zero-voltage switching occurs for $R < R_{crit}$, with R_{crit} given by Eq. (19.54) below.

For the LCC example, we can therefore conclude that, for $f_s < f_0$, zero-current switching occurs for all values of R . For $f_s > f_\infty$, zero-voltage switching occurs for all values of R . For $f_0 < f_s < f_\infty$, the boundary between ZVS and ZCS is given by Eq. (19.54).

Theorem 2: If the tank network is purely reactive, then the boundary between zero-current switching and zero-voltage switching occurs when the load resistance R is equal to the critical value R_{crit} , given by

$$R_{crit} = \|Z_{o0}\| \sqrt{\frac{-Z_{i\infty}}{Z_{i0}}} \quad (19.54)$$

This theorem relies on the assumption that zero-current switching occurs when the tank input impedance is capacitive in nature, while zero-voltage switching occurs for inductive input impedances. The boundary therefore occurs where the phase of $Z_i(j\omega)$ is zero. This definition gives a necessary but not sufficient condition for zero-voltage switching when significant semiconductor output capacitance is present.

The result is derived by finding the value of R which causes the imaginary part of $Z_i(j\omega)$ in Eq. (19.47) to be zero. Since the tank network is assumed to ideal and lossless, the impedances $Z_{o\infty}$, Z_{o0} , and $Z_{i\infty}$ must have zero real parts. Hence,

$$\text{Im}(Z_i(R_{crit})) = \text{Im}(Z_{i\infty}) \text{Re} \left(\frac{1 + \frac{Z_{o0}}{R_{crit}}}{1 + \frac{Z_{o\infty}}{R_{crit}}} \right) = \text{Im}(Z_{i\infty}) \left(\frac{1 - \frac{Z_{o0}Z_{o\infty}}{R_{crit}^2}}{1 + \frac{\|Z_{o\infty}\|^2}{R_{crit}^2}} \right) = 0 \quad (19.55)$$

where $\text{Im}(Z)$ and $\text{Re}(Z)$ denote the imaginary and real parts of the complex quantity Z . The nontrivial solution to Eq. (19.55) is given by

$$1 = \frac{Z_{o0}Z_{o\infty}}{R_{crit}^2} \quad (19.56)$$

hence,

$$R_{crit} = \sqrt{Z_{o0}Z_{o\infty}} \quad (19.57)$$

A useful equivalent form makes use of the reciprocity identities

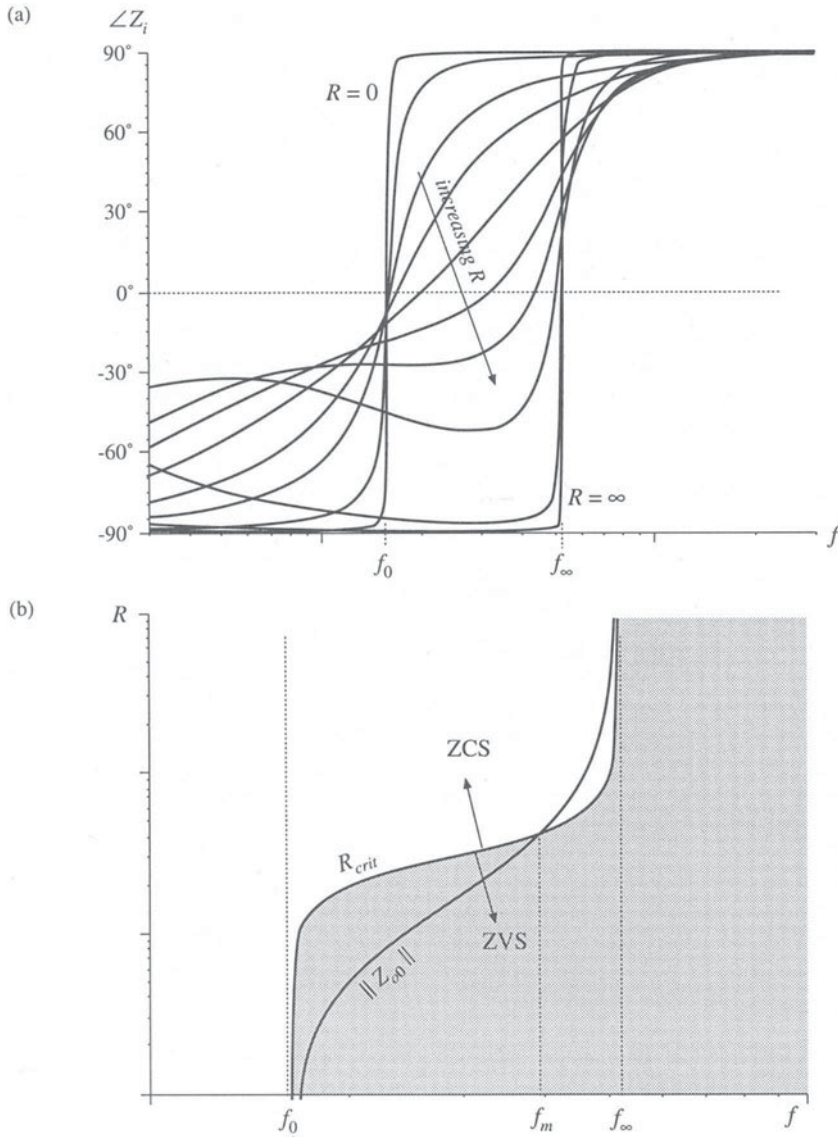


Fig. 19.38 ZCS/ZVS boundary, LCC inverter example: (a) variation of tank network input impedance phase shift with load resistance, (b) Comparison of R_{crit} with matched-load impedance $\parallel Z_{o0} \parallel$.

$$\frac{Z_{o0}}{Z_{o\infty}} = \frac{Z_{r0}}{Z_{r\infty}} \quad (19.58)$$

Use of Eq. (19.58) to eliminate $Z_{o\infty}$ from Eq. (19.57) leads to

$$R_{crit} = \|Z_{o0}\| \sqrt{\frac{-Z_{i\infty}}{Z_{i0}}} \quad (19.59)$$

This is the desired result. The quantity Z_{o0} is the inverter output impedance, and $R = \|Z_{o0}\|$ corresponds to operation at matched load with maximum output power. The impedances $Z_{i\infty}$ and Z_{i0} are purely imaginary, and hence Eq. (19.59) has no real solution unless $Z_{i\infty}$ and Z_{i0} are of opposite phase. As illustrated in Fig. 19.37, if at a given frequency $Z_{i\infty}$ and Z_{i0} are both inductive, then zero-voltage switching occurs for all loads. Zero-current switching occurs for all loads when $Z_{i\infty}$ and Z_{i0} are both capacitive. Therefore, Theorem 2 is proved.

Figure 19.38(a) illustrates the phase response of $Z_i(j\omega)$ as R varies from 0 to ∞ , for the LCC inverter. A typical dependence of R_{crit} and the matched-load impedance $\|Z_{o0}\|$ on frequency is illustrated in Fig. 19.38(b). Zero-voltage switching occurs for all loads when $f > f_\infty$, and zero-current switching occurs for all loads when $f < f_0$. Over the range $f_0 < f < f_\infty$, Z_{i0} is inductive while $Z_{i\infty}$ is capacitive; hence, zero-voltage switching occurs for $R < R_{crit}$ while zero-current switching occurs for $R > R_{crit}$. At frequency f_m , $R_{crit} = \|Z_{o0}\|$, and hence the ZVS/ZCS boundary is encountered exactly at matched load. It is commonly desired to obtain zero-voltage switching at matched load, with low circulating currents and good efficiency at light load. It is apparent that this requires operation in the range $f_0 < f < f_m$. Zero-voltage switching will then be obtained under matched-load and short-circuit conditions, but will be lost at light load. The choice of element values such that $\|Z_{i0}\| \ll \|Z_{i\infty}\|$ is advantageous in that the range of loads leading to zero-voltage switching is maximized.

19.4.4 Another Example

As a final example, let us consider selection of the resonant tank elements to obtain a given output characteristic at a certain switching frequency, and let's evaluate the effect of this choice on R_{crit} . It is desired to operate a resonant inverter at switching frequency $f_s = 100$ kHz, with an input voltage of $V_g = 160$ V. The converter should be capable of producing an open-circuit peak output voltage $V_{oc} = 400$ V, and should also produce a nominal output of 150 Vrms at 25 W. It is desired to select resonant tank elements that accomplish this.

The specifications imply that the converter should exhibit an open-circuit transfer function of

$$\|H_\infty(j\omega_s)\| = \frac{V_{oc}}{V_{s1}} = \frac{(400 \text{ V})}{\left(\frac{4}{\pi} 160 \text{ V}\right)} = 1.96 \quad (19.60)$$

The required short-circuit current is found by solving Eq. (19.42) for I_{sc} :

$$I_{sc} = \frac{I}{\sqrt{1 - \left(\frac{V}{V_{oc}}\right)^2}} \quad (19.61)$$

The specifications also imply that the peak voltage and current at the nominal operating point are

$$\begin{aligned}
 V &= 150\sqrt{2} = 212 \text{ V} \\
 I &= \frac{P}{V_{rms}} \sqrt{2} = \frac{25 \text{ W}}{150 \text{ V}} \sqrt{2} = 0.236 \text{ A} \\
 R_{nom} &= \frac{V}{I} = 900 \Omega
 \end{aligned} \tag{19.62}$$

Substitution of Eq. (19.62) into Eq. (19.61) yields

$$I_{sc} = \frac{(0.236 \text{ A})}{\sqrt{1 - \left(\frac{212 \text{ V}}{400 \text{ V}}\right)^2}} = 0.278 \text{ A} \tag{19.63}$$

Matched load therefore occurs at the operating point

$$\begin{aligned}
 V_{mat} &= \frac{V_{oc}}{\sqrt{2}} = 283 \text{ V} \\
 I_{mat} &= \frac{I_{sc}}{\sqrt{2}} = 0.196 \text{ A} \\
 \|Z_{o0}(j\omega_s)\| &= \frac{V_{oc}}{I_{sc}} = 1439 \Omega
 \end{aligned} \tag{19.64}$$

Let us select the values of the tank elements in the LCC tank network illustrated in Fig. 19.39(a). The impedances of the series and parallel branches can be represented using the reactances X_s and X_p illustrated in Fig. 19.39(b), with

$$\begin{aligned}
 jX_s &= j\omega_s L + \frac{1}{j\omega_s C_s} = j\left(\omega_s L - \frac{1}{\omega_s C_s}\right) \\
 jX_p &= \frac{1}{j\omega_s C_p} = j\left(-\frac{1}{\omega_s C_p}\right)
 \end{aligned} \tag{19.65}$$

The transfer function $H_\infty(j\omega_s)$ is given by the voltage divider formula

$$H_\infty(j\omega_s) = \frac{jX_p}{jX_s + jX_p} \tag{19.66}$$

The output impedance $Z_{o0}(j\omega_s)$ is given by the parallel combination

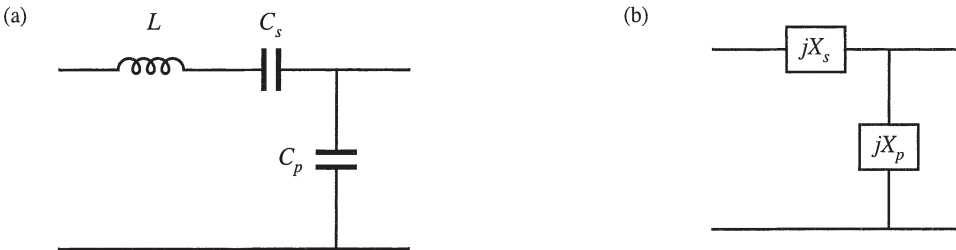


Fig. 19.39 Tank network of the LCC inverter example: (a) schematic, (b) representation of series and parallel branches by reactances X_s and X_p .

$$Z_{o0}(j\omega_s) = jX_s \parallel jX_p = \frac{-X_s X_p}{j(X_s + X_p)} \quad (19.67)$$

Solution of Eqs. (19.66) and (19.67) for X_p and X_s leads to

$$\begin{aligned} jX_p &= \frac{Z_{o0}(j\omega_s)}{1 - H_{\infty}(j\omega_s)} \\ X_s &= X_p \frac{1 - H_{\infty}(j\omega_s)}{H_{\infty}(j\omega_s)} \end{aligned} \quad (19.68)$$

Hence, the capacitance C_p should be chosen equal to

$$\begin{aligned} X_p &= -1499 \, \Omega \\ C_p &= -\frac{1}{\omega_s X_p} = \frac{H_{\infty}(j\omega_s) - 1}{\omega_s \| Z_{o0}(j\omega_s) \|} = \frac{(1.96) - 1}{(2\pi \, 100 \, \text{kHz})(1439 \, \Omega)} \cong 1 \, \text{nF} \end{aligned} \quad (19.69)$$

and the reactance of the series branch should be chosen according to

$$X_s = X_p \frac{1 - H_{\infty}(j\omega_s)}{H_{\infty}(j\omega_s)} = (-1493 \, \Omega) \frac{1 - (1.96)}{(1.96)} = 733 \, \Omega \quad (19.70)$$

Since X_s is comprised of the series combination of the inductor L and capacitor C_s , there is a degree of freedom in choosing the values of L and capacitor C_s to realize X_s . For example, we could choose C_s very large (tending to a short circuit); this effectively would result in a parallel resonant converter with $L = X_s/\omega_s = 1.17 \, \text{mH}$. For nonzero C_s , L must be chosen according to

$$L = \frac{1}{\omega_s} \left(X_s + \frac{1}{\omega_s C_s} \right) \quad (19.71)$$

For example, the choice $C_s = C_p = 1.06 \, \text{nF}$ leads to $L = 3.5 \, \text{mH}$. Designs using different C_s will exhibit exactly the same characteristics at the design frequency; however, the behavior at other switching frequencies will differ.

For the tank network illustrated in Fig. 19.39, the value of R_{crit} is completely determined by the parameters of the output characteristic ellipse; i.e., by the specification of V_g , V_{oc} and I_{sc} . Note that $Z_{o\infty}$, the tank output impedance with the tank input port open-circuited, is equal to jX_p . Substitution of expressions for $Z_{o\infty}$ and Z_{o0} into Eq. (19.57) leads to the following expression for R_{crit} :

$$R_{crit} = \sqrt{\frac{Z_{o0}^2(j\omega_s)}{1 - H_{\infty}(j\omega_s)}} \quad (19.72)$$

Since Z_{o0} and H_{∞} are determined by the operating point specifications, then R_{crit} is also. Evaluation of Eq. (19.72) for this example leads to $R_{crit} = 1466 \, \Omega$. Therefore, the inverter will operate with zero-voltage switching for $R < 1466 \, \Omega$, including at the nominal operating point $R = 900 \, \Omega$. Other topologies of tank network, more complex than the circuit illustrated in Fig. 19.39(b), may have additional degrees of freedom that allow R_{crit} to be independently chosen.

The choice $C_s = 3C_p = 3.2 \, \text{nF}$ leads to $L = 1.96 \, \mu\text{H}$. The following frequencies are obtained:

$$\begin{aligned}
f_{\infty} &= 127 \text{ kHz} \\
f_m &= 100.6 \text{ kHz} \\
f_s &= 100.0 \text{ kHz} \\
f_0 &= 64 \text{ kHz}
\end{aligned} \tag{19.73}$$

Regardless of how C_s is chosen, the open-circuit tank input impedance is

$$Z_{j\omega} = j(X_s + X_p) = j(733 \Omega + (-1493 \Omega)) = -j760 \Omega \tag{19.74}$$

Therefore, when the load is open-circuited, the transistor peak current has magnitude

$$I_{s1} = \frac{V_{s1}}{\|Z_{j\omega}\|} = \frac{\frac{4}{\pi}(160 \text{ V})}{760 \Omega} = 0.268 \text{ A} \tag{19.75}$$

When the load is short-circuited, the transistor peak current has magnitude

$$I_{s1} = \frac{V_{s1}}{\|Z_{j\omega}\|} = \frac{V_{s1}}{|X_s|} = \frac{\frac{4}{\pi}(160 \text{ V})}{(733 \Omega)} = 0.278 \text{ A} \tag{19.76}$$

which is nearly the same as the result in Eq. (19.75). The somewhat large open-circuit switch current occurs because of the relatively-high specified open-circuit output voltage; lower values of V_{oc} would reduce the result in Eq. (19.75).

19.5 EXACT CHARACTERISTICS OF THE SERIES AND PARALLEL RESONANT CONVERTERS

The exact steady-state behavior of resonant converters can be determined via methods such as state-plane analysis. A detailed analysis of resonant dc–dc converters is beyond the scope of this book. However, the exact steady-state characteristics of ideal series [1, 13–20] and parallel [6, 22–25] resonant dc–dc converters (Fig. 19.40) are summarized in this section. Small-signal ac modeling has also been described in the literature; several relevant papers are [27–30].

19.5.1 Series Resonant Converter

At a given switching frequency, the series resonant dc–dc converter can operate in one continuous conduction mode, and possibly in several discontinuous conduction modes. The mode index k is defined as the integer that satisfies

$$\frac{f_0}{k+1} < f_s < \frac{f_0}{k} \quad \text{or} \quad \frac{1}{k+1} < F < \frac{1}{k} \tag{19.77}$$

where $F = f_s/f_0$ is the normalized switching frequency. The subharmonic number ξ is defined as

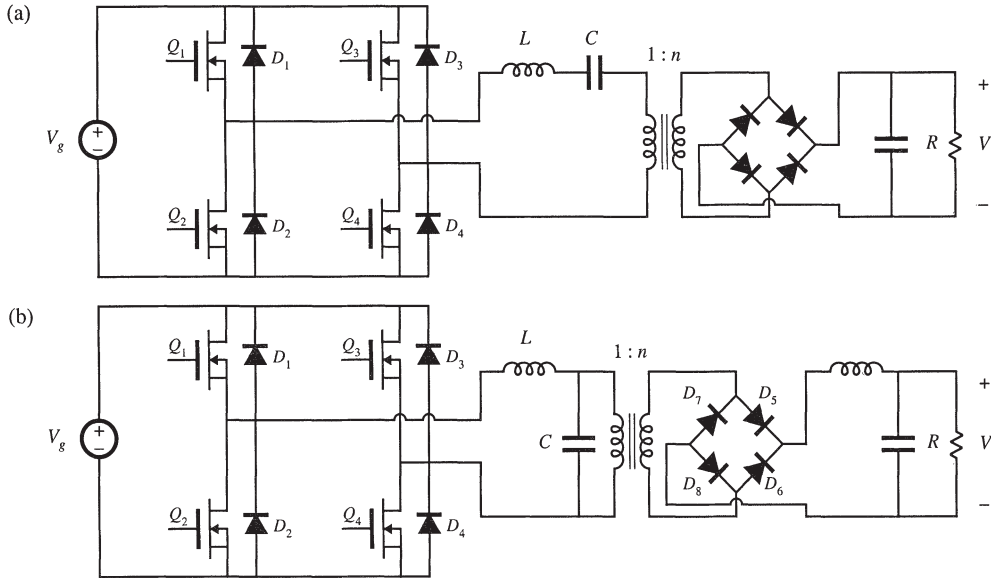


Fig. 19.40 Transformer-isolated resonant dc-dc converters: (a) series resonant converter, (b) parallel resonant converter.

$$\xi = k + \frac{1 + (-1)^k}{2} \quad (19.78)$$

Values of k and ξ as functions of f_s are summarized in Fig. 19.41(a). The subharmonic number ξ denotes the dominant harmonic that excites the tank resonance. When the converter is heavily loaded, it operates in type k continuous conduction mode. As the load is reduced (i.e., as the load resistance R is increased), the converter enters the type k discontinuous conduction mode. Further reducing the load causes the converter to enter the type $(k - 1)$ DCM, type $(k - 2)$ DCM, ..., type 1 DCM. There is no type 0 DCM, and hence when the converter operates above resonance, only the type 0 continuous conduction mode is possible.

In the type k continuous conduction mode, the series resonant converter exhibits elliptical output characteristics, given by

$$M^2 \xi^2 \sin^2\left(\frac{\gamma}{2}\right) + \frac{1}{\xi^2} \left(\frac{J\gamma}{2} + (-1)^k\right)^2 \cos^2\left(\frac{\gamma}{2}\right) = 1 \quad (19.79)$$

For the transformer-isolated converters of Fig. 19.40, M and J are related to the load voltage V and load current I according to

$$M = \frac{V}{nV_g} \quad J = \frac{InR_0}{V_g} \quad (19.80)$$

Again, R_0 is the tank characteristic impedance, referred to the transformer primary side. The quantity γ is the angular length of one-half of the switching period:

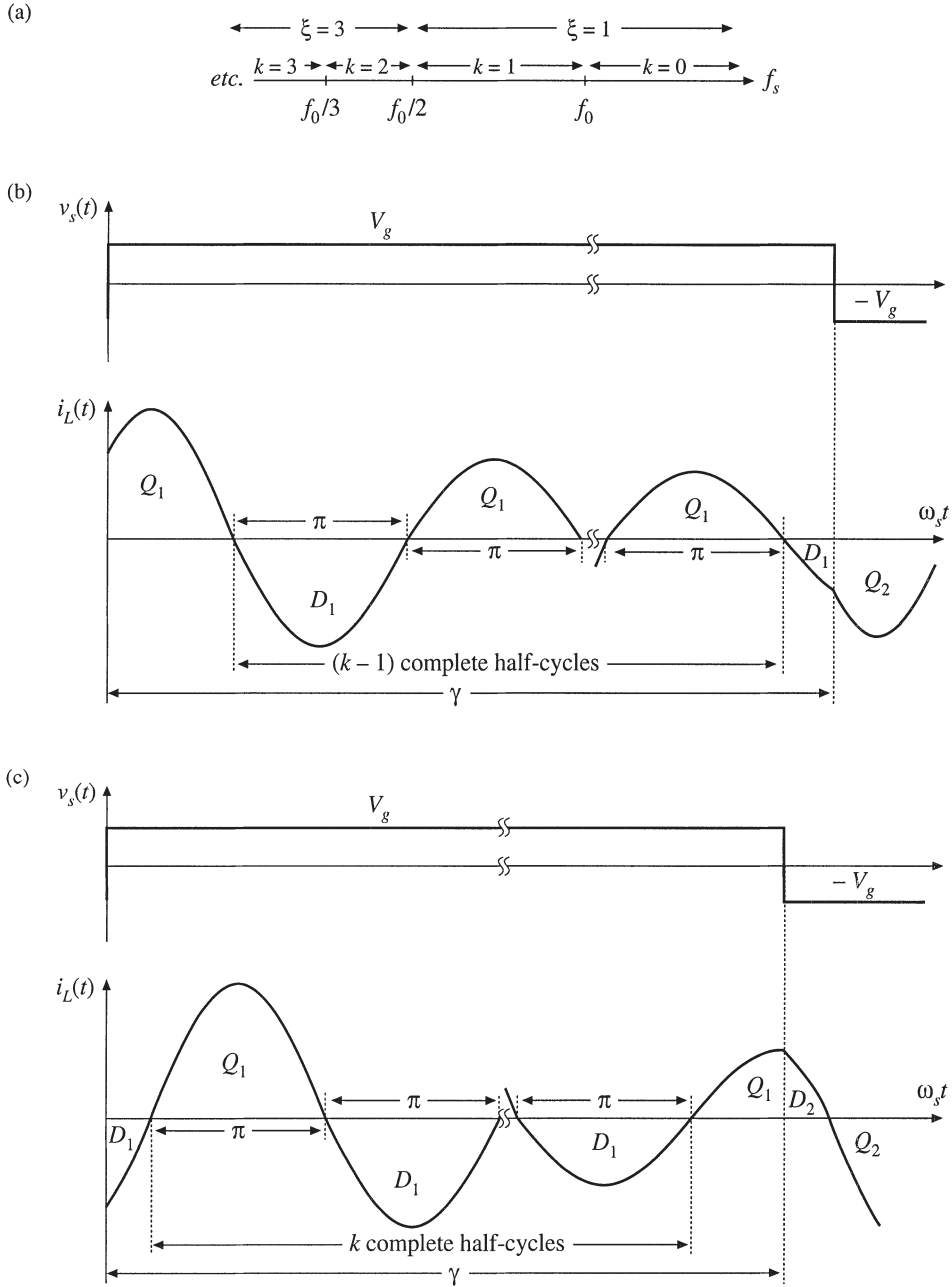


Fig. 19.41 Continuous conduction modes of the series resonant converter: (a) switching frequency ranges over which various mode indices k and subharmonic numbers ξ occur; (b) tank inductor current waveform, type k CCM, for odd k ; (c) tank inductor current waveform, type k CCM, for even k .

$$\gamma = \frac{\omega_0 T_s}{2} = \frac{\pi}{F} \quad (19.81)$$

Equation (19.79) is valid only for k satisfying Eq. (19.77). It predicts that the voltage conversion ratio M is restricted to the range

$$0 \leq M \leq \frac{1}{\xi} \quad (19.82)$$

This is consistent with Eq. (19.21).

Typical CCM tank current waveforms are illustrated in Fig. 19.41. When k is even, the tank inductor current is initially negative. In consequence, the switch network antiparallel diodes conduct first, for a fraction of a half resonant cycle. If k is odd, then each half switching period is initiated by conduction of the switch network transistors. In either case, this is followed by $(\xi - 1)$ complete tank half-cycles of ringing. The half-switching period is then concluded by a subinterval shorter than one complete resonant half-cycle, in which the device that did not initially conduct is on. The next half switching period then begins, and is symmetrical.

The steady-state control-plane characteristic can be found for a resistive load R obeying $V = IR$, by substitution of the normalized relation $J = MQ$ into Eq. (19.79), where $Q = n^2 R_0 / R$. Use of the quadratic formula and some algebraic manipulations allows solution for M , as a function of load (via Q) and switching frequency (via γ):

$$M = \frac{\left(\frac{Q\gamma}{2}\right)}{\xi^4 \tan^2\left(\frac{\gamma}{2}\right) + \left(\frac{Q\gamma}{2}\right)^2} \left[(-1)^{k+1} + \sqrt{1 + \frac{\left[\xi^2 - \cos^2\left(\frac{\gamma}{2}\right)\right] \left[\xi^4 \tan^2\left(\frac{\gamma}{2}\right) + \left(\frac{Q\gamma}{2}\right)^2\right]}{\left(\frac{Q\gamma}{2}\right)^2 \cos^2\left(\frac{\gamma}{2}\right)}} \right] \quad (19.83)$$

This is the closed-form relationship between the conversion ratio M and the switching frequency, for a resistive load. It is valid for any continuous conduction mode k .

The type k discontinuous conduction modes, for k odd, occur over the frequency range

$$f_s < \frac{f_0}{k} \quad (19.84)$$

In these modes, the output voltage is independent of both load current and switching frequency, and is described by

$$M = \frac{1}{k} \quad (19.85)$$

The type k discontinuous conduction mode, for odd k , occurs over the range of load currents given by

$$\frac{2(k+1)}{\gamma} > J > \frac{2(k-1)}{\gamma} \quad (19.86)$$

In the odd discontinuous conduction modes, the tank current rings for k complete resonant half cycles. All four output bridge rectifier diodes then become reverse-biased, and the tank current remains at zero until the next switching half-period begins, as illustrated in Fig. 19.42. Series resonant converters are not

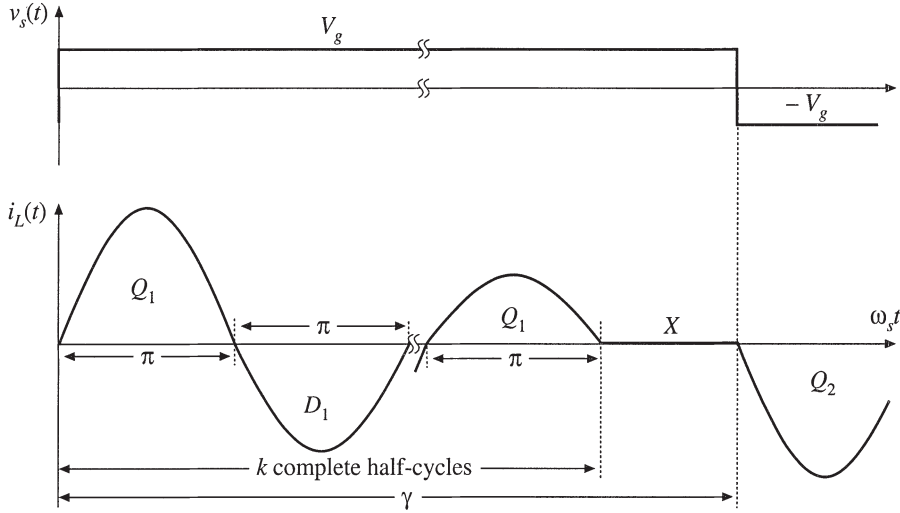


Fig. 19.42 Tank inductor current waveform, type k DCM, for odd k .

normally purposely designed to operate in odd discontinuous conduction modes, because the output voltage is not controllable. Nonetheless, when the load is removed with $f_s < f_0$, the series resonant converter operates in $k = 1$ DCM with $M = 1$.

The type k discontinuous conduction mode, for k even, also occurs over the frequency range

$$f_s < \frac{f_0}{k} \quad (19.87)$$

Even discontinuous conduction modes exhibit current source characteristics, in which the load current is a function of switching frequency and input voltage, but not of the load voltage. The output relationship is:

$$J = \frac{2k}{\gamma} \quad (19.88)$$

Operation in this mode occurs for

$$\frac{1}{k-1} > M > \frac{1}{k+1} \quad (19.89)$$

In the even discontinuous conduction modes, the tank current rings for k complete resonant half-cycles during each switching half-period. All four output bridge then become reverse-biased, and the tank current remains at zero until the next switching half-period is initiated. Tank current waveforms are illustrated in Fig. 19.43 for even DCM.

The series resonant converter possesses some unusual properties when operated in an even discontinuous conduction mode. A dc equivalent circuit is given in Fig. 19.44, consisting of a gyrator with gyration conductance $g = 2k/gn^2R_0$. The gyrator has the property of transforming circuits into their dual networks; in the typical dc-dc converter application, the input voltage source V_g is effectively transformed into its dual, an output current source of value gV_g . Series resonant converters have been purposely designed to operate in the $k = 2$ DCM, at power levels of several tens of kW.

The complete control plane characteristics can now be plotted using Eqs. (19.77) to (19.89).

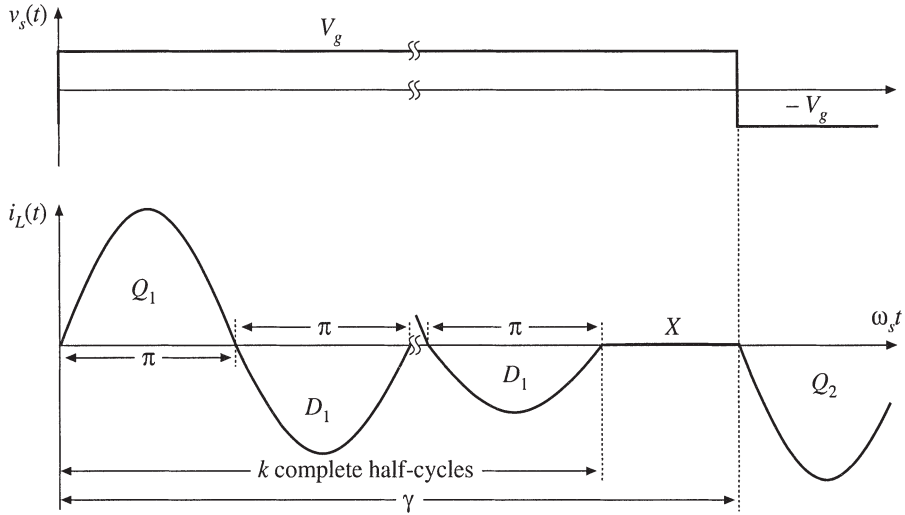
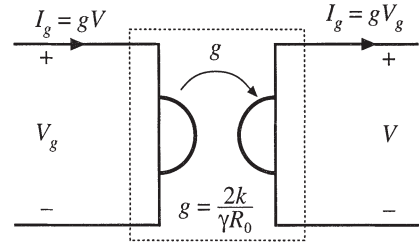


Fig. 19.43 Tank inductor current waveform, type k DCM, for even k .

Fig. 19.44 Steady-state equivalent circuit model for an even discontinuous conduction mode: an effective gyrator. The converter exhibits current source characteristics.



The result is shown in Fig. 19.45, and the mode boundaries are explicitly diagrammed in Fig. 19.46. It can be seen that, for operation above resonance, the only possible operating mode is the $k = 0$ CCM, and that the output voltage decreases monotonically with increasing switching frequency. Reduction in load current (or increase in load resistance, which decreases Q) causes the output voltage to increase. A number of successful designs that operate above resonance and utilize zero-voltage switching have been documented in the literature [7,21].

Operation below resonance is complicated by the presence of subharmonic and discontinuous conduction modes. The $k = 1$ CCM and $k = 2$ DCM are well behaved, in that the output voltage increases monotonically with increasing switching frequency. Increase of the load current again causes the output voltage to decrease. Successful designs that operate in these modes and employ zero-current switching are numerous. However, operation in the higher-order modes ($k = 2$ CCM, $k = 4$ DCM, etc.) is normally avoided.

Given F and Q , the operating mode can be evaluated directly, using the following algorithm. First, the continuous conduction mode k corresponding to operation at frequency F with heavy loading is found:

$$k = \text{INT}\left(\frac{1}{F}\right) \quad (19.90)$$

where $\text{INT}(x)$ denotes the integer part of x . Next, the quantity k_1 is determined:

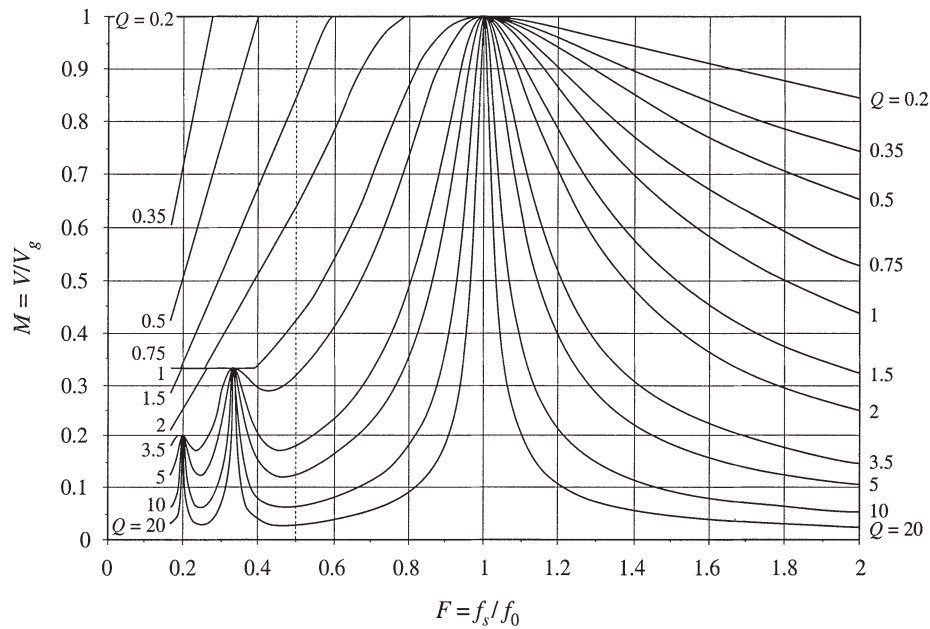


Fig. 19.45 Complete control plane characteristics of the series resonant converter, for the range $0.2 \leq F \leq 2$.

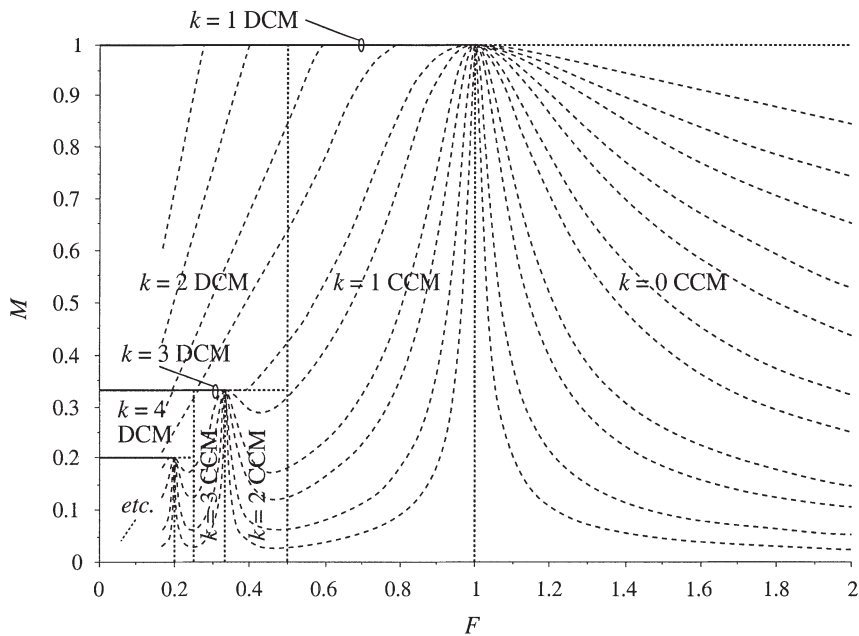


Fig. 19.46 Continuous and discontinuous conduction mode boundaries.

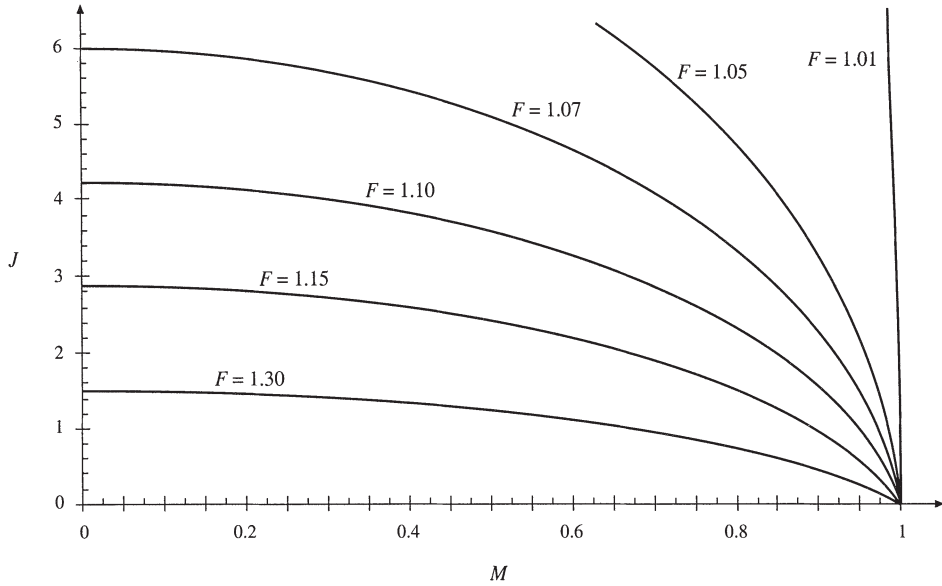


Fig. 19.47 Output characteristics, $k = 0$ CCM (above resonance).

$$k_1 = \text{INT} \left(\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{Q\pi}{2F}} \right) \quad (19.91)$$

The converter operates in type k CCM provided that:

$$k_1 > k \quad (19.92)$$

Otherwise, the converter operates in type k_1 DCM. A simple algorithm can therefore be defined, in which the conversion ratio M is computed for a given F and Q . First, Eqs. (19.90) to (19.92) are evaluated, to determine the operating mode. Then, the appropriate equation (19.83), (19.85), or (19.88) is evaluated to find M .

Output I - V plane characteristics for the $k = 0$ CCM, plotted using Eq. (19.79), are shown in Fig. 19.47. The constant-frequency curves are elliptical, and all pass through the point $M = 1$, $J = 0$. For a given switching frequency, the operating point is given by the intersection of the elliptical converter output characteristic with the load I - V characteristic.

Output plane characteristics that combine the $k = 1$ CCM, $k = 1$ DCM, and $k = 2$ DCM are shown in Fig. 19.48. These were plotted using Eqs. (19.79), (19.85), and (19.88). These curves were plotted with the assumption that the transistors are allowed to conduct no longer than one tank half-cycle during each switching half-period; this eliminates subharmonic modes and causes the converter to operate in $k = 2$ or $k = 1$ DCM whenever $f_s < 0.5f_0$. It can be seen that the constant-frequency curves are elliptical in the continuous conduction mode, vertical (voltage source characteristic) in the $k = 1$ DCM, and horizontal (current source characteristic) in the $k = 2$ DCM.

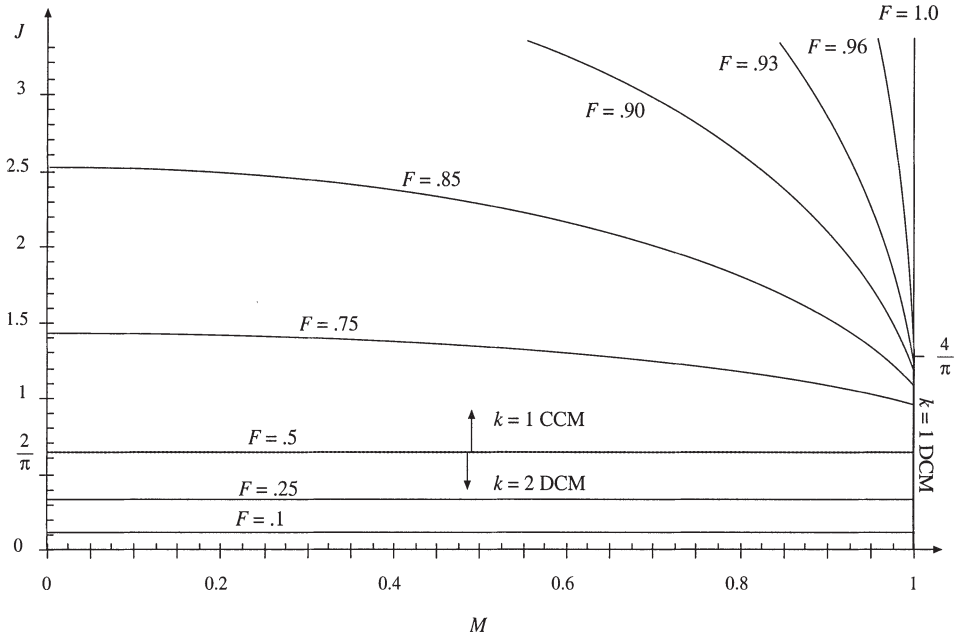


Fig. 19.48 Output characteristics, $k = 1$ CCM, $k = 1$ DCM, and $k = 2$ DCM (below resonance).

19.5.2 Parallel Resonant Converter

For operation in the frequency range $0.5f_0 < f_s < \infty$, the parallel resonant dc-dc converter exhibits one continuous conduction mode and one discontinuous conduction mode. Typical CCM switch voltage $v_s(t)$, tank inductor current $i_L(t)$, and tank capacitor voltage $v_C(t)$ waveforms are illustrated in Fig. 19.49. The CCM converter output characteristics are given by

$$M = \left(\frac{2}{\gamma} \right) \left(\varphi - \frac{\sin(\varphi)}{\cos\left(\frac{\gamma}{2}\right)} \right) \quad (19.93)$$

$$\varphi = \begin{cases} -\cos^{-1} \left(\cos\left(\frac{\gamma}{2}\right) + J \sin\left(\frac{\gamma}{2}\right) \right) & \text{for } 0 < \gamma < \pi \text{ (above resonance)} \\ +\cos^{-1} \left(\cos\left(\frac{\gamma}{2}\right) + J \sin\left(\frac{\gamma}{2}\right) \right) & \text{for } \pi < \gamma < 2\pi \text{ (below resonance)} \end{cases} \quad (19.94)$$

and where M , J , and γ are again defined as in Eqs. (19.80) and (19.81). Given the normalized load current J and the half-switching-period-angle γ , one can evaluate Eq. (19.94) to find φ , and then evaluate Eq. (19.93) to find the converter voltage conversion ratio M . In other words, the output voltage can be found for a given load current and switching frequency, without need for computer iteration.

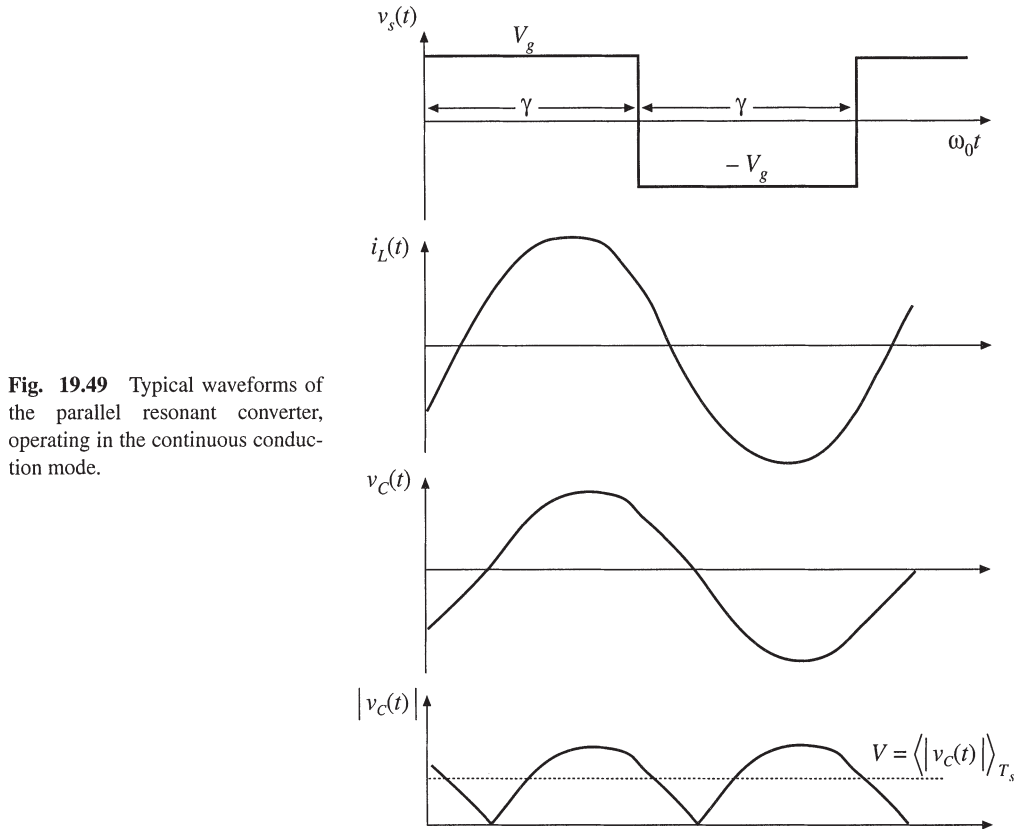


Fig. 19.49 Typical waveforms of the parallel resonant converter, operating in the continuous conduction mode.

A discontinuous conduction mode mechanism occurs in the parallel resonant converter which is the dual of the discontinuous conduction mode mechanism of the series resonant converter. In this mode, a discontinuous subinterval occurs in which all four output bridge rectifier diodes are forward-biased, and the tank capacitor voltage remains at zero. This mode occurs both above and below resonance when the converter is heavily loaded. Typical DCM tank capacitor voltage and inductor current waveforms are illustrated in Fig. 19.50. The condition for operation in the discontinuous conduction mode is

$$\begin{aligned} J &> J_{crit}(\gamma) && \text{for DCM} \\ J &< J_{crit}(\gamma) && \text{for CCM} \end{aligned} \quad (19.95)$$

where

$$J_{crit}(\gamma) = -\frac{1}{2} \sin(\gamma) + \sqrt{\sin^2\left(\frac{\gamma}{2}\right) + \frac{1}{4} \sin^2(\gamma)} \quad (19.96)$$

The discontinuous conduction mode is described by the following set of equations:

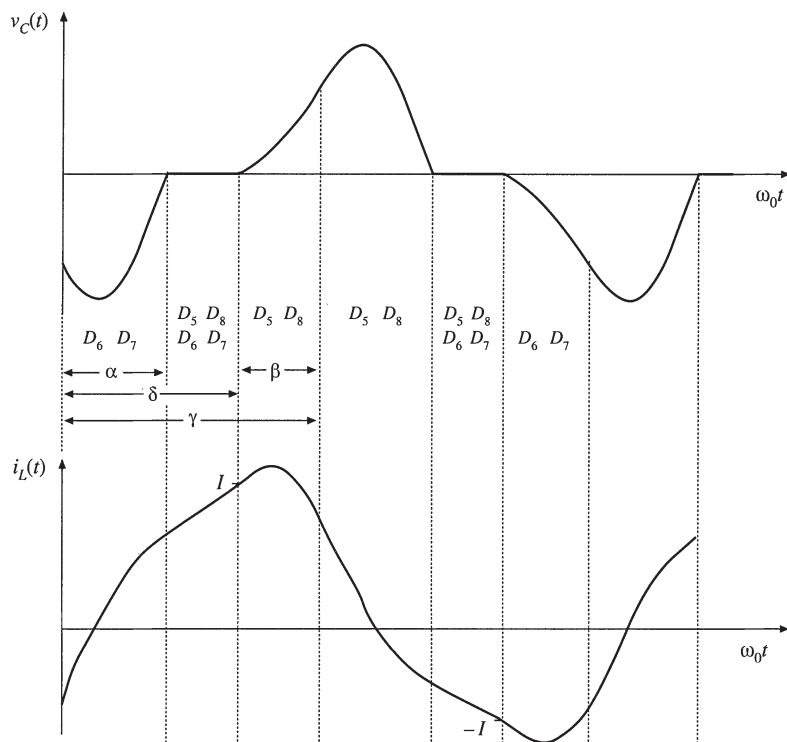


Fig. 19.50 Typical waveforms of the parallel resonant converter, operating in the discontinuous conduction mode.

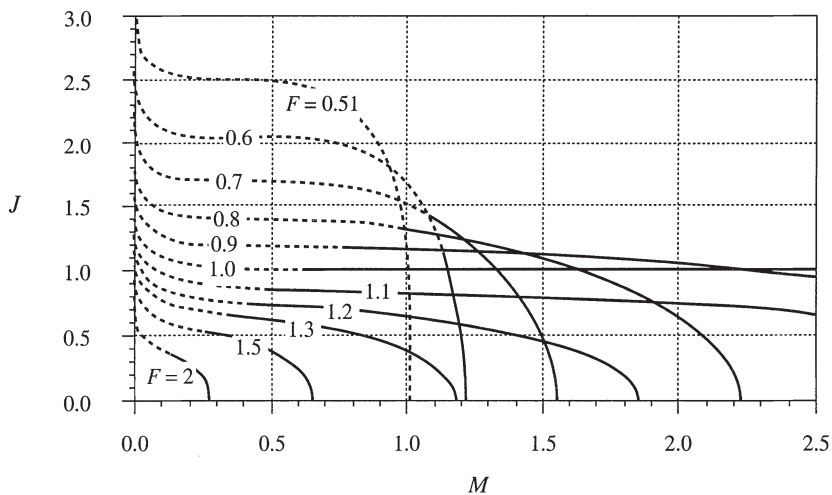


Fig. 19.51 Exact output characteristics of the parallel resonant converter, for $F > 0.5$. Solid curves: CCM, dashed curves: DCM.

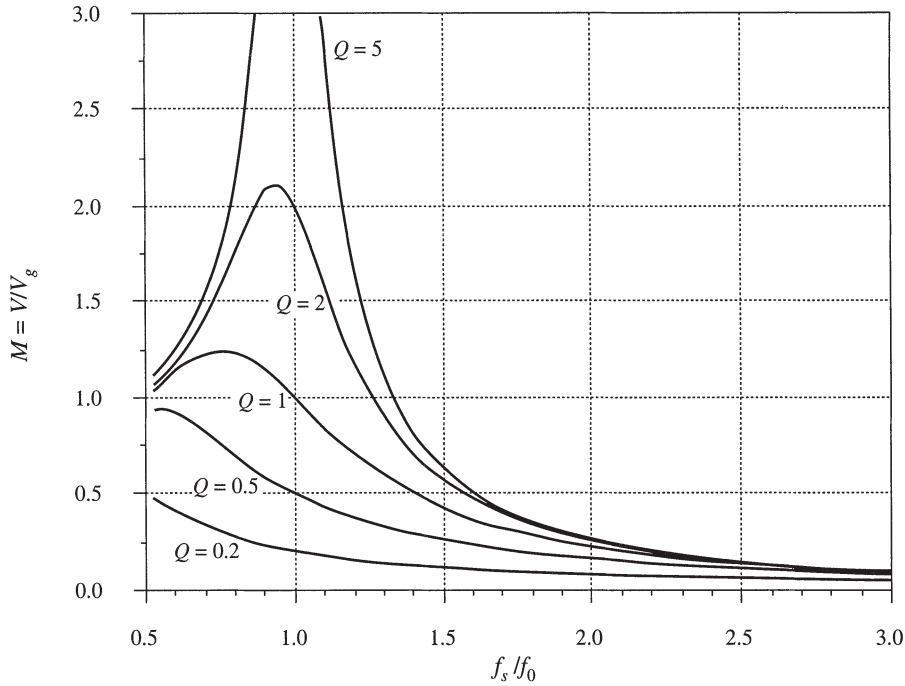


Fig. 19.52 Exact control characteristics of the parallel resonant converter, with a resistive load. Both CCM and DCM operation is included, for $0.5 \leq F \leq 3$.

$$\begin{aligned}
 M_{C0} &= 1 - \cos(\beta) \\
 J_{L0} &= J + \sin(\beta) \\
 \cos(\alpha + \beta) - 2 \cos(\alpha) &= -1 \\
 -\sin(\alpha + \beta) + 2 \sin(\alpha) + (\delta - \alpha) &= 2J \\
 \beta + \delta &= \gamma \\
 M &= 1 + \left(\frac{2}{\gamma}\right)(J - \delta)
 \end{aligned} \tag{19.97}$$

Unfortunately, the solution to this set of equations is not known in closed form, because of the mixture of linear and trigonometric terms. In consequence, the equations must be solved iteratively. For a given γ and J , a computer is used to iteratively find the angles α , β , and δ . M is then evaluated, and the output plane characteristics can be plotted. The result is given in Fig. 19.51. The dashed lines are the DCM solutions, and the solid lines are the valid CCM solutions. Figure 19.51 describes the complete dc behavior of the ideal parallel resonant converter for all switching frequencies above $0.5f_0$. For given values of normalized switching frequency $F = f_s/f_0 = \pi/\gamma$, the relationship between the normalized output current J and the normalized output voltage M is approximately elliptical. At resonance ($F = 1$), the CCM ellipse degenerates to the horizontal line $J = 1$, and the converter exhibits current source characteristics. Above resonance, the converter can both step up the voltage ($M > 1$) and step down the voltage ($M < 1$). The normalized load current is then restricted to $J < 1$, corresponding to $I < V_g/nR_0$. For a given switching frequency greater than the resonant frequency, the actual limit on maximum load current is even more restrictive than this limit. Below resonance, the converter can also step up and step down the volt-

age. Normalized load currents J greater than one are also obtainable, depending on M and F . However, no solutions occur when M and J are simultaneously large.

In Fig. 19.52, the control plane characteristics are plotted for a resistive load. The parameter Q is defined for the parallel resonant converter as $Q = R/n^2 R_0$. The normalized load current is then given by $J = M/Q$.

19.6 SUMMARY OF KEY POINTS

1. The sinusoidal approximation allows a great deal of insight to be gained into the operation of resonant inverters and dc–dc converters. The voltage conversion ratio of dc–dc resonant converters can be directly related to the tank network transfer function. Other important converter properties, such as the output characteristics, dependence (or lack thereof) of transistor current on load current, and zero-voltage- and zero-current-switching transitions, can also be understood using this approximation. The approximation is accurate provided that the effective Q factor is sufficiently large, and provided that the switching frequency is sufficiently close to resonance.
2. Simple equivalent circuits are derived, which represent the fundamental components of the tank network waveforms, and the dc components of the dc terminal waveforms.
3. Exact solutions of the ideal dc–dc series and parallel resonant converters are listed here as well. These solutions correctly predict the conversion ratios, for operation not only in the fundamental continuous conduction mode, but in discontinuous and subharmonic modes as well.
4. Zero-voltage switching mitigates the switching loss caused by diode recovered charge and semiconductor device output capacitances. When the objective is to minimize switching loss and EMI, it is preferable to operate each MOSFET and diode with zero-voltage switching.
5. Zero-current switching leads to natural commutation of SCRs, and can also mitigate the switching loss due to current tailing in IGBTs.
6. The input impedance magnitude $\|Z_i\|$, and hence also the transistor current magnitude, are monotonic functions of the load resistance R . The dependence of the transistor conduction loss on the load current can be easily understood by simply plotting $\|Z_i\|$ in the limiting cases as $R \rightarrow \infty$ and as $R \rightarrow 0$, or $\|Z_{i\infty}\|$ and $\|Z_{i0}\|$.
7. The ZVS/ZCS boundary is also a simple function of $Z_{i\infty}$ and Z_{i0} . If ZVS occurs at open-circuit and at short-circuit, then ZVS occurs for all loads. If ZVS occurs at short-circuit, and ZCS occurs at open-circuit, then ZVS is obtained at matched load provided that $\|Z_{i\infty}\| > \|Z_{i0}\|$.
8. The output characteristics of all resonant inverters considered here are elliptical, and are described completely by the open-circuit transfer function magnitude $\|H_{\infty}\|$, and the output impedance $\|Z_{o0}\|$. These quantities can be chosen to match the output characteristics to the application requirements.

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PROBLEMS

- 19.1** Analysis of a half-bridge dc–dc parallel resonant converter, operated above resonance. In Fig. 19.53, the elements C_b , L_F , and C_F are large in value, and have negligible switching ripple. You may assume that all elements are ideal. You may use the sinusoidal approximation as appropriate.

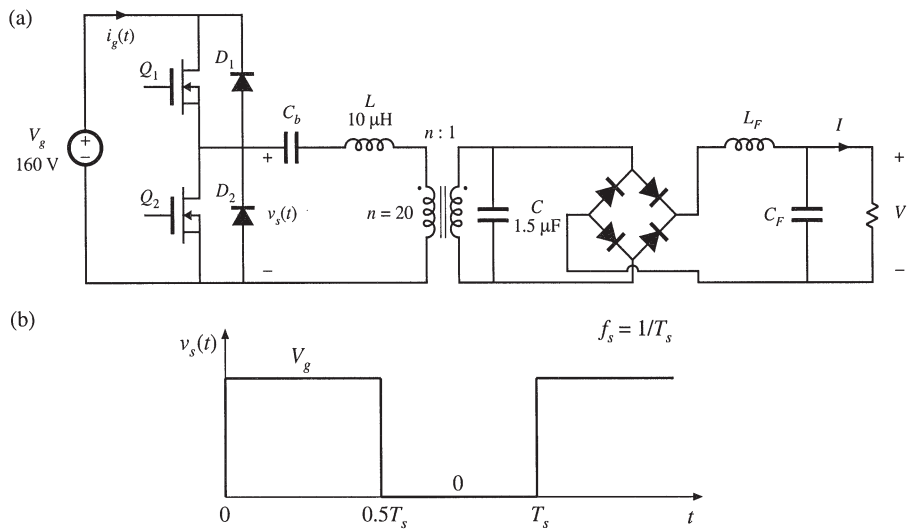


Fig. 19.53 Half-bridge parallel resonant converter of Problem 19.1: (a) schematic, (b) switch voltage waveform.

- (a) Sketch the waveform of the current $i_g(t)$.
- (b) Construct an equivalent circuit for this converter, similar to Fig. 19.22, which models the fundamental components of the tank waveforms and the dc components of the converter input current and output voltage. Clearly label the values and/or give expressions for all elements in your model, as appropriate.
- (c) Solve your model to derive an expression for the conversion ratio $V/V_g = M(F, Q_e, n)$. At rated (maximum) load, this converter produces $I = 20$ A at $V = 3.3$ V.
- (d) What is the converter switching frequency f_s at rated load?
- (e) What is the magnitude of the peak transistor current at rated load?
- At minimum load, the converter produces $I = 2$ A at $V = 3.3$ V.

- (f) What is the converter switching frequency f_s at minimum load?
- (g) What is the magnitude of the peak transistor current at minimum load? Compare with your answer from part (e)—what happens to the conduction loss and efficiency at minimum load?
- 19.2** A dc–dc resonant converter contains an LCC tank network [Fig. 19.1(d)], with an output filter containing a filter inductor as in the parallel resonant dc–dc converter.
- (a) Sketch an equivalent circuit model for this converter, based on the approximate sinusoidal analysis method of Section 19.1. Give expressions for all elements in your model.
- (b) Solve your model, to derive an expression for the conversion ratio $M = V/V_g$. Express M as a function of $F = f_s/f_\infty$, $Q_e = R_e/R_0$, and $n = C_s/C_p$, where f_∞ is defined as in Eq. (19.50) and R_0 is

$$R_0 = \sqrt{\frac{L(C_s + C_p)}{C_s C_p}}$$

- (c) Plot M vs. F , for $n = 1$ and $Q_e = 1, 2$, and 5 .
- (d) Plot M vs. F , for $n = 0.25$ and $Q_e = 1, 2$, and 5 .
- 19.3** Dual of the series resonant converter. In the converter illustrated in Fig. 19.54, L_{F1} , L_{F2} , and C_F are large filter elements, whose switching ripples are small. L and C are tank elements, whose waveforms $i_L(t)$ and $v_C(t)$ are nearly sinusoidal.

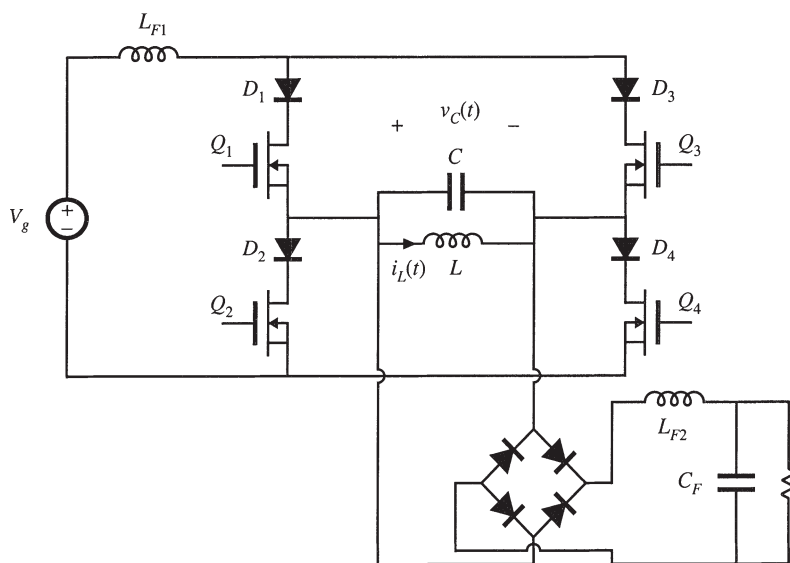


Fig. 19.54 Dual of the series resonant converter, Problem 19.3.

- (a) Using the sinusoidal approximation method, develop equivalent circuit models for the switch network, tank network, and rectifier network.
- (b) Sketch a Bode diagram of the parallel LC parallel tank impedance.
- (c) Solve your model. Find an analytical solution for the converter voltage conversion ratio $M = V/V_g$, as a function of the effective Q_e and the normalized switching frequency $F = f_s/f_0$. Sketch M vs. F .
- (d) What can you say about the validity of the sinusoidal approximation for this converter? Which

parts of your M vs. F plot of part (c) are valid and accurate?

- 19.4** The converter of Problem 19.3 operates below resonance.
- Sketch the waveform $v_C(t)$. For each subinterval, label: (i) which of the diodes D_1 to D_4 and transistors Q_1 to Q_4 conduct current, and (ii) which devices block voltage.
 - Does the reverse recovery process of diodes D_1 to D_4 lead to switching loss? Do the output capacitances of transistors Q_1 to Q_4 lead to switching loss?
 - Repeat parts (a) and (b) for operation above resonance.
- 19.5** A parallel resonant converter operates with a dc input voltage of $V_g = 270$ V. The converter supplies 5 V to a dc load. The dc load power varies over the range 20 W to 200 W. It is desired to operate the power transistors with zero voltage switching. The tank element values are $L = 57$ μ H, $C_p = 0.9$ nF, referred to the transformer primary. The parallel resonant tank network contains an isolation transformer having a turns ratio of 52:1.
- Define F as in Eq. (19.19). Derive an expression for F , as a function of M and Q_e .
 - Determine the switching frequency, peak transistor current, and peak tank capacitor voltage at the maximum load power operating point.
 - Determine the switching frequency, peak transistor current, and peak tank capacitor voltage at the minimum load power operating point.
- 19.6** In a certain resonant inverter application, the dc input voltage is $V_g = 320$ V. The inverter must produce an approximately sinusoidal output voltage having a frequency of 200 kHz. Under no load (output open-circuit) conditions, the inverter should produce a peak-to-peak output voltage of 1500 V. The nominal resistive operating point is 200 Vrms applied to 100 Ω . A nonisolated LCC inverter is employed. It is desired that the inverter operate with zero-voltage switching, at least for load resistances less than 200 Ω .
- Derive expressions for the output open-circuit voltage V_{oc} and short-circuit current I_{sc} of the LCC inverter. Express your results as functions of $F = f_s/f_\infty$, V_g , $R_\infty = L/C_s \parallel C_p$ and $n = C_s/C_p$. The open-circuit resonant frequency f_∞ is defined in Eq. (19.50).
 - To meet the given specifications, how should the short-circuit current I_{sc} be chosen?
 - Specify tank element values that meet the specifications.
 - Under what conditions does your design operate with zero-voltage switching?
 - Compute the peak transistor current under no-load and short-circuit conditions.
- 19.7** A series resonant dc–dc converter operates with a dc input voltage of $V_g = 550$ V. The converter supplies 30 kV to a load. The dc load power varies over the range 5 kW to 25 kW. It is desired to operate the power transistors with zero-voltage switching. The maximum feasible switching frequency is 50 kHz. An isolation transformer having a 1:n turns ratio is connected in series with the tank network. The peak tank capacitor voltage should be no greater than 2000 V, referred to the primary.
- Derive expressions for the peak tank capacitor voltage and peak tank inductor current.
 - Select values for the tank inductance, tank capacitance, and turns ratio, such that the given specifications are met. Attempt to minimize the peak tank inductor current, while maximizing the worst-case minimum switching frequency.
- 19.8** Figure 19.55 illustrates a full-bridge resonant inverter containing an LLC tank network.
- Sketch the Bode diagrams of the input impedance under short-circuit and open-circuit conditions: $\|Z_{i0}(j\omega)\|$ and $\|Z_{i\infty}(j\omega)\|$. Give analytical expressions for the resonant frequencies and asymptotes.
 - Describe the conditions on switching frequency and load resistance that lead to zero-voltage switching.
 - Derive an expression for the frequency f_m , where $\|Z_{i0}\| = \|Z_{i\infty}\|$.

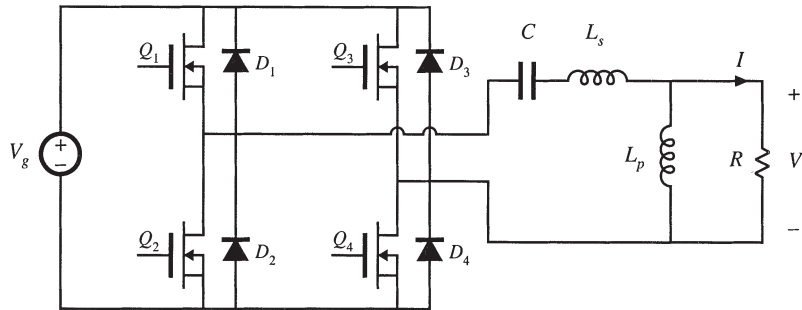


Fig. 19.55 LLC inverter of Problem 19.8.

- (d) Sketch the Bode plot of $\|H_{\infty}(j\omega)\|$. Label the resonant frequency, and give analytical expressions for the asymptotes.

19.9

You are given the LLC inverter circuit of Fig. 19.56. Under nominal conditions, this converter operates at switching frequency $f_s = 100$ kHz. All elements are ideal.

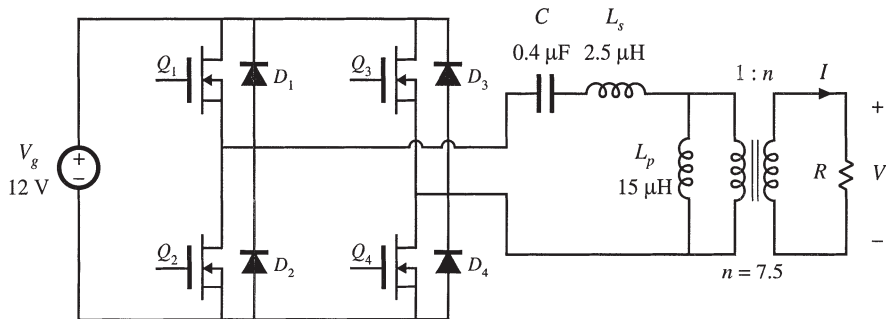


Fig. 19.56 Transformer-isolated LLC inverter, Problem 19.9.

- Determine the numerical values of the open-circuit peak output voltage V_{oc} and the short-circuit peak output current I_{sc} .
- Sketch the elliptical output characteristic. Over what portion of this ellipse does the converter operate with zero-voltage switching? Does it operate with zero-voltage switching at matched load?
- Sketch the Bode plots of $\|Z_{i0}\|$ and $\|Z_{o0}\|$, and label the numerical values of f_0 , f_{∞} , f_m , and f_s .
- What is the numerical value of the peak transistor current when $R = 0$? When $R \rightarrow \infty$?
- The inverter operates with load resistances that can vary between 500Ω and an open circuit. What is the resulting range of output voltage? Does the inverter always operate with zero-voltage switching?

19.10

It is desired to obtain a converter with current source characteristics. Hence, a series resonant converter is designed for operation in the $k = 2$ discontinuous conduction mode. The switching frequency is chosen to be $f_s = 0.225f_0$, where f_0 is the tank resonant frequency (consider only open-loop operation). The load R is a linear resistance which can assume any positive value: $0 \leq R < \infty$.

- Plot the output characteristics (M vs. J), for all values of R in the range $0 \leq R < \infty$. Label mode boundaries, evaluate the short-circuit current, and give analytical expressions for the output characteristics.

- (b) Over what range of R (referred to the tank characteristic impedance R_0) does the converter operate as intended, in the $k = 2$ discontinuous conduction mode?
- 19.11** The parallel resonant converter as a single-phase high-quality rectifier. It is desired to utilize a transformer-isolated parallel resonant dc–dc converter in a single-phase low-harmonic rectifier system. By properly varying the converter switching frequency, a near-ideal rectifier system that can be modeled as in Fig. 18.12 is obtained. You may utilize the results of Section 19.5.2 to answer this problem. The parallel resonant tank network contains an isolation transformer having a $1:n$ turns ratio. You may use either approximate graphical analysis or computer iteration to answer parts (b) and (c).
- (a) Plot the normalized input characteristics (normalized input voltage $m_g = nv_g/v$ vs. normalized input current $j_g = i_g n R_0 / v$) of the parallel resonant converter, operated in the continuous conduction mode above resonance. Plot curves for $F = f_s / f_0 = 1.0, 1.1, 1.2, 1.3, 1.5$, and 2.0 . Compare these characteristics with the desired linear resistive input characteristic $v_g / i_g = R_{emulated}$.
- (b) The converter is operated open-loop, with $F = 1.1$. The applied normalized input voltage is a rectified sinusoid of unity magnitude: $m_g(t) = |\sin(\omega t)|$. Sketch the resulting normalized input current waveform $j_g(t)$. Approximately how large is the peak current? The crossover dead time?
- (c) A feedback loop is now added, which regulates the input current to follow the input voltage such that $i_g(t) = v_g(t) / R_{emulated}$. You may assume that the feedback loop operates perfectly. For the case $R_{emulated} = R_0$, and with the same applied $m_g(t)$ waveform as in part (b), sketch the switching frequency waveform for one ac line period [i.e., show how the controller must vary F to regulate $i_g(t)$]. What is the maximum value of F ? *Note:* In practice, the converter would be designed to operate with a smaller peak value of j_g , so that the switching frequency variations would be better behaved.
- (d) Choose element values (tank inductance, tank capacitance, and transformer turns ratio) such that the converter of part (c) meets the following specifications:
- | | |
|-----------------------------|-----------------|
| Ac input voltage | 120 Vrms, 60 Hz |
| Dc output voltage | 42 V |
| Average power | 800 W |
| Maximum switching frequency | 200 kHz |

Refer the element values to the primary side of the transformer.

20

Soft Switching

In addition to the resonant circuits introduced in Chapter 19, there has been much interest in reducing the switching loss of the PWM converters of the previous chapters. Several of the more popular approaches to obtaining *soft switching* in buck, boost, and other converters, are discussed in this chapter.

Mechanisms that cause switching loss are discussed in Chapter 4, including diode reverse recovery, semiconductor output capacitances, and IGBT current tailing. Soft switching involves mitigation of one or more of these switching loss mechanisms in a PWM converter. The energy that would otherwise be lost is recovered, and is transferred to the converter source or load. The operation of a semiconductor device, during a given turn-on or turn-off switching transition, can be classified as hard-switched, zero-current switched, or zero-voltage switched. Operation of diodes and transistors with soft switching is examined in Section 20.1. In particular, it is preferable to operate diodes with zero-voltage switching at their turn-off transitions, and to operate MOSFETs with zero-voltage switching during their turn-on transitions. However, zero-voltage switching comes at the expense of increased conduction loss, and so the engineer must consider the effect of soft switching on the overall converter efficiency.

Resonant switch converters are a broad class of converters in which the PWM switch network of a conventional buck, boost, or other converter is replaced with a switch cell containing resonant elements. These resonant elements are positioned such that the semiconductor devices operate with zero-current or zero-voltage switching, and such that one or more of the switching loss mechanisms is reduced or eliminated. Other soft-switching approaches may employ resonant switching transitions, but otherwise exhibit the approximately rectangular waveforms of hard-switched converters. In any case, the resulting hybrid converter combines the properties of the resonant switching network and the parent hard-switched PWM converter.

Soft-switching converters can exhibit reduced switching loss, at the expense of increased conduction loss. Obtaining zero-voltage or zero-current switching requires that the resonant elements have large ripple; often, these elements are operated in a manner similar to the discontinuous conduction

modes of the series or parallel resonant converters. As in other resonant schemes, the objectives of designing such a converter are: (1) to obtain smaller transformer and low-pass filter elements via increase of the switching frequency, and/or (2) to reduce the switching loss induced by component nonidealities such as diode stored charge, semiconductor device capacitances, and transformer leakage inductance and winding capacitance.

The resonant switch and soft-switching ideas are quite general, and can be applied to a variety of topologies and applications. A large number of resonant switch networks have been documented in the literature; a few basic approaches are listed here [1–24]. The basic zero-current-switching quasi-resonant switch network is analyzed in detail in Section 20.2. Expressions for the average components of the switch network terminal waveforms are found, leading to determination of the *switch conversion ratio* μ . The switch conversion ratio μ performs the role of the duty cycle d of CCM PWM switch networks. For example, the buck converter exhibits conversion ratio M equal to μ . Both half-wave and full-wave ringing of the tank network is considered; these lead to different switch conversion ratio functions μ . In general, given a PWM CCM converter having conversion ratio $M(d)$, we can replace the PWM switch network with a resonant switch network having switch conversion ratio μ . The resulting quasi-resonant converter will then have conversion ratio $M(\mu)$. So we can obtain soft-switching versions of all of the basic converters (buck, boost, buck-boost, forward, flyback, etc.), that exhibit zero-voltage or zero-current switching and other desirable properties.

In Section 20.3, the characteristics of several other resonant switch networks are listed: the zero-voltage-switching quasi-resonant switch network, the zero-current-switching and zero-voltage-switching quasi-square-wave networks, and the multiresonant switch network. One can obtain zero-voltage switching in all transistors and diodes using these networks.

Several related soft-switching approaches are now popular, which attain zero-voltage switching of the transistor or transistors in commonly-used converters. The zero-voltage transition approach finds application in full-bridge buck-derived converters. Active-clamp snubbers are often added to forward and flyback converters, to attain zero-voltage switching and to reset the transformer. These circuits lead to zero-voltage switching of the transistors, but (less-than-optimal) zero-current switching of the secondary-side diodes. Nonetheless, high efficiency can be achieved. An auxiliary resonant-commutated pole can achieve zero-voltage switching in voltage-source inverters. These converters are briefly discussed in Section 20.4.

20.1 SOFT-SWITCHING MECHANISMS OF SEMICONDUCTOR DEVICES

When loosely used, the terms “zero-current switching” and “zero-voltage switching” normally refer to one or more switching transitions of the transistor in a converter. However, to fully understand how a converter generates switching loss, one must closely examine the switching transitions of every semiconductor device. As described in Section 4.3, there are typically several mechanisms that are sources of significant switching loss. At the turn-off transition of a diode, its reverse-recovery process can induce loss in the transistor or other elements of the converter. The energy stored in the output capacitance of a MOSFET can be lost when the MOSFET turns on. IGBTs can lose significant energy during their turn-off transition, owing to the current-tailing phenomenon. The effects of zero-current switching and zero-voltage switching on each of these devices is discussed in detail below.

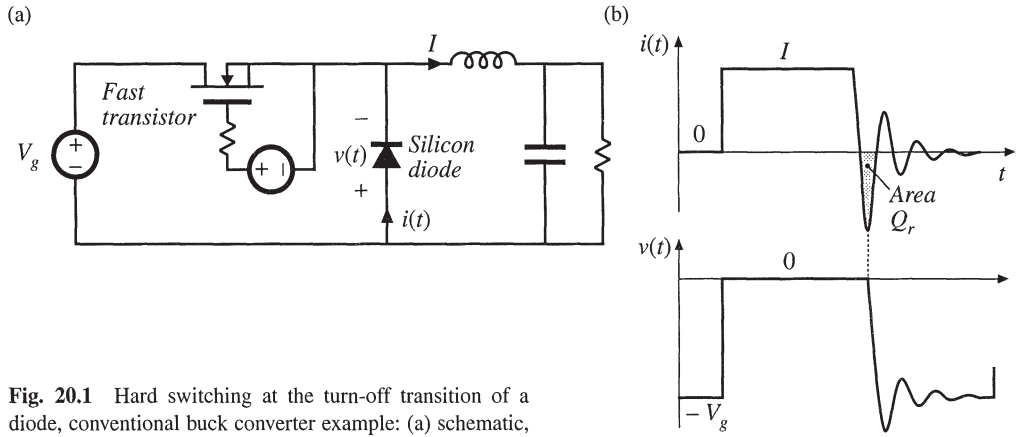


Fig. 20.1 Hard switching at the turn-off transition of a diode, conventional buck converter example: (a) schematic, (b) diode voltage and current waveforms.

20.1.1 Diode Switching

As discussed in Chapter 4, the reverse-recovery process usually leads to significant switching loss associated with the turn-off transition of diodes. This is often the largest single source of loss in a hard-switched converter. Normally, negligible loss is associated with the turn-on transition of power diodes. Three types of diode turn-off transition waveforms are commonly encountered in modern switching converters: hard switching, zero-current switching, and zero-voltage switching.

Figure 20.1 illustrates a conventional hard-switched PWM buck converter. The diode voltage and current waveforms $v(t)$ and $i(t)$ are also illustrated, with an exaggerated reverse recovery time. The output inductor current ripple is small. The diode turns off when the transistor is turned on; the reverse recovery process leads to a negative peak current of large amplitude. The diode must immediately support the full reverse voltage V_g , and hence both $v(t)$ and $i(t)$ must change with large slopes during reverse recovery. As described in Section 4.3.2, hard switching of the diode induces energy loss W_D in the transistor, given approximately by

$$W_D = V_g Q_r + t_r V_g I \quad (20.1)$$

where Q_r is the diode recovered charge and t_r is the reverse recovery time, both taken to be positive quantities. The recovered charge is relatively large because the slope di/dt is large during the turn-off transition. The resonant circuit formed by the diode output capacitance C_j and the diode package and other wiring inductances leads to ringing at the end of the reverse recovery time.

Figure 20.2 illustrates zero-current switching at the turn-off transition of a diode. The converter example is a quasi-resonant zero-voltage switching buck converter (see Section 20.3.1). The output inductor current ripple is again small. However, tank inductor L_r is now connected in series with the diode. The resulting diode current waveform $i(t)$ changes with a limited slope as shown. The diode reverse-recovery process commences when $i(t)$ passes through zero and becomes negative. The negative $i(t)$ actively removes stored charge from the diode; during this reverse recovery time, the diode remains forward-biased. When the stored charge is removed, then the diode voltage must rapidly change to $-V_g$. As described in Section 4.3.3, energy W_D is stored in inductor L_r at the end of the reverse recovery time, given by

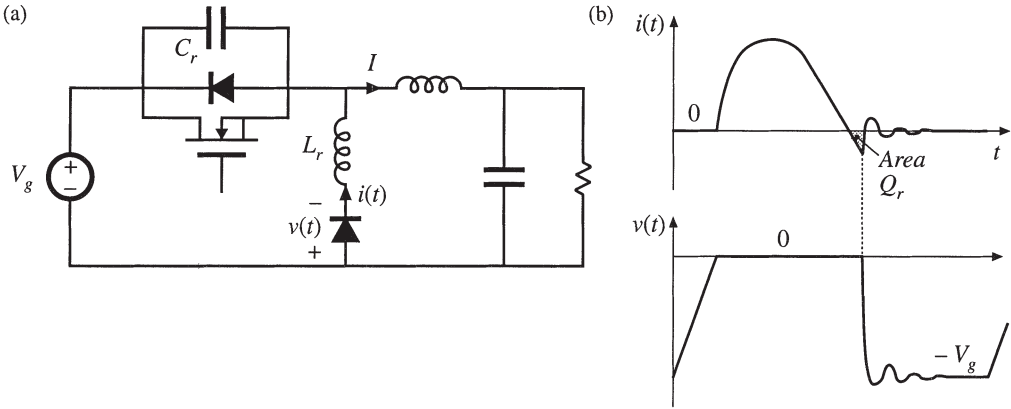


Fig. 20.2 Zero-current switching at the turn-off transition of a diode, ZVS quasi-resonant buck converter example: (a) converter schematic, (b) diode voltage and current waveforms.

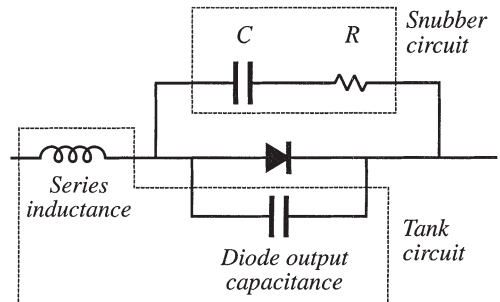
$$W_D = V_g Q_r \quad (20.2)$$

The resonant circuit formed by L_r and the diode output capacitance C_j then cause this energy to be circulated between L_r and C_j . This energy is eventually dissipated by parasitic resistive elements in the circuit, and hence is lost. Since Eqs. (20.1) and (20.2) are similar in form, the switching losses induced by the reverse-recovery processes of diodes operating with hard switching and with zero-current switching are similar in magnitude. Zero-current switching may lead to somewhat lower loss because the reduced di/dt leads to less recovered charge Q_r . Zero-current switching of diodes also typically leads to increased peak inverse diode voltage during the ringing of L_r and C_j , because of the relatively large value of L_r .

When a diode operates with hard switching or zero-current switching, and when substantial inductance is present in series with the diode, then significant ringing is observed in the diode voltage waveform. A resonant circuit, comprised of the series inductance and the diode output capacitance, is excited by the diode reverse recovery process, and the resulting ringing voltage can be of large enough magnitude to lead to breakdown and failure of the diode. A common example is the diodes on the secondary side of a hard-switched transformer-isolated converter; the resonant circuit is then formed by the transformer leakage inductance and the diode output capacitance. Other examples are the circuits of Figs. 20.2 and 20.36, in which the series inductance is a discrete tank inductor.

A simple snubber circuit that is often used to protect the diode from excessive reverse voltage is

Fig. 20.3 A dissipative snubber circuit, for protection of a diode from excessive voltage caused by ringing.



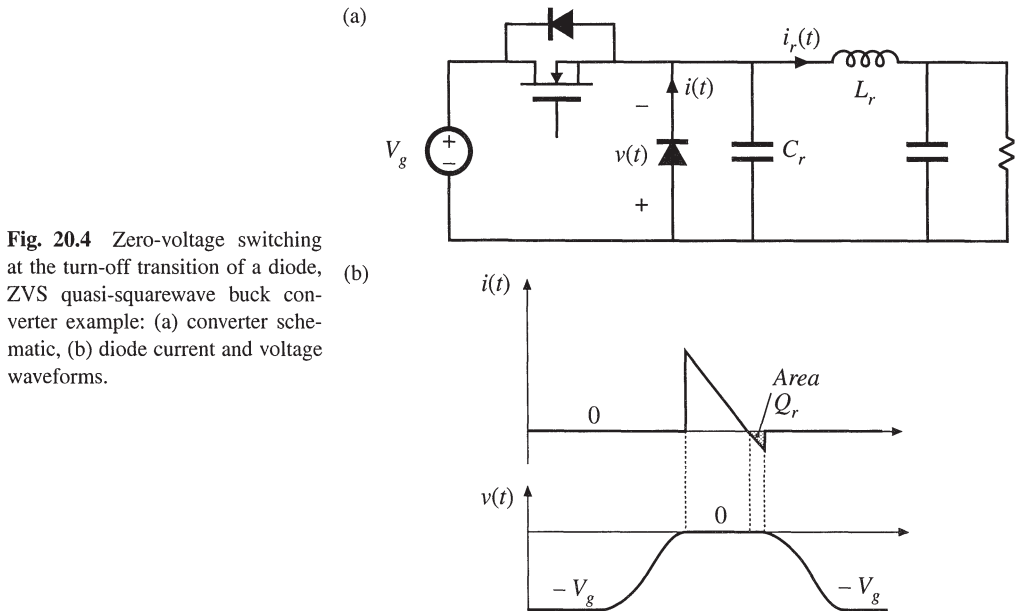


Fig. 20.4 Zero-voltage switching at the turn-off transition of a diode, ZVS quasi-square wave buck converter example: (a) converter schematic, (b) diode current and voltage waveforms.

illustrated in Fig. 20.3. Resistor R damps the ringing of the resonant circuit. Capacitor C prevents the off-state voltage of the diode from causing excessive power loss in R . Nonetheless, the energy consumed by R per switching period is typically greater than Eqs. (20.1) or (20.2).

Figure 20.4 illustrates zero-voltage switching at the turn-off transition of a diode. The figure illustrates the example of a zero-voltage switching quasi-square wave buck converter, discussed in Section 20.3.3. The output inductor L_r of this converter assumes the role of the tank inductor, and exhibits large current ripple that causes the current $i_r(t)$ to reverse polarity. While the diode conducts, its current $i(t)$ is equal to $i_r(t)$. When $i_r(t)$ becomes negative, the diode continues to conduct until its stored charge Q_r has been removed. The diode then becomes reverse-biased, and $i_r(t)$ flows through capacitor C_r and the diode output capacitance C_j . The diode voltage and current both change with limited slope in this type of switching, and the loss induced by the diode reverse-recovery process is negligible because the waveforms are not significantly damped by parasitic resistances in the circuit, and because the peak currents during reverse recovery are relatively low. The diode stored charge and diode output capacitance both behave as an effective nonlinear capacitor that can be combined with (or replace) tank capacitor C_r . Snubber circuits such as Fig. 20.3 are not necessary when the diode operates with zero-voltage switching.

Thus, zero-voltage switching at the turn-off transition of a diode is the preferred approach, that leads to minimum switching loss. Zero-current switching at the turn-off transition can be problematic, because of the high peak inverse voltage induced across the diode by ringing.

20.1.2 MOSFET Switching

The switching loss mechanisms typically encountered by a MOSFET in a hard-switched converter are discussed in Chapter 4, and typical MOSFET voltage and current waveforms are illustrated in Fig. 20.5. The most significant components of switching loss in the MOSFET of this circuit are: (1) the loss

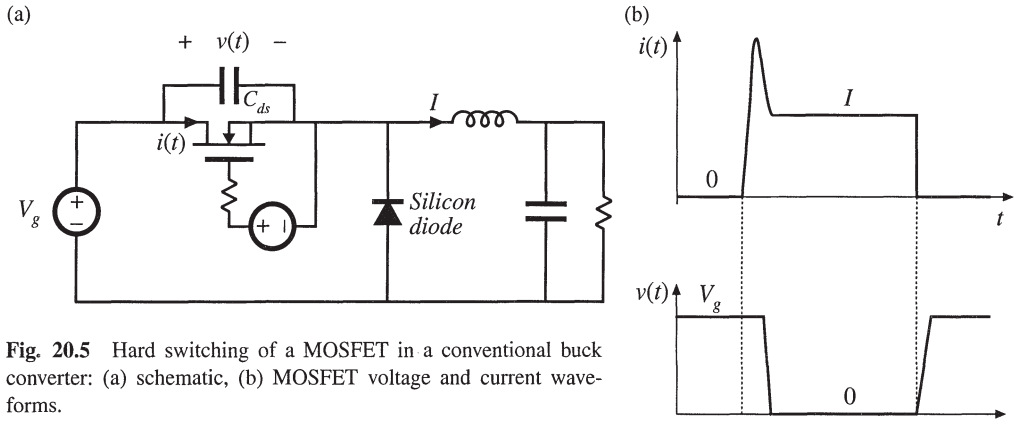


Fig. 20.5 Hard switching of a MOSFET in a conventional buck converter: (a) schematic, (b) MOSFET voltage and current waveforms.

induced by the diode reverse recovery process, and (2) the loss of the energy stored in the MOSFET output capacitance C_{ds} . Both loss mechanisms occur during the MOSFET turn-on process.

In the hard-switched circuit of Fig. 20.5, there is essentially no switching loss incurred during the MOSFET turn-off transition. This occurs because of the substantial output capacitance C_{ds} of the MOSFET. This capacitance holds the voltage $v(t)$ close to zero while the MOSFET turns off, so that the turn-off switching loss is very small. After the MOSFET has turned off, the output inductor current I flows through C_{ds} . The voltage $v(t)$ then increases until $v = V_g$ and the diode becomes forward biased.

However, when the MOSFET turns on, a high peak current flows through the MOSFET channel, induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode. This leads to substantial energy loss during the hard-switched turn-on transition of the MOSFET.

When a MOSFET (or other transistor) operates with hard switching, and when substantial inductance is present in series with the MOSFET, then significant ringing is observed in the MOSFET voltage waveform. A resonant circuit, composed of the MOSFET output capacitance and the series inductance, is excited when the MOSFET turns off, and the resulting ringing voltage can be of large enough magnitude to lead to breakdown and failure of the MOSFET. A common example is the MOS-

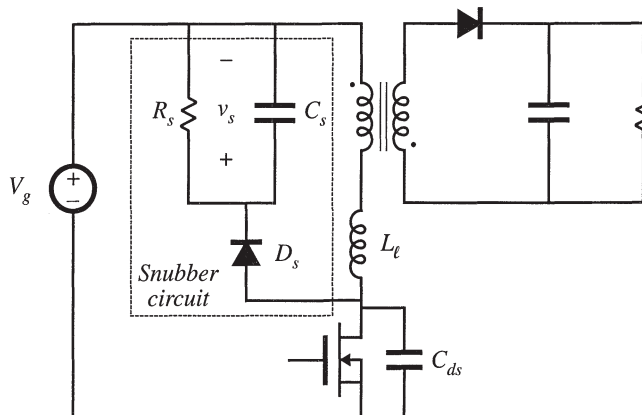


Fig. 20.6 Insertion of a dissipative voltage-clamped snubber circuit into a flyback converter. The MOSFET voltage is clamped to a peak value of $(V_g + v_s)$.

FET of the flyback converter, in which series inductance is introduced by the transformer leakage inductance. An R - C snubber circuit, similar to that used for the diode in Fig. 20.3, can be used to protect the MOSFET from damage caused by excessive applied voltage. Another common snubber circuit is illustrated in Fig. 20.6. When the MOSFET turns off, the current flowing in the transformer leakage inductance L_ℓ begins to flow into the MOSFET capacitance C_{ds} . These parasitic elements then ring, and the peak transistor voltage can significantly exceed the ideal value of $(D/D')V_g$.

One simple way to design the snubber circuit of Fig. 20.6 is to choose the capacitance C_s to be large, so that $v_s(t) \approx V_s$ contains negligible switching ripple. The resistance R_s is then chosen so that the power consumption of R_s at the desired voltage V_s is equal to the switching loss caused by L_ℓ :

$$\frac{V_s^2}{R_s} \approx \frac{1}{2} Li^2 f_s \quad (20.3)$$

The current i is equal to the current flowing in the transformer primary just before the MOSFET is turned off. This approximate expression is useful for obtaining a first estimate of how to choose R_s to obtain a given desired V_s .

Zero-current switching does not affect the switching loss that arises from the MOSFET output capacitance, and it may or may not influence the loss induced by diode reverse recovery. In consequence, zero-current switching is of little or no help in improving the efficiency of converters that employ MOSFETs.

Zero-voltage switching can prevent both diode reverse recovery and semiconductor output capacitances from inducing switching loss in MOSFETs. An example is illustrated in Fig. 20.7. This circuit is again a zero-voltage switching quasi-squarewave example, discussed in Section 20.3.3. The converter circuit naturally discharges the energy stored in C_{ds} , before the MOSFET is switched on. When the drain-to-source voltage $v(t)$ passes through zero, the MOSFET body diode becomes forward-biased. The MOSFET can then be turned on at zero voltage, without incurring turn-on switching loss. The MOSFET turn-on transition must be completed before the tank inductor current $i_r(t)$ becomes positive. The MOSFET turn-off transition is also lossless, and is similar to the hard-switched case discussed above.

Zero-voltage switching of a MOSFET also causes its body diode to operate with zero-voltage switching. This can eliminate the switching loss associated with reverse recovery of the slow body diode, and improve the reliability of circuits that forward-bias this diode.

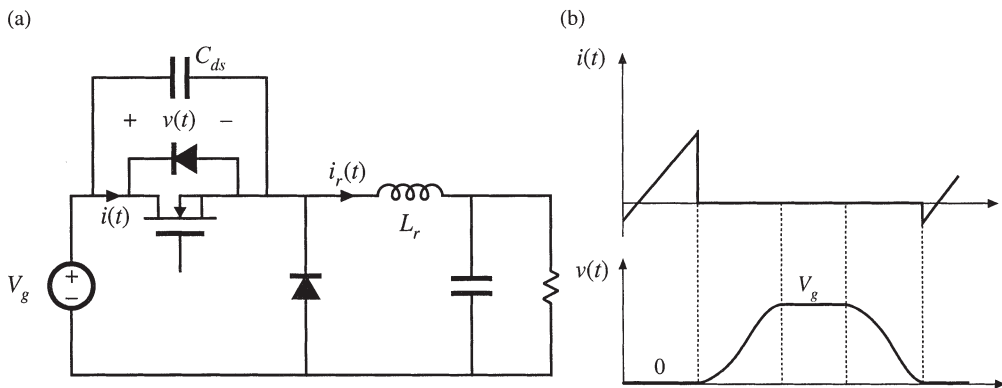


Fig. 20.7 Zero-voltage switching of a MOSFET, ZVS quasi-squarewave buck converter example. The MOSFET, its body diode, and its output capacitance C_{ds} are illustrated. (a) converter schematic, (b) MOSFET voltage and current waveforms.

Zero-voltage switching can also eliminate the overvoltage problems associated with transformer leakage inductances, removing the need for voltage-clamped snubber circuits such as in Fig. 20.6. An example is discussed in Section 20.4.2.

20.1.3 IGBT Switching

Like the MOSFET, the IGBT typically encounters substantial switching loss during its turn-on transition, induced by the reverse-recovery process of diodes within the converter. In addition, the IGBT exhibits significant switching loss during its turn-off transition, caused by the current tailing phenomenon (*see* Chapter 4).

Zero-voltage switching has been successfully applied to IGBT circuits—an example is the auxiliary resonant commutation circuit discussed in Section 20.4.3. This has the principal advantage of eliminating the switching loss caused by diode reverse recovery. Although zero-voltage switching can reduce the loss incurred during the turn-off transition, it is difficult to eliminate the substantial loss caused by current tailing.

20.2 THE ZERO-CURRENT SWITCHING QUASI-RESONANT SWITCH CELL

Figure 20.8(a) illustrates a generic buck converter, consisting of a switch cell cascaded by an L – C low-pass filter. When the switch cell is realized as in Fig. 20.8(b), then a conventional PWM buck converter is obtained. Figures 20.8(b) and (c) illustrate two other possible realizations of the switch cell: the half-wave and full-wave zero-current-switching quasi-resonant switches [1, 2]. In these switch cells, a resonant tank capacitor C_r is placed in parallel with diode D_2 , while resonant tank capacitor L_r is placed in series with the active transistor element.

Both resonant switch cells require a two-quadrant SPST switch. In the half-wave switch cell of Fig. 20.8(c), diode D_1 is added in series with transistor Q_1 . This causes the Q_1 – D_1 SPST switch to turn off at the first zero crossing of the tank inductor current $i_1(t)$. In the full-wave switch cell of Fig. 20.8(d), antiparallel diode D_1 allows bidirectional flow of the tank inductor current $i_1(t)$. With this switch network, the Q_1 – D_1 SPST switch is normally turned off at the second zero-crossing of the $i_1(t)$ waveform. In either switch cell, the L_r and C_r elements are relatively small in value, such that their resonant frequency f_0 is greater than the switching frequency f_s , where

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} = \frac{\omega_0}{2\pi} \quad (20.4)$$

In the analysis which follows, it is assumed that the converter filter element values L and C have negligible switching ripple. Hence, the switch cell terminal waveforms $v_1(t)$ and $i_2(t)$ are well-approximated by their average values:

$$\begin{aligned} i_2(t) &\approx \langle i_2(t) \rangle_{T_s} \\ v_1(t) &\approx \langle v_1(t) \rangle_{T_s} \end{aligned} \quad (20.5)$$

with the average defined as in Eq. (7.3). In steady-state, we can further approximate $v_1(t)$ and $i_2(t)$ by their dc components V_1 and I_2 :

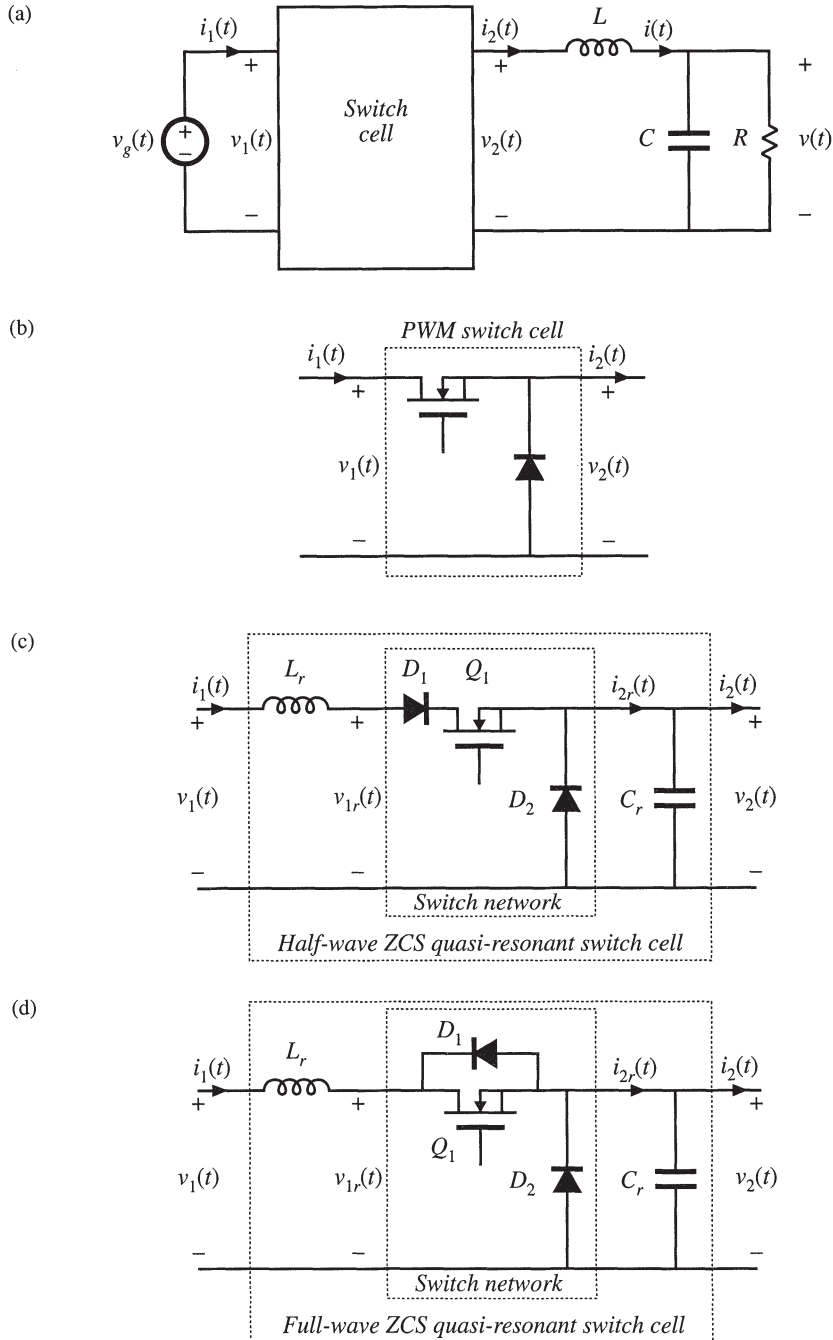


Fig. 20.8 Implementation of the switch cell in a buck converter: (a) buck converter, with arbitrary switch cell; (b) PWM switch cell; (c) half-wave ZCS quasi-resonant switch cell; (d) full-wave ZCS quasi-resonant switch cell.

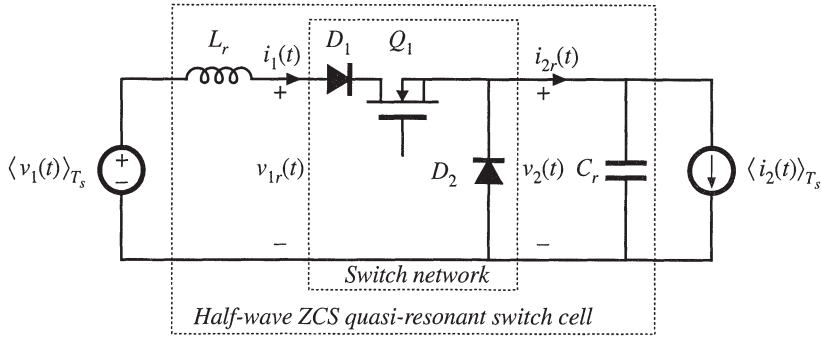


Fig. 20.9 The half-wave ZCS quasi-resonant switch cell, driven by the terminal quantities $\langle v_1(t) \rangle_{T_s}$ and $\langle i_2(t) \rangle_{T_s}$.

$$\begin{aligned} i_2(t) &\approx I_2 \\ v_1(t) &\approx V_1 \end{aligned} \quad (20.6)$$

Thus, the small-ripple approximation is employed for the converter filter elements, as usual.

To understand the operation of the half-wave ZCS quasi-resonant switch cell, we can solve the simplified circuit illustrated in Fig. 20.9. In accordance with the averaged switch modeling approach of Sections 7.4 and 11.1, it is desired to determine the average terminal waveforms $\langle v_2(t) \rangle_{T_s}$ and $\langle i_1(t) \rangle_{T_s}$, as functions of the applied quantities $\langle v_1(t) \rangle_{T_s}$ and $\langle i_2(t) \rangle_{T_s}$. The switch conversion ratio μ is then given by

$$\mu = \frac{\langle v_2(t) \rangle_{T_s}}{\langle v_{1r}(t) \rangle_{T_s}} = \frac{\langle i_1(t) \rangle_{T_s}}{\langle i_2(t) \rangle_{T_s}} \quad (20.7)$$

In steady state, we can write

$$\mu = \frac{V_2}{V_1} = \frac{I_1}{I_2} \quad (20.8)$$

The steady-state analysis of this section employs Eq. (20.8) to determine μ .

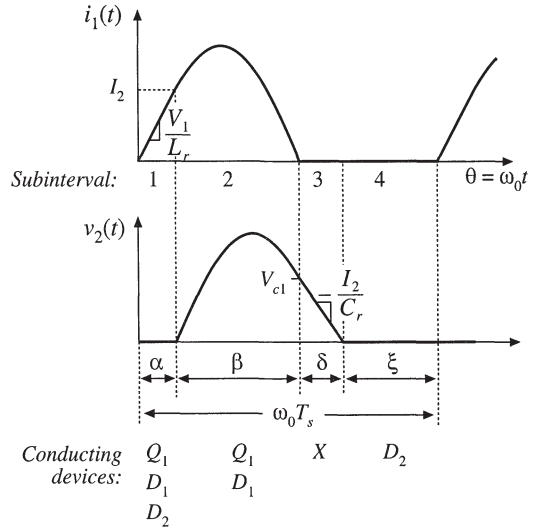
20.2.1 Waveforms of the Half-Wave ZCS Quasi-Resonant Switch Cell

Typical waveforms of the half-wave cell of Fig. 20.9 are illustrated in Fig. 20.10. Each switching period consists of four subintervals as shown, having angular lengths α , β , δ , and ξ . The switching period begins when the controller turns on transistor Q_1 . The initial values of the tank inductor current $i_1(t)$ and tank capacitor voltage $v_2(t)$ are zero. During subinterval 1, all three semiconductor devices conduct. Diode D_2 is forward-biased because $i_1(t)$ is less than I_2 . In consequence, during subinterval 1 the switch cell reduces to the circuit of Fig. 20.11.

The slope of the inductor current is given by

$$\frac{di_1(t)}{dt} = \frac{V_1}{L_r} \quad (20.9)$$

Fig. 20.10 Tank inductor current and capacitor voltage waveforms, for the half-wave ZCS quasi-resonant switch of Fig. 20.9.



with the initial condition $i_1(0) = 0$. The solution is

$$i_1(t) = \frac{V_1}{L_r} t = \omega_0 t \frac{V_1}{R_0} \quad (20.10)$$

where the tank characteristic impedance R_0 is defined as

$$R_0 = \sqrt{\frac{L_r}{C_r}} \quad (20.11)$$

It is convenient to express the waveforms in terms of the angle $\theta = \omega_0 t$, instead of time t . At the end of subinterval 1, $\omega_0 t = \alpha$. The subinterval ends when diode D_2 becomes reverse-biased. Since the diode D_2 current is equal to $I_2 - i_1(t)$, this occurs when $i_1(t) = I_2$. Hence, we can write

$$i_1(\alpha) = \alpha \frac{V_1}{R_0} = I_2 \quad (20.12)$$

Solution for α yields

$$\alpha = \frac{I_2 R_0}{V_1} \quad (20.13)$$

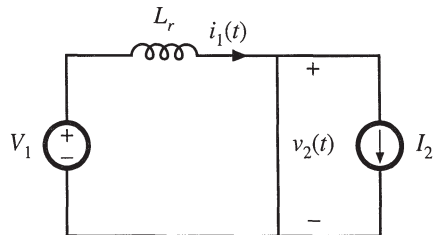
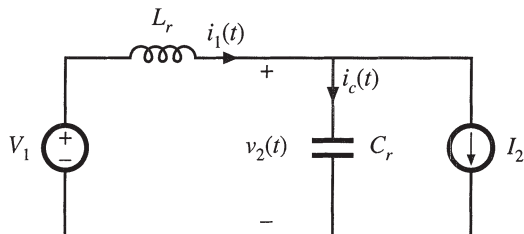


Fig. 20.11 Circuit of the switch network during subinterval 1.

Fig. 20.12 Circuit of the switch network during subinterval 2.



During subinterval 2, transistor Q_1 and diode D_1 conduct, while diode D_2 is reverse-biased. The switch network then becomes the circuit illustrated in Fig. 20.12. The resonant L_r - C_r tank network is excited by the constant sources V_1 and I_2 . The network equations are

$$\begin{aligned} L_r \frac{di_1(\omega_0 t)}{dt} &= V_1 - v_2(\omega_0 t) \\ C_r \frac{dv_2(\omega_0 t)}{dt} &= i_1(\omega_0 t) - I_2 \end{aligned} \quad (20.14)$$

with the initial conditions

$$\begin{aligned} v_2(\alpha) &= 0 \\ i_1(\alpha) &= I_2 \end{aligned} \quad (20.15)$$

The solution is

$$\begin{aligned} i_1(\omega_0 t) &= I_2 + \frac{V_1}{R_0} \sin(\omega_0 t - \alpha) \\ v_2(\omega_0 t) &= V_1 \left(1 - \cos(\omega_0 t - \alpha) \right) \end{aligned} \quad (20.16)$$

The tank inductor current rises to a peak value given by

$$I_{1pk} = I_2 + \frac{V_1}{R_0} \quad (20.17)$$

The subinterval ends at the first zero crossing of $i_1(t)$. If we denote the angular length of the subinterval as β , then we can write

$$i_1(\alpha + \beta) = I_2 + \frac{V_1}{R_0} \sin(\beta) = 0 \quad (20.18)$$

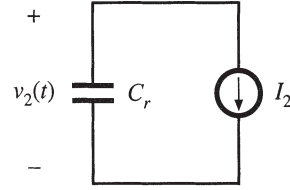
Solution for $\sin(\beta)$ yields

$$\sin(\beta) = -\frac{I_2 R_0}{V_1} \quad (20.19)$$

Care must be employed when solving Eq. (20.19) for the angle β . It can be observed from Fig. 20.10 that the angle β is greater than π . The correct branch of the arcsine function must be selected, as follows:

$$\beta = \pi + \sin^{-1} \left(\frac{I_2 R_0}{V_1} \right) \quad (20.20)$$

Fig. 20.13 Circuit of the switch network during subinterval 3.



where

$$-\frac{\pi}{2} < \sin^{-1}(x) \leq \frac{\pi}{2}$$

Note that the inequality

$$I_2 < \frac{V_1}{R_0} \quad (20.21)$$

must be satisfied; otherwise, there is no solution to Eq. (20.19). At excessive load currents, where Eq. (20.21) is not satisfied, the tank inductor current never reaches zero, and the transistor does not switch off at zero current.

The tank capacitor voltage at the end of subinterval 2 is found by evaluation of Eq. (20.16) at $\omega_0 t = (\alpha + \beta)$. The $\cos(\beta)$ term can be expressed as

$$\cos(\beta) = -\sqrt{1 - \sin^2(\beta)} = -\sqrt{1 - \left(\frac{I_2 R_0}{V_1}\right)^2} \quad (20.22)$$

Substitution of Eq. (20.22) into Eq. (20.16) leads to

$$v_2(\alpha + \beta) = V_{c1} = V_1 \left(1 + \sqrt{1 - \left(\frac{I_2 R_0}{V_1}\right)^2} \right) \quad (20.23)$$

At the end of subinterval 2, diode D_1 becomes reverse-biased. Transistor Q_1 can then be switched off at zero current.

During subinterval 3, all semiconductor devices are off, and the switch cell reduces to the circuit of Fig. 20.13. The tank capacitor C_r is discharged by the filter inductor current I_2 . Hence, the tank capacitor voltage v_2 decreases linearly to zero. The circuit equations are

$$\begin{aligned} C_r \frac{dv_2(\omega_0 t)}{dt} &= -I_2 \\ v_2(\alpha + \beta) &= V_{c1} \end{aligned} \quad (20.24)$$

The solution is

$$v_2(\omega_0 t) = V_{c1} - I_2 R_0 (\omega_0 t - \alpha - \beta) \quad (20.25)$$

Subinterval 3 ends when the tank capacitor voltage reaches zero. Diode D_2 then becomes forward-biased. Hence, we can write

$$v_2(\alpha + \beta + \delta) = V_{c1} - I_2 R_0 \delta = 0 \quad (20.26)$$

where δ is the angular length of subinterval 3. Solution for δ yields

$$\delta = \frac{V_{c1}}{I_2 R_0} = \frac{V_1}{I_2 R_0} \left(1 - \sqrt{1 - \left(\frac{I_2 R_0}{V_1} \right)^2} \right) \quad (20.27)$$

Subinterval 4, of angular length ξ , is identical to the diode conduction subinterval of the conventional PWM switch network. Diode D_2 conducts the filter inductor current I_2 , and the tank capacitor voltage v_2 is equal to zero. Transistor Q_1 is off, and the input current i_1 is equal to zero.

The angular length of the switching period is

$$\omega_0 T_s = \alpha + \beta + \delta + \xi = \frac{2\pi f_0}{f_s} = \frac{2\pi}{F} \quad (20.28)$$

where

$$F = \frac{f_s}{f_0} \quad (20.29)$$

Quasi-resonant switch networks are usually controlled by variation of the switching frequency f_s or, in normalized terms, by variation of F . Note that the interval lengths α , β , and δ are determined by the response of the tank network. Hence, control of the switching frequency is equivalent to control of the fourth subinterval length ξ . The subinterval length ξ must be positive, and hence, the minimum switching period is limited as follows:

$$\omega_0 T_s \geq \alpha + \beta + \delta \quad (20.30)$$

Substitution of Eqs. (20.13), (20.20), and (20.27) into Eq. (20.30) yields

$$\frac{2\pi}{F} \geq \frac{I_2 R_0}{V_1} + \pi + \sin^{-1} \left(\frac{I_2 R_0}{V_1} \right) + \frac{V_1}{I_2 R_0} \left(1 - \sqrt{1 - \left(\frac{I_2 R_0}{V_1} \right)^2} \right) \quad (20.31)$$

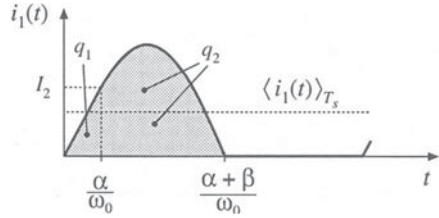
This expression limits the maximum switching frequency, or maximum F , of the half-wave ZCS quasi-resonant switch cell.

20.2.2 The Average Terminal Waveforms

It is now desired to solve for the power processing function performed by the switch network. The switch conversion ratio μ is a generalization of the duty cycle d . It expresses how a resonant switch network controls the average voltages and currents of a converter. In our buck converter example, we can define μ as the ratio of $\langle v_2(t) \rangle_{T_s}$ to $\langle v_1(t) \rangle_{T_s}$, or equivalently, the ratio of $\langle i_1(t) \rangle_{T_s}$ to $\langle i_2(t) \rangle_{T_s}$. In a hard-switched PWM network, this ratio is equal to the duty cycle d . Hence, analytical results derived for hard-switched PWM converters can be adapted to quasi-resonant converters, simply by replacing d with μ . In this section, we derive an expression for μ , by averaging the terminal waveforms of the switch network.

The switch input current waveform $i_1(t)$ of Fig. 20.10 is reproduced in Fig. 20.14. The average switch input current is given by

Fig. 20.14 Input current waveform $i_1(t)$, and the areas q_1 and q_2 during subintervals 1 and 2 respectively.



$$\langle i_1(t) \rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} i_1(t) dt = \frac{q_1 + q_2}{T_s} \quad (20.32)$$

The charge quantities q_1 and q_2 are the areas under the $i_1(t)$ waveform during the first and second subintervals, respectively. The charge q_1 is given by the triangle area formula

$$q_1 = \int_0^{\frac{\alpha}{\omega_0}} i_1(t) dt = \frac{1}{2} \left(\frac{\alpha}{\omega_0} \right) (I_2) \quad (20.33)$$

The time α/ω_0 is the length of subinterval 1. The charge q_2 is

$$q_2 = \int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_1(t) dt \quad (20.34)$$

According to Fig. 20.12, during subinterval 2 the current $i_1(t)$ can be related to the tank capacitor current $i_C(t)$ and the switch output current I_2 by the node equation

$$i_1(t) = i_C(t) + I_2 \quad (20.35)$$

Substitution of Eq. (20.35) into Eq. (20.34) leads to

$$q_2 = \int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_C(t) dt + \int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} I_2 dt \quad (20.36)$$

Both integrals in Eq. (20.36) can easily be evaluated, as follows. Since the second term involves the integral of the constant current I_2 , this term is

$$\int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} I_2 dt = I_2 \frac{\beta}{\omega_0} \quad (20.37)$$

The first term in Eq. (20.36) involves the integral of the capacitor current over subinterval 2. Hence, this term is equal to the change in capacitor charge over the second subinterval:

$$\int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_C(t) dt = C \left(v_2 \left(\frac{\alpha+\beta}{\omega_0} \right) - v_2 \left(\frac{\alpha}{\omega_0} \right) \right) \quad (20.38)$$

(recall that $\Delta q = C\Delta v$ in a capacitor). During the second subinterval, the tank capacitor voltage is initially zero, and has a final value of V_{c1} . Hence, Eq. (20.38) reduces to

$$\int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_C(t) dt = C(V_{c1} - 0) = CV_{c1} \quad (20.39)$$

Substitution of Eqs. (20.37) and (20.39) into Eq. (20.36) leads to the following expression for q_2 :

$$q_2 = CV_{c1} + I_2 \frac{\beta}{\omega_0} \quad (20.40)$$

Equations (20.33) and (20.40) can now be inserted into Eq. (20.32), to obtain the following expression for the switch input current:

$$\langle i_1(t) \rangle_{T_s} = \frac{\alpha I_2}{2\omega_0 T_s} + \frac{CV_{c1}}{T_s} + \frac{\beta I_2}{\omega_0 T_s} \quad (20.41)$$

Substitution of Eq. (20.41) into (20.8) leads to the following expression for the switch conversion ratio:

$$\mu = \frac{\langle i_1(t) \rangle_{T_s}}{I_2} = \frac{\alpha}{2\omega_0 T_s} + \frac{CV_{c1}}{I_2 T_s} + \frac{\beta}{\omega_0 T_s} \quad (20.42)$$

Finally, the quantities α , β , and V_{c1} can be eliminated, using Eqs. (20.13), (20.20), (20.23). The result is

$$\mu = F \frac{1}{2\pi} \left[\frac{1}{2} J_s + \pi + \sin^{-1}(J_s) + \frac{1}{J_s} \left(1 + \sqrt{1 - J_s^2} \right) \right] \quad (20.43)$$

where

$$J_s = \frac{I_2 R_0}{V_1} \quad (20.44)$$

Equation (20.43) is of the form

$$\mu = F P_{\frac{1}{2}}(J_s) \quad (20.45)$$

where

$$P_{\frac{1}{2}}(J_s) = \frac{1}{2\pi} \left[\frac{1}{2} J_s + \pi + \sin^{-1}(J_s) + \frac{1}{J_s} \left(1 + \sqrt{1 - J_s^2} \right) \right] \quad (20.46)$$

Thus, the switch conversion ratio μ is directly controllable by variation of the switching frequency, through F . The switch conversion ratio is also a function of the applied terminal voltage V_1 and current I_2 , via J_s . The function $P_{\frac{1}{2}}(J_s)$ is sketched in Fig. 20.15. The switch conversion ratio μ is sketched in Fig. 20.16, for various values of F and J_s . These characteristics are similar in shape to the function $P(J_s)$, and are simply scaled by the factor F . It can be seen that the conversion ratio μ is a strong function

Fig. 20.15 The function $P_{\frac{1}{2}}(J_s)$.

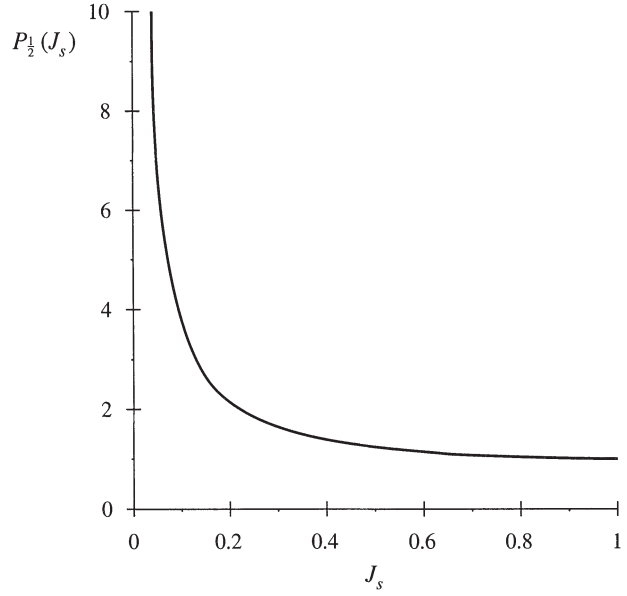
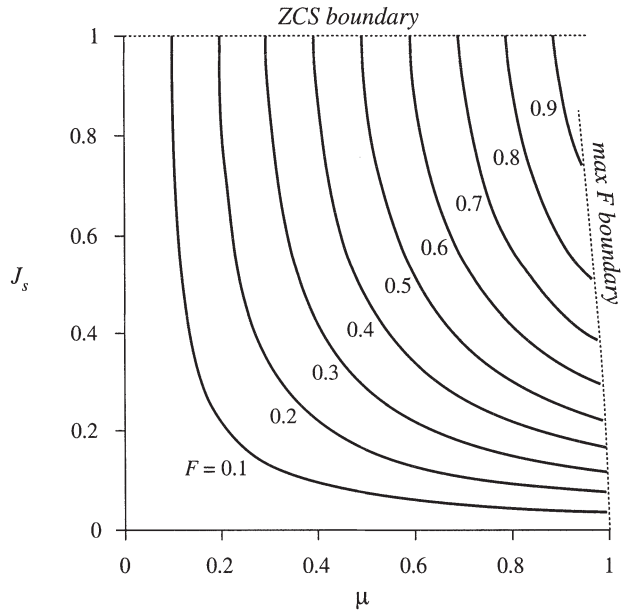


Fig. 20.16 Characteristics of the half-wave ZCS quasi-resonant switch.



of the current I_2 , via J_s . The characteristics end at $J_s = 1$; according to Eq. (20.31), the zero current switching property is lost when $J_s > 1$. The characteristics also end at the maximum switching frequency limit given by Eq. (20.31). This expression can be simplified by use of Eq. (20.43), to express the limit in terms of μ as follows:

$$\mu \leq 1 - \frac{J_s F}{4\pi} \quad (20.47)$$

The switch conversion ratio μ is thus limited to a value slightly less than 1.

The averaged waveforms of converters containing half-wave ZCS quasi-resonant switches can now be determined. The results of the analysis of PWM converters operating in the continuous conduction mode can be directly adapted to the related quasi-resonant converters, simply by replacing the duty cycle d with the switch conversion ratio μ . For the buck converter example, the conversion ratio is

$$M = \frac{V}{V_g} = \mu \quad (20.48)$$

This result could also be derived by use of the principle of inductor volt-second balance. The average voltage across the filter inductor is $(\mu V_g - V)$. Upon equating this voltage to zero, we obtain Eq. (20.48).

In the buck converter, I_2 is equal to the load current I , while V_1 is equal to the converter input voltage V_g . Hence, the quantity J_s is

$$J_s = \frac{IR_0}{V_g} \quad (20.49)$$

Zero current switching occurs for

$$I \leq \frac{V_g}{R_0} \quad (20.50)$$

The output voltage can vary over the range

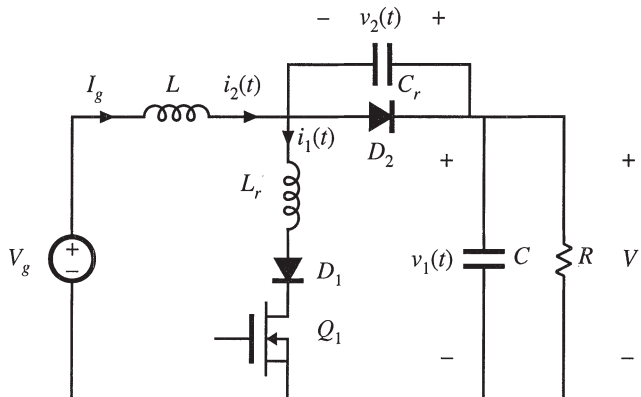
$$0 \leq V \leq V_g - \frac{FIR_0}{4\pi} \quad (20.51)$$

which nearly coincides with the PWM output voltage range $0 \leq V \leq V_g$.

A boost converter employing a half-wave ZCS quasi-resonant switch is illustrated in Fig. 20.17. The conversion ratio of the boost converter is given by

$$M = \frac{V}{V_g} = \frac{1}{1 - \mu} \quad (20.52)$$

Fig. 20.17 Boost converter containing a half-wave ZCS quasi-resonant switch.



The half-wave switch conversion ratio μ is again given by Eqs. (20.44) to (20.46). For the boost converter, the applied switch voltage V_1 is equal to the output voltage V , while the applied switch current I_2 is equal to the filter inductor current, or I_g . Hence, the quantity J_s is

$$J_s = \frac{I_2 R_0}{V_1} = \frac{I_g R_0}{V} \quad (20.53)$$

Also, the input current I_g of the boost converter is related to the load current I according to

$$I_g = \frac{I}{1-\mu} \quad (20.54)$$

Equations (20.52) to (20.54), in conjunction with Eqs. (20.44) to (20.46), describe the averaged waveforms of the half-wave quasi-resonant ZCS boost converter.

20.2.3 The Full-Wave ZCS Quasi-Resonant Switch Cell

The full-wave ZCS quasi-resonant switch cell is illustrated in Fig. 20.8(d). It differs from the half-wave cell in that elements D_1 and Q_1 are connected in antiparallel, to form a current-bidirectional two-quadrant switch. Typical tank inductor current and tank capacitor voltage waveforms are illustrated in Fig. 20.18. These waveforms are similar to those of the half-wave case, except that the Q_1/D_1 switch interrupts the tank inductor current $i_1(t)$ at its second zero-crossing. While $i_1(t)$ is negative, diode D_1 conducts, and transistor Q_1 can be turned off at zero current.

The analysis is nearly the same as for the half-wave case, with the exception of subinterval 2. The subinterval 2 angular length β and final voltage V_{c1} can be shown to be

$$\beta = \begin{cases} \pi + \sin^{-1}(J_s) & \text{(half wave)} \\ 2\pi - \sin^{-1}(J_s) & \text{(full wave)} \end{cases} \quad (20.55)$$

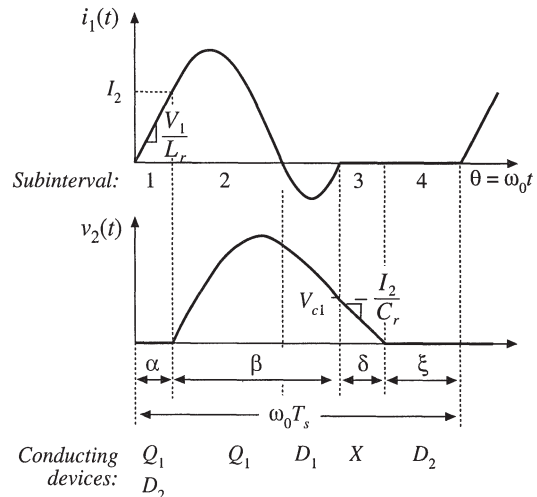
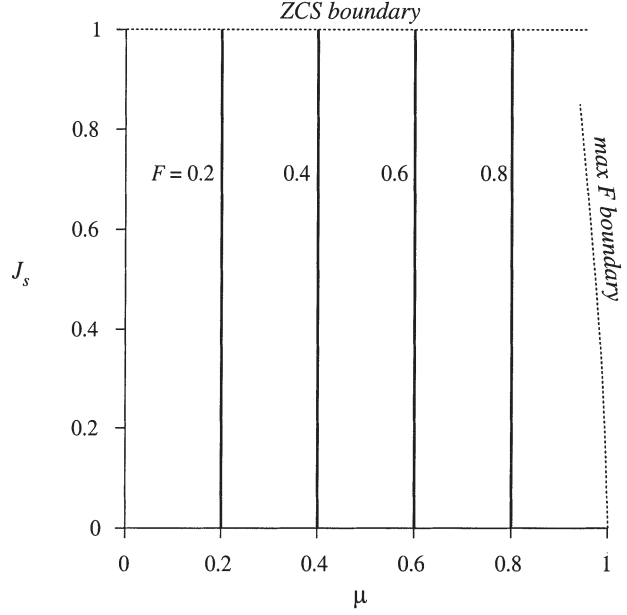


Fig. 20.18 Tank inductor current and capacitor voltage waveforms, for the full-wave ZCS quasi-resonant switch cell of Fig. 20.8(d).

Fig. 20.19 Characteristics of the full-wave ZCS quasi-resonant switch.



$$V_{c1} = \begin{cases} V_1 (1 + \sqrt{1 - J_s^2}) & \text{(half wave)} \\ V_1 (1 - \sqrt{1 - J_s^2}) & \text{(full wave)} \end{cases} \quad (20.56)$$

In either case, the switch conversion ratio μ is given by Eq. (20.42). For the full-wave switch, one obtains

$$\mu = F P_1(J_s) \quad (20.57)$$

where $P_1(J_s)$ is given by

$$P_1(J_s) = \frac{1}{2\pi} \left[\frac{1}{2} J_s + 2\pi - \sin^{-1}(J_s) + \frac{1}{J_s} (1 - \sqrt{1 - J_s^2}) \right] \quad (20.58)$$

In the full-wave case, $P_1(J_s)$ is essentially independent of J_s :

$$P_1(J_s) \approx 1 \quad (20.59)$$

The worst-case deviation of $P_1(J_s)$ from 1 occurs as J_s tends to 1, where $P_1(J_s)$ tends to 0.96. So $P_1(J_s)$ lies within 4% of unity for $0 < J_s < 1$. Hence, for the full-wave case, it is a good approximation to express the switch conversion ratio as

$$\mu \approx F = \frac{f_s}{f_0} \quad (20.60)$$

The full-wave quasi-resonant switch therefore exhibits voltage-source output characteristics, controllable

by F . Equations describing the average waveforms of CCM PWM converters can be adapted to apply to full-wave ZCS quasi-resonant converters, simply by replacing the duty cycle d with the normalized switching frequency F . The conversion ratios of full-wave quasi-resonant converters exhibit negligible dependence on the load current.

The variation of the switch conversion ratio μ with F and J_s is plotted in Fig. 20.19. For a typical voltage regulator application, the range of switching frequency variations is much smaller in the full-wave mode than in the half-wave mode, because μ does not depend on the load current. Variations in the load current do not induce the controller to significantly change the switching frequency.

20.3 RESONANT SWITCH TOPOLOGIES

So far, we have considered the zero-current-switching quasi-resonant switch cell, illustrated in Fig. 20.20. The ideal SPST switch is realized using a voltage-bidirectional or current-bidirectional two-quadrant switch, to obtain half-wave or full-wave ZCS quasi-resonant switch networks, respectively.

The resonant elements L_r and C_r can be moved to several different positions in the converter, without altering the basic switch properties. For example, Fig. 20.21 illustrates connection of the resonant tank capacitor C_r between the cathode of diode D_2 , and the converter output or input terminals. Although this may change the dc component of the tank capacitor voltage, the ac components of the tank capacitor voltage waveform are unchanged. Also, the terminal voltage waveform $v_2(t)$ is unchanged. The voltages $v_g(t)$ and $v(t)$ contain negligible high-frequency ac components, and hence the converter input and output terminal potentials can be considered to be at high-frequency ac ground.

A test to determine the topology of a resonant switch network is to replace all low-frequency filter inductors with open circuits, and to replace all dc sources and low-frequency filter capacitors with short circuits [13]. The elements of the resonant switch cell remain. In the case of the zero-current-switching quasi-resonant switch, the network of Fig. 20.22 is always obtained.

It can be seen from Fig. 20.22 that diode D_2 switches on and off at the zero crossings of the tank capacitor voltage $v_2(t)$, while the switch elements Q_1 and D_1 switch at the zero crossings of the tank inductor current $i_1(t)$. Zero voltage switching of diode D_2 is highly advantageous, because it essentially eliminates the switching loss caused by the recovered charge and output capacitance of diode D_2 . Zero current switching of Q_1 and D_1 can be used to advantage when Q_1 is realized by an SCR or IGBT. However, in high-frequency converters employing MOSFETs, zero current switching of Q_1 and D_1 is generally a poor choice. Significant switching loss due to the output capacitances of Q_1 and D_1 may be observed. In addition, in the full-wave case, the recovered charge of diode D_1 leads to significant ringing

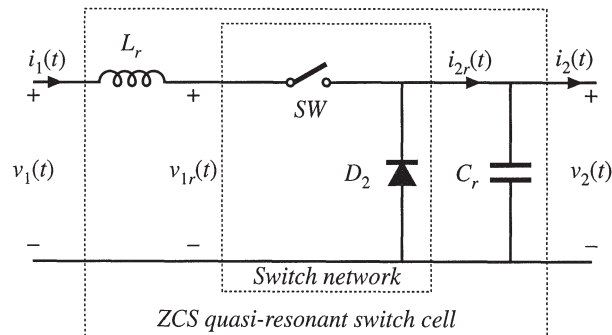


Fig. 20.20 Basic ZCS quasi-resonant switch cell.

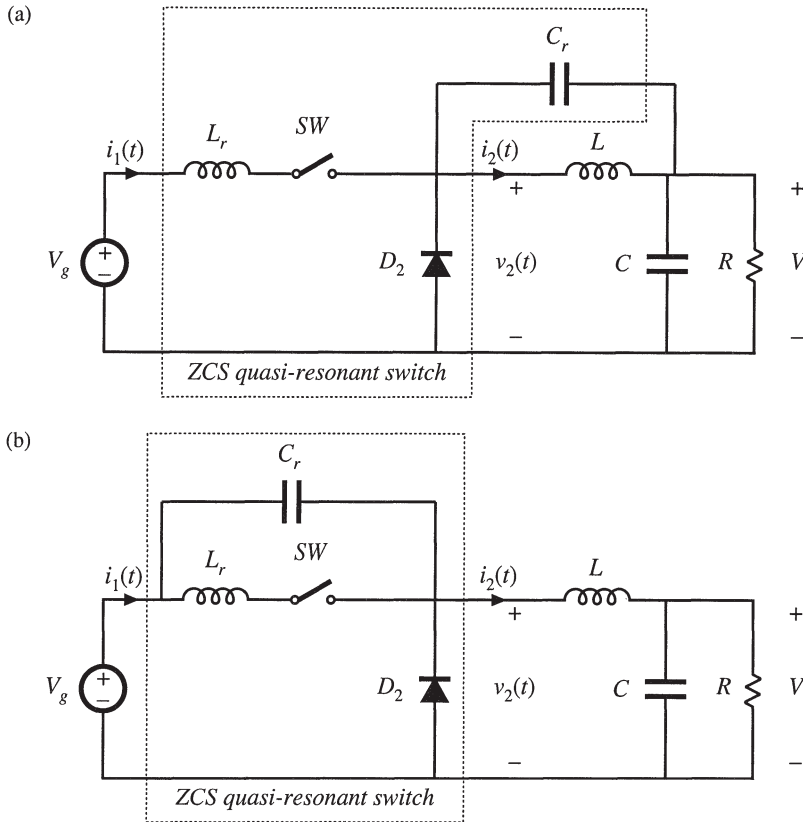
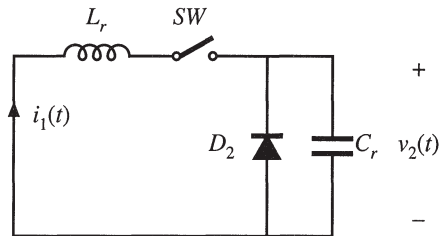


Fig. 20.21 Connection of the tank capacitor of the ZCS quasi-resonant cell to other points at ac ground: (a) connection to the dc output, (b) connection to the dc input. In each case, the ac components of the waveforms are unchanged.

Fig. 20.22 Elimination of converter low-frequency elements causes the ZCS quasi-resonant switch cell to reduce to this network.



and switching loss at the end of subinterval 2 [3].

The ZCS quasi-resonant switch exhibits increased conduction loss, relative to an equivalent PWM switch, because the peak transistor current is increased. The peak transistor current is given by Eq. (20.17); since $J_s \leq 1$, the peak current is $I_{1pk} \geq 2I_2$. In addition, the full-wave ZCS switch exhibits poor efficiency at light load, owing to the conduction loss caused by circulating tank currents. The half-wave ZCS switch exhibits additional conduction loss due to the added forward voltage drop of diode D_1 . The peak transistor voltage is V_1 , which is identical to the PWM case.

20.3.1 The Zero-Voltage-Switching Quasi-Resonant Switch

The resonant switch network illustrated in Fig. 20.23 is the dual of the network of Fig. 20.22. This network is known as the zero-voltage-switching quasi-resonant switch [4]. Since the tank capacitor C_r appears in parallel with the SPST switch, the elements Q_1 and D_1 used to realize the SPST switch turn on and off at zero voltage. The tank inductor L_r is effectively in series with diode D_2 , and hence diode D_2 switches at zero current. Converters containing ZVS quasi-resonant switches can be realized in a number of ways. The only requirement is that, when the low-frequency filter inductors, filter capacitors, and sources are replaced by open- or short-circuits as described above, then the high-frequency switch network of Fig. 20.23 should remain.

For example, a zero-voltage-switching quasi-resonant buck converter is illustrated in Fig. 20.24(a). Typical tank capacitor voltage and tank inductor current waveforms are given in Fig. 20.24(b). A current-bidirectional realization of the two-quadrant SPST switch is shown; this causes the ZVS quasi-resonant switch to operate in the half-wave mode. Use of a voltage-bidirectional two-quadrant SPST switch allows full-wave operation.

By analysis similar to that of Section 20.2, it can be shown that the switch conversion ratio μ of the half-wave ZVS quasi-resonant switch is

$$\mu = 1 - FP_{\frac{1}{2}}\left(\frac{1}{J_s}\right) \quad (20.61)$$

The function $P_{\frac{1}{2}}(J_s)$ is again given by Eq. (20.46), and the quantity J_s is defined in Eq. (20.44). For the full-wave ZVS quasi-resonant switch, one obtains

$$\mu = 1 - FP_1\left(\frac{1}{J_s}\right) \quad (20.62)$$

where $P_1(J_s)$ is given by Eq. (20.58). The condition for zero voltage switching is

$$J_s \geq 1 \quad (20.63)$$

Thus, the zero voltage switching property is lost at light load. The peak transistor voltage is given by

$$\text{peak transistor voltage } V_{cr,pk} = (1 + J_s)V_1 \quad (20.64)$$

This equation predicts that load current variations can lead to large voltage stress on transistor Q_1 . For example, if it is desired to obtain zero voltage switching over a 5:1 range of load current variations, then J_s should vary between 1 and 5. According to Eq. (20.64), the peak transistor voltage then varies between two times and six times the applied voltage V_1 . The maximum transistor current is equal to the applied current I_2 . Although the maximum transistor current in the ZVS quasi-resonant switch is identical to that

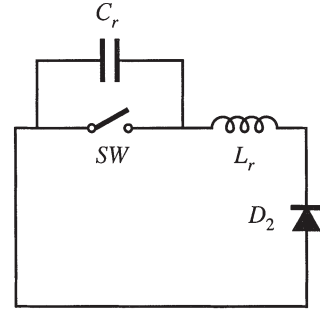


Fig. 20.23 Elimination of converter low-frequency elements reduces the ZVS quasi-resonant switch cell to this network.

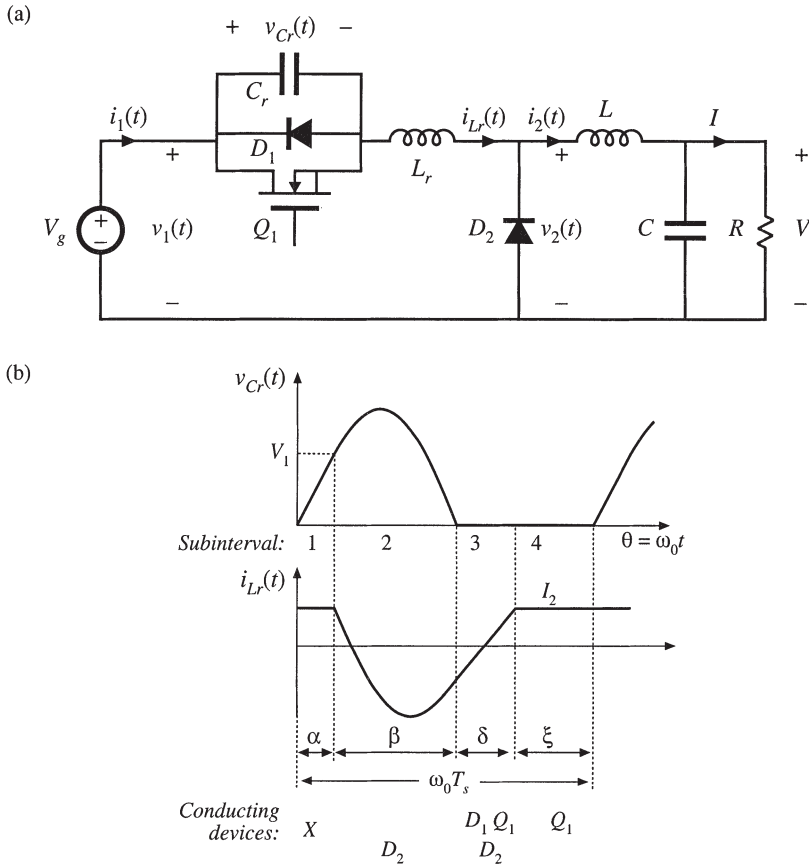


Fig. 20.24 A ZVS quasi-resonant buck converter: (a) circuit, (b) tank waveforms.

of the PWM switch, the peak transistor blocking voltage is substantially increased. This leads to increased conduction loss, because transistor on-resistance increases rapidly with rated blocking voltage.

20.3.2 The Zero-Voltage-Switching Multiresonant Switch

The resonant switch network of Fig. 20.25 contains tank capacitor C_d in parallel with diode D_2 , as in the ZCS switch network of Fig. 20.22. In addition, it contains tank capacitor C_s in parallel with the SPST switch, as in the ZVS switch network of Fig. 20.23. In consequence, all semiconductor elements switch at zero voltage. This three-element resonant switch network is known as the zero-voltage-switching multiresonant switch (ZVS MRS). Since no semiconductor output capacitances or diode recovered charges lead to ringing or switching loss, the ZVS MRS exhibits very low switching loss. For the same reason, generation of electromagnetic interference is reduced.

A half-wave ZVS MRS realization of the buck converter is illustrated in Fig. 20.26. In a typical design that must operate over a 5:1 load range and with $0.4 \leq \mu \leq 0.6$, the designer might choose a maximum F of 1.0, a maximum J of 1.4, and $C_d/C_s = 3$, where these quantities are defined as follows:

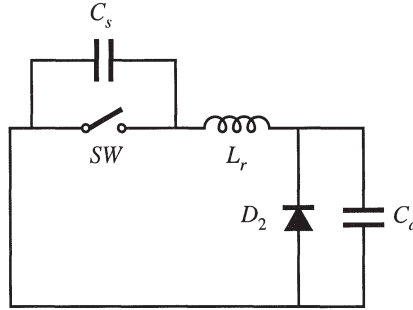


Fig. 20.25 Elimination of converter low-frequency elements reduces the ZVS multiresonant switch cell to this network.

$$\begin{aligned} f_0 &= \frac{1}{2\pi\sqrt{LC_t}} & R_0 &= \sqrt{\frac{L}{C_t}} \\ F &= \frac{f_s}{f_0} & J &= \frac{I_2 R_0}{V_1} \end{aligned} \quad (20.65)$$

As usual, the conversion ratio is defined as $\mu = V_2/V_1$. The resulting peak transistor voltage for this typical design is approximately $2.8V_1$, while the peak transistor current is $2I_2$. Hence, conduction losses are higher than in an equivalent PWM switch. The range of switch conversion ratios μ is a function of the capacitor ratio C_d/C_s ; in a good design, values of μ ranging from nearly one to nearly zero can be obtained, with a wide range of dc load currents and while maintaining zero voltage switching.

Analysis and design charts for the ZVS MRS are given in [5–8]. Results for the typical choice $C_d = 3C_s$ are plotted in Fig. 20.27. These plots illustrate how the switch conversion ratio μ varies as a function of load current and switching frequency. Figure 20.27(a) also illustrates the boundary of zero-voltage switching; ZVS is lost for operation outside the dashed lines. Decreasing the ratio of C_d to C_s reduces the area of the ZVS region.

Other resonant converters in which all semiconductor devices operate with zero voltage switching are known. Examples include some operating modes of the parallel and LCC resonant converters described in Chapter 19, as well as the class-E converters described in [10–12].

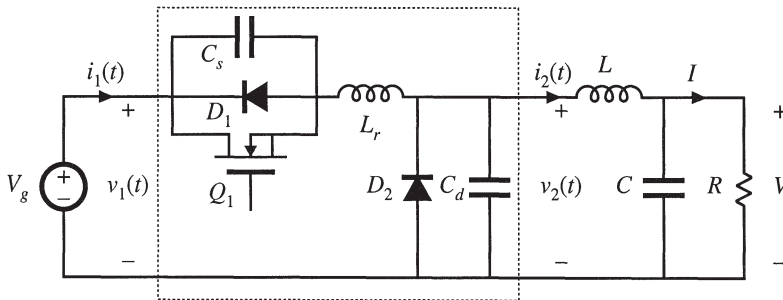


Fig. 20.26 Half-wave ZVS multiresonant buck converter.

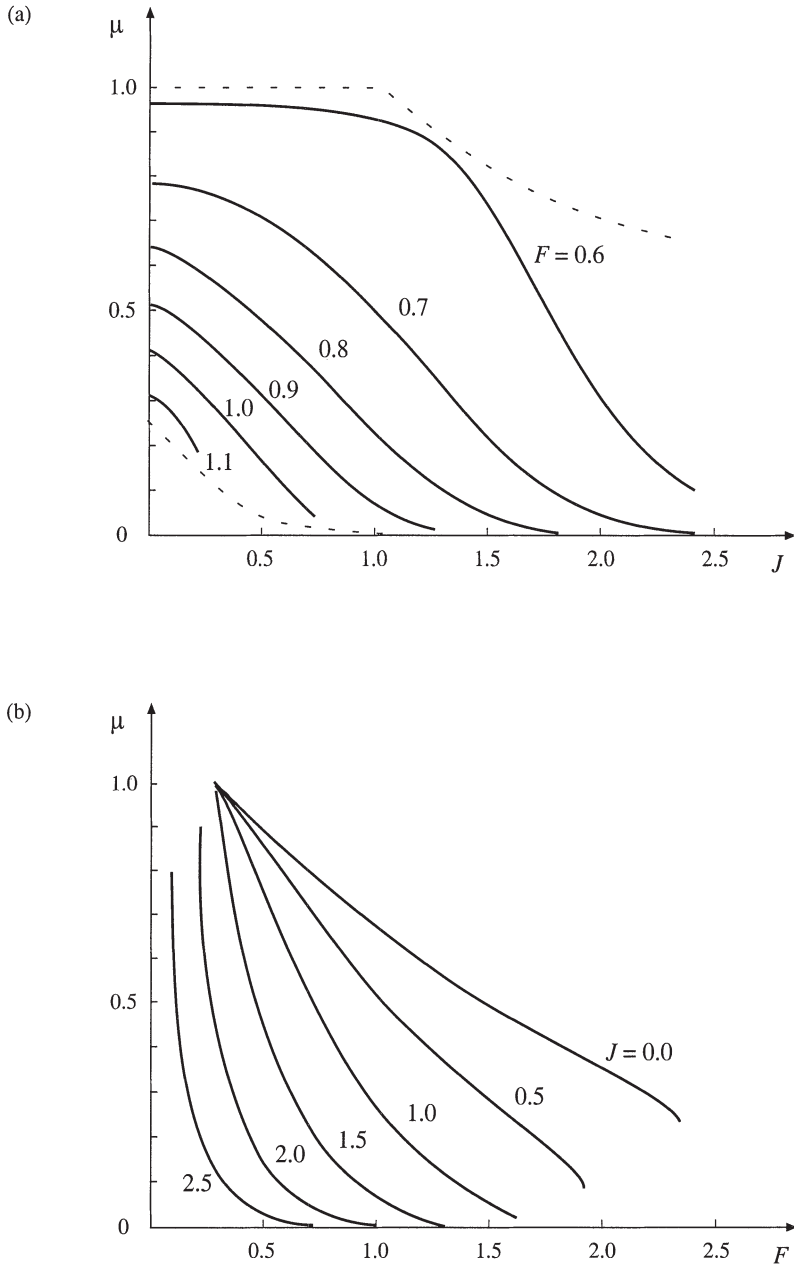


Fig. 20.27 Conversion ratio μ for the multi-resonant switch with $C_d = 3C_s$: (a) conversion ratio μ vs. normalized current J (solid lines: conversion ratio; dashed lines: boundaries of zero-voltage switching), (b) conversion ratio μ vs. normalized switching frequency F .

20.3.3 Quasi-Square-Wave Resonant Switches

Another basic class of resonant switch networks is the quasi-square wave converters. Both zero-voltage switching and zero-current switching versions are known; the resonant tank networks are illustrated in Fig. 20.28. In the network of Fig. 20.28(a), all semiconductor devices are effectively in series with the tank inductor, and hence operate with zero-current switching. In the network of Fig. 20.28(b), all semiconductor devices are effectively in parallel with the tank capacitor, and hence operate with zero-voltage switching.

Figure 20.29 illustrates implementation of a zero current switching quasi-square wave resonant switch, in a buck converter with input filter. Elements L_f and C_f are large in value, and constitute a single-section L - C input filter. Elements L_r and C_r form the series resonant tank; these elements are placed in series with input filter capacitor C_f . Since C_r and C_f are connected in series, they can be combined into a single small-value capacitor. In this zero-current-switching converter, the peak transistor current is identical to the peak transistor current of an equivalent PWM converter. However, the peak transistor blocking voltage is increased. The ZCS QSW resonant switch exhibits a switch conversion ratio μ that is restricted to the range $0 \leq \mu \leq 0.5$. Analysis of this resonant switch is given in [13–14].

A buck converter, containing a zero-voltage-switching quasi-square wave (ZVS QSW) resonant switch, is illustrated in Fig. 20.30. Typical waveforms are given in Fig. 20.31. Since the tank inductor L_r and the output filter inductor L are connected in parallel, these two elements can be combined into a single inductor having a small value nearly equal to L_r . Analyses of the ZVS QSW resonant switch are given in [14,15,18]. A related full-bridge converter is described in [16]. The ZVS QSW resonant switch is notable because zero voltage switching is obtained in all semiconductor devices, yet the peak transistor voltage is identical to that of an equivalent PWM switch [13]. However, the peak transistor currents are increased.

Characteristics of the zero-voltage-switching quasi-square wave resonant switch are plotted in Fig. 20.32. The switch conversion ratio $\mu = V_2/V_1$ is plotted as a function of normalized switching fre-

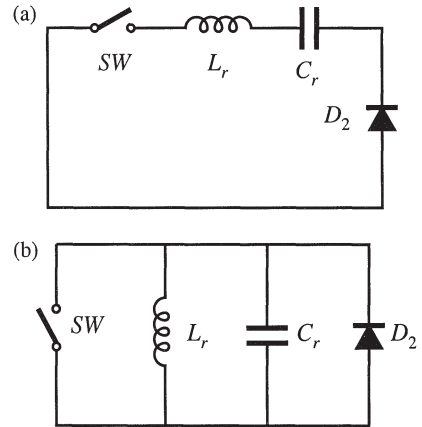


Fig. 20.28 Elimination of converter low-frequency elements reduces the quasi-square-wave switch cells to these networks: (a) ZCS quasi-square-wave network, (b) ZVS quasi-square-wave network.

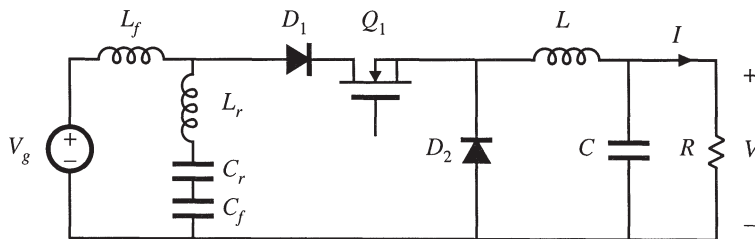


Fig. 20.29 Incorporation of a ZCS quasi-square-wave resonant switch into a buck converter containing an L - C input filter.

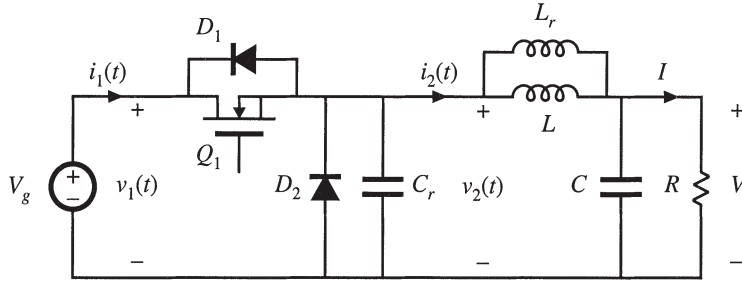


Fig. 20.30 Incorporation of a ZVS quasi-square-wave resonant switch into a buck converter.

Fig. 20.31 Waveforms of the ZVS quasi-square-wave resonant switch converter of Fig. 20.30.

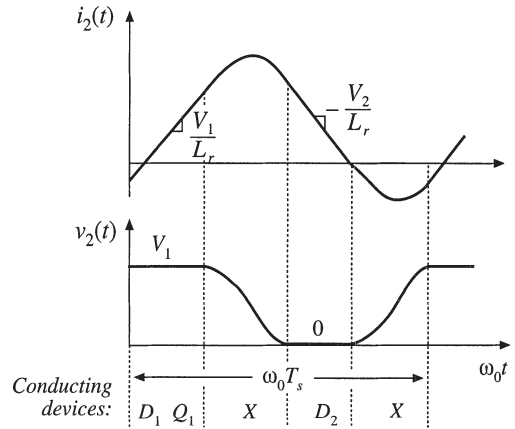
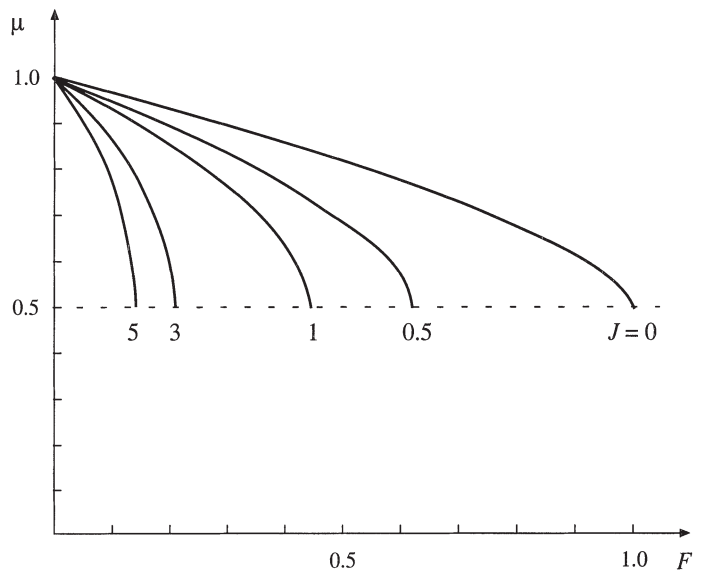


Fig. 20.32 Characteristics of the ZVS quasi-square wave resonant switch network: switch conversion ratio μ , as a function of F and J . Dashed line: ZVS boundary.



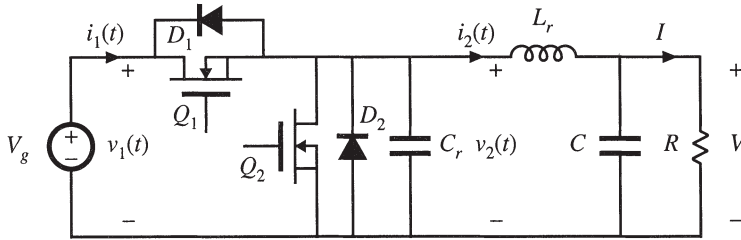


Fig. 20.33 Quasi-square wave ZVS buck converter containing a synchronous rectifier.

quency F and normalized output current J , where these quantities are defined as follows:

$$\begin{aligned} f_0 &= \frac{1}{2\pi\sqrt{L_r C_r}} & R_0 &= \sqrt{\frac{L_r}{C_r}} \\ F &= \frac{f_s}{f_0} & J &= \frac{I_2 R_0}{V_1} \end{aligned} \quad (20.66)$$

In addition, the zero-voltage-switching boundary is plotted. It can be seen that the requirement for zero-voltage switching limits the switch conversion ratio μ to the range $0.5 \leq \mu \leq 1$. In consequence, the buck converter of Fig. 20.30 cannot produce output voltages less than $0.5V_g$ without losing the ZVS property. A version which attains $0 \leq \mu \leq 1$, at the expense of increased transistor voltage stress, is described in [17]. In addition, the two-switch version of the ZVS-QSW switch can operate with ZVS for $\mu < 0.5$.

A useful variant of the converter of Fig. 20.30 involves replacement of the diode with a synchronous rectifier, as illustrated in Fig. 20.33 [8,9]. The second transistor introduces an additional degree of freedom in control of the converter, because this transistor can be allowed to conduct longer than the diode would otherwise conduct. This fact can be used to extend the region of zero-voltage switching to conversion ratios approaching zero, and also to operate the converter with constant switching frequency.

Typical tank element waveforms for the circuit of Fig. 20.33 are illustrated in Fig. 20.34. These waveforms resemble those of the single switch case, Fig. 20.31, except that the tank current is negative while transistor Q_2 conducts. The duty cycle D is defined with respect to the turn-off transitions

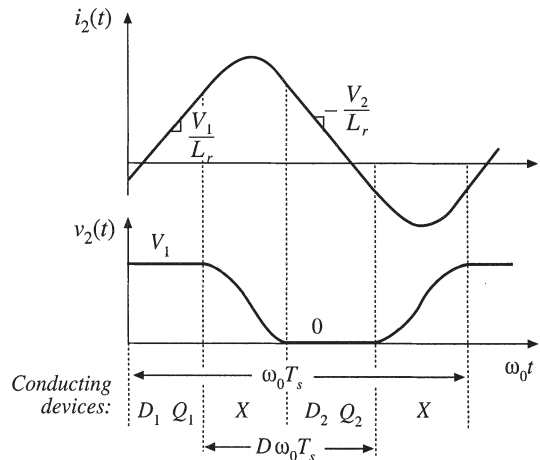


Fig. 20.34 Waveforms for the two-switch QSW-ZVS converter of Fig. 20.33.

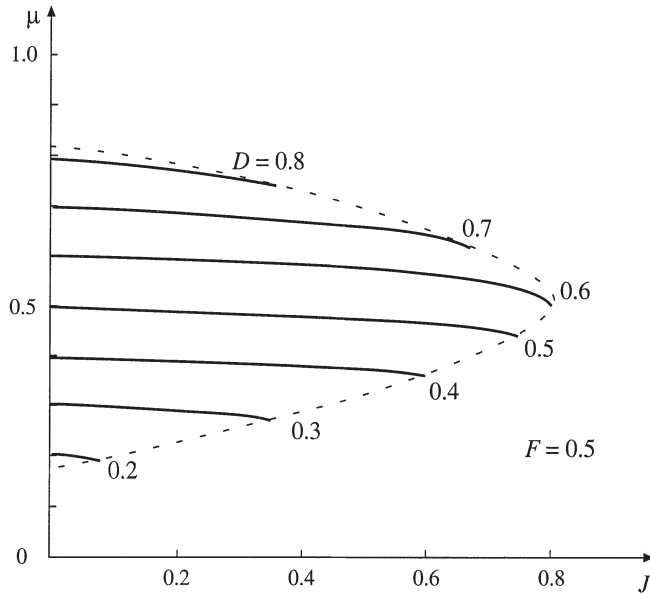


Fig. 20.35 Conversion ratio μ , as a function of duty cycle D and normalized load current J , for the two-switch QSW-ZVS switch illustrated in Fig. 20.33. Curves are plotted for constant-frequency control with $F = 0.5$. The dashed line is the zero-voltage switching boundary.

of transistors Q_1 and Q_2 , as illustrated.

Characteristics of the two-switch QSW-ZVS switch network are plotted in Fig. 20.35, for the case of constant switching frequency at $F = 0.5$. The boundary of zero-voltage switching is also illustrated. Operation at a lower value of F causes the ZVS boundary to be extended to larger values of J , and to values of μ that more closely approach the extreme values $\mu = 0$ and $\mu = 1$.

To the commutation intervals can be neglected, one would expect that the switch conversion ratio μ is simply equal to the duty cycle D . It can be seen from Fig. 20.35 that this is indeed the case. The characteristics are approximately horizontal lines, nearly independent of load current J .

Zero-voltage switching quasi-square wave converters exhibit very low switching loss, because all semiconductor elements operate with zero-voltage switching. In the constant-frequency case containing a synchronous rectifier, the converter behavior is nearly the same as for the hard-switched PWM case, since $\mu \approx D$. The major disadvantage is the increased conduction loss, caused by the reversal of the inductor current.

20.4 SOFT SWITCHING IN PWM CONVERTERS

The quasi-square wave approach of the previous section is notable because it attains zero-voltage switching without increasing the peak voltage applied to the transistor. Several related soft-switching approaches have now become popular, which also attain zero-voltage switching without increasing the transistor peak voltage stress. In this section, popular zero-voltage switching versions of the full bridge, forward, and flyback converters, as well as the voltage-source inverter, are briefly discussed.

20.4.1 The Zero-Voltage Transition Full-Bridge Converter

It is possible to obtain soft switching in other types of converters as well. An example is the zero-voltage transition (ZVT) converter based on the full-bridge transformer-isolated buck converter, illustrated in Fig. 20.36 [25–28]. The transistor and diode output capacitances are represented in the figure by capacitances C_{leg} . Commutating inductor L_c is placed in series with the transformer; the net inductance L_c includes both transformer leakage inductance and the inductance of an additional discrete element. This inductor causes the full-bridge switch network to drive an effective inductive load, and results in zero-voltage switching of the primary-side semiconductor devices. Although the waveforms are not sinusoidal, it can nonetheless be said that the switch network output current $i_c(t)$ lags the voltage $v_s(t)$, because the zero crossings of $i_c(t)$ occur after the ZVS switching transitions are completed.

The output voltage is controlled via phase control. As illustrated in Fig. 20.37, both halves of the bridge switch network operate with a 50% duty cycle, and the phase difference between the half-bridge switch networks is controlled. The idealized waveforms of Fig. 20.37 neglect the switching transitions, and the subinterval numbers correspond to those of the more detailed Fig. 20.38. The phase shift variable ϕ lies in the range $0 \leq \phi \leq 1$, and assumes the role of the duty cycle d in this converter. The quantity ϕ is defined as

$$\phi = \frac{(t_1 - t_0)}{\left(\frac{T_s}{2}\right)} \quad (20.67)$$

By volt-second balance on the secondary-side filter inductor, the conversion ratio $M(\phi)$ is expressed as

$$M(\phi) = \frac{V}{V_g} = n\phi \quad (20.68)$$

This expression neglects the lengths of the switching transitions.

Although the circuit appears symmetrical, the phase-shift control scheme introduces an asymmetry that causes the two half-bridge switch networks to behave quite differently during the switching transitions. During subintervals 4 and 10, energy is actively transmitted from the source V_g through the switches and transformer. These subintervals are initiated by the switching of the half-bridge network

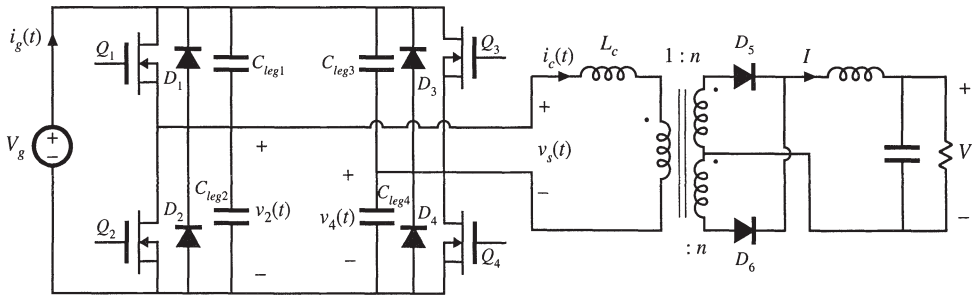


Fig. 20.36 Zero-voltage transition converter, based on the full-bridge isolated buck converter.

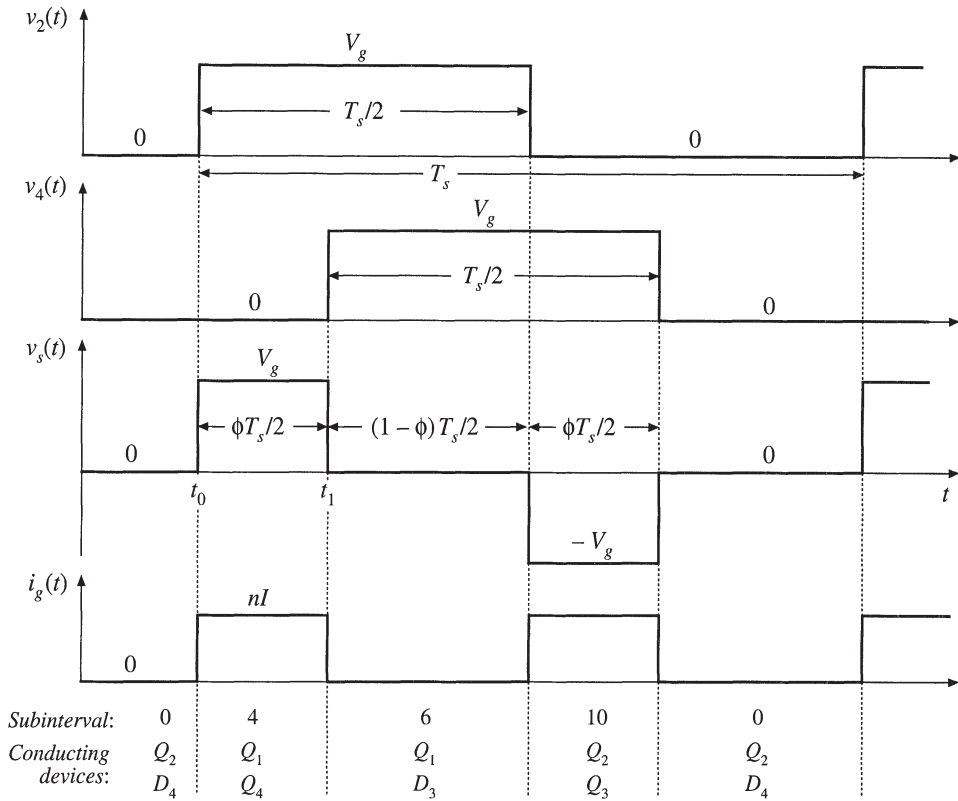


Fig. 20.37 Phase-shift control of the ZVT full-bridge converter. Switching transitions are neglected in this figure, and subinterval numbering follows Fig. 20.38.

composed of the elements Q_1 , D_1 , Q_2 , and D_2 , called the “passive-to-active” (P–A) transition [27]. Subintervals 4 and 10 are terminated by the switching of the half-bridge network comprised by the elements Q_3 , D_3 , Q_4 , and D_4 , called the “active-to-passive” (A–P) transition.

The turn-on and turn-off switching processes of this converter are similar to the zero-voltage-switching turn-off process described in the previous section. Detailed primary-side waveforms are illustrated in Fig. 20.38. During subinterval 0, Q_2 and D_4 conduct. If the transformer magnetizing current i_M is negligible, then the commutating inductor current is given by $i_c(t_0) = -nI$, where I is the load current. The passive-to-active transition is initiated when transistor Q_2 is turned off. The negative i_c then causes capacitors C_{leg1} and C_{leg2} to charge, increasing $v_2(t)$. During subinterval 1, L_c , C_{leg1} , and C_{leg2} form a resonant network that rings with approximately sinusoidal waveforms. If sufficient energy was initially stored in L_c , then $v_2(t)$ eventually reaches V_g , terminating subinterval 1. Diode D_1 then clamps $v_2(t)$ to V_g during subinterval 2. Transistor Q_1 is turned on at zero voltage during subinterval 2; in practice, this is implemented by insertion of a small delay between the switching transitions of transistors Q_2 and Q_1 .

If L_c does not initially store sufficient energy to charge the total capacitance ($C_{leg1} + C_{leg2}$) from $v_2 = 0$ to $v_2 = V_g$ during subinterval 1, then $v_2(t)$ will never reach V_g . Switching loss will then occur when transistor Q_1 is turned on. This situation typically occurs at light load, where I is small. Sometimes, the design engineer may choose to simply accept this power loss; after all, other losses such as conduction loss are small at light load. An alternative is to modify the circuit to increase the energy stored in L_c at

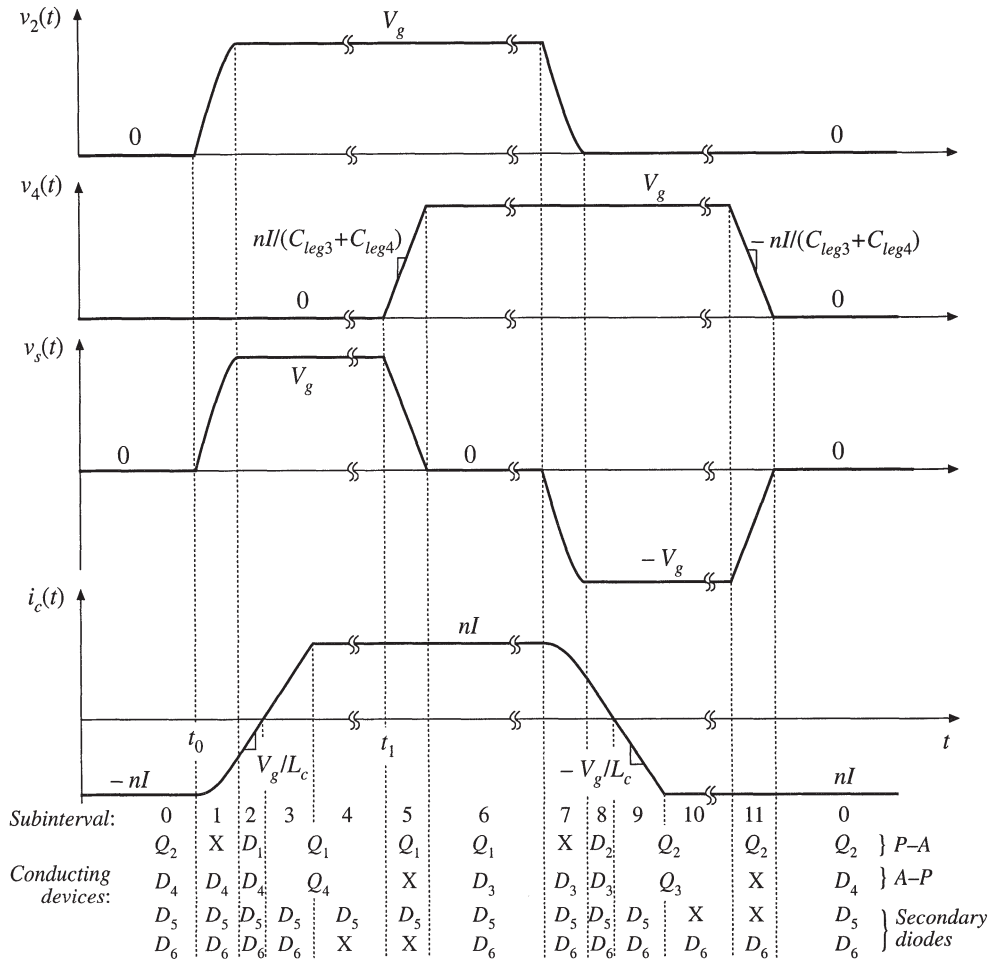


Fig. 20.38 Detailed diagram of primary-side waveforms of the ZVT full-bridge converter, illustrating the zero-voltage switching mechanisms. An ideal transformer is assumed.

$t = t_0$ under light load conditions. One way to accomplish this is to increase the transformer magnetizing current $i_M(t_0)$ to a significant level; at the beginning of subinterval 1, i_c is then equal to $i_c(t_0) = -nI + i_M(t_0)$ with $i_M(t_0) < 0$. At light load where I is small, the magnetizing current maintains the required level of i_c .

During subintervals 0, 1, 2, and 3, secondary-side diodes D_5 and D_6 both conduct; hence, zero voltage appears across all transformer windings. In consequence, voltage V_g is applied to commutating inductor L_c during subintervals 2 and 3, causing $i_c(t)$ to increase with slope V_g/L_c . Current $i_c(t)$ reaches zero at the end of subinterval 2, and increases to the positive value $+nI$ at the end of subinterval 3. The reversal of polarity of $i_c(t)$ enables zero-voltage switching during the next switching transitions, subinterval 5 and subintervals 7–9.

At the end of subinterval 3, the current in diode D_6 has decreased to zero. D_6 then becomes reverse-biased, with zero-current switching. At this instant, diode D_6 must begin to block voltage $2nV_g$.

The output capacitance of D_6 prevents the voltage from changing immediately to $2nV_g$; instead, the resonant circuit formed by L_c and the D_6 output capacitance begins to ring in a manner similar to Fig. 4.54. Peak D_6 voltages are typically observed that are considerably in excess of $2nV_g$, and it is usually necessary to add voltage-clamp snubbers that prevent the secondary-side diode voltages from exceeding a safe value. Several dissipative and non-dissipative approaches are discussed in [26–28].

The active-to-passive switching transition occurs during subinterval 5. This subinterval is initiated when transistor Q_4 is turned off. The positive current $i_c(t_1)$ is equal to the reflected load current nI , and charges capacitors C_{leg3} and C_{leg4} from $v_4 = 0$ to $v_4 = V_g$. Subinterval 5 ends when v_4 reaches V_g ; Diode D_3 then becomes forward-biased. Transistor Q_3 is then turned on during subinterval 6, with zero-voltage switching. This is typically implemented by insertion of a small delay between the switching of transistors Q_4 and Q_3 . Because i_c is constant and equal to nI during subinterval 5, the active-to-passive transition maintains zero-voltage switching at all load currents.

Circuit behavior during the next half switching period, comprising subintervals 6 to 11, is symmetrical and therefore similar to the behavior observed during subintervals 0 to 5. The switching transitions of transistors Q_1 and Q_2 are passive-to-active transitions, and occur with zero-voltage switching provided that sufficient energy is stored in L_c as described above. The switching transitions of Q_3 and Q_4 are active-to-passive, and occur with zero-voltage switching at all loads.

The zero-voltage transition converter exhibits low primary-side switching loss and generated EMI. Conduction loss is increased with respect to an ideal PWM full-bridge topology, because of the current i_c that circulates through the primary-side semiconductors during subintervals 0 and 6. However, this increase in conduction loss can be small if the range of input voltage variations is narrow. This soft-switching approach has now found commercial success.

20.4.2 The Auxiliary Switch Approach

A similar approach can be used in forward, flyback, and other transformer-isolated converters. As illustrated in Fig. 20.39, an “active-clamp snubber” network consisting of a capacitor and auxiliary MOSFET Q_2 is added, that is effectively in parallel with the original power transistor Q_1 [29]. The MOSFET body diodes and output drain-to-source capacitances, as well as the transformer leakage inductance L_t , participate in the circuit operation. These elements lead to zero-voltage switching, with waveforms similar to those of the ZVT full-bridge converter of Section 20.4.1 or the two-transistor QSW-ZVS switch of Section 20.3.3. The transistors are driven by complementary signals; for example, after turning off Q_1 , the controller waits for a short delay time and then turns on Q_2 .

The active-clamp snubber can be viewed as a voltage-clamp snubber, similar to the dissipative snubber illustrated in Fig. 20.6. However, the snubber contains no resistor; instead, MOSFET Q_2 allows bidirectional power flow, so that the energy stored in capacitor C_s can flow back into the converter.

The voltage v_s can be found by volt-second inductance on the transformer magnetizing inductance. If the lengths of the commutation intervals are neglected, and if the voltage ripple in $v_s(t)$ can be neglected, then one finds that

$$V_s = \frac{D}{D'} V_g \quad (20.69)$$

The voltage v_s is effectively an unloaded output of the converter. With the two-quadrant switch provided by Q_2 , this output operates in continuous conduction mode with no load, and hence the peak voltage of Q_1 is clamped to the minimum level necessary to balance the volt-seconds applied to the transformer magnetizing inductance.

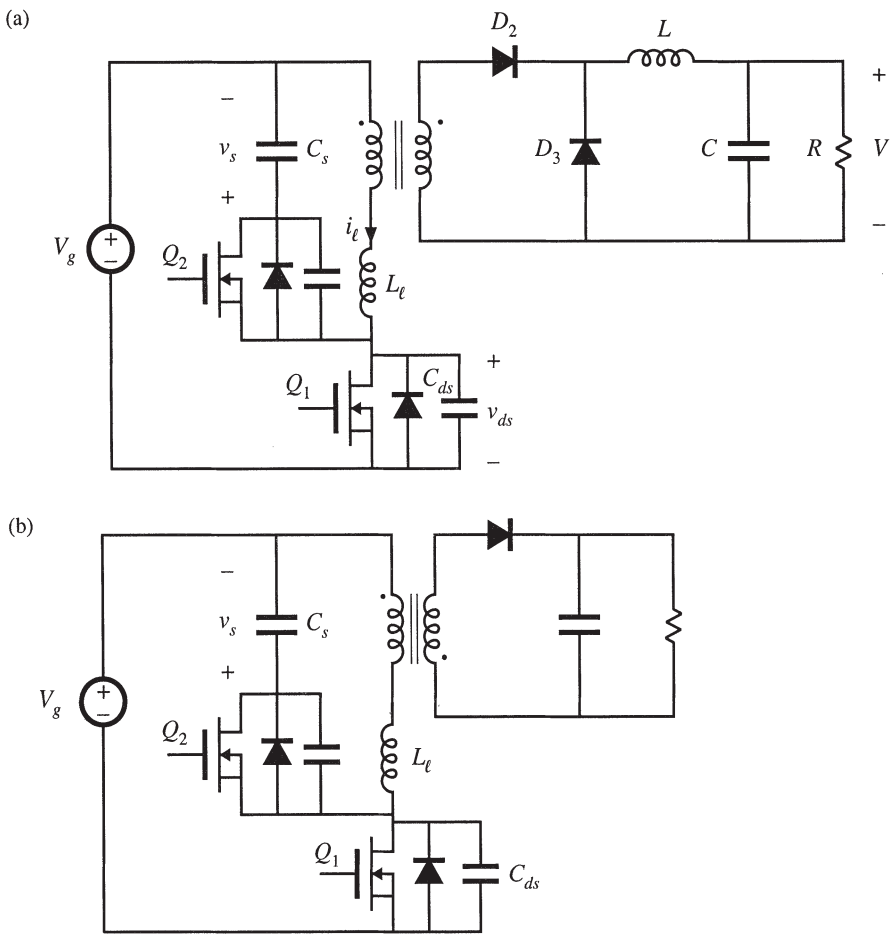


Fig. 20.39 Active-clamp snubber circuits: (a) forward converter, (b) flyback converter.

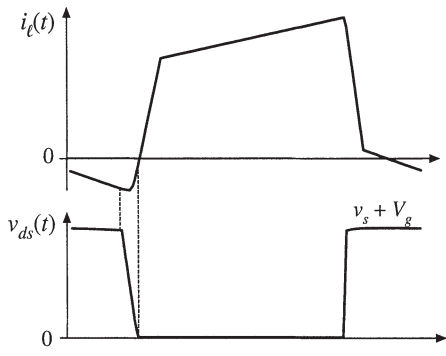


Fig. 20.40 Waveforms of the active-clamp snubber circuit of Fig. 20.39(a).

Typical waveforms for a forward converter incorporating an active-clamp snubber are illustrated in Fig. 20.40. The current $i_L(t)$ reverses direction while Q_2 conducts. When Q_2 turns off, capacitor C_{ds} begins to discharge. When v_{ds} reaches zero, the body diode of Q_1 becomes forward-biased. Q_1 can then be turned on at zero voltage.

An added benefit of the active clamp snubber, when used in a forward converter, is that it resets the transformer. Consequently, the converter can operate at any duty cycle, including duty cycles greater than 50%. When the converter must operate with a wide range of input voltages, this can allow substantial improvements in transistor stresses and efficiency. The MOSFETs in Fig. 20.39 operate with zero-voltage switching, while the secondary-side diodes operate with zero-current switching.

This approach is quite versatile, and similar auxiliary circuits can be added to other converter circuits to obtain zero-voltage switching [30,31].

20.4.3 Auxiliary Resonant Commutated Pole

The auxiliary resonant commutated pole (ARCP) is a related circuit that uses an auxiliary four-quadrant switch (or two equivalent two-quadrant switches) to obtain soft switching in the transistors of a bridge inverter circuit [32–34]. This approach finds application in dc–ac inverter circuits. Figure 20.41 illustrates a half-bridge circuit, or one phase of a three-phase voltage-source inverter, driving an ac load. This circuit can lead to zero-voltage switching that mitigates the switching loss induced by the reverse recovery of diodes D_1 and D_2 . Filter inductor L_f is relatively large, so that the output current $i_a(t)$ is essentially constant during the resonant commutation interval. Capacitors C_{ds} are relatively small, and model the output capacitances of the semiconductor devices. Inductor L_r is also relatively small, and elements L_r and C_{ds} form a resonant circuit that rings during part of the commutation process. Semiconductor switching devices Q_3 , Q_4 , D_3 , and D_4 form an auxiliary four-quadrant switch that turns on to initiate the resonant commutation process.

Typical commutation waveforms are illustrated in Fig. 20.42(a), for the case in which the ac load current i_a is positive. Diode D_2 is initially conducting the output current i_a . It is desired to turn off D_2 and turn on Q_1 , with zero-voltage switching. This is accomplished with the following sequence:

- Interval 1. Turn on transistor Q_3 . Devices D_2 , Q_3 , and D_4 conduct.
- Interval 2. When the current in D_2 reaches zero, D_2 turns off. A resonant ringing interval occurs.
- Interval 3. When the voltage v_{an} reaches $V_g/2$, diode D_1 begins to become forward-biased. Transistor Q_1 is then immediately turned on at zero voltage.

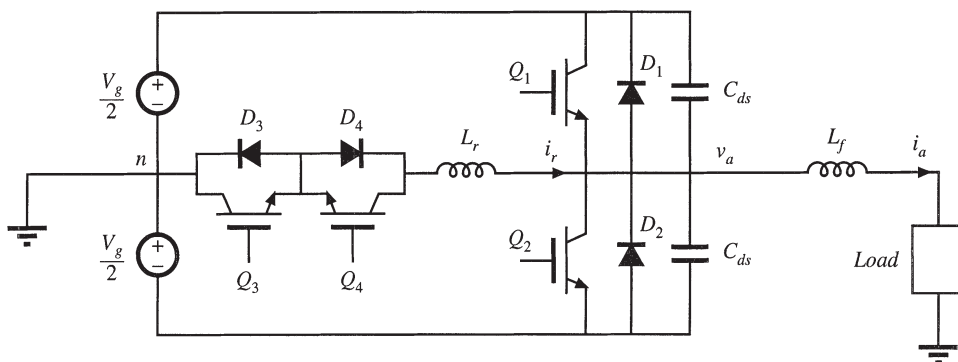


Fig. 20.41 Half-bridge circuit driving an ac load, with ARCP zero-voltage switching.

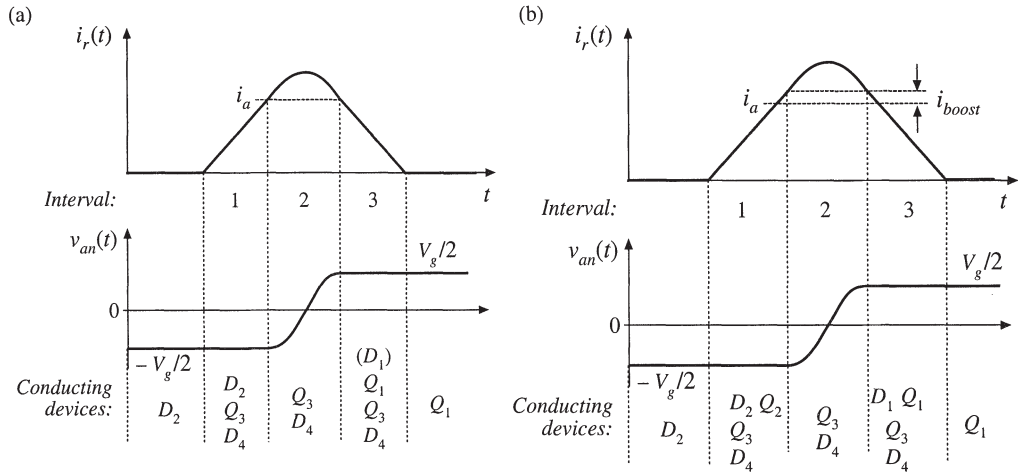


Fig. 20.42 Waveforms of the ARCP circuit of Fig. 20.41: (a) basic waveforms, (b) with current boost.

At the conclusion of interval 3, $i_r(t)$ reaches zero and diode D_3 turns off. For negative current, the process for commutation of diode D_1 is similar, except that transistor Q_4 and diode D_3 conduct the resonant current $i_r(t)$.

One issue related to the waveforms of Fig. 20.42(a) is that the circuit always operates at the boundary of zero-voltage switching. At the end of interval 2, diode D_1 is not actually forward-biased, because its current never actually becomes positive. Instead, transistor Q_1 should be turned on at the beginning of interval 3. If transistor Q_1 is gated on late, then the continued ringing will cause voltage $v_{an}(t)$ to decrease, and zero-voltage switching will be lost.

To further assist in the zero-voltage switching commutation process, transistor Q_2 can be turned on while D_2 conducts, as illustrated in Fig. 20.42(b). Transistor Q_2 is used to lengthen the duration of interval 1: now, when the current $i_r(t)$ exceeds current i_a by an amount i_{boost} , then the controller turns off Q_2 to end interval 1. This causes diode D_1 to become forward-biased during the beginning of interval 3. Transistor Q_1 is then turned on with zero-voltage switching, while D_1 is conducting.

Regardless of whether the circuit operates with the waveforms of Fig. 20.42(a) or (b), the ARCP approach eliminates the switching loss caused by the reverse recovery of diodes D_1 and D_2 . Unlike the previous circuits of this chapter, the ARCP has no circulating currents that cause conduction loss, because the tank inductor current $i_r(t)$ is nonzero only in the vicinity of the commutation interval. The approach of Fig. 20.42(a) does not completely eliminate the loss caused by the device output capacitances. This loss is eliminated using the current boost of Fig. 20.42(b), but additional conduction loss is incurred because of the increased peak $i_r(t)$. The waveforms of Fig. 20.42(b) may, in fact, lead to reduced efficiency relative to Fig. 20.42(a)!

20.5 SUMMARY OF KEY POINTS

1. In a resonant switch converter, the switch network of a PWM converter is replaced by a switch network containing resonant elements. The resulting hybrid converter combines the properties of the resonant switch network and the parent PWM converter.
2. Analysis of a resonant or soft-switching switch cell involves determination of the switch conversion ratio μ . The resonant switch waveforms are determined, and are then averaged. The switch conversion ratio μ is

a generalization of the PWM CCM duty cycle d . The results of the averaged analysis of PWM converters operating in CCM can be directly adapted to the related resonant switch converter, simply by replacing d with μ .

3. In the zero-current-switching quasi-resonant switch, diode D_2 operates with zero-voltage switching, while transistor Q_1 and diode D_1 operate with zero-current switching. In the zero-voltage-switching quasi-resonant switch, the transistor Q_1 and diode D_1 operate with zero-voltage switching, while diode D_2 operates with zero-current switching.
4. In the zero-voltage-switching multiresonant switch, all semiconductor devices operate with zero-voltage switching. In consequence, very low switching loss is observed.
5. In the quasi-square-wave zero-voltage-switching resonant switches, all semiconductor devices operate with zero-voltage switching, and with peak voltages equal to those of the parent PWM converter. The switch conversion ratio is restricted to the range $0.5 \leq \mu \leq 1$. Versions containing synchronous rectifiers can operate with values of μ approaching zero.
6. The zero-voltage transition approach, as well as the active-clamp snubber approach, lead to zero-voltage switching of the transistors and zero-current switching of the diodes. These approaches have been successful in substantially improving the efficiencies of transformer-isolated converters. The auxiliary resonant commutated pole induces zero-voltage switching in bridge circuits such as the voltage-source inverter.

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PROBLEMS

- 20.1** In the forward converter of Fig. 20.43, L and C are large filter elements while L_p , L_s , and C_r have relatively small values. The transformer reset mechanism is not shown; for this problem, you may assume that the transformer is ideal.

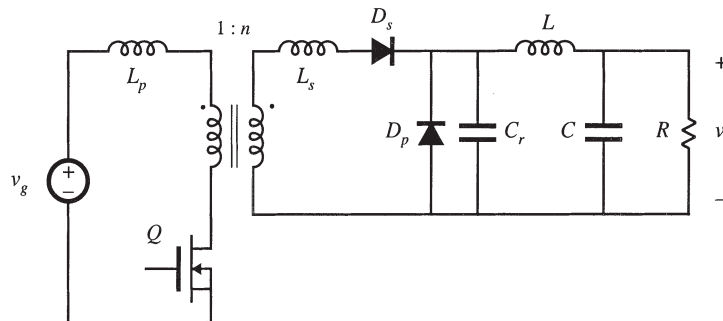


Fig. 20.43 Forward converter with resonant switch, Problem 20.1.

- (a) Classify the resonant switch.

- (b) Which semiconductor devices operate with zero-voltage switching? With zero-current switching?
- (c) What is the resonant frequency?

20.2

In the high-voltage converter of Fig. 20.44, capacitor C is relatively large in value. The transformer model includes an ideal $1:n$ transformer, in conjunction with magnetizing inductance L_{mp} (referred to the primary side) and winding capacitance C_{ws} (referred to the secondary side). Transistor Q and diode D_p exhibit total output capacitance C_p , while the output capacitance of diode D_s is C_s . Other nonidealities, such as transformer leakage inductance, can be ignored. The resonant switch is well-designed, such that all elements listed above contribute to ideal operation of the converter and resonant switch.

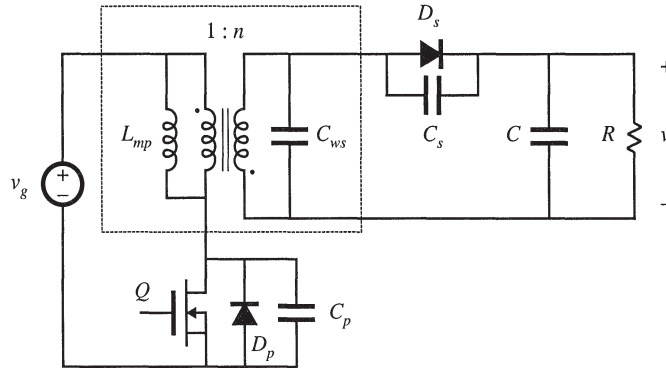


Fig. 20.44 High-voltage dc-dc converter containing a resonant switch network, Problem 20.2.

- (a) What type of resonant switch is employed? What is the parent PWM converter?
- (b) Which semiconductor devices operate with zero-voltage switching? With zero-current switching?
- (c) What is the tank resonant frequency?
- (d) Sketch the waveforms of the transistor drain-to-source voltage and transformer magnetizing current.

20.3

In the transformer-isolated dc-dc converter of Fig. 20.45, capacitors C_1 and C_2 and inductors L_1 and L_M are relatively large in value, so that they have small switching ripples. The transformer model includes an ideal $1:n$ transformer, in conjunction with magnetizing inductance L_M (referred to the primary side) and leakage inductances $L_{\ell 1}$ and $L_{\ell 2}$ as shown. Transistor Q_1 exhibits output capacitances C_{ds} , while the output capacitance of diode D_1 is C_d . MOSFET Q_1 contains a body diode (not explicitly shown). Other nonidealities can be ignored. The resonant switch is well-designed, such that all elements listed above contribute to ideal operation of the converter and resonant switch.

- (a) What type of resonant switch is employed? What is the parent PWM converter?
- (b) Which semiconductor devices operate with zero-voltage switching? With zero-current switching?

20.4

A buck-boost converter is realized using a half-wave ZCS quasi-resonant switch. The load resistance has value R , the input voltage has value V_g , and the converter switching frequency is f_s .

- (a) Sketch the circuit schematic.
- (b) Write the complete system of equations that can be solved to determine the output voltage V_i in terms of the quantities listed above and the component values. It is not necessary to actually solve your equations. You may also quote results listed in this textbook.

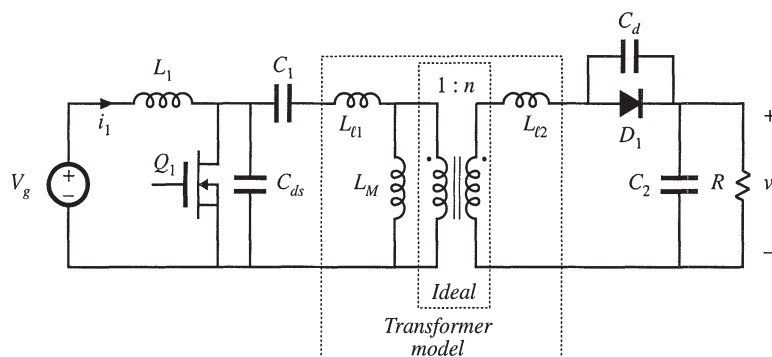


Fig. 20.45 Transformer-isolated dc-dc converter containing a resonant switch network, Problem 20.3.

20.5 It is desired to design a half-wave zero-current-switching quasi-resonant forward converter to operate with the following specifications: $V_g = 320$ V, $V = 42$ V, $5 \text{ W} \leq P \leq 100$ W. Design the converter to operate with a maximum switching frequency of 1 MHz and a switch conversion ratio of $\mu = 0.45$. Attempt to minimize the peak transistor current, while maintaining zero current switching at all operating points. You may neglect the transformer magnetizing current, and ignore the transformer reset scheme.

- Specify your choices for the turns ratio n , and the tank elements L_r and C_r , referred to the transformer secondary side.
- For your design of part (a), what is the minimum switching frequency?
- What is the worst-case peak transistor current?

20.6 Analysis of the ZVS quasi-resonant switch of Fig. 20.24.

- For each subinterval, sketch the resonant switch cell circuit, and derive expressions for the tank inductor current and capacitor voltage waveforms.
- For subinterval 2, in which Q_1/D_1 are off and D_2 conducts, write the loop equation which relates the tank capacitor voltage, tank inductor voltage, and any other network voltages as appropriate. Hence, for subinterval 2 relate the integral of the tank capacitor voltage to the change in tank inductor current.
- Determine the switch-network terminal-waveform average values, and hence derive an expression for the switch conversion ratio μ . Verify that your result coincides with Eq. (20.61).

20.7 Analysis of the full-bridge zero-voltage transition converter of Section 20.4.1. The converter of Fig. 20.36 operates with the waveforms illustrated in Fig. 20.38. According to Eq. (20.68), the conversion ratio of this converter is given approximately by $M(\phi) = n\phi$.

Derive an exact expression for M , based on the waveforms given in Fig. 20.38. Your result should be a function of the length of subinterval 4, the load current, the switching frequency, and the values of the inductance and capacitances. *Note:* there is a reasonably simple answer to this question.

Appendices

Appendix A

RMS Values of Commonly Observed Converter Waveforms

The waveforms encountered in power electronics converters can be quite complex, containing modulation at the switching frequency and often also at the ac line frequency. During converter design, it is often necessary to compute the rms values of such waveforms. In this appendix, several useful formulas and tables are developed which allow these rms values to be quickly determined.

RMS values of the doubly-modulated waveforms encountered in PWM rectifier circuits are discussed in Section 18.5.

A.1 SOME COMMON WAVEFORMS

DC, Fig. A.1:

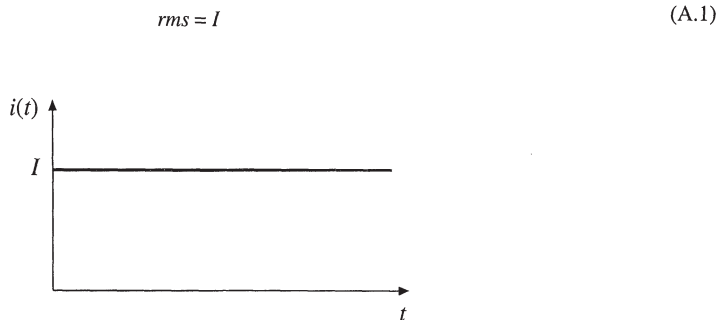


Fig. A.1

DC plus linear ripple, Fig. A.2:

$$rms = I \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i}{I} \right)^2} \quad (A.2)$$

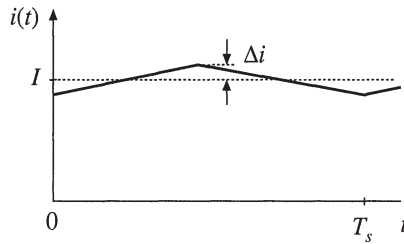


Fig. A.2

Square wave, Fig. A.3:

$$rms = I_{pk} \quad (A.3)$$

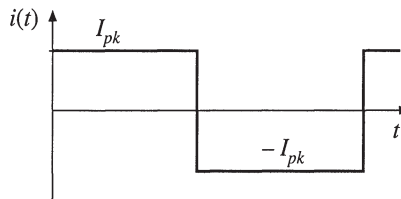


Fig. A.3

Sine wave, Fig. A.4:

$$rms = \frac{I_{pk}}{\sqrt{2}} \quad (A.4)$$

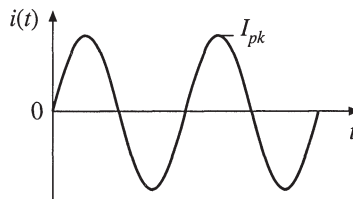
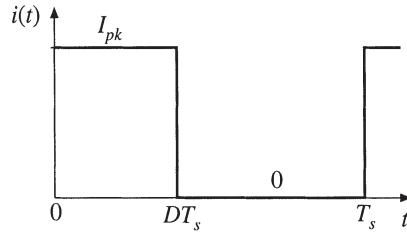


Fig. A.4

Pulsating waveform, Fig. A.5:

$$rms = I_{pk} \sqrt{D} \quad (A.5)$$

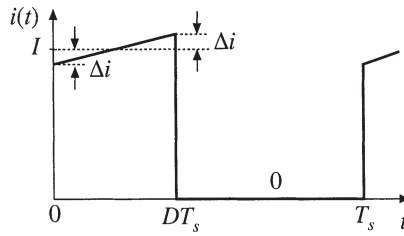
Fig. A.5



Pulsating waveform with linear ripple, Fig. A.6:

$$rms = I\sqrt{D}\sqrt{1 + \frac{1}{3}\left(\frac{\Delta i}{I}\right)^2} \quad (A.6)$$

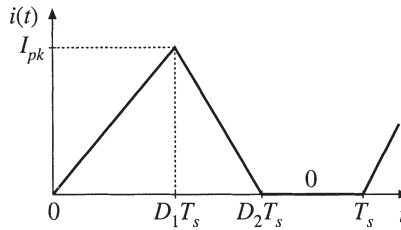
Fig. A.6



Triangular waveform, Fig. A.7:

$$rms = I_{pk}\sqrt{\frac{D_1 + D_2}{3}} \quad (A.7)$$

Fig. A.7



Triangular waveform, Fig. A.8:

$$rms = I_{pk}\sqrt{\frac{D_1}{3}} \quad (A.8)$$

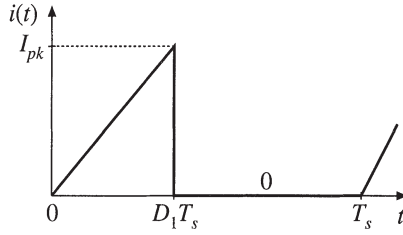


Fig. A.8

Triangular waveform, no dc component, Fig. A.9:

$$rms = \frac{\Delta i}{\sqrt{3}} \quad (\text{A.9})$$

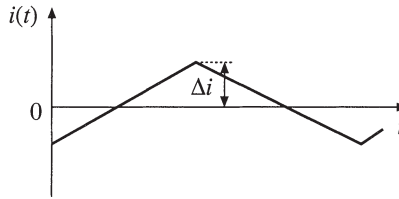


Fig. A.9

Center-tapped bridge winding waveform, Fig. A.10:

$$rms = \frac{1}{2} I_{pk} \sqrt{1 + D} \quad (\text{A.10})$$

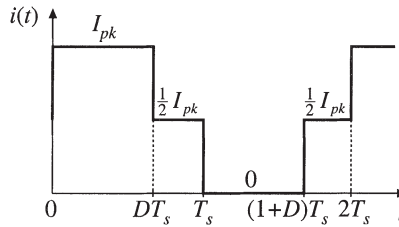


Fig. A.10

General stepped waveform, Fig. A.11:

$$rms = \sqrt{D_1 I_1^2 + D_2 I_2^2 + \dots} \quad (\text{A.11})$$

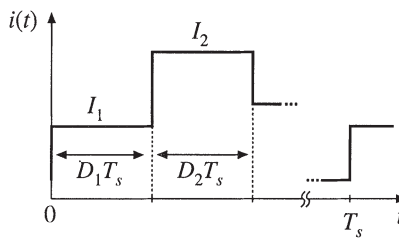
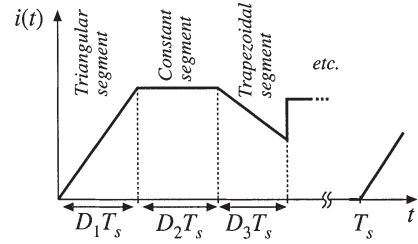


Fig. A.11

Fig. A.12 General piecewise waveform.



A.2 GENERAL PIECEWISE WAVEFORM

For a periodic waveform composed of n piecewise segments as in Fig. A.12, the rms value is

$$rms = \sqrt{\sum_{k=1}^n D_k u_k} \quad (\text{A.12})$$

where D_k is the duty cycle of segment k , and u_k is the contribution of segment k . The u_k s depend on the shape of the segments—several common segment shapes are listed below:

Constant segment, Fig. A.13:

$$u_k = I_1^2 \quad (\text{A.13})$$

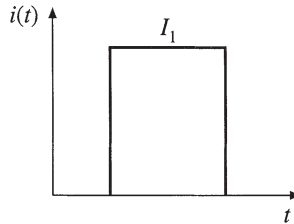


Fig. A.13

Triangular segment, Fig. A.14:

$$u_k = \frac{1}{3} I_1^2 \quad (\text{A.14})$$

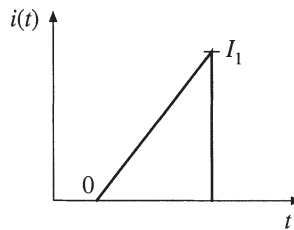


Fig. A.14

Trapezoidal segment, Fig. A.15:

$$u_k = \frac{1}{3} (I_1^2 + I_1 I_2 + I_2^2) \quad (\text{A.15})$$

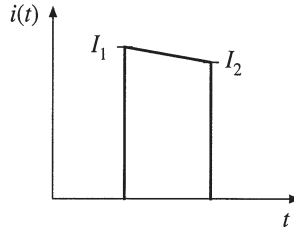


Fig. A.15

Sinusoidal segment, half or full period, Fig. A.16:

$$u_k = \frac{1}{2} I_{pk}^2 \quad (\text{A.16})$$

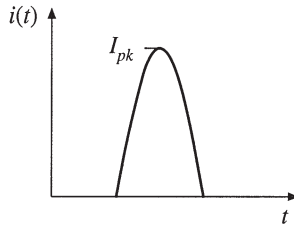


Fig. A.16

Sinusoidal segment, partial period: as in Fig. A.17, a sinusoidal segment of less than one half-period, which begins at angle θ_1 and ends at angle θ_2 . The angles θ_1 and θ_2 are expressed in radians:

$$u_k = \frac{1}{2} I_{pk}^2 \left(1 - \frac{\sin(\theta_2 - \theta_1) \cos(\theta_2 + \theta_1)}{(\theta_2 - \theta_1)} \right) \quad (\text{A.17})$$

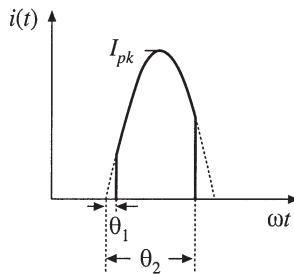


Fig. A.17

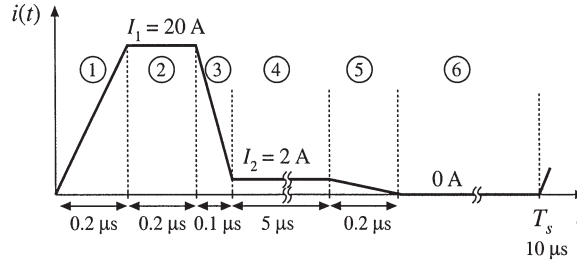


Fig. A.18 Example: an approximate transistor current waveform, including estimated current spike due to diode stored charge.

Example

A transistor current waveform contains a current spike due to the stored charge of a freewheeling diode. The observed waveform can be approximated as shown in Fig. A1.18. Estimate the rms current.

The waveform can be divided into six approximately linear segments, as shown. The D_k and u_k for each segment are

1. Triangular segment:

$$D_1 = (0.2 \mu s) / (10 \mu s) = 0.02$$

$$u_1 = I_1^2 / 3 = (20 \text{ A})^2 / 3 = 133 \text{ A}^2$$

2. Constant segment:

$$D_2 = (0.2 \mu s) / (10 \mu s) = 0.02$$

$$u_2 = I_1^2 = (20 \text{ A})^2 = 400 \text{ A}^2$$

3. Trapezoidal segment:

$$D_3 = (0.1 \mu s) / (10 \mu s) = 0.01$$

$$u_3 = (I_1^2 + I_2^2 + I_3^2) / 3 = 148 \text{ A}^2$$

4. Constant segment:

$$D_4 = (5 \mu s) / (10 \mu s) = 0.5$$

$$u_4 = I_2^2 = (2 \text{ A})^2 = 4 \text{ A}^2$$

5. Triangular segment:

$$D_5 = (0.2 \mu s) / (10 \mu s) = 0.02$$

$$u_5 = I_2^2 / 3 = (2 \text{ A})^2 / 3 = 1.3 \text{ A}^2$$

6. Zero segment:

$$u_6 = 0$$

The rms value is

$$rms = \sqrt{\sum_{k=1}^6 D_k u_k} = 3.76 \text{ A} \quad (\text{A.18})$$

Even though its duration is very short, the current spike has a significant impact on the rms value of the current—without the current spike, the rms current is approximately 2.0 A.

Appendix B

Simulation of Converters

Computer simulation can be a powerful tool in the engineering design process. Starting from design specifications, an initial design typically includes selection of system and circuit configurations, as well as component types and values. In this process, component and system models are constructed based on vendor-supplied data, and by applications of analysis and modeling techniques. These models, validated by experimental data whenever possible, are the basis upon which the designer can choose parameter values and verify the achieved performance against the design specifications. One must take into account the fact that actual parameter values will not match their nominal values because of inevitable production tolerances, changes in environmental conditions (such as temperature), and aging. In the design verification step, worst-case analysis (or other reliability and production yield analysis) is performed to judge whether the specifications are met under all conditions, i.e., for expected ranges of component parameter values. Computer simulation is very well suited for this task: using reliable models and appropriate simulation setups, the system performance can be tested for various sets of component parameter values. One can then perform design iterations until the worst-case behavior meets specifications, or until the system reliability and production yield are acceptably high.

In the design verification of power electronic systems by simulation, it is often necessary to use component and system models of various levels of complexity:

1. *Detailed, complex models that attempt to accurately represent physical behavior of devices.* Such models are necessary for tasks that involve finding switching times, details of switching transitions and switching loss mechanisms, or instantaneous voltage and current stresses. Component vendors often provide libraries of such device models. To complete a detailed circuit model, one must also carefully examine effects of packaging and board interconnects. With fast-switching power semiconductors, simulation time steps of a few nanoseconds or less may be required, especially during on/off switching transitions. Because of the complexity of detailed device models, and the fine time resolution, the simulation tasks can be very time consuming. In practice, time-domain simulations using detailed device models are usually performed only

on selected parts of the system, and over short time intervals involving a few switching cycles at most. Devices for power converters, and detailed physical device modeling, are areas of active research and development beyond the scope of this book.

2. *Simplified device models.* Since an on/off switching transition usually takes a small fraction of a switching cycle, the basic operation of switching power converters can be explained using simplified, idealized device models. For example, a MOSFET can be modeled as a switch with a small (ideally zero) on-resistance R_{on} when on, and a very large off-resistance (ideally an open circuit) when off. Such simplified models yield physical insight into the basic operation of switching power converters, and provide the starting point for developments of analytical models described throughout this book. Simplified device models are also useful for time-domain simulations aimed at verifying converter and controller operation, switching ripples, current and voltage stresses, and responses to load or input transients. Since device models are simple, and details of switching transitions are ignored, tasks that require simulations over many switching cycles can be completed efficiently using general-purpose circuit simulators. In addition, specialized tools have been developed to support fast transient simulation of switching power converters based on idealized, piecewise-linear device models [1-7], or a combination of piecewise-linear and nonlinear models [8].
3. *Averaged converter models.* Averaged models that are well suited for prediction of converter steady-state and dynamic responses are discussed throughout this book. These models are essential design tools because they provide physical insight and lead to analytical results that can be used in the design process to select component parameter values for a given set of specifications. In the design verification step, simulations of averaged converter models can be performed to test for losses and efficiency, steady-state voltages and currents, stability, and large-signal transient responses. Since switching transitions and ripples are removed by averaging, simulations over long time intervals and over many sets of parameter values can be completed efficiently. As a result, averaged models are also well suited for simulations of large electronic systems that include switching converters. Furthermore, since large-signal averaged models are nonlinear, but time-invariant, small-signal ac simulations can be used to generate various frequency responses of interest. Selected references on averaged converter modeling for simulation are listed at the end of this chapter [9-18].

Averaged models for computer simulation are covered in this appendix. Based on the material presented in Section 7.4, averaged switch models for computer simulation of converters operating in continuous conduction mode are described in Section B.1. Application examples include finding SEPIC dc conversion ratio and efficiency, and large-signal transient responses of a buck-boost converter. Section B.2 describes an averaged switch model suitable for simulation of converters that may operate either in continuous conduction mode or in discontinuous conduction mode. Application examples include finding SEPIC open-loop frequency responses in CCM and DCM, loop-gain, phase margin and closed-loop responses of a buck voltage regulator, and current harmonics in a DCM boost rectifier. Based on the results from Chapter 12, a simulation model for converters with current programmed control is described in Section B.3, together with a buck converter example that compares control-to-output frequency responses with current programmed control against duty-cycle control.

It is assumed that the reader is familiar with basics of Spice circuit simulations. All simulation models and examples in this appendix are prepared using the PSpice circuit simulator [19]. Netlists are included to help explain details of model implementation and simulation analysis options. Usually, instead of writing netlists, the user would enter circuit diagrams and analysis options from a front-end schematic capture tool. The examples and the library *switch.lib* of subcircuit models described in this appendix are available on-line. Similar models and examples can be constructed for use with other simulation tools.

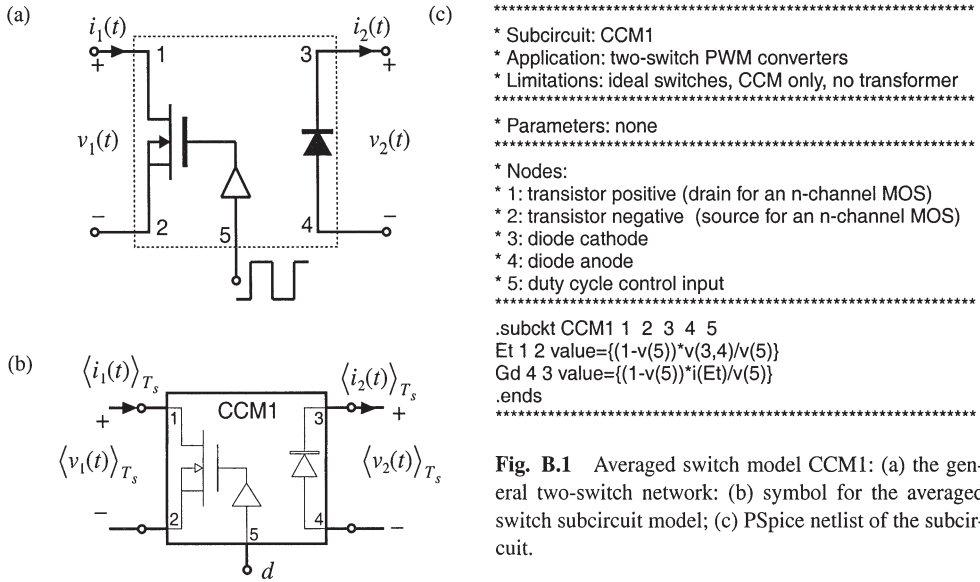


Fig. B.1 Averaged switch model CCM1: (a) the general two-switch network; (b) symbol for the averaged switch subcircuit model; (c) PSpice netlist of the subcircuit.

B.1 AVERAGED SWITCH MODELS FOR CONTINUOUS CONDUCTION MODE

The central idea of the *averaged switch modeling* described in Section 7.4 is to identify a switch network in the converter, and then to find an averaged circuit model. The resulting averaged switch model can then be inserted into the converter circuit to obtain a complete model of the converter. An important feature of the averaged switch modeling approach is that the same model can be used in many different converter configurations; it is not necessary to rederive an averaged equivalent circuit for each particular converter. This feature is also very convenient for construction of averaged circuit models for simulation. A general-purpose subcircuit represents a large-signal nonlinear averaged switch model. The converter averaged circuit for simulation is then obtained by replacing the switch network with this subcircuit. Based on the discussion in Section 7.4, subcircuits that represent CCM averaged switch models are described in this section, together with application examples.

B.1.1 Basic CCM Averaged Switch Model

The large-signal averaged switch model for the general two-switch network of Fig. 7.39(a) is shown in Fig. 7.39(c). A PSpice subcircuit implementation of this model is shown in Fig. B.1. The subcircuit has five nodes. The transistor port of the averaged switch network is connected between the nodes 1 and 2, while the diode port is comprised of nodes 3 and 4. The duty ratio $d = v(5)$ is the control input to the subcircuit at the node 5. The quantity $v(5)$ is a voltage that is equal to the duty cycle, and that lies in the range zero to one volt. Figure B.1(c) shows the netlist of the subcircuit. The netlist consists of only four lines of code and several comment lines (the lines starting with *). The `.subckt` line defines the name (CCM1) of the subcircuit and the interface nodes. The value of the controlled voltage source E_p , which

models the transistor port of the averaged switch network, is written according to Eq. (7.136):

$$\langle v_1(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle v_2(t) \rangle_{T_s} \quad (\text{B.1})$$

Note that $v(3,4)$ in the subcircuit of Fig. B.1 is equal to the switch network independent input $\langle v_2(t) \rangle_{T_s}$. Also, $d(t) = v(5)$, and $d'(t) = 1 - d(t) = 1 - v(5)$. The value of the controlled current source G_d , which models the diode port, is computed according to Eq. (7.137):

$$\langle i_2(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle i_1(t) \rangle_{T_s} \quad (\text{B.2})$$

The switch network independent input $\langle i_1(t) \rangle_{T_s}$ equals the current $i(E_r)$ through the controlled voltage source E_r . The .ends line completes the subcircuit netlist. The subcircuit CCM1 is included in the model library *switch.lib*.

An advantage of the subcircuit CCM1 of Fig. B.1 is that it can be used to construct an averaged circuit model for simulation of any two-switch PWM converter operating in continuous conduction mode, subject to the assumptions that the switches can be considered ideal, and that the converter does not include a step-up or step-down transformer. The subcircuit can be further refined to remove these limitations. In converters with an isolation transformer, the right-hand side of Eqs. (B.1) and (B.2) should be divided by the transformer turns ratio. Inclusion of switch conduction losses is discussed in the next section.

A disadvantage of the model in Fig. B.1 is that Eqs. (B.1) and (B.2) have a discontinuity at duty cycle equal to zero. In applications of the subcircuit, it is necessary to restrict the duty-cycle to the range $0 < D_{\min} \leq d \leq 1$.

Following the approach of this section, subcircuits can be constructed for the large-signal averaged models of the buck switch network (see Fig. 7.50(a), and Eqs. (7.150)), and the boost switch network (see Fig. 7.46(a) and Eqs. (7.146)). An advantage of these models is that their defining equations do not have the discontinuity problem at $d = 0$.

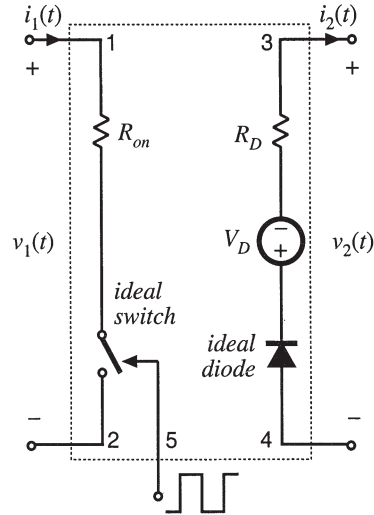
B.1.2 CCM Averaged Switch Model that Includes Switch Conduction Losses

Let us modify the model of Fig. B.1 to include switch conduction losses. Figure B.2 shows simple device models that include transistor and diode conduction losses in the general two-switch network of Fig. B.1(a). The transistor is modeled as an ideal switch in series with an on-resistance R_{on} . The diode is modeled as an ideal diode in series with a forward voltage drop V_D and resistance R_D .

Construction of dc equivalent circuits to find dc conversion ratio and efficiency of converters is discussed in Chapter 3. Derivation of an averaged switch model that includes conduction losses arising from R_{on} and V_D is described in Section 7.4.5. Following the same averaged switch modeling approach, we can find the following relationships that describe the averaged switch model for the switch network of Fig. B.2:

$$\langle v_1(t) \rangle_{T_s} = \left(\frac{R_{on}}{d(t)} + \frac{d'(t)R_D}{d^2(t)} \right) \langle i_1(t) \rangle_{T_s} + \frac{d'(t)}{d(t)} \left(\langle v_2(t) \rangle_{T_s} + V_D \right) \quad (\text{B.3})$$

Fig. B.2 Switch network model that includes conduction loss elements R_{on} , V_D and R_D .



(a)

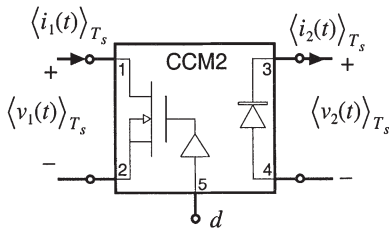


Fig. B.3 Subcircuit implementation of the CCM averaged switch model that includes conduction losses: (a) circuit symbol; (b) PSpice netlist for the subcircuit.

(b)

```
*****
* MODEL: CCM2
* Application: two-switch PWM converters, includes
*             conduction losses due to Ron, VD, RD
* Limitations: CCM only, no transformer
*****
* Parameters:
*   Ron = transistor on-resistance
*   VD = diode forward voltage drop
*   RD = diode on-resistance
*****
* Nodes:
*   1: transistor positive (drain for an n-channel MOS)
*   2: transistor negative (source for an n-channel MOS)
*   3: diode cathode
*   4: diode anode
*   5: duty cycle control input
*****
.subckt CCM2 1 2 3 4 5
+params: Ron=0 VD=0 RD=0
Er 1 1x value={i(Et)*(Ron+(1-v(5))*RD/v(5))/v(5)}
Et 1x 2 value={{(1-v(5))*v(3,4)+VD)/v(5)}}
Gd 4 3 value={{(1-v(5))*i(Et)/v(5)}}
.ends
*****
```

$$\langle i_2(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle i_1(t) \rangle_{T_s} \quad (\text{B.4})$$

A subcircuit implementation of the averaged switch model described by Eqs. (B.3) and (B.4) is shown in Fig. B.3. The subcircuit terminal nodes are the same as in the CCM1 subcircuit: the transistor port is between the nodes 1 and 2; the diode port is between the nodes 3 and 4; the duty ratio $d = v(5)$ is the con-

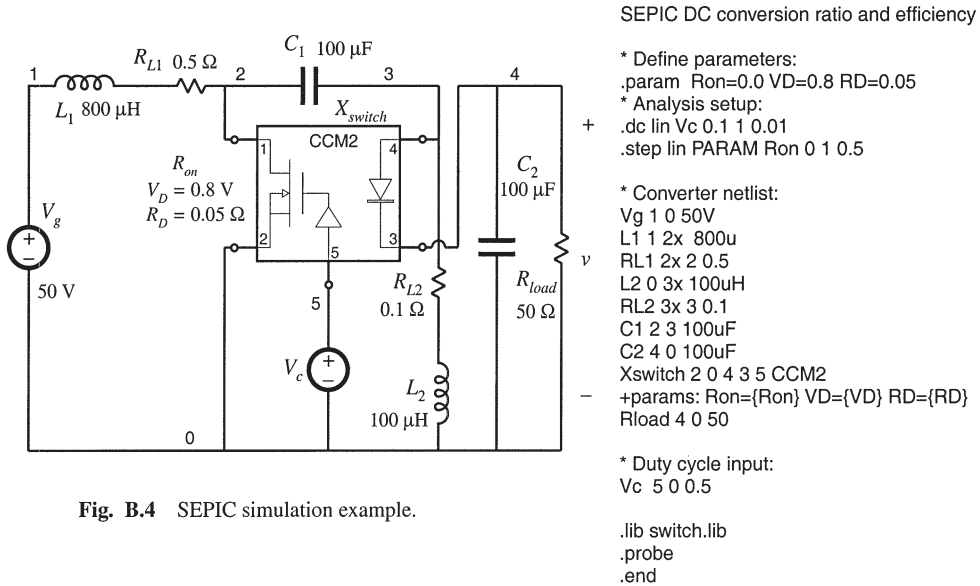


Fig. B.4 SEPIC simulation example.

trol input to the subcircuit at the node 5. Two controlled voltage sources in series, E_r and E_p , are used to generate the port 1 (transistor) averaged voltage according to Eq. (B.3). The controlled voltage source E_r models the voltage drop across the equivalent resistance $R_{on}/d(t) + d'(t)R_D/d^2(t)$ in Eq. (B.3). Note that this equivalent resistance is a nonlinear function of the switch duty cycle $d(t)$. The controlled voltage source E_p shows how the port 1 (transistor) averaged voltage depends on the port 2 (diode) averaged voltage. The controlled current source G_d models the averaged diode current according to Eq. (B.4). The subcircuit CCM2 has three parameters (R_{on} , V_D , and R_D) that can be specified when the subcircuit is used in a converter circuit. The default values of the subcircuit parameters, $R_{on} = 0$, $V_D = 0$, and $R_D = 0$, are defined in the .subckt line. These values correspond to the ideal case of no conduction losses. The subcircuit CCM2 is included in the model library *switch.lib*.

The model of Fig. B.3 is based on the simple device models of Fig. B.2. It is assumed that inductor current ripples are small and that the converter operates in continuous conduction mode. Many practical converters, however, must operate in discontinuous conduction mode at low duty cycles where the diode forward voltage drop is comparable to or larger than the output voltage. In such cases, the model of Fig. B.2, which includes V_D as a fixed voltage generator, gives incorrect, physically impossible results for polarities of converter voltages and currents, losses and efficiency.

B.1.3 Example: SEPIC DC Conversion Ratio and Efficiency

Let us consider an example of how the subcircuit CCM2 can be used to generate dc conversion ratio and efficiency curves for a CCM converter. As an example, Figure B.4 shows a SEPIC averaged circuit model. The converter circuit can be found in Fig. 6.38(a), or in Fig. 7.37. To construct the averaged circuit model for simulation, the switch network is replaced by the subcircuit CCM2. In the converter netlist shown in Fig. B.4, the X_{switch} line shows how the subcircuit is connected to other parts of the converter. The switch duty cycle is set by the voltage source V_c . All other parts of the converter circuit are simply copied to the averaged circuit model. Inductor winding resistances $R_{L1} = 0.5 \Omega$ and $R_{L2} = 0.1 \Omega$ are

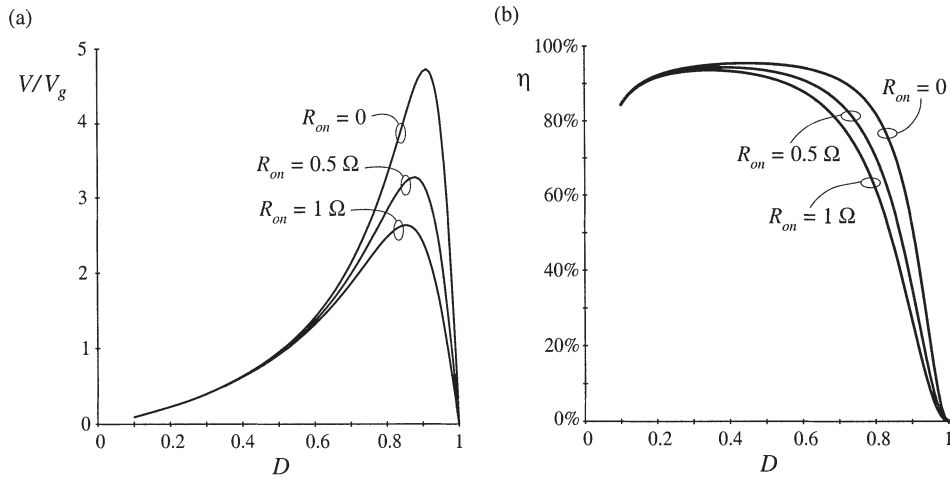


Fig. B.5 SEPIC simulation example: (a) dc conversion ratio and (b) efficiency.

included to model copper losses of the inductors L_1 and L_2 , respectively. The switch conduction loss parameters are defined by the .param line in the netlist: $R_{on} = 0$, $V_D = 0.8$ V, $R_D = 0.05 \Omega$. Notice how these values are passed to the subcircuit CCM2 in the X_{switch} line. In this example, all other losses in the converter are neglected. A dc sweep analysis (see the .dc line in the netlist) is set to vary the dc voltage source V_c from 0.1 V to 1 V, in 0.01 V increments, which corresponds to varying the switch duty cycle over the range from $D = 0.1$ to $D = 1$. The range of duty cycles from zero to 0.1 is not covered because of the model discontinuity problem at $D = 0$ (discussed in Section B.1.1), and because the model predictions for conduction losses at low duty cycles are not valid, as discussed in Section B.1.2. The dc sweep analysis is repeated for values of the switch on-resistance in the range from $R_{on} = 0 \Omega$ to $R_{on} = 1 \Omega$ in 0.5Ω increments (see the .step line in the netlist). The .lib line refers to the *switch.lib* library, which contains definitions of the subcircuit CCM2 and all other subcircuit models described in this appendix.

Simulation results for the dc output voltage V and the converter efficiency η are shown in Fig. B.5. Several observations can be made based on the modeling approach and discussions presented in Chapter 3. At low duty cycles, efficiency drops because the diode forward voltage drop is comparable to the output voltage. At higher duty cycles, the converter currents increase, so that the conduction losses increase. Eventually, for duty cycles approaching 1, both the output voltage and the efficiency approach zero. Given a desired dc output voltage and efficiency, the plots in Fig. B.5 can be used to select the transistor with an appropriate value of the on-resistance.

B.1.4 Example: Transient Response of a Buck–Boost Converter

In addition to steady-state conversion characteristics, it is often of interest to investigate converter transient responses. For example, in voltage regulator designs, it is necessary to verify whether the output voltage remains within specified limits when the load current takes a step change. As another example, during a start-up transient when the converter is powered up, converter components can be exposed to significantly higher stresses than in steady state. It is of interest to verify that component stresses are

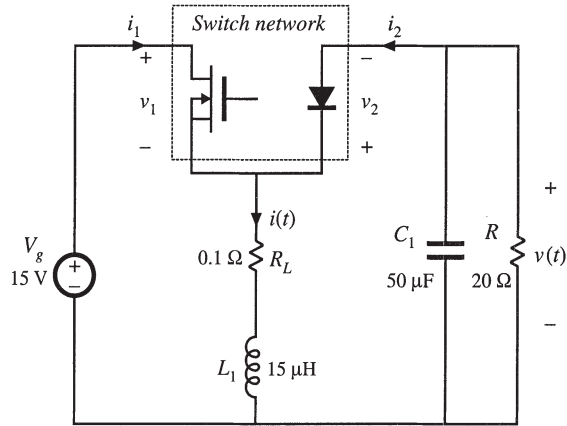


Fig. B.6 Buck-boost converter example.

within specifications or to make design modifications to reduce the stresses. In these examples, transient simulations can be used to test for converter responses.

Transient simulations can be performed on the converter switching circuit model or on the converter averaged circuit model. As an example, let us apply these two approaches to investigate a start-up transient response of the buck-boost converter shown in Fig. B.6.

Figure B.7 shows a switching circuit model of the buck-boost converter. The inductor winding resistance R_L is included to model the inductor copper losses. The MOSFET is modeled as a voltage-controlled switch S_{q1} controlled by a pulsating voltage source v_c . The switch .model line specifies the switch on-resistance $R_{on} = 50 \text{ m}\Omega$, and the switch off-resistance $R_{off} = 10 \text{ M}\Omega$. The switch is on when the controlling voltage v_c is greater than $V_{on} = 6 \text{ V}$, and off when the controlling voltage v_c is less than $V_{off} = 4 \text{ V}$. The pulsating source v_c has the pulse amplitude equal to 10 V. The period is $T_s = 1/f_s = 10 \mu\text{s}$, the rise and fall times are $t_r = t_f = 100 \text{ ns}$, and the pulse width is $t_p = 7.9 \mu\text{s}$. The switch duty cycle is $D = (t_p + 0.5(t_r + t_f))/T_s = 0.8$. The built-in nonlinear Spice model is used for the diode. In the diode .model statement, only the parameter I_s is specified, to set the forward voltage drop across the diode. The switch and the diode models used in this example are very simple. Conduction losses are modeled in a simple manner, and details of complex device behavior during switching transitions are neglected.

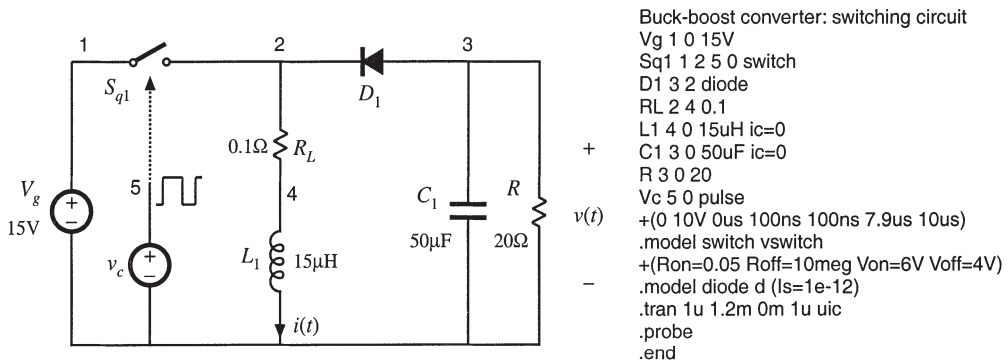


Fig. B.7 Buck-boost converter simulation example, switching circuit model.

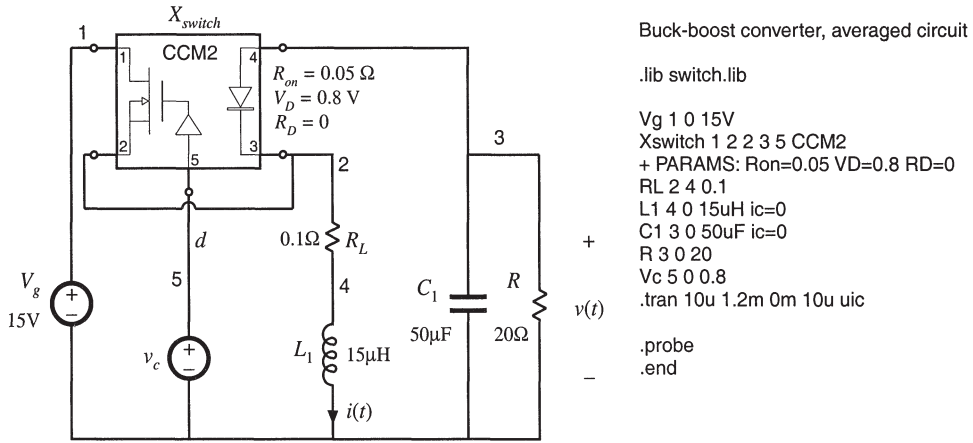


Fig. B.8 Buck-boost converter simulation example, averaged circuit model.

Therefore, the circuit model of Fig. B.7 cannot be used to examine switching transitions or to predict switching losses in the converter. Nevertheless, basic switching operation is modeled, and a transient simulation can be used to find out how the converter waveforms evolve in time over many switching cycles. Transient simulation parameters are defined by the .tran line: the output time step is 1 μ s, the final simulation time is 1.2 ms, the output waveforms are generated from the start of simulation at time equal to zero, and the maximum allowed time step is 1 μ s. The uic (“use initial conditions”) option tells the simulator to start with all capacitor voltages and inductor currents equal to the specified initial values. For example, ic=0 in the L_1 line sets the initial inductor current to zero. In Spice, the default initial conditions are always zero, so that ic=0 statements can be omitted.

An averaged circuit model of the buck-boost converter is shown in Fig. B.8. This circuit model is obtained by replacing the switch network in the converter of Fig. B.6 by the CCM2 subcircuit. Notice that the circuits and the netlists of Figs. B.7 and Fig. B.8 are very similar. The only difference is that the switching devices in the converter circuit of Fig. B.7 are replaced by the CCM2 subcircuit X_{switch} in Fig. B.8. Also, the pulsating source $v_c(t)$ in the switching circuit is replaced by a constant voltage source v_c equal to the switch duty cycle $D = 0.8$.

The inductor current and the capacitor voltage waveforms during the start-up transient are shown in Fig. B.9. For comparison, the waveforms obtained by transient simulation of the switching converter circuit shown in Fig. B.7, and by simulation of the averaged circuit model of Fig. B.8 are shown. Switching ripples can be observed in the waveforms obtained by simulation of the switching circuit model. The converter transient response is governed by the converter natural time constants. Since these time constants are much longer than the switching period, the converter start-up transient responses in Fig. B.9 take many switching cycles to reach the steady state. In the results obtained by simulation of the averaged circuit model, the switching ripples are removed, but the low-frequency portions of the converter transient responses, which are governed by the natural time constants of the converter network, match very closely the responses obtained by simulation of the switching circuit.

Based on the results shown in Fig. B.9, we can see that converter components are exposed to significantly higher current stresses during the start-up transient than during steady state operation. The problem of excessive stresses in the start-up transient is quite typical for switching power converters. Practical designs usually include a “soft-start” circuit, where the switch duty cycle is slowly increased

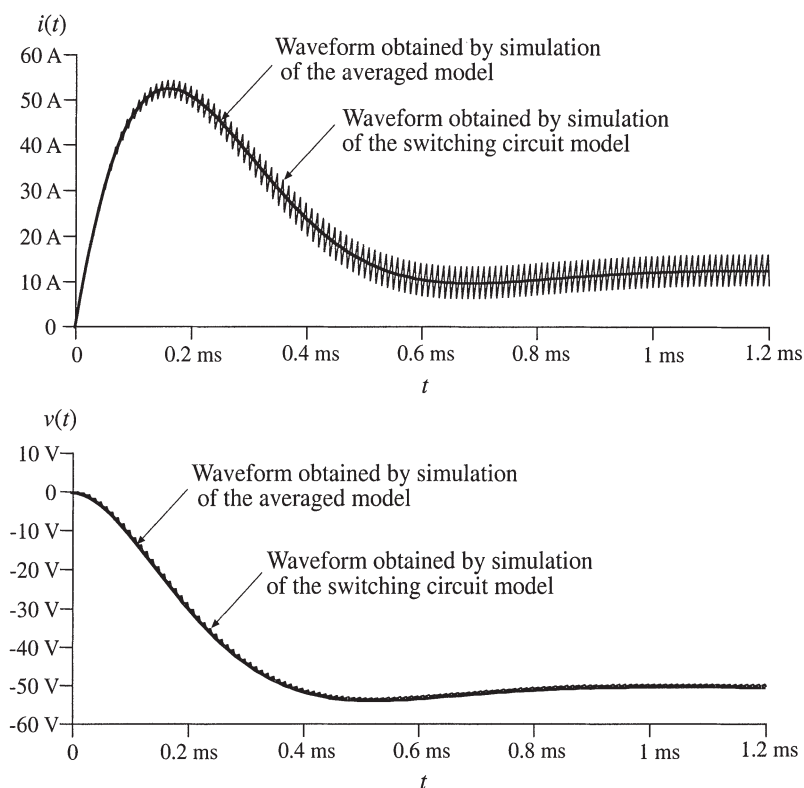


Fig. B.9 Inductor current and output voltage waveforms obtained by transient simulation of the switching converter circuit shown in Fig. B.7, and by simulation of the averaged circuit model of Fig. B.8

from zero to the steady-state value to reduce start-up transient stresses.

This simulation example illustrates how an averaged circuit model can be used in place of a switching circuit model to investigate converter large-signal transient responses. An advantage of the averaged circuit model is that transient simulations can be completed much more quickly because the averaged model is time invariant, and the simulator does not spend time computing the details of the fast switching transitions. This advantage can be important in simulations of larger electronic systems that include switching power converters. Another important advantage also comes from the fact that the averaged circuit model is nonlinear but time-invariant: ac simulations can be used to linearize the model and generate small-signal frequency responses of interest. This is not possible with switching circuit models. Examples of small-signal ac simulations can be found in Sections B.2 and B.3.

B.2 COMBINED CCM/DCM AVERAGED SWITCH MODEL

The models and examples of Section B.1 are all based on the assumption that the converters operate in continuous conduction mode (CCM). As discussed in Chapters 5 and 11, all converters containing a diode rectifier operate in discontinuous conduction mode (DCM) if the load current is sufficiently low. In some cases, converters are purposely designed to operate in DCM. It is therefore of interest to develop

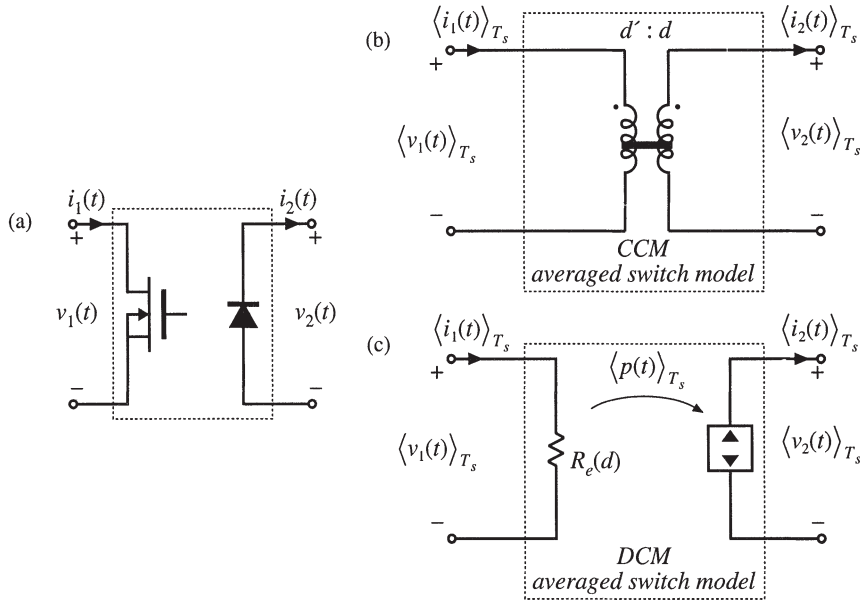


Fig. B.10 Summary of averaged switch modeling: (a) general two-switch network, (b) averaged switch model in CCM, and (c) averaged switch model in DCM.

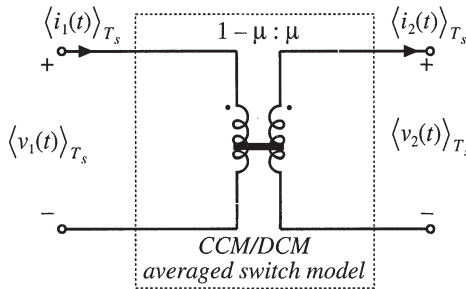


Fig. B.11 A general averaged switch model using the equivalent switch conversion ratio μ .

averaged models suitable for simulation of converters that may operate in either CCM or DCM.

Figure B.10 illustrates the general two-switch network, and the corresponding large-signal averaged models in CCM and DCM. The CCM averaged switch model, which is derived in Section 7.4, is an ideal transformer with $d' : d$ turns ratio. In DCM, the large-signal averaged switch model is a loss-free resistor, as derived in Section 11.1. Our objective is to construct a combined CCM/DCM averaged switch model that reduces to the model of Fig. B.10(a) or to the model of Fig. B.10(c) depending on the operating mode of the converter. Let us define an effective switch conversion ratio $\mu(t)$, so that the averaged switch model in both modes has the same form as in CCM, as shown in Fig. B.11. If the converter operates in CCM, then the switch conversion ratio $\mu(t)$ is equal to the switch duty cycle $d(t)$,

$$\mu = d \quad (\text{B.5})$$

If the converter operates in DCM, then the effective switch conversion ratio can be computed so that the terminal characteristics of the averaged-switch model of Fig. B.11 match the terminal characteristics of the loss-free resistor model of Fig. B.10(c). Matching the port 1 characteristics gives

$$\langle v_1(t) \rangle_{T_s} = \frac{1-\mu}{\mu} \langle v_2(t) \rangle_{T_s} = R_e \langle i_1(t) \rangle_{T_s} \quad (\text{B.6})$$

which can be solved for the switch conversion ratio μ ,

$$\mu = \frac{1}{R_e \langle i_1(t) \rangle_{T_s} + \langle v_2(t) \rangle_{T_s}} \quad (\text{B.7})$$

It can be verified that matching the port 2 characteristics of the models in Figs. B.10(c) and B.11 gives exactly the same result for the effective switch conversion ratio in DCM.

The switch conversion ratio $\mu(t)$ can be considered a generalization of the duty cycle $d(t)$ of CCM switch networks. Based on this approach, models and results developed for converters in CCM can be used not only for DCM but also for other operating modes or even for other converter configurations by simply replacing the switch duty cycle $d(t)$ with the appropriate switch conversion ratio $\mu(t)$ [21-24]. For example, if $M(d)$ is the conversion ratio in CCM, then $M(\mu)$, with μ given by Eq. (B.7), is the conversion ratio in DCM. The switch conversion ratio in DCM depends on the averaged terminal voltage and current, as well as the switch duty cycle d through the effective resistance $R_e = 2L/d^2T_s$. If the converter is completely unloaded, then the average transistor current $\langle i_1(t) \rangle_{T_s}$ is zero, and the DCM switch conversion ratio becomes $\mu = 1$. As a result, the dc output voltage attains the maximum possible value $V = V_g M(1)$. This is consistent with the results of the steady-state DCM analyses in Chapter 5 and Section 11.1.

To construct a combined CCM/DCM averaged switch model based on the general averaged switch model of Fig. B.11, it is necessary to specify which of the two expressions for the switch conversion ratio to use: Eq. (B.5), which is valid in CCM, or Eq. (B.7), which is valid in DCM. At the CCM/DCM boundary, these two expressions must give the same result, $\mu = d$. If the load current decreases further, the converter operates in DCM, the average switch current $\langle i_1(t) \rangle_{T_s}$ decreases, and the DCM switch conversion ratio in Eq. (B.7) becomes greater than the switch duty cycle d . We conclude that the correct value of the switch conversion ratio, which takes into account operation in CCM or DCM, is the larger of the two values computed using Eq. (B.5) and Eq. (B.7).

Figure B.12 shows an implementation of the combined CCM/DCM model as a PSpice subcircuit CCM-DCM1. This subcircuit has the same five interface nodes as the subcircuits CCM1 and CCM2 of Section B.1. The controlled sources E_t and G_d model the port 1 (transistor) and port 2 (diode) averaged characteristics, as shown in Fig. B.11. The switch conversion ratio μ is equal to the voltage $v(u)$ at the subcircuit node u . The controlled voltage source E_u computes the switch conversion ratio as the greater of the two values obtained from Eqs. (B.5) and (B.7). The controlled current source G_a , the zero-value voltage source V_a , and the resistor R_a form an auxiliary circuit to ensure that the solution found by the simulator has the transistor and the diode currents with correct polarities, $\langle i_1(t) \rangle_{T_s} > 0$, $\langle i_2(t) \rangle_{T_s} > 0$. The subcircuit parameters are the inductance L relevant for CCM/DCM operation, and the switching frequency f_s . The default values in the subcircuit are arbitrarily set to $L = 100 \mu\text{H}$ and $f_s = 100 \text{ kHz}$.

The PSpice subcircuit CCM-DCM1 of Fig. B.12 can be used for dc, ac, and transient simula-

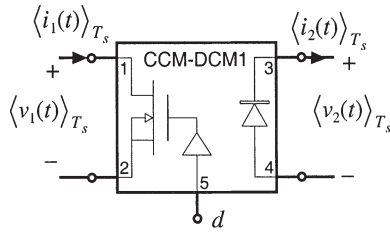


Fig. B.12 Implementation of the combined CCM/DCM averaged switch model.

```
*****
* MODEL: CCM-DCM1
* Application: two-switch PWM converters, CCM or DCM
* Limitations: ideal switches, no transformer
*****
* Parameters:
*   L = equivalent inductance for DCM
*   fs = switching frequency
*****
* Nodes:
* 1: transistor positive (drain for an n-channel MOS)
* 2: transistor negative (source for an n-channel MOS)
* 3: diode cathode
* 4: diode anode
* 5: duty cycle control input
*****
.subckt CCM-DCM1 1 2 3 4 5
+ params: L=100u fs=1E5
Et 1 2 value={{(1-v(u))*v(3,4)/v(u)}}
Gd 4 3 value={{(1-v(u))*i(Et)/v(u)}}
Ga 0 a value={MAX(i(Et),0)}
Va a b
Ra b 0 1k
Eu u 0 table {MAX(v(5),
+ v(5)*v(5)/(v(5)*v(5)+2*L*fs*(Va)/v(3,4))} (0 0) (1 1)
.ends
*****
```

tions of PWM converters containing a transistor switch and a diode switch. This subcircuit is included in the model library *switch.lib*. It can be modified further for use in converters with isolation transformer.

B.2.1 Example: SEPIC Frequency Responses

As an example, Fig. B.13 shows a SEPIC circuit and the averaged circuit model obtained by replacing the switch network with the CCM-DCM1 subcircuit of Fig. B.12. A part of the circuit netlist is included in Fig. B.13. The connections and the parameters of the CCM-DCM1 subcircuit are defined by the X_{switch} line. In the SEPIC, the inductance parameter $L = 83.3 \mu\text{H}$ is equal to the parallel combination of L_1 and L_2 . The voltage source v_c sets the quiescent value of the duty cycle to $D = 0.4$, and the small-signal ac value to $\hat{d} = 1$. Ac simulation is performed on a linearized circuit model, so that amplitudes of all small-signal ac waveforms are directly proportional to the amplitude of the ac input, regardless of the input ac amplitude value. For example, the control-to-output transfer function is $G_{vd} = \hat{v}/\hat{d}$, where $\hat{v} = v(4)$ in the circuit of Fig. B.13(b). We can set the input ac amplitude to 1, so that the control-to-output transfer function G_{vd} can be measured directly as $v(5)$. This setup is just for convenience in finding small-signal frequency responses by simulation. For measurements of converter transfer functions in an experimental circuit (see Section 8.5), the actual amplitude of the small-signal ac variation $\hat{d}$ would be set to a fraction of the quiescent duty cycle D . Parameters of the ac simulation are set by the .ac line in the netlist: the signal frequency is swept from the minimum frequency of 5 Hz to the maximum frequency of 50 kHz in 201 points per decade.

Figure B.14 shows magnitude and phase responses of the control-to-output transfer function obtained by ac simulations for two different values of the load resistance: $R = 40 \Omega$, for which the converter operates in CCM, and $R = 50 \Omega$, for which the converter operates in DCM. For these two operating

points, the quiescent (dc) voltages and currents in the circuit are nearly the same. Nevertheless, the frequency responses are qualitatively very different in the two operating modes. In CCM, the converter exhibits a fourth-order response with two pairs of high- Q complex-conjugate poles and a pair of complex-conjugate zeros. Another RHP (right-half plane) zero can be observed at frequencies approaching 50 kHz. In DCM, there is a dominant low-frequency pole followed by a pair of complex-conjugate poles and a pair of complex-conjugate zeros. The frequencies of the complex poles and zeros are very close in value. A high-frequency pole and a RHP zero contribute additional phase lag at higher frequencies.

In the design of a feedback controller around a converter that may operate in CCM or in DCM, one should take into account that the crossover frequency, the phase margin, and the closed-loop responses can be substantially different depending on the operating mode. This point is illustrated by the example of the next section.

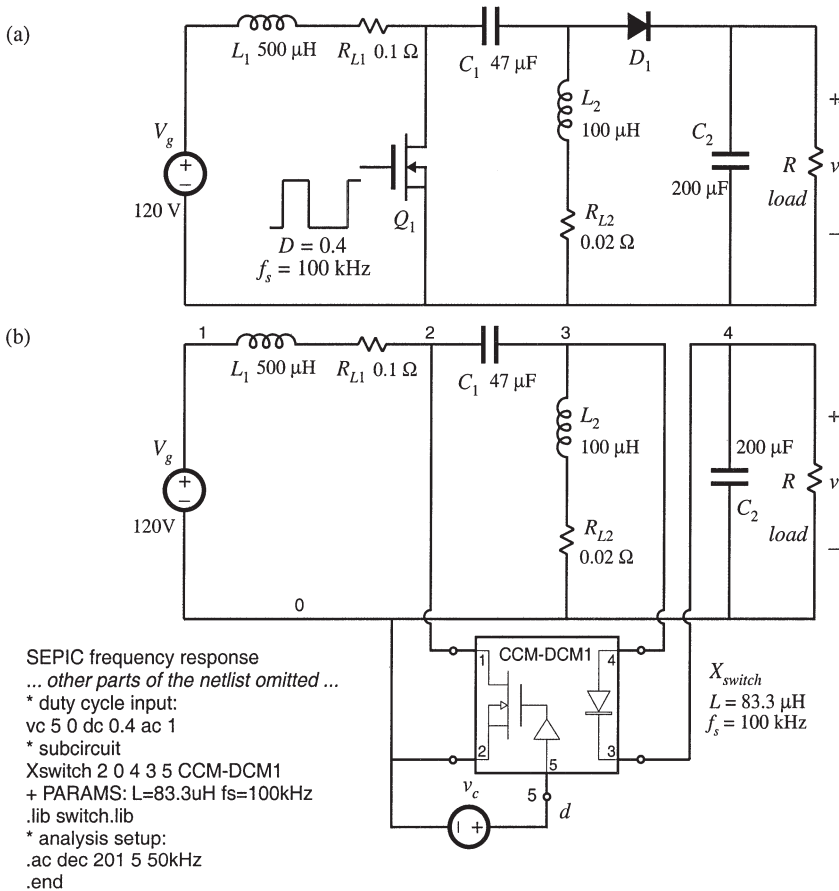


Fig. B.13 SEPIC simulation example: (a) converter circuit, (b) averaged circuit model for simulation.

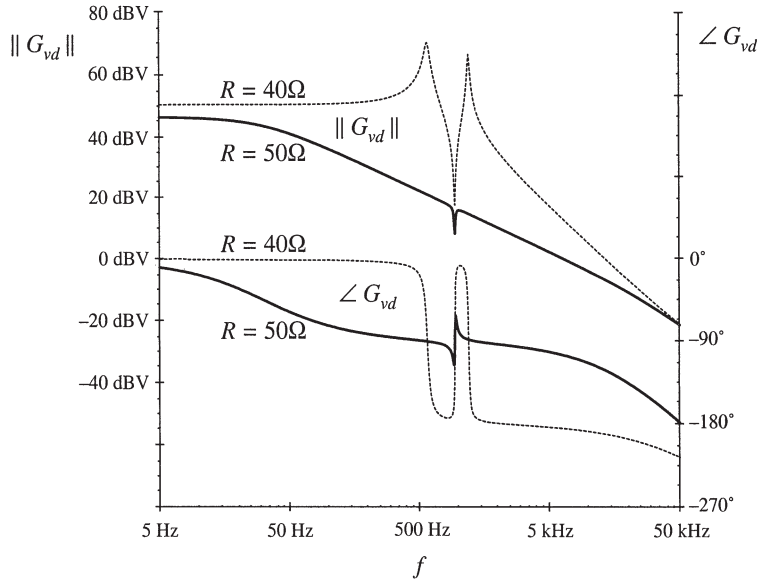


Fig. B.14 Magnitude and phase responses of the control-to-output transfer function obtained by simulation of the SEPIC example, for two values of the load resistance. For $R = 50 \Omega$, the converter operates in DCM (solid lines), and for $R = 40 \Omega$, the converter operates in CCM (dotted lines).

B.2.2 Example: Loop Gain and Closed-Loop Responses of a Buck Voltage Regulator

A controller design for a buck converter example is discussed in Section 9.5.4. The converter and the block diagram of the controller are shown in Fig. 9.22. This converter system is designed to regulate the dc output voltage at $V = 15 \text{ V}$ for the load current up to 5 A . Let us test this design by simulation. An averaged circuit model of a practical realization of the buck voltage regulator described in Section 9.5.4 is shown in Fig. B.15. The MOSFET and the diode switch are replaced by the averaged switch model implemented as the CCM-DCM1 subcircuit. The pulse-width modulator with $V_M = 4 \text{ V}$ is modeled according to the discussion in Section 7.6 as a dependent voltage source E_{pwm} controlled by the PWM input voltage v_x . The value of E_{pwm} is equal to $1/V_M = 0.25$ times the PWM input voltage v_x , with a limit for the minimum value set to 0.1 V , and a limit for the maximum value set to 0.9 V . The output of the pulse-width modulator is the control duty-cycle input to the CCM-DCM1 averaged switch subcircuit. Given the specified limits for E_{pwm} , the switch duty cycle $d(t)$ can take values in the range:

$$D_{\min} \leq d(t) \leq D_{\max} \quad (\text{B.8})$$

where $D_{\min} = 0.1$, and $D_{\max} = 0.9$. Practical PWM integrated circuits often have a limit $D_{\max} < 1$ for the maximum possible duty cycle. The voltage sensor and the compensator are implemented around an op-amp LM324. With very large loop gain in the system, the steady-state error voltage is approximately zero, i.e., the dc voltages at the plus and the minus inputs of the op-amp are almost the same,

$$G_{cm}H = \frac{R_3}{R_1 + R_2} \quad (\text{B.13})$$

$$f_z = \frac{\omega_z}{2\pi} = \frac{1}{2\pi R_2 C_2} \quad (\text{B.14})$$

$$f_L = \frac{\omega_L}{2\pi} = \frac{1}{2\pi R_3 C_3} \quad (\text{B.15})$$

and

$$f_p = \frac{\omega_p}{2\pi} = \frac{1}{2\pi(R_1 \parallel R_2)C_2} \quad (\text{B.16})$$

The design described in Section 9.5.4 resulted in the following values for the gain and the corner frequencies:

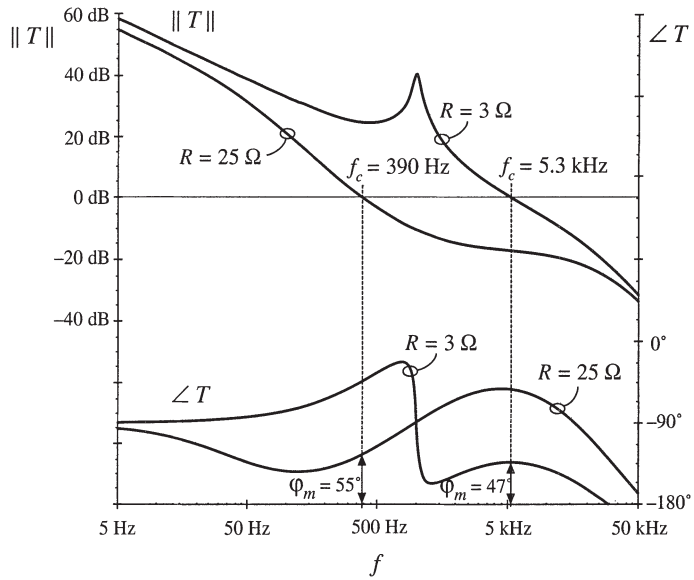
$$G_{cm}H = 3.7 (1/3) = 1.23, \quad f_z = 1.7 \text{ kHz}, \quad f_L = 500 \text{ Hz}, \quad f_p = 14.5 \text{ kHz} \quad (\text{B.17})$$

Eqs. (B.10) and (B.13) to (B.17) can be used to select the circuit parameter values. Let us (somewhat arbitrarily) choose $C_2 = 1.1 \text{ nF}$. Then, from Eq. (B.14), we have $R_2 = 85 \text{ k}\Omega$, and Eq. (B.16) yields $R_1 = 11 \text{ k}\Omega$. From Eq. (B.13) we obtain $R_3 = 120 \text{ k}\Omega$, and Eq. (B.15) gives $C_3 = 2.7 \text{ k}\Omega$. Finally, $R_4 = 47 \text{ k}\Omega$ is found from Eq. (B.10). The voltage regulator design can now be tested by simulations of the circuit in Fig. B.15.

Loop gains can be obtained by simulation using exactly the same techniques described in Section 9.6 for experimental measurement of loop gains [20]. Let us apply the voltage injection technique of Section 9.6.1. An ac voltage source v_z is injected between the compensator output and the PWM input. This is a good injection point since the output impedance of the compensator built around the op-amp is small, and the PWM input impedance is very large (infinity in the circuit model of Fig. B.15). With the ac source amplitude set (arbitrarily) to 1, and no other ac sources in the circuit, ac simulations are performed to find the loop gain as

$$T(s) = \frac{\hat{v}_y}{\hat{v}_x} = -\frac{v(6)}{v(7)} \quad (\text{B.18})$$

To perform ac analysis, the simulator first solves for the quiescent (dc) operating point. The circuit is then linearized at this operating point, and small-signal frequency responses are computed for the specified range of signal frequencies. Solving for the quiescent operating point involves numerical solution of a system of nonlinear equations. In some cases, the numerical solution does not converge and the simulation is aborted with an error message. In particular, convergence problems often occur in circuits with feedback, especially when the loop gain at dc is very large. This is the case in the circuit of Fig. B.15. To help convergence when the simulator is solving for the quiescent operating point, one can specify approximate or expected values of node voltages using the .nodeset line as shown in Fig. B.15. In this case, we know by design that the quiescent output voltage is close to 15 V ($v(3) = 15$), that the negative input of the op-amp is very close to the reference ($v(5) = 5$), and that the quiescent duty cycle is approximately $D = V/V_g = 0.536$, so that $v(8) = 0.536 \text{ V}$. Given these approximate node voltages, the numerical solution converges, and the following quiescent operating points are found by the simulator for two values of the load resistance R :

Fig. B.16 Loop gain in the buck voltage regulator example.

$$R = 3 \, \Omega, v(3) = 15.2 \, \text{V}, v(5) = 5.0 \, \text{V}, v(7) = 2.173 \, \text{V}, v(8) = 0.543 \, \text{V}, D = 0.543 \quad (\text{B.19})$$

$$R = 25 \, \Omega, v(3) = 15.2 \, \text{V}, v(5) = 5.0 \, \text{V}, v(7) = 2.033 \, \text{V}, v(8) = 0.508 \, \text{V}, D = 0.508 \quad (\text{B.20})$$

For the nominal load resistance $R = 3 \, \Omega$, the converter operates in CCM, so that $D = V/V_g$. For $R = 25 \, \Omega$, the same dc output voltage is obtained for a lower value of the quiescent duty cycle, which means that the converter operates in DCM.

The magnitude and phase responses of the loop gain found for the operating points given by Eqs. (B.19) and (B.20) are shown in Fig. B.16. For $R = 3 \, \Omega$, the crossover frequency is $f_c = 5.3 \, \text{kHz}$, and the phase margin is $\phi_M = 47^\circ$, very close to the values ($f_c = 5 \, \text{kHz}$, $\phi_M = 52^\circ$) that we designed for in Section 9.5.4. At light load, for $R = 25 \, \Omega$, the loop gain responses are considerably different because the converter operates in DCM. The crossover frequency drops to $f_c = 390 \, \text{Hz}$, while the phase margin is $\phi_M = 55^\circ$.

The magnitude responses of the line-to-output transfer function are shown in Fig. B.17, again for two values of the load resistance, $R = 3 \, \Omega$ and $R = 25 \, \Omega$. The open-loop responses are obtained by braking the feedback loop at node 8, and setting the dc voltage at this node to the quiescent value D of the duty cycle. For $R = 3 \, \Omega$, the open-loop and closed-loop responses can be compared to the theoretical plots shown in Fig. 9.32. At 100 Hz, the closed-loop magnitude response is $0.012 \Rightarrow -38 \, \text{dB}$. A 1 V, 100 Hz variation in $v_g(t)$ would induce a 12 mV variation in the output voltage $v(t)$. For $R = 25 \, \Omega$, the closed loop magnitude response is $0.02 \Rightarrow -34 \, \text{dB}$, which means that the 1 V, 100 Hz variation in $v_g(t)$ would induce a 20 mV variation in the output voltage. Notice how the regulator performance in terms of rejecting the input voltage disturbance is significantly worse at light load than at the nominal load.

A test of the transient response to a step change in load is shown in Fig. B.18. The load current is initially equal to 1.5 A, and increases to $i_{\text{LOAD}} = 5 \, \text{A}$ at $t = 0.1 \, \text{ms}$. When the converter is operated in

Fig. B.17 Line to output response of the buck voltage regulator.

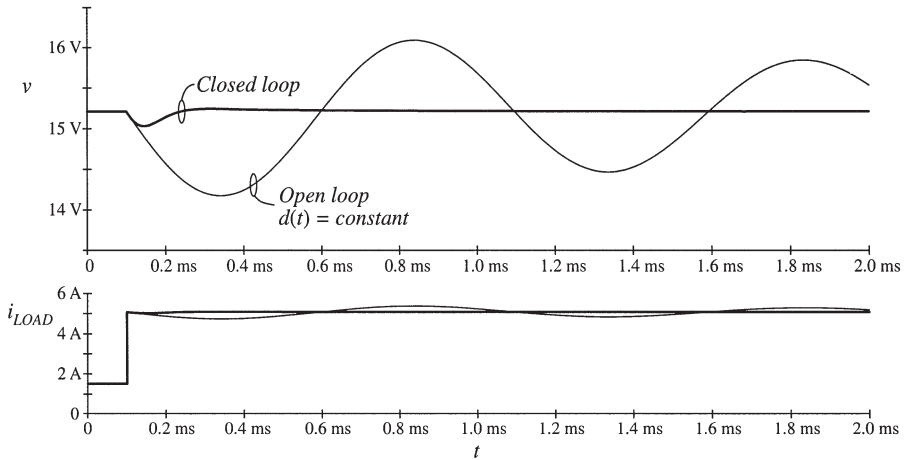
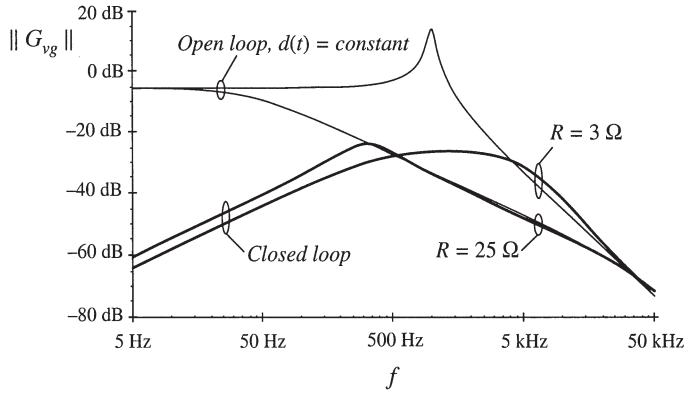


Fig. B.18 Load transient response of the buck voltage regulator example.

open loop at constant duty cycle, the response is governed by the natural time constants of the converter network. A large undershoot and long lightly-damped oscillations can be observed in the output voltage. With the feedback loop closed, the controller dynamically adjusts the duty cycle $d(t)$ trying to maintain the output voltage constant. The output voltage drops by about 0.2 V, and it returns to the regulated value after a short, well-damped transient.

The voltage regulator example of Fig. B.15 illustrates how the performance can vary significantly if the regulator is expected to supply a wide range of loads. In practice, further tests would also be performed to account for expected ranges of input voltages, and variations in component parameter values. Design iterations may be necessary to ensure that performance specifications are met under worst case conditions.

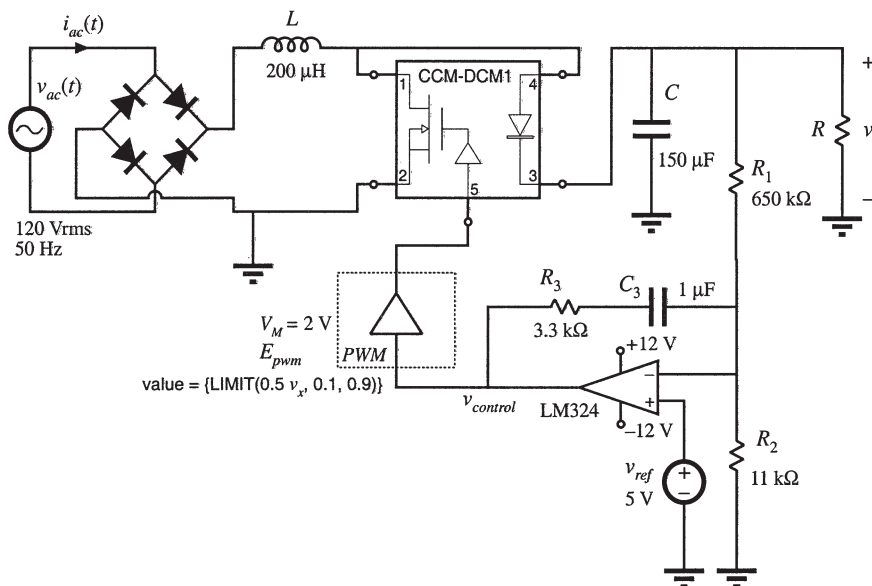


Fig. B.19 DCM boost rectifier example.

B.2.3 Example: DCM Boost Rectifier

Converters switching at frequencies much above the ac line frequency can be used to construct near-ideal rectifiers where power is taken from the ac line without generation of line current harmonics. Approaches to construction of low-harmonic rectifiers are discussed in Chapter 18. One simple solution is based on the boost converter operating in discontinuous conduction mode, as described in Section 18.2.1. When a boost DCM converter operates at a constant switch duty cycle, the input current approximately follows the input voltage. The DCM effective resistance $2L/d^2(t)T_s$ is an approximation of the emulated resistance R_e of the DCM boost rectifier. Ac line current harmonics are not zero, but the rectifier can still be designed to meet harmonic limits. In this section we consider a DCM boost rectifier example and test its performance by simulation.

An averaged circuit model of the boost DCM rectifier is shown in Fig. B.19. Full-wave rectified 120 Vrms, 50 Hz ac line voltage is applied to the input of the boost converter. The converter switches are replaced by the CCM-DCM1 averaged switch subcircuit. It is desired to regulate the dc output voltage at $V = 300$ V at output power up to $P_{out} = 120$ W across the load R . The switching frequency is $f_s = 100$ kHz. Let us select the inductance L so that the converter always operates in DCM. From Eq. (18.24), the condition for DCM is:

$$L < \frac{\left(1 - \frac{V_M}{V}\right) R_e}{2f_s} \quad (\text{B.21})$$

where R_e is the emulated resistance of the rectifier and V_M is the peak of the ac line voltage. When line

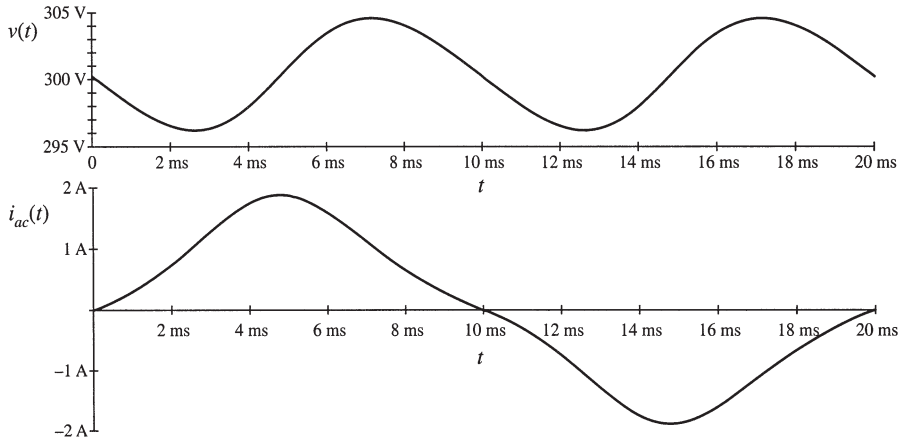


Fig. B.20 Output voltage and ac line current in the DCM boost rectifier example.

current harmonics and losses are neglected, the rectifier emulated resistance R_e at the specified load power P is

$$R_e = \frac{V_M^2}{2P} \quad (\text{B.22})$$

Given $V_M = 170$ V and R_e found from Eq. (B.22), Eq. (B.21) gives $L < 260$ μH . The selected inductance is $L = 200$ μH . A low-bandwidth voltage feedback loop is closed around the converter to regulate the dc output voltage. The output voltage is sensed and compared to the reference v_{ref} . A PI compensator is constructed around the LM324 op-amp. The output $v_{control}$ of the compensator is the input to the pulse-width modulator. By adjusting the switch duty ratio d , $v_{control}$ adjusts the emulated resistance $R_e = 2L/d^2T_s$ of the rectifier, and thereby controls the power taken from the ac line. In steady state, the input power matches the output power. The dc output voltage V is regulated at the value set by the reference voltage v_{ref} and the voltage divider composed of R_1 and R_2 , as follows:

$$V = v_{ref} \frac{R_1 + R_2}{R_1} = 300 \text{ V} \quad (\text{B.23})$$

Modeling of the low-bandwidth voltage regulation loop is discussed in Section 18.4.2.

It is of interest to find ac line current harmonics. First, a long transient simulation is performed to reach steady-state operation. Then, current harmonics are computed using Fourier analysis applied to the ac line current waveform $i_{ac}(t)$ during one line cycle in steady state. Figure B.20 shows the steady-state ac line current and output voltage obtained for $R = 900$ Ω , i.e., for 100 W of output power. The output voltage has a dc component equal to 300 V, and an ac ripple component at twice the line frequency. The peak-to-peak voltage ripple at twice the line frequency is approximately 8 V, which compares well with the value (7 V) found from Eq. (18.91). The ac line current has noticeable distortion. The spectrum of the ac line current is shown in Fig. B.21. The largest harmonic, the third, has an amplitude of 16.6% of the fundamental, and the total harmonic distortion is 16.7%.

We can also examine what happens if the rectifier is overloaded. The steady-state ac line current waveform for the case when the load resistance is $R = 500$ Ω , and the output power is 180 W, is shown in

Fig. B.21 Spectrum of the ac line current in the DCM boost rectifier.

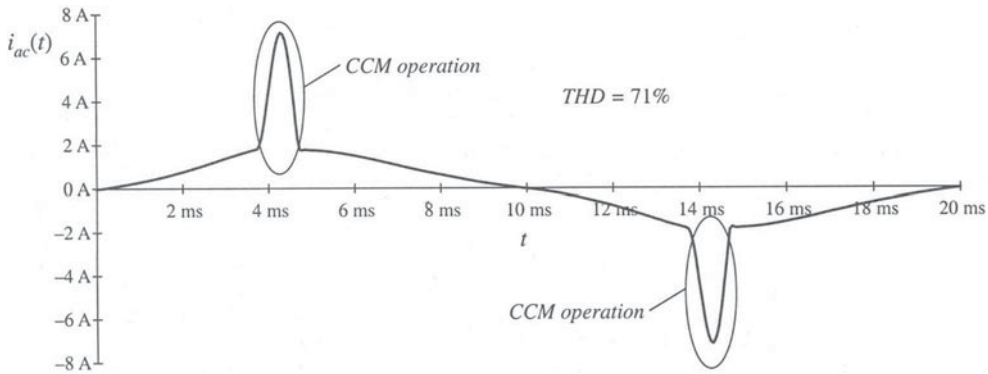
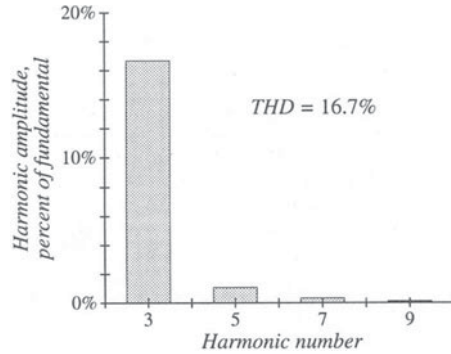


Fig. B.22 Ac line current of the DCM boost rectifier example, when the output is overloaded.

Fig. B.22. The boost converter operates in CCM near the peak of the ac line voltage; this results in current spikes and significant harmonic distortion.

B.3 CURRENT PROGRAMMED CONTROL

In the current programmed mode (CPM), which is studied in Chapter 12, the transistor switching is controlled so that the peak transistor current follows a control signal. The transistor duty cycle $d(t)$ is not directly controlled, but depends on the CPM control input as well as on other converter voltages and currents. In this section, large-signal averaged relationships in CPM are written in a form suitable for implementation as a subcircuit for simulation.

B.3.1 Current Programmed Mode Model for Simulation

Typical inductor current and voltage waveforms of CPM converters operating in continuous conduction mode or in discontinuous conduction mode are shown in Fig. B.23. Signal $i_c(t)$ is the CPM control input. An artificial ramp having slope $-m_a$ is added to the control input. In the first subinterval,

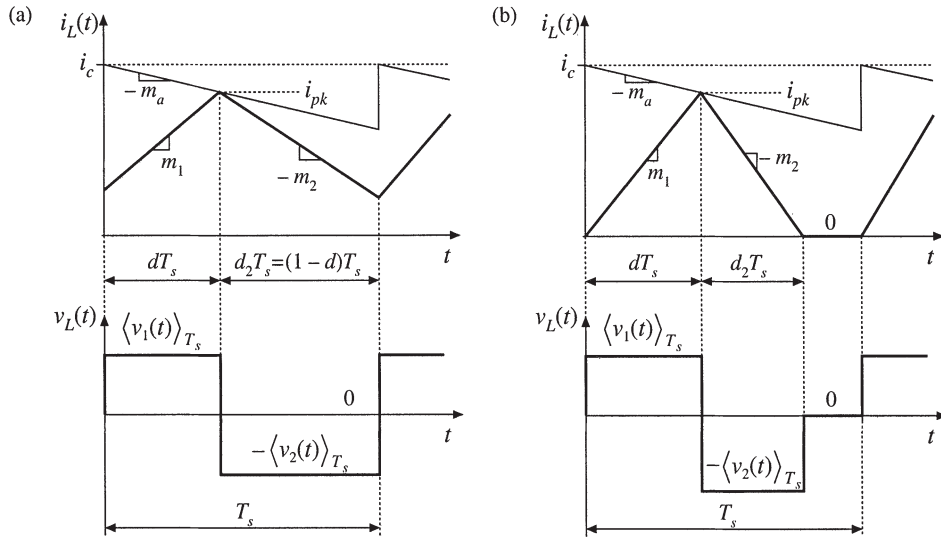


Fig. B.23 Current programmed mode waveforms: (a) continuous conduction mode; (b) discontinuous conduction mode.

when the transistor is on, the inductor current increases with slope m_1 given by:

$$m_1 = \frac{\langle v_1(t) \rangle_{T_s}}{L} \quad (\text{B.24})$$

It is assumed that voltage ripples are small so that the voltage $v_1(t)$ across the inductor is approximately equal to the averaged value $\langle v_1(t) \rangle_{T_s}$. The length of the first subinterval is $d(t)T_s$. The transistor is turned off when the inductor current reaches the peak value i_{pk} equal to:

$$i_{pk} = i_c - m_a d T_s \quad (\text{B.25})$$

In the second subinterval, when the transistor is off and the diode is on, the inductor current decreases with a negative slope $-m_2$. With the assumption the voltage ripples are small, the slope m_2 is given by:

$$m_2 = \frac{\langle v_2(t) \rangle_{T_s}}{L} \quad (\text{B.26})$$

The length of the second subinterval is $d_2(t)T_s$. In CCM, the second subinterval lasts until the end of the switching cycle. Therefore:

$$d_2 = 1 - d \quad (\text{B.27})$$

In DCM, the current drops to zero before the end of the switching period. The length of the second subinterval can be computed from:

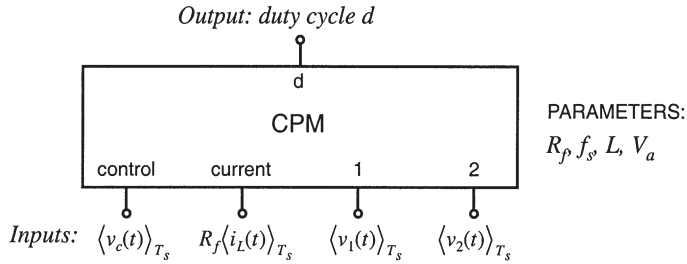


Fig. B.24 Current programmed mode (CPM) subcircuit.

$$d_2 = \frac{i_{pk}}{m_2 T_s} \quad (\text{B.28})$$

If the converter operates in DCM, d_2 computed from Eq. (B.28) is smaller than $1 - d$. If the converter operates in CCM, $1 - d$ is smaller than d_2 computed from Eq. (B.28). In general, the length of the second subinterval can be found as the smaller of the two values computed using Eqs. (B.27) and (B.28).

The average inductor current can be found by computing the area under the inductor current waveform in Fig. B.23:

$$\langle i_L(t) \rangle_{T_s} = d \left(i_{pk} - \frac{m_1 d T_s}{2} \right) + d_2 \left(i_{pk} - \frac{m_2 d_2 T_s}{2} \right) \quad (\text{B.29})$$

The relationship given by Eq. (B.29) is valid for both CCM and DCM provided that the second subinterval length is computed as the smaller of the values obtained from Eqs. (B.27) and (B.28).

Based on Eqs. (B.24) to (B.29), an averaged CPM subcircuit model is constructed in the form shown in Fig. B.24. The inputs to the CPM subcircuit are the control input $\langle v_c(t) \rangle_{T_s} = R_f \langle i_c(t) \rangle_{T_s}$, the measured inductor current $R_f \langle i_L(t) \rangle_{T_s}$, and the inductor voltages $\langle v_1(t) \rangle_{T_s}$ and $\langle v_2(t) \rangle_{T_s}$ of the two subintervals. The output of the subcircuit is the switch duty cycle d . The parameters of the CPM subcircuit are the equivalent current-sense resistance R_f , the inductance L , the switching frequency $f_s = 1/T_s$, and the amplitude V_a of the artificial ramp:

$$V_a = m_a T_s R_f \quad (\text{B.30})$$

In the subcircuit implementation, the length of the second subinterval is computed as the smaller of the values given by Eqs. (B.27) and (B.28):

$$d_2 = \text{MIN} \left(1 - d, \frac{i_{pk}}{m_2 T_s} \right) \quad (\text{B.31})$$

Next, the switch duty cycle is found by solving Eq. (B.29). There are many different ways the switch duty cycle can be expressed in terms of other quantities. Although mathematically equivalent to Eq. (B.29), these different forms of solving for d result in different convergence performance of the numerical solver in the simulator. In the CPM subcircuit available in the *switch.lib* library, the duty cycle is found from:

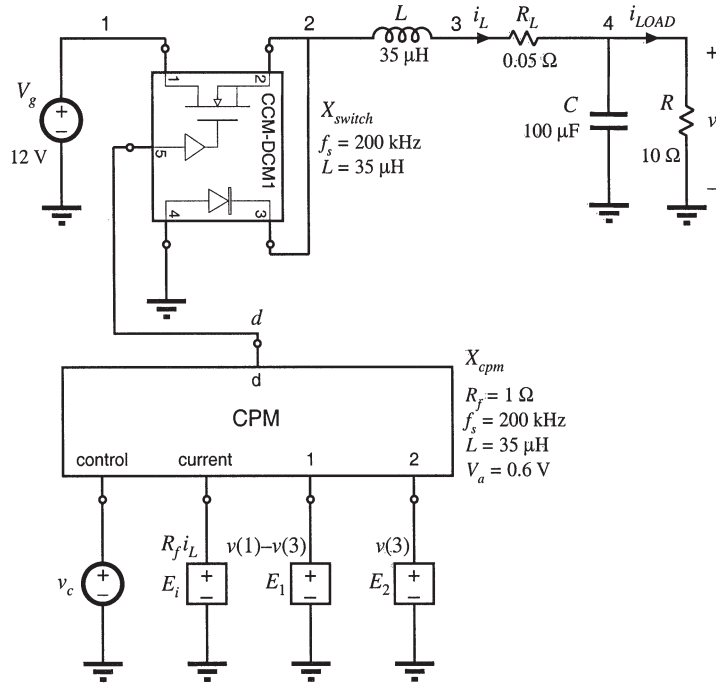


Fig. B.25 CPM buck converter example.

$$d = \frac{2i_c(d + d_2) - 2\langle i_L(t) \rangle_{T_s} - m_2 d_2^2 T_s}{2m_d(d + d_2)T_s + m_1 d T_s} \quad (\text{B.32})$$

which is obtained by inserting Eq. (B.25) into Eq. (B.29). This implicit expression (notice that d is on both sides of the equation) is used by the numerical solver in the simulator to compute the switch duty cycle d .

B.3.2 Example: Frequency Responses of a Buck Converter with Current Programmed Control

To illustrate an application of the CPM subcircuit, let us consider the example buck converter circuit model of Fig. B.25. To construct this averaged circuit model, the switches are replaced by the CCM-DCM1 averaged switch subcircuit. The control input to the CPM subcircuit is the independent voltage source v_c . Three dependent voltage sources are used to generate other inputs to the CPM subcircuit. The controlled voltage source E_i is proportional to the inductor current i_L . The controlled voltage source E_1 is equal to $v(1) - v(3)$, which is equal to the voltage $\langle v_1(t) \rangle_{T_s}$ applied across the inductor during the first subinterval when the transistor is on and the diode is off. The controlled voltage source E_2 is equal to $v(3)$, which is equal to the voltage $\langle v_2(t) \rangle_{T_s}$ applied across the inductor during the second subinterval when the transistor is off and the diode is on.

Ac simulations are performed at the quiescent operating point obtained for the dc value of the

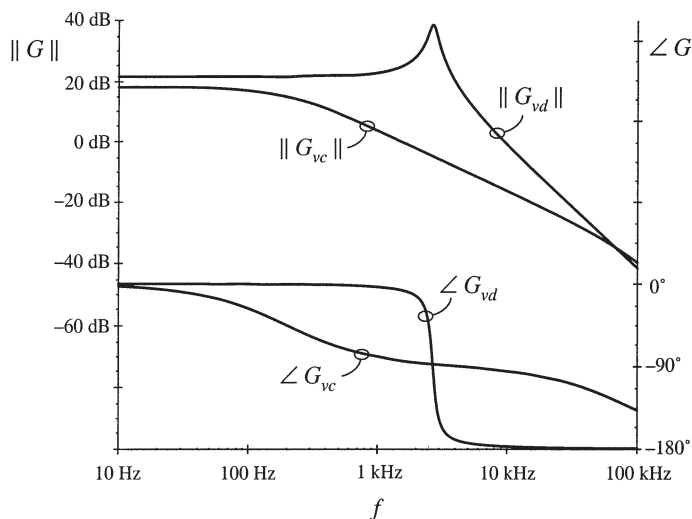


Fig. B.26 Comparison of CPM control with duty-cycle control, for the control-to-output frequency response of the buck converter example.

control input equal to $V_c = 1.4$ V. At the quiescent operating point, the switch duty cycle is $D = 0.676$, the dc output voltage is $V = 8.1$ V, and the dc component of the inductor current is $I_L = 0.81$ A. The converter operates in CCM.

Magnitude and phase responses of the control-to-output transfer functions $G_{vc}(s) = \hat{v}/\hat{v}_c$ and $G_{vd}(s) = \hat{v}/\hat{d}$ are shown in Fig. B.26. The duty-cycle to output voltage transfer function $G_{vd}(s)$ exhibits the familiar second-order high-Q response. Peaking in the magnitude response and a steep change in phase from 0° to -180° occur around the center frequency of the pair of complex-conjugate poles. In contrast, the CPM control-to-output response has a dominant low-frequency pole. The phase lag is around -90° in a wide range of frequencies. A high frequency pole contributes to additional phase lag at higher frequencies. The frequency responses of Fig. B.26 illustrate an advantage of CPM control over duty-cycle control. Because of the control-to-output frequency response dominated by the single low-frequency pole, it can be much easier to close a wide-bandwidth outer voltage feedback loop around the CPM controlled power converter than around a converter where the duty cycle is the control input.

Another advantage of CPM control is in rejection of input voltage disturbances. Line-to-output frequency responses for duty-cycle control and CPM control in the buck example are compared in Fig. B.27. At practically all frequencies of interest, CPM control offers more than 30 dB better attenuation of input voltage disturbances.

It is also interesting to compare the output impedance of the converter with duty-cycle control versus CPM control. The results are shown in Fig. B.28. At low frequencies, duty-cycle controlled converter has very low output impedance determined by switch and inductor resistances. As the frequency goes up, the output impedance increases as the impedance of the inductor increases. At the resonant frequency of the output LC filter, significant peaking in the output impedance of the duty-cycle controlled converter can be observed. At higher frequencies, the output impedance is dominated by the impedance of the filter capacitor, which decreases with frequency. In the CPM controlled converter, the low-frequency impedance is high. It is equal to the parallel combination of the load resistance and the CPM out-

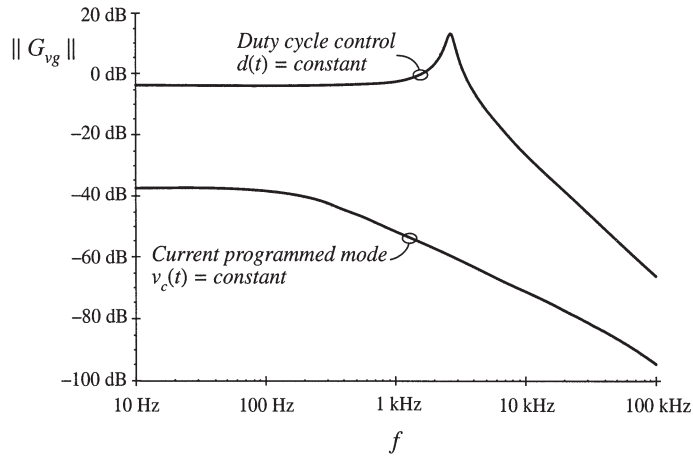


Fig. B.27 Comparison of CPM control with duty-cycle control, for the line-to-output frequency response of the buck converter example.

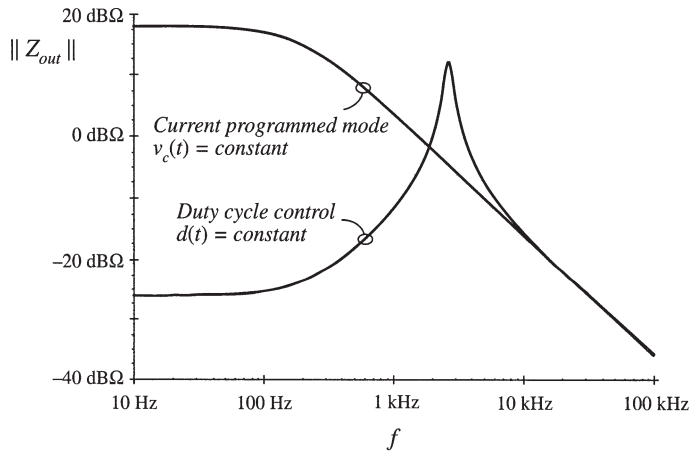


Fig. B.28 Comparison of CPM control with duty-cycle control, for the output impedance of the buck converter example.

put resistance. Because of the lossless damping introduced by CPM control, the series inductor does not affect the output impedance. As the frequency goes up, the output impedance becomes dominated by the output filter capacitor and it decreases with frequency. At high frequencies the output impedances of the duty-cycle and CPM controlled converters have the same asymptotes.

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Appendix C

Middlebrook's Extra Element Theorem

The *Extra Element Theorem* of R. D. Middlebrook [1–3] shows how a transfer function is changed by the addition of an impedance to the network. The theorem allows one to determine the effects of this extra element on any transfer function of interest, without solving the system all over again. The Extra Element Theorem is a powerful technique of design-oriented analysis. It leads to impedance inequalities which guarantee that an element does not substantially alter a transfer function. The Extra Element Theorem is employed in Chapter 10, where it leads to a relatively simple methodology for designing input filters that do not degrade the loop gains of switching regulators. It is also employed in Section 19.4, to determine how the load resistance affects the properties of a resonant inverter. In this appendix, Middlebrook's Extra Element Theorem is derived, based on the principle of superposition. Its application is illustrated via examples.

C.1 BASIC RESULT

Consider the linear circuit of Fig. C.1(a). This network contains an input $v_{in}(s)$ and an output $v_{out}(s)$. In addition, it contains a port whose terminals are open-circuited. It is assumed that the transfer function from $v_{in}(s)$ to $v_{out}(s)$ is known, and is given by

$$\frac{v_{out}(s)}{v_{in}(s)} = G(s) \Big|_{Z(s) \rightarrow \infty} \quad (\text{C.1})$$

The Extra Element Theorem tells us how the transfer function $G(s)$ is modified when an impedance $Z(s)$ is connected between the terminals at the port, as in Fig. C.1(b). The result is

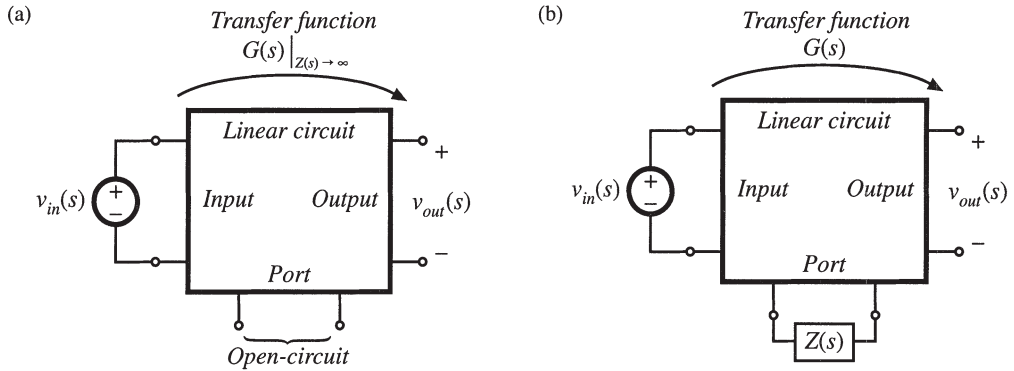


Fig. C.1 How an added element changes a transfer function $G(s)$: (a) original conditions, before addition of the new element; (b) addition of element having impedance $Z(s)$.

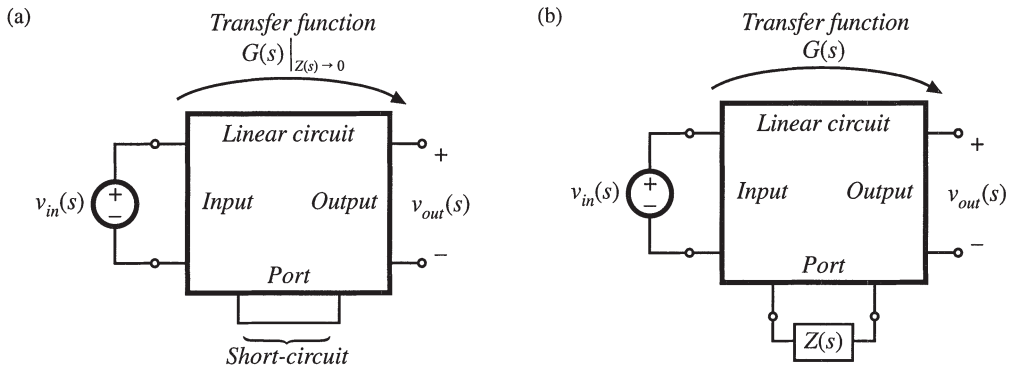


Fig. C.2 The dual form of the Extra Element Theorem, in which the extra element replaces a short circuit: (a) original conditions, (b) addition of element having impedance $Z(s)$.

$$\frac{v_{out}(s)}{v_{in}(s)} = \left(G(s) \big|_{Z(s) \rightarrow \infty} \right) \left(\frac{1 + \frac{Z_N(s)}{Z(s)}}{1 + \frac{Z_D(s)}{Z(s)}} \right) \quad (\text{C.2})$$

The right-hand side terms involving $Z(s)$ account for the influence of $Z(s)$ on $G(s)$, and are known as the *correction factor*.

The Extra Element Theorem also applies to the dual form illustrated in Fig. C.2. In this form, the transfer function is initially known under the conditions that the port is short-circuited. In Fig. C.2(b), the short-circuit is replaced by the impedance $Z(s)$. In this case, the addition of the impedance $Z(s)$ causes the transfer function to become

$$\frac{v_{out}(s)}{v_{in}(s)} = \left(G(s) \big|_{Z(s) \rightarrow 0} \right) \left(\frac{1 + \frac{Z(s)}{Z_N(s)}}{1 + \frac{Z(s)}{Z_D(s)}} \right) \quad (\text{C.3})$$

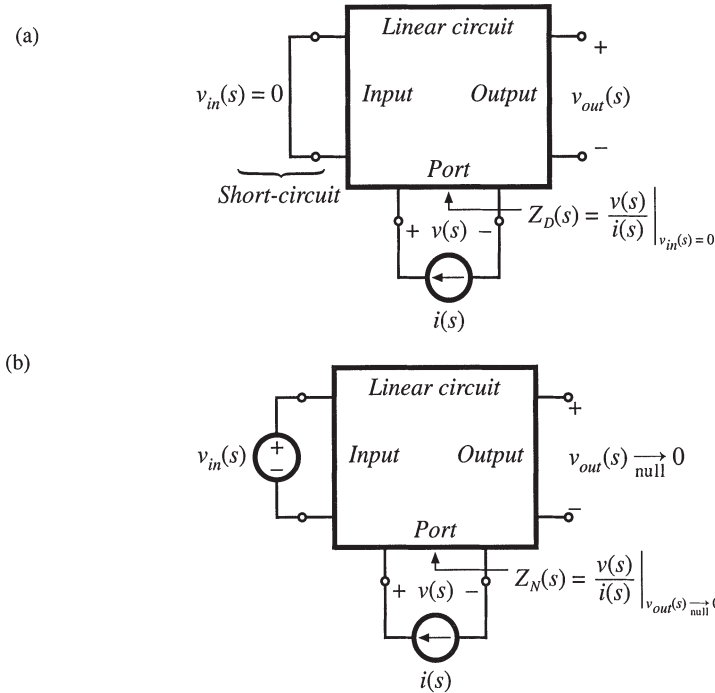


Fig. C.3 Determination of the quantities $Z_N(s)$ and $Z_D(s)$: (a) $Z_D(s)$ is the Thevenin-equivalent impedance at the port, and is measured with the input $v_{in}(s)$ set to zero; (b) $Z_N(s)$ is the impedance seen at the port under the condition that the output is nulled.

The $Z_N(s)$ and $Z_D(s)$ terms in Eqs. (C.2) and (C.3) are identical. By equating the $G(s)$ expressions of Eqs. (C.2) and (C.3), one can show that

$$\frac{G(s) \Big|_{Z(s) \rightarrow \infty}}{G(s) \Big|_{Z(s) \rightarrow 0}} = \frac{Z_D(s)}{Z_N(s)} \quad (\text{C.4})$$

This is known as the *reciprocity relationship*.

The quantities $Z_N(s)$ and $Z_D(s)$ can be found by measuring impedances at the port. The term $Z_D(s)$ is the Thevenin equivalent impedance seen looking into the port, also known as the driving-point impedance. As illustrated in Fig. C.3(a), this impedance is found by setting the independent source $v_{in}(s)$ to zero, and then measuring the impedance between the terminals of the port:

$$Z_D(s) = \frac{v(s)}{i(s)} \Big|_{v_{in}(s)=0} \quad (\text{C.5})$$

Thus, $Z_D(s)$ is the impedance between the port terminals when the input $v_{in}(s)$ is set to zero.

Determination of the impedance $Z_N(s)$ is illustrated in Fig. C.3(b). The term $Z_N(s)$ is found under the conditions that the output $v_{out}(s)$ is *nulled* to zero. A current source $i(s)$ is connected to the terminals of the port. In the presence of the input signal $v_{in}(s)$, the current $i(s)$ is adjusted so that the output $v_{out}(s)$ is nulled to zero. Under these conditions, the quantity $Z_N(s)$ is given by

$$Z_N(s) = \left. \frac{v(s)}{i(s)} \right|_{v_{out}(s) \xrightarrow{\text{null}} 0} \quad (\text{C.6})$$

Note that *nulling* the output is not the same as *shorting* the output. If one simply shorted the output, then a current would flow through the short, which would induce voltage drops and currents in other elements of the network. These voltage drops and currents are not present when the output is nulled. The null condition of Fig. C.3(b) does not employ any connections to the output of the circuit. Rather, the null condition employs the adjustment of the independent sources $v_{in}(s)$ and $i(s)$ in a special way that causes the output $v_{out}(s)$ to be zero. By superposition, $v_{out}(s)$ can be expressed as a linear combination of $v_{in}(s)$ and $i(s)$; therefore, for a given $v_{in}(s)$, it is always possible to choose an $i(s)$ that will cause $v_{out}(s)$ to be zero. Under these null conditions, $Z_N(s)$ is measured as the ratio of $v(s)$ to $i(s)$. In practice, the circuit analysis to find $Z_N(s)$ is simpler than analysis of $Z_D(s)$, because the null condition causes many of the signals within the circuit to be zero. Several examples are given in Section C.4.

The input and output quantities need not be voltages, but could also be currents or other signals that can be set or nulled to zero. The next section contains a derivation of the Extra Element Theorem with a general input $u(s)$ and output $y(s)$.

C.2 DERIVATION

Figure C.4(a) illustrates a general linear system having an input $u(s)$ and an output $y(s)$. In addition, the system contains an electrical port having voltage $v(s)$ and current $i(s)$, with the polarities illustrated. Initially, the port is open-circuited: $i(s) = 0$. The transfer function of this system, with the port open-circuited, is

$$G_{old}(s) = \left. \frac{y(s)}{u(s)} \right|_{i(s)=0} \quad (\text{C.7})$$

The objective of the extra element theorem is to determine the new transfer function $G(s)$ that is obtained when an impedance $Z(s)$ is connected to the port:

$$G(s) = \frac{y(s)}{u(s)} \quad (\text{C.8})$$

The situation is illustrated in Fig. C.4(b). It can be seen that the conditions at the port are now given by

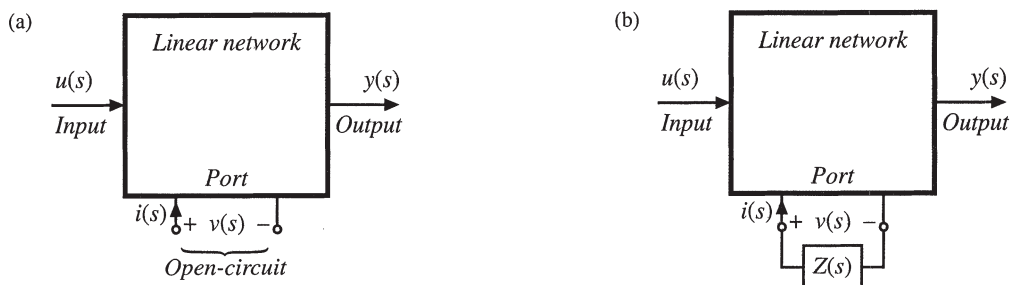
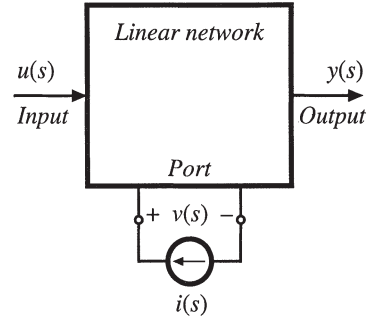


Fig. C.4 Modification of a linear network by addition of an extra element: (a) original system, (b) modified system, with impedance $Z(s)$ connected at an electrical port.

Fig. C.5 Current injection at the electrical port, by addition of independent current source $i(s)$.



$$v(s) = -i(s)Z(s) \quad (\text{C.9})$$

To express the new transfer function $G(s)$ in Eq. (C.8) in terms of the original transfer function $G_{old}(s)$ of Eq. (C.7), we use current injection at the port, as illustrated in Fig. C.5. There are now two independent inputs: the input $u(s)$ and the independent current source $i(s)$. The dependent quantities $y(s)$ and $v(s)$ can be expressed as functions of these independent inputs using the principle of superposition:

$$y(s) = G_{old}(s)u(s) + G_i(s)i(s) \quad (\text{C.10})$$

$$v(s) = G_v(s)u(s) + Z_D(s)i(s) \quad (\text{C.11})$$

where

$$G_{old}(s) = \left. \frac{y(s)}{u(s)} \right|_{i(s)=0} \quad (\text{C.12})$$

$$G_i(s) = \left. \frac{y(s)}{i(s)} \right|_{u(s)=0} \quad (\text{C.13})$$

$$Z_D(s) = \left. \frac{v(s)}{i(s)} \right|_{u(s)=0} \quad (\text{C.14})$$

$$G_v(s) = \left. \frac{v(s)}{u(s)} \right|_{i(s)=0} \quad (\text{C.15})$$

are the transfer functions from the independent inputs to the respective dependent quantities $y(s)$ and $v(s)$.

The transfer function $G(s)$ can be found by elimination of $v(s)$ and $i(s)$ from the system of equations (C.9) to (C.11), and solution for $y(s)$ as a function of $u(s)$. The result is

$$G(s) = \frac{y(s)}{u(s)} = G_{old}(s) - \frac{G_v(s)G_i(s)}{Z(s) + Z_D(s)} \quad (\text{C.16})$$

This intermediate result expresses the new transfer function $G(s)$ as a function of the original transfer function $G_{old}(s)$ and the extra element $Z(s)$, as well as the quantities $Z_D(s)$, $G_v(s)$, and $G_i(s)$.

Equation (C.14) gives a direct way to find the quantity $Z_D(s)$. $Z_D(s)$ is the driving-point impedance at the port, when the input $u(s)$ is set to zero. This quantity can be found either by conventional circuit analysis or simulation, or by laboratory measurement.

Although $G_v(s)$ and $G_i(s)$ could also be determined from the definitions (C.13) and (C.15), it is preferable to eliminate these quantities, and instead express $G(s)$ as a function of the impedances at the given port. This can be accomplished via the following thought experiment. In the presence of the input $u(s)$, we adjust the independent current source $i(s)$ in the special way that causes the output $y(s)$ to be nulled to zero. The impedance $Z_N(s)$ is defined as the ratio of $v(s)$ to $i(s)$ under these null conditions:

$$Z_N(s) = \frac{v(s)}{i(s)} \Big|_{y(s) \xrightarrow{\text{null}} 0} \quad (\text{C.17})$$

The value of $i(s)$ that achieves the null condition $y(s) \xrightarrow{\text{null}} 0$ can be found by setting $y(s) = 0$ in Eq. (C.10), as follows:

$$\left[G_{old}(s)u(s) + G_i(s)i(s) \right] \xrightarrow{\text{null}} 0 \quad (\text{C.18})$$

Hence, the output $y(s)$ is nulled when the inputs $u(s)$ and $i(s)$ are related as follows:

$$u(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} = -\frac{G_i(s)}{G_{old}(s)} i(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} \quad (\text{C.19})$$

Under this null condition, the voltage $v(s)$ is given by

$$\begin{aligned} v(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} &= G_v(s)u(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} + Z_D(s)i(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} \\ &= \left(-\frac{G_v(s)G_i(s)}{G_{old}(s)} + Z_D(s) \right) i(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} \end{aligned} \quad (\text{C.20})$$

which follows from Eqs. (C.11) and (C.19). Substitution of Eq. (C.17) into Eq. (C.20) yields

$$v(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} = Z_N(s)i(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} = \left(-\frac{G_v(s)G_i(s)}{G_{old}(s)} + Z_D(s) \right) i(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} \quad (\text{C.21})$$

Hence,

$$Z_N(s) = Z_D(s) - \frac{G_v(s)G_i(s)}{G_{old}(s)} \quad (\text{C.22})$$

Solution for the quantity $G_v(s)G_i(s)$ yields

$$G_v(s)G_i(s) = (Z_D(s) - Z_N(s))G_{old}(s) \quad (\text{C.23})$$

Thus, the unknown quantities $G_v(s)$ and $G_i(s)$ can be related to $Z_N(s)$ and $Z_D(s)$, which are properties of the port at which the new impedance $Z(s)$ will be connected, and to the original transfer function $G_{old}(s)$.

The final step is to substitute Eq. (C.23) into Eq. (C.16), leading to

$$G(s) = G_{old}(s) - \frac{Z_D(s) - Z_N(s)}{Z(s) + Z_D(s)} G_{old}(s) \quad (C.24)$$

This expression can be simplified as follows:

$$G(s) = G_{old}(s) \frac{1 + \frac{Z_N(s)}{Z(s)}}{1 + \frac{Z_D(s)}{Z(s)}} \quad (C.25)$$

or,

$$G(s) = \left(G(s) \Big|_{Z(s) \rightarrow \infty} \right) \left(\frac{1 + \frac{Z_N(s)}{Z(s)}}{1 + \frac{Z_D(s)}{Z(s)}} \right) \quad (C.26)$$

This is the desired result. It states how the transfer function $G(s)$ is modified by addition of the extra element $Z(s)$. The right-most term in Eq. (C.26) is called the *correction factor*; this term gives a quantitative measure of the change in $G(s)$ arising from the introduction of $Z(s)$.

Derivation of the dual result, Eq. (C.3), follows similar steps.

C.3 DISCUSSION

The general form of the extra element theorem makes it useful for designing a system such that unwanted circuit elements do not degrade the desirable system performance already obtained. For example, suppose that we already know some transfer function or similar quantity $G(s)$, under simplified or ideal conditions, and have designed the system such that this quantity meets specifications. We can then use the extra element theorem to answer the following questions:

What is the effect of a parasitic element $Z(s)$ that was not included in the original analysis?

What happens if we later decide to add some additional components having impedance $Z(s)$ to the system?

Can we establish some conditions on $Z(s)$ that ensure that $G(s)$ is not substantially changed?

A common application of the extra element theorem is the determination of conditions on the extra element that guarantee that the transfer function $G(s)$ is not significantly altered. According to Eqs. (C.2) and (C.26), this will occur when the correction factor is approximately equal to unity. The conditions are:

$$\begin{aligned} \|Z(j\omega)\| &\gg \|Z_N(j\omega)\| \\ \|Z(j\omega)\| &\gg \|Z_D(j\omega)\| \end{aligned} \quad (C.27)$$

This gives a formal way to show when an impedance can be ignored: one can plot the impedances $\|Z_N(j\omega)\|$ and $\|Z_D(j\omega)\|$, and compare the results with a plot of $\|Z(j\omega)\|$. The impedance $Z(s)$ can be ignored over the range of frequencies where the inequalities (C.27) are satisfied.

For the dual case in which the new impedance is inserted where there was previously a short circuit, Eq. (C.3), the inequalities are reversed:

$$\begin{aligned} \|Z(j\omega)\| &\ll \|Z_N(j\omega)\| \\ \|Z(j\omega)\| &\ll \|Z_D(j\omega)\| \end{aligned} \quad (\text{C.28})$$

This equation shows how to limit the magnitude $\|Z(j\omega)\|$, to avoid significantly changing the transfer function $G(s)$.

For quantitative design, Eqs. (C.27) and (C.28) raise an additional question: By what factor should $\|Z(j\omega)\|$ exceed (or be less than) $\|Z_N(j\omega)\|$ and $\|Z_D(j\omega)\|$, in order for the inequalities of Eq. (C.27) or (C.28) to be well satisfied? This question can be answered by plotting the magnitudes and phases of the correction factor terms, as a function of the magnitudes and phases of (Z/Z_N) and (Z/Z_D) .

Figure C.6 shows contours of constant $\|1 + Z/Z_N\|$, as a function of the magnitude and phase of Z/Z_N . Figure C.7 shows similar contours of constant $\angle(1 + Z/Z_N)$. It can be seen that, when $\|Z/Z_N\|$ is less than -20 dB, then the maximum deviation caused by the numerator $(1 + Z/Z_N)$ term is less than ± 1 dB in magnitude, and less than $\pm 7^\circ$ in phase. For $\|Z/Z_N\|$ less than -10 dB, the maximum deviation caused by the numerator $(1 + Z/Z_N)$ term is less than ± 3.5 dB in magnitude, and less than $\pm 20^\circ$ in phase.

Figures C.8 and C.9 contain contours of constant $\|1/(1 + Z/Z_D)\|$ and $\angle 1/(1 + Z/Z_D)$, respectively, as a function of the magnitude and phase of Z/Z_D . These plots contain minus signs because the terms appear in the denominator of the correction factor; otherwise, they are identical to Figs. C.6 and C.7. Again, for $\|Z/Z_D\|$ less than -20 dB, the maximum deviation caused by the denominator $(1 + Z/Z_D)$ term is less than ± 1 dB in magnitude, and less than $\pm 7^\circ$ in phase. For $\|Z/Z_D\|$ less than -10 dB, the maximum deviation caused by the denominator $(1 + Z/Z_D)$ term is less than ± 3.5 dB in magnitude, and less than $\pm 20^\circ$ in phase.

C.4 EXAMPLES

C.4.1 A Simple Transfer Function

The first example illustrates how the Extra Element Theorem can be used to find a transfer function essentially by inspection. We are given the circuit illustrated in Fig. C.10. It is desired to solve for the transfer function

$$G(s) = \frac{v_2(s)}{v_1(s)} \quad (\text{C.29})$$

and to express this transfer function in factored pole-zero form. One way to do this is to employ the Extra Element Theorem, treating the capacitor C as an “extra” element. As illustrated in Fig. C.11, the electrical port is taken to be at the location of the capacitor, and the “original conditions” are taken to be the case when the capacitor impedance is infinite, i.e., an open circuit. Under these original conditions, the transfer function is given by the voltage divider composed of resistors R_1 , R_3 , and R_4 . Hence, $G(s)$ can be expressed as

$$\frac{v_2(s)}{v_1(s)} = G(s) = \left(\frac{R_4}{R_1 + R_3 + R_4} \right) \left(\frac{1 + \frac{Z_N}{Z}}{1 + \frac{Z_D}{Z}} \right) \quad (\text{C.30})$$

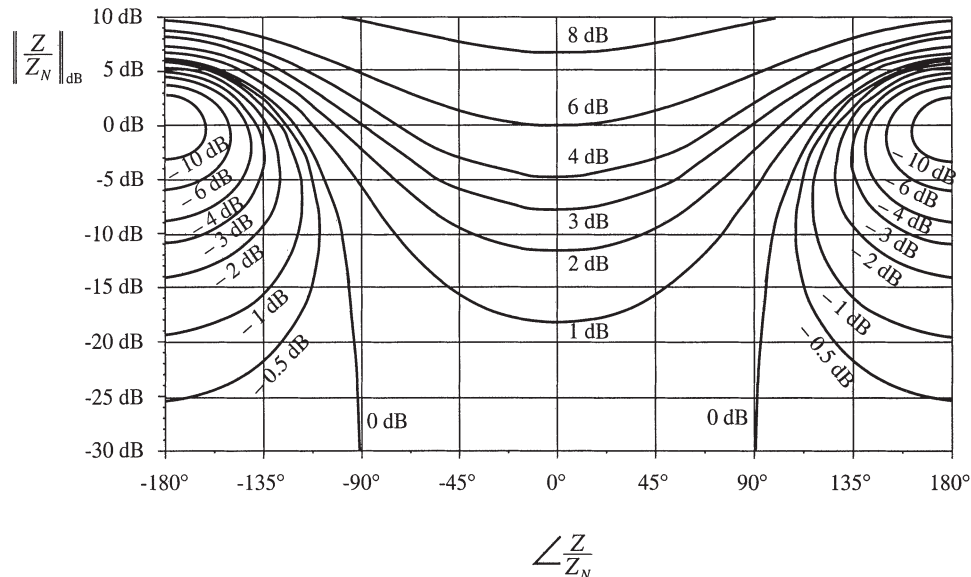


Fig. C.6 Contours of constant $\left\| 1 + \frac{Z}{Z_N} \right\|$, as a function of the magnitude and phase of $\frac{Z}{Z_N}$.

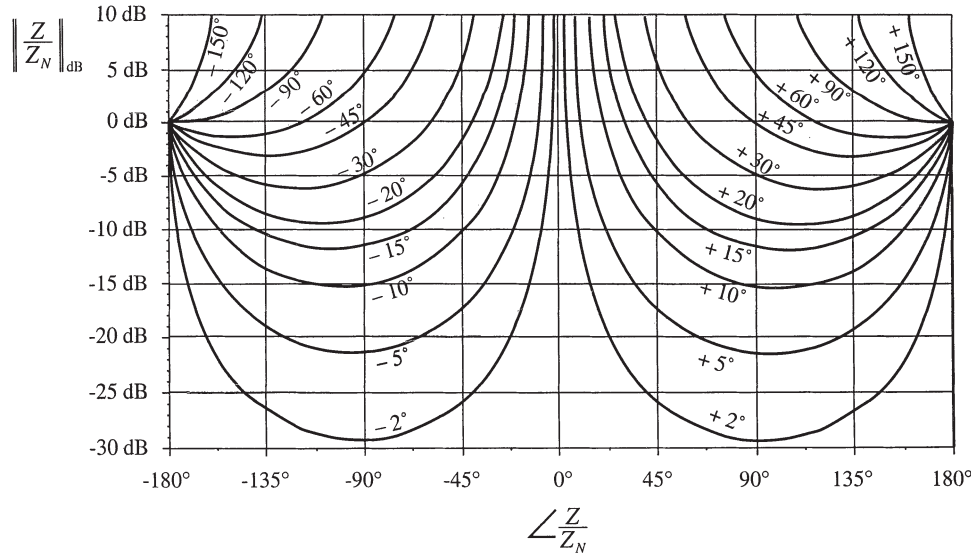


Fig. C.7 Contours of constant $\angle (1 + \frac{Z}{Z_N})$, as a function of the magnitude and phase of $\frac{Z}{Z_N}$.

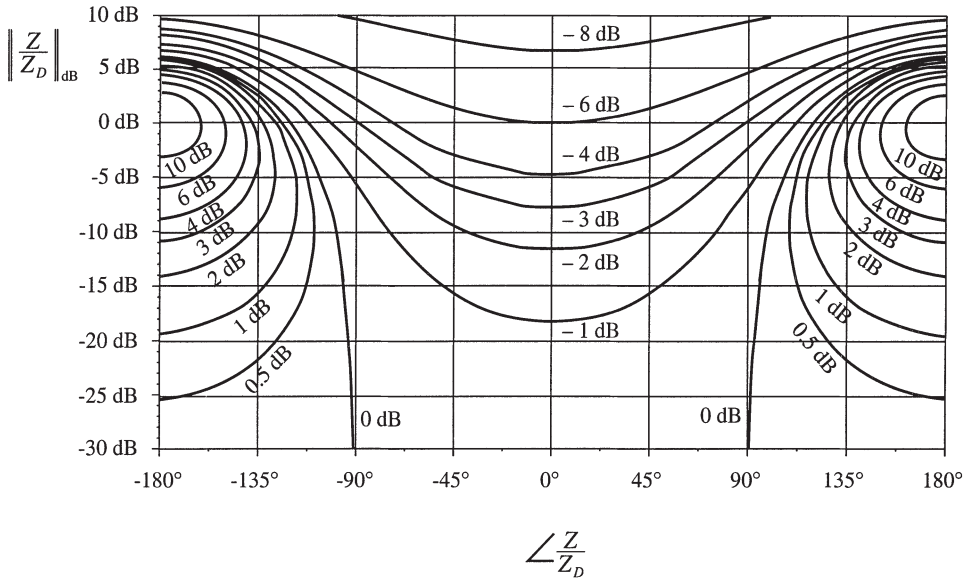


Fig. C.8 Contours of constant $\|1/(1 + Z/Z_D)\|$, as a function of the magnitude and phase of Z/Z_D

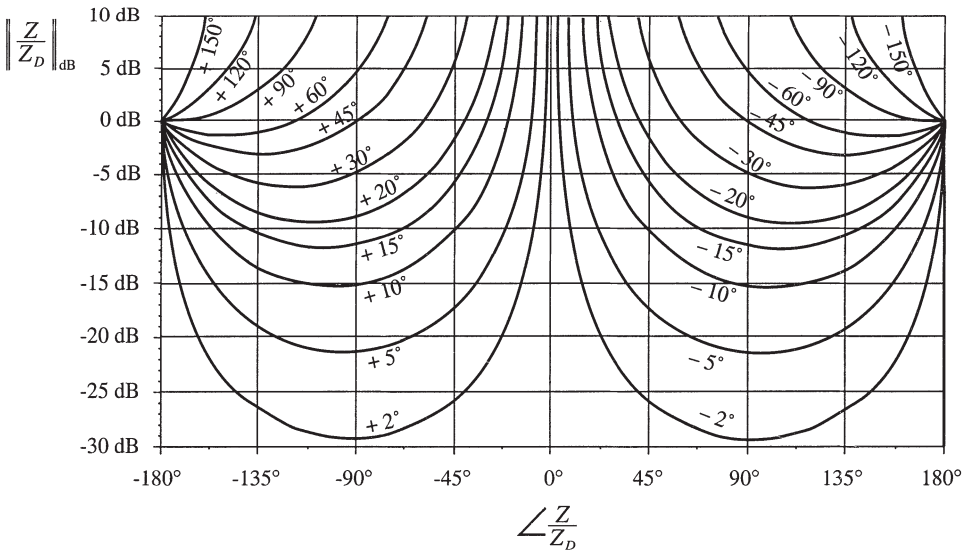


Fig. C.9 Contours of constant $\angle 1/(1 + Z/Z_D)$, as a function of the magnitude and phase of Z/Z_D

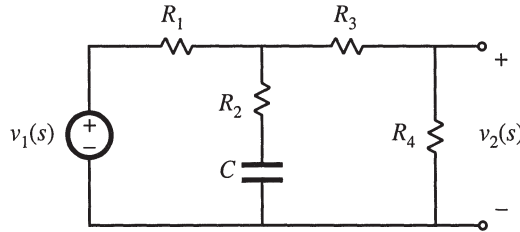


Fig. C.10 R-C circuit example of Section C.4.1.

where $Z(s)$ is the capacitor impedance $1/sC$.

The impedance $Z_D(s)$ is the Thevenin equivalent impedance seen at the port where the capacitor is connected. As illustrated in Fig. C.12(a), this impedance is found by setting the independent source $v_1(s)$ to zero, and then determining the impedance between the port terminals. The result is:

$$Z_D = R_2 + R_1 \parallel (R_3 + R_4) \quad (\text{C.31})$$

Figure C.12(b) illustrates determination of the impedance $Z_N(s)$. A current source $i(s)$ is connected to the port, in place of the capacitor. In the presence of the input $v_1(s)$, the current source $i(s)$ is adjusted so that the output $v_2(s)$ is nulled. Under these null conditions, the impedance $Z_N(s)$ is found as the ratio of $v(s)$ to $i(s)$.

It is easiest to find $Z_N(s)$ by first determining the effect of the null condition on the signals in the circuit. Since v_2 is nulled to zero, there is no current through the resistor R_4 . Since R_3 is connected in series with R_4 , there is also no current through R_3 , and hence no voltage across R_3 . Therefore, the voltage v_3 in Fig. C.12(b) is equal to v_2 , i.e.,

$$v_3 = v_2 \xrightarrow{\text{null}} 0 \quad (\text{C.32})$$

Therefore, the voltage v is given by iR_2 . The impedance Z_N is

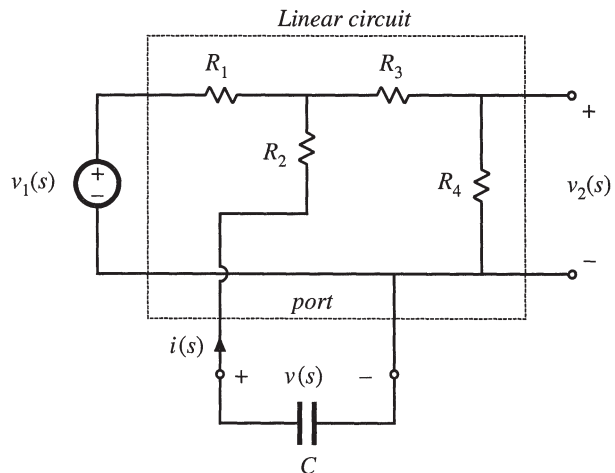


Fig. C.11 Manipulation of the circuit of Fig. C.10 into the form of Fig. C.1.

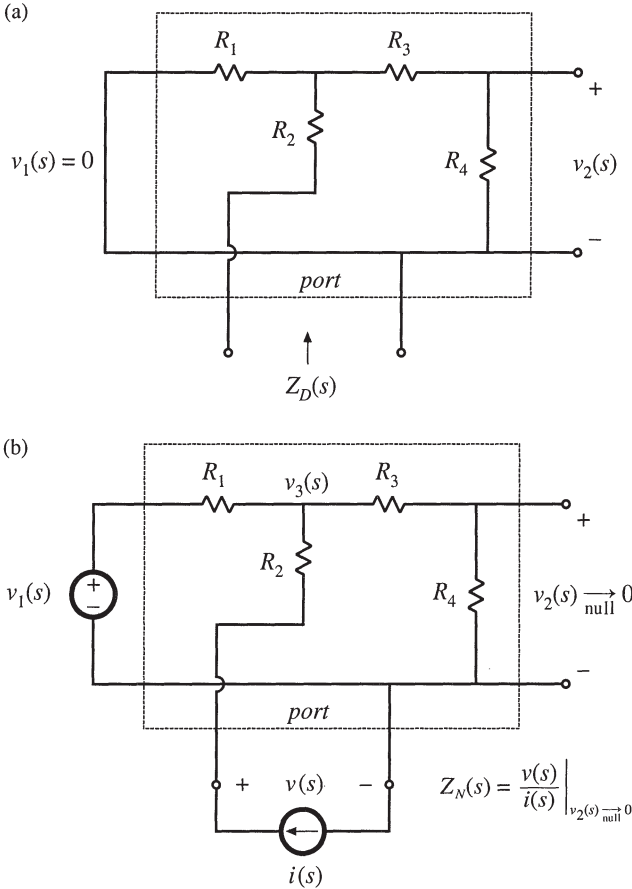


Fig. C.12 Measurement of the quantities $Z_N(s)$ and $Z_D(s)$: (a) determination of $Z_D(s)$, (b) determination of $Z_N(s)$.

$$Z_N(s) = \left. \frac{v(s)}{i(s)} \right|_{v_2(s) \xrightarrow{\text{null}} 0} = R_2 \quad (\text{C.33})$$

Note that, in general, the independent sources v_1 and i are nonzero during the Z_N measurement. For this example, the null condition implies that the current $i(s)$ flows entirely through the path composed of R_2 , R_1 , and v_1 .

The transfer function $G(s)$ is found by substitution of Eqs. (C.31) and (C.33) into Eq. (C.30):

$$G(s) = \left(\frac{R_4}{R_1 + R_3 + R_4} \right) \frac{(1 + sCR_2)}{\left(1 + sC \left[R_2 + R_1 \parallel (R_3 + R_4) \right] \right)} \quad (\text{C.34})$$

For this example, the result is obtained in standard normalized pole-zero form, because the capacitor is the only dynamic element in the circuit, and because the “original conditions,” in which the capacitor impedance tends to an open circuit, coincide with dc conditions in the circuit. A similar procedure can be

applied to write the transfer function of a circuit, containing an arbitrary number of reactive elements, in normalized form via an extension of the Extra Element Theorem [3].

C.4.2 An Unmodeled Element

We are told that the transformer-isolated parallel resonant inverter of Fig. C.13 has been designed with the assumption that the transformer is ideal. The approximate sinusoidal analysis techniques of Chapter 19 were employed to model the inverter. It is now desired to specify a transformer; this requires that limits be specified on the minimum allowable transformer magnetizing inductance. One way to approach this problem is to view the transformer magnetizing inductance as an extra element, and to derive conditions that guarantee that the presence of the transformer magnetizing inductance does not significantly change the tank network transfer function $G(s)$.

Figure C.14 illustrates the equivalent circuit model of the inverter, derived using the approximate sinusoidal analysis technique of Section 19.1. The switch network output voltage $v_s(t)$ is modeled by its fundamental component $v_{s1}(t)$, a sinusoid. The tank transfer function $G(s)$ is given by:

$$G(s) = \frac{v_o(s)}{v_{s1}(s)} \quad (\text{C.35})$$

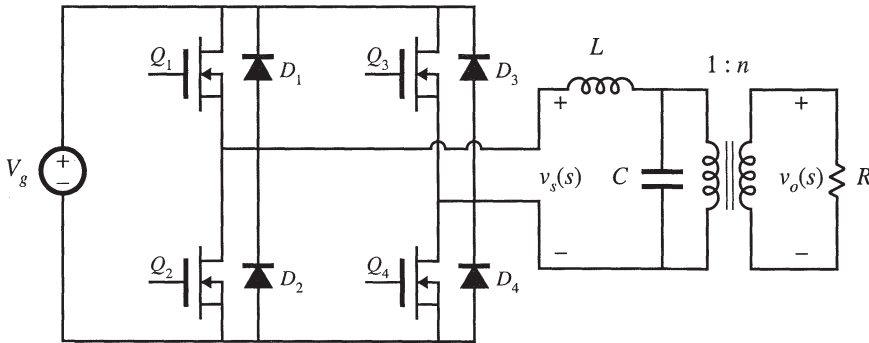


Fig. C.13 Parallel resonant inverter example.

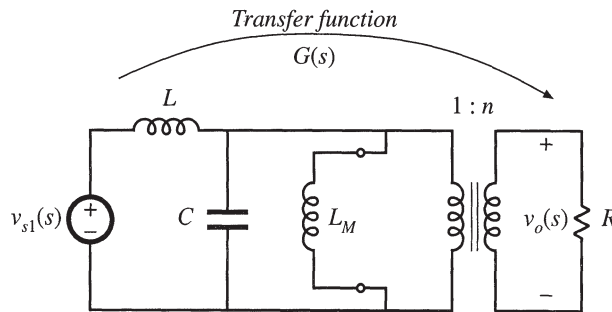


Fig. C.14 Equivalent circuit model of the tank network, based on the approximate sinusoidal analysis technique.

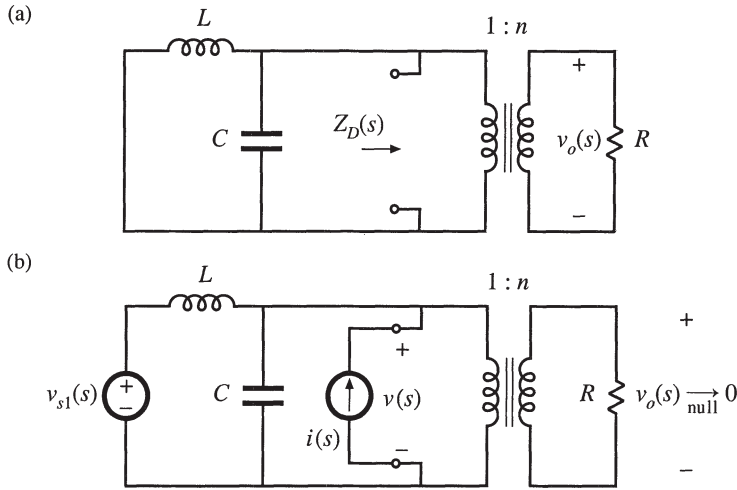


Fig. C.15 Measurement of $Z_N(s)$ and $Z_D(s)$: (a) determination of $Z_D(s)$, (b) determination of $Z_N(s)$.

Under the conditions that the transformer is ideal (i.e., the transformer magnetizing inductance L_M is open circuited), then the transfer function is given by:

$$G(s) \Big|_{L_M \rightarrow \infty} = \frac{n}{1 + s \frac{n^2 L}{R} + s^2 LC} \quad (\text{C.36})$$

We can therefore employ the extra element theorem to determine how finite magnetizing inductance changes $G(s)$. With reference to Fig. C.1, the system input is $v_{s1}(s)$, the output is the voltage $v_o(s)$, and the “port” is the primary winding of the transformer, where the magnetizing inductance is connected. In the presence of the magnetizing inductance, the transfer function becomes

$$G(s) = \left(G(s) \Big|_{L_M \rightarrow \infty} \right) \frac{\left(1 + \frac{Z_N(s)}{Z(s)} \right)}{\left(1 + \frac{Z_D(s)}{Z(s)} \right)} \quad (\text{C.37})$$

where $Z(s)$ is the impedance of the magnetizing inductance referred to the primary winding, sL_M .

Figure C.15(a) illustrates determination of $Z_D(s)$. The input source $v_{s1}(s)$ is set to zero, and the impedance between the terminals of the port is found. It can be seen that the impedance $Z_D(s)$ is the parallel combination of the impedances of the tank inductor, tank capacitor, and the reflected load resistance:

$$Z_D(s) = \frac{R}{n^2} \parallel sL \parallel \frac{1}{sC} \quad (\text{C.38})$$

Figure C.15(b) illustrates determination of $Z_N(s)$. In the presence of the input source $v_{s1}(s)$, a current $i(s)$ is injected at the port as shown. This current is adjusted such that the output $v_o(s)$ is nulled. Under these conditions, the quantity $Z_N(s)$ is given by $v(s)/i(s)$. It can be seen that nulling $v_o(s)$ also nulls the voltage $v(s)$. Therefore,

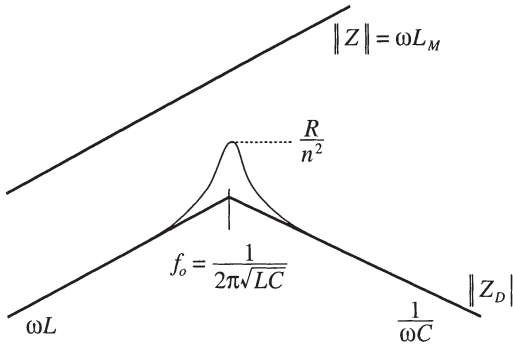


Fig. C.16 To avoid significantly changing the transfer function $G(s)$, the transformer should be designed such that $\|Z\| \gg \|Z_D\|$.

$$Z_N(s) = \left. \frac{v(s)}{i(s)} \right|_{v_o(s) \text{ null } 0} = 0 \quad (\text{C.39})$$

Note that, in general, $i(s)$ will not be equal to zero during the $Z_N(s)$ measurement. The null condition is achieved by setting the source $i(s)$ equal to the value $-v_{s1}(s)/sL$. Thus, in the presence of finite magnetizing inductance, the transfer function $G(s)$ can be expressed as follows:

$$G(s) = \left(G(s) \Big|_{L_M \rightarrow \infty} \right) \frac{\left(1 + \frac{0}{Z(s)} \right)}{\left(1 + \frac{Z_D(s)}{Z(s)} \right)} = \frac{\left(G(s) \Big|_{L_M \rightarrow \infty} \right)}{\left(1 + \frac{Z_D(s)}{Z(s)} \right)} \quad (\text{C.40})$$

We can now plot the impedance inequalities (C.27) that guarantee that the magnetizing inductance does not substantially modify $G(s)$. The $Z_D(s)$ given in Eq. (C.38) is the impedance of a parallel resonant circuit. Construction of the magnitude of this impedance is described in Section 8.3.4, with results illustrated in Fig. C.16. To avoid affecting the transfer function $G(s)$, the impedance of the magnetizing inductance must be much greater than $\|Z_D(j\omega)\|$ over the range of expected operating frequencies. It can be seen that this will indeed be the case provided that the impedance of the magnetizing inductance is greater than the impedances of both the tank inductance and the reflected load impedance:

$$\begin{aligned} L_M &\gg L, \text{ and} \\ \omega_0 L_M &\gg \frac{R}{n^2} \end{aligned} \quad (\text{C.41})$$

where $\omega_0 = 1/(\sqrt{LC})$. These conditions can be further reduced to

$$\begin{aligned} L_M &\gg L, \text{ and} \\ L_M &\gg \frac{R}{n^2} \sqrt{LC} \end{aligned} \quad (\text{C.42})$$

C.4.3 Addition of an Input Filter to a Converter

As discussed in Chapter 10, the addition of an input filter to a switching regulator can significantly alter its loop gain $T(s)$. Hence, it is desirable to design the input filter so that it does not substantially change

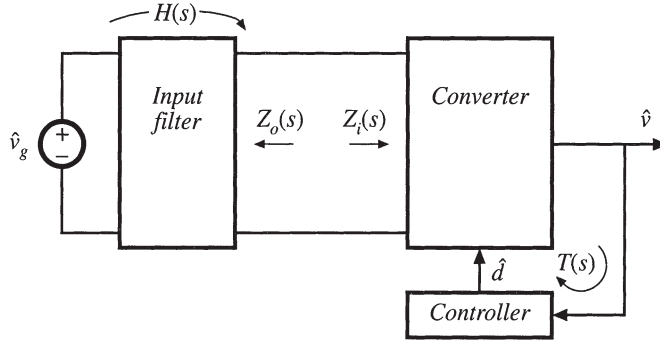


Fig. C.17 Addition of an input filter to a switching voltage regulator system.

the converter control-to-output transfer function $G_{vd}(s)$. The Extra Element Theorem can provide design criteria that show how to design such an input filter.

Figure C.17 illustrates the addition of an input filter to a switching voltage regulator system. The control-to-output transfer function of the converter power stage is given by:

$$G_{vd}(s) = \left. \frac{\hat{v}(s)}{\hat{d}(s)} \right|_{\hat{v}_g(s)=0} \quad (\text{C.43})$$

The quantity $Z_o(s)$ is the Thevenin equivalent output impedance of the input filter. Upon setting $\hat{v}_g(s)$ to zero in Fig. C.17, the system of Fig. C.18 is obtained. It can be recognized that this system is of the same form as Fig. C.2, in which the “extra element” is the output impedance $Z_o(s)$ of the added input filter. With no input filter [$Z_o(s) = 0$], the “original” transfer function $G_{vd}(s)|_{Z_o(s)=0}$ is obtained. In the presence of the input filter, $G_{vd}(s)$ is expressed according to Eq. (C.3):

$$G_{vd}(s) = \left(G_{vd}(s) \Big|_{Z_o(s) \rightarrow 0} \right) \left(\frac{1 + \frac{Z(s)}{Z_N(s)}}{1 + \frac{Z(s)}{Z_D(s)}} \right) \quad (\text{C.44})$$

where

$$Z_D(s) = Z_i(s) \Big|_{\hat{d}(s)=0} \quad (\text{C.45})$$

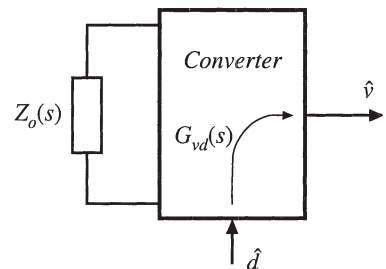


Fig. C.18 Determination of the control-to-output transfer function $G_{vd}(s)$ for the system of Fig. C.17.

is the impedance seen looking into the power input port of the converter when $\hat{d}$ is set to zero, and

$$Z_N(s) = Z_i(s) \Big|_{\hat{v}(s) \xrightarrow{\text{null}} 0} \quad (\text{C.46})$$

is the impedance seen looking into the power input port of the converter when the converter output $\hat{v}$ is nulled. The null condition is achieved by injecting a test current source $\hat{i}_{test}$ at the converter input port, in the presence of $\hat{d}$ variations, and adjusting $\hat{i}_{test}$ such that $\hat{v}$ is nulled. Derivation of expressions for $Z_N(s)$ and $Z_D(s)$ for a buck converter example is described in Section 10.3.1.

According to Eq. (C.28), the input filter does not significantly affect $G_{vd}(s)$ provided that

$$\begin{aligned} \|Z_o(j\omega)\| &\ll \|Z_N(j\omega)\| \\ \|Z_o(j\omega)\| &\ll \|Z_D(j\omega)\| \end{aligned} \quad (\text{C.47})$$

These inequalities can provide an effective set of criteria for designing the input filter. Bode plots of $\|Z_N(j\omega)\|$ and $\|Z_D(j\omega)\|$ are constructed, and then the filter element values are chosen to satisfy (C.47). Several examples of this procedure are explained in Chapter 10.

C.4.4 Dependence of Transistor Current on Load in a Resonant Inverter

The conduction loss caused by circulating tank currents is a major problem in resonant converter design. These currents are independent of, or only weakly dependent on, the load current, and lead to poor efficiency at light load. The origin of this problem is the weak dependence of the tank network input impedance on the load resistance. For example, Fig. C.19 illustrates the model of the ac portion of a resonant inverter, derived using the sinusoidal approximation of Section 19.1. The resonant network contains the tank inductors and capacitors of the converter, and the load is the resistance R . The current $i_s(t)$ flowing in the effective sinusoidal source is equal to the switch current. This model predicts that the switch current $i_s(s)$ is equal to $v_{s1}(s)/Z_i(s)$, where $Z_i(s)$ is the input impedance of the resonant tank network. If we want the switch current to track the load current, then at the switching frequency $\|Z_i\|$ should be dominated by, or at least strongly influenced by, the load resistance R . Unfortunately, this is often not consistent with other requirements, in which Z_i is dominated by the impedances of the tank elements. To design a resonant converter that exhibits good properties, the engineer must develop physical insight into how the load resistance R affects the tank input impedance and output voltage.

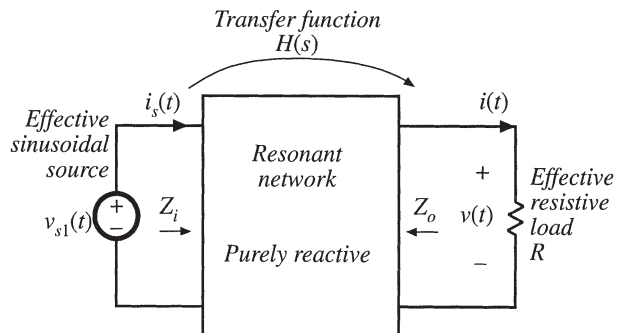


Fig. C.19 Resonant inverter model.

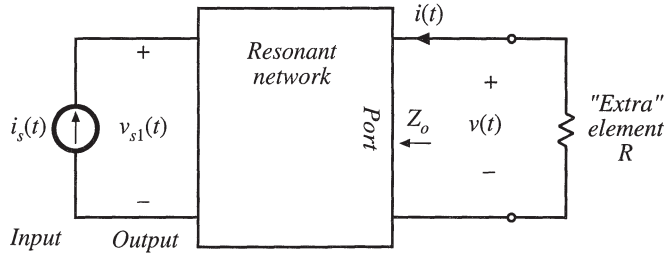


Fig. C.20 Application of the Extra Element Theorem to the system of Fig. C.19, to expose the dependence of $Z_i(s)$ on R .

To expose the dependence of $Z_i(s)$ on the load resistance R , we can treat R as the “extra” element as in Fig. C.20. The input impedance $Z_i(s)$ is viewed as the transfer function from the current i_s to the voltage v_{s1} ; in this sense, i_s is the “input” and v_{s1} is the “output.” Equations (C.2) and (C.3) then imply that $Z_i(s)$ can be expressed as follows:

$$Z_i(s) = \frac{v_{s1}(s)}{i_s(s)} = Z_{i0}(s) \frac{\left(1 + \frac{R}{Z_N(s)}\right)}{\left(1 + \frac{R}{Z_D(s)}\right)} = Z_{i\infty}(s) \frac{\left(1 + \frac{Z_N(s)}{R}\right)}{\left(1 + \frac{Z_D(s)}{R}\right)} \quad (\text{C.48})$$

Here, the impedance $Z_{i0}(s)$ is

$$Z_{i0}(s) = Z_i(s) \Big|_{R \rightarrow 0} \quad (\text{C.49})$$

i.e., the input impedance $Z_i(s)$ when the load terminals are shorted. Likewise, the impedance $Z_{i\infty}(s)$ is

$$Z_{i\infty}(s) = Z_i(s) \Big|_{R \rightarrow \infty} \quad (\text{C.50})$$

which is the input impedance $Z_i(s)$ when the load is disconnected (open circuited).

Determination of $Z_N(s)$ and $Z_D(s)$ is illustrated in Fig. C.21. The quantity $Z_N(s)$ is found by nulling the “output” v_{s1} to zero, and then solving for $v(s)/i(s)$. The quantity $Z_N(s)$ coincides with the conventional output impedance $Z_o(s)$ illustrated in Fig. C.19. In Fig. C.21(a), the act of nulling v_{s1} is equivalent to shorting the source v_{s1} of Fig. C.19. In Section 19.4, the quantity $Z_N(s)$ is denoted $Z_{o0}(s)$, because it coincides with the converter output impedance with the switch network shorted.

The quantity $Z_D(s)$ is found by setting the “input” i_s to zero, and then solving for $v(s)/i(s)$. The quantity $Z_D(s)$ coincides with the output impedance $Z_o(s)$ illustrated in Fig. C.19, under the conditions that the source v_{s1} is open-circuited. In Section 19.4, the quantity $Z_D(s)$ is denoted $Z_{o\infty}(s)$, because it coincides with the converter output impedance with the switch network open-circuited.

The reciprocity relationship, Eq. (C.4), becomes

$$\frac{Z_{i\infty}(s)}{Z_{i0}(s)} = \frac{Z_{o\infty}(s)}{Z_{o0}(s)} \quad (\text{C.51})$$

The above results are used in Section 19.4 to expose how conduction losses and the zero-voltage switching boundary depend on the loading of a resonant converter.

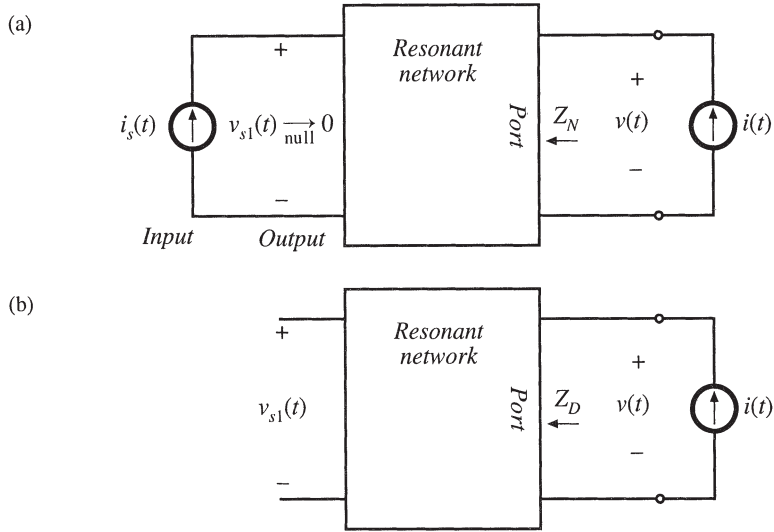


Fig. C.21 Determination of the quantities $Z_N(s)$ and $Z_D(s)$ for the network of Fig. C.20: (a) finding $Z_N(s)$, (b) finding $Z_D(s)$.

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Appendix D

Magnetics Design Tables

Geometrical data for several standard ferrite core shapes are listed here. The geometrical constant K_g is a measure of core size, useful for designing inductors and transformers that attain a given copper loss [1]. The K_g method for inductor design is described in Chapter 14. K_g is defined as

$$K_g = \frac{A_c^2 W_A}{MLT} \quad (\text{D.1})$$

where A_c is the core cross-sectional area, W_A is the window area, and MLT is the winding mean-length-per-turn. The geometrical constant K_{gfe} is a similar measure of core size, which is useful for designing ac inductors and transformers when the total copper plus core loss is constrained. The K_{gfe} method for magnetics design is described in Chapter 15. K_{gfe} is defined as

$$K_{gfe} = \frac{W_A A_c^{2(1-1/\beta)}}{MLT \ell_m^{2/\beta}} u(\beta) \quad (\text{D.2})$$

where ℓ_m is the core mean magnetic path length, and β is the core loss exponent:

$$P_{fe} = K_{fe} B_{max}^\beta \quad (\text{D.3})$$

For modern ferrite materials, β typically lies in the range 2.6 to 2.8. The quantity $u(\beta)$ is defined as

$$u(\beta) = \left[\left(\frac{\beta}{2} \right)^{-\left(\frac{\beta}{\beta+2} \right)} + \left(\frac{\beta}{2} \right)^{\left(\frac{2}{\beta+2} \right)} \right]^{-\left(\frac{\beta+2}{\beta} \right)} \quad (\text{D.4})$$

$u(\beta)$ is equal to 0.305 for $\beta = 2.7$. This quantity varies by roughly 5% over the range $2.6 \leq \beta \leq 2.8$. Values of K_{gfe} are tabulated for $\beta = 2.7$; variation of K_{gfe} over the range $2.6 \leq \beta \leq 2.8$ is typically quite small.

Thermal resistances are listed in those cases where published manufacturer's data are available. The thermal resistances listed are the approximate temperature rise from the center leg of the core to ambient, per watt of total power loss. Different temperature rises may be observed under conditions of forced air cooling, unusual power loss distributions, etc. Listed window areas are the winding areas for conventional single-section bobbins.

An American Wire Gauge table is included at the end of this appendix.

D.1 POT CORE DATA

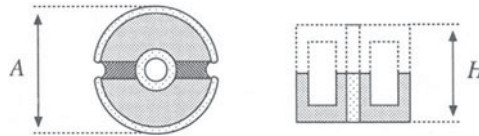


Fig. D.1

Core type	Geometrical constant	Geometrical constant	Cross-sectional area	Bobbin winding area	Mean length per turn	Magnetic path length	Thermal resistance	Core weight
(AH)	K_g	K_{gfe}	A_c	W_A	MLT	ℓ_m	R_{th}	
(mm)	cm ⁵	cm ^x	(cm ²)	(cm ²)	(cm)	(cm)	(°C/W)	(g)
704	$0.738 \cdot 10^{-6}$	$1.61 \cdot 10^{-6}$	0.070	$0.22 \cdot 10^{-3}$	1.46	1.0		0.5
905	$0.183 \cdot 10^{-3}$	$256 \cdot 10^{-6}$	0.101	0.034	1.90	1.26		1.0
1107	$0.667 \cdot 10^{-3}$	$554 \cdot 10^{-6}$	0.167	0.055	2.30	1.55		1.8
1408	$2.107 \cdot 10^{-3}$	$1.1 \cdot 10^{-3}$	0.251	0.097	2.90	2.00	100	3.2
1811	$9.45 \cdot 10^{-3}$	$2.6 \cdot 10^{-3}$	0.433	0.187	3.71	2.60	60	7.3
2213	$27.1 \cdot 10^{-3}$	$4.9 \cdot 10^{-3}$	0.635	0.297	4.42	3.15	38	13
2616	$69.1 \cdot 10^{-3}$	$8.2 \cdot 10^{-3}$	0.948	0.406	5.28	3.75	30	20
3019	0.180	$14.2 \cdot 10^{-3}$	1.38	0.587	6.20	4.50	23	34
3622	0.411	$21.7 \cdot 10^{-3}$	2.02	0.748	7.42	5.30	19	57
4229	1.15	$41.1 \cdot 10^{-3}$	2.66	1.40	8.60	6.81	13.5	104

D.2 EE CORE DATA

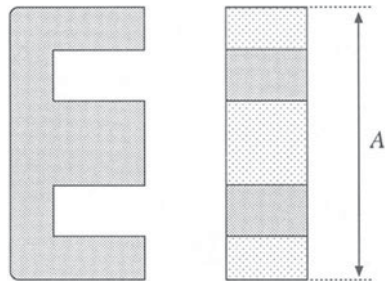


Fig. D.2

Core type	Geometrical constant	Geometrical constant	Cross-sectional area	Bobbin winding area	Mean length per turn	Magnetic path length	Core weight
(A)	K_g	K_{gfe}	A_c	W_A	MLT	ℓ_m	(g)
(mm)	(cm ⁵)	(cm ⁴)	(cm ²)	(cm ²)	(cm)	(cm)	
EE12	$0.731 \cdot 10^{-3}$	$0.458 \cdot 10^{-3}$	0.14	0.085	2.28	2.7	2.34
EE16	$2.02 \cdot 10^{-3}$	$0.842 \cdot 10^{-3}$	0.19	0.190	3.40	3.45	3.29
EE19	$4.07 \cdot 10^{-3}$	$1.3 \cdot 10^{-3}$	0.23	0.284	3.69	3.94	4.83
EE22	$8.26 \cdot 10^{-3}$	$1.8 \cdot 10^{-3}$	0.41	0.196	3.99	3.96	8.81
EE30	$85.7 \cdot 10^{-3}$	$6.7 \cdot 10^{-3}$	1.09	0.476	6.60	5.77	32.4
EE40	0.209	$11.8 \cdot 10^{-3}$	1.27	1.10	8.50	7.70	50.3
EE50	0.909	$28.4 \cdot 10^{-3}$	2.26	1.78	10.0	9.58	116
EE60	1.38	$36.4 \cdot 10^{-3}$	2.47	2.89	12.8	11.0	135
EE70/68/19	5.06	$75.9 \cdot 10^{-3}$	3.24	6.75	14.0	18.0	280

D.3 EC CORE DATA

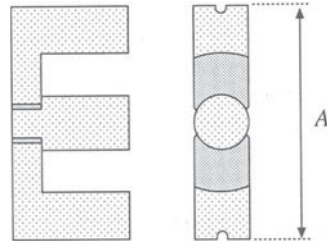


Fig. D.3

Core type	Geometrical constant	Geometrical constant	Cross-sectional area	Bobbin winding area	Mean length per turn	Magnetic path length	Thermal resistance	Core weight
(A)	K_g	K_{gfe}	A_c	W_A	MLT	ℓ_m	R_{th}	
(mm)	(cm ⁵)	(cm ⁶)	(cm ²)	(cm ²)	(cm)	(cm)	(°C/W)	(g)
EC35	0.131	$9.9 \cdot 10^{-3}$	0.843	0.975	5.30	7.74	18.5	35.5
EC41	0.374	$19.5 \cdot 10^{-3}$	1.21	1.35	5.30	8.93	16.5	57.0
EC52	0.914	$31.7 \cdot 10^{-3}$	1.80	2.12	7.50	10.5	11.0	111
EC70	2.84	$56.2 \cdot 10^{-3}$	2.79	4.71	12.9	14.4	7.5	256

D.4 ETD CORE DATA

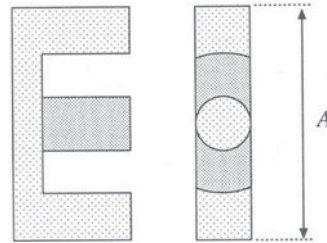


Fig. D.4

Core type	Geometrical constant	Geometrical constant	Cross-sectional area	Bobbin winding area	Mean length per turn	Magnetic path length	Thermal resistance	Core weight
(A)	K_g	K_{gfe}	A_c	W_A	MLT	ℓ_m	R_{th}	
(mm)	(cm ⁵)	(cm ⁶)	(cm ²)	(cm ²)	(cm)	(cm)	(°C/W)	(g)
ETD29	0.0978	$8.5 \cdot 10^{-3}$	0.76	0.903	5.33	7.20		30
ETD34	0.193	$13.1 \cdot 10^{-3}$	0.97	1.23	6.00	7.86	19	40
ETD39	0.397	$19.8 \cdot 10^{-3}$	1.25	1.74	6.86	9.21	15	60
ETD44	0.846	$30.4 \cdot 10^{-3}$	1.74	2.13	7.62	10.3	12	94
ETD49	1.42	$41.0 \cdot 10^{-3}$	2.11	2.71	8.51	11.4	11	124

D.5 PQ CORE DATA

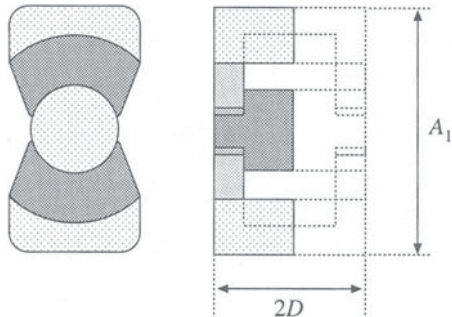


Fig. D.5

Core type	Geometrical constant	Geometrical constant	Cross-sectional area	Bobbin winding area	Mean length per turn	Magnetic path length	Core weight
$(A_1/2D)$	K_g	K_{gfe}	A_c	W_A	MLT	ℓ_m	
(mm)	(cm ⁵)	(cm ^x)	(cm ²)	(cm ²)	(cm)	(cm)	(g)
PQ 20/16	$22.4 \cdot 10^{-3}$	$3.7 \cdot 10^{-3}$	0.62	0.256	4.4	3.74	13
PQ 20/20	$33.6 \cdot 10^{-3}$	$4.8 \cdot 10^{-3}$	0.62	0.384	4.4	4.54	15
PQ 26/20	$83.9 \cdot 10^{-3}$	$7.2 \cdot 10^{-3}$	1.19	0.333	5.62	4.63	31
PQ 26/25	0.125	$9.4 \cdot 10^{-3}$	1.18	0.503	5.62	5.55	36
PQ 32/20	0.203	$11.7 \cdot 10^{-3}$	1.70	0.471	6.71	5.55	42
PQ 32/30	0.384	$18.6 \cdot 10^{-3}$	1.61	0.995	6.71	7.46	55
PQ 35/35	0.820	$30.4 \cdot 10^{-3}$	1.96	1.61	7.52	8.79	73
PQ 40/40	1.20	$39.1 \cdot 10^{-3}$	2.01	2.50	8.39	10.2	95

D.6 AMERICAN WIRE GAUGE DATA

AWG#	Bare area, 10^{-3} cm^2	Resistance, $10^{-6} \Omega/\text{cm}$	Diameter, cm
0000	1072.3	1.608	1.168
000	850.3	2.027	1.040
00	674.2	2.557	0.927
0	534.8	3.224	0.825
1	424.1	4.065	0.735
2	336.3	5.128	0.654
3	266.7	6.463	0.583
4	211.5	8.153	0.519
5	167.7	10.28	0.462
6	133.0	13.0	0.411
7	105.5	16.3	0.366
8	83.67	20.6	0.326
9	66.32	26.0	0.291
10	52.41	32.9	0.267
11	41.60	41.37	0.238
12	33.08	52.09	0.213
13	26.26	69.64	0.190
14	20.02	82.80	0.171
15	16.51	104.3	0.153
16	13.07	131.8	0.137
17	10.39	165.8	0.122
18	8.228	209.5	0.109
19	6.531	263.9	0.0948
20	5.188	332.3	0.0874
21	4.116	418.9	0.0785
22	3.243	531.4	0.0701
23	2.508	666.0	0.0632
24	2.047	842.1	0.0566
25	1.623	1062.0	0.0505
26	1.280	1345.0	0.0452
27	1.021	1687.6	0.0409
28	0.8046	2142.7	0.0366
29	0.6470	2664.3	0.0330

Continued

AWG#	Bare area, 10^{-3} cm^2	Resistance, $10^{-6} \Omega/\text{cm}$	Diameter, cm
30	0.5067	3402.2	0.0294
31	0.4013	4294.6	0.0267
32	0.3242	5314.9	0.0241
33	0.2554	6748.6	0.0236
34	0.2011	8572.8	0.0191
35	0.1589	10849	0.0170
36	0.1266	13608	0.0152
37	0.1026	16801	0.0140
38	0.08107	21266	0.0124
39	0.06207	27775	0.0109
40	0.04869	35400	0.0096
41	0.03972	43405	0.00863
42	0.03166	54429	0.00762
43	0.02452	70308	0.00685
44	0.0202	85072	0.00635

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